

COMPAL CONFIDENTIAL

MODEL NAME : *Abacus-MT*

COMPAL P/N :

PCB NO : *LA-1682*

Revision : *0.2*

Abacus-MT Schematics Document uFCBGA/uFCPGA NorthWood MT

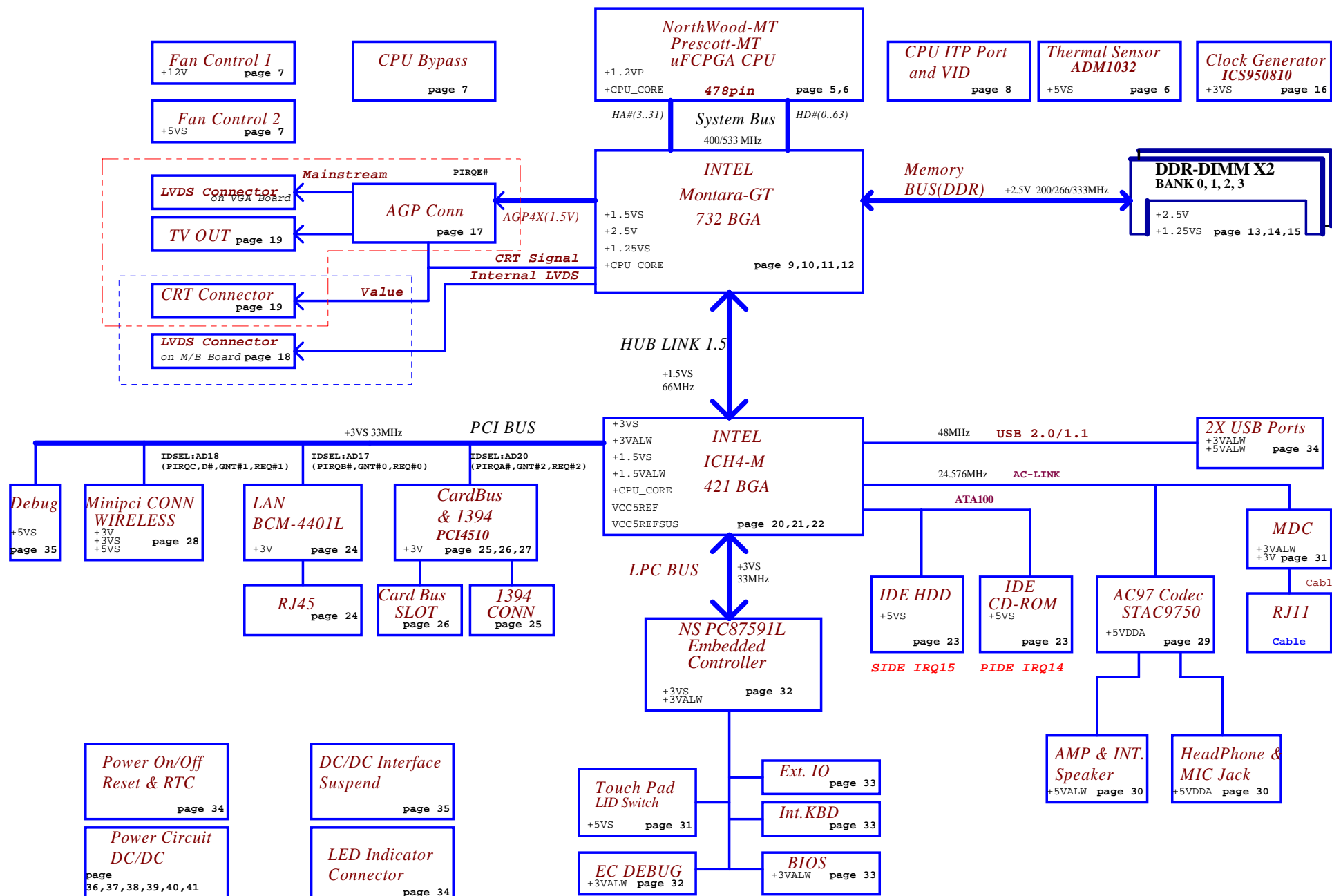
2003-02-25

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Title		
Cover Sheet		
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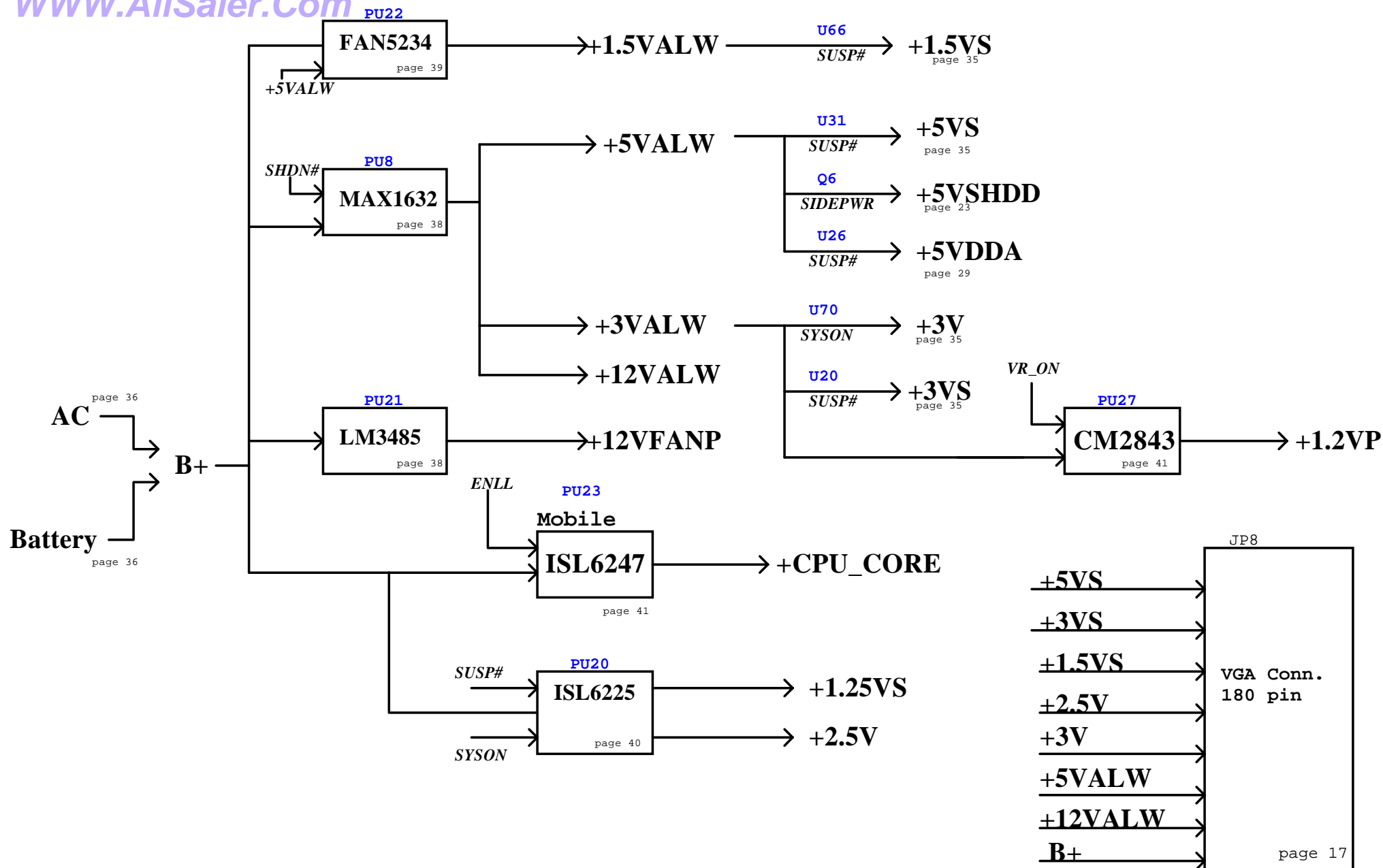
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Block Diagram			
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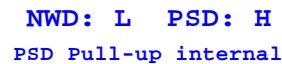


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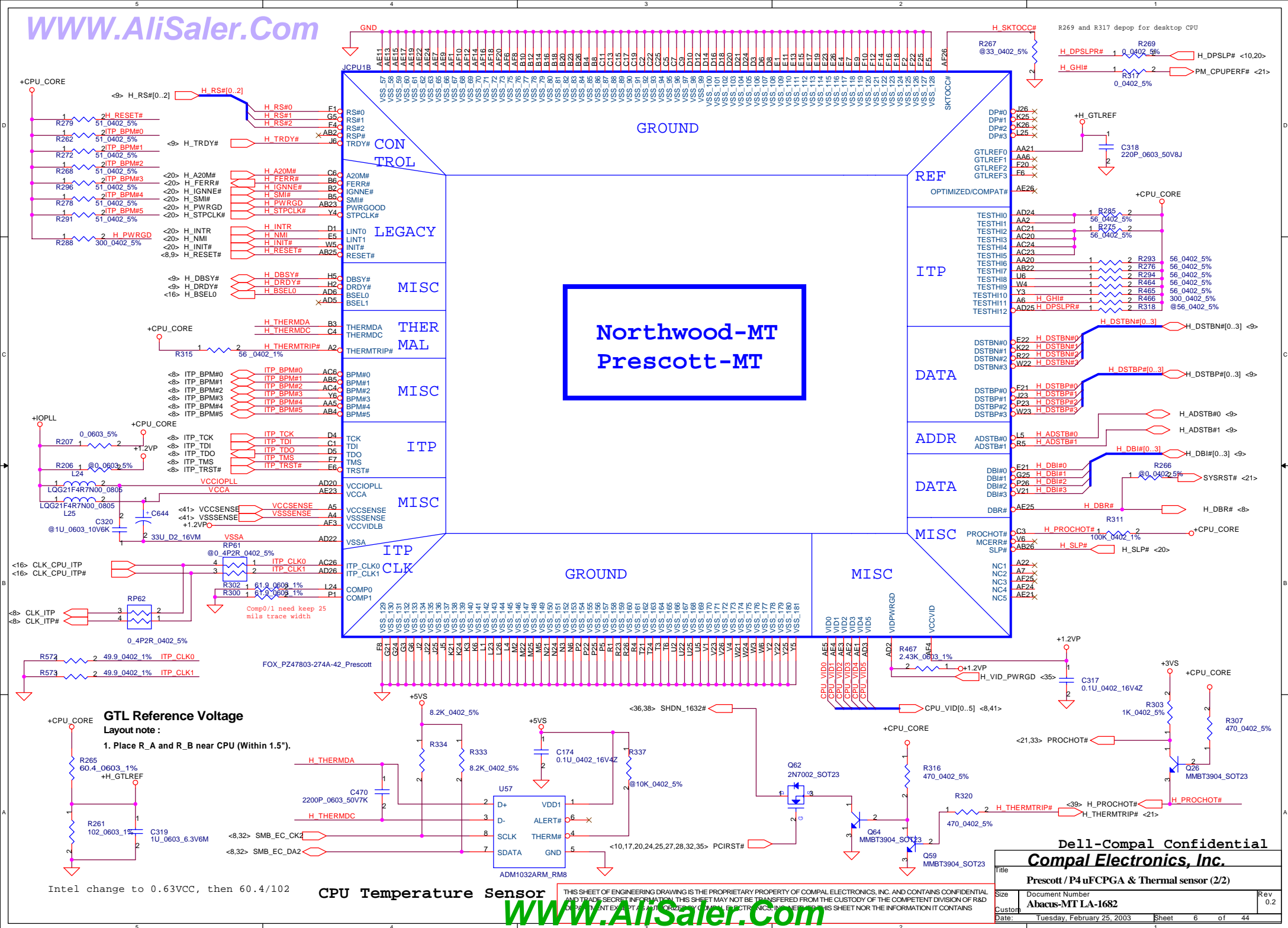
POWER DIAGRAM			
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Layout note :

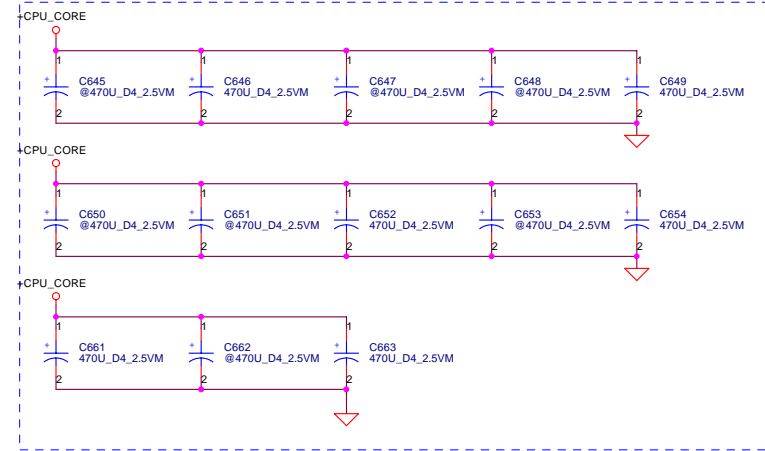
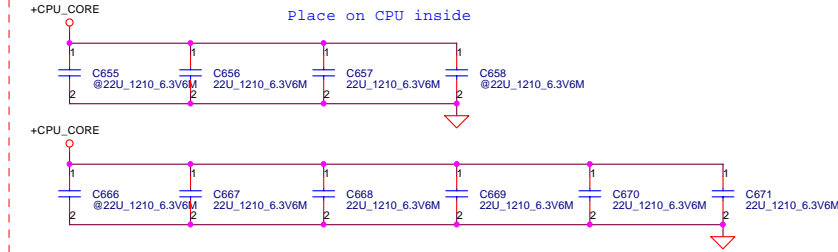
Place close to CPU, Use 2-3 vias per PAD.
Place 22uF caps x31 pcs, populated 14pcs.

Layout note :

Place close to CPU power and ground pin as possible (<1inch)

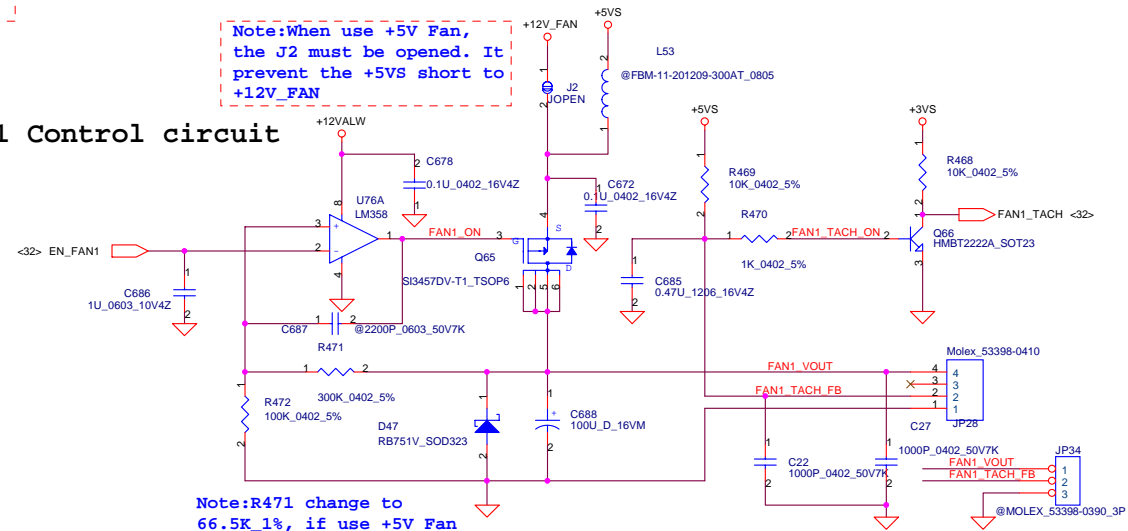
For Desktop's CPU:

470uF \times 15/10m ohm each
Total 0.67m ohm



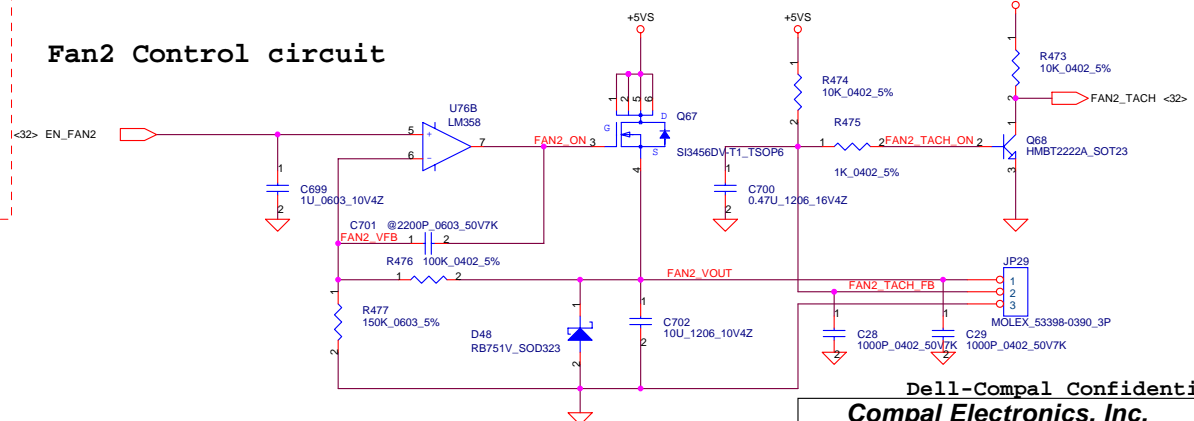
Note: When use +5V Fan, the J2 must be opened. It prevent the +5VS short to +12V_FAN

Fan1 Control circuit



Note: R471 change to 66.5K_1%, if use +5V Fan

Fan2 Control circuit



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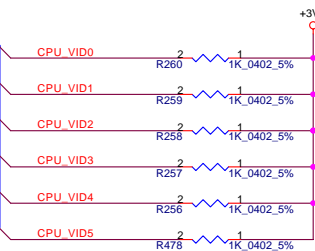
CPU Decoupling CAP. & Fan control

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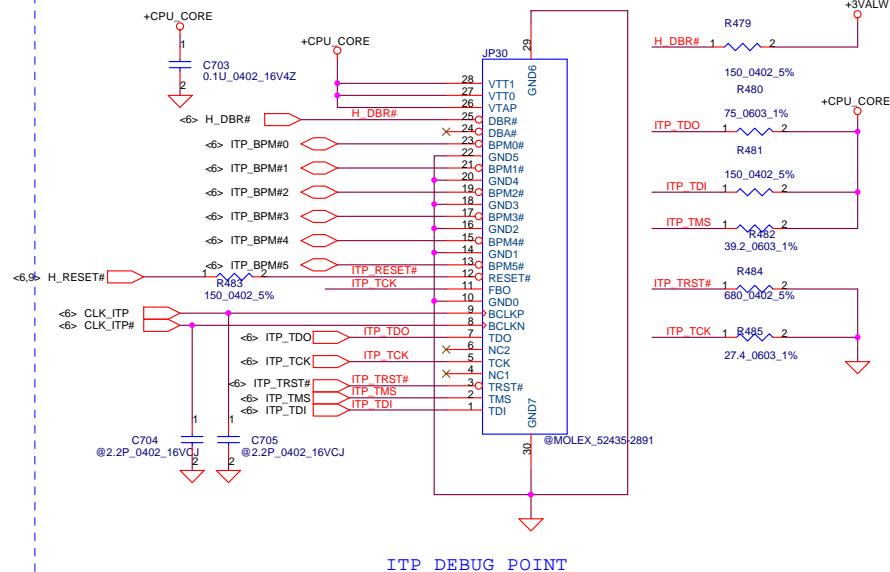
<6,41> CPU_VID[0..5]

VID [0..5]



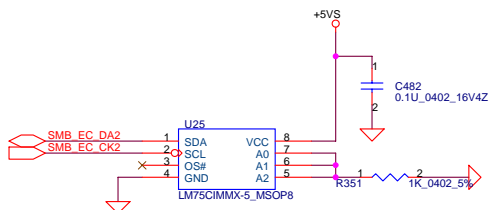
VID 5 for Prescott-MT

VID	4	3	2	1	0	V
	0	1	0	1	1	1.5750
	0	1	1	0	0	1.5500
	0	1	1	0	1	1.5250
	0	1	1	1	0	1.5000
	0	1	1	1	1	1.4750
	1	0	0	0	0	1.4500
	1	0	0	0	1	1.4250
	1	0	0	1	0	1.4000
	1	0	0	1	1	1.3750
	1	0	1	0	0	1.3500
	1	0	1	0	1	1.3250
	1	0	1	1	0	1.3000
	1	1	0	0	0	1.2750
	1	1	0	0	1	1.2500
	1	1	0	1	0	1.2250
	1	1	0	1	1	1.2000
	1	1	1	0	0	1.1750
	1	1	1	0	1	1.1500
	1	1	1	1	0	1.1250
	1	1	1	1	1	1.1000
	1	1	1	1	1	off

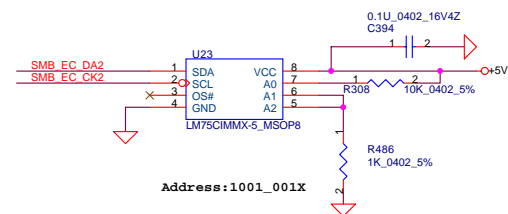


ITP Debug Connector

<6,32> SMB_EC_DA2
<6,32> SMB_EC_CK2



Address:1001_000X



Address:1001_001X

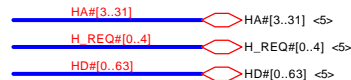
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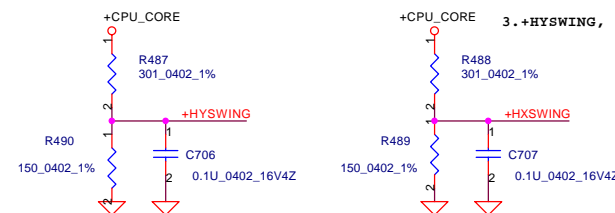
CPU VID & ITP PORT

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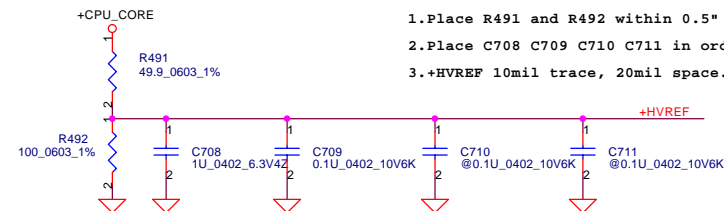


- 1.Place R487 and R490 within 0.5" of U77 pin K28
- 2.Place R488 and R489 within 0.5" of U77 pin B18
- 3.+HYSWING, +HXSING 10mil trace, 20mil space.



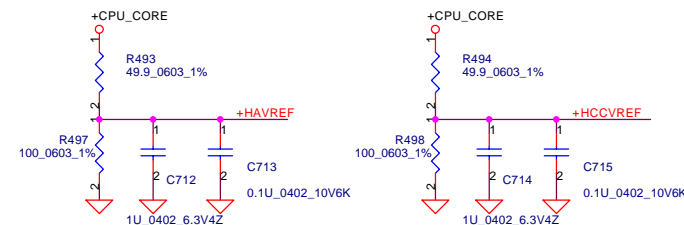
Host data Ref. Voltage

- 1.Place R491 and R492 within 0.5" of U77 pin K21 J21 J17
- 2.Place C708 C709 C710 C711 in order from U77 to divider
- 3.+HVREF 10mil trace, 20mil space.

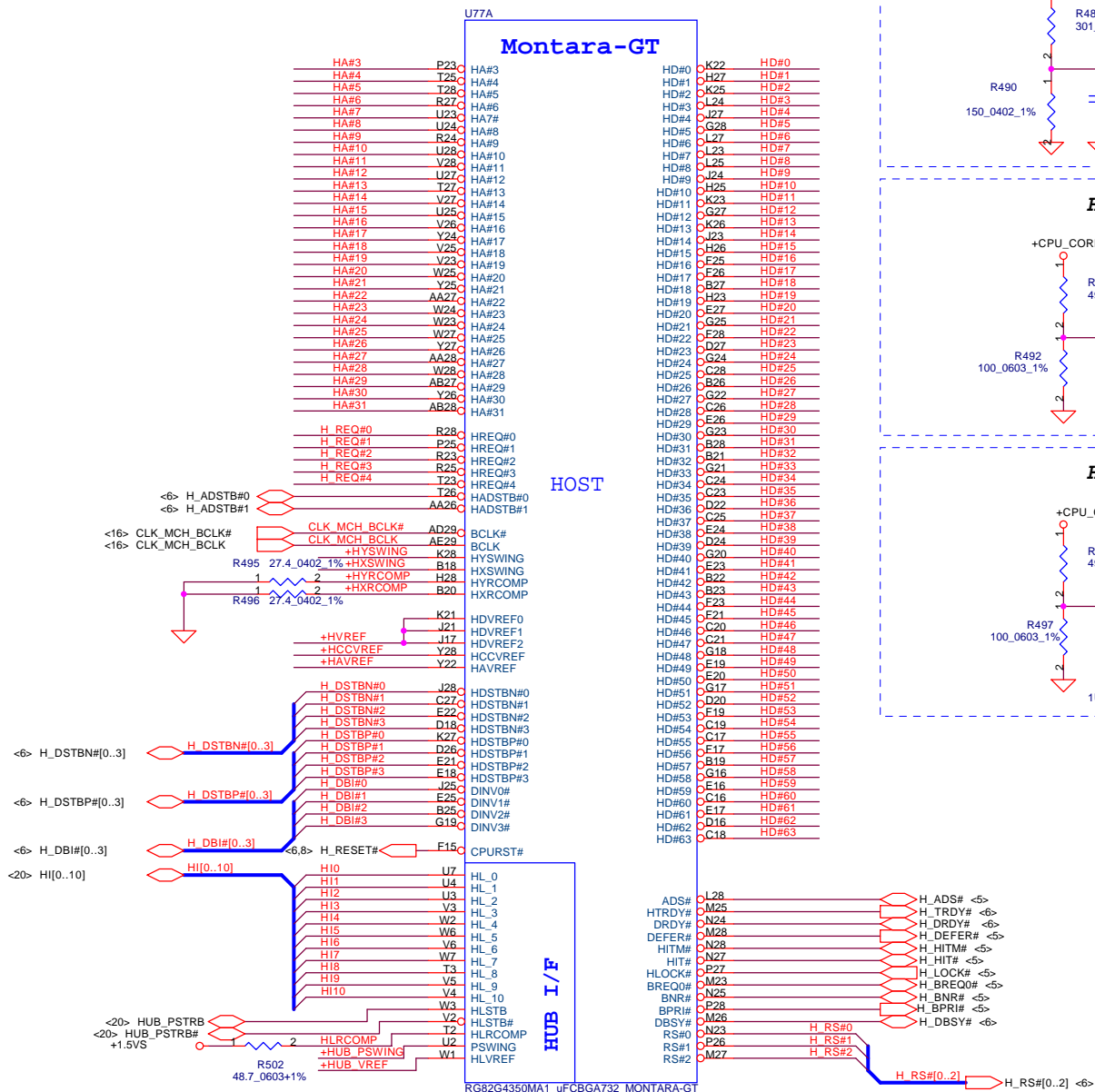
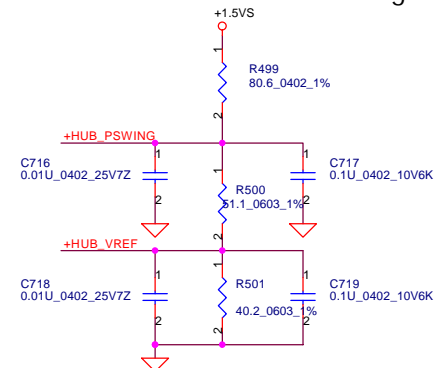


Host Address	Ref. Voltage
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- +CPU_CORE
R494
49.9_0603_1%



HUBLink reference Voltage

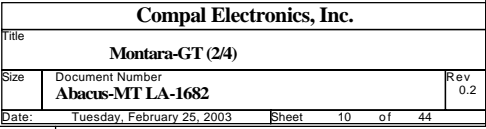


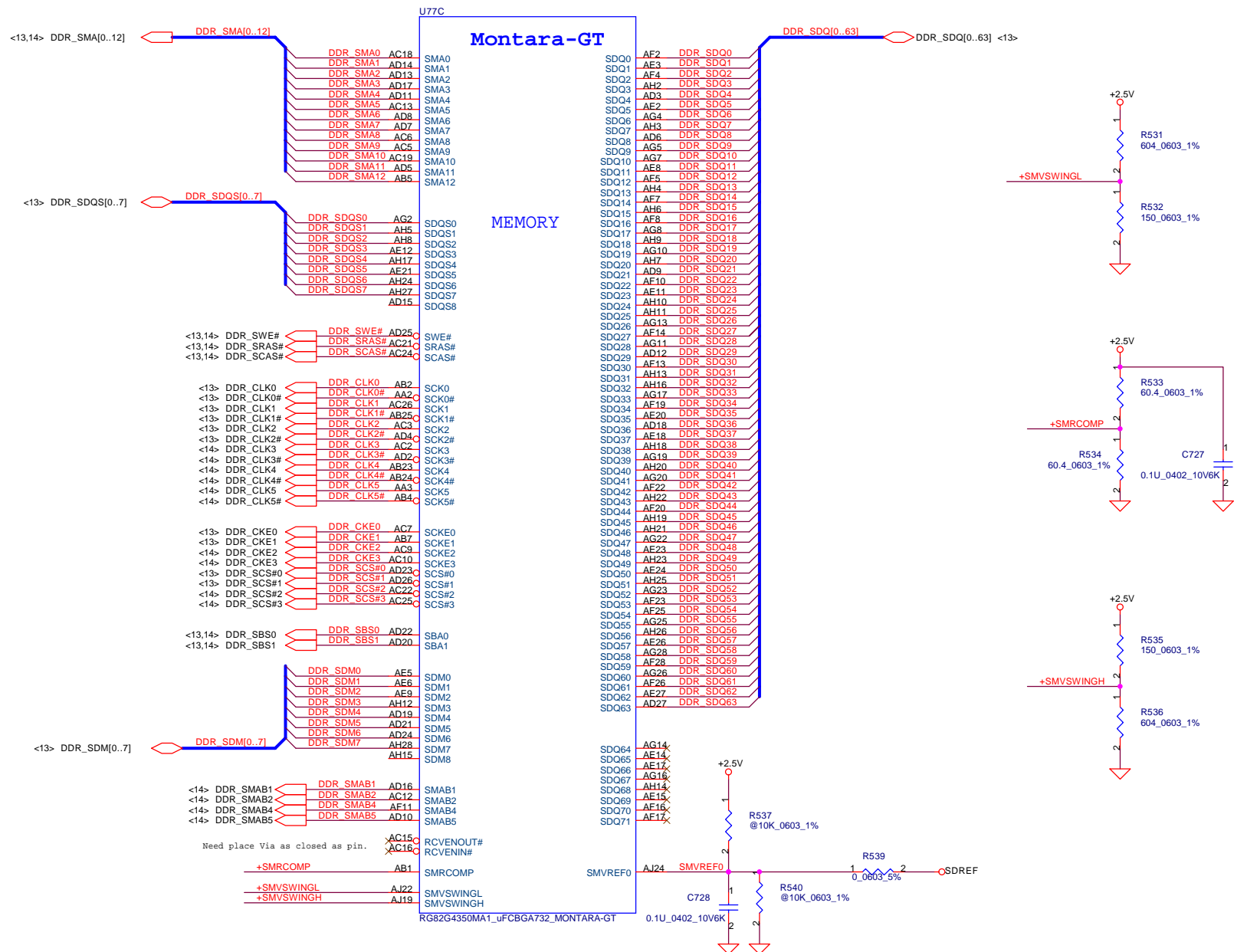
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Montara-GT (1/4)

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Montara-GT (1/4)			
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TOPOLOGY 2 FOR DDR

SMAA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

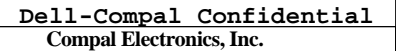
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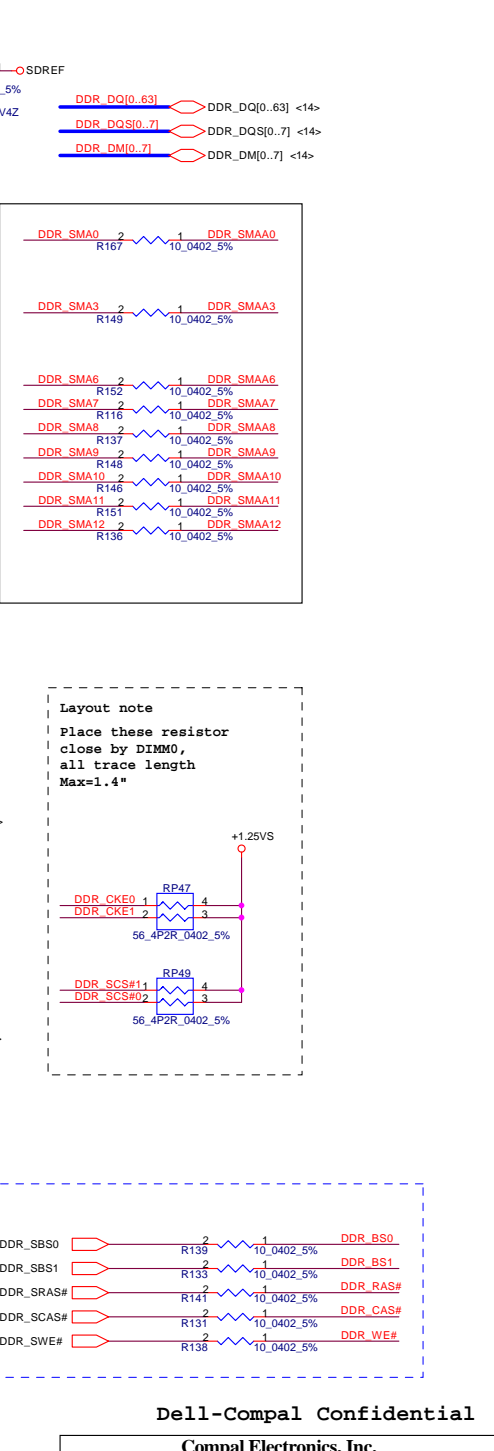
Montara-GT (3/4)

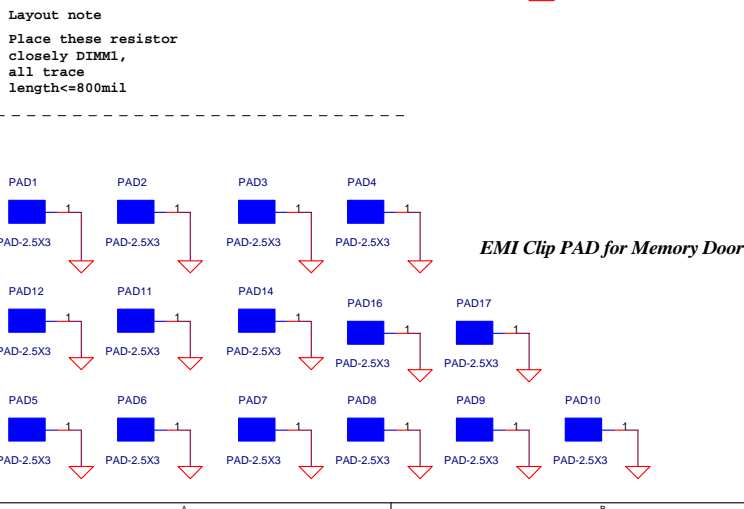
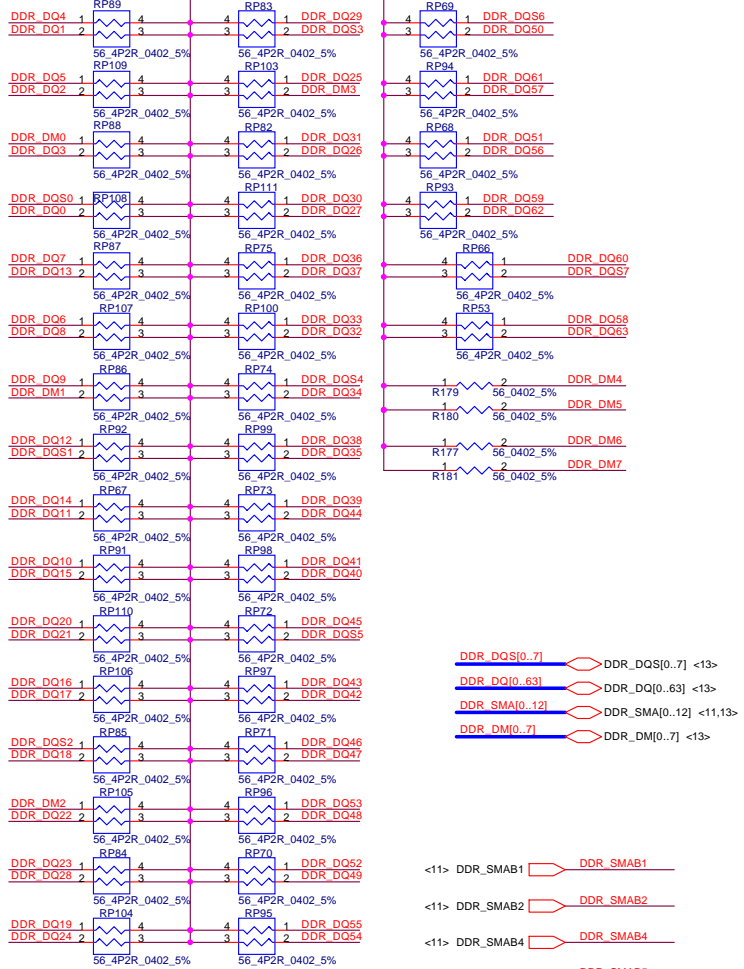
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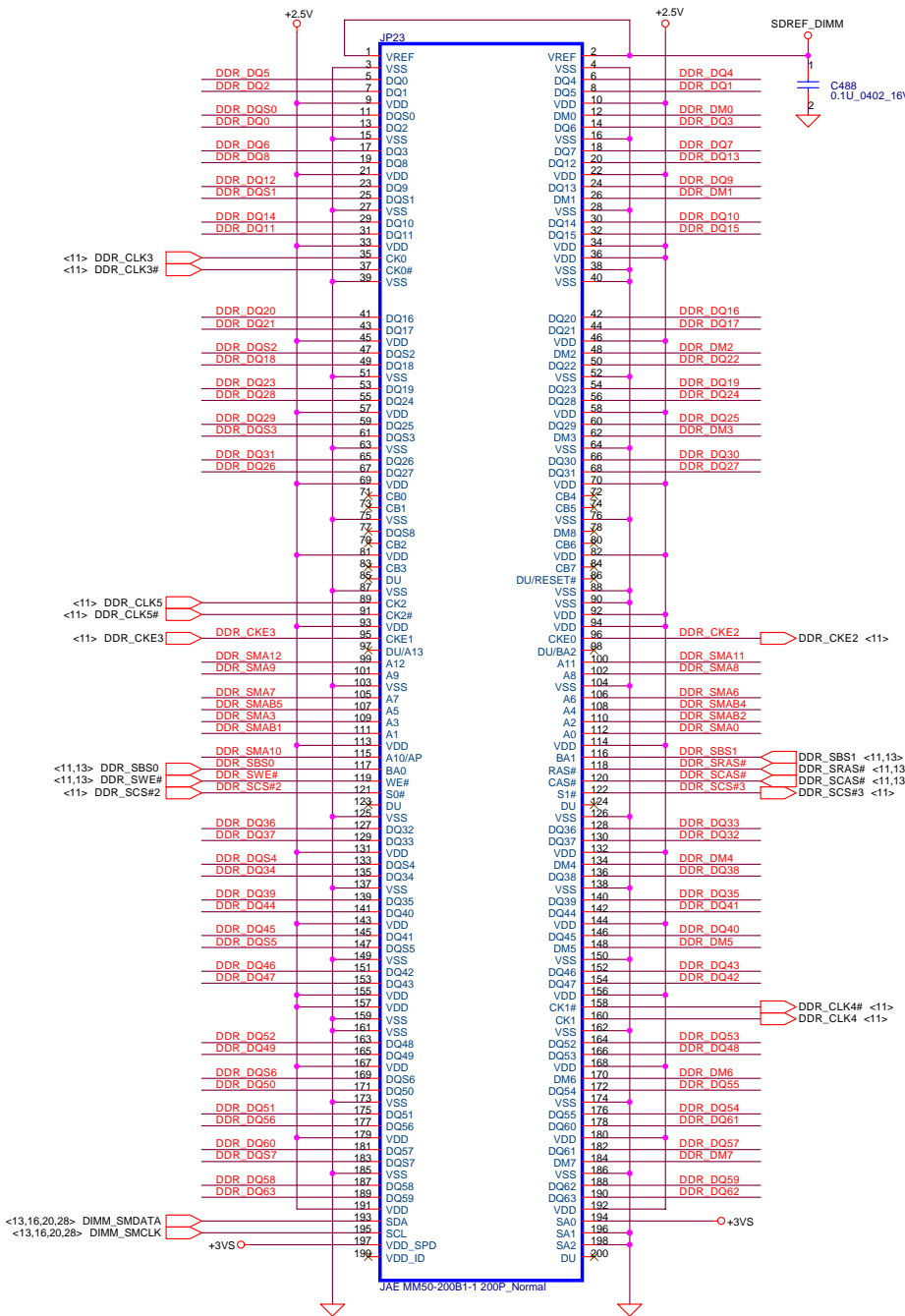


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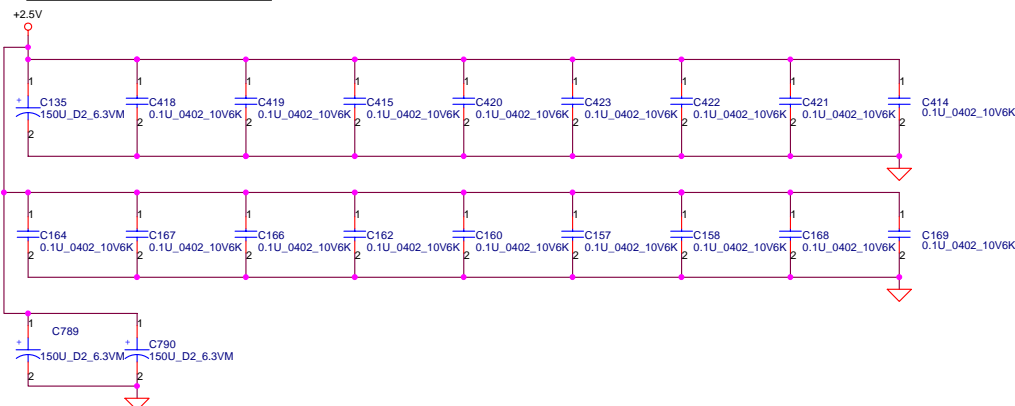
DDR TOPOLOGY 2 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#



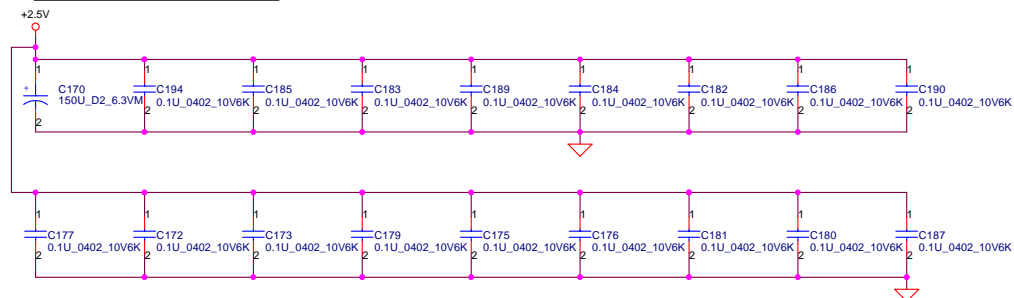
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DDR-SODIMM SLOT1			
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Layout note :
Distribute as close as possible to DDR-SODIMM1.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS

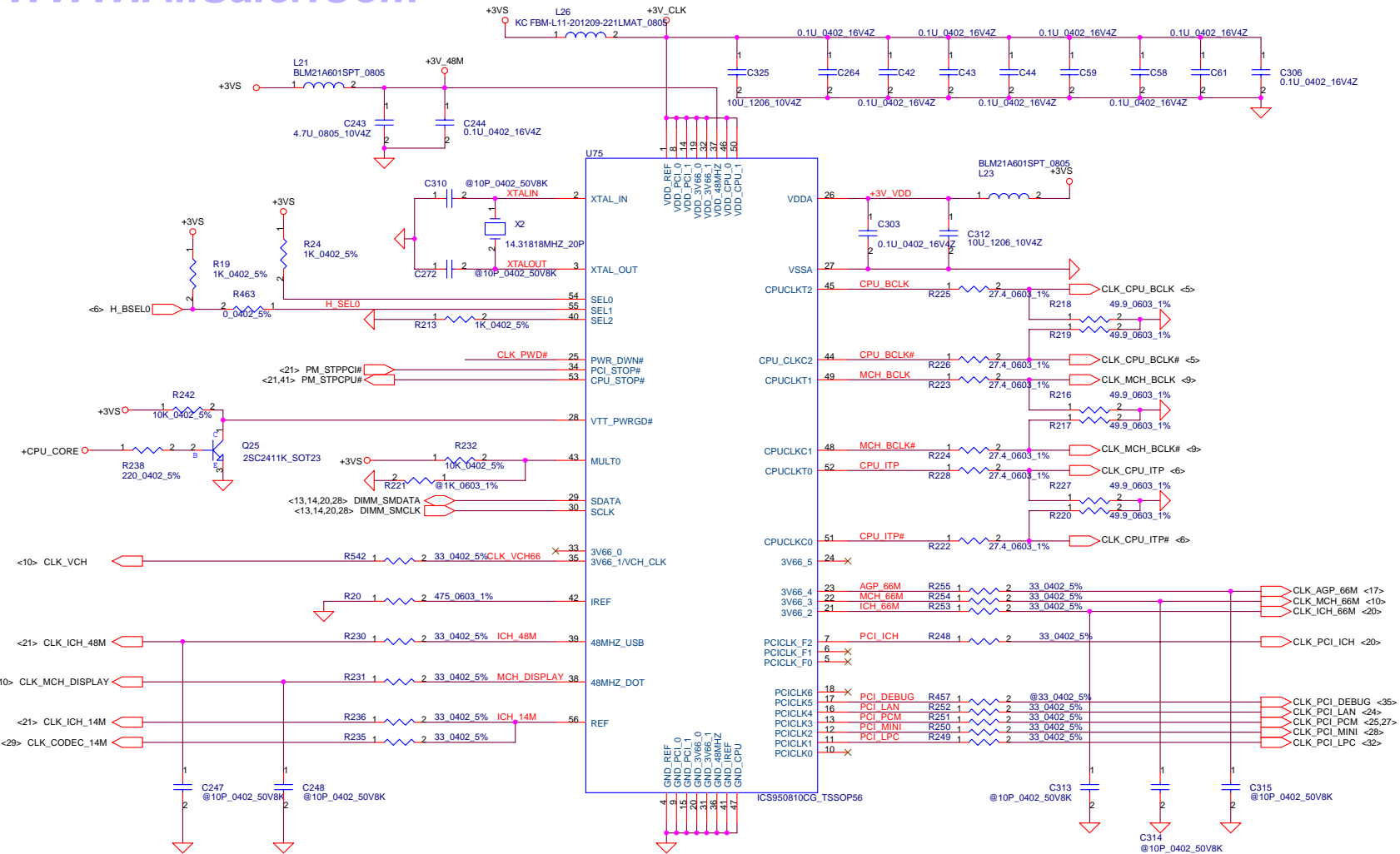


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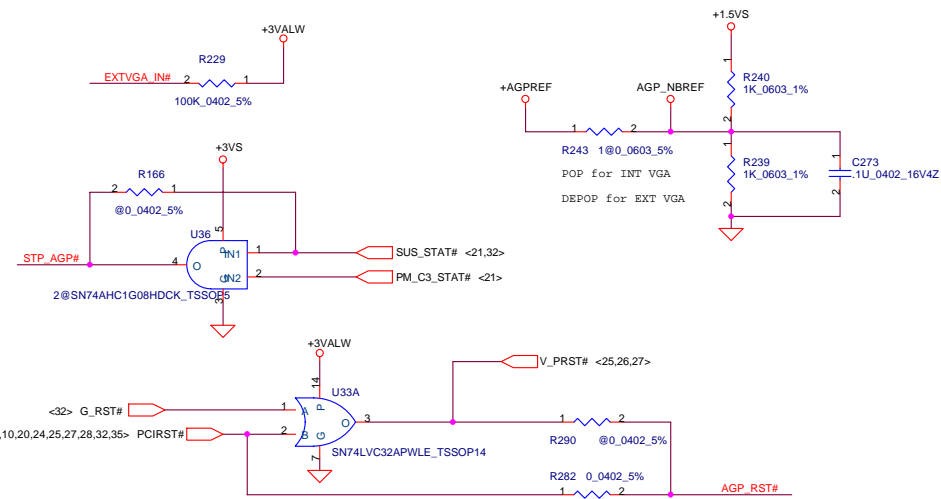
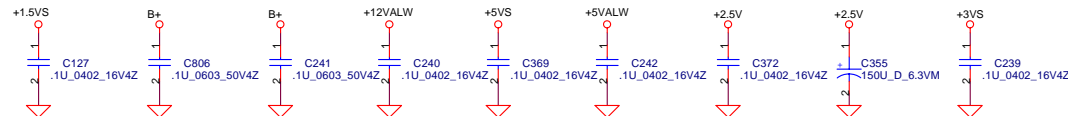
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Title			
DDR SODIMM Decoupling			
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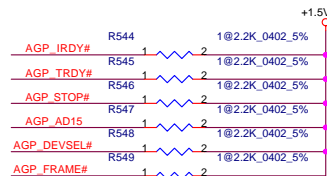
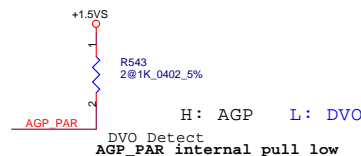
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<10> AGP_ST[0..2] AGP_ST[0..2]
 <10> AGP_SBA[0..7] AGP_SBA[0..7]
 <10> AGP_AD[0..31] AGP_AD[0..31]
 <10> AGP_CBE[0..3] AGP_CBE[0..3]



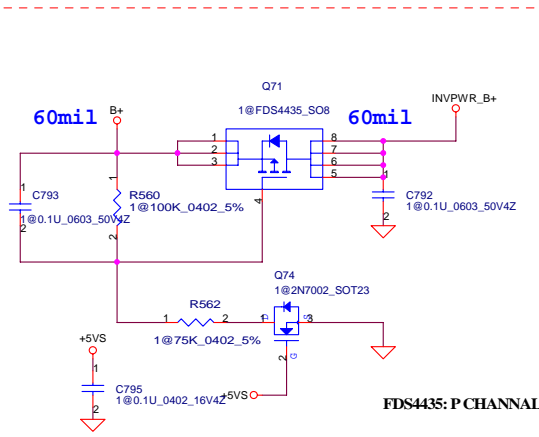
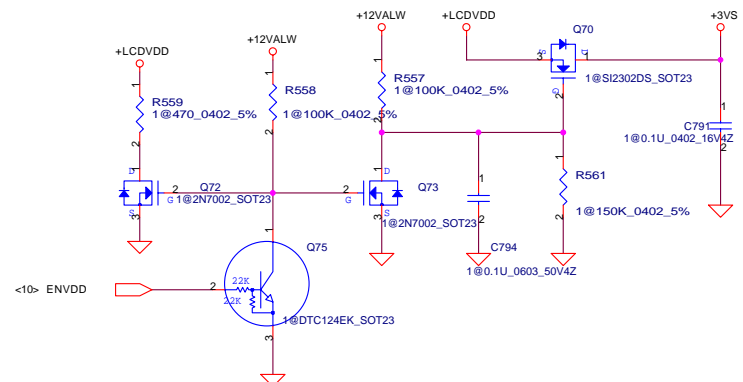
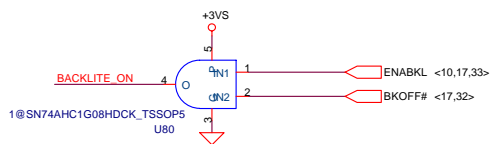
AGP_RST# = PCI_RST#



* EXTVA_IN# 1: internal graphic 2: external AGP

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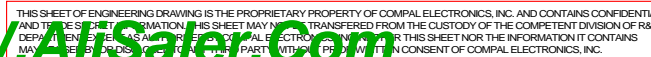
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External AGP			
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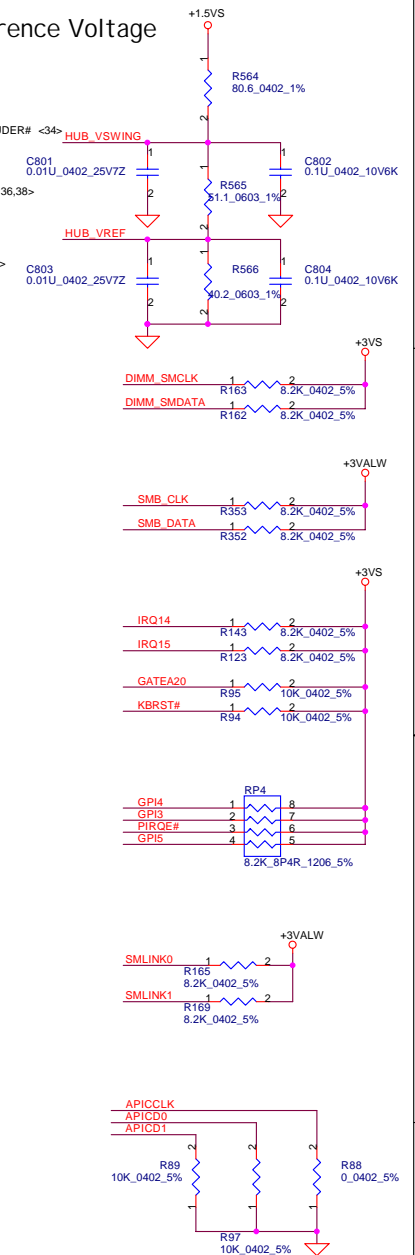
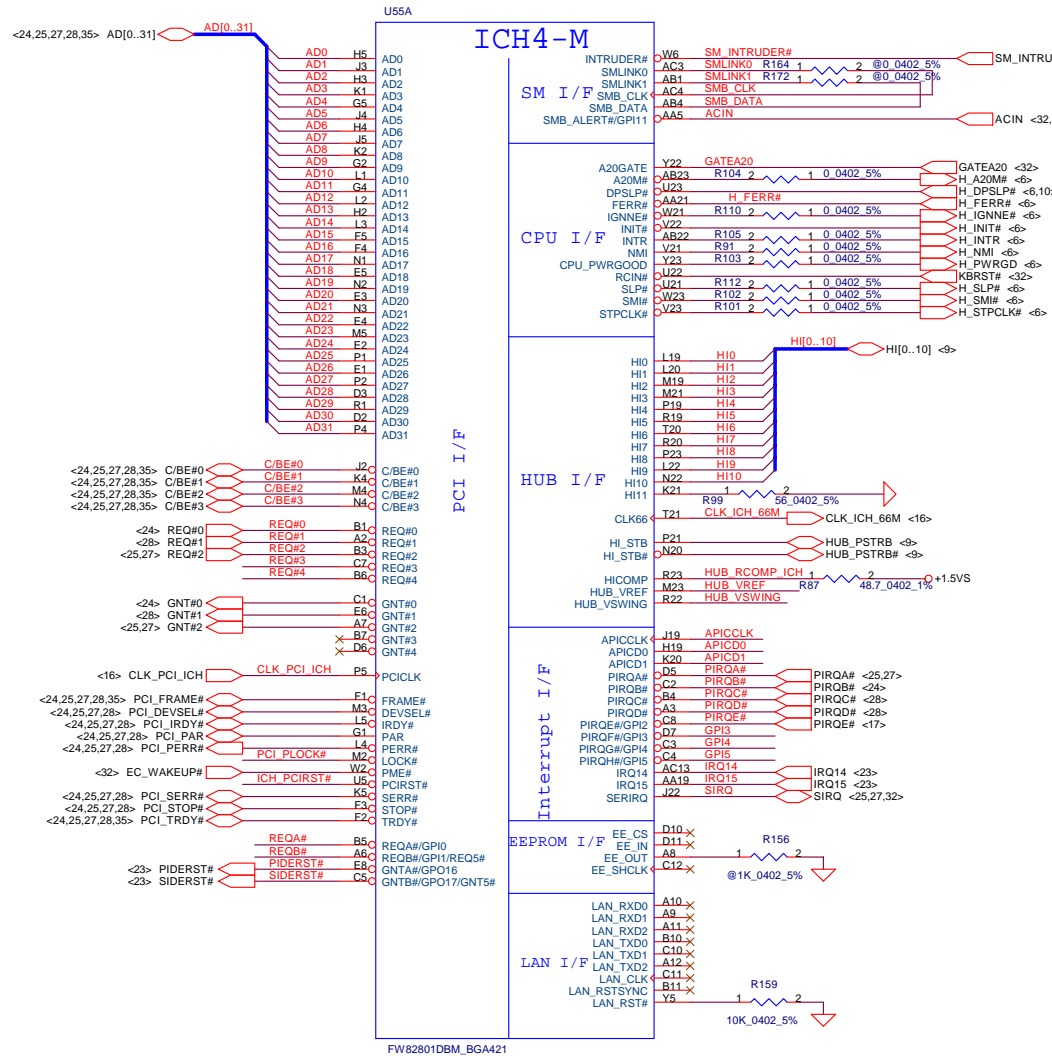
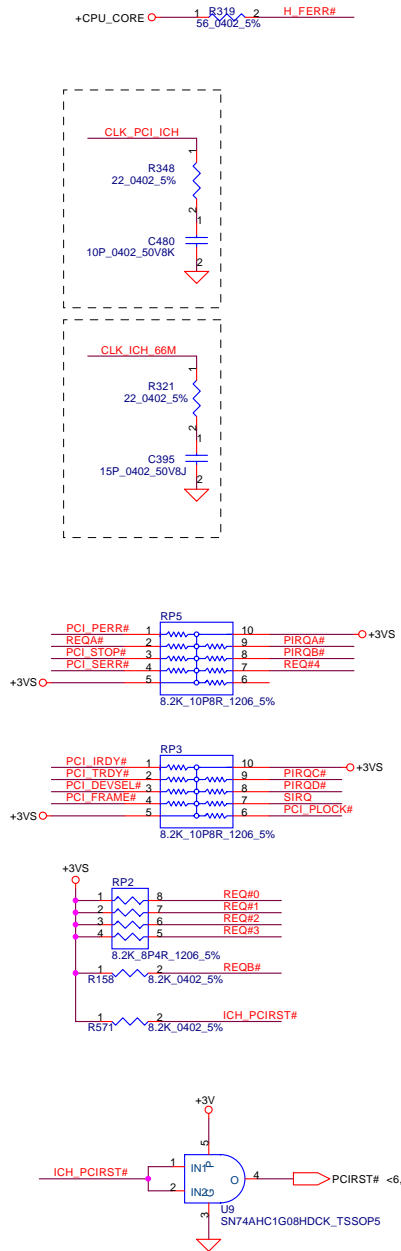


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Internal LVDs

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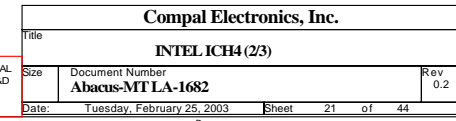


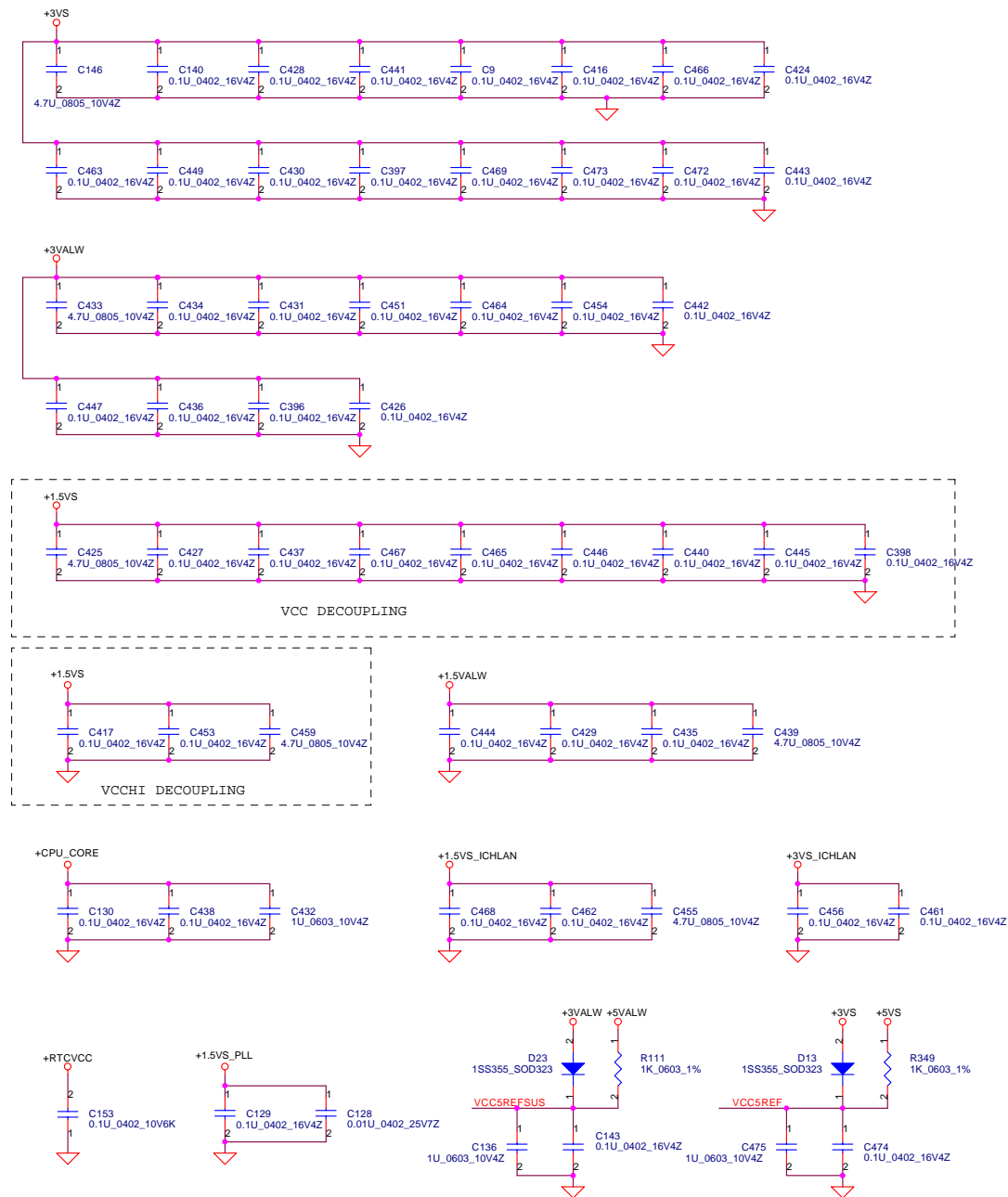
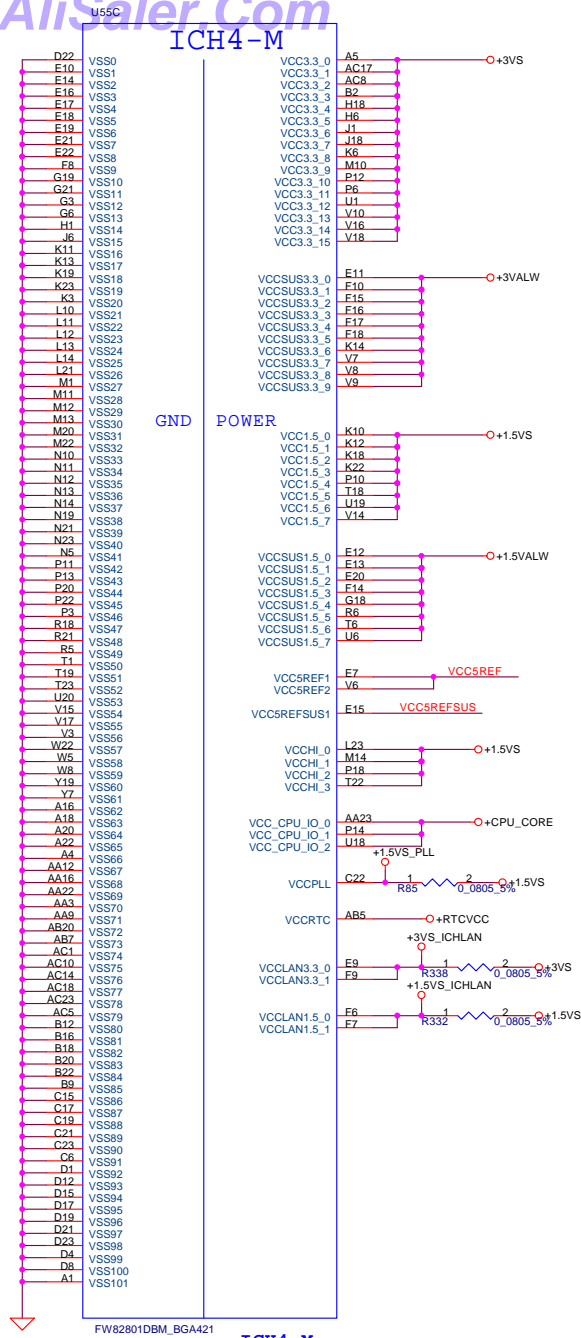
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INTEL ICH4 (1/3)

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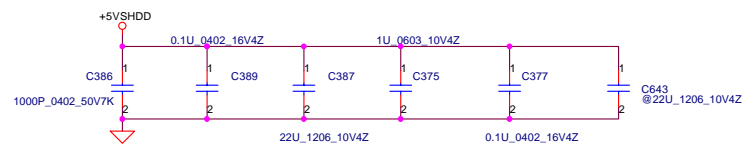
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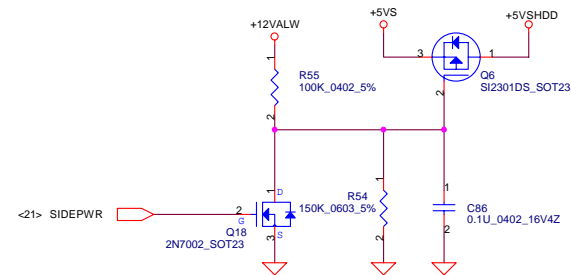
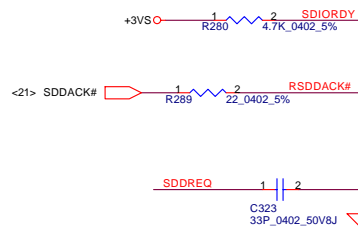
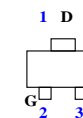
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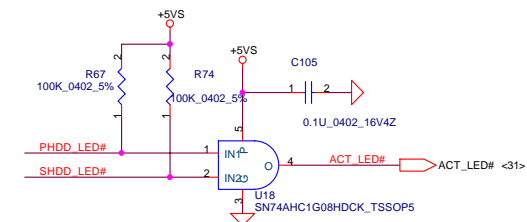
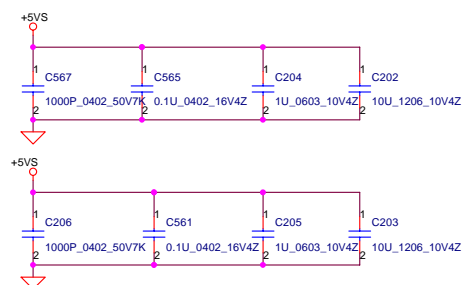
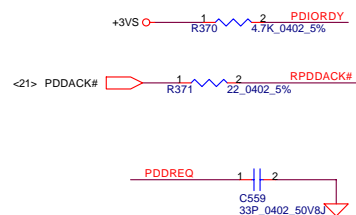
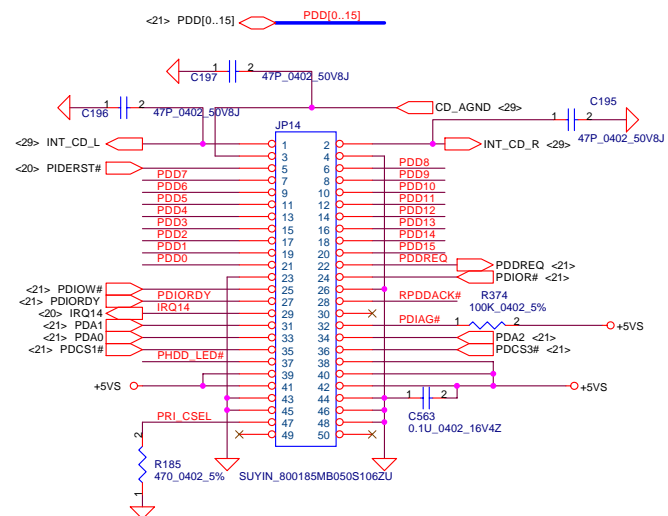
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SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +8V



CD-ROM Connector



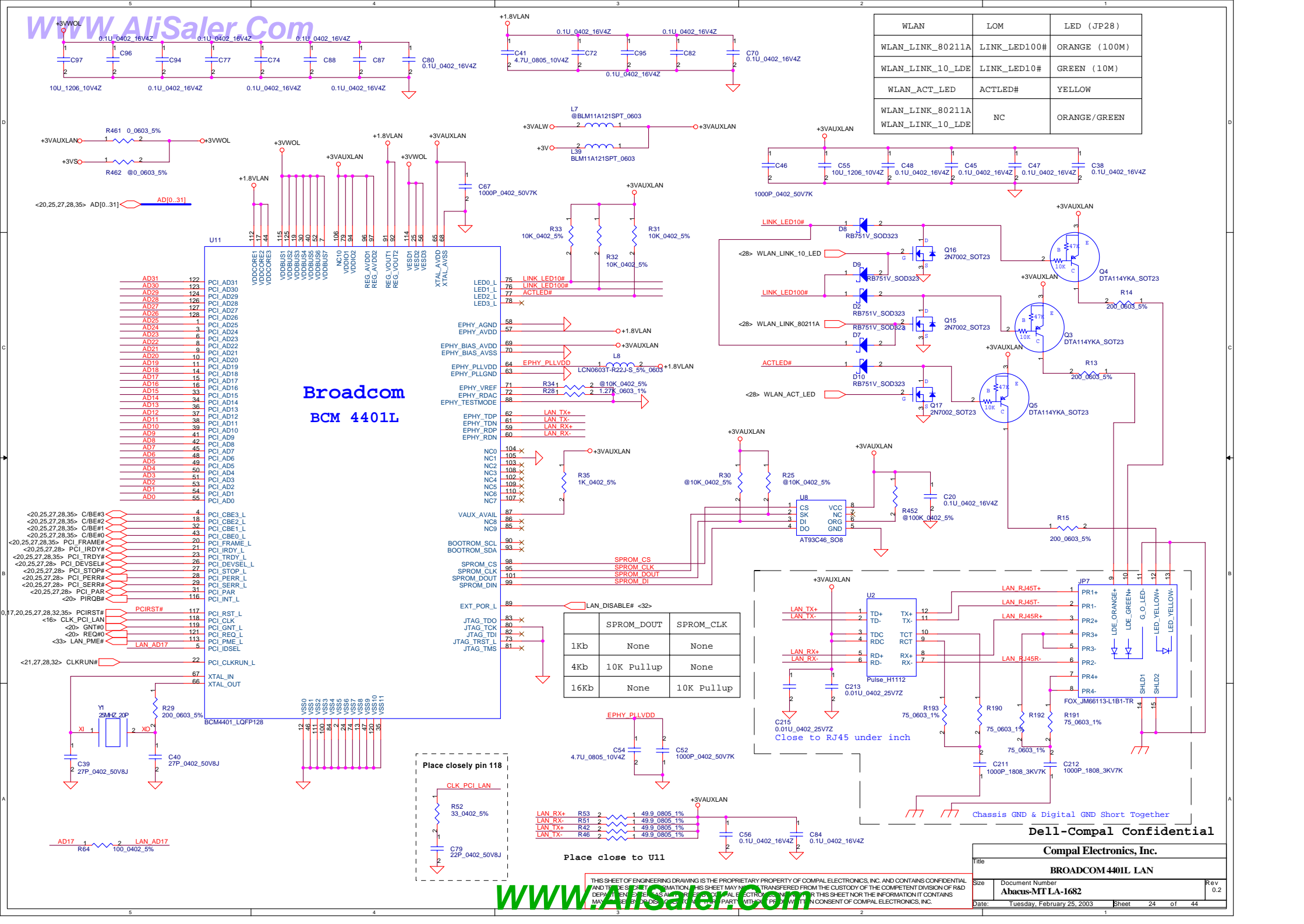
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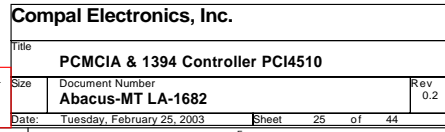
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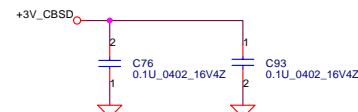
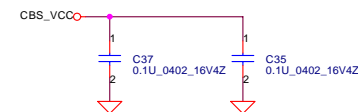
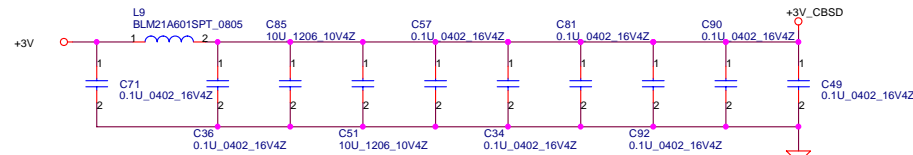
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Title			
BROADCOM 4401L LAN			
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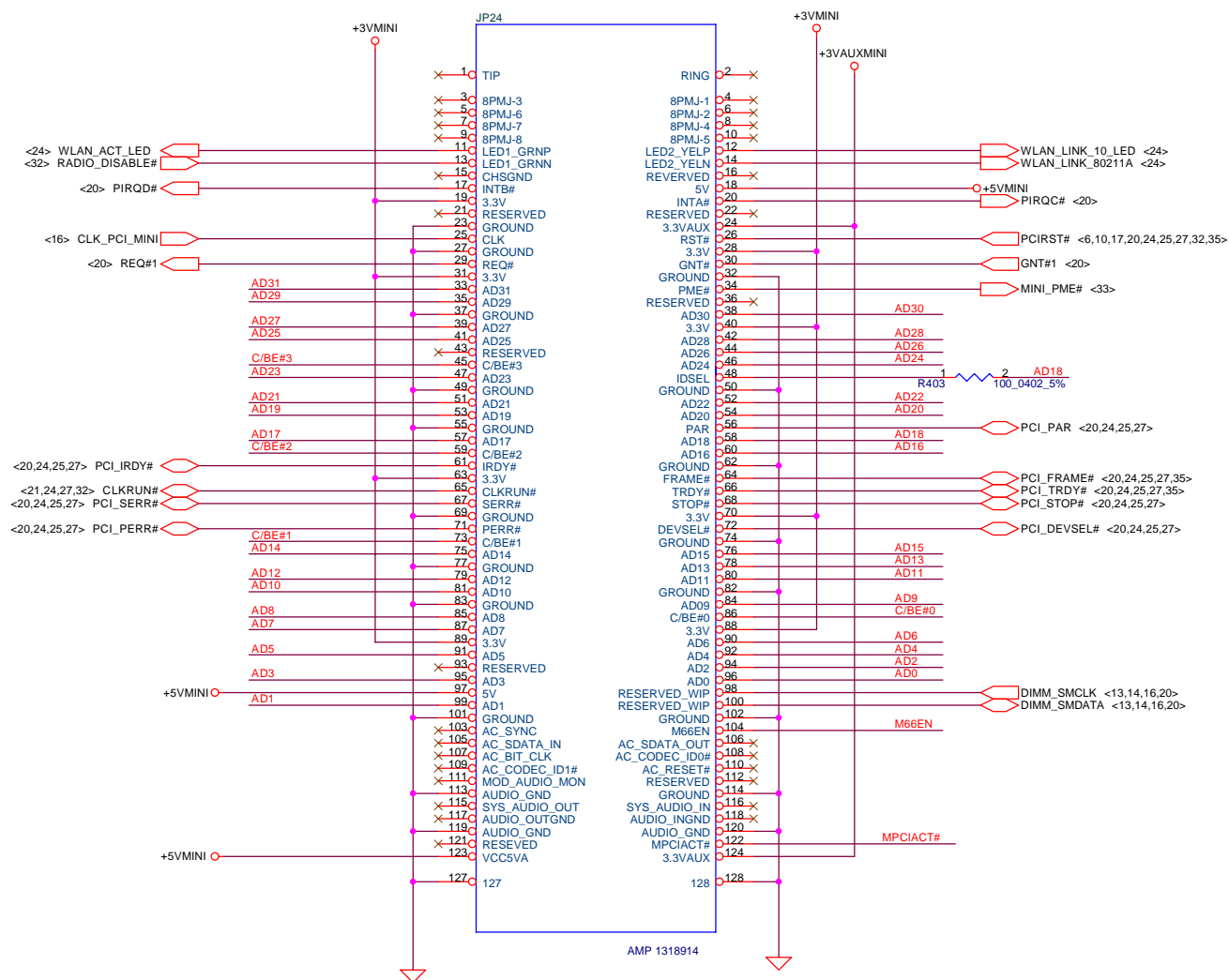


Title	PCMCIA Socket		
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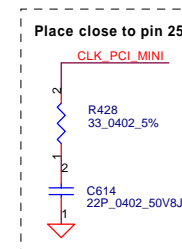




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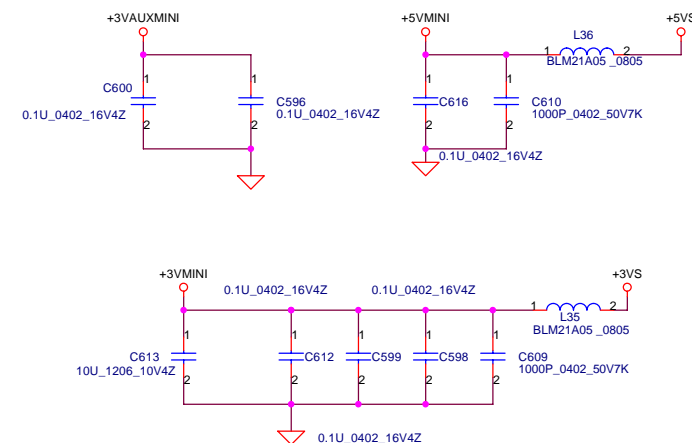
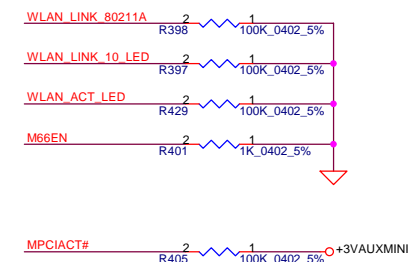
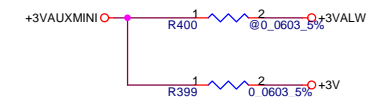
MINI PCI TYPE III



WIRELESS SUPPORT ONLY



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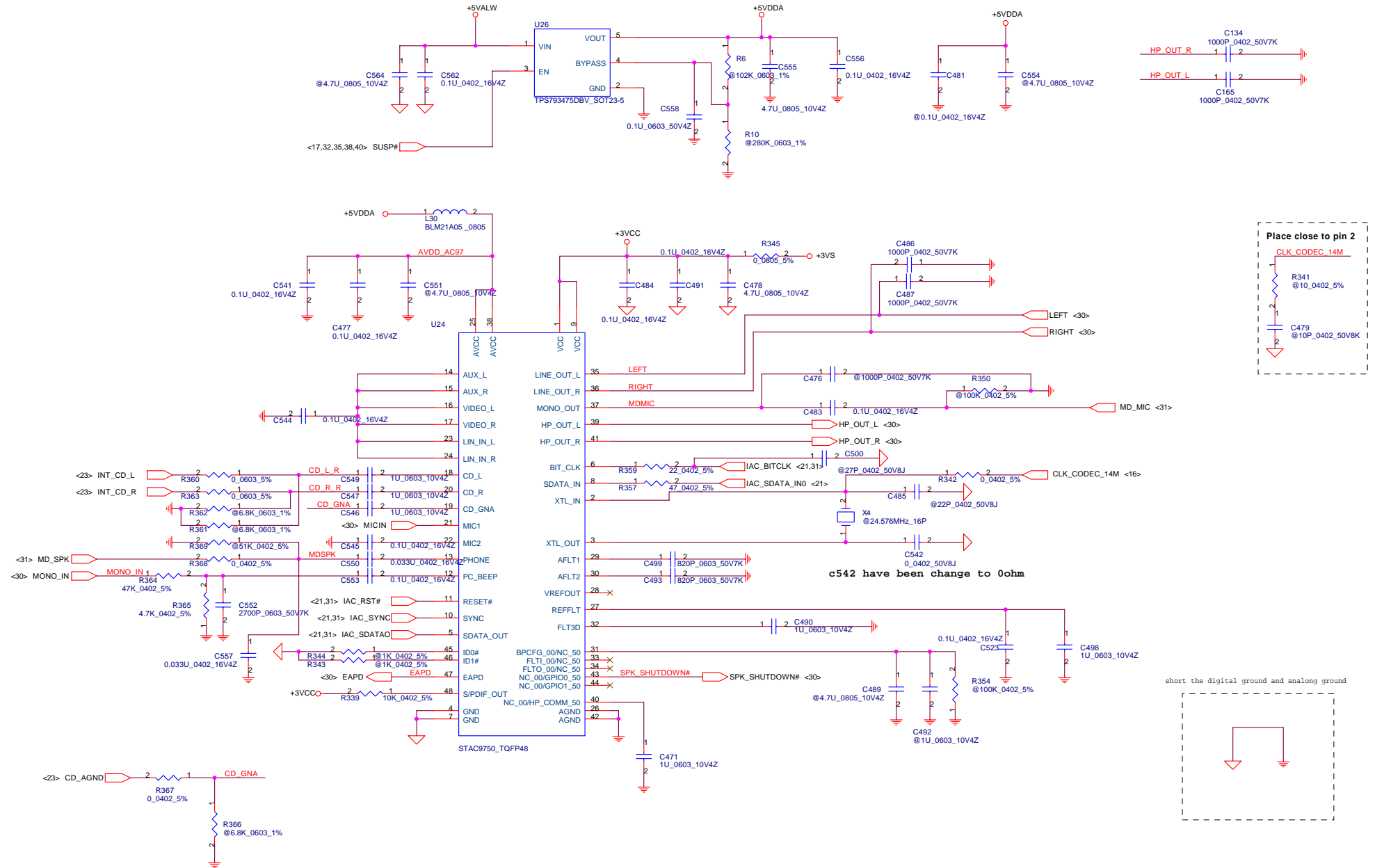


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Title		
MiniPci Port		
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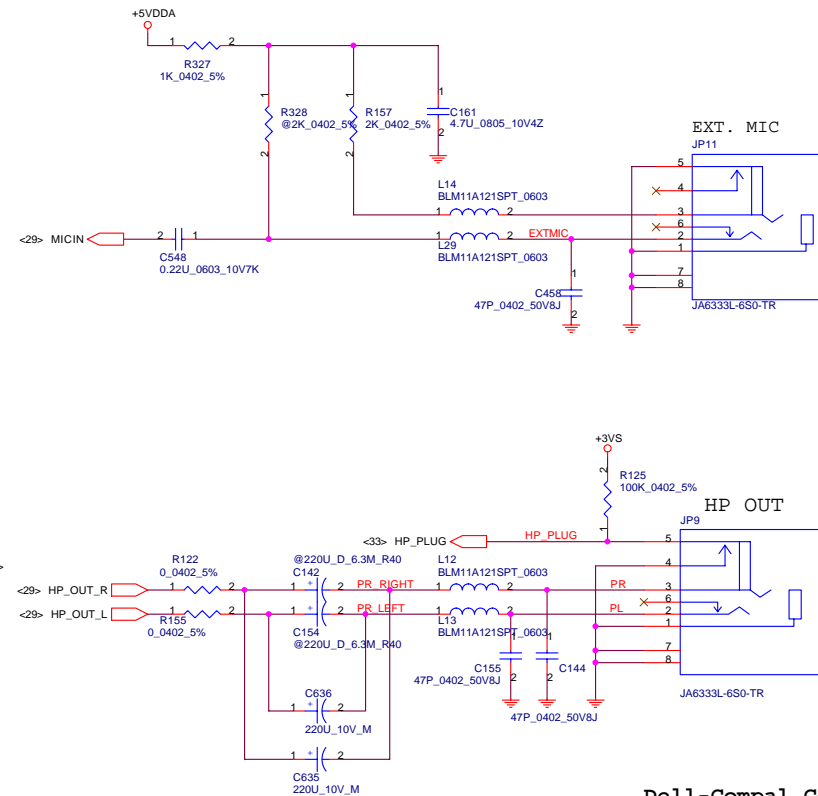
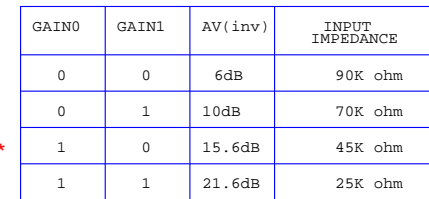


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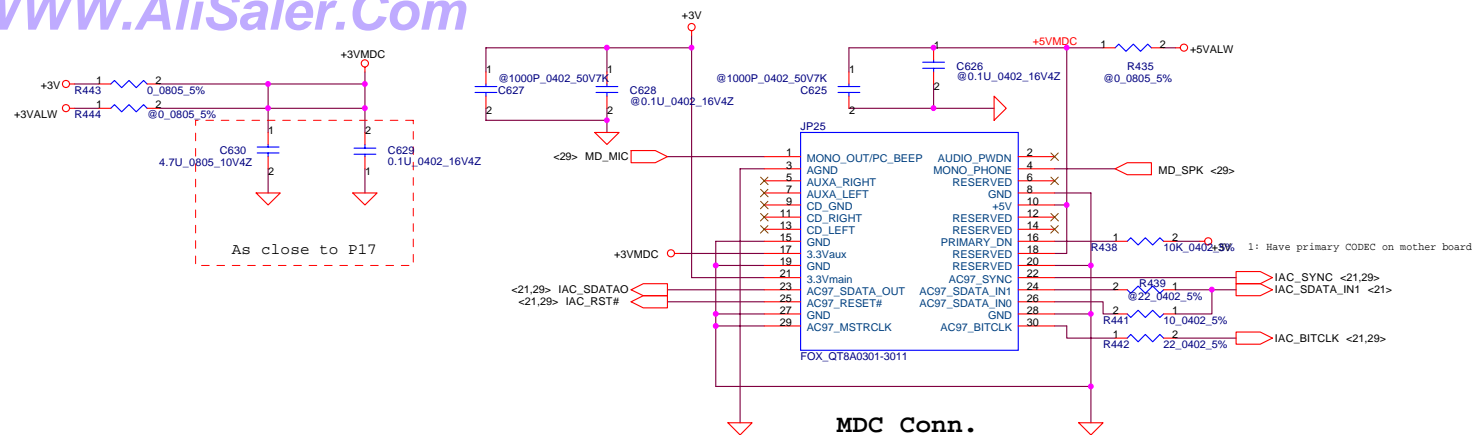
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Title		
AC97 CODEC		
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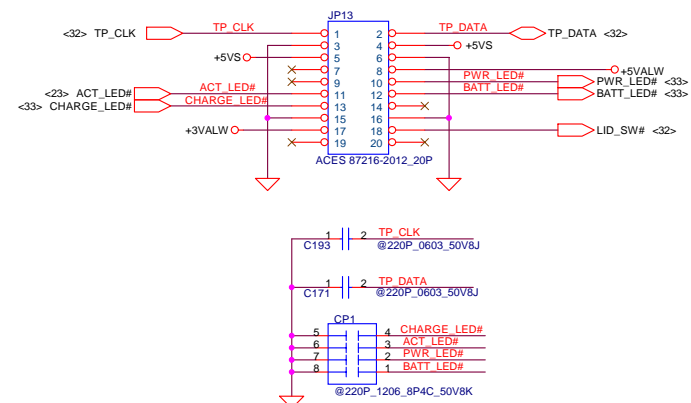
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Title			
AMP & Audio Jack			
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Touch Pad & Status LED Conn.

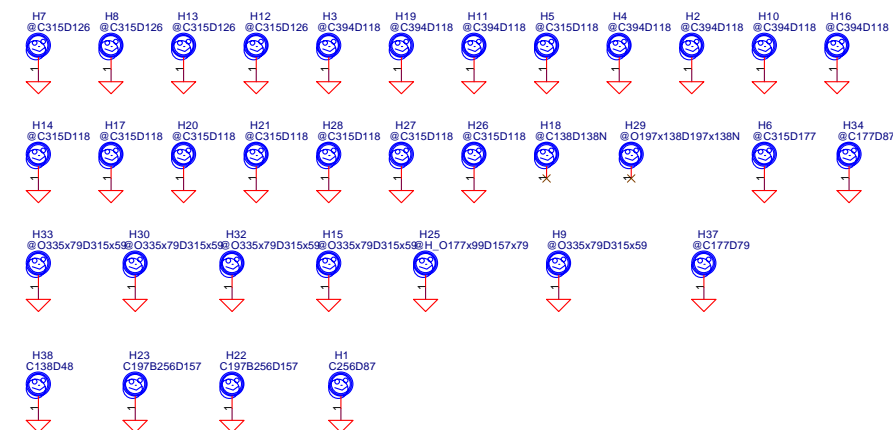


MDC Note

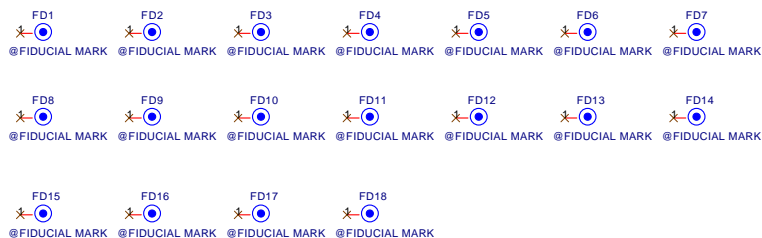
Pin 1 is NC for Pctel and connexant MDC modem

Pin 2 is NC for Pctel and connexant MDC modem

Screw Hole



Fiducial Mark

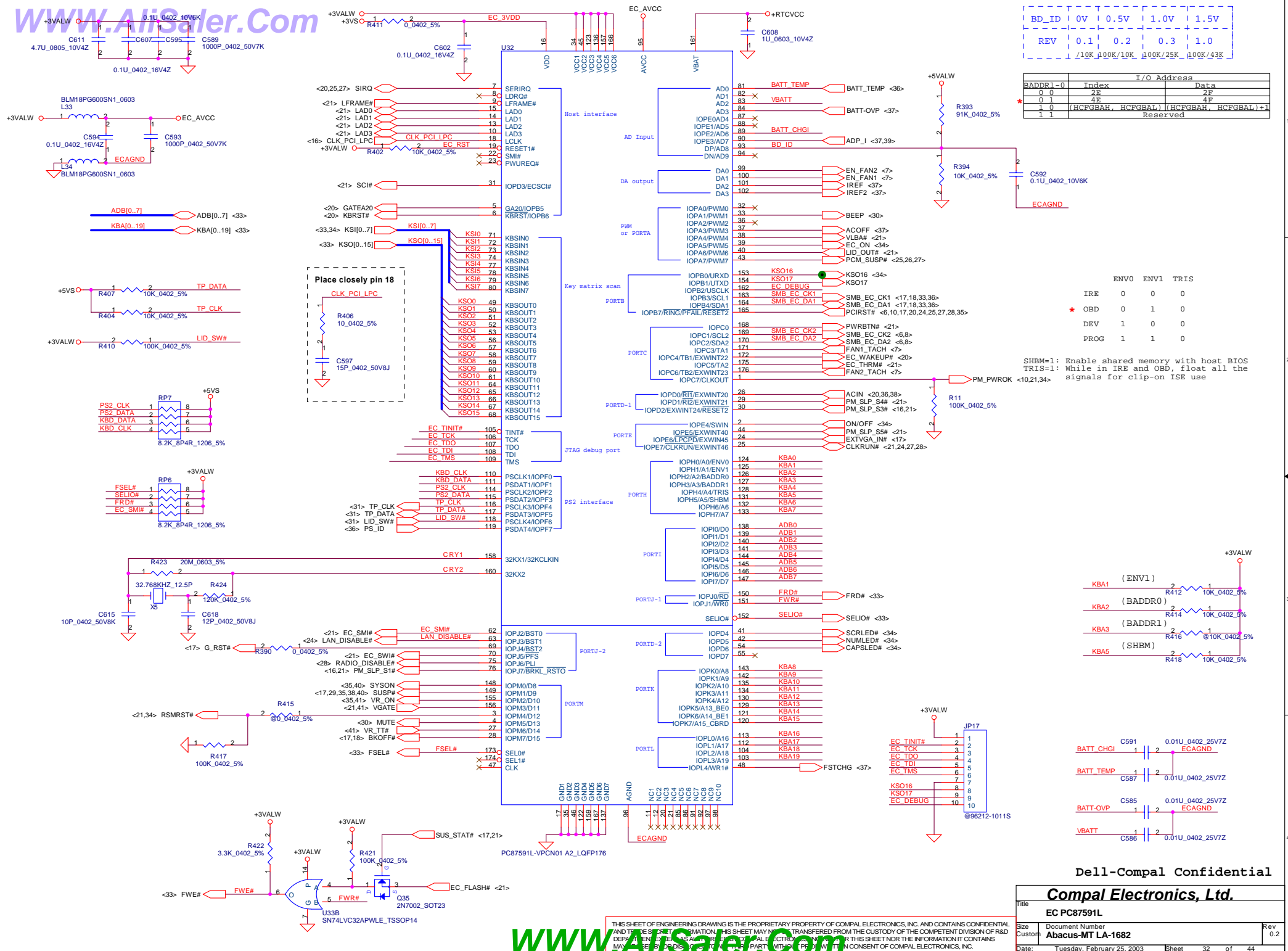


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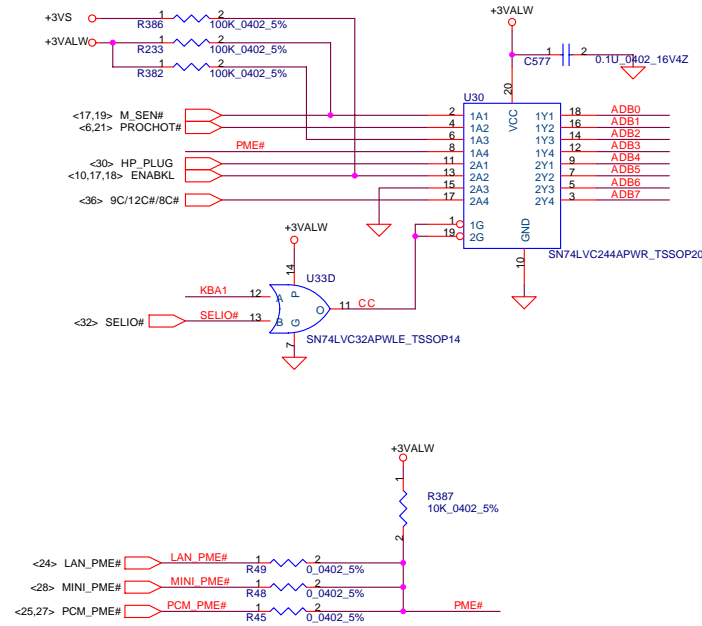
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Compal Electronics, Inc.			
Title			
MDC / SWITCH Connector			
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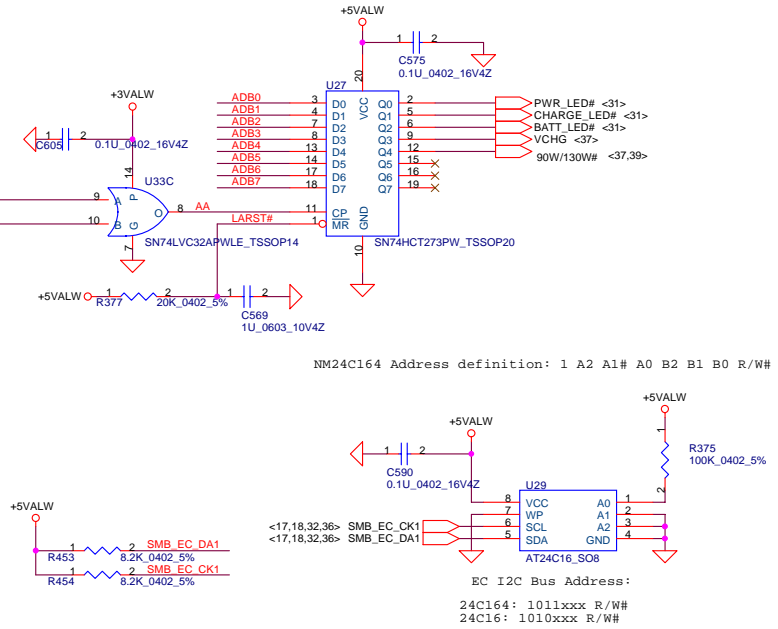
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Input Port

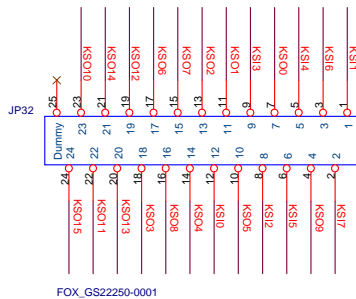


Output Port



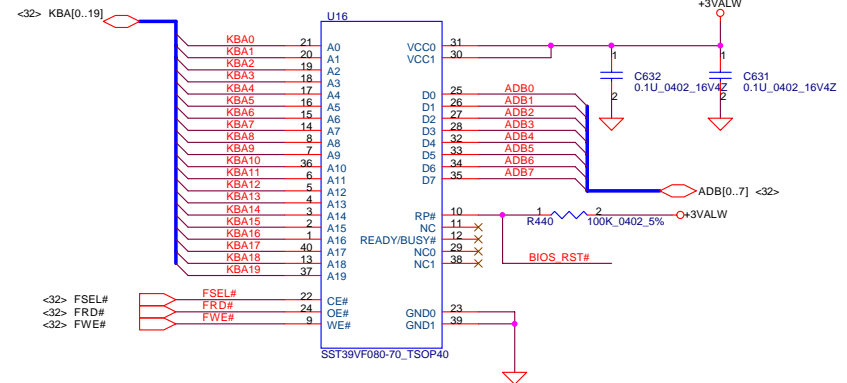
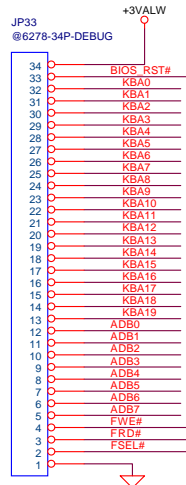
Internal KB connector

INT_KBD CONN.



FOX_GS22250-0001

can swap



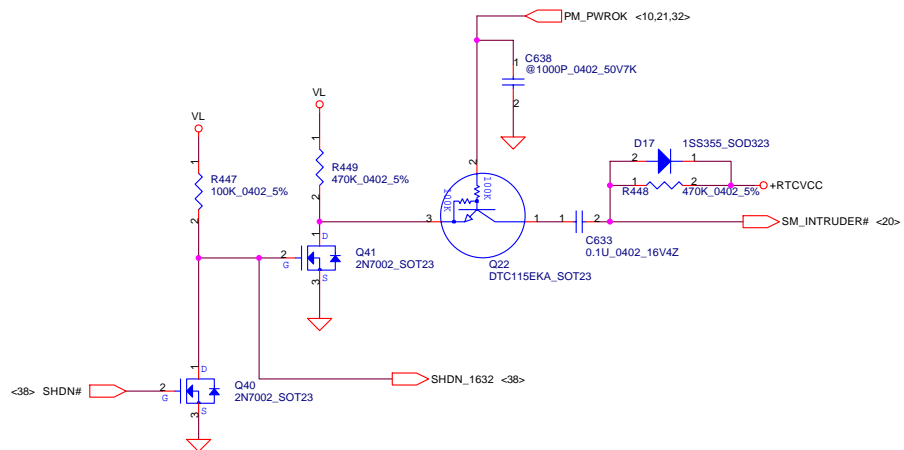
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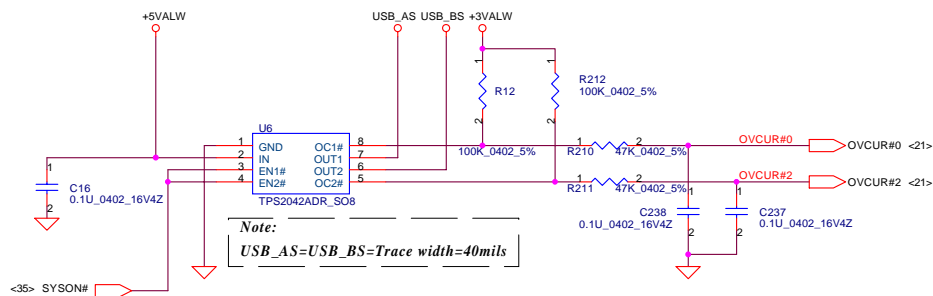
EC Extend I/O KB Conn. & BIOS

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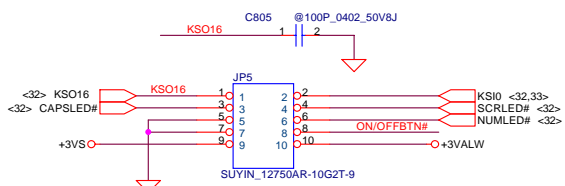
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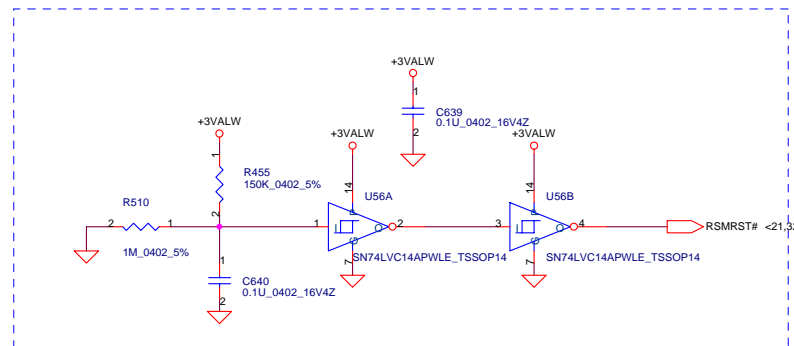
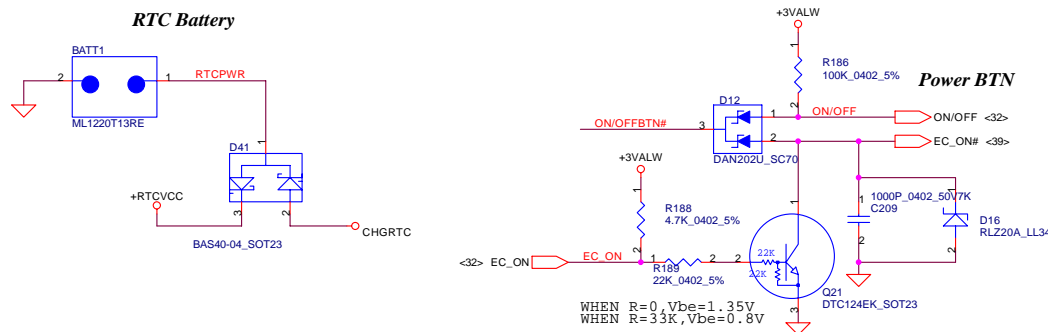
USB Over Current



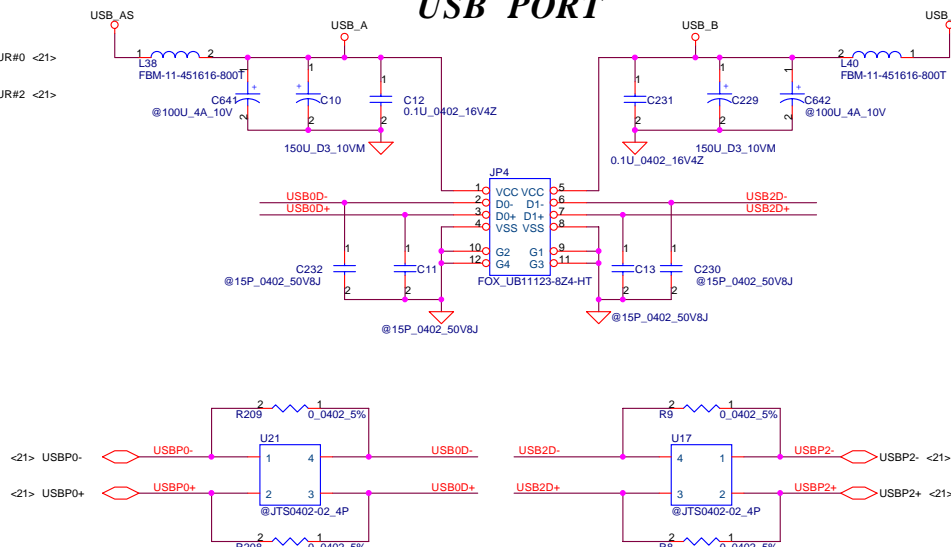
Note:
USB_AS=USB_BS=Trace width=40mils



Power SW Function Button



USB PORT



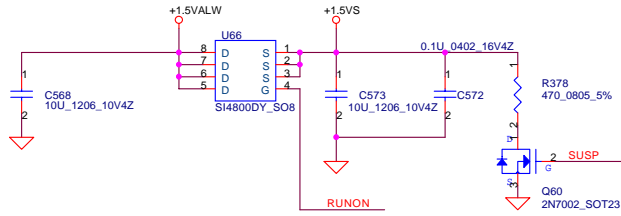
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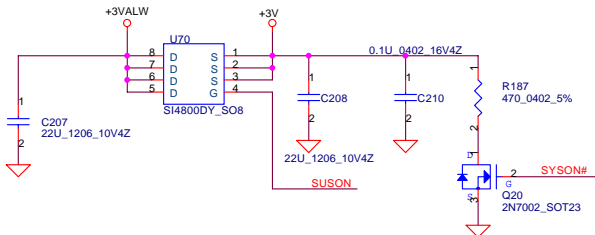
Power OK/Reset/RTC battery/USB Conn

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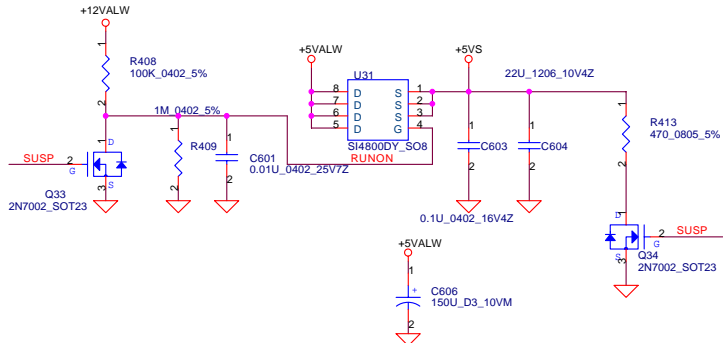
+1.5VALW to +1.5VS Transfer



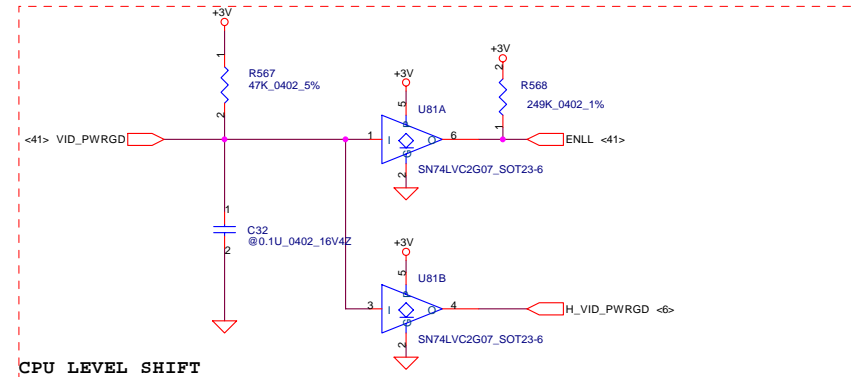
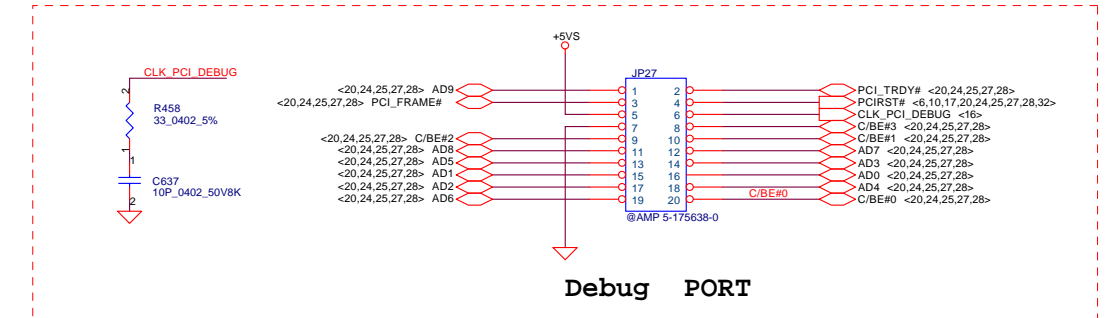
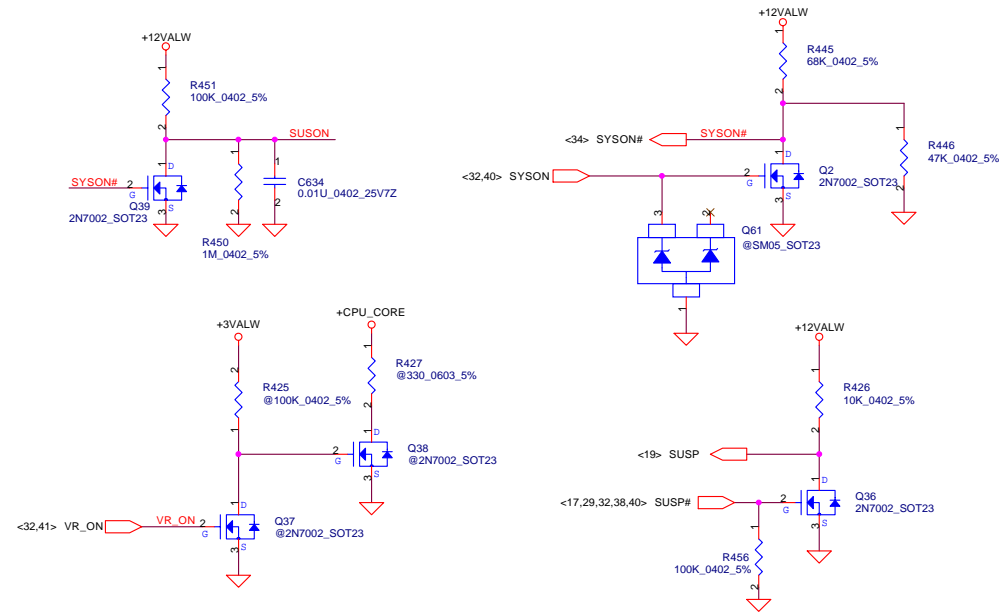
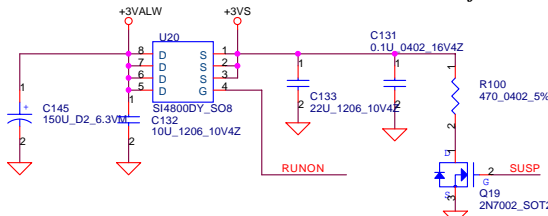
+3VALW to +3V Transfer



+5VALW to +5VS Transfer



+3VALW to +3VS Transfer



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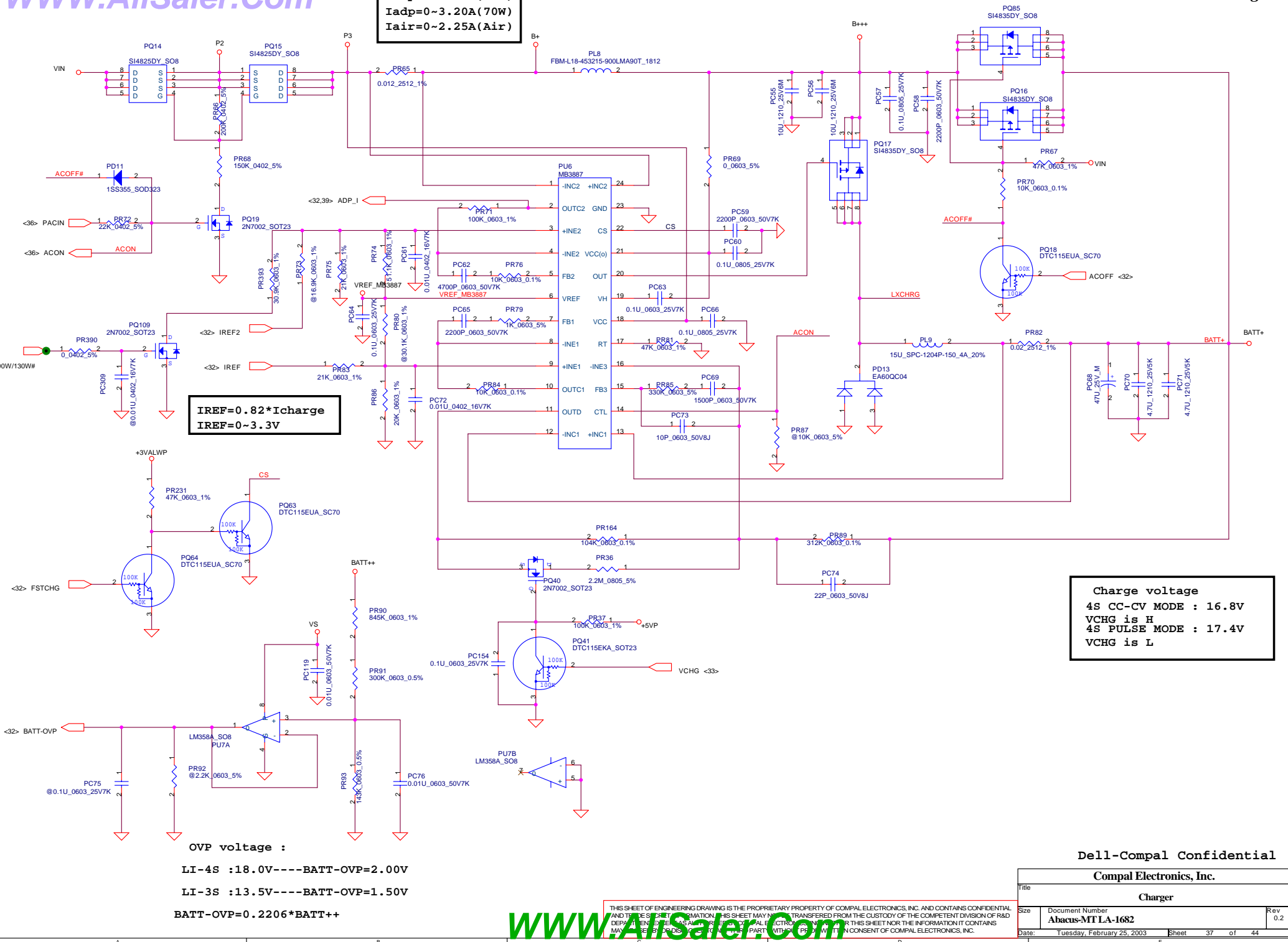
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DC/DC Circuit / Debug Port

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Iadp=0~4.10A(90W)
Iadp=0~3.20A(70W)
Iair=0~2.25A(Air)



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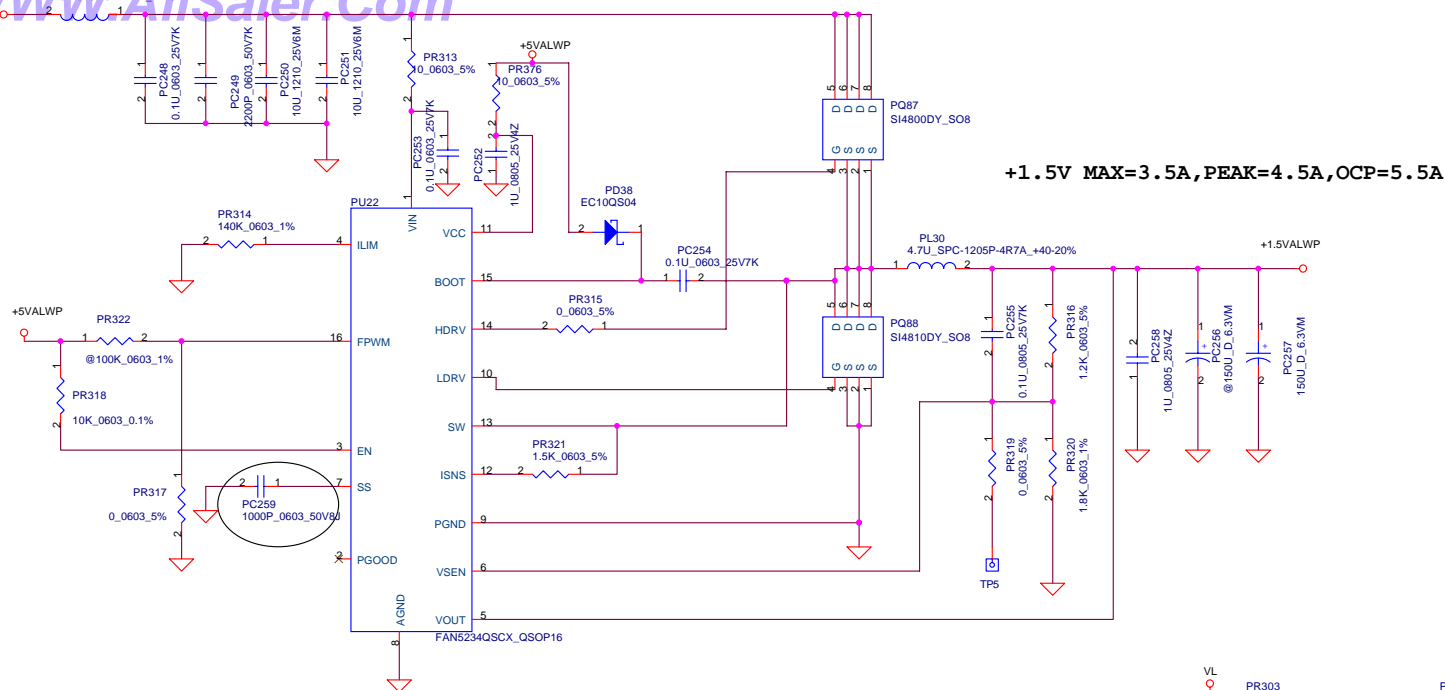
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Charger

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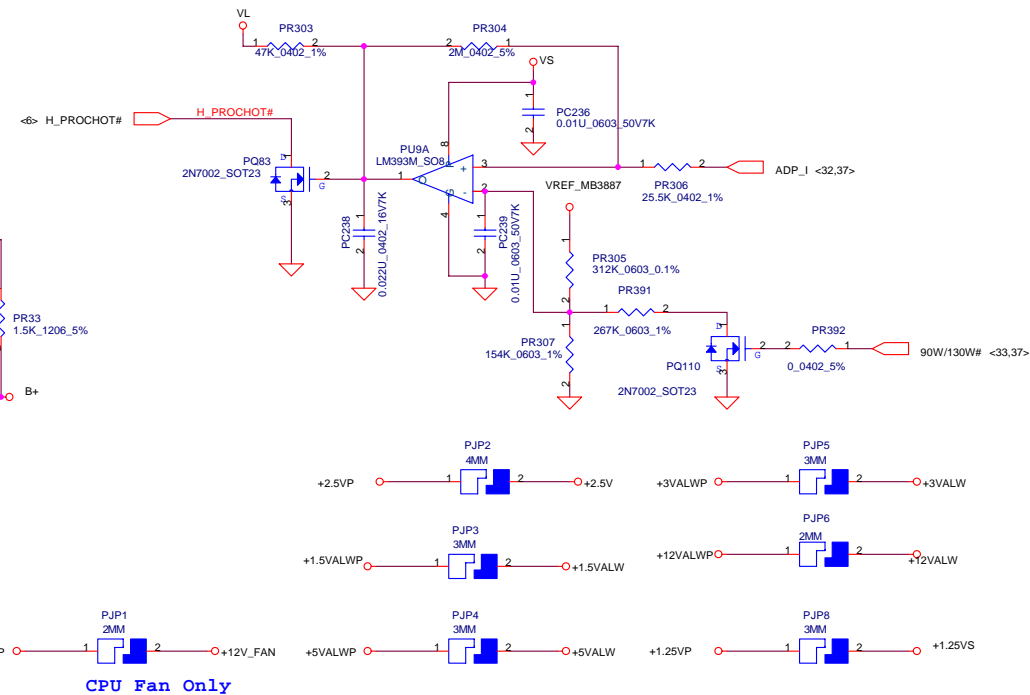
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Adaptor Current Detector(90W)
ADP_I : 1.207V.... clock throttle(lin=5.03A)
ADP_I : 1.145V....No clock throttle(lin=4.77A)

Adaptor Current Detector(130W)
ADP_I : 1.673V.... clock throttle(lin=6.97A)
ADP_I : 1.61V....No clock throttle(lin=6.71A)

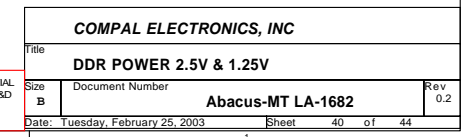


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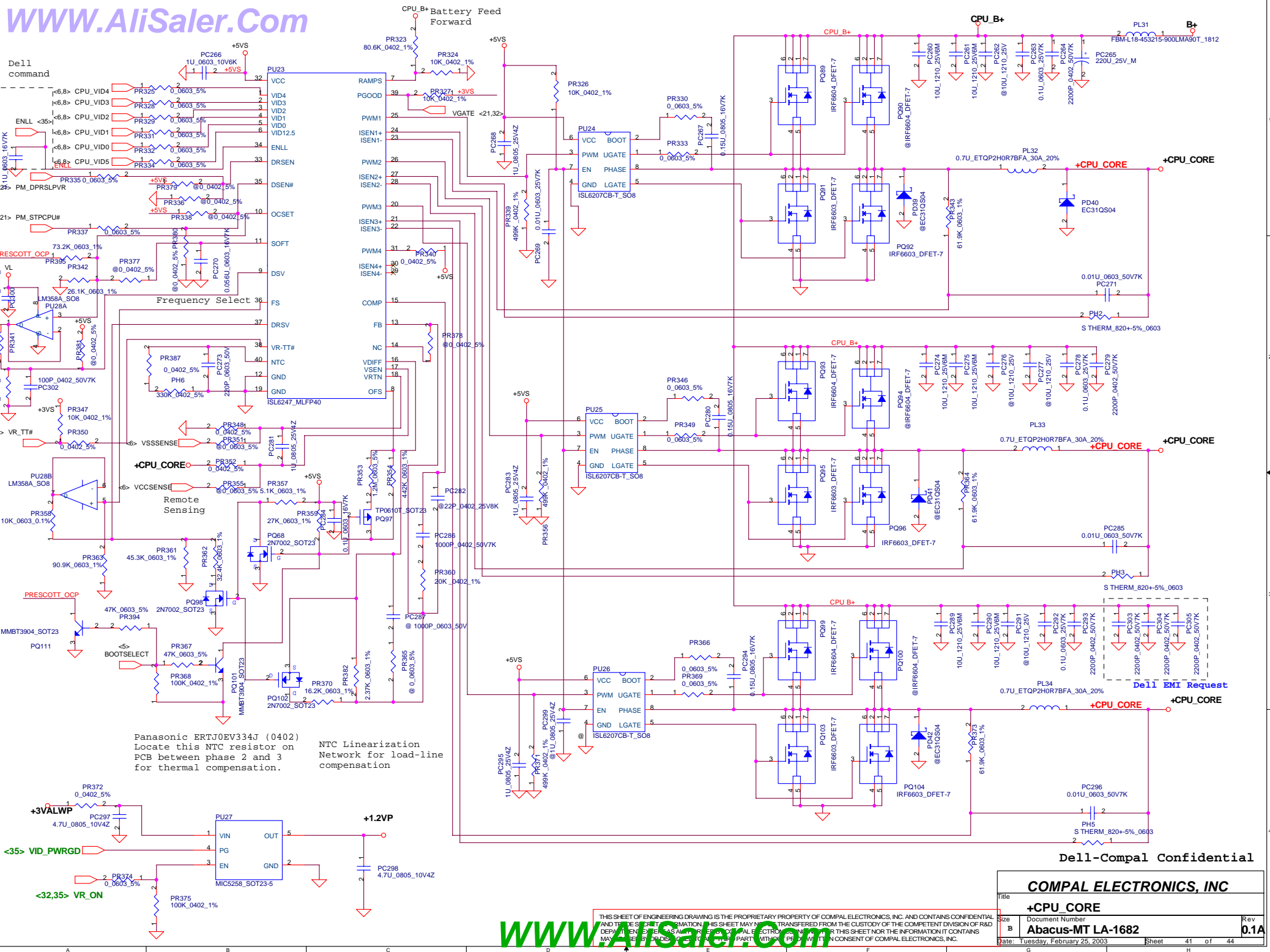
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+1.5VS

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Dell
command



I tem	Fixed Issue	Reason for change	CKT Rev.	PG#	Modify List	B.Ver#	Phase
1	+CPU_CORE voltage error	CPU ID net error	0.1A	P41	Swap net CPU_VID0 and CPU_VID4 , CPU_VID1 and CPU_VID3(rework)	0.1	SST
2	FAN turns on when system off with battery only	need to add a switch to control 12V_FAN power when system off with battery only	0.1A	P38	add a switch for 12V_FAN with PR388 200K 5% 0402 PR389 150K 5% 0402 PC307 1uF/25V 0805 PC308 0.01uF/50V 0603 PQ107 2N7002 PQ108 SI2303DS	0.2	PT
3	doulbe pulses on the output of U81.4 when the input U81.3 slowly rises to 1.58v	for H-VID_PWRGD transtion timing with VID_PWRGD meet Intel SPEC.	0.1A	P41	change PU27 CM2843 to PU27 MIC5258	0.2	PT
4	MOSFET SMT damage	to provide MOSFET damage	0.1A	P41	Change PQ89, PQ90, PQ91, PQ92, PQ93, PQ94, PQ95, PQ96, PQ99, PQ100, PQ103, PQ104 symbol footprint	0.2	PT
5	Issue found in ISL6225BCA	Oscillation behavior found in ISL6225BCA	0.1A	P40	change PU20 from ISL6225BCA to ISL6225CA		
6	Load line is not suit Intel SPEC.	Change load line	0.1A	P41	Change PR354 from 340K to 442K and PR382 from 1.91K to 2.49K	0.2	PT
7	Adapter is 90W/130W	Detect adapter 130W/90W	0.1A	P37	Add PQ109,PR390,PC309,PR393	0.2	PT
8	Change capacitor materal	Capacitor material is not available	0.1A	P38	Change PC245 from100U to 15U	0.2	PT
9	Adapter is 90W/130W	Detect adapter 130W/90W	0.1A	P39	Add PR391,PQ110,PR392,and change PR305 from 0 to 115K	0.2	PT
10	Load line test	Base on Dell power team load line test	0.1A	P41	De-pop PC282,change PR382 to 2.37K, PR361 to 45.3K,PR341 to 442 Ohm,PR344 to 25.5K,PR343,PR364,PR373 to 61.9K	0.2	PT
11	+RTCCLK and S3# will a pulse when AC plug in	delay +3VALW output	0.1A	P38	Change PC104 to 1000P	0.2	PT
12	+RTCCLK and S3# will a pulse when AC plug in	delay +1.5VALW output rise time	0.1A	P39	Change PC259 to 1000P; PD38 EC10QS04 for cost down		
13	12V FAN OCP point	Change 12V FAN OCP point,and modofy circuit	0.1A	P38	Change PR311 to 59K,PC244 to 470P, PC245 to 15uF/25V	0.2	PT
14	Issue found in ISL6225BCA	With fix PWM condition	0.1A	P40	Change PR290 to 0 and De-pop PR288	0.2	PT
15	Not easy to adjust OCP setting only, due to DVS and OCSET both within same network divider	separate OCP setting point from the DSV setting point; Particularly, use the BootSelect signal to control different OCP setting points for NW CPU and Prescott-MT CPU	0.1A	P41	Use the PU28A for DSV setting only; use PR342 26.1K for NW CPU ocp setting; for prescott-MT CPU ocp setting, add PR395 73.2K, PQ111 MMBT3904, PR394 47K, and change PR367 to 47K. Dep PR378 requested from Dell	0.2	PT
						0.2	PT
						0.2	PT

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Title		Power PIR	
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Item	Fixed Issue	Reason for change	CKT Rev.	PG#	Modify List	B.Ver#	Phase
1	System can't turn on	B+ is shutdown when AC in,Because the timing sequence of +12VALW is later than +12V_FAN	0.1A	P7	Change U76 VCC net from +12VALW to +12V_FAN(rework)	0.1	SST
2	H_VID_PWRGD delay time from VID_PWRGD is not enough	VID_PWRGD with H_VID_PWRGD Sequence need to meet the Intel specification (H_VID_PWRGD delay 1~10ms from VID_PWRGD)	0.1A	P35	Change R567 on BOM SD028100200 10K_0402_5% to SD028200200 20K_0402_5% and add C32 0.1U_0402_16V4Z	0.2	PT
3	Abacus and Abacus-MT K/B is different	Change K/B connector to Abacus compatible	0.1A	P33	Change K/B connector JP32 from SP01J00133L S H-CONN JAE FK2S030W11 30P to SP01F005110 S H-CONN FOXCONN GS22250-0001 25P P1 and delete the net KSO17 and C805	0.2	PT
4	LA-1682 MB INVPWR_B+ can't used the LS-1452 VGA BD	We will use the LS-1452 to BDW11/12 project, will reduce some parts for External Graphic	0.1A	P17	Change net pin 164/166/168/170 of JP8 from INVPWR_B+ to B+ and Q71, C793, C795, R560, R562, Q74 add "1@"	0.2	PT
5	Board ID change	Board ID change for EC code, due to the KB change	0.1A	P32	Change Board ID to 0.5V ,So replace and pop the R393 with SD028910200 S RES 1/16W 91K +-5% 0402	0.2	PT
6	KB back to Abacus	JP5 pin1 signal KSO17 change to KSO16	0.1A	P34	JP5 pin1 signal KSO17 change to KSO16	0.2	PT
7	Prevent EMI impact	Prevent CLK_AGP_66M antenna impact when no used	0.1A	P17	Add R17 1@33_0402_5% (SD028330A00 S RES 1/16W 33 +-5% 0402) And C33 1@10P_0402_25V8K (SE068100K00 S CER CAP 10P 25V +-10% NPO 0402)	0.2	PT
8	Lan EEPROM Material control	U8 will used the eeprom same as Abacus	0.1A	P24	Change the BOM U8 from SA093461030 without LAN code to SA093461040 with Abacus LAN code	0.2	PT
9	Extra connector	Jp33 just for A-test BIOS debug connector	0.1A	P33	Remove Jp33 on BOM	0.2	PT
10	RTCCLK ringback	Need to add series termination on RTCCLK at the ICH because of signal quality/undershoot and ringback at Q69	0.1A	P21	Add R18 SD028220A00 S RES 1/16W 22 +-5% 0402 and C62 SE068101K00 S CER CAP 100P 25V +-10% NPO 0402	0.2	PT
11	Part Number error	Correct U77 A2 revision Part Number	0.1A	P21	Change the BOM U77 from SA243500000 S IC RG82G4350M A1 UFCBGA-732 MONTARA-GT to SA828520100 S IC RG82852GME A2 UFCBGA-732 MONTARA-GT.	0.2	PT SST
12	Reversed the capacitor about RTCCLK circuit	Just do the reserved the RTCCLK modify waveform cap.	0.1A	P21	Depop the C62 (add @)	0.2	PT
13	Extra Pads about @C659 & @C660	Remove capacitor @C659 & @C660 extra component from PCB because we have not used.	0.1A	P7	Depop the parts C659 & C660 from Circuit & PCB	0.2	PT
14	H_VID_PWRGD waveform have negative pulse after rise up at VID_PWRGD voltage at 1.58V(riseing)	H_VID_PWRGD waveform abnormal	0.1A	P35	Change R567 on BOM from SD028200200 20K_0402_5% to SD028470200 10K_0402_5% and pop C32 0.1U_0402_16V4Z	0.2	PT
15	Default the ITPCLK/ITPCLK# to Intel circuit specification.	For meet Intel specification	0.1A	P6	Add @ to RP61 and add SD014499A09 49.9 +-1% 0603 R572/R573 for ITPCLK/ITPCLK# pull down	0.2	PT
16	Audio cost reduction from Dell request	Cost reduction	0.1A	P29 P30	Depop the parts C481, C554, C551 C553, C483, C622, C623, C624 change from 1uF to 0.1uF	0.2	PT
17	Improve audio performance	Improve audio performance	0.1A	P29	Populate C490 1uF	0.2	PT
18	Investigate Beep circuit cost down	Cost	0.1A	P30	Add R132 0 ohm, but depop. Test at PT step	0.2	PT
19	Fix HP plug in phonejack delay time	Plug in External SPK will delay some timing	0.1A	P30	C588 change from 4.7uF_0805 to 0.47uF_0603, and depop C580	0.2	PT
20	Reversed the capacitor about Fan circuit	C687 & C701 make the voltage leakage so depop the parts .	0.1A	P7	Depop the parts C687,C701 (add @)	0.2	PT
21	1394 can not link at 400 speed.	Improve 1394 link test by TI test tool	0.1A	P25	Depop C223, C216, R198, R197, R196, R194, R199 add C822(270P), C823(1uF), R574(5.1K), R575-R578(56.2)	0.2	PT

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