DR1 (Roberts) Schematics Document

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2008-10-02

REV : A00

DY : Nopop Component

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Cover Page

Size: Custom | Document Number: Roberts | Rev: A00

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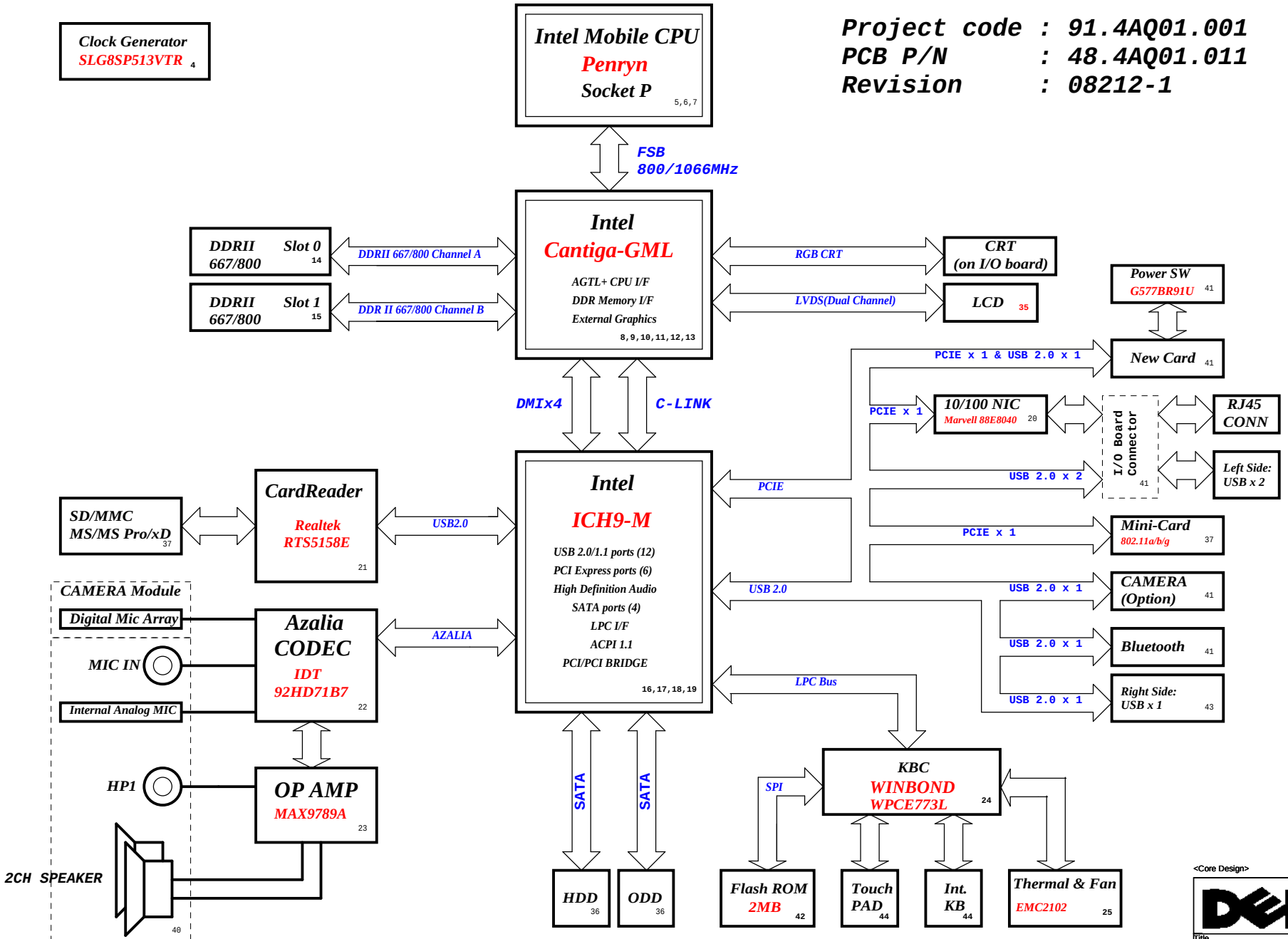
Roberts Block Diagram

Project code : 91.4AQ01.001
PCB P/N : 48.4AQ01.011
Revision : 08212-1



CPU DC/DC ISL6266A 28,29

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51117 30

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC MAX17020 27

INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 31

INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

SYSTEM DC/DC APL5912 32

INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC LDO 34

INPUTS	OUTPUTS
+5V_ALW	+5V_RUN
+3.3V_ALW	+3.3V_RUN

MAXIM CHARGER MAX8731A 26

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3 DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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Title: Table of Content

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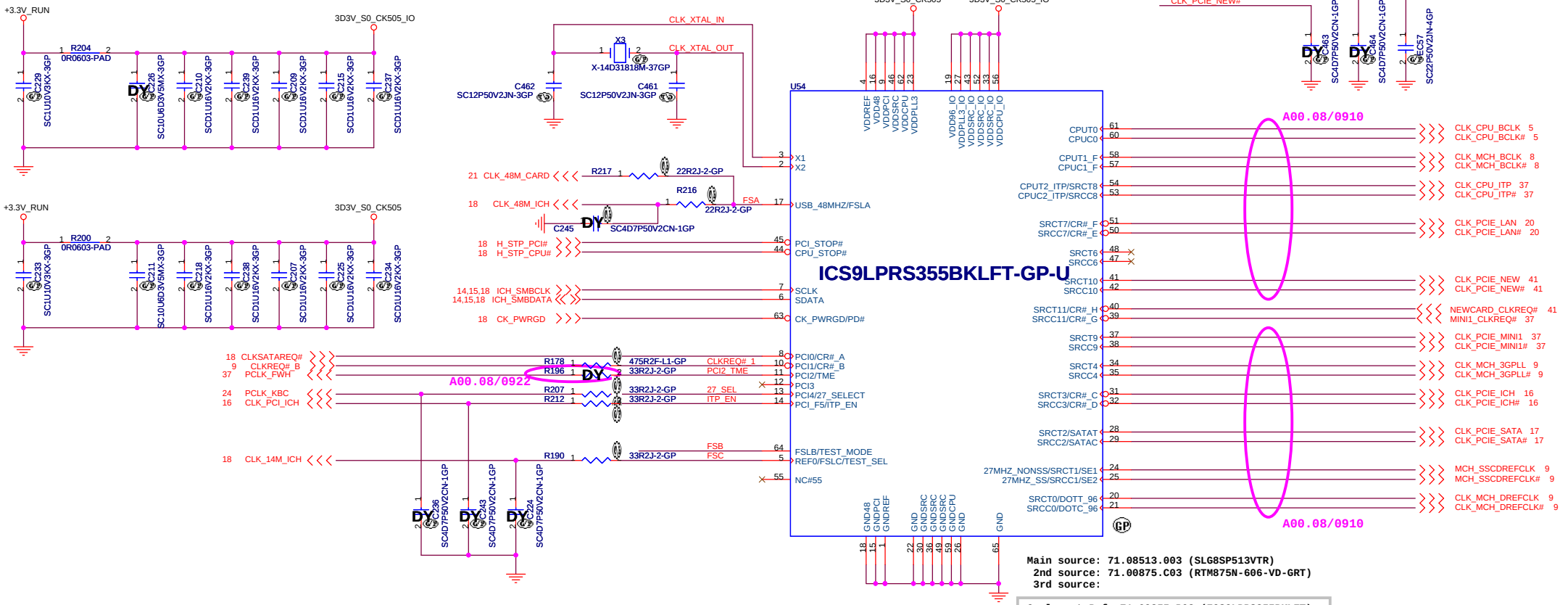
SSID = CLOCK



ITP_EN	Output
0	SRC8
1	CPU_ITP

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	GM45
1	SRCT0	SRCC0	PM45

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator SLG8SP513VTR

Size: Custom | Document Number: Roberts | Rev: A00

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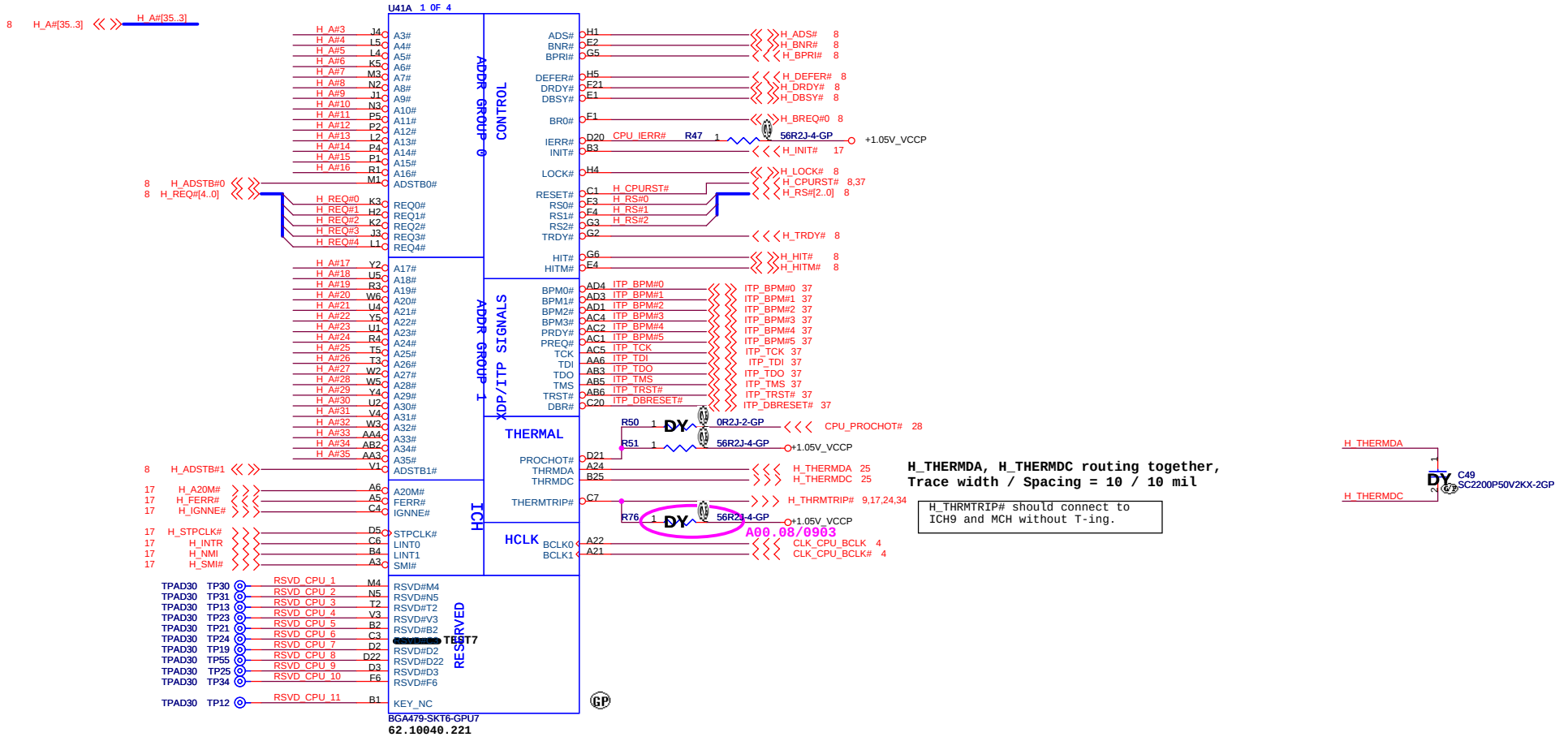
SSID = CPU



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Title: CPU-FSB(1/3)

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SSID = CPU

H_DINV#[3..0] H_DINV#[3..0] 8
H_DSTBN#[3..0] H_DSTBN#[3..0] 8
H_DSTBP#[3..0] H_DSTBP#[3..0] 8
H_D#[63..0] H_D#[63..0] 8

U41B 2 OF 4

DATA GRP0 / DATA GRP2 / DATA GRP1 / DATA GRP3

H_D#0	E22	D0#	D32#	Y22	H_D#32
H_D#1	F24	D1#	D33#	AB24	H_D#33
H_D#2	E26	D2#	D34#	V24	H_D#34
H_D#3	G22	D3#	D35#	V26	H_D#35
H_D#4	F23	D4#	D36#	V23	H_D#36
H_D#5	G25	D5#	D37#	T22	H_D#37
H_D#6	E25	D6#	D38#	U25	H_D#38
H_D#7	E23	D7#	D39#	U23	H_D#39
H_D#8	K24	D8#	D40#	Y25	H_D#40
H_D#9	G24	D9#	D41#	W22	H_D#41
H_D#10	J24	D10#	D42#	Y23	H_D#42
H_D#11	J23	D11#	D43#	W24	H_D#43
H_D#12	H22	D12#	D44#	W25	H_D#44
H_D#13	E26	D13#	D45#	AA23	H_D#45
H_D#14	K22	D14#	D46#	AA24	H_D#46
H_D#15	H23	D15#	D47#	AB25	H_D#47
8 H_DSTBN#0	J26	DSTBN0#	DSTBN2#	Y26	H_DSTBN#2 8
8 H_DSTBP#0	H26	DSTBP0#	DSTBP2#	AA26	H_DSTBP#2 8
8 H_DINV#0	H25	DINV0#	DINV2#	U22	H_DINV#2 8
H_D#16	N22	D16#	D48#	AE24	H_D#48
H_D#17	K25	D17#	D49#	AD24	H_D#49
H_D#18	P26	D18#	D50#	AA21	H_D#50
H_D#19	R23	D19#	D51#	AB22	H_D#51
H_D#20	L23	D20#	D52#	AB21	H_D#52
H_D#21	M24	D21#	D53#	AC26	H_D#53
H_D#22	L22	D22#	D54#	AD20	H_D#54
H_D#23	M23	D23#	D55#	AE22	H_D#55
H_D#24	P25	D24#	D56#	AF23	H_D#56
H_D#25	P23	D25#	D57#	AC25	H_D#57
H_D#26	P22	D26#	D58#	AF21	H_D#58
H_D#27	T24	D27#	D59#	AD21	H_D#59
H_D#28	R24	D28#	D60#	AC22	H_D#60
H_D#29	L25	D29#	D61#	AD23	H_D#61
H_D#30	T25	D30#	D62#	AF22	H_D#62
H_D#31	N25	D31#	D63#	AC23	H_D#63
8 H_DSTBN#1	L26	DSTBN1#	DSTBN3#	AE25	H_DSTBN#3 8
8 H_DSTBP#1	M26	DSTBP1#	DSTBP3#	AF24	H_DSTBP#3 8
8 H_DINV#1	N24	DINV1#	DINV3#	AC20	H_DINV#3 8

MISC

	AD26	GTLREF	COMP0	R26	COMP0 R350 1 27D4R2F-L1-GP
R53 1 DY 1KR2J-1-GP TEST1	C23	TEST1	COMP1	U26	COMP1 R349 1 54D9R2F-L1-GP
R60 1 DY 1KR2J-1-GP TEST2	D25	TEST2	COMP2	AA1	COMP2 R14 1 27D4R2F-L1-GP
R58 1 DY 1KR2J-1-GP CPU_TEST3	C24	TEST3	COMP3	Y1	COMP3 R13 1 54D9R2F-L1-GP
R7 1 DY 1KR2J-1-GP CPU_TEST5	AE26	TEST4			
	AF1	TEST5	DPRSTP#	E5	H_DPRSTP# 9,17,28
	A26	TEST6	DPSLP#	B5	H_DPSLP# 17
			DPWR#	D24	H_DPWR# 8
4 CPU_BSEL0	B22	BSEL0	PWRGOOD	D6	H_PWRGOOD 17,34
4 CPU_BSEL1	B23	BSEL1	SLP#	D7	H_CPUSLP# 8
4 CPU_BSEL2	C21	BSEL2	PSI#	AE6	PSI# 28

BGA479-SKT6-GPU7
62.10040.221

Layout notes
Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

+1.05V_VCCP
R357 1KR2F-3-GP
CPU_GTLREF0
R354 2KR2F-3-GP
DY C376 SC1KP50V2KX-1GP

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Route the CPU_TEST3 and CPU_TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

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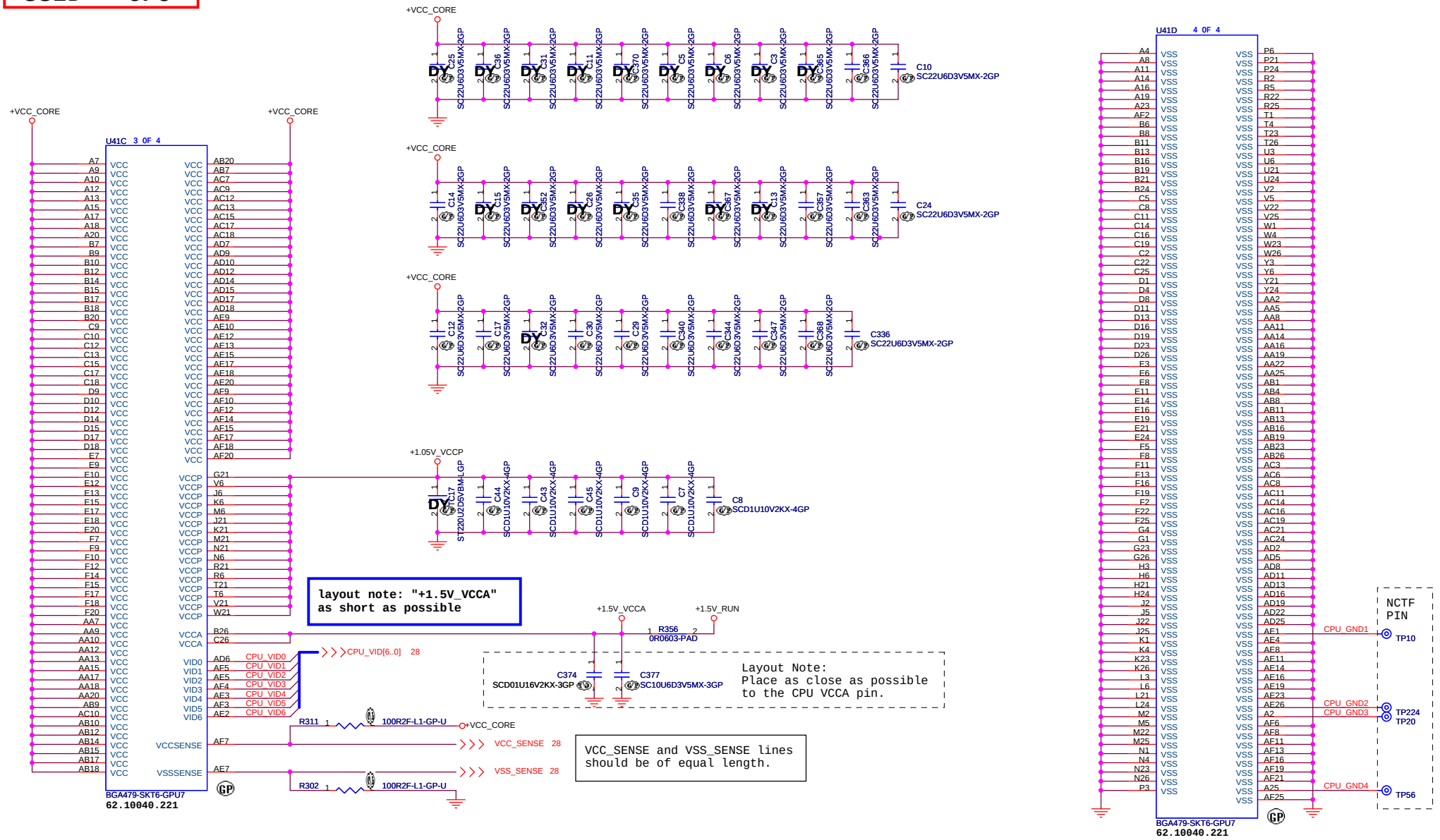
Title: CPU-FSB(2/3)
Size: Custom | Document Number: Roberts | Rev: A00
Date: Thursday, October 02, 2008 | Sheet 6 of 58

SSID = CPU



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Title: CPU-Power(3/3)

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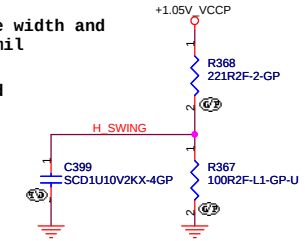
Date: Thursday, October 02, 2008 | Sheet 7 of 58

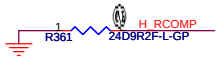
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

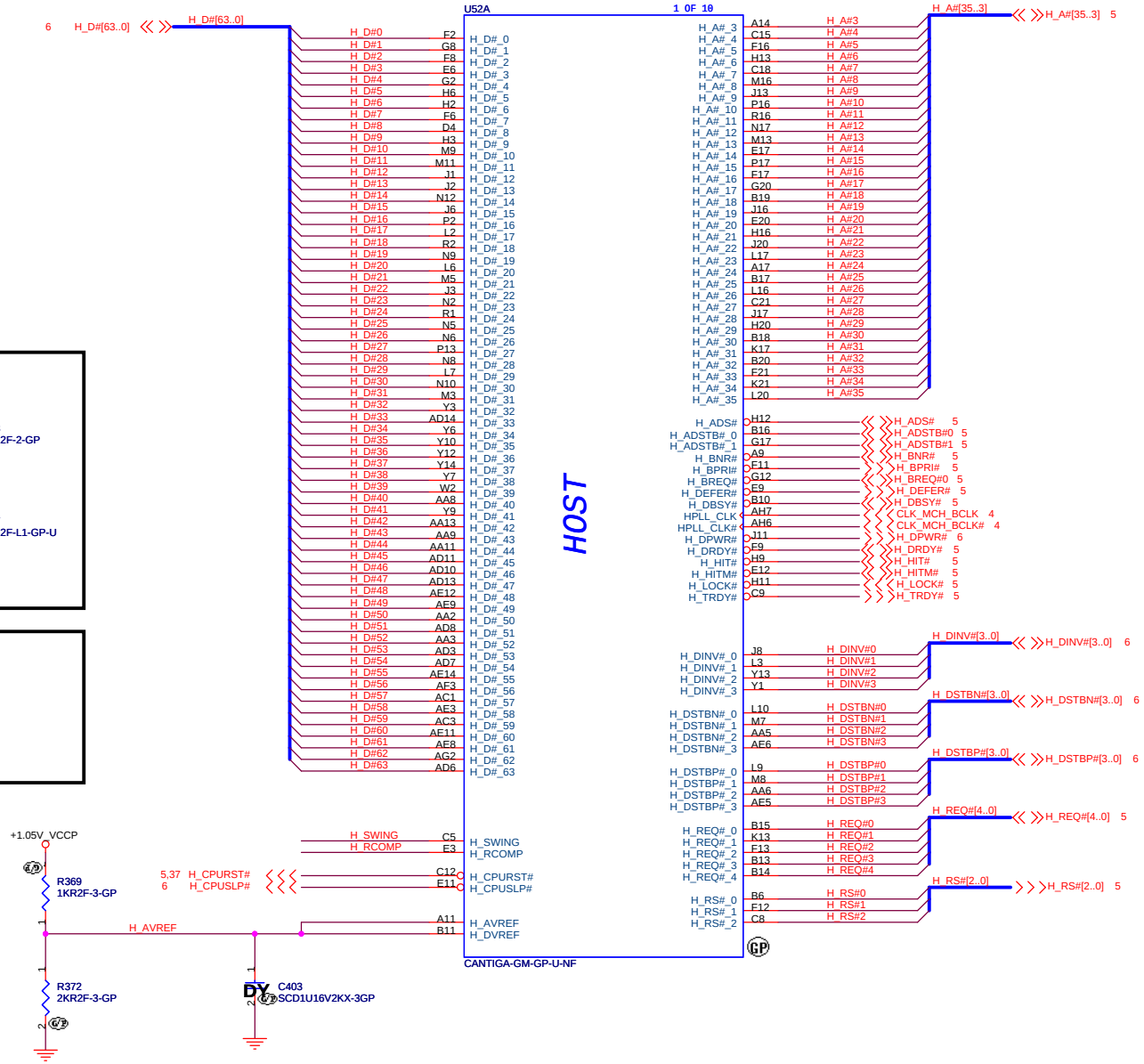
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R51 near to the chip (< 0.5")



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Title: Cantiga-HOST(1/6)

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SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled

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RSVD: RESERVED#M36, RESERVED#N36, RESERVED#R33, RESERVED#T33, RESERVED#AH9, RESERVED#AH10, RESERVED#AH12, RESERVED#AH13, RESERVED#K12, RESERVED#AL34, RESERVED#AK34, RESERVED#AN35, RESERVED#AM35, RESERVED#T24, RESERVED#B31, RESERVED#B2, RESERVED#M1, RESERVED#AY21, RESERVED#BG23, RESERVED#BF23, RESERVED#BH18, RESERVED#BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0, SA_CK_1, SB_CK_0, SB_CK_1, SA_CK#_0, SA_CK#_1, SB_CK#_0, SB_CK#_1, SA_CKE_0, SA_CKE_1, SB_CKE_0, SB_CKE_1, SA_CS#_0, SA_CS#_1, SB_CS#_0, SB_CS#_1, SA_ODT_0, SA_ODT_1, SB_ODT_0, SB_ODT_1, SM_RCOMP, SM_RCOMP#, SM_RCOMP_VOH, SM_RCOMP_VOL, SM_VREF, SM_PWROK, SM_REXT, SM_DRAMRST#

CLK: DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#, PEG_CLK, PEG_CLK#

DMI: DMI_RXN_0..3, DMI_RXP_0..3, DMI_TXN_0..3, DMI_TXP_0..3

CFG: CFG_0..CFG_20

GRAPHICS VID: GFX_VID_0..4, GFX_VR_EN

PM: PM_SYNC#, PM_DPRSTP#, PM_EXT_TS#_0, PM_EXT_TS#_1, PWROK, RSTIN#, THERMTRIP#, DPRSLPVR

ME: CL_CLK, CL_DATA, CL_PWROK, CL_RST#, CL_VREF

MISC: DDPC_CTRLCLK, DDPC_CTRLDATA, SDVO_CTRLCLK, SDVO_CTRLDATA, CLKREQ#, ICH_SYNC#, TSATN#

HDA: HDA_BCLK, HDA_RST#, HDA_SDI, HDA_SDO, HDA_SYNC

NC: NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

CANTIGA-GM-GP-U-NF

FSB setting: MCH_CLKSEL0, MCH_CLKSEL1, MCH_CLKSEL2

R104 2K21R2F-GP CFG11; R128 2K21R2F-GP CFG18; R117 4K02R2F-GP CFG19; R121 4K02R2F-GP CFG20; RN20 SRN10KJ-5-GP PM_EXTTS#0 PM_EXTTS#1

R383 2K21R2F-GP CFG5; R112 2K21R2F-GP CFG6; R111 2K21R2F-GP CFG7; R102 2K21R2F-GP CFG8; R382 4K02R2F-GP CFG9; R375 2K21R2F-GP CFG10; R101 2K21R2F-GP CFG12; R105 2K21R2F-GP CFG13; R103 2K21R2F-GP CFG16

R380 80D6R2F-L-GP; R377 80D6R2F-L-GP; R142 10KR2J-3-GP; R145 10KR2J-3-GP; R374 499R2F-2-GP; R122 1KR2F-3-GP; R116 3K01R2F-3-GP; R119 1KR2F-3-GP; C159 SC2D2U10V3KX-1GP; C162 SCD01U16V2KX-3GP; C145 SC2D2U10V3KX-1GP; C151 SCD01U16V2KX-3GP

R370 56R2J-4-GP; R371 10KR2J-3-GP; Q19 MMBT3904WT1G-GP; TSATN#_KBC

R126 1KR2F-3-GP; R130 499R2F-2-GP; C175 SCD1U10V2KX-4GP; MCH_CLVREF ~= 0.35V

R131 10KR2J-3-GP; CLKREQ#_B

R94 100R2F-L1-GP-U; C94 SC100P50V2JN-3GP

TP86, TP88, TP84, TP85, TP87, TP271

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Title: Cantiga-DMI/CFG(2/6)

Size: Custom | Document Number: Roberts | Rev: A00

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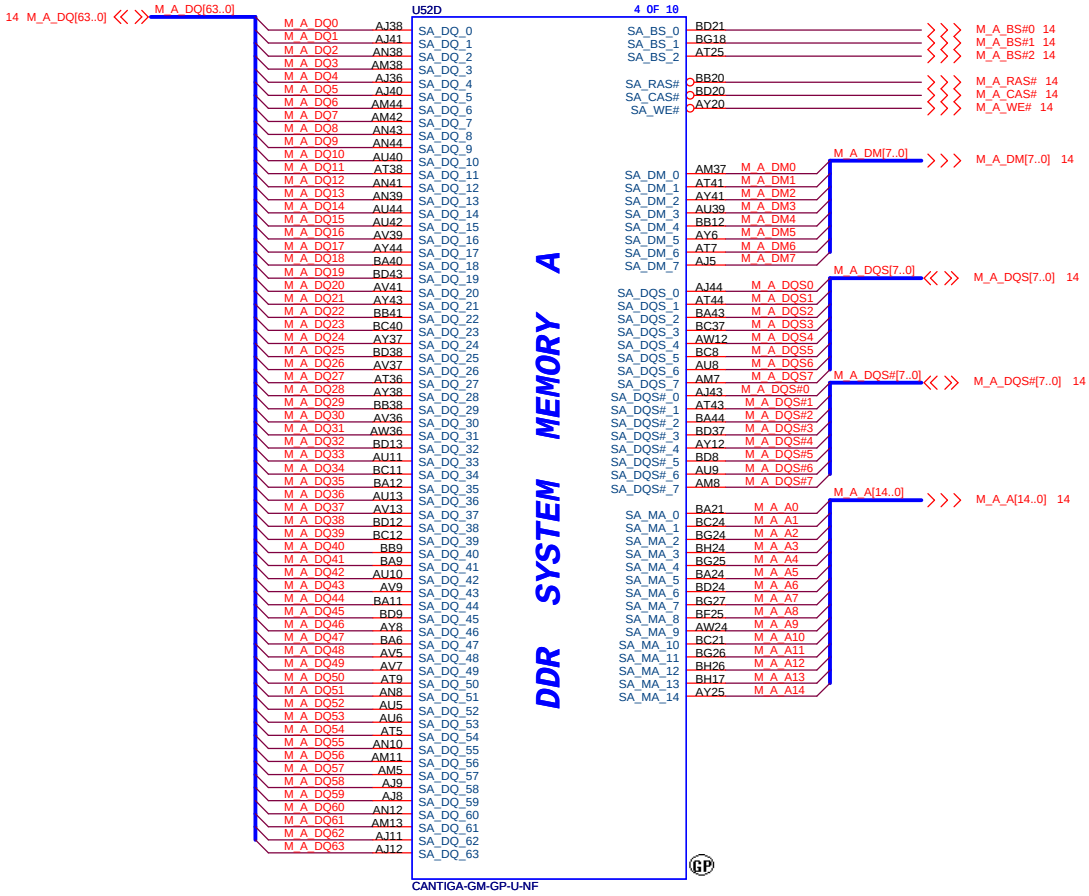
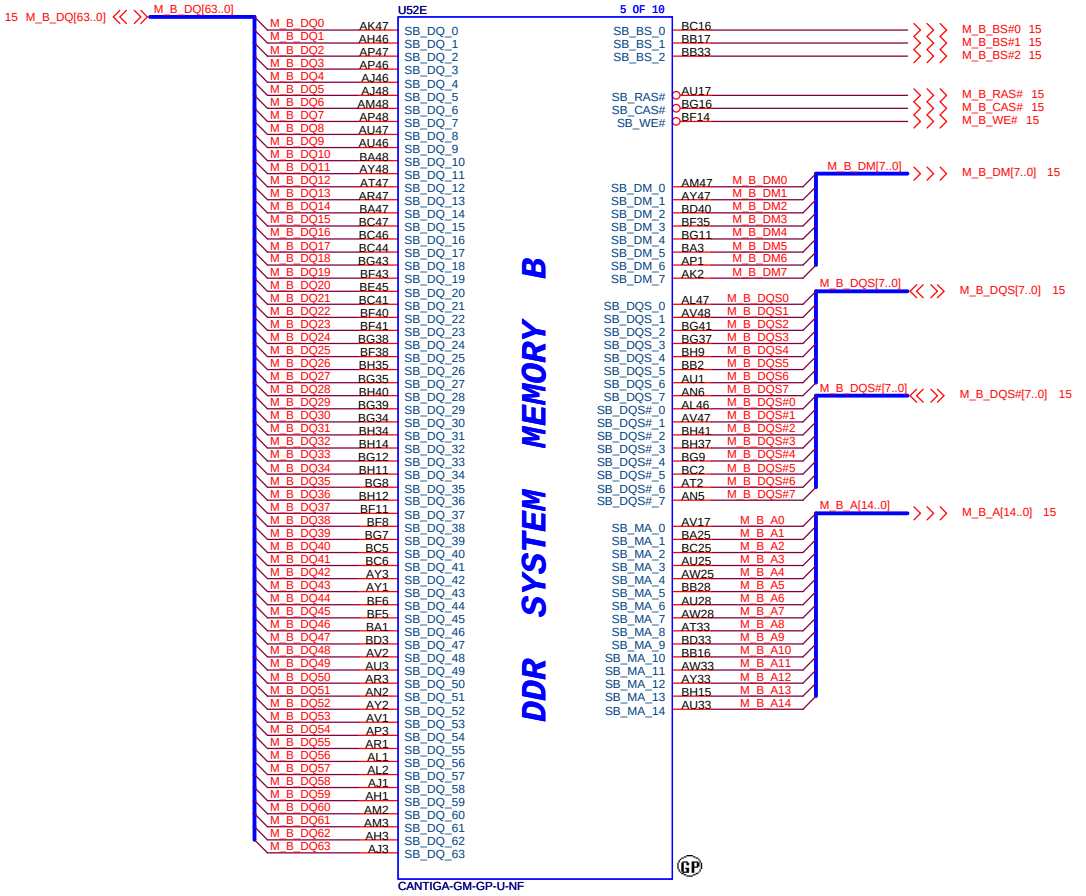
SSID = MCH





<Core Design>

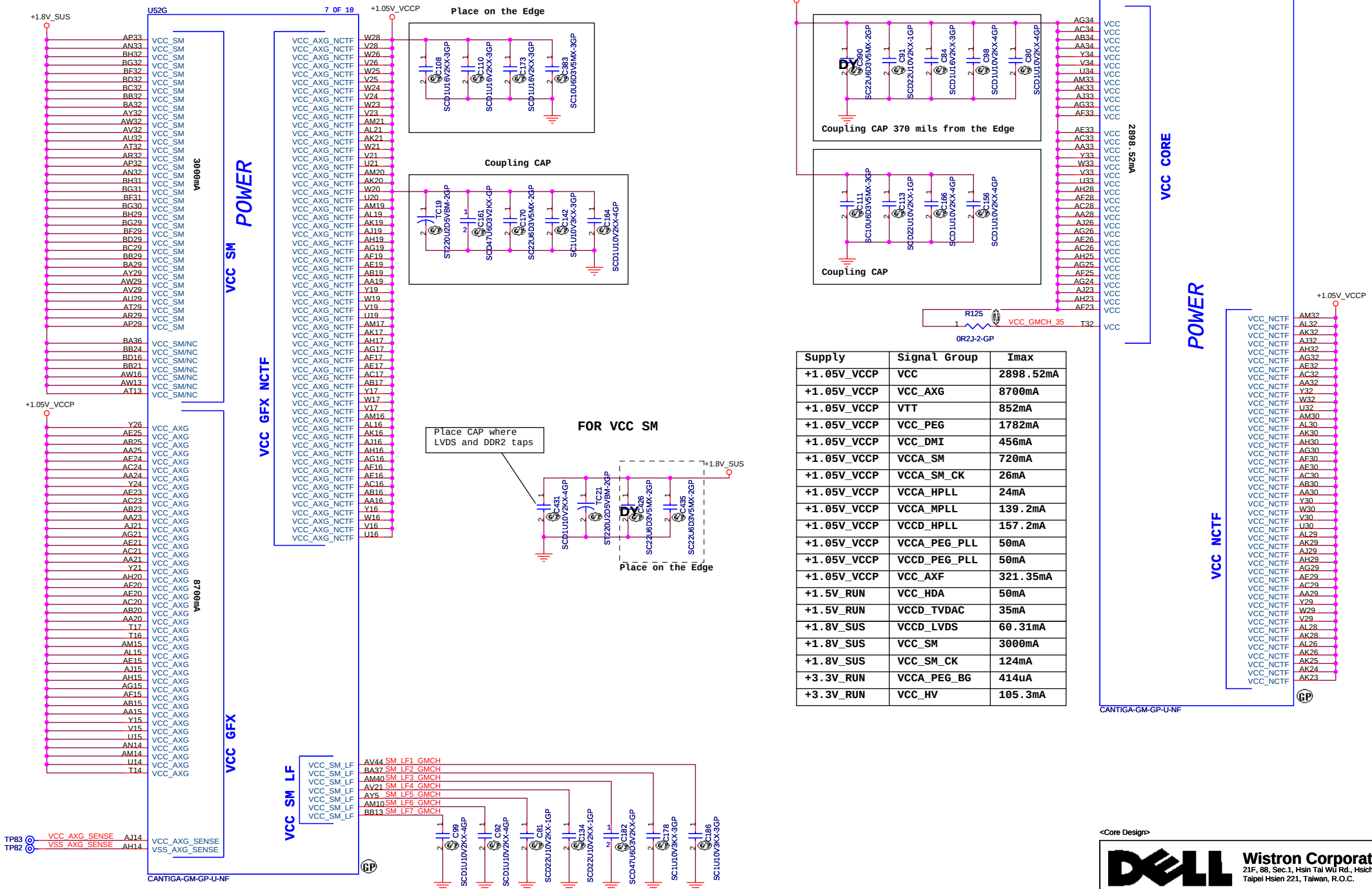
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DDR(3/6)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 10 of 58

SSID = MCH



FOR VCC CORE

Supply	Signal Group	Imax
+1.05V_VCCP	VCC	2898.52mA
+1.05V_VCCP	VCC_AXG	8700mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCC_HDA	50mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCCD_LVDS	60.31mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+3.3V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

<Core Design>

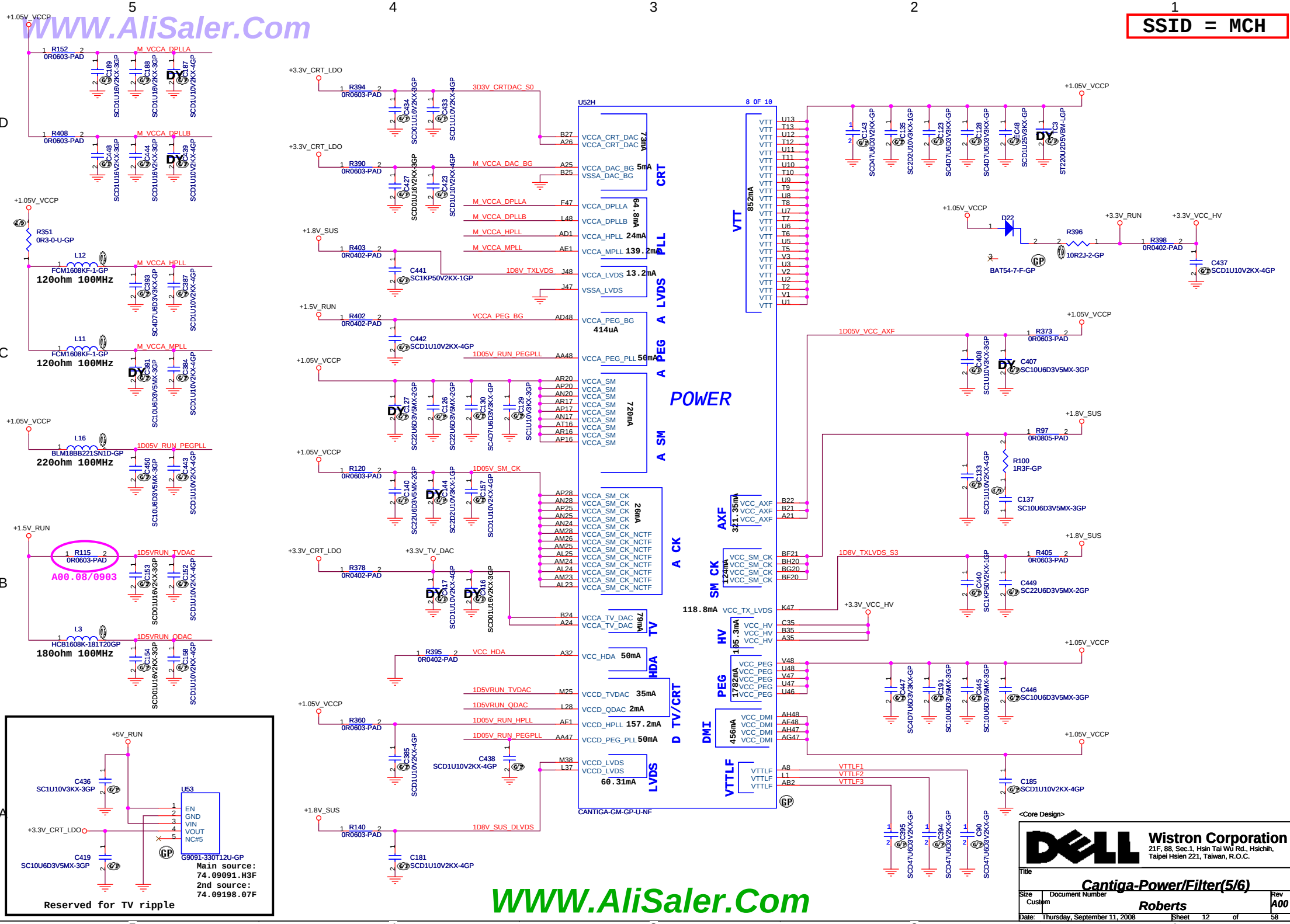
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Power(4/6)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, September 11, 2008 | Sheet 11 of 58

SSID = MCH



SSID = MCH

U52I 9 OF 10

VSS

CANTIGA-GM-GP-U-NF

U52J 10 OF 10

VSS

VSS_NCTF

VSS_SCB

NC

CANTIGA-GM-GP-U-NF

NCTF PIN

U52C 3 OF 10

PCI-EXPRESS GRAPHICS

LVDS

VGA

CANTIGA-GM-GP-U-NF

Place R105 close to MCH within 500 mils.

CRT_IREF routing Trace width use 20 mil.

5V @ ext. CRT side

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-GND/LVDS/VGA(6/6)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 13 of 58

SSID = MEMORY

10 M_A_DQS#[7..0]
10 M_A_DQ[63..0]
10 M_A_DM[7..0]
10 M_A_DQS[7..0]
10 M_A_A[14..0]

DM2

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
M_A_A14 86 A14
84 A15
10 M_A_BS#2 85 A16/BA2
M_A_BS#0 107 BA0
10 M_A_BS#1 106 BA1

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 17 DQ2
M_A_DQ3 19 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 14 DQ6
M_A_DQ7 16 DQ7
M_A_DQ8 23 DQ8
M_A_DQ9 25 DQ9
M_A_DQ10 35 DQ10
M_A_DQ11 37 DQ11
M_A_DQ12 20 DQ12
M_A_DQ13 22 DQ13
M_A_DQ14 36 DQ14
M_A_DQ15 38 DQ15
M_A_DQ16 43 DQ16
M_A_DQ17 45 DQ17
M_A_DQ18 55 DQ18
M_A_DQ19 57 DQ19
M_A_DQ20 44 DQ20
M_A_DQ21 46 DQ21
M_A_DQ22 56 DQ22
M_A_DQ23 58 DQ23
M_A_DQ24 61 DQ24
M_A_DQ25 63 DQ25
M_A_DQ26 73 DQ26
M_A_DQ27 75 DQ27
M_A_DQ28 62 DQ28
M_A_DQ29 64 DQ29
M_A_DQ30 74 DQ30
M_A_DQ31 76 DQ31
M_A_DQ32 123 DQ32
M_A_DQ33 125 DQ33
M_A_DQ34 135 DQ34
M_A_DQ35 137 DQ35
M_A_DQ36 124 DQ36
M_A_DQ37 126 DQ37
M_A_DQ38 134 DQ38
M_A_DQ39 136 DQ39
M_A_DQ40 141 DQ40
M_A_DQ41 143 DQ41
M_A_DQ42 151 DQ42
M_A_DQ43 153 DQ43
M_A_DQ44 140 DQ44
M_A_DQ45 142 DQ45
M_A_DQ46 152 DQ46
M_A_DQ47 154 DQ47
M_A_DQ48 157 DQ48
M_A_DQ49 159 DQ49
M_A_DQ50 173 DQ50
M_A_DQ51 175 DQ51
M_A_DQ52 158 DQ52
M_A_DQ53 160 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 179 DQ56
M_A_DQ57 181 DQ57
M_A_DQ58 189 DQ58
M_A_DQ59 191 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 11 DQS0#
M_A_DQS#1 29 DQS1#
M_A_DQS#2 49 DQS2#
M_A_DQS#3 68 DQS3#
M_A_DQS#4 129 DQS4#
M_A_DQS#5 146 DQS5#
M_A_DQS#6 167 DQS6#
M_A_DQS#7 186 DQS7#

M_A_DQS0 13 DQS0
M_A_DQS1 31 DQS1
M_A_DQS2 51 DQS2
M_A_DQS3 70 DQS3
M_A_DQS4 131 DQS4
M_A_DQS5 148 DQS5
M_A_DQS6 169 DQS6
M_A_DQS7 188 DQS7

9 M_ODT0 M_ODT0 114 OTD0
9 M_ODT1 M_ODT1 119 OTD1

1 VREF
2 VSS
202 GND
MH1
MH2

RAS# 108 M_A_RAS# 10
WE# 109 M_A_WE# 10
CAS# 113 M_A_CAS# 10
CS0# 110 M_CS0# 9
CS1# 115 M_CS1# 9
CKE0 79 M_CKE0 9
CKE1 80 M_CKE1 9
CK0 30 M_CLK_DDR0 M_CLK_DDR0 9
CK0# 32 M_CLK_DDR#0 M_CLK_DDR#0 9
CK1 164 M_CLK_DDR1 M_CLK_DDR1 9
CK1# 166 M_CLK_DDR#1 M_CLK_DDR#1 9

DM0 10 M_A_DM0
DM1 26 M_A_DM1
DM2 52 M_A_DM2
DM3 67 M_A_DM3
DM4 130 M_A_DM4
DM5 147 M_A_DM5
DM6 170 M_A_DM6
DM7 185 M_A_DM7

SDA 195 ICH_SMBDATA ICH_SMBDATA 4,15,18
SCL 197 ICH_SMBCLK ICH_SMBCLK 4,15,18
VDDSPD 199 +3.3V_RUN
SA0 198 R55 1 10KR2J-3-GP
SA1 200 R56 1 10KR2J-3-GP
NC#50 50 PM_EXTTS#0 9
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163

+1.8V_SUS
VDD 81 82 87 88 95 96 103 104 111 112 117 118

VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196 GND 201

MH2

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C72 DUMMY-C2
C74 DUMMY-C2
C192 DUMMY-C2
C195 DUMMY-C2

+3.3V_RUN
C54 SCD1U16V2KX-3GP
C53 SC22U10V3KX-1GP

Layout Note:
Place near DM1

+1.8V_SUS
C132 SC22D2U10V3KX-1GP
C122 SC22D2U10V3KX-1GP
C60 SC22D2U10V3KX-1GP
C138 SC22D2U10V3KX-1GP
C116 SC22D2U10V3KX-1GP
C93 SCD1U16V2KX-3GP
C109 SCD1U16V2KX-3GP
C100 SCD1U16V2KX-3GP
C106 SCD1U16V2KX-3GP
C8 ST220U2D5VBM-LGP

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.

+0.9V_DDR_VTT
C101 C409 C103 C96 C83 C432 C87 C114 C118 C119 C115 C428 C420
SCD1U16V2KX-3GP

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".

+0.9V_DDR_VTT
RN37 M_A_A9 M_A_A12
RN6 M_A_A13
RN31 M_A_A10 M_A_BS#0
RN35 M_A_A5 M_A_A8
RN4 M_ODT0 M_CS0#
RN10 M_A_A6 M_A_A2
RN12 M_CKE1 M_A_A14
RN33 M_A_A1 M_A_A3
RN29 M_A_WE# M_A_CAS#
RN39 M_CKE0 M_A_BS#2
RN28 M_CS1# M_ODT1
RN8 M_A_BS#1 M_A_RAS#
RN11 M_A_A11 M_A_A7
RN17 M_A_A0 M_A_A4
SRN56J-4-GP

+V_DDR_MCH_REF
C203 SCD1U16V2KX-3GP
C202 SC2D2U10V3KX-1GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1
Size: Custom
Document Number: Roberts
Rev: A00
Date: Thursday, October 02, 2008
Sheet 14 of 58

SSID = MEMORY

10 M_B_DQS#[7..0]
10 M_B_DQ[63..0]
10 M_B_DM[7..0]
10 M_B_DQS[7..0]
10 M_B_A[14..0]

DM1

MH1 MH2

M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14
M_B_BS#2
M_B_BS#0 M_B_BS#1

M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#

M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7

CK0 CK0# CK1 CK1#

M_CLK_DDR2 M_CLK_DDR#2 M_CLK_DDR3 M_CLK_DDR#3

M_CLK_DDR2 9
M_CLK_DDR#2 9
M_CLK_DDR3 9
M_CLK_DDR#3 9

SA0 SA1

R57 10KR2J-3-GP
R54 10KR2J-3-GP

+3.3V_RUN

VDD_SPD +3.3V_RUN

EC12 SCD1U25V3KX-GP

+1.8V_SUS

VDD ×24

VSS ×144

PM_EXTTS#1 → NC#50
NC#69
NC#83
NC#120
NC#163/TEST

M_CS2# M_CS3# M_CKE2 M_CKE3 M_B_RAS# M_B_CAS# M_B_WE#

CS0# CS1# CKE0 CKE1 RAS# CAS# WE#

4,14,18 ICH_SMBCLK → ICH_SMBCLK → SCL
4,14,18 ICH_SMBDATA → ICH_SMBDATA → SDA

M_ODT2 M_ODT3 → ODT0 ODT1

+V_DDR_MCH_REF → VREF

GND ×2

SLT_SODIMM200-3&GP
200.7.E31

put near connector

M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3

C71 DUMMY-C2
C75 DUMMY-C2
C193 DUMMY-C2
C197 DUMMY-C2

+3.3V_RUN

C52 SCD1U16V2KX-3GP
C56 SC2D2U10V3KX-1GP

Layout Note:
Place near DM2

+1.8V_SUS

C136 SC2D2U10V3KX-1GP
C97 SC2D2U10V3KX-1GP
C107 SC2D2U10V3KX-1GP
C112 SC2D2U10V3KX-1GP
C105 SC2D2U10V3KX-1GP
C124 SCD1U16V2KX-3GP
C150 SCD1U16V2KX-3GP
C104 SCD1U16V2KX-3GP
C131 SCD1U16V2KX-3GP
C4 ST220U2D5VBM-LGP

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.

+0.9V_DDR_VTT

C430 C415 C425 C418 C414 C406 C405 C95 C410 C417 C88 C404 C102
SCD1U16V2KX-3GP / SCD1U16V2KX-3GP / SCD1U16V2KX-3GP

Layout Note:
Place these resistors close to DM2,
all trace length Max=1.5".

+0.9V_DDR_VTT

RN7 M_B_WE# M_B_CAS# → M_ODT2 M_B_A13
RN27
RN13 M_B_BS#2 M_CKE2 → M_B_A14 M_B_A11
RN38
RN16 M_B_A5 M_B_A8 → M_B_A7 M_B_A6
RN36
RN32 M_B_BS#1 M_B_A0 → M_B_A4 M_B_A2
RN34
RN15 M_B_A1 M_B_A3 → M_B_A10 M_B_BS#0
RN9
RN5 M_ODT3 M_CS3# → M_B_RAS# M_CS2#
RN30
RN40 M_CKE3 → M_B_A12 M_B_A9
RN14

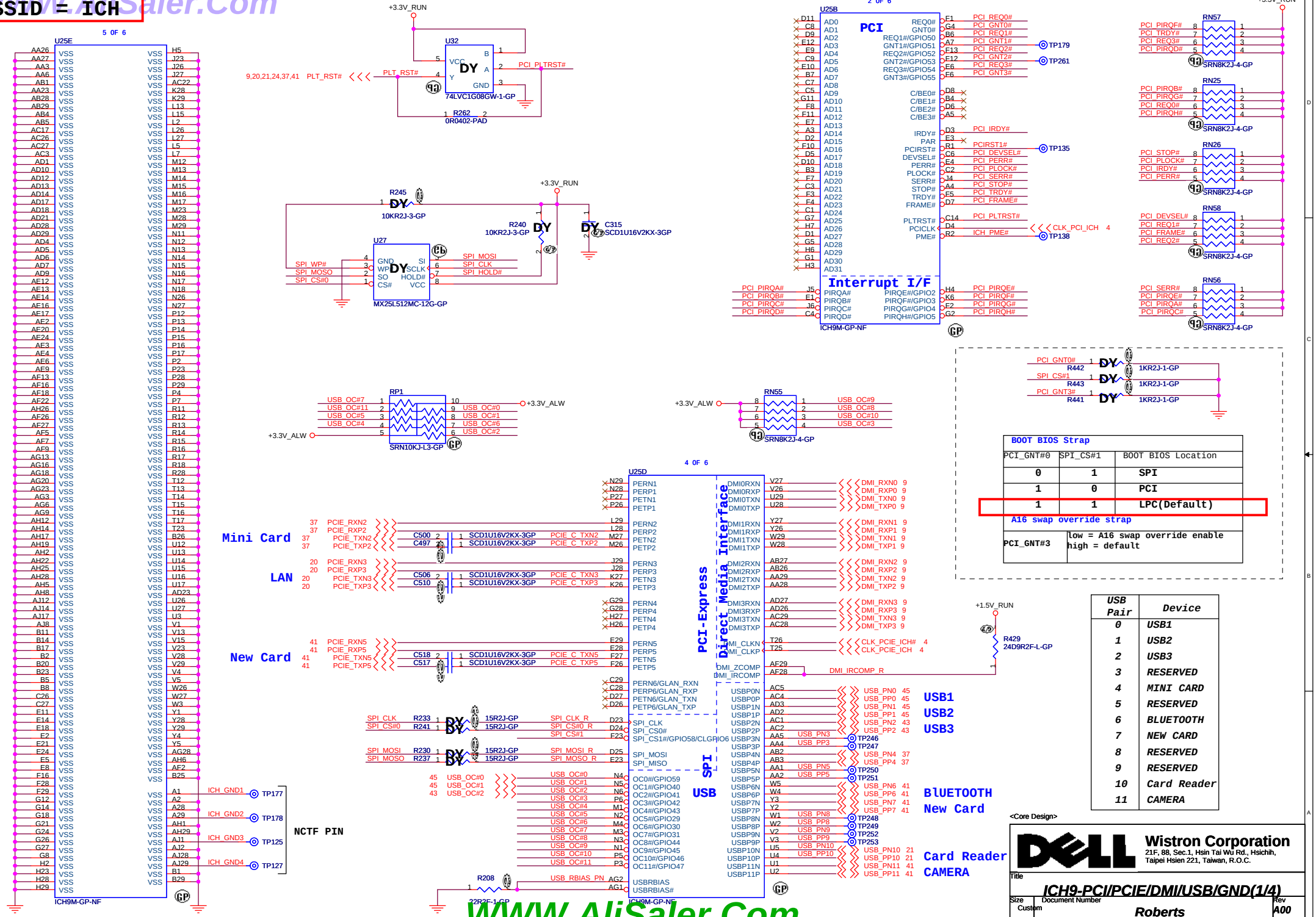
SRN56J-4-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2
Size: Custom | Document Number: Roberts | Rev: A00
Date: Thursday, October 02, 2008 | Sheet 15 of 58

SSID = ICH



BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

<Core Design>

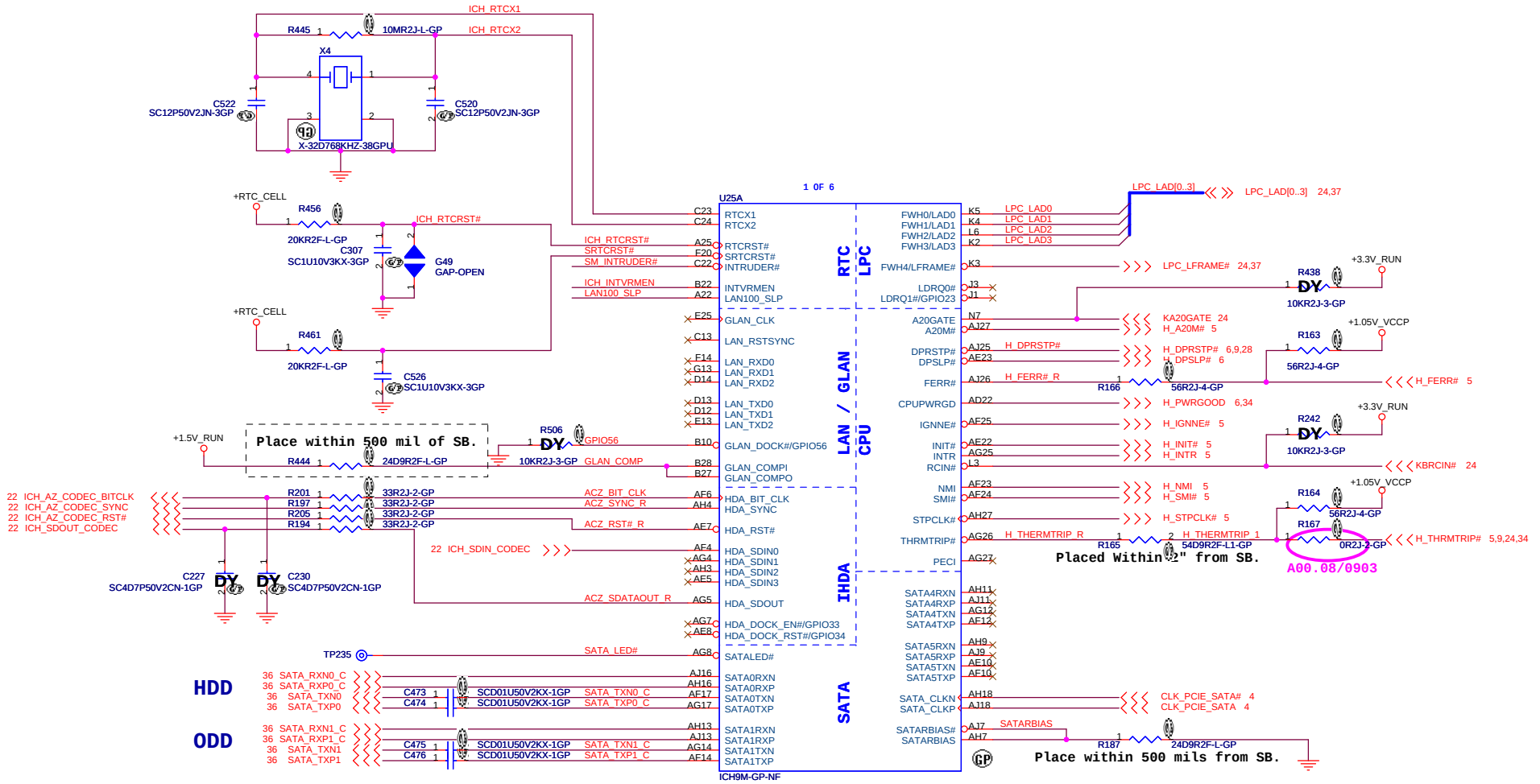
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

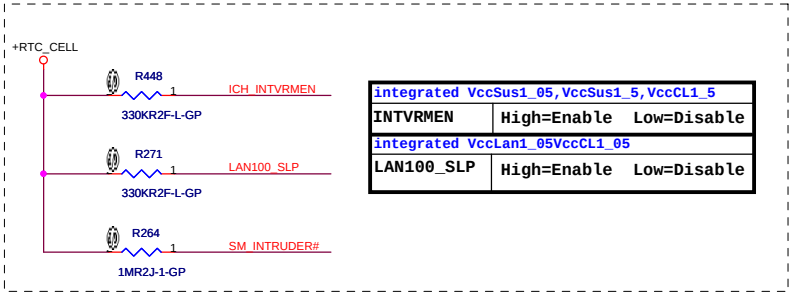
Title: ICH9-PCI/PCIE/DMI/USB/GND(1/4)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 16 of 58

SSID = ICH





integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

<Core Design>

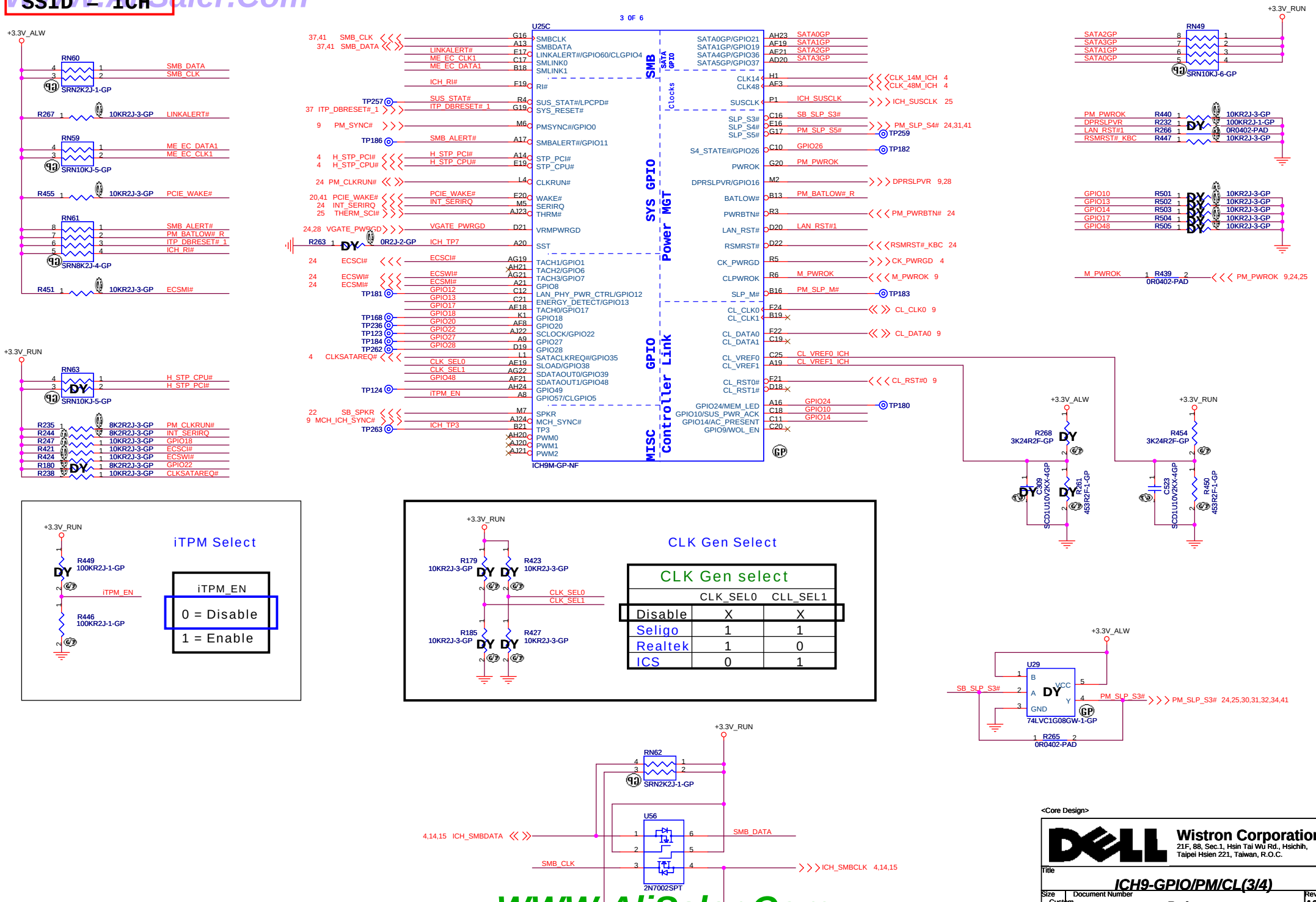
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(2/4)

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 17 of 58

SSID = ICH



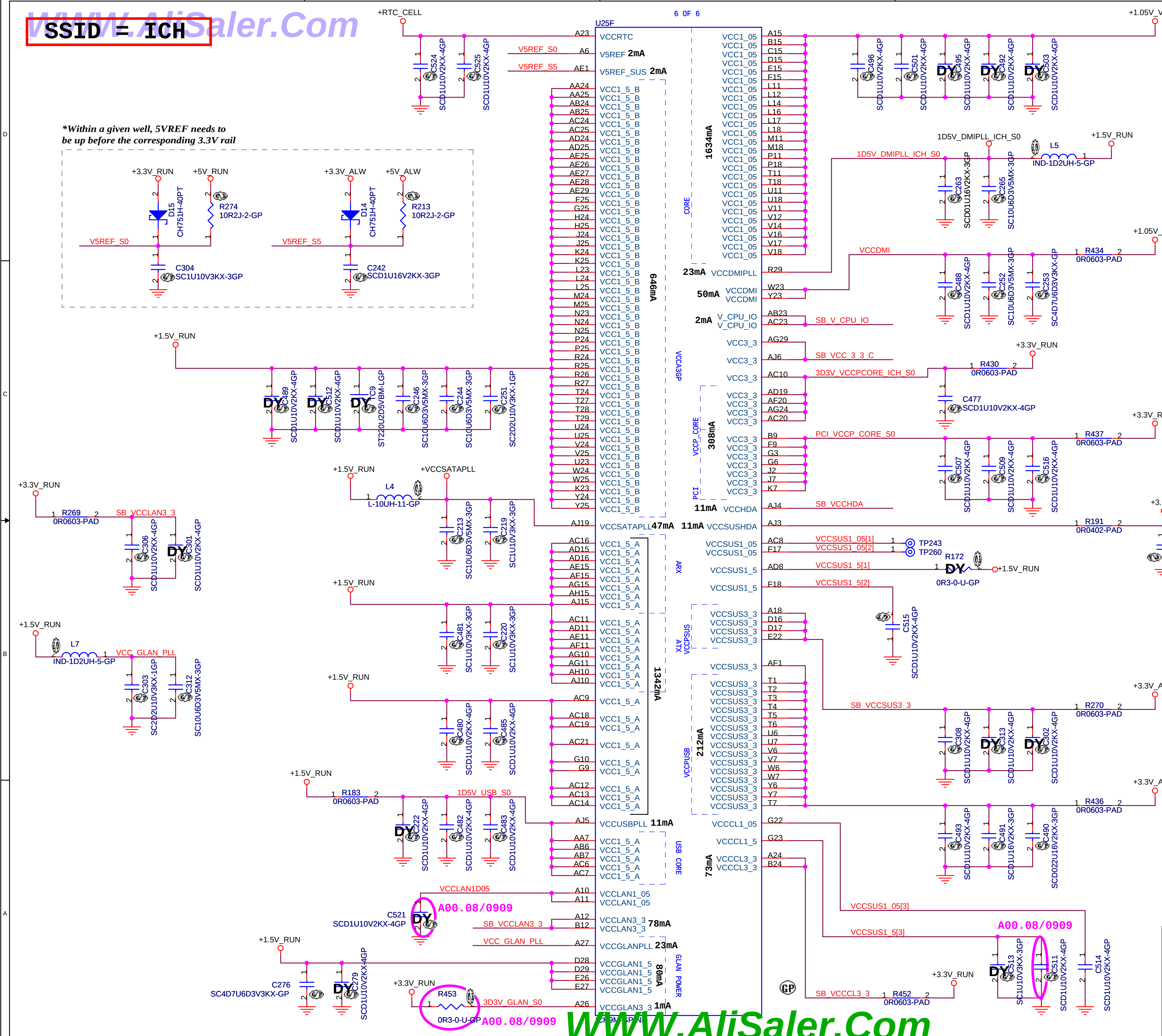
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-GPIO/PM/CL(3/4)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 18 of 58

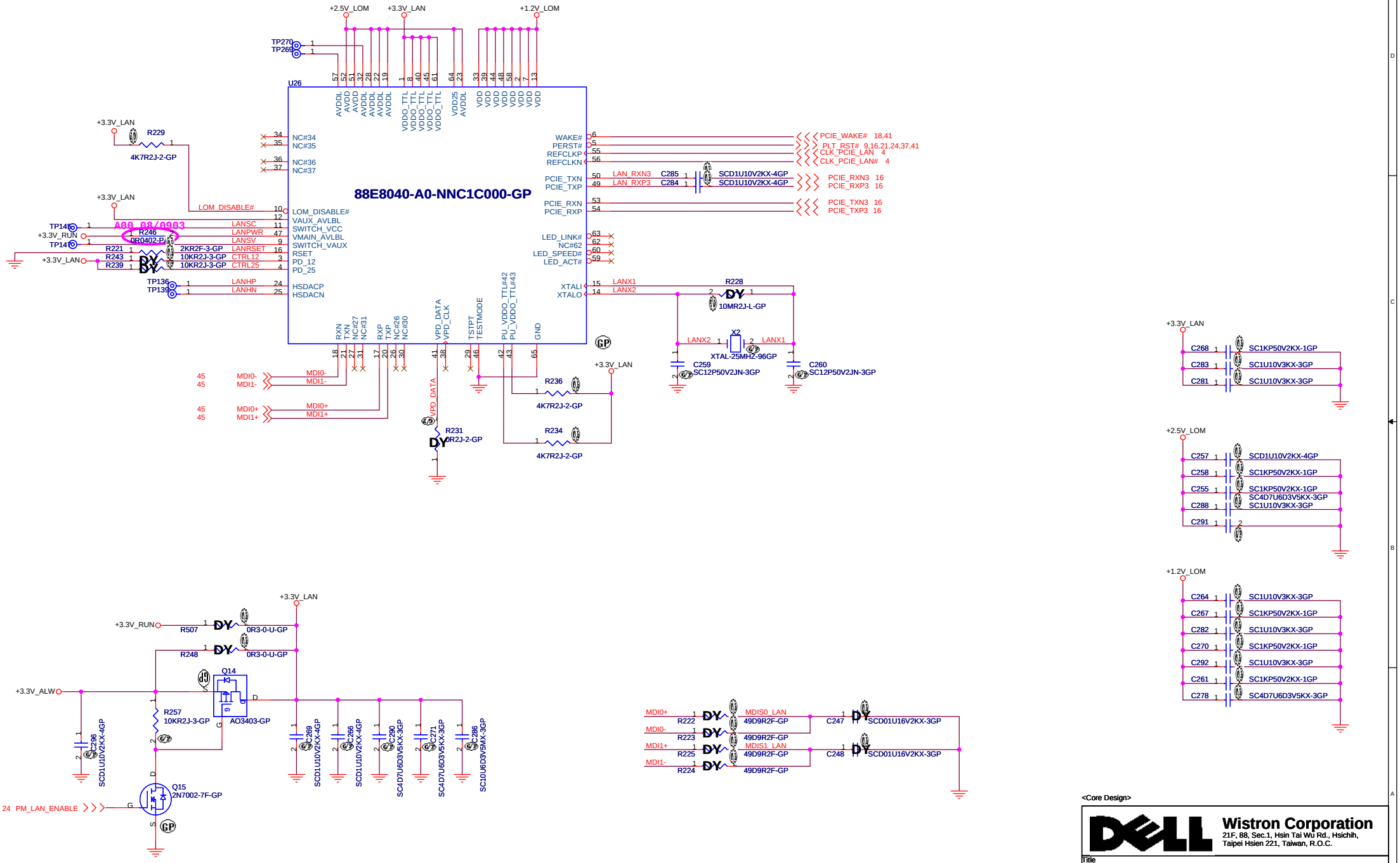


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH9-POWER(4/4)	
Size: Custom	Document Number: Roberts	Rev: A00
Date: Thursday, September 11, 2008	Sheet 19 of 58	

SSID = LOM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Marvell-88E8040

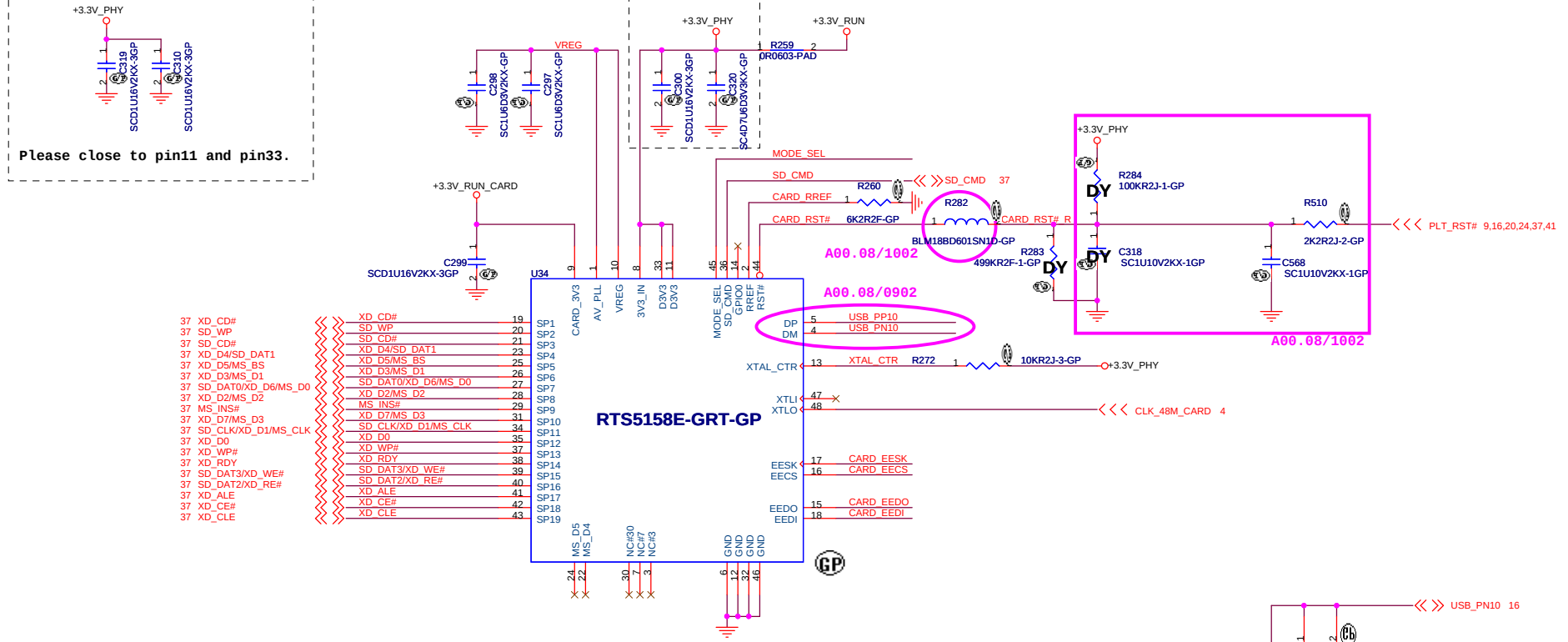
Size: Custom | Document Number: Roberts | Rev: A00

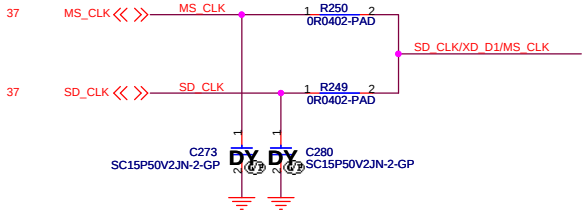
Date: Thursday, October 02, 2008 | Sheet 20 of 58

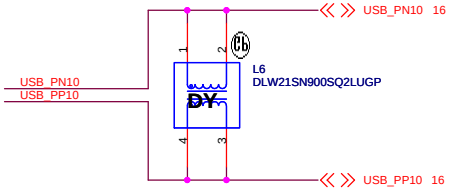
SSID = SDIO

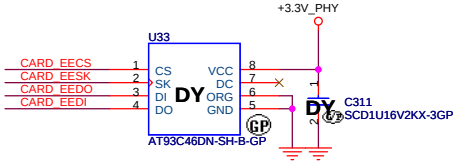
Please close to pin8.

Please close to pin11 and pin33.





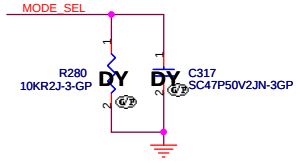




Reserve for changing USB VID/PID.

Power mode select

No staff R and C for power saving mode.



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5158E

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 21 of 58

SSID = AUDIO

Place C914 close to pin1
Place C915 close to pin9

+3.3V_RUN
C537 SCD1U10V2KX-4GP
C530 SC1U6D3V2KX-GP
C533 SCD1U10V2KX-4GP

+3.3V_RUN
R467 0R0402-PAD
C529 SCD1U10V2KX-4GP

U61
92HD71B7A5NLGXB3X8-GP

DVDD_CORE
DVDD_CORE
NC#40/OTP
DVDD_IO
BITCLK
SDI_CODEC
SDO
SYNC
RESET#
DMIC_CLK
VOL_UP/DMIC_0/GPIO1
VOL_DN/DMIC_1/GPIO2
EAPD/GPIO0/SPDIF_OUT0OR1
SPDIF_OUT0
GPIO5
GPIO6
GPIO7/SPDIF_OUT1
DVSS
GND

AVDD1
AVDD2
SENSE_A
SENSE_B/NC#34
PORTA_L
PORTA_R
NC#37
PORTB_L
PORTB_R
VREFOUT_B
PORTC_L
PORTC_R
VREFOUT_C
PORTD_L
PORTD_R
PORTE_L
PORTE_R
VREFOUT_E/GPIO4
PORTF_L
PORTF_R
GPIO3
NC#18
NC#19
NC#20
PCBEEP
MONO_OUT
CAP2
VREFFILT
AVSS1
AVSS2

+VDDA
C550 SCD1U10V2KX-4GP
C555 SC1U10V3KX-3GP

+VDDA
R487 20KR2F-L-GP

+VDDA
R479 5K1R2F-2-GP

R473 39K2R2F-L-GP → AUD_HP1_JD# 23,40
R478 20KR2F-L-GP → EXT_MIC_JD# 40
C541 SC1KP50V2KX-1GP

17 ICH_AZ_CODEC_BITCLK → R463 22R2J-2-GP → ICH_AZ_CODEC_BITCLK_R
17 ICH_SDIN_CODEC → R465 33R2J-2-GP → SB_AZ_CODEC_SDIN0_R
17 ICH_SDOUT_CODEC
17 ICH_AZ_CODEC_SYNC
17 ICH_AZ_CODEC_RST#
DY C532 SC4D7P50V2CN-1GP

41 AUD_DMIC_IN0 → AUD_DMIC_CLK / AUD_DMIC_IN0

SENSE_A ← AUD_SENSE_A
SENSE_B/NC#34 ← AUD_SENSE_B

PORTA_L / PORTA_R ← AUD_HP1_OUT_L / AUD_HP1_OUT_R
→ AUD_HP1_OUT_L 23
→ AUD_HP1_OUT_R 23

PORTB_L / PORTB_R / VREFOUT_B ← AUD_EXT_MIC_L / AUD_EXT_MIC_R / AUD_VREFOUT_B
→ AUD_EXT_MIC_L 40
→ AUD_EXT_MIC_R 40
→ AUD_VREFOUT_B 40

PORTC_L / PORTC_R / VREFOUT_C ← AUD_INT_MIC_L / AUD_INT_MIC_R / AUD_VREFOUT_C
C547 SC1U10V3KX-3GP
C549 SC1U10V3KX-3GP
R292 4K7R2J-2-GP
→ INT_MIC_L_R 40

PORTD_L / PORTD_R ← AUD_LINE_OUT_L / AUD_LINE_OUT_R
C560 SC1U6D3V2KX-GP
→ AUD_LINE_OUT_L 23
→ AUD_LINE_OUT_R 23

Port A---> HP
Port B---> Ext Mic
Port C---> Int Mic
Port D---> Speaker

AUD_PC_BEEP
Trace width>15 mils
PC BEEP

PCBEEP ← AUD_PC_BEEP
C531 SCD1U10V2KX-4GP
SB_SPKR_R
R464 499KR2F-1-GP
From SB
SB_SPKR 18

CAP2 / VREFFILT ← AUD_CAP2 / AUD_VREFFLT
C558 SC10U6D3V5MX-3GP
C561 SC10U6D3V5MX-3GP
R468 DUMMY-C2

Azalia I/F EMI
ICH_SDOUT_CODEC
R466 47R2J-2-GP
ICH_AZ_CODEC_SDOUT1
DY C528 SCD1U10V2KX-4GP

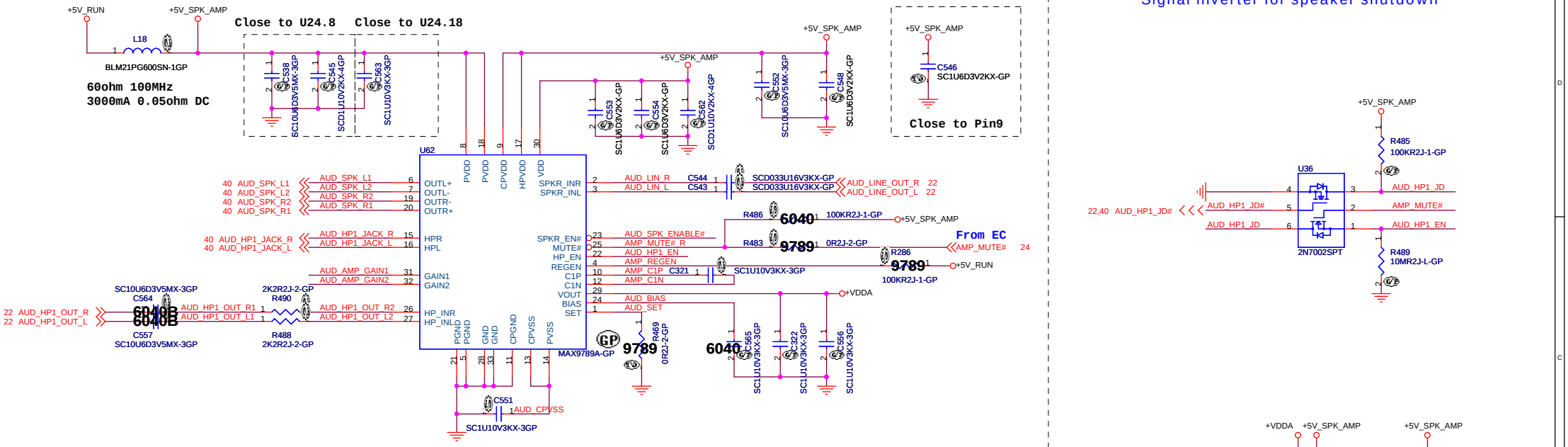
+3.3V_RUN
U59 74LVC1G125DC-GP
41 AUD_DMIC_CLK_G
EC154 SC22P50V2JN-4GP
R477 22R2J-2-GP
AUD_DMIC_CLK

<Core Design>

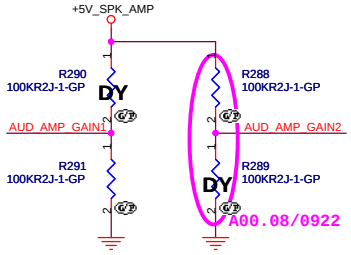
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC 92HD71B7
Size: Custom | Document Number: Roberts | Rev: A00
Date: Thursday, October 02, 2008 | Sheet 22 of 58

SSID = AUDIO



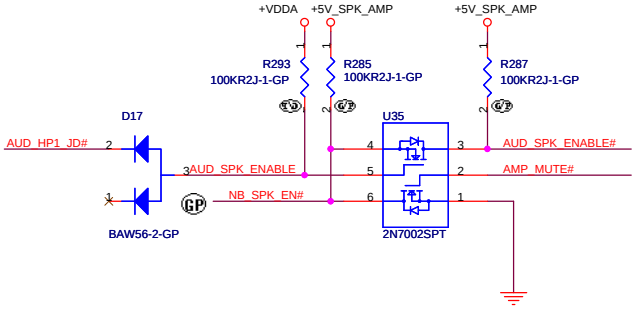
GAIN SETTING

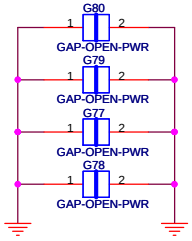


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

	Main source	Second source
	TPA6040A (74.06040.013)	MAX9789A (74.09789.013)
R486	100K	No ASM
R483	No ASM	0 Ohm
R469	No ASM	0 Ohm
R286	No ASM	100K
C535	0.033uF	No ASM
C566	0.033uF	No ASM
C565	1uF	No ASM
C567	No ASM	0.1uF
C564	10uF	2.2uF
C557	10uF	2.2uF

Signal inverter for speaker shutdown





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 23 of 58

CAP close to VCC-GND pin pair

SSID = KBC

MB VERSION ID

MB VERSION ID	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
-1	0	1	1

KBC CLK EMI

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Winbond WPC773L

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 24 of 58

SSID = Thermal

+5V_RUN
C386 SC4D7U6D3V5KX-3GP
C389 SCD1U16V2KX-3GP
+3.3V_RUN
R63 10KR2J-3-GP
R66 DY 0R2J-2-GP
+5V_RUN
R348 DY 10KR2J-3-GP
EMC2102_FAN_TACH
D6 RB551V30-GP
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH_1 36
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE 36
+3.3V_RTC_LDO
R346 DY 49D9R2F-GP
RN3 SRN4K7J-8-GP
+3.3V_RUN
THERM_SCL 24
THERM_SDA 24
+3.3V_RUN
R340 49D9R2F-GP
EMC2102_VDD_3D3
C60 SCD1U16V2KX-3GP

1.For CPU Sensor

5 H_THERMDC
C50 SC470P50V3JN-2GP
5 H_THERMDA
Layout notice : Both H_THERMDA and THERMDC routing 10 mil trace width and 10 mil spacing.
Layout notice : Both DN2 and DP2 routing 10 mil trace width and 10 mil spacing.

U8 EMC2102

Pin	Name
1	VDD_3V
2	DN1
3	DP1
4	DN2
5	DP2
6	DN3
7	DP3
8	NC#8
9	SHDN_SEL
10	FAN_MODE
11	TRIP_SET
12	SYS_SHDN#
13	THERMTRIP#
14	POWER_OK#
15	NC#15
16	EM2102_RESET#
17	EMC2102_CLK_SEL
18	CLK_32K
19	ALERT#
20	GND
21	NC#21
22	SMDATA
23	SMCLK
24	VDD_5Vb
25	FANb
26	FANa
27	VDD_5Va
28	TACH
29	GND

EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
EMC2102-DZK-GP

+3.3V_RUN
R89 8K2R2J-3-GP
THERM_SCI# 18
R87 DY 0R2J-2-GP
R88 10KR2J-3-GP

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

C388 must be near Q18
Q18 MMBT3904-3-GP
C388 DY SC470P50V3JN-2GP
C61 SC470P50V3JN-2GP
C61 must be near EMC2102

2.System Sensor, Put between CPU and NB.

C37 must be near Q1
Q1 MMBT3904-3-GP
C37 DY SC470P50V3JN-2GP
C63 SC470P50V3JN-2GP
C63 must be near EMC2102

3.HW T8 sensor

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

R85 10KR2J-3-GP
R84 10KR2J-3-GP
+3.3V_RUN
R67 DY 10KR2J-3-GP
EMC2102_SHDN
+3.3V_RUN
R68 DY 10KR2J-3-GP
EMC2102_FAN_mode
R71 10KR2J-3-GP

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

+3.3V_RUN
R362 10KR2J-3-GP
+3.3V_RTC_LDO
R347 10KR2J-3-GP
Q17 2N7002-7F-GP
PURE_HW_SHUTDOWN# 24,34
V_DEGREE

+3.3V_RUN
A00.08/0922
C78 SCD1U16V2KX-3GP
R82 10KR2F-2-GP
C70 SCD1U16V2KX-3GP
R78 2K37R2F-GP

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)

T8 shutdown is set 88 deg-C.

TP223 EMC2102_FAN_TACH_1
TP72 EMC2102_FAN_DRIVE

32K suspend clock output

18 ICH_SUSCLK
Q13 2N7002-7F-GP
CLK_32K_R
R219 10R2J-2-GP
CLK_32K
C249 DY SC4D7P50V2CN-1GP
RUN_POWER_ON

EM2102_RESET#
18,24,30,31,32,34,41 PM_SLP_S3#
U10 74LVC1G08GW-1-GP
+3.3V_ALW
C82 DY SCD1U16V2KX-3GP
PM_PWROK 9,18,24

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: Custom | Document Number: Roberts | Rev: A00
Date: Thursday, October 02, 2008 | Sheet 25 of 58

SSID = Charger

Adaptor In Soft-Start Circuit

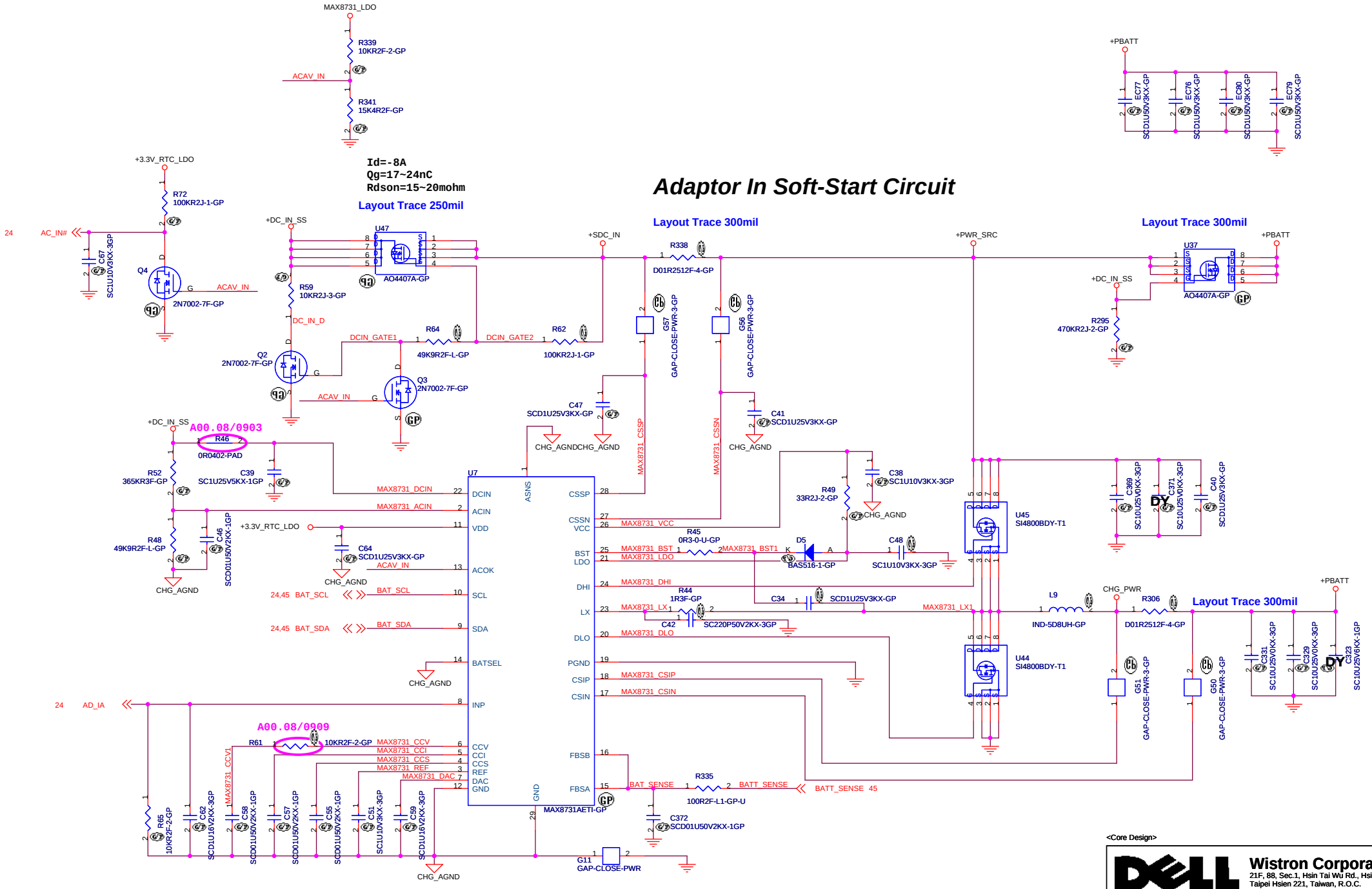
Id=-8A
Qg=17~24nC
Rdson=15~20mohm

Layout Trace 250mil

Layout Trace 300mil

Layout Trace 300mil

Layout Trace 300mil



<Core Design>

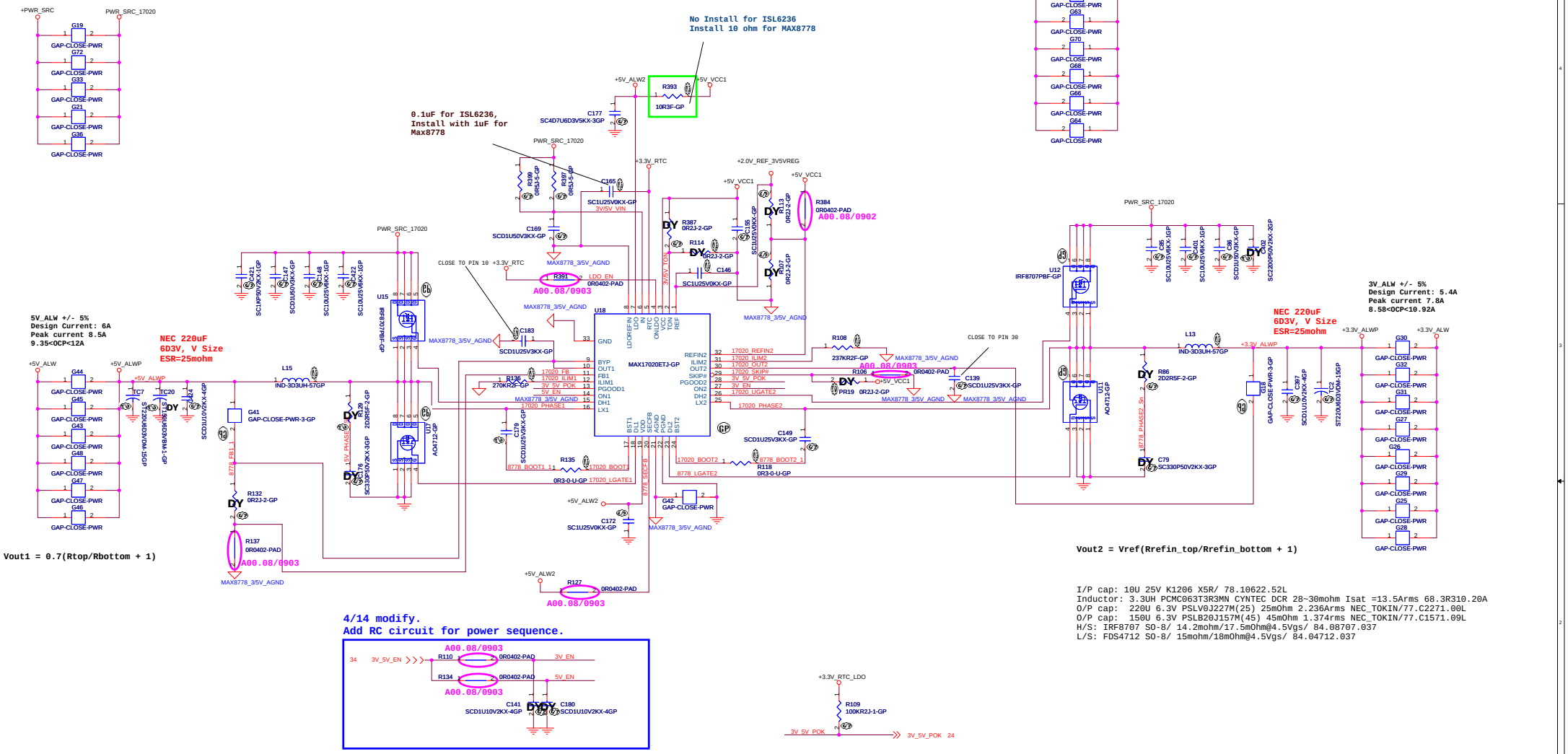
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 26 of 58

SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

SKIPSEL	GND	Open/REF (2V)	High (VCC or 3.3V)
Operating Mode	pulse-skipping mode	ultrasonic mode	forced-PWM operation

TONSEL	GND	Open (REF)	High (VCC)
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

LDOREFIN	GND	VCC	VLDOREFIN = 0.5V
Operating Mode	4.90/5.0/5.10	3.23/3.3/3.37	0.96/1.0/1.04

FB1	GND	VCC	
Operating Mode	4.925/5.00/5.075	1.482/1.50/1.518	

REFIN2	5V	RTC (3.3V)	
Operating Mode	3.255/3.30/3.345	1.038/1.050 /1.062	

<Core Design>

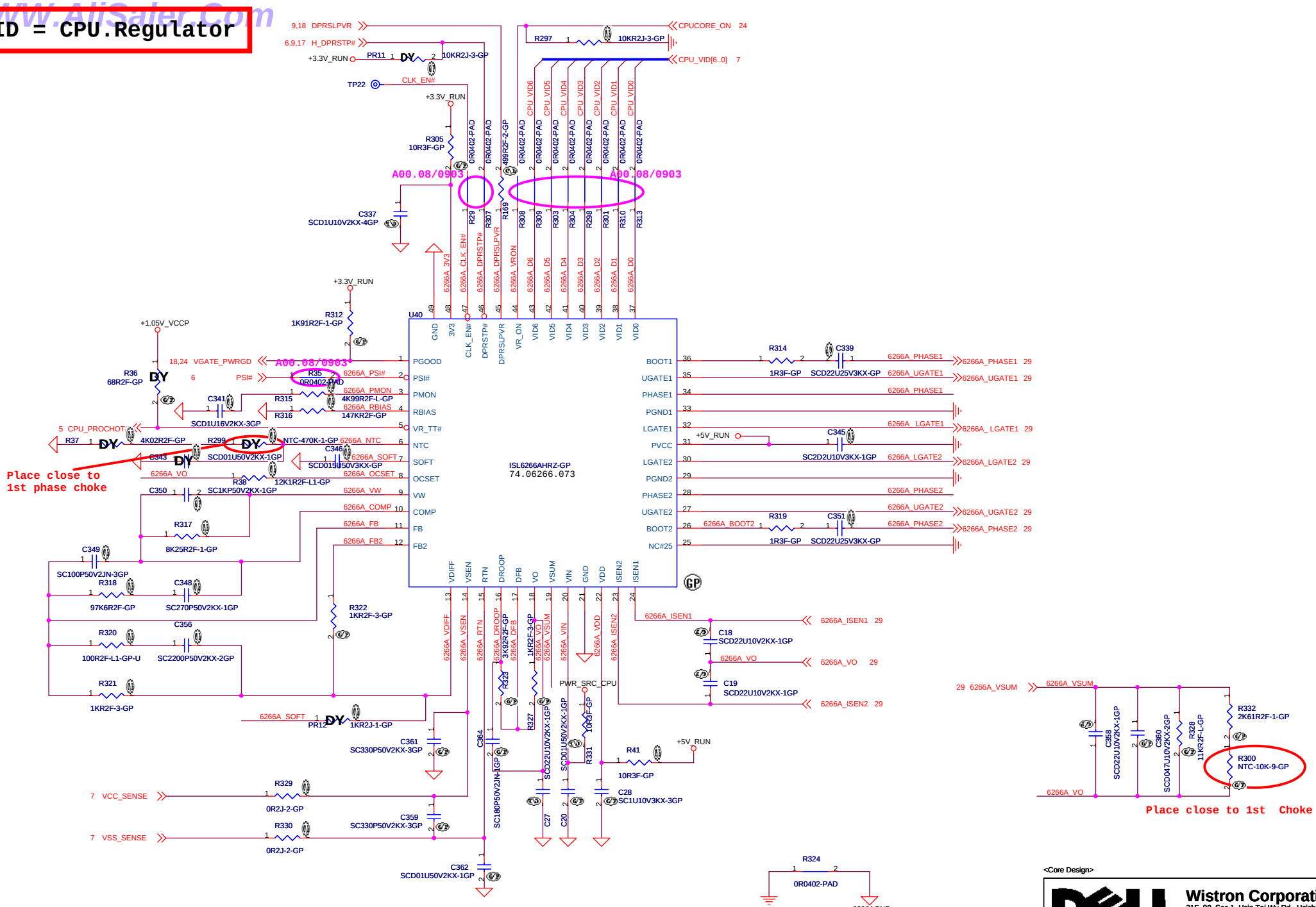
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V/5V

Size	Document Number	Rev
A2	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 27 of 58

SSID = CPU.Regulator



<Core Design>

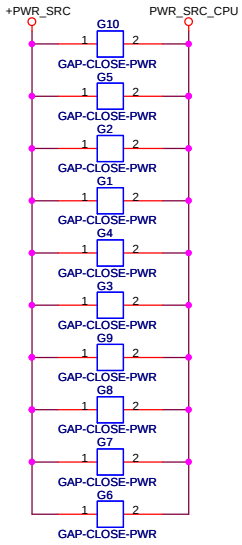
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

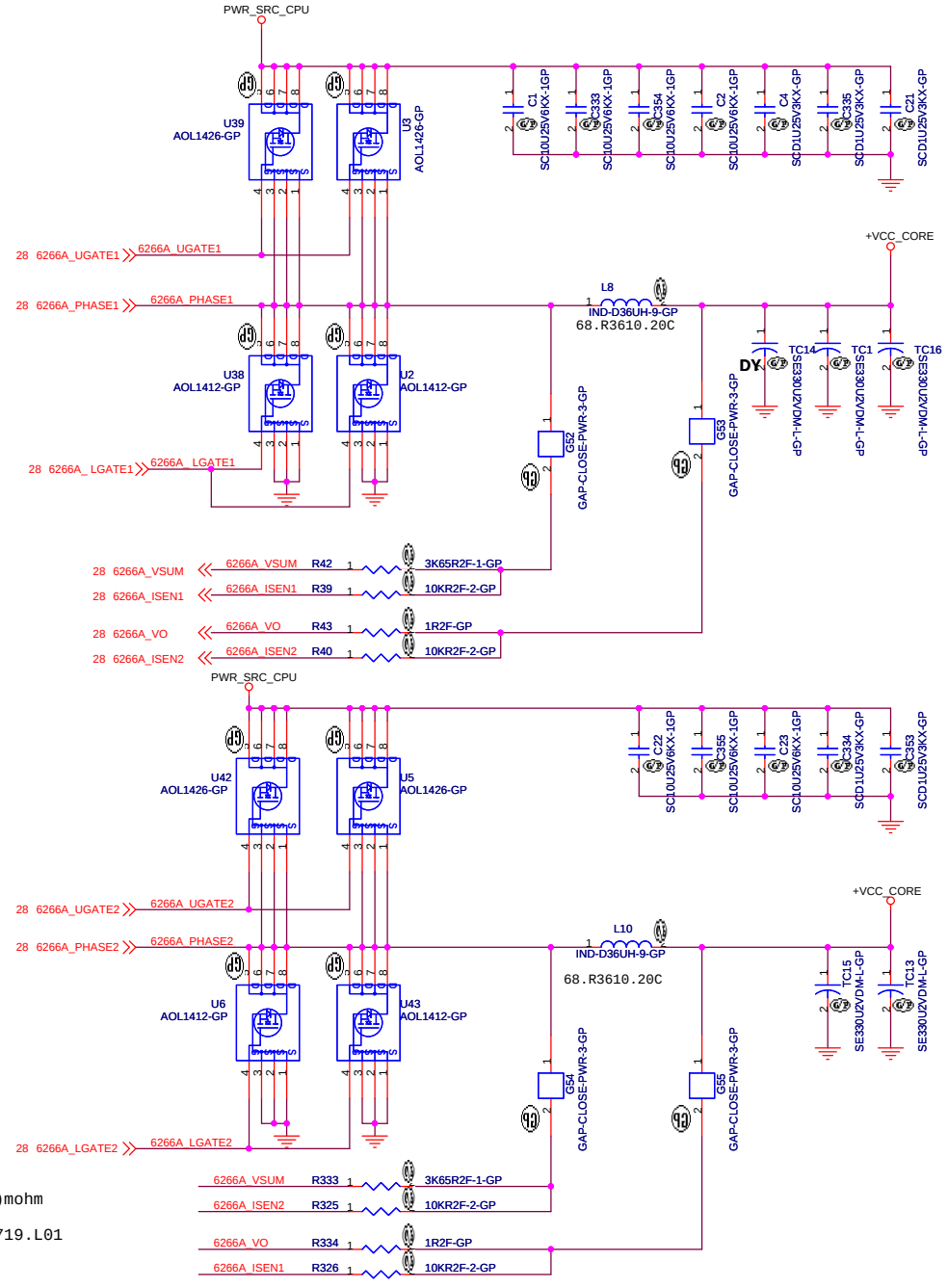
Title: CPU VCORE POWER(1/2)

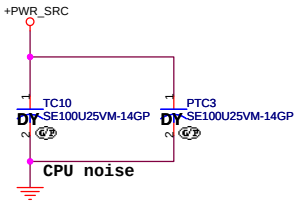
Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 28 of 58

SSID = CPU.Regulator







I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037

<Core Design>

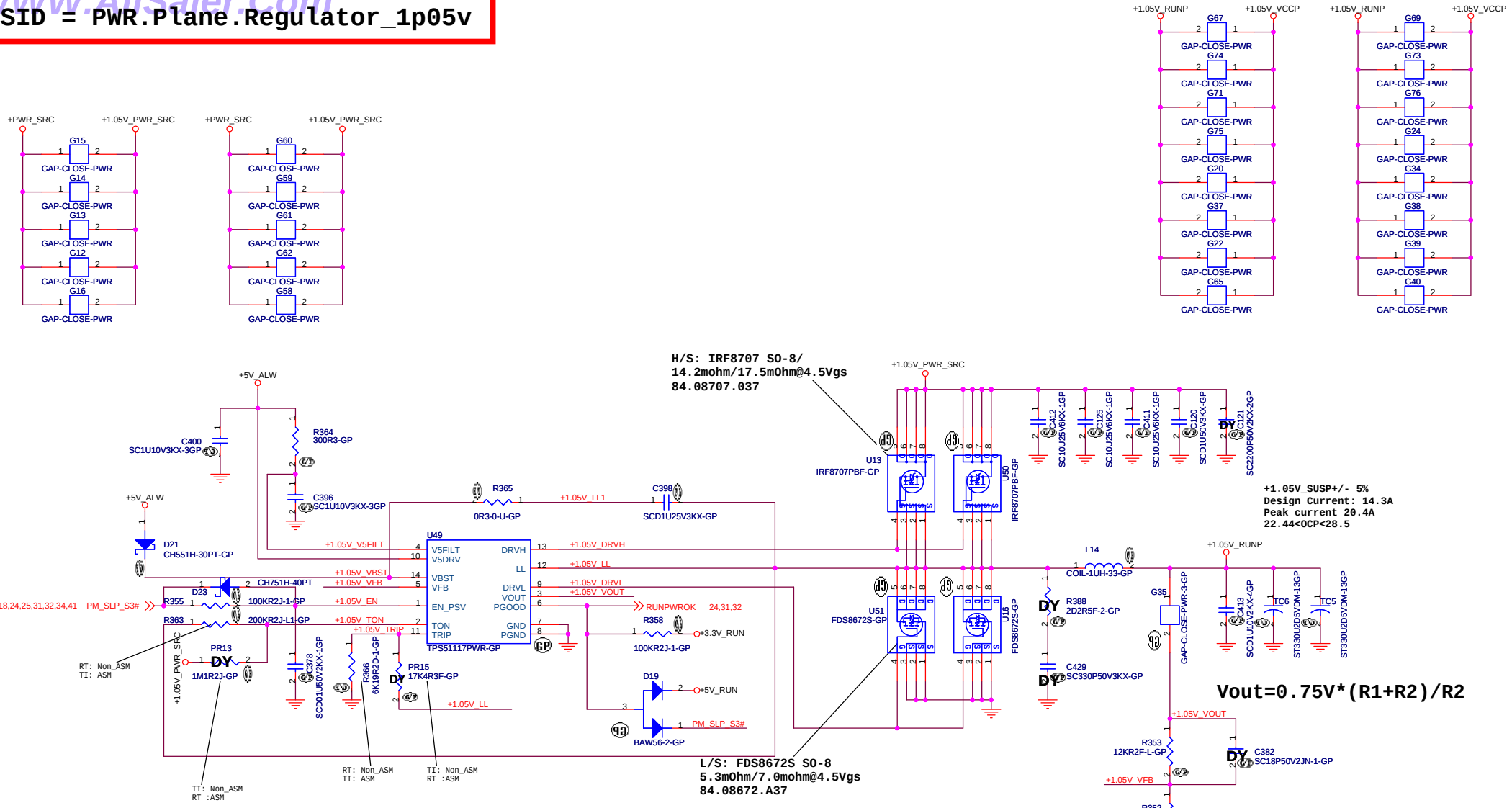
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 29 of 58

SSID = PWR.Plane.Regulator_1p05v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC104T1R0MN Cyntec DCR:3.0 ~3.5mohm Isat =40Arms 68.1R01A.20A
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: IRF8707 SO-8/14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->350KHz

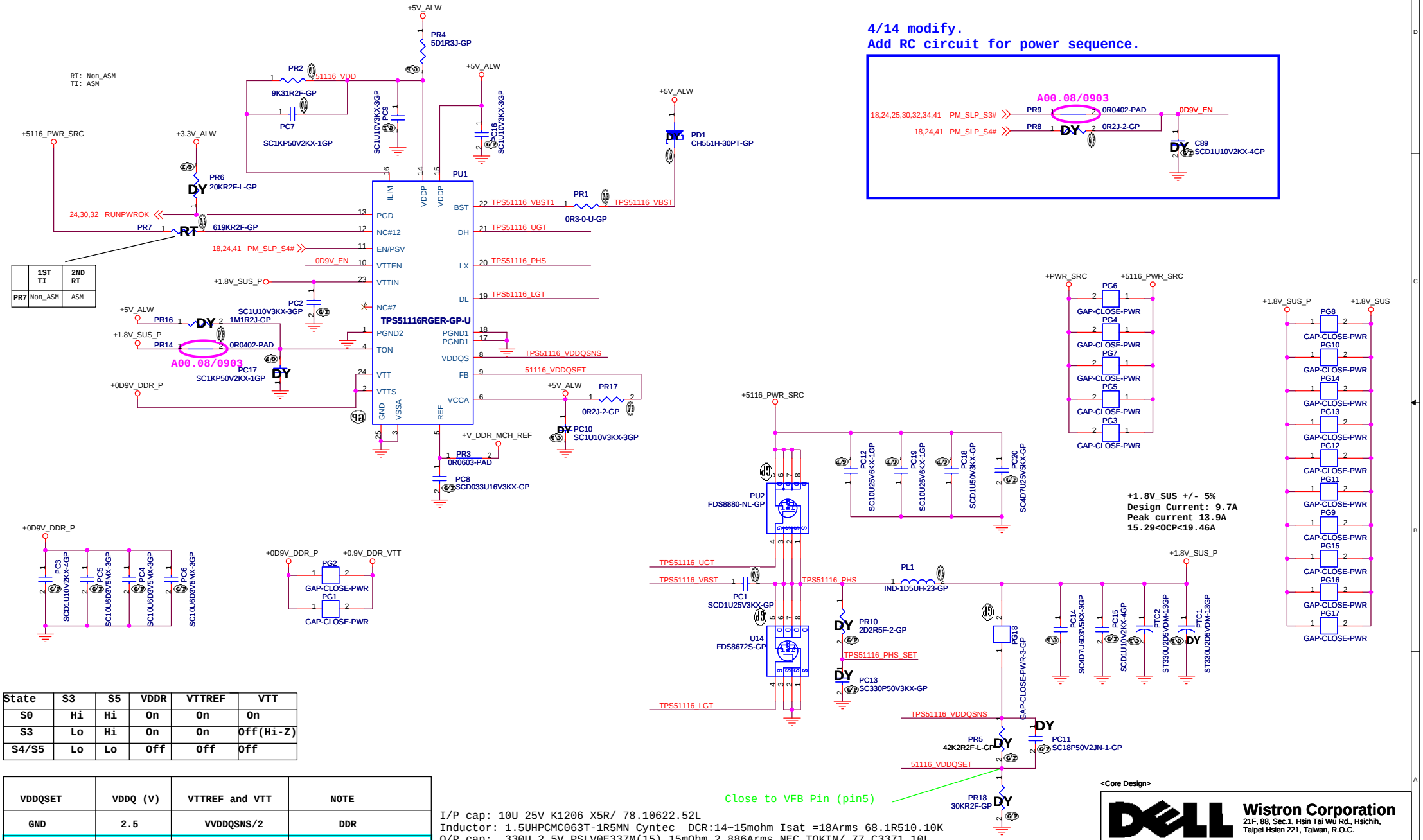
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 1.05V	
Size: Custom	Document Number: Roberts	Rev: A00
Date: Thursday, October 02, 2008	Sheet 30 of 58	

SSID = PWR.Plane.Regulator_1p8v0p9v

TI TPS51116 for 1.8V and 0.9V



	1ST TI	2ND RT
PR7	Non_ASM	ASM

RT: Non_ASM
TI: ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC063T-1R5MN Cyntec DCR:14~15mohm Isat =18Arms 68.1R510.10K
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq ->400KHz

<Core Design>

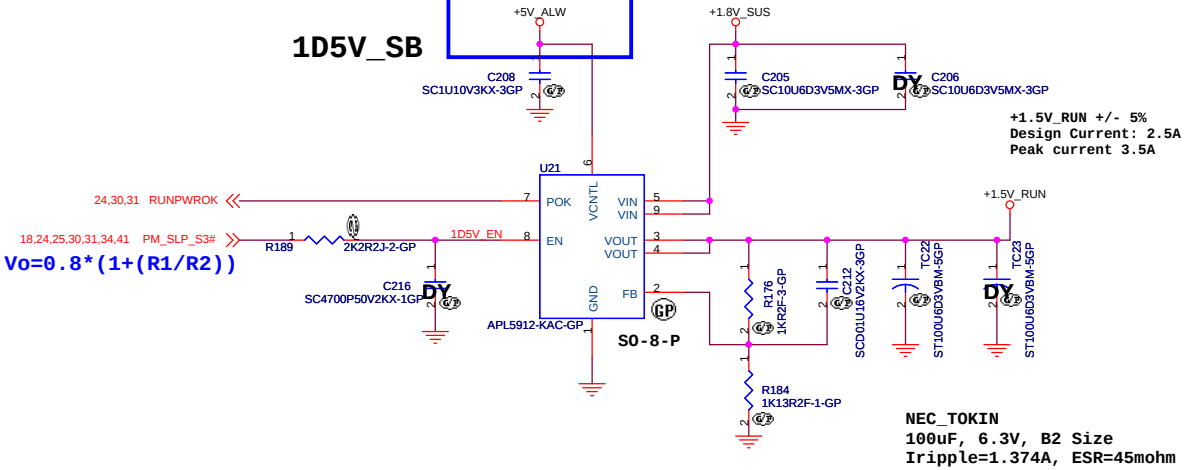
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.8V/0.9V
Size: Custom | Document Number: Roberts | Rev: A00
Date: Thursday, October 02, 2008 | Sheet 31 of 58

SSID = PWR.Plane.Regulator_1p5v

Change from +5V_RUN to +5V_ALW,
please confrim it is okay.

1D5V_SB



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.5V

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 32 of 58

(Blanking)

<Core Design>

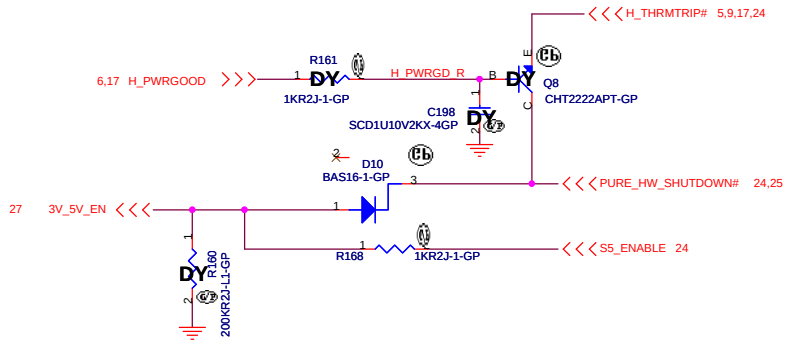
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA Power

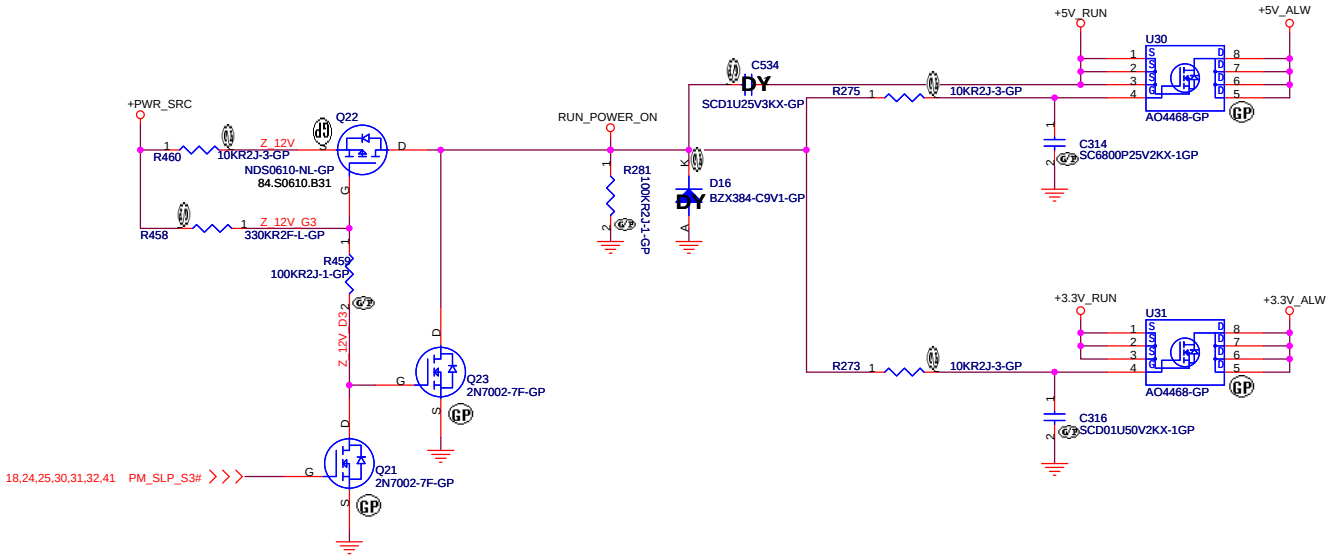
Size: Custom | Document Number: Roberts | Rev: A00

Date: Tuesday, September 09, 2008 | Sheet 33 of 58

SSID = Reset.Suspend



Run Power



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

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Custom	Roberts	A00

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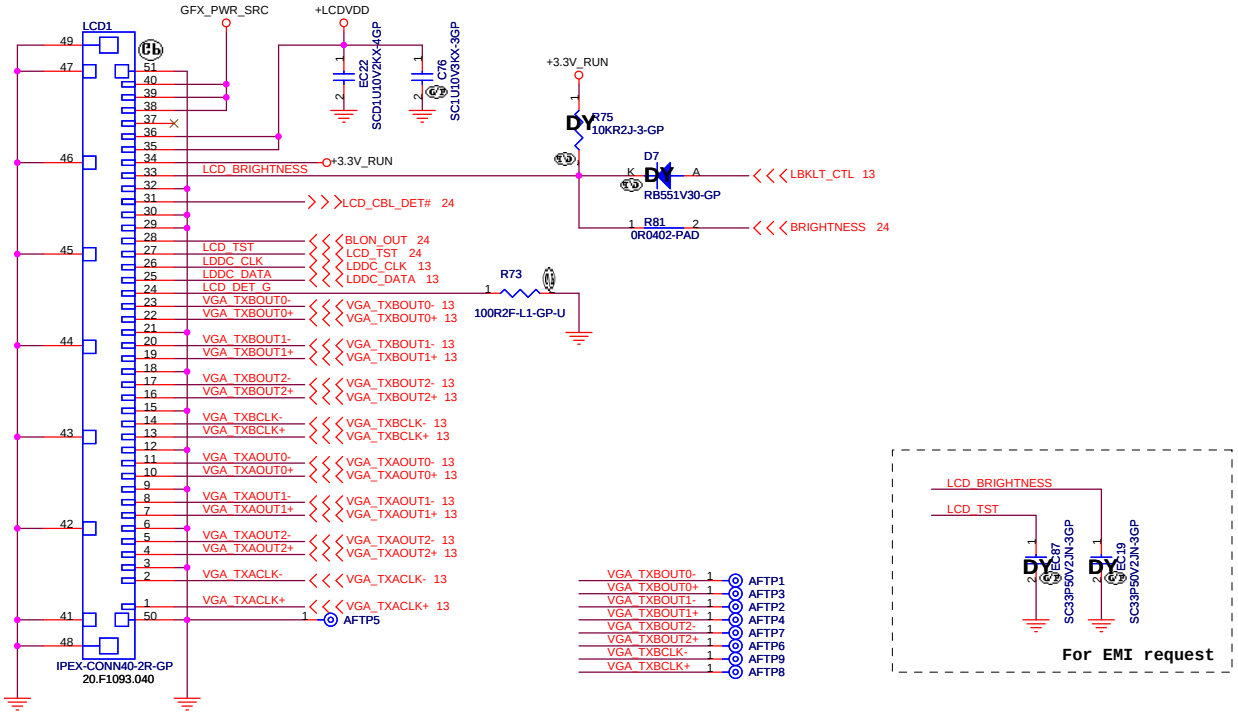
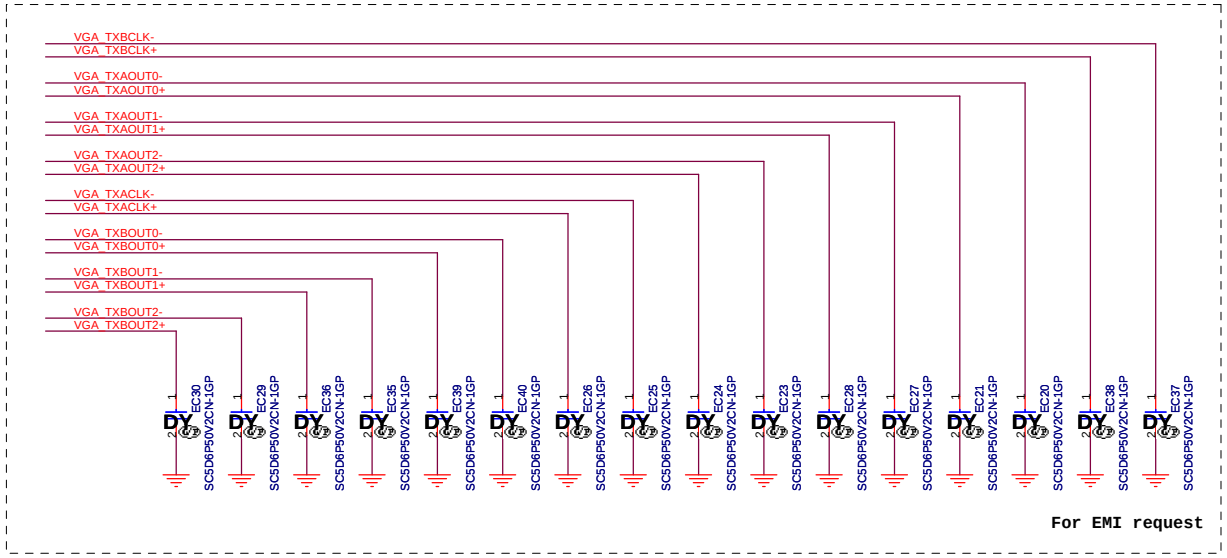
SSID = VIDEO

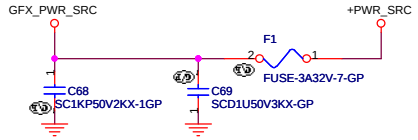
LVDS CONNECTOR





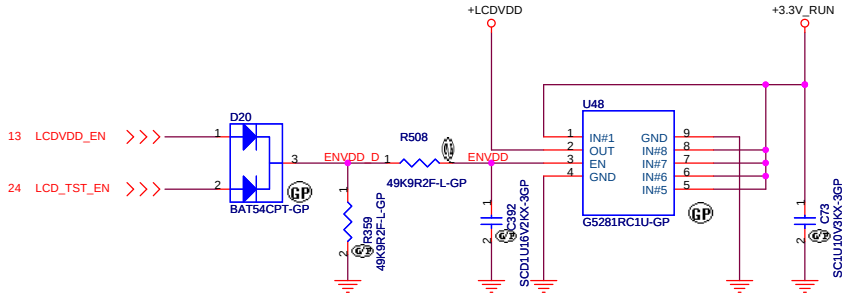
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

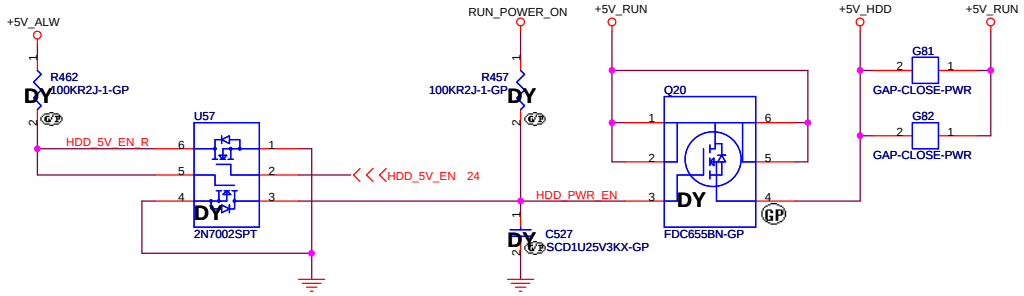
Title: LCD/Inverter Connector

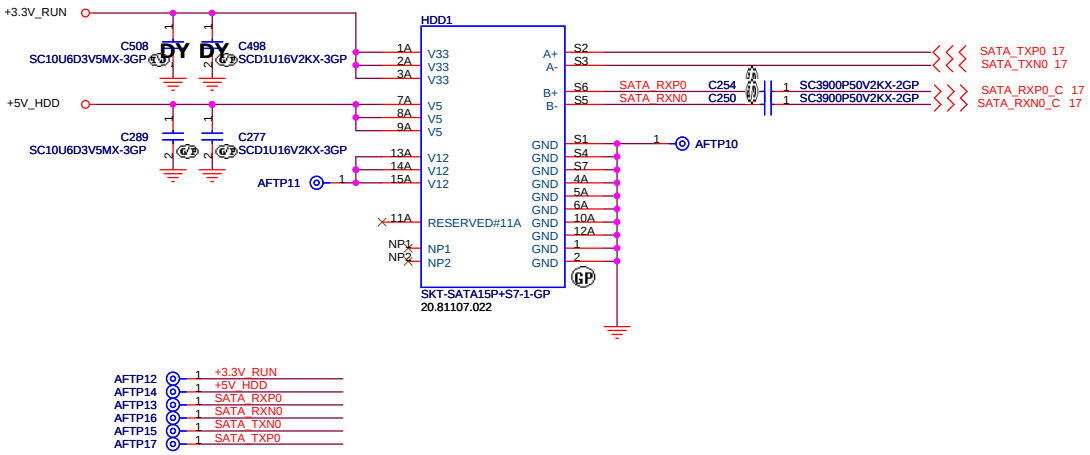
Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 35 of 58

SSID = SATA

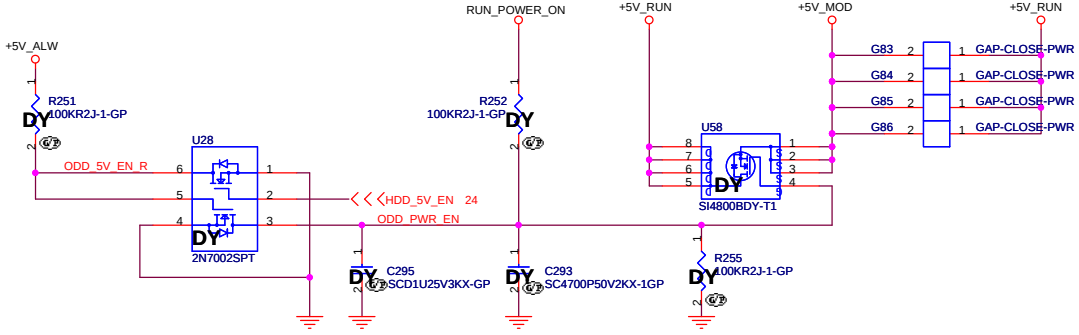
SATA HDD Connector

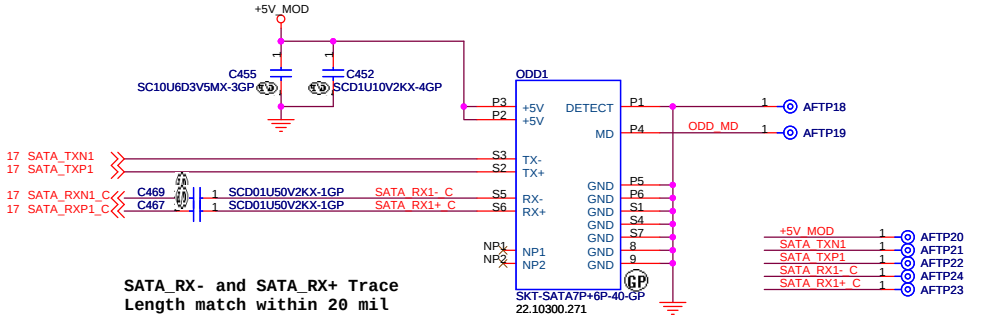




SSID = SATA

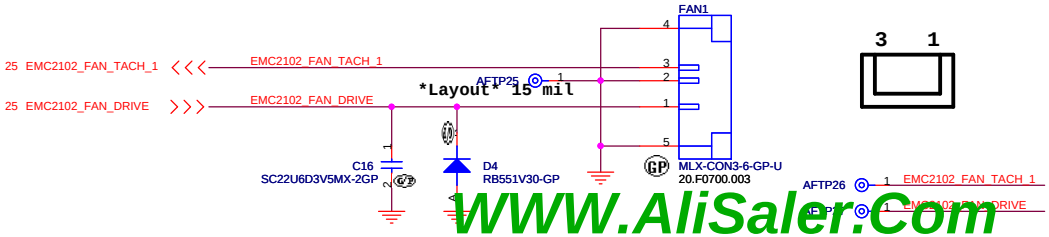
ODD Connector





SSID = Thermal

Fan Connector



<Core Design>

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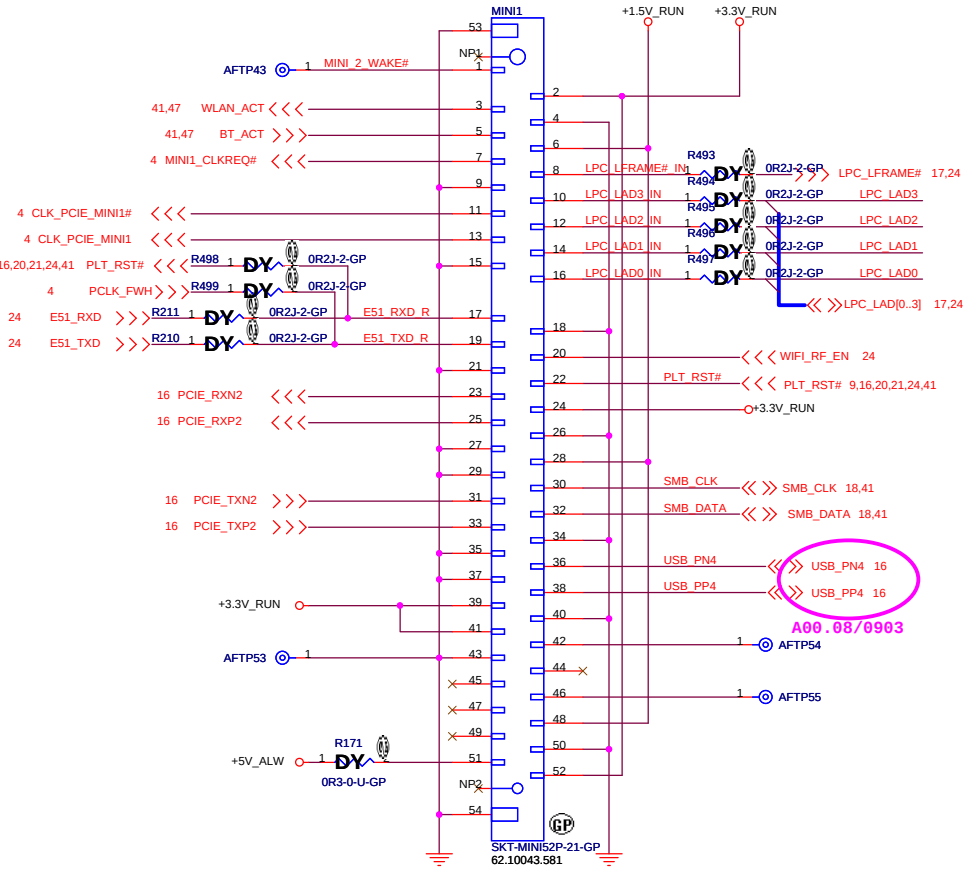
Title: HDD/ODD/FAN

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 36 of 58

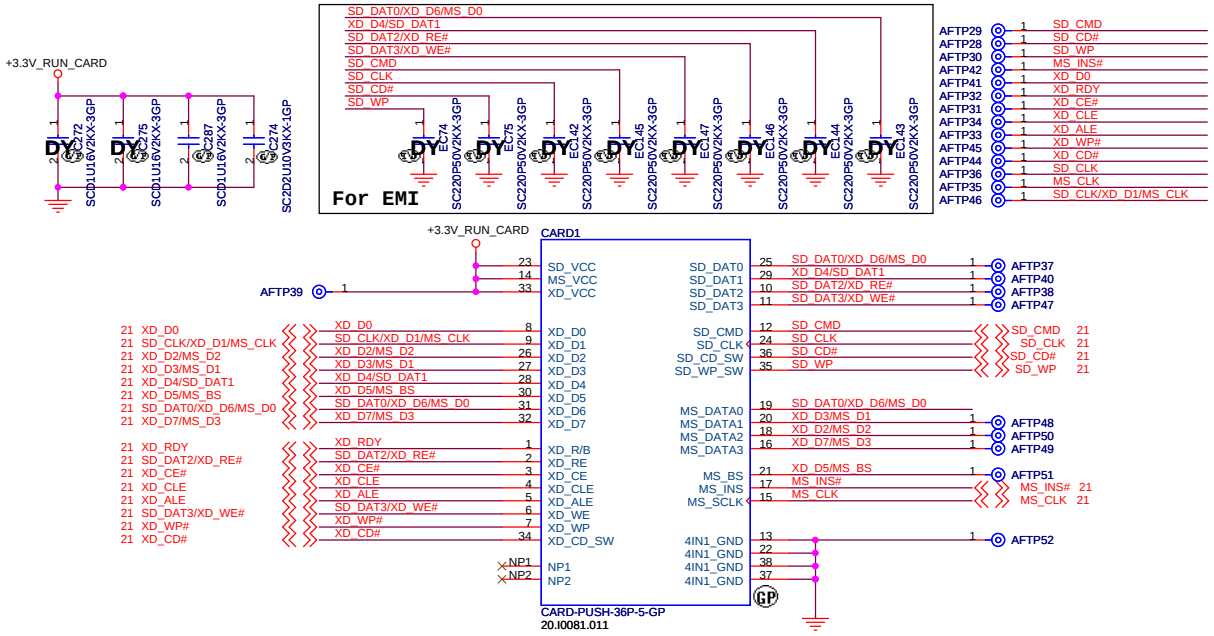
SSID = Wireless

Mini Card Connector(802.11a/b/g)



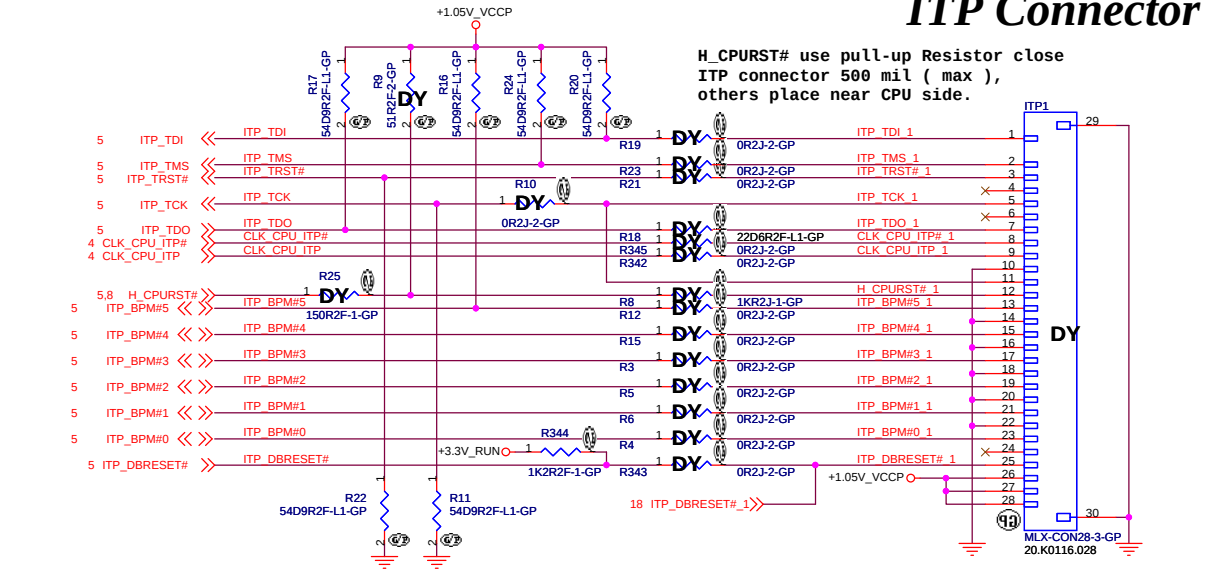
SSID = SDIO

SD/XD/MS Card Reader



SSID = User.Interface

ITP Connector



+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)

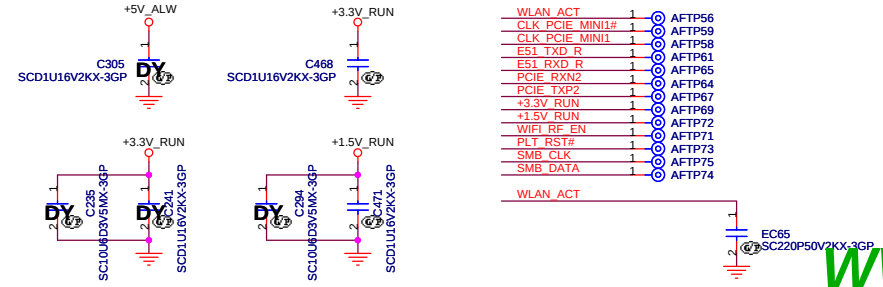
CPU

TCK(PIN AC5)

ITP Connector

TCK(PIN 5)

FBO(PIN 11)



<Core Design>

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Title: MINICARD(WLAN)/SD/ITP CONN

Size	Document Number	Rev
Custom	Roberts	A00

Date: Thursday, October 02, 2008 Sheet 37 of 58

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WWAN)

Size: Custom | Document Number: Roberts | Rev: A00

Date: Monday, September 22, 2008 | Sheet 38 of 58

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

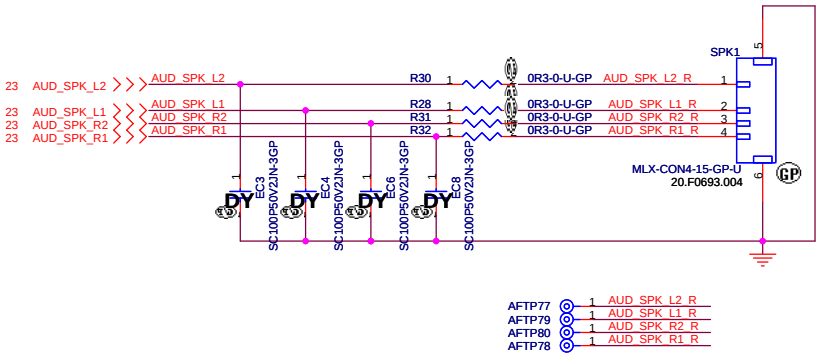
Title: MINICARD(WPAN)

Size: Custom | Document Number: Roberts | Rev: A00

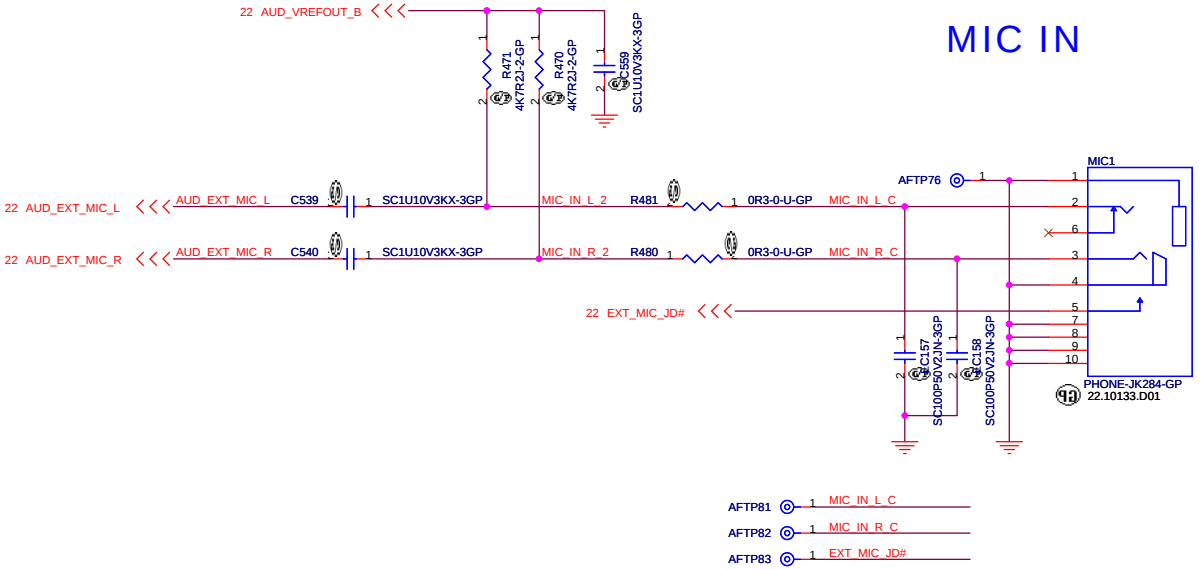
Date: Monday, September 22, 2008 | Sheet 39 of 58

SSID = AUDIO

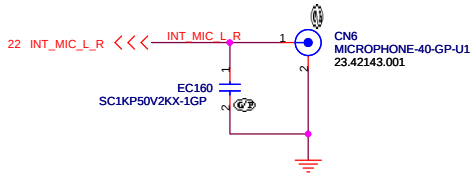
Speaker Connector



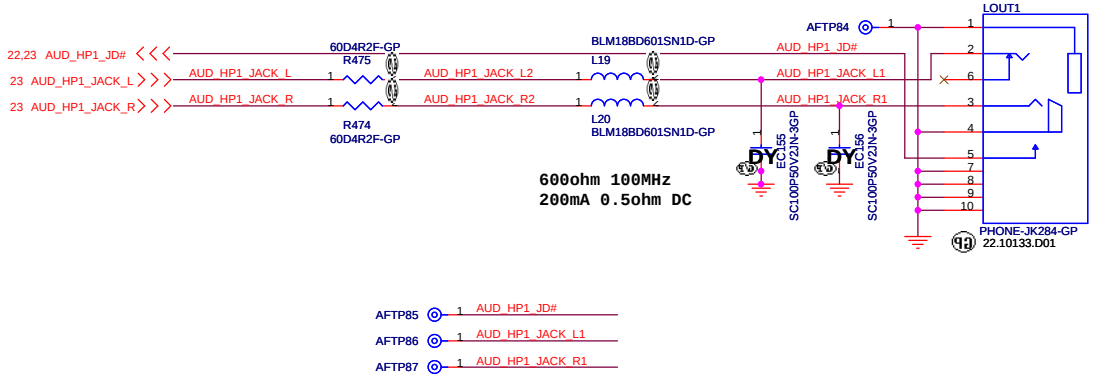
MIC IN



Internal Microphone



LINE1 OUT



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

Size: Custom | Document Number: **Roberts** | Rev: **A00**

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SSID = ExpressCard

Place them Near to Chip

+3.3V_ALW +1.5V_RUN +3.3V_RUN +3.3V_CARD +1.5V_CARD +3.3V_CARDAUX

C499 SCD1U16V2KX-3GP
C504 SCD1U16V2KX-3GP
C487 SCD1U16V2KX-3GP
C256 SC4D7U6D3V5KX-3GP
C484 SC10U6D3V5MX-3GP
C486 SCD1U16V2KX-3GP
C262 SC10U6D3V5MX-3GP
C502 SCD1U16V2KX-3GP
C505 SCD1U16V2KX-3GP

AFTP92	1	PCIE_TXP5
AFTP96	1	PCIE_TXN5
AFTP95	1	PCIE_RXP5
AFTP98	1	PCIE_RXN5
AFTP97	1	CLK_PCIE_NEW
AFTP100	1	CLK_PCIE_NEW#
AFTP99	1	+3.3V_ALW
AFTP101	1	LID_CLOSE#
AFTP102	1	CPUSB#
AFTP103	1	USB_PP7
AFTP104	1	USB_PN7
AFTP105	1	NEWCARD_CLKREQ#
AFTP106	1	+3.3V_CARD
AFTP108	1	PERST#
AFTP110	1	+3.3V_CARDAUX
AFTP109	1	PCIE_WAKE#
AFTP112	1	+1.5V_CARD
AFTP111	1	SMB_DATA
AFTP113	1	SMB_CLK

NEWCARD_OC# → AFTP114 → PM_SLP_S3# 18,24,25,30,31,32,34

U55 G577BR91U-GP

GND GND OC# RCLKEN STBY#

NC#16 1_5VIN 1_5VOUT 3_3VOUT 3_3VIN

+1.5V_RUN +1.5V_CARD +3.3V_CARD +3.3V_RUN

SHDN# PERST# CPUSB# CPPE# SYSRST#

PERST# CPUSB# CPPE# NRST

RN24 SRN100KJ-6-GP

PM_SLP_S4# 18,24,31

+3.3V_ALW

R435 0R2J-2-GP

C494 DY SC22P50V2JN-4GP

PLT_RST# 9,16,20,21,24,37

AUXOUT ALVOUT 1_5VIN 3_3VOUT 3_3VIN

+3.3V_CARDAUX +3.3V_ALW +1.5V_CARD

+3.3V_RUN +3.3V_CARD +1.5V_RUN

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

New Card Connector

NEW1 FOX-CONN30A-9GP 20.F0908.030

AFTP121 1 CPPE#
4 NEWCARD_CLKREQ#
+3.3V_CARD
PERST#
+3.3V_CARDAUX
18,20 PCIE_WAKE#
+1.5V_CARD
18,37 SMB_DATA
18,37 SMB_CLK
AFTP123 1 CONN_TP2
AFTP122 1 CONN_TP3

AFTP120

PCIE_TXP5 16
PCIE_TXN5 16
PCIE_RXP5 16
PCIE_RXN5 16
CLK_PCIE_NEW 4
CLK_PCIE_NEW# 4
+3.3V_ALW
LID_CLOSE# 24
CPUSB#
USB_PP7 16
USB_PN7 16

EC70 DY SC5P50V2CN-2GP
EC69 DY SC5P50V2CN-2GP

SSID = User.Interface

Camera Connector

CAMERA1 ACES-CON8-3-GP-U 20.F0779.008

AUD_DMIC_CLK_G_R R69 1 33R2J-2-GP
AUD_DMIC_IN0_R R70 1 33R2J-2-GP
+3.3V_CAMERA
USB_PN11
USB_PP11

CAMERA_DET# 24
AUD_DMIC_CLK_G 22
AUD_DMIC_IN0 22

AFTP107 C65 SC4D7P50V2CN-1GP

EC17 DY SC33P50V2JN-3GP
EC18 DY SC33P50V2JN-3GP

L2 DLW21SN900SQ2LUGP

USB_PN11 16
USB_PP11 16

Digital Mic Power

+3.3V_RUN → R77 0R0603-PAD → +3.3V_CAMERA

EC16 DY SCD1U16V2KX-3GP
C66 SC4D7U6D3V3KX-GP

AUD_DMIC_IN0_R
AUD_DMIC_CLK_G_R

EC15 DY SC220P50V2KX-3GP
EC14 DY SC220P50V2KX-3GP

AFTP89	1	CAMERA_DET#
AFTP88	1	AUD_DMIC_CLK_G_R
AFTP90	1	AUD_DMIC_IN0_R
AFTP91	1	+3.3V_CAMERA
AFTP93	1	USB_PN11
AFTP94	1	USB_PP11

SSID = User.Interface

Bluetooth Module conn.

+3.3V_RUN

BT1 FOX-CON10-GP-U 20.F0711.010

37,47 BT_ACT
37,47 WLAN_ACT
16 USB_PP6
16 USB_PN6
24,47 BLUETOOTH_EN

R74 DY 100KR2J-1-GP
R83 10KR2J-3-GP
C77 SC2D2U10V3KX-1GP
EC33 DY SC22P50V2JN-4GP
EC31 DY SC22P50V2JN-4GP
EC32 DY SC220P50V2KX-3GP

AFTP116	1	USB_PP6
AFTP115	1	USB_PN6
AFTP117	1	BLUETOOTH_EN
AFTP118	1	WLAN_ACT
AFTP119	1	+3.3V_RUN

<Core Design>

Wistron Corporation
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Title: Bluetooth/CAM/New Card
Size: Custom
Document Number: Roberts
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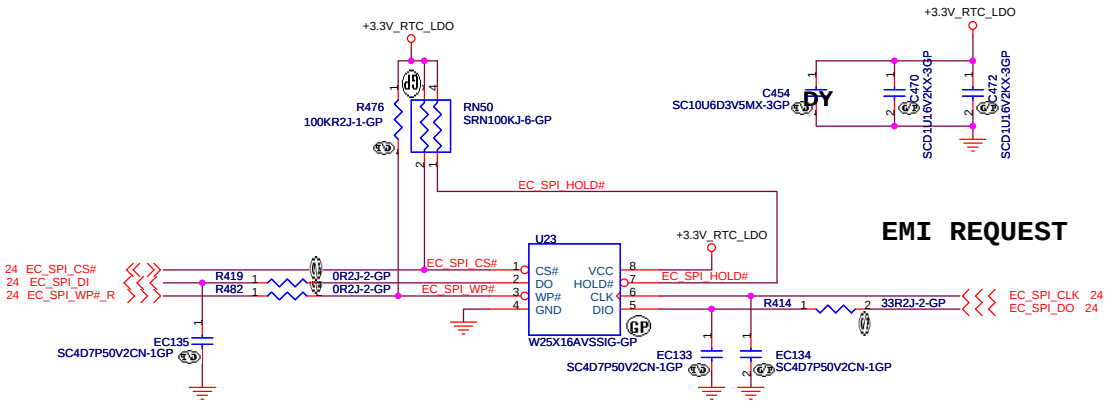
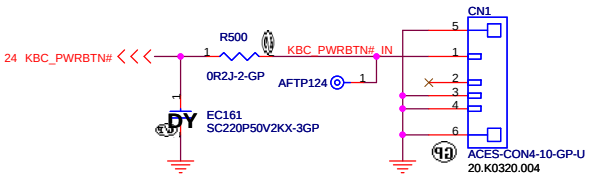
SPI FLASH ROM (16M bits)

SSID = Flash.ROM



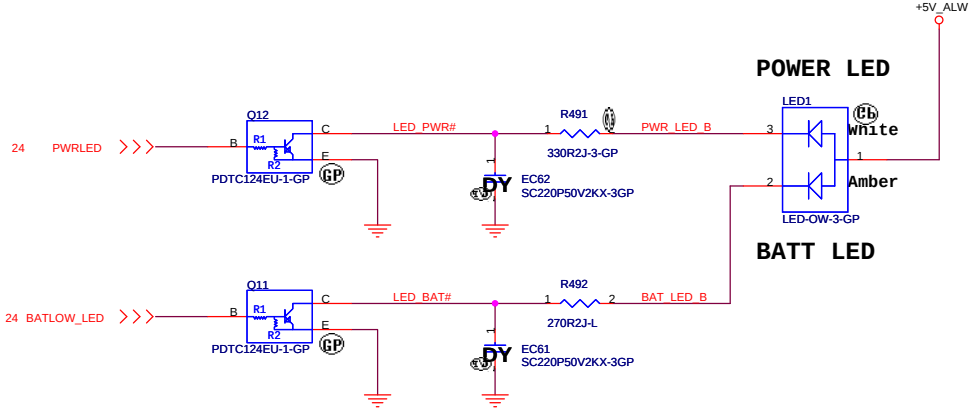
SSID = User.Interface

Power Dash Board to Board CONN



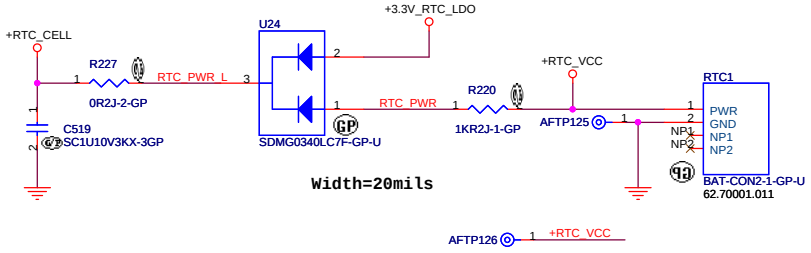
SSID = User.Interface

Power/Battery LED



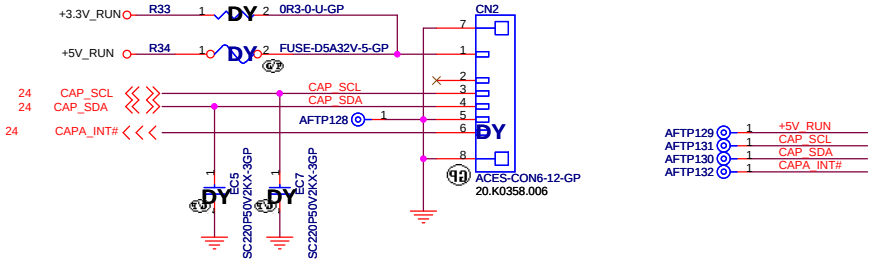
SSID = RBATT

RTC Connector



SSID = User.Interface

Capacitive Button



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH/LED/Power Dash/RTC/Cap

Size: Custom | Document Number: Roberts | Rev: A00

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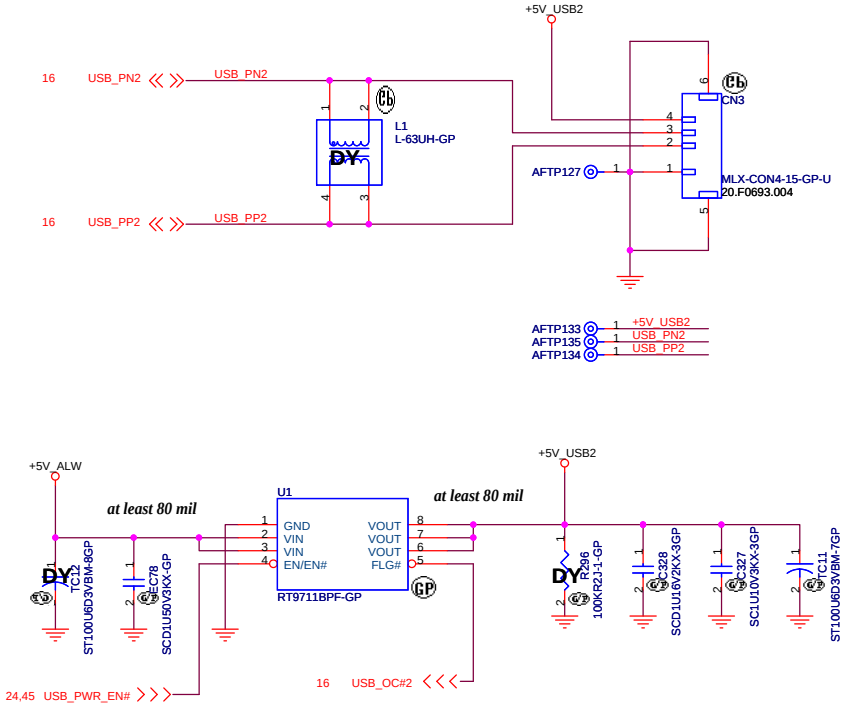
SSID = USB

Right USB Port CONN



<Core Design>

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Title: USB

Size: Custom | Document Number: Roberts | Rev: A00

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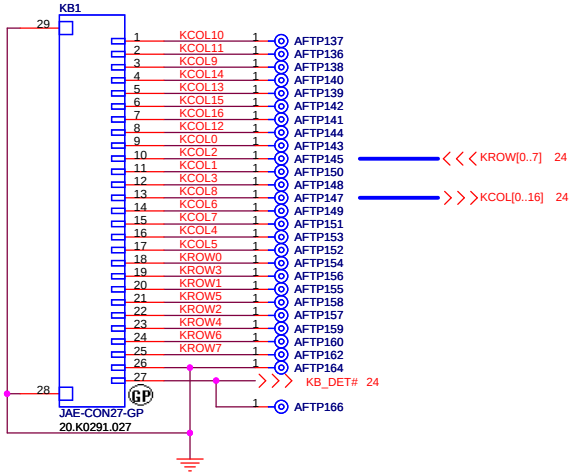
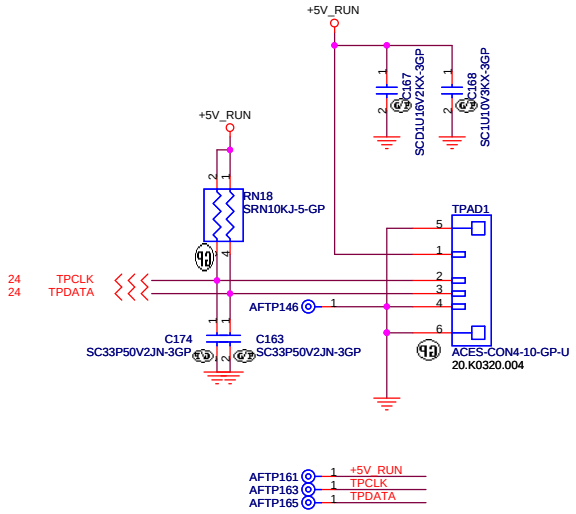
SSID = KBC

Internal KeyBoard Connector

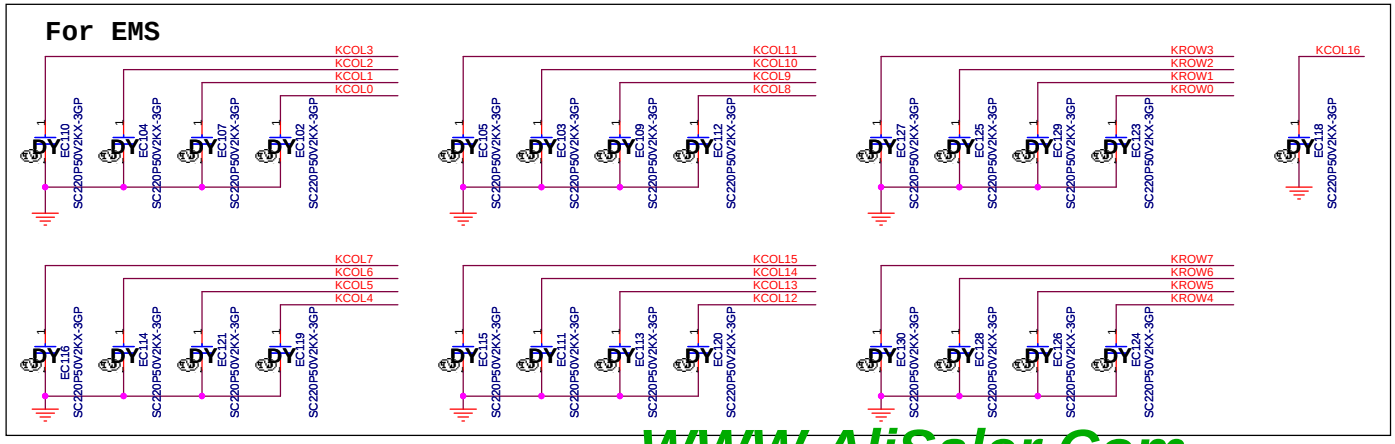


SSID = Touch.Pad

TouchPad Connector



For EMS



<Core Design>

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Title: KeyBoard/Touch Pad

Size: Custom | Document Number: Roberts | Rev: A00

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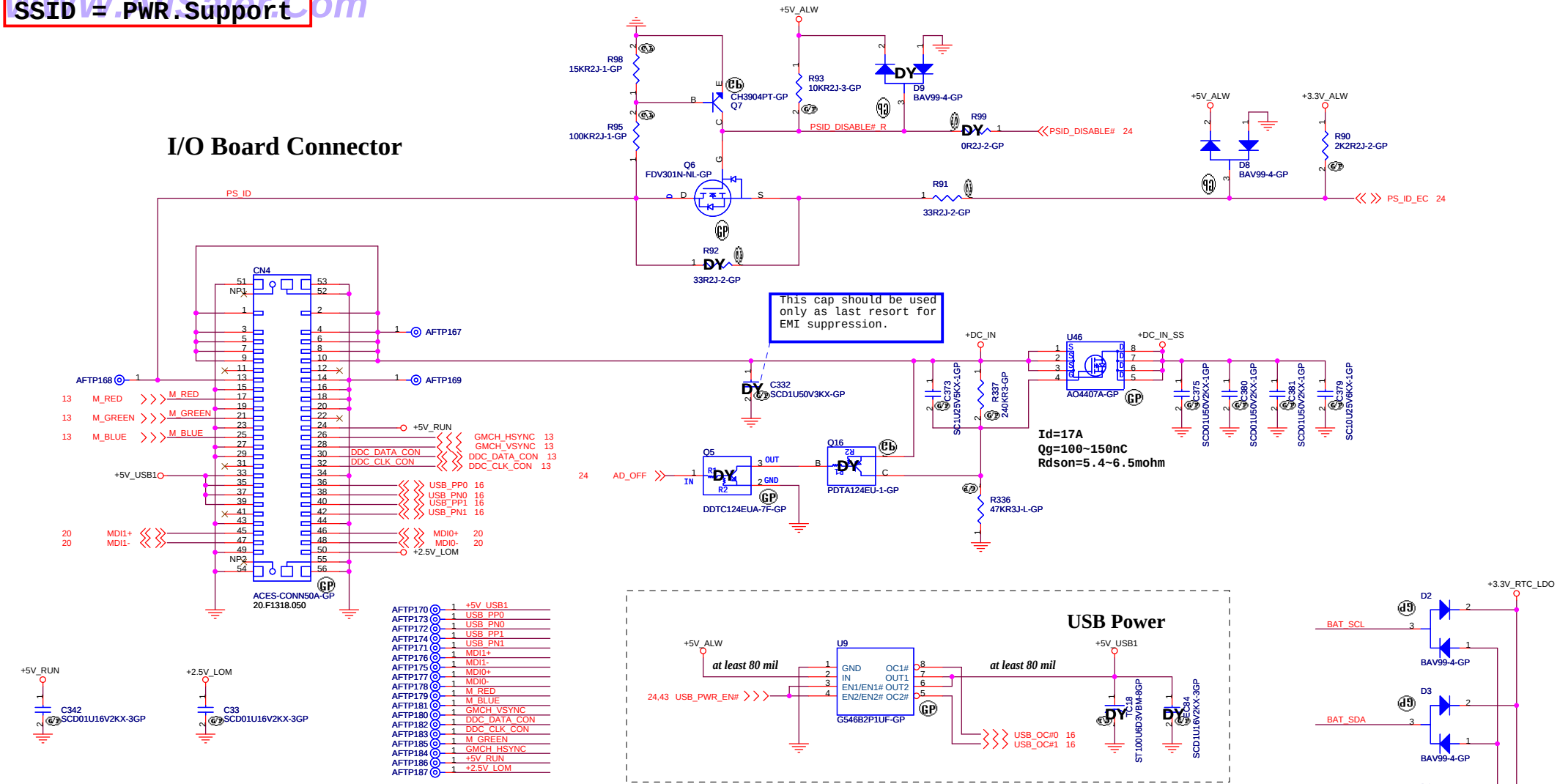
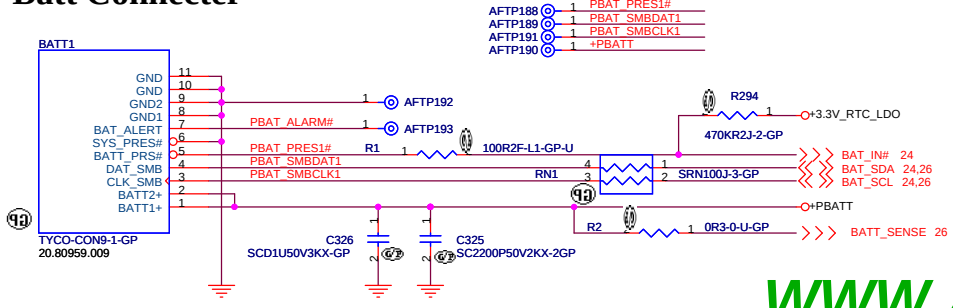
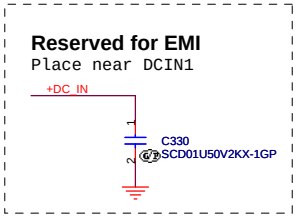
SSID = PWR.Support

I/O Board Connector



Batt Connecter





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LEFT IO/DCIN/BATT CONN

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 45 of 58

SSID = LOM

SSID = VIDEO

(Blanking)

<Core Design>

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Title: LAN CONNECTOR / CRT

Size: Custom | Document Number: Roberts | Rev: A00

Date: Tuesday, September 09, 2008 | Sheet 46 of 58

SSID = Mechanical

+3.3V_RTC_LDO

+3.3V_RUN

+5V_ALW

+DC_IN_SS

+PWR_SRC

+1.05V_VCCP

24,41 BLUETOOTH_EN
37,41 WLAN_ACT
37,41 BT_ACT

+5V_MOD

+5V_ALW

+3.3V_ALW

+0.9V_DDR_VTT

+1.8V_SUS

+3.3V_RUN

+5V_RUN

+5V_RUN

+3.3V_RUN

+3.3V_RUN

+PWR_SRC

For TP button holder touch.

34.4W005.001	34.4W004.001	34.4W001.001
Mini Card BOSS	New Card BOSS	NB Thermal BOSS

BOSS Placement

Spring

<Core Design>

Wistron Corporation
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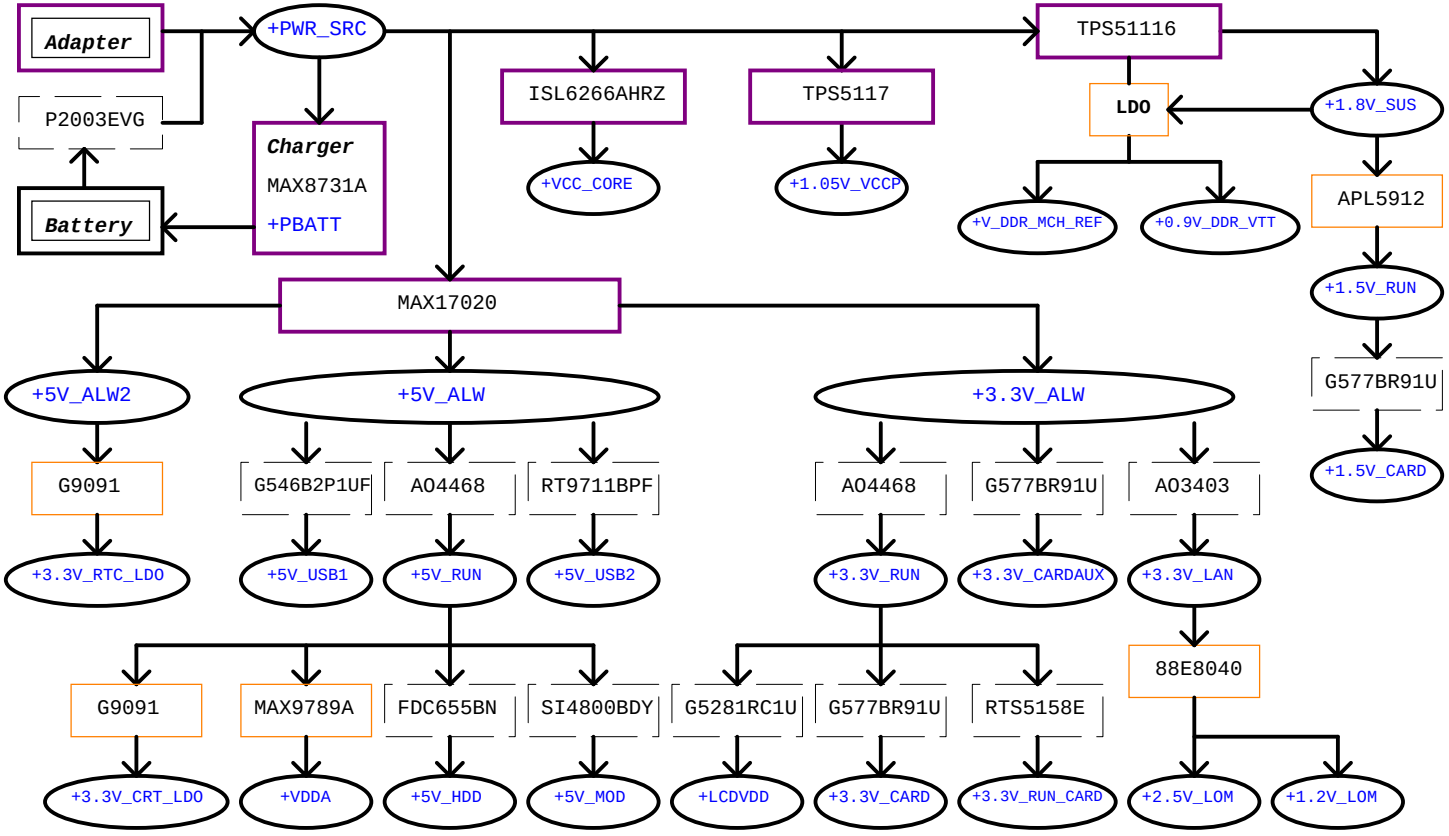
Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC

Size: Custom | Document Number: Roberts | Rev: A00

Date: Thursday, October 02, 2008 | Sheet 47 of 58



Power Shape

Regulator	LDO	Switch

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Block Diagram*

Size	Document Number	Rev
Custom	*Roberts*	*A00*

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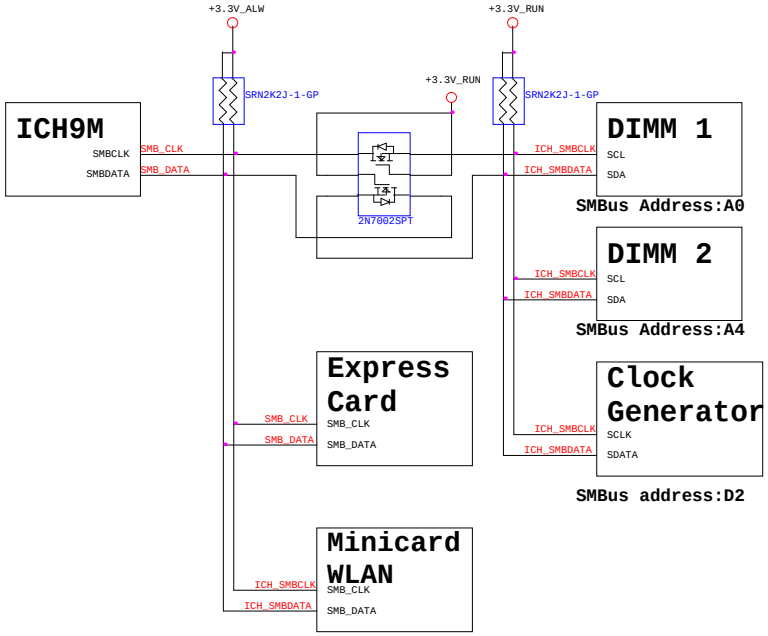
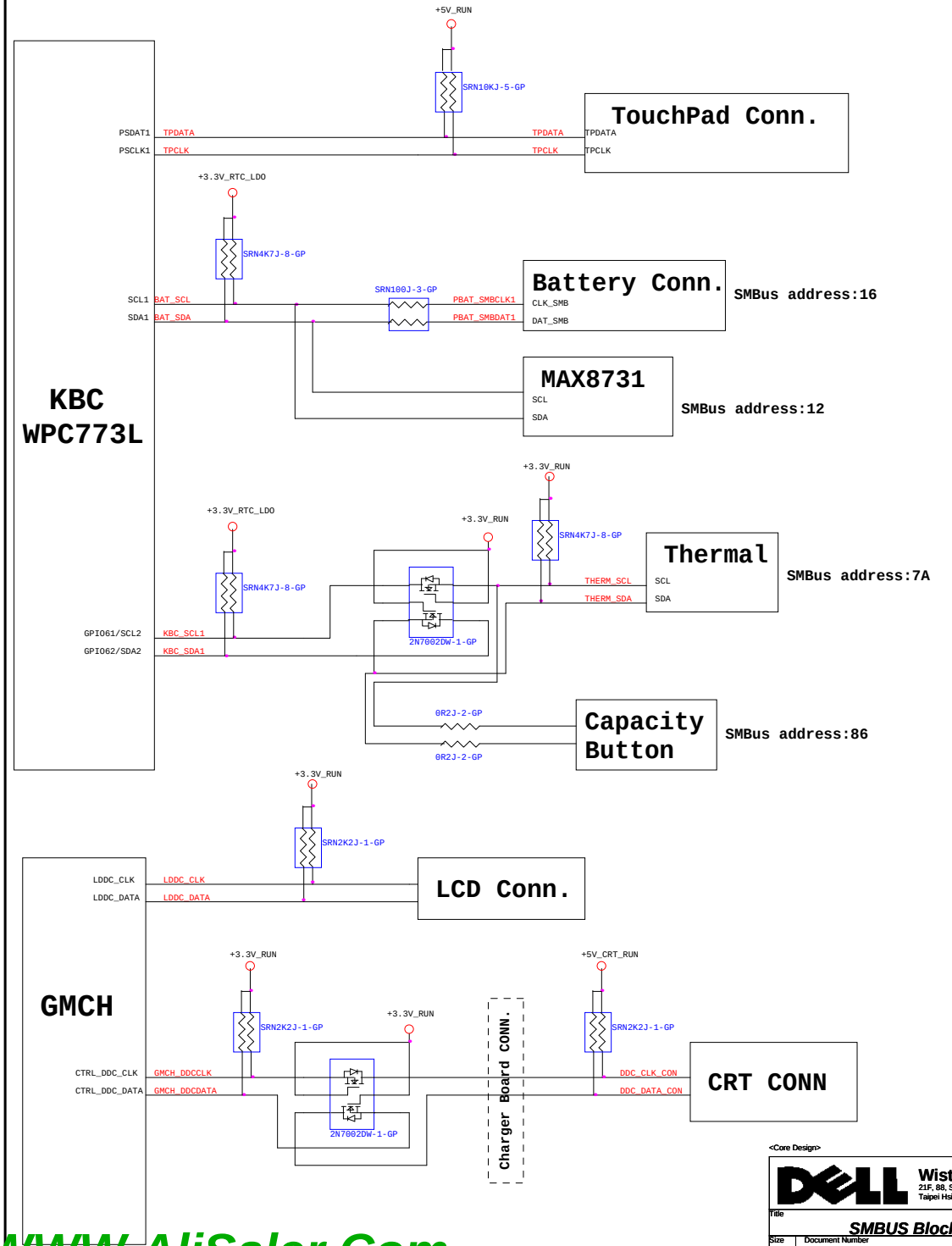
ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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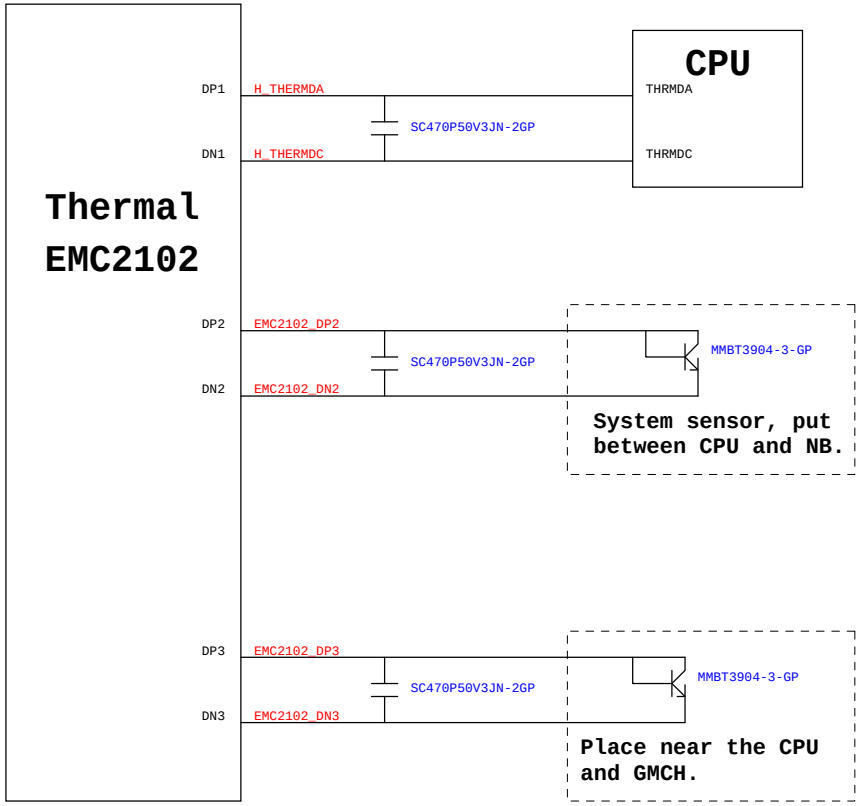
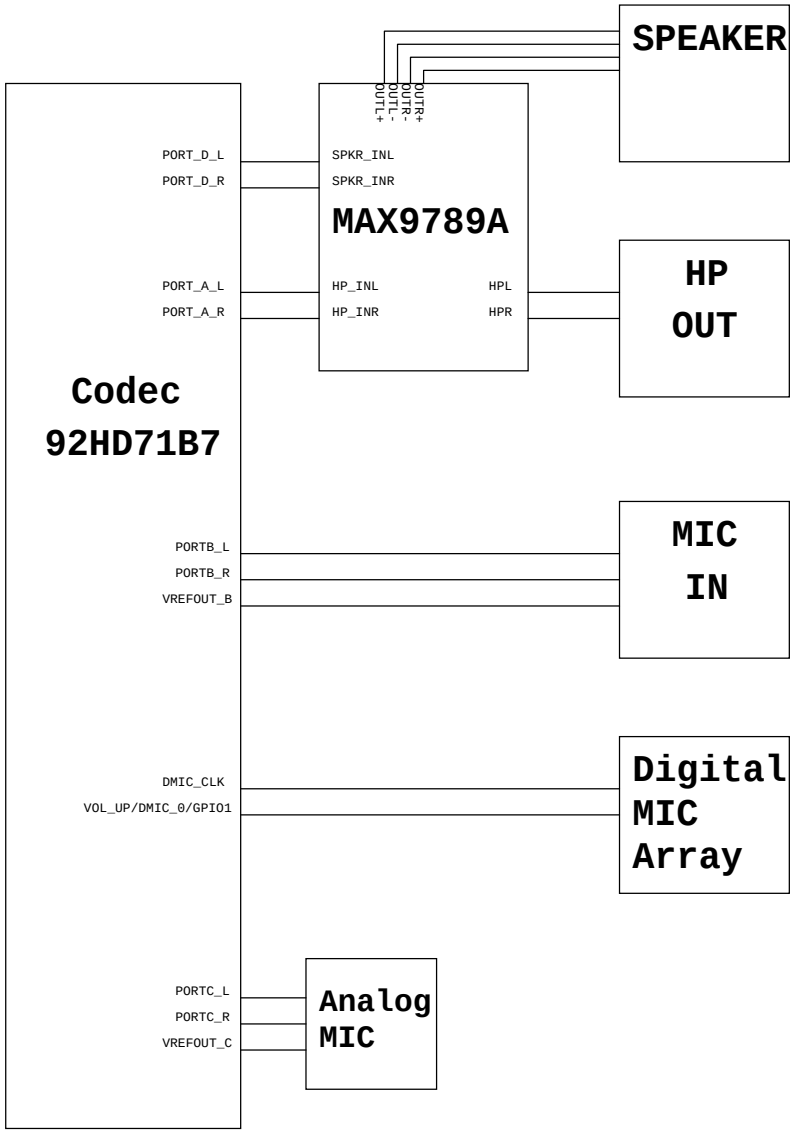
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Title: VGA-PCIE(1/4)

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Title: VGA-VRAM(2/4)

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Title: VGA-HDMI/STRAP(3/4)

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Title: VGA-LVDS/TV/CRT/(4/4)

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Title: VRAM

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	45	CN4 Pin.51 from +DC_IN change to GND.	CN4 Pin.51 should be ground.	EE
		2	24	Dummy R422	LID SW is push-pull type, no need pull high.	EE
		3	41	CAMERA1 conn reduce from 10 to 8 pin.	Follow camera design.	EE
		4	42	RTC1 CONN change p/n: 22.70031.001 to 62.70001.011.	Qty issue to change another.	EE
		5	46	Exchange H14 and H6 names.	Correction. H14 for mini card boss ; H6 is hole.	EE
06/05		6	42	Reverse LED1.	Correction. Amber for BAT_LED_B ; White for PWR_LED_B.	EE
		7	37,41	Remove CN5 and related circuit in page.41. Add dummy R: R493, R494, R495, R496, R497, R498, R499	Remove debug board connector. For debug mini card, change LPC Bus to mini card base. Set dummy res to avoid damaging MB or additional mini card.	EE
		8	37	Dummy R210, R211	For debug mini card. Set dummy res to avoid damaging MB or additional mini card.	EE
		9	24	Dummy R150. Staff R151.	PCB Version for SB.	EE
06/06		10	42	CN1 Pin.2 set to NC. Add R500 and dummy EC161.	Avoid shorting between KBC_PWRBTN# and GND. New R and C are for EMC pre-location.	EE
		11	24	Dummy R406. Change R425, R422, R409, R406, R401, R404 to 100K ohm.	Dummy R406 for no keyboard detect function. R change to 100k for save power.	EE
06/10		12	36	Update HDD symbol.	Update symbol and footprint for only SATA HDD. (no co-layout)	EE
		13	35~45	Change All TP near connectors to AFTP (ZZ.AFT30.101).	For AFTE test pad.	EE
		14	04	Change C461 and C462 from 15pF to 12pF.	For X3 cap choice by report suggestion.	EE
		15	17	Change C520 and C522 from 15pF to 12pF.	For X4 cap choice by report suggestion.	EE
06/12		16	24,42	Add 0 ohm R482 on EC_SPI_WP# and link to KBC/GPIO30. Change RN50 to 100k and Add R476 for EC_SPI_WP#.	KBC can control WP# of Flash ROM. R change to 100k for save power.	EE
		17	40	Change L19 and L20 to 68.00082.531.	For EMI.	EE
		18	45	Change M_RED to CN4 Pin.17 ; M_GREEN to CN4 Pin.21 ; M_BLUE to CN4 Pin.25. CN4 Pin.23 and Pin.27 to GND.	Avoiding noise to impact CRT signals.	EE
		19	47	Add H20.	Add square GND for TP button holder touch.	EE
06/16		20	42	Dummy CN2, R34.	Cap. button function is disable.	EE
		21	47	Add dummy EC162, EC163, EC164. Add dummy EC165, EC166. Add dummy EC167, EC168, EC169.	For EMI.	EE
06/17		22	04	Change R216 to 22 ohm.	The same clock dirve to U25 and U34.	EE
06/18		23	44	Dummy EC110, EC104, EC107, EC102, EC105, EC103, EC109, EC112, EC127, EC125, EC129, EC123, EC118, EC116, EC114, EC121, EC119, EC115, EC111, EC113, EC120, EC130, EC128, EC126, EC124.	For EMI.	EE
06/19		24	43	Short R26, R27.	No need 0 ohm R.	EE
		25	47	Add SW1.	ME request.	EE
		26	35	LCD1.38 link to GFX_PWR_SRC ; LCD1.37 set NC ; LCD1.35 link to +LCDVDD ; LCD1.34 link to +3.3V_RUN ; LCD1.33 link to LCD_BRIGHTNESS ; LCD1.32 to GND ; LCD1.31 link to LCD_CBL_DET#.	For LED backlight panel.	EE
		27	18	Dummy R179, R423.	SW check vender ID by SMBus.	EE
		28	24	Dummy R416, R418.	Cap. button function is disable.	EE
		29	40	Change LOUT1 and MIC1 to 22.10133.D01.	Change jack source.	EE
		30	17,18	Dummy U25.B10 link R506 to GND; U25.C18 link R501 to GND; Dummy U25.C21 link R502 to GND; U25.C11 link R503 to GND; Dummy U25.AE18 link R504 to GND; U25.AF21 link R505 to GND. Dummy R421, R424.	Avoiding abnormal action in U25(ICH9-M).	EE
06/23		31	25	Change R82 to 20K 1% ; Change R78 to 10K 1%.	For T8 shutdown is set 88 deg-C.	EE
		32	47	Add dummy EC170, EC171, EC172, EC173, EC174.	For EMI.	EE
06/27		33	42	Change U23 to 72.25X16.A01.	Better performance.	EE

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Title: Change List - EE (1/2)

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
07/30	X02	34	18	Staff R421, R424. (PT build cut-in)	Avoiding always issue interrupt event.	EE
		35	23	Dummy R290 ; Staff R291. (PT build cut-in)	Adjust audio amp. gain value.	EE
		36	20	Add dummy R507.	Add RUN power for LAN.	EE
		37	21	Short R253, R254.	No need 0 ohm R.	EE
		38	24	Staff R138, R150 ; Dummy R141, R151.	PCB Version for SC.	EE
		39	35	Add R508 ; Change R359 to 49.9k ohm.	For LCD power sequence.	EE
		40	22,23	Move C535 (Change 0.033uF), R472 to page.23. Remove C536 (Change 0.033uF), C542. Add R484 to gnd ; Add C566 for AUD_SET, C567 for AUD_BIAS. C565 for 6040 only.	For PC beep.	EE
		41	36	Material change: HDD1	ME request.	EE
		42	37	Material change: CARD1	ME request.	EE
		43	47	Material change: SPR4	ME request.	EE
		44	09	Add TP271 for U52/ SDVO_CTRLDATA.	TP.	EE
08/06		45	41	Short R79, R80.	No need 0 ohm R.	EE
		46	04	Symbol change: U54.	For clock generator co-layout.	EE
		47	-	Change to close line: R204, R200, R356, R139, R152, R408, R394, R390, R403, R402, R96, R120, R378, R360, R140, R373, R97, R405, R155, R154, R262, R266, R439, R265, R226, R269, R174, R175, R183, R432, R433, R434, R430, R431, R437, R191, R177, R270, R188, R436, R452, R259, R282, R250, R249, R467, R153, R81, R77.	No need 0 ohm R.	EE
		48	24,32	Move R182 to page.24.	Movement.	EE
		49	37	Short R428, R426 ; Add DY L21.	Pre-location for Minicard USB trace.	EE
08/07		50	-	Short R139, R96 , R155, R154, R226, R174, R175, R432, R433.	No need 0 ohm R.	EE
		51	19	Staff C488.	For DMI.	EE
08/11		52	23	Use 2.2uF C564 and C557 for Maxim U62 IC.	For improving bobo sound.	EE
		53	32	Material change: TC23. (DY)	Material issue.	EE
08/15		54	11	Material change: TC19, TC21.	Material issue.	EE
09/02	A00	55	21	USB_PP10 for U34.5 ; USB_PN10 for U34.4. (ST build cut-in)	Schematic modification.	EE
		56	24	Staff R151 ; Dummy R150.	PCB Version for -1(Xbuild).	EE
		57	24	Add dummy R509 to gnd for KBC GPIO24. (09/10 update)	For GM45.	EE
09/03		58	05,17	Dummy R76 ; Staff R167	For H_THRMTRIP# to SB.	EE
		59	12,20,24	Change to close line: R115, R246, R182, R158, R159, R170.	No need 0 ohm R.	EE
		60	37	Remove L21.	No need L21.	EE
09/09		61	19	Staff R453, C511 ; DY C521.	Follow Intel DG 2.0.	EE
09/10		62	04	Short RN42, RN43, RN44, RN45, RN48, RN22, RN23, RN54, RN53, RN52, RN51.	No need 0 ohm R.	EE
		63	21	Add dummy R510 and C568. Staff R282 0 ohm.	For U34 power bounce issue.	EE
09/22		64	04	Dummy R196.	For debug. Normally, no need it.	EE
		65	25	R82 change to 10k ; R78 change to 2.37k.	For T8 thermal shutdown setting.	EE
		66	23	Staff R288 ; Dummy R289.	For Audio amp. gain.	EE
10/02		67	21	Dummy R284, C318. Staff R282 to Bead 68.00082.531. Staff R510 to 2.2K ; Staff C568.	For U34 power bounce issue.	EE

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Title: Change List - EE (2/2)

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	32	R189 change to 2.2K ohm, C216 dummy.	For +1.5V_RUN sequence.	Power EE
		2	30	C378 change to 0.01uF.	For +1.05V_VCCP sequence.	Power EE
		3	34	C316 change from 4.7nF to 0.01uF.	For +3.3V_RUN sequence and improve +3.3V_ALW voltage drop due to SW(U31) turn on quickly (higher loading).	Power EE
		4	34	Staff C314 and change from 4.7nF to 6.8nF.	For +5V_RUN sequence and improve +5V_ALW voltage drop due to SW(U30) turn on quickly (higher loading).	Power EE
06/05		5	36	Dummy Q20, U57, R462, R457, C527 and U58, U28, R251, R252, C293, C295 Change R258, R256 to G81, G82 Change R278, R279, R277, R276 to G83, G84, G85, G86	No sniffer function, no control HDD & ODD power.	Power EE
06/06		6	27	R136 change to 270k and R108 change to 237k	For 5V/3.3V OCP	Power EE
		7	28	R38 change to 12.1k R323 change to 3.92k , C360 change to 0.047 uF 10V X7R	R38 for VCORE OCP R323 and C360 for transient and load line.	Power EE
		8	31	PC9 to GND.	PC9 to GND otherwise DC-DC IC can not obtain power to generate 1.8V/0.9V output.	Power EE
		9	31	PR2 change to 9.31k ohm.	For 1.8V OCP.	Power EE
		10	30	Add D23.	For power sequence.	Power EE
06/10		11	18,24	Remove U60, R482, R476 and change trace name VRMPWRGD to VGATE_PWRGD.	For power sequence.	Power EE
06/18		12	31	PR7.1 link to +5116_PWR_SRC.	Reserve for other source.	Power EE
06/23		13	30	Rename "+1.05V_SUSP" to "+1.05V_RUNP"	Correct naming.	Power EE
		14	26,45	Material change: U37, U46, U47.	NIKO-SEM P2003EVG component has some risk.	Power EE
07/30	X02	15	31	Change PR7 value from 622k to 619k ohm.	For 2nd source.	Power EE
08/11		16	26,45	Material change: U37, U46, U47.	Power team request.	Power EE
09/03	A00	17	26,27, 28,31	Change to close line: R46 ,R137 ,R127,R106 ,R384 ,R391 ,R35 ,R29 ,R307 ,R308 ,R309 ,R303 ,R304 , R298 ,R301 ,R310 ,R313 ,PR14.	No need 0 ohm R.	Power EE
		18	26	R61 change 4.7k to 10k.	Power team request.	Power EE
XX		19				
XX		20				
		21				
		22				
XX		23	x	x	x	Power EE
XX		24	x	x	x	Power EE
		25	x	x	x	Power EE

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Title: Change List - Power

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