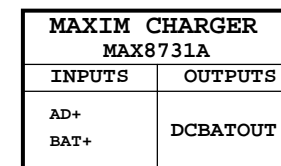
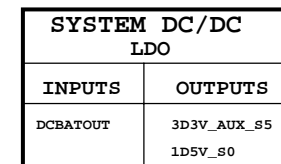
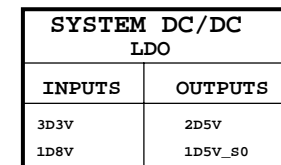
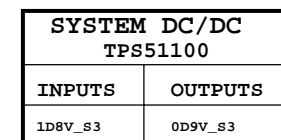
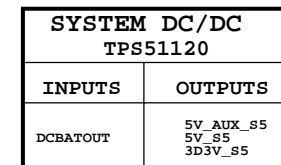
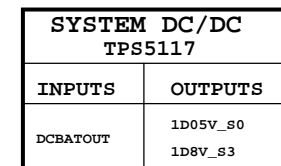
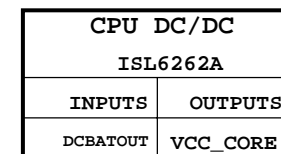
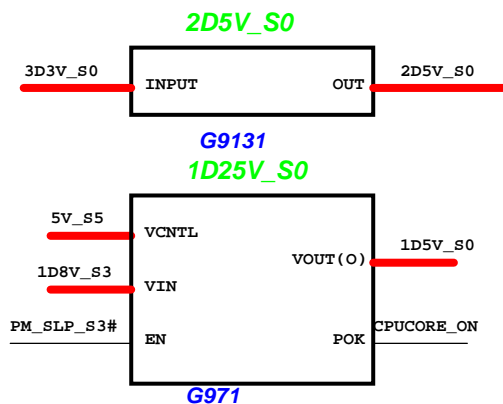
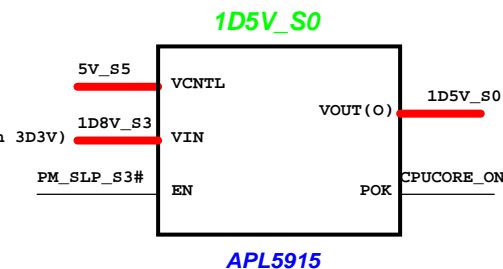
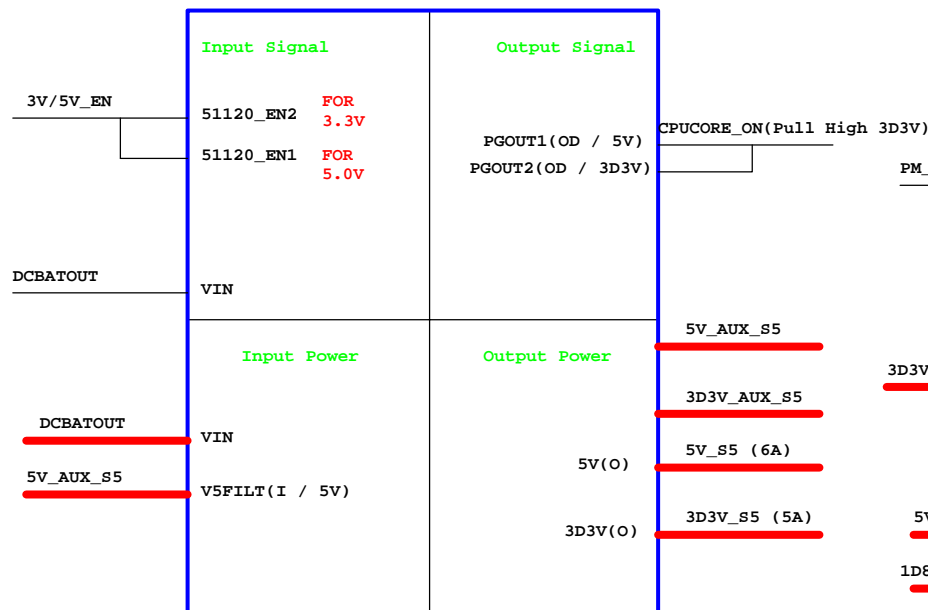
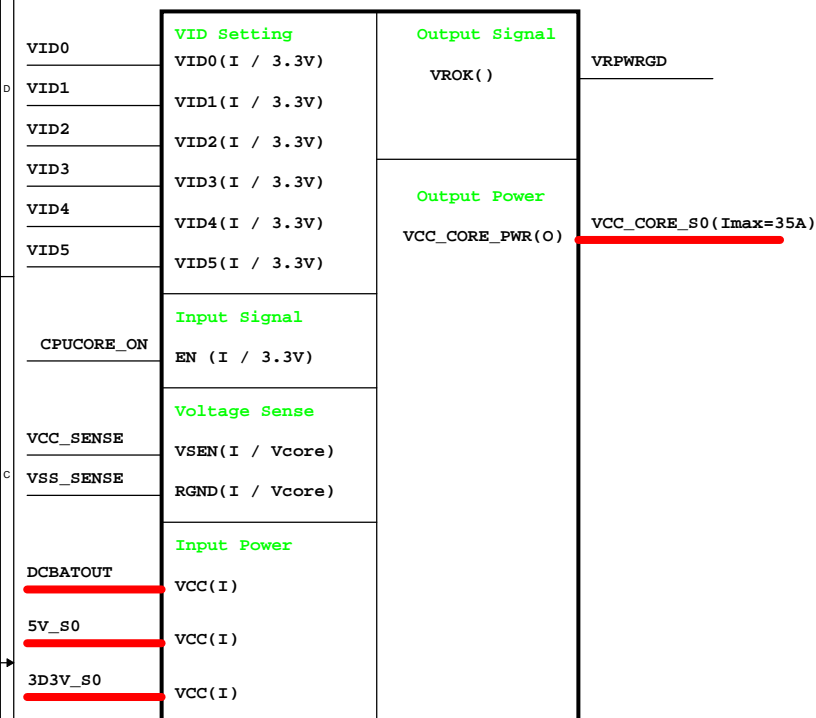


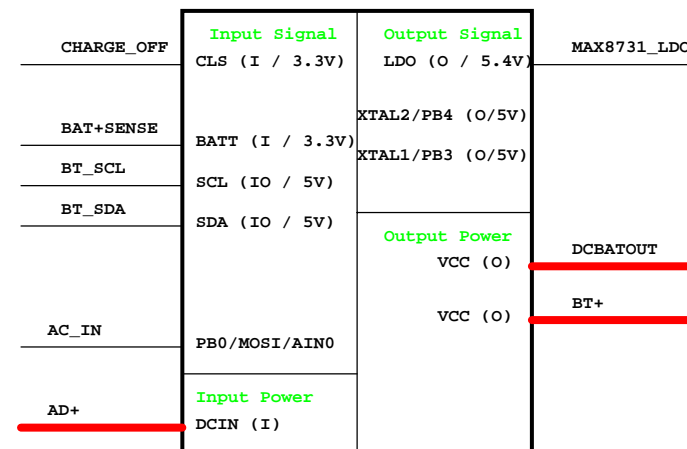
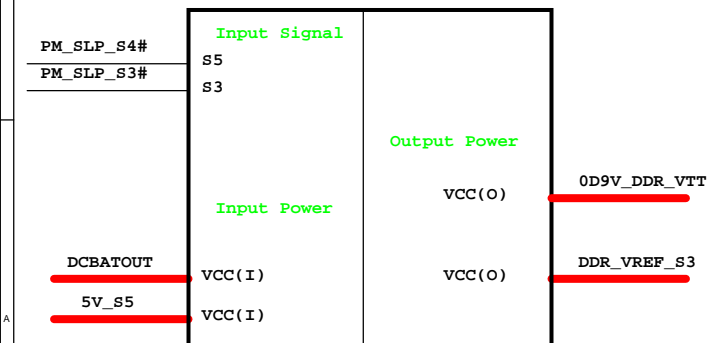
PCB P/N : 07211

Revision : -1

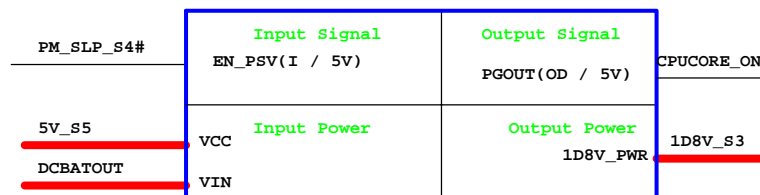


CPU_CORE
ISL6262ATI TPS51120
3D3V/5V

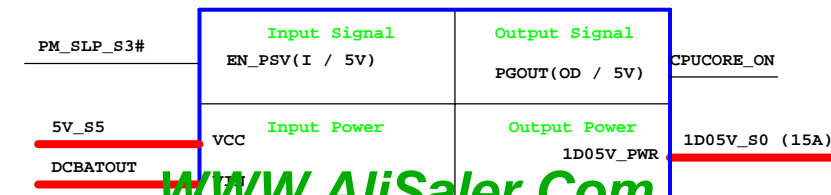
Charger_MAX8731A

TI TPS51100
0.9V/DDR_VREF_S3

TPS51117_1D8V_S3



TPS51117_1D05V



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Block Diagram		
Size A3	Document Number	Rev -1
Date: Wednesday, September 12, 2007 Sheet 2 of 47		

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVPtp3	AZ_DOUT_ICH	Description	
0	0	RSVD	
0	1	Enter XOR Chain	
1	0	Normal Operation(default)	
1	1	Set PCIe port cofig bit1	

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

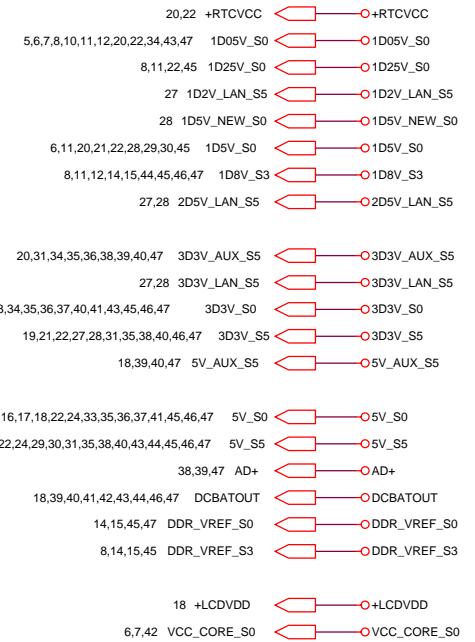
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
	TBD



INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 8	Low Power PCI Express	Low Power mode
CFG 9	PCI Express Graphics Lane Reversal	Normal Mode(Lanes number in order)
CFG 16	FSB Dynamic ODT	Disabled
CFG 19	DMI Lane Reserved	Reserved Lane
CFG 20	Concurrent SDVO/PCIe	Only PCIe or SDVO is operation
SDVO_CTRL_DATA	NO SDVO Card Present	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation


<Core Design>

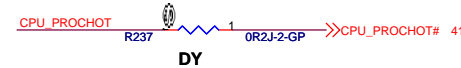
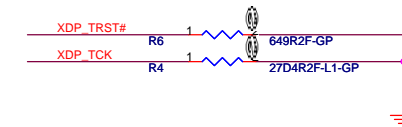
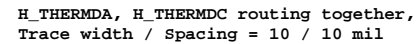
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Table of Content		
Size A3	Document Number DS2-Intel	Rev -1
Date: Wednesday, September 12, 2007	Sheet 3 of 47	



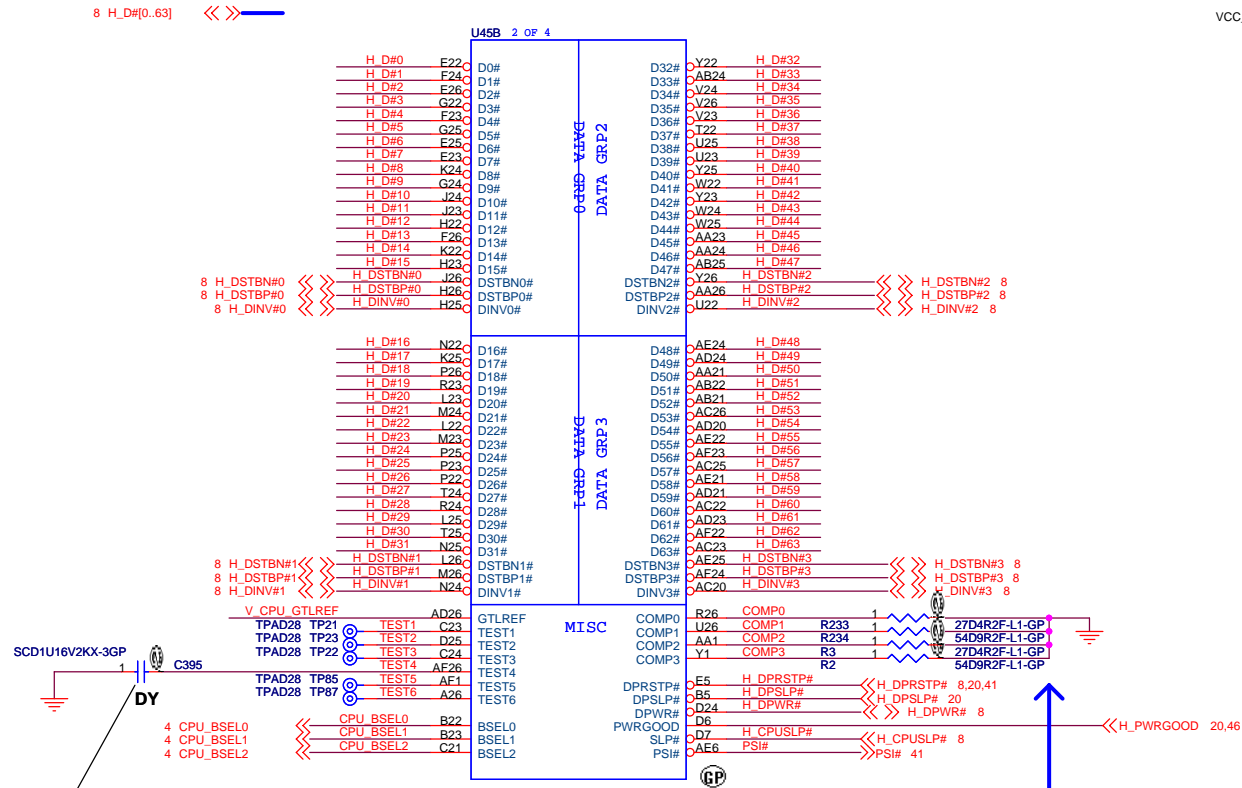
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Clock generator ICS9LPRS365			
A3	Document Number	DS2-Intel	Rev -1
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layout note:Zo =55
ohm , 0.5" MAX for
GTLREF

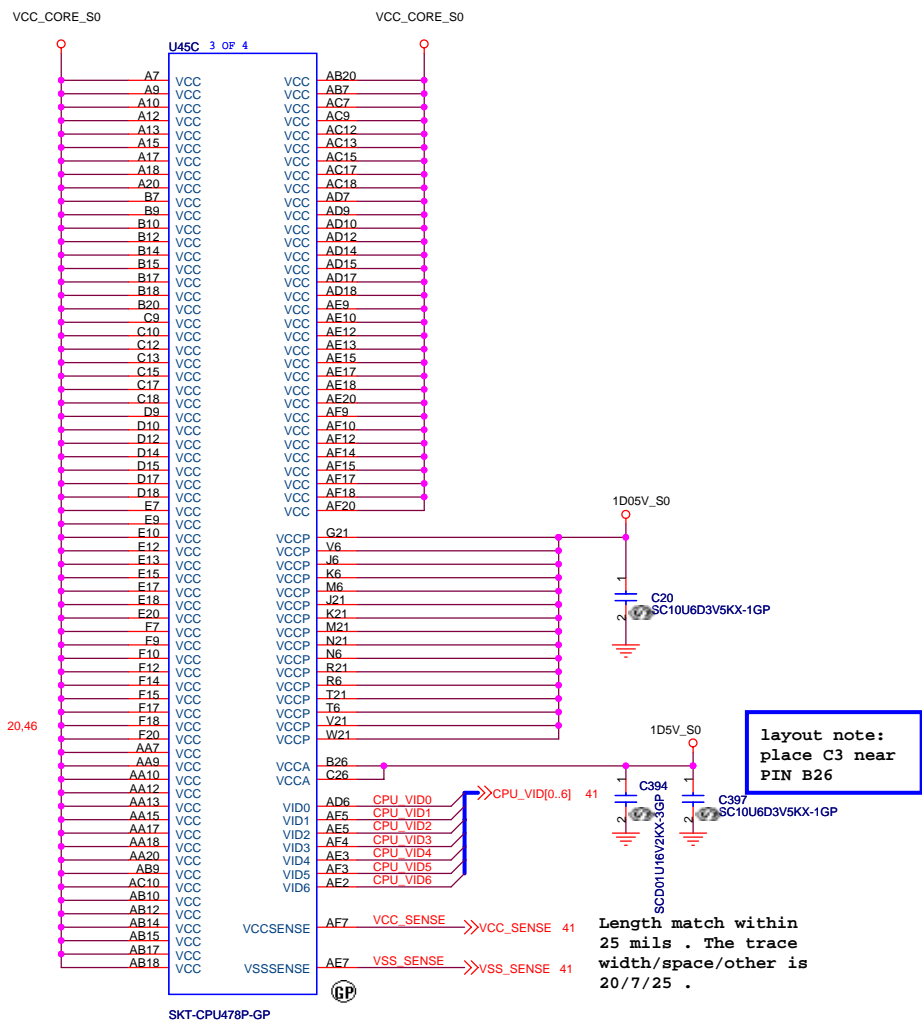
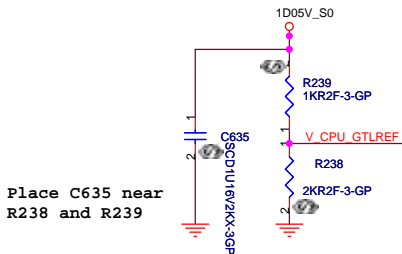


PLACE C25 close to the TEST4 PIN,
make sure TEST3,TEST4,TEST5 trace
routing is reference to GND and
away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

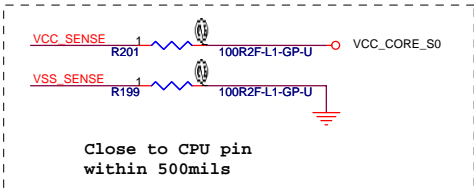
Resistor Placed
within 0.5" of CPU
pin. Trace should
be at least 25 mils
away from any other
toggling signal .
COMP[0,2] trace
width is 18 mils.
COMP[1,3] trace
width is 4 mils .

Close to CPU
pin AD26
Z0=55 ohm
with in
500mils .



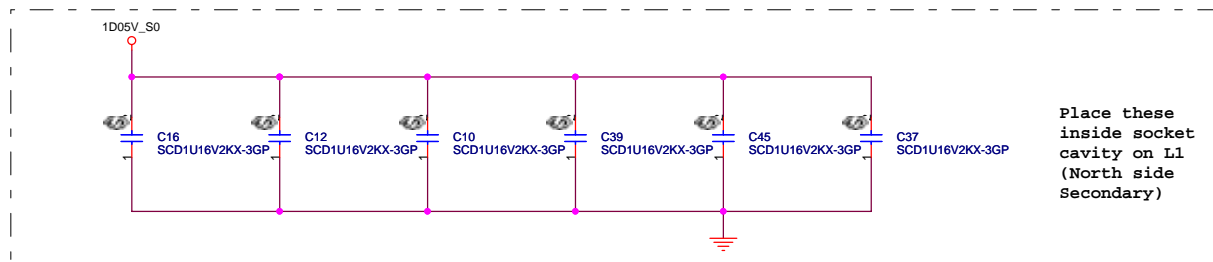
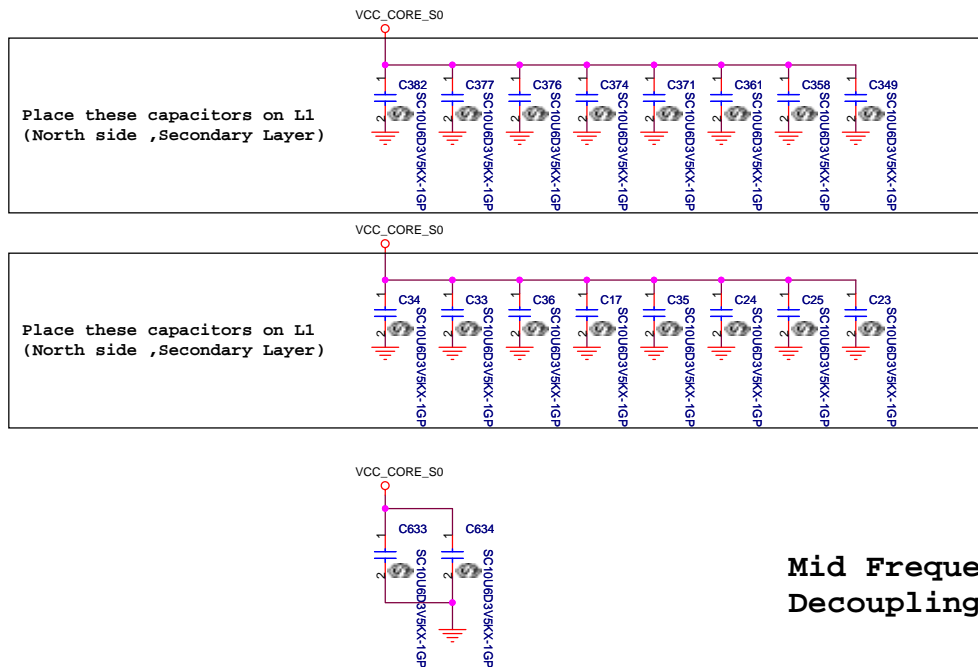
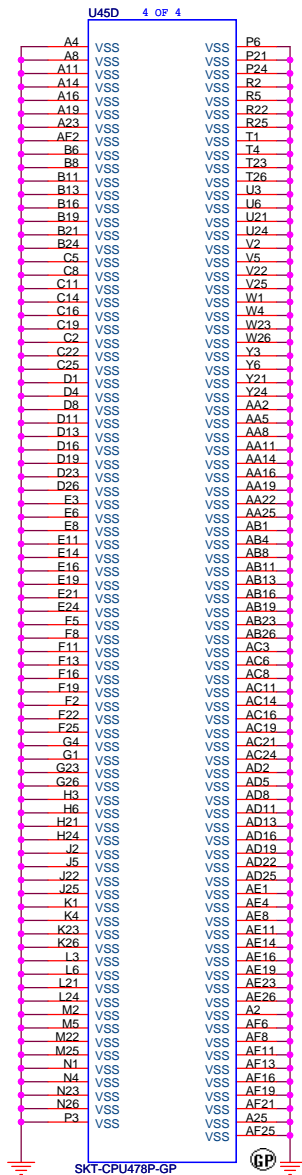
layout note:
place C3 near
PIN B26

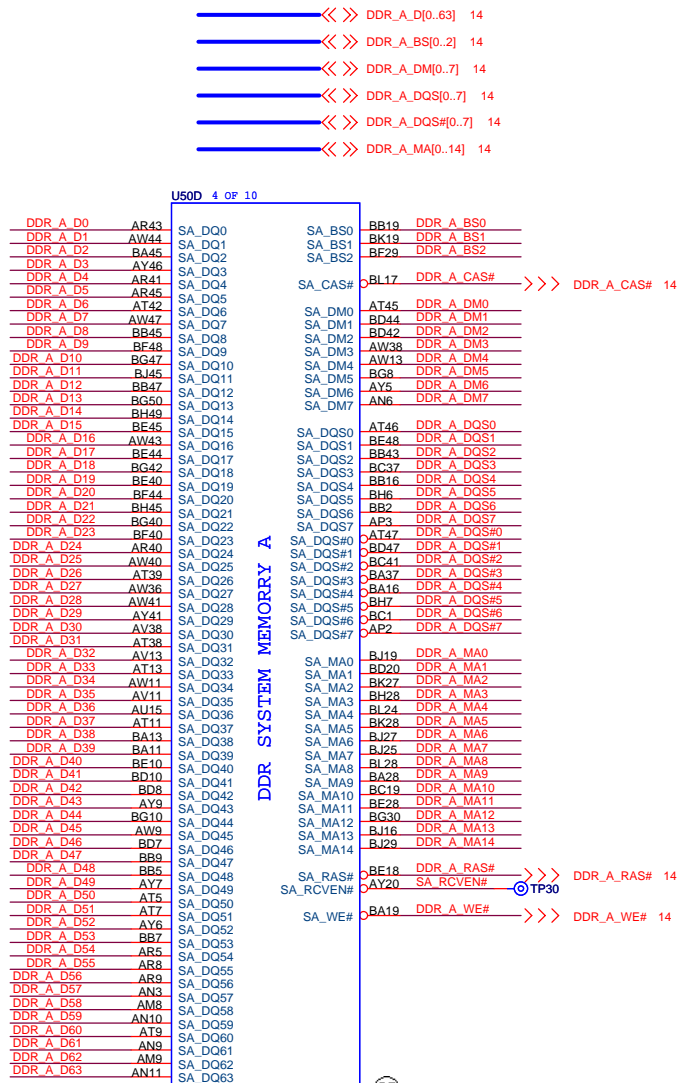
Length match within
25 mils . The trace
width/space/other is
20/7/25 .



<Core Design>

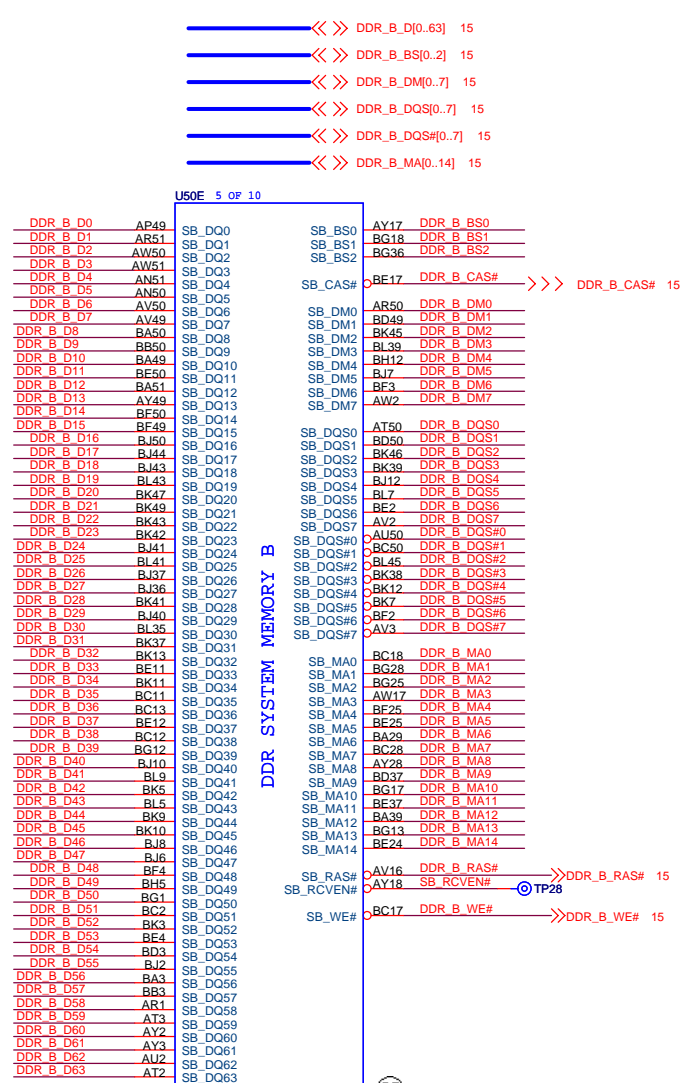
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Title			
Meron(2/3)-AGTL+PWR			
Size A3	Document Number		Rev
DS2-Intel		-1	
Date:	Wednesday, September 12, 2007	Sheet	6 of 47





CRESTLINE-GP-U-NF

NB:71.GM965.A0U

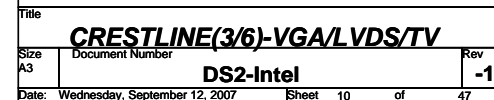


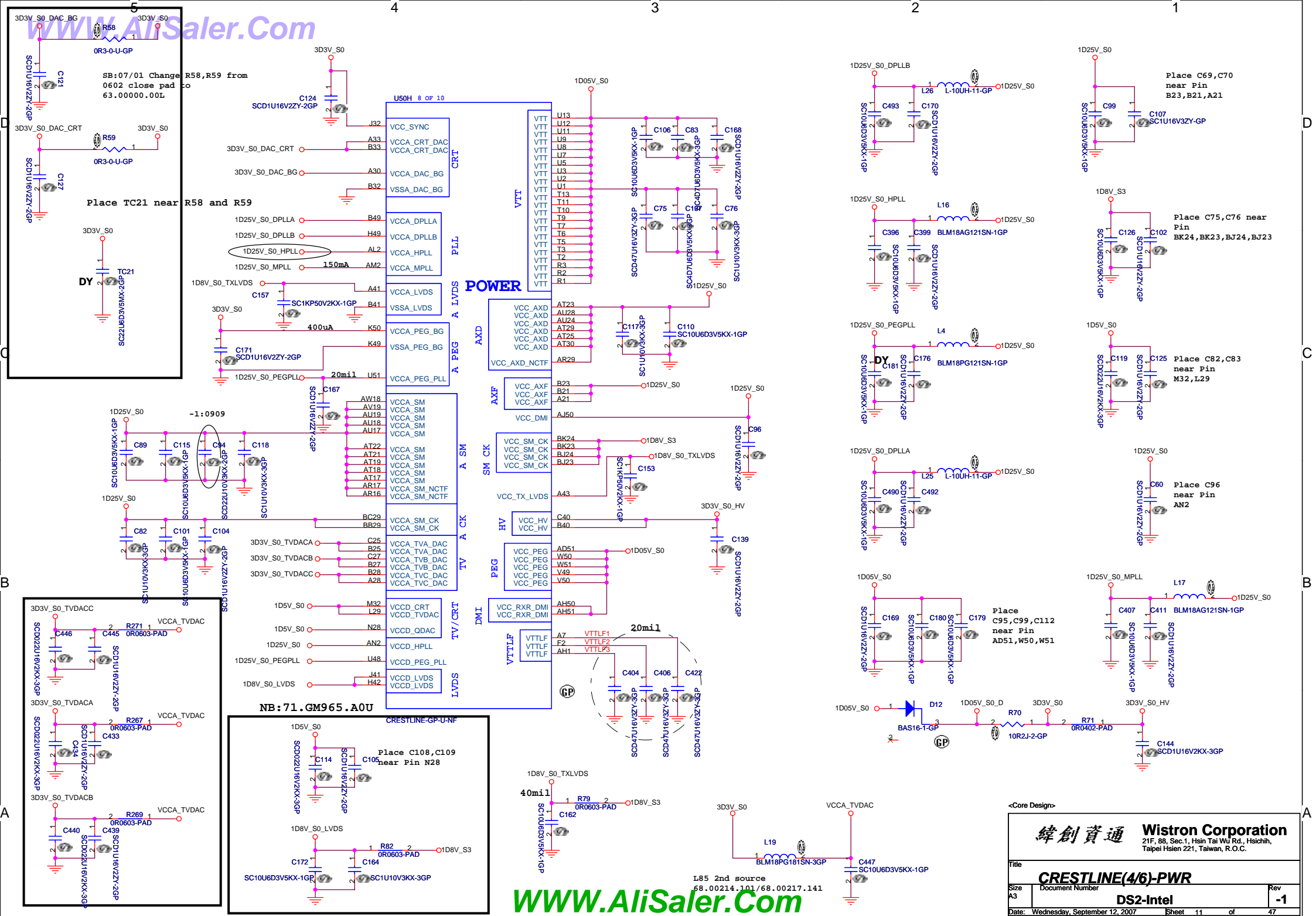
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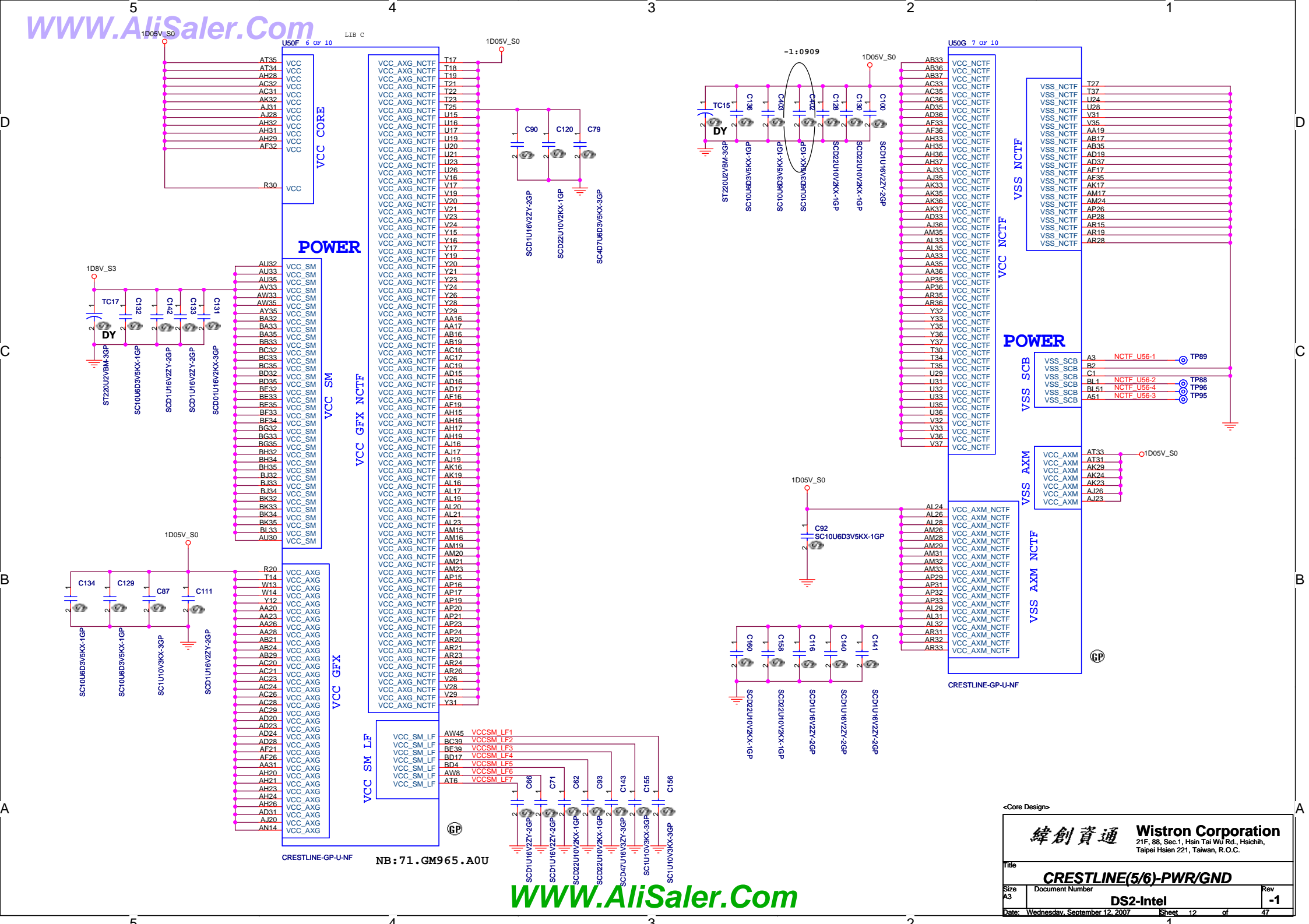
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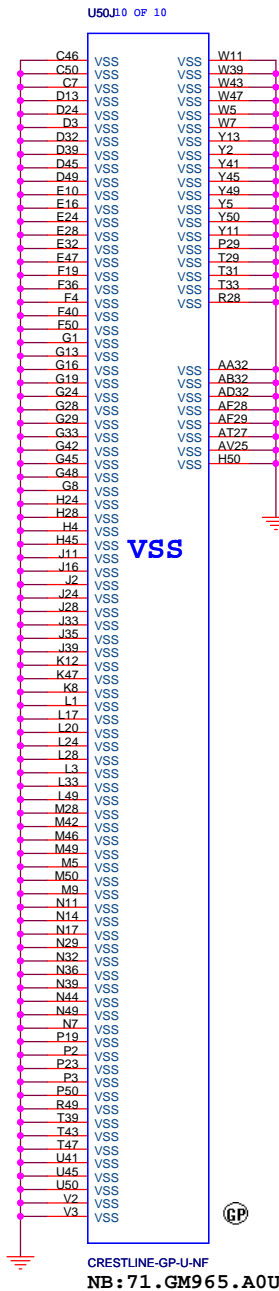
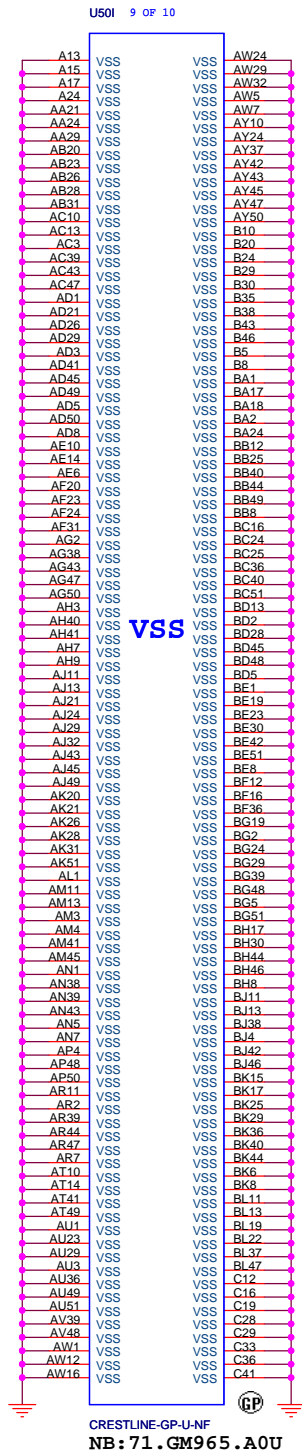
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<p>緯創資通 Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchiu, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title CRESTLINE(2/6)-DDR2 A/B CH</p>	
<p>Size A3</p>	<p>Document Number DS2-Intel</p>
<p>Date: Wednesday, September 12, 2007</p>	<p>Sheet 9 of 47</p>
<p>Rev -1</p>	



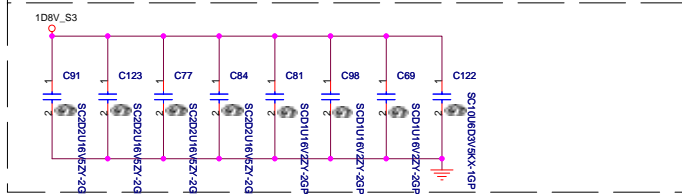




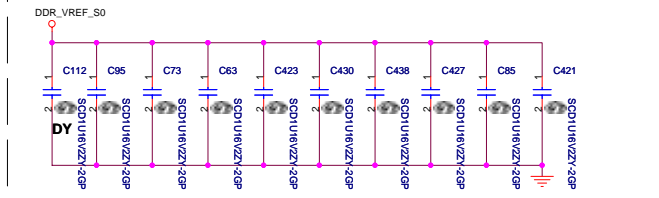


9 DDR_A_DQS#0..7] << >>
 9 DDR_A_DQ#0..63] << >>
 9 DDR_A_DM#0..7] << >>
 9 DDR_A_DQS#0..7] << >>
 9 DDR_A_MA#0..14] << >>
 9 DDR_A_BS#0..2] << >>

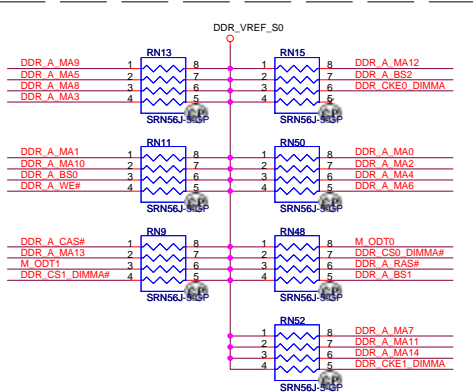
Layout Note:
Place near DM1



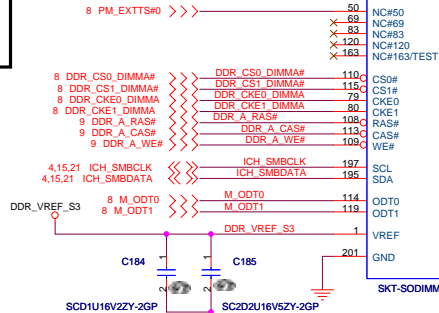
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V5



change to 8P4R



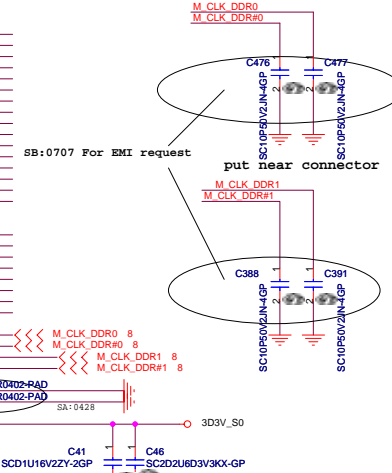
Layout Note:
Place these resistors
closely DM1, all
trace length Max=1.5"



DM2

DDR_A_MA0	102	A0	DDR_A_DQS0	13	DDR_A_DQS0
DDR_A_MA1	101	A1	DDR_A_DQS1	31	DDR_A_DQS1
DDR_A_MA2	100	A2	DDR_A_DQS2	51	DDR_A_DQS2
DDR_A_MA3	99	A3	DDR_A_DQS3	70	DDR_A_DQS3
DDR_A_MA4	98	A4	DDR_A_DQS4	131	DDR_A_DQS4
DDR_A_MA5	97	A5	DDR_A_DQS5	148	DDR_A_DQS5
DDR_A_MA6	94	A6	DDR_A_DQS6	169	DDR_A_DQS6
DDR_A_MA7	92	A7	DDR_A_DQS7	188	DDR_A_DQS7
DDR_A_MA8	93	A8	DDR_A_DQS#0	211	DDR_A_DQS#0
DDR_A_MA9	91	A9	DDR_A_DQS#1	229	DDR_A_DQS#1
DDR_A_MA10	90	A10/AP	DDR_A_DQS#2	249	DDR_A_DQS#2
DDR_A_MA11	89	A11	DDR_A_DQS#3	268	DDR_A_DQS#3
DDR_A_MA12	89	A12	DDR_A_DQS#4	289	DDR_A_DQS#4
DDR_A_MA13	116	A13	DDR_A_DQS#5	309	DDR_A_DQS#5
DDR_A_MA14	86	A14	DDR_A_DQS#6	329	DDR_A_DQS#6
DDR_A_BS2	85	A15	DDR_A_DQS#7	349	DDR_A_DQS#7
DDR_A_BS2	85	A16_BA2			
DDR_A_BS0	107	BA0	DDR_A_DM0	10	DDR_A_DM0
DDR_A_BS1	106	BA1	DDR_A_DM1	26	DDR_A_DM1
DDR_A_D0	5	DO0	DDR_A_DM2	67	DDR_A_DM2
DDR_A_D1	7	DO1	DDR_A_DM3	130	DDR_A_DM3
DDR_A_D2	17	DO2	DDR_A_DM4	147	DDR_A_DM4
DDR_A_D3	19	DO3	DDR_A_DM5	165	DDR_A_DM5
DDR_A_D4	4	DO4	DDR_A_DM6	185	DDR_A_DM6
DDR_A_D5	6	DO5	DDR_A_DM7	205	DDR_A_DM7
DDR_A_D6	14	DO6	M_CLK_DDR0	30	M_CLK_DDR0
DDR_A_D7	16	DO7	M_CLK_DDR#0	32	M_CLK_DDR#0
DDR_A_D8	23	DO8	M_CLK_DDR#0	164	M_CLK_DDR#1
DDR_A_D9	25	DO9	M_CLK_DDR#1	166	M_CLK_DDR#1
DDR_A_D10	35	DO10			
DDR_A_D11	37	DO11			
DDR_A_D12	20	DO12			
DDR_A_D13	22	DO13			
DDR_A_D14	36	DO14			
DDR_A_D15	38	DO15			
DDR_A_D16	43	DO16			
DDR_A_D17	45	DO17			
DDR_A_D18	55	DO18			
DDR_A_D19	57	DO19			
DDR_A_D20	44	DO20			
DDR_A_D21	46	DO21			
DDR_A_D22	56	DO22			
DDR_A_D23	58	DO23			
DDR_A_D24	61	DO24			
DDR_A_D25	63	DO25			
DDR_A_D26	73	DO26			
DDR_A_D27	75	DO27			
DDR_A_D28	64	DO28			
DDR_A_D29	64	DO29			
DDR_A_D30	74	DO30			
DDR_A_D31	76	DO31			
DDR_A_D32	123	DO32			
DDR_A_D33	125	DO33			
DDR_A_D34	135	DO34			
DDR_A_D35	137	DO35			
DDR_A_D36	124	DO36			
DDR_A_D37	126	DO37			
DDR_A_D38	134	DO38			
DDR_A_D39	136	DO39			
DDR_A_D40	141	DO40			
DDR_A_D41	143	DO41			
DDR_A_D42	151	DO42			
DDR_A_D43	153	DO43			
DDR_A_D44	140	DO44			
DDR_A_D45	142	DO45			
DDR_A_D46	152	DO46			
DDR_A_D47	154	DO47			
DDR_A_D48	157	DO48			
DDR_A_D49	159	DO49			
DDR_A_D50	173	DO50			
DDR_A_D51	175	DO51			
DDR_A_D52	158	DO52			
DDR_A_D53	160	DO53			
DDR_A_D54	174	DO54			
DDR_A_D55	176	DO55			
DDR_A_D56	179	DO56			
DDR_A_D57	181	DO57			
DDR_A_D58	189	DO58			
DDR_A_D59	191	DO59			
DDR_A_D60	180	DO60			
DDR_A_D61	182	DO61			
DDR_A_D62	182	DO62			
DDR_A_D63	184	DO63			
PM_EXTTS#0	50	NC#50			
	59	NC#59			
	83	NC#83			
	120	NC#120			
	163	NC#163			
DDR_CS0_DIMMA#	110	CS0#			
DDR_CS1_DIMMA#	115	CS1#			
DDR_CKE0_DIMMA	70	CKE0			
DDR_CKE1_DIMMA	80	CKE1			
DDR_A_RAS#	108	RAS#			
DDR_A_CAS#	113	CAS#			
DDR_A_WE#	109	WE#			
ICH_SMBCLK	197	SCL			
ICH_SMBDATA	195	SDA			
M_ODT0	114	ODT0			
M_ODT1	119	ODT1			
VREF	1	VREF			
GND	201	GND			
GND	202	GND			

Main Source: 62.10017.E31
2nd Source: 62.10017.A41



SB:0707 For EMI request

put near connector

3D3V_S0

1D8V_S3

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

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SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

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SCD2U16V2ZY-2GP

SCD1U16V2ZY-2GP

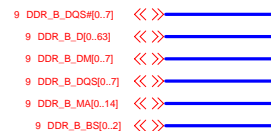
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SCD1U16V2ZY-2GP

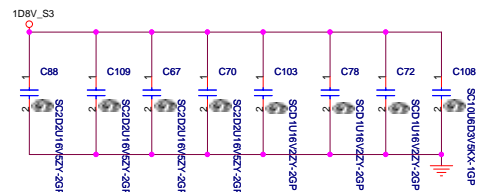
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SCD1U16V2ZY-2GP

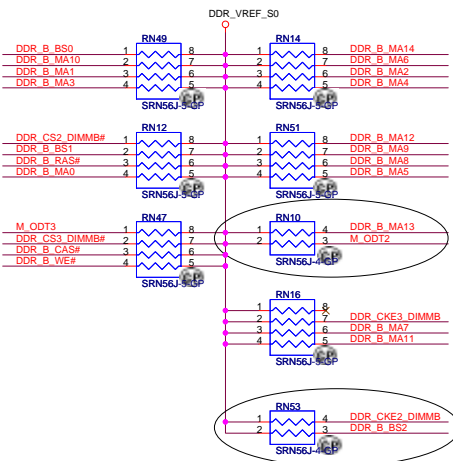
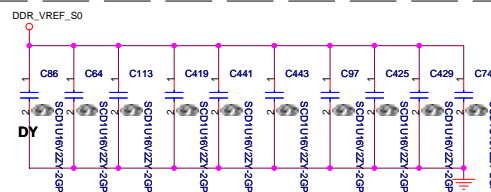
SCD2U16V2ZY-2GP



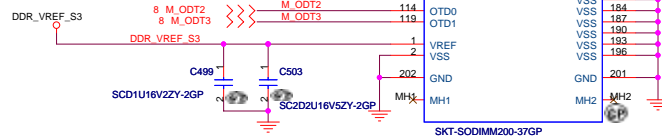
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"



Main Source:62.10017.E21
2nd Source: 62.10017.A51

DM1

DDR B MA0102A0

DDR B MA1101A1

DDR B MA2100A2

DDR B MA399A3

DDR B MA498A4

DDR B MA597A5

DDR B MA696A6

DDR B MA795A7

DDR B MA894A8

DDR B MA993A9

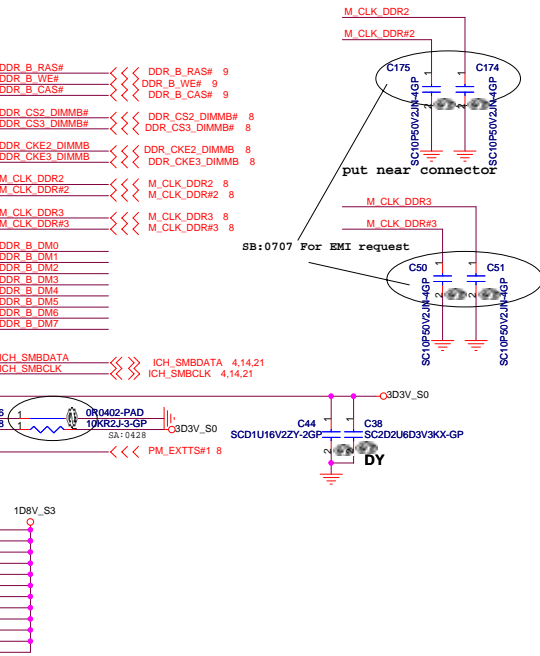
DDR B MA10105Q/A#

DDR B MA1190A10

DDR B MA1291A11

DDR B MA13116A12

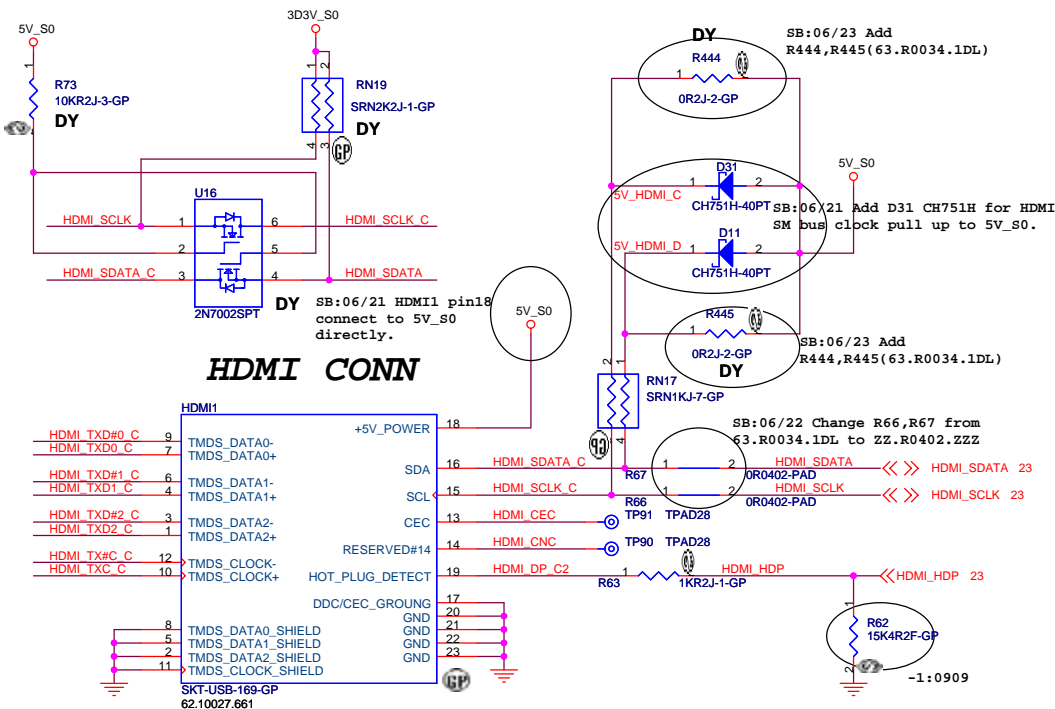
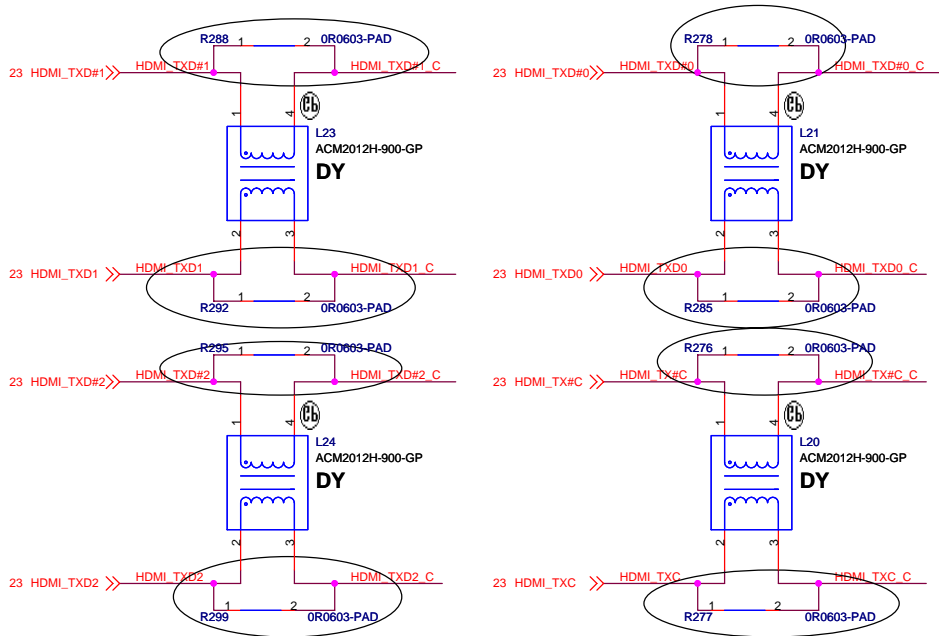
DDR B MA1486A13



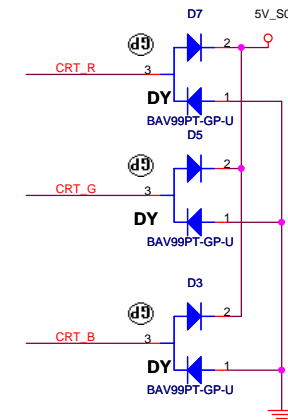
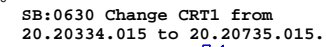
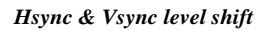
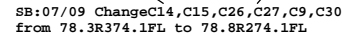
put near connector

SB:0707 For EMI request

HDMI I/F & CONNECTOR

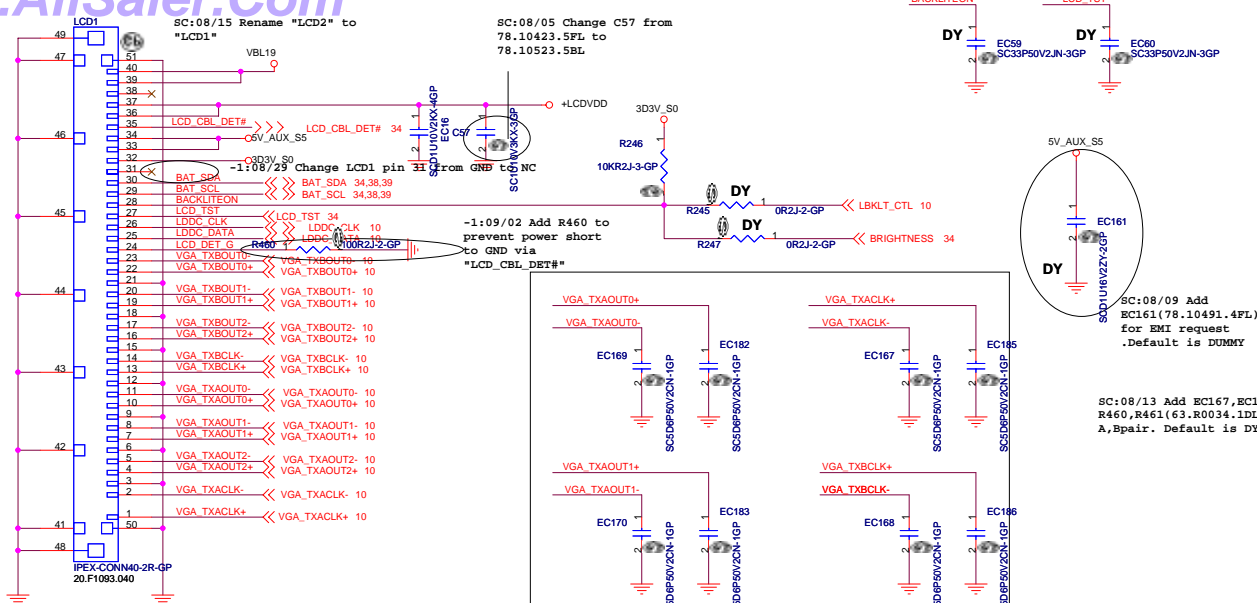


TV OUT CONN (Optional) Move to Right I/O Board



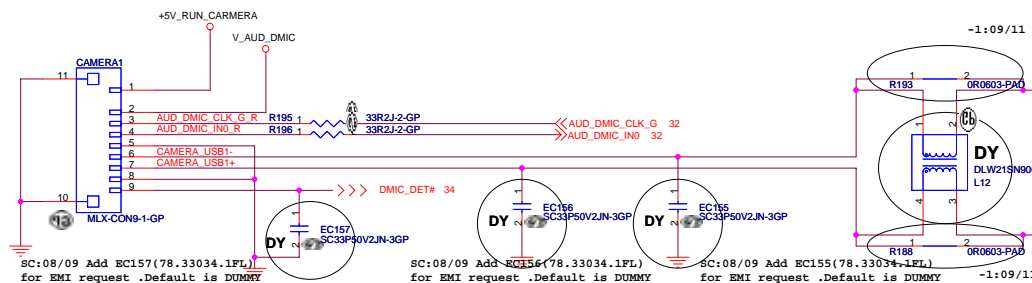
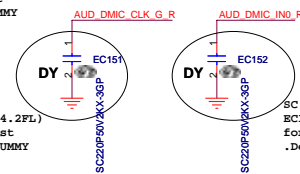
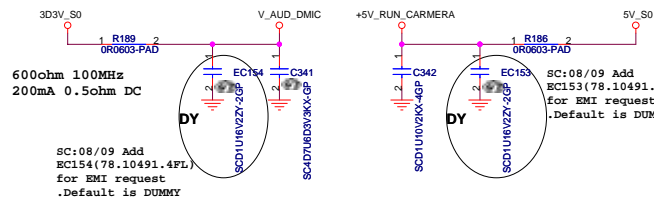
Sheet 17 of 47

SC:08/09 Add LCD2 (20.F1093.040), please check LCD1 and LCD 2 layout overlap possibility.

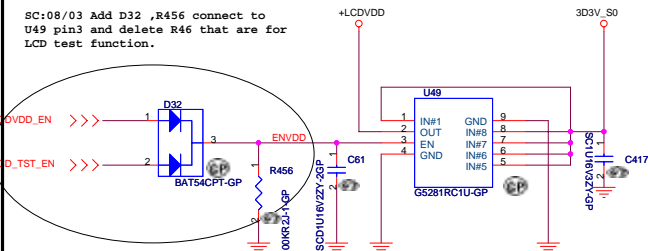
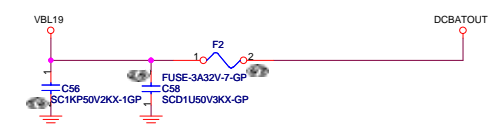


Mic Power

CAMERA Power



INVERTER POWER

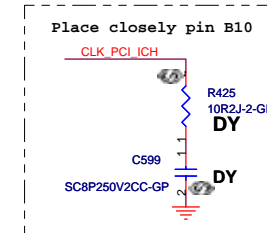
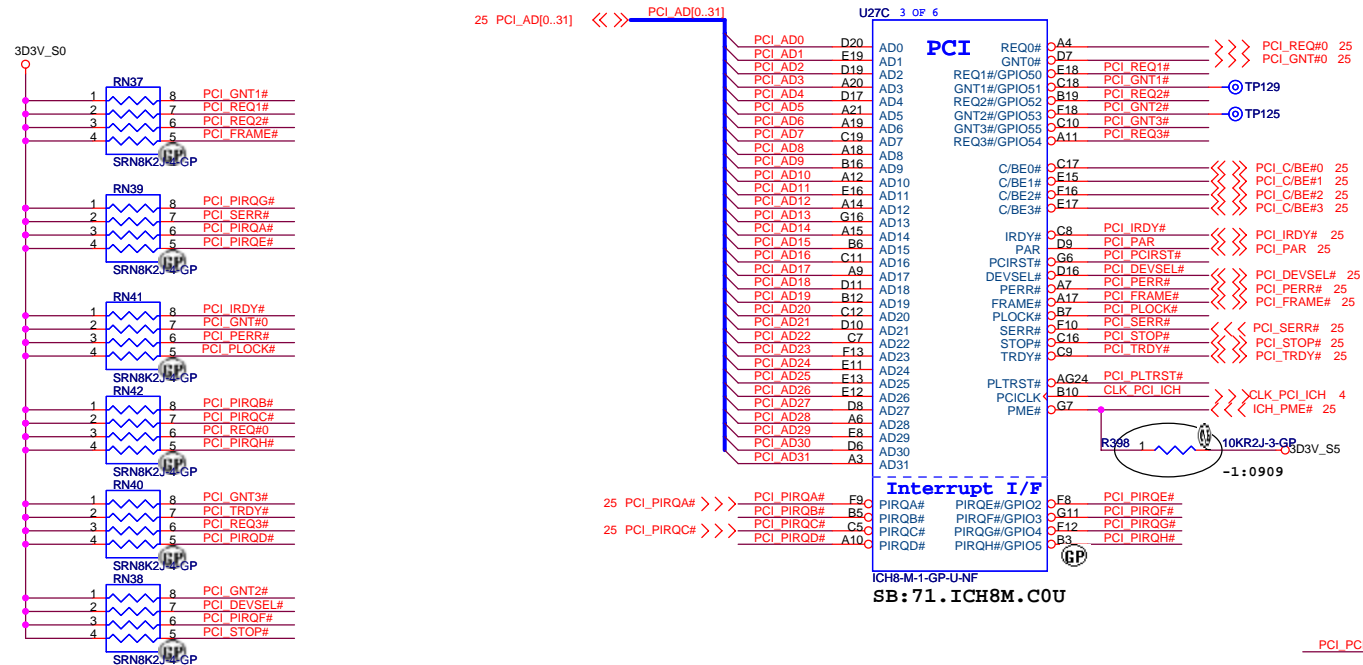


LCD POWER

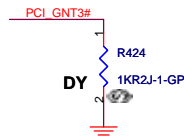
<Core Design>

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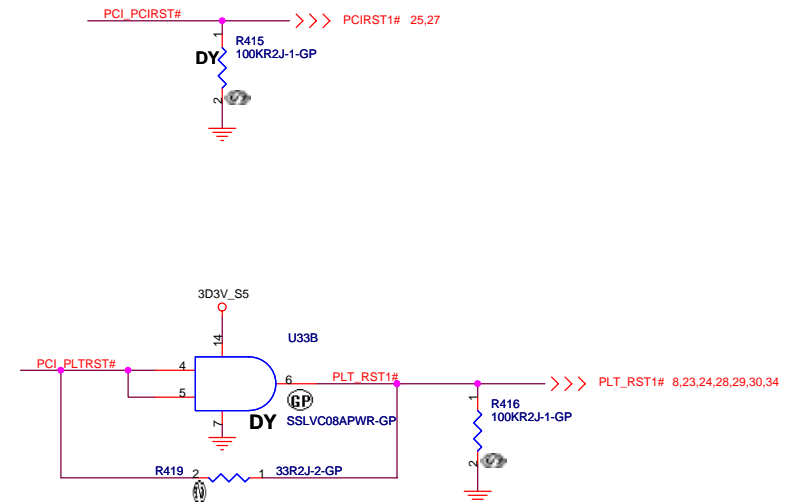
Title			LCD/Inverter Connector
Size	Document Number		DS2-Intel
Custom			Rev -1
Date: Wednesday, September 12, 2007			Sheet 18 of 47

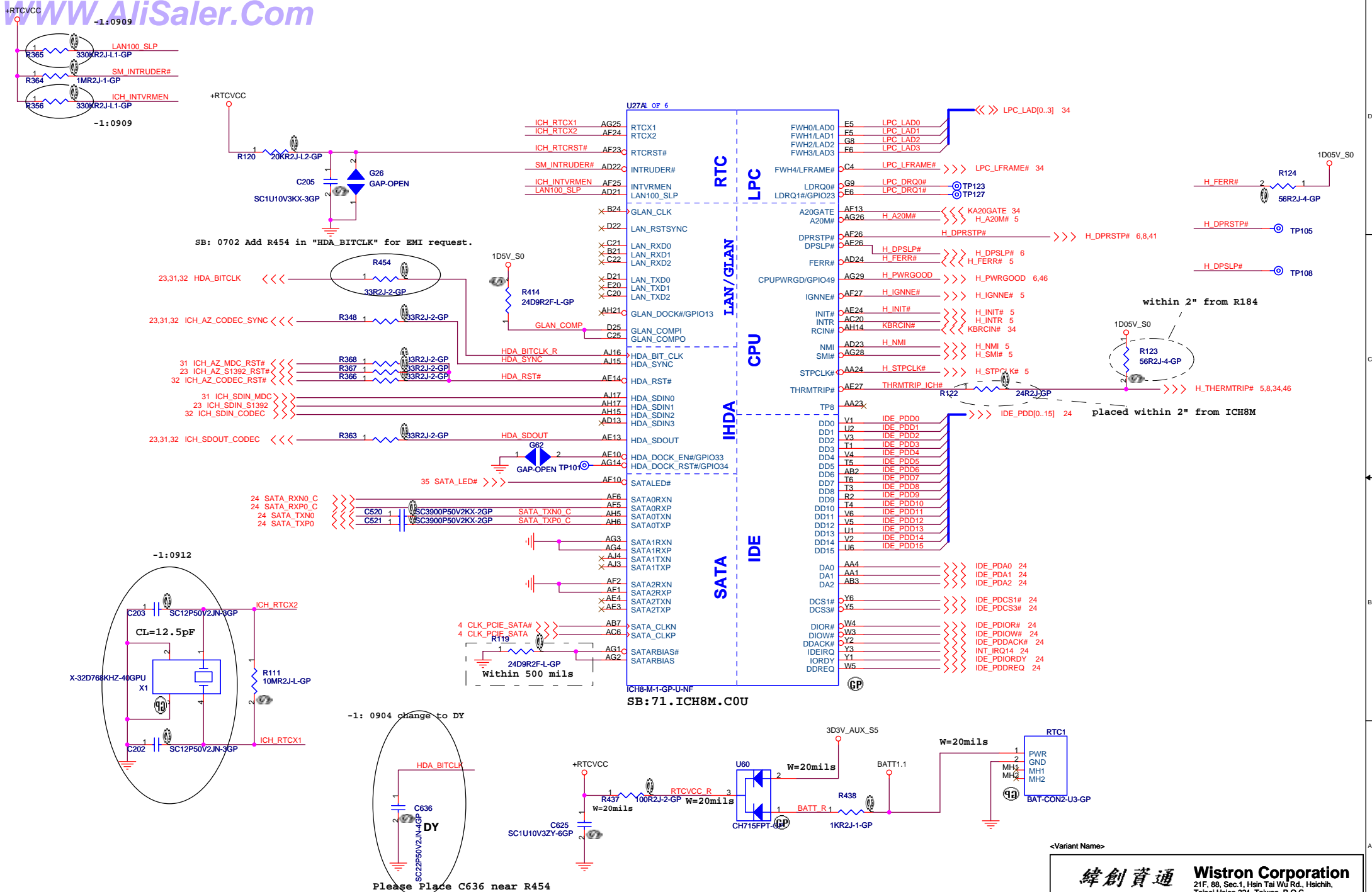


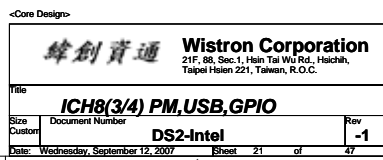
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

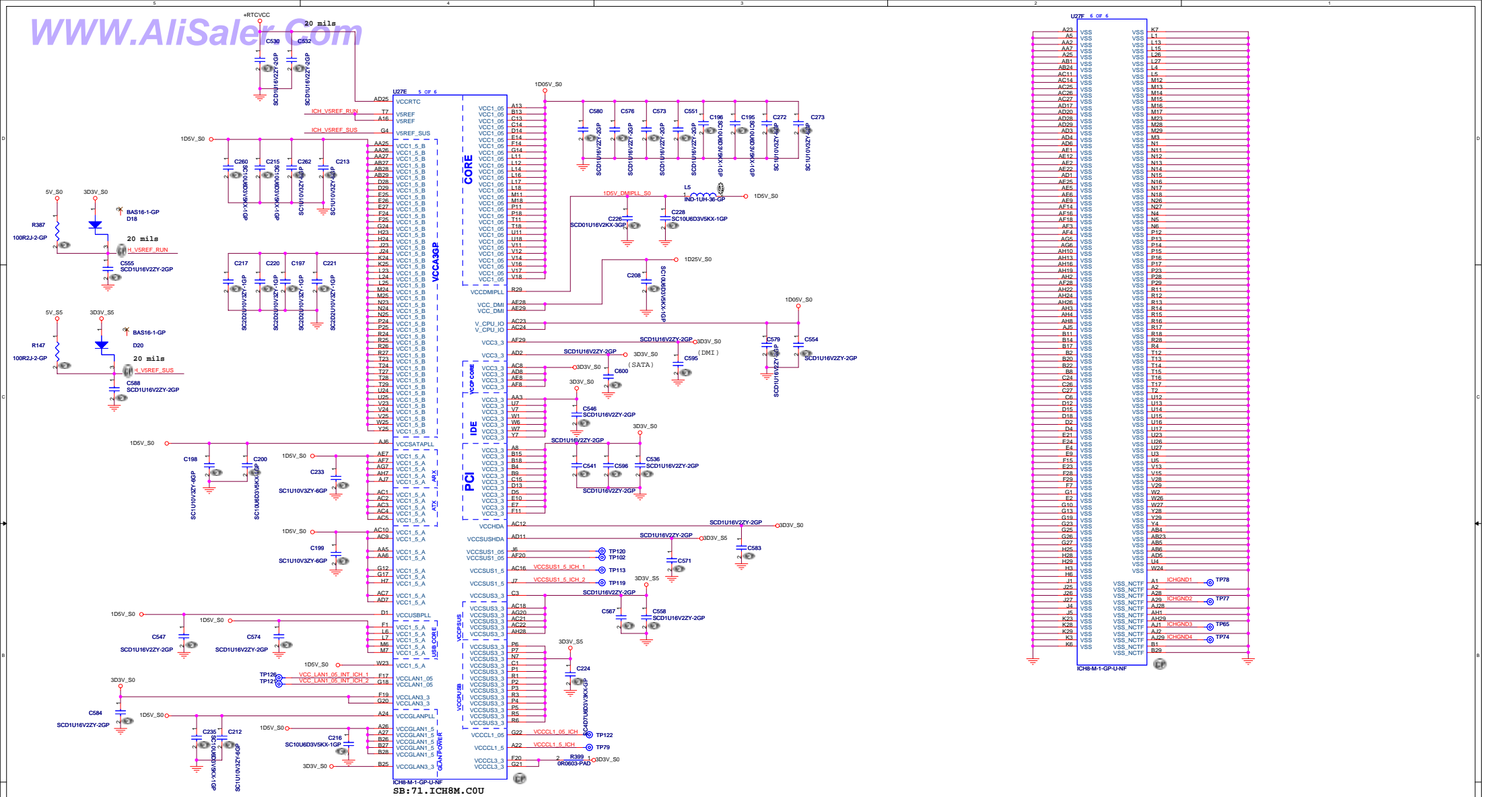


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



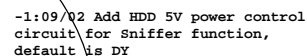
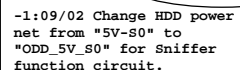




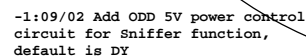


~Variant Name~





```
-1:09/02 Change ODD power
net from "5V-S0" to
"ODD_5V_S0" for Sniffer
function circuit.
```



-1:0906 Add C639 for
"ODD 5V EN#"

<Core Design>

緯創資通

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Title	Author	Year	Journal	Volume	Page

HD/CDROM/USB

Size

Document Number

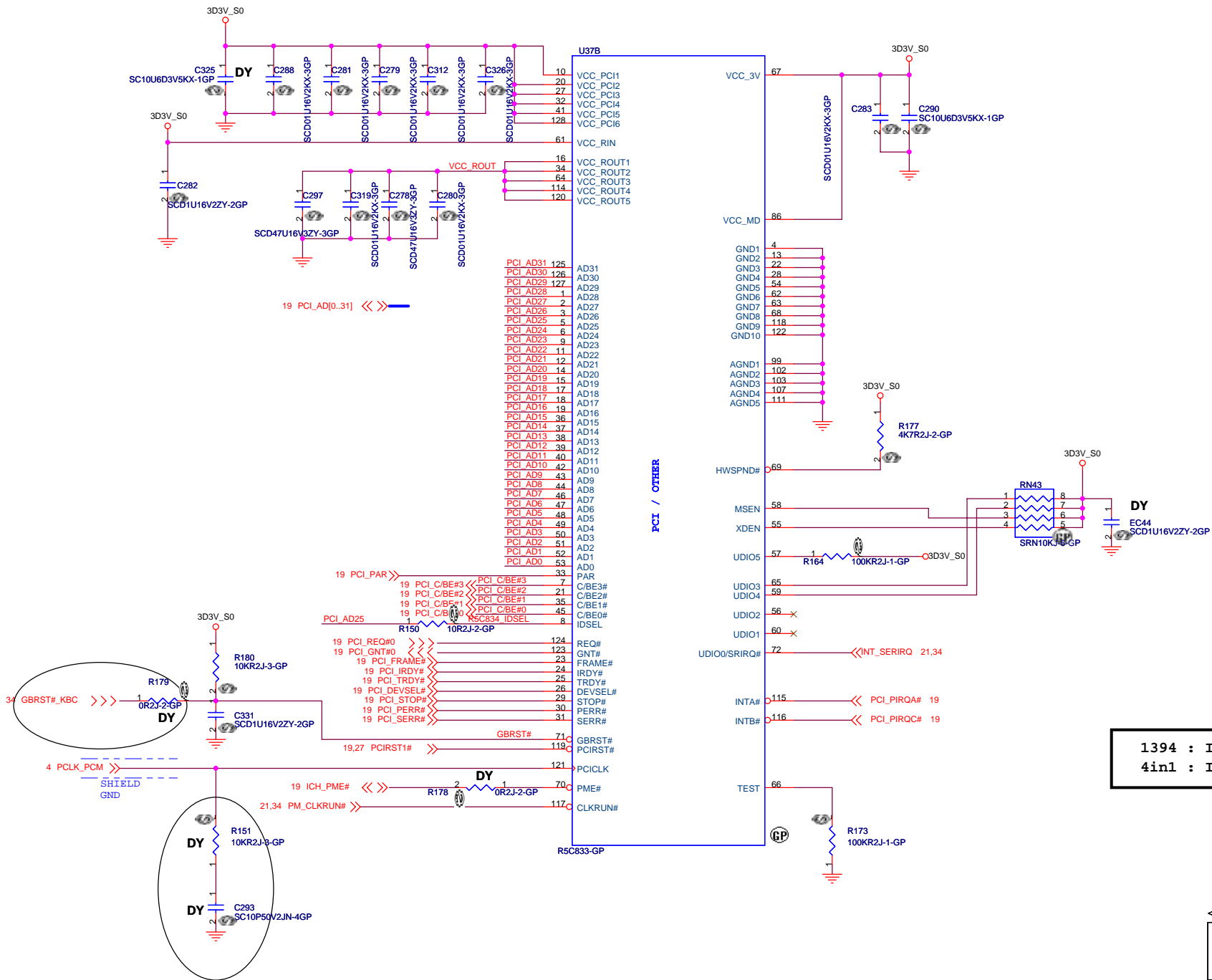
DS2-Intel

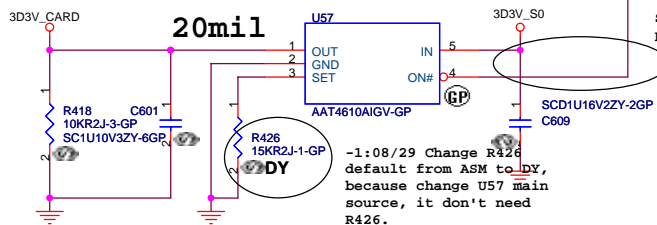
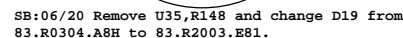
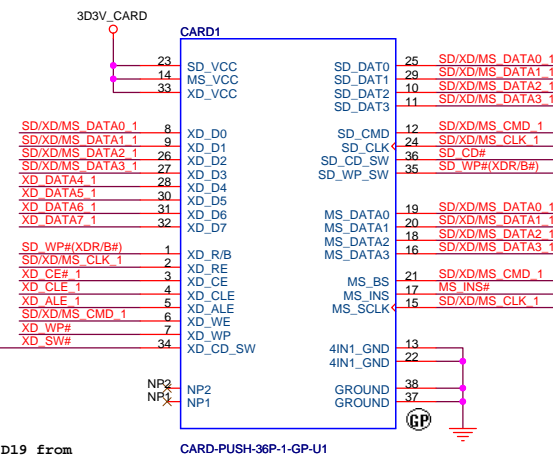
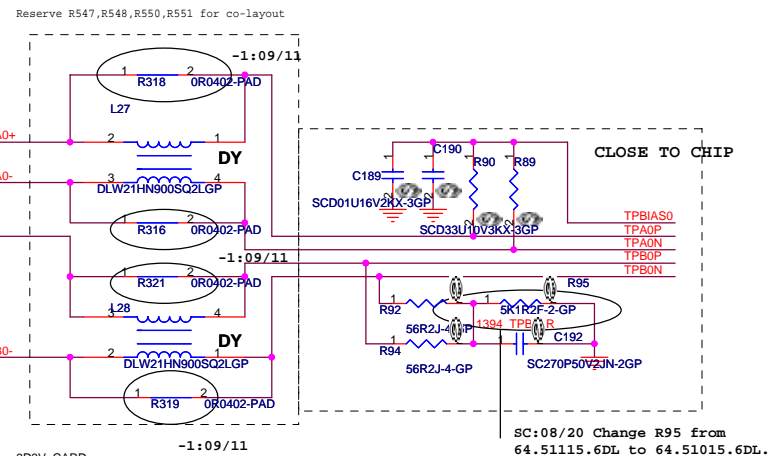
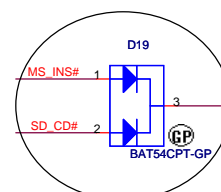
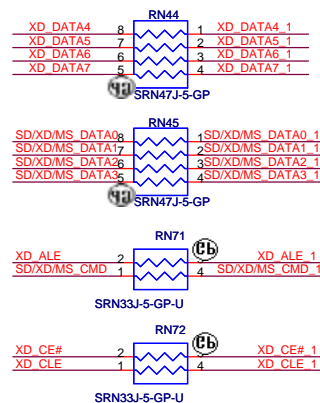
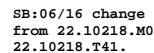
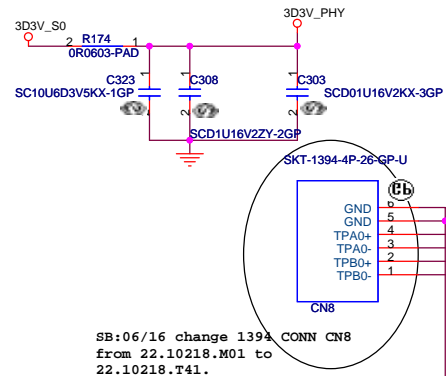
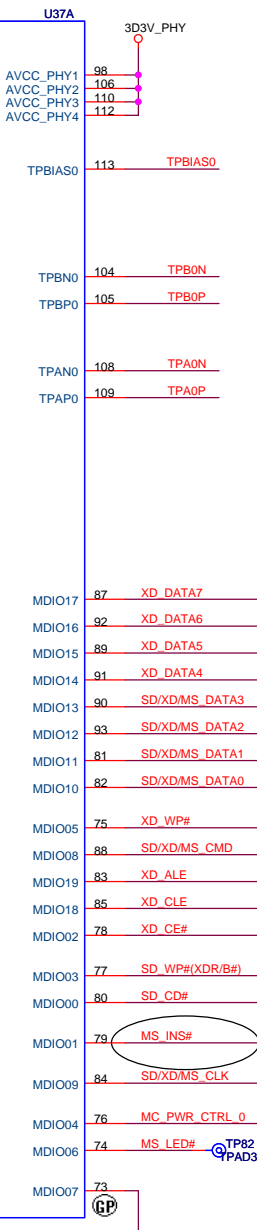
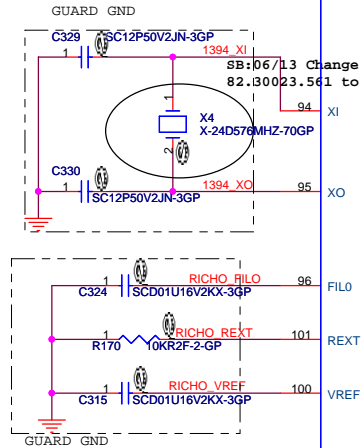
-1

Date: Wednesday, September 12, 2007

Sheet

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For SD Card Power

SB:06/20 Remove R427 and change U57
pin4 connect to "MC_PWR_CTRL_0"

	R426
AAT4610AIGV	15K
RT9711DPBG	DY
G5240D2T1U	DY

-1:08/29 Change R426
default from ASM to LD,
because change U57 main
source, it don't need
R426.

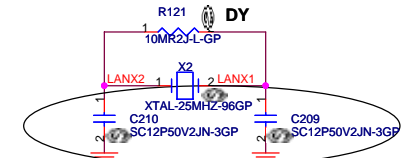
<Core Design>

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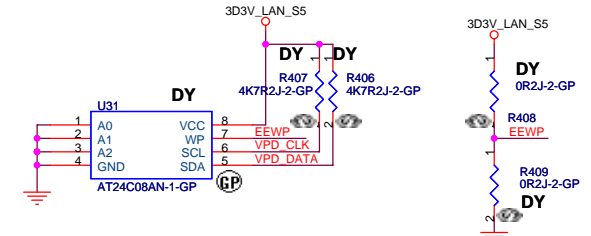
Title			
R5C832/IEEE1394/SD			
Size A3	Document Number		Rev
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	R394	R354	R357	R362	R372	R377	C528	C544
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

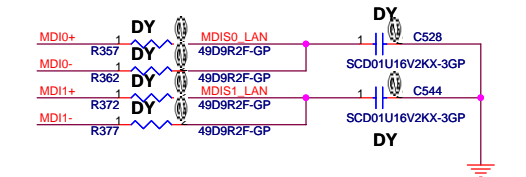
Note:Default is 88E8040



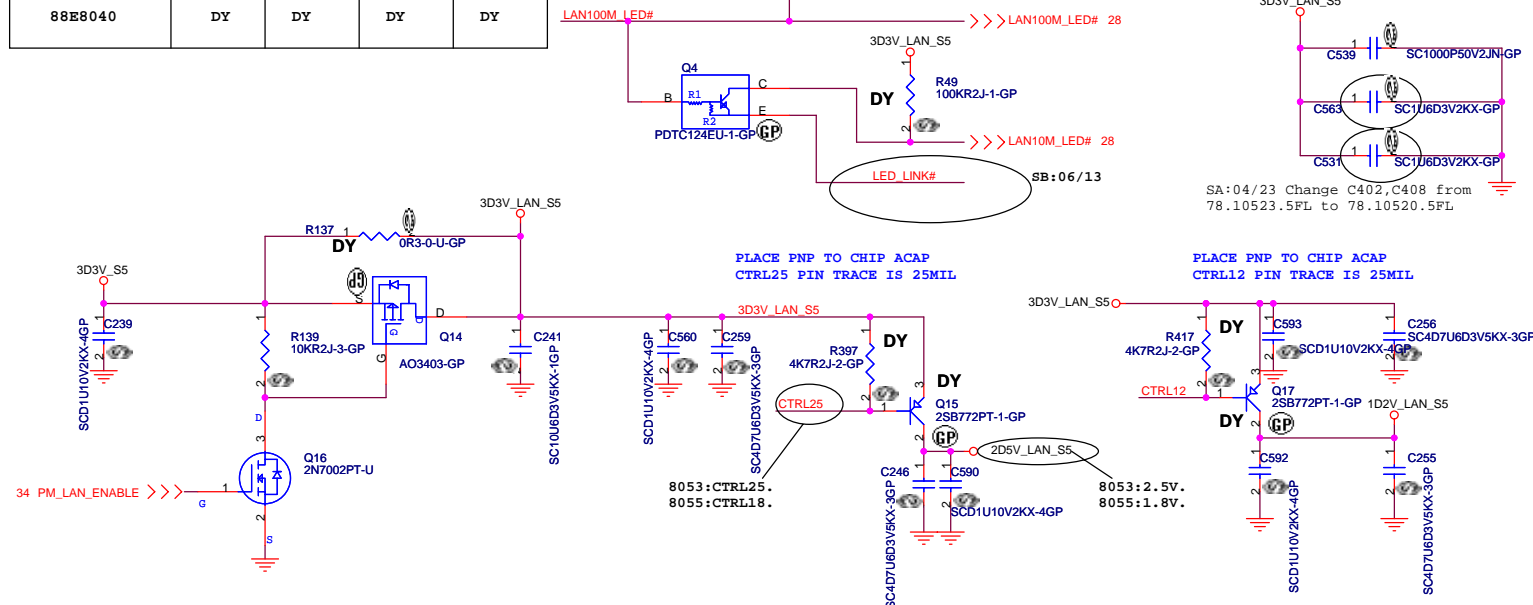
SB:06/13 Change C209,C210 from 27P to 12P



Pull up for AT24C08 another pull low



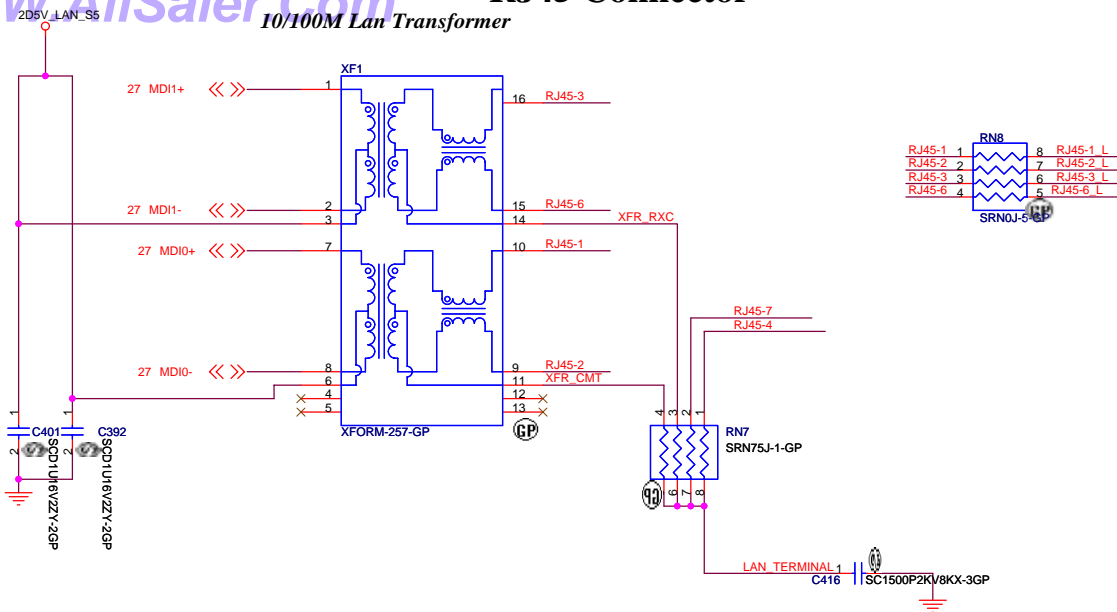
	R397	Q15	R417	Q17
88E8039	4K7	2SB772PT	4K7	2SB772PT
88E8040	DY	DY	DY	DY



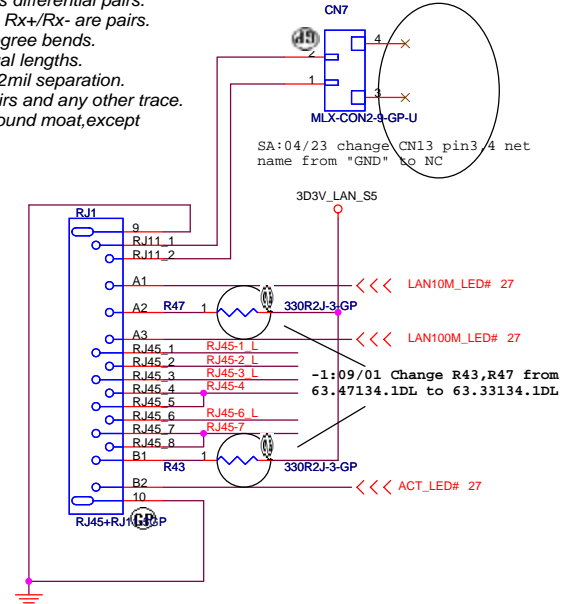
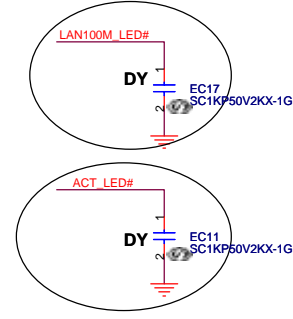
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
LAN MARVELL			
Size A3	Document Number		Rev
	DS2-Intel		-1
Date:	Wednesday, September 12, 2007	Sheet 27 of 47	



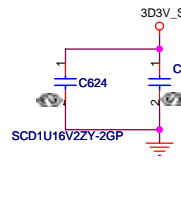
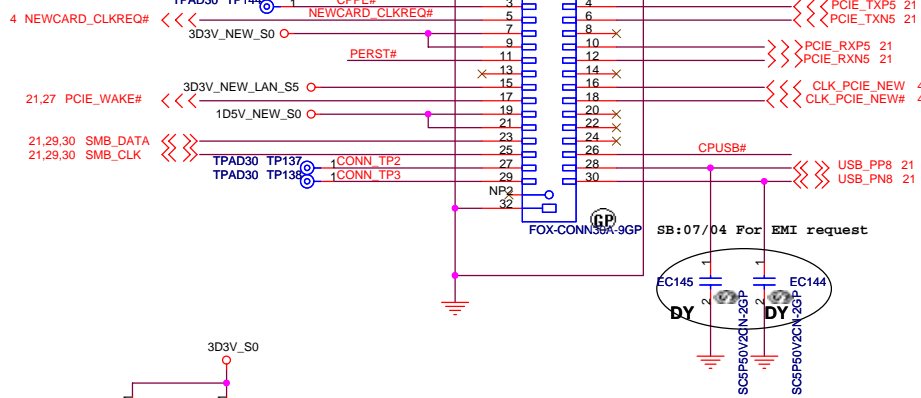
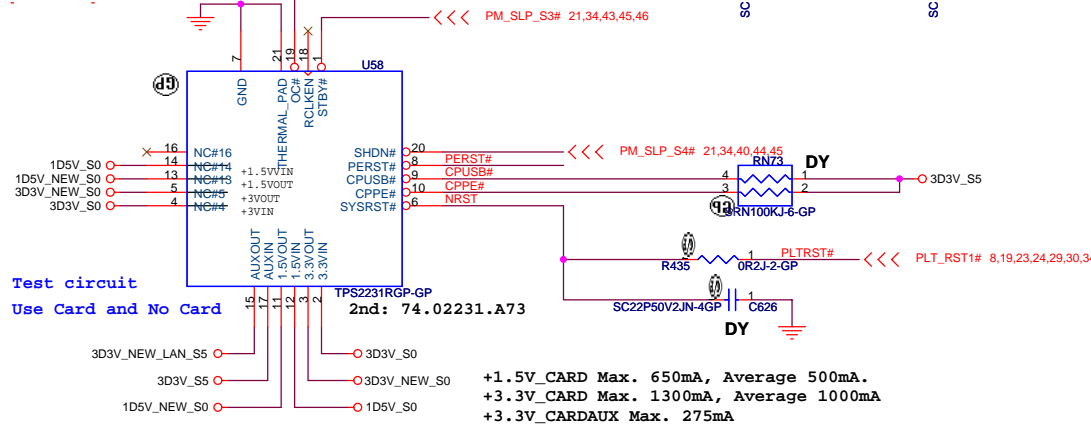
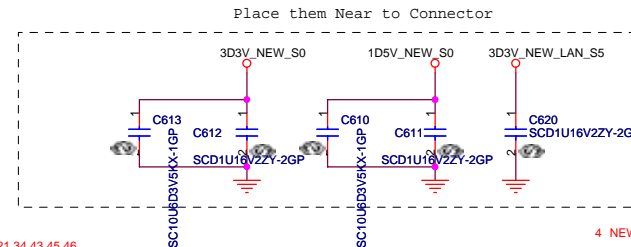
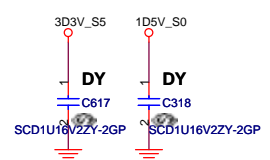
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



Green : Link up
Blinking : TX/RX activity

NEWCARD Connector

Place them Near to Chip



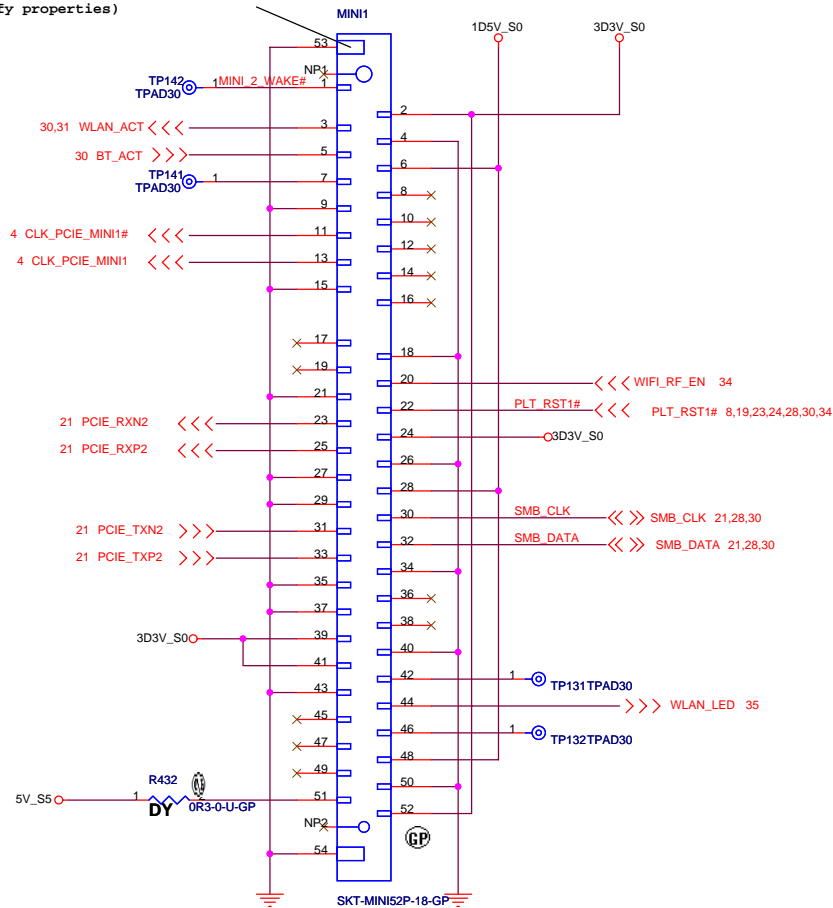
<Core Design>

緯創資通 Wistron Corporation
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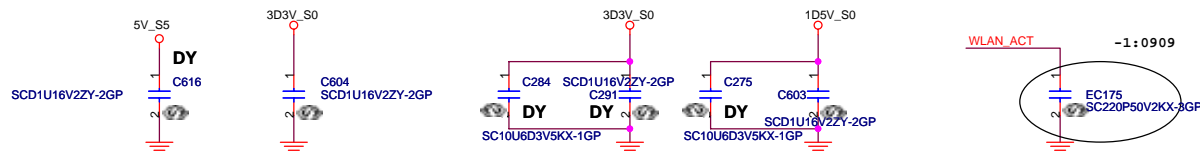
Title		
LAN connector/NEW CARD/SIM		
Size	Document Number	Rev
A3	DS2-Intel	-1
Date: Wednesday, September 12, 2007		
Sheet 26 of 47		

Mini Card Connector 1(802.11a/b/g)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)

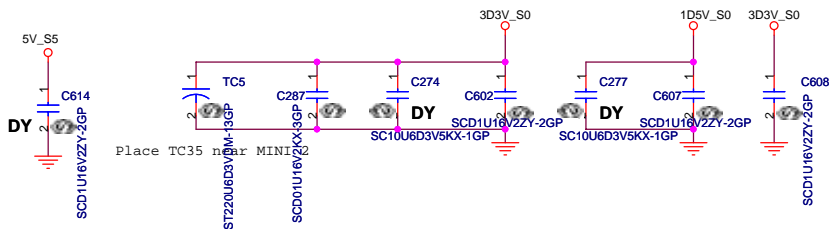


Main Source:62.10043.431
2nd Source: 20.F0992.052

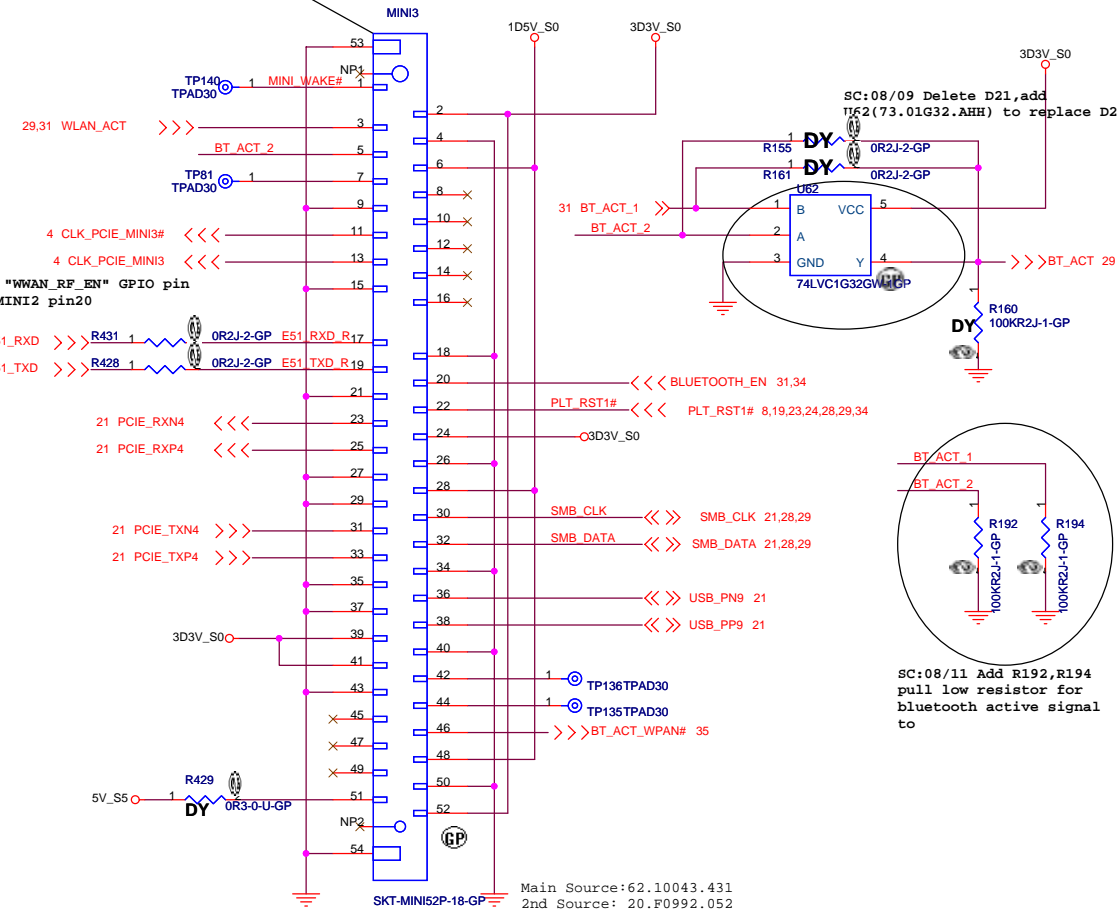


<Core Design>			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINI CARD CONN 1			
Size	Document Number	Rev	
A3	DS2-Intel	-1	
Date:	Wednesday, September 12, 2007	Sheet	29 of 47

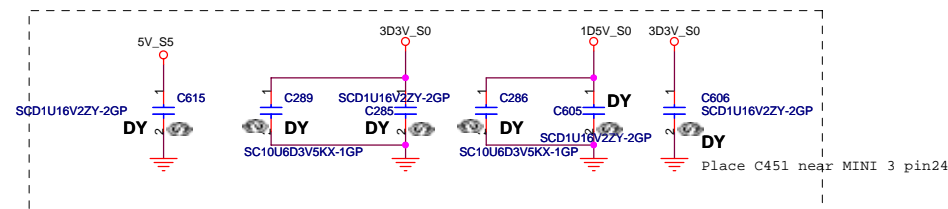
SB:06/22 Change MINI1,2,3 slot from
62.10043.431 to 62.10043.551(only
modify properties)



```
SB:06/22 Change MINI1,2,3 slot from
62.10043.431 to 62.10043.551(only
modify properties)
```

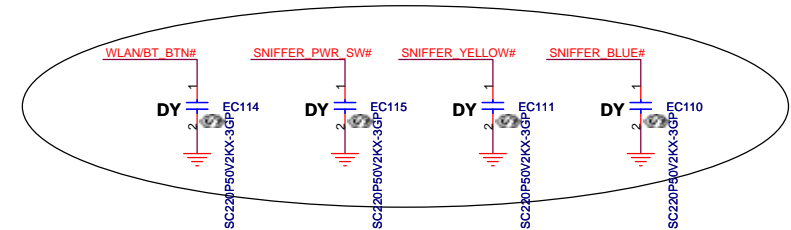
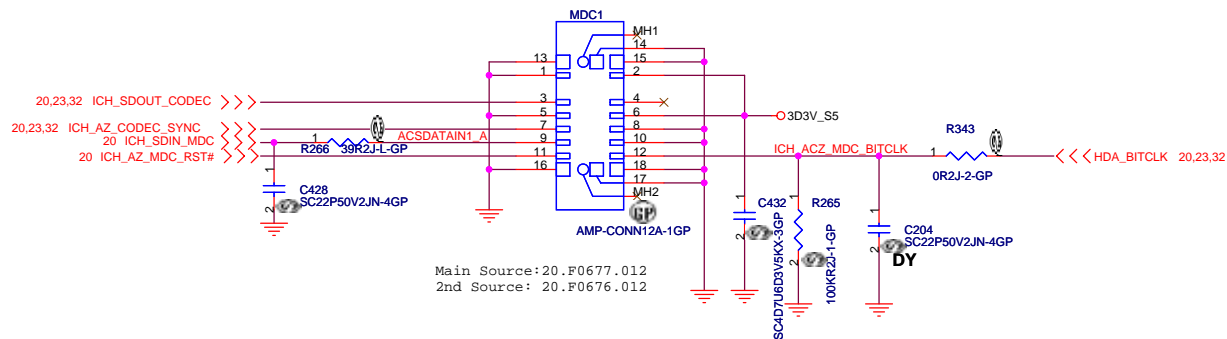
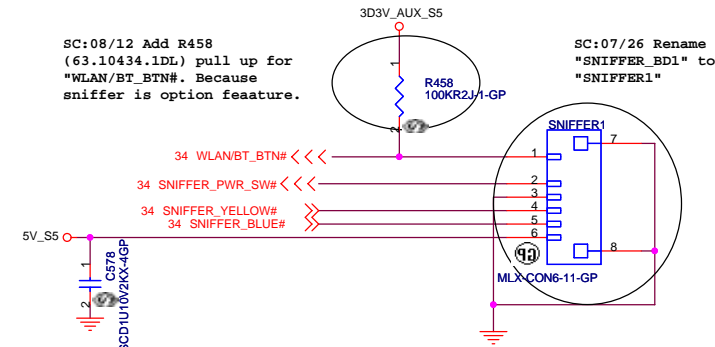
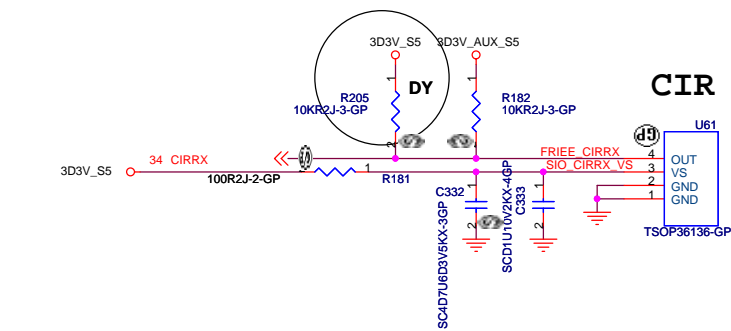


SC:08/11 Add R192,R194
pull low resistor for
bluetooth active signal
to

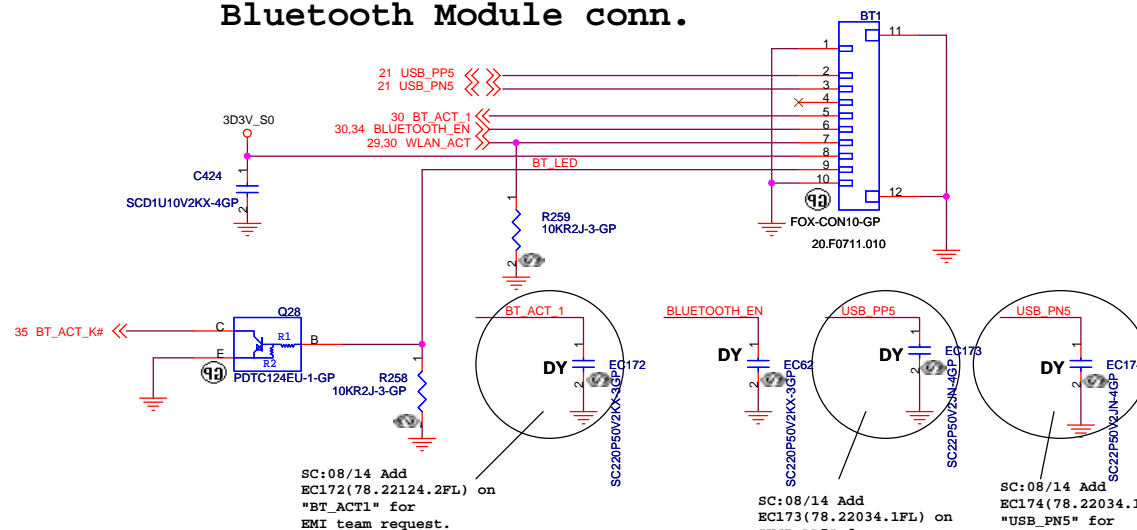


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Title			
MINI CARD CONN 2 & 3			
Size A3	Document Number		Rev
	DS2-Intel		-1
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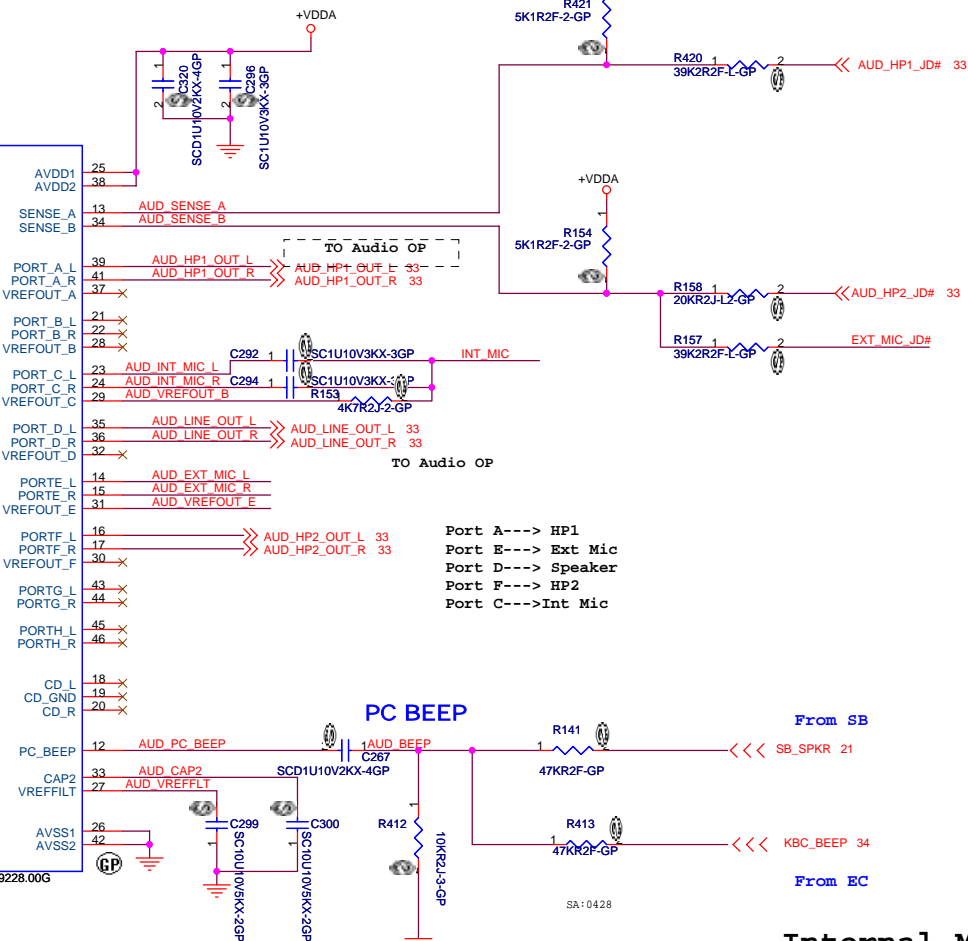
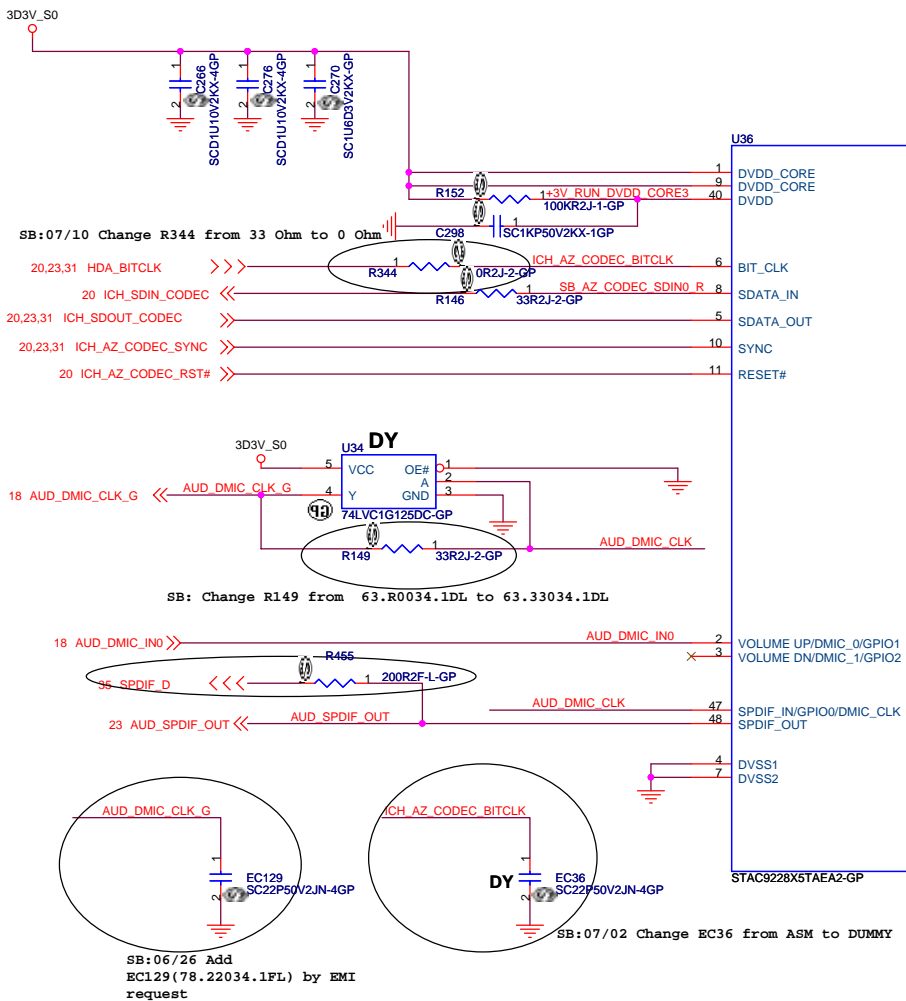


Bluetooth Module conn.



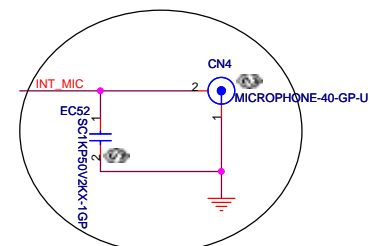
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Title			
MDC&RJ11 CONN			
Size	Document Number		Rev
A3			-1
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Internal Microphone

-1:09/06 Change Int. MIC from 23.42132.001 to 23.42143.001

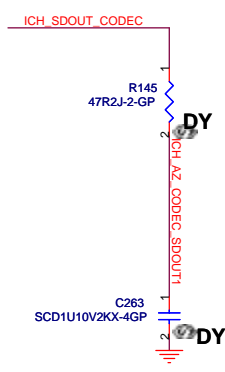


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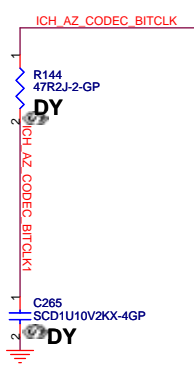
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			AUDIO CODEC STAC9228		
Size	Document Number	DS2-Intel			Rev
A3					-1
Date: Wednesday, September 12, 2007			Sheet 32 of 47		

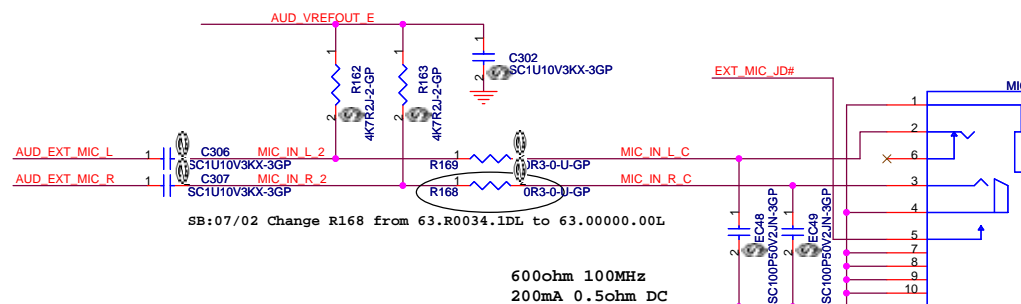
Azalia I/F EMI



Azalia I/F EMI

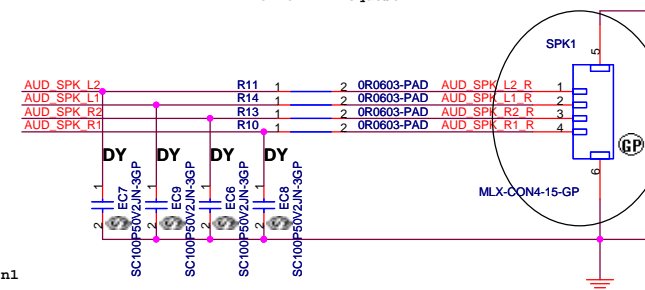


MIC IN

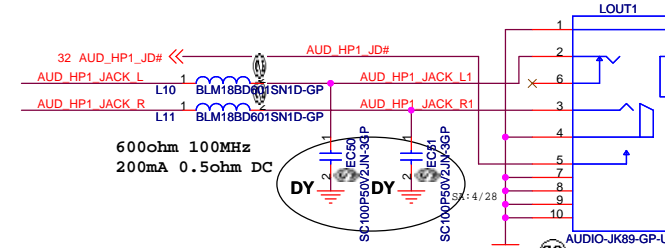


Speaker

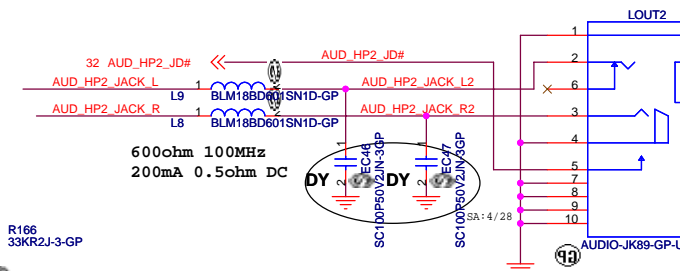
SC:08/11 Change SPK1 pin define that follow ME request



LINE1 OUT



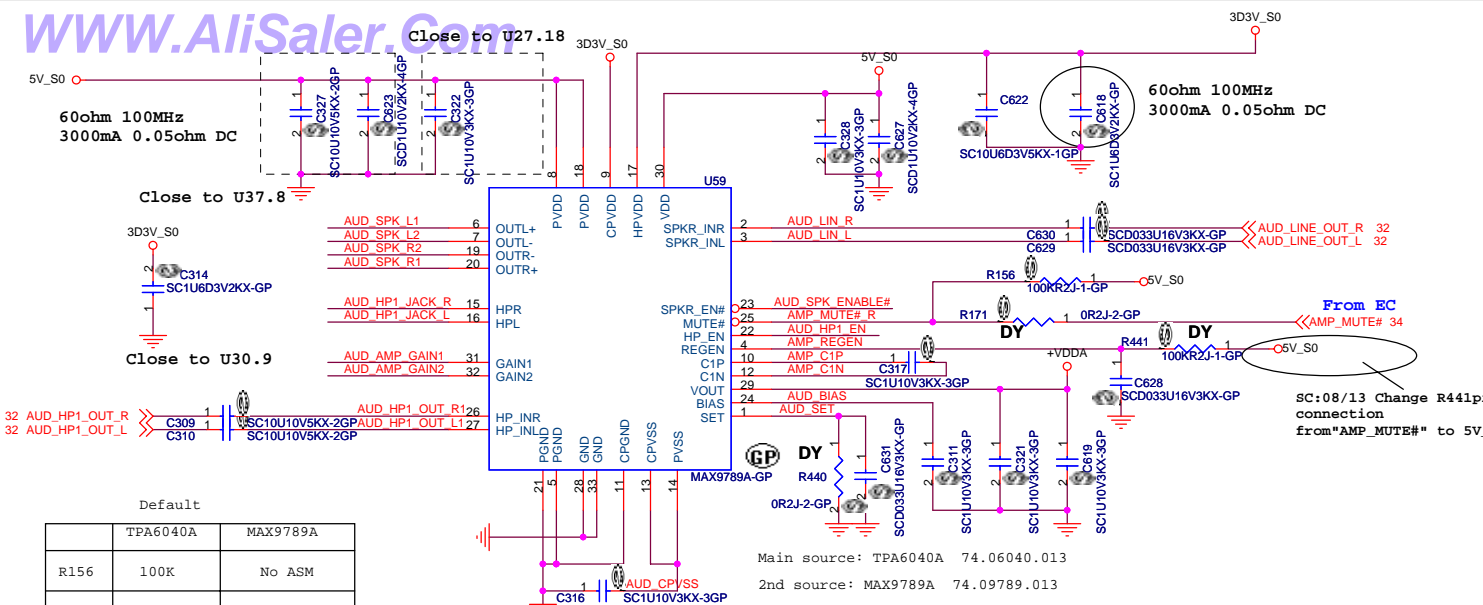
LINE2 OUT



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

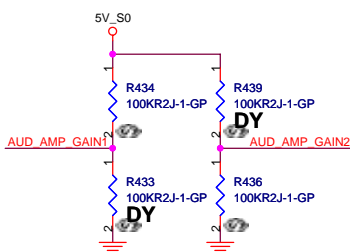
Title			AUDIO AMP/SPEAKER
Size	Document Number	Rev	
A3		DS2-Intel	
Date: Wednesday, September 12, 2007		Sheet	33 of 47



Default

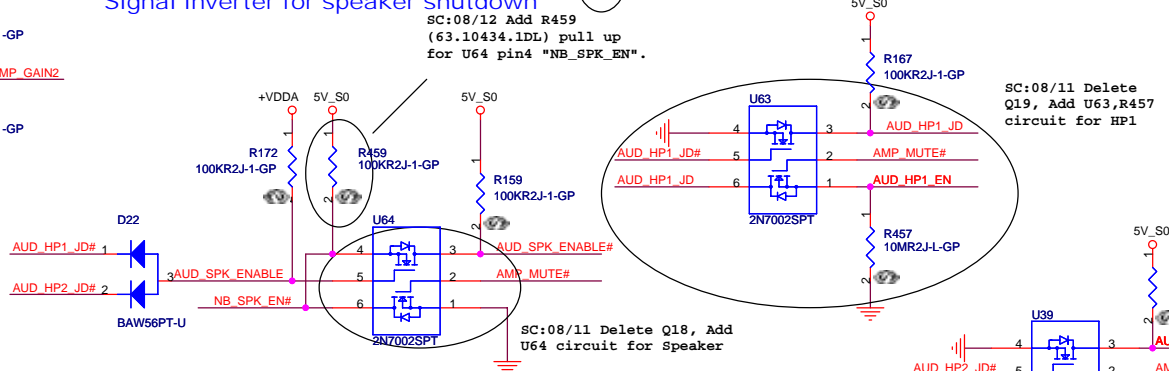
	TPA6040A	MAX9789A
R156	100K	No ASM
R171	No ASM	0 Ohm
R440	No ASM	0 Ohm
R441	No ASM	100K
C631	0.33uF	No ASM
C628	0.33uF	No ASM

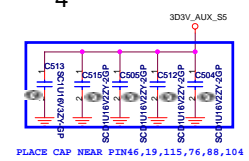
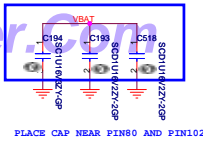
GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



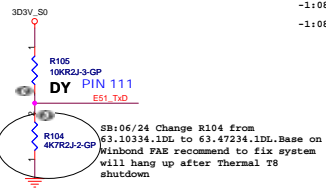


WPC8763L STRAP PIN

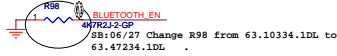
JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	NO PD	GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE
Forces the device to float all its output and I/O pins,if an external 10 K Ω pull-down resistor is connected.

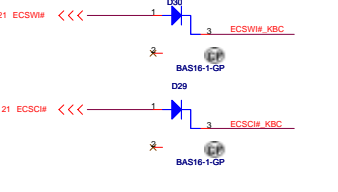
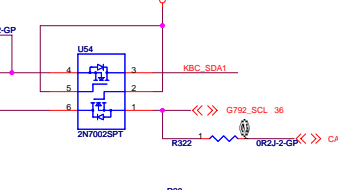
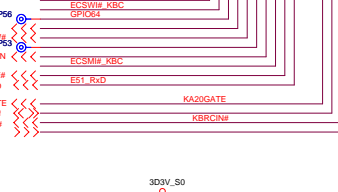
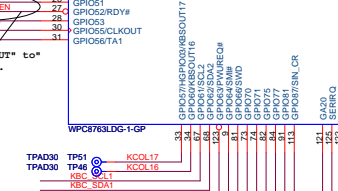
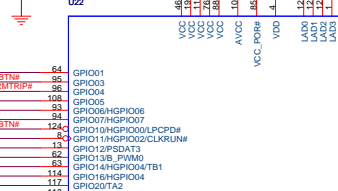
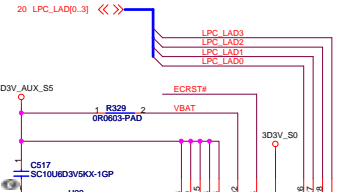
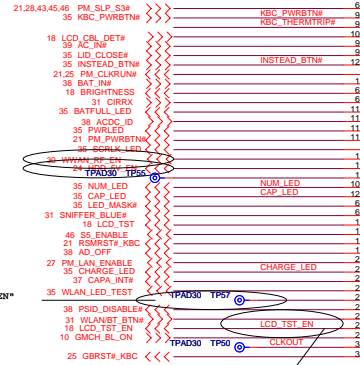
BADDR1-0 (PIN 111, 112) I/O Base Address.
10K Ω external pull-down resistor on BADDR1: Core defined

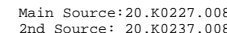


SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.

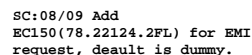
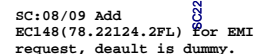


-1:08/30 Change Pin10 from NC to be "WAN_RF_EN"
-1:08/30 Change Pin11 from NC to be "BDD_5V_EN"
-1: 08/29 change Pin24 from "WAN_RF_EN" to NC, because pin24 is H/W strapping pin. it has H/W concern.

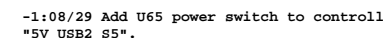




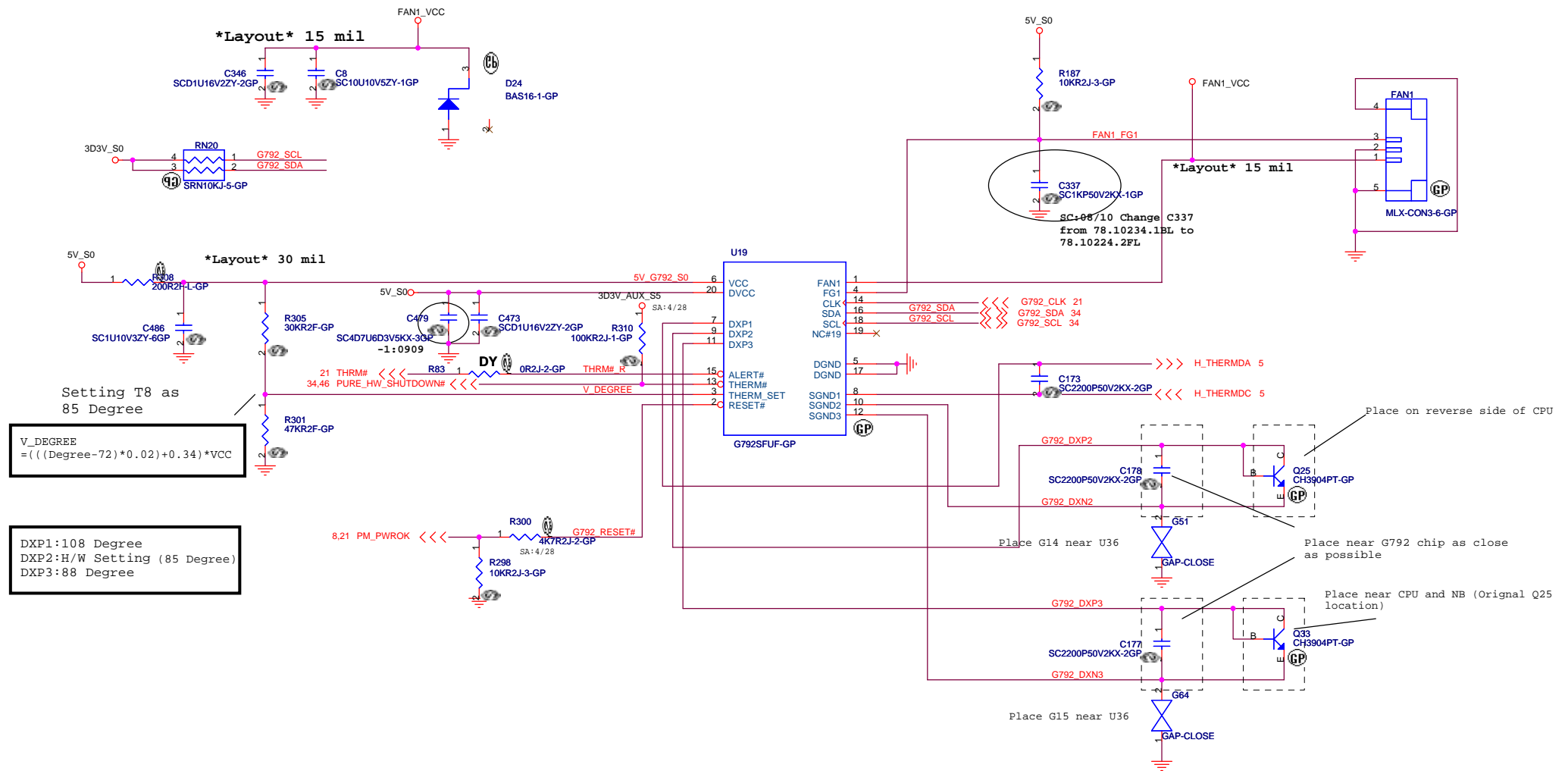
-1:09/02 Change CN3(LED Board) pin assignment.



```
-1:08/29 Rename CN6
pin2,pin4 power net  become
"5V USB2 S5".
```

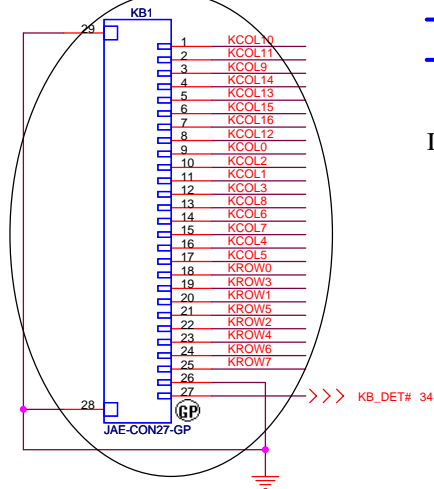


Title			
<i>FWH and Board to Board CONN</i>			
Size A3	Document Number	Rev	
	DS2-Intel		-1
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<Core Design>

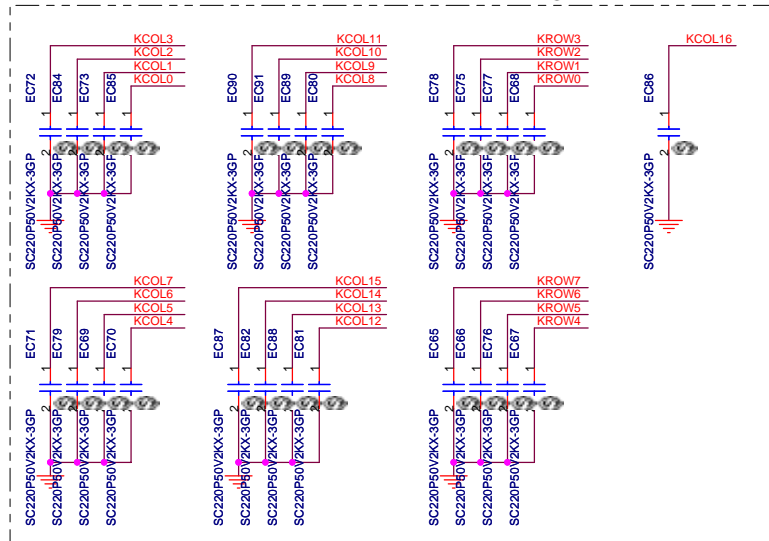
SB:06/27 Change K/B connector from 20.F0694.025 to 20.K0291.027



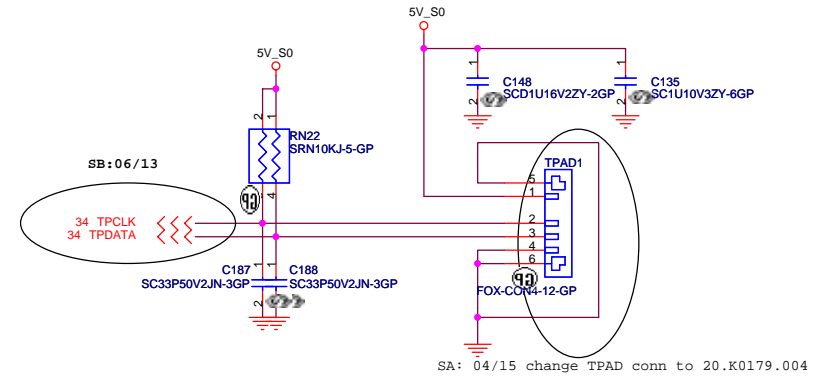
<<< KROW[0..7] 34
>>> KCOL[0..16] 34

Internal Keyboard Connector

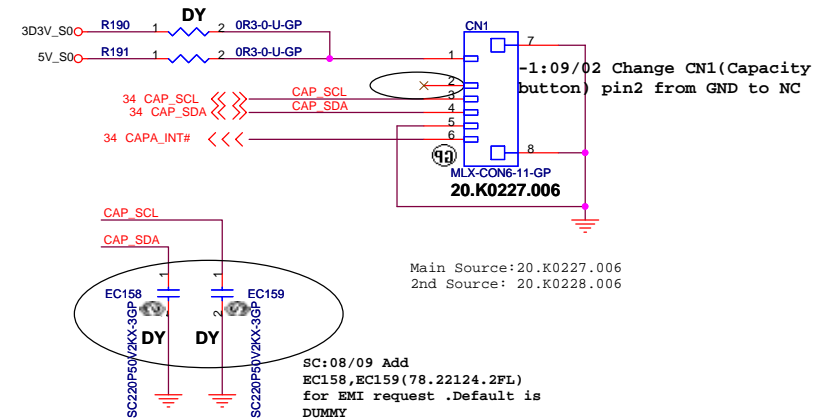
for EMI



TouchPad Connector



CAPACITY BUTTON



<Core Design>

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Title

KeyBoard-CONN

Size
A3

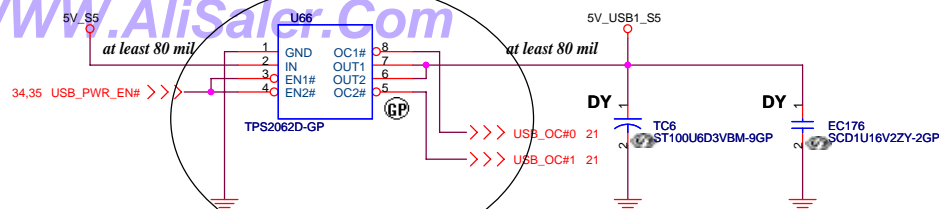
Document Number

DS2-Intel

Rev
-1

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Sheet 37 of 47



-1:08/30 Add U66 power switch to control USB power

SB: 06/27 Change CN5 from 20.F1089.028 to 20.F1134.024

Left I/O Connector

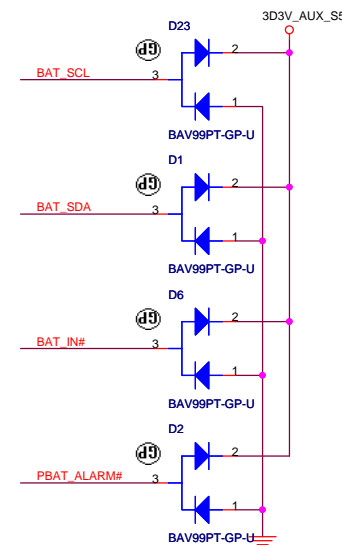
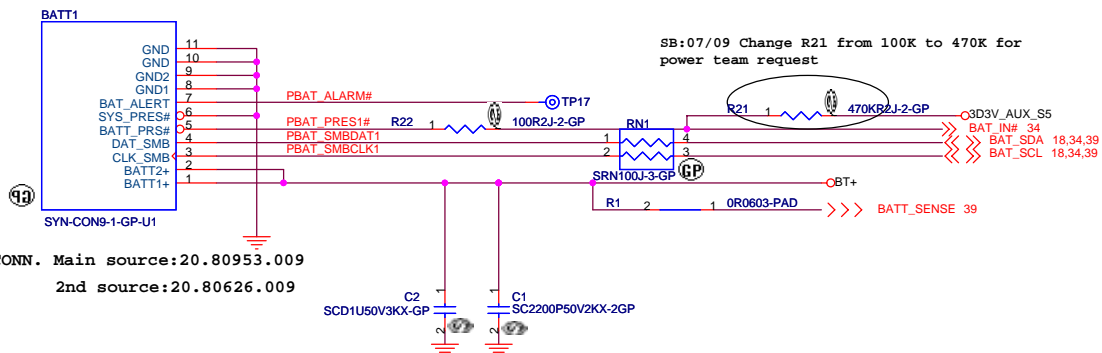
CONN 24PIN(AC-In+USB)

Reserved for EMI

Place near DCIN1

Left I/O Board to Board CONN

Batt Connector



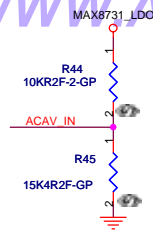
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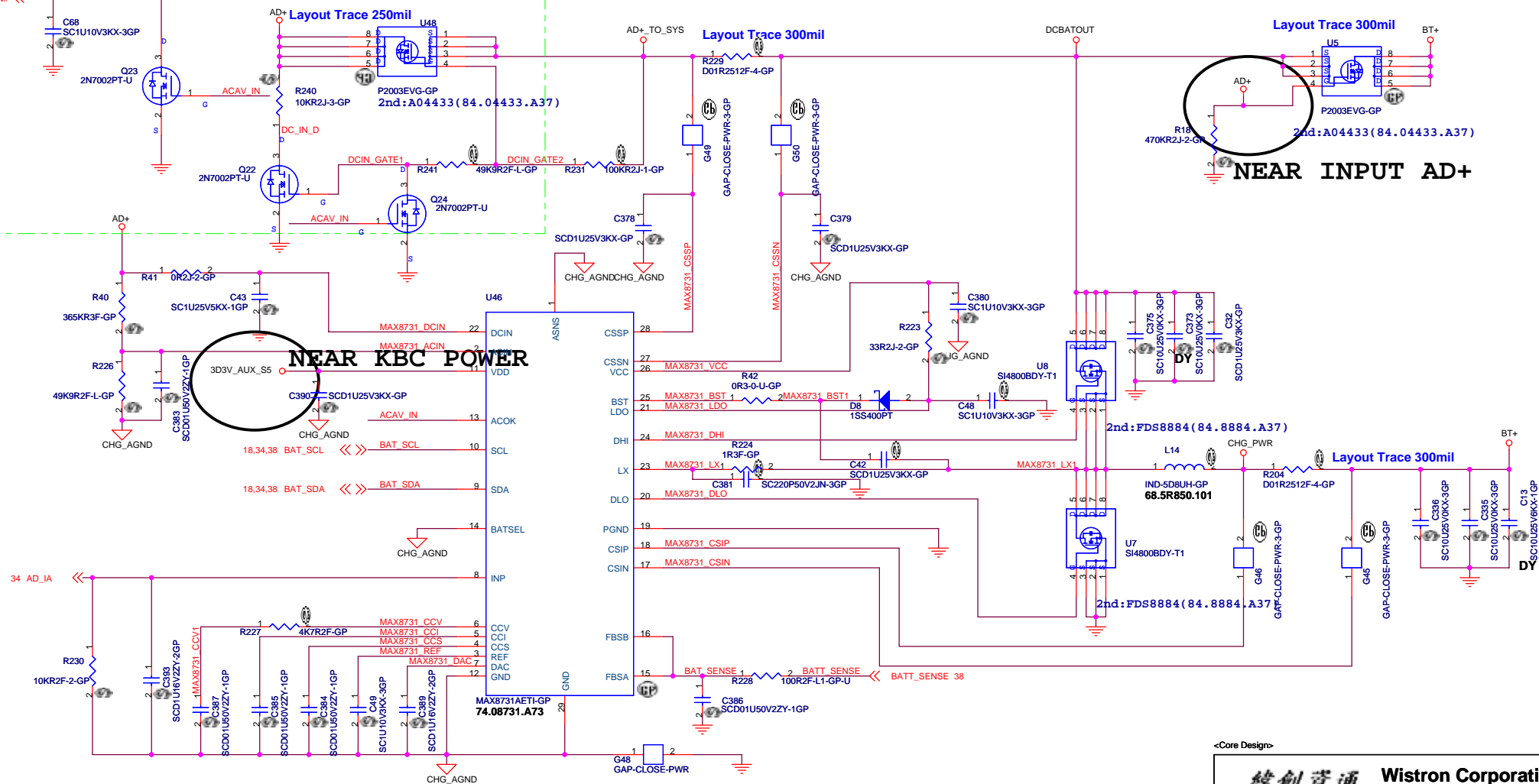
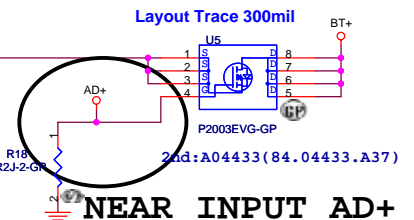
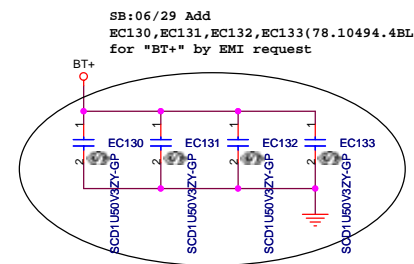
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
AD/BATT CONN			
Size	Document Number	Rev	
A3		-1	
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NEAR

Adaptor In Soft-Start Circuit



<Core Design>

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Title

CHARGER MAX8731

Size

Document Number

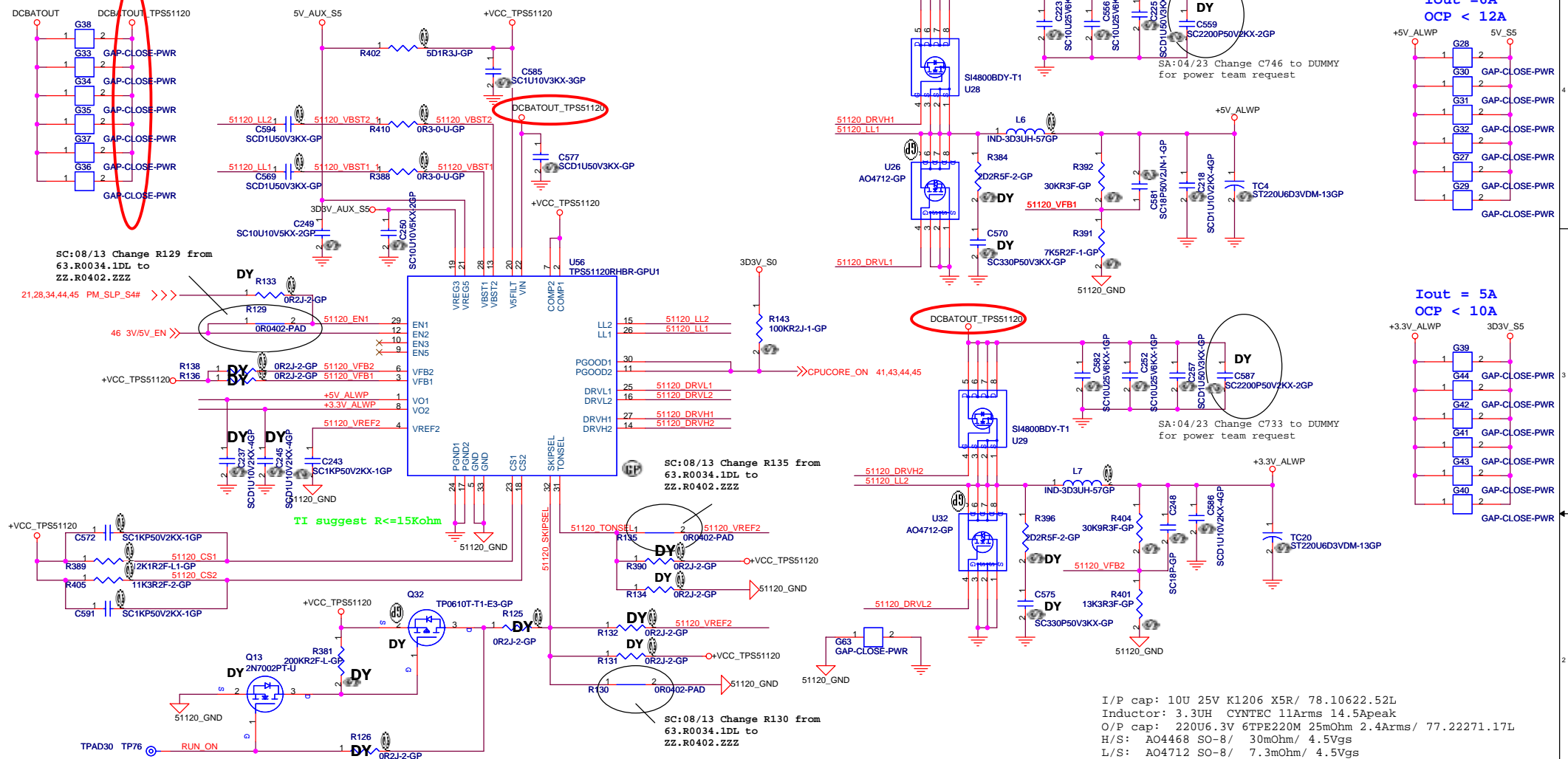
DS2-Intel

Date: Wednesday, September 12, 2007

She

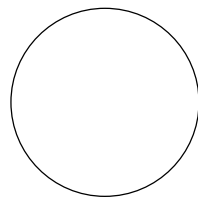
Rev

-1



$$V_{out} = 1V * (R1 + R2) / R2$$

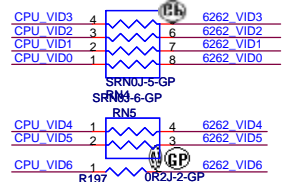
	GN2	UREF2	FLD2N	V5PIL2
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



5 CPU_PROCHOT# <<-

470K /0402 size

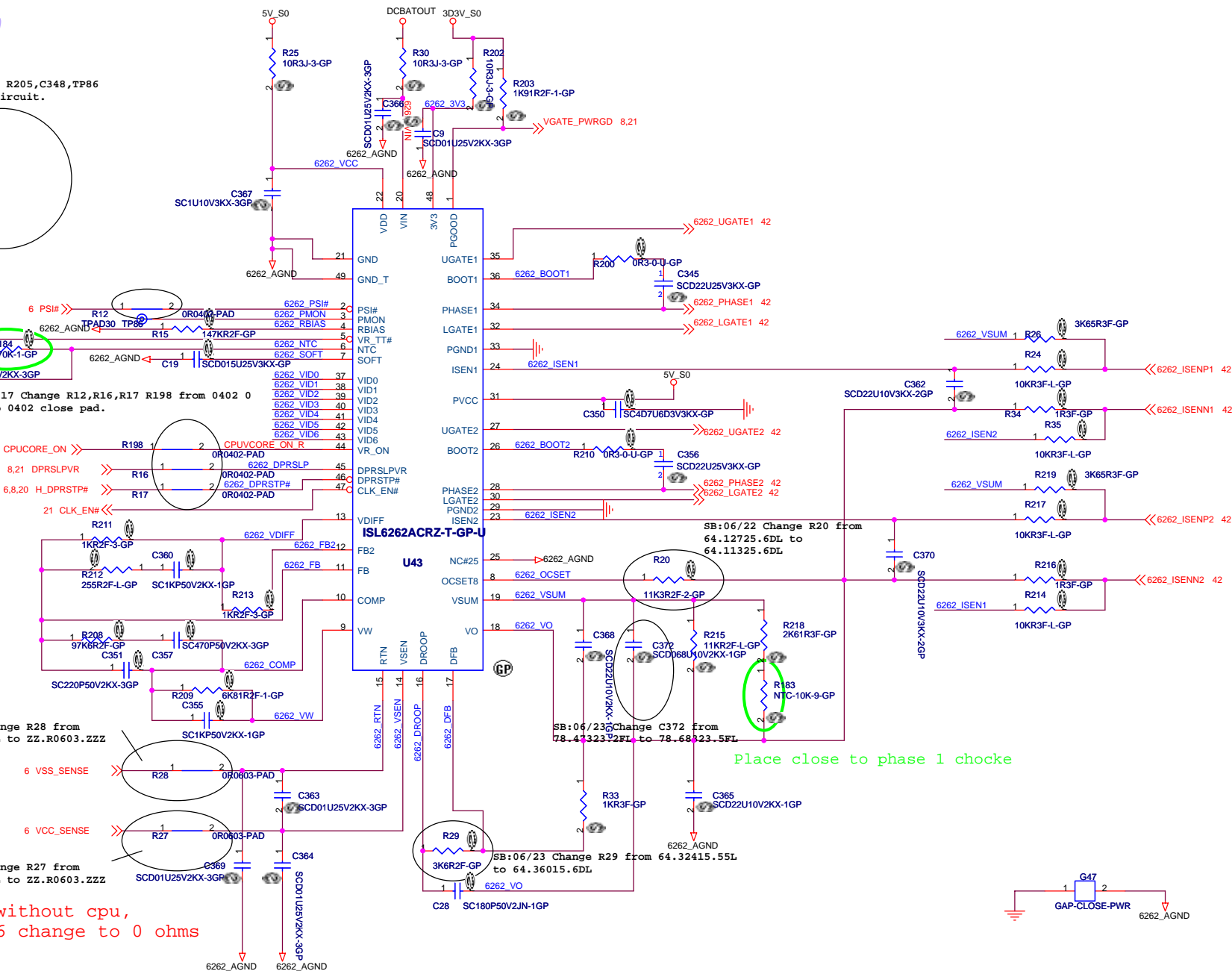
If $NTC=330K\Omega$, $R_{10}=8.66K$



SC:08/13 Change R28 from
63.00000.00L to ZZ.R0603.ZZZ

SC:08/13 Change R27 from
63.00000.00L to ZZ.R0603.ZZZ

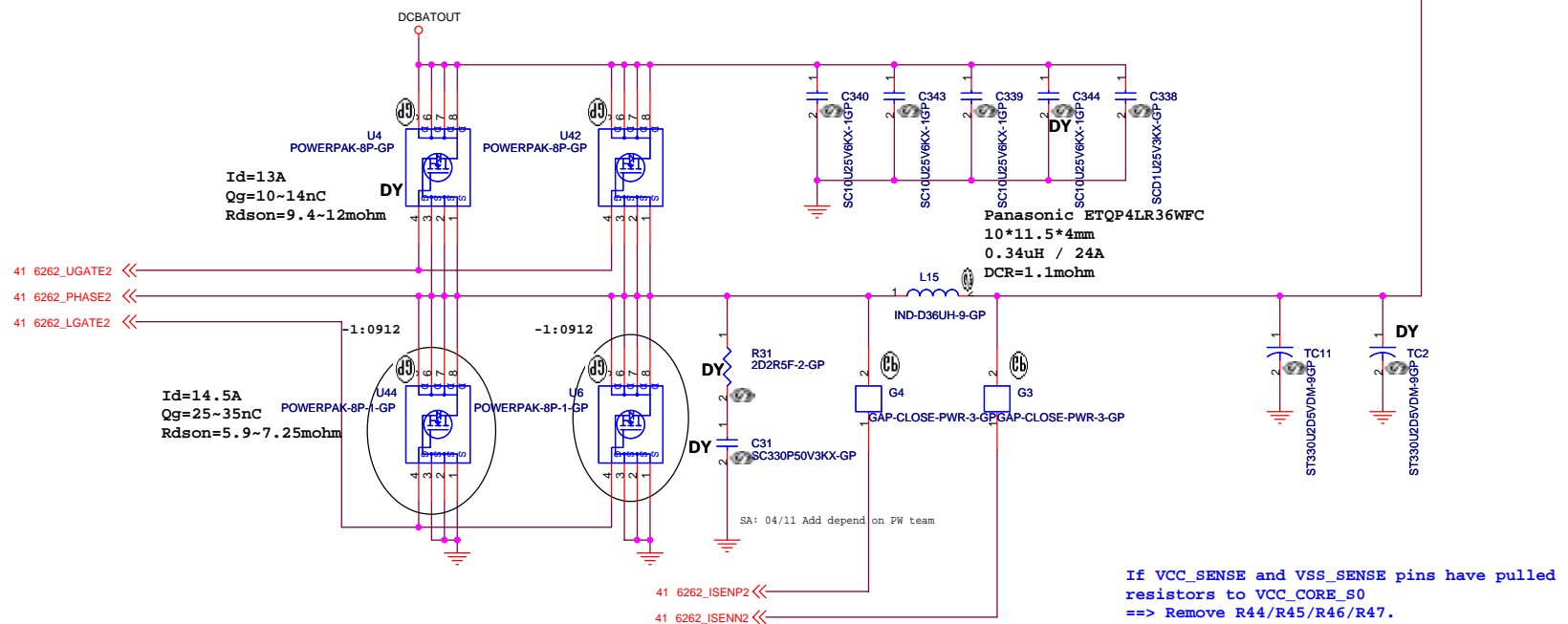
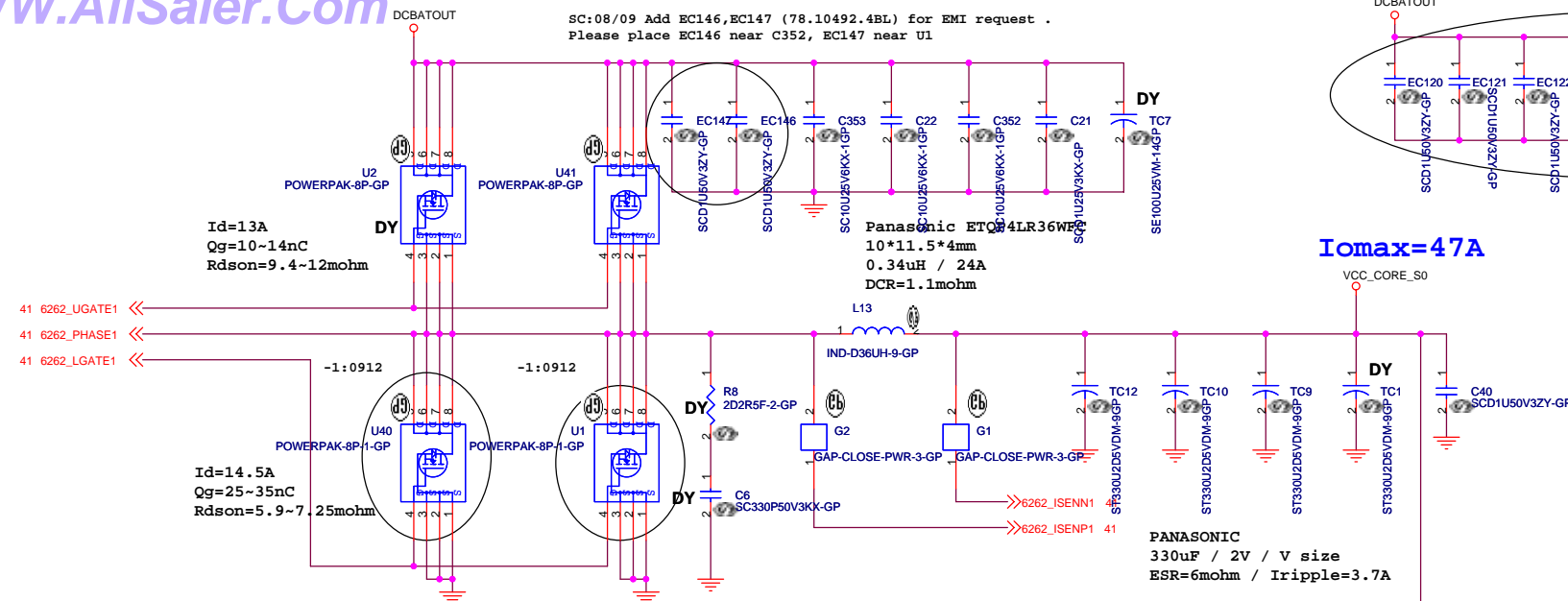
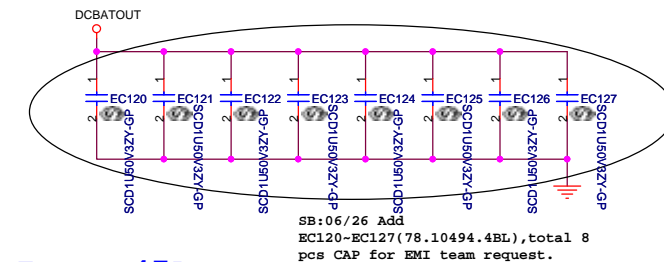
When test without cpu,
R483 & R486 change to 0 ohms



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Title			
DC-DC VCCCPUCORE 1/2			
Size	Document Number	Rev	
A3	DS2-Intel	-1	
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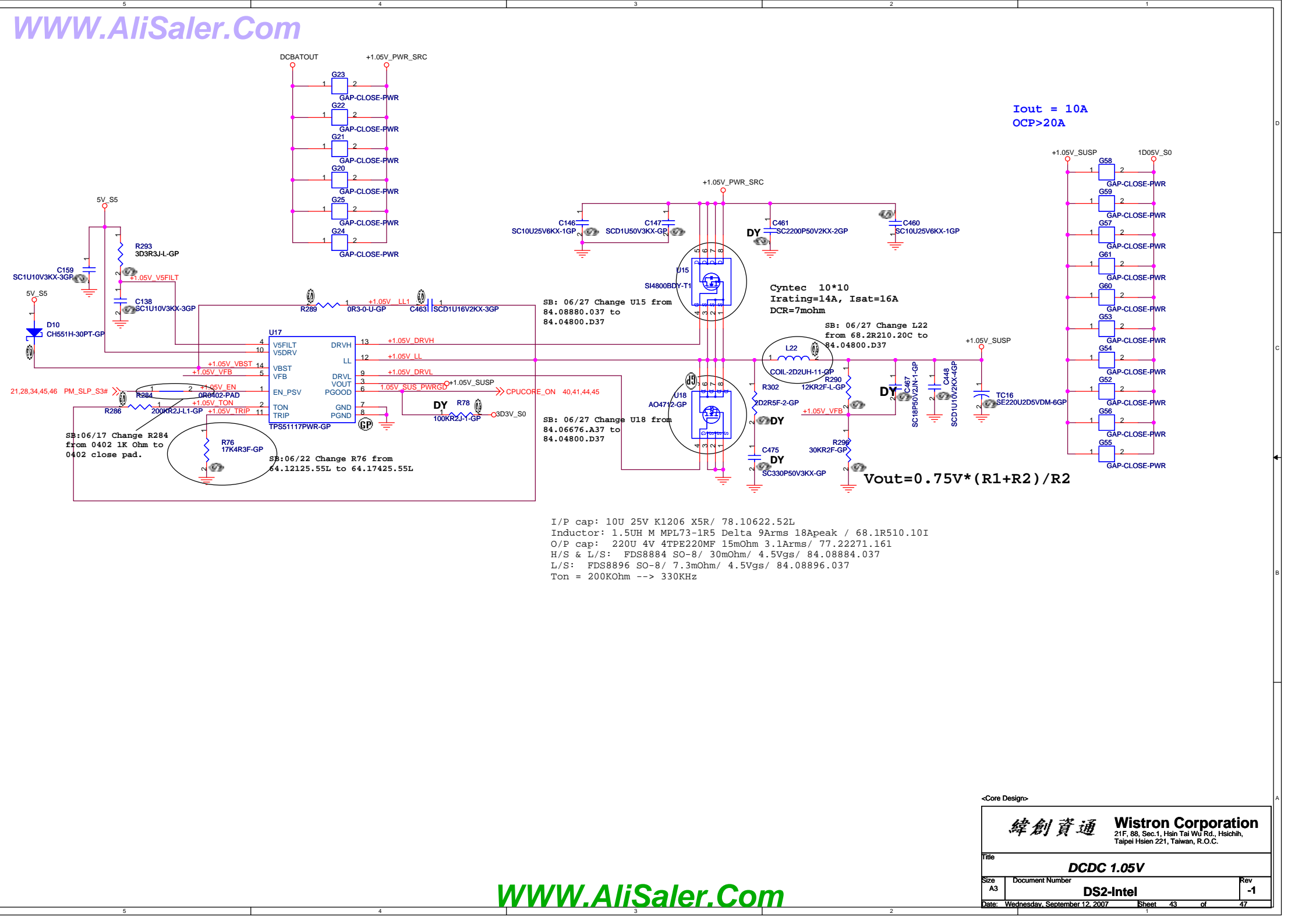


If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
==> Remove R44/R45/R46/R47.

<Core Design>

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Title			
DC-DC VCCCPUCORE 2/2			
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**I_{out} = 10A
OCP > 20A**

Cyntec 10*10
Irating=14A, Isat=16A
DCR=7mohm

V_{out}=0.75V*(R1+R2)/R2

SB: 06/17 Change R284 from 0402 1K Ohm to 0402 close pad.

SB: 06/22 Change R76 from 64.12125.55L to 64.17425.55L

SB: 06/27 Change U15 from 84.08880.037 to 84.04800.D37

SB: 06/27 Change L22 from 68.2R210.20C to 84.04800.D37

SB: 06/27 Change U18 from 84.06676.A37 to 84.04800.D37

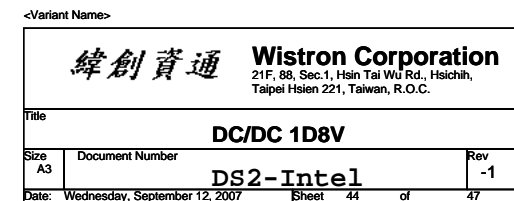
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
Ton = 200KOhm --> 330KHZ

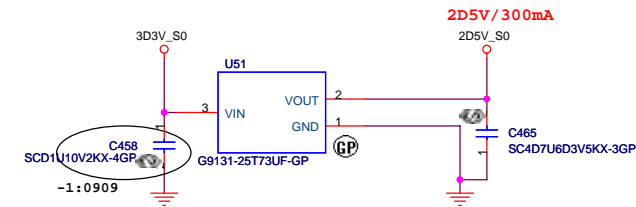
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DCDC 1.05V	
Size A3	Document Number	Rev -1
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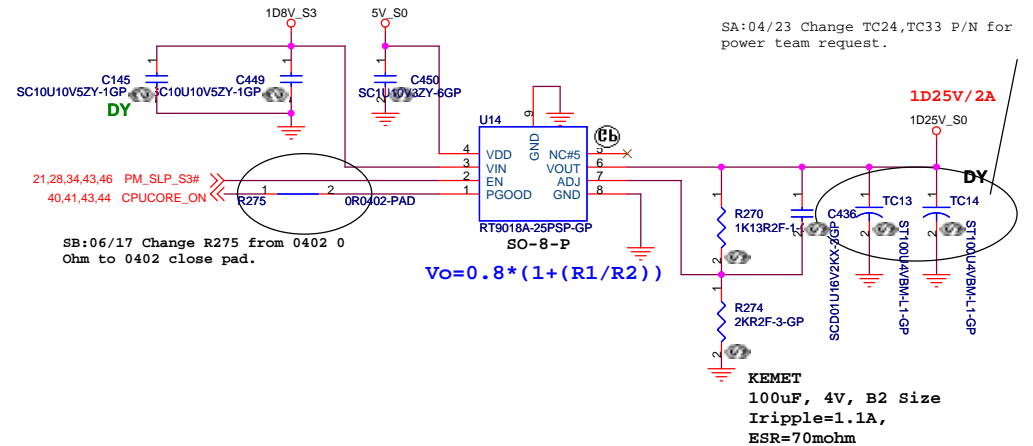
DS2-Intel

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```
SSID = PWR.Plane.Regulator_0.9V
```



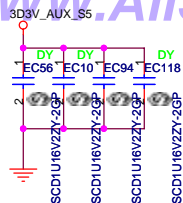
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

DC/DC 1D8V

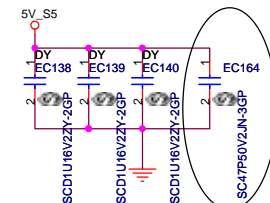
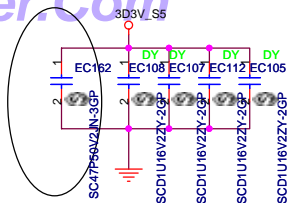
DS2-Intel

2007	Sheet
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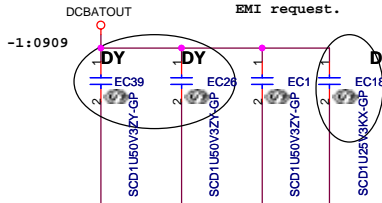
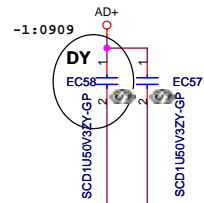
Date: Wednesday, September 12, 2007 Sheet 45 of 47



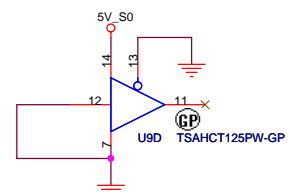
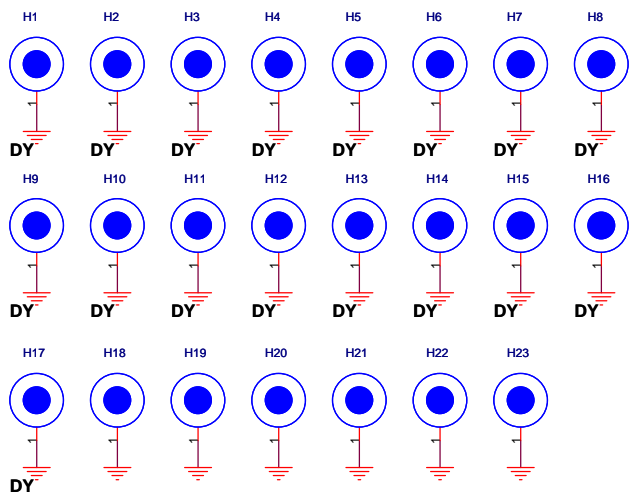
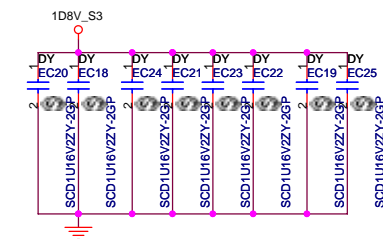
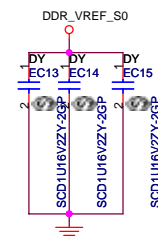
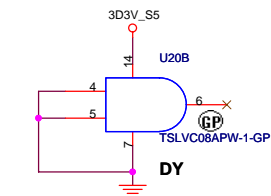
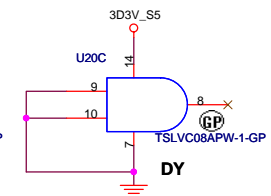
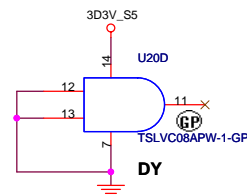
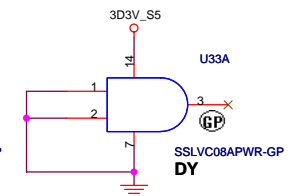
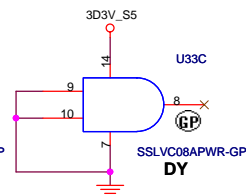
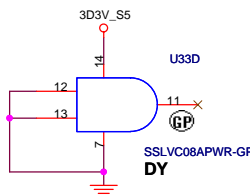
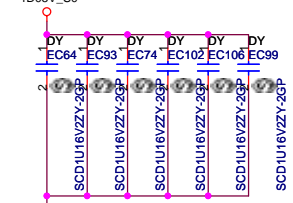
SC:08/11 Add EC162 on 3D3V_S5 for RF team Request.



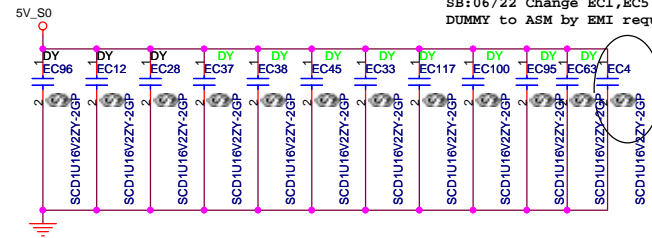
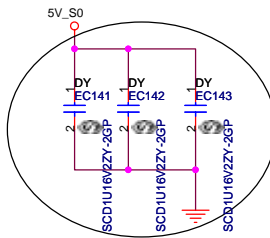
SC:08/11 Add EC164 on 5V_S5 for RF team Request.



-1:0904 Add EC187(78.10422.2BL) for DCBATOUT decoupling, this is for EMI request.

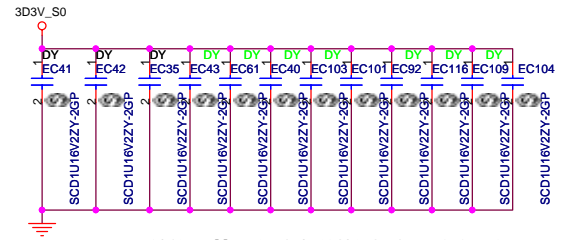
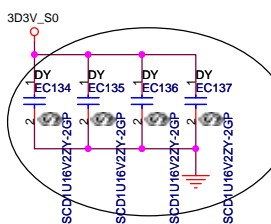


SB:06/29 Add EC141, EC142, EC143(78.10491.4FL) for EMI request

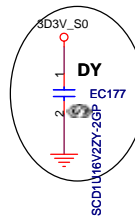


SB:06/22 Change EC1, EC5 from DUMMY to ASM by EMI request.

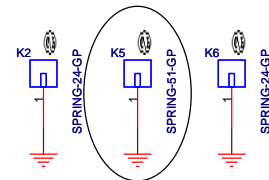
SB:06/29 Add EC134, EC135, EC136, EC137(78.10491.4FL) for EMI request



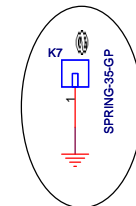
SC:08/15 Add EC177(78.10491.4FL) on 3D3V_S0, this is for EMI request. Default is DY



SC:08/09 Change K5 spring from 34.45T31.001to 34.4B312.002 for ME request



Place this spring near U40(bottom side)



SC:08/11 Change K7 from 34.39S07.001 to 34.41P18.001.This change is for EMI request

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsien 221, Taiwan, R.O.C.		
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