Alba Discrete ATI M92-LP gDDR2 Schematics

uFCPGA Mobile Penryn

Intel Cantiga-PM + ICH9M

2009-03-23

REV : SA

DY : Nopop Component

GM : Pop when Cantiga is GM

PM : Pop when Cantiga is PM

G/P : BOM control if Cantiga is PM

<Core Design>

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Title: *Cover Page*

Size: Custom | Document Number: *Alba Discrete* | Rev: *SB*

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ALBA Discrete Block Diagram

PCB LAYER
L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

Project code : 91.4BK01.001
Part Number : 48.4BK13.0SA
PCB P/N : 09207
Revision : SA

Clock Generator
SLG8SP513VTR 7

Intel Mobile CPU
Penryn
Socket P 8,9

FSB
800/1066MHz

VRAM(gDDR2)
32Mbx16x4 (512MB) 57,58

CRT 42
LCD 41
RGB CRT
LVDS(Dual Channel)

ATI M92-LP 53,54,55,56

PCIe x 16

Intel
Cantiga-GM
AGTL+ CPU I/F
DDR Memory I/F
External Graphics
10,11,12,13,14,15

DDRII 800 Channel A
DDR II 800 Channel B

DDRII 800 Slot 0 16
DDRII 800 Slot 1 17

Power SW
TPS2231RGP 50

New Card
(On Express Card board) 50

PCIE x 1 & USB 2.0 x 1

PCIE x 1

10/100 LOM
RTL8103EL 25

RJ45
CONN 42

USB 2.0 x 2

Left Side:
USB x 2 46

DMIx4
CONTROL-LINK

(7 in 1)SD/MMC
MS/MS Pro/xD
(On Express Card board)

CardReader
Realtek
RTS5159 50

USB2.0

Intel
ICH9-M
USB 2.0/1.1 ports (12)
PCI Express ports (6)
High Definition Audio
SATA ports (4)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
18,19,20,21

PCIE

PCIE x 1

Mini-Card
802.11a/b/g/n 43

USB 2.0

USB 2.0 x 1

CAMERA
(Option) 47

USB 2.0 x 1

Bluetooth 45

USB 2.0 x 1

Right Side:
USB x 1 51

Digital Mic Array
(Option) 47

Internal Mic 44

AZALIA

Azalia
CODEC
OP AMP
IDT
92HD81 22

MIC IN
HP OUT
(On Express Card board)

2CH SPEAKER
44

LPC Bus

SATA
SATA

HDD 44
ODD 44

SPI

KBC
WINBOND
WPCE773L 26

Flash ROM
2MB 47

Touch
PAD 45

Int.
KB 45

Thermal
& Fan
EMC2102 28,44

CPU DC/DC ISL6266A 34,35	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51117 36	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC TPS51125 33	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

LDO L6935TR 37	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC TPS51117 38	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS

SYSTEM DC/DC TPS51117 39	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER MAX8731A 32	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

LDO TPS51100 38	
INPUTS	OUTPUTS
+1.8V_SUS	+V_DDR_MCH_REF +0.9V_DDR_VTT

LDO L6935TR 37	
INPUTS	OUTPUTS
+1.8V_SUS	+1.1V_RUN

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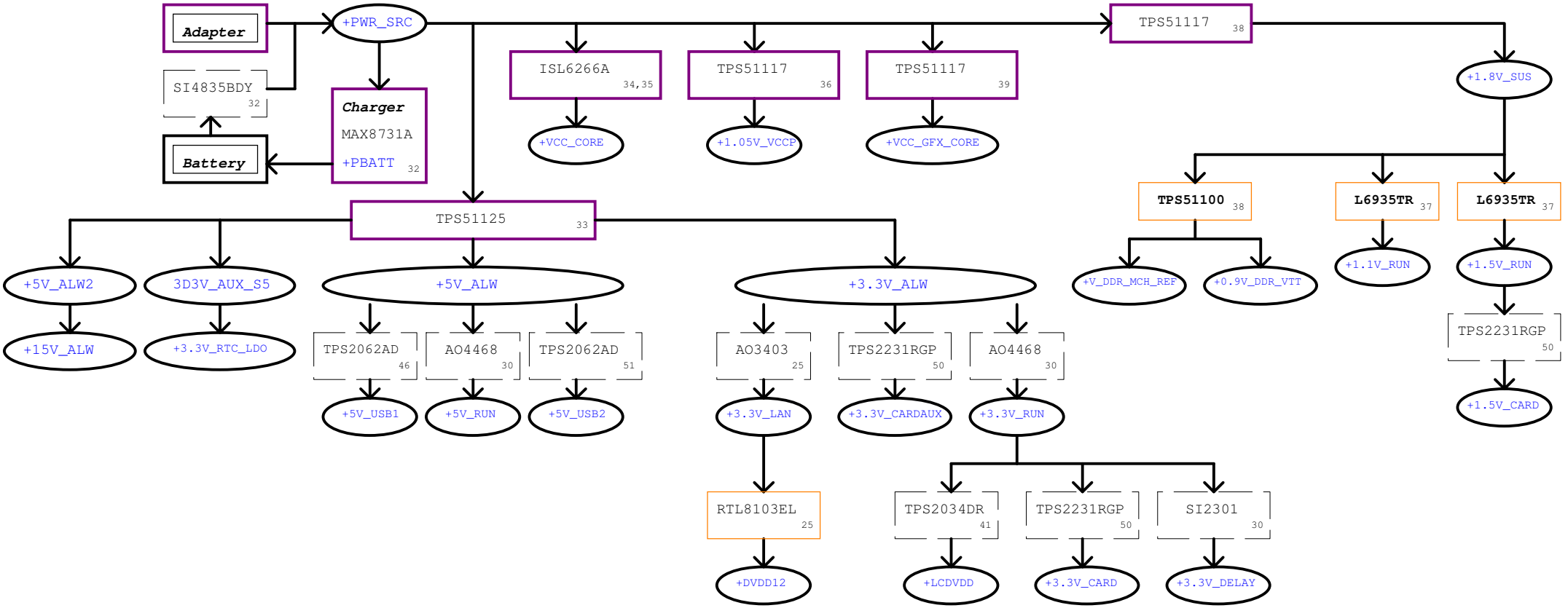

Power Shape

Regulator	LDO	Switch

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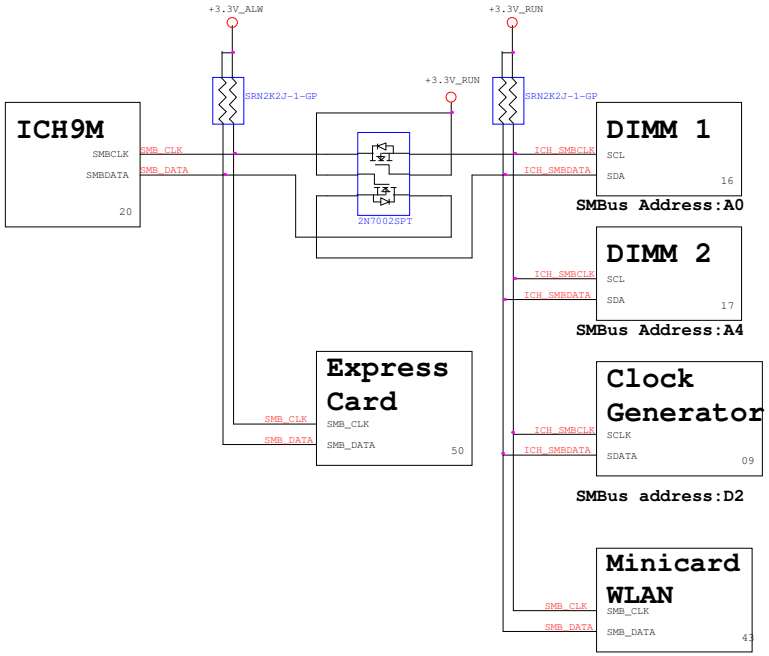
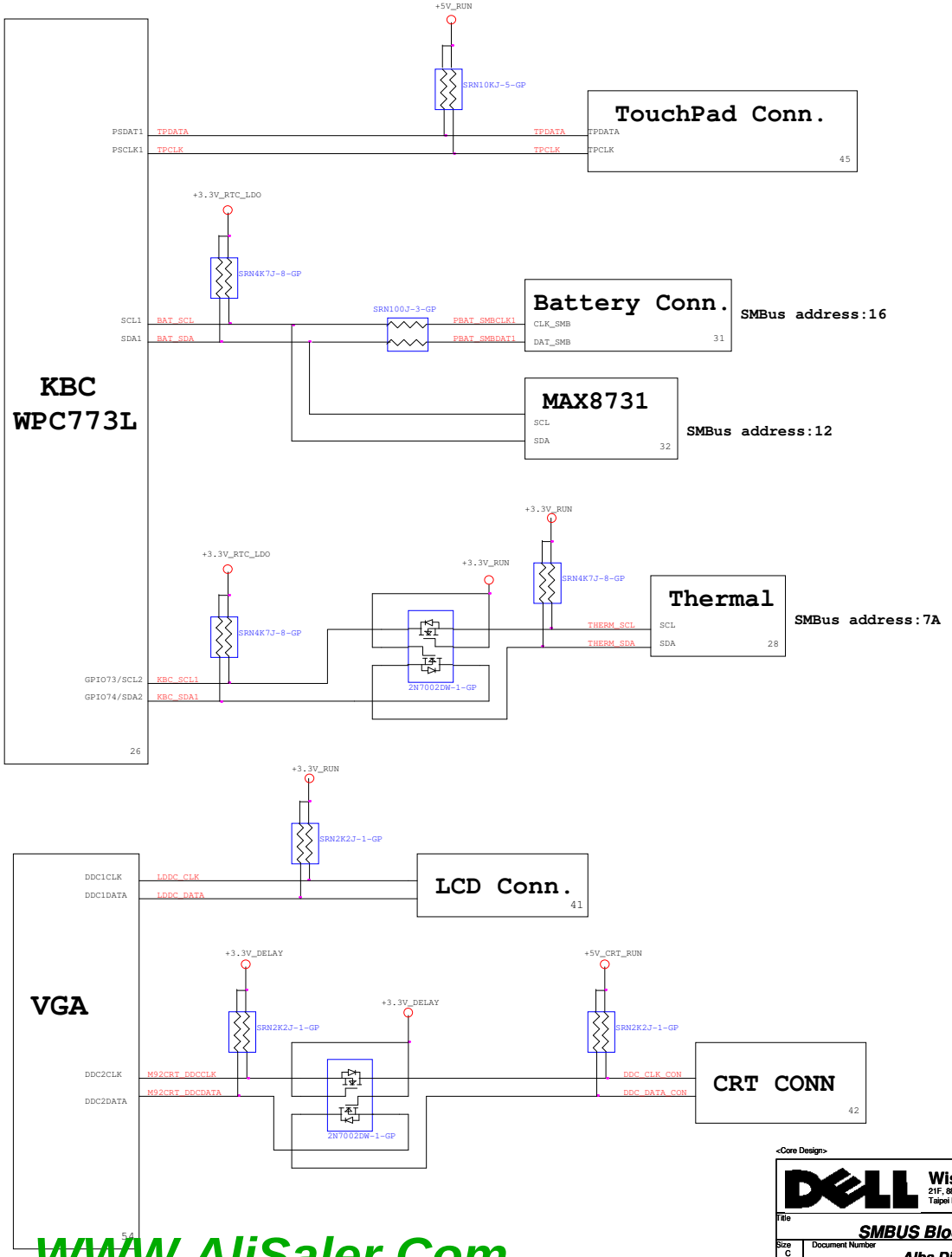
ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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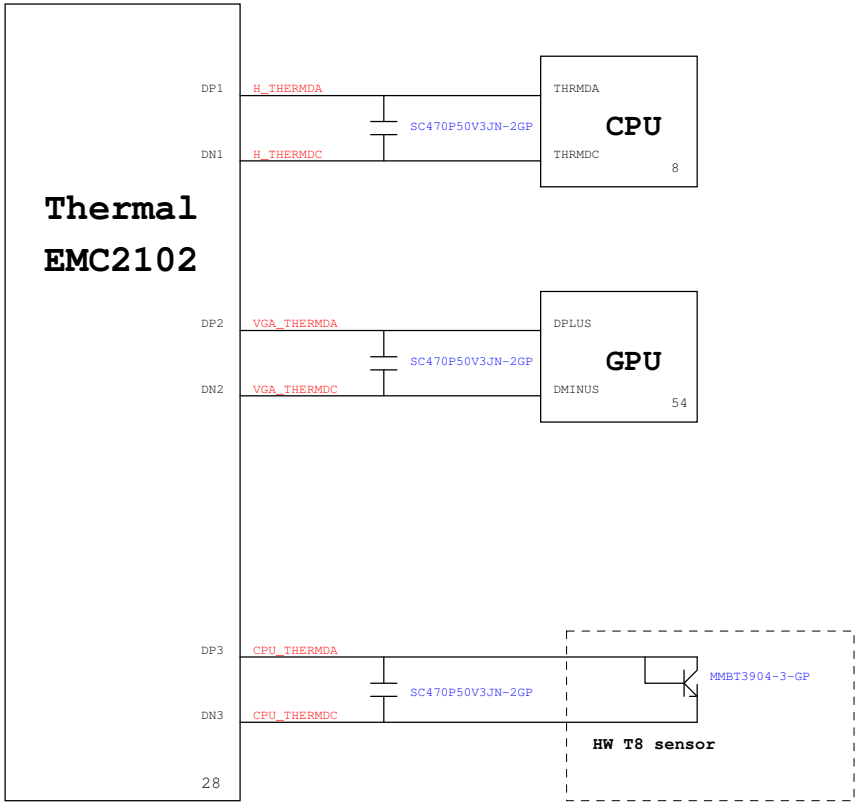
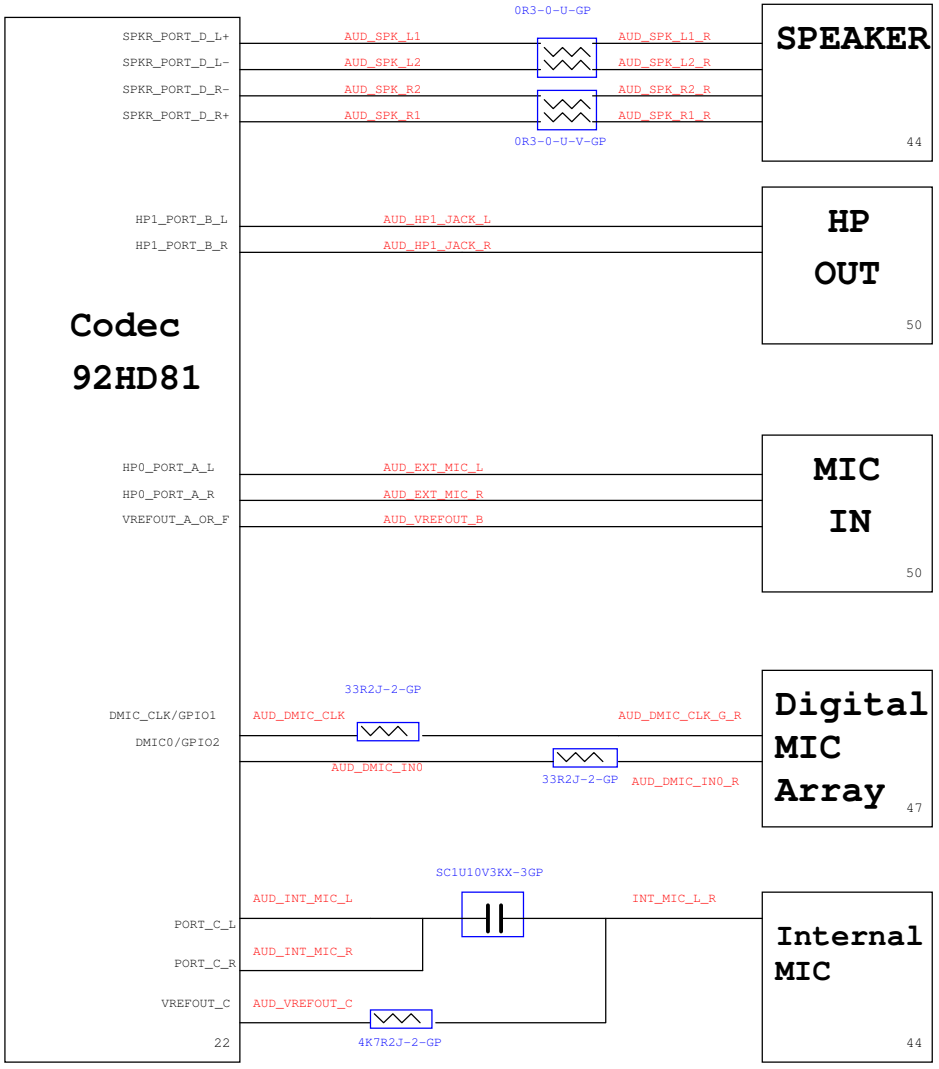
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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SSID = CLOCK

ALBA X00

ALBA X00

U701 ICS9LPRS355BKLFT-GP-U

Main source: 71.08513.003 (SLG8SP513VTR)
Second source: 71.00875.C03 (RTM875N-606-VD-GRT)

GM 20090310

GM 20090310

GM 20090311

ITP_EN	Output
0	SRC8
1	CPU_ITP

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	UMA
1	SRCT0	SRCC0	Discrete

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator SLG8SP513VTR

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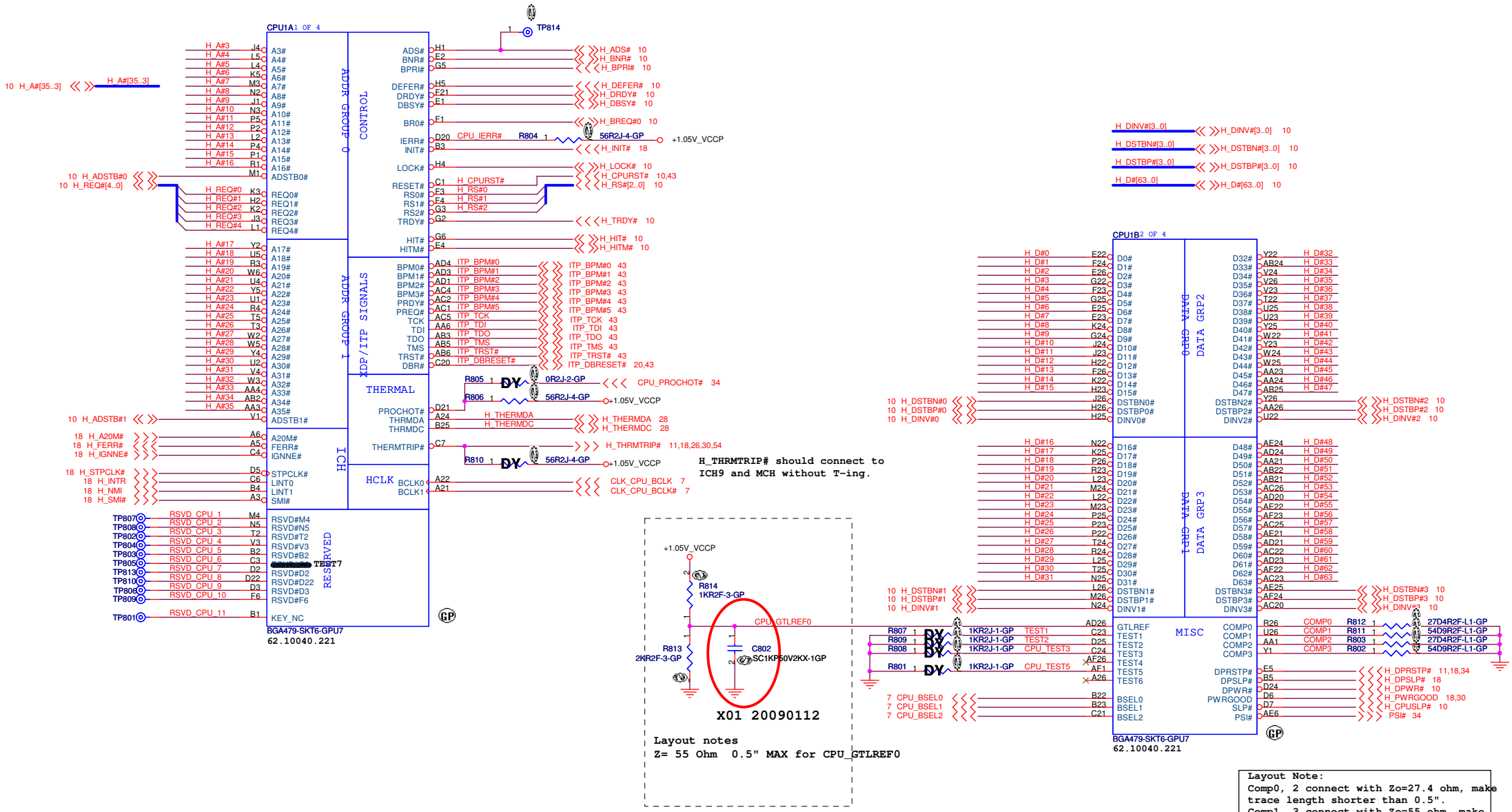
SSID = CPU



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Title: CPU-FSB(1/2)

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SSID = CPU

+VCC_CORE

C907 SC22U6D3V5MX-2GP
C914 SC22U6D3V5MX-2GP
C926 SC22U6D3V5MX-2GP

X01 20090106

+1.05V_VCCP

CPU1C 3 OF 4

BGA479-SKT6-GPU7
62.10040.221

layout note: "+1.5V_VCCA" as short as possible

+1.5V_VCCA
+1.5V_RUN
R903 0R3-0-U-GP
C939 SCD01U16V2KX-3GP
C940 SC10U6D3V5MX-3GP

Layout Note:
Place as close as possible to the CPU VCCA pin.

CPU_VID[6..0] 34

R902 100R2F-L1-GP-U
R901 100R2F-L1-GP-U
PG901 GAP-CLOSE-PWR-GP
PG902 GAP-CLOSE-PWR-GP

VCC_SENSE 34
VSS_SENSE 34

VCC_SENSE and VSS_SENSE lines should be of equal length.

CPU1D 4 OF 4

BGA479-SKT6-GPU7
62.10040.221

NCTF PIN
CPU_GND1 TP902
CPU_GND2 TP901
CPU_GND3 TP903
CPU_GND4 TP904

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Title: CPU-Power(2/2)
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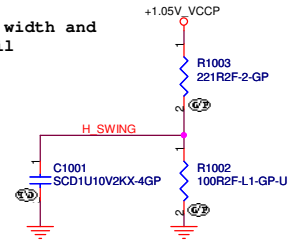
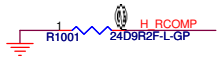
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

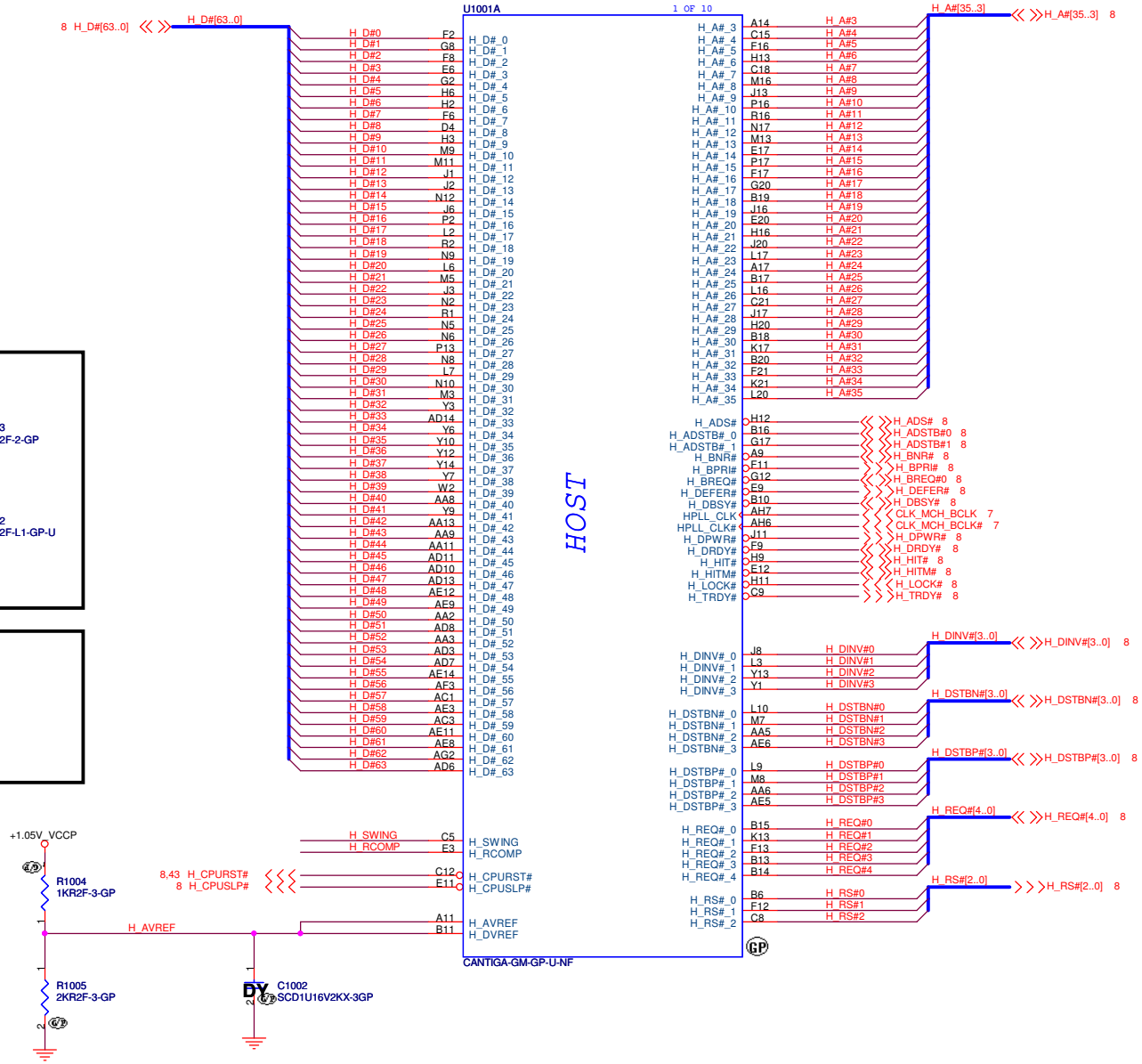
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R1001 near to the chip (< 0.5")



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Title: Cantiga-HOST(1/6)

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SSID = MCH

★ is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 ★
CFG 6	ITPM enable	ITPM disable ★
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality ★
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder ★
CFG 10	PCIE loopback enable	PCIE loopback disable ★
CFG 12	ALLZ mode enable	ALLZ mode disable ★
CFG 13	XOR mode enable	XOR mode disable ★
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable ★
CFG 19 DMI Lane Reserved	Normal operation ★	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational ★	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable ★	SDVO interface enable
L_DDC_DATA	LFP disable ★	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled ★	SDVO/iHDMI/DP interface enabled

U1001B 2 OF 10

RSVD: RESERVED#M36, RESERVED#N36, RESERVED#R33, RESERVED#T33, RESERVED#AH9, RESERVED#AH10, RESERVED#AH12, RESERVED#AH13, RESERVED#K12, RESERVED#AL34, RESERVED#AK34, RESERVED#AN35, RESERVED#AM35, RESERVED#T24, RESERVED#B31, RESERVED#B2, RESERVED#M1, RESERVED#AY21, RESERVED#BG23, RESERVED#BF23, RESERVED#BH18, RESERVED#BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0, SA_CK_1, SB_CK_0, SB_CK_1, SA_CK#_0, SA_CK#_1, SB_CK#_0, SB_CK#_1, SA_CKE_0, SA_CKE_1, SB_CKE_0, SB_CKE_1, SA_CS#_0, SA_CS#_1, SB_CS#_0, SB_CS#_1, SA_ODT_0, SA_ODT_1, SB_ODT_0, SB_ODT_1, SM_RCOMP, SM_RCOMP#, SM_RCOMP_VOH, SM_RCOMP_VOL, SM_VREF, SM_PWROK, SM_REXT, SM_DRAMRST#

CLK: DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#, PEG_CLK, PEG_CLK#

DMI: DMI_RXN_0..3, DMI_RXP_0..3, DMI_TXN_0..3, DMI_TXP_0..3

CFG: CFG_0..CFG_20

PM: PM_SYNC#, PM_DPRSTP#, PM_EXT_TS#_0, PM_EXT_TS#_1, PWROK, RSTIN#, THERMTRIP#, DPRSLPVR

GRAPHICS VID: GFX_VID_0..4, GFX_VR_EN

ME: CL_CLK, CL_DATA, CL_PWROK, CL_RST#, CL_VREF

MISC: DDPC_CTRLCLK, DDPC_CTRLDATA, SDVO_CTRLCLK, SDVO_CTRLDATA, CLKREQ#, ICH_SYNC#, TSATN#

HDA: HDA_BCLK, HDA_RST#, HDA_SDI, HDA_SDO, HDA_SYNC

NC: NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

CANTIGA-GM-GP-S-NF

M_CLK_DDR0..3 16/17, M_CKE0..3 16/17, M_CS0#..M_CS3# 16/17, M_ODT0..3 16/17, M_RCOMPP, M_RCOMPN, SM_RCOMP_VOH, SM_RCOMP_VOL, CANTIGA_SM_VREF, SM_REXT, R1123 499R2F-2-GP, CLK_MCH_DREFCLK 7, CLK_MCH_DREFCLK# 7, MCH_SSCDREFCLK 7, MCH_SSCDREFCLK# 7, CLK_MCH_3GPLL 7, CLK_MCH_3GPLL# 7

GM 20090310

DMI_ITXN0..3_MRXN0..3 19, DMI_ITXP0..3_MRXP0..3 19, DMI_IRXN0..3_MTXN0..3 19, DMI_IRXP0..3_MTXP0..3 19

RN1102 PM SRN0J-6-GP (CLK_MCH_DREFCLK, CLK_MCH_DREFCLK#)

RN1103 PM SRN0J-6-GP (MCH_SSCDREFCLK, MCH_SSCDREFCLK#)

GM 20090310

+1.8V_SUS

R1126 80D6R2F-L-GP, R1125 80D6R2F-L-GP

SM_RCOMP_VOH: R1113 1KR2F-3-GP, C1104 SC2D2U10V3KX-1GP, C1105 SCD01U16V2KX-3GP, R1109 3K01R2F-3-GP

SM_RCOMP_VOL: C1102 SC2D2U10V3KX-1GP, C1103 SCD01U16V2KX-3GP, R1111 1KR2F-3-GP

+1.8V_SUS: R1119 DY 10KR2F-2-GP, R1129 DY 10KR2F-2-GP

+V_DDR_MCH_REF: R1139 0R3-0-U-GP

C1144 DY SCD1U10V2KX-4GP, C1143 DY SCD1U10V2KX-4GP

+3.3V_RUN

R1105 DY 2K21R2F-GP CFG11
R1115 DY 2K21R2F-GP CFG18
R1110 DY 4K02R2F-GP CFG19
R1112 DY 4K02R2F-GP CFG20
RN1101 SRN10KJ-5-GP (PM_EXTTS#0, PM_EXTTS#1)

R1128 DY 2K21R2F-GP CFG5
R1108 DY 2K21R2F-GP CFG6
R1107 DY 2K21R2F-GP CFG7
R1103 DY 2K21R2F-GP CFG8
R1127 DY 4K02R2F-GP CFG9
R1124 DY 2K21R2F-GP CFG10
R1102 DY 2K21R2F-GP CFG12
R1106 DY 2K21R2F-GP CFG13
R1104 DY 2K21R2F-GP CFG16

FSB setting: 7 MCH_CLKSEL0, 7 MCH_CLKSEL1, 7 MCH_CLKSEL2

TP1103, TP1105, TP1101, TP1102, TP1104

20 PM_SYNC#, 8,18,34 H_DPRSTP#, 16 PM_EXTTS#0, 17 PM_EXTTS#1

20,26,28 PM_PWROK — R1118 0R2J-2-GP — PWROK_R

19,25,26,43,50 PLT_RST# — R1101 100R2J-2-GP — RSTIN#

C1101 DY SC100P50V2JN-3GP

8,18,26,30,54 H_THRMTRIP#, 20,34 DPRSLPVR

+1.05V_VCCP: R1114 1KR2F-3-GP, C1106 SCD1U10V2KX-4GP, R1116 499R2F-2-GP

MCH_CLVREF ~= 0.35V

TP1106

CLKREQ#_B 7, MCH_ICH_SYNC# 20

+1.05V_VCCP: R1121 56R2J-4-GP

+3.3V_RUN: R1122 DY 10KR2J-3-GP

TSATN#_KBC 26

Q1101 DY MMBT3904WT1G-GP

+3.3V_RUN: R1117 10KR2J-3-GP (CLKREQ#_B)

<Core Design>

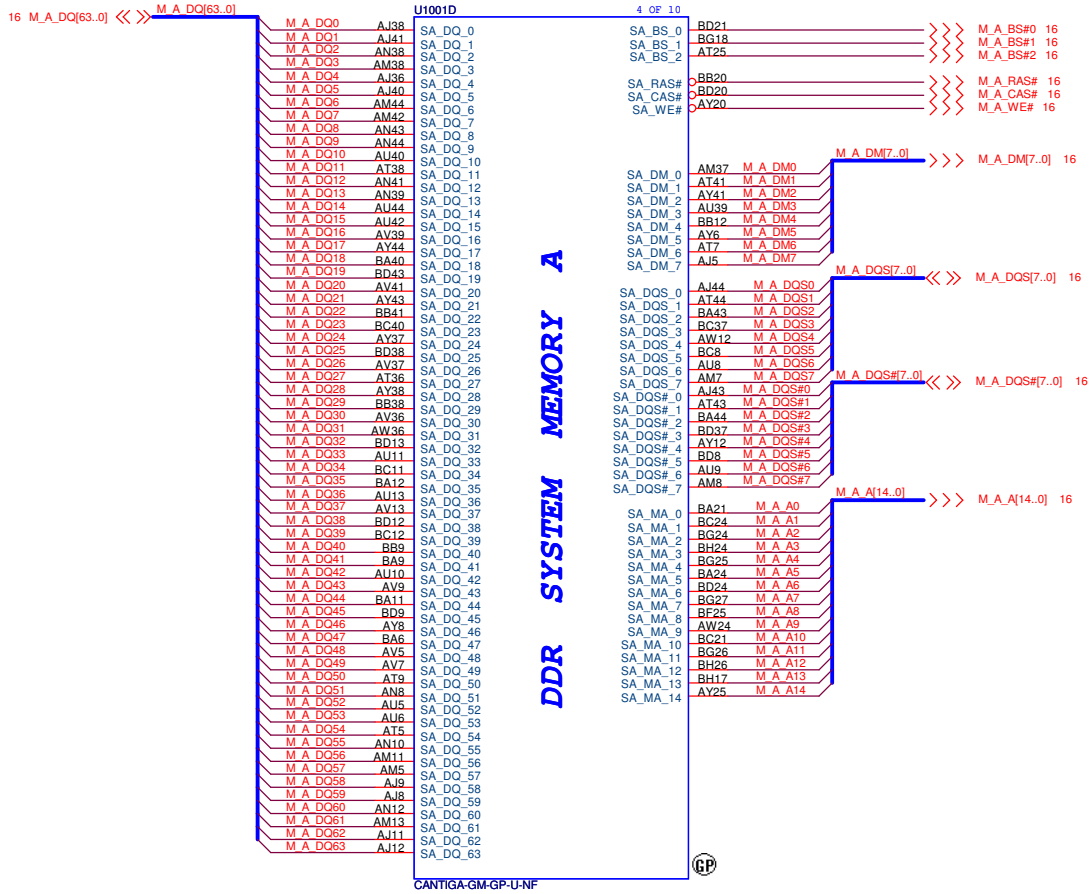
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

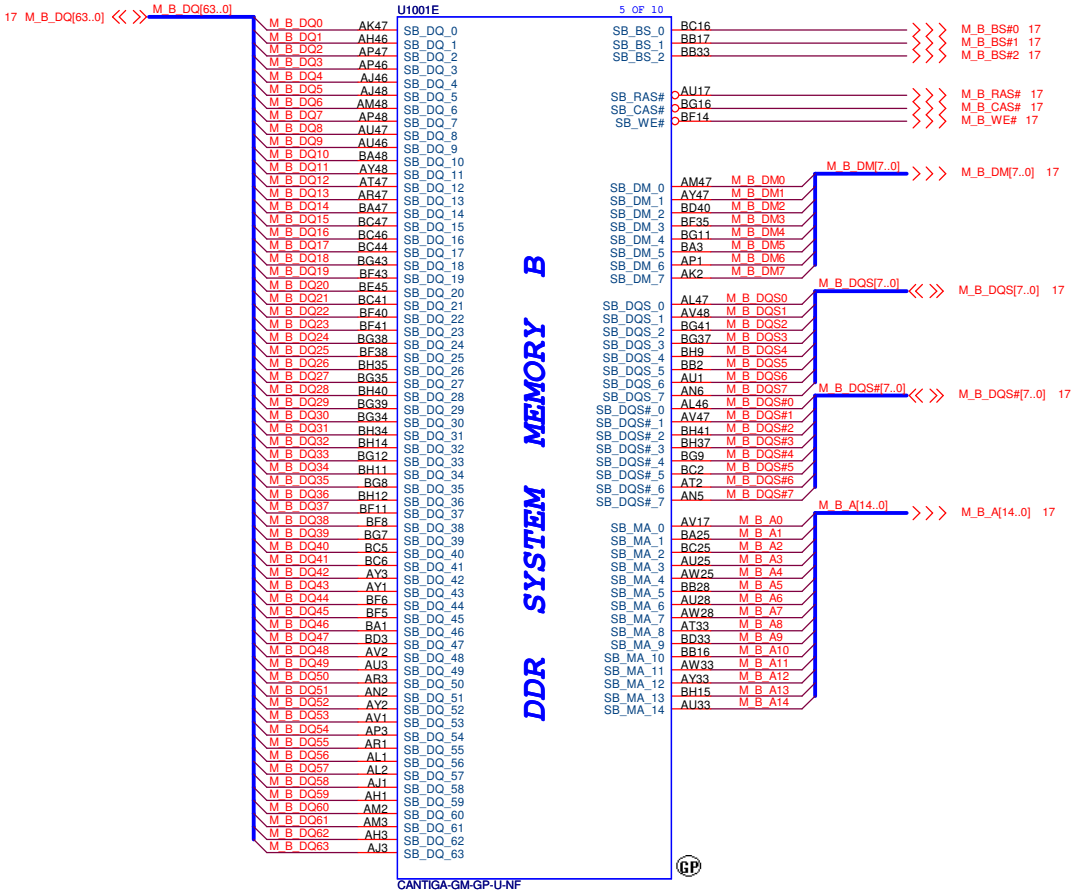
Title: Cantiga-DMI/CFG(2/6)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 11 of 59

SSID = MCH





<Core Design>

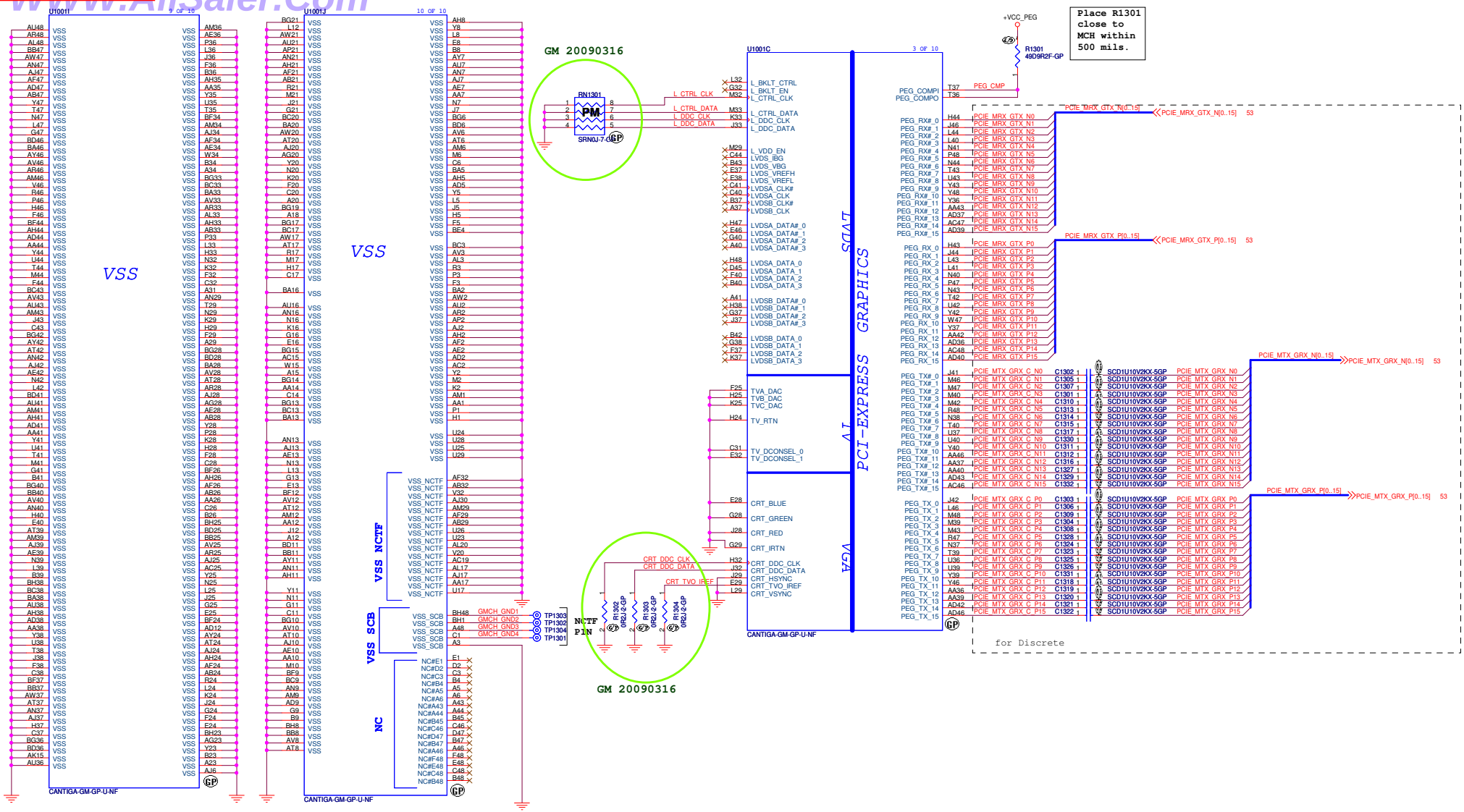
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DDR(3/6)

Size: Custom | Document Number: Alba Discrete | Rev: SB

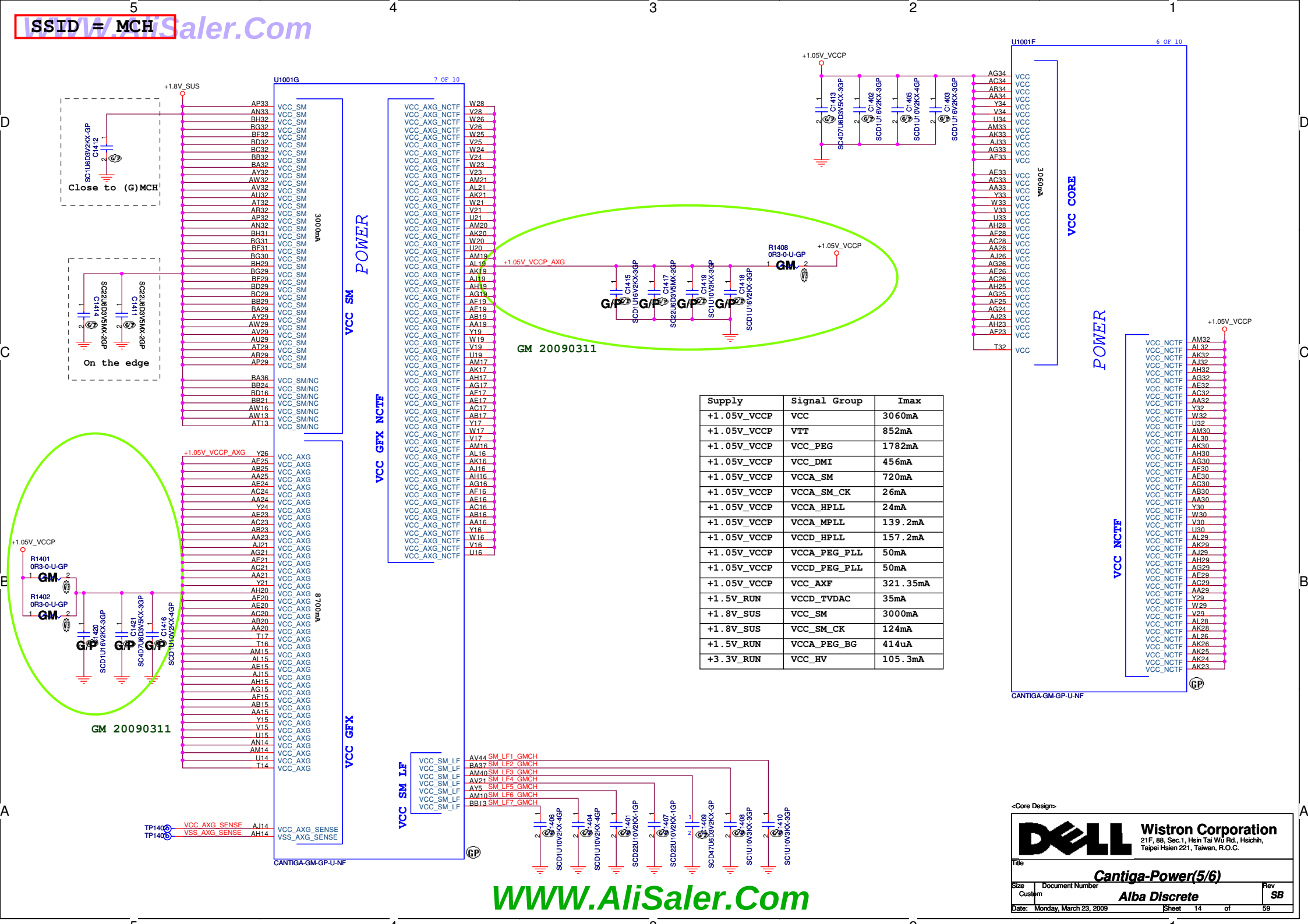
Date: Monday, March 23, 2009 | Sheet 12 of 59

SSID = MCH



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cantiga-GND/LVDS/VGA(4/6)
Size C
Document Number
Alba Discrete
Rev SB
Date: Monday, March 23, 2009
Sheet 13 of 59

SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

<Core Design>

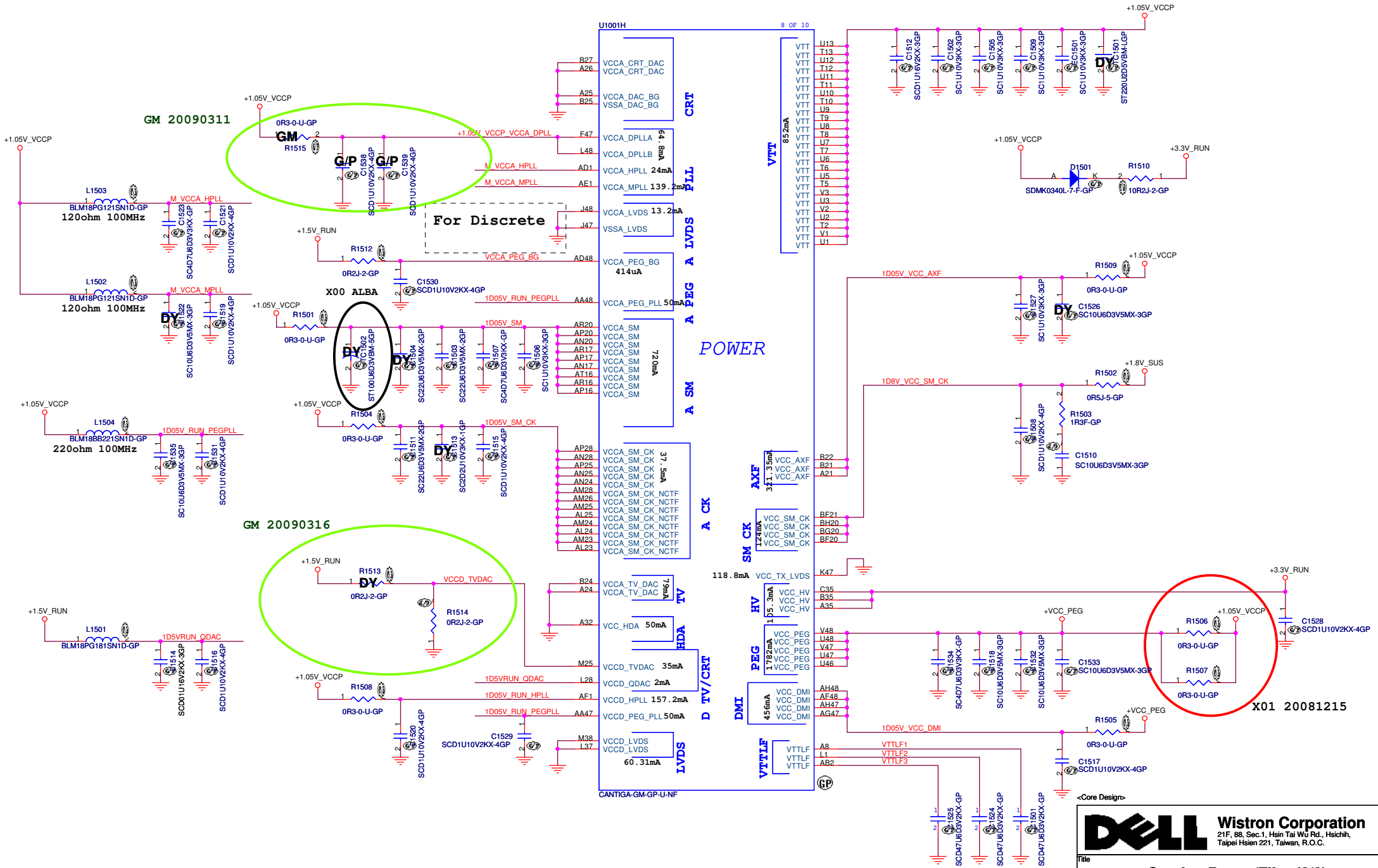
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Power(5/6)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 14 of 59

SSID = MCH



SSID = MEMORY

12 M_A_DQS#[7..0]
12 M_A_DQ[63..0]
12 M_A_DM[7..0]
12 M_A_DQS[7..0]
12 M_A_A[14..0]

DM1

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
M_A_A14 86 A14
84 A15
12 M_A_BS#2 M_A_BS#2 85 A16/BA2
12 M_A_BS#0 M_A_BS#0 107 BA0
12 M_A_BS#1 M_A_BS#1 106 BA1

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 17 DQ2
M_A_DQ3 19 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 14 DQ6
M_A_DQ7 16 DQ7
M_A_DQ8 23 DQ8
M_A_DQ9 25 DQ9
M_A_DQ10 35 DQ10
M_A_DQ11 37 DQ11
M_A_DQ12 20 DQ12
M_A_DQ13 22 DQ13
M_A_DQ14 36 DQ14
M_A_DQ15 38 DQ15
M_A_DQ16 43 DQ16
M_A_DQ17 45 DQ17
M_A_DQ18 55 DQ18
M_A_DQ19 57 DQ19
M_A_DQ20 44 DQ20
M_A_DQ21 46 DQ21
M_A_DQ22 56 DQ22
M_A_DQ23 58 DQ23
M_A_DQ24 61 DQ24
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M_A_DQ26 73 DQ26
M_A_DQ27 75 DQ27
M_A_DQ28 62 DQ28
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M_A_DQ30 74 DQ30
M_A_DQ31 76 DQ31
M_A_DQ32 123 DQ32
M_A_DQ33 125 DQ33
M_A_DQ34 135 DQ34
M_A_DQ35 137 DQ35
M_A_DQ36 124 DQ36
M_A_DQ37 126 DQ37
M_A_DQ38 134 DQ38
M_A_DQ39 136 DQ39
M_A_DQ40 141 DQ40
M_A_DQ41 143 DQ41
M_A_DQ42 151 DQ42
M_A_DQ43 153 DQ43
M_A_DQ44 140 DQ44
M_A_DQ45 142 DQ45
M_A_DQ46 152 DQ46
M_A_DQ47 154 DQ47
M_A_DQ48 157 DQ48
M_A_DQ49 159 DQ49
M_A_DQ50 173 DQ50
M_A_DQ51 175 DQ51
M_A_DQ52 158 DQ52
M_A_DQ53 160 DQ53
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M_A_DQ56 179 DQ56
M_A_DQ57 181 DQ57
M_A_DQ58 189 DQ58
M_A_DQ59 191 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 11 /DQS0
M_A_DQS#1 29 /DQS1
M_A_DQS#2 49 /DQS2
M_A_DQS#3 68 /DQS3
M_A_DQS#4 129 /DQS4
M_A_DQS#5 146 /DQS5
M_A_DQS#6 167 /DQS6
M_A_DQS#7 186 /DQS7

M_A_DQS0 13 DQS0
M_A_DQS1 31 DQS1
M_A_DQS2 51 DQS2
M_A_DQS3 70 DQS3
M_A_DQS4 131 DQS4
M_A_DQS5 148 DQS5
M_A_DQS6 169 DQS6
M_A_DQS7 188 DQS7

M_ODT0 114 ODT0
M_ODT1 119 ODT1

1 VREF
2 VSS
202 GND

/RAS 108
/WE 109
/CAS 113
M_A_RAS# 12
M_A_WE# 12
M_A_CAS# 12

/CS0 110
/CS1 115
M_CS0# 11
M_CS1# 11

CKE0 79
CKE1 80
M_CKE0 11
M_CKE1 11

CK0 30
/CK0 32
M_CLK_DDR0 11
M_CLK_DDR#0 11

CK1 164
/CK1 166
M_CLK_DDR1 11
M_CLK_DDR#1 11

10 DM0
26 DM1
52 DM2
67 DM3
130 DM4
147 DM5
170 DM6
185 DM7
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

SDA 195
SCL 197
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 7,17,20,43
ICH_SMBCLK 7,17,20,43

199 VDDSPD

SA0 198
SA1 200

ALBA X00

PM_EXTTS#0 11

NC#50 50
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163

+1.8V_SUS

VDD 81 82 87 88 95 96 103 104 111 112 117 118

VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196

201 GND

DDR2-200P-10-U1
02.10017.881

Height 6.5mm

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1

C1603 DUMMY-C2
C1604 DUMMY-C2
C1623 DUMMY-C2
C1624 DUMMY-C2

+3.3V_RUN

C1602 SCD1U16V2KX-3GP
C1601 SC2D2U10V3KX-1GP

Layout Note:
Place near DM1

+1.8V_SUS

C1620 SC1U10V3KX-3GP
C1619 SC1U10V3KX-3GP
C1622 SC2D2U10V3KX-1GP
C1621 SC2D2U10V3KX-1GP
C1616 SC1U10V3KX-3GP
C1607 SCD1U16V2KX-3GP
C1613 SCD1U10V2KX-4GP
C1609 SC1U603V2KX-GP
C1612 SCD1U10V2KX-4GP
C1601 ST220U2D5VBM-LGP

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.

+0.9V_DDR_VTT

C1610 C1627 C1611 C1608 C1605 C1630 C1606 C1614 C1617 C1618 C1615 C1629 C1628
SCD1U16V2KX-3GP

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".

+0.9V_DDR_VTT

RN1601 SRN56J-5-GP
M_A_A5 M_A_A8 M_A_A9 M_A_A12

RN1605 SRN56J-4-GP
M_CKE0 M_A_BS#2

R1663 56R2J-4-GP
M_A_A13

RN1602 SRN56J-5-GP
M_ODT0 M_CS0# M_A_BS#1 M_A_RAS#

RN1606 SRN56J-5-GP
M_A_A3 M_A_A1 M_A_A10 M_A_BS#0

RN1603 SRN56J-5-GP
M_ODT1 M_CS1# M_A_CAS# M_A_WE#

RN1607 SRN56J-5-GP
M_A_A7 M_A_A11 M_A_A14 M_CKE1

RN1604 SRN56J-5-GP
M_A_A0 M_A_A2 M_A_A4 M_A_A6

+V_DDR_MCH_REF

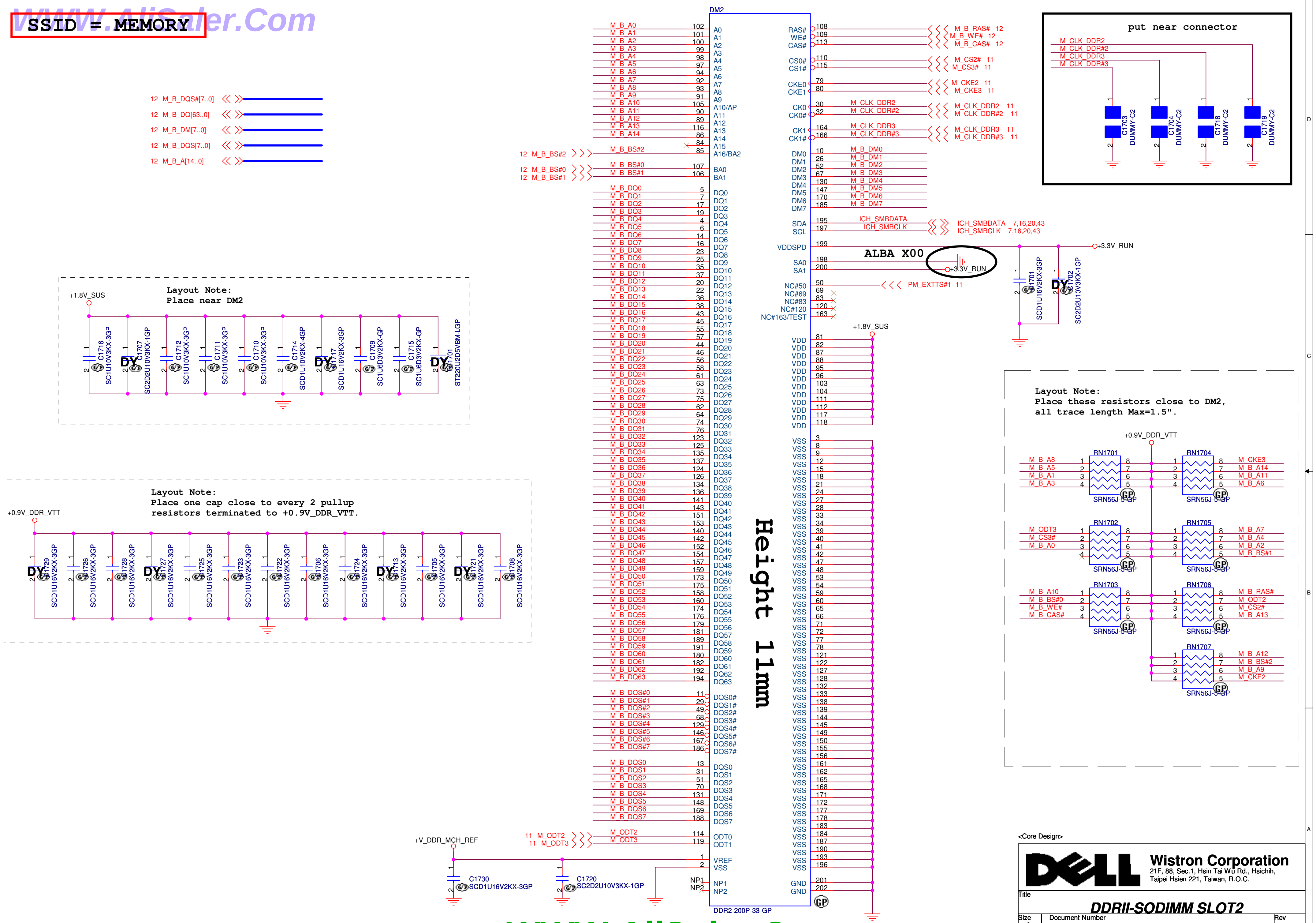
C1626 SCD1U16V2KX-3GP
C1625 SC2D2U10V3KX-1GP

11 M_ODT0
11 M_ODT1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1
Size: Custom
Document Number: Alba Discrete
Rev: SB
Date: Monday, March 23, 2009
Sheet 16 of 59



SSID = MEMORY
12 M_B_DQS#[7..0]
12 M_B_DQ[63..0]
12 M_B_DM[7..0]
12 M_B_DQS[7..0]
12 M_B_A[14..0]
DM2
DDR2-200P-33-GP
Height 11mm
M_B_A0 … M_B_A14
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
12 M_B_BS#2
12 M_B_BS#0
12 M_B_BS#1
M_B_DQ0 … M_B_DQ63
DQ0 … DQ63
M_B_DQS#0 … M_B_DQS#7
DQS0# … DQS7#
M_B_DQS0 … M_B_DQS7
DQS0 … DQS7
11 M_ODT2
11 M_ODT3
ODT0 ODT1
VREF VSS NP1 NP2
+V_DDR_MCH_REF
C1730 SCD1U16V2KX-3GP
C1720 SC2D2U10V3KX-1GP
RAS# WE# CAS# CS0# CS1# CKE0 CKE1 CK0 CK0# CK1 CK1#
M_B_RAS# 12
M_B_WE# 12
M_B_CAS# 12
M_CS2# 11
M_CS3# 11
M_CKE2 11
M_CKE3 11
M_CLK_DDR2 11
M_CLK_DDR#2 11
M_CLK_DDR3 11
M_CLK_DDR#3 11
DM0 … DM7
M_B_DM0 … M_B_DM7
SDA SCL
ICH_SMBDATA 7,16,20,43
ICH_SMBCLK 7,16,20,43
VDDSPD
SA0 SA1
ALBA X00
+3.3V_RUN
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
PM_EXTTS#1 11
+1.8V_SUS
VDD VSS GND
C1701 SCD1U16V2KX-3GP
C1702 SC2D2U10V3KX-1GP
put near connector
C1703 DUMMY-C2
C1704 DUMMY-C2
C1718 DUMMY-C2
C1719 DUMMY-C2
Layout Note:
Place near DM2
C1716 SC1U10V3KX-3GP
C1707 SC2D2U10V3KX-1GP
C1712 SC1U10V3KX-3GP
C1711 SC1U10V3KX-3GP
C1710 SC1U10V3KX-3GP
C1714 SCD1U10V2KX-4GP
C1717 SCD1U16V2KX-3GP
C1709 SC1U6D3V2KX-GP
C1715 SC1U6D3V2KX-GP
TC1701 ST220U2D5VBM-LGP
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.
+0.9V_DDR_VTT
C1729 C1726 C1728 C1727 C1725 C1723 C1722 C1706 C1724 C1713 C1705 C1721 C1708 SCD1U16V2KX-3GP
Layout Note:
Place these resistors close to DM2,
all trace length Max=1.5".
RN1701 RN1702 RN1703 RN1704 RN1705 RN1706 RN1707 SRN56J-5-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDRII-SODIMM SLOT2**

Size: Custom | Document Number: **Alba Discrete** | Rev: **SB**

Date: Monday, March 23, 2009 | Sheet 17 of 59

SSID = ICH

ICH_RTCX1 — R1812 10MR2J-L-GP — ICH_RTCX2

X1801 — X-32D768KHZ-38GPU

C1807 SC12P50V3JN-GP — X02 20090219

C1806 SC12P50V3JN-GP — X02 20090219

+RTC_CELL — R1814 20KR2F-L-GP — ICH_RTCRST# — C1801 SC1U10V3KX-3GP — G1801 GAP-OPEN

+RTC_CELL — R1815 20KR2F-L-GP — C1808 SC1U10V3KX-3GP

+1.5V_RUN — R1811 24D9R2F-L-GP — Place within 500 mil of SB.

R1821 DY 10KR2J-3-GP — GPIO56 — GLAN_COMP

22 ICH_AZ_CODEC_BITCLK — R1822 33R2J-2-GP — ACZ_BIT_CLK

22 ICH_AZ_CODEC_SYNC — R1823 33R2J-2-GP — ACZ_SYNC_R

22 ICH_AZ_CODEC_RST# — R1824 33R2J-2-GP — ACZ_RST#_R

22 ICH_SDOUT_CODEC — R1825 33R2J-2-GP — ACZ_SDATAOUT_R

X01 20081208

22 ICH_SDIN_CODEC — Removed X01 20081208

TP1801 — SATA_LED#

HDD

44 SATA_IRXN0_HTXN0_C — C1802 SCD01U50V2KX-1GP — SATA_ITXN0_HRXN0_C — 44 SATA_ITXN0_HRXN0

44 SATA_IRXP0_HTXP0_C — C1803 SCD01U50V2KX-1GP — SATA_ITXP0_HRXP0_C — 44 SATA_ITXP0_HRXP0

ODD

44 SATA_IRXN1_OTXN1_C — C1804 SCD01U50V2KX-1GP — SATA_ITXN1_ORXN1_C — 44 SATA_ITXN1_ORXN1

44 SATA_IRXP1_OTXP1_C — C1805 SCD01U50V2KX-1GP — SATA_ITXP1_ORXP1_C — 44 SATA_ITXP1_ORXP1

Removed X01 20081208 — ICH_AZ_CODEC_BITCLK — DY EC1802 SC4D7P50V2CN-1GP

Lay Out Close U1801

+RTC_CELL — R1813 330KR2F-L-GP — ICH_INTVRMEN

R1809 330KR2F-L-GP — LAN100_SLP

R1808 1MR2J-1-GP — SM_INTRUDER#

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

U1801A — 1 OF 6 — ICH9M-GP-NF

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#

LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23

LAN / GLAN: INTVRMEN, LAN100_SLP, GLAN_CLK, LAN_RSTSYNC, LAN_RXD0, LAN_RXD1, LAN_RXD2, LAN_TXD0, LAN_TXD1, LAN_TXD2, GLAN_DOCK#/GPIO56, GLAN_COMPI, GLAN_COMPO

CPU: A20GATE, A20M#, DPRSTP#, DPSLP#, FERR#, CPUPWRGD, IGNNE#, INIT#, INTR, RCIN#, NMI, SMI#, STPCLK#, THRMTRIP#, PECI

HDA: HDA_BIT_CLK, HDA_SYNC, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDOUT, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO34, SATALED#

SATA: SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP, SATA4RXN, SATA4RXP, SATA4TXN, SATA4TXP, SATA5RXN, SATA5RXP, SATA5TXN, SATA5TXP, SATA_CLKN, SATA_CLKP, SATARBIAS#, SATARBIAS

LPC_LAD[0..3] — LPC_LAD[0..3] 26

LPC_LFRAME# — R1816 0R2J-2-GP DY — LPC_LFRAME#_IN — LPC_LFRAME#_IN 43

LPC_LAD3 — R1817 0R2J-2-GP DY — LPC_LAD3_IN — LPC_LAD3_IN 43

LPC_LAD2 — R1818 0R2J-2-GP DY — LPC_LAD2_IN — LPC_LAD2_IN 43

LPC_LAD1 — R1819 0R2J-2-GP DY — LPC_LAD1_IN — LPC_LAD1_IN 43

LPC_LAD0 — R1820 0R2J-2-GP DY — LPC_LAD0_IN — LPC_LAD0_IN 43

For MINICARD debug board.

LPC_LFRAME# 26

R1810 DY 10KR2J-3-GP — +3.3V_RUN

KA20GATE 26 — H_A20M# 8

R1801 56R2J-4-GP — +1.05V_VCCP

H_DPRSTP# 8,11,34 — H_DPSLP# 8

R1804 56R2J-4-GP — H_FERR# 8

H_PWRGOOD 8,30

R1807 DY 10KR2J-3-GP — +3.3V_RUN

H_IGNNE# 8

H_INIT# 8 — H_INTR 8

KBRCIN# 26

H_NMI 8 — H_SMI# 8

R1802 56R2J-4-GP — +1.05V_VCCP

H_STPCLK# 8

R1803 54D9R2F-L1-GP — H_THERMTRIP_1 — R1805 0R2J-2-GP — H_THRMTRIP# 8,11,26,30,54

Placed Within 2" from SB.

CLK_PCIE_SATA# 7 — CLK_PCIE_SATA 7

SATARBIAS — R1806 24D9R2F-L-GP — Place within 500 mils from SB.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(1/4)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 18 of 59

SSID = ICH

U1801E — 5 OF 6 — ICH9M-GP-NF

U1902 — 74LVC1G08GW-1-GP

11,25,26,43,50 PLT_RST# → PLT_RST# → PCI_PLTRST#

R1907 0R2J-2-GP

53 PLTRST_ICH_DELAY# → R1913 DY 0R2J-2-GP

X01 20081208

U1801B — 2 OF 6 — PCI — Interrupt I/F — ICH9M-GP-NF

PCI_REQ0# PCI_GNT0# PCI_REQ1# PCI_GNT1# PCI_REQ2# PCI_GNT2# PCI_REQ3# PCI_GNT3#

TP1907 TP1916 TP1903 TP1904

PCI_IRDY# PCI_DEVSEL# PCI_PERR# PCI_PLOCK# PCI_SERR# PCI_STOP# PCI_TRDY# PCI_FRAME# PCI_PLTRST#

CLK_PCI_ICH 7 ICH_PME#

PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD#

PCI_PIRQE# PCI_PIRQF# PCI_PIRQG# PCI_PIRQH#

+3.3V_RUN

RN1905 PCI_PIRQF# PCI_TRDY# PCI_REQ3# PCI_PIRQD# — SRN8K2J-4-GP

RN1901 PCI_PIRQB# PCI_PIRQG# PCI_REQ0# PCI_PIRQH# — SRN8K2J-4-GP

RN1902 PCI_STOP# PCI_PLOCK# PCI_IRDY# PCI_PERR# — SRN8K2J-4-GP

RN1906 PCI_DEVSEL# PCI_REQ1# PCI_FRAME# PCI_REQ2# — SRN8K2J-4-GP

RN1904 PCI_SERR# PCI_PIRQE# PCI_PIRQA# PCI_PIRQC# — SRN8K2J-4-GP

RP1901 USB_OC#7 USB_OC#11 USB_OC#5 USB_OC#4 → USB_OC#0 USB_OC#1 USB_OC#6 USB_OC#2 — +3.3V_ALW — SRN10KJ-L3-GP

RN1903 USB_OC#9 USB_OC#8 USB_OC#10 USB_OC#3 — +3.3V_ALW — SRN8K2J-4-GP

PCI_GNT0# R1910 DY 1KR2J-1-GP

SPI_CS#1 R1911 DY 1KR2J-1-GP

PCI_GNT3# R1909 DY 1KR2J-1-GP

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

U1801D — 4 OF 6 — PCI-Express — Direct Media Interface — SPI — USB — ICH9M-GP-NF

Mini Card: 43 PCIE_IRXN2_MTXN2 / 43 PCIE_IRXP2_MTXP2 / 43 PCIE_ITXN2_MRXN2 / 43 PCIE_ITXP2_MRXP2 — C1903 C1902 SCD1U16V2KX-3GP — PCIE_ITXN2_MRXN2_C / PCIE_ITXP2_MRXP2_C

LAN: 25 PCIE_IRXN3_RTXN3 / 25 PCIE_IRXP3_RTXP3 / 25 PCIE_ITXN3_LRXN3 / 25 PCIE_ITXP3_LRXP3 — C1904 C1905 SCD1U16V2KX-3GP — PCIE_ITXN3_LRXN3_C / PCIE_ITXP3_LRXP3_C

New Card: 50 PCIE_IRXN5_NTXN5 / 50 PCIE_IRXP5_NTXP5 / 50 PCIE_ITXN5_NRXN5 / 50 PCIE_ITXP5_NRXP5 — C1907 C1906 SCD1U16V2KX-3GP — PCIE_ITXN5_NRXN5_C / PCIE_ITXP5_NRXP5_C

DMI0RXN DMI0RXP DMI0TXN DMI0TXP → DMI_IRXN0_MTXN0 11 / DMI_IRXP0_MTXP0 11 / DMI_ITXN0_MRXN0 11 / DMI_ITXP0_MRXP0 11

DMI1RXN DMI1RXP DMI1TXN DMI1TXP → DMI_IRXN1_MTXN1 11 / DMI_IRXP1_MTXP1 11 / DMI_ITXN1_MRXN1 11 / DMI_ITXP1_MRXP1 11

DMI2RXN DMI2RXP DMI2TXN DMI2TXP → DMI_IRXN2_MTXN2 11 / DMI_IRXP2_MTXP2 11 / DMI_ITXN2_MRXN2 11 / DMI_ITXP2_MRXP2 11

DMI3RXN DMI3RXP DMI3TXN DMI3TXP → DMI_IRXN3_MTXN3 11 / DMI_IRXP3_MTXP3 11 / DMI_ITXN3_MRXN3 11 / DMI_ITXP3_MRXP3 11

DMI_CLKN → CLK_PCIE_ICH# 7 / DMI_CLKP → CLK_PCIE_ICH 7

DMI_ZCOMP DMI_IRCOMP → DMI_IRCOMP_R

+1.5V_RUN — R1908 24D9R2F-L-GP

TP1917 SPI_CLK / TP1918 SPI_CS0# / SPI_CS1# SPI_CS1#/GPIO58/CLGPIO6

TP1920 SPI_MOSI / TP1919 SPI_MISO

USB_RBIAS_PN → R1912 22R6J2-L-GP — USB_RBIAS_PN USBRBIAS USBRBIAS#

46 USB_OC#0 / 46 USB_OC#1 / 51 USB_OC#2 → USB_OC#0 USB_OC#1 USB_OC#2 USB_OC#3 USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9 USB_OC#10 USB_OC#11

USBP0N USBP0P USBP1N USBP1P → USB_PN0 46 / USB_PP0 46 / USB_PN1 46 / USB_PP1 46 — USB1

USBP2N USBP2P → USB_PN2 / USB_PP2 — USB2

USBP3N USBP3P → USB_PN3 / USB_PP3 — TP1908 TP1909 — USB3

USBP4N USBP4P → USB_PN4 43 / USB_PP4 43 — MINI CARD

USBP5N USBP5P → USB_PN5 / USB_PP5 — TP1912 TP1913 — BlUETOOTH

USBP6N USBP6P → USB_PN6 45 / USB_PP6 45 — New Card

USBP7N USBP7P → USB_PN7 50 / USB_PP7 50

USBP8N USBP8P → USB_PN8 / USB_PP8 — TP1910 TP1911

USBP9N USBP9P → USB_PN9 / USB_PP9 — TP1914 TP1915

USBP10N USBP10P → USB_PN10 50 / USB_PP10 50 — Card Reader

USBP11N USBP11P → USB_PN11 47 / USB_PP11 47 — CAMERA

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

NCTF PIN: ICH_GND1 TP1905 / ICH_GND2 TP1906 / ICH_GND3 TP1901 / ICH_GND4 TP1902

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-PCI/PCIE/DMI/USB/GND(2/4)

Size: Custom | Document Number: Alba Discrete | Rev: SB

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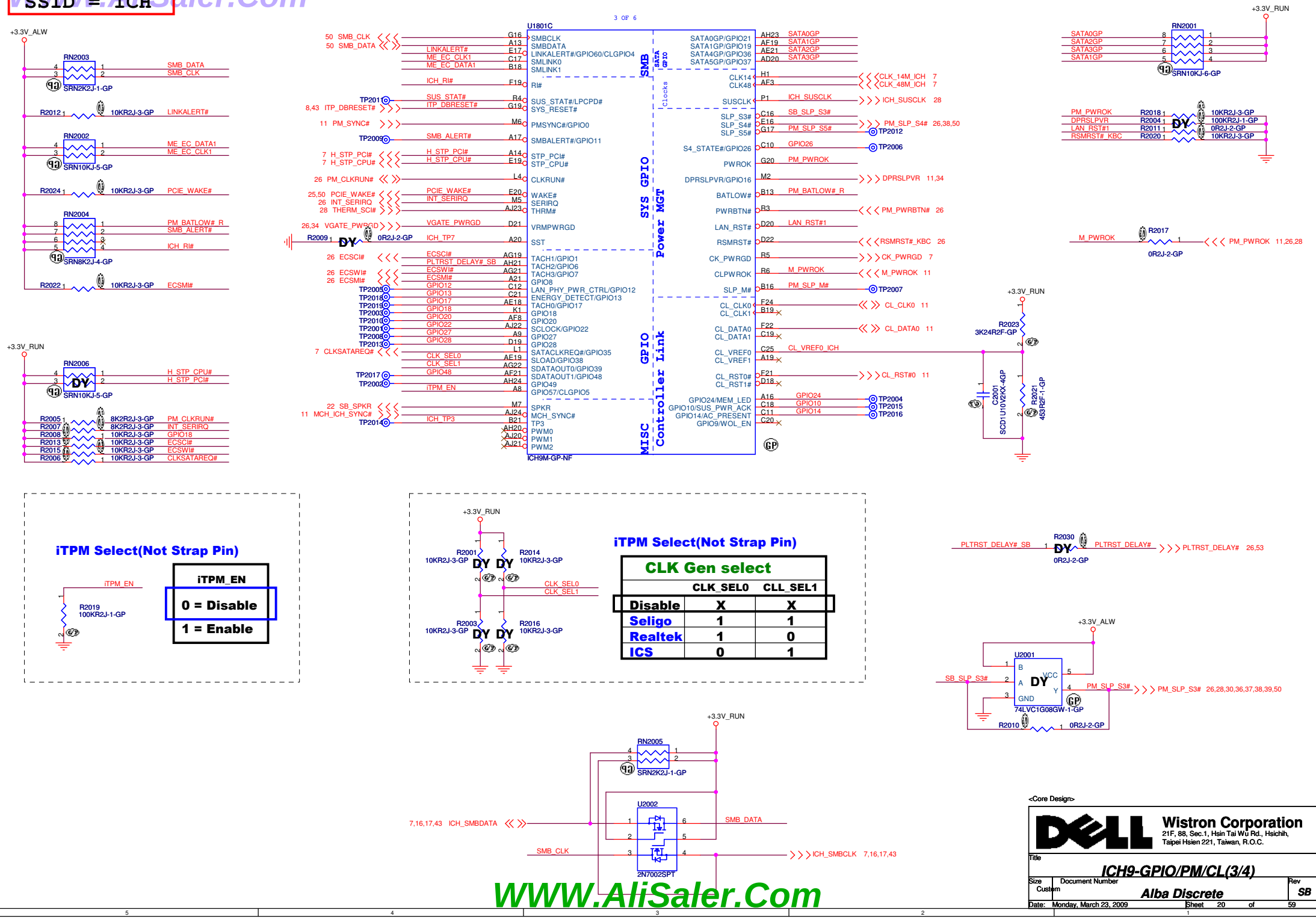
SSID = ICH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

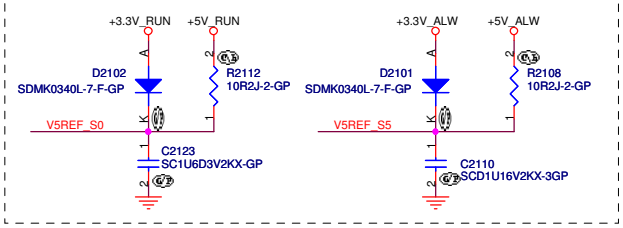
Title: ICH9-GPIO/PM/CL(3/4)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 20 of 59

SSID = ICH

**Within a given well, 5VREF needs to be up before the corresponding 3.3V rail*



<Core Design>

Wistron Corporation
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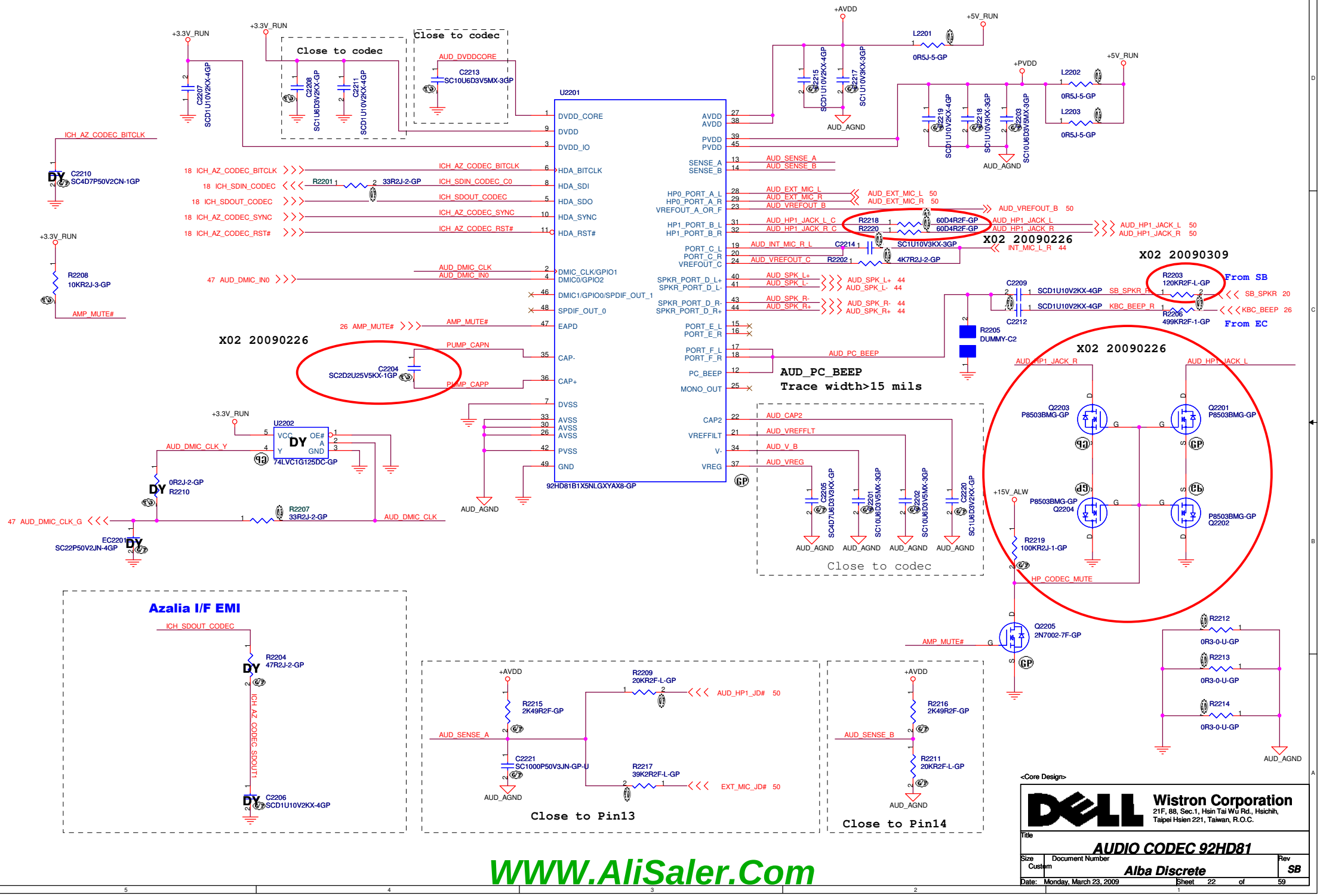
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-POWER(4/4)
Size: Custom | Document Number: Alba Discrete | Rev: SB
Date: Monday, March 23, 2009 | Sheet 21 of 59

SSID = AUDIO



<Core Design>

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Title: AUDIO CODEC 92HD81

Size: Custom | Document Number: Alba Discrete | Rev: SB

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<Core Design>

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Title: (Reserve)

Size: Custom | Document Number: Alba Discrete | Rev: SB

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Title: (Reserve)

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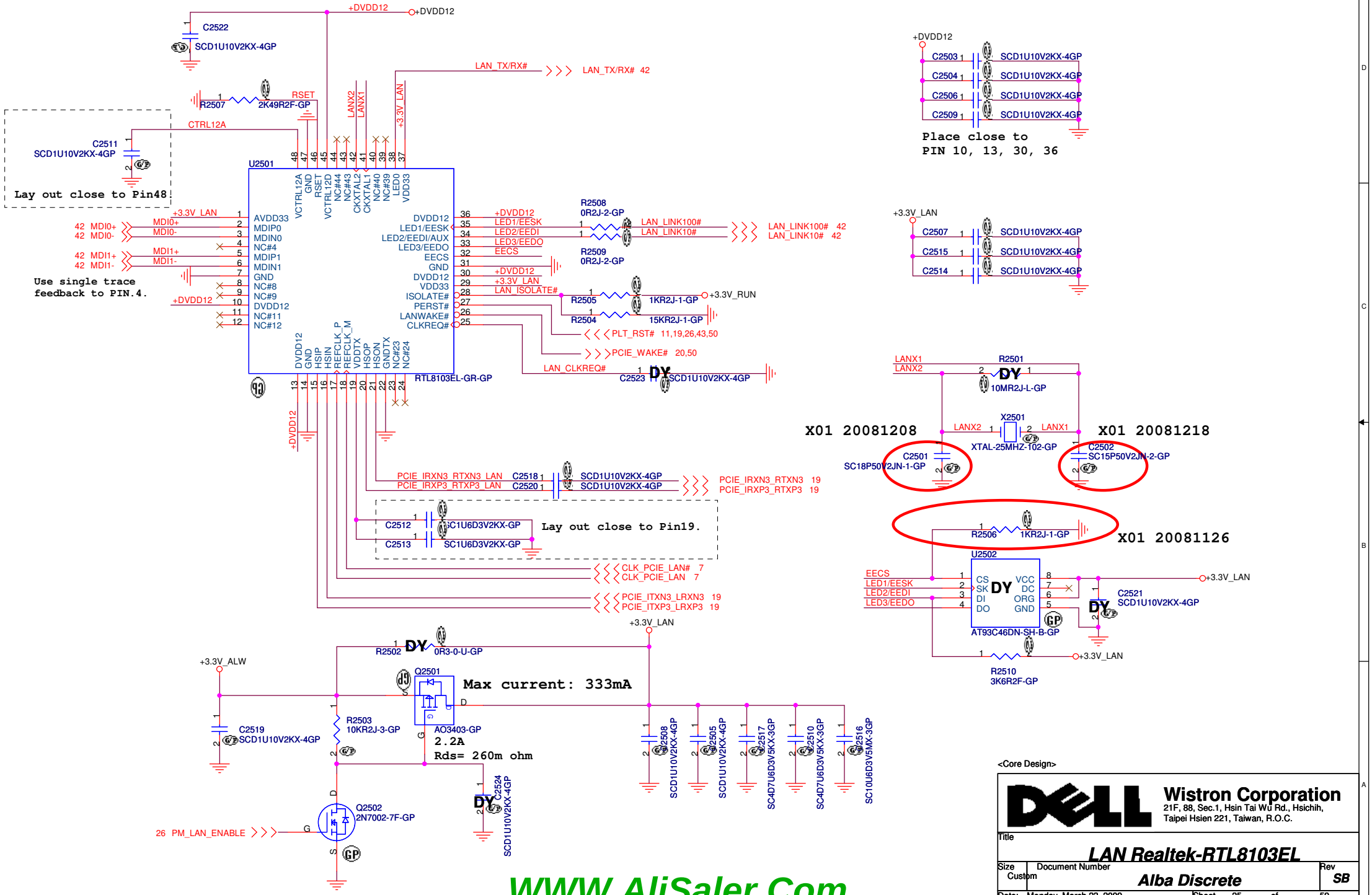
SSID = LOM



<Core Design>

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Title: LAN Realtek-RTL8103EL

Size: Custom | Document Number: Alba Discrete | Rev: SB

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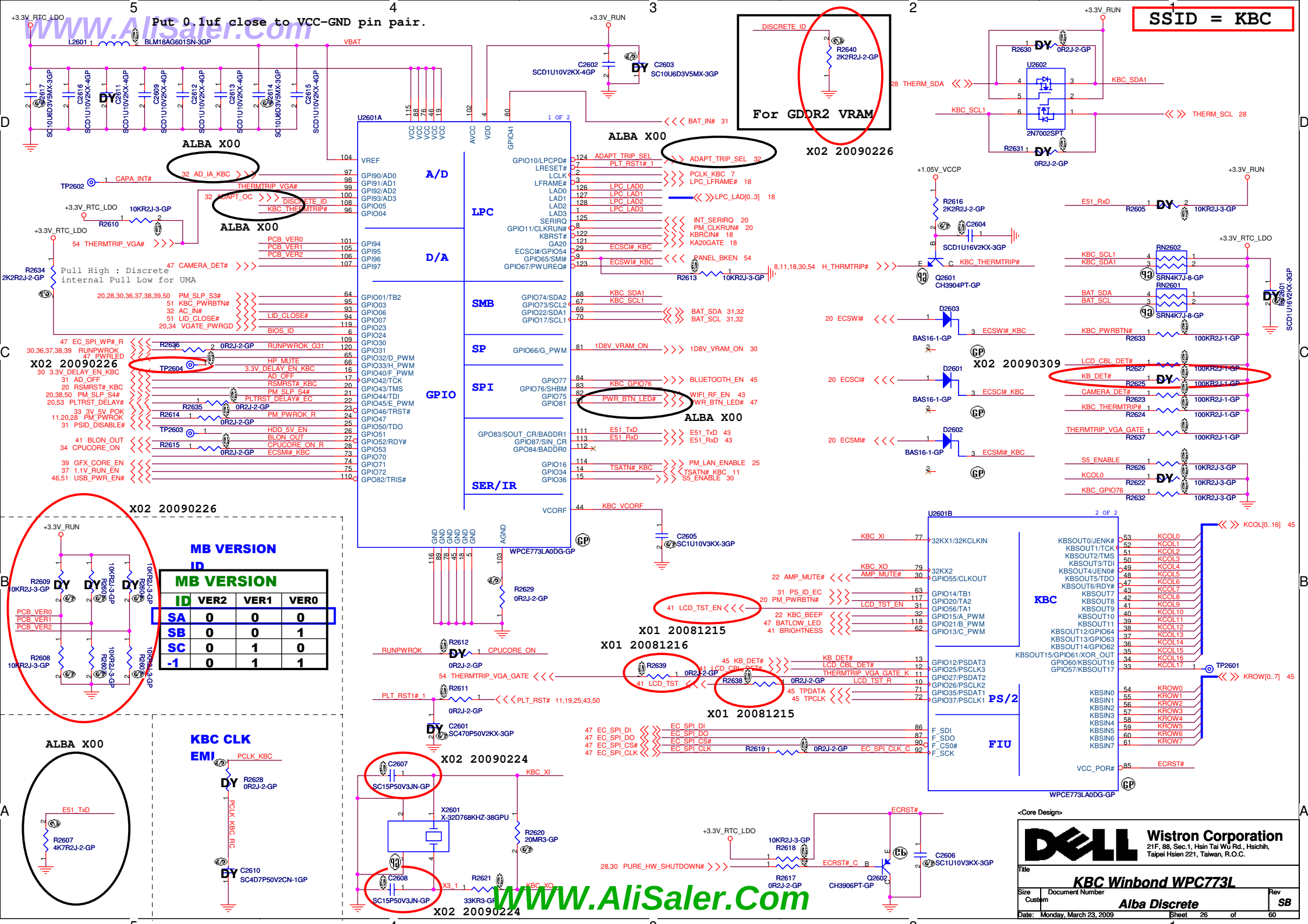
SSID = KBC
Put 0.1uf close to VCC-GND pin pair.
WWW.AliSaler.Com
For GDDR2 VRAM
X02 20090226
ALBA X00
X02 20090309
X01 20081215
X01 20081216
X02 20090224
MB VERSION ID
MB VERSION
ID VER2 VER1 VER0
SA 0 0 0
SB 0 0 1
SC 0 1 0
-1 0 1 1
KBC CLK EMI
U2601A
U2601B
WPCE773LA0DG-GP
A/D
LPC
D/A
SMB
SP
GPIO
SPI
SER/IR
KBC
PS/2
FIU
Pull High : Discrete
internal Pull Low for UMA
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KBC Winbond WPC773L
Alba Discrete
Monday, March 23, 2009

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Title: (Reserve)

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SSID = Thermal

X01 20081215

+5V_RUN
C2810 SC4D7U6D3V5KX-3GP
C2812 SCD1U16V2KX-3GP
+3.3V_RUN
R2801 10KR2J-3-GP
R2802 DY 0R2J-2-GP
+5V_RUN
R2817 DY 10KR2J-3-GP
EMC2102_FAN_TACH
D2801 B0530WS-7-F-GP
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH_1 44
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE 44
+3.3V_RTC_LDO
R2815 DY 49D9R2F-GP
RN2801 SRN4K7J-8-GP
+3.3V_RUN
THERM_SCL 26
THERM_SDA 26
+3.3V_RUN
R2814 49D9R2F-GP
EMC2102_VDD_3D3
C2803 SCD1U16V2KX-3GP
U2801
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
C2804 SC470P50V3JN-2GP
H_THERMDC
H_THERMDA
VGA_THERMDC
VGA_THERMDA
T8_THERMDC
T8_THERMDA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
EMC2102
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
+3.3V_RUN
R2812 8K2R2J-3-GP
R2810 DY 0R2J-2-GP
ALERT#
THERM_SCI# 20
R2811 0R2J-2-GP
CLK_32K
EMC2102_CLK_SEL
EM2102_RESET#
ALBA X00
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil
54 VGA_THERMDC
54 VGA_THERMDA
C2802 SC470P50V3JN-2GP
GPU Sensor
Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
ALBA X00
RN2802 SRN10KJ-5-GP
+3.3V_RUN
+3.3V_RTC_LDO
R2803 DY 10KR2J-3-GP
EMC2102_SHDN
ALBA X00
+3.3V_RUN
R2804 DY 10KR2J-2-GP
EMC2102_FAN_mode
R2805 0R2J-2-GP
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
R2818 10KR2J-3-GP
R2816 10KR2J-3-GP
Q2803 2N7002-7F-GP
PURE_HW_SHUTDOWN# 26,30
V_DEGREE
C2801 must be near Q2801
Q2801 MMBT3904-3-GP
C2801 DY SC470P50V3JN-2GP
C2805 SC470P50V3JN-2GP
C2805 must be near EMC2102
3.HW T8 sensor
Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.
TP2800 EMC2102_FAN_TACH_1
TP2801 EMC2102_FAN_DRIVE
+3.3V_RUN
C2807 SCD1U16V2KX-3GP
R2806 10KR2F-2-GP
C2806 SCD1U16V2KX-3GP
R2807 2K37R2F-GP
TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 88 deg-C.
32K suspend clock output
20 ICH_SUSCLK
Q2802 2N7002-7F-GP
CLK_32K_R
R2813 10R2J-2-GP
CLK_32K
C2809 DY SC4D7P50V2CN-1GP
RUN_POWER_ON 30
Lay out close to SKT2(CPU socket)
8 H_THERMDA
H_THERMDA
C2833 DY SC2200P50V2KX-2GP
8 H_THERMDC
H_THERMDC
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil
ALBA X00
R2833 10KR2J-3-GP DY
EM2102_RESET#
20,26,30,36,37,38,39,50 PM_SLP_S3#
U2802 74LVC1G08GW-1-GP
+3.3V_ALW
C2808 DY
SCD1U16V2KX-3GP
PM_PWROK 11,20,26

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: Custom
Document Number: Alba Discrete
Rev: SB
Date: Monday, March 23, 2009
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<Core Design>

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Title

(Reserve)

Size	Document Number	Rev
Custom	*Alba Discrete*	*SB*

Date: Monday, March 23, 2009 Sheet 29 of 59

SSID = Reset.Suspend

Max current: 115mA

Q3005
SI2301BDS-T1-GP

+3.3V_ALW
+3.3V_DELAY
X02 20090304
1.8A
Rds= 0.15 ohm
R3011
100KR2J-1-GP
C3005
SC22U6D3V5MX-2GP
3.3V_DELAY_EN#
C3007
SC1U6D3V2KX-GP
Q3003
2N7002SPT
R3015
100R2F-L1-GP-U
3.3V_DELAY_1
X01 20090112

8,18 H_PWRGOOD
R3002
1KR2J-1-GP
H_PWRGD_R
Q3001
CHT2222APT-GP
C3001
SCD1U10V2KX-4GP
H_THRMTRIP# 8,11,18,26,54
D3001
BAS16-1-GP
PURE_HW_SHUTDOWN# 26,28
33 3V_5V_EN
R3001
200KR2J-L1-GP
R3003
1KR2J-1-GP
S5_ENABLE 26

26 3.3V_DELAY_EN_KBC
3.3V_DELAY_EN_KBC
R3013
0R2J-2-GP
26,36,37,38,39 RUNPWROK
R3012
75KR2F-GP
3.3V_DELAY_EN
C3006
SCD1U16V2KX-3GP
Optional RC network to fine tune PWR SEQ.

+3.3V_RTC_LDO
R3009
100KR2J-1-GP
X01 20081215
PM_RUN_EN#
Q3002
2N7002SPT
+15V_ALW
R3010
10KR2J-3-GP
20,26,28,36,37,38,39,50 PM_SLP_S3#
RUN_POWER_ON 28

Max current: 6243.3mA
+5V_RUN
+5V_ALW
R3005
10KR2J-3-GP
RUN_ON_5V
U3001
AO4468-GP
11.6A
Rds=14m ohm
C3002
SC6800P25V2KX-1GP

Max current: 4865.6mA
+3.3V_RUN
+3.3V_ALW
R3004
10KR2J-3-GP
RUN_ON_3D3V
U3002
AO4468-GP
11.6A
Rds=14m ohm
C3003
SCD01U50V2KX-1GP

+3.3V_RTC_LDO
R3014
100KR2J-1-GP
1D8V_VRAM_ON#
+15V_ALW
R3008
10KR2J-3-GP
+1.8V_RUN
R3016
10R3F-GP
Q3006
2N7002-7F-GP
2N7002SPT
Q3004
X01 20090112
26 1D8V_VRAM_ON
1D8V_VRAM_ON

+1.8V_RUN
C3033
SC10U6D3V5KX-1GP
Max current: 5386mA
+1.8V_SUS
RUN_ON_1D8V
U3003
FDS8880-NL-GP
10.7A
Rds=12m ohm
C3004
SCD01U50V2KX-1GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

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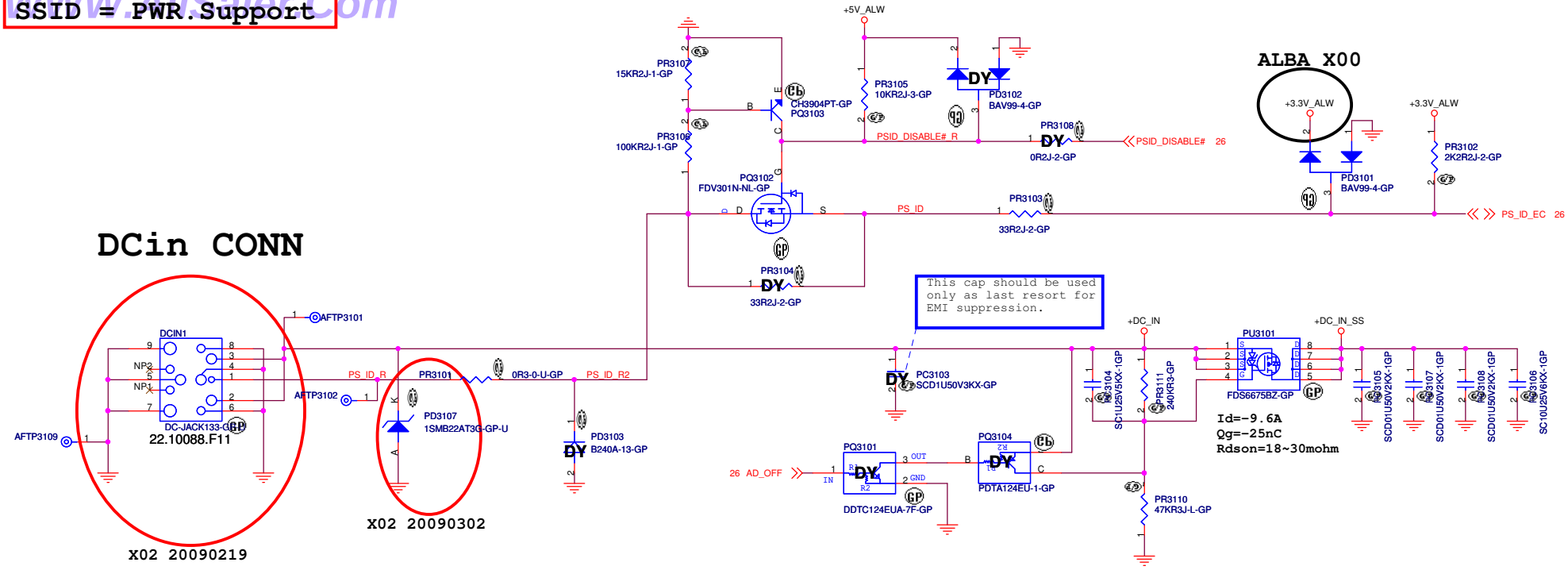
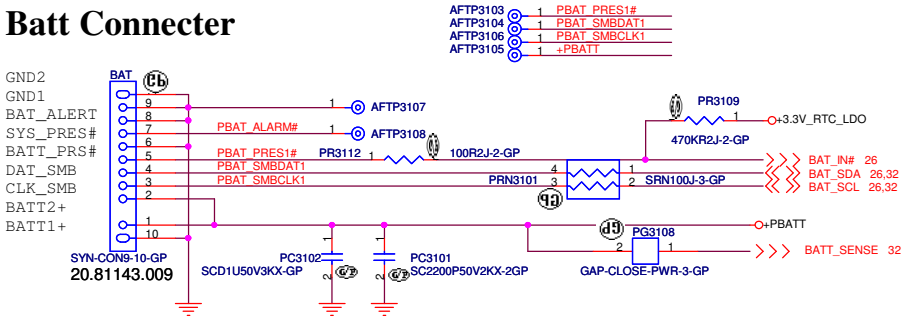
SSID = PWR.Support

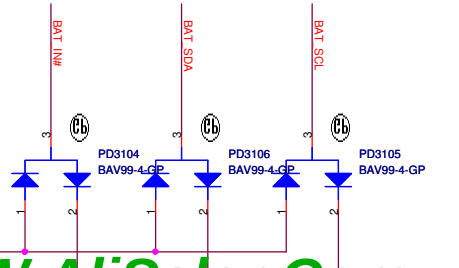
ALBA X00

DCin CONN



Batt Connecter





<Core Design>

Wistron Corporation
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Title: DC IN/BATT CONN/USB CONN

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 31 of 59

SSID = Charger

Adaptor In Soft-Start Circuit

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm
Layout Trace 250mil

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm
Layout Trace 300mil

Layout Trace 300mil

Layout Trace 300mil

X02 20090302

X02 20090302

X01 20081215

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR3202	PR3205	PR3207	PR3208
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor

ADAPT_TRIP_SEL=1 Adapter is 90w

ADAPT_TRIP_SEL=0 Adapter is 65w

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

Size: Custom | Document Number: Alba Discrete | Rev: SB

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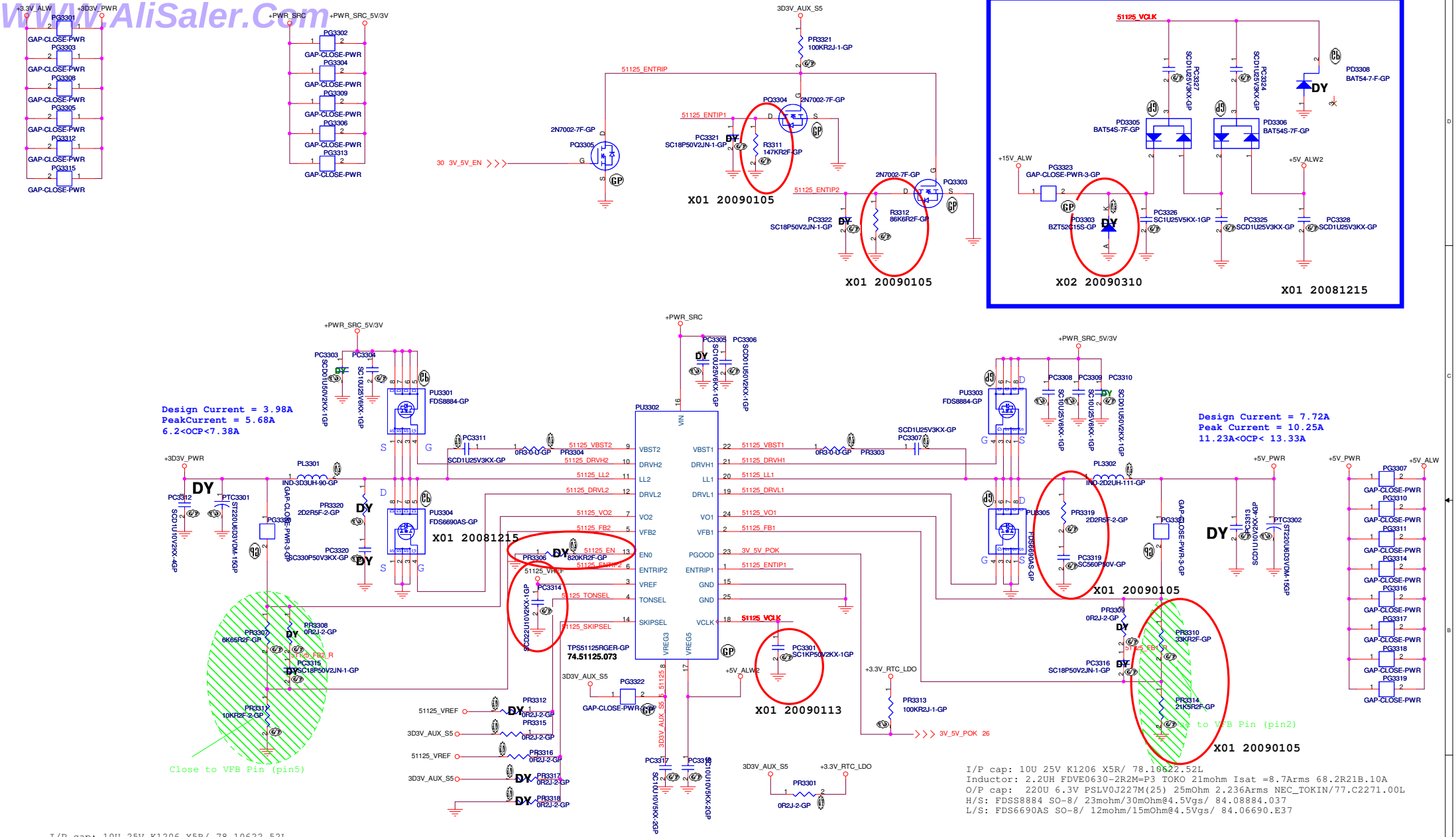


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH FDV0630-3R3M=P3 TOKO 31mohm Isat =6.9Arms 68.3R31A.10E
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

Eiger

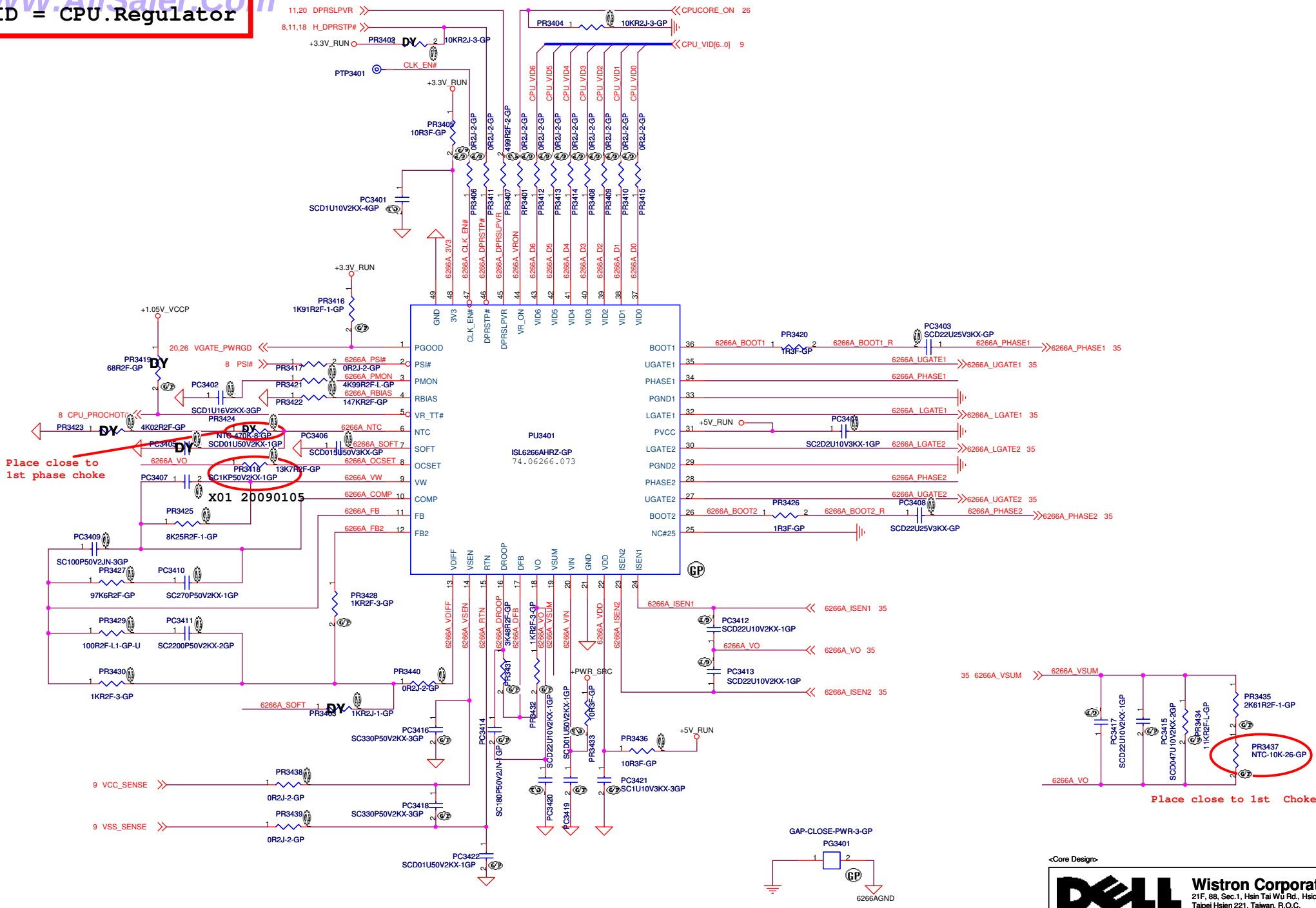
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 33 of 59

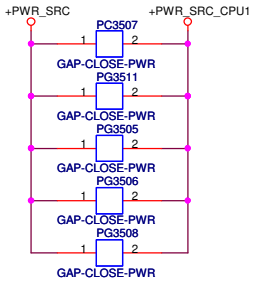
SSID = CPU.Regulator

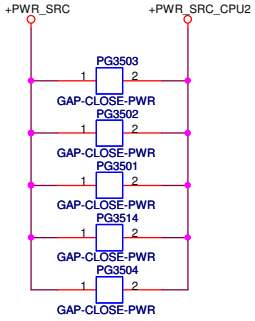


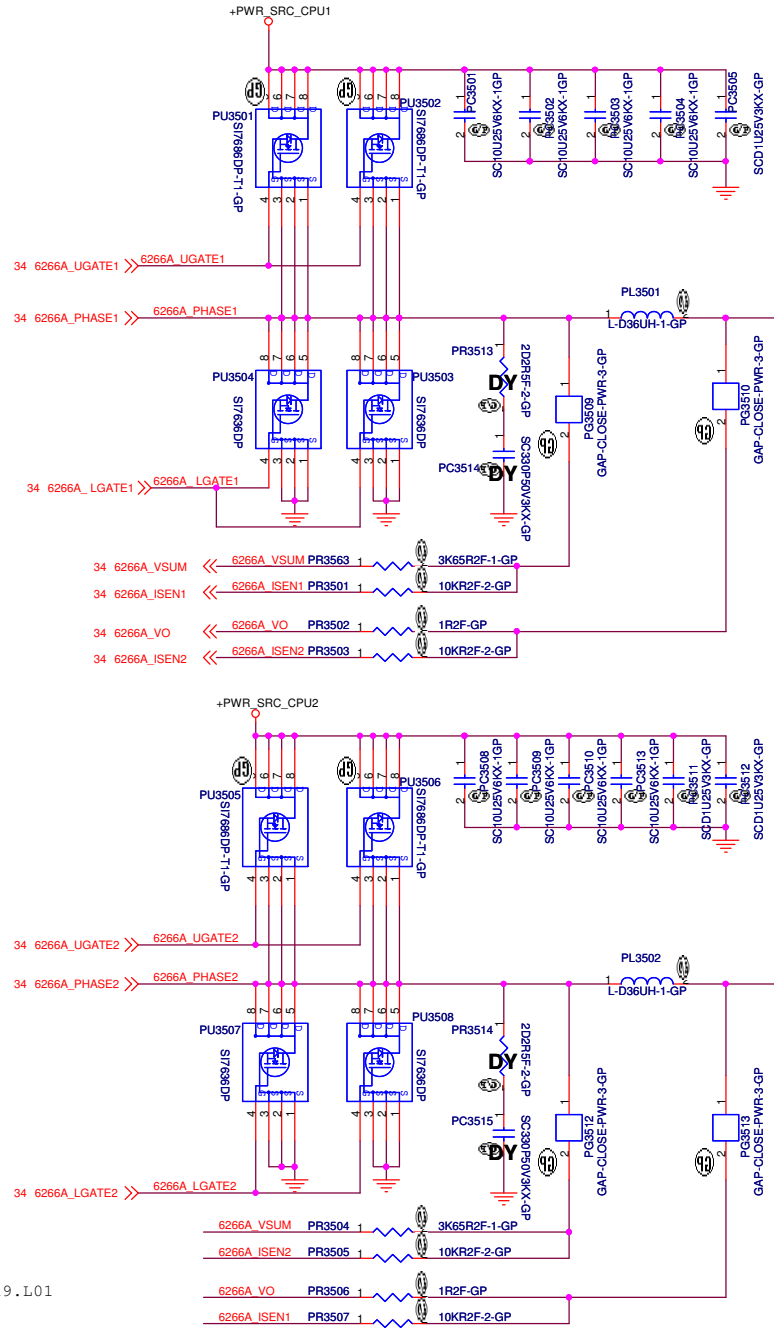
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

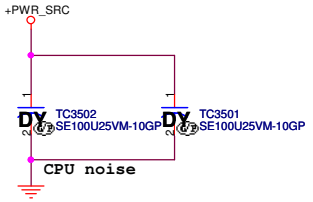
Title: CPU VCORE POWER(1/2)
Size: Custom
Document Number: Alba Discrete
Rev: SB
Date: Monday, March 23, 2009
Sheet 34 of 59

SSID = CPU.Regulator









I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

<Core Design>

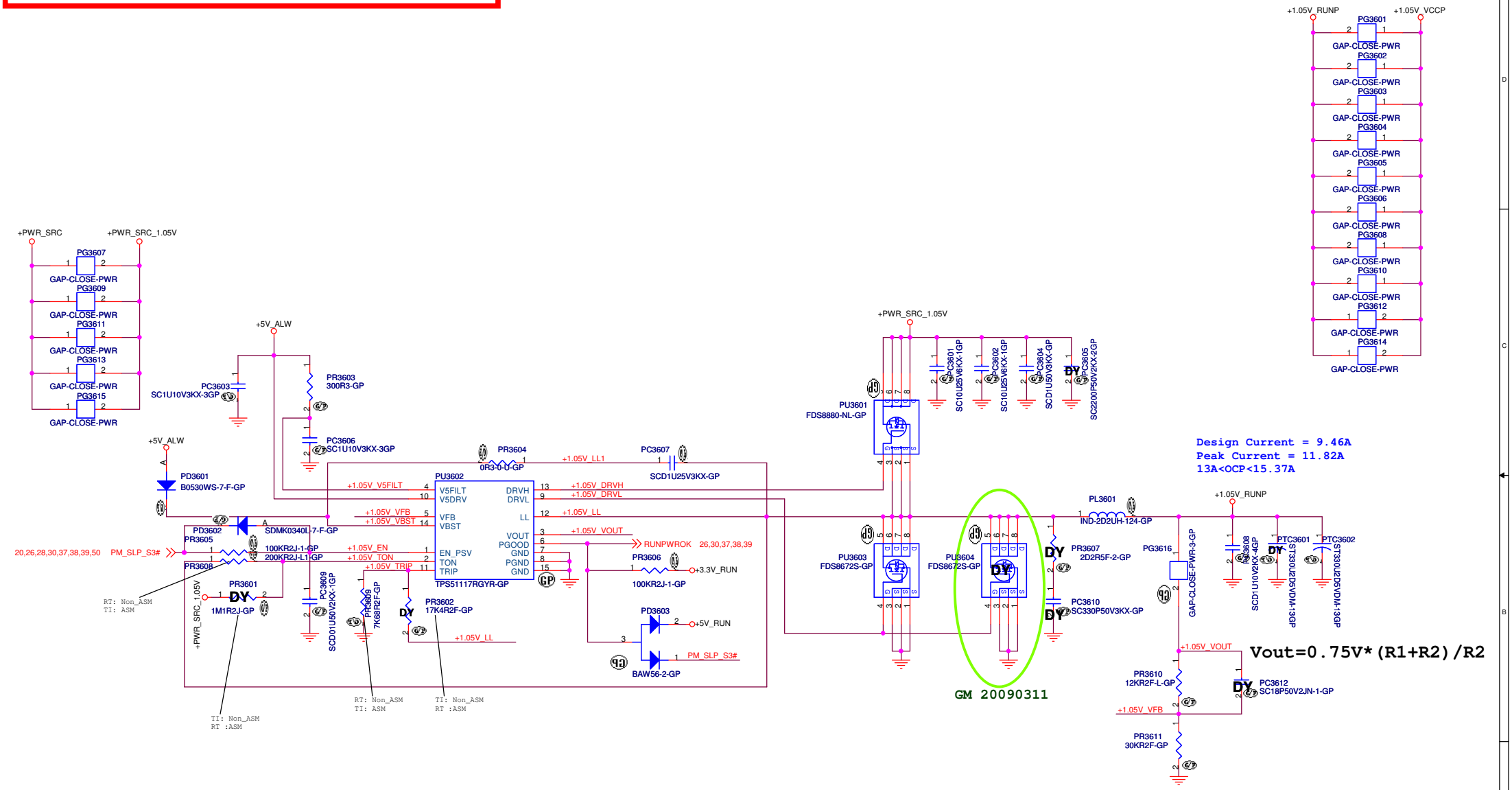
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 35 of 59

SSID = PWR.Plane.Regulator_1p05v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->350KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 1.05V	
Size: Custom	Document Number: Alba Discrete	Rev: SB
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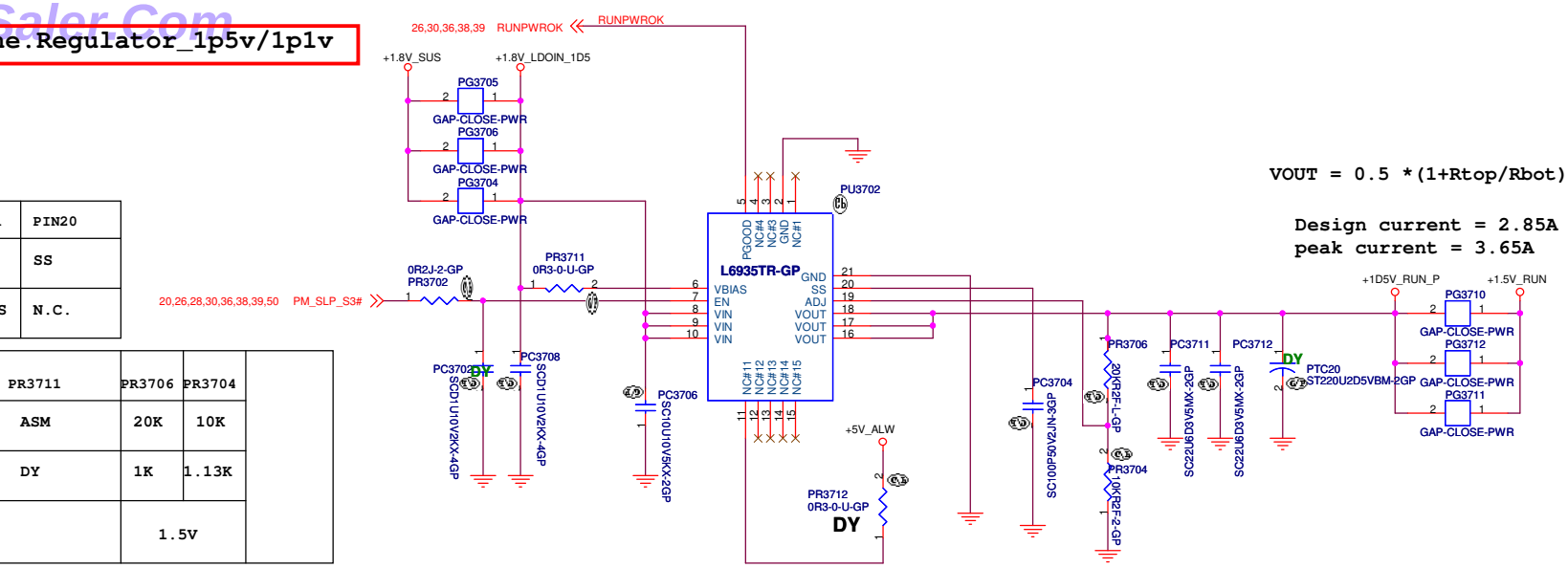
SSID = PWR.Plane.Regulator_1p5v/1p1v

Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

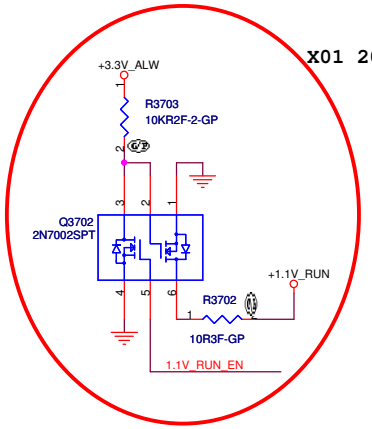
Vendor	PR3712	PR3711	PR3706	PR3704	
L6935	DY	ASM	20K	10K	
RTXX35	ASM	DY	1K	1.13K	
			1.5V		



VOUT = 0.5 *(1+Rtop/Rbot)

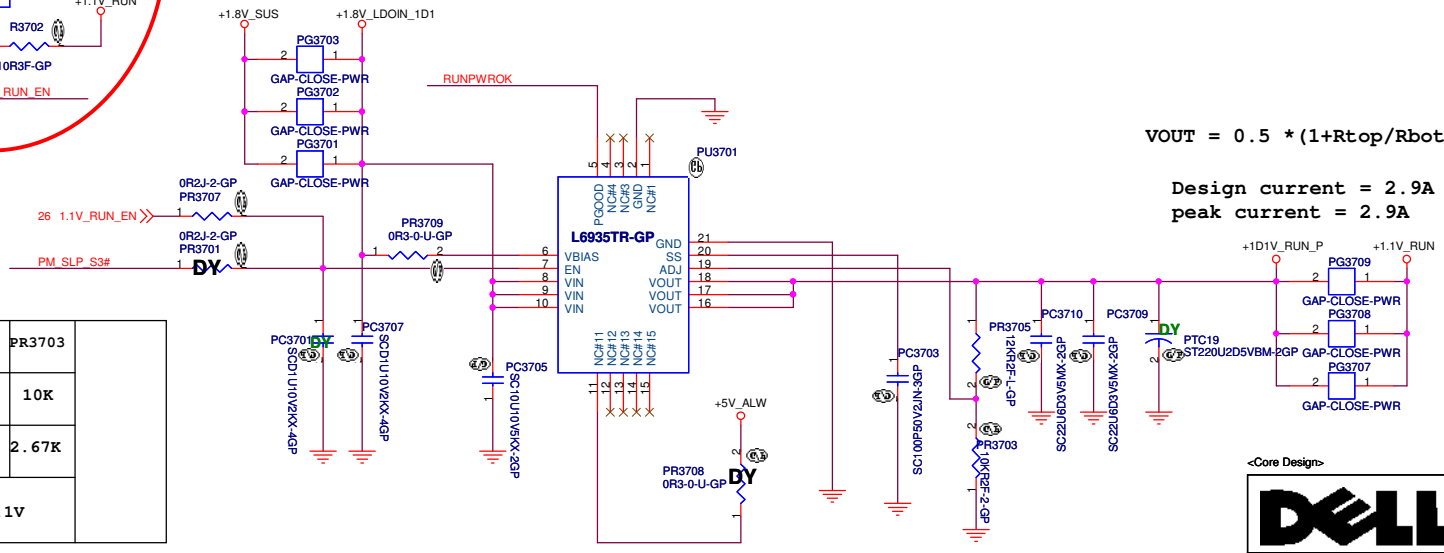
Design current = 2.85A
peak current = 3.65A

X01 20090112



Vendor	PIN6	PIN11	PIN20
L6935	VBIAS	N.C.	SS
RTXX35	N.C.	VBIAS	N.C.

Vendor	PR3708	PR3709	PR3705	PR3703	
L6935	DY	ASM	20K	10K	
RTXX35	ASM	DY	1.02K	2.67K	
			1.1V		



VOUT = 0.5 *(1+Rtop/Rbot)

Design current = 2.9A
peak current = 2.9A

<Core Design>

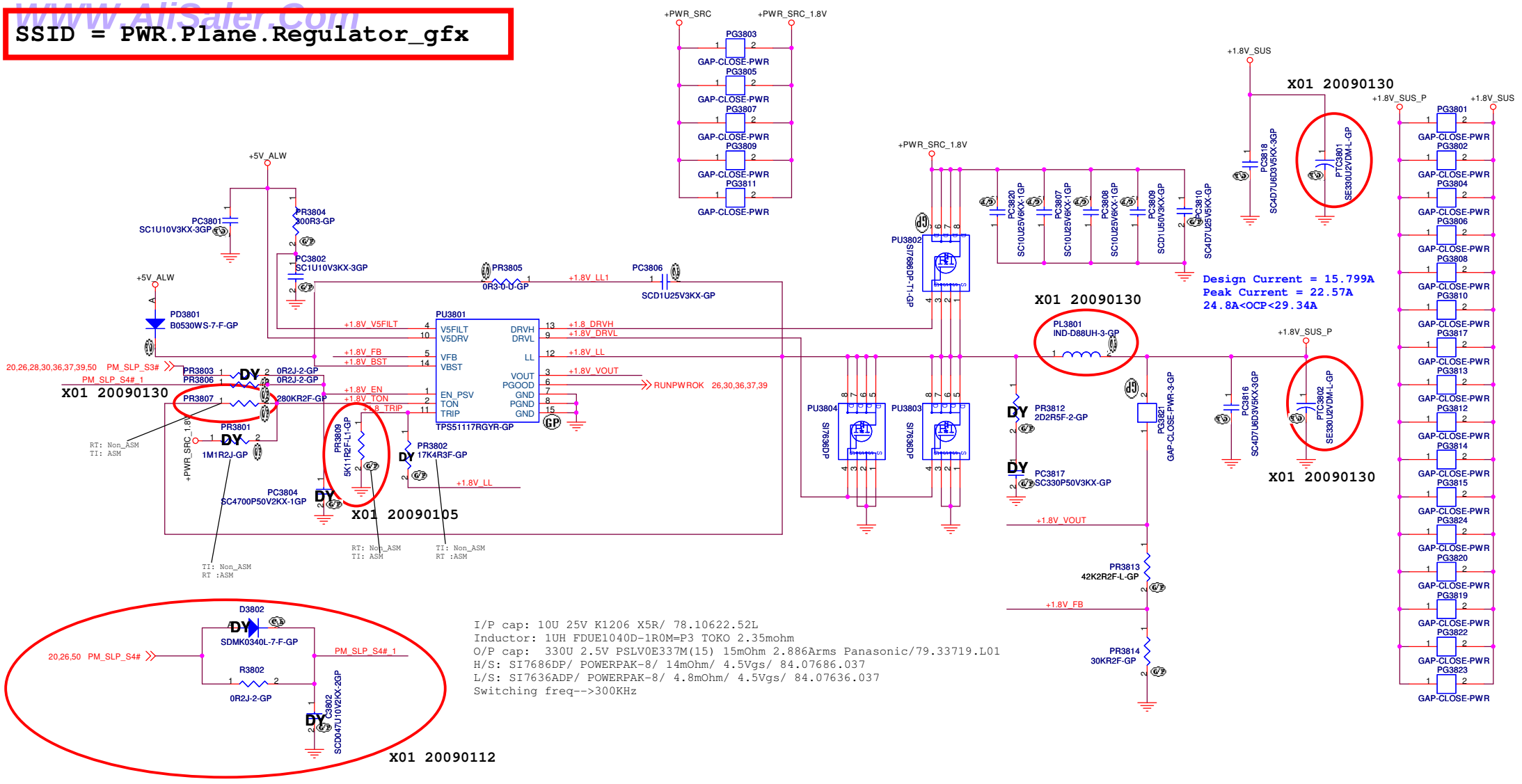
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

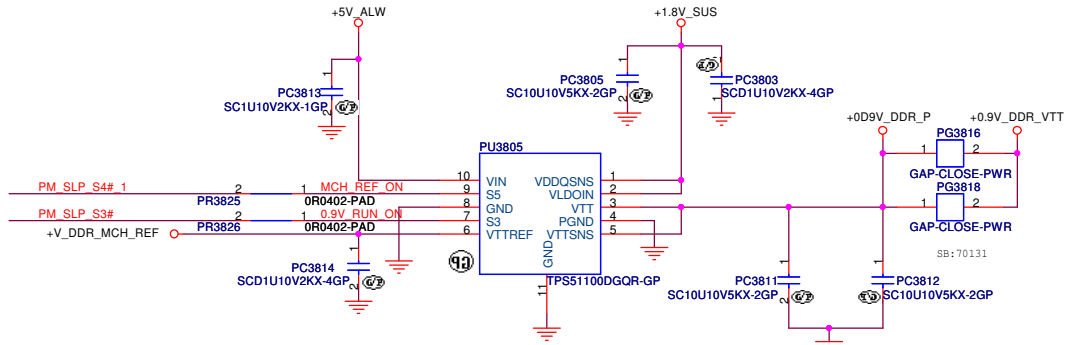
Title: DC to DC L6935_1.5V / L6935_1.1V

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 37 of 59

SSID = PWR.Plane.Regulator_gfx





<Core Design>

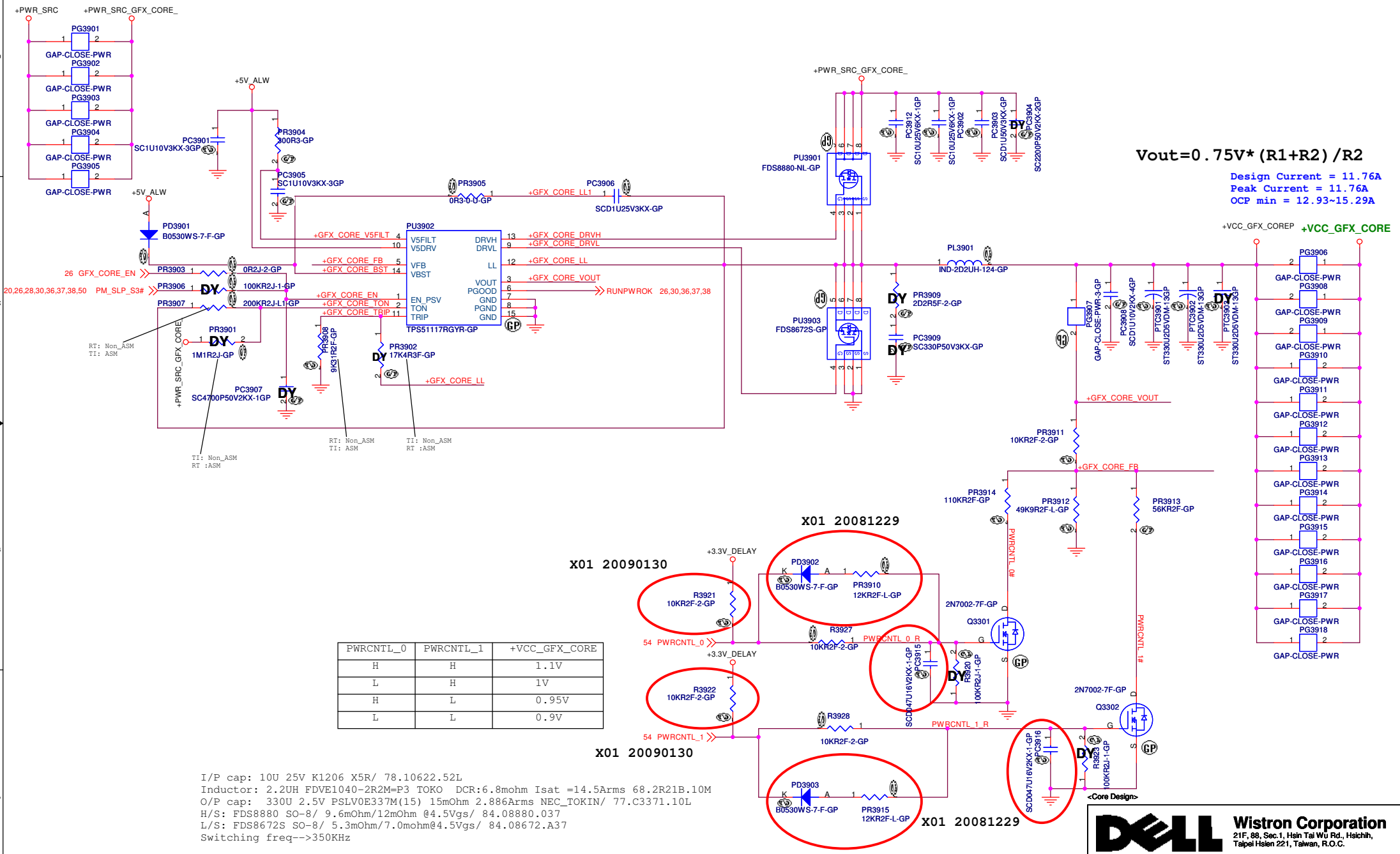
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.8V/0.9V

Size: A3 | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 38 of 59

SSID = PWR.Plane.Regulator_gfx



PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.1V
L	H	1V
H	L	0.95V
L	L	0.9V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->350KHz

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE
Size: A3 | Document Number: Alba Discrete | Rev: SB
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(Blank)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserve)

Size: Custom | Document Number: Alba Discrete | Rev: SB

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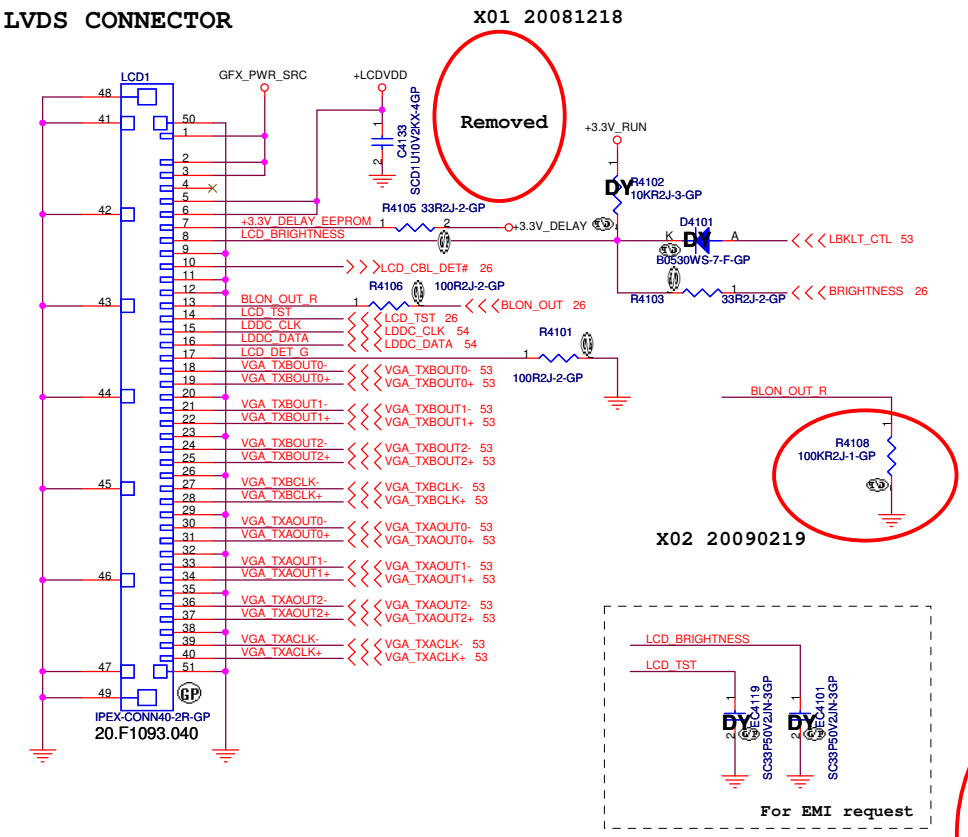
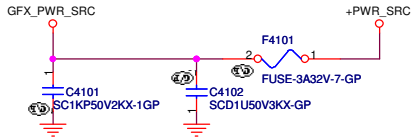
SSID = VIDEO

LVDS CONNECTOR

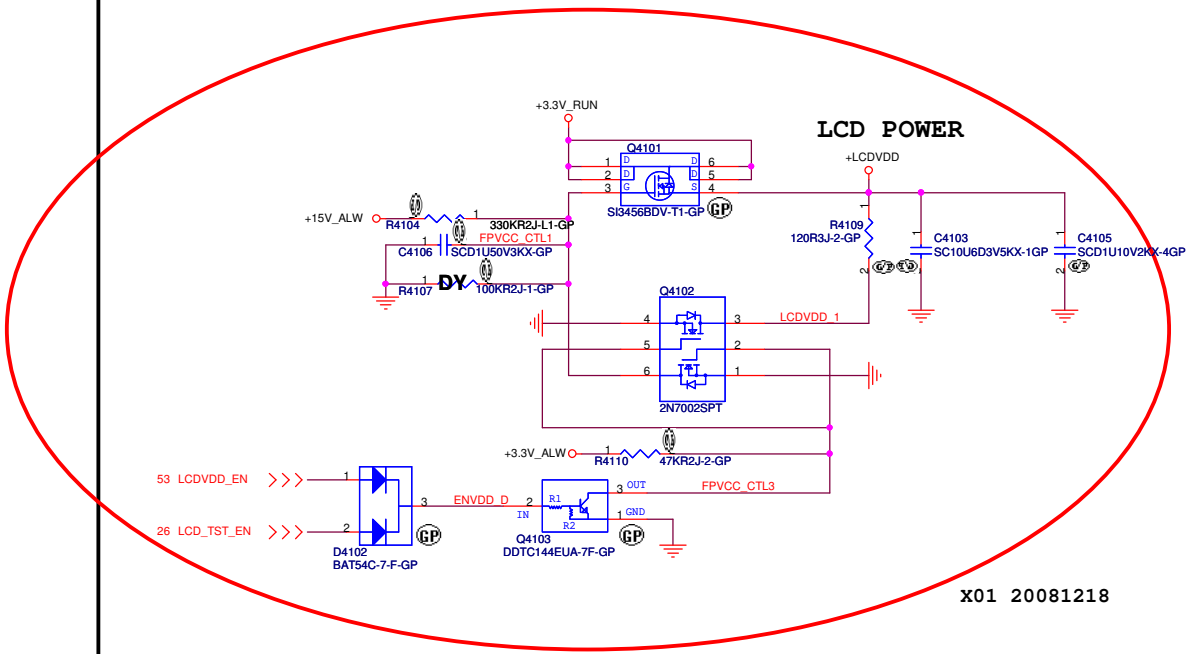


SSID = Inverter

INVERTER POWER



SSID = VIDEO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: Custom | Document Number: Alba Discrete | Rev: SB

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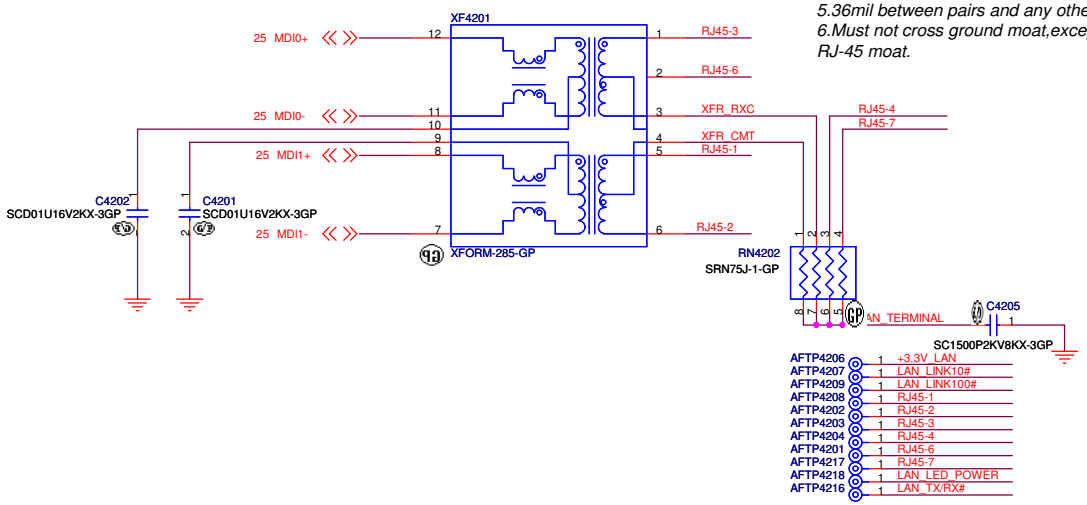
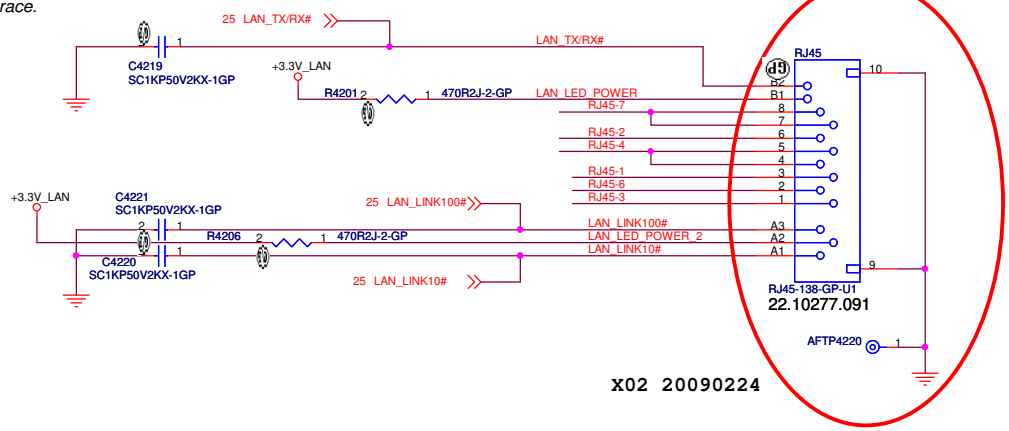
SSID = LOM

1.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
2.No vias, No 90 degree bends.
3.pairs must be equal lengths.
4.6mil trace width,12mil separation.
5.36mil between pairs and any other trace.
6.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector

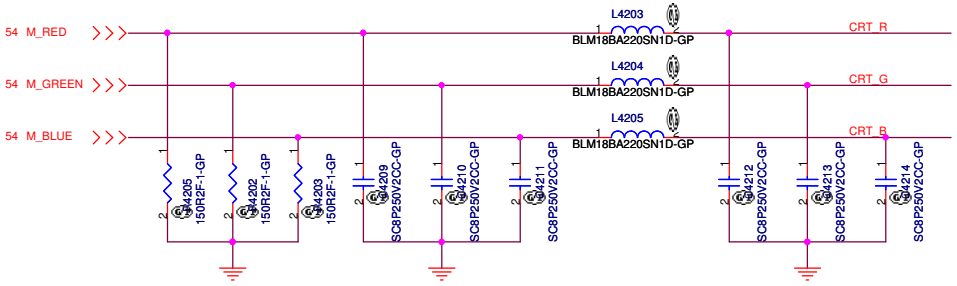


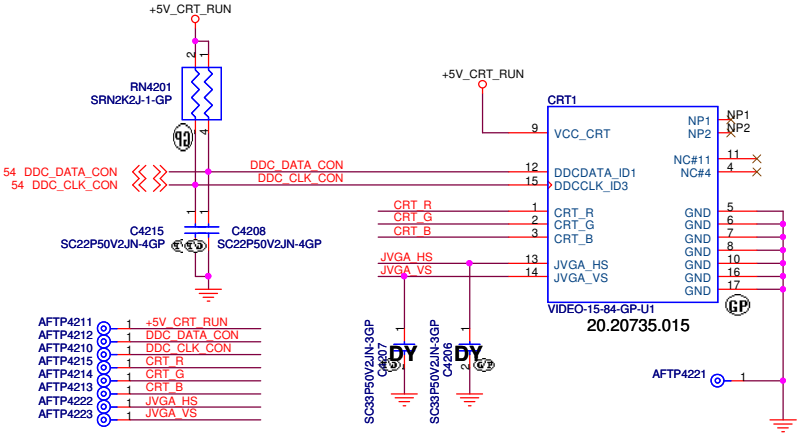
X02 20090224

SSID = VIDEO

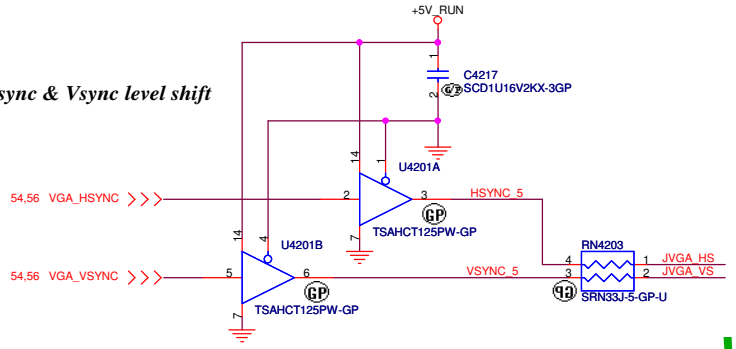
Layout Note:

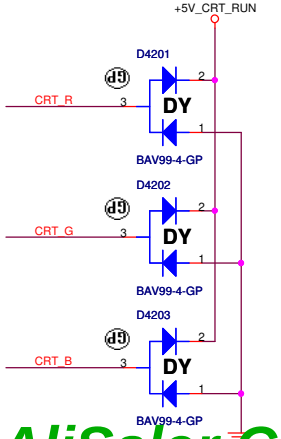
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

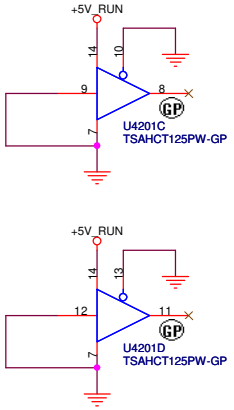


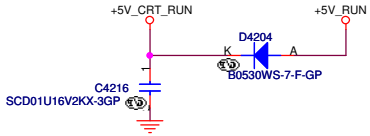


Hsync & Vsync level shift









<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN/CRT Connector
Size: Custom | Document Number: Alba Discrete | Rev: SB
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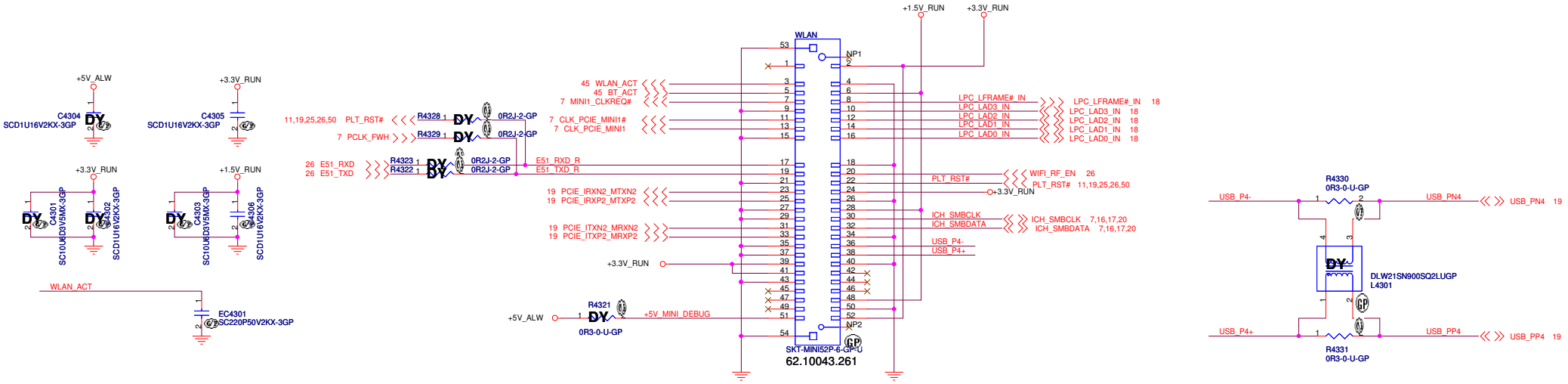
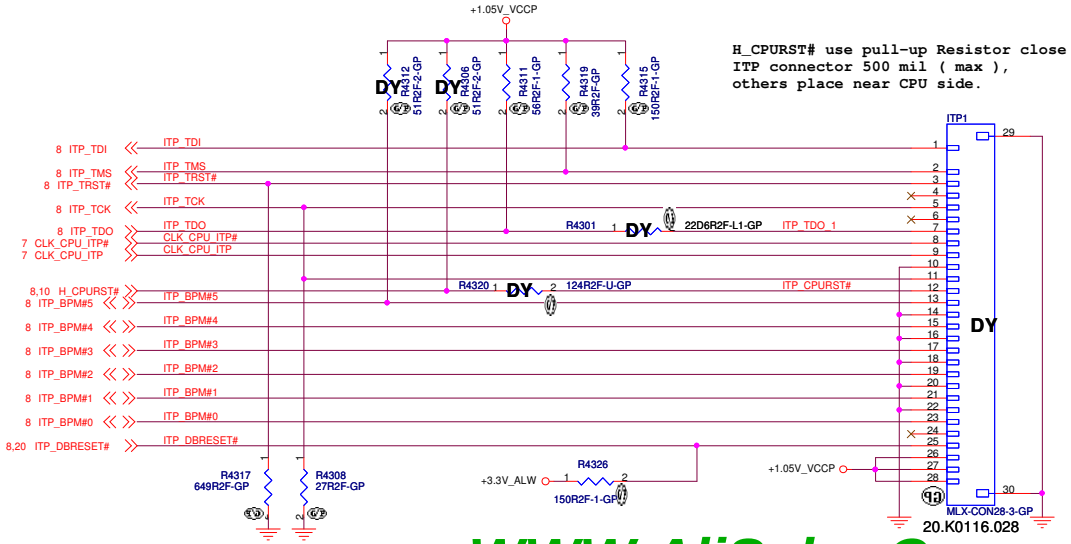
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



SSID = User.Interface

ITP Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size: Custom | Document Number: Alba Discrete | Rev: SB

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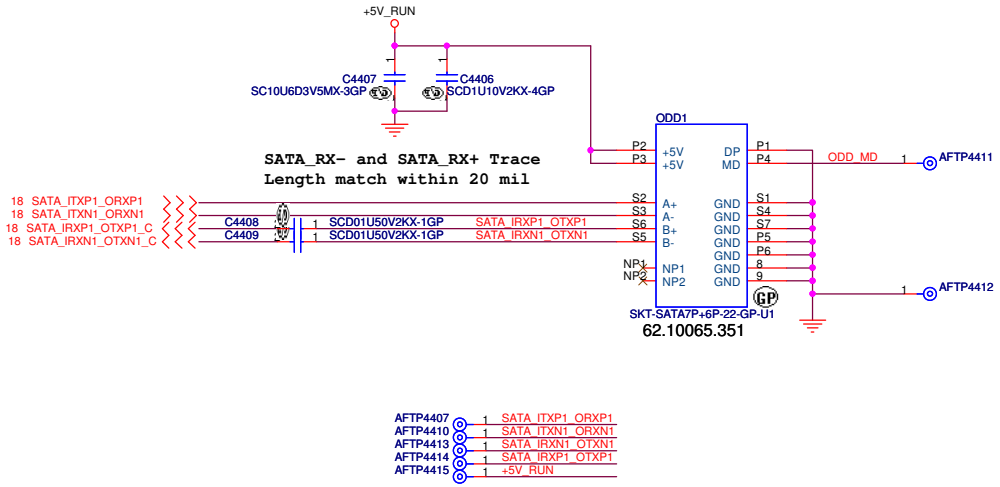
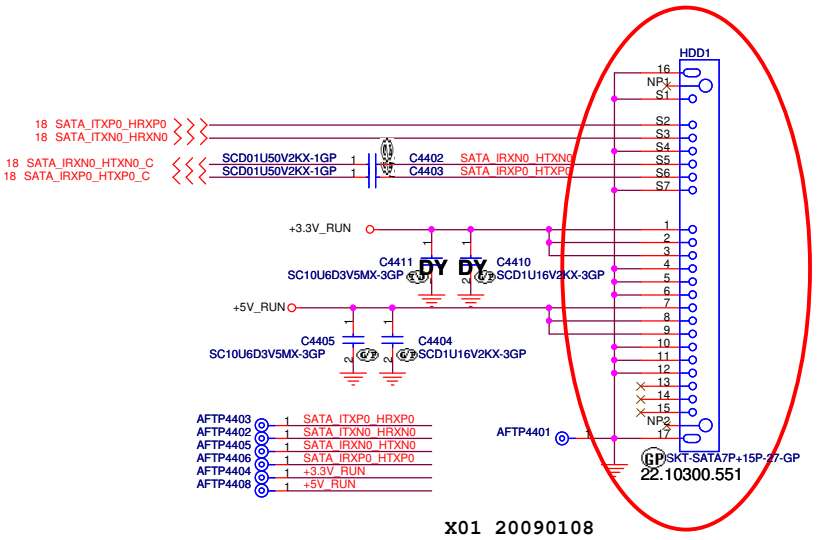
SSID = SATA

ODD Connector



SSID = SATA

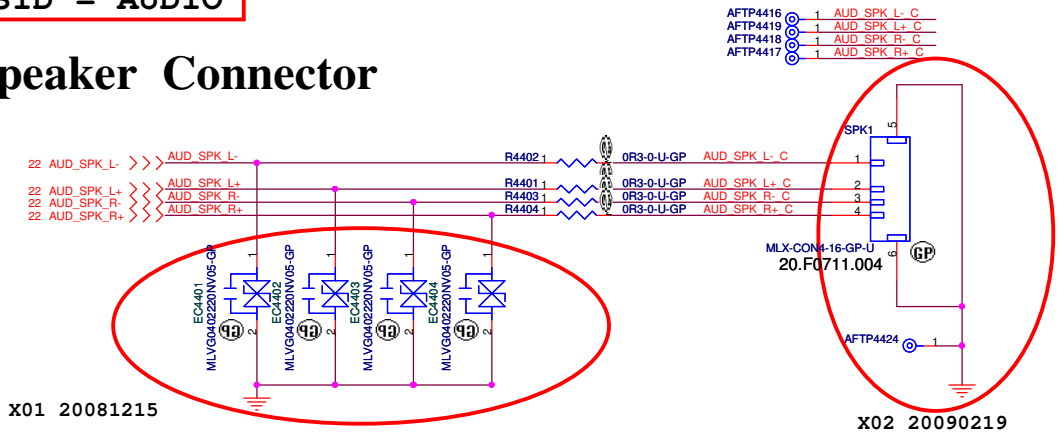
SATA HDD Connector



X01 20090108

SSID = AUDIO

Speaker Connector

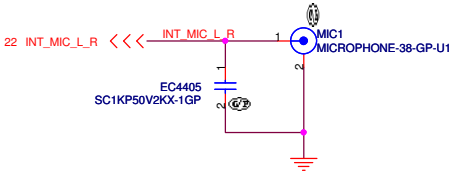


X01 20081215

X02 20090219

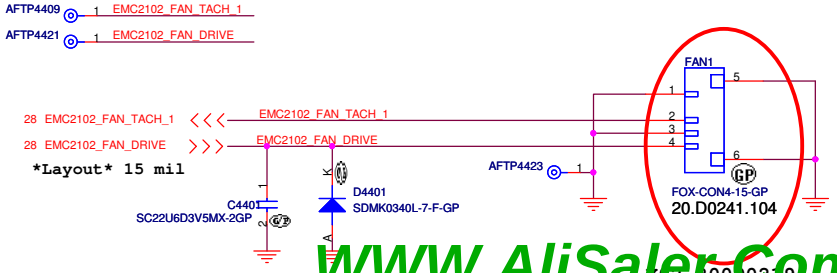
SSID = AUDIO

Internal MIC



SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD/FAN/SPEAKER/MIC

Size	Document Number	Rev
Custom	Alba Discrete	SB

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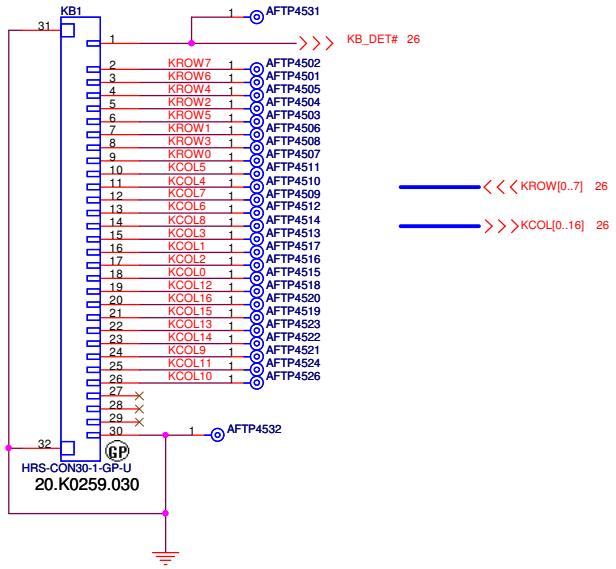
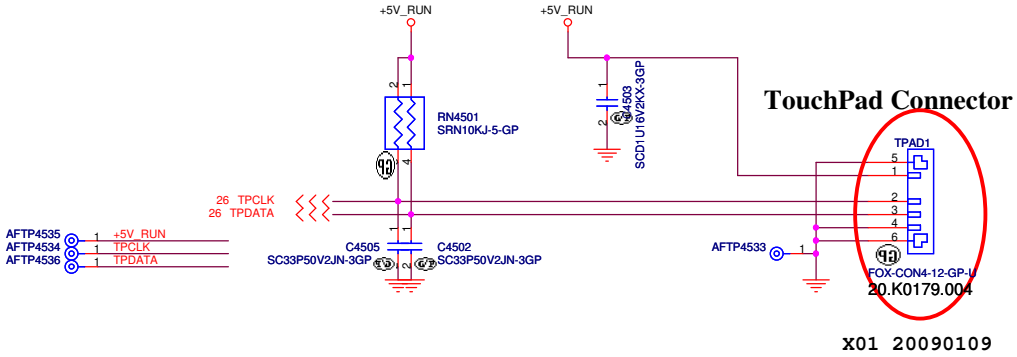
SSID = KBC

Internal KeyBoard Connector



SSID = Touch.Pad

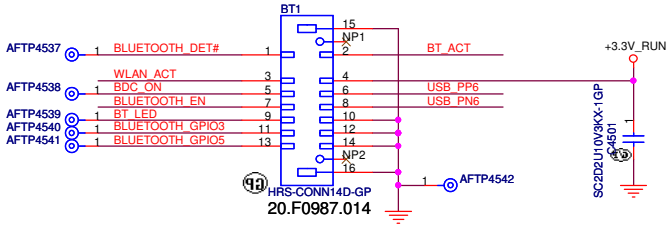


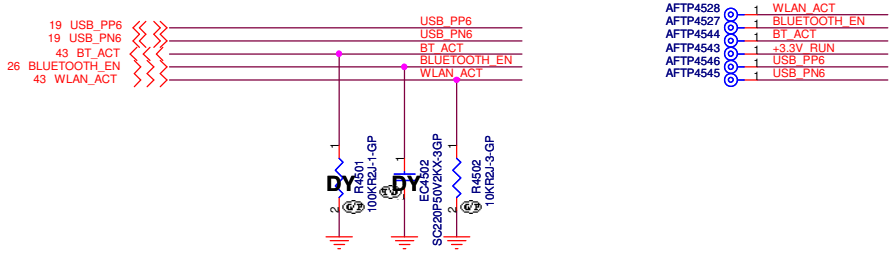
TouchPad Connector

X01 20090109

SSID = User.Interface

Bluetooth Module conn.





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard/TouchPad/BT

Size: Custom | Document Number: Alba Discrete | Rev: SB

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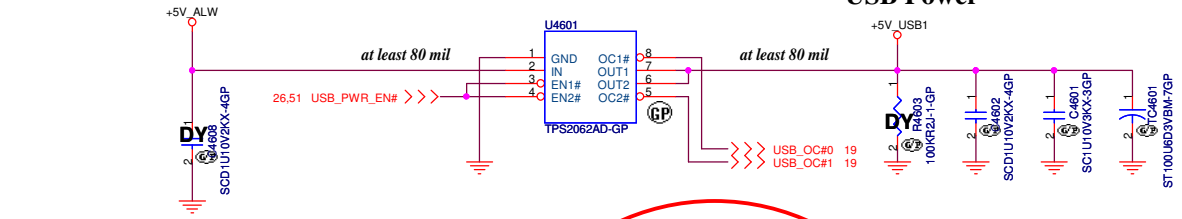
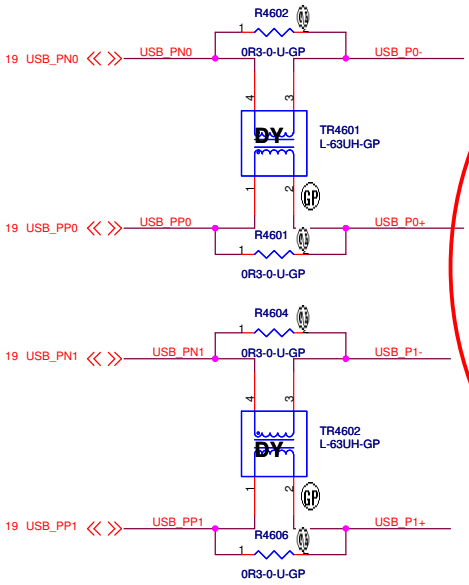
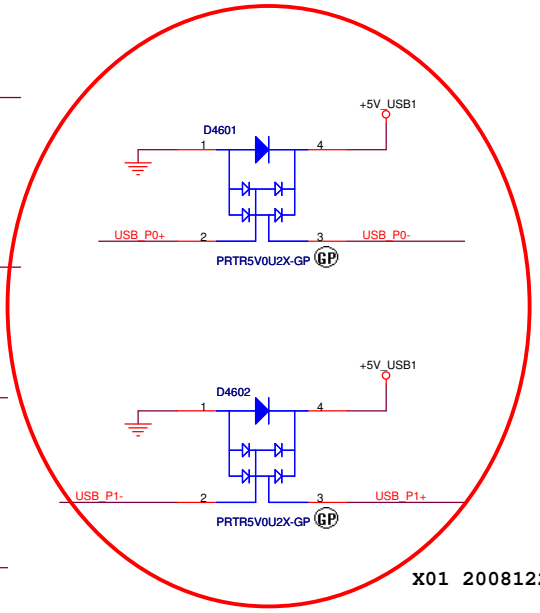
Remove Modem

X01 20081208

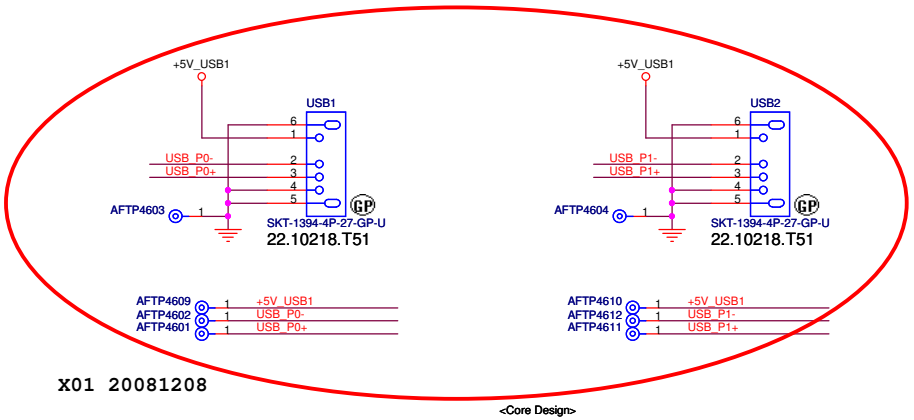
USB Power







X01 20081222



X01 20081208

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC CONN

Size: Custom | Document Number: Alba Discrete | Rev: SB

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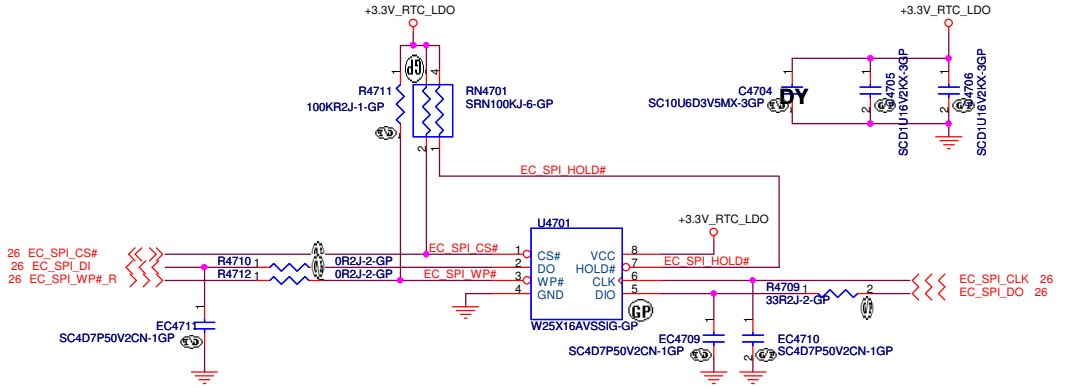
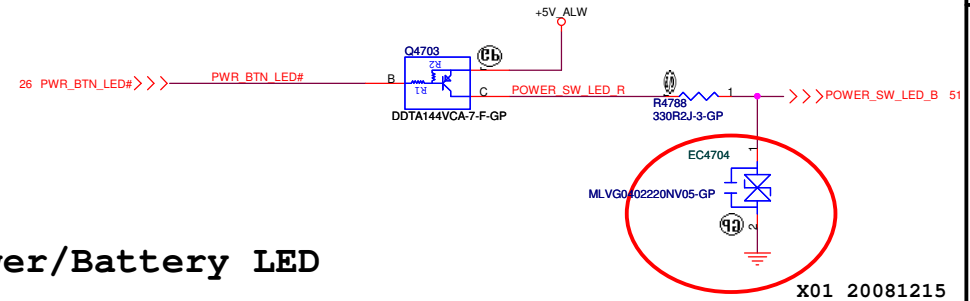
SSID = Flash.ROM

SPI FLASH ROM (16M bits)



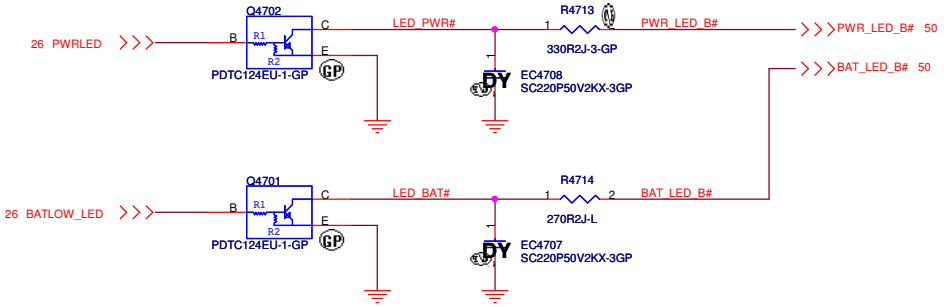
SSID = User.Interface

Power Button LED



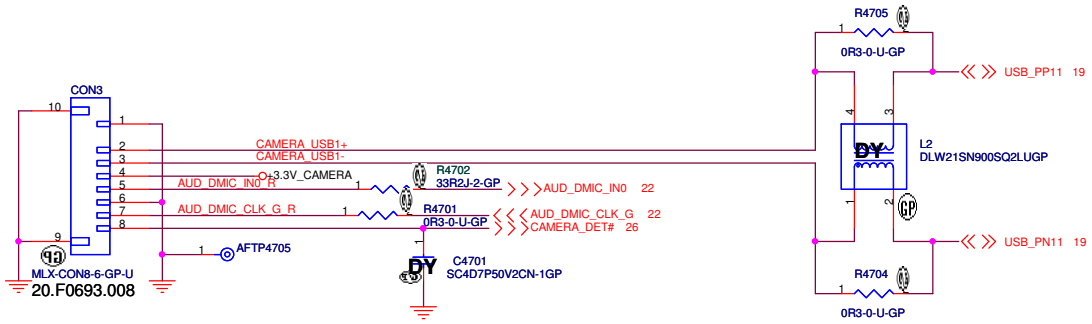
X01 20081215

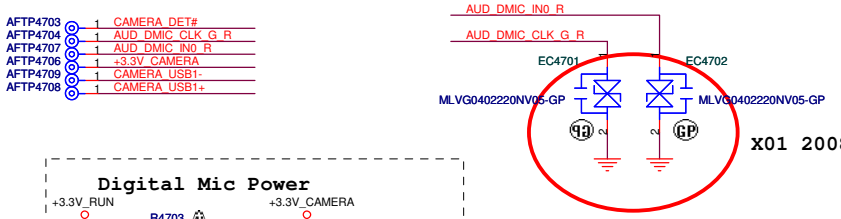
Power/Battery LED



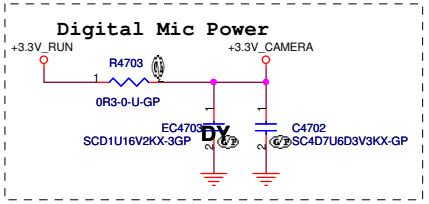
Camera Connector

SSID = User.Interface



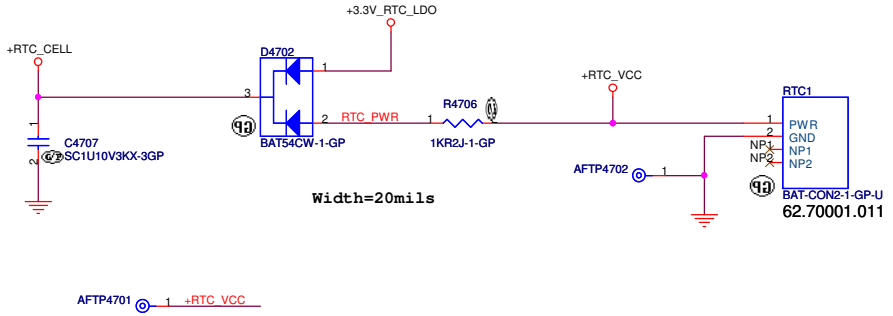


X01 20081215



SSID = RBATT

RTC Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPI Flash/LED/Camera/RTC

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 47 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserve)

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 48 of 59

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

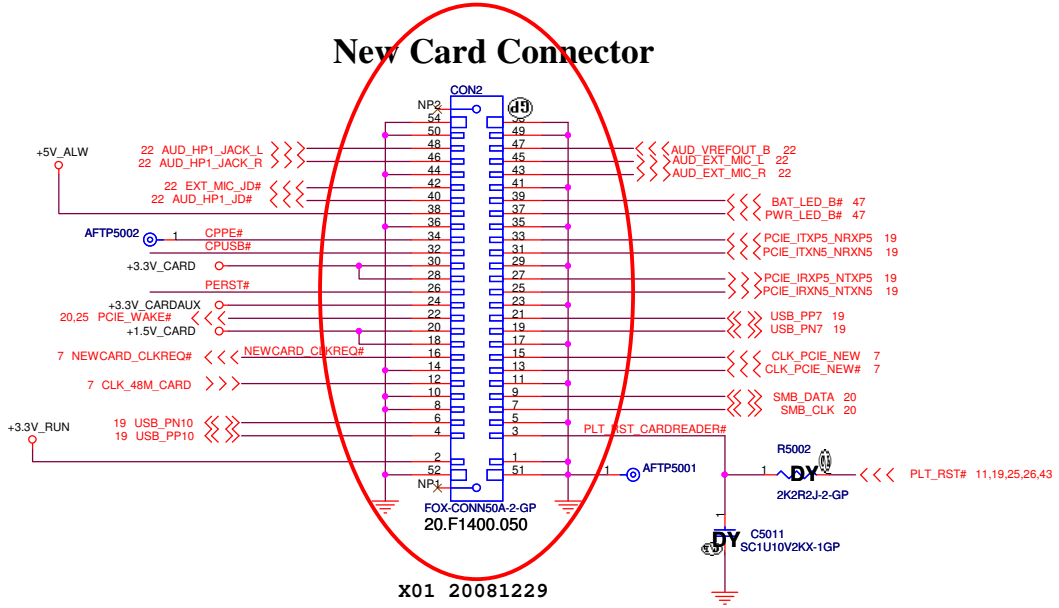
Title: (Reserve)

Size: Custom | Document Number: Alba Discrete | Rev: SB

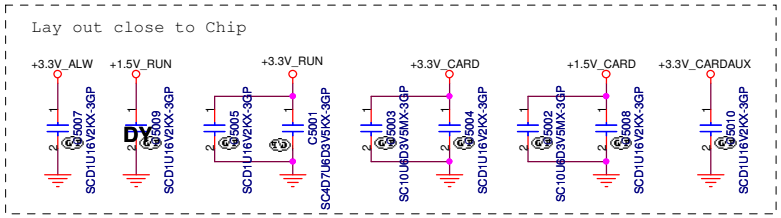
Date: Monday, March 23, 2009 | Sheet 49 of 59

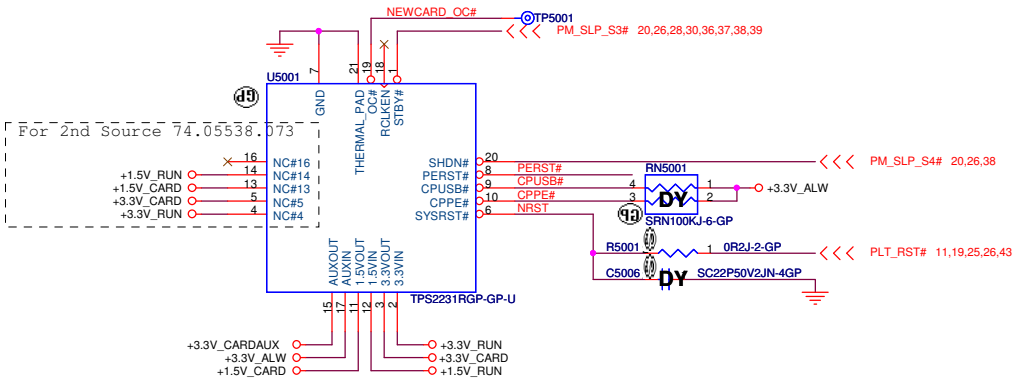
SSID = ExpressCard

New Card Connector



X01 20081229





+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

AFTP5029 1 PWR_LED_B#
AFTP5032 1 BAT_LED_B#
AFTP5031 1 +5V_ALW
AFTP5030 1 PLT_RST_CARDREADER#
AFTP5020 1 PCIE_ITXP5_NRXP5
AFTP5025 1 PCIE_ITXN5_NRXN5
AFTP5023 1 PCIE_IRXP5_NTXP5
AFTP5024 1 PCIE_IRXN5_NTXN5
AFTP5026 1 AUD_VREFOUT_B
AFTP5004 1 AUD_HP1_JACK_L
AFTP5006 1 AUD_HP1_JACK_R
AFTP5007 1 +3.3V_RUN
AFTP5009 1 CPUSB#
AFTP5005 1 USB_PP7
AFTP5008 1 USB_PN7
AFTP5011 1 AUD_EXT_MIC_L
AFTP5010 1 AUD_EXT_MIC_R
AFTP5017 1 EXT_MIC_JD#
AFTP5013 1 AUD_HP1_JD#
AFTP5014 1 CLK_48M_CARD
AFTP5012 1 NEWCARD_CLKREQ#
AFTP5019 1 +3.3V_CARD
AFTP5015 1 PERST#
AFTP5022 1 +3.3V_CARDAUX
AFTP5021 1 PCIE_WAKE#
AFTP5016 1 +1.5V_CARD
AFTP5018 1 SMB_DATA
AFTP5003 1 SMB_CLK
AFTP5027 1 USB_PN10
AFTP5028 1 USB_PP10

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

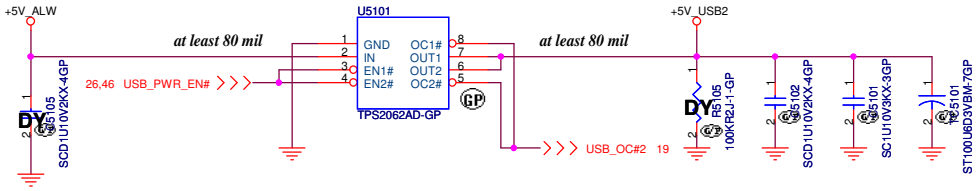
Title: **Express Card Board CONN**

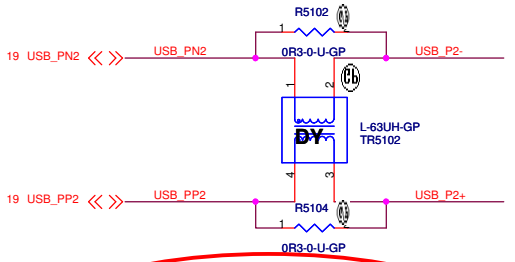
Size: Custom | Document Number: **Alba Discrete** | Rev: **SB**

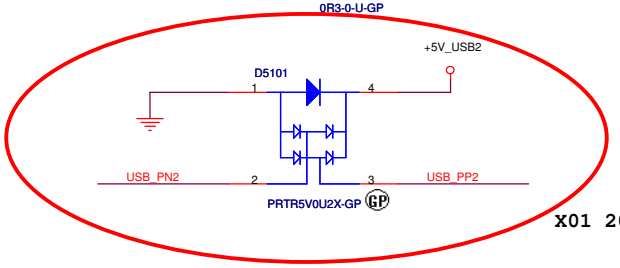
Date: Monday, March 23, 2009 | Sheet 50 of 59

SSID = USB

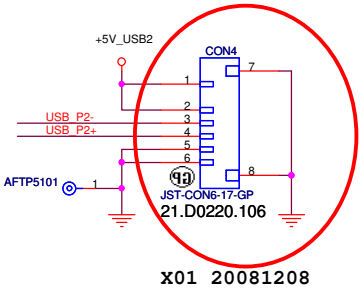
USB Power



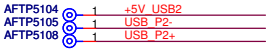




X01 20081222



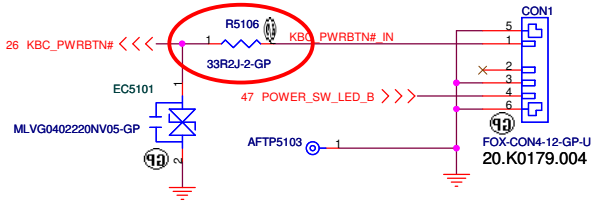
X01 20081208

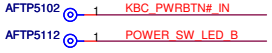


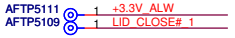
SSID = User.Interface

Power Button Board CONN

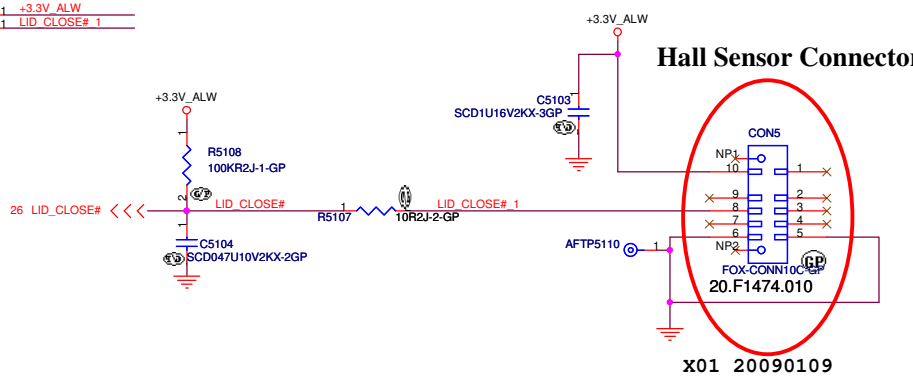
X01 20090130







Hall Sensor Connector



X01 20090109

<Core Design>

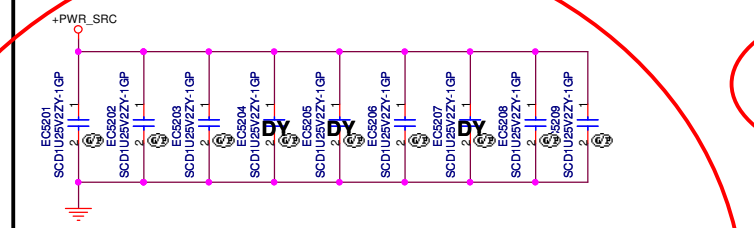
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Button/Hall Sensor/USB Board

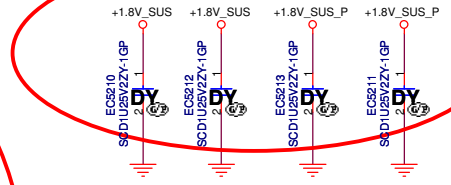
Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 51 of 59

SSID = Mechanical



EMI Request



X02 20090305

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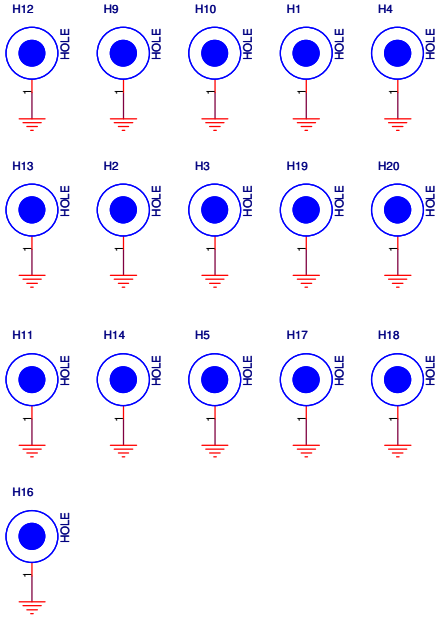
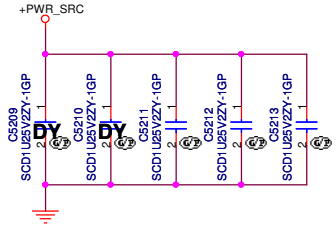
X01 20081208

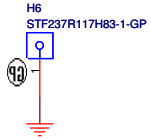




Roger Request

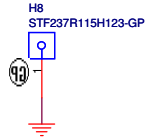
X01 20081215

Thermal



34.4CK01.001

Bluetooth



34.4A902.001

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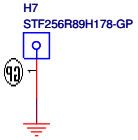
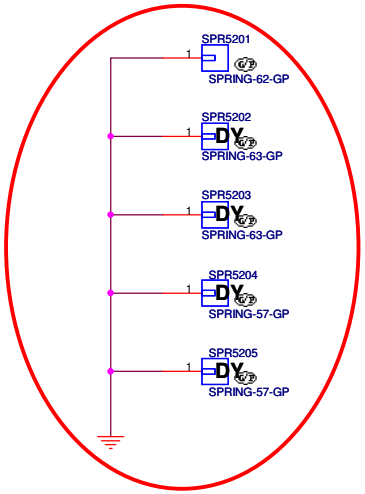
X01 20081208

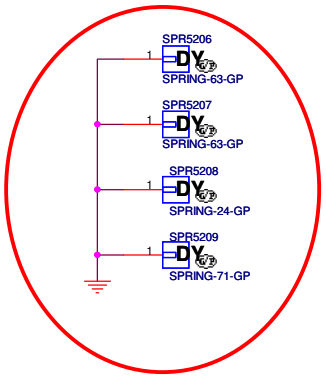
MINI CARD



34.4B417.001



X01 20090105



X02 20090304

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components

Size: Custom | Document Number: Alba Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 52 of 59

SSID = VIDEO

U5301A — 1 OF 7 — PCI EXPRESS INTERFACE

PCIE_MTX_GRX_P0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIE_MRX_GTX_R_P0	C5302	PCIE_MRX_GTX_P0
PCIE_MTX_GRX_N0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIE_MRX_GTX_R_N0	C5304	PCIE_MRX_GTX_N0
PCIE_MTX_GRX_P1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PCIE_MRX_GTX_R_P1	C5301	PCIE_MRX_GTX_P1
PCIE_MTX_GRX_N1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIE_MRX_GTX_R_N1	C5305	PCIE_MRX_GTX_N1
PCIE_MTX_GRX_P2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIE_MRX_GTX_R_P2	C5303	PCIE_MRX_GTX_P2
PCIE_MTX_GRX_N2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIE_MRX_GTX_R_N2	C5306	PCIE_MRX_GTX_N2
PCIE_MTX_GRX_P3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIE_MRX_GTX_R_P3	C5314	PCIE_MRX_GTX_P3
PCIE_MTX_GRX_N3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIE_MRX_GTX_R_N3	C5316	PCIE_MRX_GTX_N3
PCIE_MTX_GRX_P4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	PCIE_MRX_GTX_R_P4	C5317	PCIE_MRX_GTX_P4
PCIE_MTX_GRX_N4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	PCIE_MRX_GTX_R_N4	C5318	PCIE_MRX_GTX_N4
PCIE_MTX_GRX_P5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	PCIE_MRX_GTX_R_P5	C5321	PCIE_MRX_GTX_P5
PCIE_MTX_GRX_N5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	PCIE_MRX_GTX_R_N5	C5322	PCIE_MRX_GTX_N5
PCIE_MTX_GRX_P6	Y30	PCIE_RX6P	PCIE_TX6P	AB27	PCIE_MRX_GTX_R_P6	C5325	PCIE_MRX_GTX_P6
PCIE_MTX_GRX_N6	W31	PCIE_RX6N	PCIE_TX6N	AB26	PCIE_MRX_GTX_R_N6	C5326	PCIE_MRX_GTX_N6
PCIE_MTX_GRX_P7	W29	PCIE_RX7P	PCIE_TX7P	Y27	PCIE_MRX_GTX_R_P7	C5329	PCIE_MRX_GTX_P7
PCIE_MTX_GRX_N7	V28	PCIE_RX7N	PCIE_TX7N	Y26	PCIE_MRX_GTX_R_N7	C5330	PCIE_MRX_GTX_N7
PCIE_MTX_GRX_P8	V30	PCIE_RX8P	PCIE_TX8P	W24	PCIE_MRX_GTX_R_P8	C5331	PCIE_MRX_GTX_P8
PCIE_MTX_GRX_N8	U31	PCIE_RX8N	PCIE_TX8N	W23	PCIE_MRX_GTX_R_N8	C5332	PCIE_MRX_GTX_N8
PCIE_MTX_GRX_P9	U29	PCIE_RX9P	PCIE_TX9P	V27	PCIE_MRX_GTX_R_P9	C5307	PCIE_MRX_GTX_P9
PCIE_MTX_GRX_N9	T28	PCIE_RX9N	PCIE_TX9N	U26	PCIE_MRX_GTX_R_N9	C5308	PCIE_MRX_GTX_N9
PCIE_MTX_GRX_P10	T30	PCIE_RX10P	PCIE_TX10P	U24	PCIE_MRX_GTX_R_P10	C5309	PCIE_MRX_GTX_P10
PCIE_MTX_GRX_N10	R31	PCIE_RX10N	PCIE_TX10N	U23	PCIE_MRX_GTX_R_N10	C5310	PCIE_MRX_GTX_N10
PCIE_MTX_GRX_P11	R29	PCIE_RX11P	PCIE_TX11P	T26	PCIE_MRX_GTX_R_P11	C5311	PCIE_MRX_GTX_P11
PCIE_MTX_GRX_N11	P28	PCIE_RX11N	PCIE_TX11N	T27	PCIE_MRX_GTX_R_N11	C5312	PCIE_MRX_GTX_N11
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PCIE_MTX_GRX_N12	N31	PCIE_RX12N	PCIE_TX12N	T23	PCIE_MRX_GTX_R_N12	C5315	PCIE_MRX_GTX_N12
PCIE_MTX_GRX_P13	N29	PCIE_RX13P	PCIE_TX13P	P27	PCIE_MRX_GTX_R_P13	C5319	PCIE_MRX_GTX_P13
PCIE_MTX_GRX_N13	M28	PCIE_RX13N	PCIE_TX13N	P26	PCIE_MRX_GTX_R_N13	C5320	PCIE_MRX_GTX_N13
PCIE_MTX_GRX_P14	M30	PCIE_RX14P	PCIE_TX14P	P24	PCIE_MRX_GTX_R_P14	C5323	PCIE_MRX_GTX_P14
PCIE_MTX_GRX_N14	L31	PCIE_RX14N	PCIE_TX14N	P23	PCIE_MRX_GTX_R_N14	C5324	PCIE_MRX_GTX_N14
PCIE_MTX_GRX_P15	L29	PCIE_RX15P	PCIE_TX15P	M27	PCIE_MRX_GTX_R_P15	C5327	PCIE_MRX_GTX_P15
PCIE_MTX_GRX_N15	K30	PCIE_RX15N	PCIE_TX15N	N26	PCIE_MRX_GTX_R_N15	C5328	PCIE_MRX_GTX_N15

All C5302–C5328: SCD1U16V2KX-3GP

CLOCK

7 CLK_PCIE_VGA → CLK_PCIE_VGA → AK30 PCIE_REFCLKP
7 CLK_PCIE_VGA# → CLK_PCIE_VGA# → AK32 PCIE_REFCLKN

L9 NC#L9
N9 NC#N9
N10 NC_PWRGOOD

20,26 PLTRST_DELAY# → PLTRST_DELAY# → AL27 PERSTB

CALIBRATION

Y22 PCIE_CALRP — R5302 1K27R2F-L-GP
AA22 PCIE_CALRN — R5303 2KR2F-3-GP — +1.1V_RUN

M92-S2-GP

19 PLTRST_ICH_DELAY# → R5305 0R2J-2-GP DY

X01 20081208

PCIE_MTX_GRX_P[0..15] → PCIE_MTX_GRX_P[0..15] 13
PCIE_MTX_GRX_N[0..15] → PCIE_MTX_GRX_N[0..15] 13
PCIE_MRX_GTX_P[0..15] → PCIE_MRX_GTX_P[0..15] 13
PCIE_MRX_GTX_N[0..15] → PCIE_MRX_GTX_N[0..15] 13

U5301F — 6 OF 7

LVDS CONTROL

VARY_BL AB11 → LBKLT_CTL 41
DIGON AB12 → LCDVDD_EN 41

TXCLK_UP_DPF3P	AH20	VGA_TXBCLK+	VGA_TXBCLK+ 41
TXCLK_UN_DPF3N	AJ19	VGA_TXBCLK-	VGA_TXBCLK- 41
TXOUT_U0P_DPF2P	AL21	VGA_TXBOUT0+	VGA_TXBOUT0+ 41
TXOUT_U0N_DPF2N	AK20	VGA_TXBOUT0-	VGA_TXBOUT0- 41
TXOUT_U1P_DPF1P	AH22	VGA_TXBOUT1+	VGA_TXBOUT1+ 41
TXOUT_U1N_DPF1N	AJ21	VGA_TXBOUT1-	VGA_TXBOUT1- 41
TXOUT_U2P_DPF0P	AL23	VGA_TXBOUT2+	VGA_TXBOUT2+ 41
TXOUT_U2N_DPF0N	AK22	VGA_TXBOUT2-	VGA_TXBOUT2- 41
TXOUT_U3P	AK24		
TXOUT_U3N	AJ23		

R5304 10KR2J-3-GP
R5301 10KR2J-3-GP

LVTMDP

TXCLK_LP_DPE3P	AL15	VGA_TXACLK+	VGA_TXACLK+ 41
TXCLK_LN_DPE3N	AK14	VGA_TXACLK-	VGA_TXACLK- 41
TXOUT_L0P_DPE2P	AH16	VGA_TXAOUT0+	VGA_TXAOUT0+ 41
TXOUT_L0N_DPE2N	AJ15	VGA_TXAOUT0-	VGA_TXAOUT0- 41
TXOUT_L1P_DPE1P	AL17	VGA_TXAOUT1+	VGA_TXAOUT1+ 41
TXOUT_L1N_DPE1N	AK16	VGA_TXAOUT1-	VGA_TXAOUT1- 41
TXOUT_L2P_DPE0P	AH18	VGA_TXAOUT2+	VGA_TXAOUT2+ 41
TXOUT_L2N_DPE0N	AJ17	VGA_TXAOUT2-	VGA_TXAOUT2- 41
TXOUT_L3P	AL19		
TXOUT_L3N	AK18		

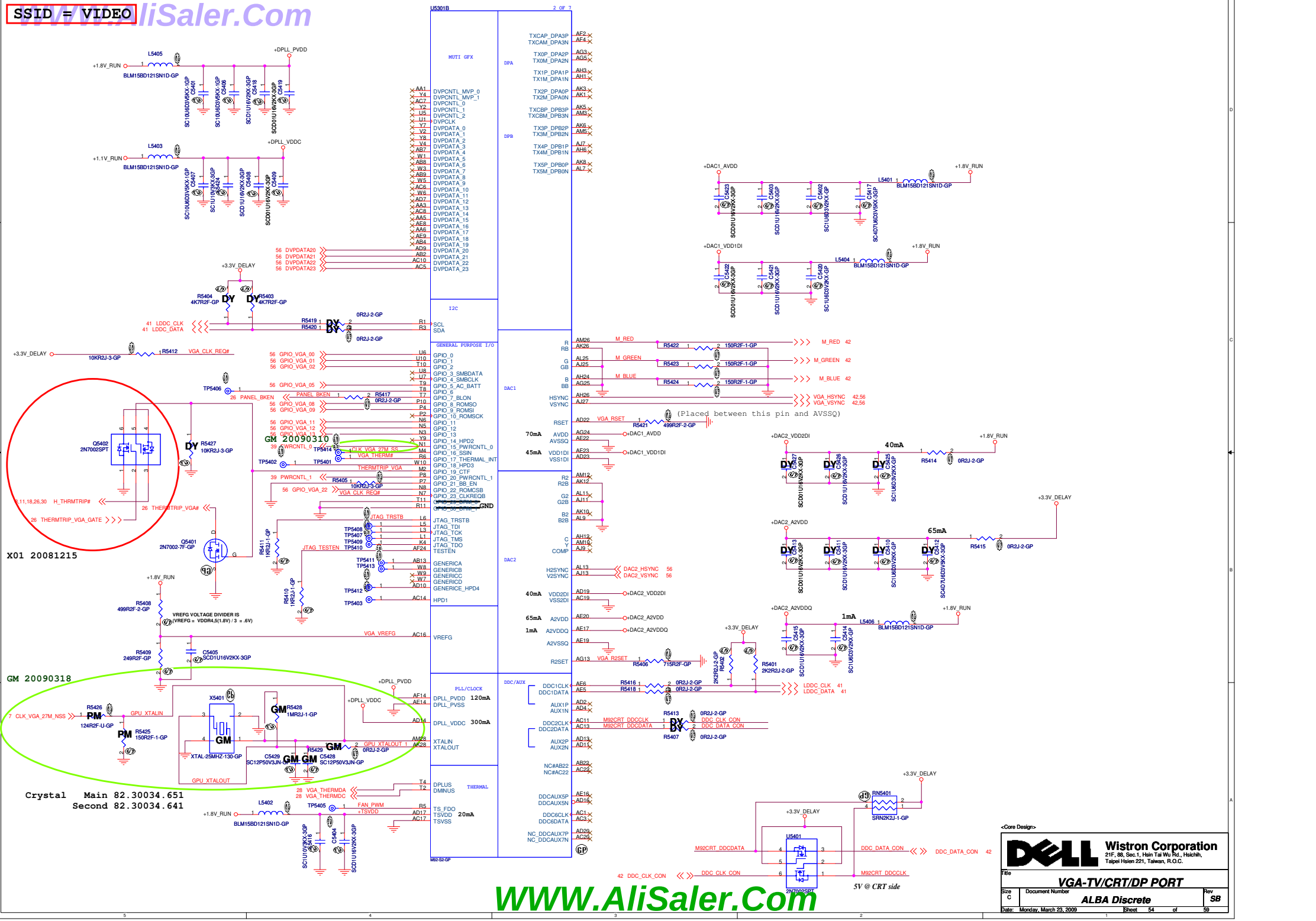
M92-S2-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)
Size: Custom | Document Number: ALBA Discrete | Rev: SB
Date: Monday, March 23, 2009 | Sheet 53 of 59

SSID = VIDEO



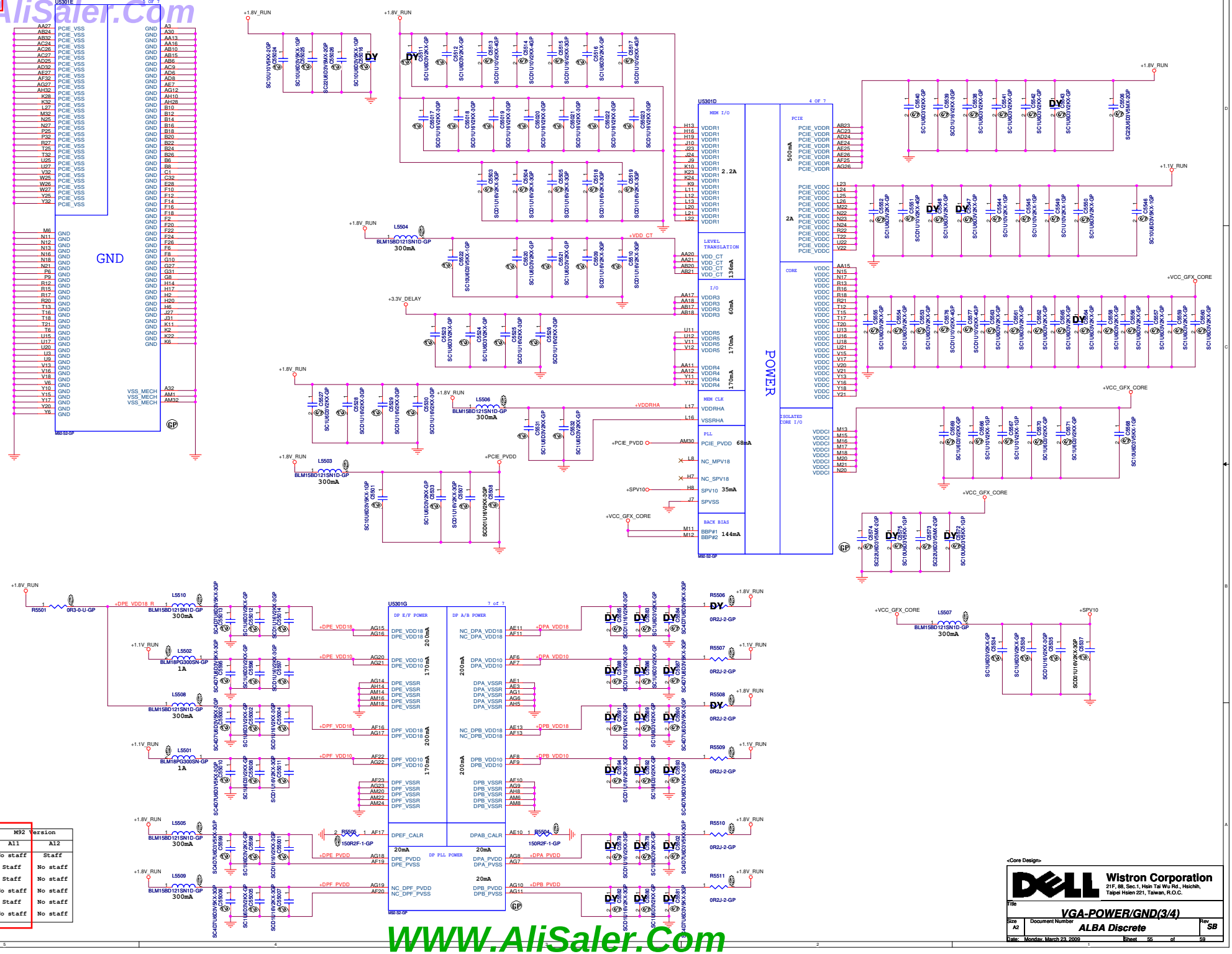
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-TV/CRT/DP PORT

Size: C | Document Number: ALBA Discrete | Rev: SB

Date: Monday, March 23, 2009 | Sheet 54 of 59

SSID = VIDEO



	M92 Version	
Part	A11	A12
R5401	No staff	Staff
Q5106	Staff	No staff
R5402	Staff	No staff
R5403	No staff	No staff
Q5107	Staff	No staff
C5384	No staff	No staff

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Title: VGA-POWER/GND(3/4)

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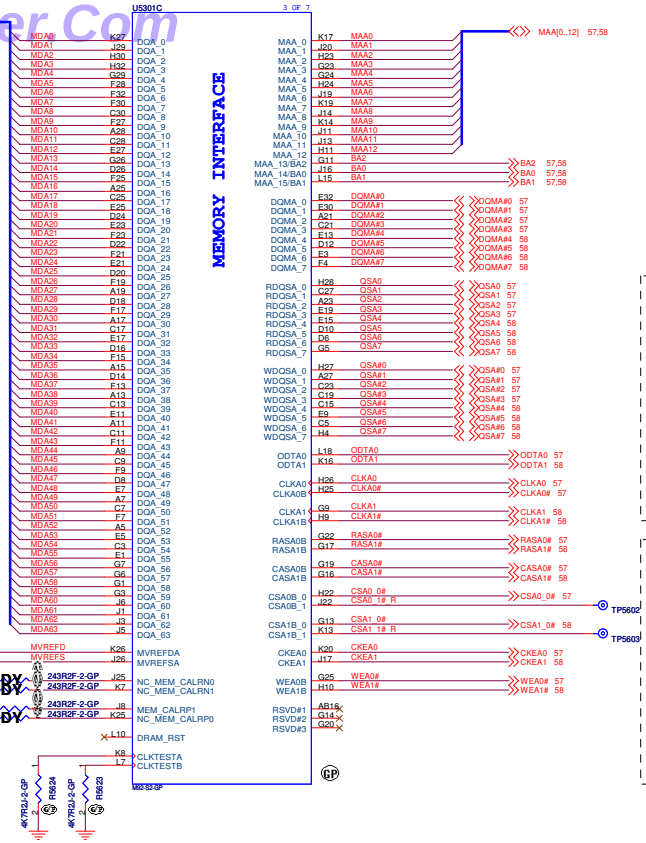
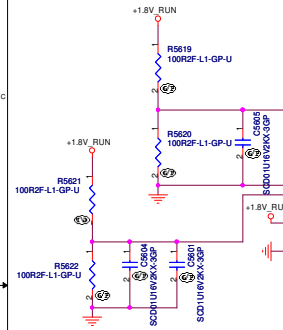
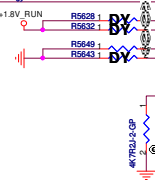
SSID = VIDEO

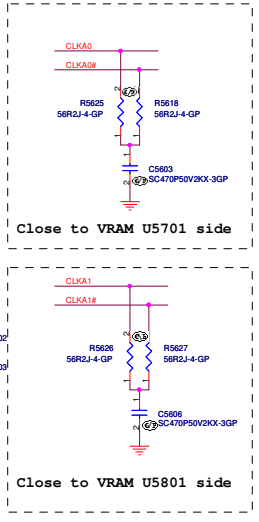
(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

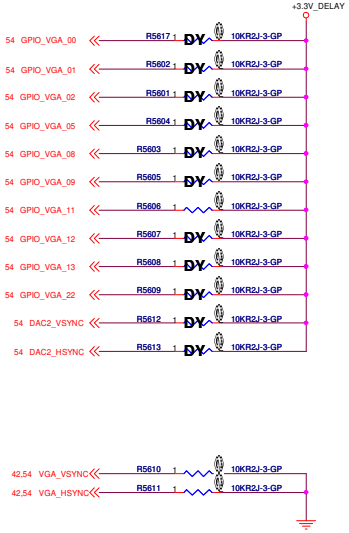
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

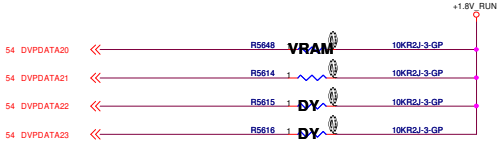












ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable V 0= 50% Tx output swing 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable V 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	V 0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] V 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 0000 - gDDR2 ---- ---- 0001 - gDDR2 64Mx16 HYNIX V 0010 - gDDR2 64Mx16 SAMSUNG 0011 - gDDR2 32Mx16 HYNIX 0100 - gDDR2 32Mx16 SAMSUNG

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Title: VGA-MEMORY/STRAPS(4/4)

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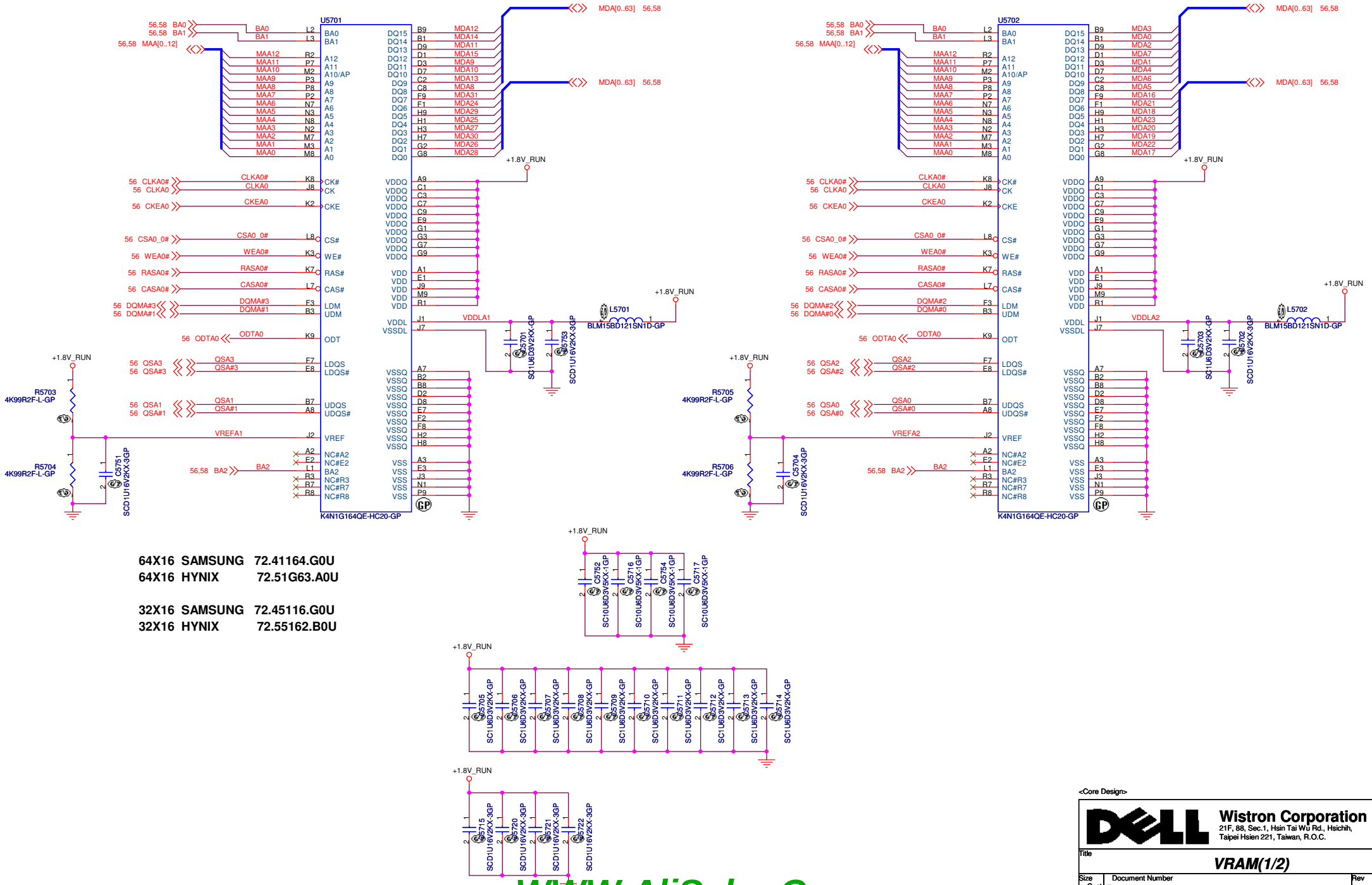

64X16 SAMSUNG 72.41164.G0U
64X16 HYNIX 72.51G63.A0U

32X16 SAMSUNG 72.45116.G0U
32X16 HYNIX 72.55162.B0U

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Title: VRAM(1/2)

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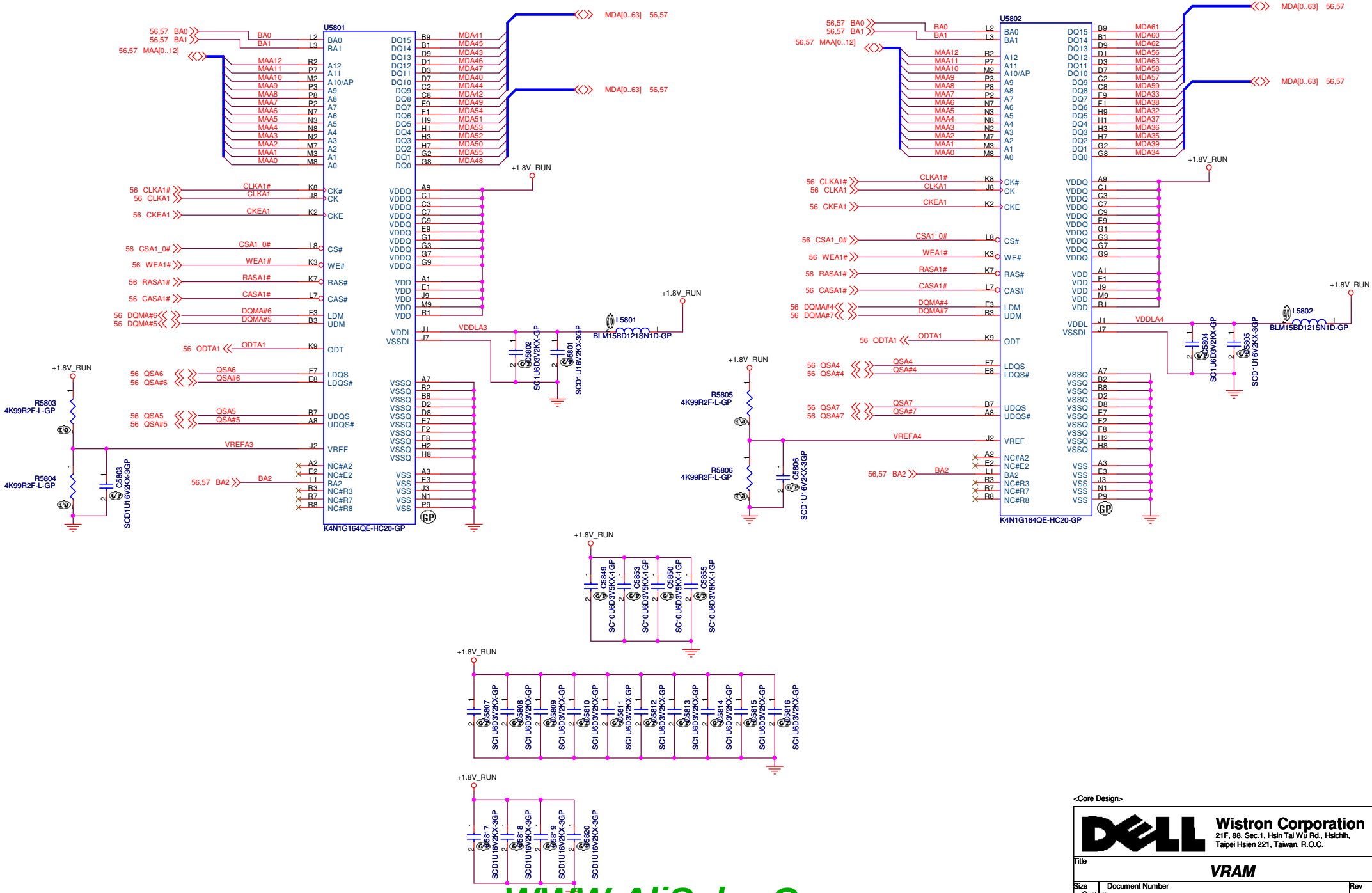

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Title: VRAM

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	18,46 52,42	2008/12/08	DELL	Remove Modem function.	Remove MDC schematics,holding,stand off.	X01
2	19,53	2008/12/08	Wistron	Reserve PLT_RST# for GPU PCIE reset.	Add R1913(DY),R5305(DY).	X01
3	25	2008/11/26	Realtek	Power down sequence issue, request by vendor.	Change R2506 to 1K ohm.	X01
4	25	2008/12/18	KDS	Follow crystal vendor test report.	Change C2501 to 18pF. C2502 to 15pF.	X01
5	26	2008/12/08	Wistron	MB version ID change.	Pop R2609,depop R2608.	X01
6	38	2008/12/08	Wistron	AMD power regulator issue.	Change 1.8V,0.9V power regulator.	X01
7	42	2008/12/08	Wistron	Follow ME connector list for touch pad connector.	Change TPAD1.	X01
8	46,51	2008/12/08	Wistron	Follow ME connector list for USB connector.	Change USB1, USB2 and CON4.	X01
9	30,33	2008/12/15	Wistron	MOSFET can not fully trun on issue.	Add +15V_ALW power circuits. And modify 3.3V_RUN, 5V_RUN enable circuits.	X01
10	8,28	2008/12/15	Wistron	Thermal sensor order changed because DTS still have accuracy problem.	Change EMC2102 first channel to CPU internal diode. Change channel to GPU inernal diode.	X01
11	15	2008/12/15	Wistron	Cantiga power rating issue.	Add R1507.	X01
12	26,54	2008/12/15	Wistron	AMD CTF glitch issue.	Reserve KBC GPIO27, Add R2639.	X01
13	40	2008/12/15	Wistron	Add panel self test for factory.	Add D4002,Pop R2638.	X01
14	32	2008/12/15	Wistron	Prevent leakage from KBC.	Change PR3203 pull high from +3.3V_ALW to +3.3V_RTC_LDO.	X01
15	44,52 51,47	2008/12/15	Wistron	Modify based on EMI test result.	POP EC5203 C5212 EC5202 C5211 C5213 EC5206 EC5201 EC5208 and POP EC4701 EC4702 EC4401 EC4402 EC4403 EC4404 EC5101 with 22P-Varistor	X01
16	41	2008/12/18	Wistron	LCD power sequence issue.	Change +LCD_VDD power produce solution.	X01
17	41	2008/12/19	Wistron	CMO LCD white screen issue.	Add R4108(DY).	X01
18	46,51	2008/12/19	Wistron	Add ESD diode for USB Port.	Add D4601,D4602,D5101.	X01
19	39	2008/12/29	Wistron	GFX CORE glitch issue.	Add PD3902,PD3903,PR3910,PR3915. Change PC3915,PC3916 to 0.047uF.	X01
20	50	2008/12/29	Wistron	Follow ME connector list for Express card board.	Change CON2 to 20.F1400.050.	X01

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
21	9	2009/01/06	Wistron	Power team request for CPU core measurement.	Add PG901,PG902. Pop C901 and depot C902.	X01
22	26	2009/01/08	Wistron	Keyboard detect issue.	Pop R2625.	X01
23	44,51	2009/01/08	Wistron	Change new connector.	Change HDD1 and CON5.	X01
24	8	2009/01/12	Wistron	For better GTL reference voltage.	Pop C802.	X01
25	30,36 37,38	2009/01/12	Wistron	Add discharge circuit for GPU powers.	Add R3016,Q3006,R3015,Q3003,Q3702,R3702 R3703,D3802,R3802,C3802.	X01
26	22,26	2009/01/13	IDT	For pop noise on YC version codec.	Add Q2201,Q2202,R2219. Add GPIO33 for HP_MUTE.	X01
27	33	2009/01/13	Wistron	For +15V_ALW issue. Prevent higher than 20V.	Add PD3303,PC3301.	X01
28	51	2009/01/30	Wistron	ESD protection concern.	Change R5106 to 33ohm.	X01
29	39	2009/01/30	Wistron	For GFX_CORE overshoot and undershoot issue.	Pop R3921,R3922. Depop R3920,R3923.	X01
30	18,26	2009/02/19	Wistron	Prevent 32768Hz crystal no oscillation from flux.	Change C1807,C1806,C2607,C2608 to 0603 size.	X02
31	22	2009/02/26	IDT	For codec pop noise issue.	Change C2204 to 2.2uf. Add Q2201,Q2202,Q2203, Q2204,Q2205. Move R2218,R2220 to main board.	X02
32	26	2009/02/26	Wistron	Change Board ID and add VRAM type select pin.	Change board ID to 010,Add GPIO5 for VRAM type	X02
33	30	2009/03/02	Wistron	+3.3V_ALW drop issue.	Add C3005.	X02
34	31,42, 44,45	2009/02/19	Wistron	Connector change request by ME.	Change RJ45,DCIN,FAN,SPEAKER connectors.	X02
35	41	2009/02/19	Wistron	LCD white screen issue.	Pop R4108.	X02
36	31,32	2009/03/02	Wistron	Power team request.	Change PD3107 to 1SMB22AT3G. Change PC3208, PC3209 to X7R.	X02
37	52	2009/03/05	Wistron	Reserve capacitors and springs for EMI.	Add location for SPR5206~SPR5209 and EC5210~EC5213.	X02
38	26	2009/03/09	Wistron	No need to support keyboard detect function.	Depop R2625.	X02
39	22	2009/03/09	Wistron	For PC_BEEP sound volume issue.	Modify R2203 to 120Kohm.	X02
40	33	2009/03/10	Wistron	+15V_ALW issue.	Depop PD3303.	X02

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