MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai UMA Schematics Document

uFCPGA Mobile Merom
Intel Crestline-GM + ICH8M

2007-03-19

REV :1.2(DELL: X02)

MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 1 OF 68	Cover Page	RELEASE DATE :	

LANAI: UMA

CLOCK
CK410M+LP
PG 21

POWER
- POWER CON. PG 59
- POWER SEQUENCE LOGIC PG 51
- POWER CHARGER PG 57
- POWER CONTROL SWITCH PG 49
- DISCHARGE PATH PG 49
  +3.3V_SUS/+5V_SUS/+3.3V_RUN
  +5V/+3.3V/+1.8V/+1.25_RUN

XDP PG 52

Merom
(478 Micro-FCPGA)
PG 7,8
(Symbol Rev.09)

POWER
- POWER I/O PG 55
  +1.5V_RUN/+1.05V_VCCP
- REGULATOR PG 58
  +VCC_GFX_CORE/+1.25V_RUN
- POWER VCORE PG 53
- POWER SYSTEM PG 54
  5V_ALW & 3.3V_ALW
- REGULATOR PG 56
  +1.8V_SUS/+0.9V_DDR_VTT

Panel Connector PG 28 — LVDS

Crestline
1299 uFCBGA
PG 9,10,11,12,13,14
(Symbol Rev.09)

533/667 MHZ DDR II → **DDR2-SODIMM1** PG 19

533/667 MHZ DDR II → **DDR2-SODIMM2** PG 19

IO Board
- CRT CONN. — VGA
- TV CONN. — TVOUT
- USB CONN.x2 — USB2.0(P2,3)
- MINI-CARD WLAN — PCIEx1 (Lane2)
- MINI-CARD WWAN — USB2.0(P9)

→ **D.B CON** PG 50 → VGA, TVOUT

SIM CARD Board
- SIM CARD

DMI INTERFACE

USB2.0(P0,P1) → **USB CONN.** PG 39 (**USB Board**)

ICH8-M
676 BGA
PG 15,16,17,18
(Symbol Rev.09)

USB2.0(P2,3)
PCIEx1 (Lane2)
USB2.0(P9)

PCIE (Lane6) → **BCM5906KMLG** QFN-68 PG 47 → **RJ45/Magnetic** PG 48

PCI → **CARD READER 1394/R5C833** PG 32,33,34

PCIE (Lane4) → **EXPRESS-CARD R5538** PG 35

USB2.0(P6)

USB2.0(P7) → **Bluetooth** PG 41

IHDA
- **AUDIO/AMP** PG 44,45,46
  - **S/PDIF TO TV CONN.** PG 30
  - **DIGITAL MIC.** PG 28
  - **Speaker CON** PG 46
  - **WtoB CON** PG 46
- **MDC** PG 36
  - **Audio Jacks *3** (**JACK Board**)
  - **RJ11** (**RJ11 Board**)

USB2.0(P5) → **CAMERA** PG 28

SATA → **SATA-HDD** PG 31

IDE → **CD-ROM** PG 31

SPI, LPC

SIO
MEC5025
128KB Flash
TMKBC
128 Pins VTQFP
PG 37

BC

SIO
ECE5011
Expander
USB 2.0 Hub(4)
128 Pins VTQFP
PG 38

SPI, PS/2
- **CIR** PG 41
- **FLASH** PG 40
- **Touchpad CON.** PG 41
- **FAN &THERMAL EMC4001** PG 43
- **USER INTERFACE** PG 42
- **SNIFFER** PG 42
- **CAPBTN CON.** PG 40

PROJECT:	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 2 OF 68	BLOCK DIAGRAM	RELEASE DATE :	

INDEX

PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***INDEX***	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 3 OF 68		RELEASE DATE :	

Footprint Definition	
Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

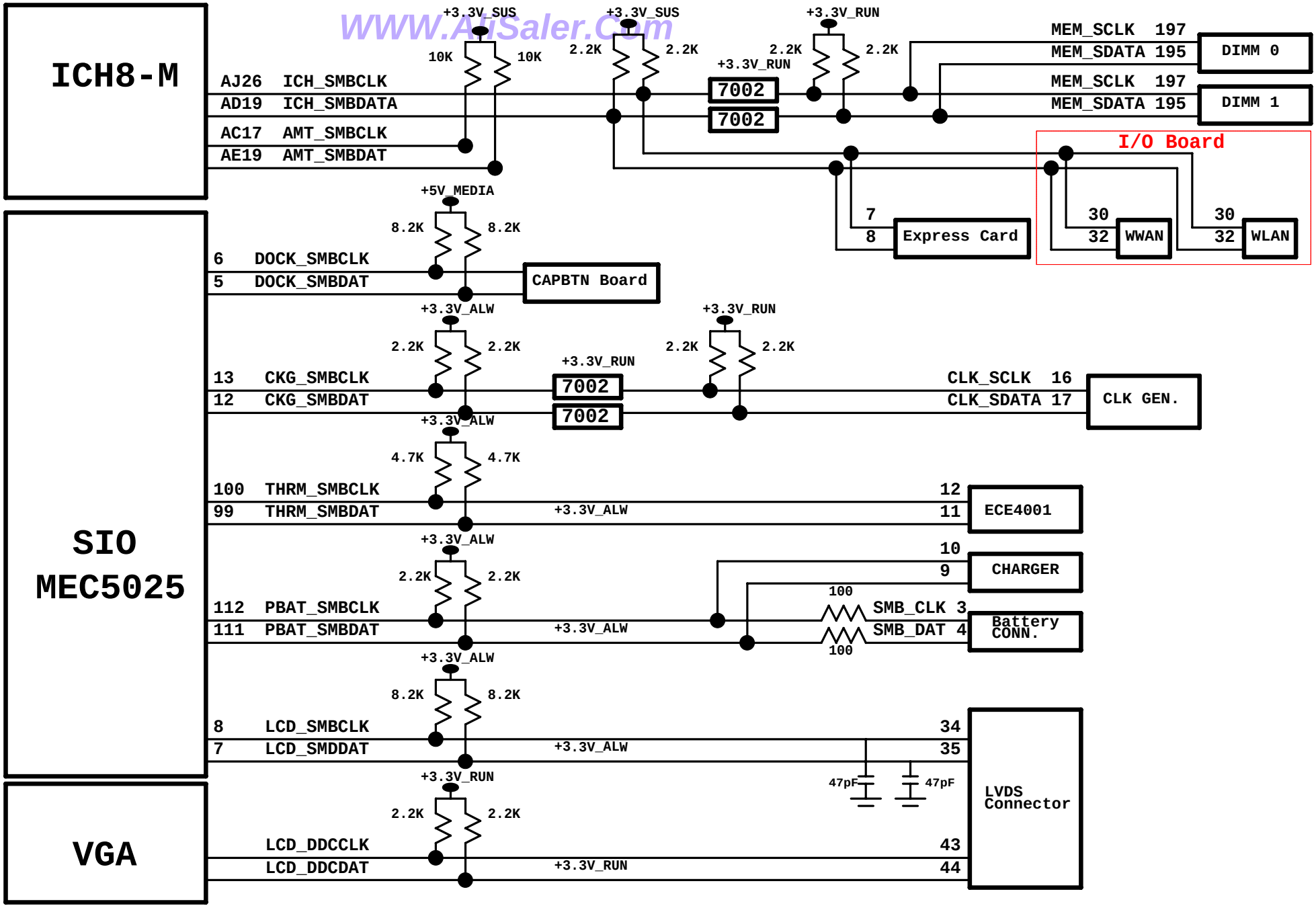
For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE			
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

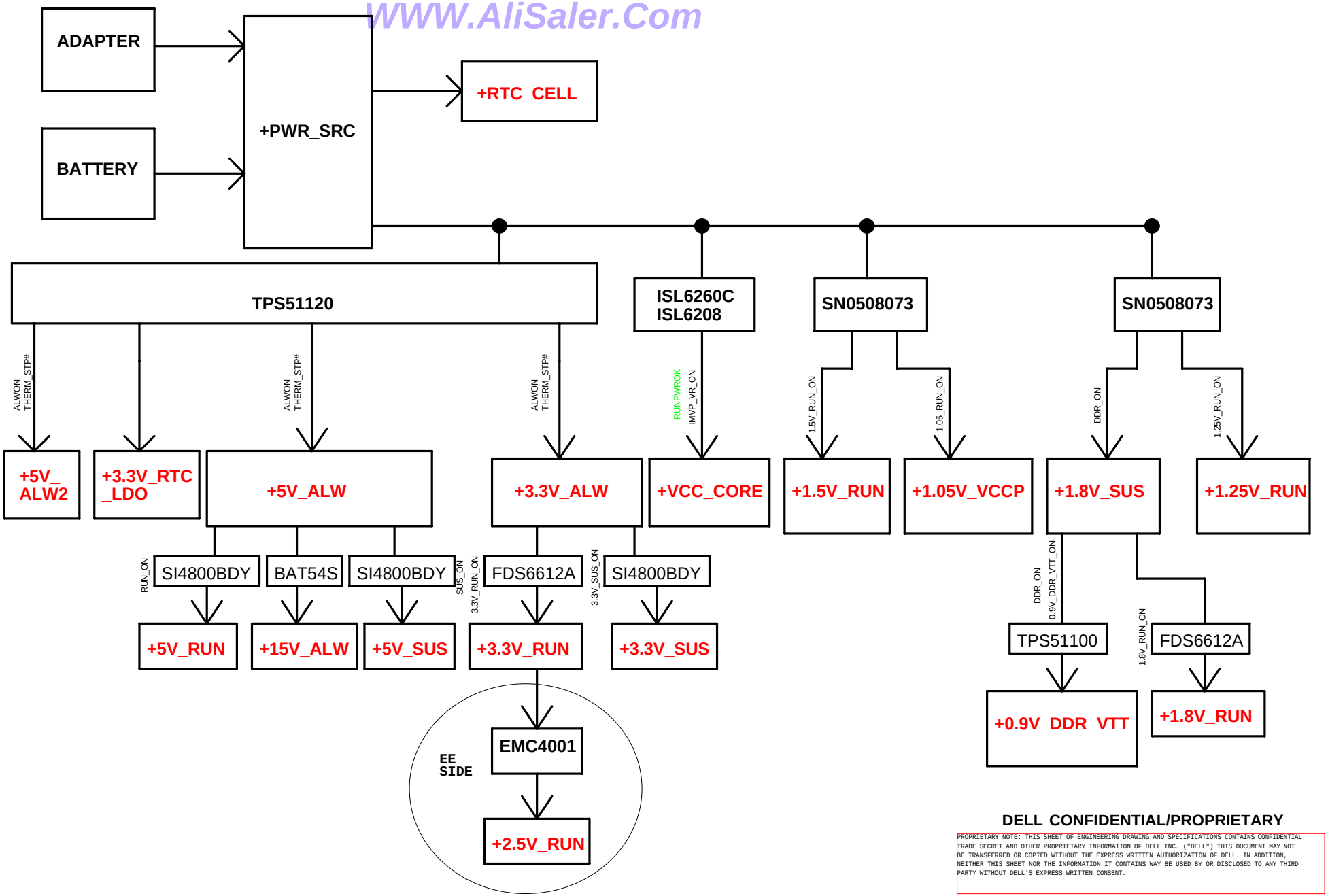
PCI Express TABLE	
Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

USB TABLE	
ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN

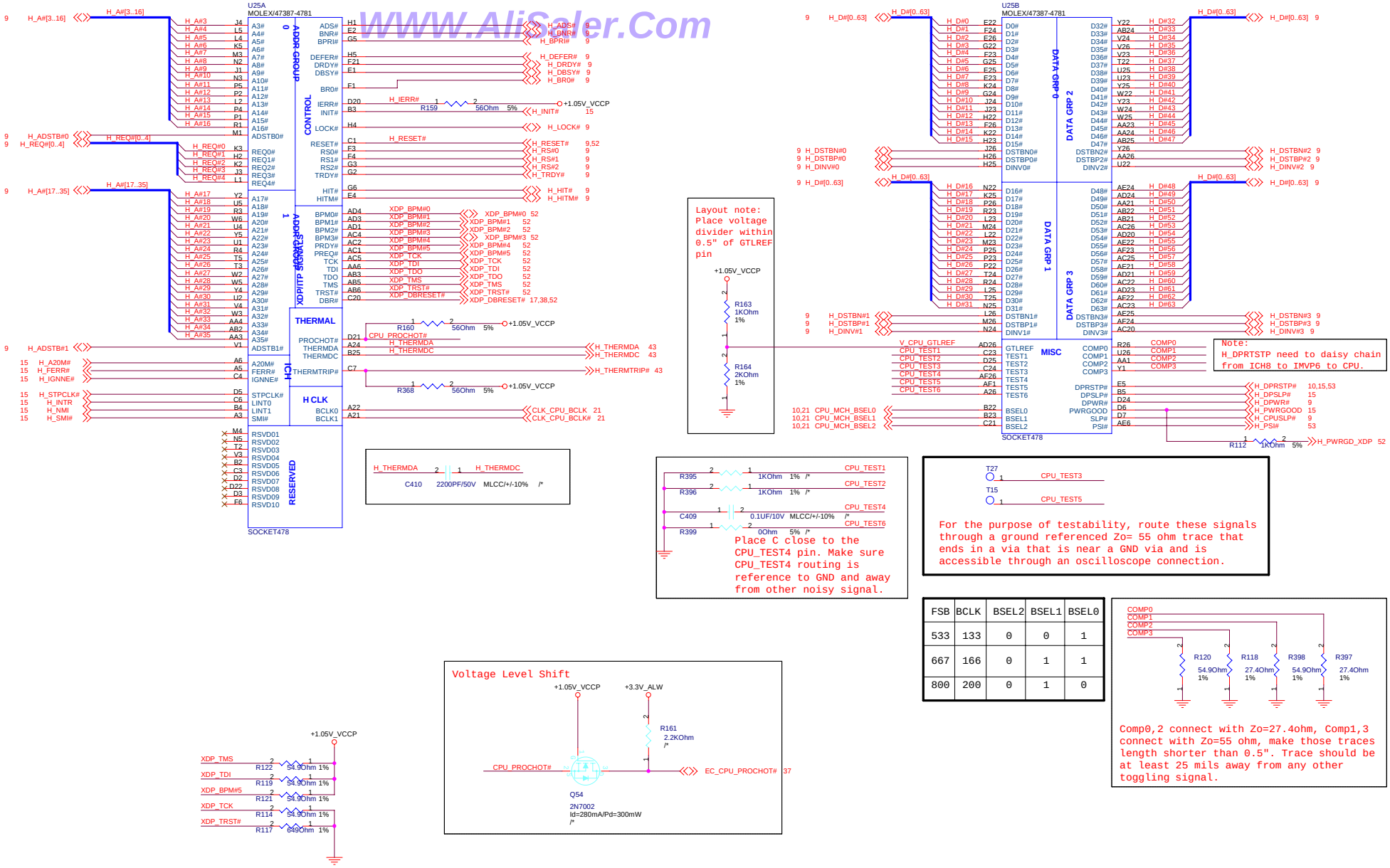


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: SMBUS BLOCK	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 5 OF 68		RELEASE DATE :	



DELL CONFIDENTIAL/PROPRIETARY

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 6 OF 68	Power Rail	RELEASE DATE :	



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ***MEROM CPU (1)***	SCHEMATIC FILE NAME: <OrgName>
		SHEET 7 OF 68		RELEASE DATE:

DESIGN ENGINEER :

All use 10U 4V (+-20% , X6S , 0805)Pb-Free.

+VCC_CORE

C403 C385 C132 C140 C390
10UF/4V MLCC/+/-20% pt_c0805

C183 C166 C400 C392 C176
10UF/4V MLCC/+/-20% pt_c0805

8 inside cavity, north side, secondary layer.

C180 C157 C159 C383 C187
10UF/4V MLCC/+/-20% pt_c0805

C131 C386 C152 C391 C402
10UF/4V MLCC/+/-20% pt_c0805

8 inside cavity, south side, secondary layer.

C126 C181 C399 C398 C397 C145
10UF/4V MLCC/+/-20% pt_c0805

6 inside cavity, north side, primary layer.

C179 C133 C396 C172 C134 C158
10UF/4V MLCC/+/-20% pt_c0805

6 inside cavity, south side, primary layer.

+1.05V_VCCP

C381 C380 C404 C193 C405 C124
0.1UF/10V MLCC/+/-10%

Layout out:
Place these inside socket cavity on North side secondary.

U25C
MOLEX/47387-4781
SOCKET478

VCC001 VCC002 VCC003 VCC004 VCC005 VCC006 VCC007 VCC008 VCC009 VCC010 VCC011 VCC012 VCC013 VCC014 VCC015 VCC016 VCC017 VCC018 VCC019 VCC020 VCC021 VCC022 VCC023 VCC024 VCC025 VCC026 VCC027 VCC028 VCC029 VCC030 VCC031 VCC032 VCC033 VCC034 VCC035 VCC036 VCC037 VCC038 VCC039 VCC040 VCC041 VCC042 VCC043 VCC044 VCC045 VCC046 VCC047 VCC048 VCC049 VCC050 VCC051 VCC052 VCC053 VCC054 VCC055 VCC056 VCC057 VCC058 VCC059 VCC060 VCC061 VCC062 VCC063 VCC064 VCC065 VCC066 VCC067

VCC068 VCC069 VCC070 VCC071 VCC072 VCC073 VCC074 VCC075 VCC076 VCC077 VCC078 VCC079 VCC080 VCC081 VCC082 VCC083 VCC084 VCC085 VCC086 VCC087 VCC088 VCC089 VCC090 VCC091 VCC092 VCC093 VCC094 VCC095 VCC096 VCC097 VCC098 VCC099 VCC100

VCCP01 VCCP02 VCCP03 VCCP04 VCCP05 VCCP06 VCCP07 VCCP08 VCCP09 VCCP10 VCCP11 VCCP12 VCCP13 VCCP14 VCCP15 VCCP16

VCCA01 VCCA02

VID0 VID1 VID2 VID3 VID4 VID5 VID6

VCCSENSE VSSSENSE

+1.05V_VCCP
CE20 220UF/4V pt_c7343d_h79 TAN/Lf_T=2000hrs_105C/+/-20%

+1.5V_RUN
C414 0.01UF/25V MLCC/+/-10% pt_c0603
C418 10UF/4V pt_c0805 MLCC/+/-20%

Layout Note:
Place 0.01U/25V near PIN B26.

100U/25V *4 Remove to POWER CIRCUIT .

+VCC_CORE
R128 100Ohm 1%
R127 100Ohm 1%
VCCSENSE
VSSSENSE

Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mils spacing and length matched to within 25 mil. Place PU and PD within 1 inch of CPU.

+VCC_CORE
No.43
CE6 CE5 CE19 CE16 CE18 CE7
220UF/2V pt_c7343d_h75 SANYO/2TPF220M7

U25D
MOLEX/47387-4781
SOCKET478

VSS001 VSS002 VSS003 VSS004 VSS005 VSS006 VSS007 VSS008 VSS009 VSS010 VSS011 VSS012 VSS013 VSS014 VSS015 VSS016 VSS017 VSS018 VSS019 VSS020 VSS021 VSS022 VSS023 VSS024 VSS025 VSS026 VSS027 VSS028 VSS029 VSS030 VSS031 VSS032 VSS033 VSS034 VSS035 VSS036 VSS037 VSS038 VSS039 VSS040 VSS041 VSS042 VSS043 VSS044 VSS045 VSS046 VSS047 VSS048 VSS049 VSS050 VSS051 VSS052 VSS053 VSS054 VSS055 VSS056 VSS057 VSS058 VSS059 VSS060 VSS061 VSS062 VSS063 VSS064 VSS065 VSS066 VSS067 VSS068 VSS069 VSS070 VSS071 VSS072 VSS073 VSS074 VSS075 VSS076 VSS077 VSS078 VSS079 VSS080 VSS081

VSS082 VSS083 VSS084 VSS085 VSS086 VSS087 VSS088 VSS089 VSS090 VSS091 VSS092 VSS093 VSS094 VSS095 VSS096 VSS097 VSS098 VSS099 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128 VSS129 VSS130 VSS131 VSS132 VSS133 VSS134 VSS135 VSS136 VSS137 VSS138 VSS139 VSS140 VSS141 VSS142 VSS143 VSS144 VSS145 VSS146 VSS147 VSS148 VSS149 VSS150 VSS151 VSS152 VSS153 VSS154 VSS155 VSS156 VSS157 VSS158 VSS159 VSS160 VSS161 VSS162 VSS163

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Merom CPU (2)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
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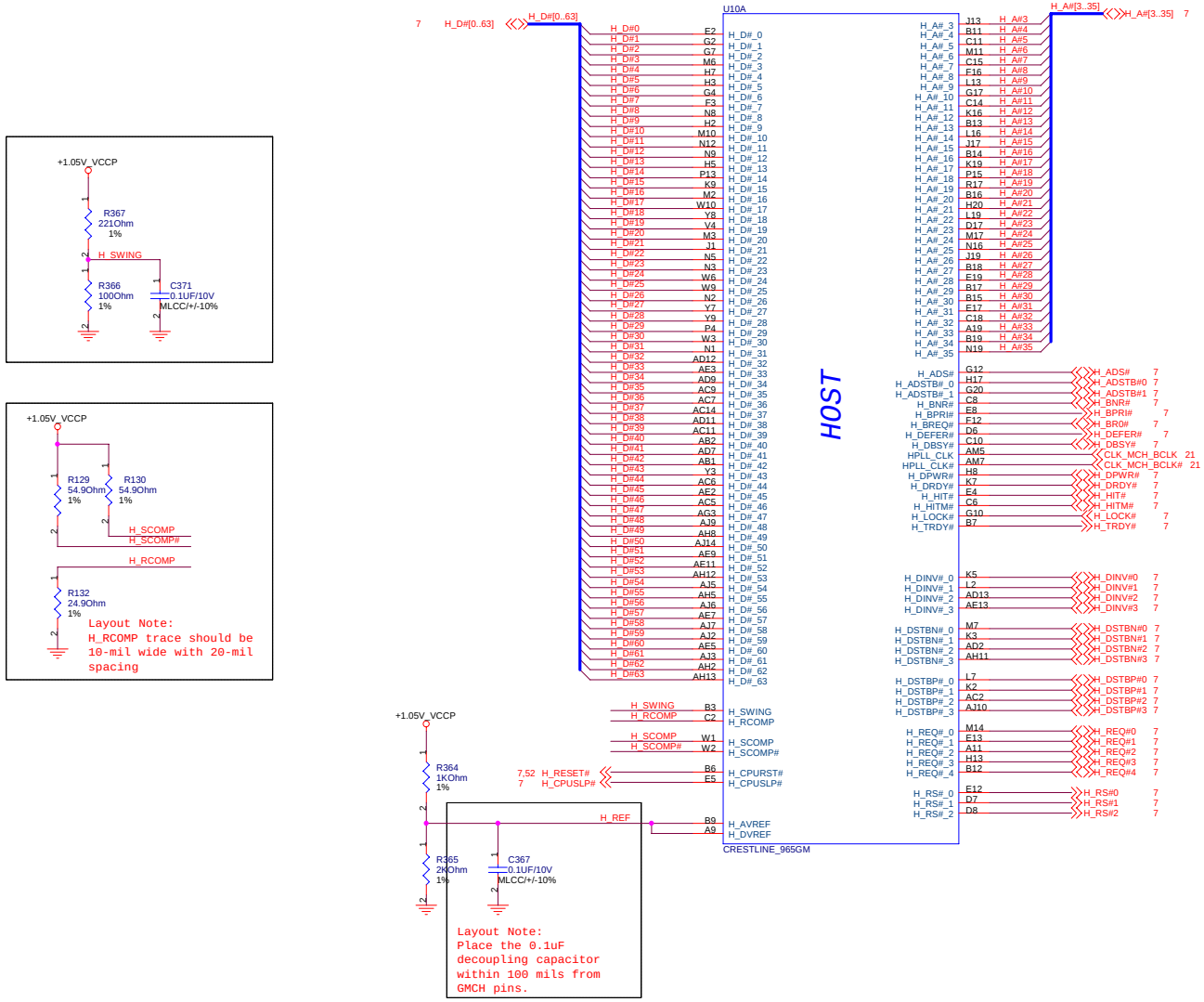
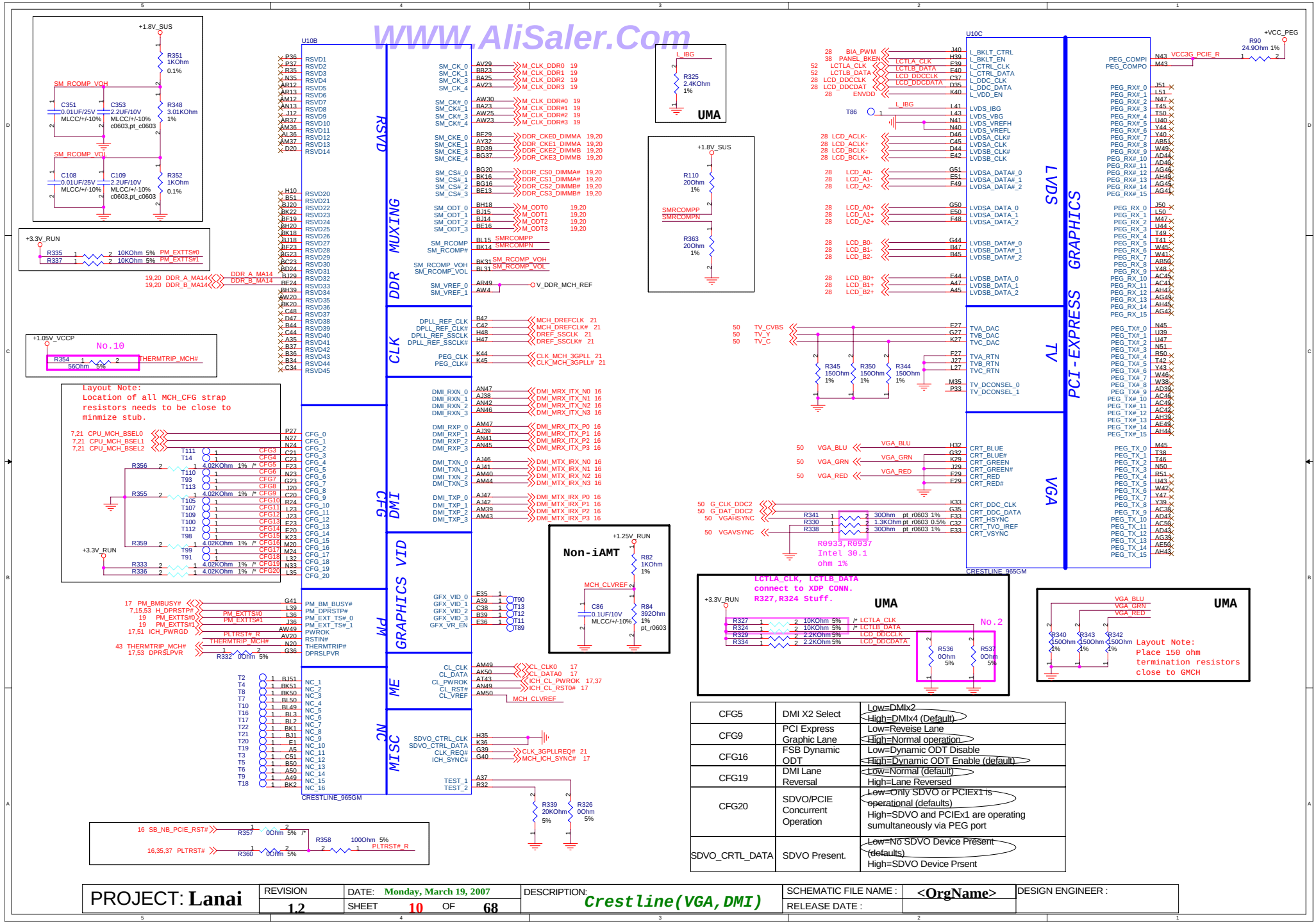


PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(HOST)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER :
		SHEET **9** OF **68**		RELEASE DATE :	



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating sumultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Prsent

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Crestline(VGA,DMI)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
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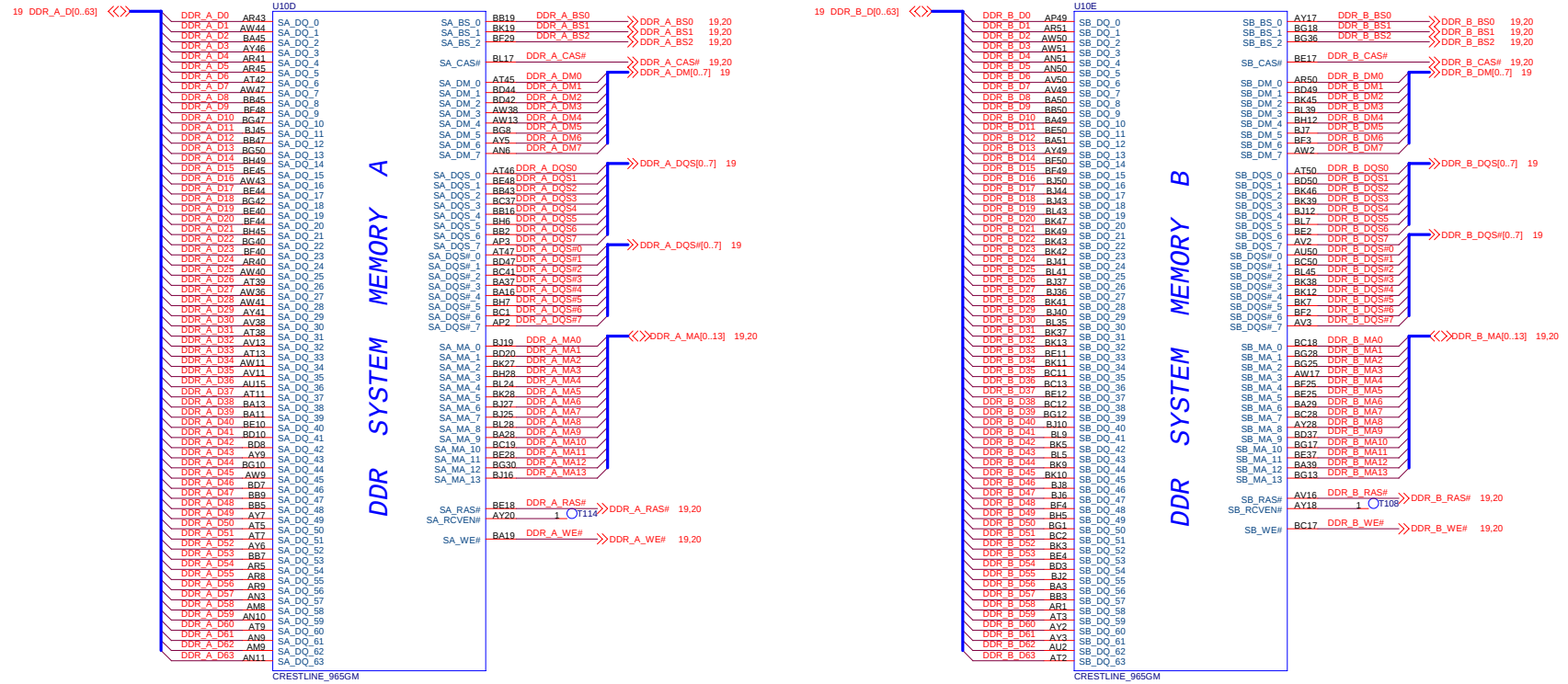
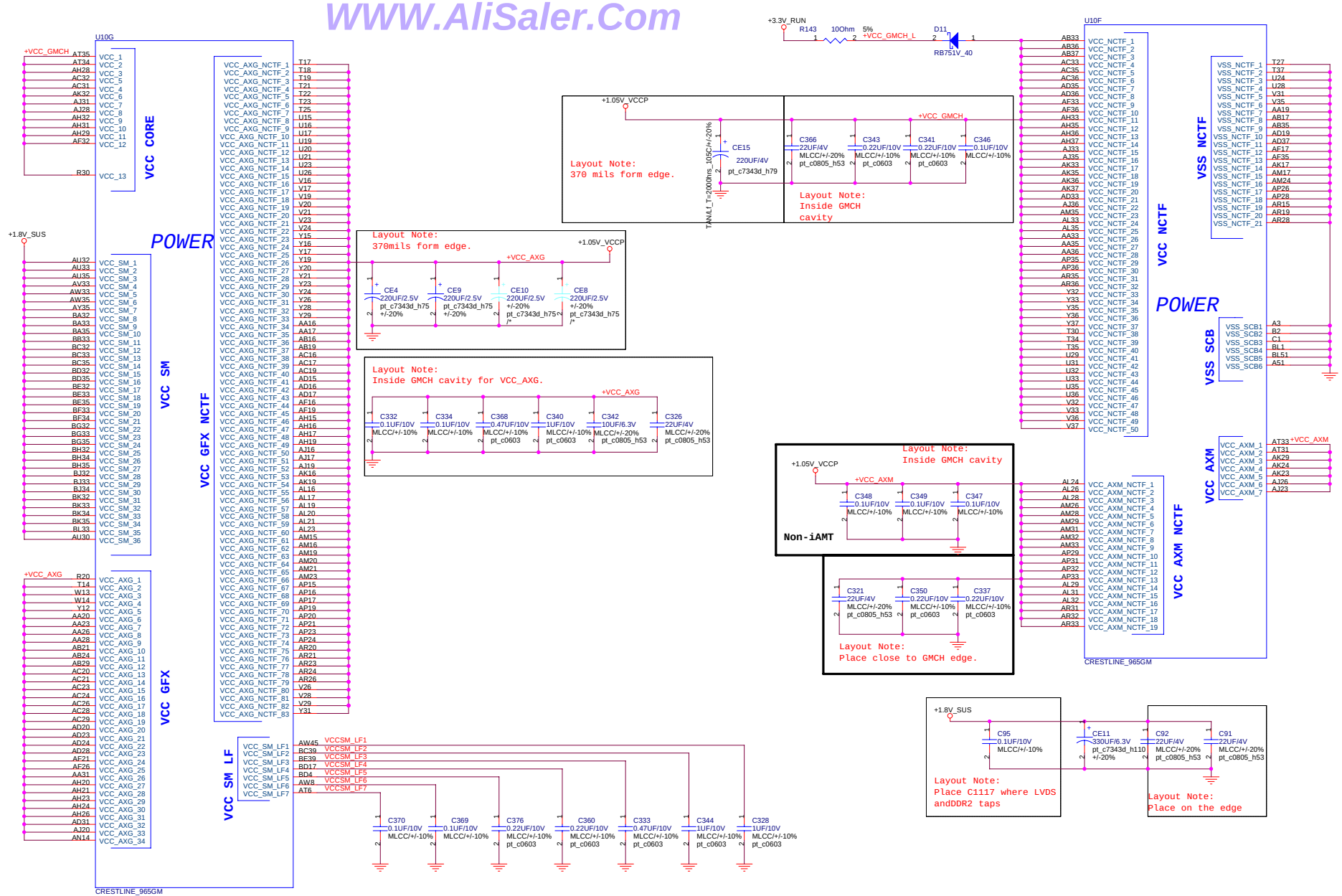
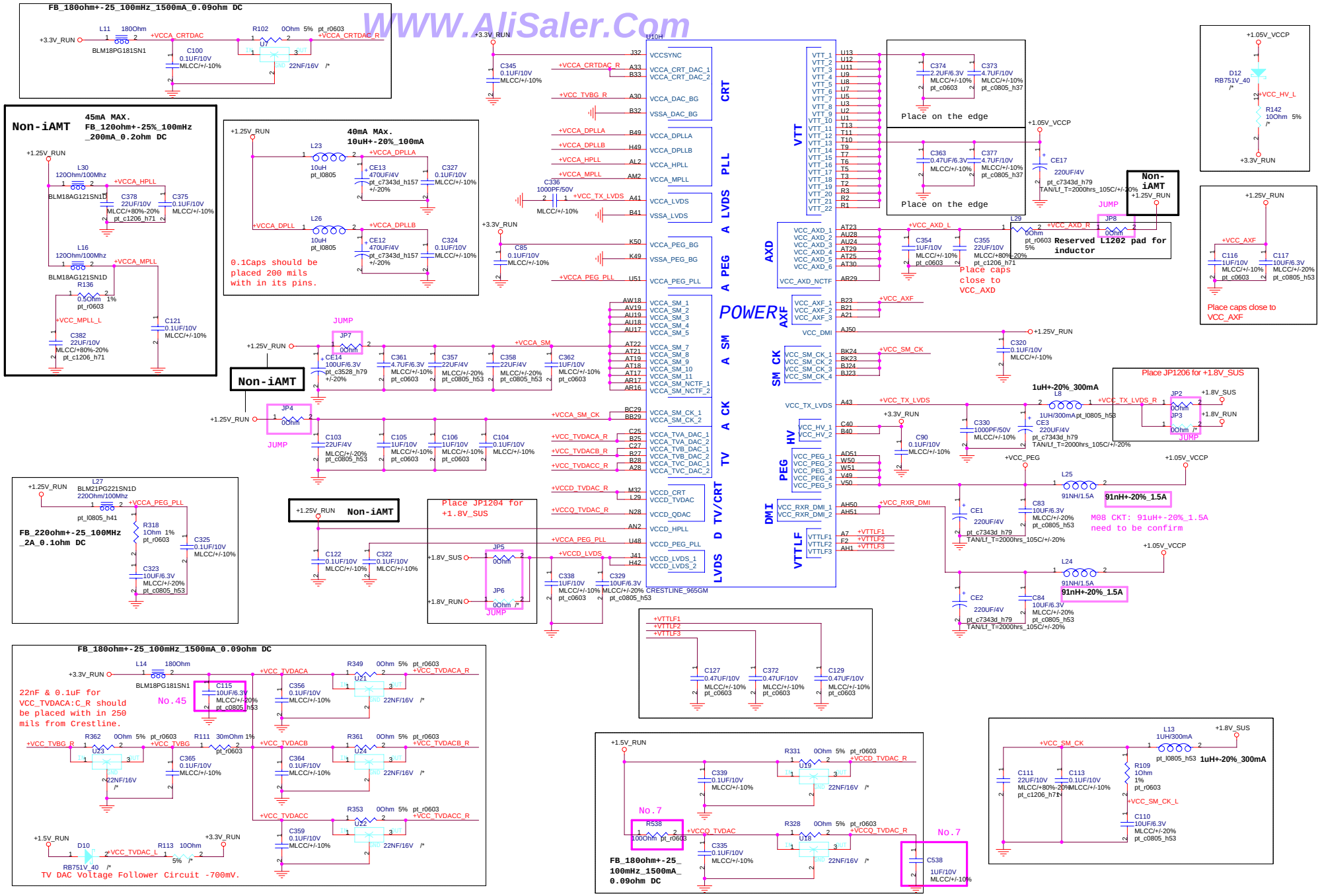


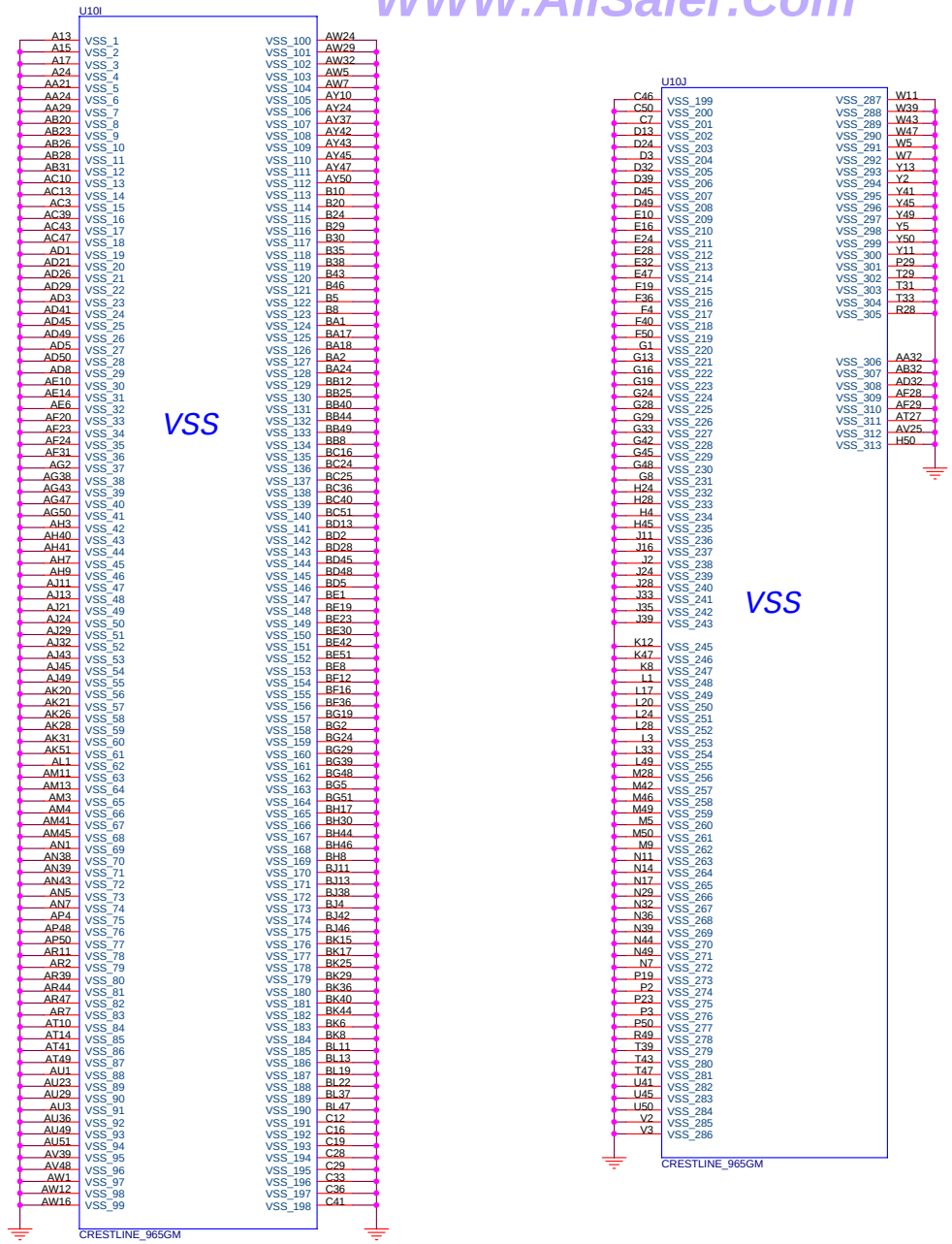
PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(DDR2)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER :	
		SHEET **11** OF **68**		RELEASE DATE :		



PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 12 OF 68	*Crestline(VCC,NCTF)*	RELEASE DATE :		



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(POWER)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER :	
		SHEET **13** OF **68**		RELEASE DATE :		



PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: *Crestline(VSS)*	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER :
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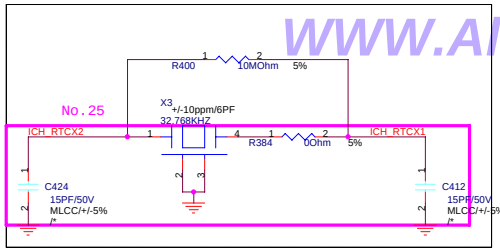
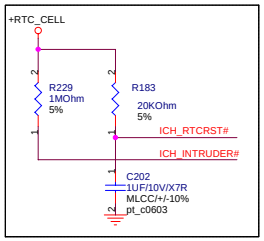
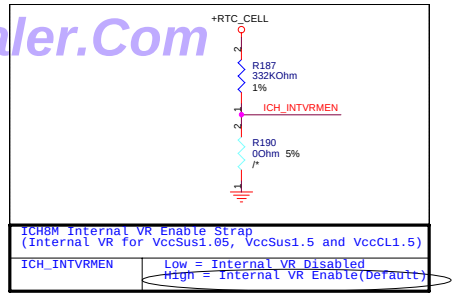
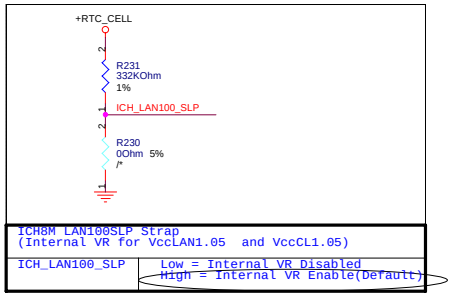
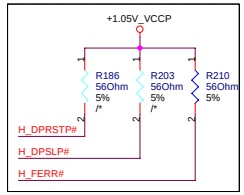
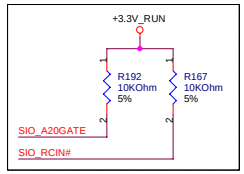


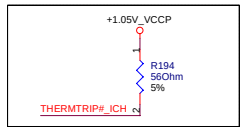


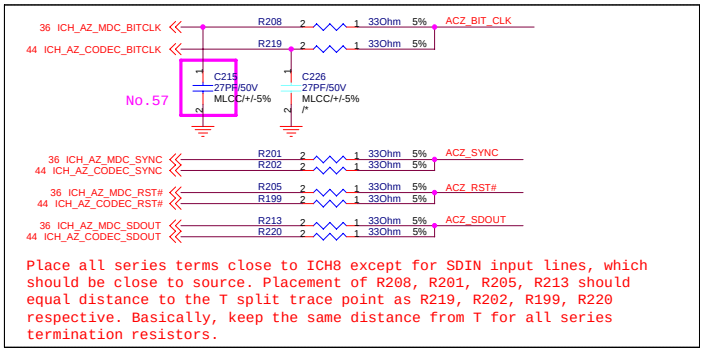




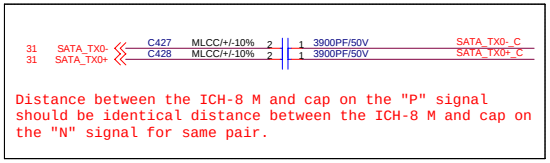




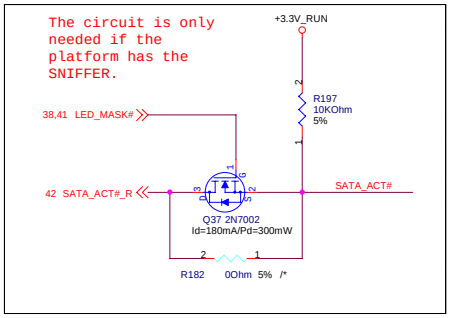


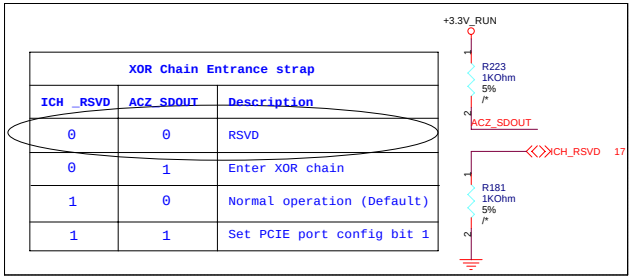


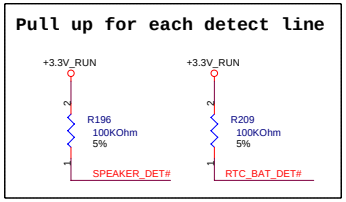
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R208, R201, R205, R213 should equal distance to the T split trace point as R219, R202, R199, R220 respective. Basically, keep the same distance from T for all series termination resistors.

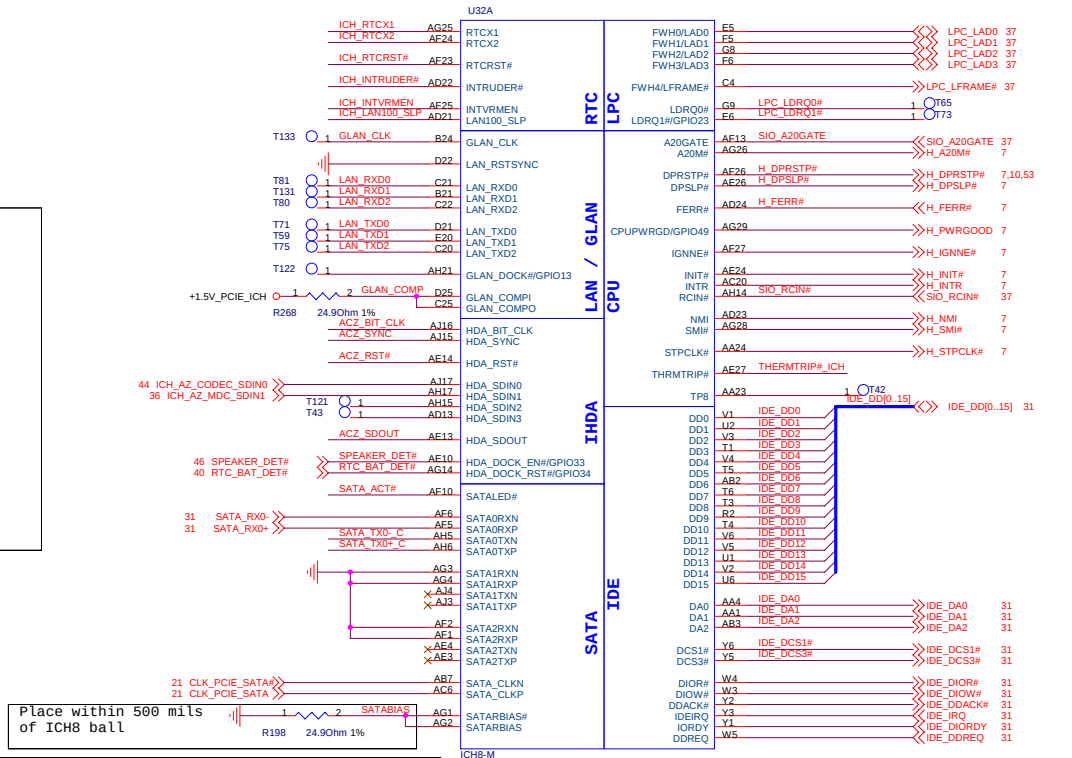


Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

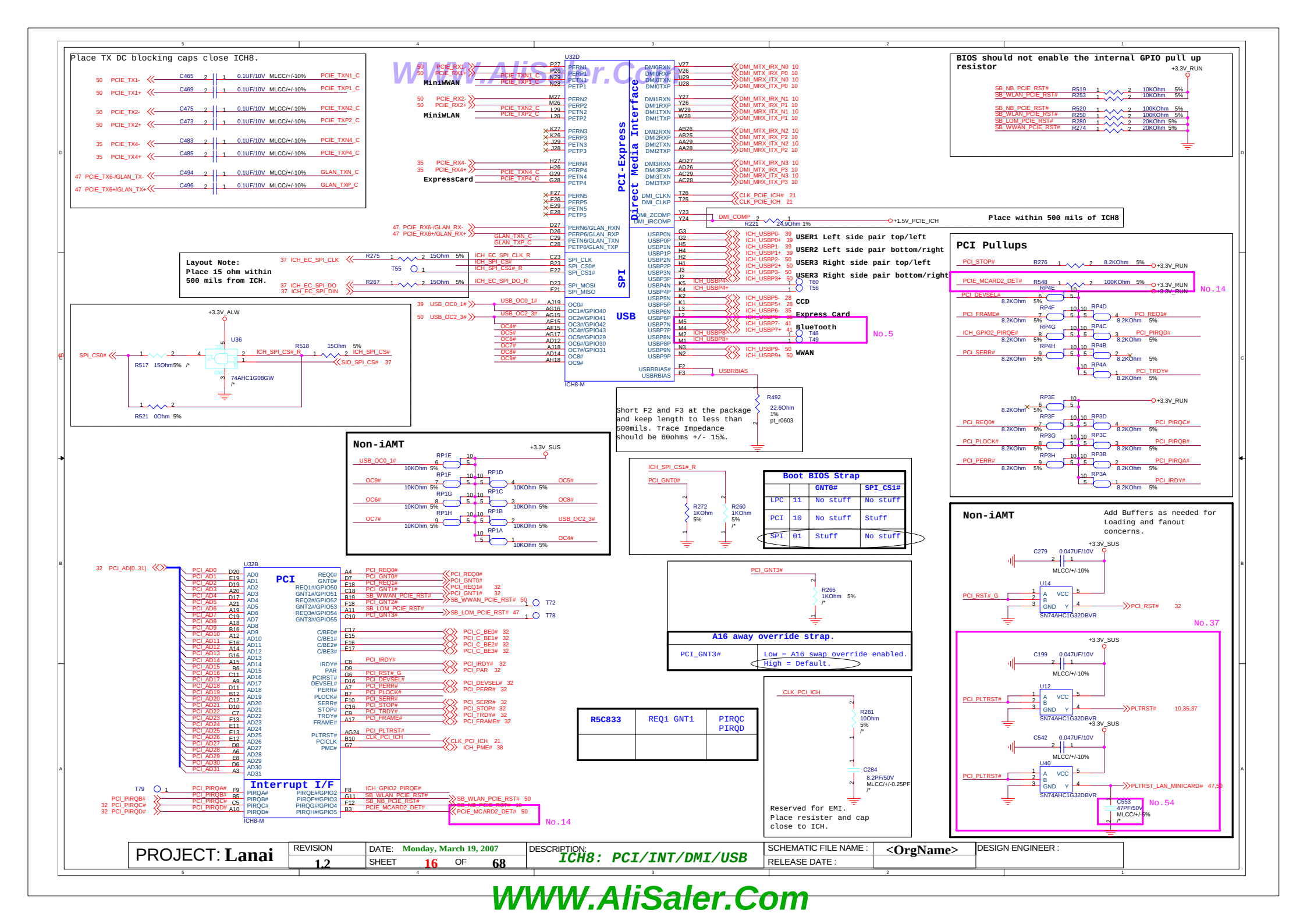








PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ICH8: IDE/AC97/LPC/RTC	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 15 OF 68		RELEASE DATE :	



Non-iAMT

+3.3V_SUS

RN37A 1 2 2.2KOhm 2 5% ICH_SMBDATA
RN37B 3 2 2.2KOhm 4 5% ICH_SMBCLK

Non-iAMT

+3.3V_SUS

R191 1 2 10KOhm 5% /* RSV_ICH_CL_RST1#
R216 1 2 10KOhm 5% AMT_SMBCLK
R217 1 2 10KOhm 5% AMT_SMBDAT
R224 1 2 10KOhm 5% ICH_RI#
R215 1 2 10KOhm 5% LOM_ICH_SMBALERT#
R214 1 2 1KOhm 5% ICH_PCIE_WAKE#

Place these close to ICH8

CLK_ICH_48M
No.26
R261 10Ohm 5%
C270 4.7PF/50V MLCC/+/-0.25PF
CLK_ICH_14M
R204 10Ohm /* 5%
C212 4.7PF/50V /* MLCC/+/-0.25PF

+3.3V_RUN

R185 8.2KOhm 5%
CLKRUN#
R184 10Ohm 5% /*

Option to "Disable " clkrun. Pulling it down will keep the clks running.

+3.3V_RUN

R422 8.2KOhm 5%

U32C

35,50 ICH_SMBCLK — ICH_SMBCLK AJ26 — SMBCLK
35,50 ICH_SMBDATA — ICH_SMBDATA AD19 — SMBDATA
T35 — RSV_ICH_CL_RST1# AG21 — LINKALERT#
AMT_SMBCLK AC17 — SMLINK0
AMT_SMBDAT AE19 — SMLINK1
SMB

ICH_RI# AF17 — RI#
T69 — F4 — SUS_STAT#/LPCPD#
7,38,52 XDP_DBRESET# — AD15 — SYS_RESET#
10 PM_BMBUSY# — AG12 — BMBUSY#/GPIO0
37 LOM_SMB_ALERT# — R173 0Ohm 5% /* — LOM_ICH_SMBALERT# AG22 — SMBALERT#/GPIO11
21 H_STP_PCI# — AE20 — STP_PCI#/GPIO15
21 H_STP_CPU# — AG18 — STP_CPU#/GPIO25
32,37 CLKRUN# — AH11 — CLKRUN#/GPIO32
38 ICH_PCIE_WAKE# — AE17 — WAKE#
32,37 IRQ_SERIRQ — AE12 — SERIRQ
RSV_THRM# — AC13 — THRM#
T46
37,51,53 IMVP_PWRGD — AJ20 — VRMPWRGD
T33 — AJ22 — TP7
SYS GPIO

USB_IDE# — A18
T120 — RSVD_GPIO6 — A9
38 SIO_EXT_WAKE# — SIO_EXT_WAKE# AH9
37 SIO_EXT_SMI# — SIO_EXT_SMI# AE16
37 SIO_EXT_SCI# — SIO_EXT_SCI# AC19
PCIE_MCARD1_DET# AG8
No.15 50 PCIE_MCARD1_DET# — R543 4.7KOhm — AH12
No.14 50 USB_MCARD1_DET# — T134 — RSVD_GPIO20 AE11
50 USB_MCARD2_DET# — T31 — USB_MCARD2_DET# AG10
USB_MCARD3_DET# AH25
31 IDE_RST_MOD AD16
21 SATA_CLKREQ# AG13
PLTRST_DELAY# AF9
T117 — RSVD_GPIO39 AJ11
No.9 28 CCD_VDD_ON — CCD_VDD_ON AD18
44 SPKR — AD9 — SPKR
10 MCH_ICH_SYNC# — R169 0Ohm 5% — MCH_ICH_SYNC#_R AJ13 — MCH_SYNC#
15 ICH_RSVD — AJ21 — TP3
ICH8-M
GPIO

TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48

SATA GPIO: SATA0GP/GPIO21 AJ12; SATA1GP/GPIO19 AJ10; SATA2GP/GPIO36 AF11; SATA3GP/GPIO37 AG11

Clocks: CLK14 AG9 — CLK_ICH_14M — CLK_ICH_14M 21; CLK48 G5 — CLK_ICH_48M — CLK_ICH_48M 21; SUSCLK D3 — ICH_SUSCLK — T76

Power MGT:
SLP_S3# AG23 — SIO_SLP_S3# 37
SLP_S4# AF21 — SIO_SLP_S4# — T36
SLP_S5# AD18 — SIO_SLP_S5# 37
S4_STATE#/GPIO26 AH27 — SIO_S4_STATE# — T124
PWROK AE23 — ICH_PWRGD — ICH_PWRGD 10,51
DPRSLPVR/GPIO16 AJ14 — DPRSLPVR — DPRSLPVR 10,53
BATLOW# AF21 — ICH_BATLOW# — R228 8.2KOhm 5% — +3.3V_SUS
PWRBTN# C2 — SIO_PWRBTN# 37
LAN_RST# AH20 — ICH_LAN_RST#
RSMRST# AG27 — R189 0Ohm 5% / R188 0Ohm 5% /* — ICH_RSMRST# 37; SUSPWROK 43,51
CK_PWRGD E1 — CLK_PWRGD 21
CLPWROK E3 — ICH_CL_PWROK — ICH_CL_PWROK 10,37
SLP_M# AJ25 — RSV_SIO_SLP_M# — T123

Controller Link:
CL_CLK0 F23 — RSV_ICH_CL_CLK1 — T39 — CL_CLK0 10
CL_CLK1 AE18
CL_DATA0 F22 — RSV_ICH_CL_DATA1 — T38 — CL_DATA0 10
CL_DATA1 AF19
CL_VREF0 D24 — CL_VREF0
CL_VREF1 AH23 — CL_VREF1 — T32
CL_RST# AJ23 — ICH_CL_RST0# 10

MISC:
CLGPIO0/GPIO24 AJ27 — PCIE_MCARD3_DET# — T30
CLGPIO1/GPIO10 AJ24 — ME_EC_ALERT — T119
CLGPIO2/GPIO14 AF22 — EC_ME_ALERT — T45
WOL_EN/GPIO9 AG19 — WOL_EN

Non-iAMT

ICH_PWRGD R200 1 2 10KOhm 5%
DPRSLPVR R420 1 2 100KOhm 5%
WOL_EN R193 1 2 100KOhm 5%
SUSPWROK R176 1 2 10KOhm 5% /*
ICH_LAN_RST# R174 1 2 1MOhm 5%
ICH_CL_PWROK R262 1 2 1MOhm 5%

+3.3V_SUS
EC_ME_ALERT R237 1 2 8.2KOhm 5%

USB_IDE# R419 1 2 8.2KOhm 5% +3.3V_RUN
SIO_EXT_SCI# R227 1 2 10KOhm 5% +3.3V_SUS

+3.3V_RUN

R212 1KOhm 5% /*
SPKR

No Reboot strap.

SPKR	Low=Default High=No Reboot

Non-iAMT

SMBus address D2

These are for backdrive issue

+3.3V_RUN
RN36A 2.2KOhm 5%
RN36B 2.2KOhm 5%
35,50 ICH_SMBDATA — Q36 2N7002 Id=180mA/Pd=300mW — MEM_SDATA 19
+3.3V_RUN
35,50 ICH_SMBCLK — Q35 2N7002 Id=180mA/Pd=300mW — MEM_SCLK 19

Pull up for each detect line

+3.3V_RUN
RP2E 100KOhm 5%
RP2F 100KOhm 5%
RP2G USB_MCARD3_DET# 100KOhm 5%
RP2H USB_MCARD2_DET# 100KOhm 5%
RP2D USB_MCARD1_DET# 100KOhm 5%
RP2C PCIE_MCARD3_DET# 100KOhm 5%
RP2B 100KOhm 5%
RP2A PCIE_MCARD1_DET# 100KOhm 5%

+3.3V_RUN

No.14
R555 1 2 100KOhm 5% RSVD_GPIO20
R235 1 2 10KOhm 5% RSV_THRM#
R168 1 2 10KOhm 5% /* MCH_ICH_SYNC#_R
R206 1 2 10KOhm 5% IRQ_SERIRQ
R424 1 2 10KOhm 5% RSVD_GPIO6
R423 1 2 10KOhm 5% RSVD_GPIO39
R195 1 2 10KOhm 5% PLTRST_DELAY#
R544 1 2 100KOhm 5% CCD_VDD_ON
No.9

+3.3V_SUS

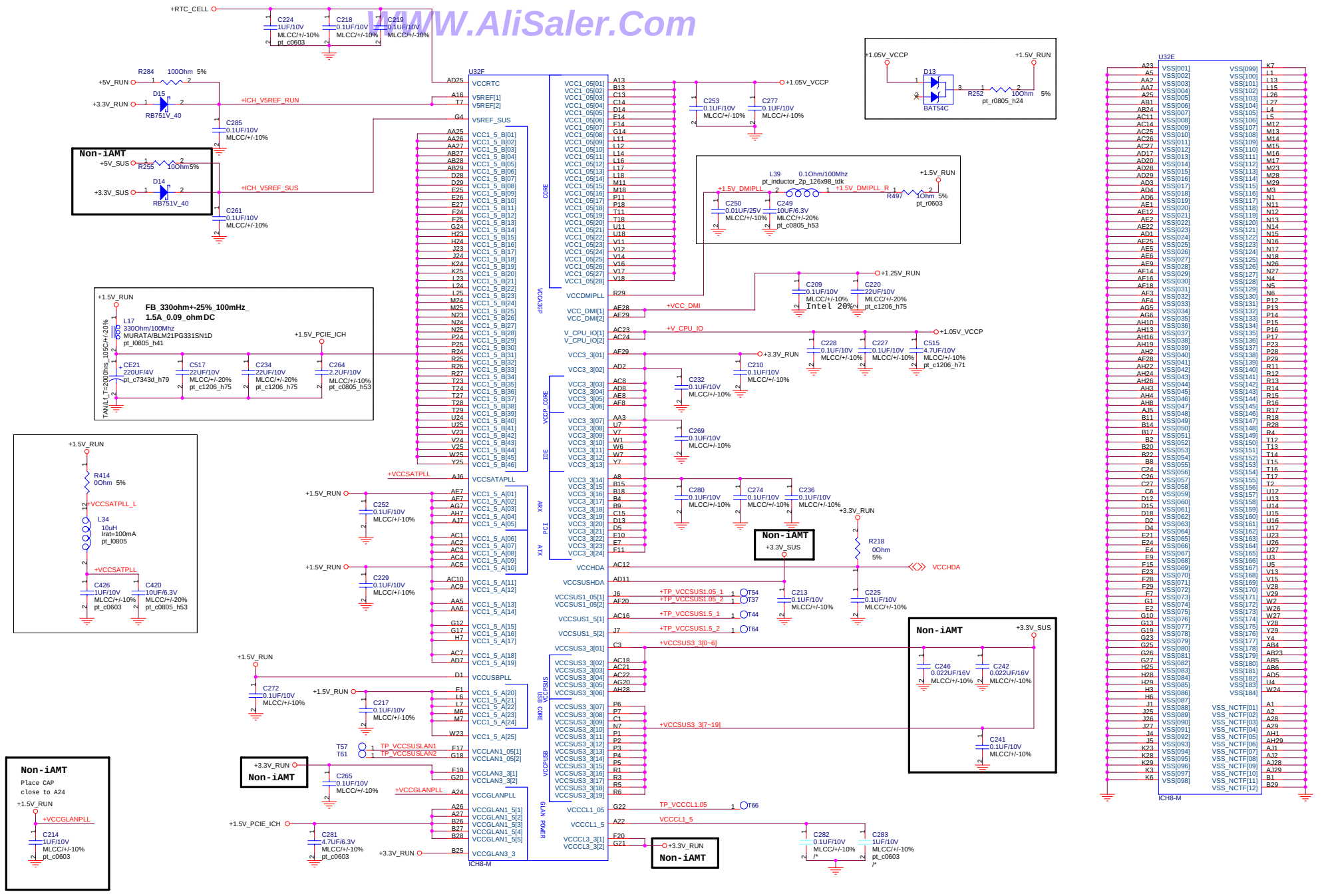
R226 1 2 10KOhm 5% SIO_EXT_SMI#

Non-iAMT

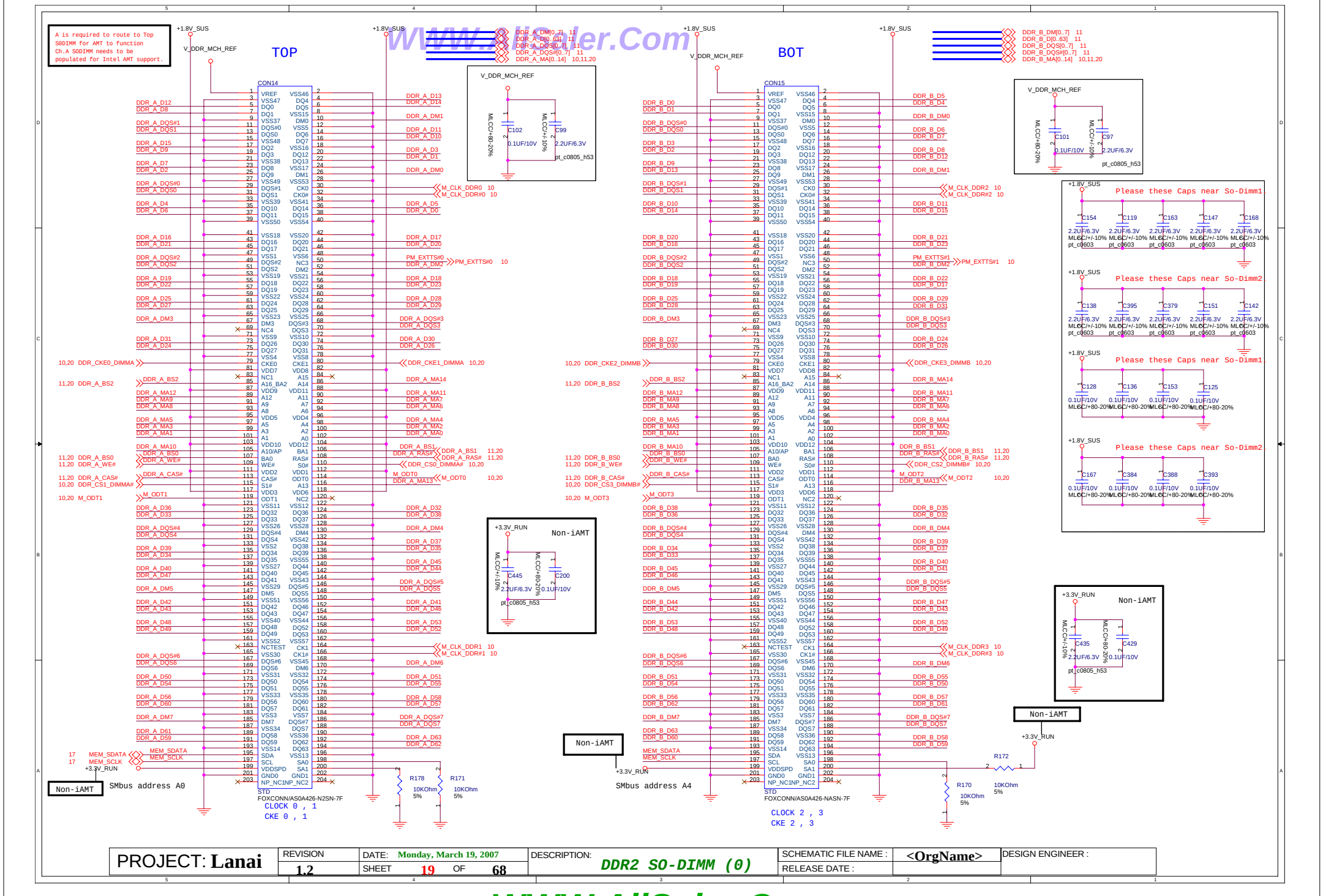
+3.3V_RUN
R277 3.24KOhm 1%
CL_VREF0
C278 0.1UF/10V MLCC/+80-20%
R278 453Ohm 1%

+3.3V_SUS
R180 3.24KOhm 1% /*
CL_VREF1
C201 0.1UF/10V MLCC/+80-20% /*
R179 453Ohm 1% /*

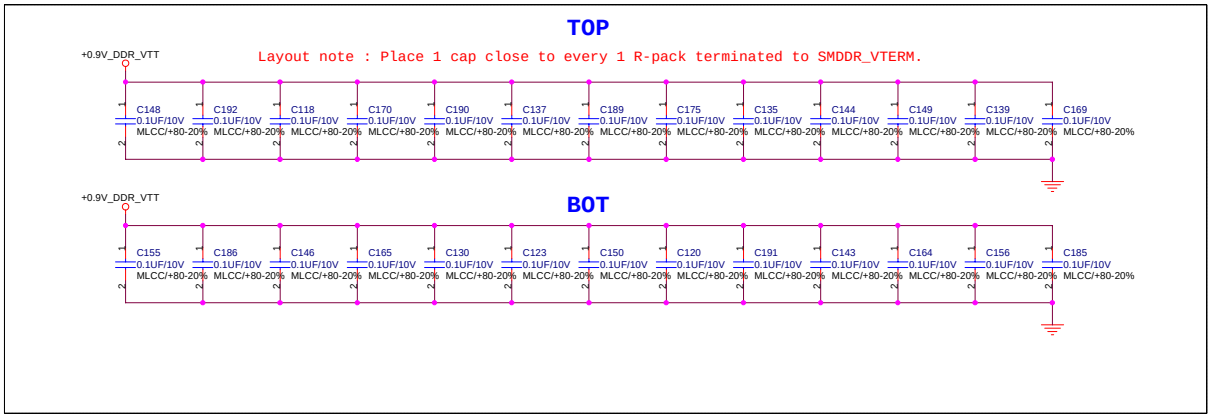
PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	SHEET 17 OF 68	DESCRIPTION: ICH8: SMB/PWR/CLK/GPIO	SCHEMATIC FILE NAME: <OrgName>	RELEASE DATE:	DESIGN ENGINEER:

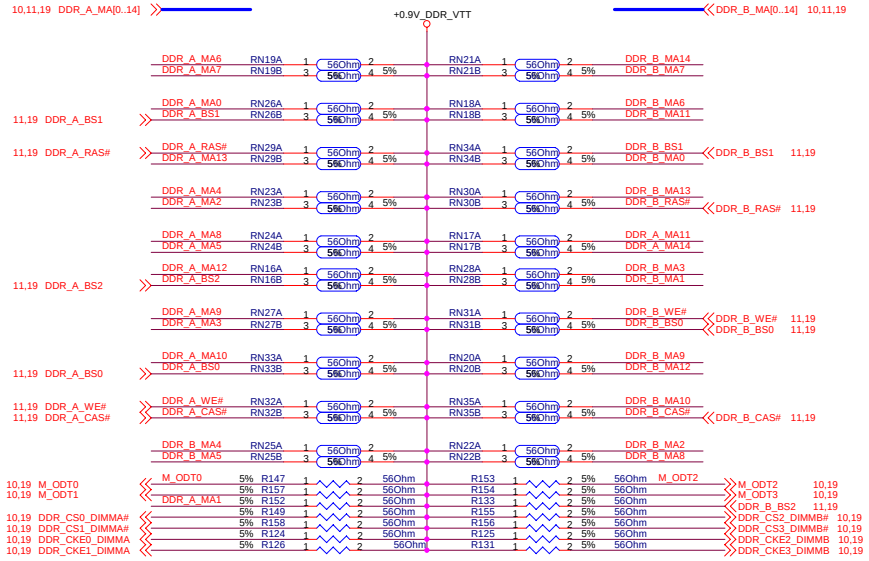


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 18 OF 68	DESCRIPTION: ICH8-M(POWER,GND)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
					RELEASE DATE :	



PROJECT: **Lanai**	REVISION: **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***DDR2 SO-DIMM (0)***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET **19** OF **68**		RELEASE DATE :		

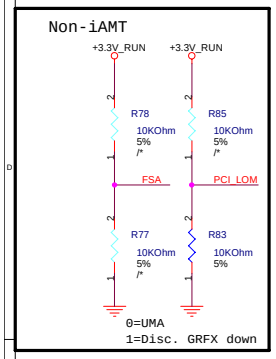


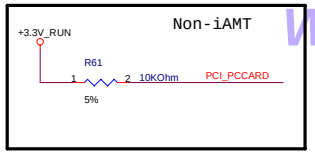


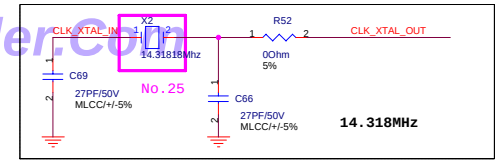
Please these resistor closely DIMMA, all trace length<750 mil.

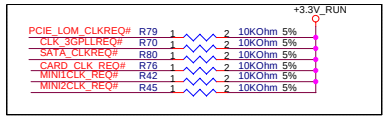
Please these resistor closely DIMMB, all trace length<750 mil.

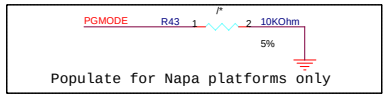
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***DDR2 SO-DIMM (1)***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET **20** OF **68**		RELEASE DATE :		

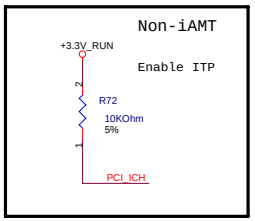


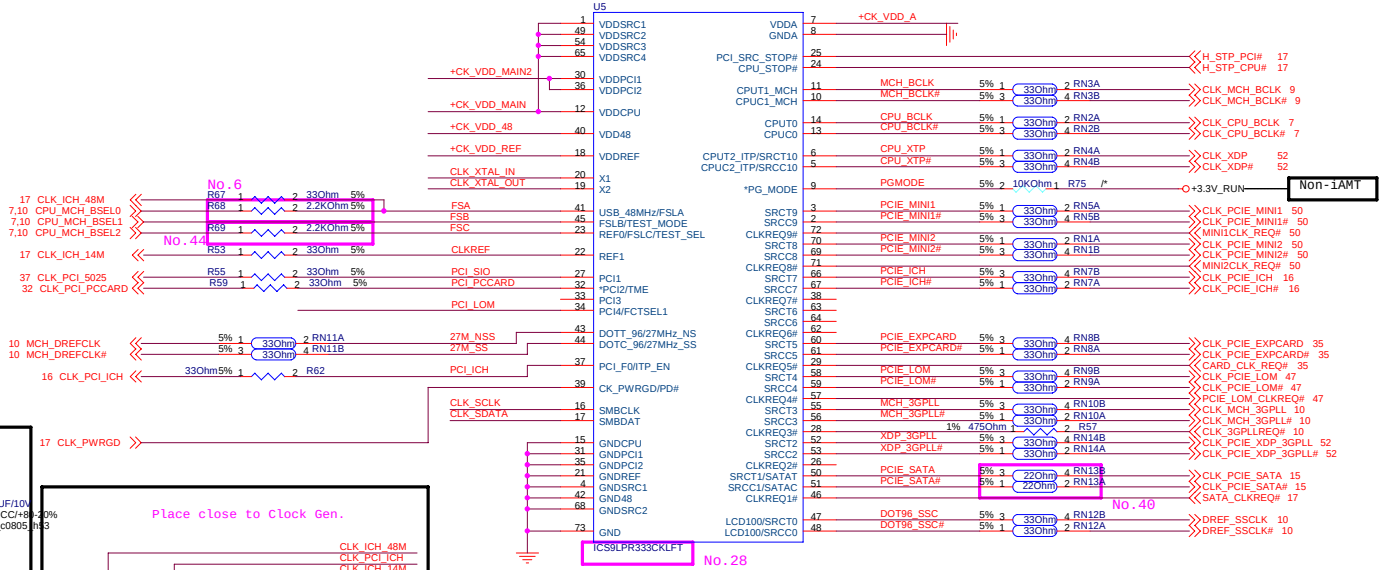


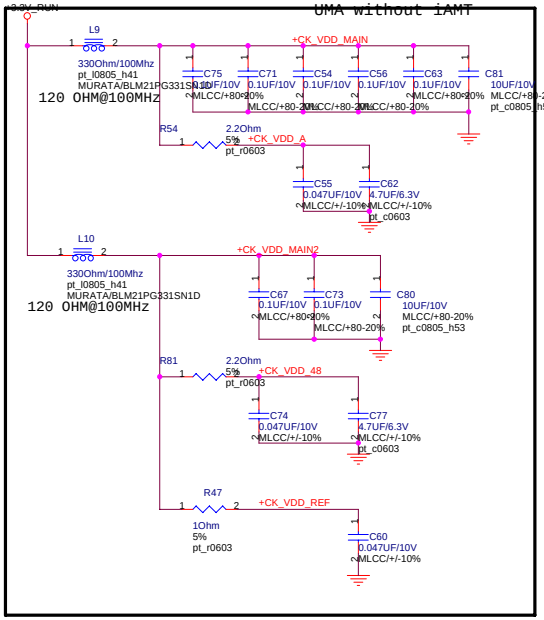


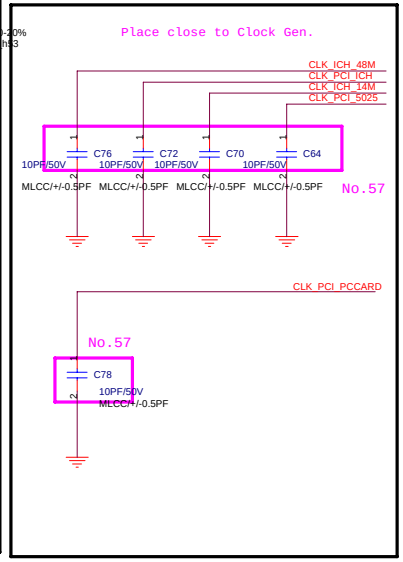


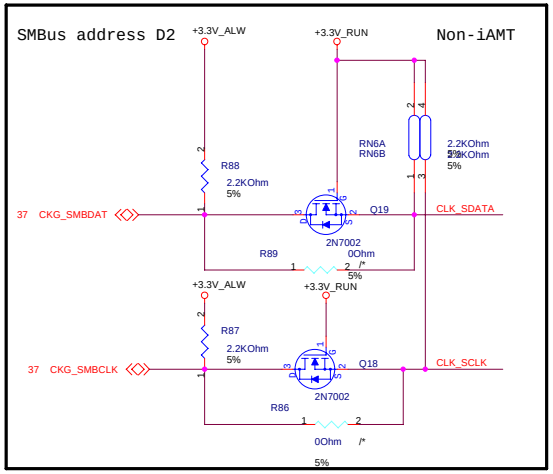












FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM=FCTSEL1

FCTSEL1(PIN 34)	Pin43	Pin44	Pin47	Pin48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27M_SSout	SRCT0	SRCC0

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 21 OF 68	CLK GEN. CY28547	RELEASE DATE :		

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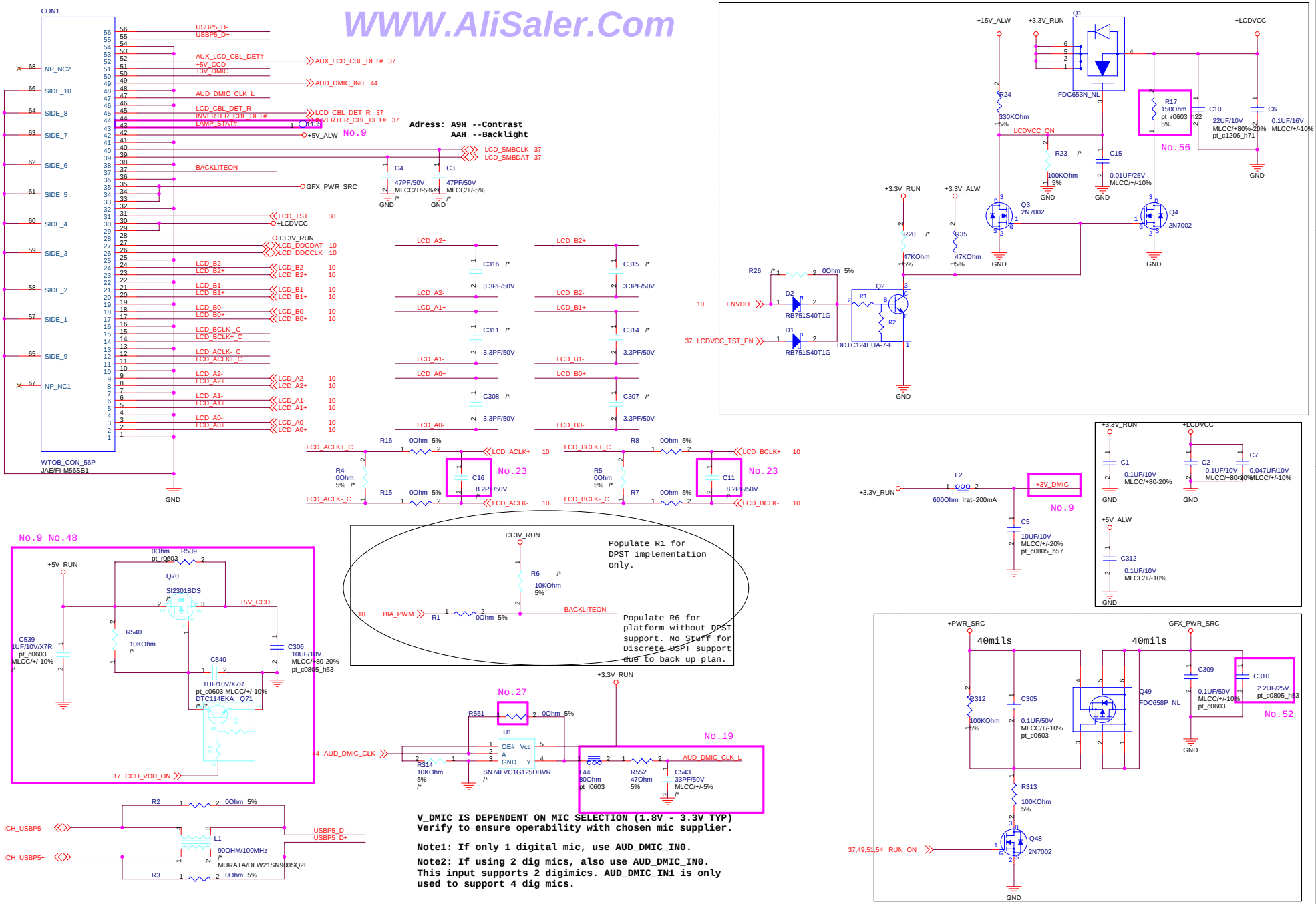
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 23 OF 68		RELEASE DATE :		

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 24 OF 68		RELEASE DATE :		

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 25 OF 68		RELEASE DATE :		

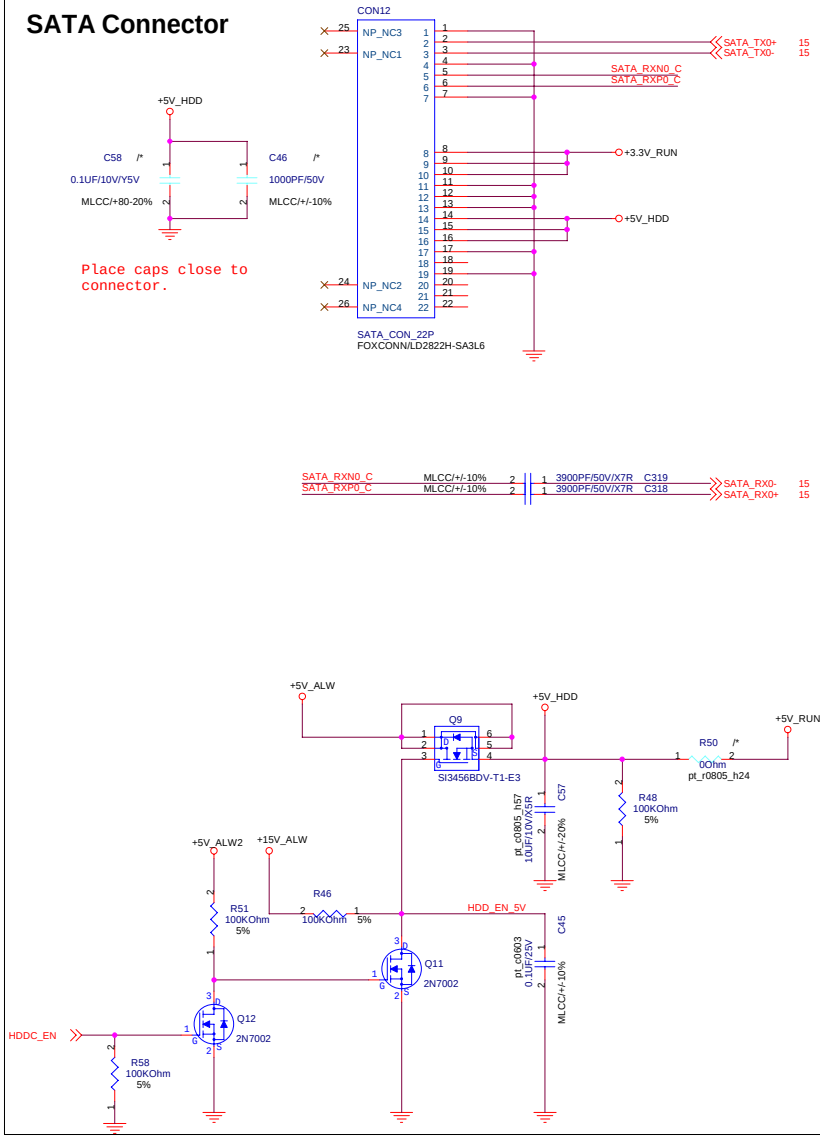
PROJECT: **Lanai**	REVISION	DATE: **Monday, March 19, 2007**	DESCRIPTION:	SCHEMATIC FILE NAME :		DESIGN ENGINEER :
	1.2	SHEET **26** OF **68**		RELEASE DATE :		

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER : *Sean Kuo*
		SHEET **27** OF **68**		RELEASE DATE :	

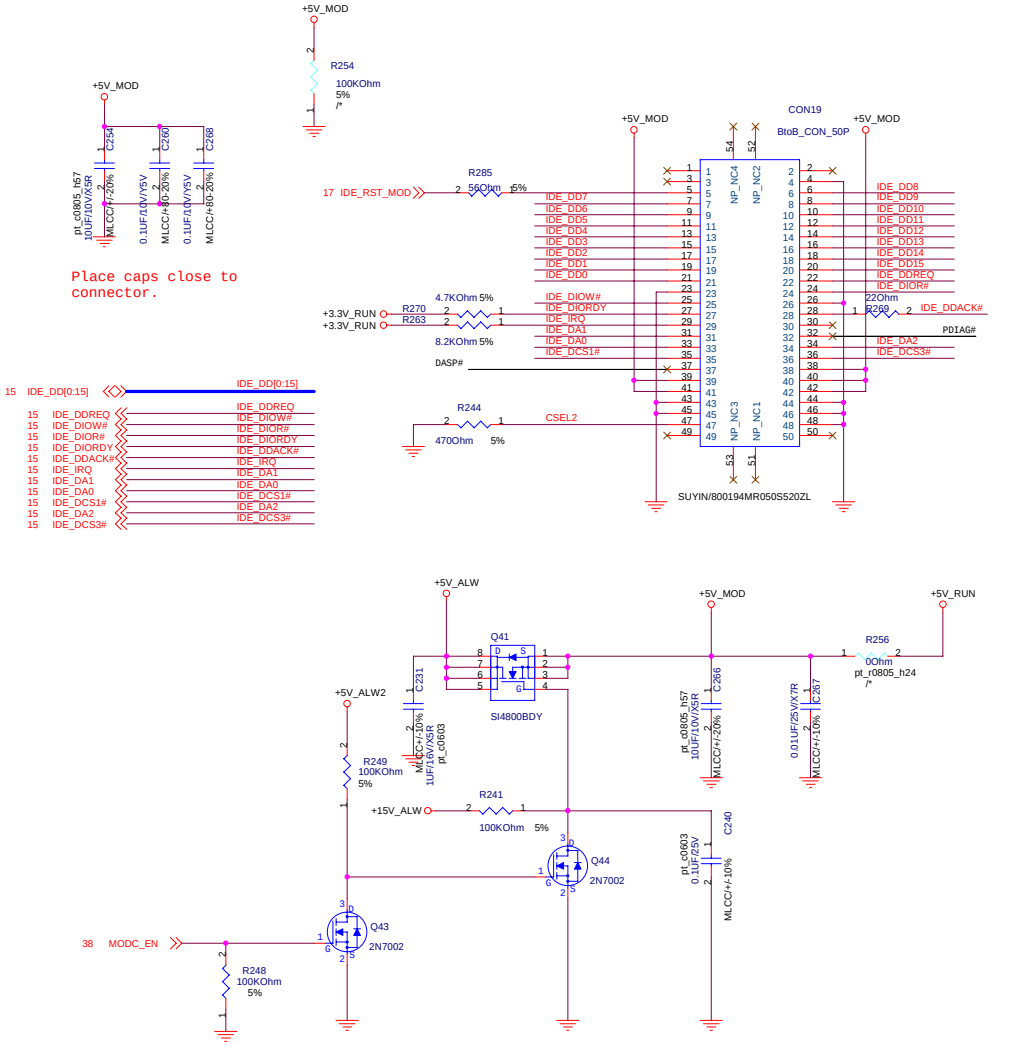


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***LVDS CON***	SCHEMATIC FILE NAME :		DESIGN ENGINEER :
		SHEET **28** OF **68**		RELEASE DATE :		

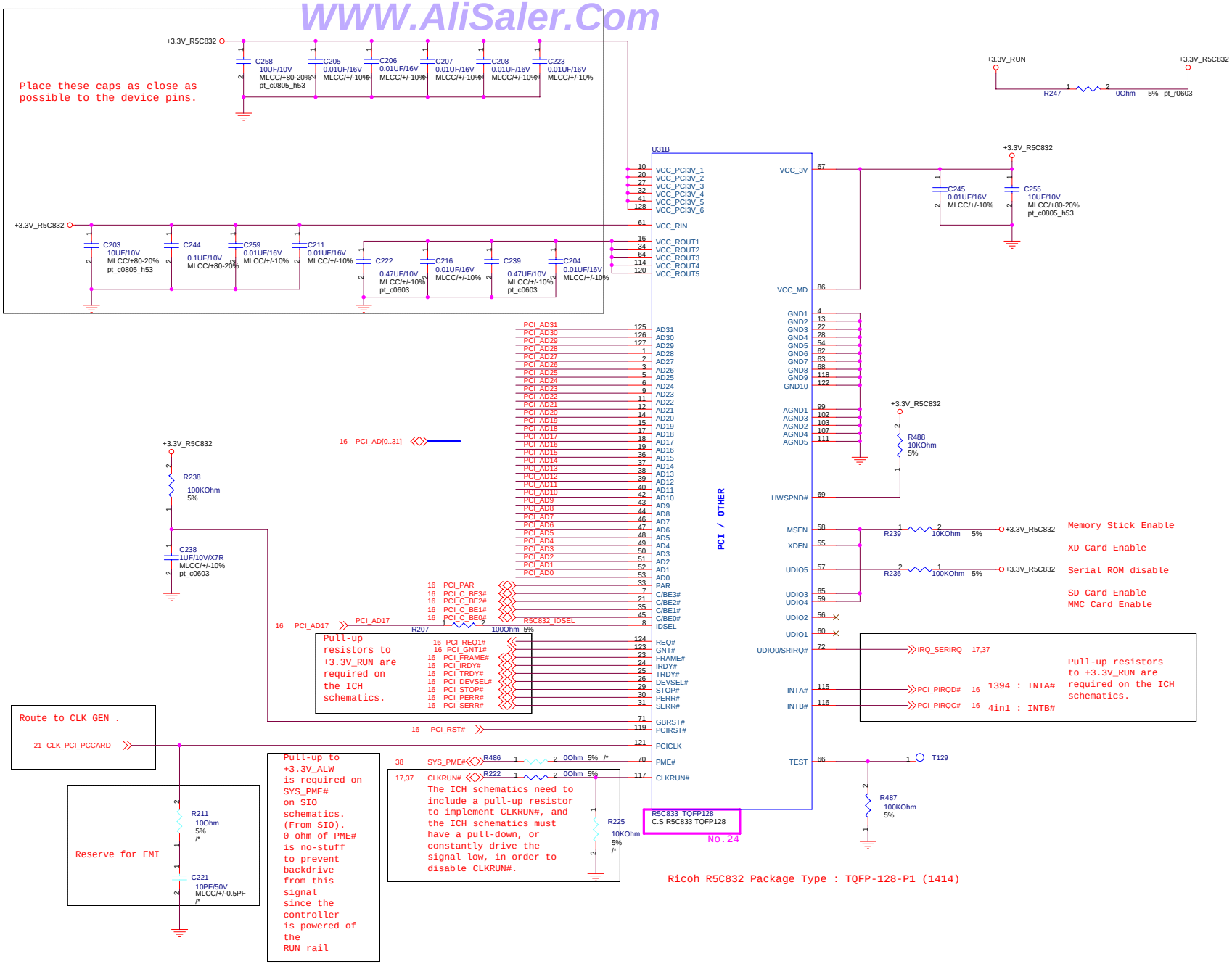
SATA Connector



ODD Connector



PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :	
	1.2	SHEET 31 OF 68	*SATA(HDD & CD_ROM)*	RELEASE DATE :			



PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 32 OF 68	*R5C833 - PCI INTERFACE*	RELEASE DATE :		

Recommended Crystal Specs from Data Sheet:

Normal Frequency : 24.576 MHz
Frequency Tolerance : +/- 50ppm @ 25C
Driver Level : .1 mW
Load capacitance : 10pF
Equ. Resistance : 50 Ohm Max
Shunt Capacitance : 7.0pF Max

No.25

C478 15PF/50V MLCC/+/-5%
X5 24.576Mhz +/-50ppm/10PF
C477 15PF/50V MLCC/+/-5%
1394_XI
1394_XO
R483 0Ohm 5%

No.24

R5C832 : 0.01uF => stuff
R5C833 : 0.01uF => No stuff

C256 0.01UF/16V MLCC/+/-10% /*
R474 10KOhm 1%
C243 0.01UF/16V MLCC/+/-10%
RICHO_FIL0
RICHO_REXT
RICHO_VREF

Place as close to R5C832 as possible.

U31A

XI
XO
FIL0
REXT
VREF
RSV

IEEE1394/SD

+3.3V_RUN_PHY

AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4

TPBIAS0
TPB0N
TPB0P
TPA0N
TPA0P

MDIO17 XD_DATA7
MDIO16 XD_DATA6
MDIO15 XD_DATA5
MDIO14 XD_DATA4
MDIO13 SD/XD/MS_DATA3
MDIO12 SD/XD/MS_DATA2
MDIO11 SD/XD/MS_DATA1
MDIO10 SD/XD/MS_DATA0
MDIO05 XD_WP#
MDIO08 SD/XD/MS_CMD
MDIO19 XD_ALE
MDIO18 XD_CLE
MDIO02 XD_CE#
MDIO03 SD_WP#(XDR/B#)
MDIO00 SD_CD#
MDIO01 XD_CDSW#
MDIO09 SD/XD/MS_CLK
MDIO04 MC_PWR_CTRL_0
MDIO06 MS_LED#
MDIO07

D20 1N4148W-7-F
D21 1N4148W-7-F
MS_INS#
R484 0Ohm 5%
TPC26T T130
C552 10PF/50V MLCC/+/-0.5PF

No.51

R5C833_TQFP128
C.S R5C833 TQFP128

No.24

+3.3V_RUN_CARD

C461 0.01UF/16V MLCC/+/-10%
C459 0.01UF/16V MLCC/+/-10%
C458 0.01UF/16V MLCC/+/-10%
R456 150KOhm 5%

Place these components close to the flash memory card connector

For SD/MS Card Power

No.24

U33 TPS2051BDBVR
MC_PWR_CTRL_0
+3.3V_R5C832
+3.3V_RUN_CARD
C481 0.1UF/10V MLCC/+80-20%
C472 1UF/10V MLCC/+80%-20% pt_c0603

CON20 TAISOL/144-2420000900
CARD_READER_41P

XD_0(GND) XD_1(CD) XD_2(R/-B) XD_3(-RE) XD_4(-CE) XD_5(CLE) XD_6(ALE) XD_7(-WE) XD_8(-WP) XD_9(GND) XD_10(D0) XD_11(D1) XD_12(D2) XD_13(D3) XD_14(D4) XD_15(D5) XD_16(D6) XD_17(D7) XD_18(VCC) MS_1(VSS) MS_2(BS)

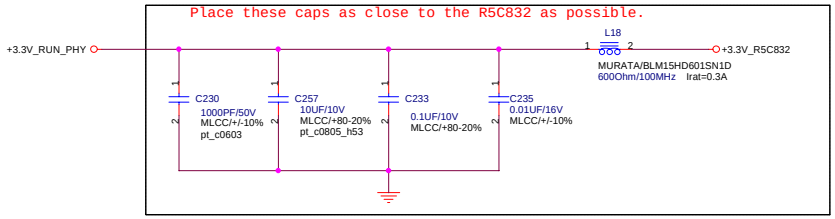
MS_3(DATA1) MS_4(DATA0) MS_5(DATA2) MS_6(INS) MS_7(DATA3) MS_8(SCLK) MS_9(VCC) MS_10(VSS) SD_1(DAT3) SD_2(CMD) SD_3(VSS) SD_4(VDD) SD_5(CLK) SD_6(VSS) SD_7(DAT0) SD_8(DAT1) SD_9(DAT2) SD(CD2/WP2/GND) SD(CD1) SD(WP1)

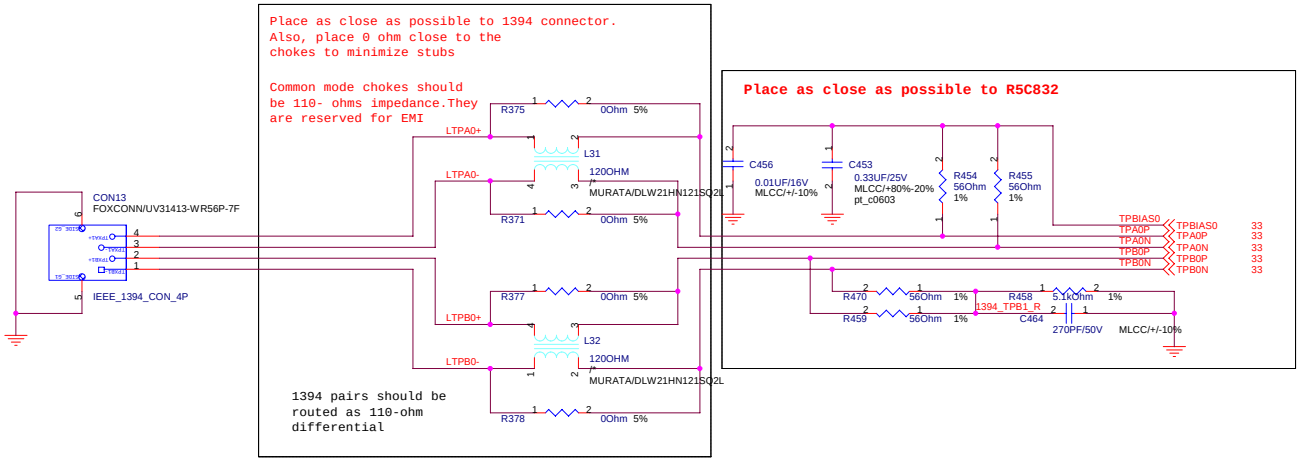
NP_NC1 NP_NC2 P_GND1 P_GND2

C457 2.2UF/16V MLCC/+/-10% pt_c0603

Q72 2N7002

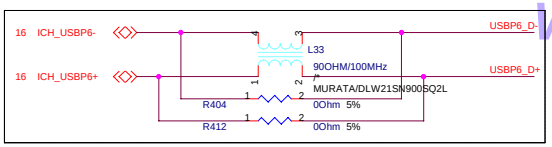
No.47

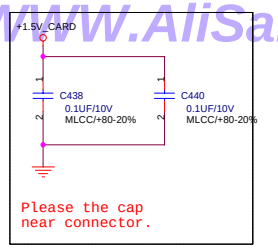


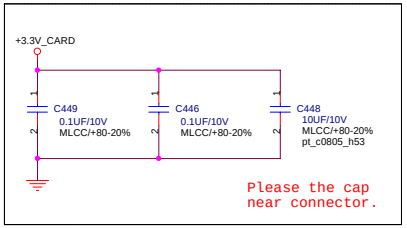


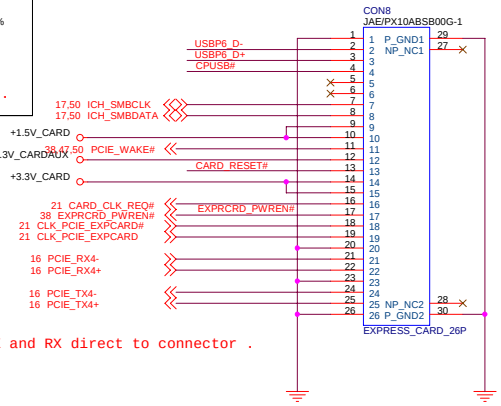
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***R5C833 - IEEE1394 PART***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 34 OF 68		RELEASE DATE :		

Express Card



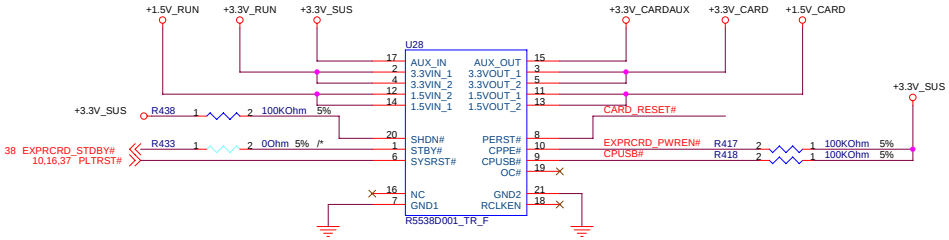


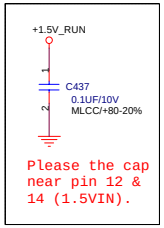


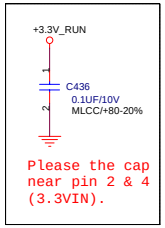


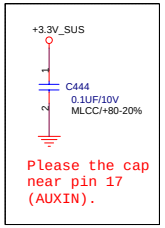
PCI-Express TX and RX direct to connector .

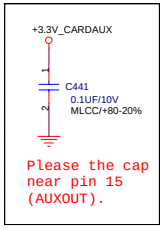
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

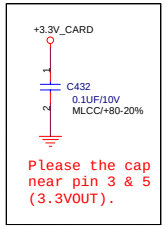


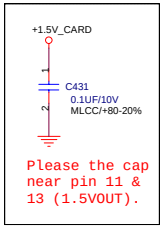




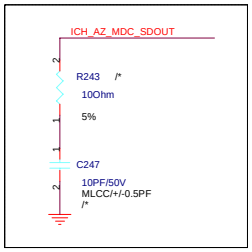


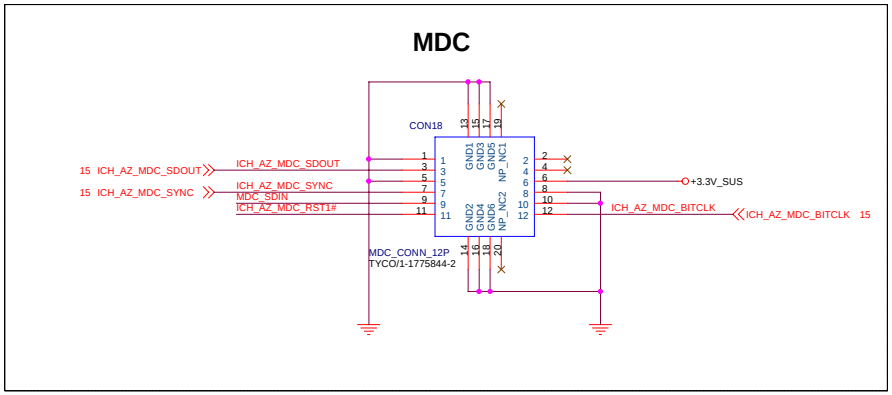


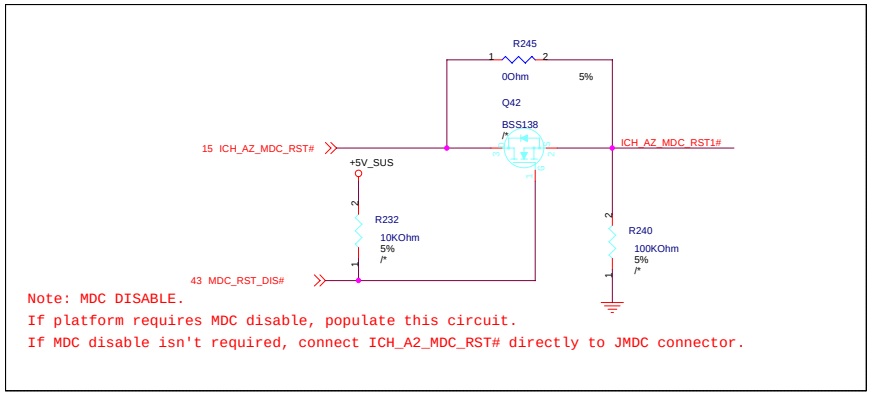


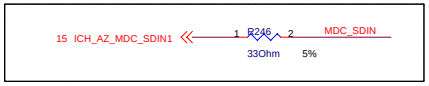


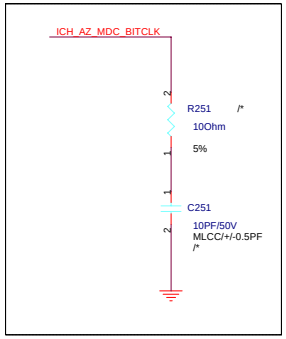
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 35 OF 68	PCI-Express Card	RELEASE DATE :		Terry_Lin

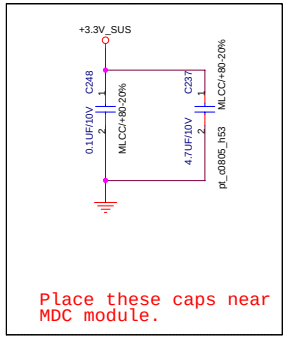












PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 36 OF 68	*MDC CONN*	RELEASE DATE :		

(GPIO4)	(GPIO5)	CHIPSET
CHIPSET_ID1	CHIPSET_ID0	Common Boot block sequence
0	0	Intel-SR
0	1	ATI-RR
1	0	TBD
1	1	Parker(Intel/ATI)

Non iAMT

Non iAMT

Place cap close to pin 121.

Place these caps close to MEC5025

Place close to pin 58

32KHz Clock

External Work Around Circuit.

For MEC5025 Rev. C : C4519= 22uF and populate workaround circuit.
For MEC5025 Rev. D : C4519= 4.7uF and depopulate workaround circuit.

Debug Serial Port Flash Recovery Port.

Not Stuff 0 ohm when doing Flash recovery.

Populate for flash corruption issue.

No.33

No.18

No.36

1 = Enabled.
0 = Disabled

Flash Recovery

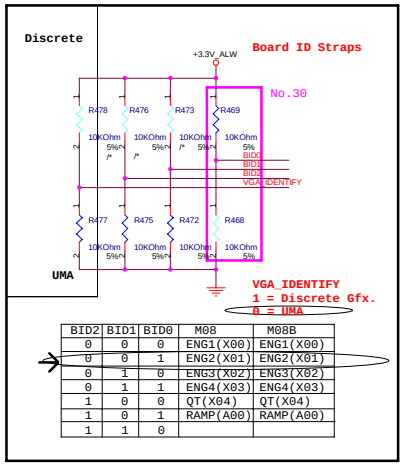
Low= Write Protected.

Flash Write Protect bottom 4K of internal bootblock flash

MLX_53398-0371

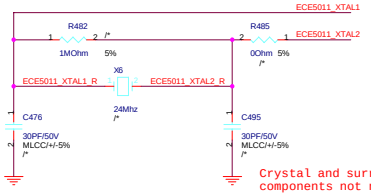
MLX_53398-0371

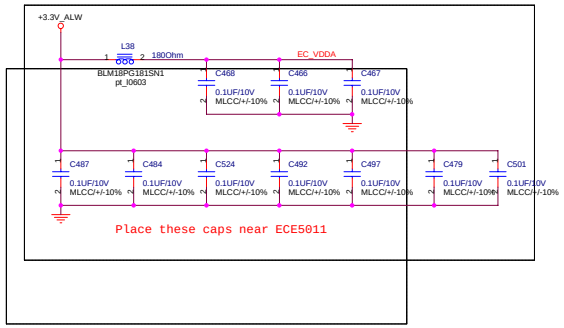
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 37 OF 68	DESCRIPTION: MEC5025	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : STANLY_HSU

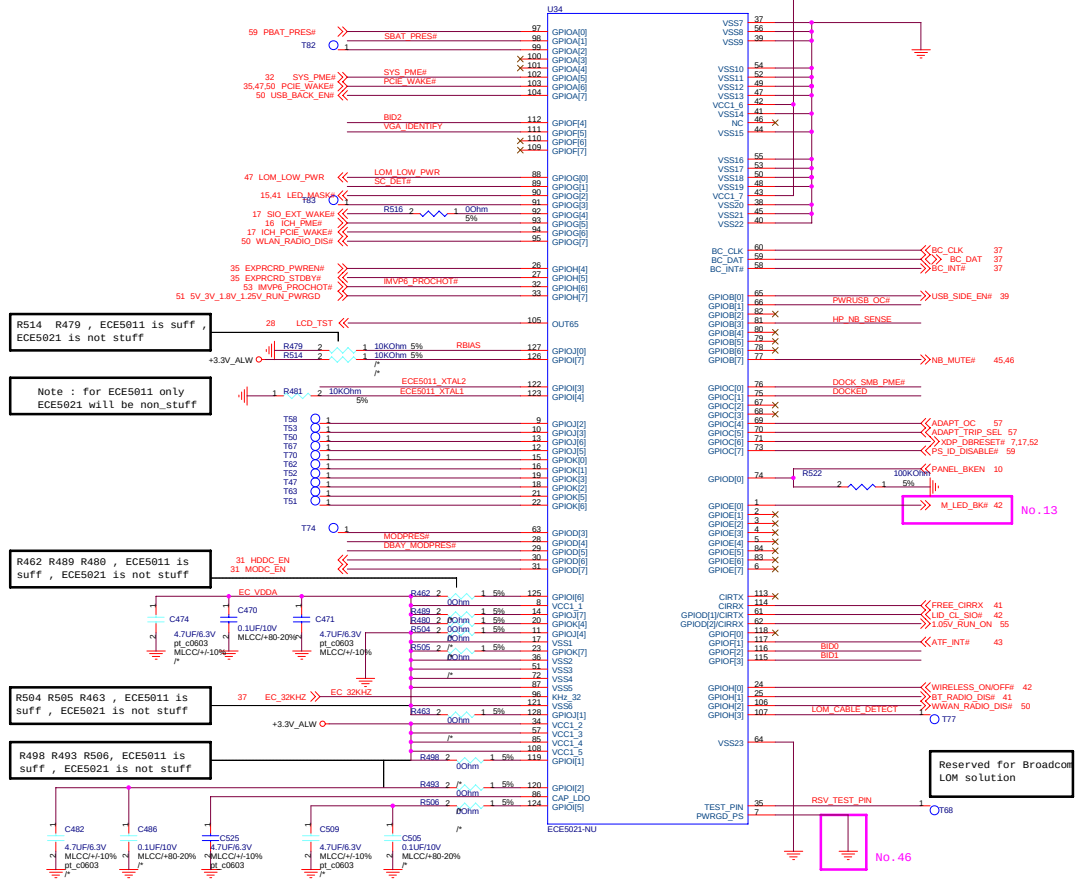


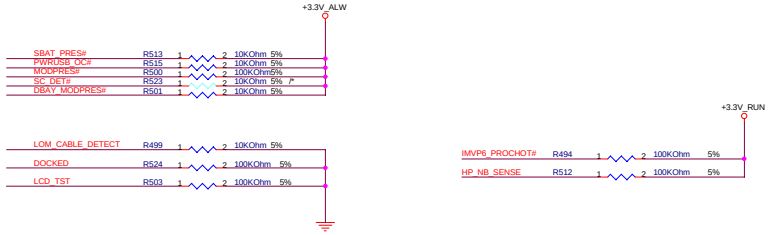
BID2	BID1	BID0	M08	M08B
0	0	0	ENG1(X00)	ENG1(X00)
0	0	1	ENG2(X01)	ENG2(X01)
0	1	0	ENG3(X02)	ENG3(X02)
0	1	1	ENG4(X03)	ENG4(X03)
1	0	0	QT(X04)	QT(X04)
1	0	1	RAMP(A00)	RAMP(A00)
1	1	0		

24MHz Clock

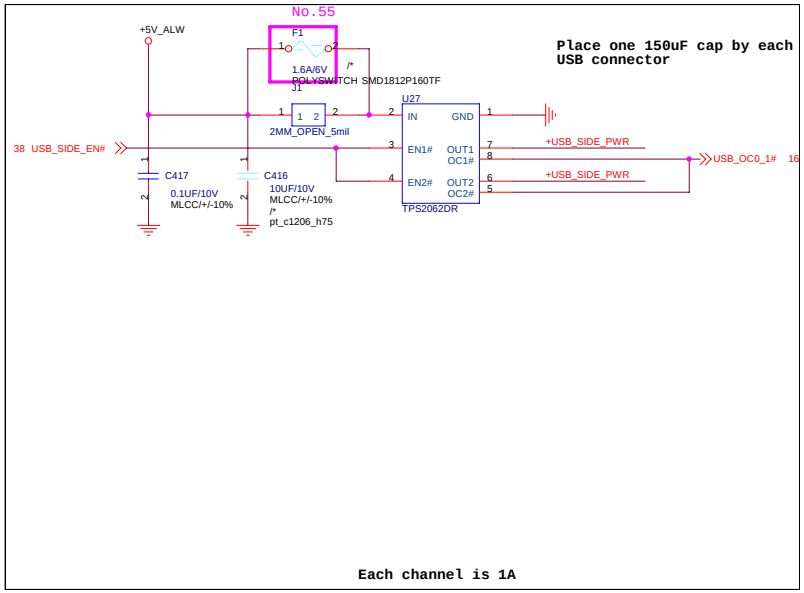


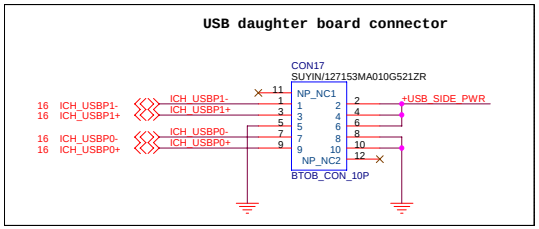




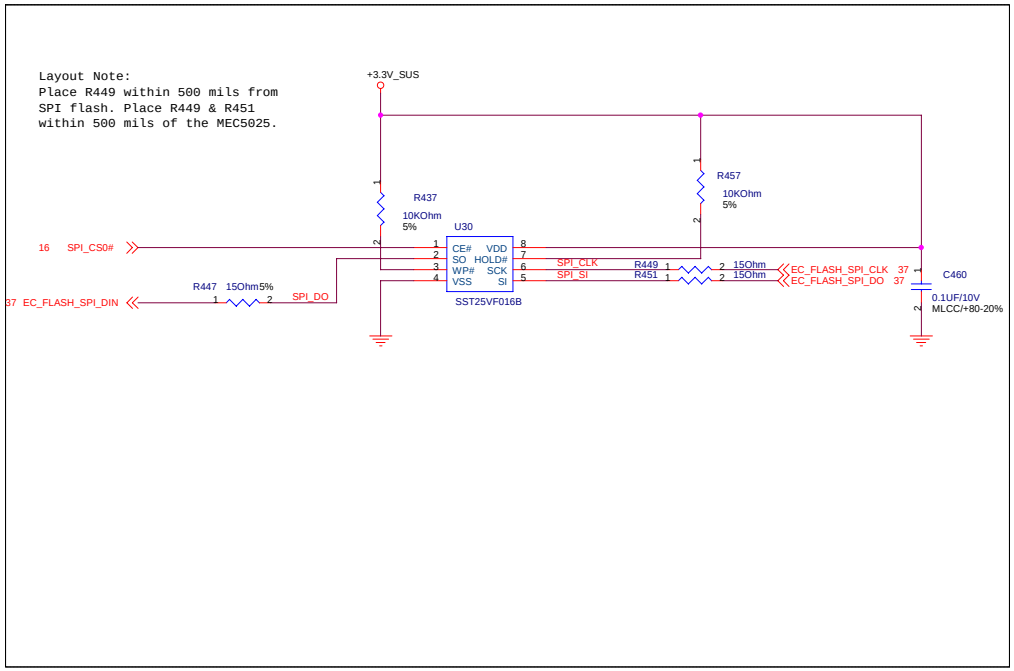


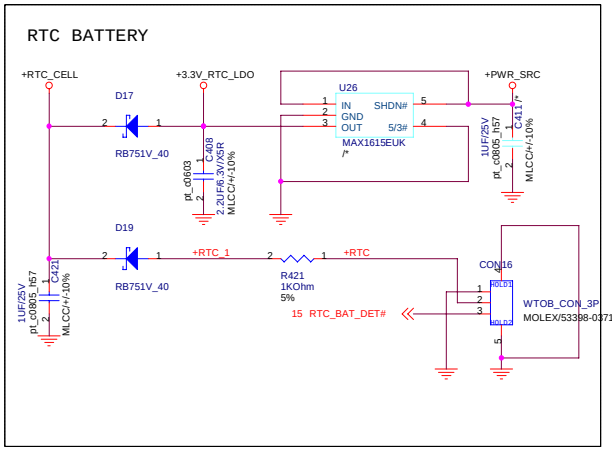
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 38 OF 68	DESCRIPTION: SUPER IO ECE5011	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : STANLY_HSU

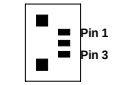




PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 39 OF 68	*USB PORT x 2*	RELEASE DATE :		*Terry_Lin*



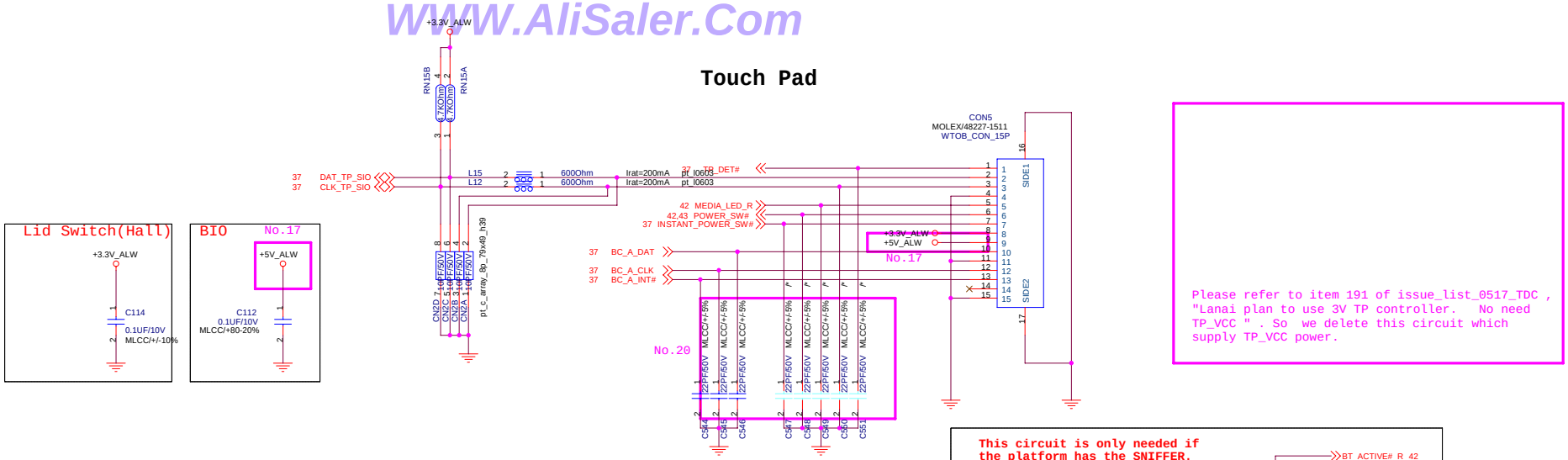




MLX_53398-0371

PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 40 OF 68	*FLASH & RTC*	RELEASE DATE :		*C.L. Ho*

Touch Pad

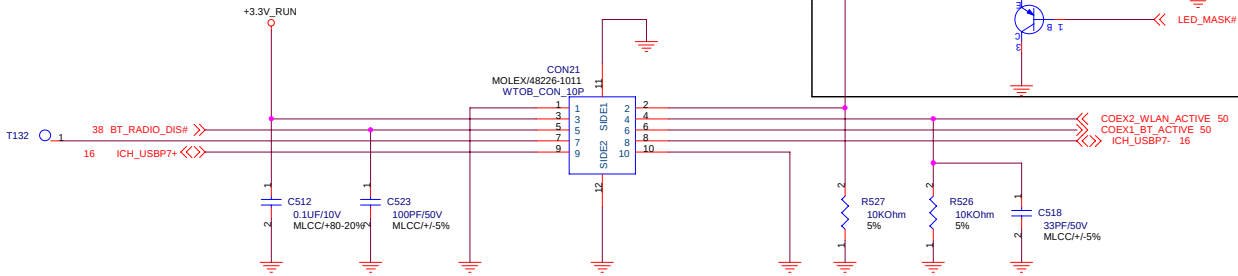


Please refer to item 191 of issue_list_0517_TDC , "Lanai plan to use 3V TP controller. No need TP_VCC " . So we delete this circuit which supply TP_VCC power.

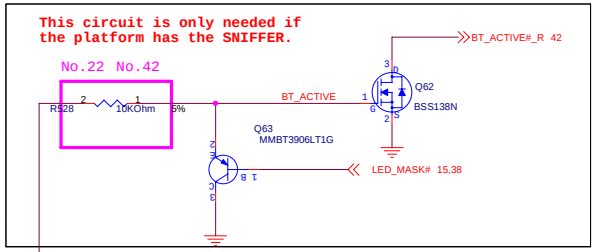
Lid Switch(Hall)

BIO

Bluetooth

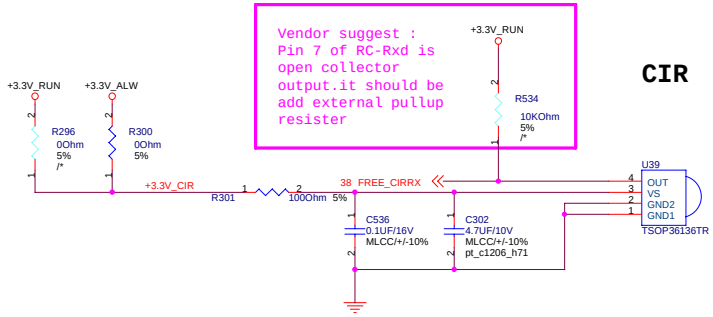


This circuit is only needed if the platform has the SNIFFER.

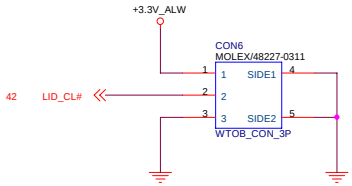


CIR

Vendor suggest : Pin 7 of RC-Rxd is open collector output.it should be add external pullup resister

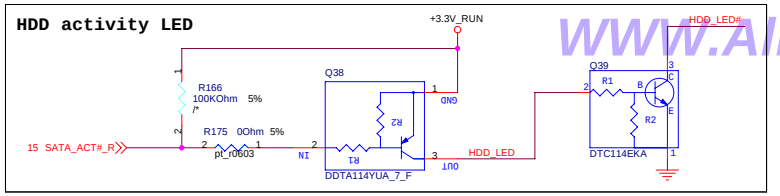


HALL SENSOR

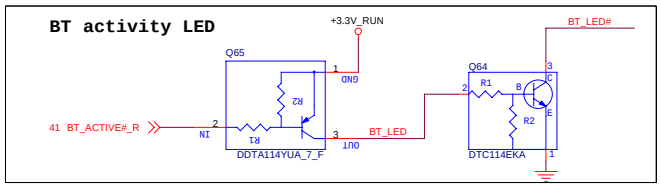


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: **TOUCH PAD & BT & CIR & LID**	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **41** OF **68**		RELEASE DATE :		

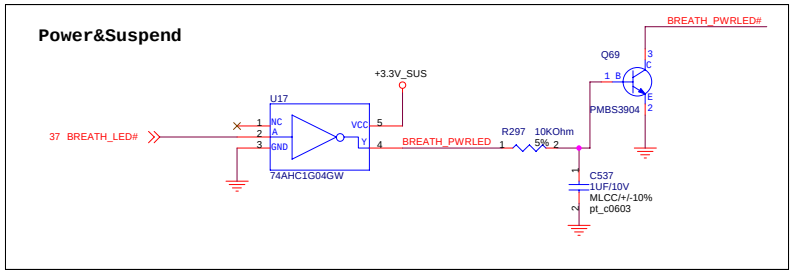
HDD activity LED



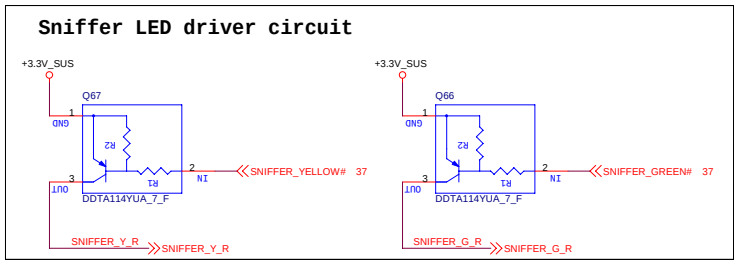
BT activity LED

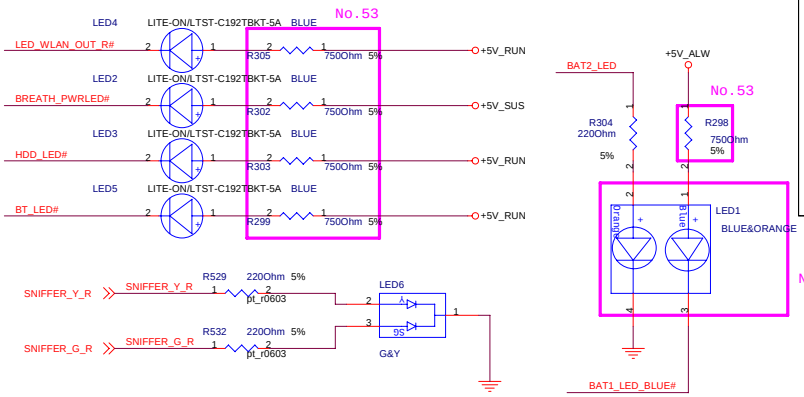


Power&Suspend

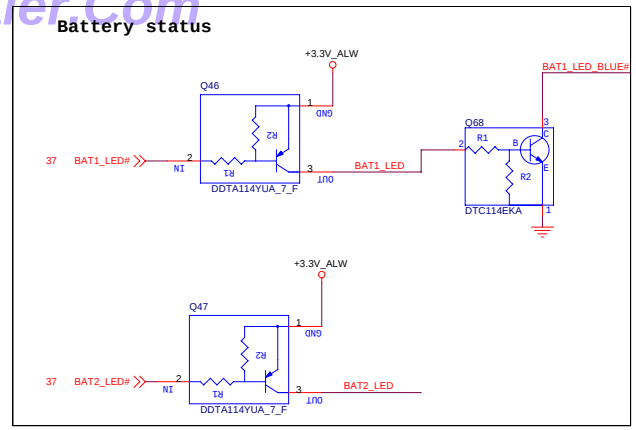


Sniffer LED driver circuit

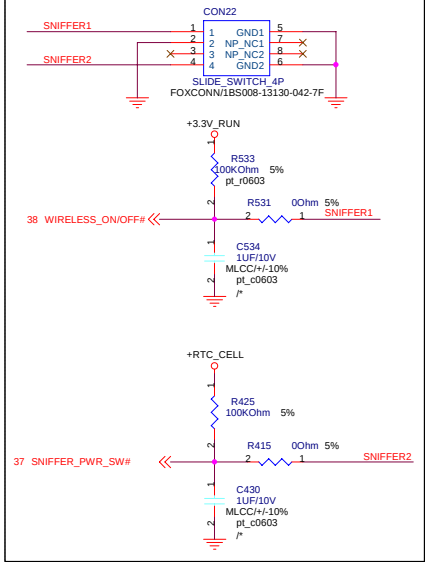




Battery status

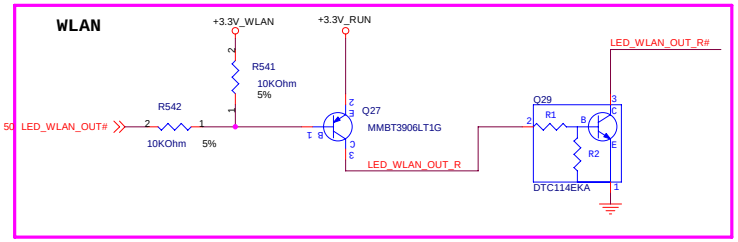


Sniffer Switch

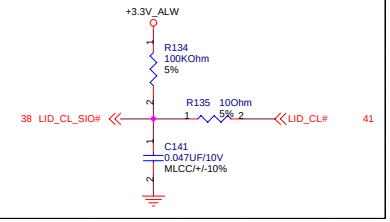


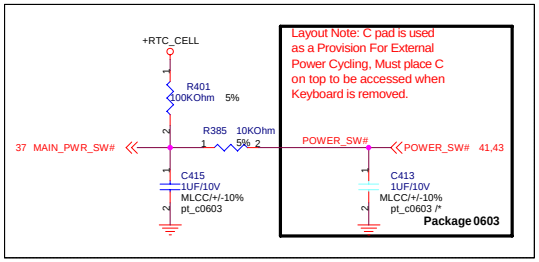
No.8

WLAN

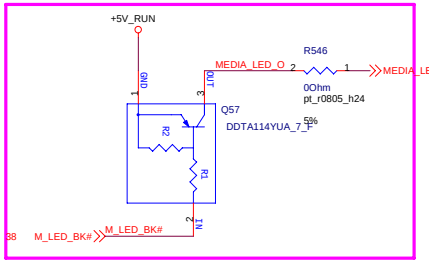


Hall Switch





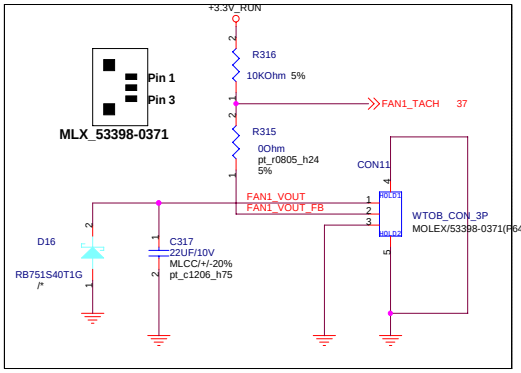
Media Bottom Board LED drive circuit

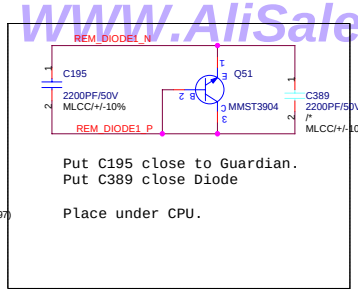


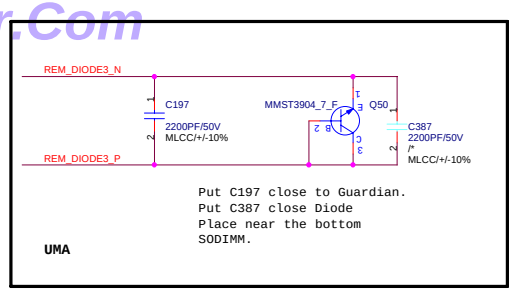
No.13 No.35

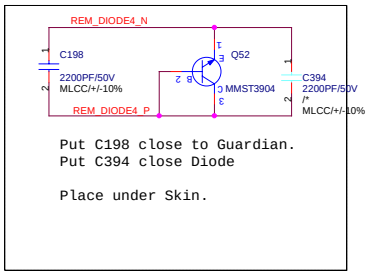
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 42 OF 68	SWITCH & LED	RELEASE DATE :		C

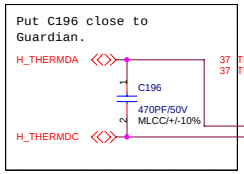
Guardian

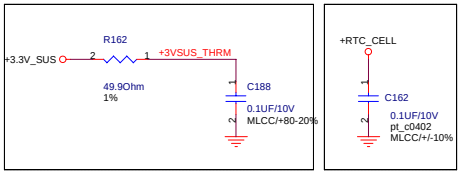


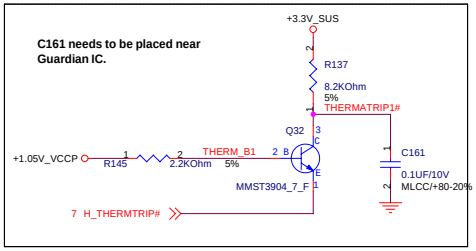


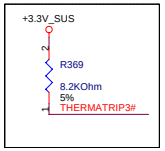


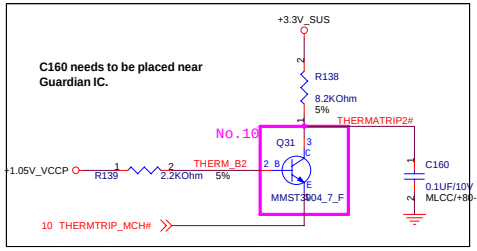


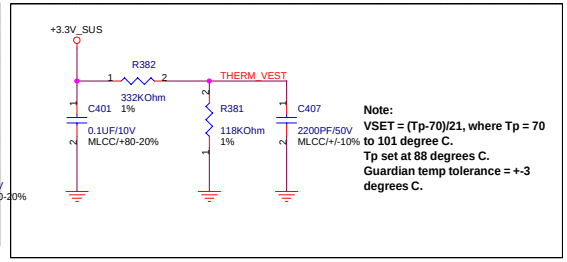


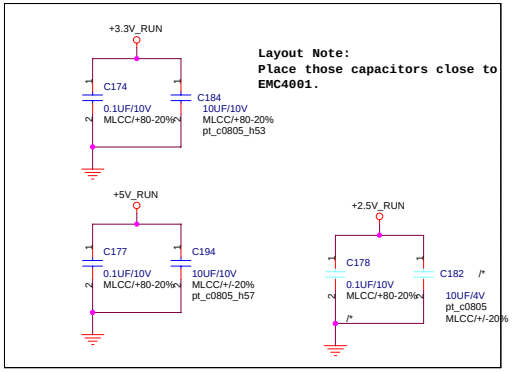


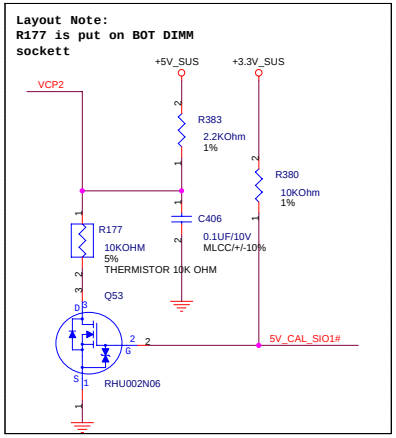


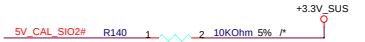


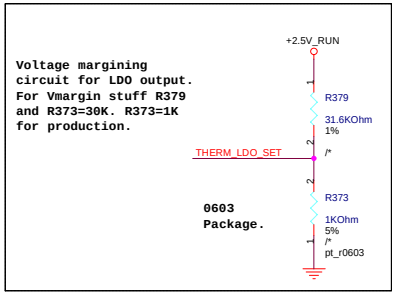


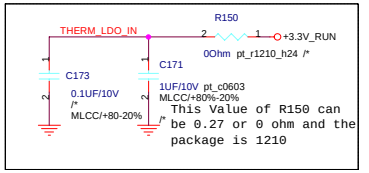






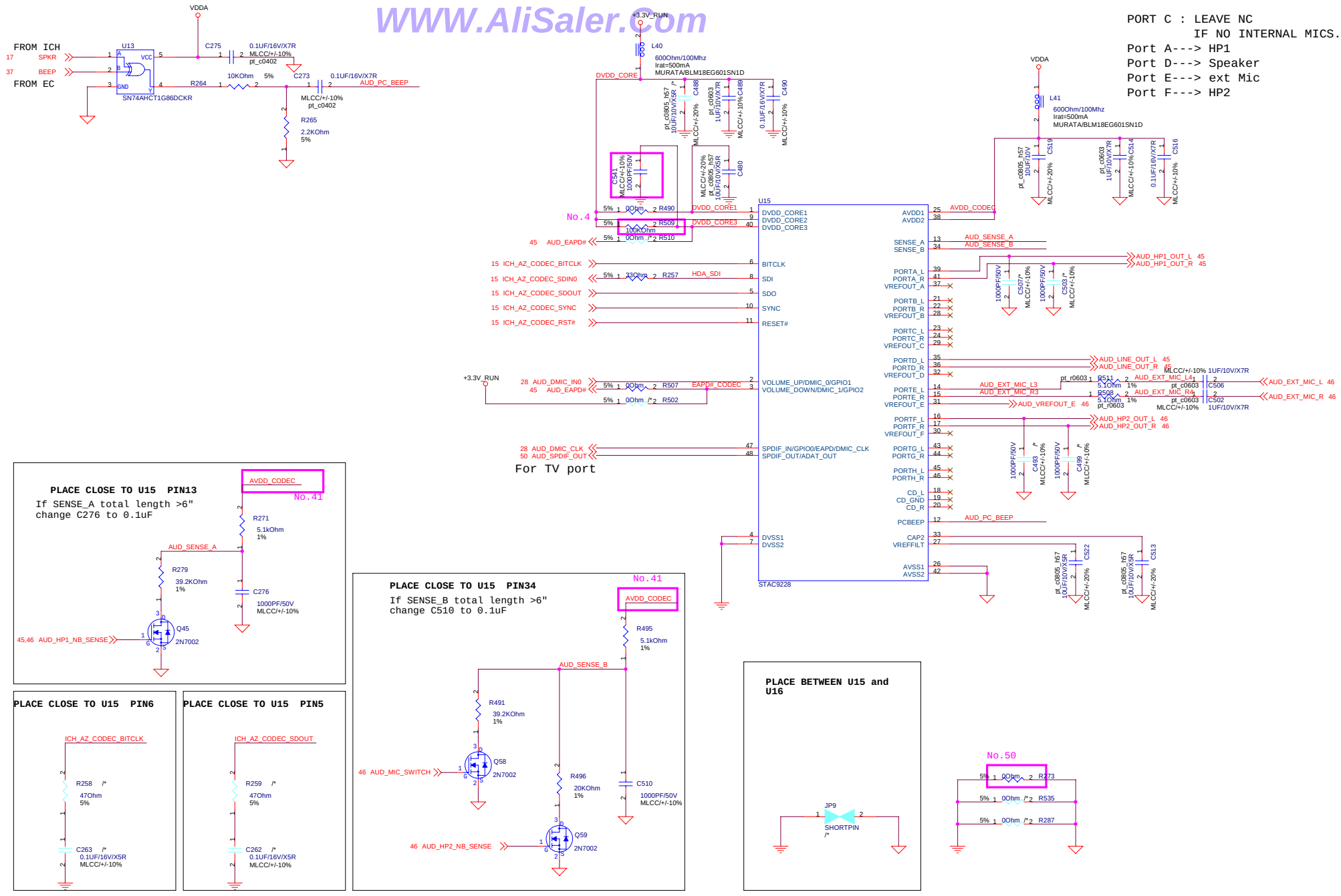




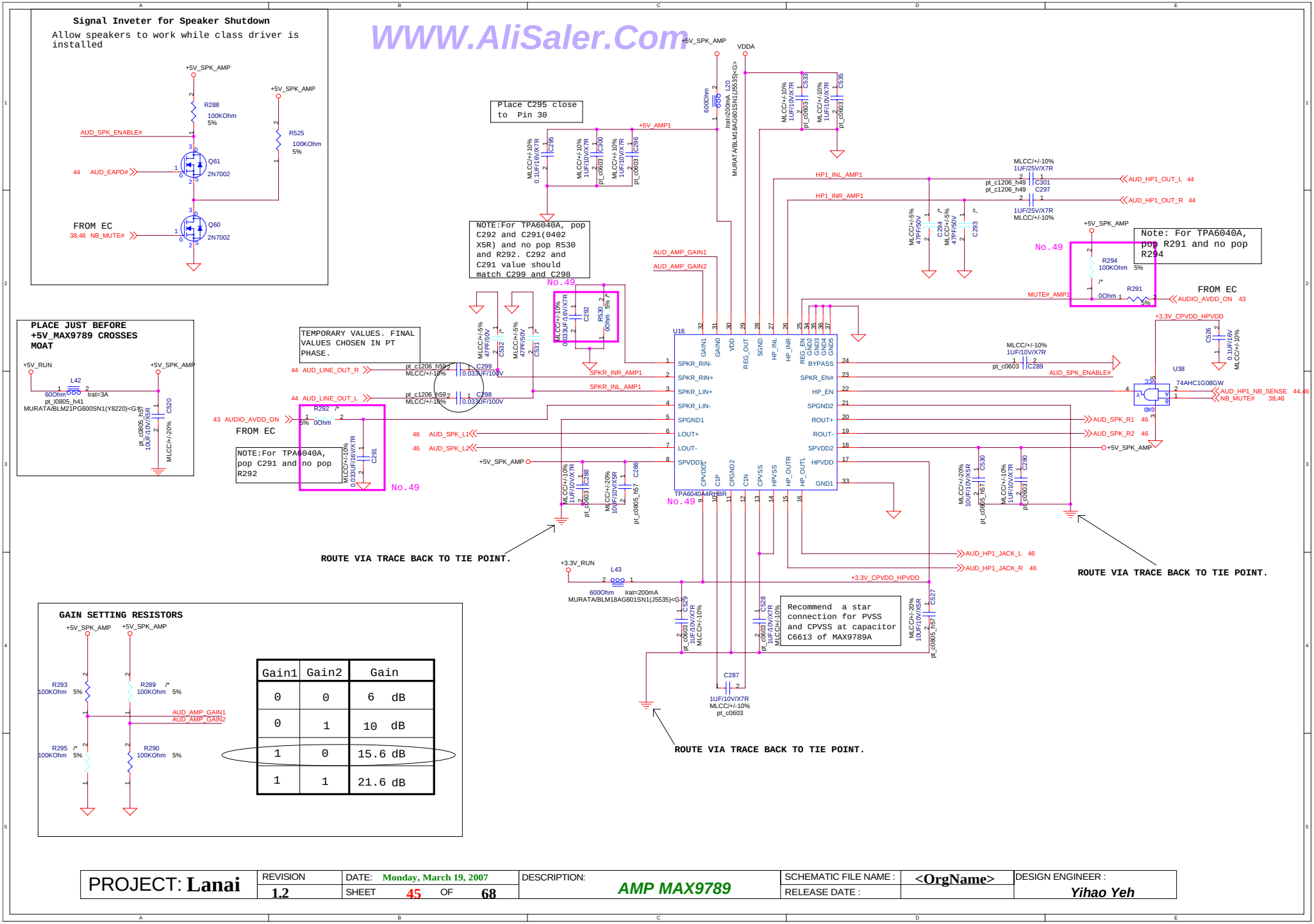


PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: EMC4001	SCHEMATIC FILE NAME :	DESIGN ENGINEER : N
		SHEET 43 OF 68		RELEASE DATE :	

PORT C : LEAVE NC
IF NO INTERNAL MICS.
Port A---> HP1
Port D---> Speaker
Port E---> ext Mic
Port F---> HP2



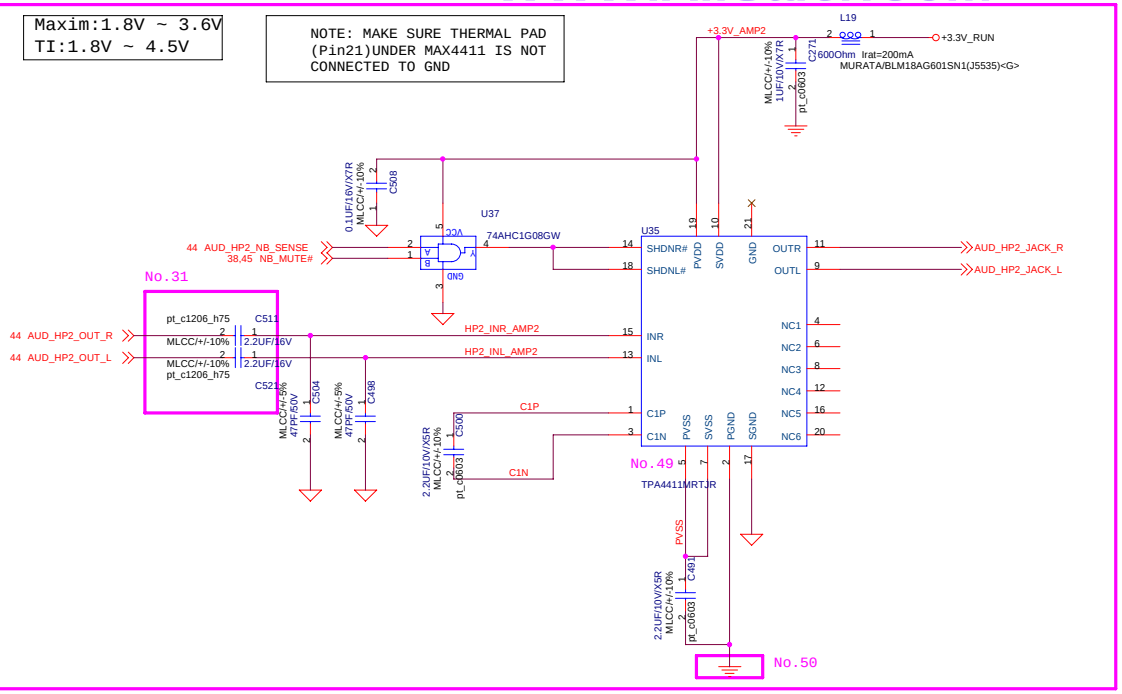
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***STAC9228***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Yihao Yeh***
		SHEET **44** OF **68**		RELEASE DATE :	



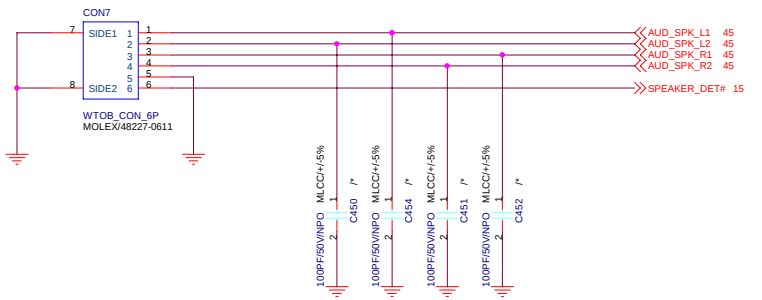
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***AMP MAX9789***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : ***Yihao Yeh***
		SHEET 45 OF 68		RELEASE DATE :		

Maxim:1.8V ~ 3.6V
TI:1.8V ~ 4.5V

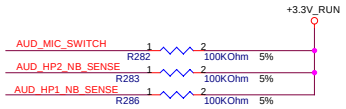
NOTE: MAKE SURE THERMAL PAD (Pin21)UNDER MAX4411 IS NOT CONNECTED TO GND

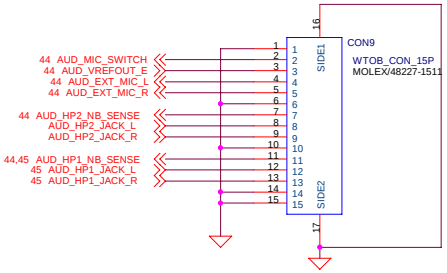


Speaker CON

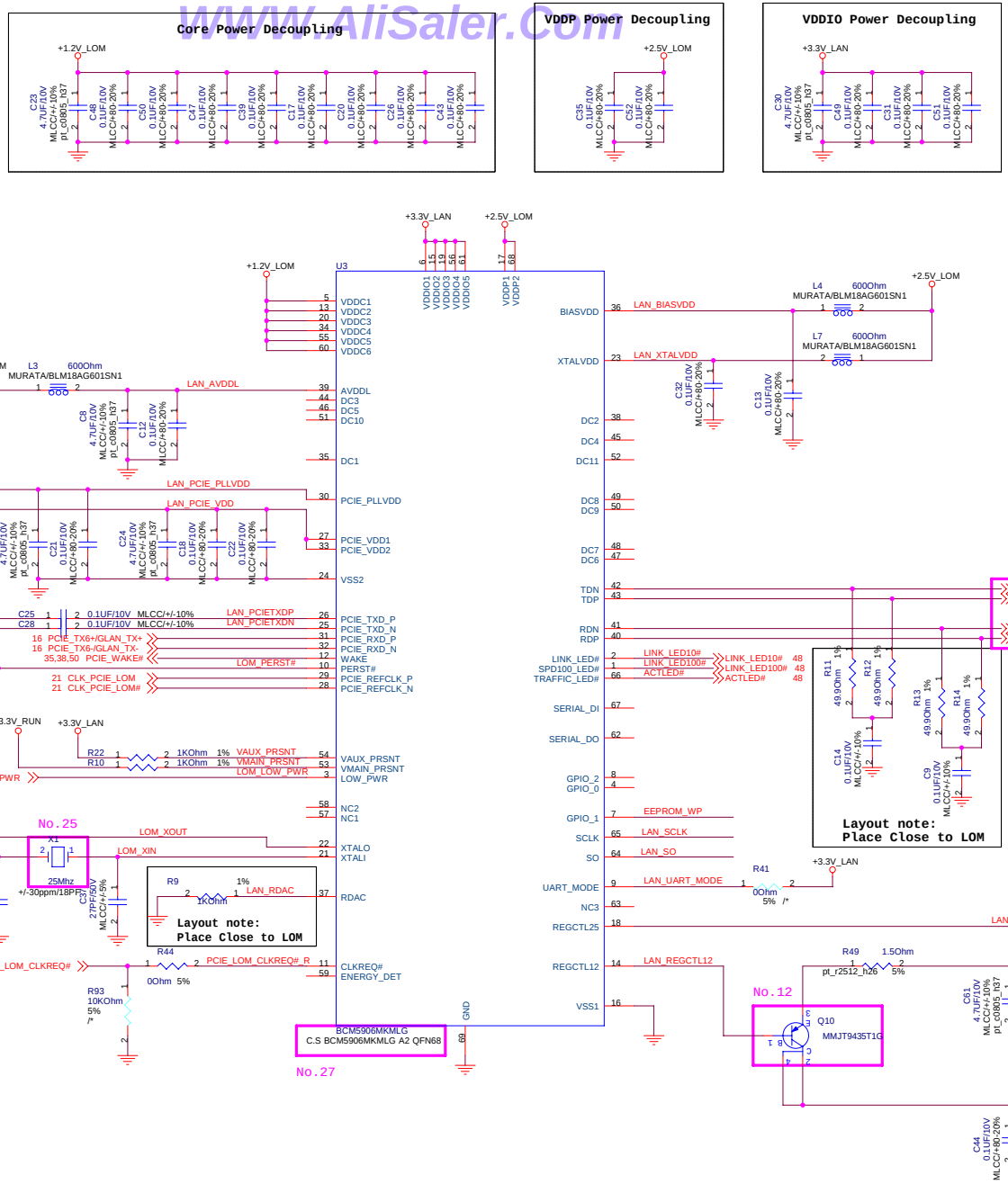


Need to adjust EMI cap values as necessary.

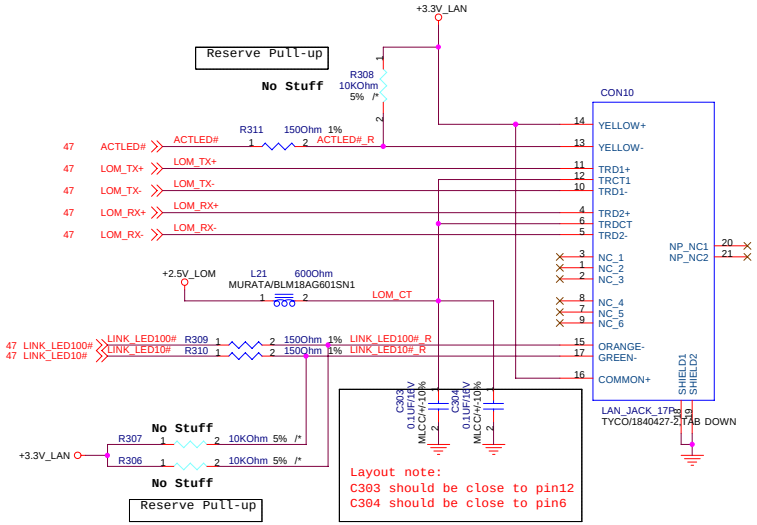




PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 46 OF 68	*AMP MAX4411 & AUDIO JACK*	RELEASE DATE :	*Yihao Yeh*

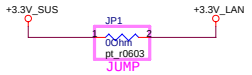


PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 47 OF 68	*LAN BCM5906MKMLG(QFN-68)*	RELEASE DATE :		*Ivan_Chou*

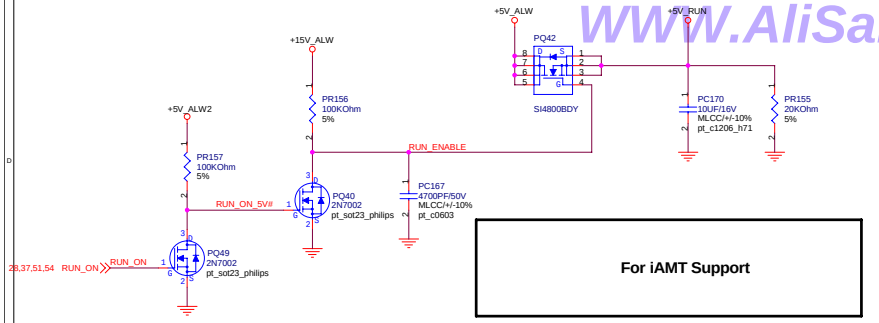


+3.3V_LAN Source Guideline:

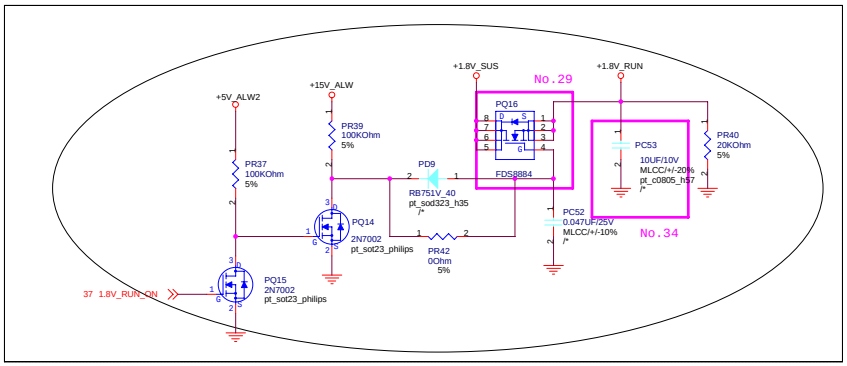
1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on_LAN is required out of S4, S5

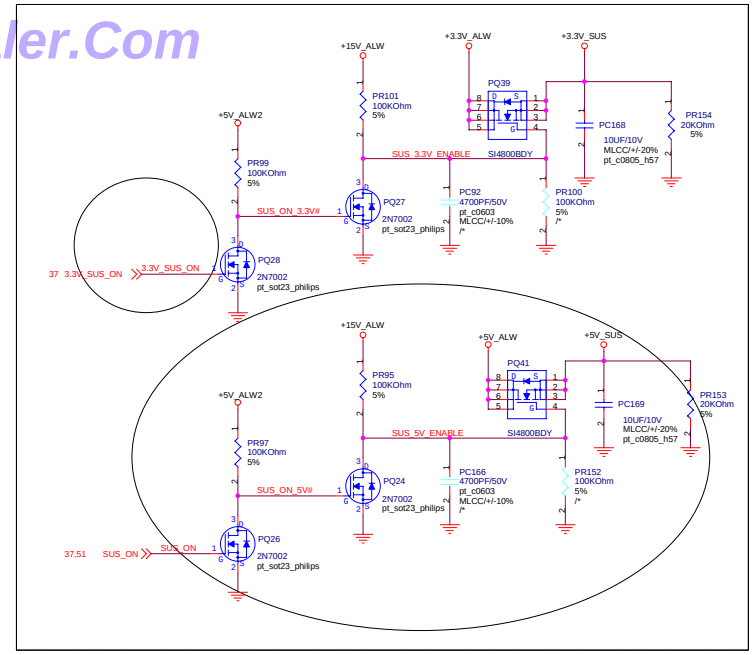


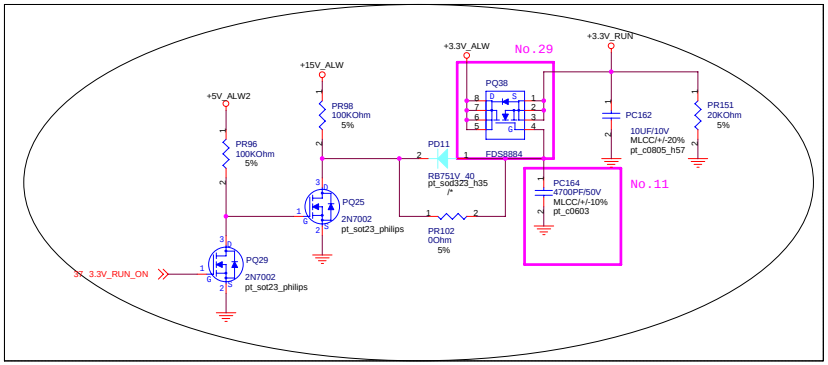
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 48 OF 68	*Magnetics and RJ-45*	RELEASE DATE :		*Ivan_Chou*

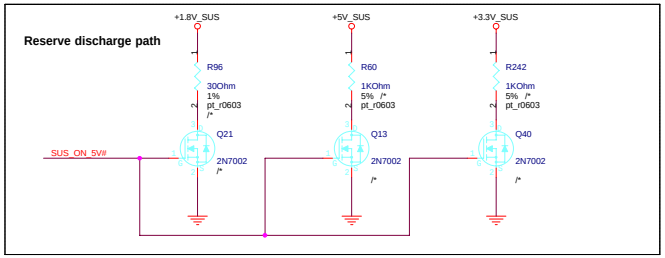


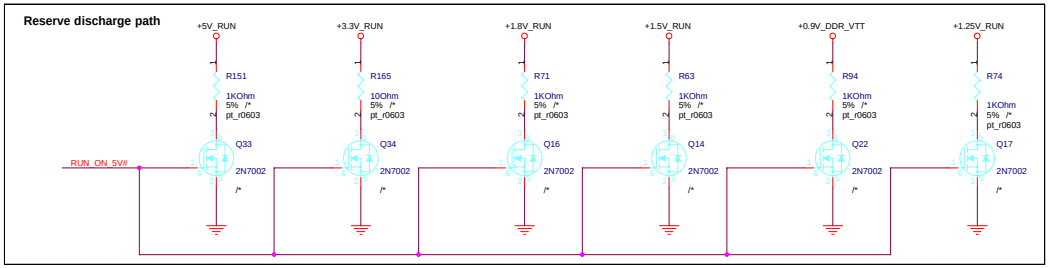
For iAMT Support







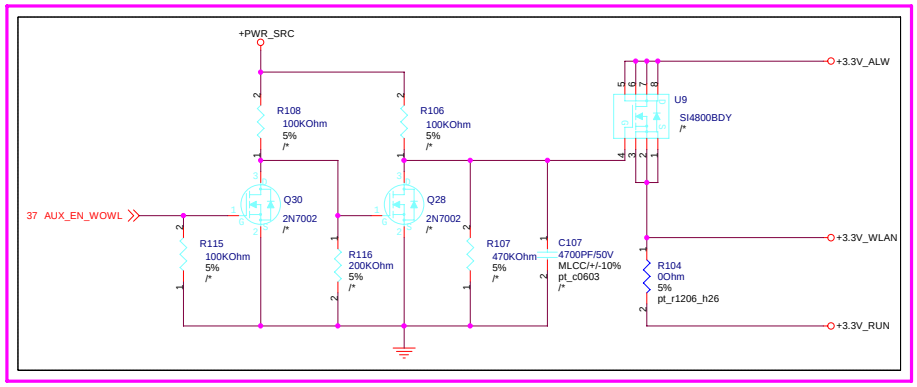


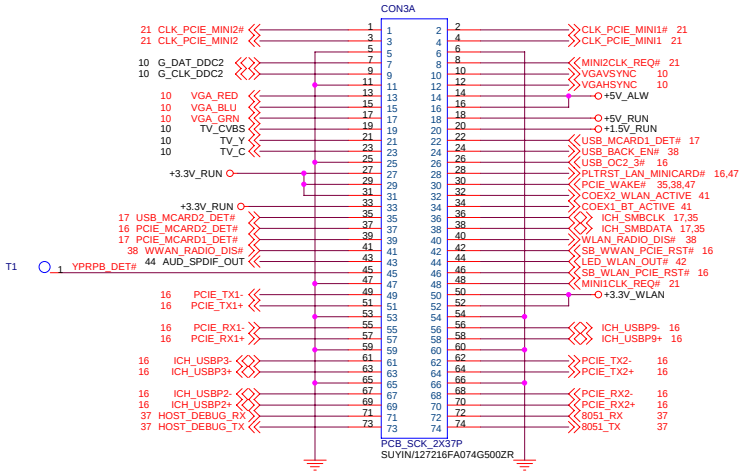


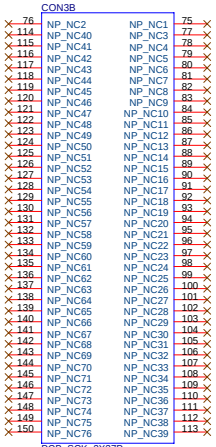
For iAMT Support

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Power Control Switch*	SCHEMATIC FILE NAME :	DESIGN ENGINEER : *Eric Ko*
		SHEET 49 OF 68		RELEASE DATE :	

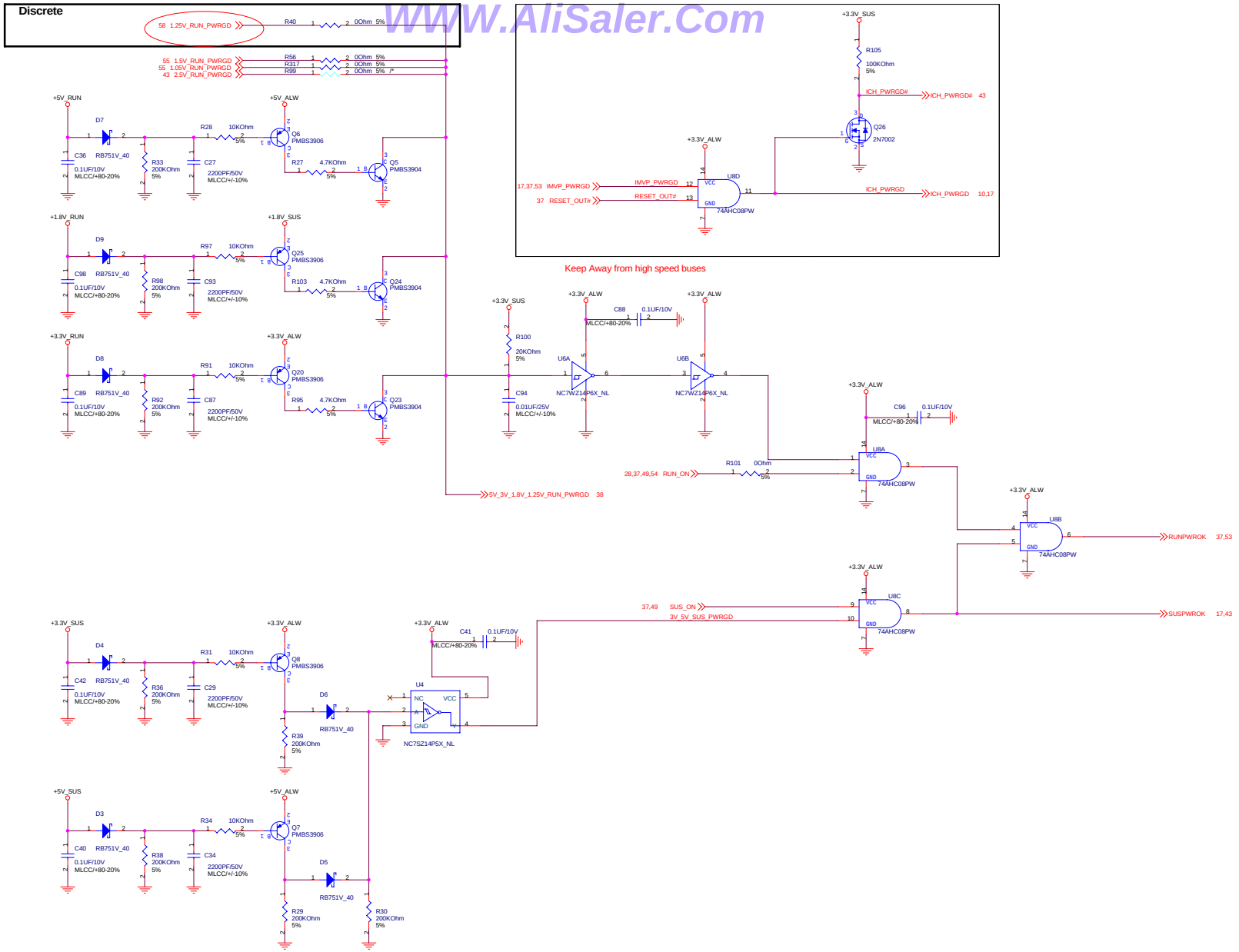
No.21





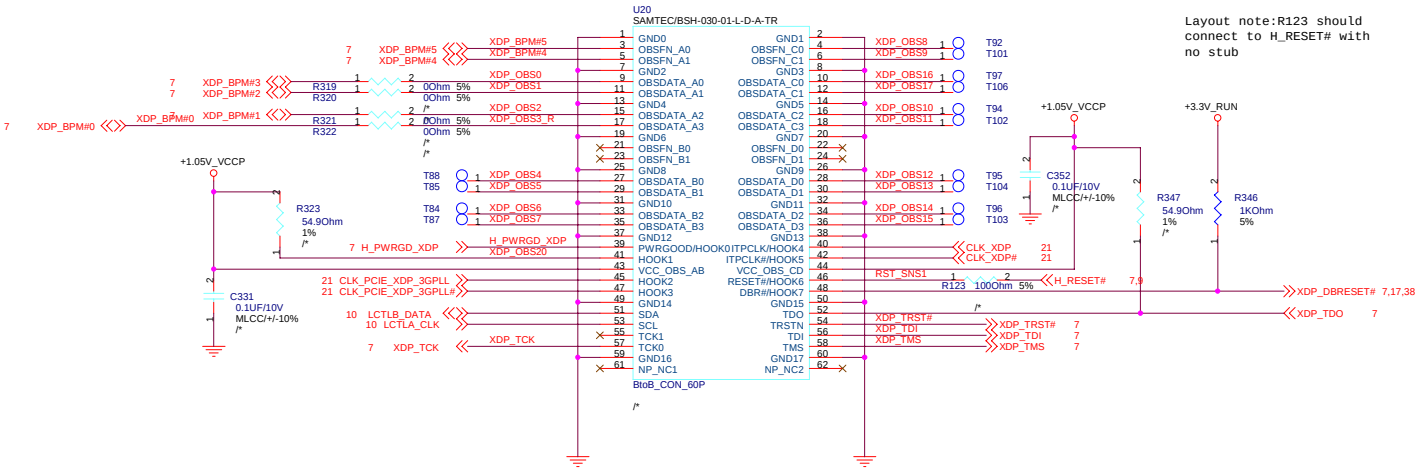


PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***BtoB CON***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***STANLY_HSU***
		SHEET **50** OF **68**		RELEASE DATE :	



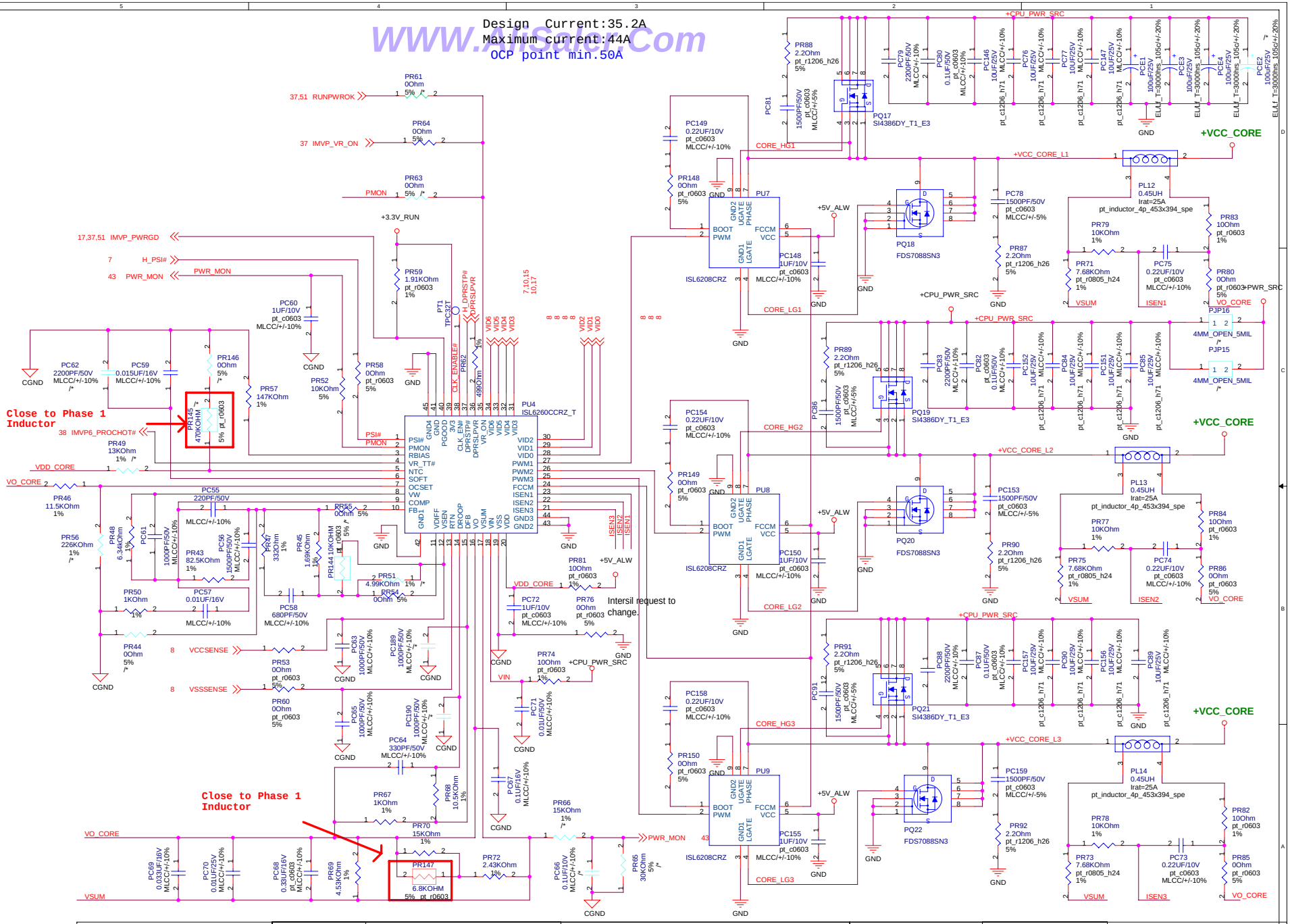
PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Power Sequence Logic*	SCHEMATIC FILE NAME :		DESIGN ENGINEER : *C.L. Ho*
		SHEET 51 OF 68		RELEASE DATE :		

XDP



PROJECT: **Lanai**	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 52 OF 68	*XDP*	RELEASE DATE :		*Terry_Lin*

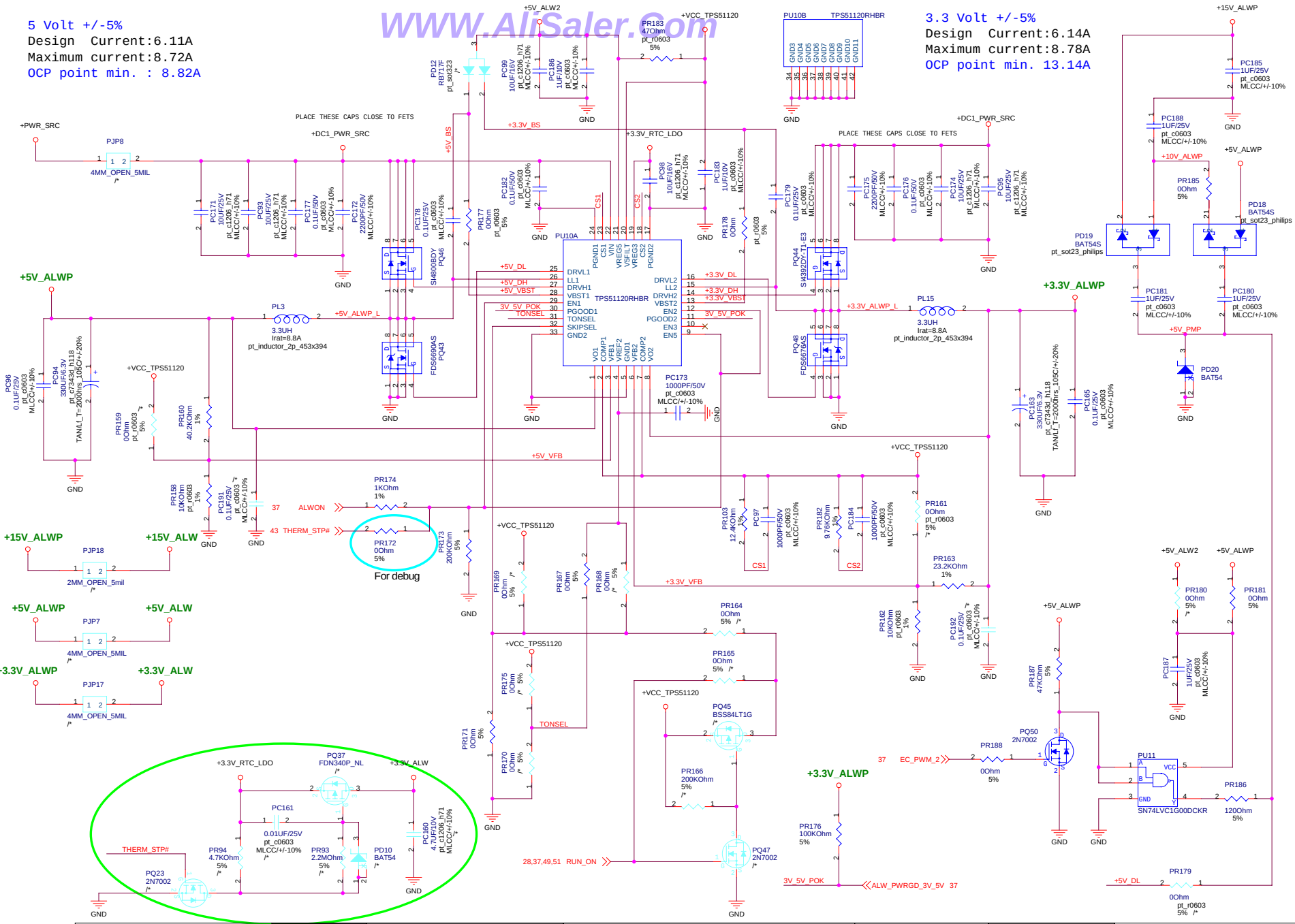
Design Current:35.2A
Maximum current:44A
OCP point min.50A



PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ***POWER_VCORE***	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: ***JEFF***
		SHEET 53 OF 68		RELEASE DATE:	

5 Volt +/-5%
Design Current:6.11A
Maximum current:8.72A
OCP point min. : 8.82A

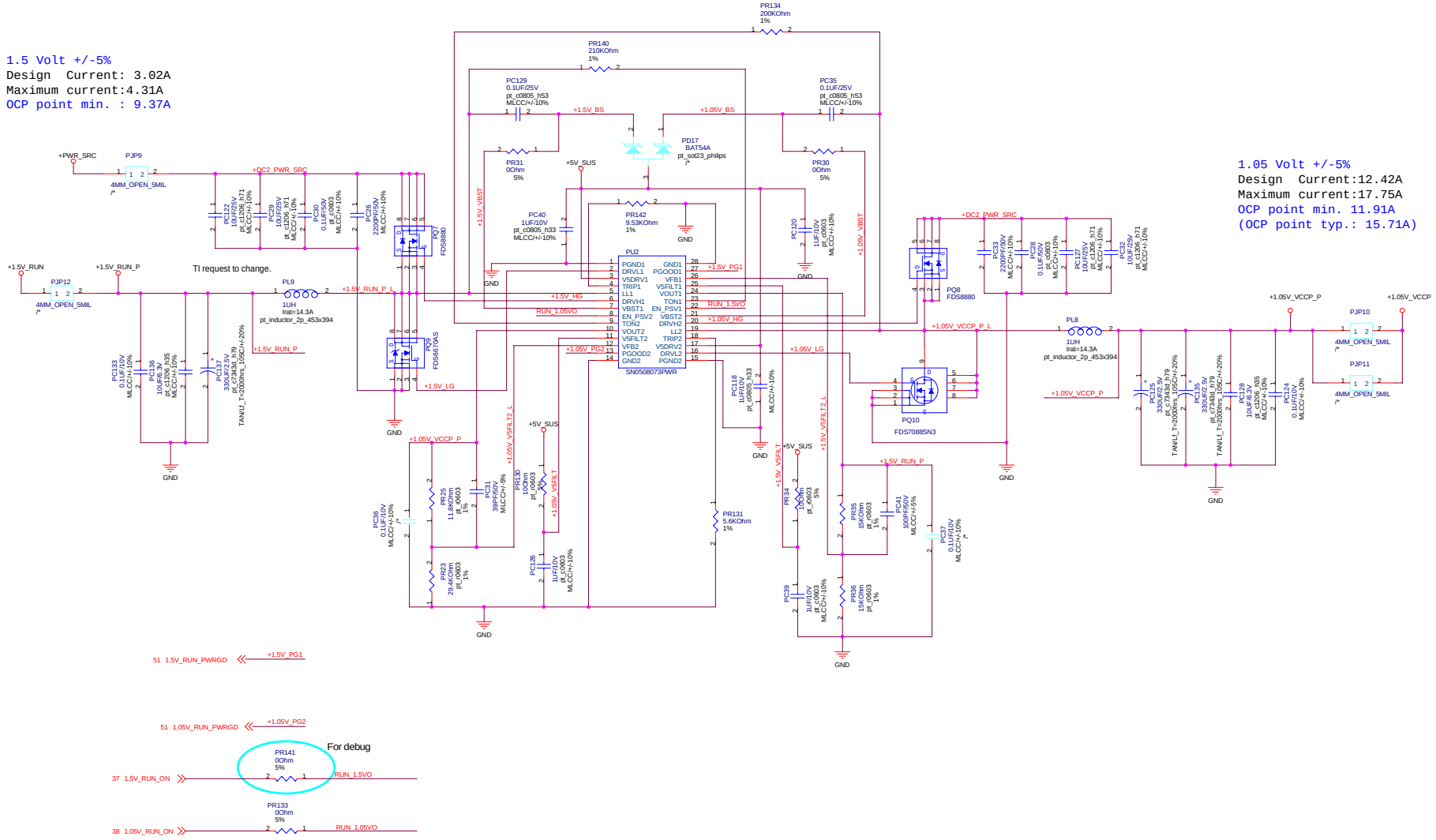
3.3 Volt +/-5%
Design Current:6.14A
Maximum current:8.78A
OCP point min. 13.14A



PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *POWER_SYSTEM 5V_ALW&3.3V_ALW*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : *JEFF*
		SHEET 54 OF 68		RELEASE DATE :	

1.5 Volt +/-5%
Design Current: 3.02A
Maximum current:4.31A
OCP point min. : 9.37A

1.05 Volt +/-5%
Design Current:12.42A
Maximum current:17.75A
OCP point min. 11.91A
(OCP point typ.: 15.71A)



PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 55 OF 68	DESCRIPTION: POWER I/O 1.5VS & 1.05VS	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER : JEFF

WWW.AliSaler.Com

TOTAL POWER=65W
-->3.34A

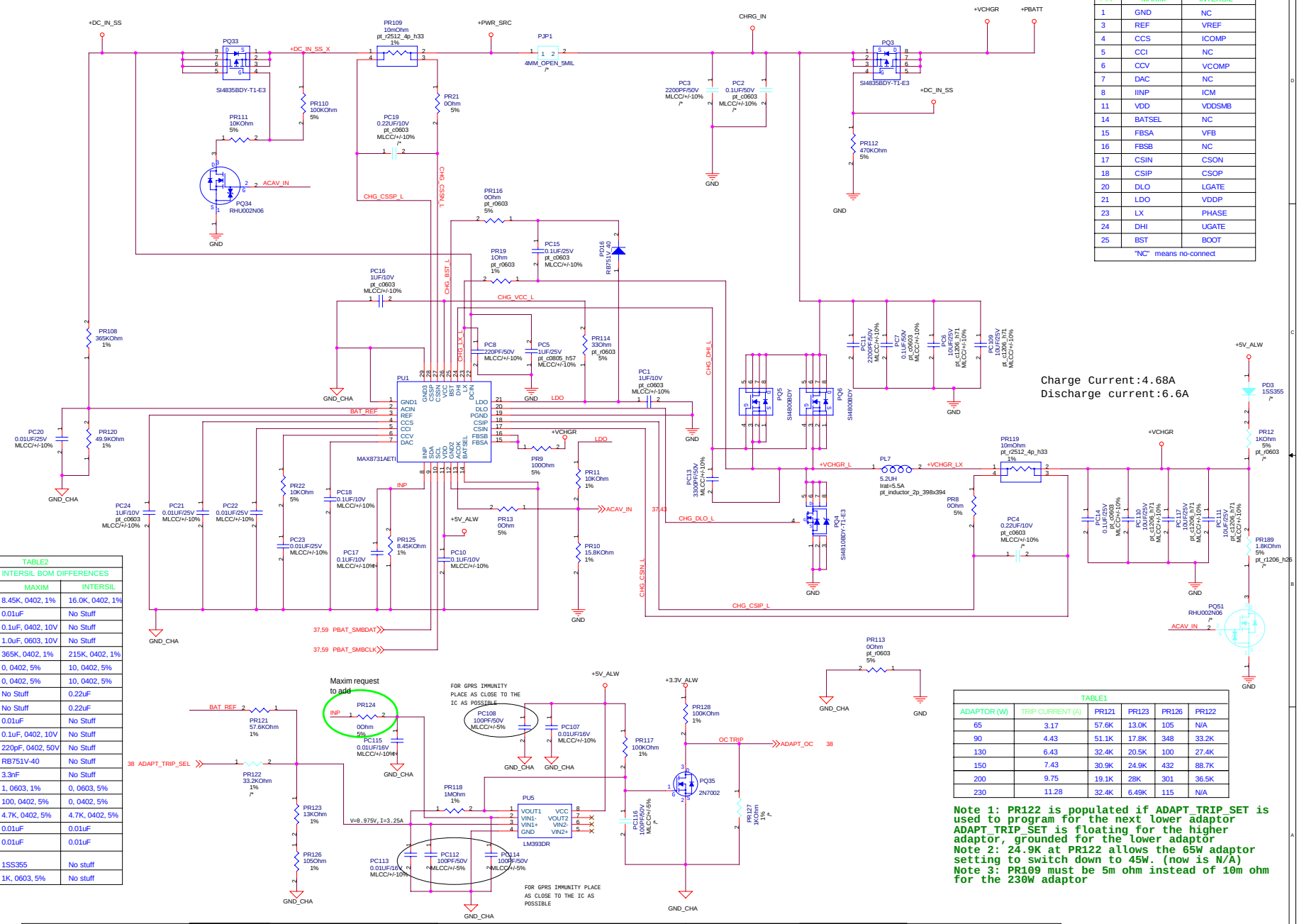


TABLE3		
PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		

TABLE2		
MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR125	8.45K, 0402, 1%	16.0K, 0402, 1%
PC115	0.01uF	No Stuff
PC17	0.1uF, 0402, 10V	No Stuff
PC24	1.0uF, 0603, 10V	No Stuff
PR108	365K, 0402, 1%	215K, 0402, 1%
PR8	0, 0402, 5%	10, 0402, 5%
PR21	0, 0402, 5%	10, 0402, 5%
PC4	No Stuff	0.22uF
PC19	No Stuff	0.22uF
PC22	0.01uF	No Stuff
PC18	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD16	RB751V-40	No Stuff
PC13	3.3nF	No Stuff
PR19	1, 0603, 1%	0, 0603, 5%
PR9	100, 0402, 5%	0, 0402, 5%
PR22	4.7K, 0402, 5%	4.7K, 0402, 5%
PC23	0.01uF	0.01uF
PC21	0.01uF	0.01uF
PD3	1SS355	No stuff
PR12	1K, 0603, 5%	No stuff

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR121	PR123	PR126	PR122
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

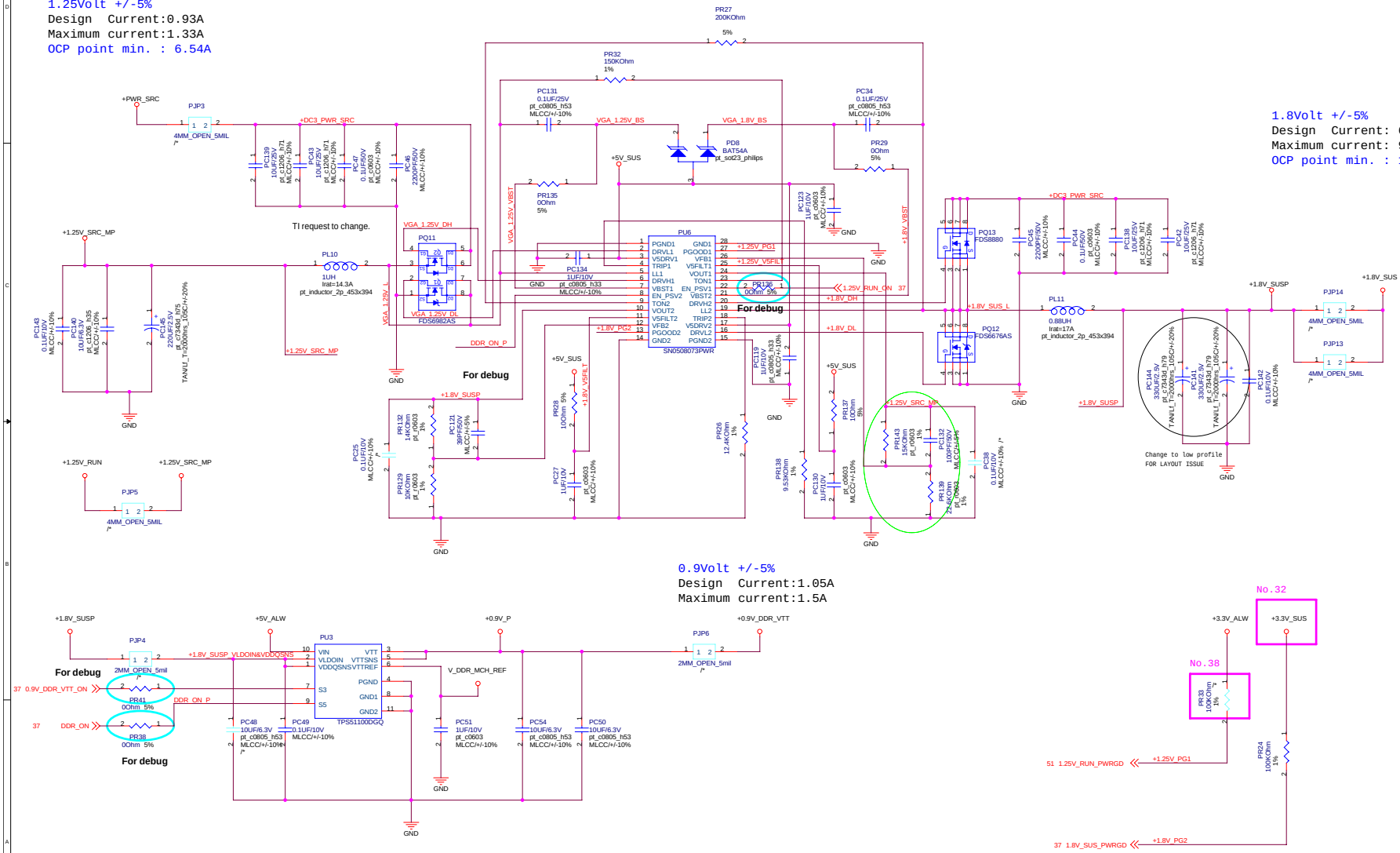
Note 1: PR122 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)
Note 3: PR109 must be 5m ohm instead of 10m ohm for the 230W adaptor

PROJECT: Lanai	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: POWER_CHARGER	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: JEFF
		SHEET 57 OF 68		RELEASE DATE:	

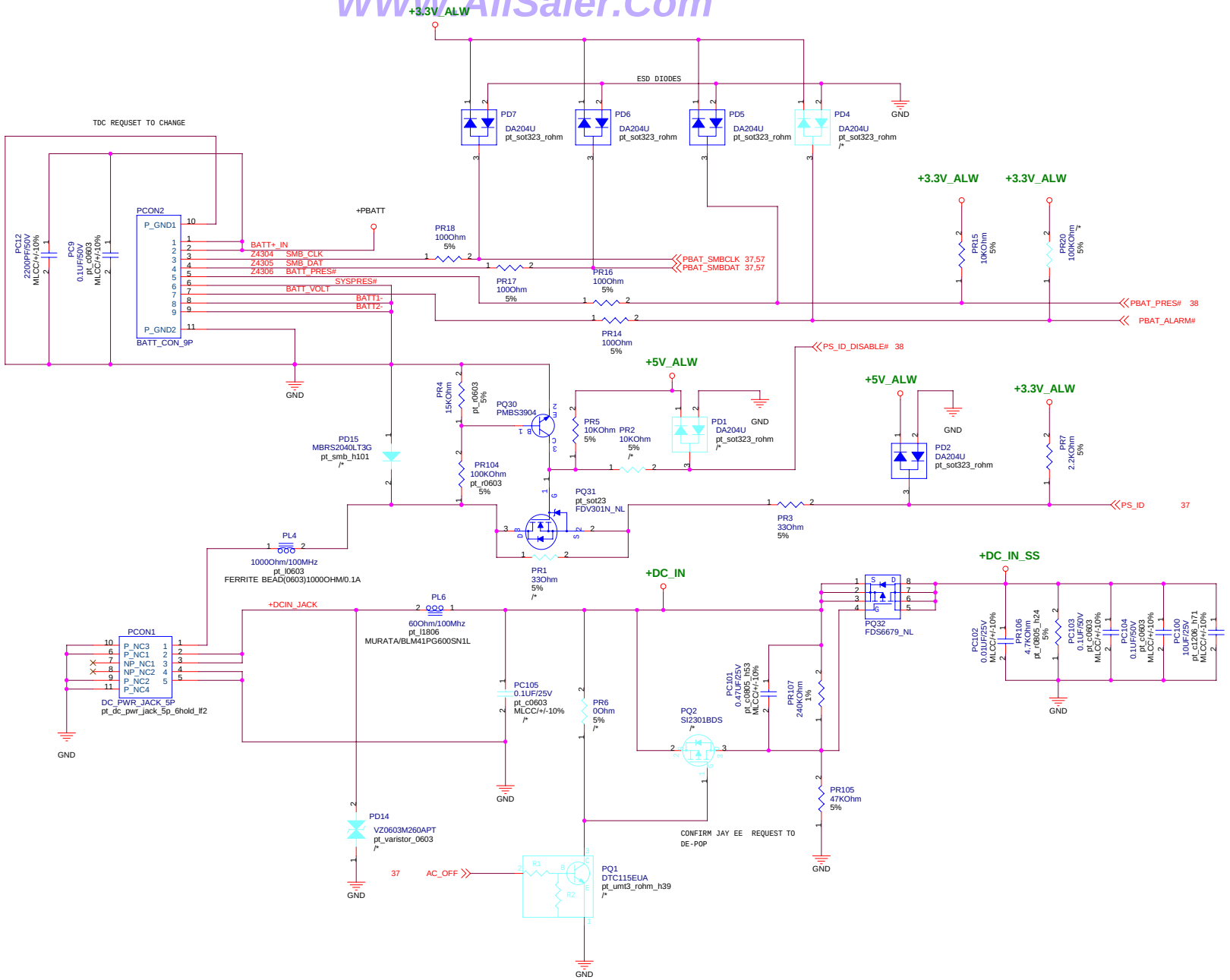
1.25Volt +/-5%
Design Current:0.93A
Maximum current:1.33A
OCP point min. : 6.54A

1.8Volt +/-5%
Design Current: 6.59A
Maximum current: 9.42A
OCP point min. : 16.93A

0.9Volt +/-5%
Design Current:1.05A
Maximum current:1.5A

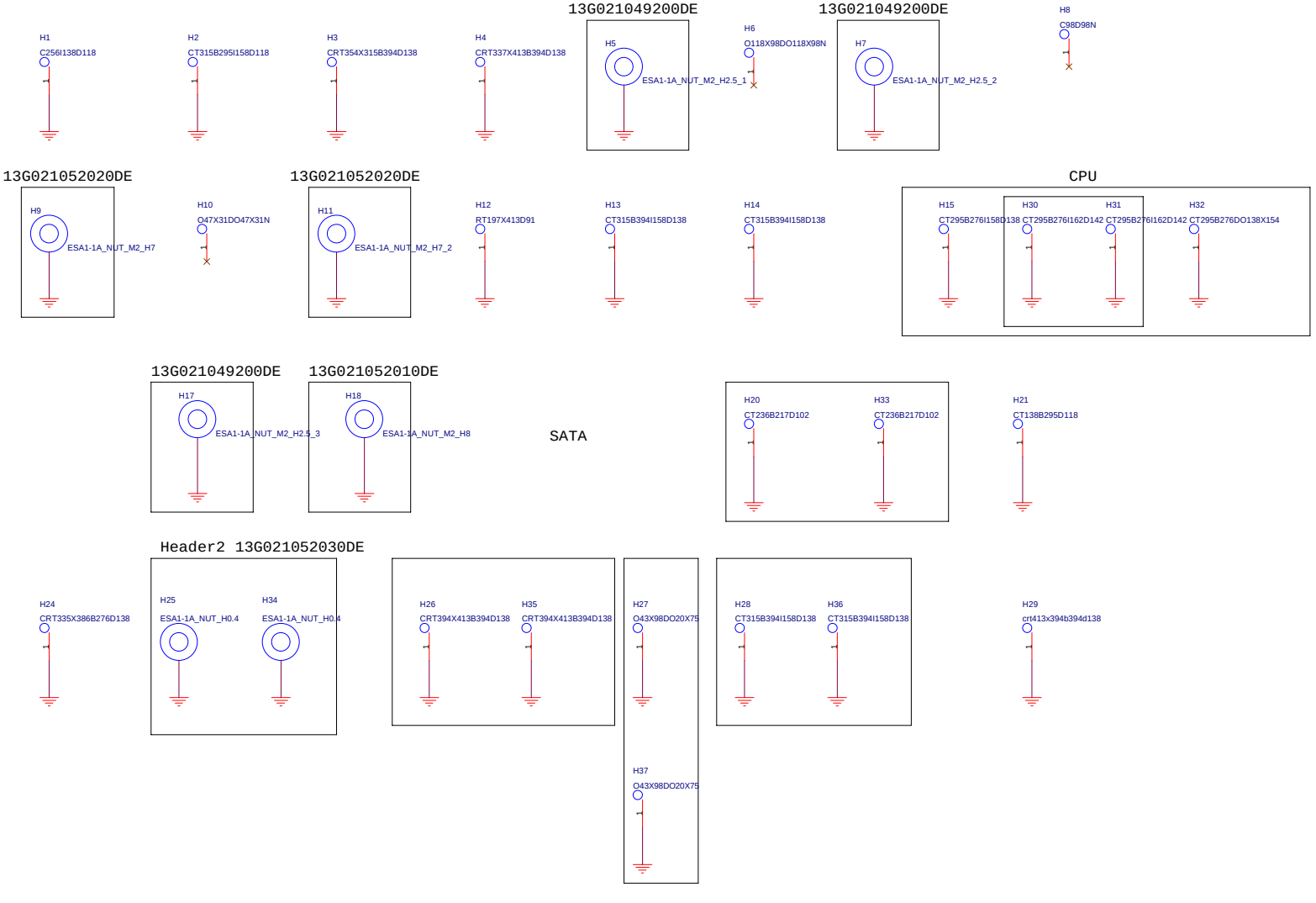


PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 58 OF 68	POWER VGA 1.25V & DDR & VTT	RELEASE DATE :		Jeff



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***POWER_CONNECTOR***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***JEFF***
		SHEET **59** OF **68**		RELEASE DATE :	

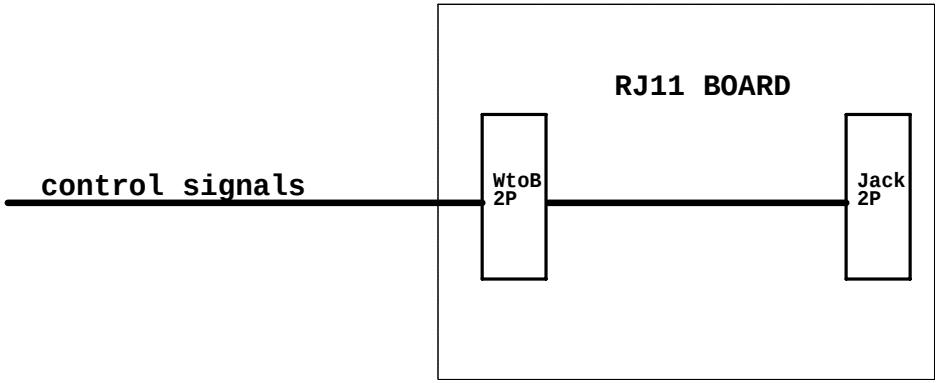
GM screw pad



PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***SCREW PAD***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **60** OF **68**		RELEASE DATE :	

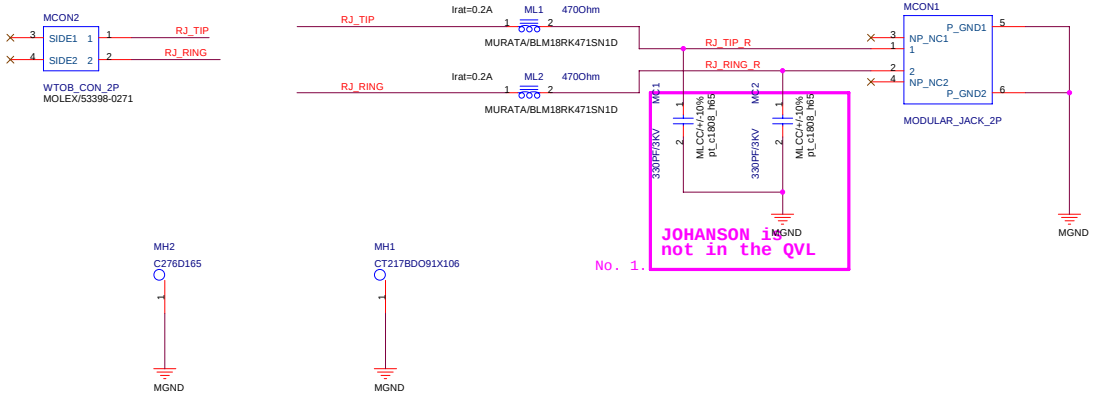
MODEL NAME : *Elsa*

Lanai:Modem Board



REV : 1.1(DELL: X01)

PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***BLOCK DIAGRAM***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Stanly_Hsu***
		SHEET **64** OF **68**		RELEASE DATE :	



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***RJ-11 CONN***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Stanly_Hsu***
		SHEET **65** OF **68**		RELEASE DATE :		

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai PP2 USB Board

REV : 1.1(DELL: X01)

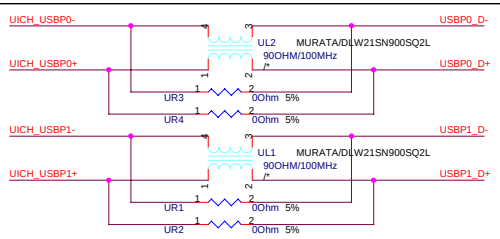
MB PCB

Part Number	Description
DA80004H0L	PCB 00B LA-3071P REV0 M/B

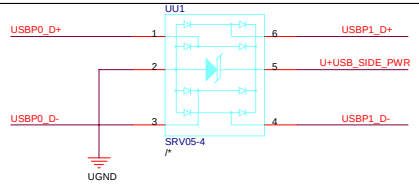
BOM NO. ???
PCB P/N: ???

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **67** OF **68**	DESCRIPTION: ***Cover Page***	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : ***Terry_Lin***

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

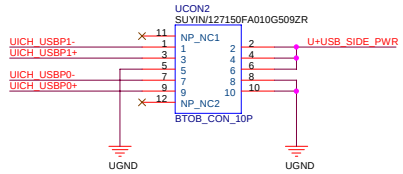


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

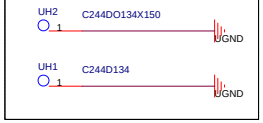


Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

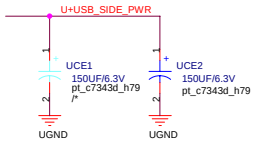
USB daughter board connector



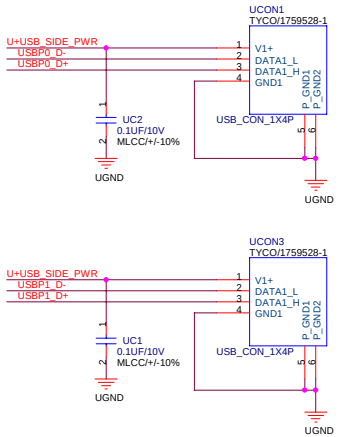
Screw hole



Place one 150uF cap by each USB connector



Each channel is 1A



Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *USB PORT (SINGLE * 2)*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : *Terry_Lin*
		SHEET 68 OF 68		RELEASE DATE :	