

Thurman UMA Schematics Document

uFCPGA Mobile Merom

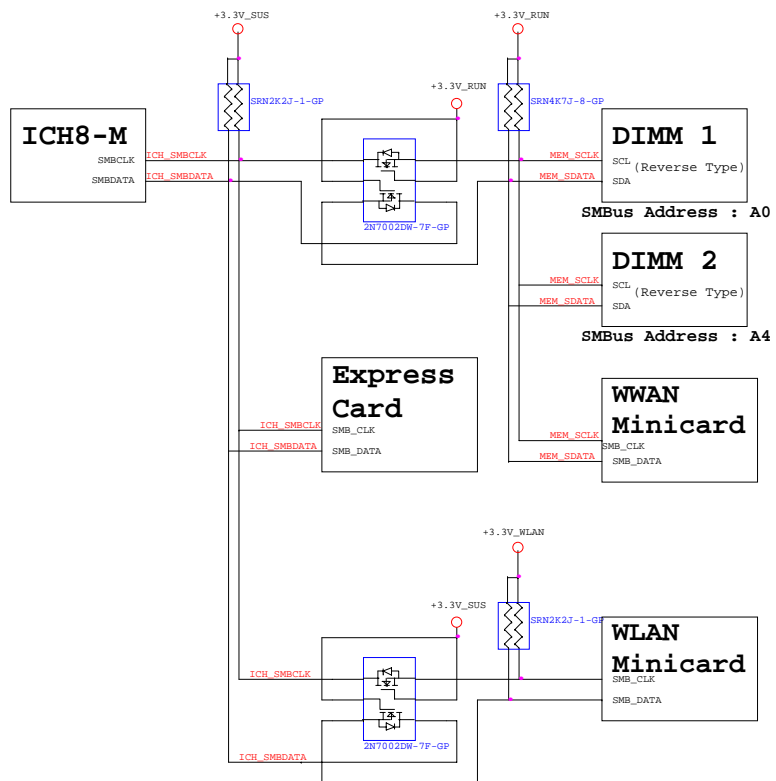
Intel Crestline-GM + ICH8M

2007-11-19

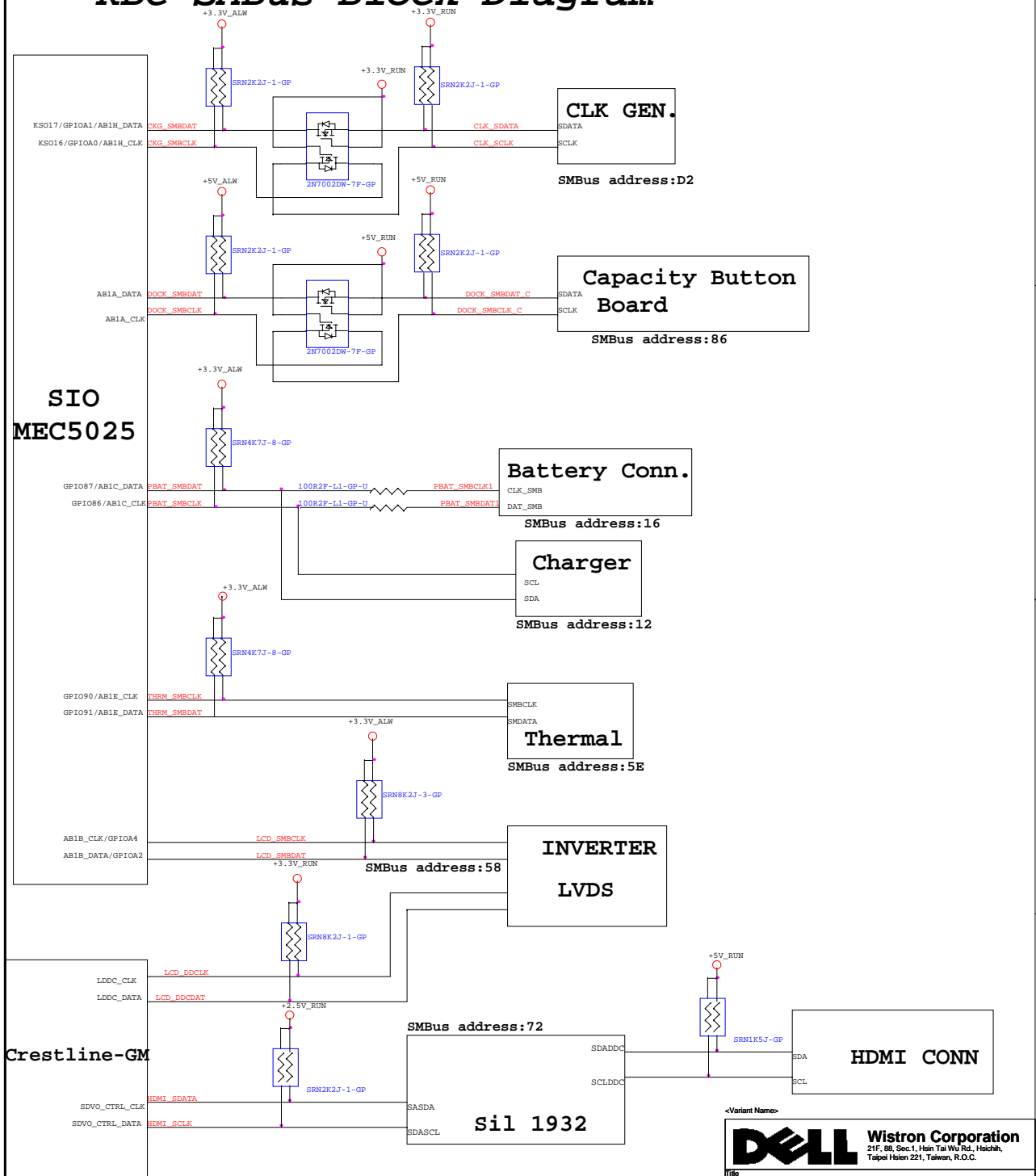
REV : -1 (DELL:A00)

<Variant Name>			
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Thurman UMA	
Size A3	Document Number	COVER PAGE	Rev -1
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ICH8 SMBus Block



KBC SMBus Block Diagram



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CLOCK GEN_CY28547

27M_SS/LCD96_100M SELECTION TABLE
 BYTE 15
 IO_VOUT[2,1,0]

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S(110)
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34	0 UMA	1 DISC.
FCTSEL1		
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL ICH8-M STRAP PIN

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16		
FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05 VccSusi_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSusi_05,VccSusi_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVD TP3	AZ DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSusi_05,VccSusi_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

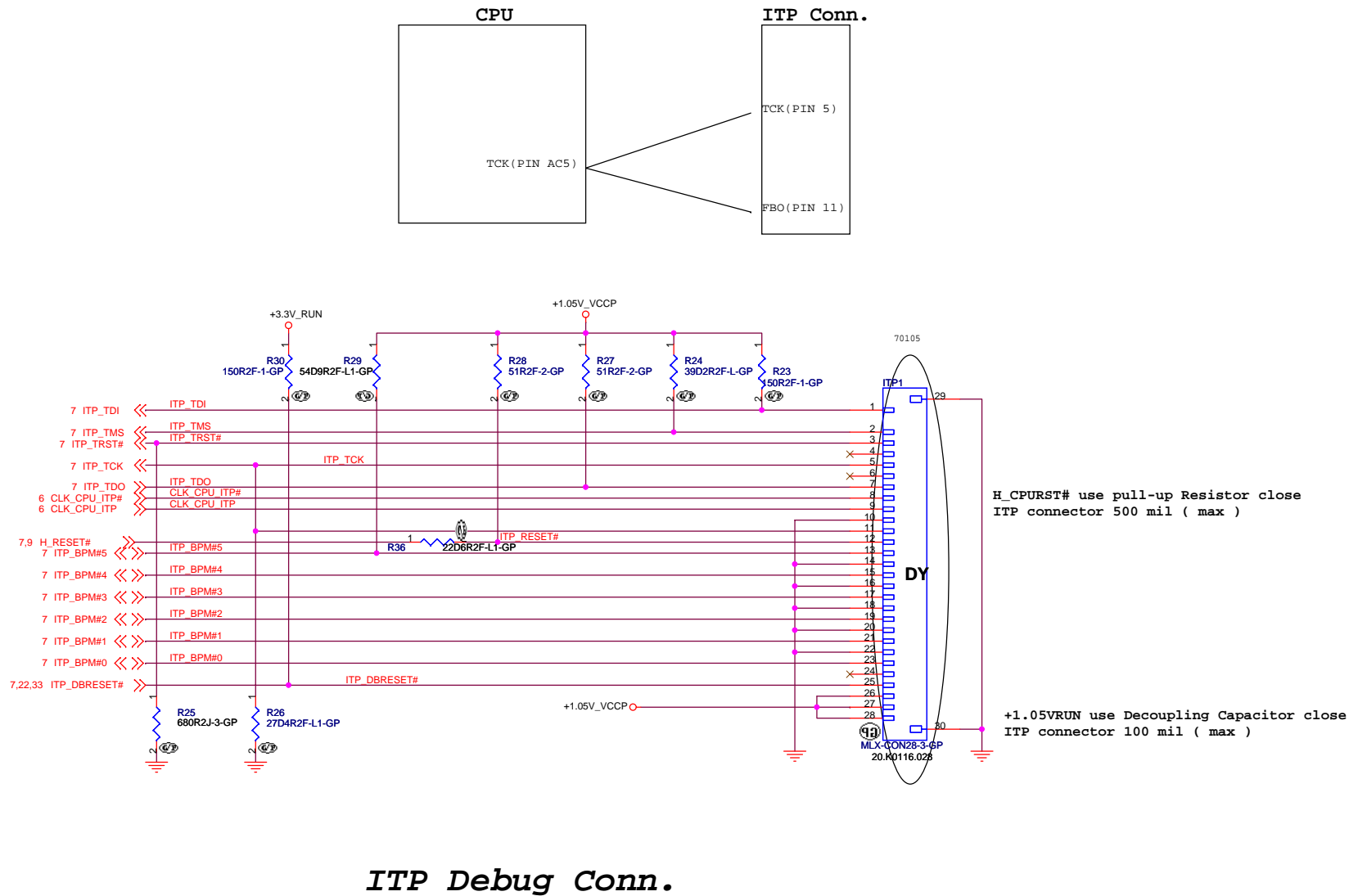
No Reboot Strap	
SPKR	LOW = Default
	High=No Reboot

8.2K PULL HIGH

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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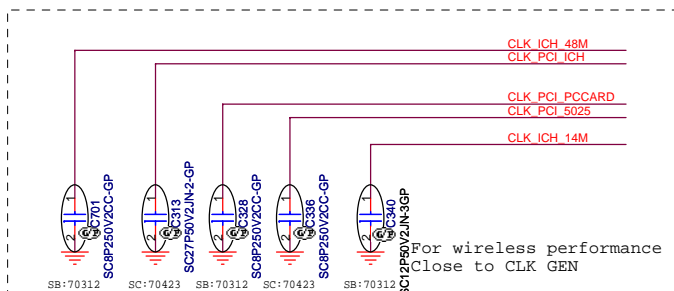
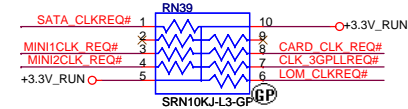
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max)

+1.05V_RUN use Decoupling Capacitor close
ITP connector 100 mil (max)

<Variant Name>

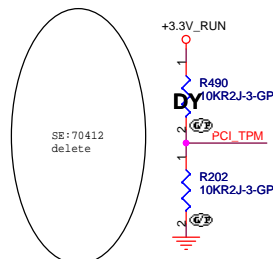
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Signal	Period	Duty Cycle	Connections	Timing
FSA (R484)	1	50%	CPU_MCH_BSEL0, CPU_MCH_BSEL1	7.10 ns
FSC (R210)	1	50%	CPU_MCH_BSEL2	7.10 ns

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M



PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PIN9	PIN39
PGMODE	DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD# (DEFAULT)

<Variant Name>

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A2

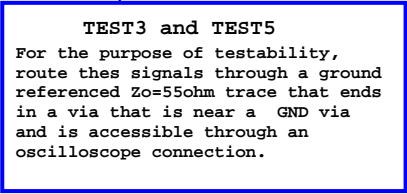
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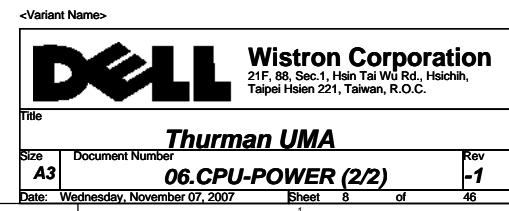
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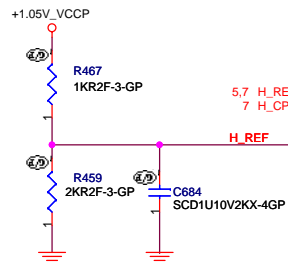
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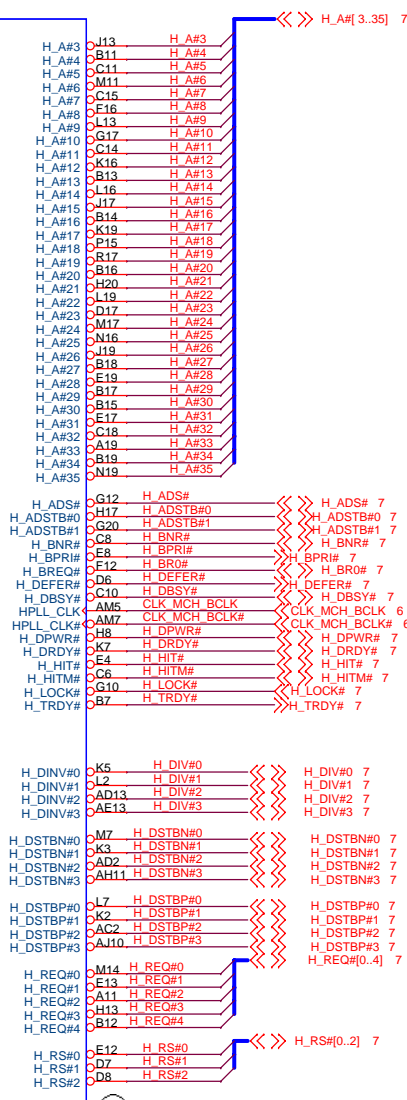
H_REF Decoupling Crestline
close Crestline 100 mil



Change to 71.CREST.M02

U56A 1 OF 10

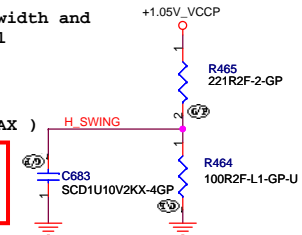
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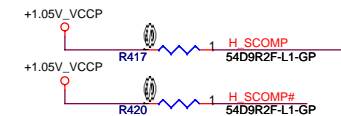
H_SWING routing Trace width and
Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close
Caliistoga 500 mil (MAX)

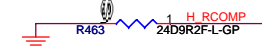
From Schematic Design
Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors
and Capacitors close Caliistoga
500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



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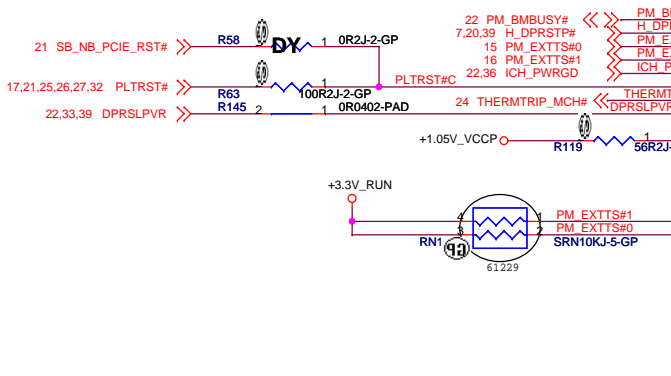
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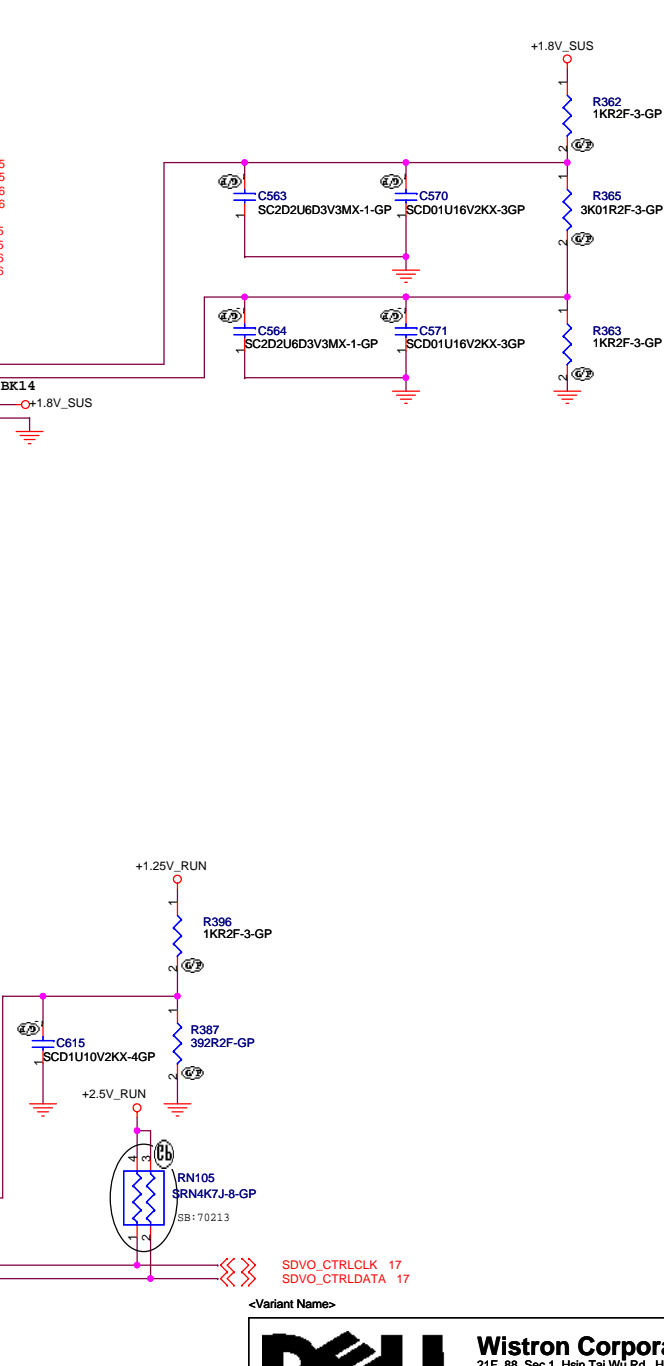
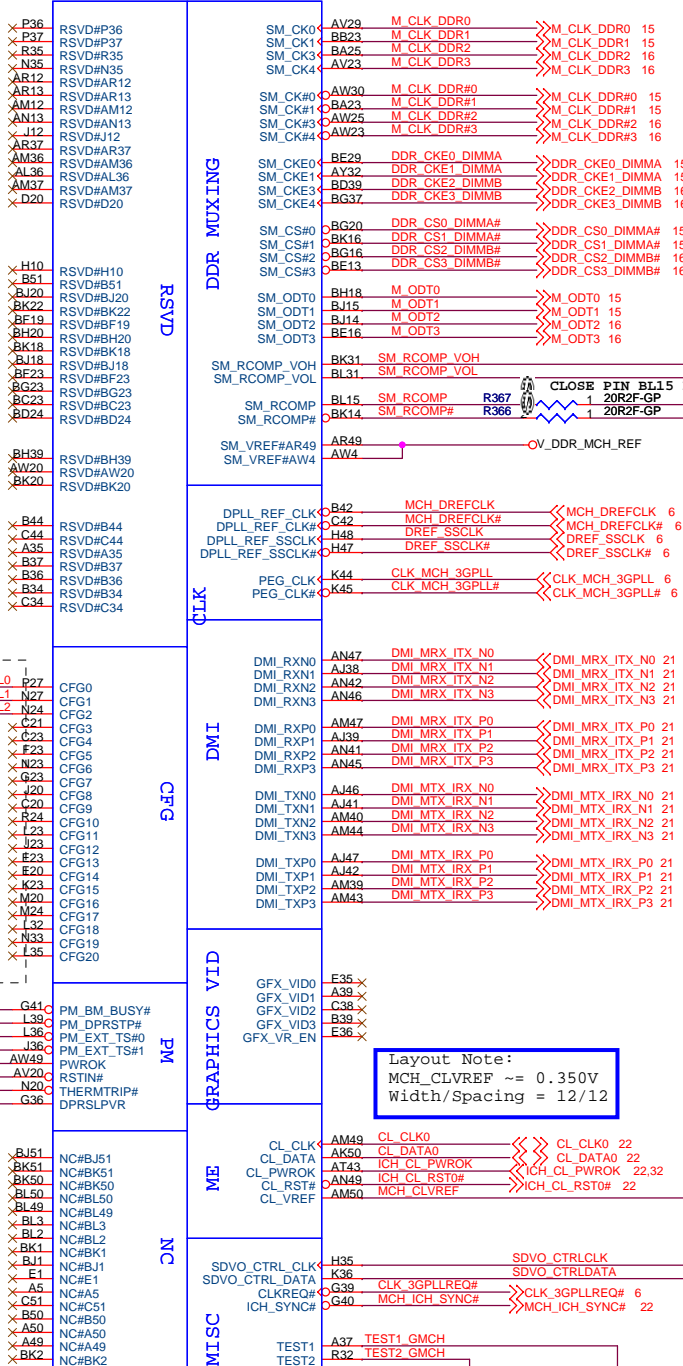
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CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16	Disabled	Enabled *
CFG 18	1.05V *	1.5V
CFG 19	Normal Operation *	Reserved Lane
CFG 20	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

CFG[13:12]	
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *
CFG[2..0] FSB Select	
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.

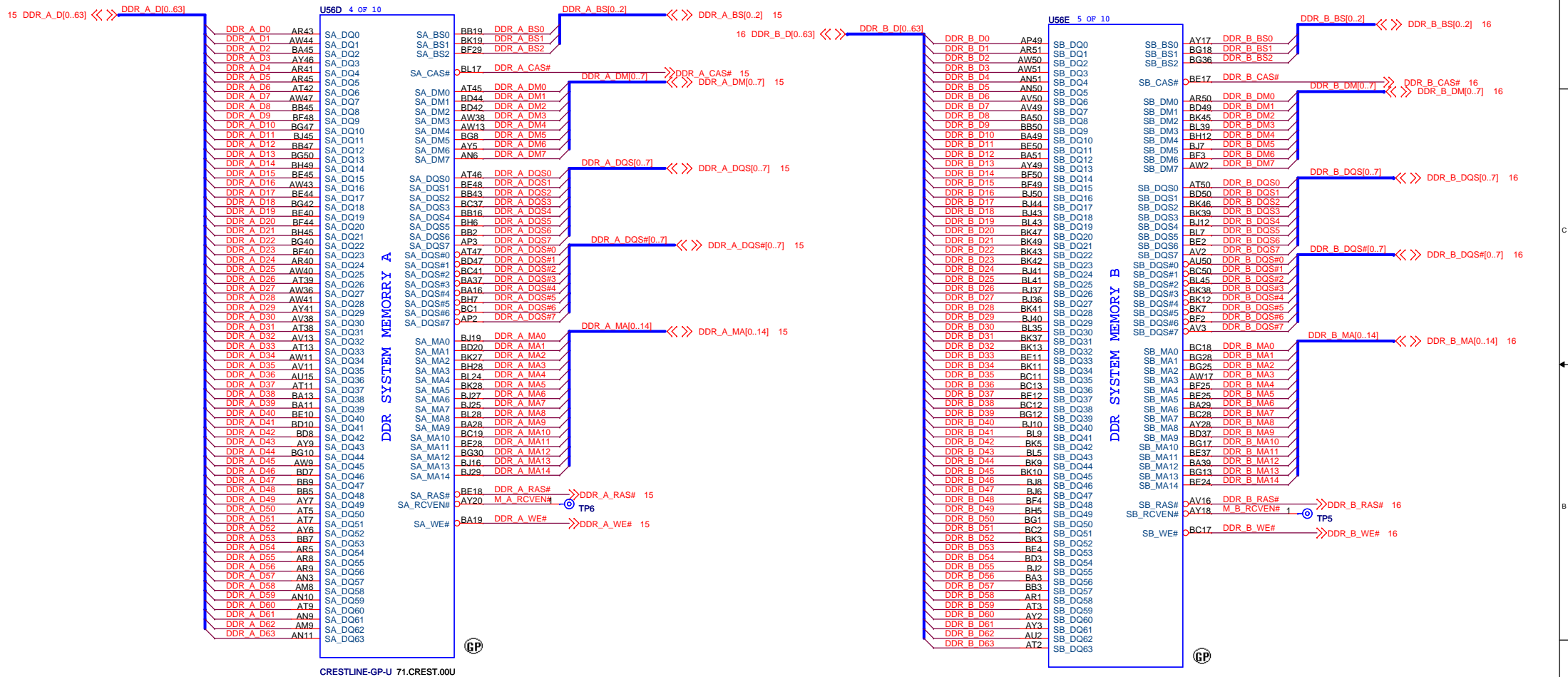


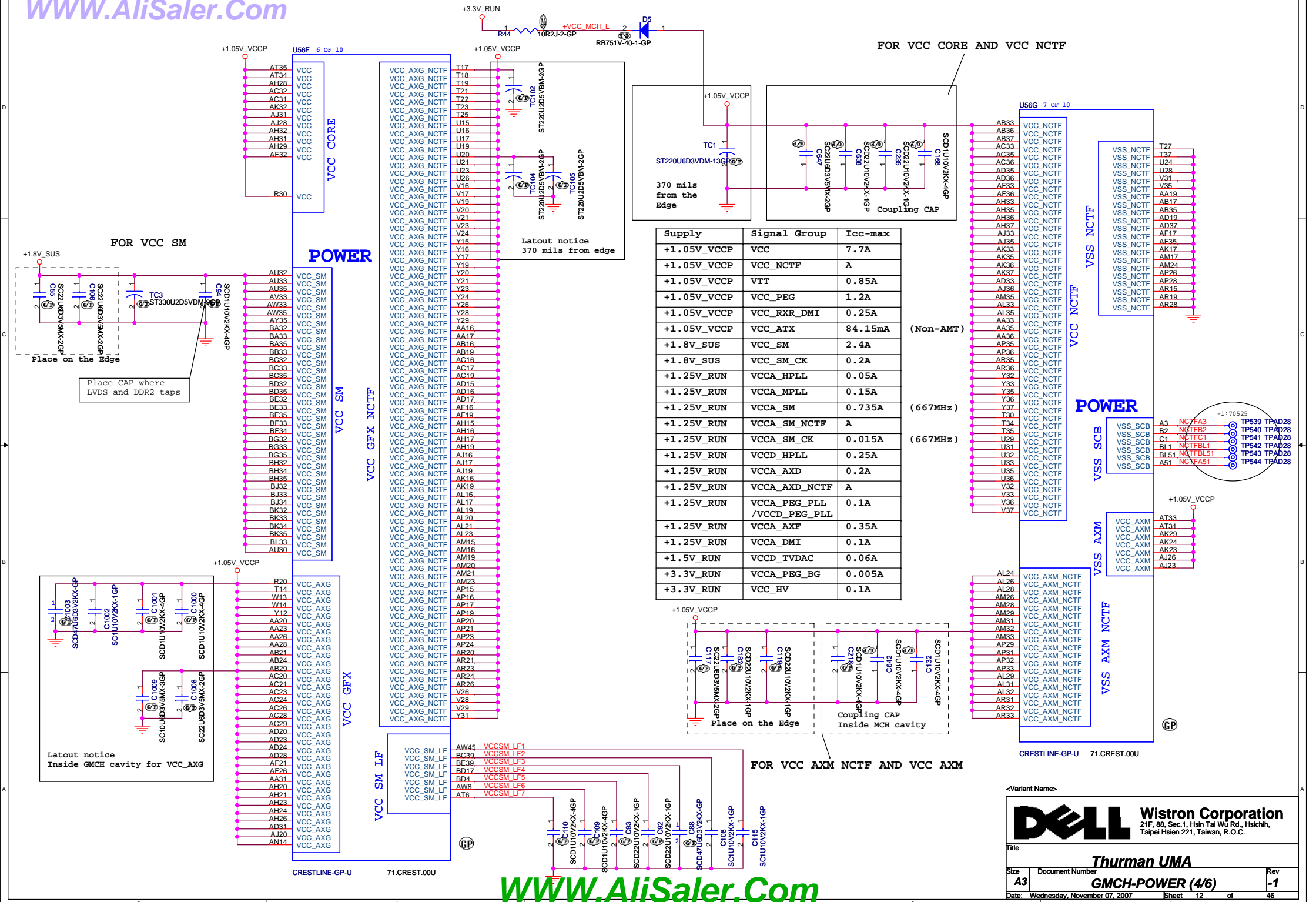
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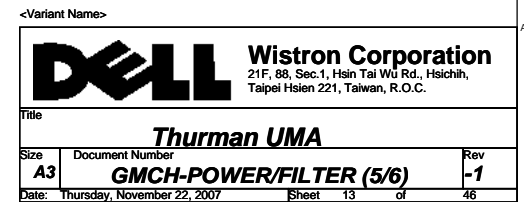


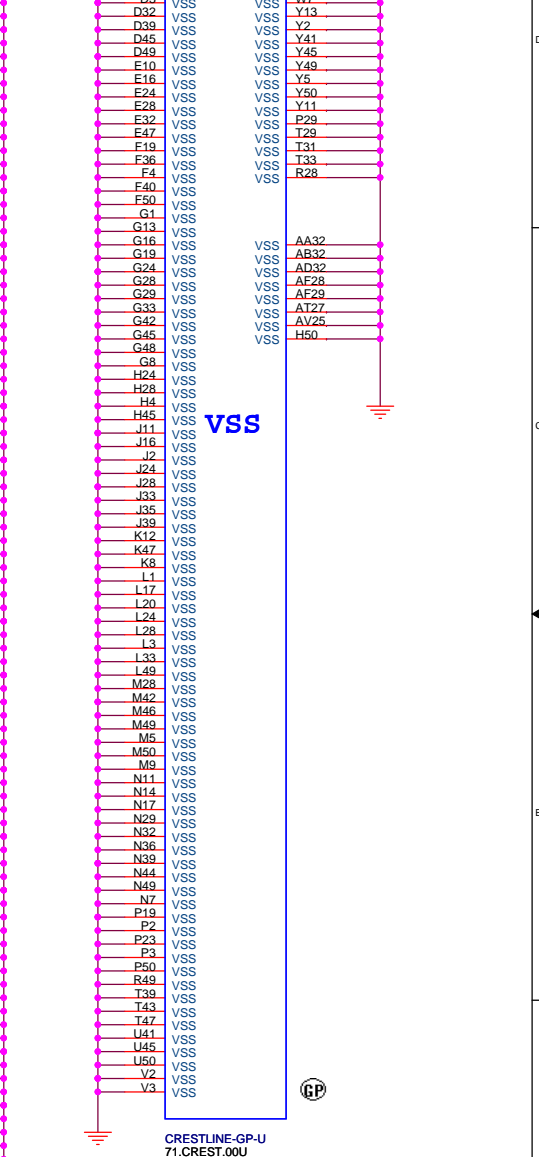
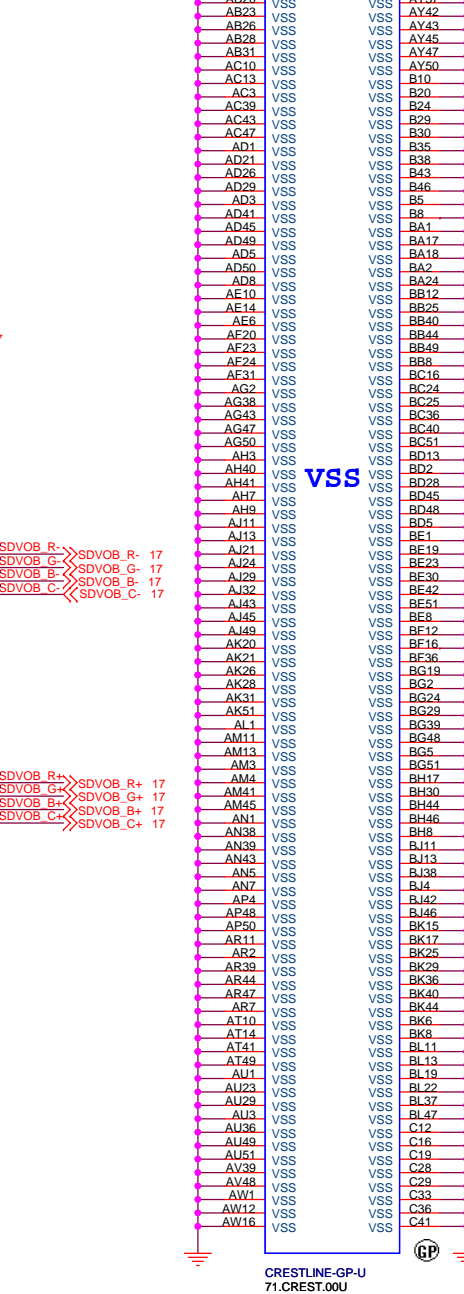
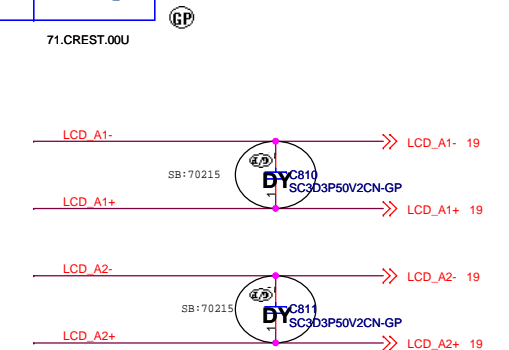
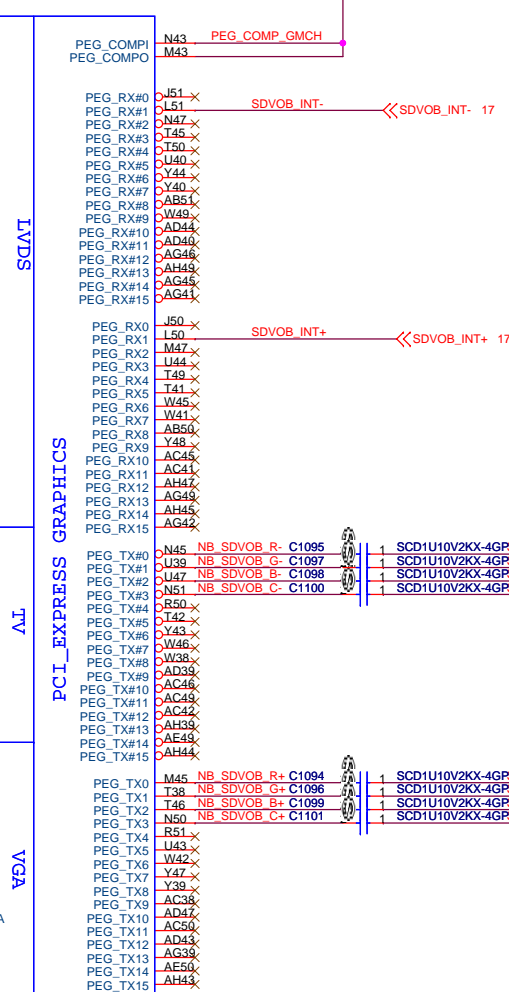
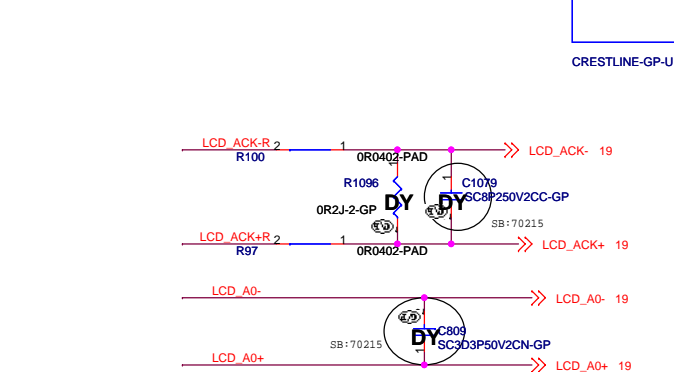
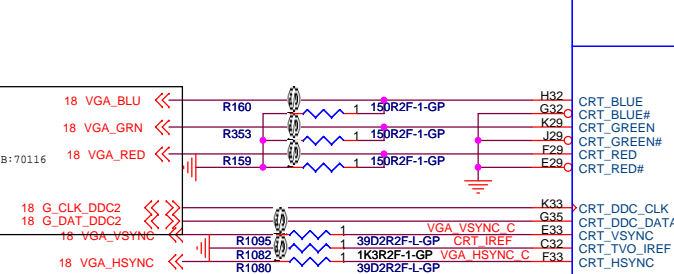
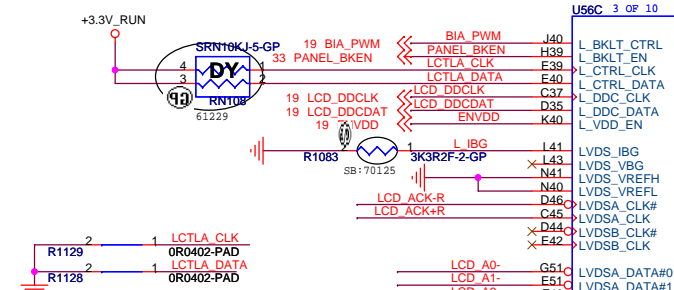
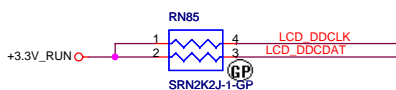
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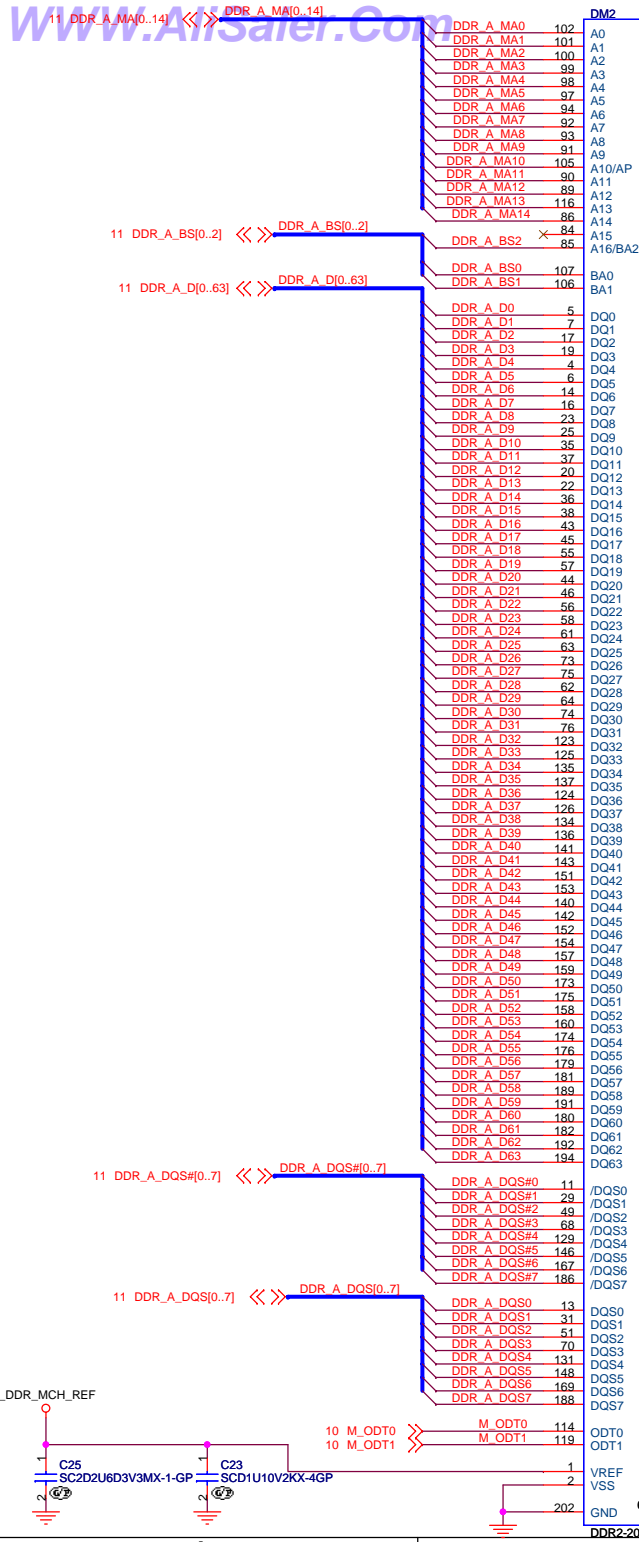
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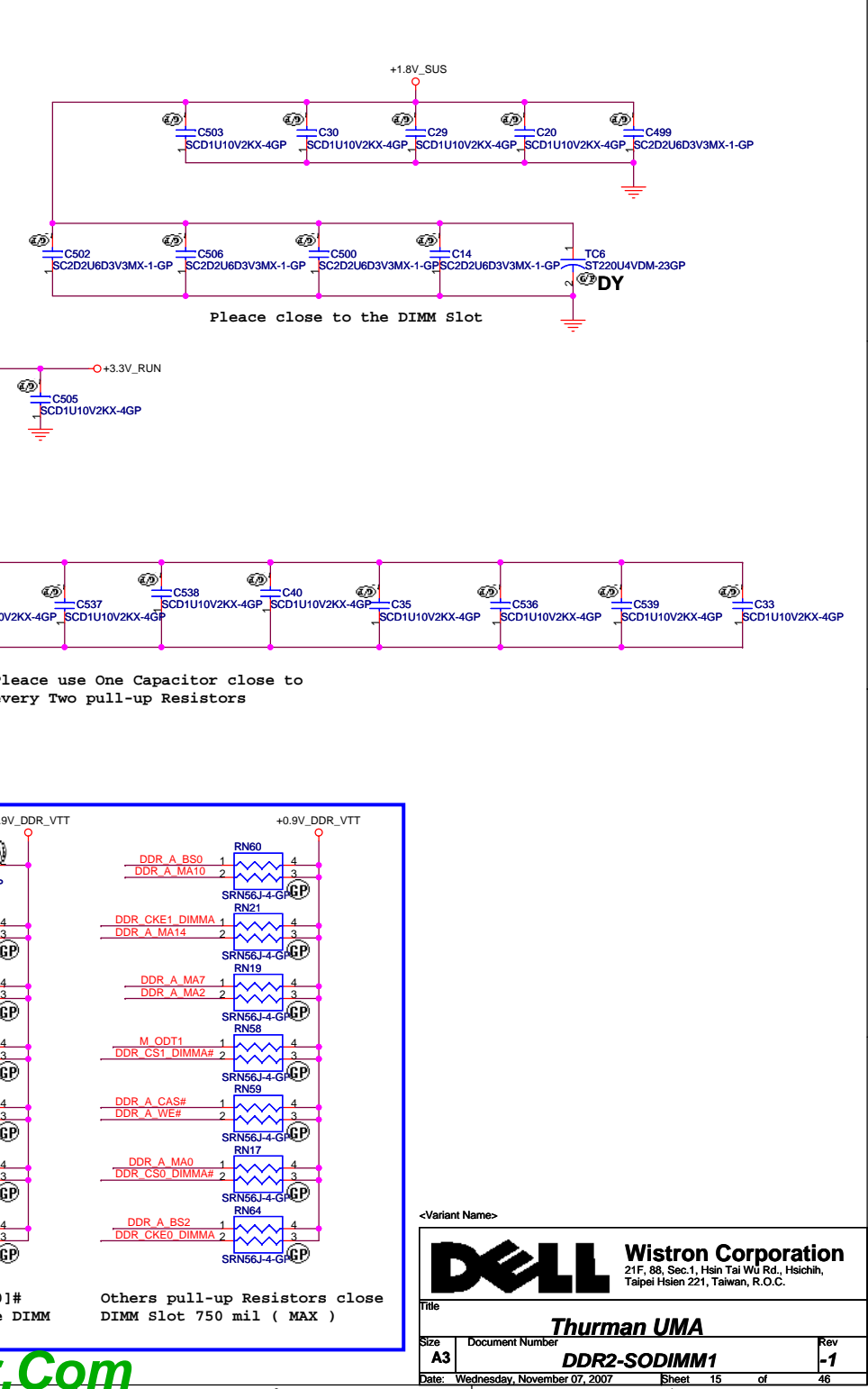
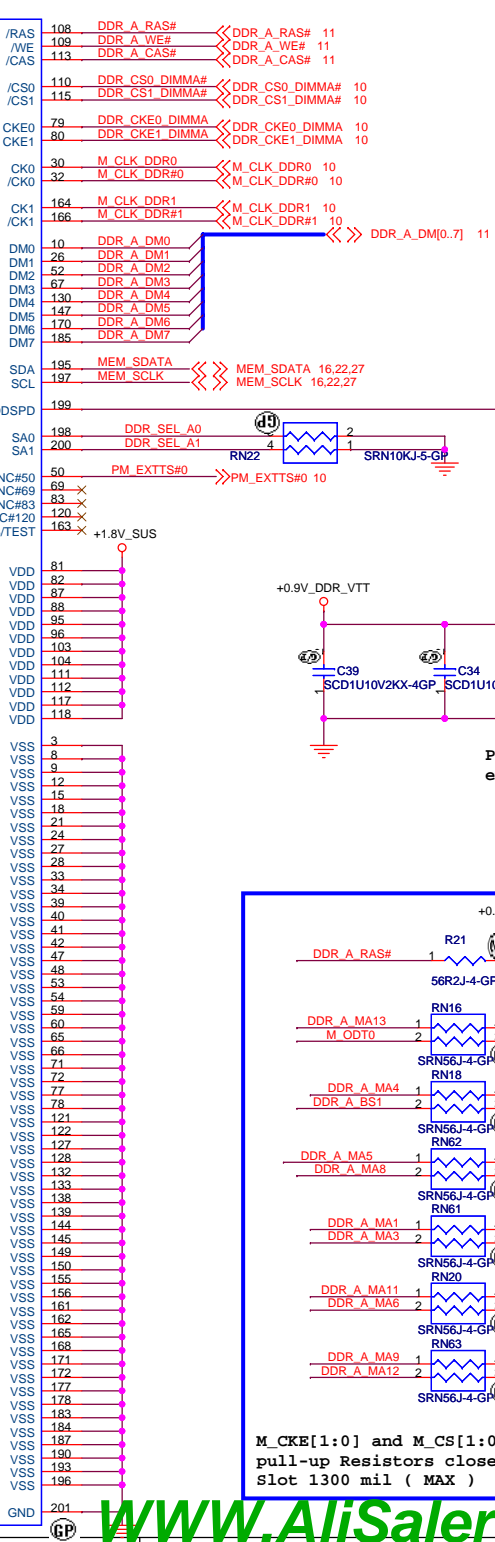








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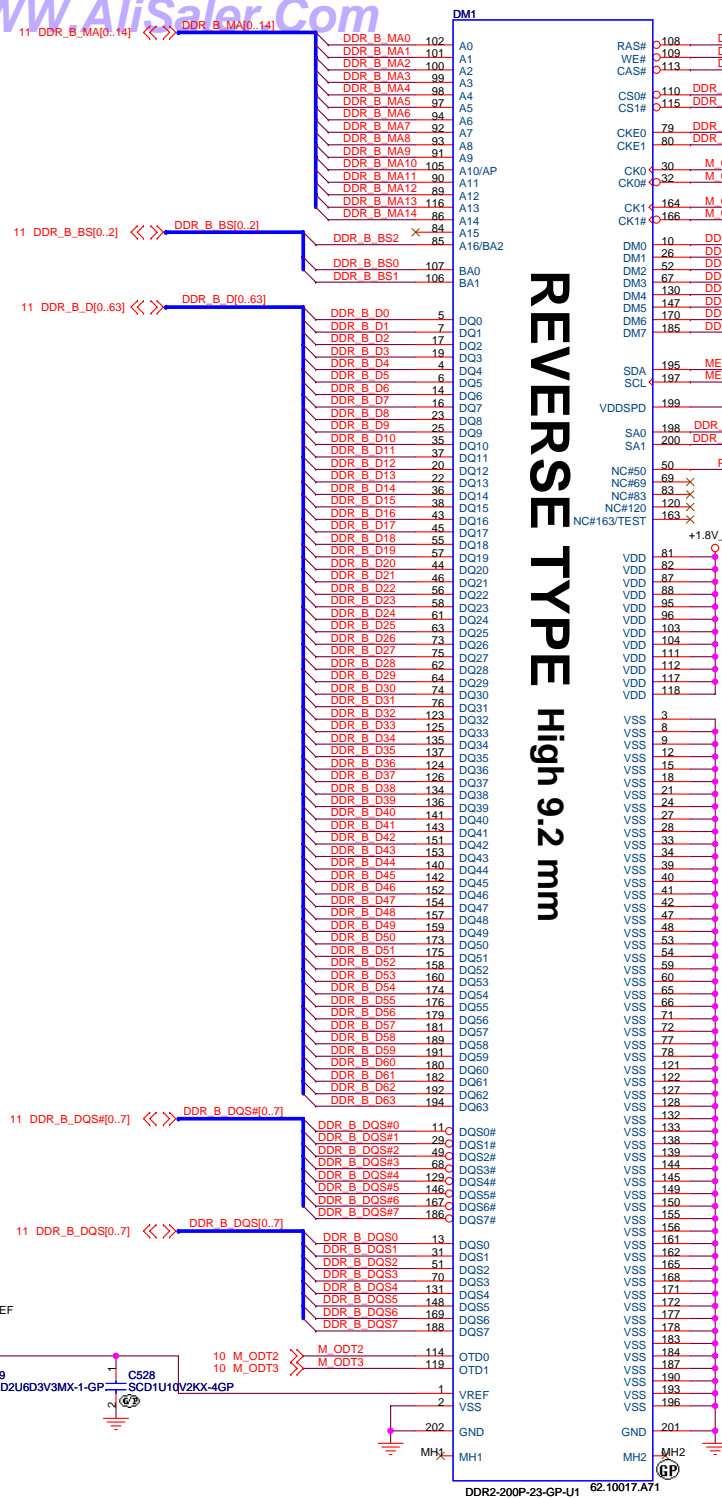
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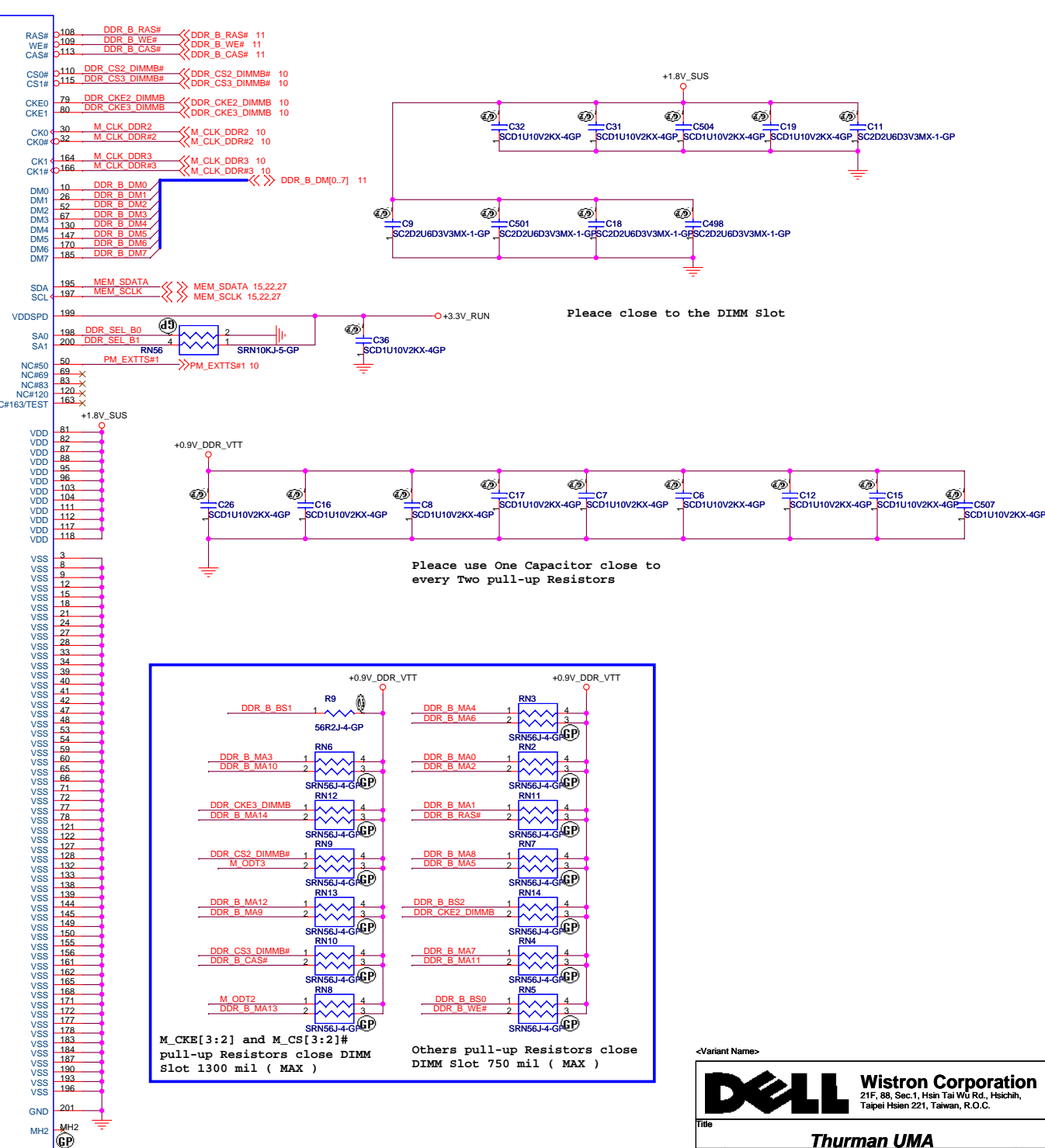
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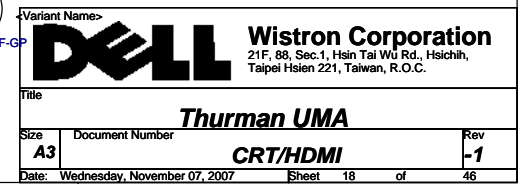
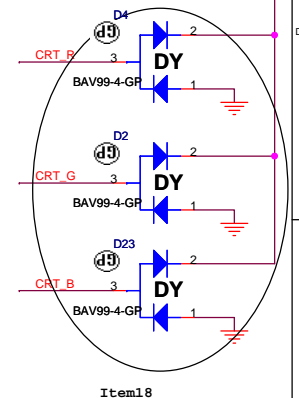


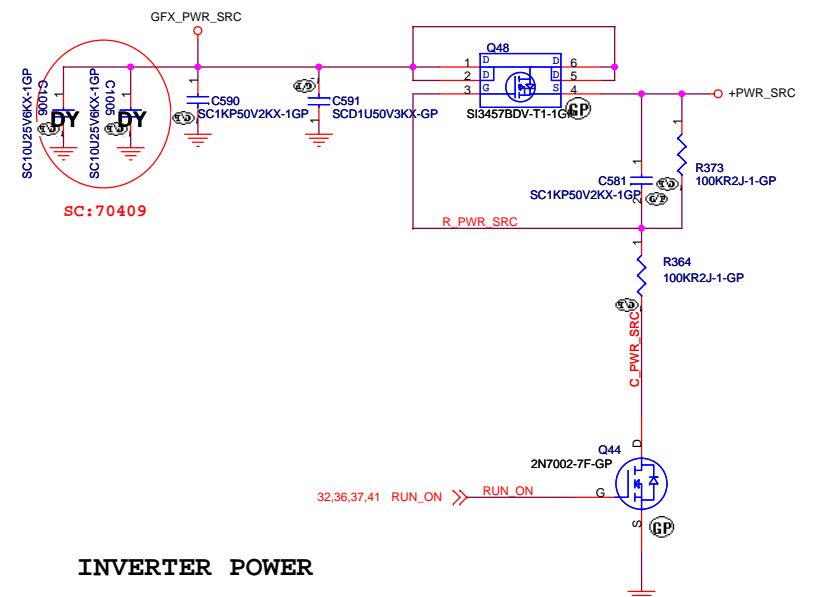
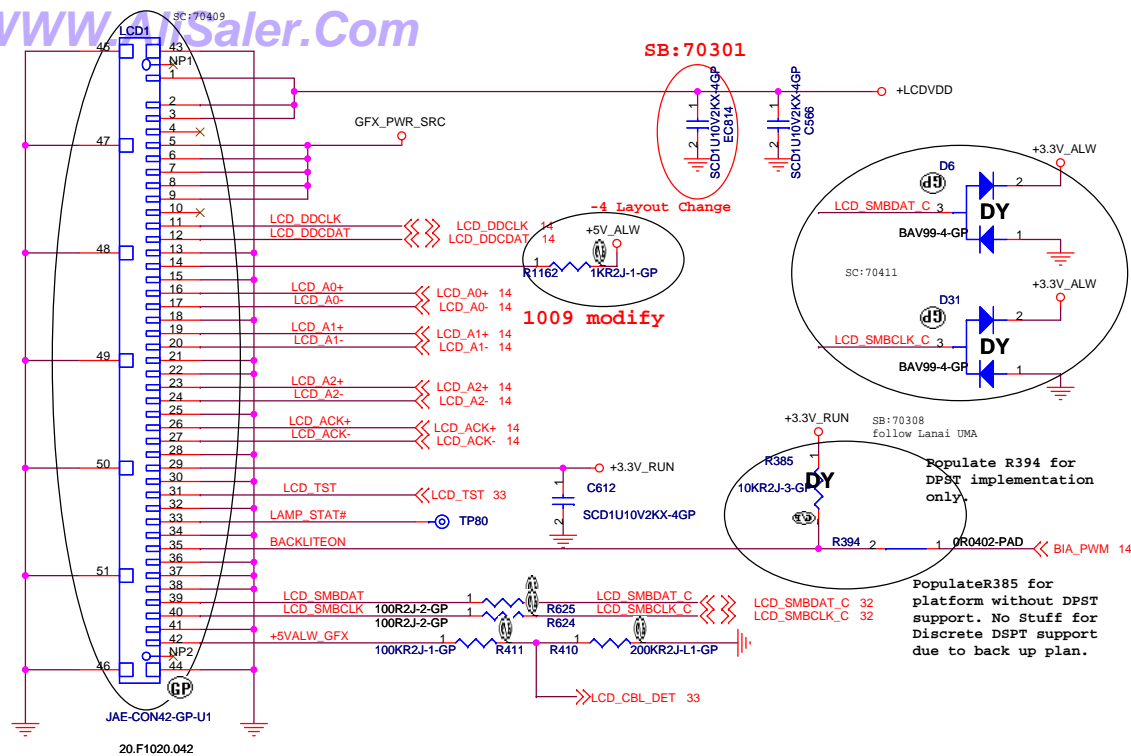
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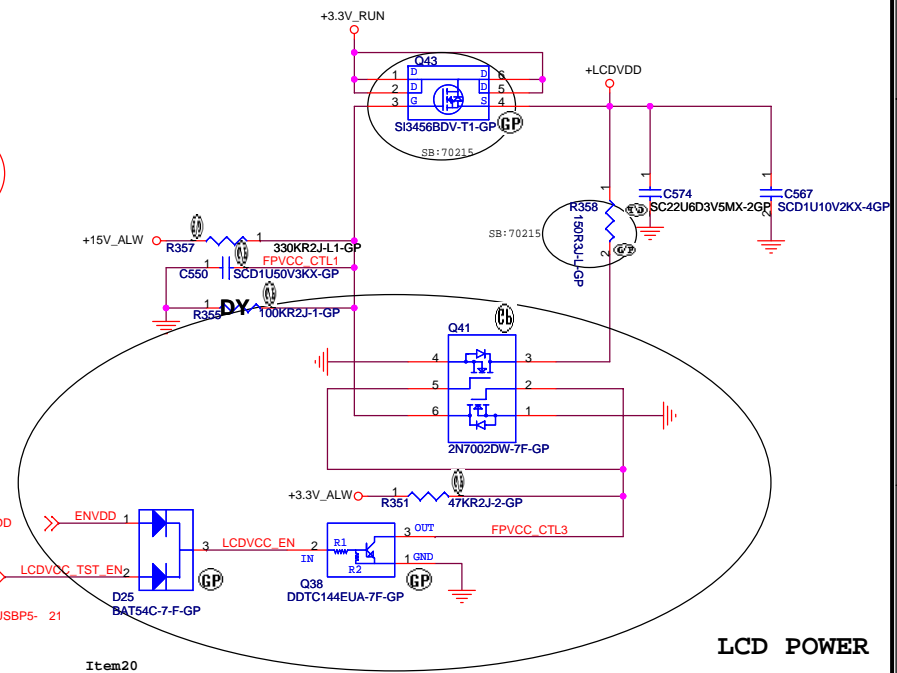
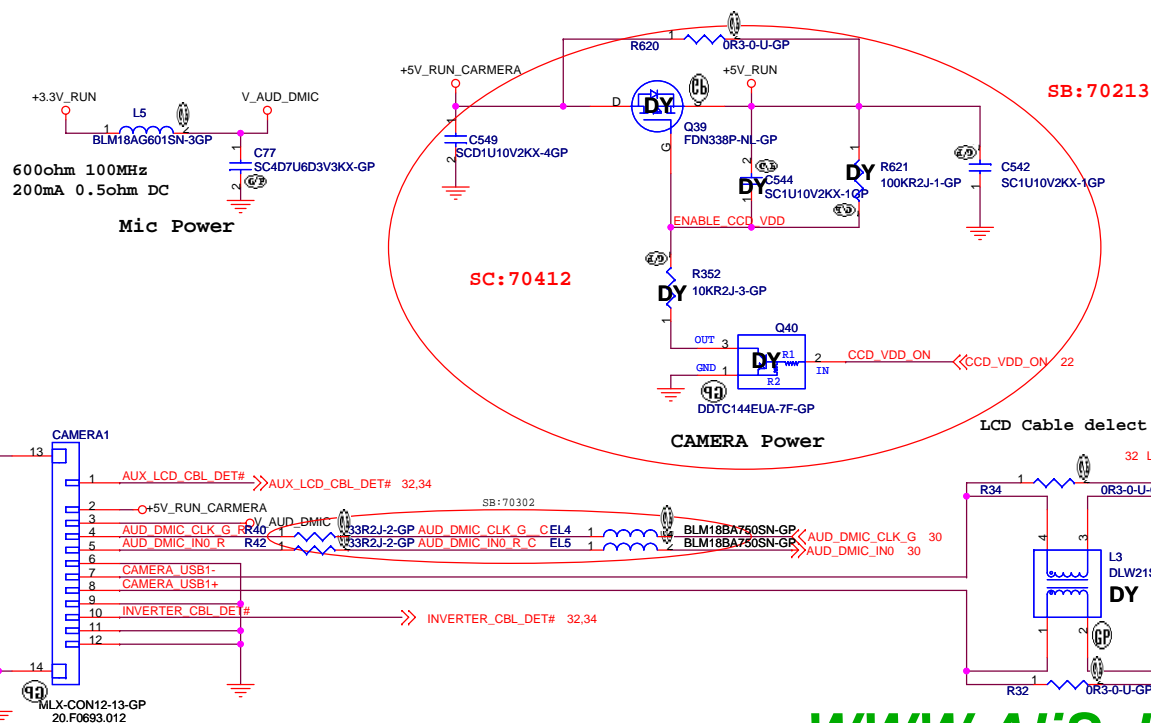


```
SPDIF: Stuff
R1123,R1113,R1115,R1117
```





INVERTER POWER



LCD POWER



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Title	
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Size

Document Number

LVDS

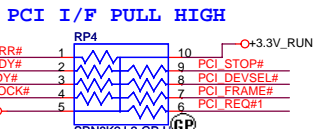
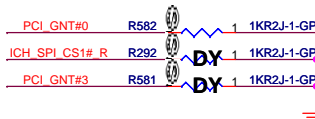
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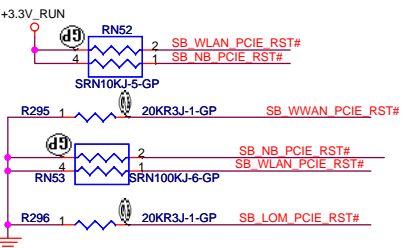
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BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

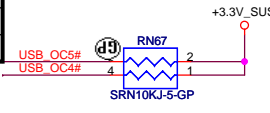
Al6 swap override strap	
PCI_GNT#3 (R168)	
low	= Al6 swap override enable
high	= default



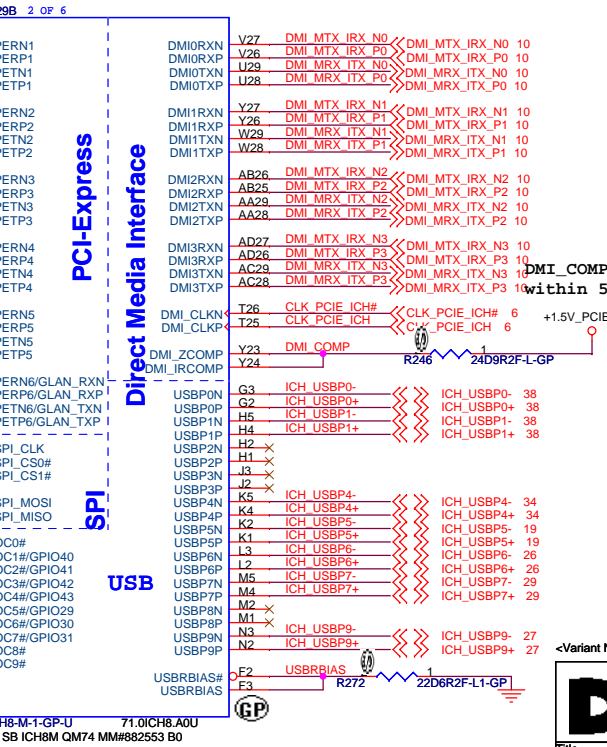
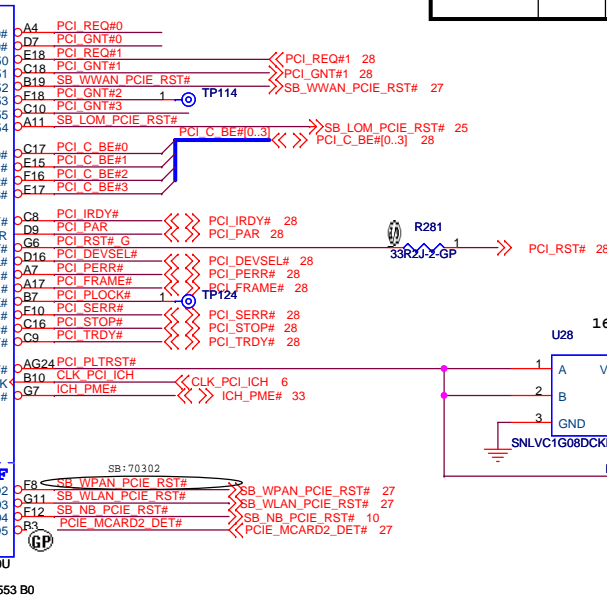
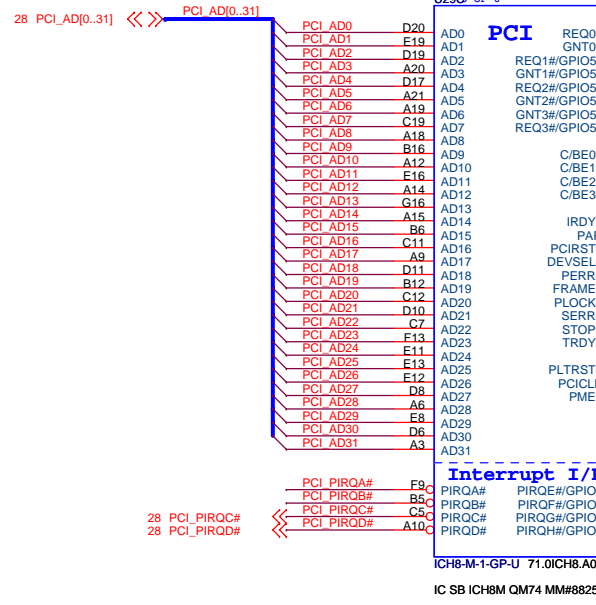
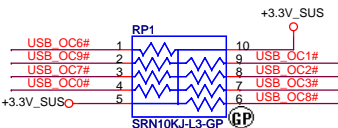
BIOS should not enable the internal GPIO pull up



PCIe Interface Routing	
LANE	Function
LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN

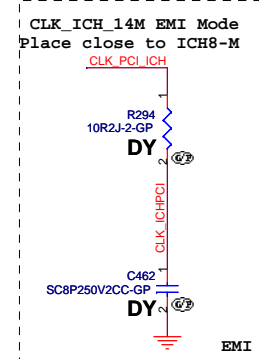
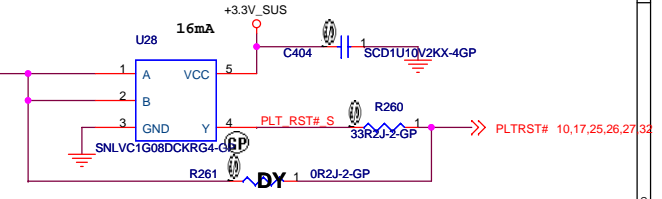


Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.



	IDSEL	INT	REQ	GNT	PCI Interface Routing
1394/MediaCard	AD17	C	1	1	

Add Buffers as need for Loading and Fanout concerns

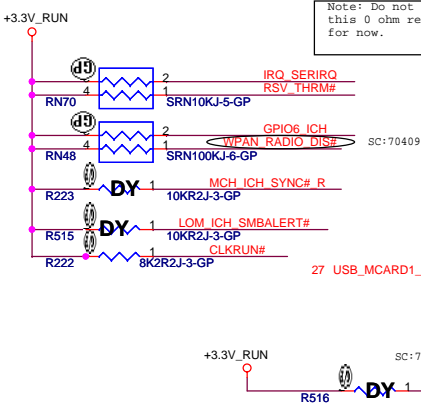
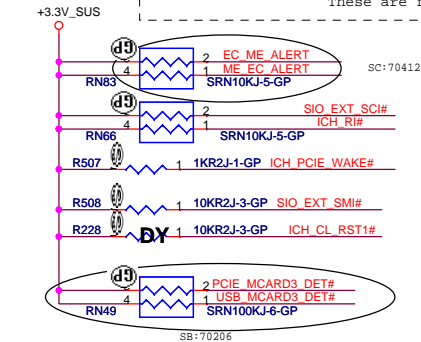
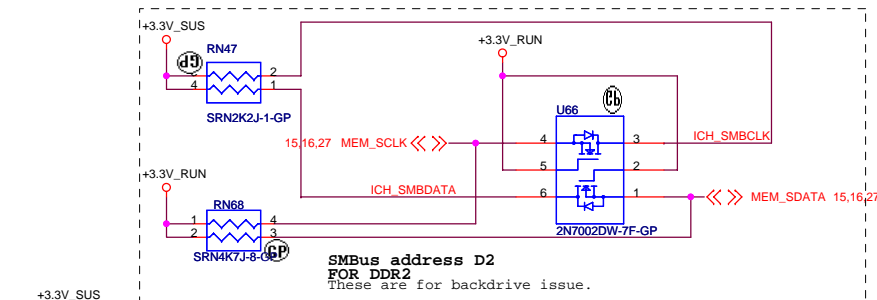


USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	MINI Card WLAN
USB9	

<Variant Name>

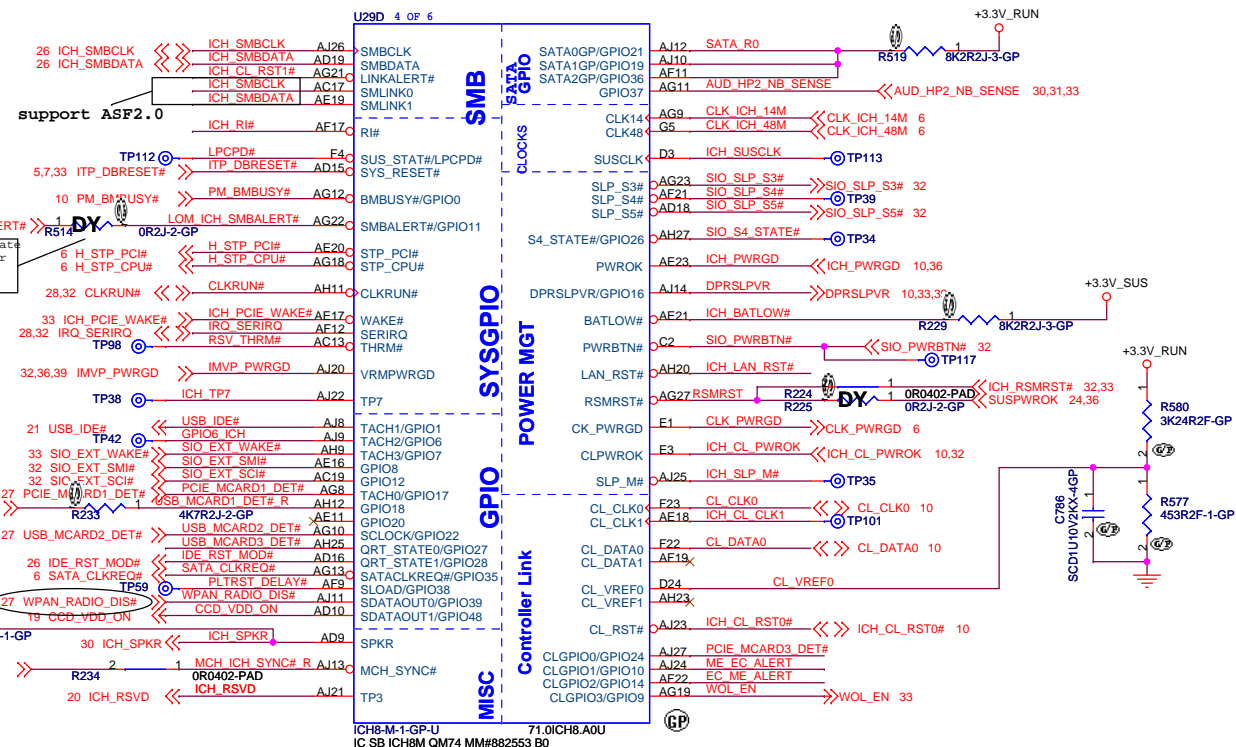
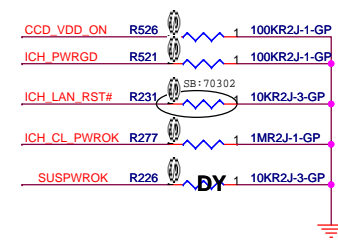
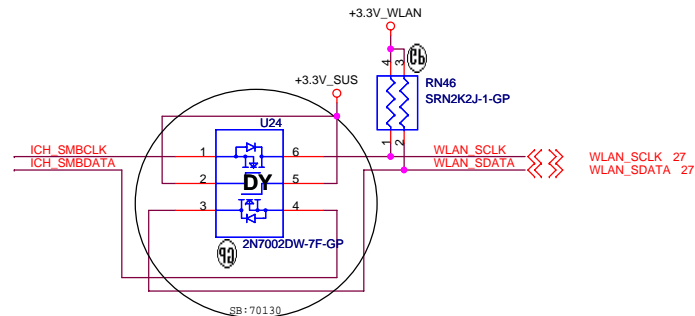
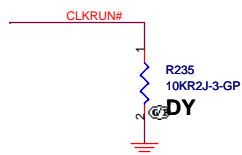


Thurman UMA		
Size	Document Number	Rev
A3	ICH8M-PCIE/USB/SPI/DMI (2/4)	-1
Date:	Thursday, November 22, 2007	Sheet 21 of 46

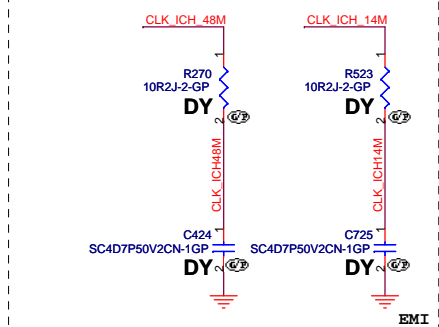


ICH8-Strap PIN

No Reboot Strap	
ICH_SPKR	LOW = Defaule
	High=No Reboot



CLK_ICH_48M and CLK_ICH_14M EMI Mode Place close to ICH8-M





Size	Document Number	Rev
Custom	ICH8M-POWER (4/4)	-1
Date: Wednesday, November 07, 2007	Sheet 23 of 46	

REM_DIODE1_N and REM_DIODE1_P
routing Trace width and Spacing
use 10 / 10 mil

Place inside CPU socket

C300 Please close to Guardian

Close to Pin5, Pin6

Close to Pin9

REM_DIODE4_N and REM_DIODE4_P
routing Trace width and Spacing
use 10 / 10 mil

Thermal sensor for Mini Card
should be placed TOP Side under WWAN CARD

C260 Please Close to Guardian

H_THERMDA and H_THERMDC
routing Trace width and
Spacing use 10 / 10 mil

C295 Please close to Guardian

7 H_THERMDA

7 H_THERMDC

+RTC_CELL

+3.3V_SUS

SCD1U10V2KX-4GP

C298

R455

332K2F-GP

SCD1U10V2KX-4GP

C664

SC2200P50V2KX-2GP

R454

118K2F-1-GP

SCD1U10V2KX-4GP

C295

SC470P50V2KX-3GP

22.36 SUSPWOK

36 ICH_PWRGD#

SCD1U10V2KX-4GP

C310

49D9R2F-GP

SCD1U10V2KX-4GP

C298

R455

332K2F-GP

SCD1U10V2KX-4GP

C664

SC2200P50V2KX-2GP

R454

118K2F-1-GP

SCD1U10V2KX-4GP

C295

SC470P50V2KX-3GP

22.36 SUSPWOK

36 ICH_PWRGD#

SCD1U10V2KX-4GP

C310

49D9R2F-GP

SCD1U10V2KX-4GP

C298

R455

332K2F-GP

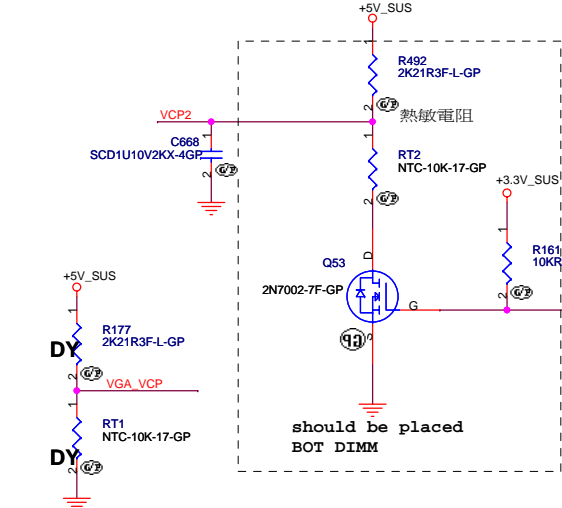
SCD1U10V2KX-4GP

C664

SC2200P50V2KX-2GP

Note :

$VSET = (T_p - 70) / 21$
 $3.3 * (R411 / R406 + R411) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degrees C
 T_p set at 88 degrees C
 Guardian temp tolerance = ± 3 degrees C



should be placed
BOT DIMM

Version B: 74.04001.A73

SB:70205

FAN1_OUT

D27

RB751V-40-1-GP

C546

SC22U6D3V5MX-2GP

SC1KP50V2KX-1GP

C532

MLX-CON4-19-GP

20.D0198.104

FAN1_DET# 33

pull up on SIO

SCD1U10V2KX-4GP

C279

SCD1U10V2KX-4GP

C285

SCD1U10V2KX-4GP

C279

SCD1U10V2KX-4GP

C285

SCD1U10V2KX-4GP

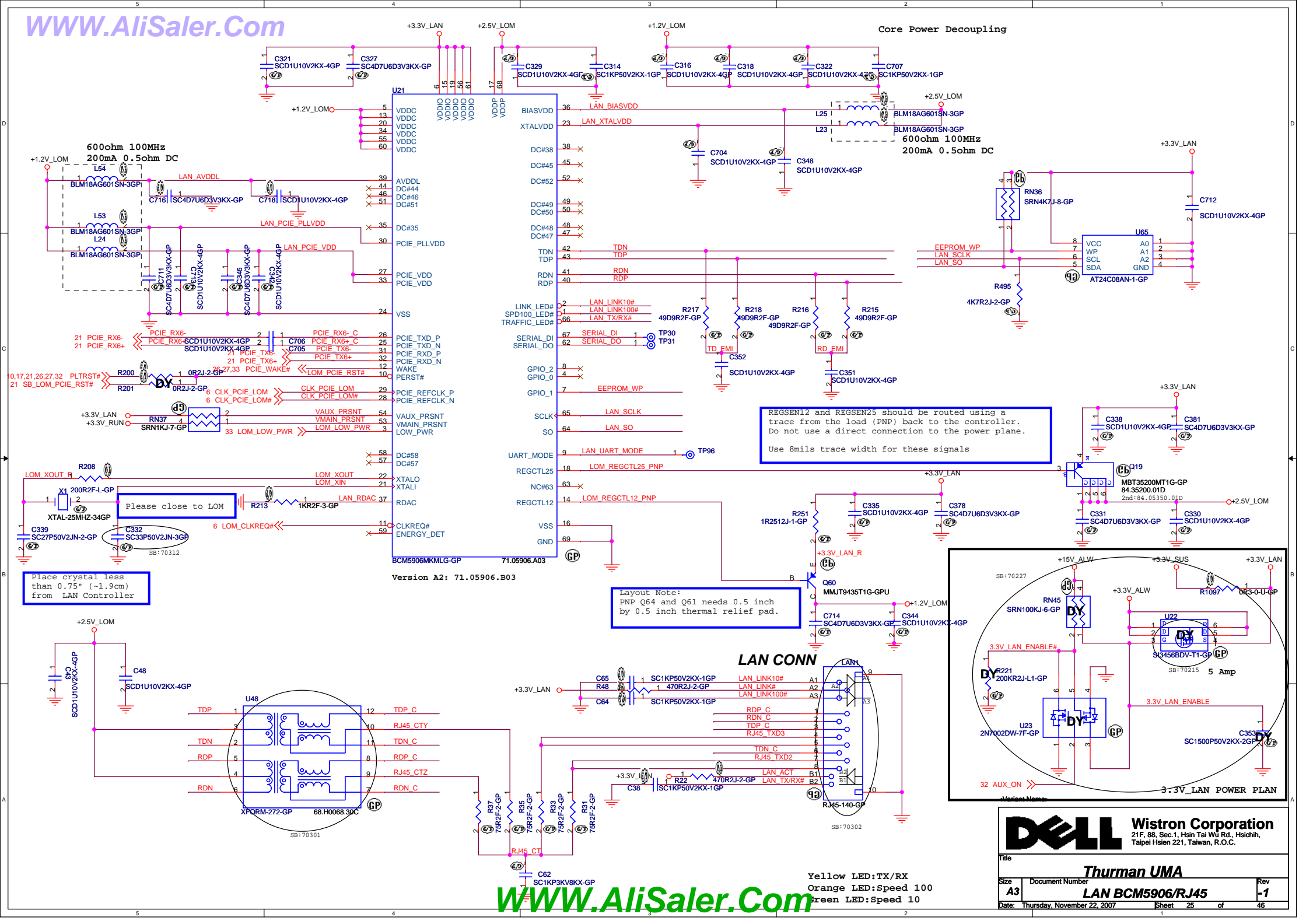
C279

SCD1U10V2KX-4GP

C285

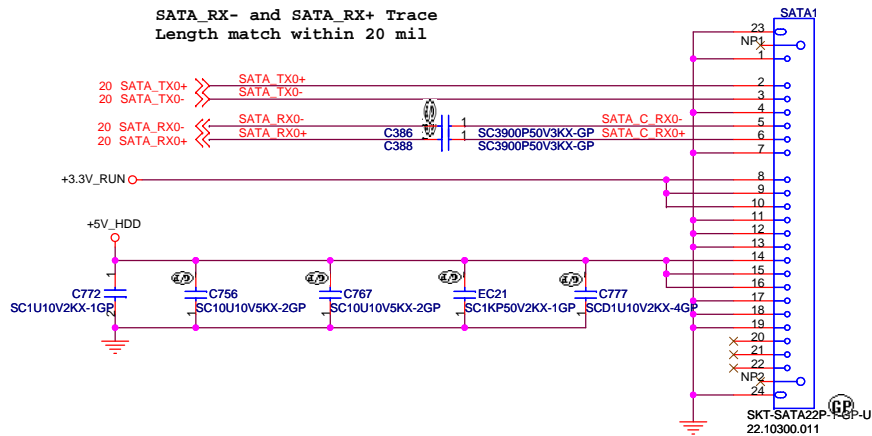
SCD1U10V2KX-4GP

C916, C459, C472 Please Close to Guardian

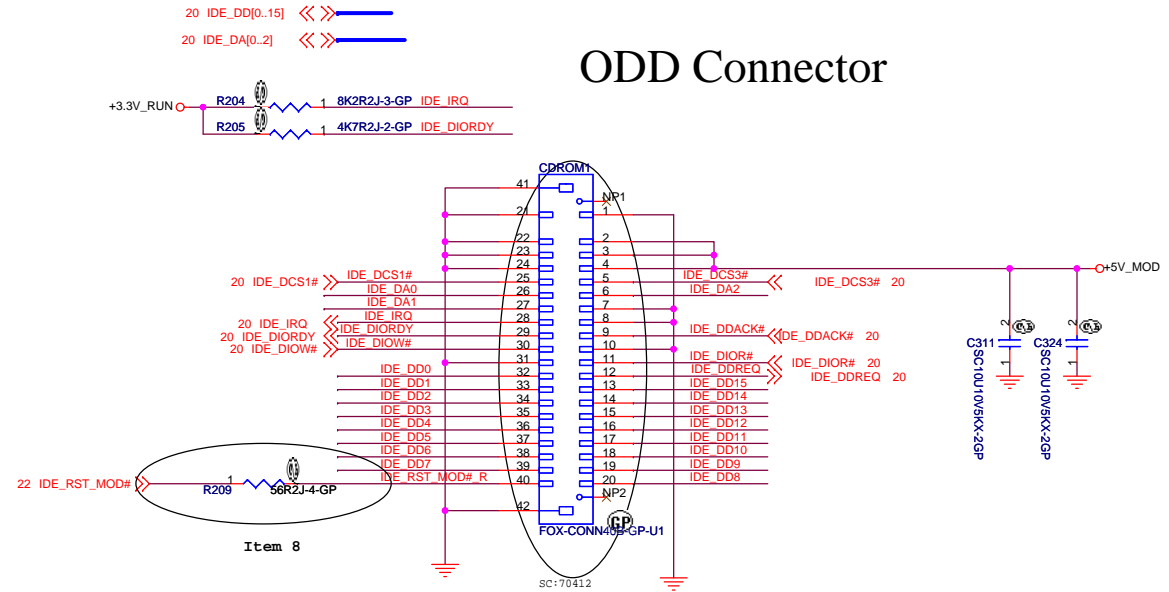


SSID = IDE & SATA

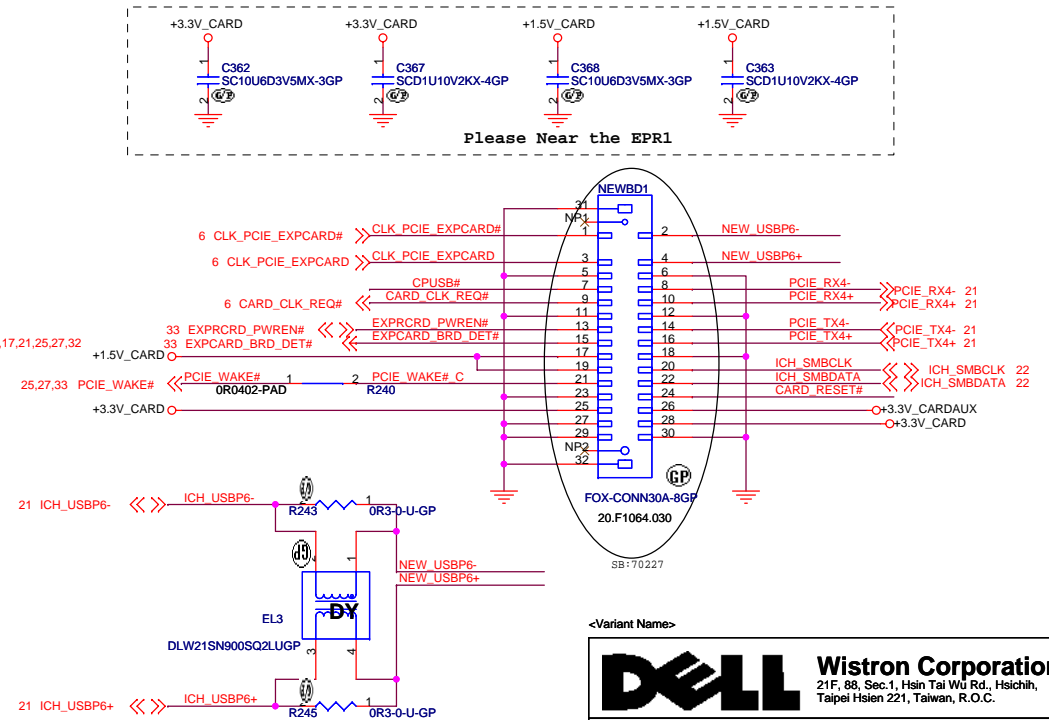
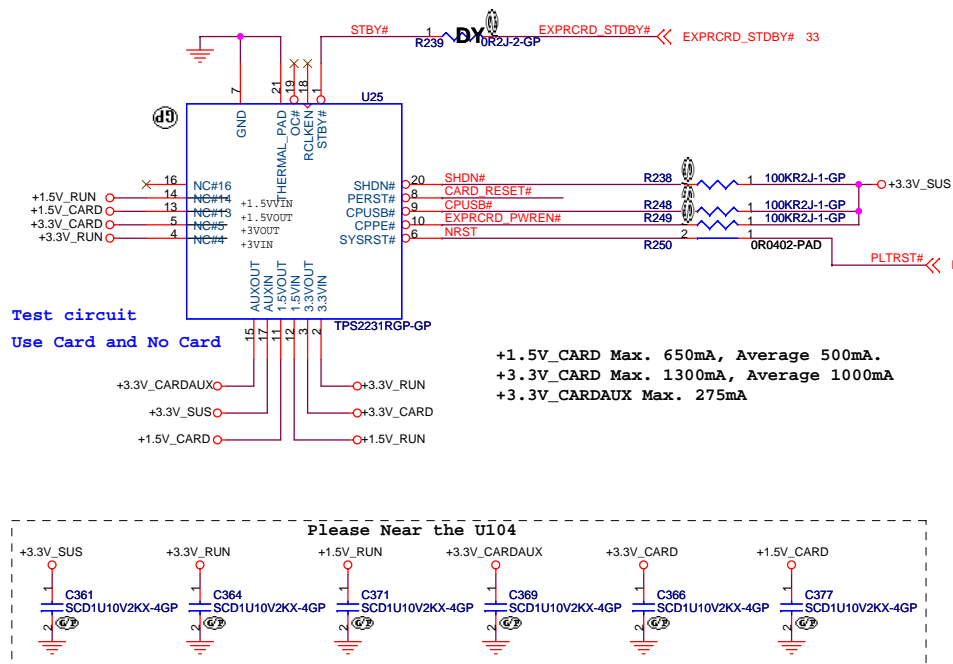
SATA HDD Connector



ODD Connector



Express Card



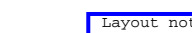
<Variant Name>

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

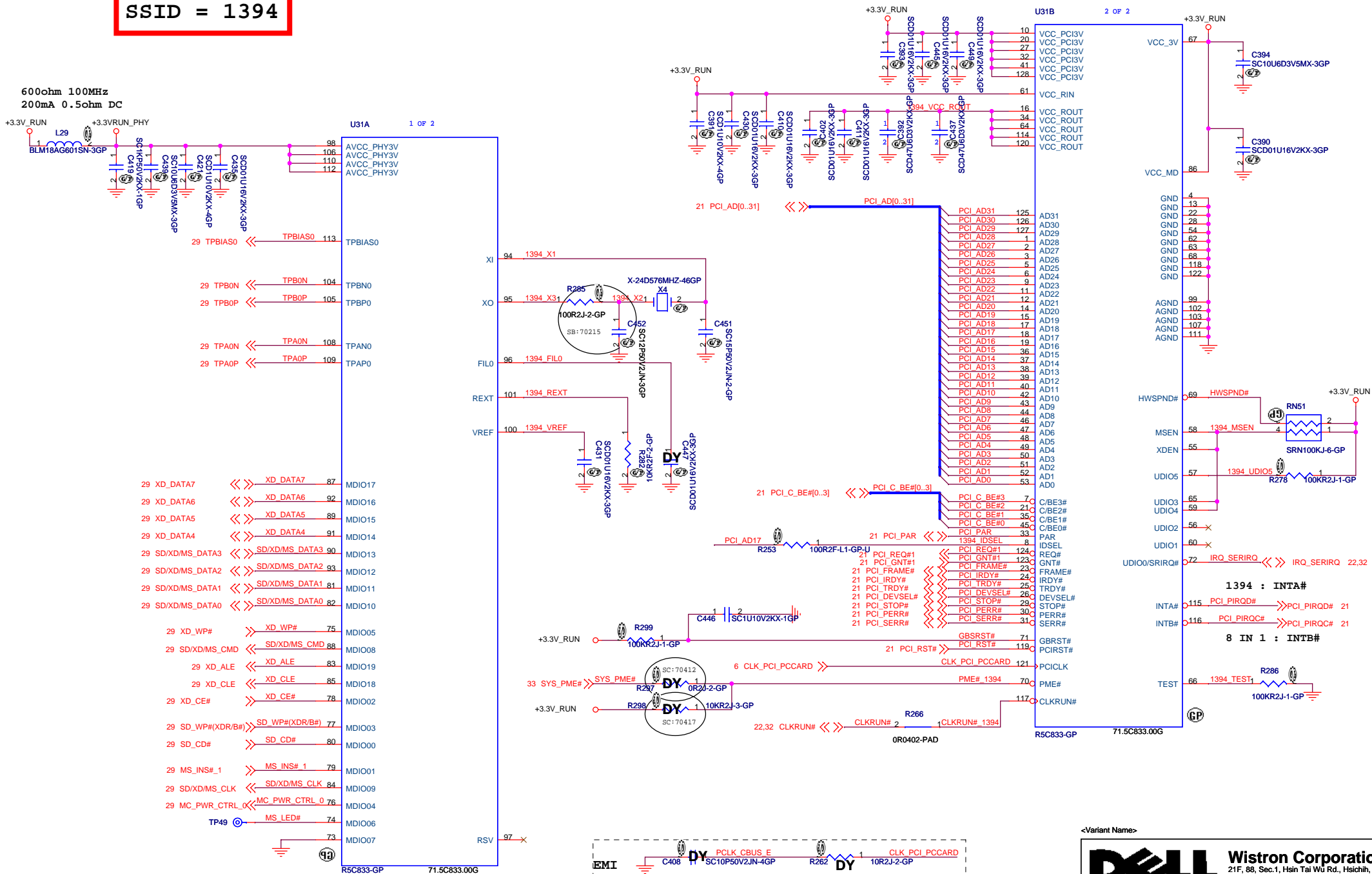
Title
Thurman UMA
Size A3 Document Number
HDD/ODD/TO EXPRESS BD CONN-1 Rev
Date: Wednesday, November 07, 2007 Sheet 26 of 46

WWW.AliSaler.Com

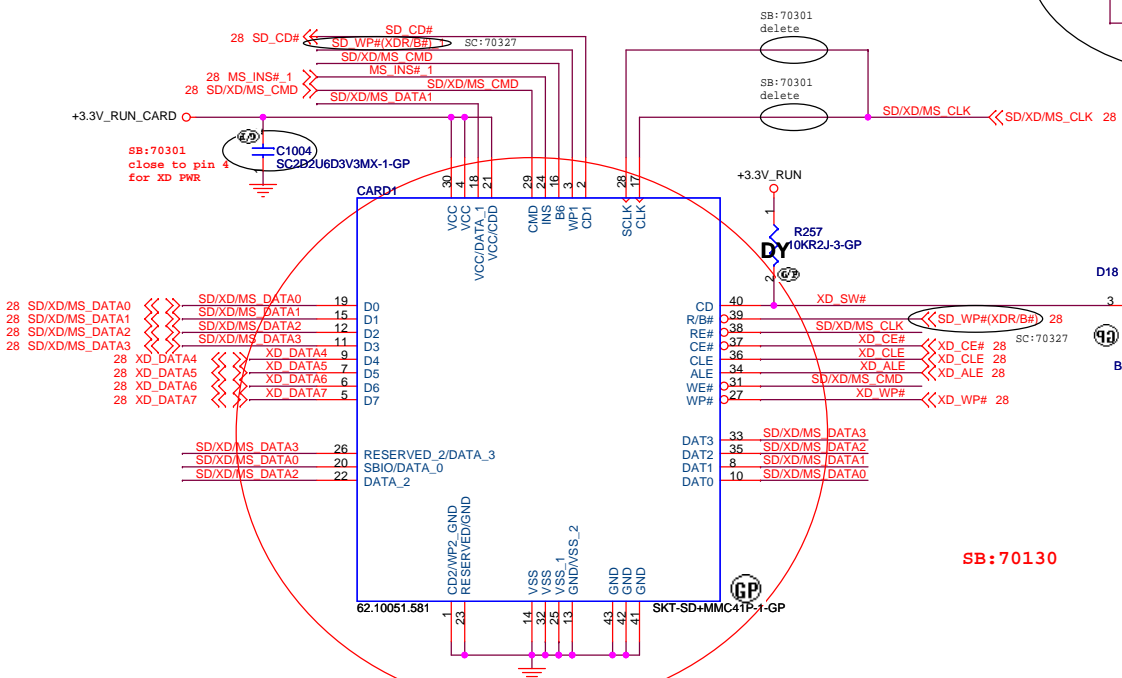
DEBUG PINS



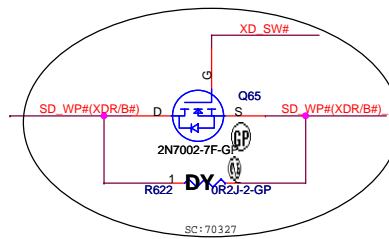
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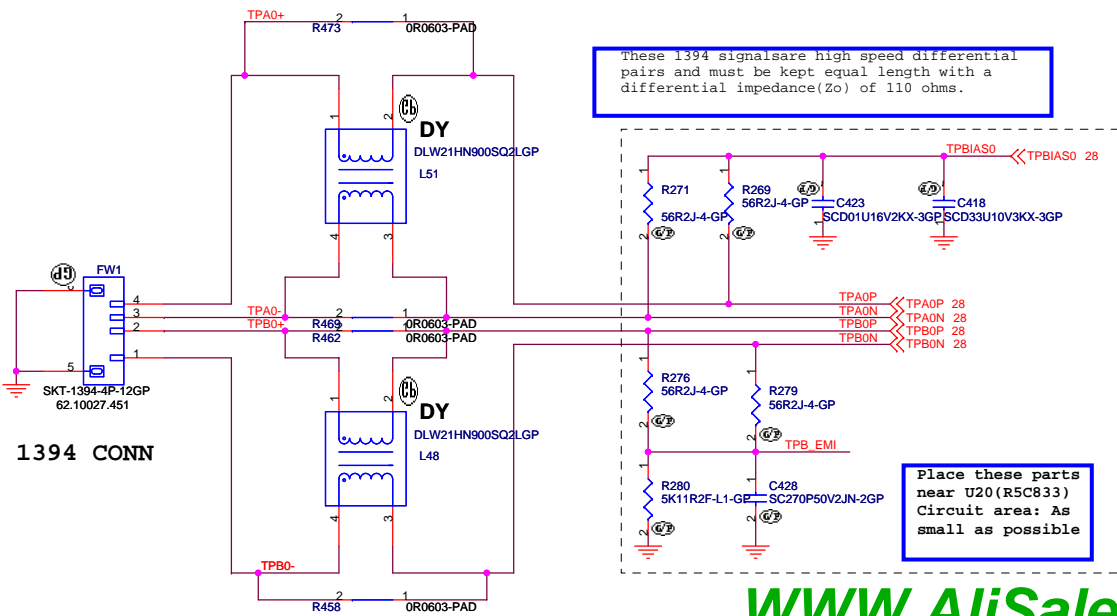
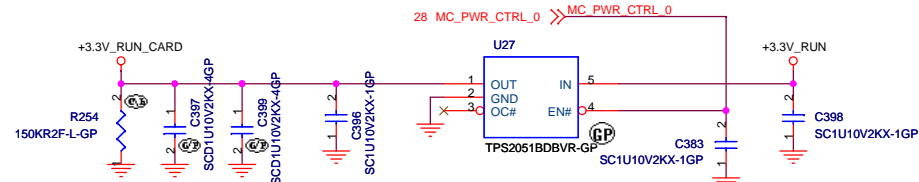
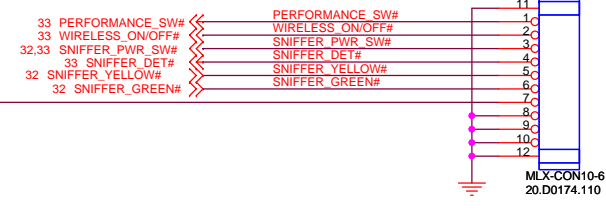
Card Reader CONN



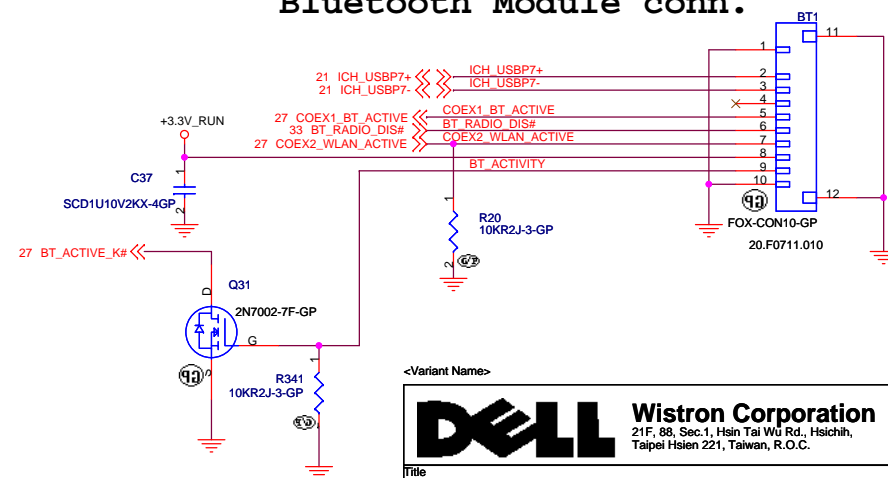
SB:70130



SNIFFER BOARD CONN



Bluetooth Module conn.



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thurman UMA

Size

Document Number

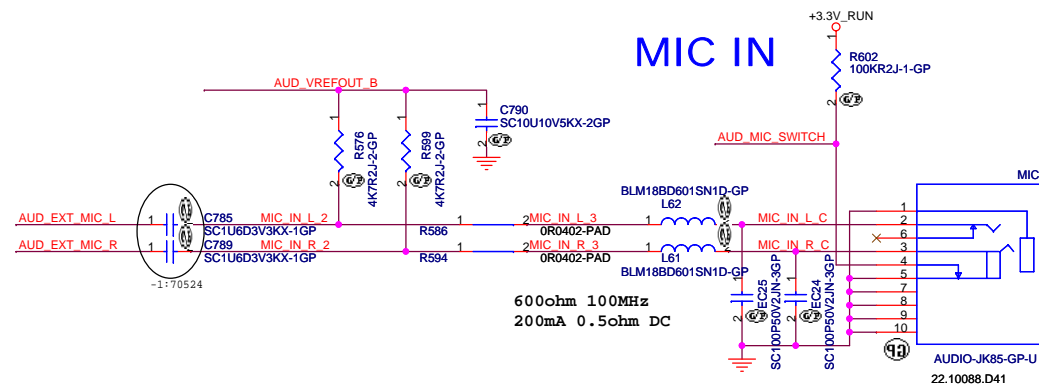
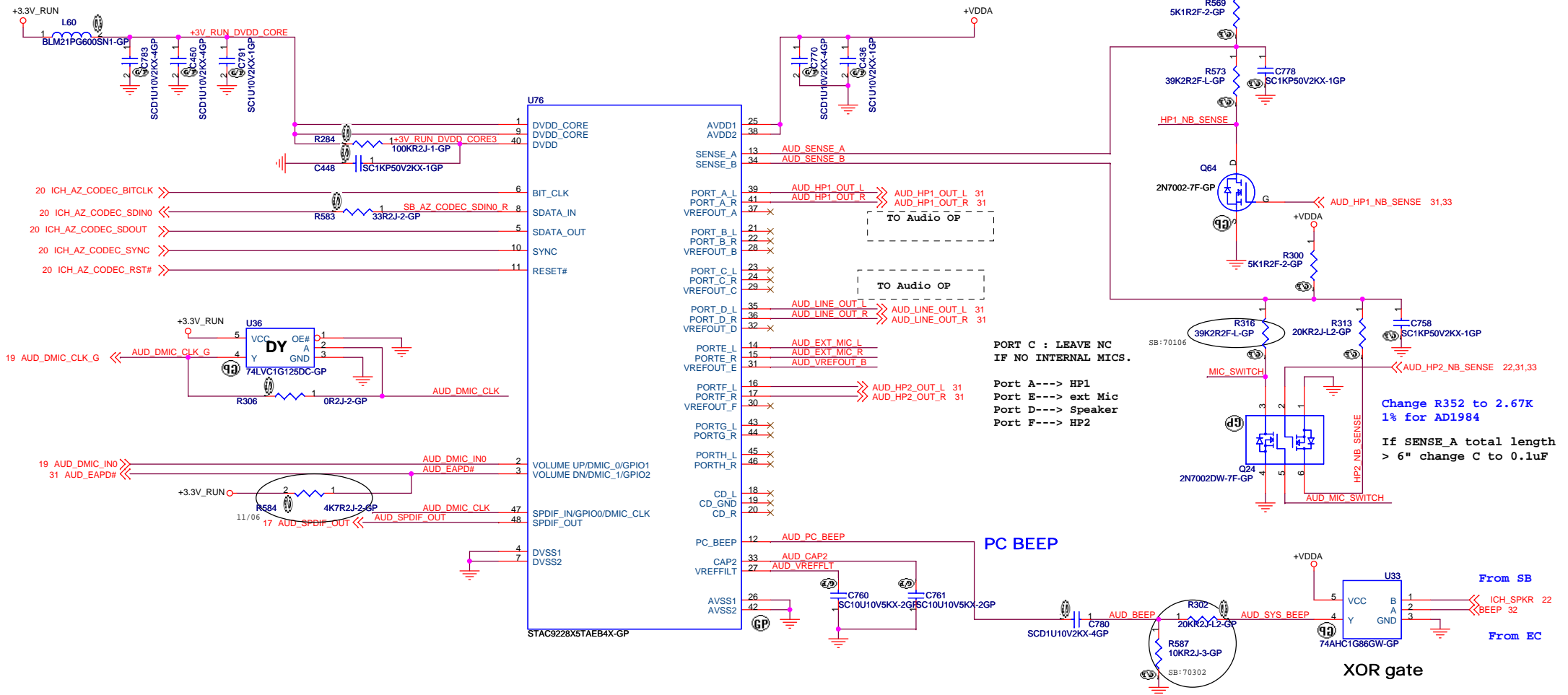
8in1 /1394/SNIFFER BD CON/BT

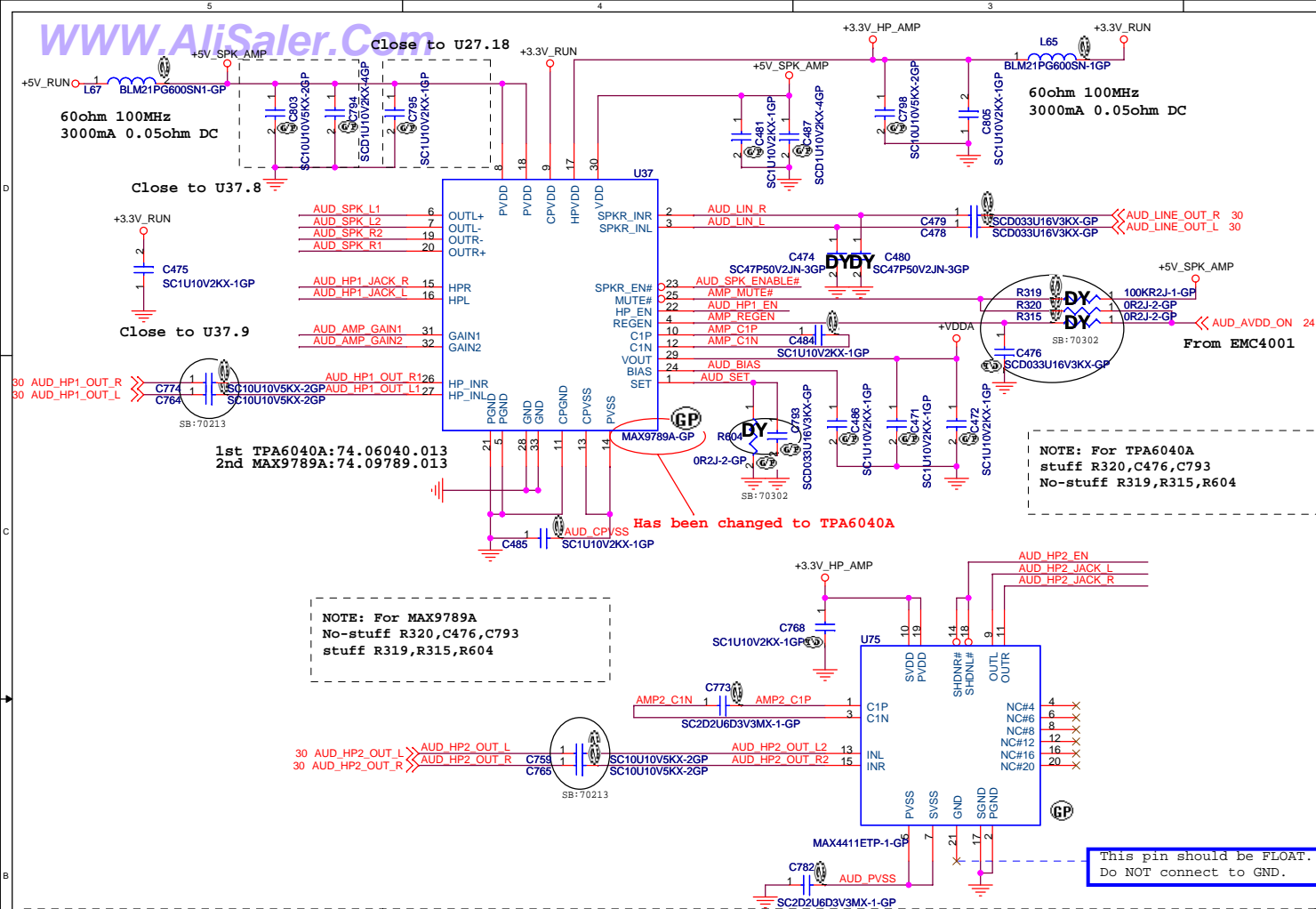
Rev

Date: Wednesday, November 07, 2007

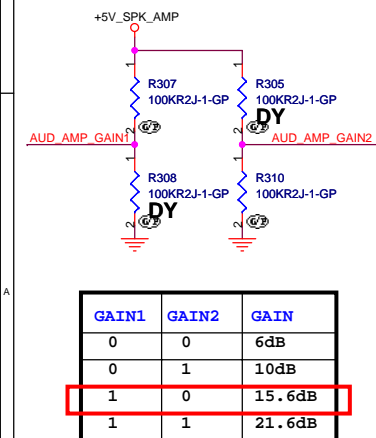
Sheet 2

46



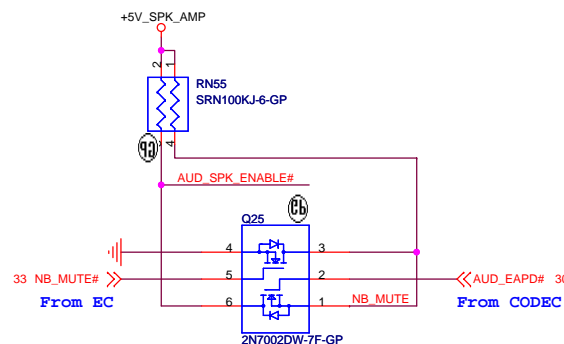


GAIN SETTING

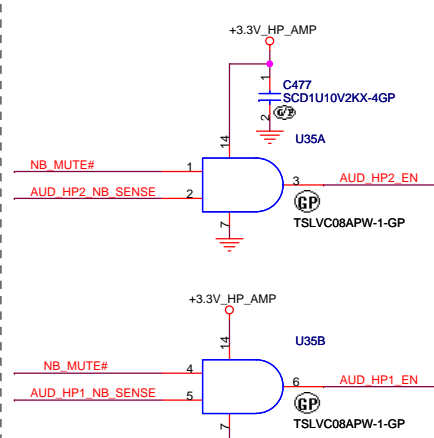


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

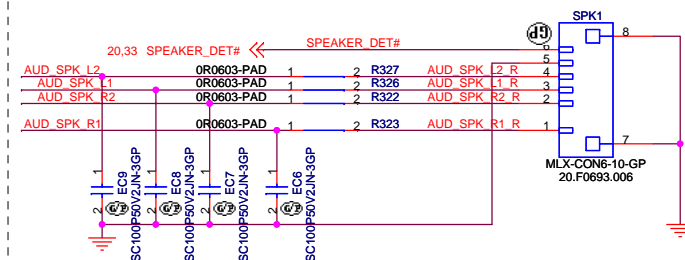
Signal inverter for speaker shutdown



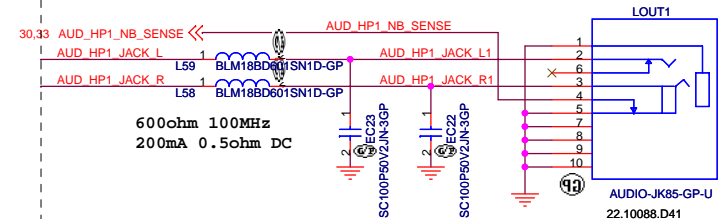
AND Gate for HP Mute Function



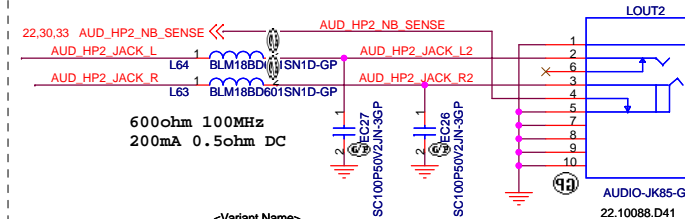
Speaker



LINE1 OUT



LINE2 OUT



<Variant Name>

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Title

Thurman UMA

Size

Document Number

AUDIO AMP

Date _____

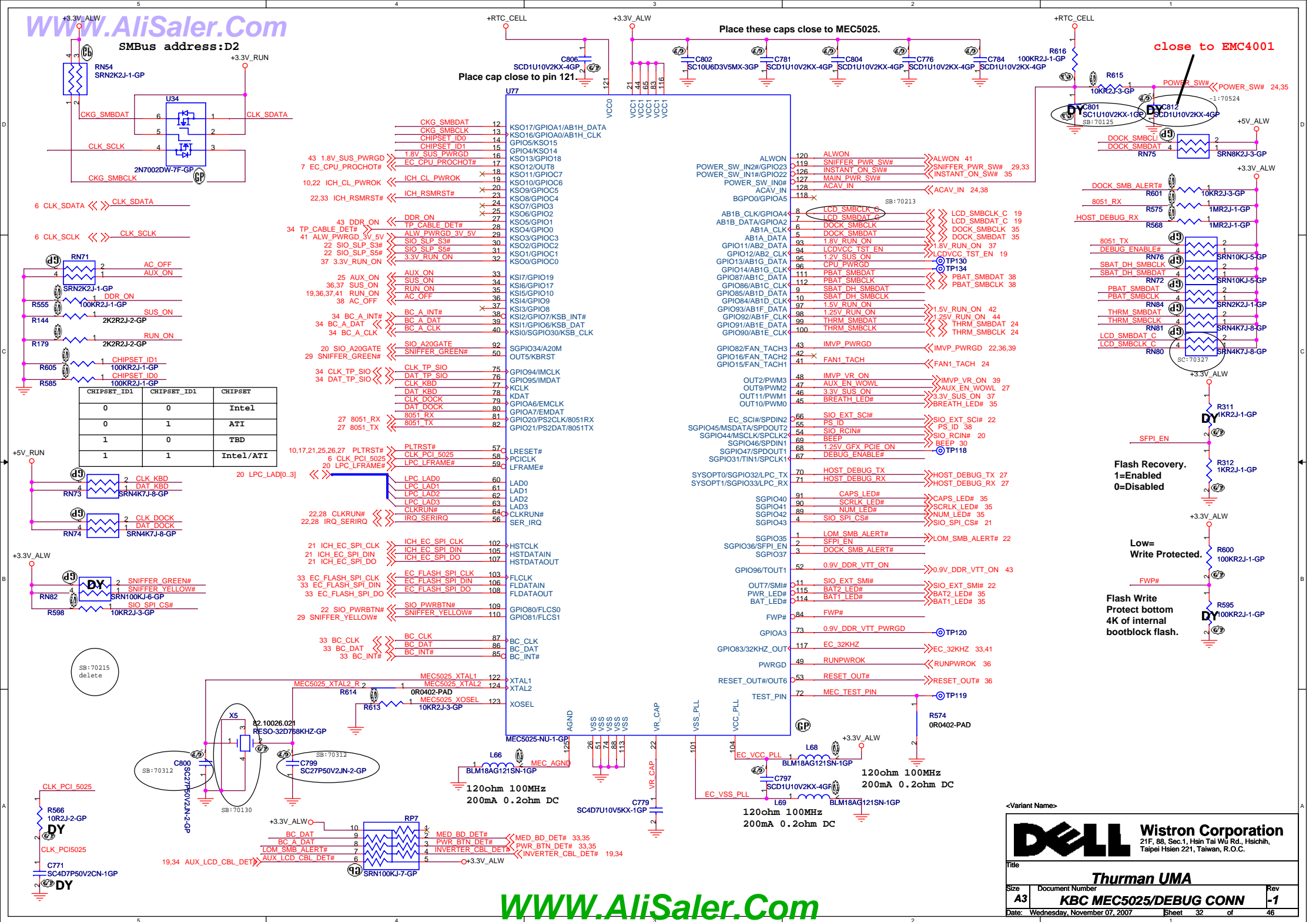
Wednesday, November 07, 2007

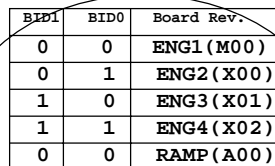
Sheet

31

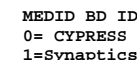
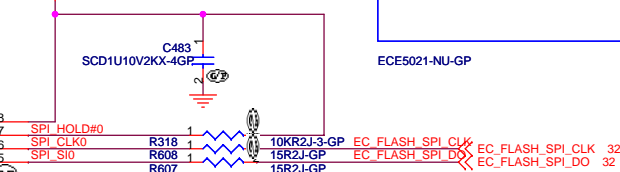
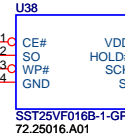
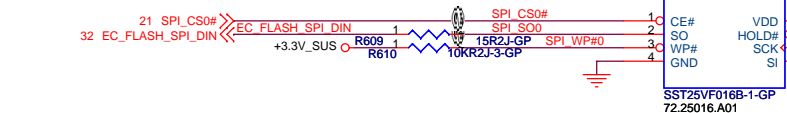
of

Rev





```
0: Intel CPU + Intel Chipset
1: Intel CPU + ATI Chipset
```



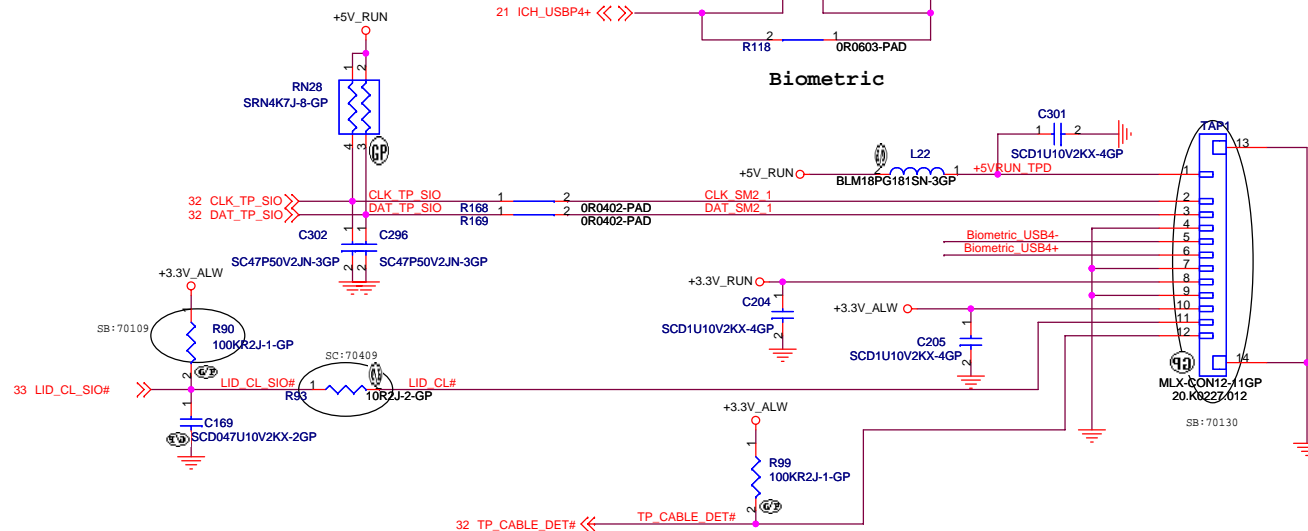
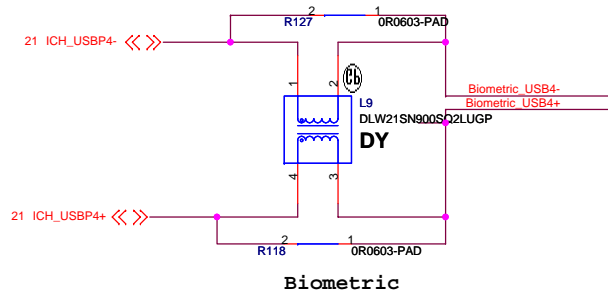
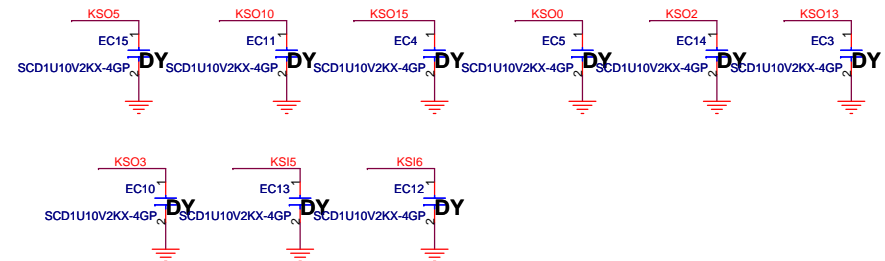
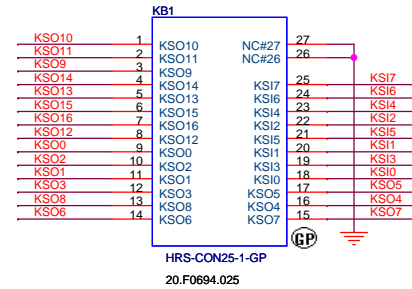
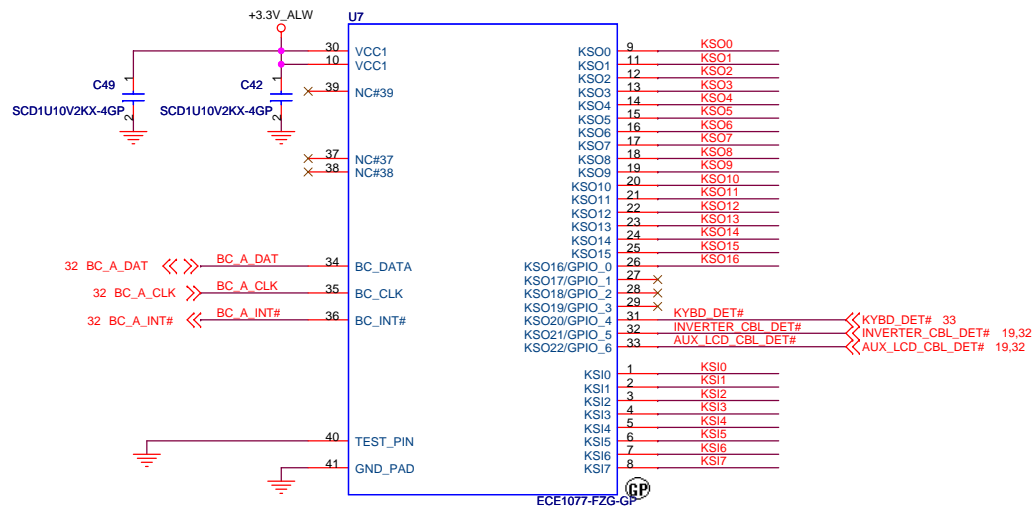
DELL

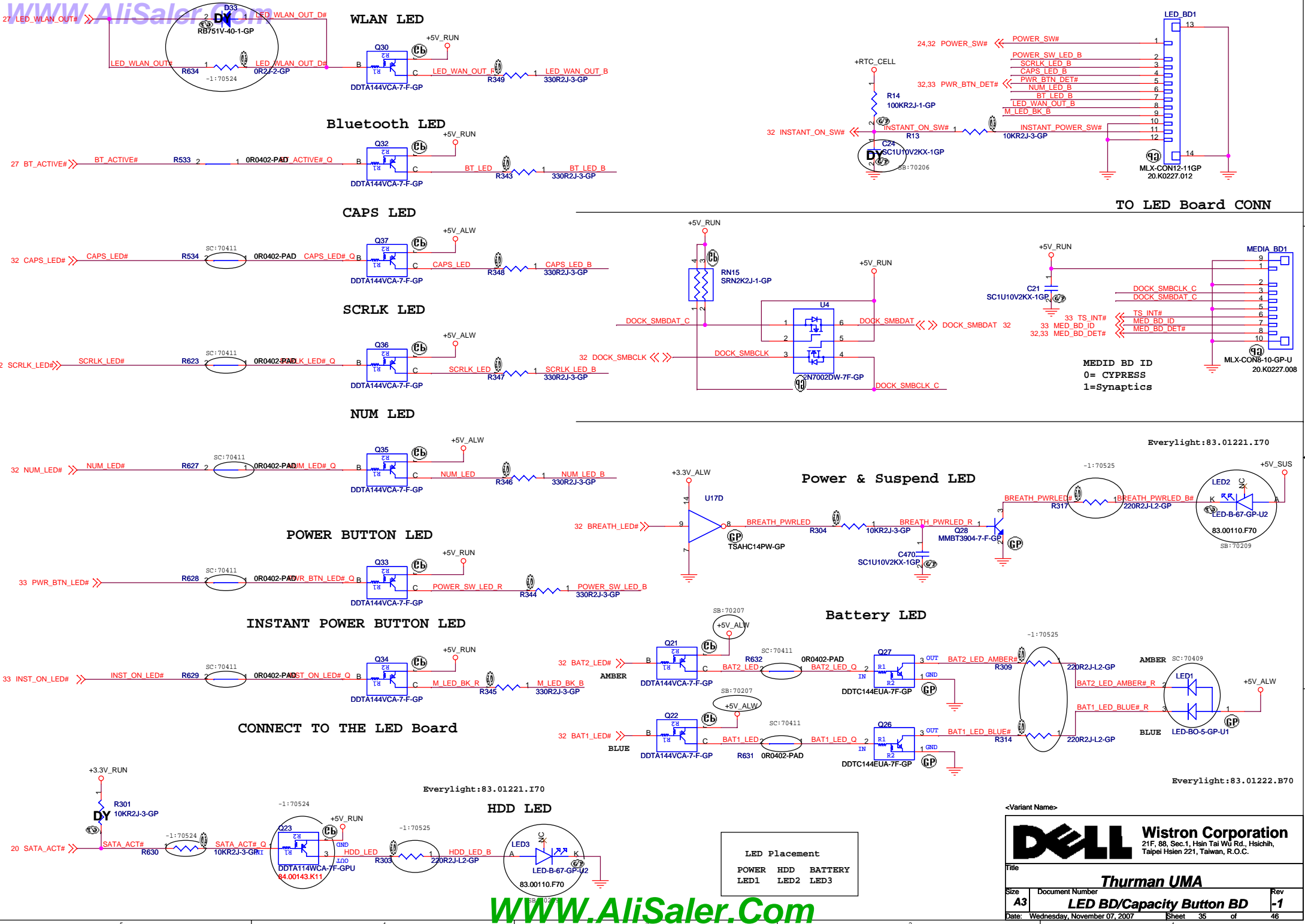
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

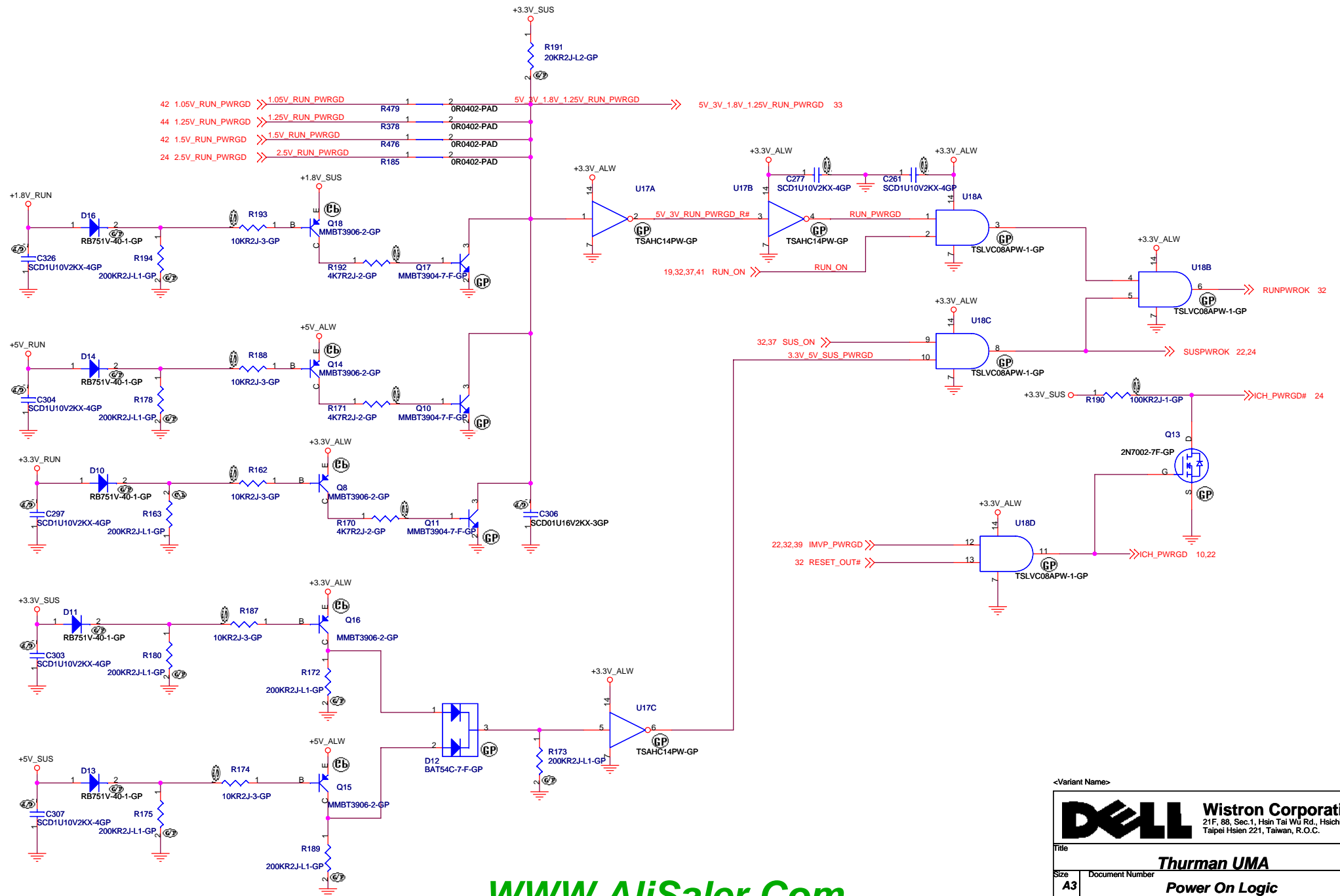
Thurman UMA

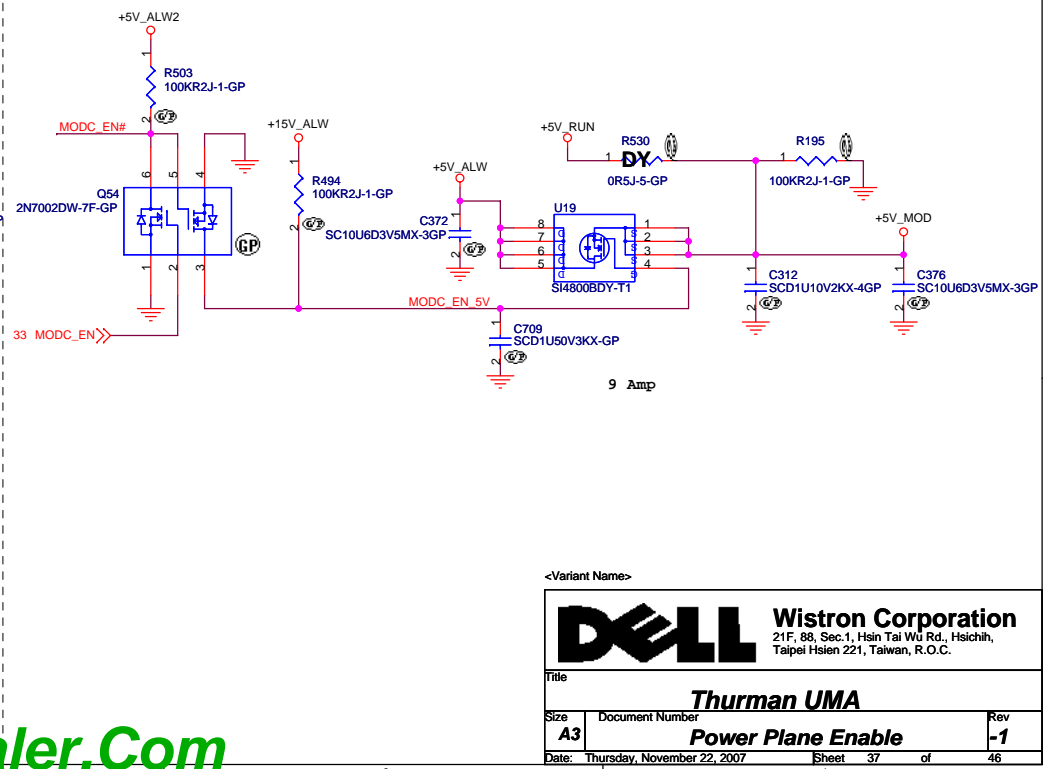
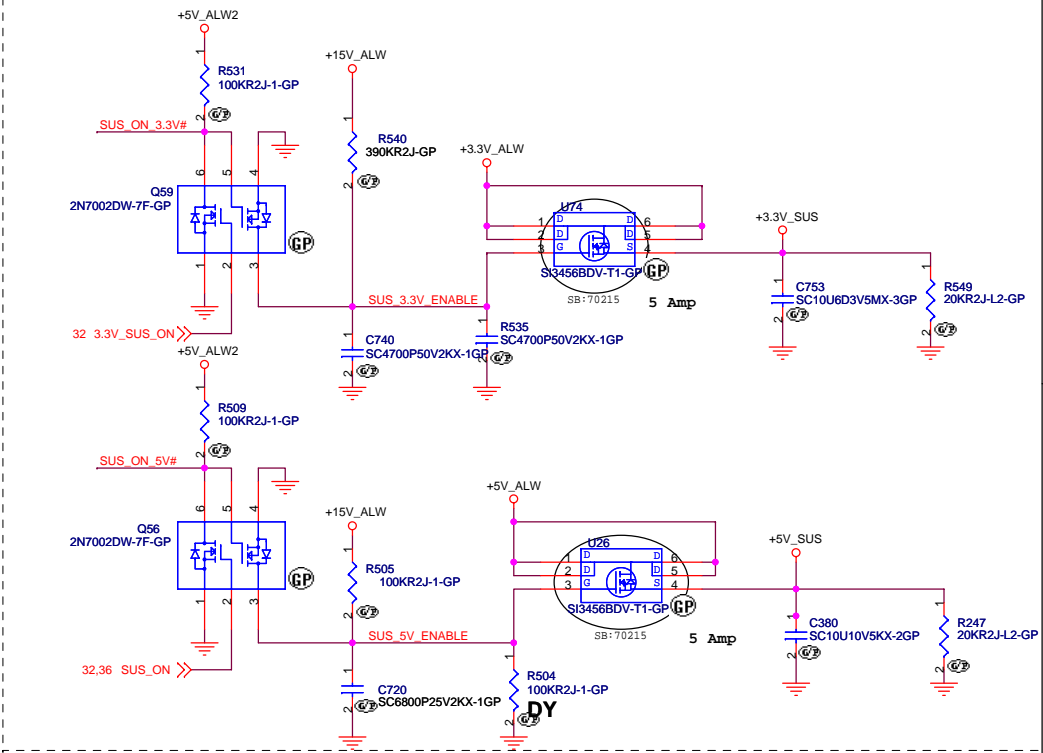
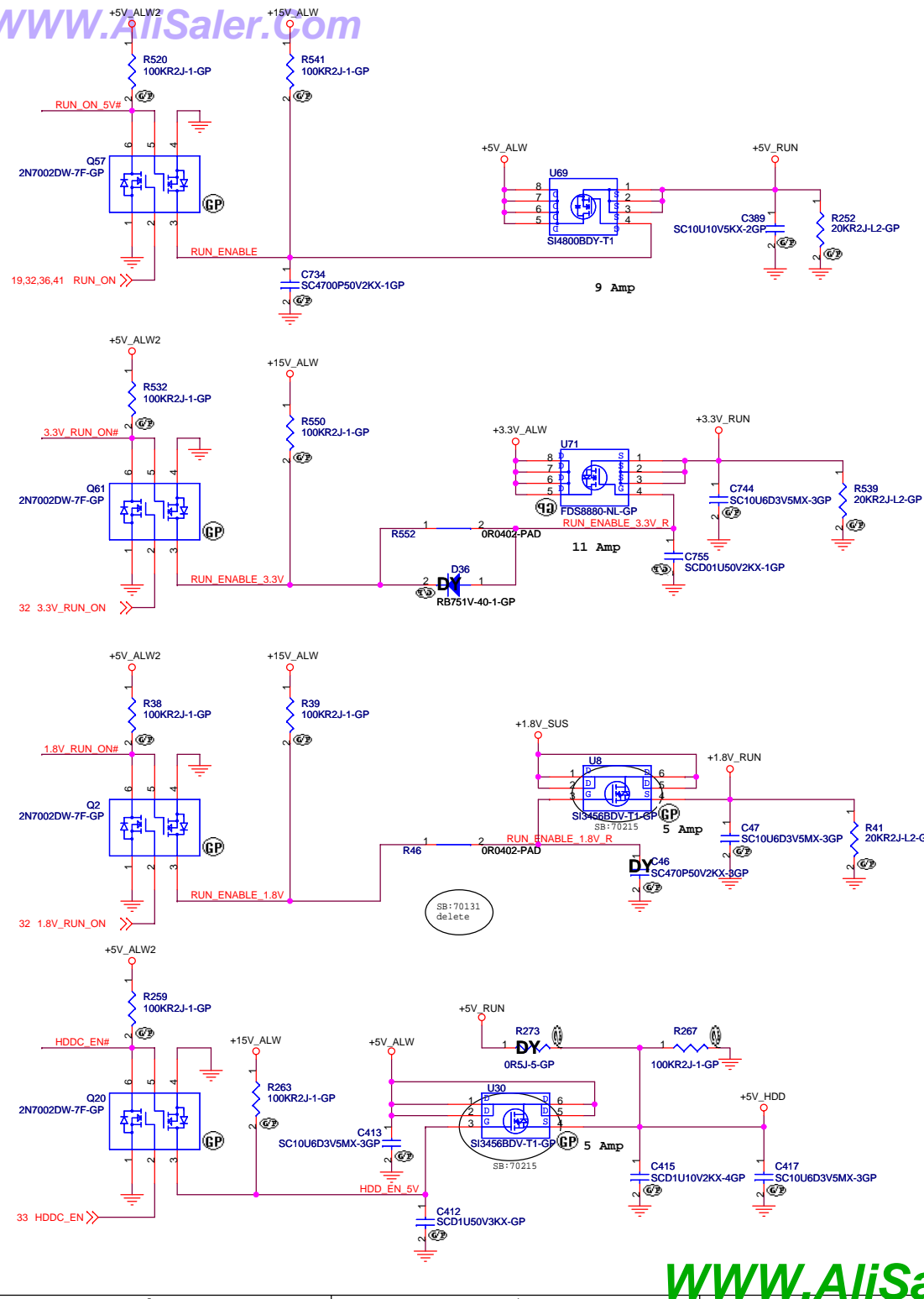
SIO ECE5011/SPI ROM

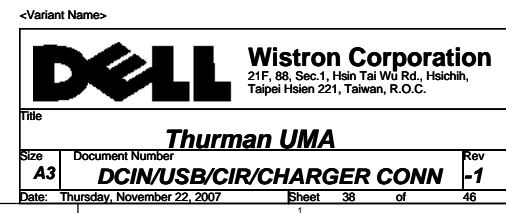
Sheet 33 of 46





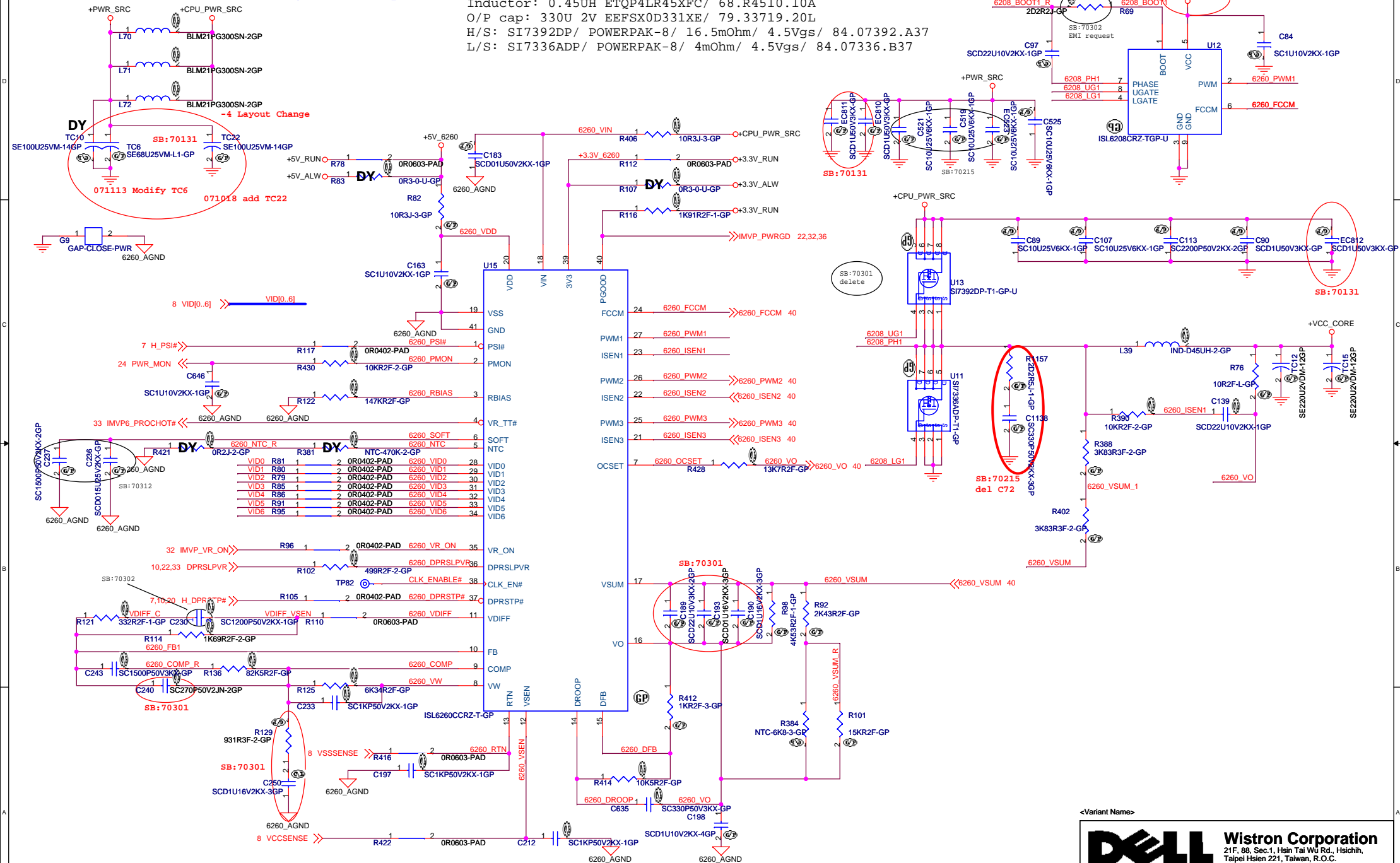






$$\text{OCP design} = 1.2 * I_{\text{peak}}$$

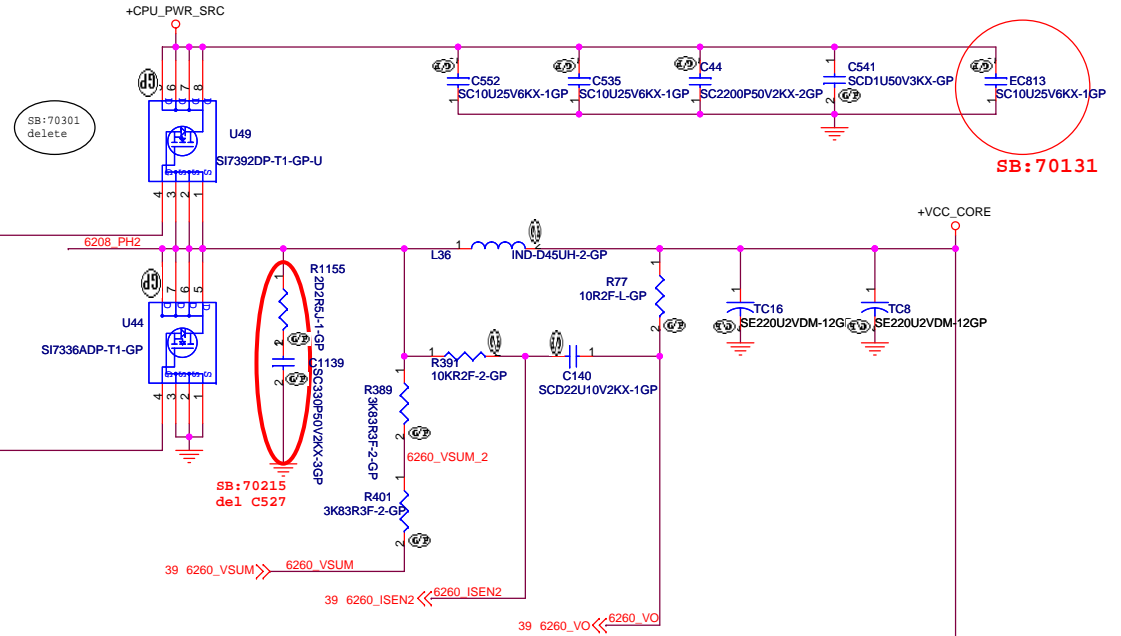
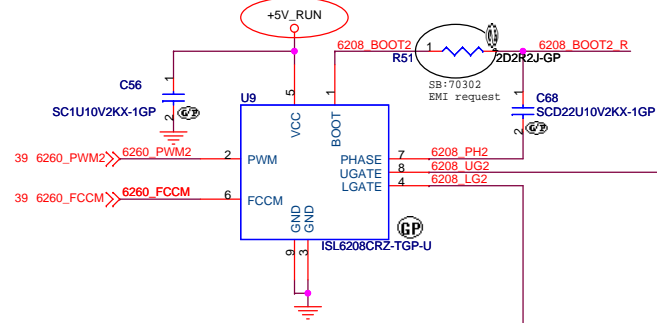
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37



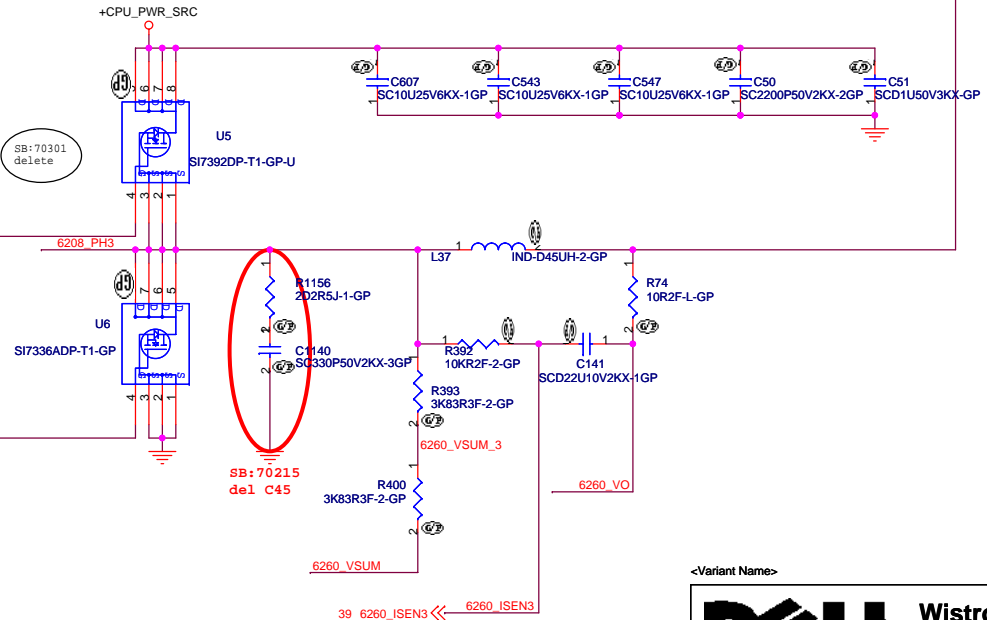
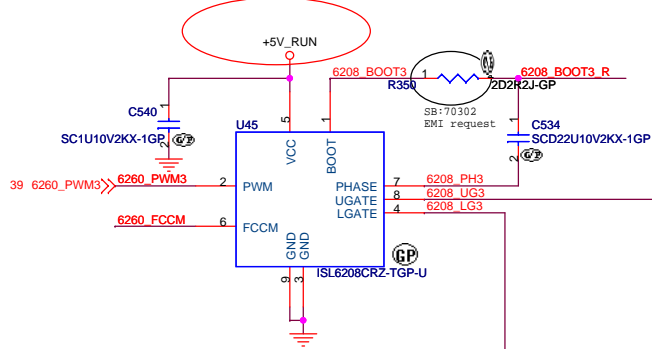
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46

Item 14



Item 14



<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thurman UMA

Size
A3

Document Number

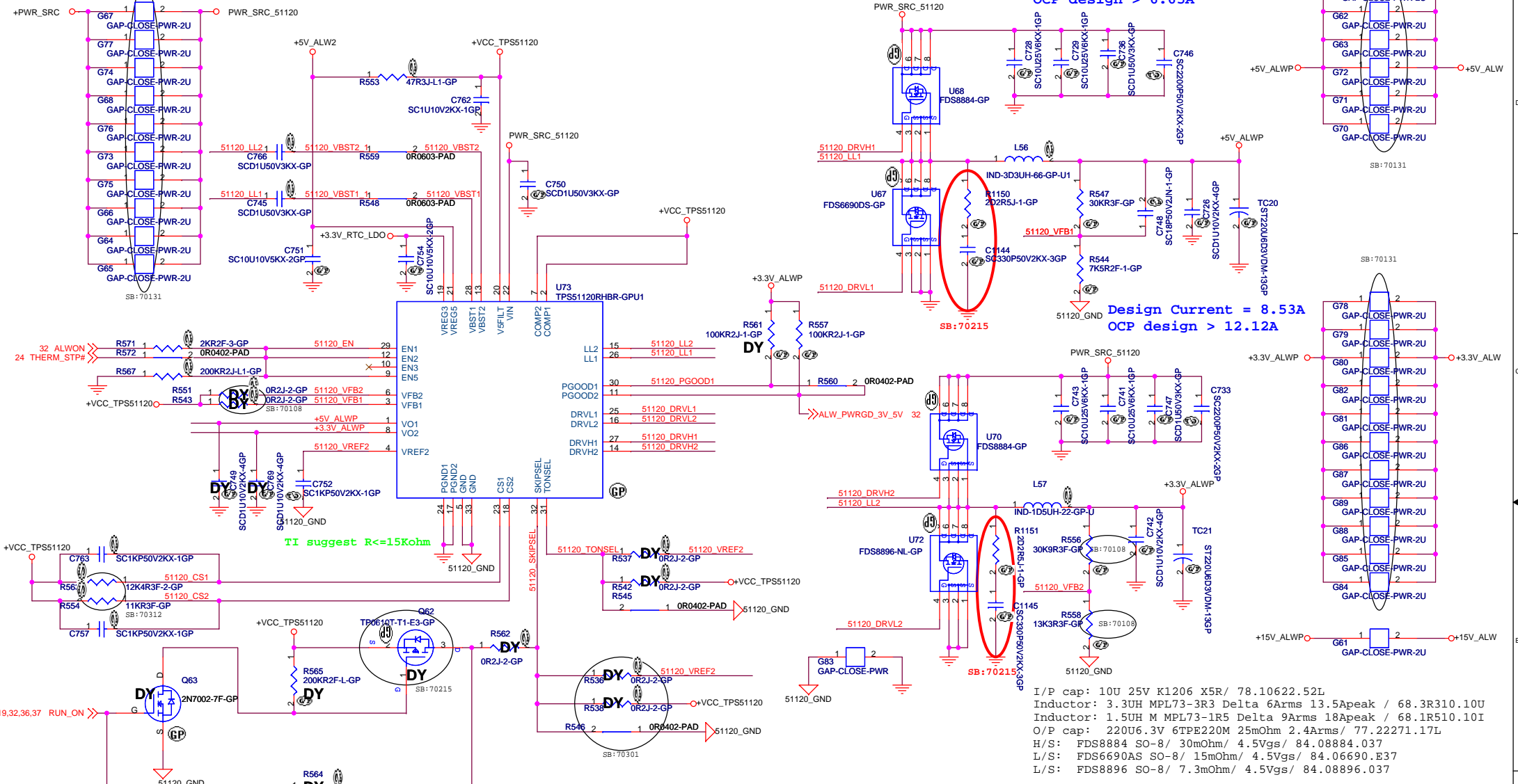
CPU Core-02

Rev

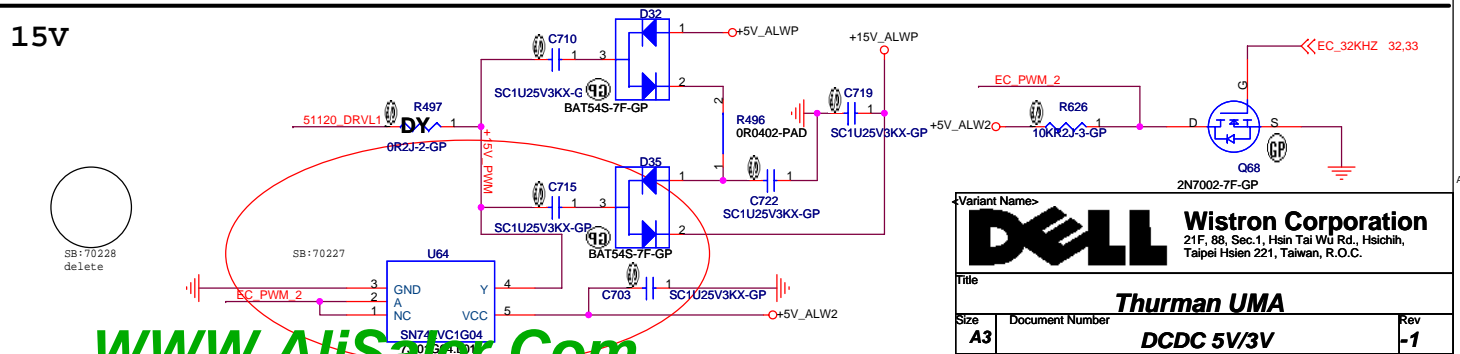
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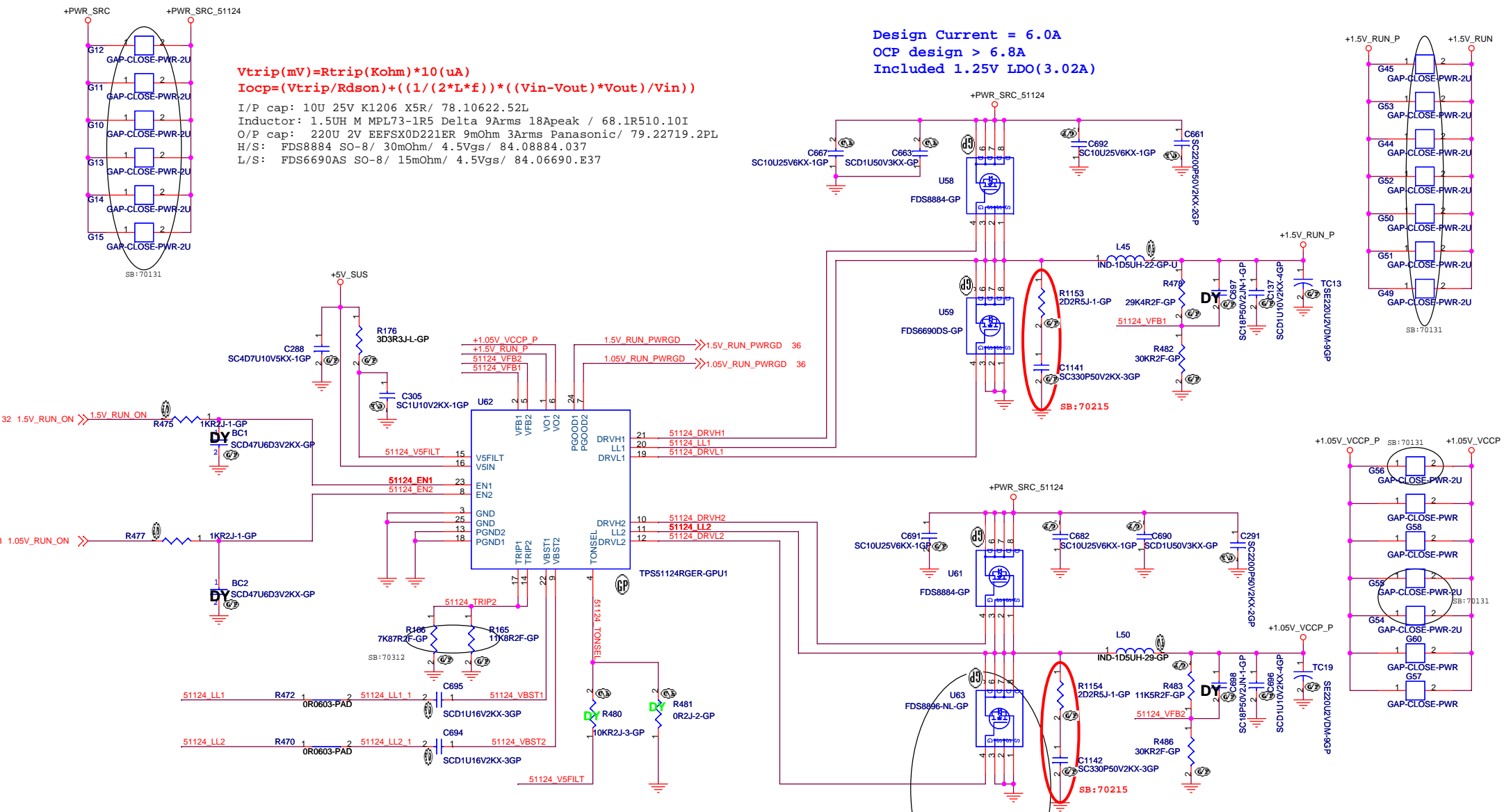
Date: Wednesday, November 07, 2007

Sheet 40 of 46

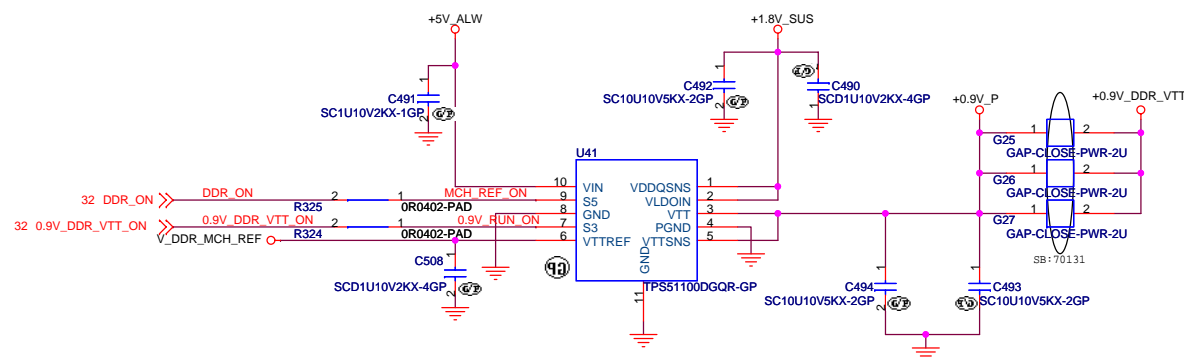
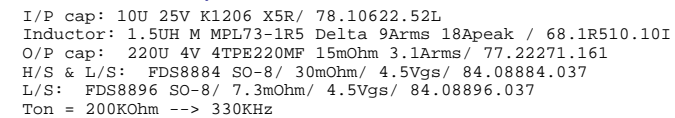


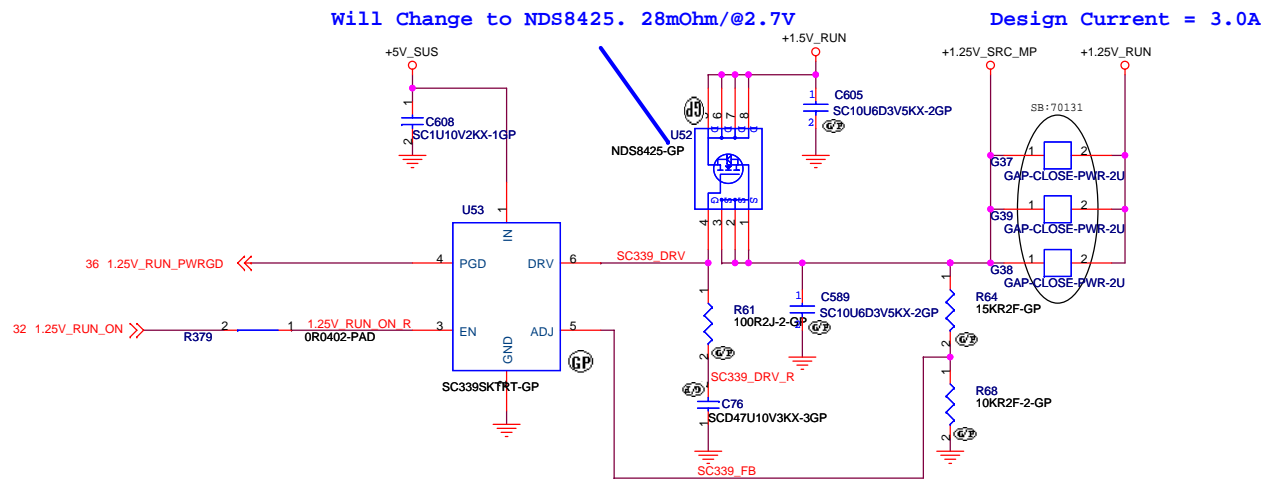
	SKIPSEL	AUTOSKIP	VREF2	PWM	VSFILT
SKIPSEL	SKIPSEL	AUTOSKIP	AUTOSKIP	PWM	PWM
COMP	N/A	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2	
VFB1	N/A	not use	ADJ.	5V Fixed Output	
VFB2	N/A	not use	ADJ.	3.3V Fixed Output	
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON	
EN3,EN5	LDO OFF	not use	LDO ON	VR203 ON	

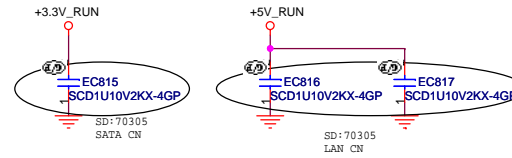
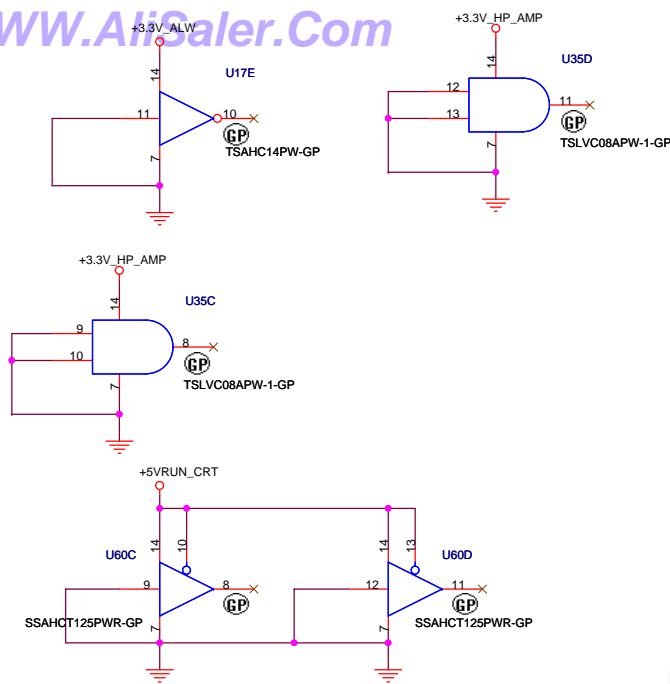




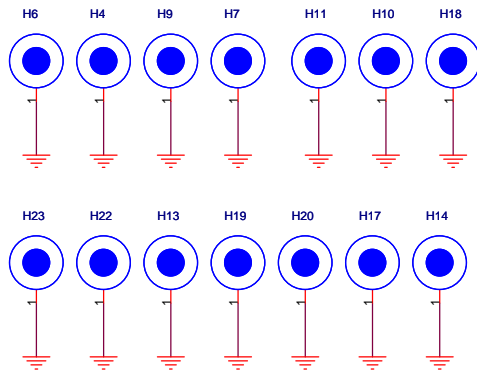
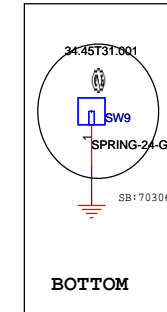
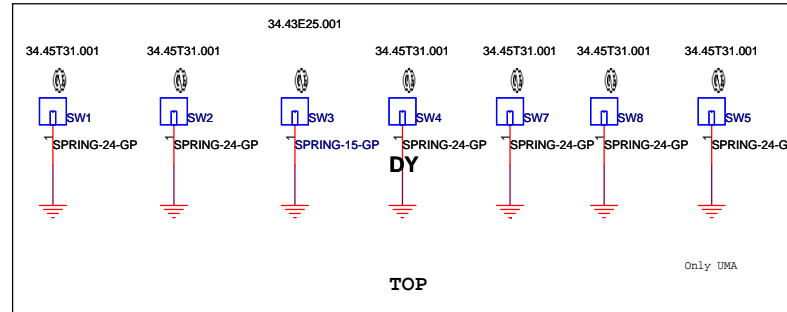
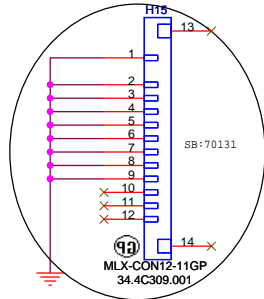
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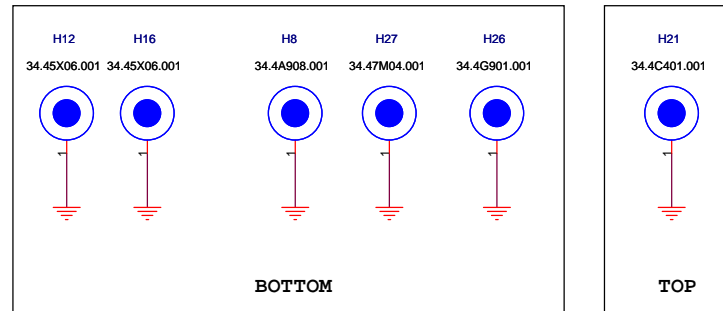




SW3 - 34.43E25.001
 SW9 - 34.49Q02.001
 SW5 - 34.34T31.001 (Only for UMA)
 others-34.45T31.001



H12, H16: 34.45X06.001
 H8: 34.4A908.001
 H27: 34.47M04.001
 H26: 34.4G901.001
 H21: 34.4C401.001



[illegible]