

## V03A DIS/UMA BLOCK DIAGRAM

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : IN3  
LAYER 7 : GND  
LAYER 8 : BOT

DDRIII-SODIMM1  
A 00  
PAGE 16

DDRIII 1333 MT/s

DDRIII-SODIMM2  
A 01  
PAGE 17

DDRIII 1333 MT/s

**CPU**  
Sandy Bridge 45W  
PGA 989  
PAGE 4~8

FDI LINK  
2.5GT /s

DMI LINK  
2.5GT /s

PCIEx16

**Nvidia**  
N12P-GE (128bit)  
29mm X 29mm  
BGA 969  
PAGE 18~22

DDR3 1GB/2GB  
128Mx16bitx8  
PG 23,24

HDMI Switch  
PAGE 26

HDMI CONN  
PAGE 26

LCD CONN  
1600 x 900 (HD) PAGE 25

Re-Driver  
SN75LVCP412RTJR  
PAGE 27

E-SATA  
PAGE 27

SATA4 300MB /S

SATA -HDD  
PAGE 28

SATA0 300MB /S

ODD  
PAGE 28

SATA1 300MB /S

3-axis Fall Sensor  
PAGE 28

SMBUS

Mobile Intel  
Series 6 Chipset

**PCH**

HM67  
Couger Point

BGA 989  
25 mm X 25 mm  
PAGE 9~15

iGFX Interfaces

INT HDMI

INT Dual CHANNEL LVDS

ESATA+USB2.0  
PAGE 27

Camera  
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Card Reader  
RTS5128-GR  
PAGE 29

FP  
PAGE 35

Touch Screen  
PAGE 34

USB2.0

USB[0]

USB[11]

USB[8]

USB[10]

USB[12]

USB[8]

Express Card  
R5538D001 PAGE 02

**EXP Board**

**LED Board**

**PB Board**

**TP Board**

**HotKey Board**

Charger	PAGE 42
3/5V	PAGE 43
1.5V_SUS/0.75V_DDR	PAGE 44
Batt/DC-IN	PAGE 41
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Keyboard Conn.  
PAGE 35

Touch Pad  
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LED  
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KBC  
ITE 8518  
PAGE 30

PWM FAN  
& Thermal  
PAGE 38

SPI ROM  
512kB  
PAGE 34

SPI  
SPI ROM  
4MB  
PAGE 34

25MHz

32.768KHz

Subwoofer  
MAX9759ETE  
PAGE 33

Audio Codec  
ALC 269Q-VB6-GR  
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Speaker  
PAGE 32

Jack  
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CRT Board  
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WLAN  
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USB3.0 Controller  
PAGE 06

LAN  
Realtek  
RTL8111E-VB-GR  
PAGE 09

BlueTooth  
PAGE 05

USB3.0 Ports x2  
PAGE 07

RJ45  
PAGE 10

USB Port x1  
PAGE 08

power State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+VCHGR +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+5V_SUS +3.3V_SUS +1.5V_SUS +1.5V_CPU +DDR_VTTREF +3.3V_LAN (for R03)	+VCC_CORE +VCC_GFX_CORE +1.05V_PCH +5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +VCCSA +0.75V_DDR_VTT +LCDVCC +VCC_DGFX_CORE	
S0	ON	ON	ON	ON	ON	
S1						
S3	ON	ON	ON	ON	OFF	
S4/S5 AC	ON	ON				
S4/S5 DC Only	ON		ON	OFF	OFF	
AC/DC No Exist	ON	OFF	OFF	OFF	OFF	

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								



+1.05V\_PCH

R309 24.9/F\_4 EDP\_COMP

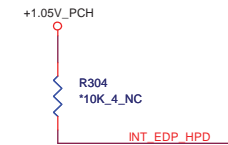
eDP\_COMP10 and ICOMPO signals should be shorted near balls and routed within 500 mils

+1.05V\_PCH

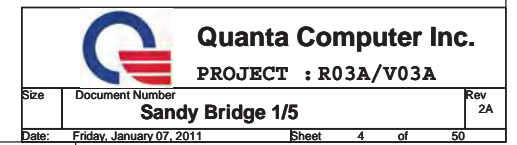
R55 24.9/F\_4 PEG\_COMP

PEG\_ICOMPI and RCOMPO signals should be routed within 500 mils

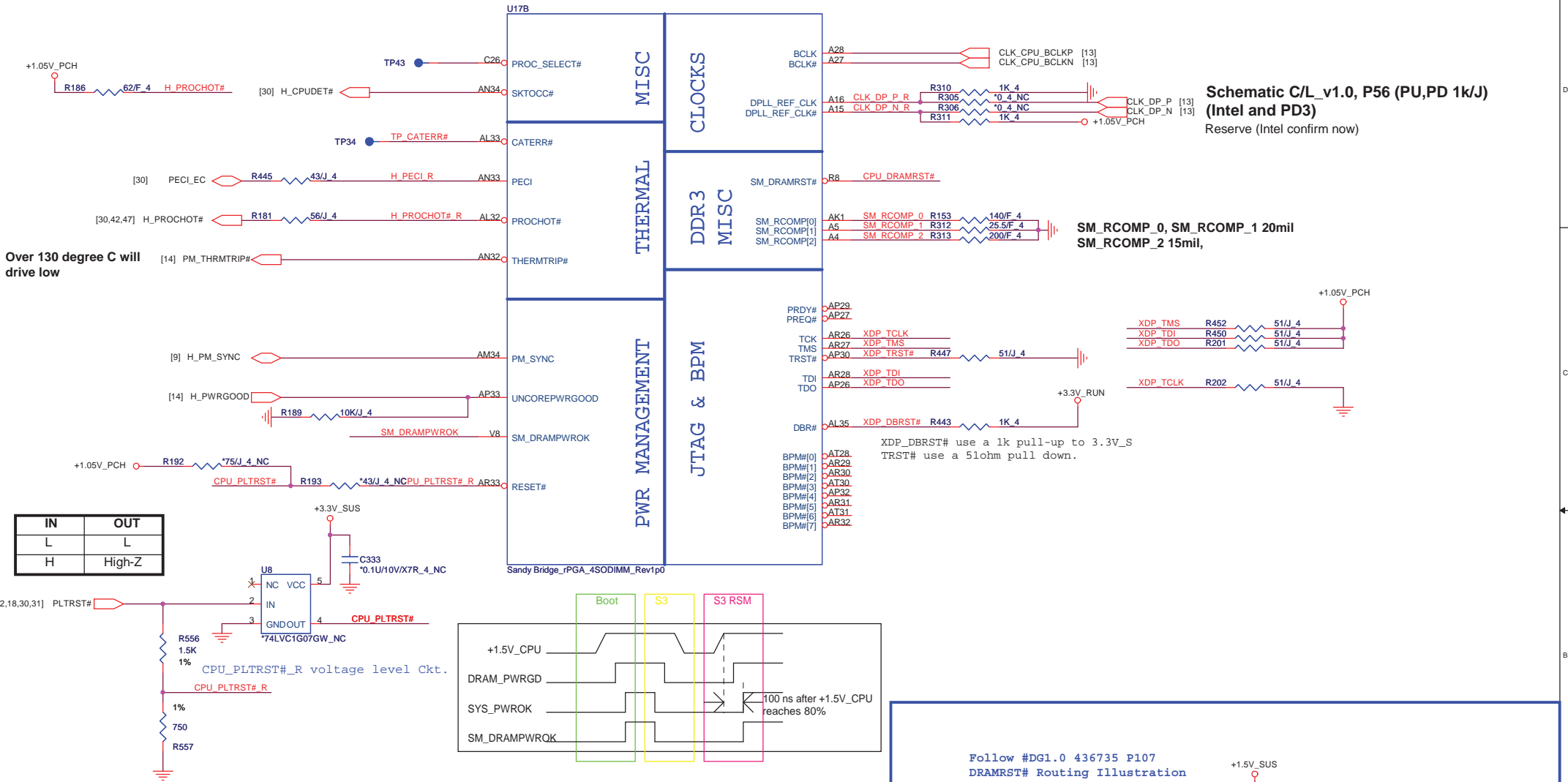
PEG\_ICOMPO signals should be routed within 500 mils



This signal can be left as no connect if entire eDP interface is disabled.



# Sandy Bridge Processor (CLK,MISC,JTAG)

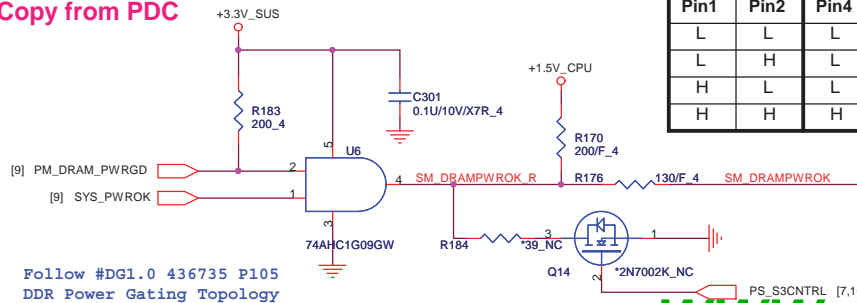


Change OD part same with PDC

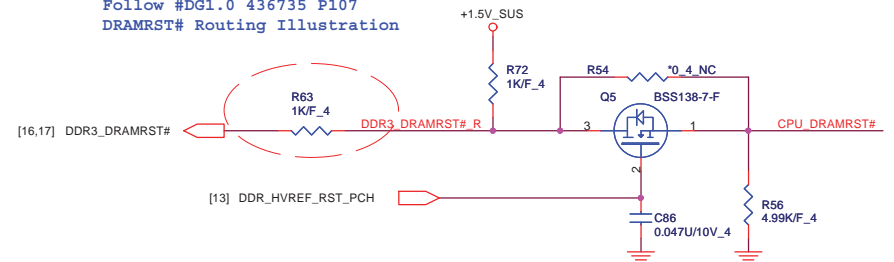
Copy from PDC

R8239, R8241 change to 5%

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H



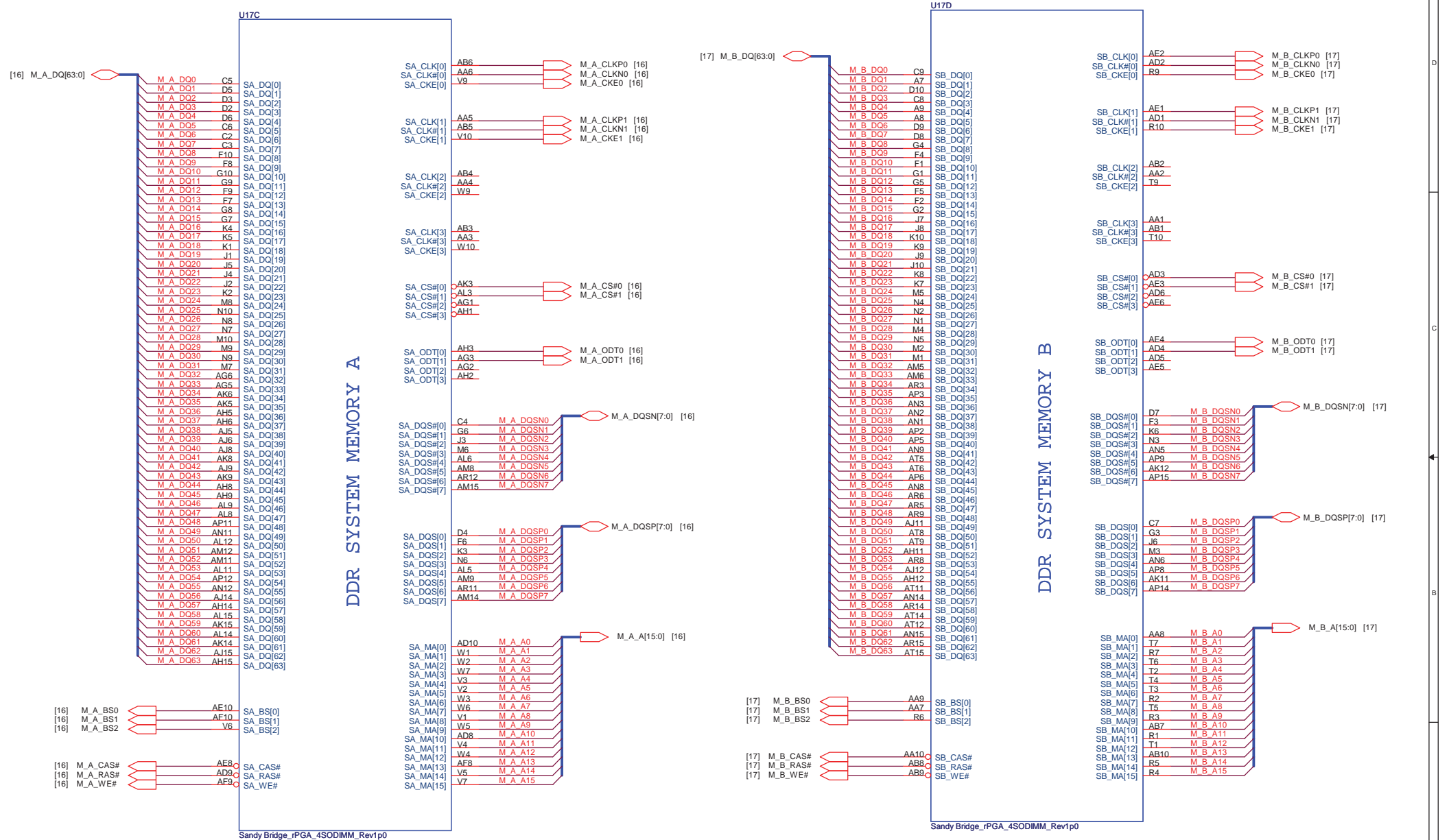
Follow #DG1.0 436735 P107  
DRAMRST# Routing Illustration



Quanta Computer Inc.

PROJECT : R03A/V03A

## Sandy Bridge Processor (DDR3)



Quanta Computer Inc.

PROJECT : R03A/V03A

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	Sandy Bridge 3/5	2A
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# Sandy Bridge Processor (POWER)

## POWER

**CPU Core Power**  
SNB 45W:95A  
470uF/4mohm x 4  
22uF x 16  
10uF x 10

C541 C501 C536 C516 C525 C482 C497  
10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8

C495 C507 C551 C178 C496 C212 C508  
10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8

C163 C205 C123 C142 C194  
10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8

C156 C170 C136 C546 C175  
10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8 10u6.3V\_8

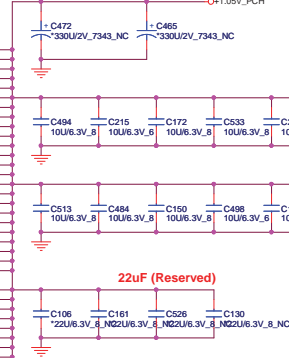
C211 C478 C491 C213 C210  
22u6.3V\_8 22u6.3V\_8 22u6.3V\_8 22u6.3V\_8 22u6.3V\_8

CORE SUPPLY

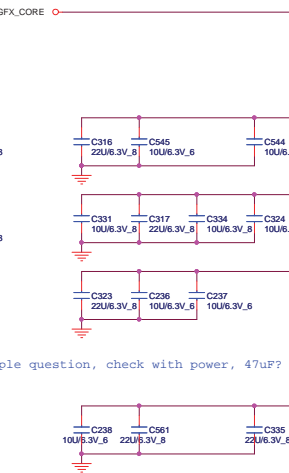
SVID

SENSE LINES

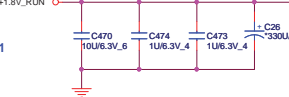
**CPU VTT**  
SNB 45W:8.5A  
330uF/6mohm x 2  
22uF x 12  
22uF x 7 (Non-stuff)



**CPU VGTT**  
SNB 45W:22A  
22uF x 12



**CPU VCCPL**  
SNB 45W:3A  
330uF/7mohm x 1  
10uF x 1  
1uF x 2



# Sandy Bridge Processor (GRAPHIC POWER)

## POWER

GRAPHICS

1.8V RAIL

MISC

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

VCCSA\_CORE

VCCSA\_VID0

VCCSA\_VID1

VCCSA\_VID2

VCCSA\_VID3

VCCSA\_VID4

VCCSA\_VID5

VCCSA\_VID6

VCCSA\_VID7

VCCSA\_VID8

VCCSA\_VID9

VCCSA\_VID10

VCCSA\_VID11

VCCSA\_VID12

VCCSA\_VID13

VCCSA\_VID14

VCCSA\_VID15

VCCSA\_VID16

VCCSA\_VID17

VCCSA\_VID18

VCCSA\_VID19

VCCSA\_VID20

VCCSA\_VID21

VCCSA\_VID22

VCCSA\_VID23

VCCSA\_VID24

VCCSA\_VID25

VCCSA\_VID26

VCCSA\_VID27

VCCSA\_VID28

VCCSA\_VID29

VCCSA\_VID30

VCCSA\_VID31

VCCSA\_VID32

VCCSA\_VID33

VCCSA\_VID34

VCCSA\_VID35

VCCSA\_VID36

VCCSA\_VID37

VCCSA\_VID38

VCCSA\_VID39

VCCSA\_VID40

VCCSA\_VID41

VCCSA\_VID42

VCCSA\_VID43

VCCSA\_VID44

VCCSA\_VID45

VCCSA\_VID46

VCCSA\_VID47

VCCSA\_VID48

VCCSA\_VID49

VCCSA\_VID50

VCCSA\_VID51

VCCSA\_VID52

VCCSA\_VID53

VCCSA\_VID54

VCCSA\_VID55

VCCSA\_VID56

VCCSA\_VID57

VCCSA\_VID58

VCCSA\_VID59

VCCSA\_VID60

VCCSA\_VID61

VCCSA\_VID62

VCCSA\_VID63

VCCSA\_VID64

VCCSA\_VID65

VCCSA\_VID66

VCCSA\_VID67

VCCSA\_VID68

VCCSA\_VID69

VCCSA\_VID70

VCCSA\_VID71

VCCSA\_VID72

VCCSA\_VID73

VCCSA\_VID74

VCCSA\_VID75

VCCSA\_VID76

VCCSA\_VID77

VCCSA\_VID78

VCCSA\_VID79

VCCSA\_VID80

VCCSA\_VID81

VCCSA\_VID82

VCCSA\_VID83

VCCSA\_VID84

VCCSA\_VID85

VCCSA\_VID86

VCCSA\_VID87

VCCSA\_VID88

VCCSA\_VID89

VCCSA\_VID90

VCCSA\_VID91

VCCSA\_VID92

VCCSA\_VID93

VCCSA\_VID94

VCCSA\_VID95

VCCSA\_VID96

VCCSA\_VID97

VCCSA\_VID98

VCCSA\_VID99

VCCSA\_VID100

VCCSA\_VID101

VCCSA\_VID102

VCCSA\_VID103

VCCSA\_VID104

VCCSA\_VID105

VCCSA\_VID106

VCCSA\_VID107

VCCSA\_VID108

VCCSA\_VID109

VCCSA\_VID110

VCCSA\_VID111

VCCSA\_VID112

VCCSA\_VID113

VCCSA\_VID114

VCCSA\_VID115

VCCSA\_VID116

VCCSA\_VID117

VCCSA\_VID118

VCCSA\_VID119

VCCSA\_VID120

VCCSA\_VID121

VCCSA\_VID122

VCCSA\_VID123

VCCSA\_VID124

VCCSA\_VID125

VCCSA\_VID126

VCCSA\_VID127

VCCSA\_VID128

VCCSA\_VID129

VCCSA\_VID130

VCCSA\_VID131

VCCSA\_VID132

VCCSA\_VID133

VCCSA\_VID134

VCCSA\_VID135

VCCSA\_VID136

VCCSA\_VID137

VCCSA\_VID138

VCCSA\_VID139

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VCCSA\_VID141

VCCSA\_VID142

VCCSA\_VID143

VCCSA\_VID144

VCCSA\_VID145

VCCSA\_VID146

VCCSA\_VID147

VCCSA\_VID148

VCCSA\_VID149

VCCSA\_VID150

VCCSA\_VID151

VCCSA\_VID152

VCCSA\_VID153

VCCSA\_VID154

VCCSA\_VID155

VCCSA\_VID156

VCCSA\_VID157

VCCSA\_VID158

VCCSA\_VID159

VCCSA\_VID160

VCCSA\_VID161

VCCSA\_VID162

VCCSA\_VID163

VCCSA\_VID164

VCCSA\_VID165

VCCSA\_VID166

VCCSA\_VID167

VCCSA\_VID168

VCCSA\_VID169

VCCSA\_VID170

VCCSA\_VID171

VCCSA\_VID172

VCCSA\_VID173

VCCSA\_VID174

VCCSA\_VID175

VCCSA\_VID176

VCCSA\_VID177

VCCSA\_VID178

VCCSA\_VID179

VCCSA\_VID180

VCCSA\_VID181

VCCSA\_VID182

VCCSA\_VID183

VCCSA\_VID184

VCCSA\_VID185

VCCSA\_VID186

VCCSA\_VID187

VCCSA\_VID188

VCCSA\_VID189

VCCSA\_VID190

VCCSA\_VID191

VCCSA\_VID192

VCCSA\_VID193

VCCSA\_VID194

VCCSA\_VID195

VCCSA\_VID196

VCCSA\_VID197



WWW.AliSaler.Com



Sandy Bridge\_rPGA\_4SODIMM\_Rev1p0

2	1
---	---



For rPGA socket, RSVD59 pin should be left NC

## CFG[6:5] (PCIe Port Bifurcation Straps)

```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

The CFG signals have a default value of '1' if not terminated on the board.

CFG2 R199 1K/F\_4



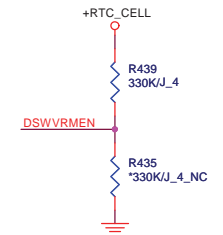
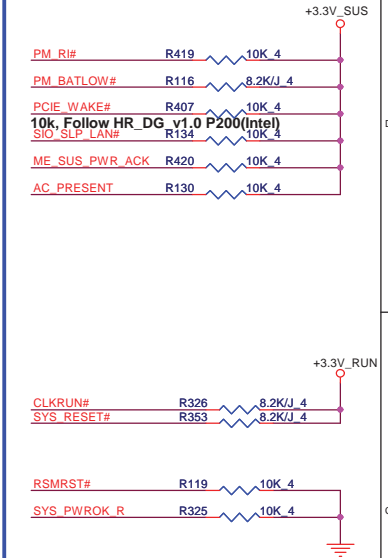
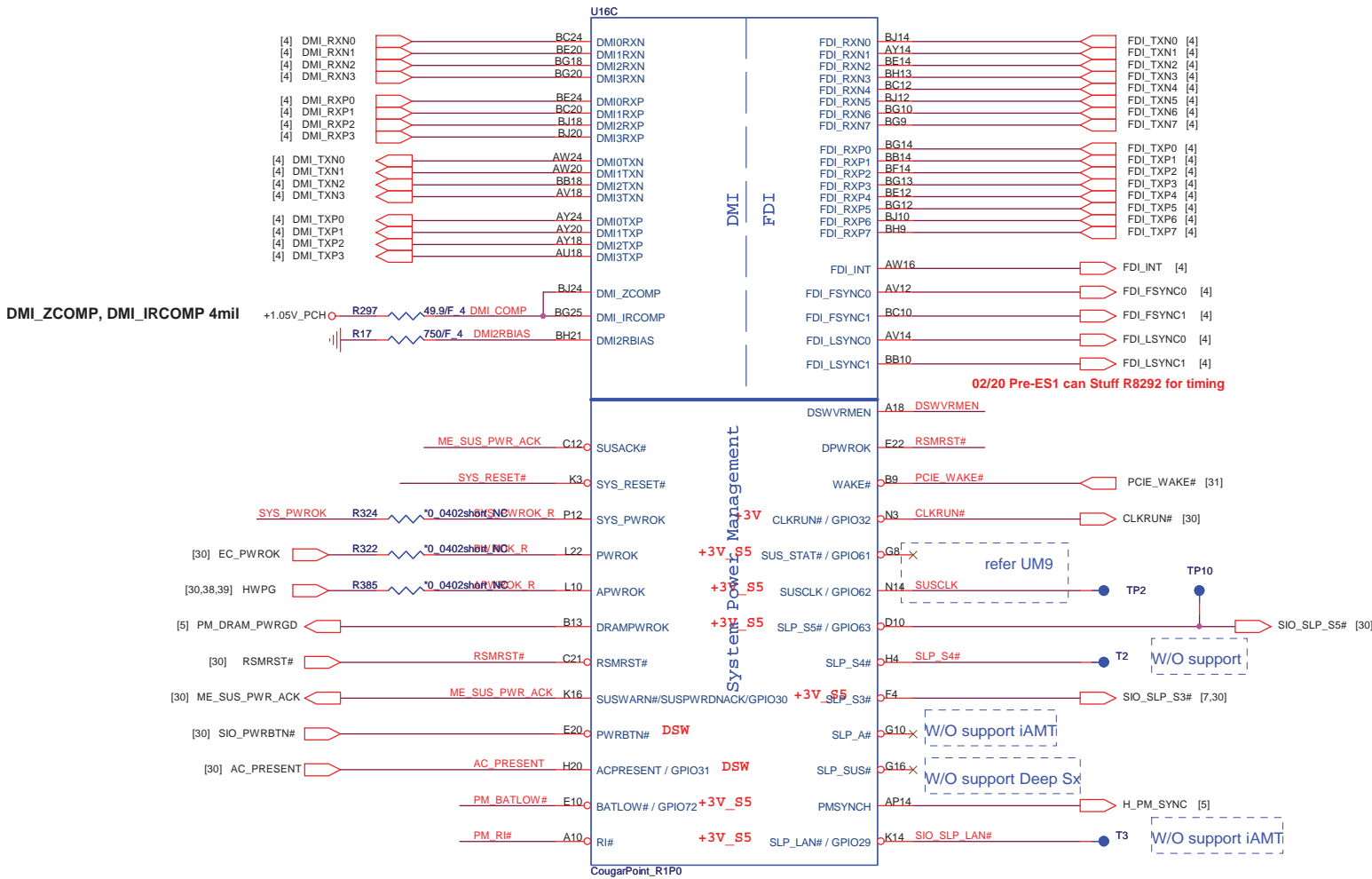
PROJECT : R03A/V03A

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## Cougar Point (DMI, FDI, PM)

## PCH Pull-high/low(CLG)

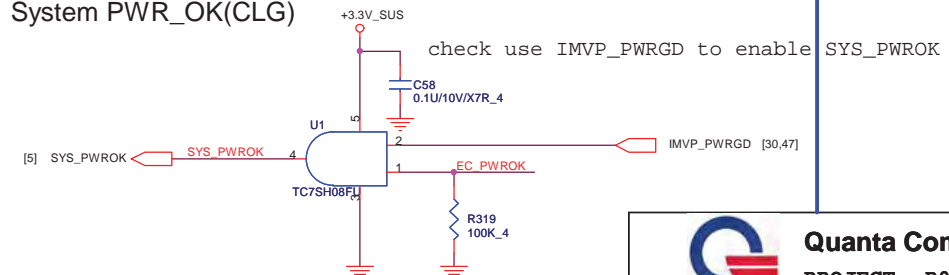


On Die DSW VR Enable

High = Enable (Default)

Low = Disable

## System PWR\_OK(CLG)

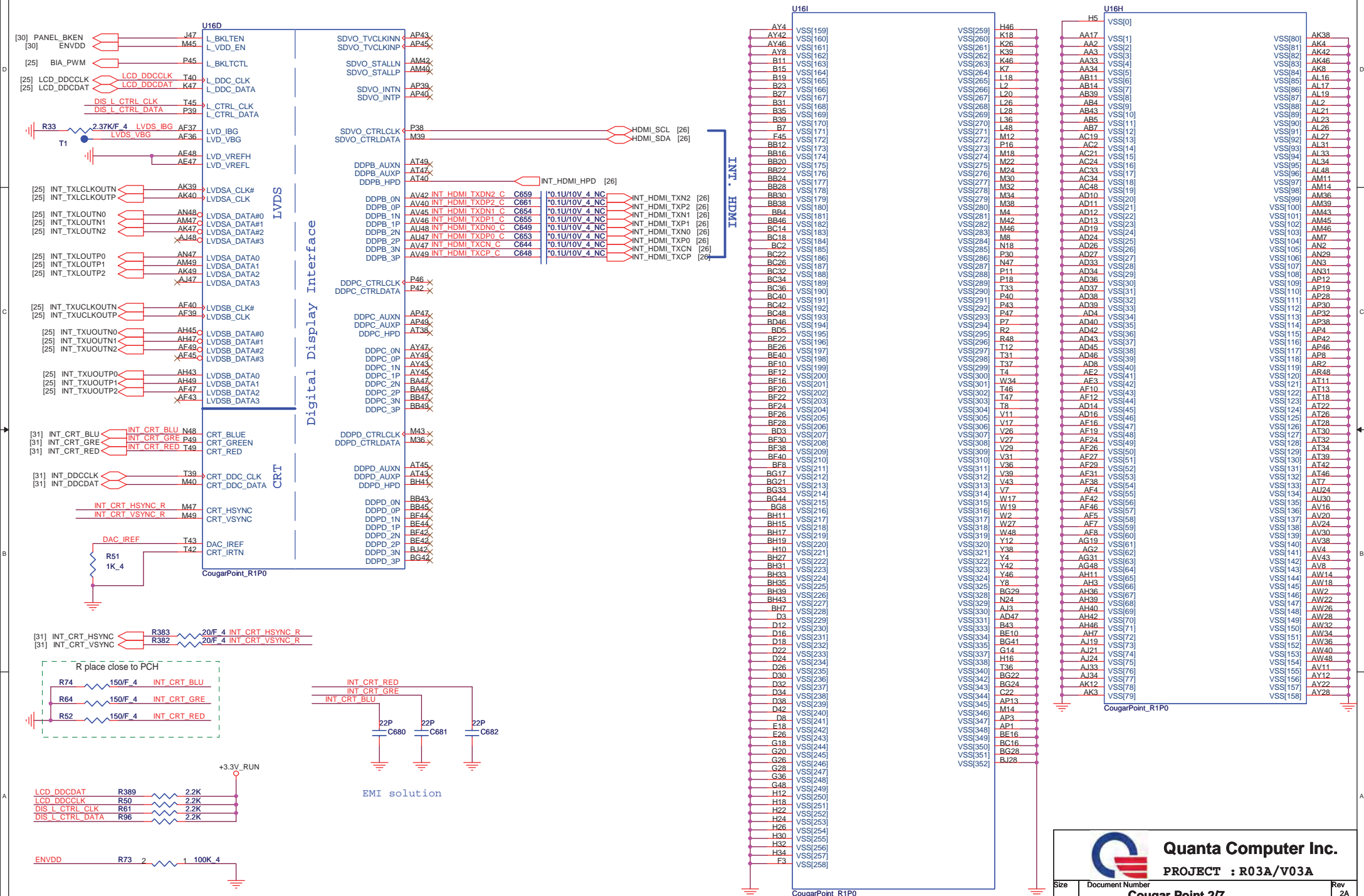


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PROJECT : R03A/V03A

## Cougar Point (LVDS,DDI)

## Cougar Point (GND)



The schematic diagram illustrates the RTC circuit. A +RTC\_CELL input is connected to a network of resistors and capacitors. Resistors R121 and R132 are both 20K. The network is connected to RTC\_RST# and SRTC\_RST# signals. Capacitors C162 and C174 are both 1uF, 6.3V/X5R, connected to ground.

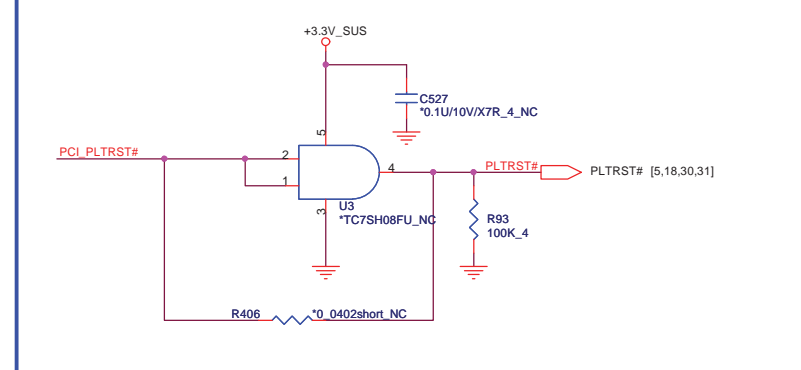


The schematic diagram illustrates the RTC circuit. A +RTC\_CELL input is connected to a network of resistors and capacitors. Resistors R121 and R132 are both 20K. The network is connected to RTC\_RST# and SRTC\_RST# signals. Capacitors C162 and C174 are both 1uF, 6.3V/X5R, connected to ground.

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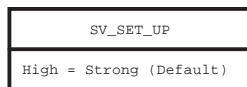
The schematic diagram illustrates the RTC circuit. A +RTC\_CELL input is connected to a network of resistors and capacitors. Resistors R121 and R132 are both 20K. The network is connected to RTC\_RST# and SRTC\_RST# signals. Capacitors C162 and C174 are both 1uF, 6.3V/X5R, connected to ground.

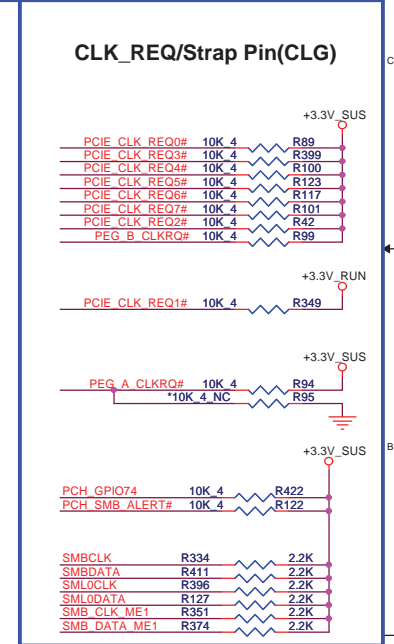
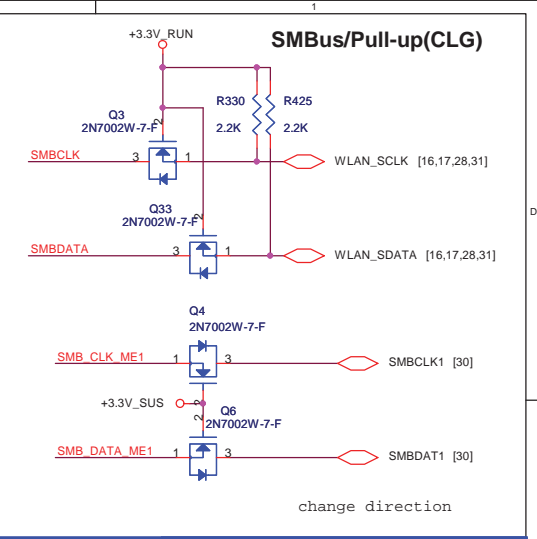
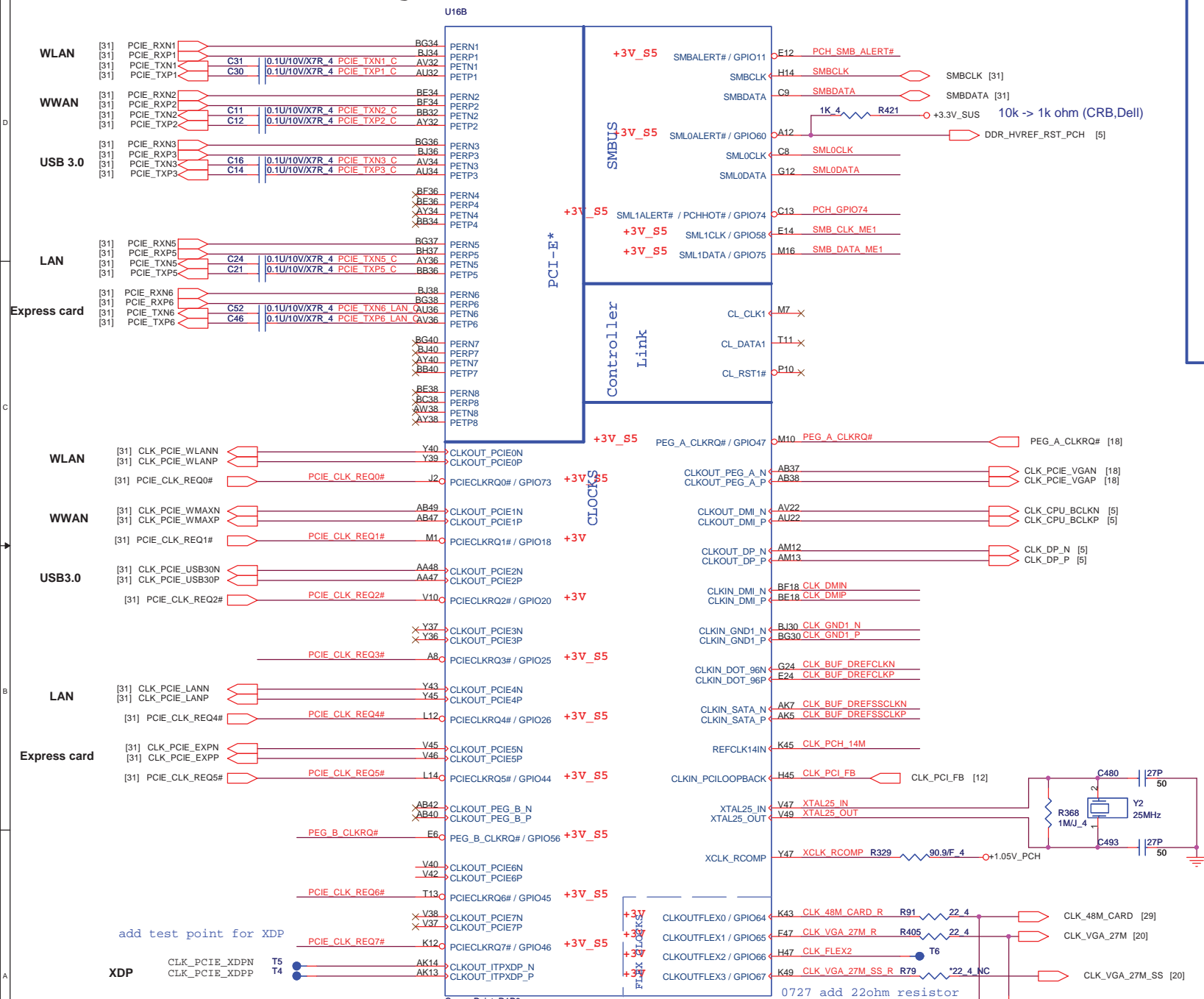
**PLTRST#(CLG)**



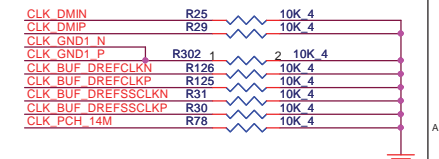
1000

DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm
<p>CheckList_1.0 p58; HR_v1.0 p450</p> <p>follow CheckList_1.5, DF_TVS pu-high 2,2k only, Remove R315</p>			





**Stuff for Integrated CLK Gen Mode**



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

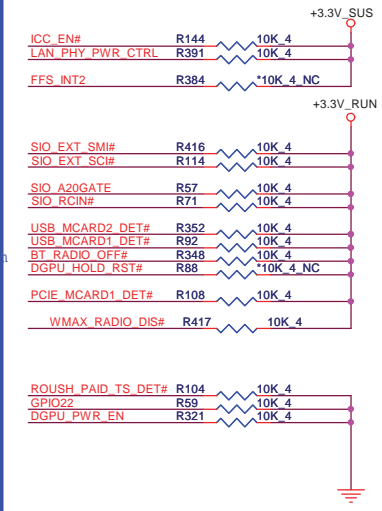
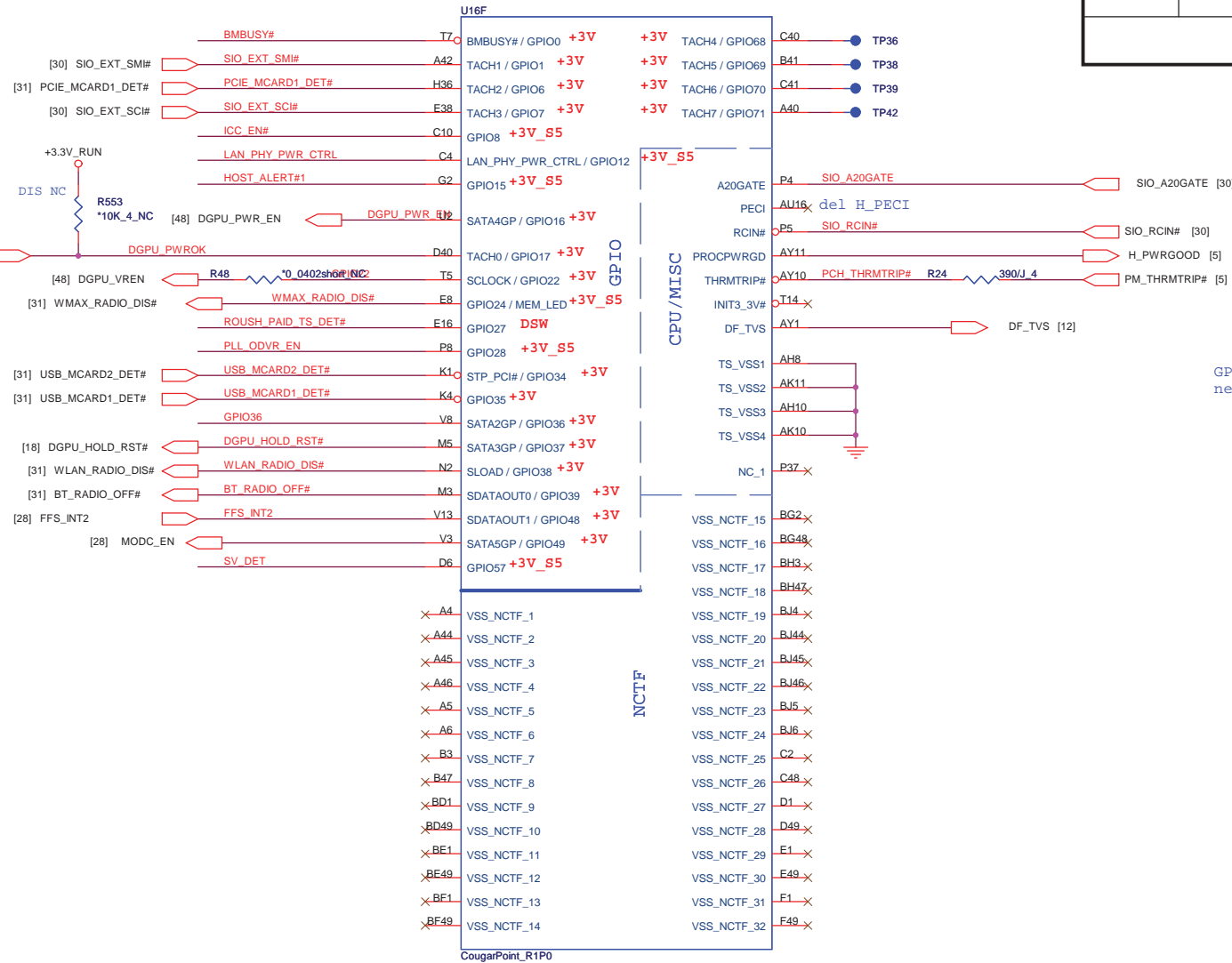


## Cougar Point (GPIO,VSS\_NCTF,RSVD)

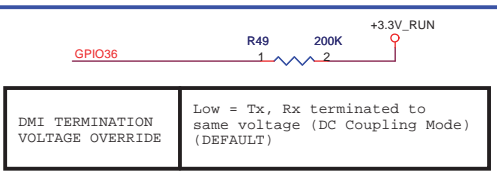
Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)



## GPIO Pull-up/Pull-down(CLG)

GPIO37 follow 14" team  
need INTEL confirm

CougarPoint\_R1P0



DMI TERMINATION  
VOLTAGE OVERRIDE

Low = Tx, Rx terminated to  
same voltage (DC Coupling Mode)  
(DEFAULT)

## SGPIO Confirm with Intel



BMBUSY#:(Intel feedback)  
Follow CRB checklist, 1K is  
for intel BIOS validation purpose.

BMBUSY#:  
If not used, require a weak pull-up  
(8.2- KΩ to 10 kΩ) to Vcc3\_3.  
CRB(V1.0)P28: it has 1K PU and  
100 ohm pull-up for validation purpose.

HOST\_ALERT#1 R381 1K 4

Intel ME Crypto Transport Layer  
Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

**MFG-TEST**

WLAN\_RADIO\_DIS# R331 R332 10K 4

**Quanta Computer Inc.**

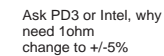
**PROJECT : R03A/V03A**

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**Cougar Point 6/7**

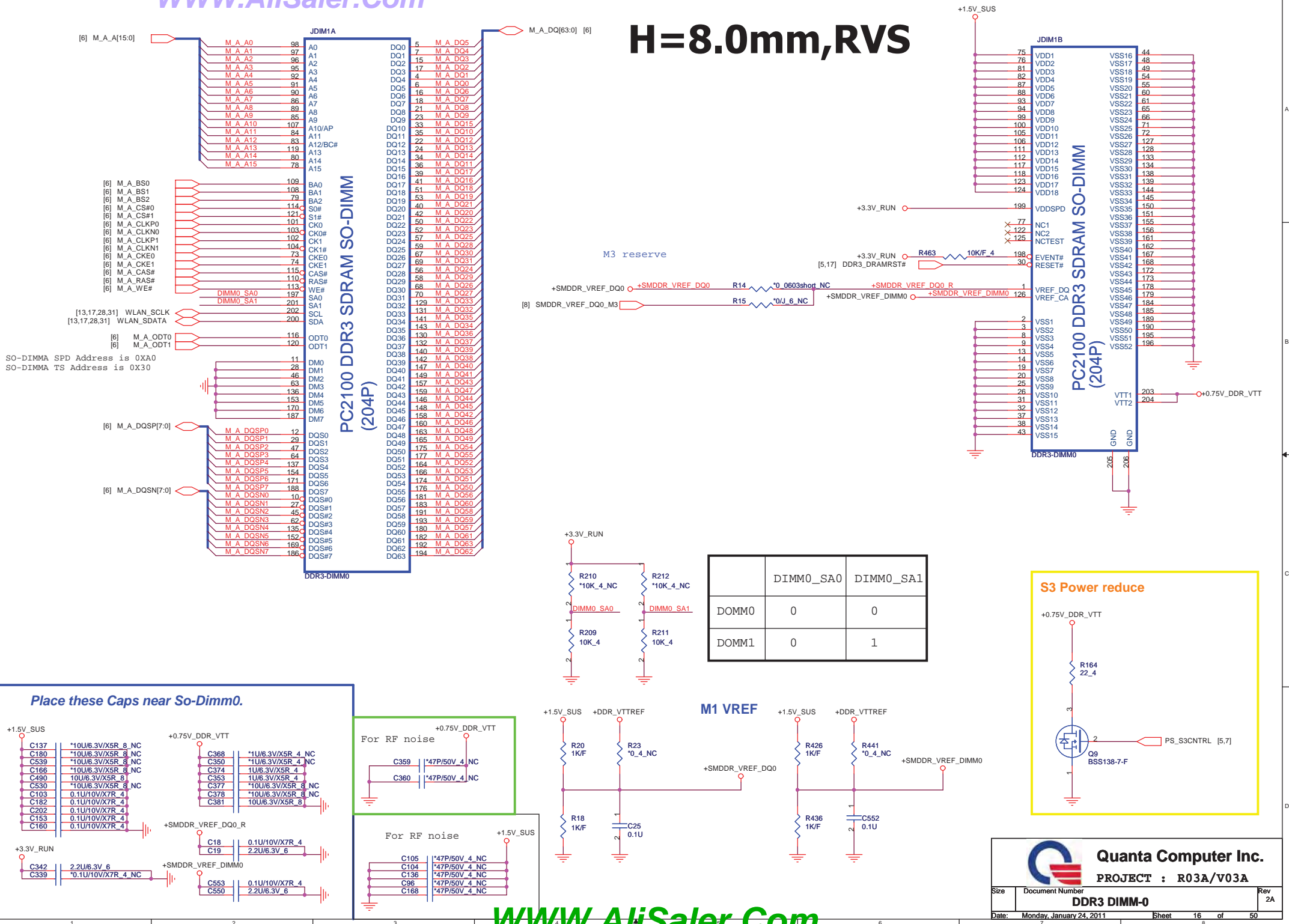
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Tie to 3.3V\_S  
don't support  
CP\_v1.0 p88

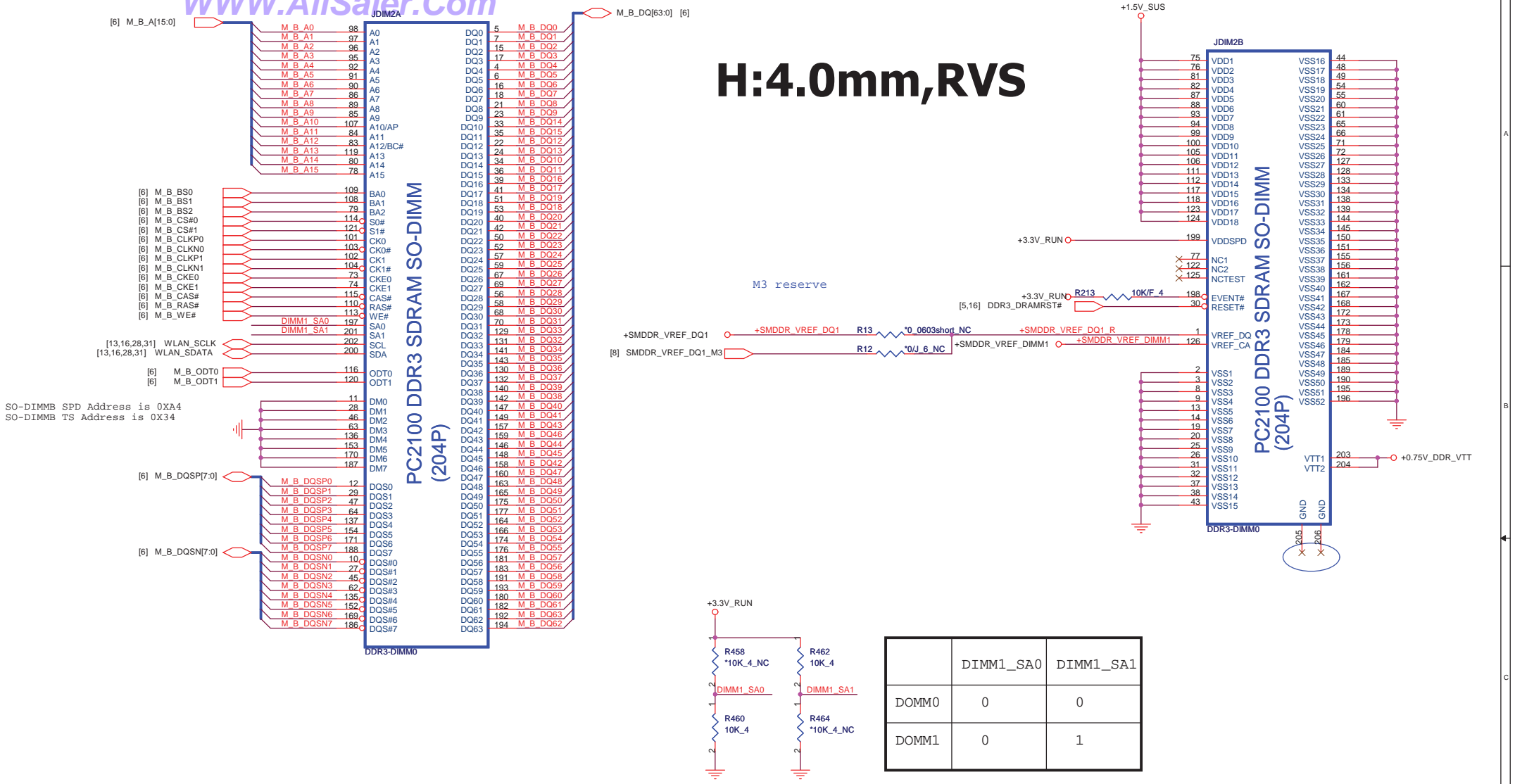




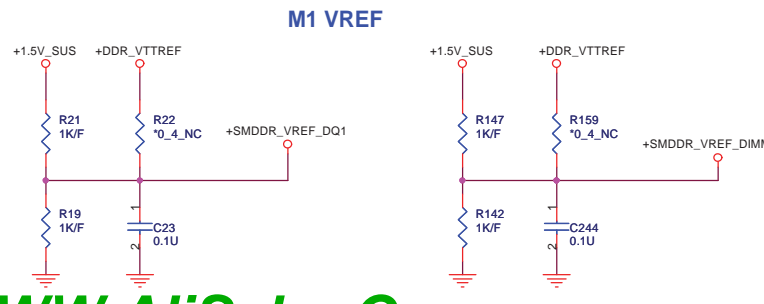
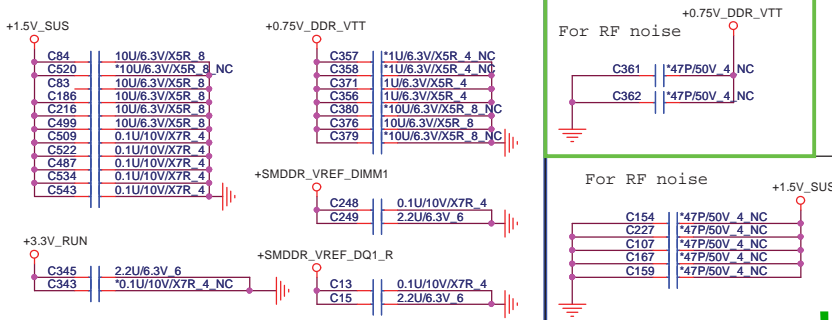
H=8.0mm,RVS



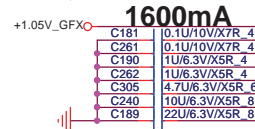
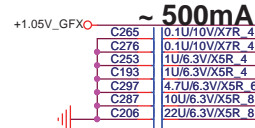
H:4.0mm,RVS



Place these Caps near So-Dimm2.



PEX\_IOVDD+PEX\_IOVDDQ >2.2A



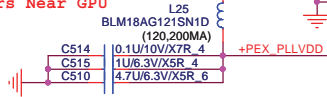
0.1u \*4 under GPU  
Others Near GPU

0.1u under GPU  
Others Near GPU

confirm with FAE  
should change power rail

**12~16 mils width**  
**120mA**

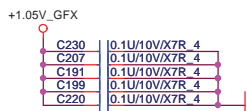
0.1u under GPU  
Others Near GPU



**120mA 12~16 mils width**



0.1u under GPU  
Others Near GPU  
add 1u near GPU as FAE confirm



1211 for Nvidia request  
add transition cap

U20A  
N12P-GE-A1

- PEX\_IOVDD\_1
- PEX\_IOVDD\_2
- PEX\_IOVDD\_3
- PEX\_IOVDD\_4
- PEX\_IOVDD\_5
- PEX\_IOVDDQ\_1
- PEX\_IOVDDQ\_2
- PEX\_IOVDDQ\_3
- PEX\_IOVDDQ\_4
- PEX\_IOVDDQ\_5
- PEX\_IOVDDQ\_6
- PEX\_IOVDDQ\_7
- PEX\_IOVDDQ\_8
- PEX\_IOVDDQ\_9
- PEX\_IOVDDQ\_10
- PEX\_IOVDDQ\_11
- PEX\_IOVDDQ\_12
- PEX\_IOVDDQ\_13
- PEX\_IOVDDQ\_14
- PEX\_IOVDDQ\_15
- PEX\_IOVDDQ\_16
- PEX\_IOVDDQ\_17
- PEX\_IOVDDQ\_18
- PEX\_IOVDDQ\_19
- PEX\_IOVDDQ\_20
- PEX\_IOVDDQ\_21
- PEX\_IOVDDQ\_22
- PEX\_IOVDDQ\_23
- PEX\_IOVDDQ\_24
- PEX\_IOVDDQ\_25

PCI EXPRESS

- PEX\_RX0
- PEX\_RX0\*
- PEX\_RX1
- PEX\_RX1\*
- PEX\_RX2
- PEX\_RX2\*
- PEX\_RX3
- PEX\_RX3\*
- PEX\_RX4
- PEX\_RX4\*
- PEX\_RX5
- PEX\_RX5\*
- PEX\_RX6
- PEX\_RX6\*
- PEX\_RX7
- PEX\_RX7\*
- PEX\_RX8
- PEX\_RX8\*
- PEX\_RX9
- PEX\_RX9\*
- PEX\_RX10
- PEX\_RX10\*
- PEX\_RX11
- PEX\_RX11\*
- PEX\_RX12
- PEX\_RX12\*
- PEX\_RX13
- PEX\_RX13\*
- PEX\_RX14
- PEX\_RX14\*
- PEX\_RX15
- PEX\_RX15\*

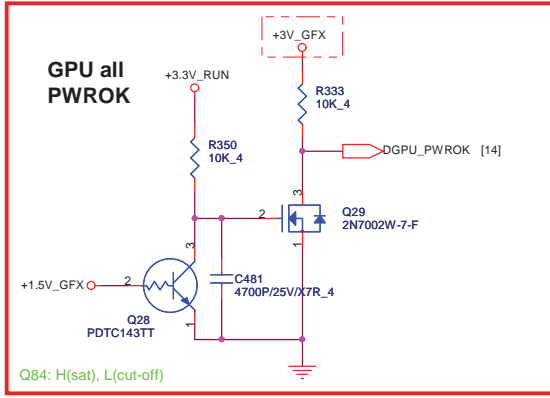
- PEX\_TX0
- PEX\_TX0\*
- PEX\_TX1
- PEX\_TX1\*
- PEX\_TX2
- PEX\_TX2\*
- PEX\_TX3
- PEX\_TX3\*
- PEX\_TX4
- PEX\_TX4\*
- PEX\_TX5
- PEX\_TX5\*
- PEX\_TX6
- PEX\_TX6\*
- PEX\_TX7
- PEX\_TX7\*
- PEX\_TX8
- PEX\_TX8\*
- PEX\_TX9
- PEX\_TX9\*
- PEX\_TX10
- PEX\_TX10\*
- PEX\_TX11
- PEX\_TX11\*
- PEX\_TX12
- PEX\_TX12\*
- PEX\_TX13
- PEX\_TX13\*
- PEX\_TX14
- PEX\_TX14\*
- PEX\_TX15
- PEX\_TX15\*

- PEX\_REFCLK
- PEX\_REFCLK\*
- PEX\_TSTCLK\_OUT
- PEX\_TSTCLK\_OUT\*
- PEX\_RST\*
- PEX\_CLKREQ\*
- PEX\_TERM\*
- TESTMODE

- AP17 PEG\_TXP15
- AN17 PEG\_TXN15
- AN19 PEG\_TXP14
- AN19 PEG\_TXN14
- AR19 PEG\_TXP13
- AR20 PEG\_TXN13
- AN20 PEG\_TXP12
- AN22 PEG\_TXN12
- AP22 PEG\_TXP11
- AR22 PEG\_TXN11
- AR22 PEG\_TXP10
- AR23 PEG\_TXN10
- AP23 PEG\_TXP9
- AN23 PEG\_TXN9
- AN25 PEG\_TXP8
- AP25 PEG\_TXN8
- AR25 PEG\_TXP7
- AR26 PEG\_TXN7
- AP26 PEG\_TXP6
- AN26 PEG\_TXN6
- AN28 PEG\_TXP5
- AP28 PEG\_TXN5
- PEX\_RX10\*
- PEX\_RX11
- PEX\_RX11\*
- PEX\_RX12
- PEX\_RX12\*
- PEX\_RX13
- PEX\_RX13\*
- PEX\_RX14
- PEX\_RX14\*
- PEX\_RX15
- PEX\_RX15\*

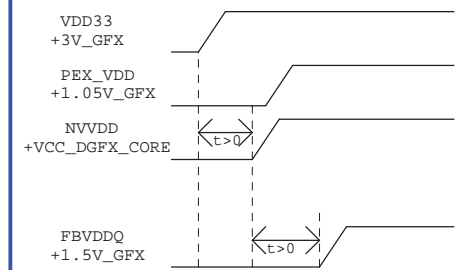
- AL17 PEG\_RXP15 C
- AM17 PEG\_RXN15 C
- AM18 PEG\_RXP14 C
- AM18 PEG\_RXN14 C
- AL19 PEG\_RXP13 C
- AL19 PEG\_RXN13 C
- AL20 PEG\_RXP12 C
- AM20 PEG\_RXN12 C
- AM21 PEG\_RXP11 C
- AM22 PEG\_RXN11 C
- AL22 PEG\_RXP10 C
- AL22 PEG\_RXN10 C
- AL23 PEG\_RXP9 C
- AM23 PEG\_RXN9 C
- AM24 PEG\_RXP8 C
- AM25 PEG\_RXN8 C
- AL25 PEG\_RXP7 C
- AK25 PEG\_RXN7 C
- AL26 PEG\_RXP6 C
- AM26 PEG\_RXN6 C
- AM27 PEG\_RXP5 C
- AM28 PEG\_RXN5 C
- AL28 PEG\_RXP4 C
- AK28 PEG\_RXN4 C
- AL29 PEG\_RXP3 C
- AM29 PEG\_RXN3 C
- AM30 PEG\_RXP2 C
- AM31 PEG\_RXN2 C
- AM31 PEG\_RXP1 C
- AM32 PEG\_RXN1 C
- AN32 PEG\_RXP0 C
- AP32 PEG\_RXN0 C

- AR16 CLK\_PCIE\_VGAP
- AR17 CLK\_PCIE\_VGAN
- AL17 PEX\_TSTCLK
- AL18 PEX\_TSTCLK#
- AM16 GPU\_RST#
- AR13 PEX\_CLKREQ#
- AG21 PEX\_TERM
- AP35 TESTMODE

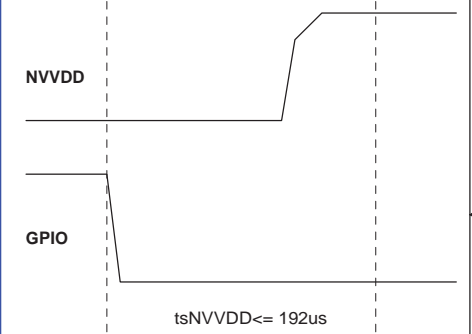


Q84: H(sat), L(cut-off)

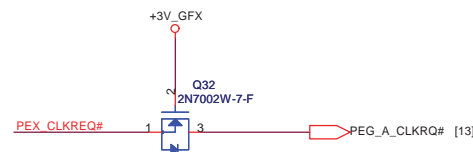
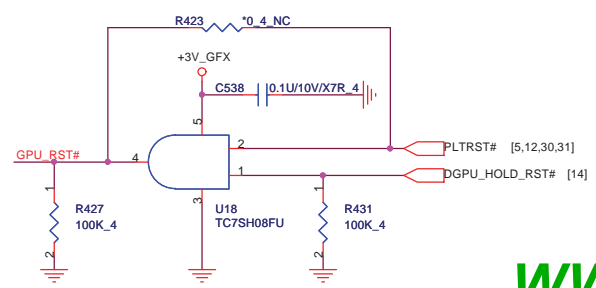
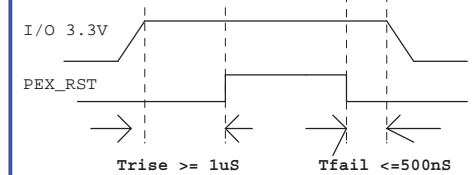
## Power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V  
NVVDD Maximum Settling Time



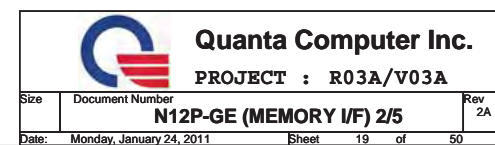
## PEX\_RST timing



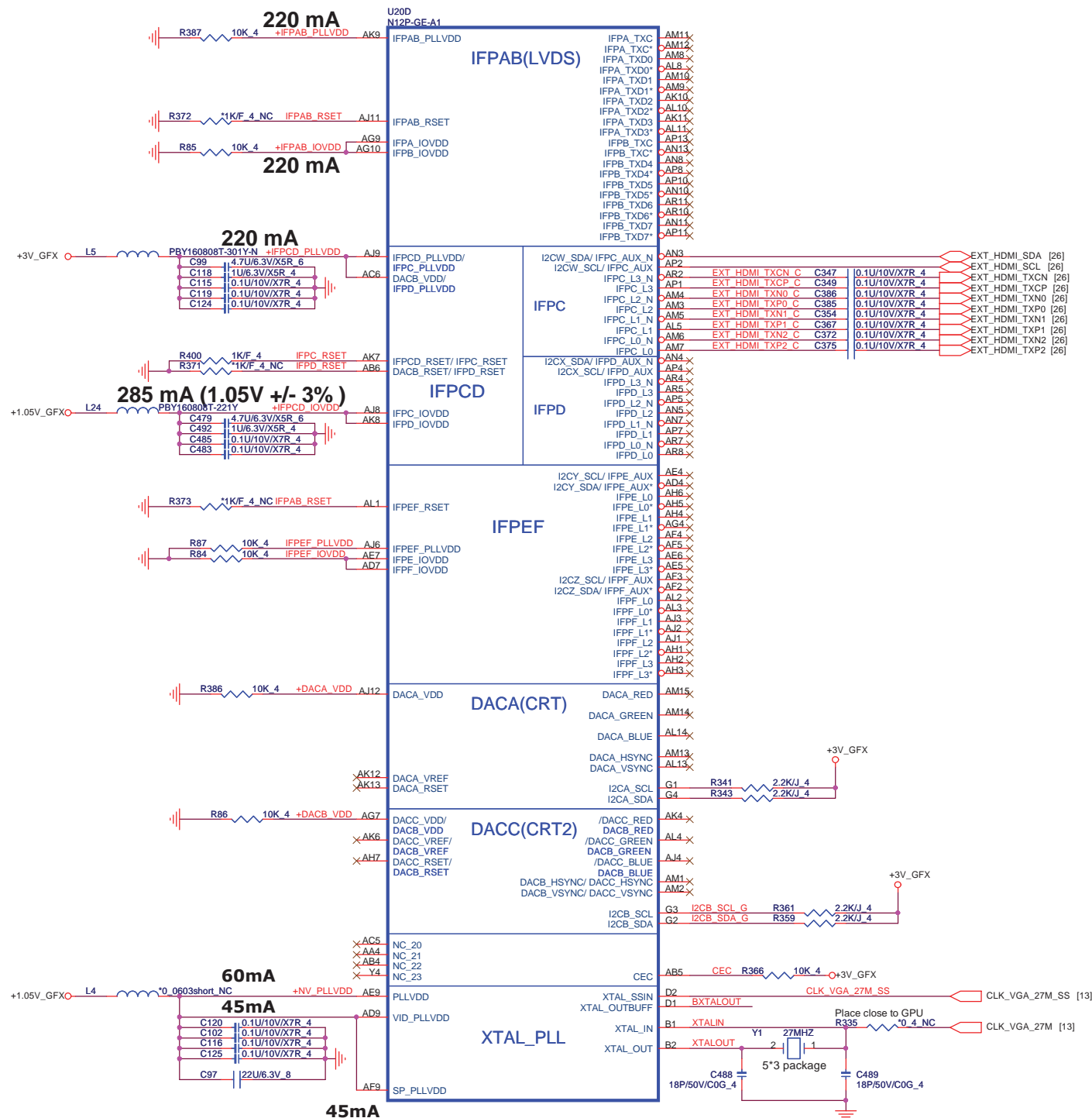
Add MOS for preventing leakage.

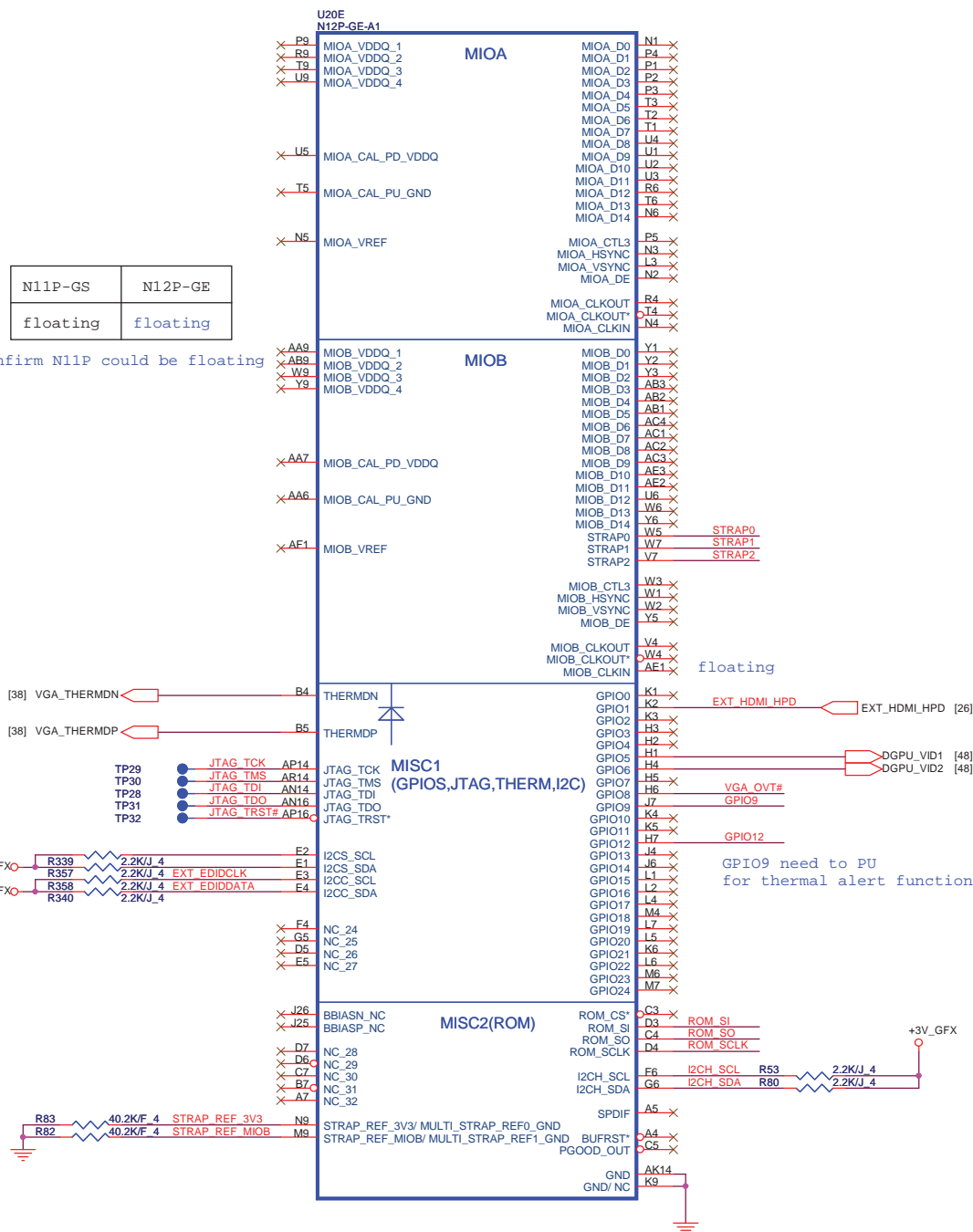


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PROJECT : R03A/V03A









N11P-GS	N12P-GE
floating	floating

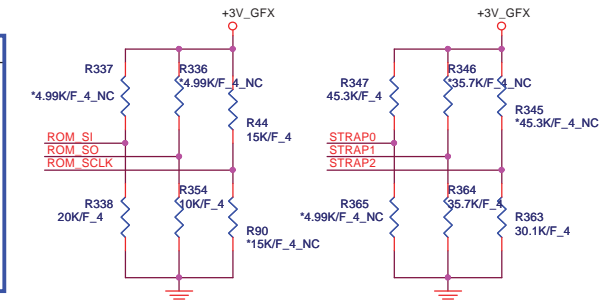
FAE confirm N11P could be floating

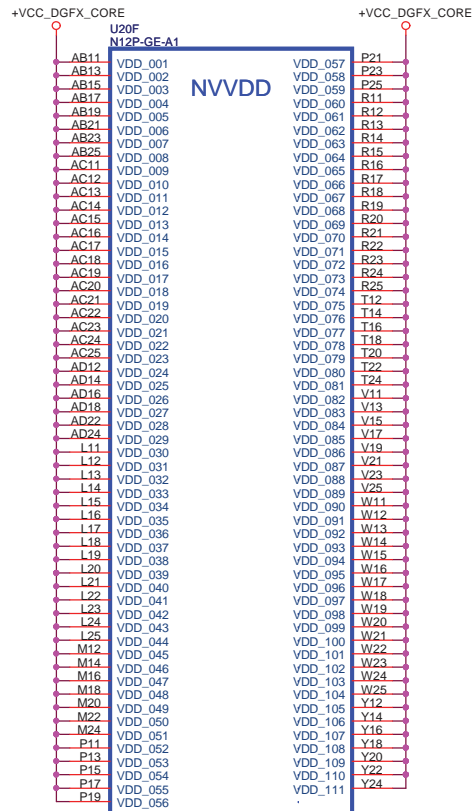
CHIP	PCI_DEVID:	STRAP2	ROM_SCLK	Default: N12P-GE
N11P-GS	0xDF0	0000 PD 5K	1010 PU 15K	AJ0N11M0T24 70=0111 0000(device ID:10000)
N12P-GE	0xDF5	0101 PD 30K	1010 PU 15K	FE=1111 1110(device ID:11110) AJ0N11P0T22

Check N11P-GS and N12P-GE

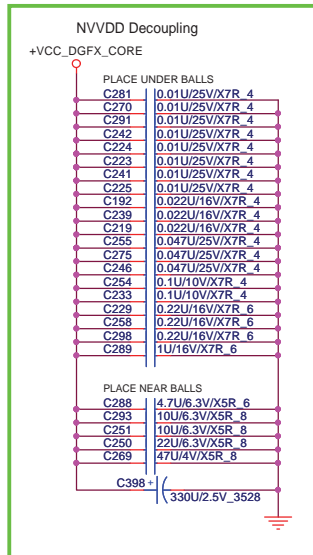
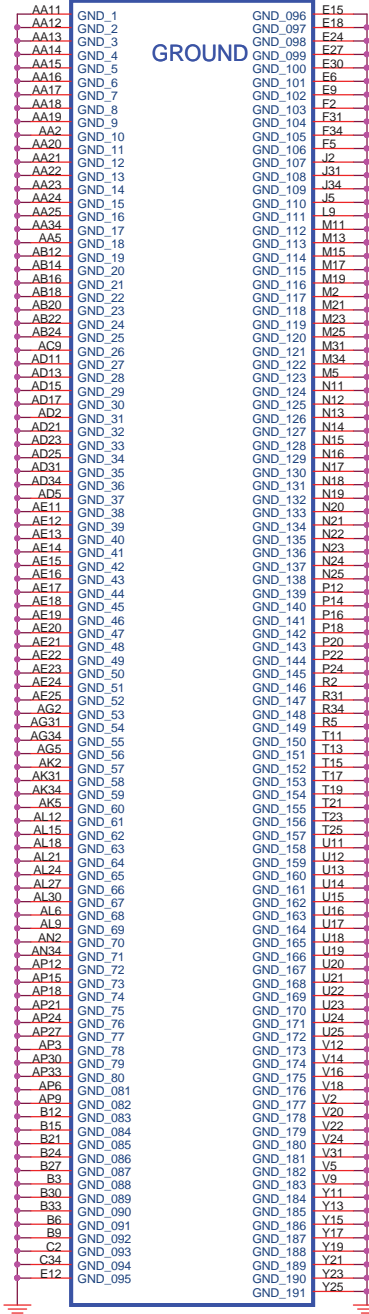
## Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111





U20G  
N12P-GE-A1



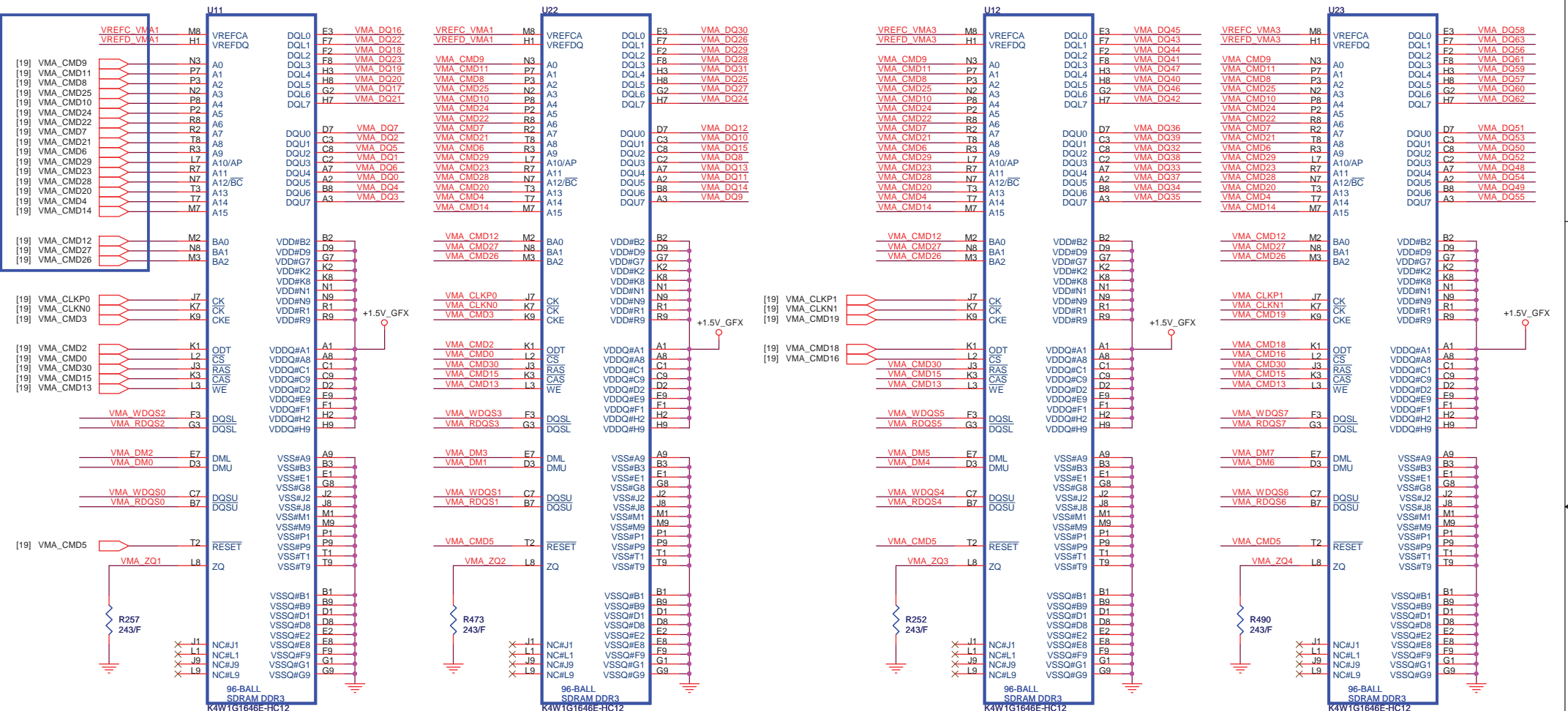
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PROJECT : R03A/V03A

Size	Document Number	N12P-GE (POWER & GND) 5/5	Rev 2A
Date:	Monday, January 24, 2011	Sheet 22	of 50

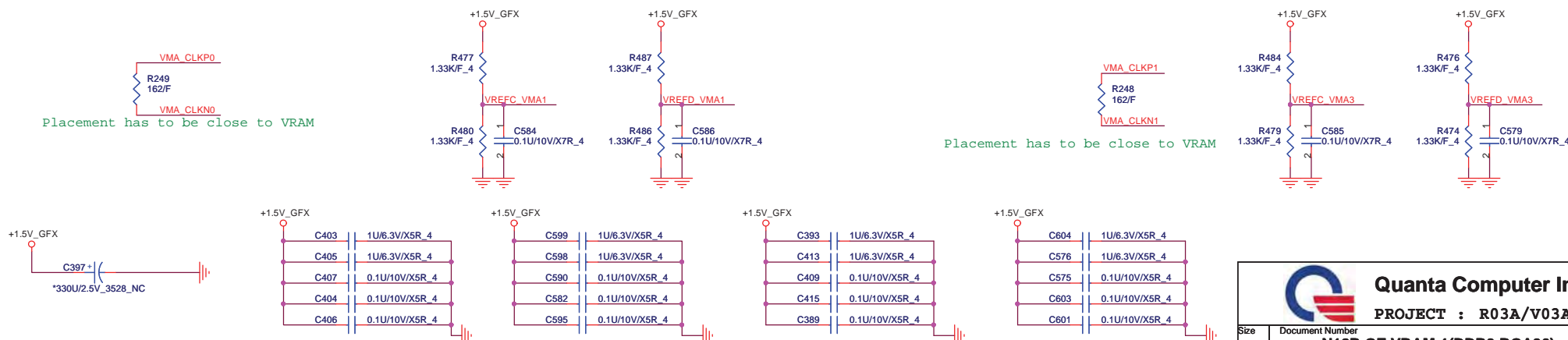


change VRAM footprint to hynix 2G(the package is bigger)

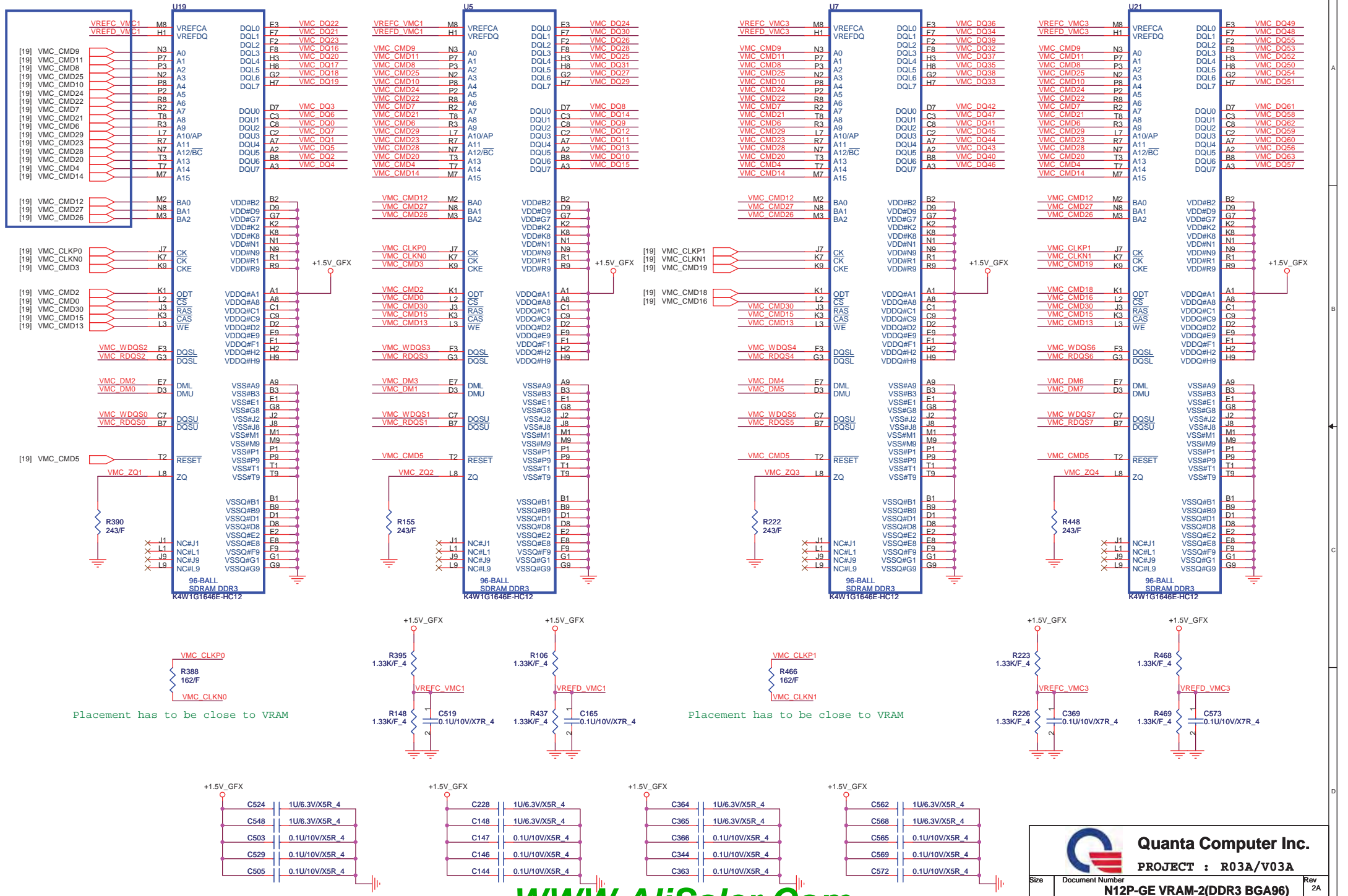


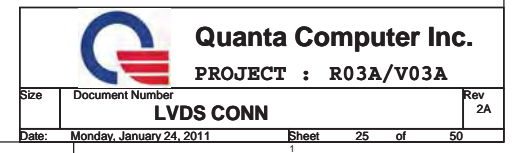
Placement has to be close to VRAM

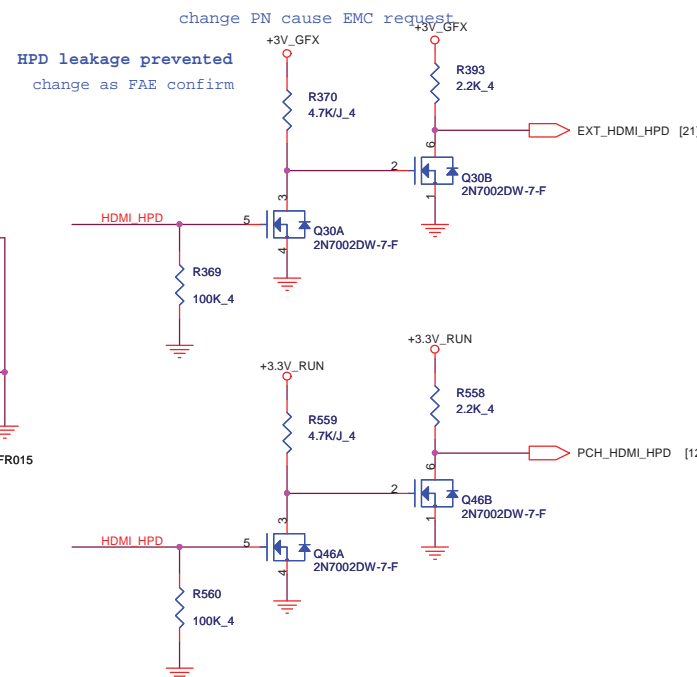
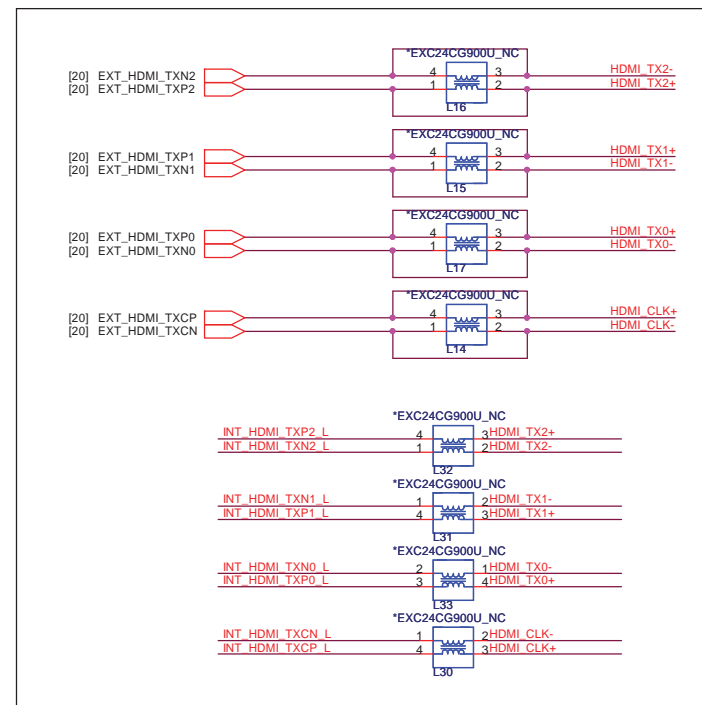
Placement has to be close to VRAM



SWAP CMD NET  
modify Mode E to Mode D

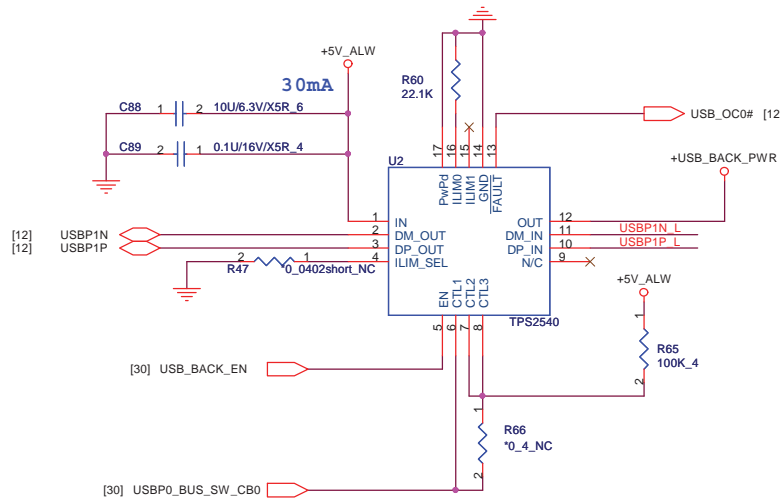






## ESATA + USB Conn + Power share

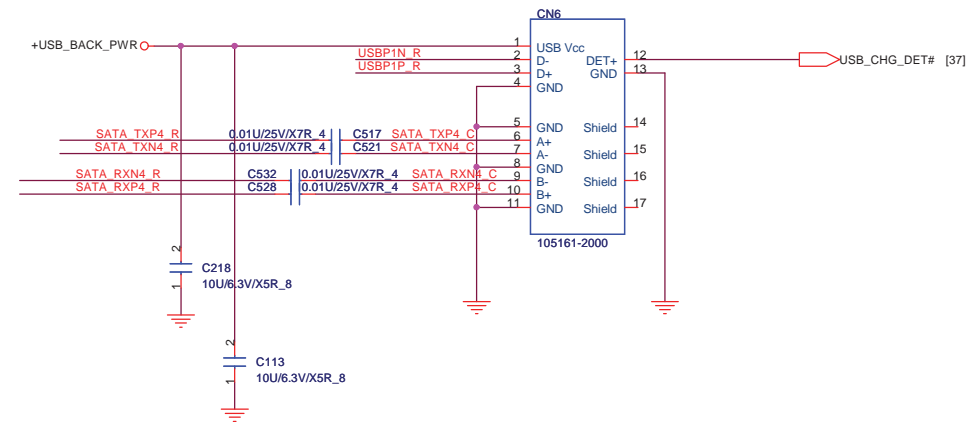
## S3/S5 USB charging circuit



USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

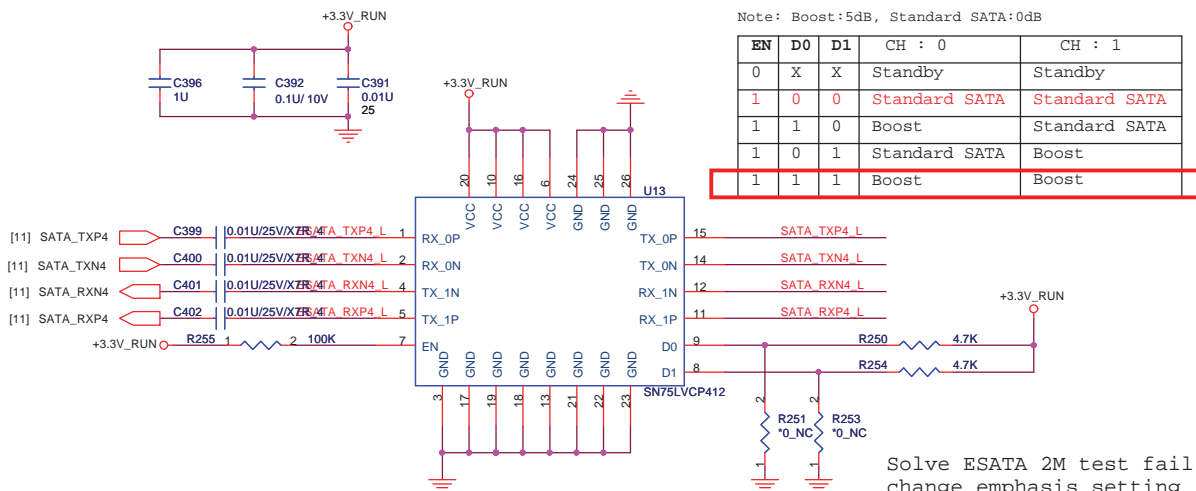
ES(PG1.0): Stuff R66, Remove R65  
MP(PG1.1): Remove R66 Stuff R65

	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

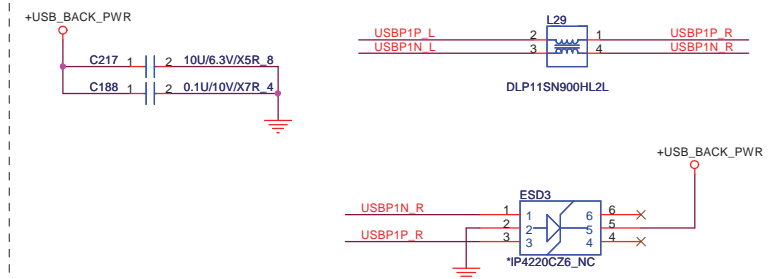


## E-SATA Re-driver

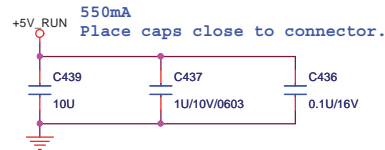
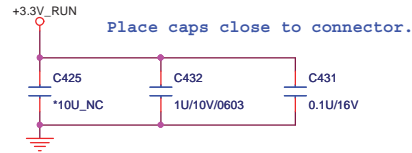
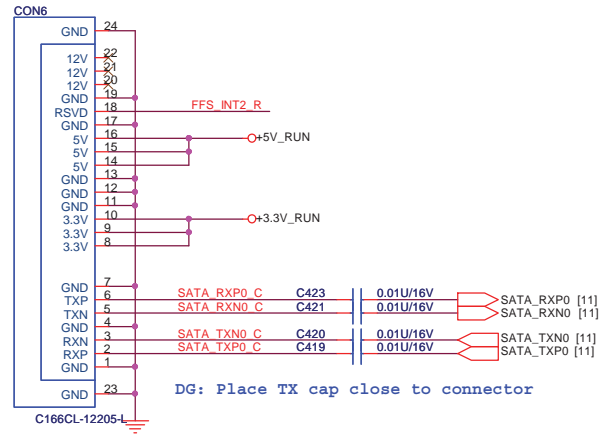
Layout Note: Please put those on the same side of MB PCB



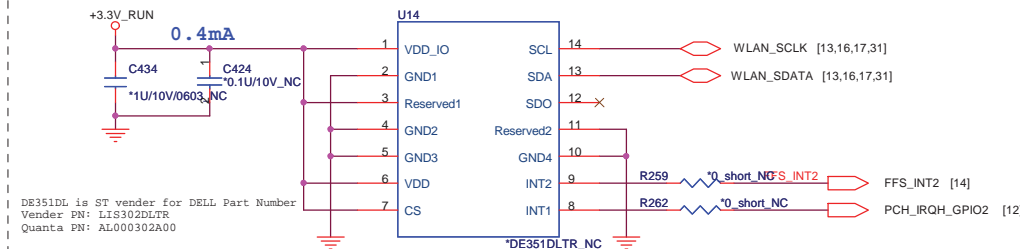
Solve ESATA 2M test fail issue,  
change emphasis setting



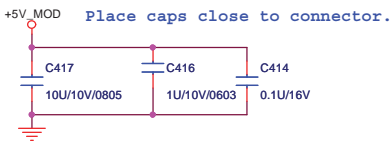
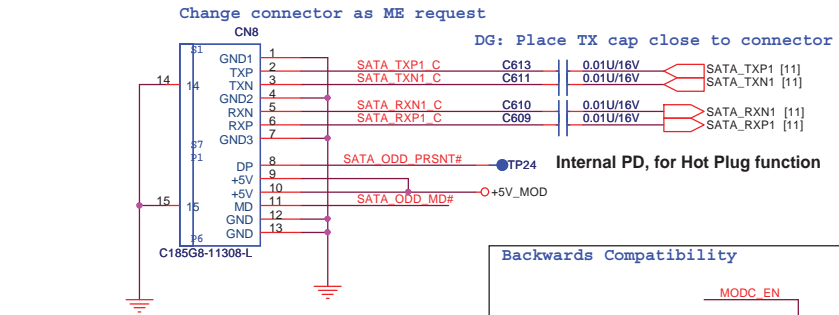
## SATA Connector



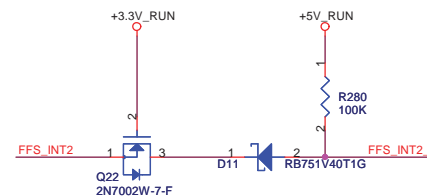
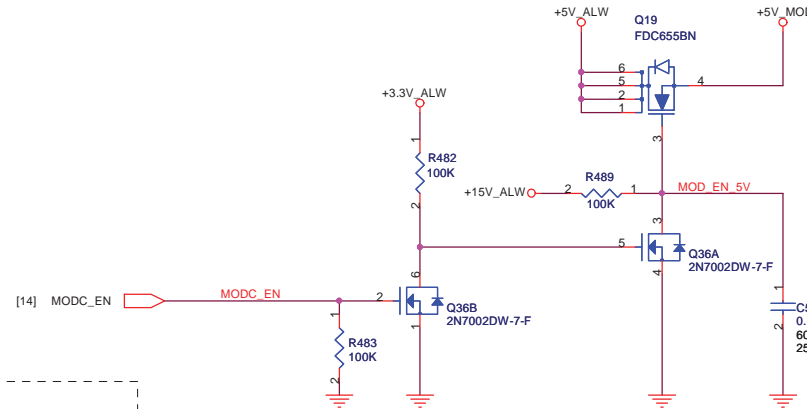
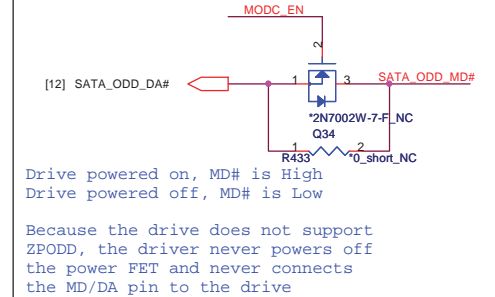
## 3-axis Fall Sensor (HDD data protector)



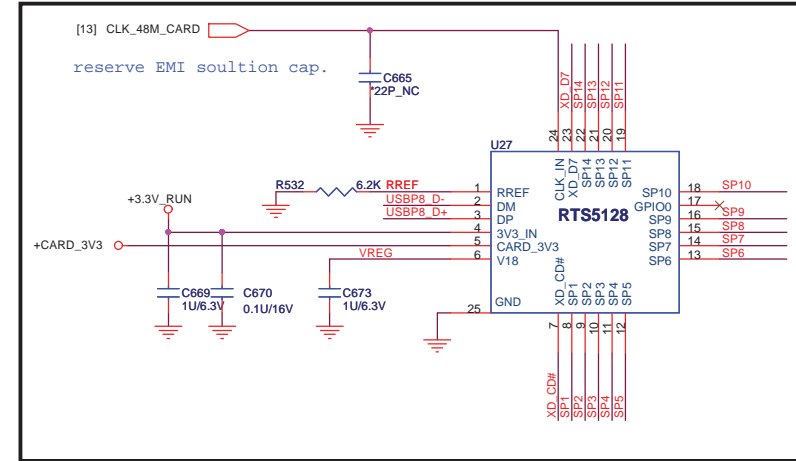
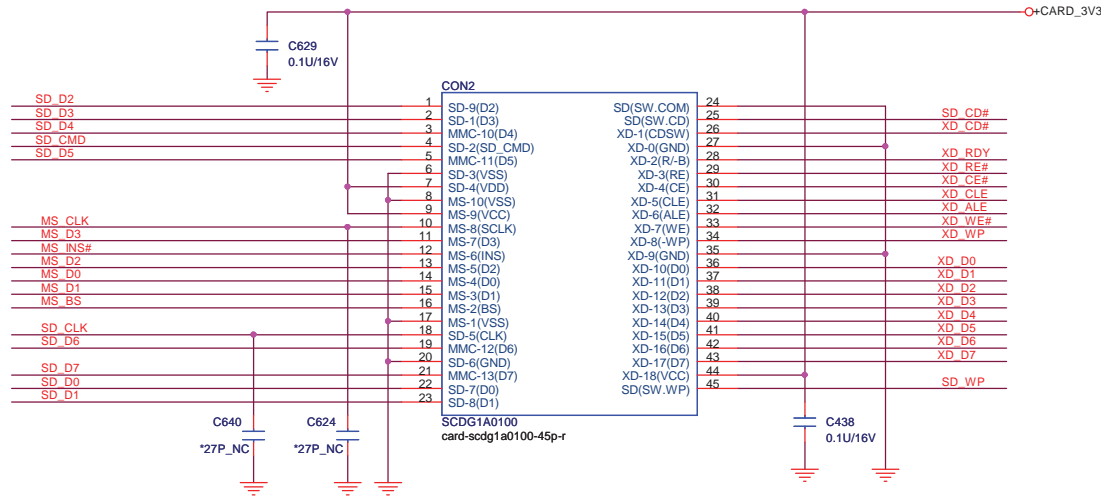
## ODD Connector



## Backwards Compatibility

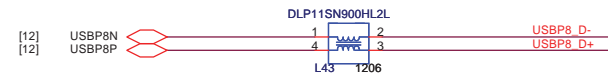


## RTS5128-QFN24

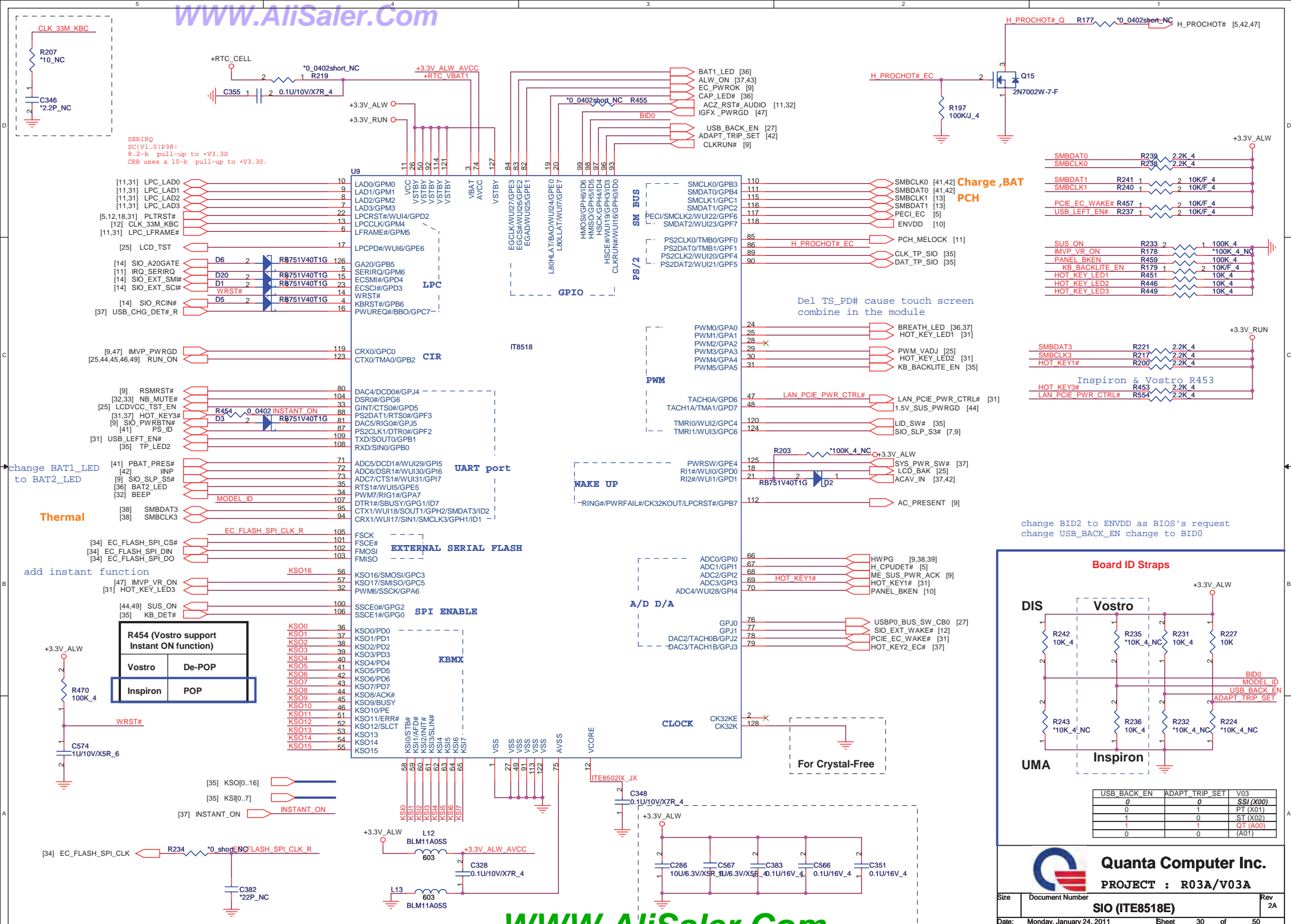


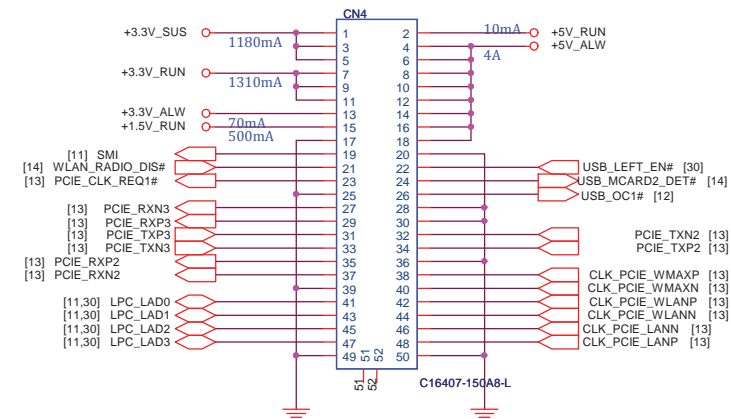
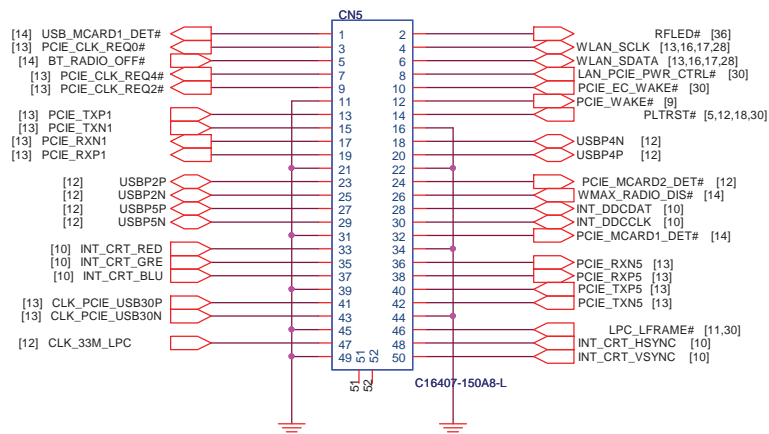
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#	SD_D1	MS_D7
SP4	XD_CLE	SD_D0	MS_D3
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	MS_D6
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6	MS_BS	

Share Pin

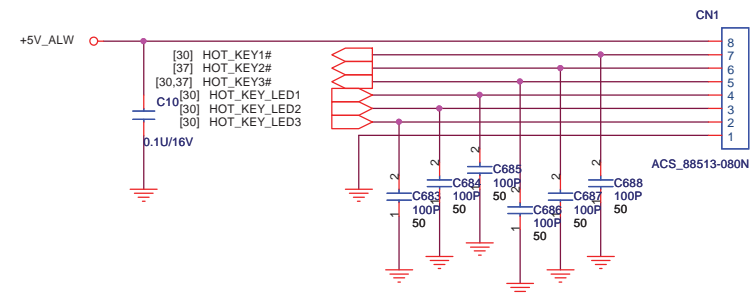




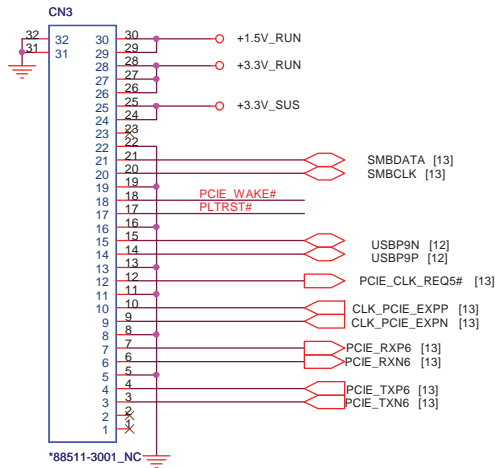


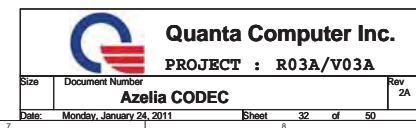


## HOTKEY CON



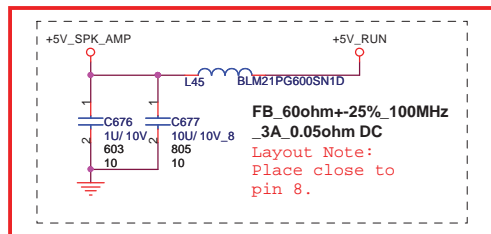
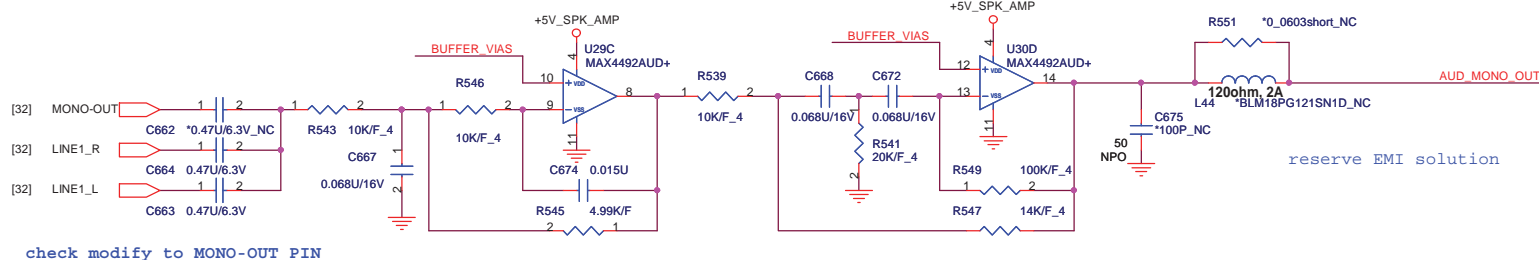
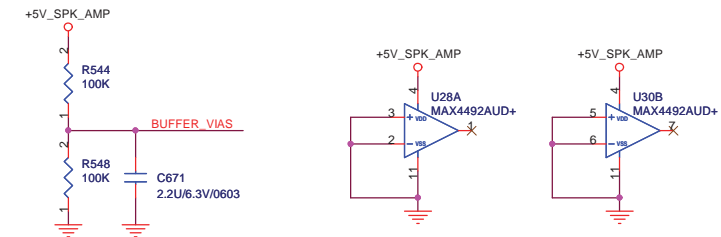
## MB to Express Card Board



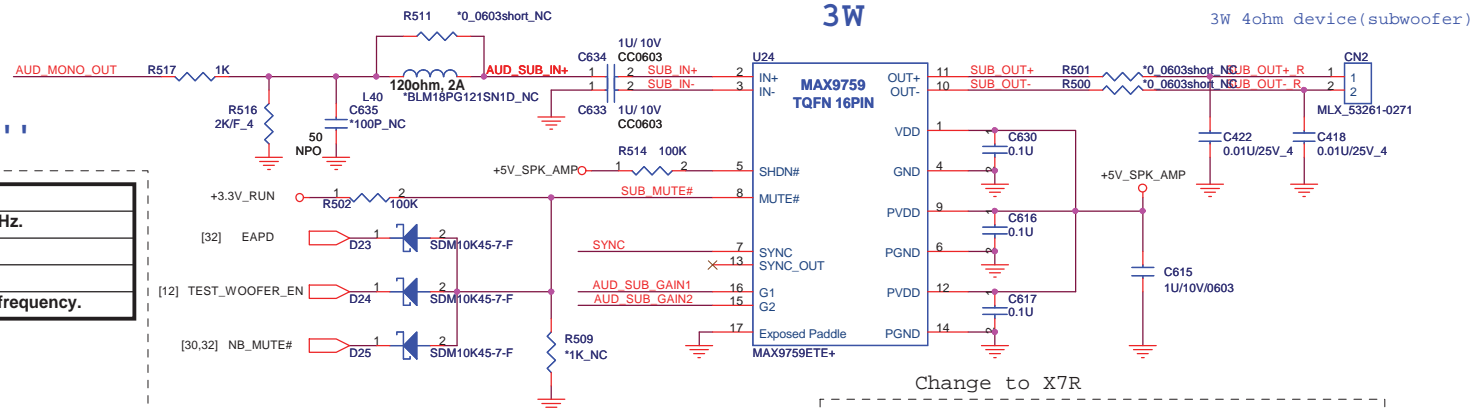


The diagram shows the SYNC pin configuration. The SYNC pin is connected to a 100k resistor (R513) to the +5V\_SPK\_AMP supply and a 100k resistor (R512) to ground. The table below defines the operating conditions for different SYNC pin states.

SYNC	Condition
VDD	Spread-spectrum mode with $f_S = 1200\text{kHz} \pm 70\text{kHz}$ .
GND	Fixed-frequency mode with $f_S = 1100\text{kHz}$ .
FLOAT	Fixed-frequency mode with $f_S = 1500\text{kHz}$ .
Clocked	Fixed-frequency mode with $f_S = \text{external clock frequency}$ .

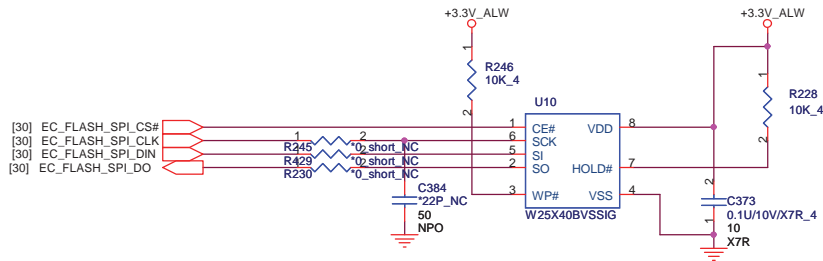


place close to connector side

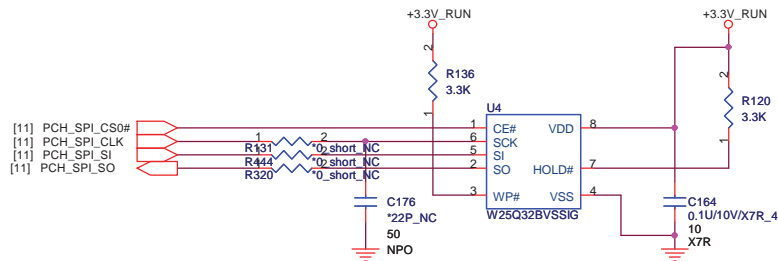


	GAIN1	GAIN2	GAIN
	0	0	24dB
	1	0	18dB
	0	1	12dB
GAIN1 GAIN2	1	1	6dB

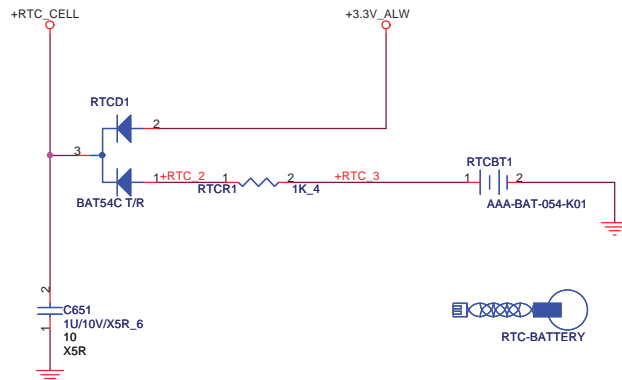
## For EC 4Mbit (512K Byte)



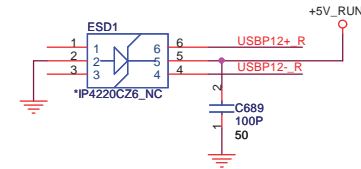
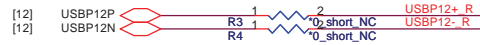
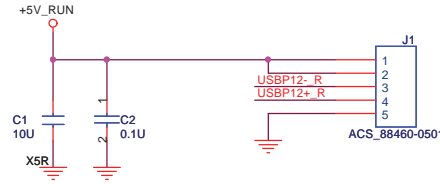
## For PCH 32Mbit (4M Byte)



## RTC



## Touch Screen Module



- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
  2. Maximum cable resistance on VCC, GND should be 150m ohm.
  3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

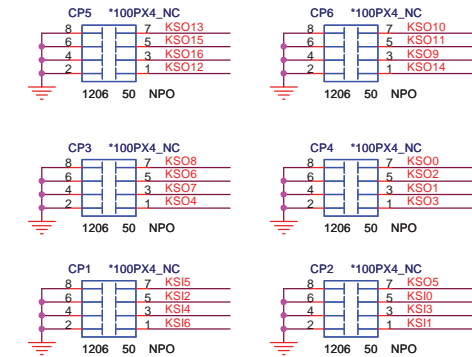
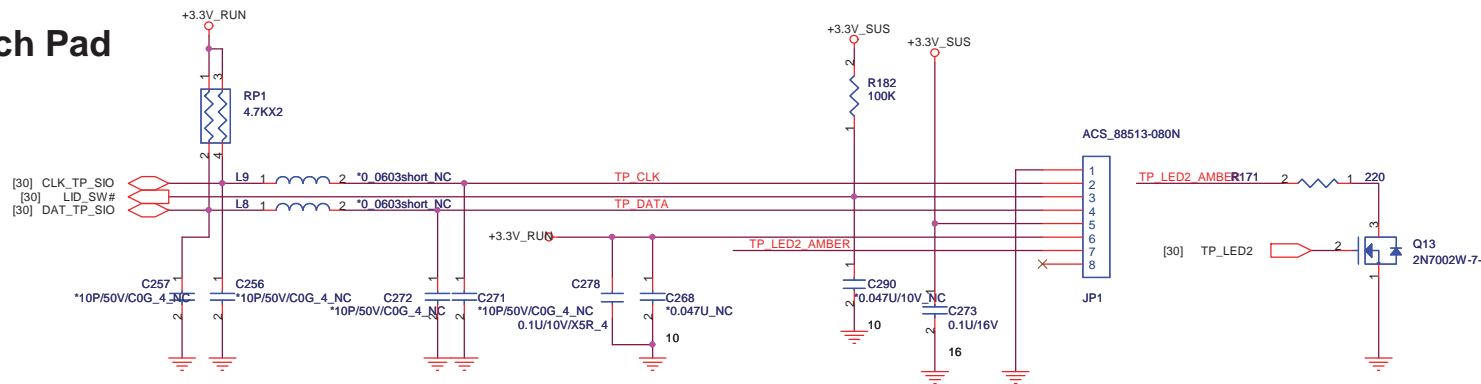


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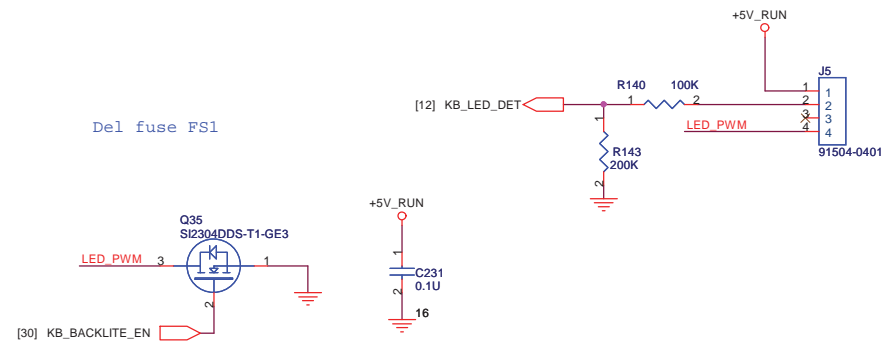
Size	Document Number	Rev
	FLASH / RTC	2A
Date:	Monday, January 24, 2011	Sheet 34 of 50

## Touch Pad

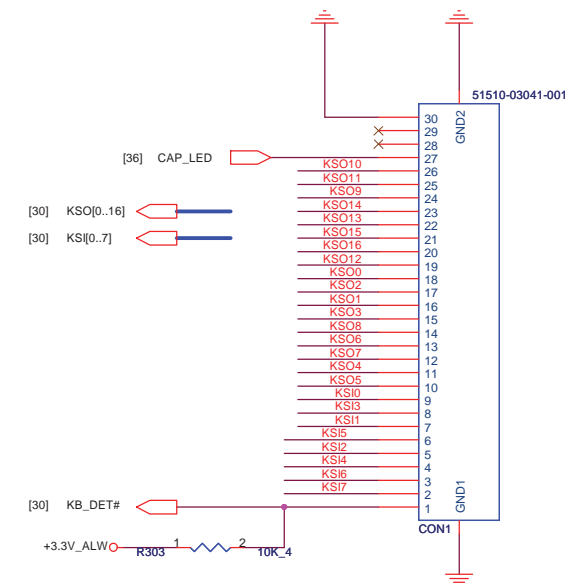


## Key board illumination

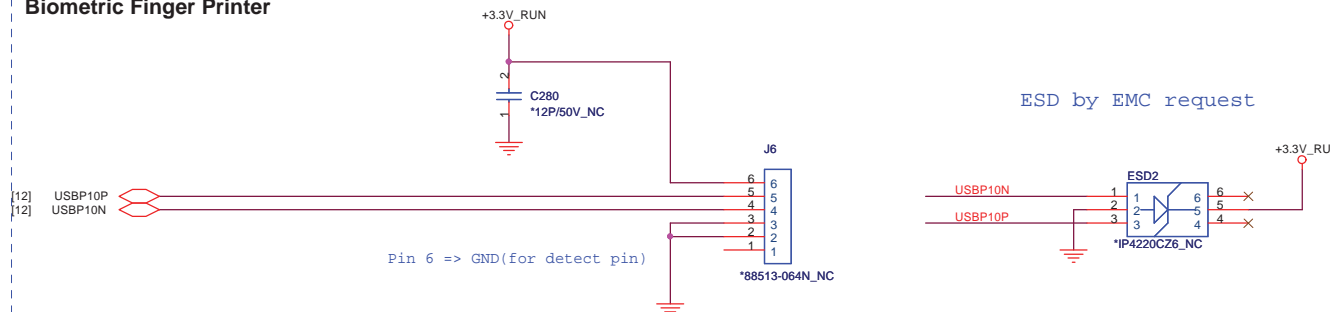
+KB\_LED power trace width >10 mil



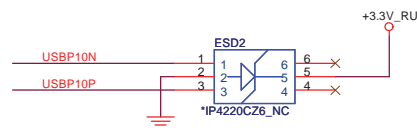
## KEYBOARD CONNECTOR



## Biometric Finger Printer



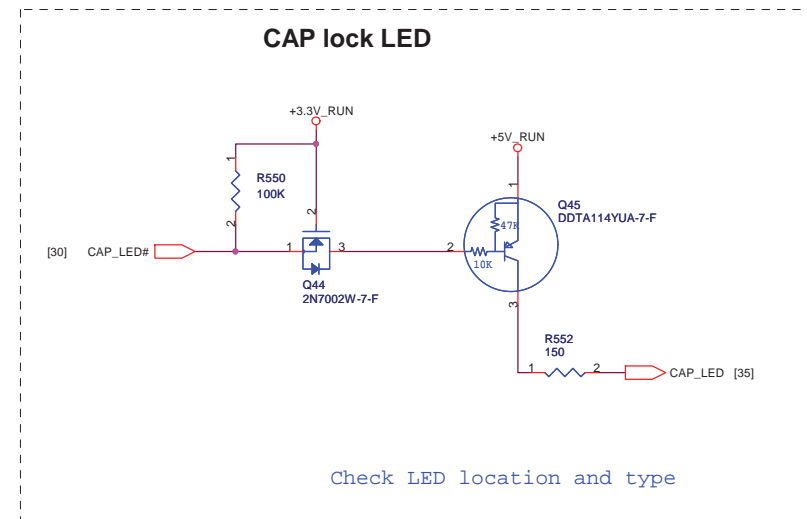
ESD by EMC request



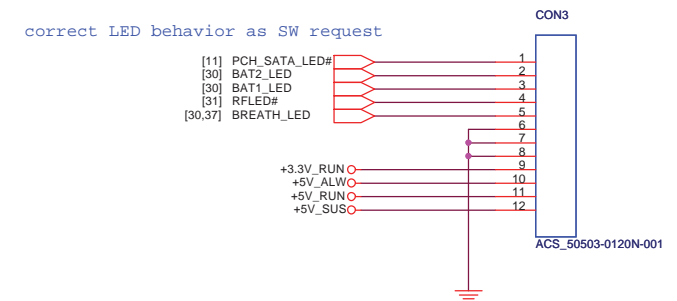
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PROJECT : R03A/V03A

Size	Document Number	Rev
	TP / KB	2A
Date:	Monday, January 24, 2011	Sheet 35 of 50



### MB to LED Board conn

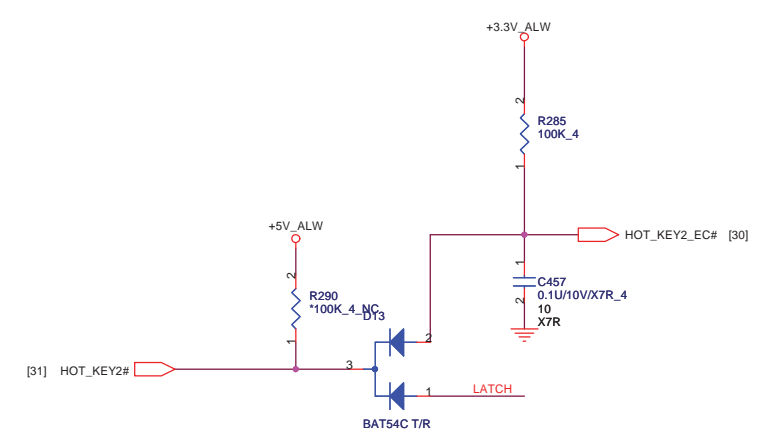
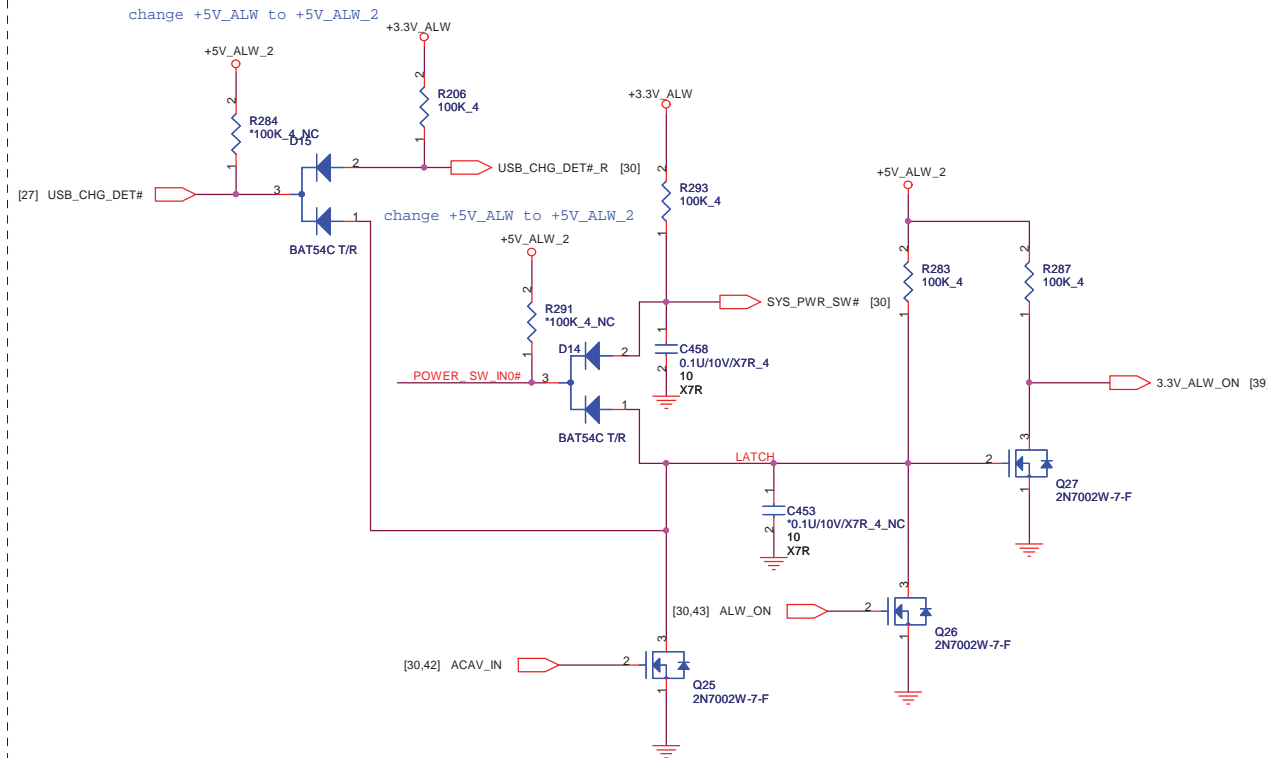


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**PROJECT : R03A/V03A**

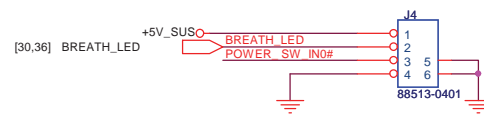
Size	Document Number	Rev
	<b>LED</b>	2A
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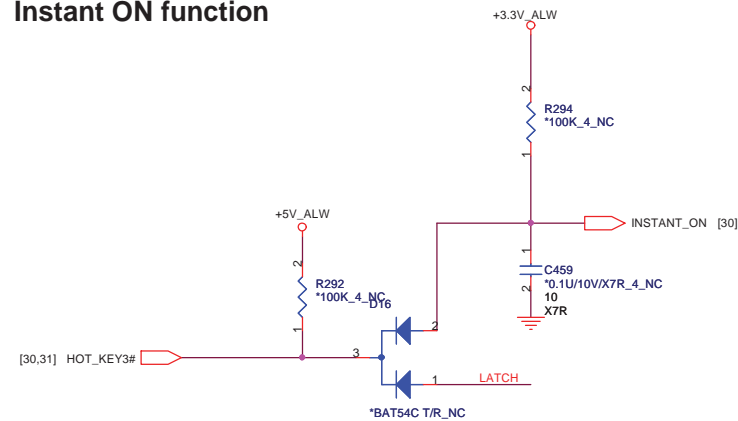
## 3VALW ON POWER LOGIC



## PWR button board form UM7



## Instant ON function

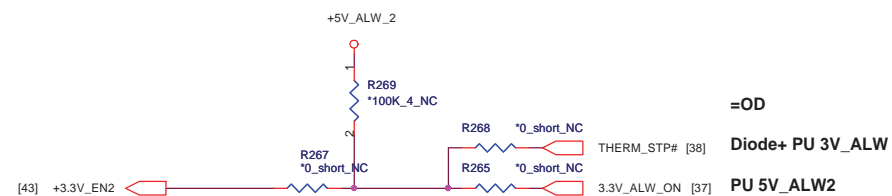
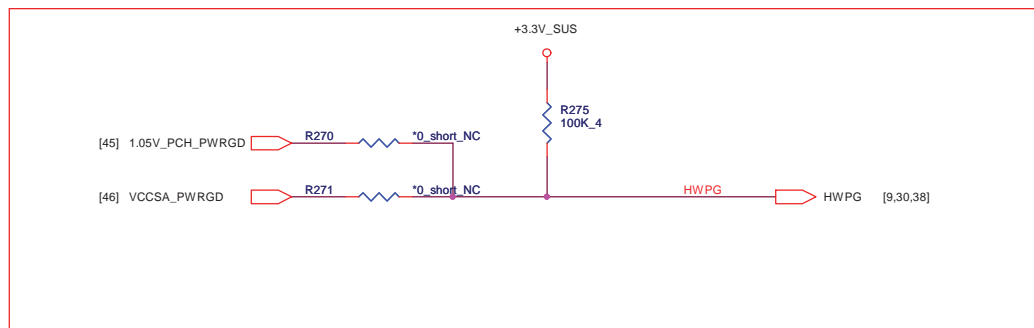


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	PWR SW/LED	2A
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=OD

Diode+ PU 3V\_ALW

PU 5V\_ALW2

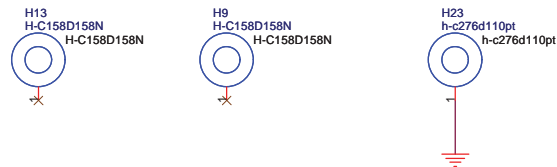
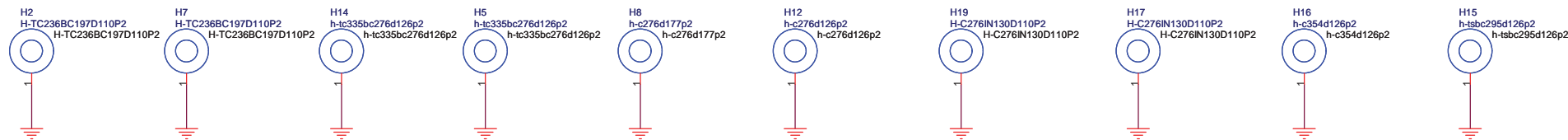


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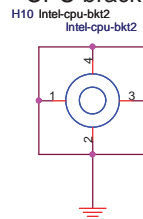
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Size	Document Number	Rev
		2A
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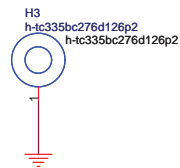
System Reset Circuit



CPU bracket



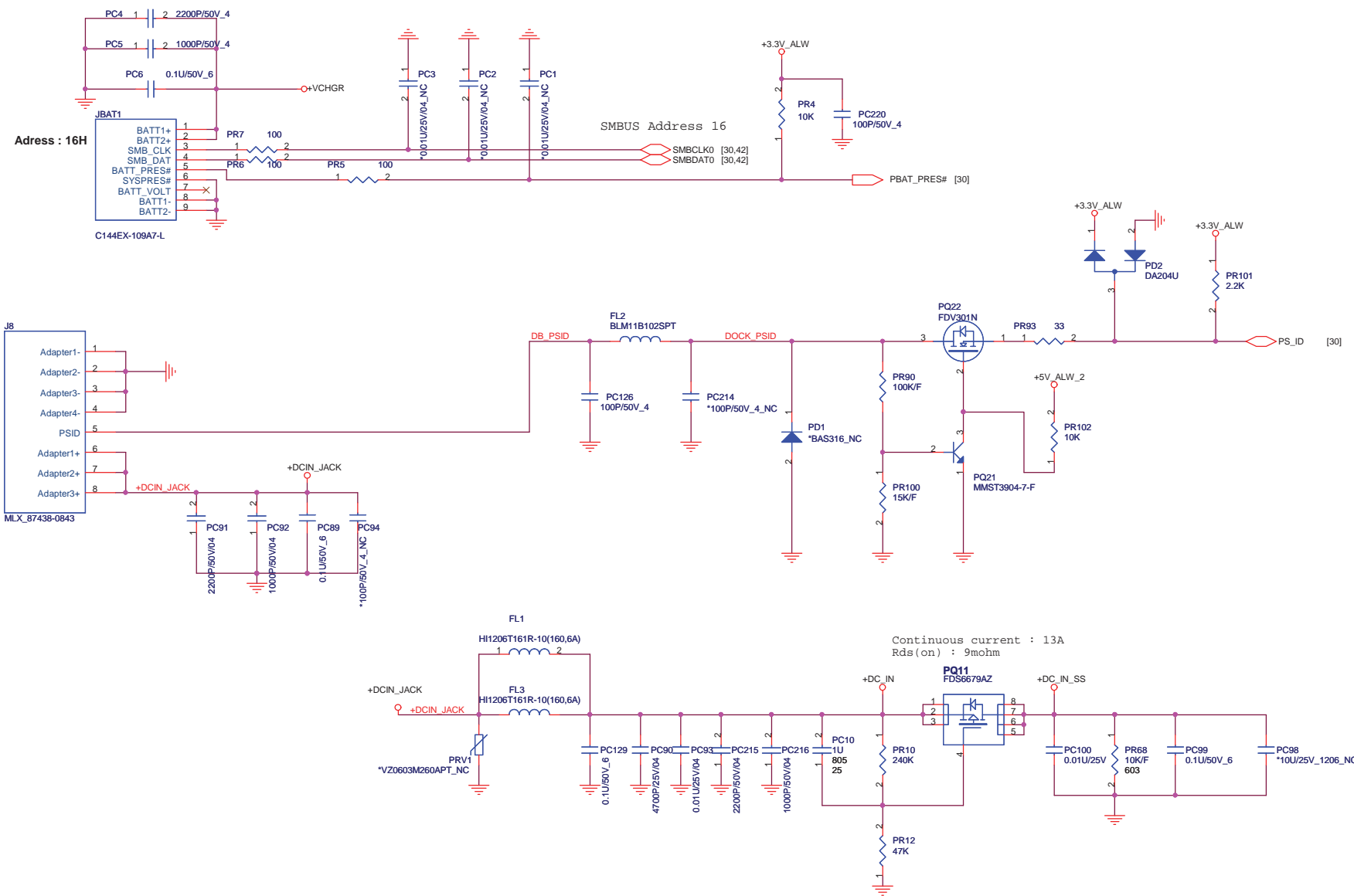
add a new hole for layout request

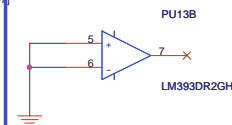
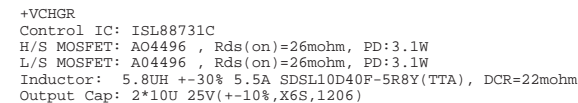



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Size	Document Number	Rev
	SCREW PAD	2A
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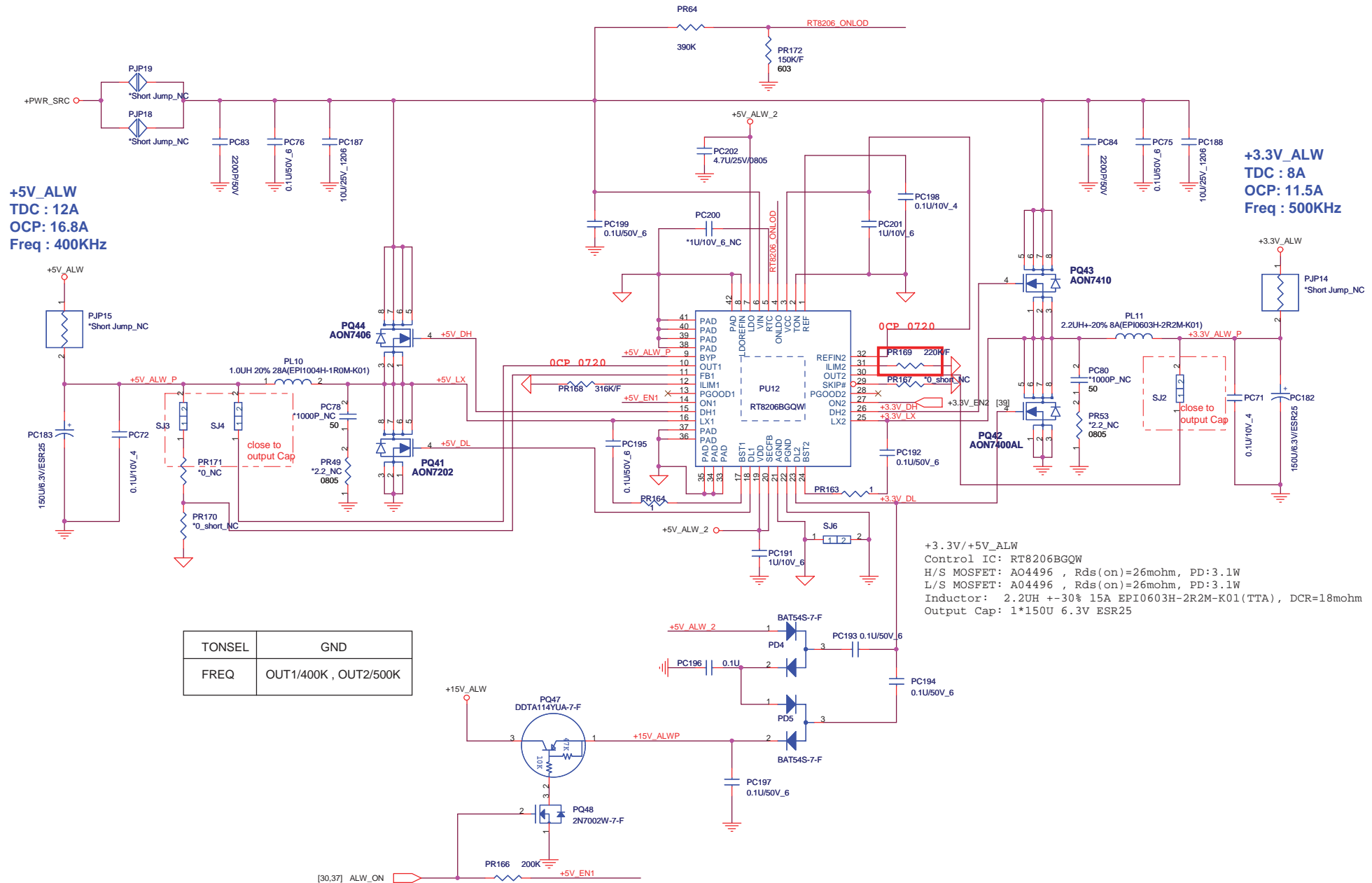




 <b>Quanta Computer Inc.</b> <b>PROJECT : R03A/V03A</b>		
Size	Document Number	Rev
	<b>Charger (ISL88731C)</b>	<b>2A</b>
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DC/DC +3V\_ALW/+5V\_ALW /+15V\_ALW

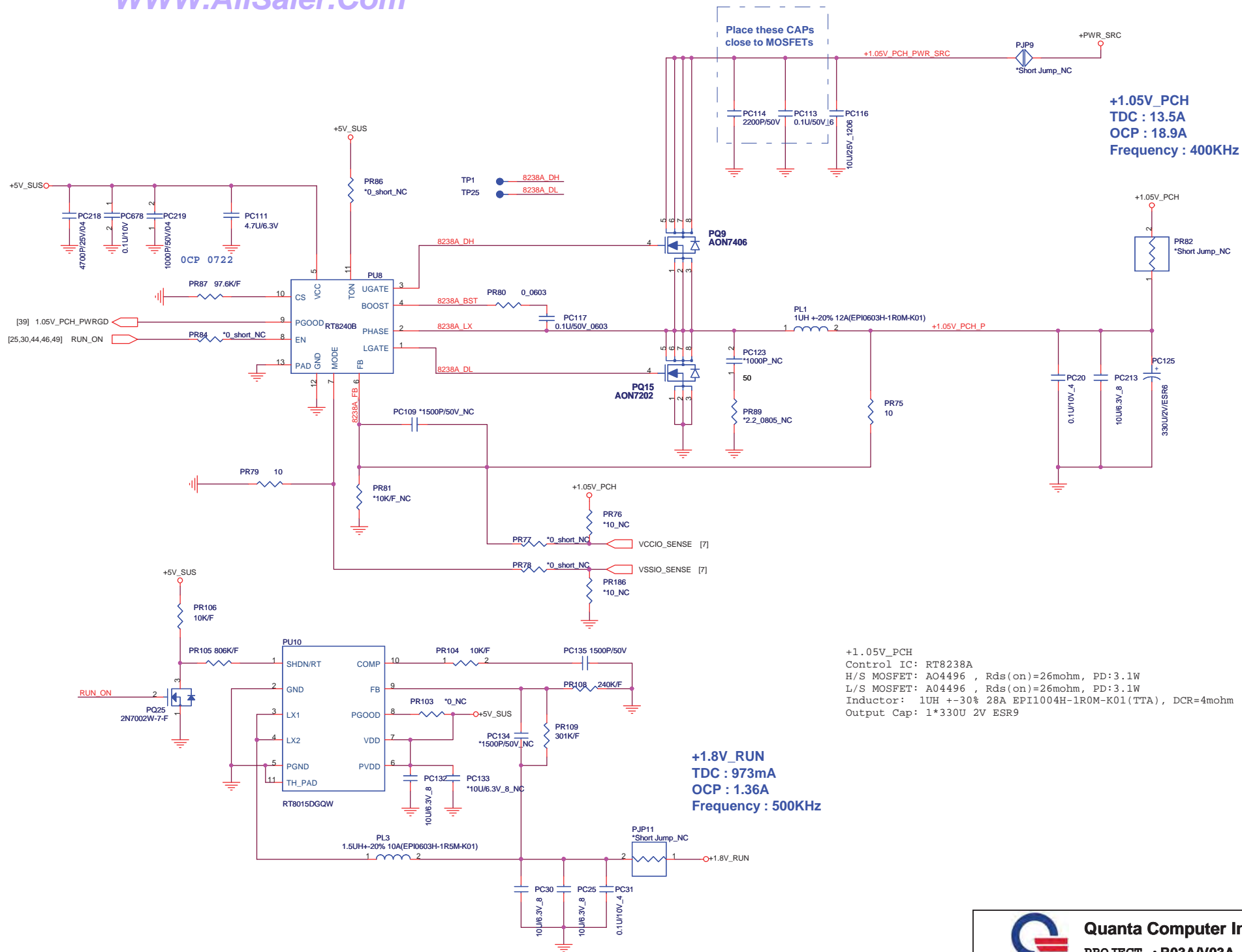


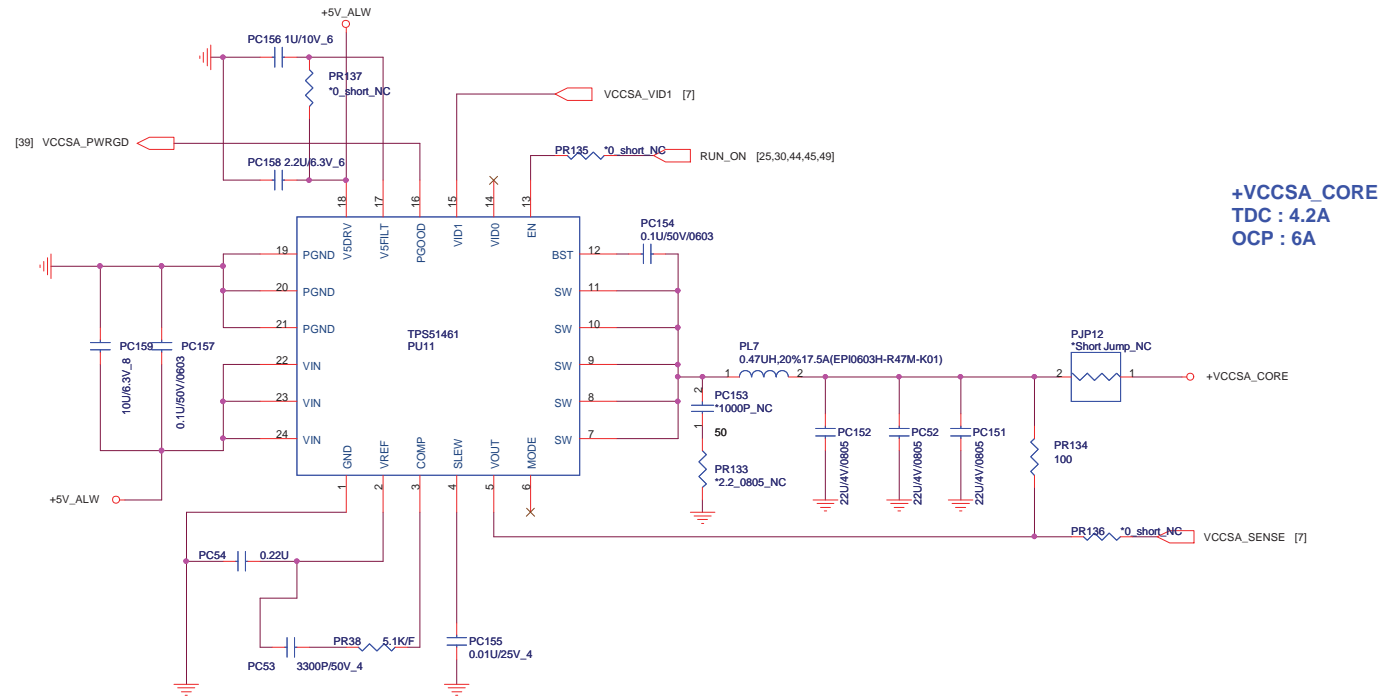


VDDQ output voltage selection

### Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)





+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low



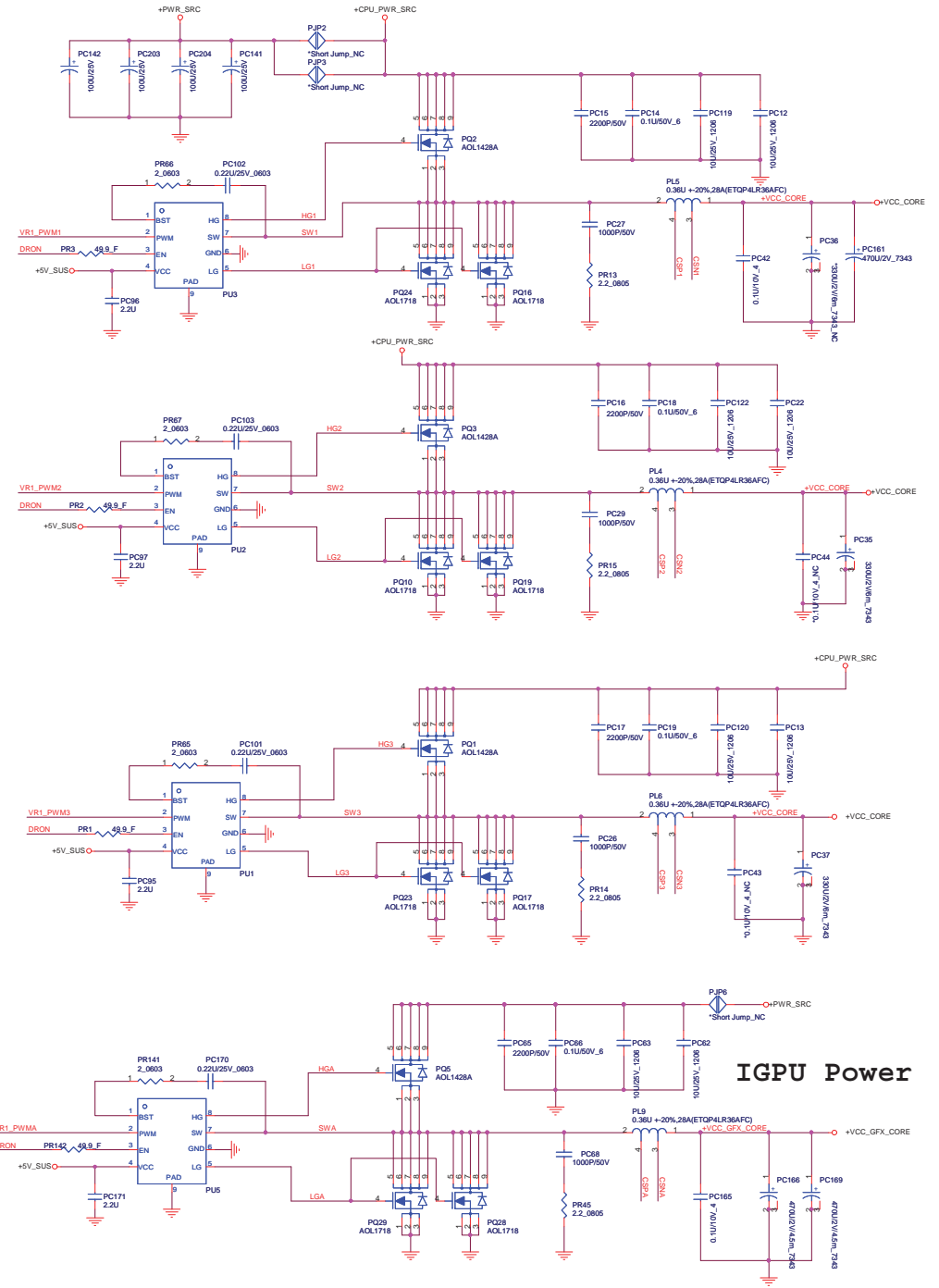
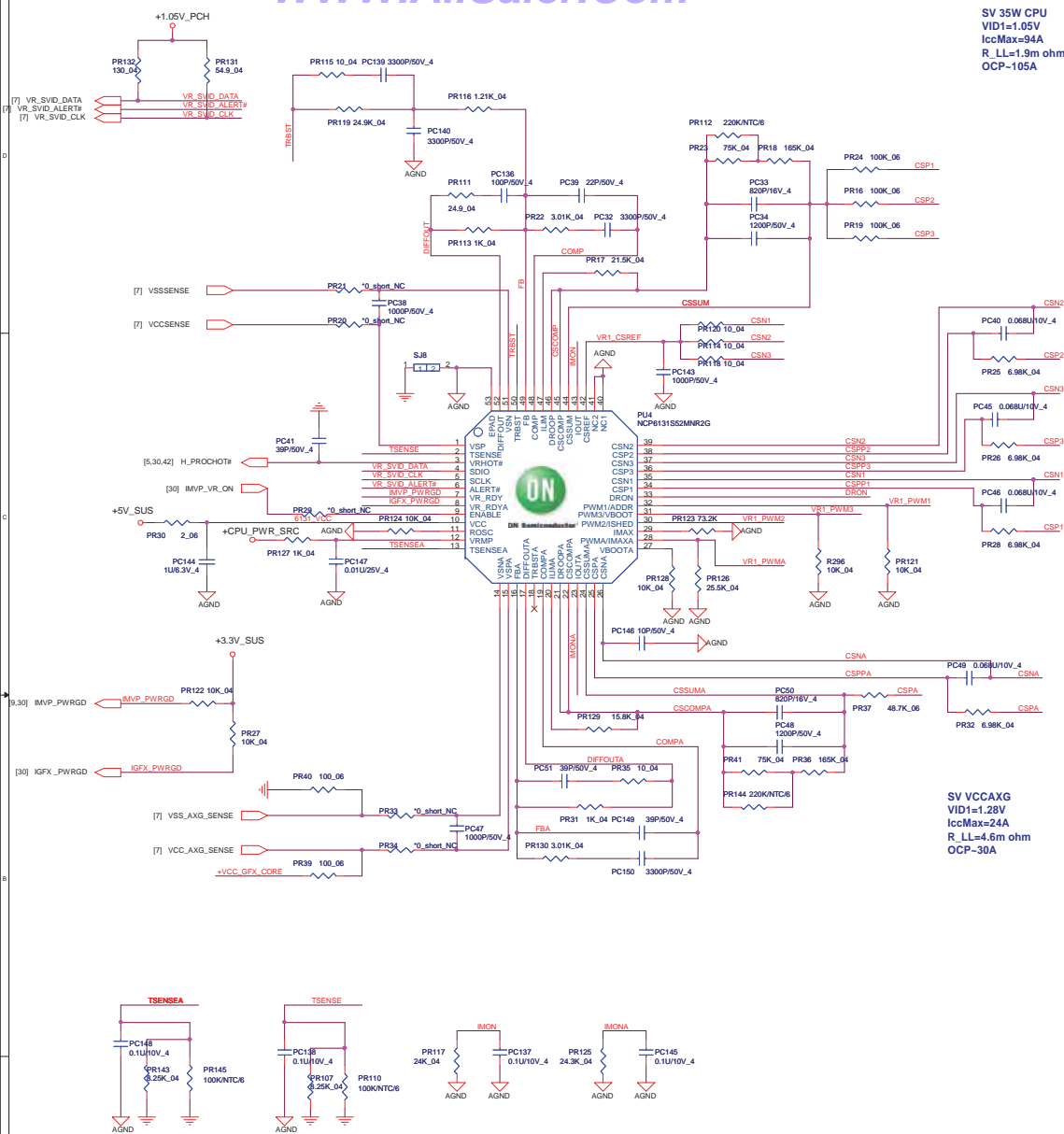
Quanta Computer Inc.

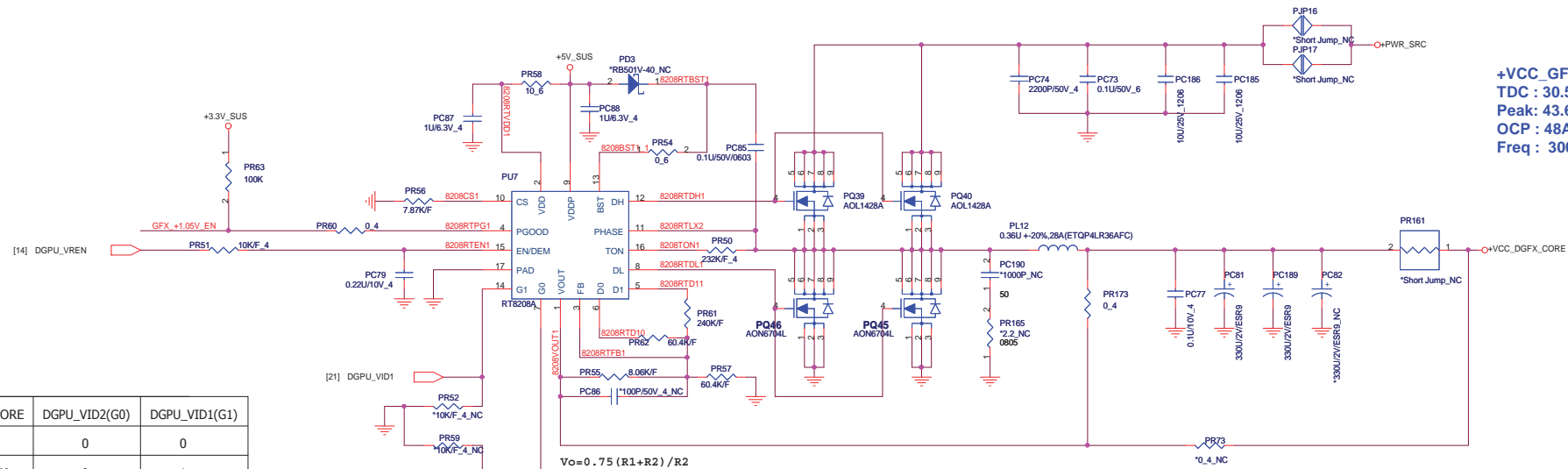
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VCCSA (TPS51461)

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+VCC_DGFX_CORE	DGPU_VID2(G0)	DGPU_VID1(G1)
0.85V	0	0
0.875V(NA)	0	1
0.95 V	1	0
0.975V	1	1

$$V_o = 0.75 (R1 + R2) / R2$$

