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QCL10 Schematics Document

AMD APU Trinity FS1r2 + FCH Hudson-M3 + GPU Seymour/Thames XT

2012-07-13

REV:1.0(A00)

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Title: Cover Page			
Size: B	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 1 of 50		

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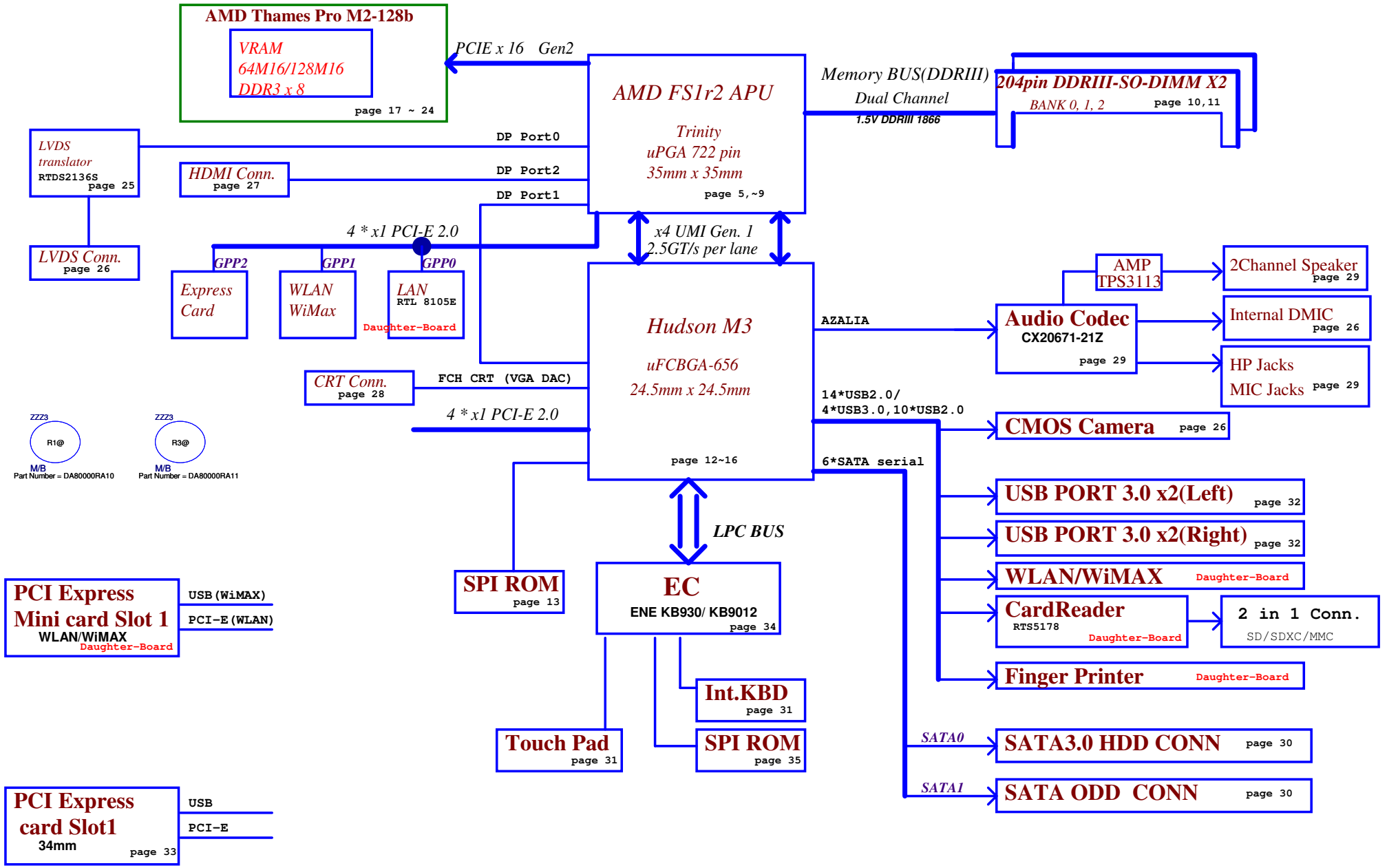

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Date: Monday, July 16, 2012	Sheet 2 of 50		

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+1.0VGS	1.0V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

FCH Hudson-M3 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	ExCARD
	PCIE3	NC
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	DEBUG PORT
Port1	WLAN
Port2	NC
Port3	FingerPrint
Port4	NC
Port5	NC
Port6	NC
Port7	CardReader
Port8	ExCARD
Port9	CAM
Port10	LP1
Port11	LP2
Port12	RP1
Port13	RP2

FCH Hudson-M3 USB Port List

Port0	LP1
Port1	LP2
Port2	RP1
Port3	RP2

EC SM Bus1 address

Device	Address	HEX
Smart Battery	000 1011	11h 0x16
Charger IC	000 1001	09h 0x12

EC SM Bus2 address

Device	Address	HEX
ADM1032ARMZ	100 1101	4Dh 0x9A
SB-TSI	100 1100	4Ch 0x98
RTD2136	100 1010	4Ah 0x94
GPU	100 0001	41h 0x82

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

BOM Structure

```
UMA@  : UMA only
DIS@  : DIS muxluss
45@   : 45 Level
9012@:  EC9012
930@:   EC930
INS@:  Inspiron
VOS@:  Vostro
M2@:  FCH M2
M3@:  FCH M3
FFS@:  FreeFallSensor
EXP@:  Express Card
FP@:  FingerPrint
EMC@: EMI&ESD part
SE@:  SEYMOUS GPU
CH@:  Chelsea GPU
X76@: VRAM
H2G@: Hynix 2G
S2G@: Samsung 2G
R1@:   R1 P/N for FCH,PCB
TMSR1@: R1 P/N for GPU,VRAM
R3@:   R3 P/N for FCH,PCB
TMSR3@: R3 P/N for GPU,VRAM
```

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Title	Notes List		
Size B	Document Number LA8251P		Rev 1.0
Date: Monday, July 16, 2012	Sheet 3 of 50		

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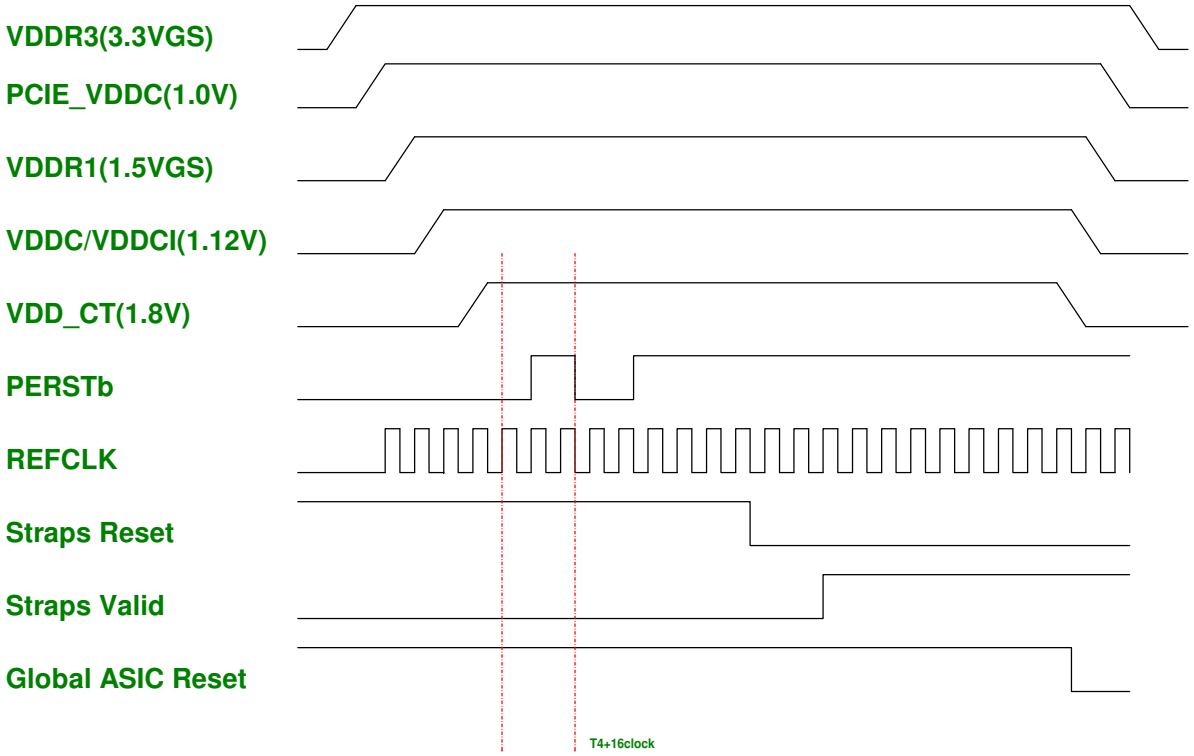
Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



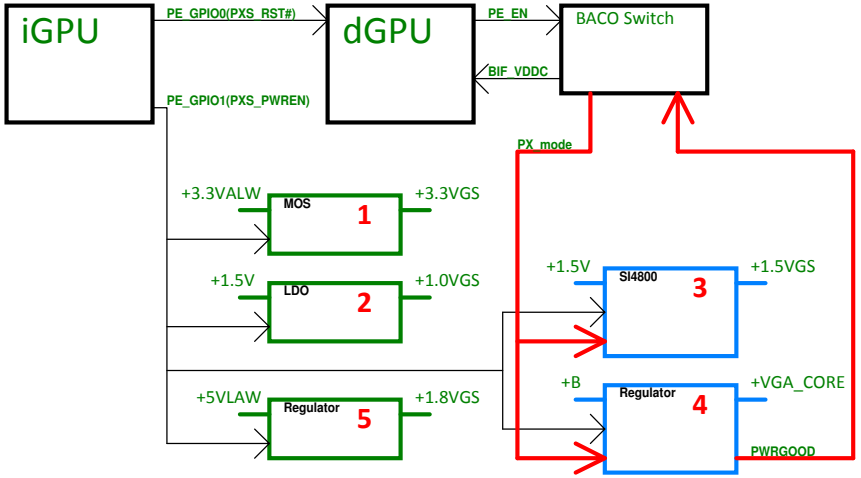
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28



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Title: dGPU Block Diagram

Size	Document Number	Rev
B	LA8251P	1.0

Date: Monday, July 16, 2012 Sheet 4 of 50

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<17> PCIE_CRX_GTX_P[0..15]
<17> PCIE_CRX_GTX_N[0..15]
PCIE_CTX_GRX_P[0..15] <17>
PCIE_CTX_GRX_N[0..15] <17>

U1A

PCI EXPRESS

PCIE_CRX_GTX_P0	AB8	P_GFX_RXP0	P_GFX_TXP0	AB2	PCIE_CTX_C_GRX_P0	C1	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P0
PCIE_CRX_GTX_N0	AB7	P_GFX_RXN0	P_GFX_TXN0	AB1	PCIE_CTX_C_GRX_N0	C2	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N0
PCIE_CRX_GTX_P1	AA9	P_GFX_RXP1	P_GFX_TXP1	AA3	PCIE_CTX_C_GRX_P1	C3	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P1
PCIE_CRX_GTX_N1	AA8	P_GFX_RXN1	P_GFX_TXN1	AA2	PCIE_CTX_C_GRX_N1	C4	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N1
PCIE_CRX_GTX_P2	AA5	P_GFX_RXP2	P_GFX_TXP2	Y5	PCIE_CTX_C_GRX_P2	C5	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P2
PCIE_CRX_GTX_N2	AA6	P_GFX_RXN2	P_GFX_TXN2	Y4	PCIE_CTX_C_GRX_N2	C6	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N2
PCIE_CRX_GTX_P3	Y8	P_GFX_RXP3	P_GFX_TXP3	Y2	PCIE_CTX_C_GRX_P3	C7	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P3
PCIE_CRX_GTX_N3	Y7	P_GFX_RXN3	P_GFX_TXN3	Y1	PCIE_CTX_C_GRX_N3	C8	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N3
PCIE_CRX_GTX_P4	W9	P_GFX_RXP4	P_GFX_TXP4	W3	PCIE_CTX_C_GRX_P4	C9	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P4
PCIE_CRX_GTX_N4	W8	P_GFX_RXN4	P_GFX_TXN4	W2	PCIE_CTX_C_GRX_N4	C10	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N4
PCIE_CRX_GTX_P5	W5	P_GFX_RXP5	P_GFX_TXP5	V5	PCIE_CTX_C_GRX_P5	C11	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P5
PCIE_CRX_GTX_N5	W6	P_GFX_RXN5	P_GFX_TXN5	V4	PCIE_CTX_C_GRX_N5	C12	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N5
PCIE_CRX_GTX_P6	V8	P_GFX_RXP6	P_GFX_TXP6	V2	PCIE_CTX_C_GRX_P6	C13	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P6
PCIE_CRX_GTX_N6	V7	P_GFX_RXN6	P_GFX_TXN6	V1	PCIE_CTX_C_GRX_N6	C14	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N6
PCIE_CRX_GTX_P7	U9	P_GFX_RXP7	P_GFX_TXP7	U3	PCIE_CTX_C_GRX_P7	C15	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P7
PCIE_CRX_GTX_N7	U8	P_GFX_RXN7	P_GFX_TXN7	U2	PCIE_CTX_C_GRX_N7	C16	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N7
PCIE_CRX_GTX_P8	U5	P_GFX_RXP8	P_GFX_TXP8	T5	PCIE_CTX_C_GRX_P8	C17	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P8
PCIE_CRX_GTX_N8	U6	P_GFX_RXN8	P_GFX_TXN8	T4	PCIE_CTX_C_GRX_N8	C18	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N8
PCIE_CRX_GTX_P9	T8	P_GFX_RXP9	P_GFX_TXP9	T2	PCIE_CTX_C_GRX_P9	C19	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P9
PCIE_CRX_GTX_N9	T7	P_GFX_RXN9	P_GFX_TXN9	T1	PCIE_CTX_C_GRX_N9	C20	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N9
PCIE_CRX_GTX_P10	R9	P_GFX_RXP10	P_GFX_TXP10	R3	PCIE_CTX_C_GRX_P10	C21	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P10
PCIE_CRX_GTX_N10	R8	P_GFX_RXN10	P_GFX_TXN10	R2	PCIE_CTX_C_GRX_N10	C22	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N10
PCIE_CRX_GTX_P11	R5	P_GFX_RXP11	P_GFX_TXP11	P5	PCIE_CTX_C_GRX_P11	C23	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P11
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PCIE_CRX_GTX_P13	N9	P_GFX_RXP13	P_GFX_TXP13	N3	PCIE_CTX_C_GRX_P13	C27	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P13
PCIE_CRX_GTX_N13	N8	P_GFX_RXN13	P_GFX_TXN13	N2	PCIE_CTX_C_GRX_N13	C28	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N13
PCIE_CRX_GTX_P14	N5	P_GFX_RXP14	P_GFX_TXP14	M5	PCIE_CTX_C_GRX_P14	C29	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P14
PCIE_CRX_GTX_N14	N6	P_GFX_RXN14	P_GFX_TXN14	M4	PCIE_CTX_C_GRX_N14	C30	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N14
PCIE_CRX_GTX_P15	M8	P_GFX_RXP15	P_GFX_TXP15	M2	PCIE_CTX_C_GRX_P15	C31	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_P15
PCIE_CRX_GTX_N15	M7	P_GFX_RXN15	P_GFX_TXN15	M1	PCIE_CTX_C_GRX_N15	C32	DIS@	1	2	0.1U 0402 16V7K	PCIE_CTX_GRX_N15

GRAPHICS

LAN <31> PCIE_CRX_DTX_P0	AE5	P_GPP_RXP0	P_GPP_TXP0	AD5	PCIE_CTX_C_DRX_P0	C33	1	2	0.1U 0402 16V7K	PCIE_CTX_DRX_P0	<31>
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WLAN <31> PCIE_FRX_DTX_P1	AD8	P_GPP_RXP1	P_GPP_TXP1	AD2	PCIE_FTX_C_DRX_P1	0.1U 0402 16V7K	1	2	C35	PCIE_FTX_DRX_P1	<31> WLAN
<31> PCIE_FRX_DTX_N1	AD7	P_GPP_RXN1	P_GPP_TXN1	AD1	PCIE_FTX_C_DRX_N1	0.1U 0402 16V7K	1	2	C36	PCIE_FTX_DRX_N1	<31>
ExCARD <33> PCIE_FRX_DTX_P2	AC9	P_GPP_RXP2	P_GPP_TXP2	AC3	PCIE_FTX_C_DRX_P2	0.1U 0402 16V7K	1	2	C50	PCIE_FTX_DRX_P2	<33> ExCARD
<33> PCIE_FRX_DTX_N2	AC8	P_GPP_RXN2	P_GPP_TXN2	AC2	PCIE_FTX_C_DRX_N2	0.1U 0402 16V7K	1	2	C51	PCIE_FTX_DRX_N2	<33>
	AC5	P_GPP_RXP3	P_GPP_TXP3	AB5							
	AC6	P_GPP_RXN3	P_GPP_TXN3	AB4							

New Add

Move from FCH for WLAN/EXP PCIE I/F. 20110819

GPP

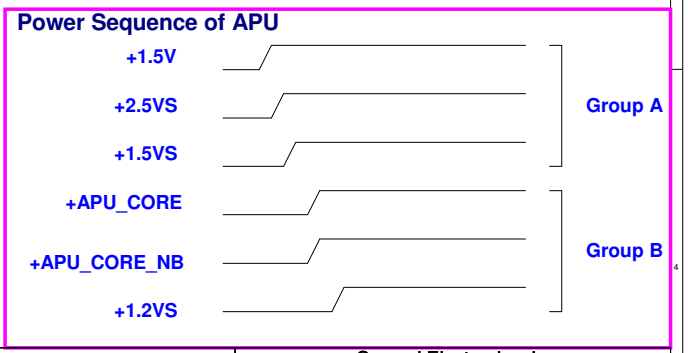
<12> UMI_RXP0	AG8	P_UMI_RXP0	P_UMI_TXP0	AG2	UMI_TXP0_C	C37	1	2	0.1U 0402 16V7K	UMI_TXP0	<12>
<12> UMI_RXN0	AG9	P_UMI_RXN0	P_UMI_TXN0	AG3	UMI_TXN0_C	C38	1	2	0.1U 0402 16V7K	UMI_TXN0	<12>
<12> UMI_RXP1	AG6	P_UMI_RXP1	P_UMI_TXP1	AF4	UMI_TXP1_C	C39	1	2	0.1U 0402 16V7K	UMI_TXP1	<12>
<12> UMI_RXN1	AG5	P_UMI_RXN1	P_UMI_TXN1	AF5	UMI_TXN1_C	C40	1	2	0.1U 0402 16V7K	UMI_TXN1	<12>
<12> UMI_RXP2	AF7	P_UMI_RXP2	P_UMI_TXP2	AF1	UMI_TXP2_C	C41	1	2	0.1U 0402 16V7K	UMI_TXP2	<12>
<12> UMI_RXN2	AF8	P_UMI_RXN2	P_UMI_TXN2	AF2	UMI_TXN2_C	C42	1	2	0.1U 0402 16V7K	UMI_TXN2	<12>
<12> UMI_RXP3	AE8	P_UMI_RXP3	P_UMI_TXP3	AE2	UMI_TXP3_C	C43	1	2	0.1U 0402 16V7K	UMI_TXP3	<12>
<12> UMI_RXN3	AE9	P_UMI_RXN3	P_UMI_TXN3	AE3	UMI_TXN3_C	C44	1	2	0.1U 0402 16V7K	UMI_TXN3	<12>

UMI

+1.2VS — 1 — R1 196_0402_1% — 2 — P_ZVDDP AG11 — P_ZVDDP
P_ZVSS AH11 — P_ZVSS — 1 — R2 196_0402_1% — 2

CONN@ LOTES_ACA-ZIF-109-P12-A_FS1R2

Power Sequence of APU



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Size: Custom	Document Number: LA8251P		Rev: 1.0
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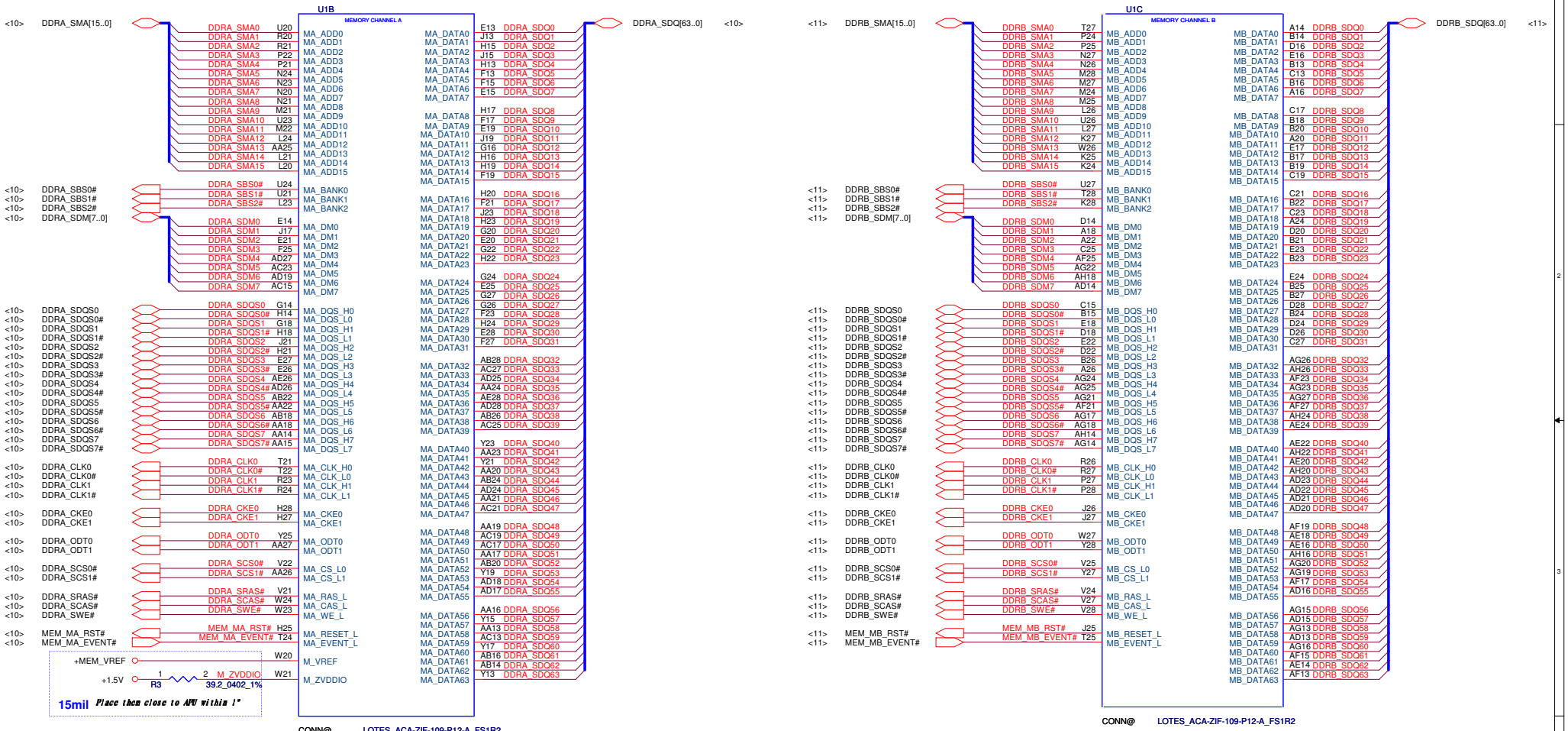

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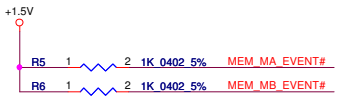
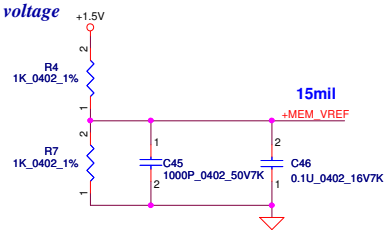


0.75V reference voltage



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/01	Deciphered Date 2013/01/01	Title: FS1r2 DDRIII Memory I/F

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Date: Monday, July 16, 2012	Sheet 6 of 50		

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Place near APU

U1D

ANALOG/DISPLAY/MISC

LVDS

DP0_TXP0_C <25> — C56 0.1U_0402_16V7K — DP0_TXP0 L3
DP0_TXN0_C <25> — C48 0.1U_0402_16V7K — DP0_TXN0 L2
DP0_TXP1_C <25> — C58 0.1U_0402_16V7K — DP0_TXP1 K5
DP0_TXN1_C <25> — C53 0.1U_0402_16V7K — DP0_TXN1 K4

To FCH

ML_VGA_TXP0 <13> — C63 0.1U_0402_16V7K — DP1_TXP0 H5
ML_VGA_TXN0 <13> — C64 0.1U_0402_16V7K — DP1_TXN0 H4
ML_VGA_TXP1 <13> — C65 0.1U_0402_16V7K — DP1_TXP1 H2
ML_VGA_TXN1 <13> — C66 0.1U_0402_16V7K — DP1_TXN1 H1
ML_VGA_TXP2 <13> — C67 0.1U_0402_16V7K — DP1_TXP2 G3
ML_VGA_TXN2 <13> — C68 0.1U_0402_16V7K — DP1_TXN2 G2
ML_VGA_TXP3 <13> — C69 0.1U_0402_16V7K — DP1_TXP3 F2
ML_VGA_TXN3 <13> — C70 0.1U_0402_16V7K — DP1_TXN3 F1

HDMI

DP2_TXP0 <27> — DP2_TXP0 L9
DP2_TXN0 <27> — DP2_TXN0 L8
DP2_TXP1 <27> — DP2_TXP1 L5
DP2_TXN1 <27> — DP2_TXN1 L6
DP2_TXP2 <27> — DP2_TXP2 K8
DP2_TXN2 <27> — DP2_TXN2 K7
DP2_TXP3 <27> — DP2_TXP3 J6
DP2_TXN3 <27> — DP2_TXN3 J5

APU_CLK <12> — AE11
APU_CLK# <12> — AD11
APU_DISP_CLK <12> — AB11
APU_DISP_CLK# <12> — AA11

APU_SVC <46> — B3
APU_SVD <46> — A3
APU_SVT <46> — C3

APU_SIC — AG12
APU_SID — AH12

<12> APU_RST# — AF10
<12,46> APU_PWRGD — AB12

APU_PROCHOT# — AC10
APU_THERMTRIP# — AE12
ALERT_L — AF12

APU_TDI — H10
APU_TDO — J10
APU_TCK — F10
APU_TMS — G10
APU_TRST# — F9
APU_DBRDY — G9
APU_DBREQ# — H9

Route as differential with VSS_SENSE

<46> APU_VDD_SEN_L — B4
<46> APU_VDDNB_SEN_H — C5
<46> APU_VDD_SEN_H — A4
A5
C4
B5

CONN@ LOTES_ACA-ZIF-109-P12-A_FS1R2

DP0_AUXP — D1 DP0_AUXP — C47 0.1U_0402_16V7K — DP0_AUXP_C <25> — To LVDS Translater
DP0_AUXN — D2 DP0_AUXN — C49 0.1U_0402_16V7K — DP0_AUXN_C <25>
DP1_AUXP — E1 ML_VGA_AUXP — C57 0.1U_0402_16V7K — ML_VGA_AUXP_C <13> — To FCH
DP1_AUXN — E2 ML_VGA_AUXN — C52 0.1U_0402_16V7K — ML_VGA_AUXN_C <13>
DP2_AUXP — D5 — HDMI_CLK <27> — To HDMI
DP2_AUXN — D6 — HDMI_DATA <27>
DP3_AUXP — E5
DP3_AUXN — E6
DP4_AUXP — F5
DP4_AUXN — F6
DP5_AUXP — G5
DP5_AUXN — G6

DP0_HPD — D3 — LVDS_HPD_R <9>
DP1_HPD — E3 — ML_VGA_HPD <9>
DP2_HPD — D7 — HDMI_DET <27>
DP3_HPD — E7
DP4_HPD — F7
DP5_HPD — G7

DP_BLON — C6
DP_DIGON — B6
DP_VARY_BL — A6 — DP_INT_PWM <9>
C1 DP_AUX_ZVSS — R16 150_0402_1%
DP_AUX_ZVSS

AD12
TEST6 — M18 — T5
TEST9 — N18 — T6
TEST10 — F11 — T1
TEST14 — G11 — T2
TEST15 — H11 — T3
TEST16 — J11 — T4
TEST17 — F12 APU_TEST17 — R18 1K_0402_5%
TEST18 — G12 APU_TEST19 — R19 1K_0402_5%
TEST19 — J12 APU_TEST20 — R21 1K_0402_5%
TEST20 — H12 APU_TEST24 — R22 1K_0402_5%
TEST24 — AE10 TEST25_H — R23 510_0402_1%
TEST25_H — AD10 TEST25_L — R24 510_0402_1% — +1.2VS
TEST25_L — L10 — T7
TEST28_H — M10 — T8
TEST28_L — P19
TEST30_H — R19
TEST30_L — K22 APU_TEST31 — R27 39.2_0402_1%
TEST31 — J19
TEST32_H — N19
TEST32_L — AA12 APU_TEST35 — R28 300_0402_5% — +1.5V
TEST35 — R29 300_0402_5%
R30 10K_0402_5% — +3VALW
FS1R2 — W10 FS1R2
DMAACTIVE_L — AC12 — ALLOW_STOP <12>
TEST4 — P18 — T11
TEST5 — R18 — T12

RSVD1 — Y10
RSVD2 — AA10
RSVD3 — Y12
RSVD4 — K21

TEST35 change to PU for HDMI can not output 20110126

If not used, pins are left unconnected (DG ref.)
20101111

DP0_AUXP R25 1.8K_0402_5%
DP0_AUXN R58 1.8K_0402_5%
ML_VGA_AUXP R10 1.8K_0402_5%
ML_VGA_AUXN R11 1.8K_0402_5%

Asserted as an input to force the processor into the HTC-active state

+1.5V — R13 1K_0402_5%
+3VS — R12 10K_0402_5%
Q1 DEL 2011/11/28
<12,39,46> APU_PROCHOT# — APU_PROCHOT# — H_PROCHOT#_EC <34>
2N7002K_SOT23-3 Q6

THERMTRIP shutdown temperature: 125 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

+1.5V — R20 1K_0402_5%
R17 10K_0402_5%
APU_THERMTRIP# — Q2 MMBT3904_NL_SOT23-3 — H_THERMTRIP# <14>

+1.5V — R26 10K_0402_5%
ALERT_L — Q5 MMBT3904_NL_SOT23-3
R55 0_0402_5% — APU_ALERT#_FCH <13>
R56 0_0402_5% — APU_ALERT#_EC <34>

CPU TSI interface level shift

+1.5V
R36 1K_0402_5% — APU_SVT
R39 1K_0402_5% — APU_SVC
R41 1K_0402_5% — APU_SVD
R42 1K_0402_5% — APU_SIC
R44 1K_0402_5% — APU_SID
R46 1K_0402_5% — APU_SID
R48 1K_0402_5% — ALLOW_STOP

+1.5VS
R57 1K_0402_5%
R52 300_0402_5% — APU_RST#
R54 300_0402_5% — APU_PWRGD

Allow_STOP leakage issue

+3VS
R615 4.7K_0402_5% — HDMI_CLK
R616 4.7K_0402_5% — HDMI_DATA

+5VS — R14 10K_0402_5%
+3VS — R31 31.6K_0402_1%
C71 0.1U_0402_16V4Z
R32 30K_0402_1%

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

APU_SID — Q78A — DMN66D0LDW-7_SOT363-6 — APU_SID_R — Q3 BSH111 1N_SOT23-3 — EC_SMB_DA — R33 0_0402_5% — EC_SMB_DA2 <18,25,34> — To EC
R610 0_0402_5% — FCH_SID <14> — To FCH

SID_G
TSI_G

APU_SIC — Q78B — DMN66D0LDW-7_SOT363-6 — APU_SIC_R — Q4 BSH111 1N_SOT23-3 — EC_SMB_CK — R34 0_0402_5% — EC_SMB_CK2 <18,25,34> — To EC
R612 0_0402_5% — FCH_SIC <14> — To FCH

HDT Debug conn

+1.5V — R37 1K_0402_5%
APU_TRST# — R43 0_0402_5%
R45 10K_0402_5%
R47 10K_0402_5%
R49 10K_0402_5%

JHDT1
APU_TCK — R35 1K_0402_5%
APU_TMS — R38 1K_0402_5%
APU_TDI — R40 1K_0402_5%
APU_TDO
APU_PWRGD
APU_RST#
APU_DBRDY
APU_DBREQ# — R50 1K_0402_5%
R51 0_0402_5% — APU_TEST19
R53 0_0402_5% — APU_TEST18
SAMTE_ASP-136446-07-B
CONN@

Aux signal are re-configured as I2C signals for DDC. APU AUX pin are 3.3V tolerant
Default follow PAWGX setting for pull-high resistor value

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

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Compal Electronics, Inc.

Title: FS1r2 Display/MISC/HDT

Size: B25 Custom | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 7 of 50

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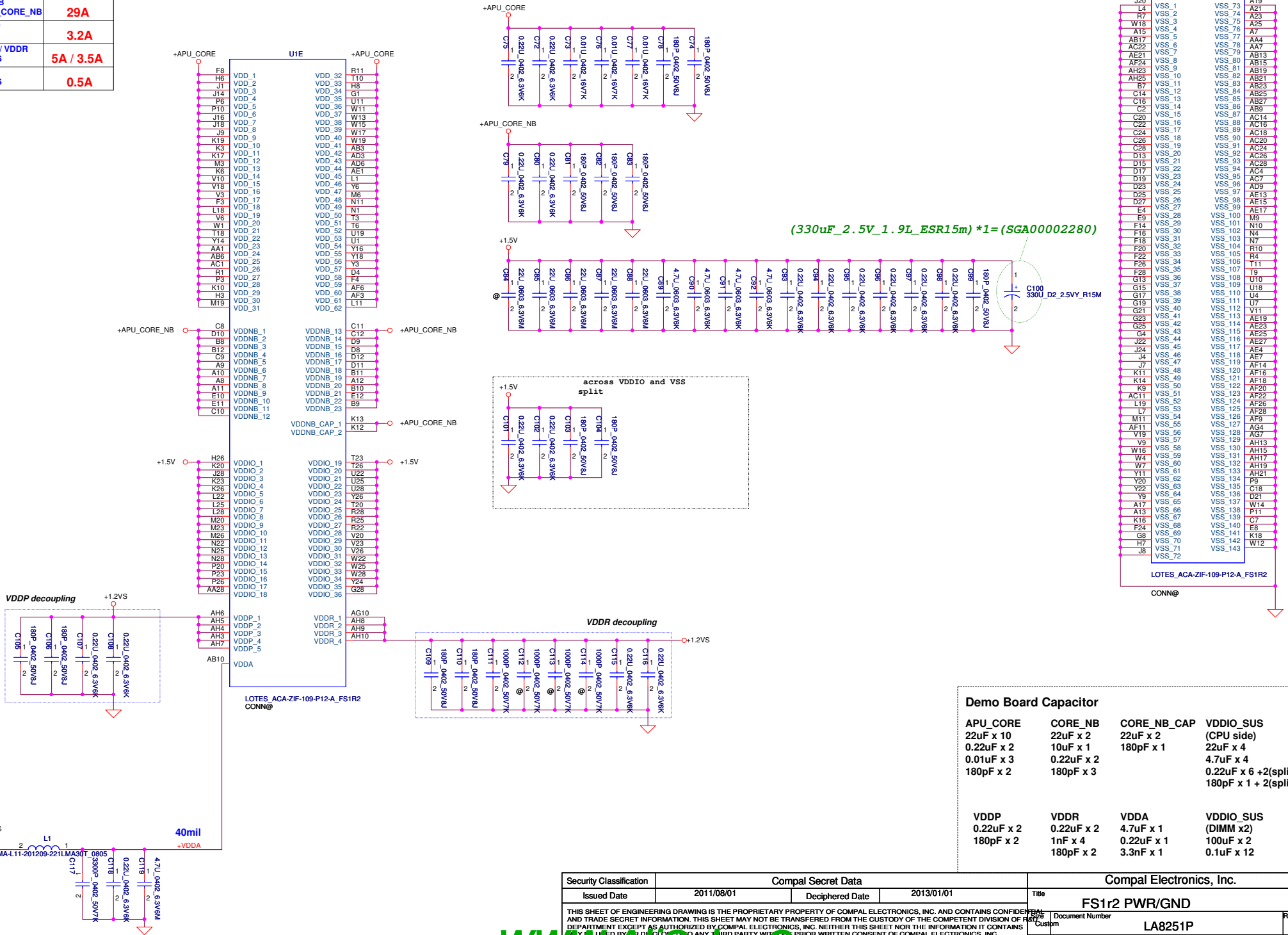
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

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Compal Electronics, Inc.

Title: FS1r2 PWR/GND

Size: B (625 Custom) | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 8 of 50

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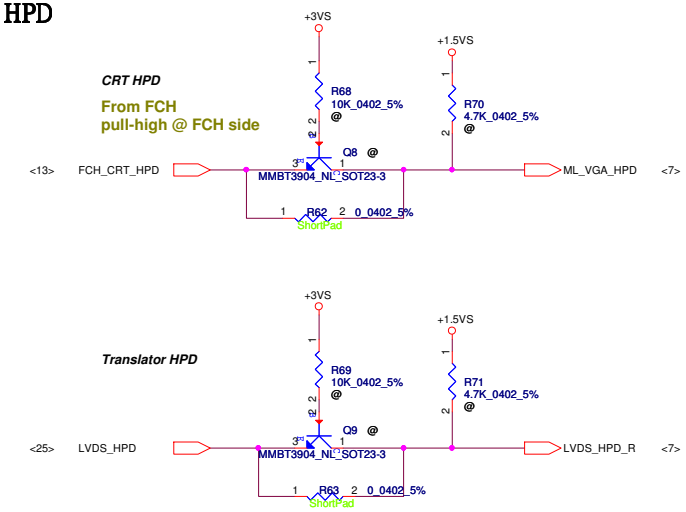
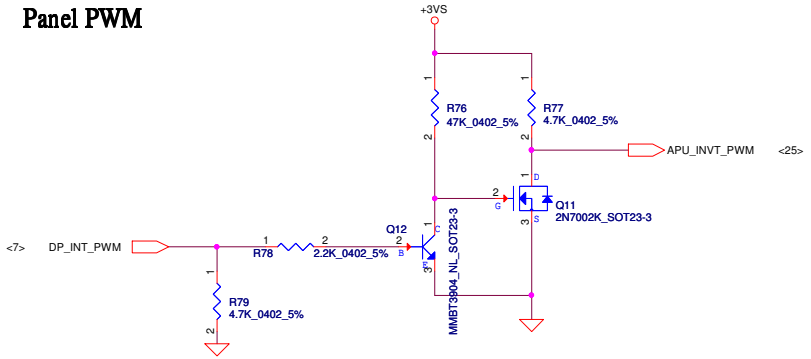
HPD



Panel PWM



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Issued Date	2011/08/01	Deciphered Date	2013/01/01

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Compal Electronics, Inc.

Title: FS1r2 Signal Level Shifter

Size	Document Number	Rev
Custom	LA8251P	1.0

Date: Monday, July 16, 2012 Sheet 9 of 50

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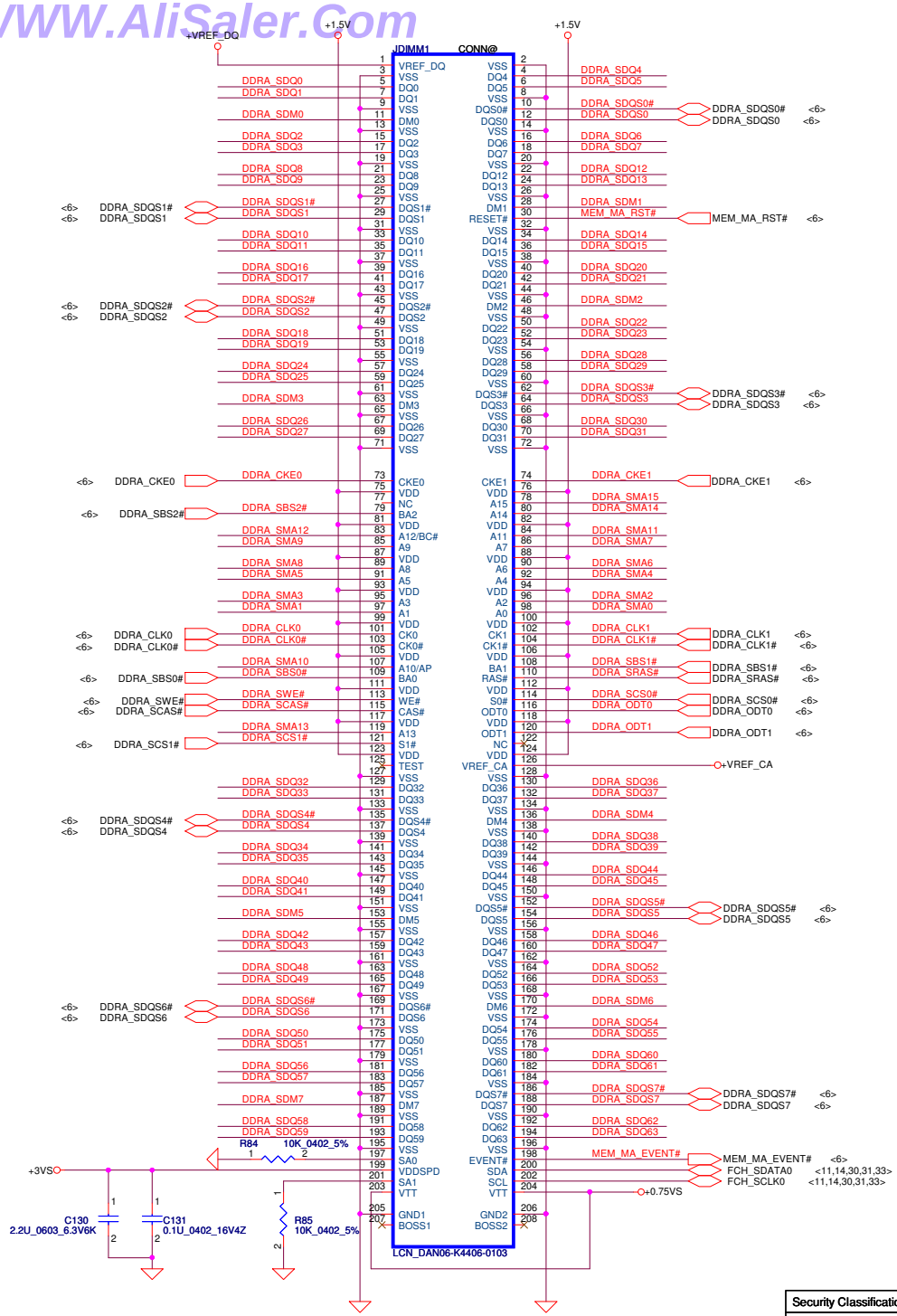


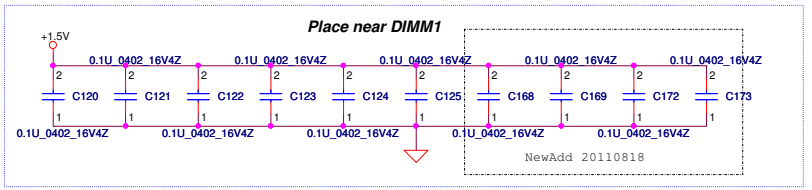
Reverse H:4mm

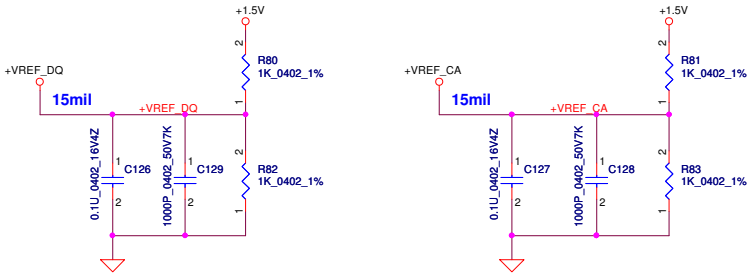
<Address: 00>

DDRA_SDQ[0..63] — DDRA_SDQ[0..63] <6>

DDRA_SDM[0..7] — DDRA_SDM[0..7] <6>

DDRA_SMA[0..15] — DDRA_SMA[0..15] <6>





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Issued Date	2011/08/01	Deciphered Date 2013/01/01	Title: DDRIII SO-DIMM 1
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 10 of 50		

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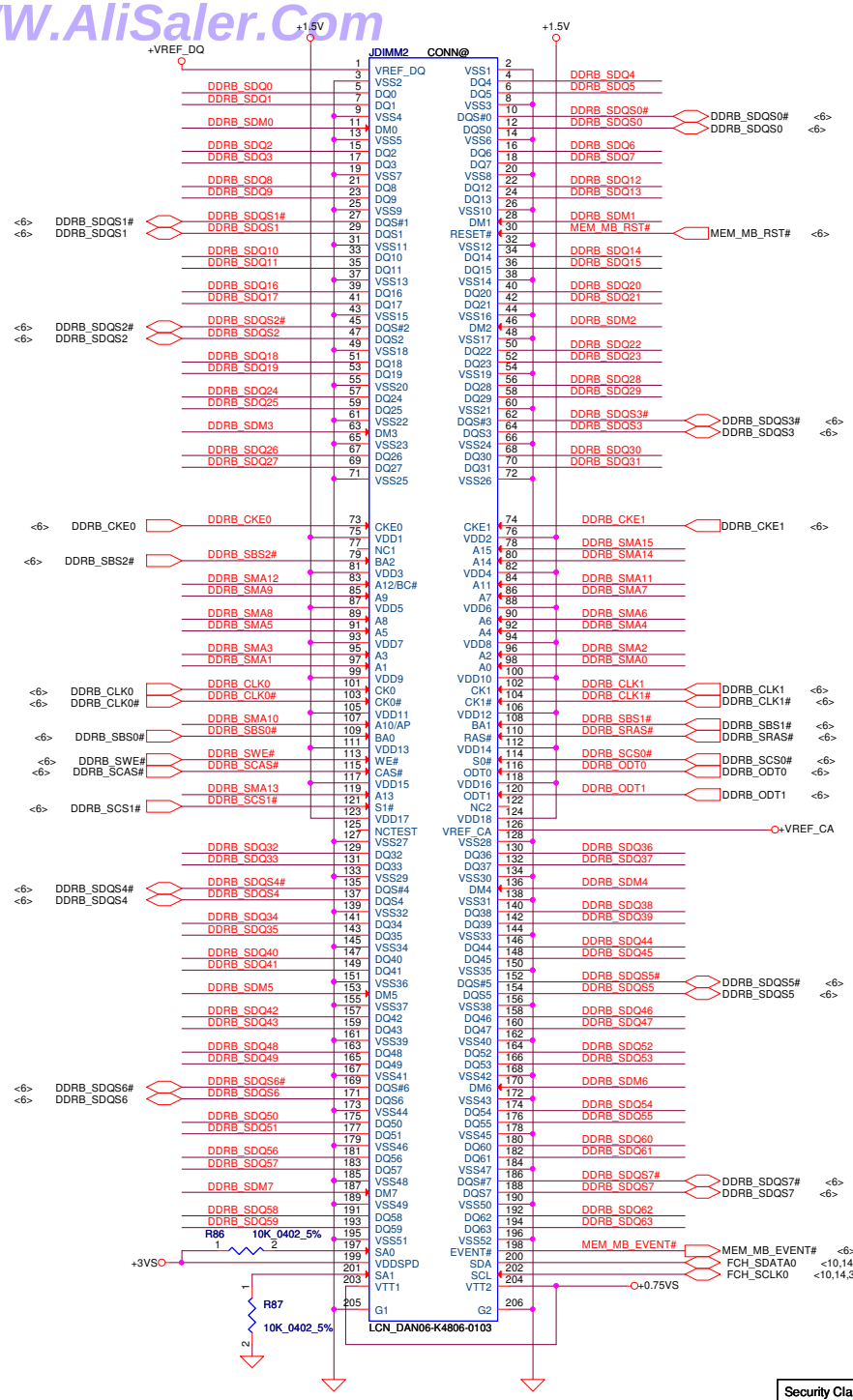
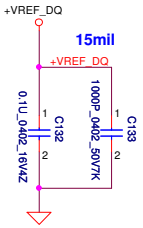
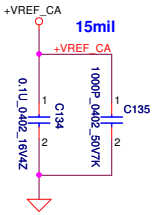
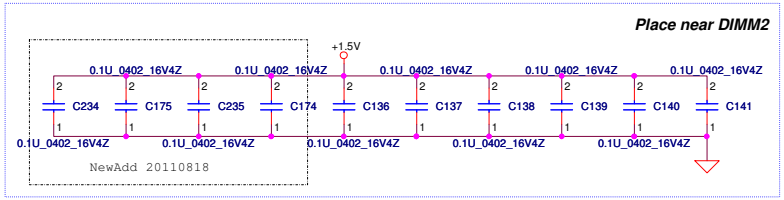
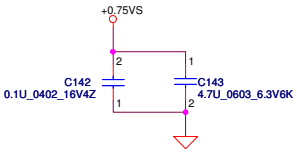


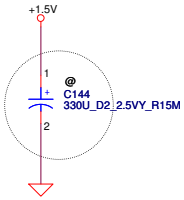
DDRB_SDQ[0..63] DDRB_SDQ[0..63] <6>
DDRB_SDM[0..7] DDRB_SDM[0..7] <6>
DDRB_SMA[0..15] DDRB_SMA[0..15] <6>











Reserve H:8mm

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Issued Date	2011/08/01	Deciphered Date	2013/01/01
Title	DDRIII SO-DIMM 2		
Size Custom	Document Number LA8251P		Rev 1.0
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R90/ C146 close to FCH

R90 100K_0402_5%
C146 150P_0402_50V8J
PLT_RST#

U2
R3@
FCH-M3
Part Number = SA000043I3L

U2A

APU_PCIE_RST# C → R89 33_0402_5% → A_RST#

UMI_RXP0 C147 0.1U_0402_16V7K UMI_RXP0_C
UMI_RXN0 C148 0.1U_0402_16V7K UMI_RXN0_C
UMI_RXP1 C149 0.1U_0402_16V7K UMI_RXP1_C
UMI_RXN1 C150 0.1U_0402_16V7K UMI_RXN1_C
UMI_RXP2 C151 0.1U_0402_16V7K UMI_RXP2_C
UMI_RXN2 C152 0.1U_0402_16V7K UMI_RXN2_C
UMI_RXP3 C153 0.1U_0402_16V7K UMI_RXP3_C
UMI_RXN3 C154 0.1U_0402_16V7K UMI_RXN3_C

UMI_TXP0 UMI_TXN0 UMI_TXP1 UMI_TXN1 UMI_TXP2 UMI_TXN2 UMI_TXP3 UMI_TXN3

R94 590_0402_1% PCIE_CALRP
R88 2K_0402_1% PCIE_CALRN
+VDDAN_11_PCIE

Move PCIE device to APU. 20110819

R95 2K_0402_1% CLK_CALRN
+1.1VS_CKVDD

SS
For "EXT" CLK mode, input to PCIE,

NSS
APU DISP <7> APU_DISP_CLK <7> APU_DISP_CLK#

APU <7> APU_CLK <7> APU_CLK#

VGA <17> CLK_PCIE_VGA <17> CLK_PCIE_VGA#
0_0402_5% ShortPad R98 CLK_PCIE_VGA_R
0_0402_5% ShortPad R99 CLK_PCIE_VGA#_R

SS
WLAN <31> CLK_PCIE_WLAN <31> CLK_PCIE_WLAN#
0_0402_5% ShortPad R102 CLK_PCIE_WLAN_R
0_0402_5% ShortPad R103 CLK_PCIE_WLAN#_R

GLAN <31> CLK_PCIE_LAN <31> CLK_PCIE_LAN#
0_0402_5% ShortPad R100 CLK_PCIE_LAN_R
0_0402_5% ShortPad R101 CLK_PCIE_LAN#_R

CLOSE TO R680
<37> LAN_X1 → R801 → CLK_LAN_25M
0_0402_5% @

ExCARD <33> CLK_PCIE_XCRD <33> CLK_PCIE_XCRD#
RX7 EXP@ 0_0402_5% CLK_PCIE_XCRD_R
RX8 EXP@ 0_0402_5% CLK_PCIE_XCRD#_R
New Add

CLOSE TO X1
<37> PCH_X1 → R800 → 25M_X1
0_0402_5% @

<31> CLK_LAN_25M → R680 @ 22_0402_5% CLK_LAN_25M_R → 14M_25M_48M_OSC

CH27 10P_0402_50V8J~D
CH28 10P_0402_50V8J~D
YH2 25MHZ_10PF_7V25000014 (GND OSC GND OSC)
25M_X1 C31 25M_X1
R106 1M_0402_5% 25M_X1 25M_X2
C33 25M_X2

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)
APU_PCIE_RST #: Reset PCIE device on APU

+3VALW
C789 @ 0.1U_0402_16V4Z
MC74VHC1G08DFT2G SC70 5P U43
APU_PCIE_RST# C → @R692 33_0402_5%
C790 @ 150P_0402_50V8J
R693 @ 8.2K_0402_5%
@R695 0_0402_5%
R694 0_0402_5% ShortPad
APU_PCIE_RST# <17>
PLT_RST# <31,33,34>
QCL10 LAN-APU,WLAN&ExCARD-FCH 20110803

R692/ C790 close to FCH

HUDSON-2

PCI_CLKS
PCICLK0 AF3
PCICLK1/GPO36 AF1 → PCI_CLK1 <16>
PCICLK2/GPO37 AF5
PCICLK3/GPO38 AG2 → PCI_CLK3 <16>
PCICLK4/14M_OSC/GPO39 AF6 → PCI_CLK4 <16>
PCIRST# AB5

PCI EXPRESS INTERFACES
PCIE_RST# A_RST#
PCIE_CALRP PCIE_CALRN
GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N
GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N

PCI INTERFACE
AD0/GPIO0 AJ3
AD1/GPIO1 AL5
AD2/GPIO2 AG4
AD3/GPIO3 AL6
AD4/GPIO4 AH3
AD5/GPIO5 AJ5
AD6/GPIO6 AL1
AD7/GPIO7 AN5
AD8/GPIO8 AN6
AD9/GPIO9 AJ1
AD10/GPIO10 AL8
AD11/GPIO11 AL3
AD12/GPIO12 AM7
AD13/GPIO13 AJ6
AD14/GPIO14 AK7
AD15/GPIO15 AN8
AD16/GPIO16 AG9
AD17/GPIO17 AM11
AD18/GPIO18 AJ10
AD19/GPIO19 AL12
AD20/GPIO20 AK11
AD21/GPIO21 AN12
AD22/GPIO22 AG12
AD23/GPIO23 AE12 → PCI_AD23 <16>
AD24/GPIO24 AC12 → PCI_AD24 <16>
AD25/GPIO25 AE13 → PCI_AD25 <16>
AD26/GPIO26 AF13 → PCI_AD26 <16>
AD27/GPIO27 AH13 → PCI_AD27 <16>
AD28/GPIO28 AH14
AD29/GPIO29 AD15
AD30/GPIO30 AC15
AD31/GPIO31 AE16
CBE0# AN3
CBE1# AJ8
CBE2# AN10
CBE3# AD12
FRAME# AG10
DEVSEL# AK9
IRDY# AL10
TRDY# AF10
PAR AE10
STOP# AH1
PERR# AM9
SERR# AH8
REQ0# AG15
REQ1#/GPIO40 AG13
REQ2#/CLK_REQ8#/GPIO41 AF15
REQ3#/CLK_REQ5#/GPIO42 AM17
GNT0# AD16 → T14 → XCRD_CLKREQ#
GNT1#/GPO44 AD13 → R223 @ 0_0402_5% → PXS_RST# <14,17>
GNT2#/SD_LED/GPO45 AD21 → R224 @ 0_0402_5% → PXS_PWREN <14,19,42,44>
GNT3#/CLK_REQ7#/GPIO46 AK17 → XCRD_CLKREQ# <33>
CLKRUN# AD19
LOCK# AH9
INTE#/GPIO32 AF18 → HDD_FALL_INT → HDD_FALL_INT <30>
INTF#/GPIO33 AE18
INTG#/GPIO34 AC16
INTH#/GPIO35 AD18

+3VS
EXP@ 8.2K_0402_5% RX6

CLOCK GENERATOR
CLK_CALRN
PCIE_RCLKP PCIE_RCLKN
DISP_CLKP DISP_CLKN
DISP2_CLKP DISP2_CLKN
APU_CLKP APU_CLKN
SLT_GFX_CLKP SLT_GFX_CLKN
GPP_CLK0P GPP_CLK0N
GPP_CLK1P GPP_CLK1N
GPP_CLK2P GPP_CLK2N
GPP_CLK3P GPP_CLK3N
GPP_CLK4P GPP_CLK4N
GPP_CLK5P GPP_CLK5N
GPP_CLK6P GPP_CLK6N
GPP_CLK7P GPP_CLK7N
GPP_CLK8P GPP_CLK8N

LPC
LPCCLK0 B25 CLK_EC33M 1 R222 2 22_0402_5% → CLK_PCI_EC <16,34>
LPCCLK1 D25 → LPC_CLK1 <16>
LAD0 C28 → LPC_AD0 <34>
LAD1 A26 → LPC_AD1 <34>
LAD2 A29 → LPC_AD2 <34>
LAD3 A31 → LPC_AD3 <34>
LFRAME# B27 → LPC_FRAME# <34>
LDRQ0# AE27
LDRQ1#/CLK_REQ6#/GPIO49 AE19 → SERIRQ <34>
SERIRQ/GPIO48

APU
DMA_ACTIVE# G25
PROCHOT# E28 APU_PROCHOT#_R R15 @ 0_0402_5% → ALLOW_STOP <7> APU_PROCHOT# <39,46,7>
APU_PG E26 → APU_PWRGD <46,7>
LDT_STP# G26
APU_RST# F26 → APU_RST# <7>

S5_PLUS
S5_CORE_EN H7
RTCCLK F1 → RTC_CLK <16,34>
INTRUDER_ALERT# F3
VDDBT_RTC_G E6 → +VDDBT_RTC
32K_X1 G2 → 32K_X1
32K_X2 G4 → 32K_X2

C158 18P_0402_50V8J 32K_X1
R107 20M_0402_5%~D
32.768KHZ_12.5PF_9H03200019 Y1
C159 18P_0402_50V8J 32K_X2
Close to HUDSON-M2/3

CLOSE TO Y1
<37> FCH_RTCX1 → R803 → 32K_X1
0_0402_5% @

APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

+RTCBATT → R135 510_0402_5% +VCOIN
+3VLP
D8 RB751V40_SC76-2 +VCOIN_RTC
D5 RB751V40_SC76-2
R105 510_0402_5% W=20mils W=20mils
C156 1U_0402_6.3V6K
CLRP1 @ SHORT PADS
R109 10M_0402_5% @
for Clear CMOS

218-0755097 A14 HUDSON-M3_FCBGA656

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Compal Electronics, Inc.

Title: FCH PCIE/CLK/PCI/LPC/RTC

Size	Document Number	Rev
Custom	LA8251P	1.0

Date: Monday, July 16, 2012 Sheet 12 of 50

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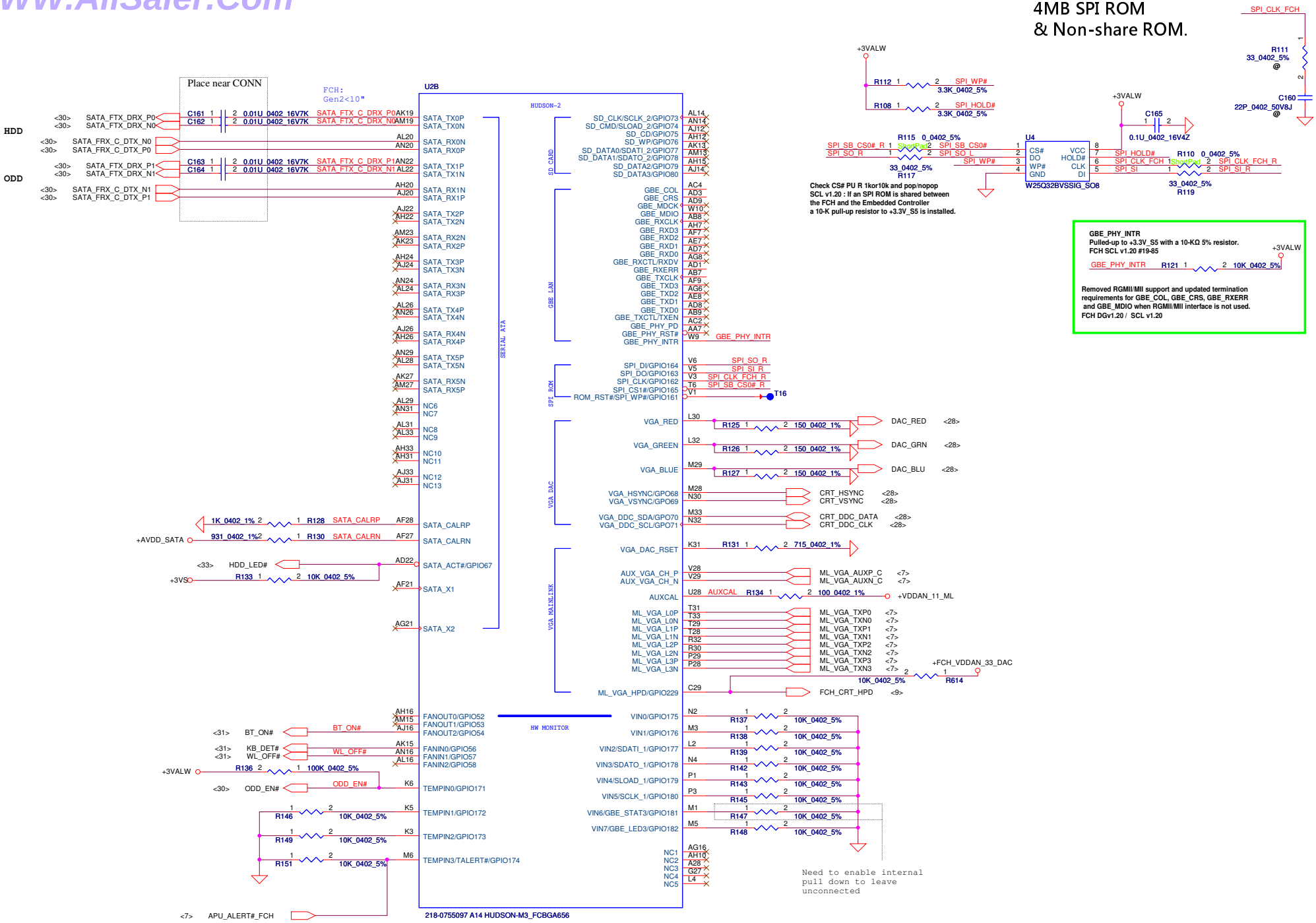
4MB SPI ROM & Non-share ROM.



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Compal Electronics, Inc.			
Title	FCH SATA/SPI/VGA/HWM/SD		
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 13 of 50		

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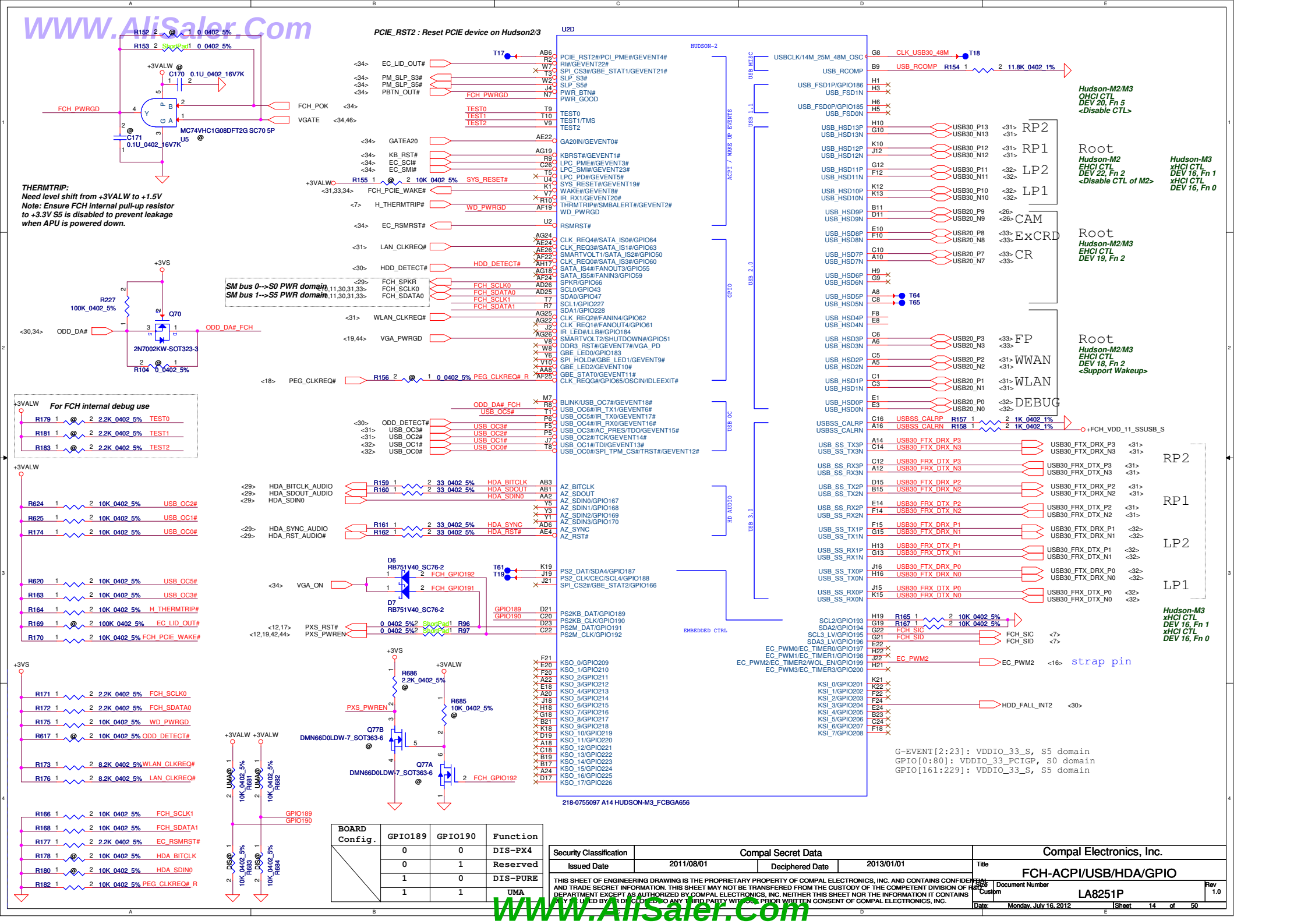

BOARD Config.	GPIO189	GPIO190	Function
	0	0	DIS-PX4
	0	1	Reserved
	1	0	DIS-PURE
	1	1	UMA

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Compal Electronics, Inc.

Title: FCH-ACPI/USB/HDA/GPIO

Size	Document Number	Rev
B2S Custom	LA8251P	1.0

Date: Monday, July 16, 2012 | Sheet 14 of 50

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U2C

HUDSON-2

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

LDO_CAP: Internally generated 1.8V supply for the RGB outputs
For A11: Cap = 1nF
For A12, Cap = DNI

+VDDXL_3.3V
Tie to +3.3V_S5 rail if USB3 Wake is supported; otherwise, tie to +3.3V_S0 rail.
Hudson-2 designs: Tie to +3.3V_S0 rail.

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDCR_11_SSUSB_S Connected to VSS.

218-0755097 A14 HUDSON-M3_FCBGA656

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Compal Electronics, Inc.

Title: FCH-PWR

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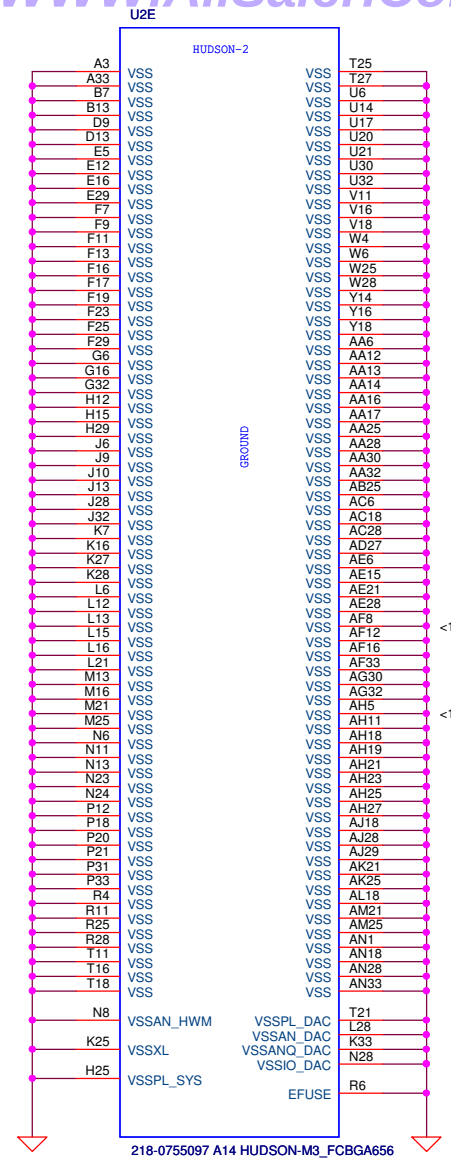


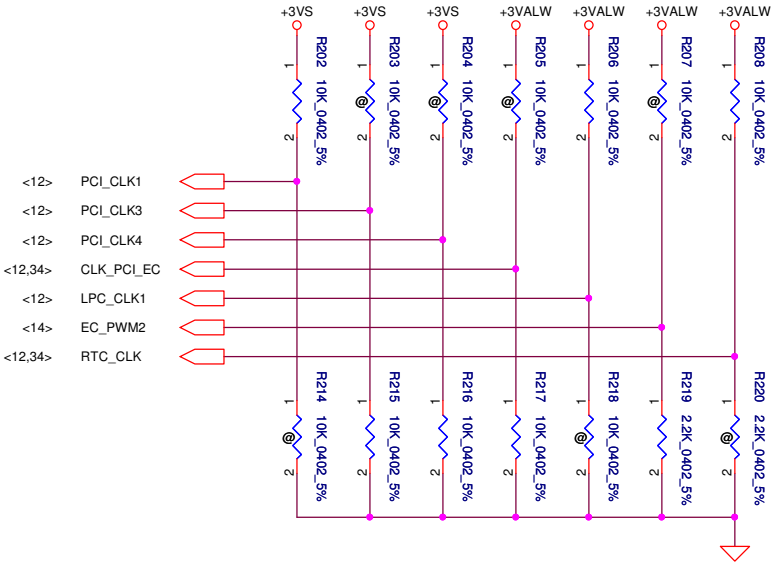
STRAP PINS

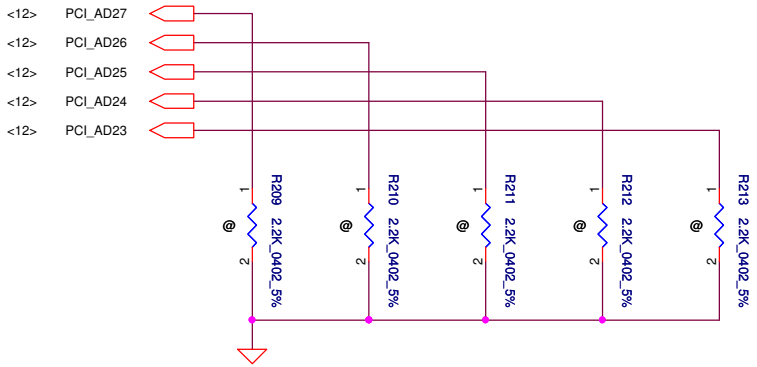
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





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			Size: B; Document Number: LA8251P; Rev: 1.0
			Date: Monday, July 16, 2012; Sheet 16 of 50

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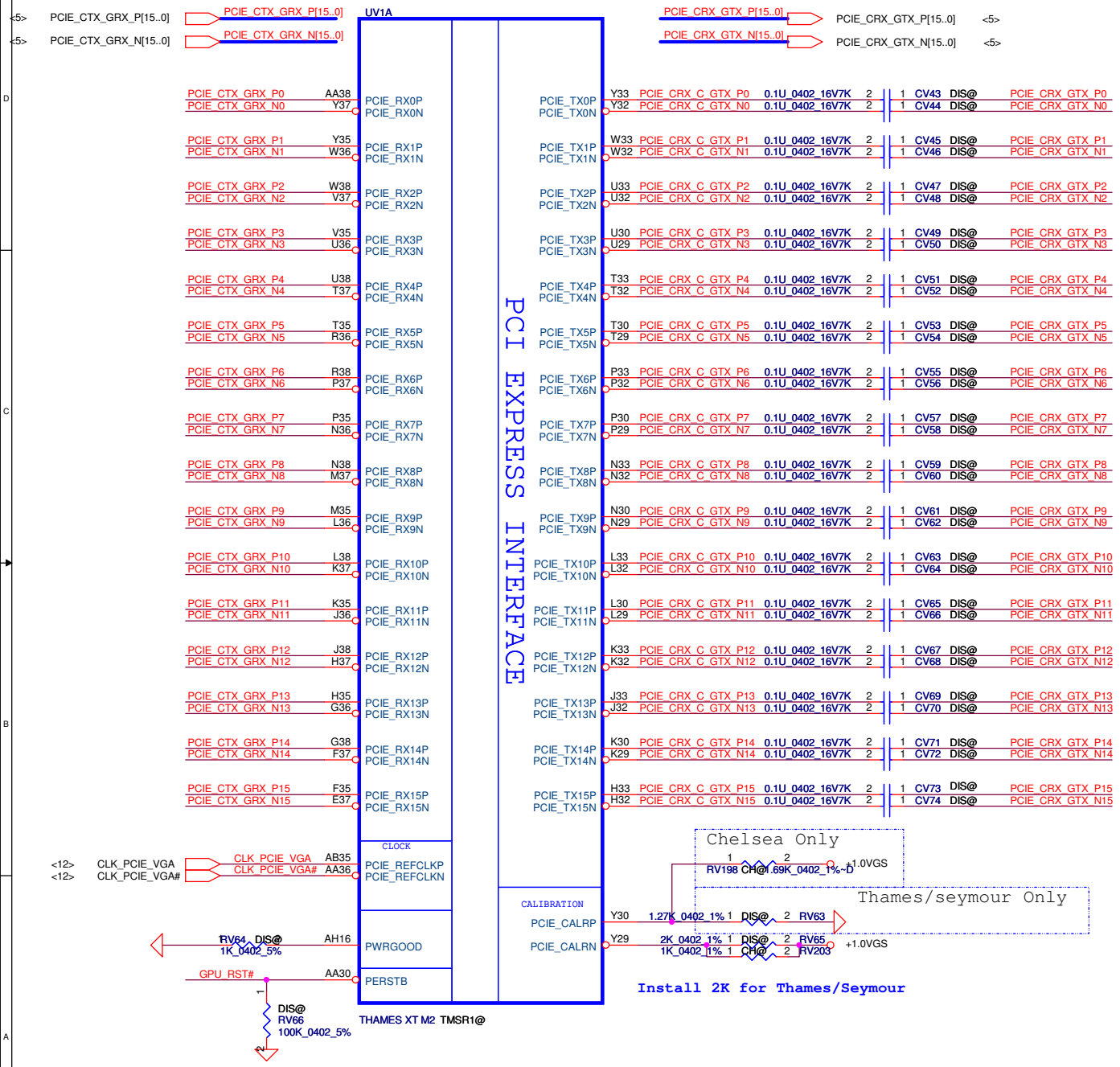
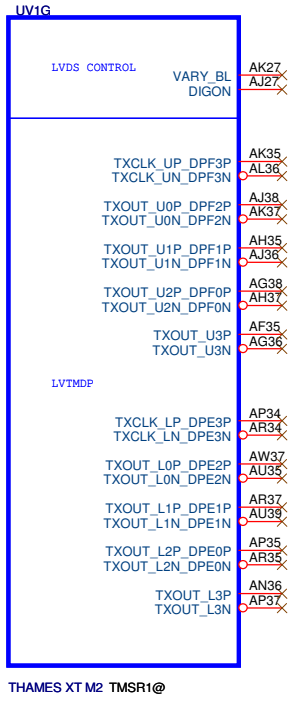
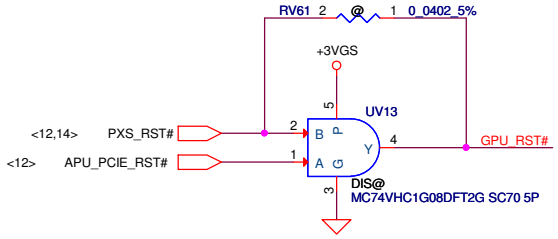
GFX PCIE LANE REVERSAL



LVDS Interface





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Title	ATI_SeymourXT_M2_PCIE/LVDS		
Size	Document Number		Rev
Custom	LA8251P		1.0
Date:	Monday, July 16, 2012	Sheet	17 of 50

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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BIF_VGA DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	H2SYNC			0
RSVD	GENERICC			0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
★64MX16 (1G) Hynix 1GB PN:SA00004LS20	RV67 1	RV70 0	RV72 0	PT
★64MX16 (1G) Samsung 1GB PN:SA00004GS0L	RV68 0	RV69 1	RV72 0	PT
128M16 (2G) Hynix 2GB PN:SA00003YO00	RV67 1	RV70 0	RV71 1	
128M16 (2G) Samsung 2GB PN:SA00004TQ00	RV68 0	RV69 1	RV71 1	

Not Share via for other GND

Reserved test pad of CRT Signals for debug

Add 12/8

NC_TSVSSQ should be tied to GND on Thames/Seymour

0.60 V level, Please VREFG Divider ans cap close to ASIC

XTALIN Voltage Swing: 1.8 V

Add 12/6 for MLPS

CLOSE TO YV1

Internal VGA Thermal Sensor

VGA Thermal Sensor ADM1032ARMZ

Closed to GPU

Address:100_1101

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Title: ATI_SeymourXT_M2_Main_MSIC

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Date: Monday, July 16, 2012 | Sheet 18 of 50

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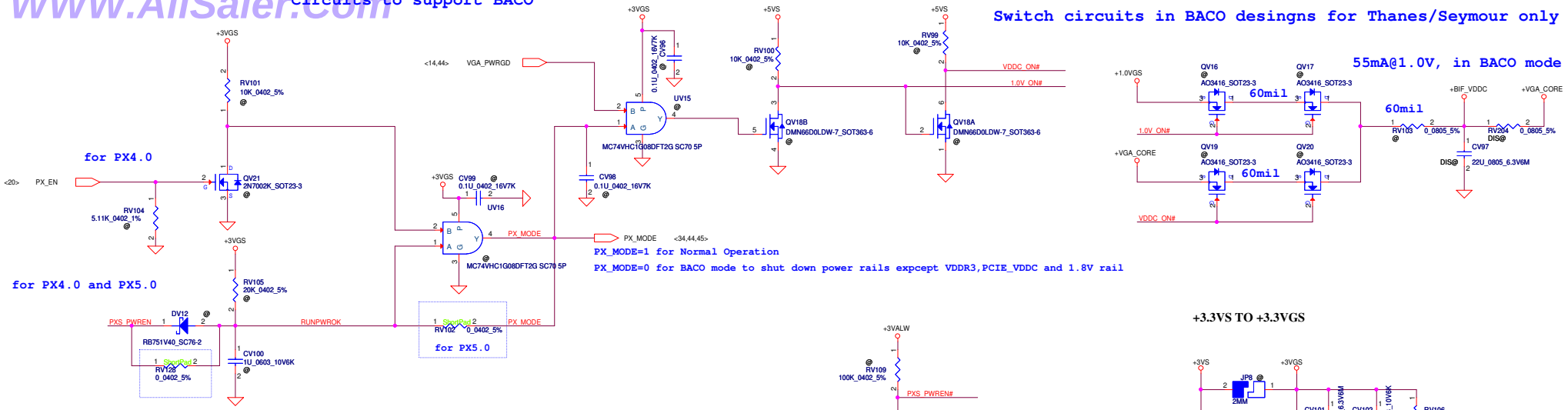
Circuits to support BACO

Switch circuits in BACO desingns for Thanes/Seymour only

55mA@1.0V, in BACO mode



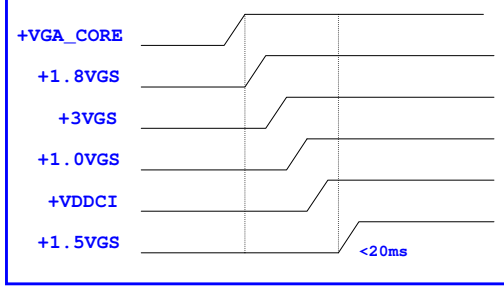
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS OFF

PX4.0 +3VGS, +1.0VGS,+1.8VGS ON

PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Chelsea



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Title	ATI_SeymourXT_M2_BACO POWER		
Size C	Document Number LA8251P		Rev 1.0
Date: Monday, July 16, 2012		Sheet 19 of 50	

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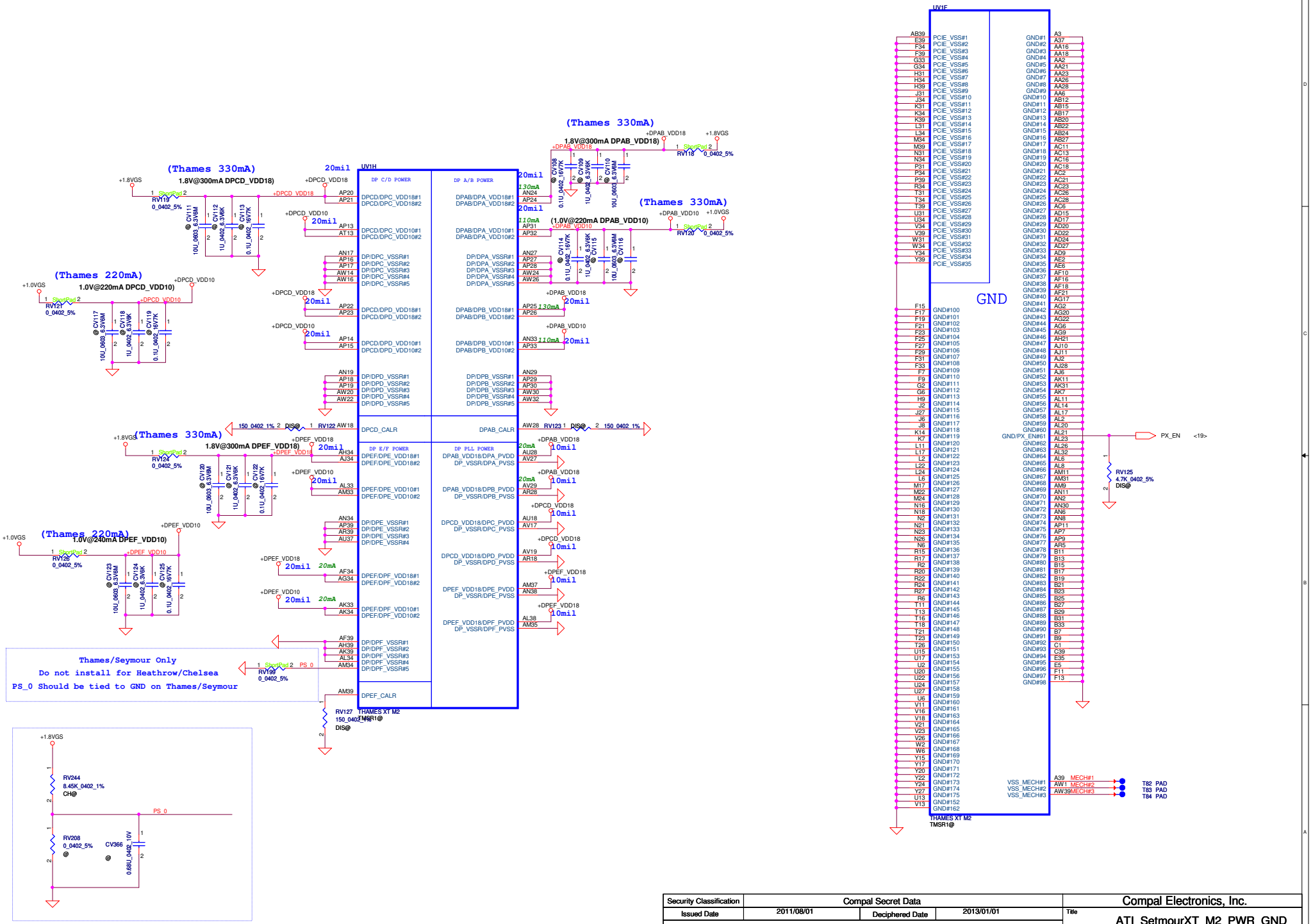

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Compal Electronics, Inc.			
Title	ATI_SetmourXT_M2_PWR_GND		
Size C	Document Number LA8251P		Rev 1.0
Date: Monday, July 16, 2012		Sheet 20 of 50	

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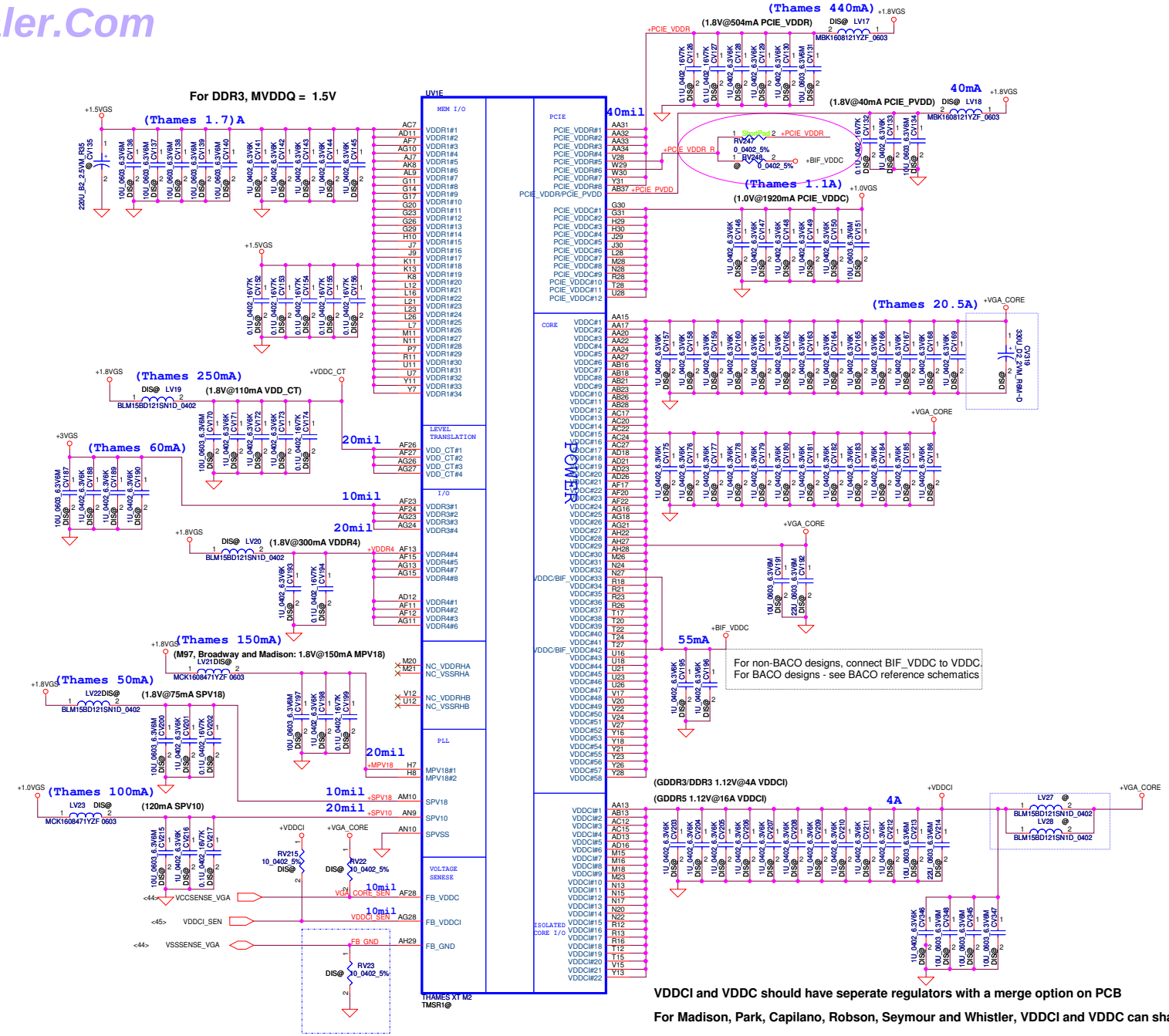

VDDCI and VDDC should have seperate regulators with a merge option on PCB

For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

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Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
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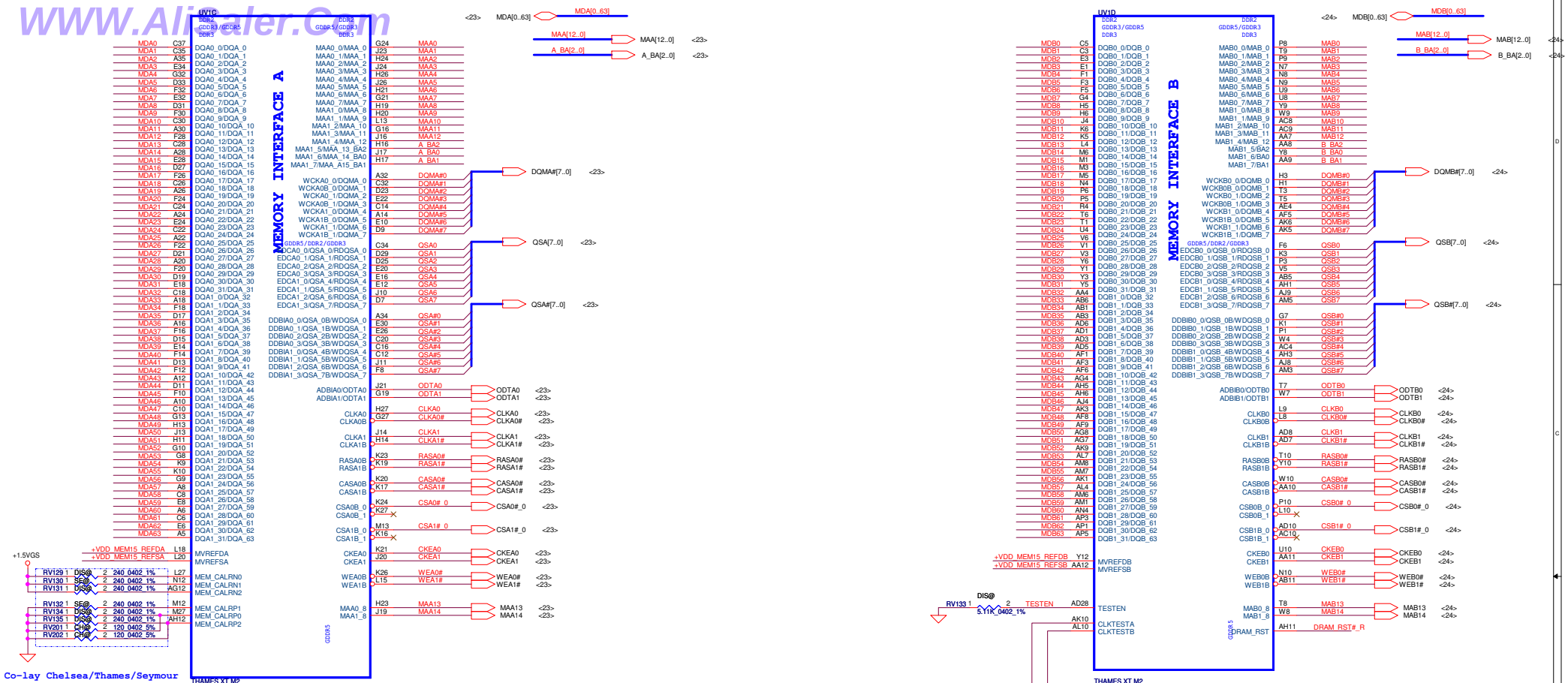

	Thames M2	Seymour M2	Chelsea M2
RV129	POP	@	@
RV130	@	POP	@
RV131	POP	@	@
RV132	@	POP	@
RV134	POP	@	@
RV135	POP	@	@
RV136	@	@	POP
RV137	@	@	POP

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Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
C	LA8251P	1.0

Date: Monday, July 16, 2012 | Sheet 22 of 50

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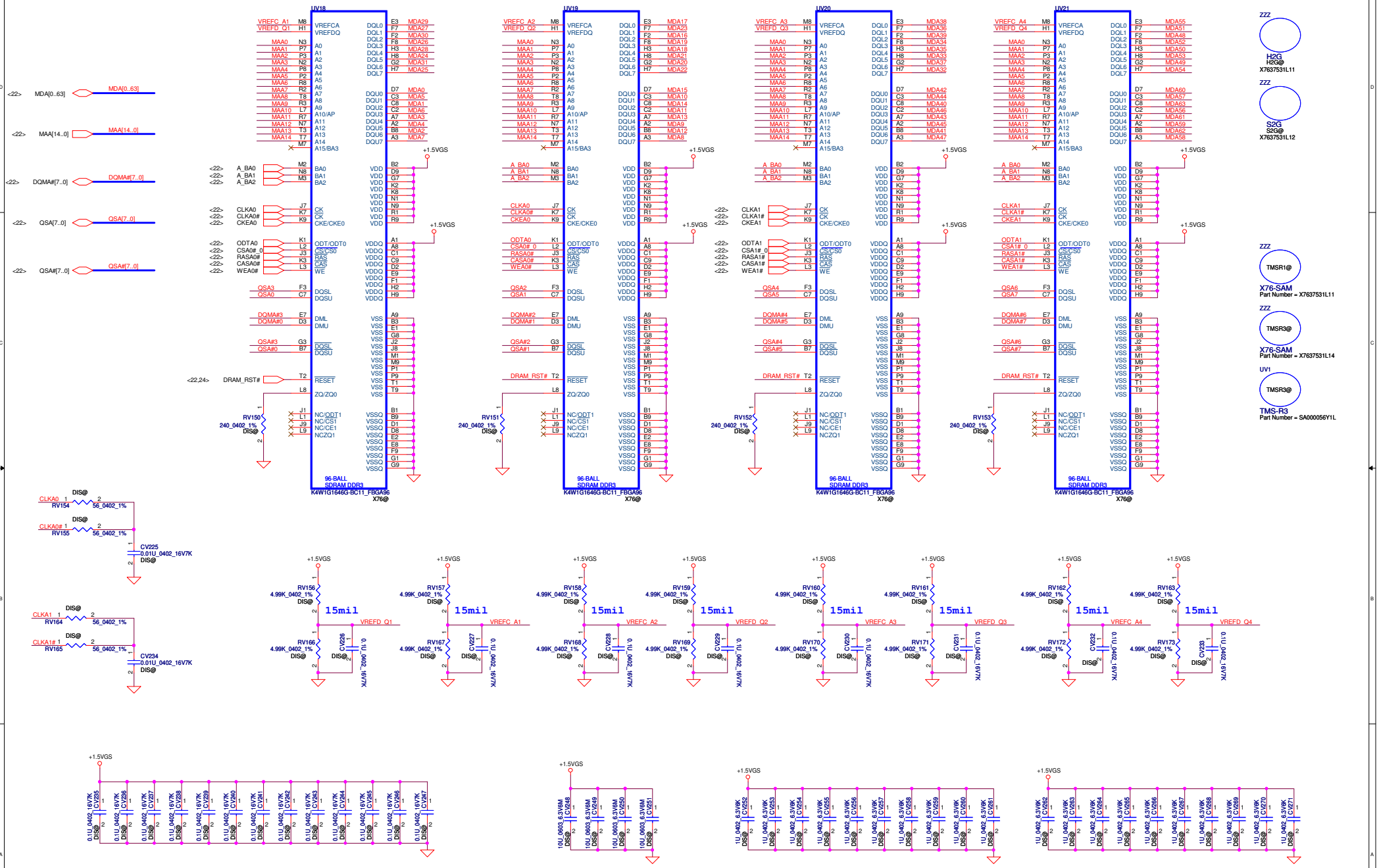
CHANNEL A: 256MB/512MB DDR3



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Compal Electronics, Inc.			
Title	ATI_SeymourXT_M2_VRAM_A		
Size C	Document Number LA8251P		Rev 1.0
Date: Monday, July 16, 2012		Sheet 23 of 50	

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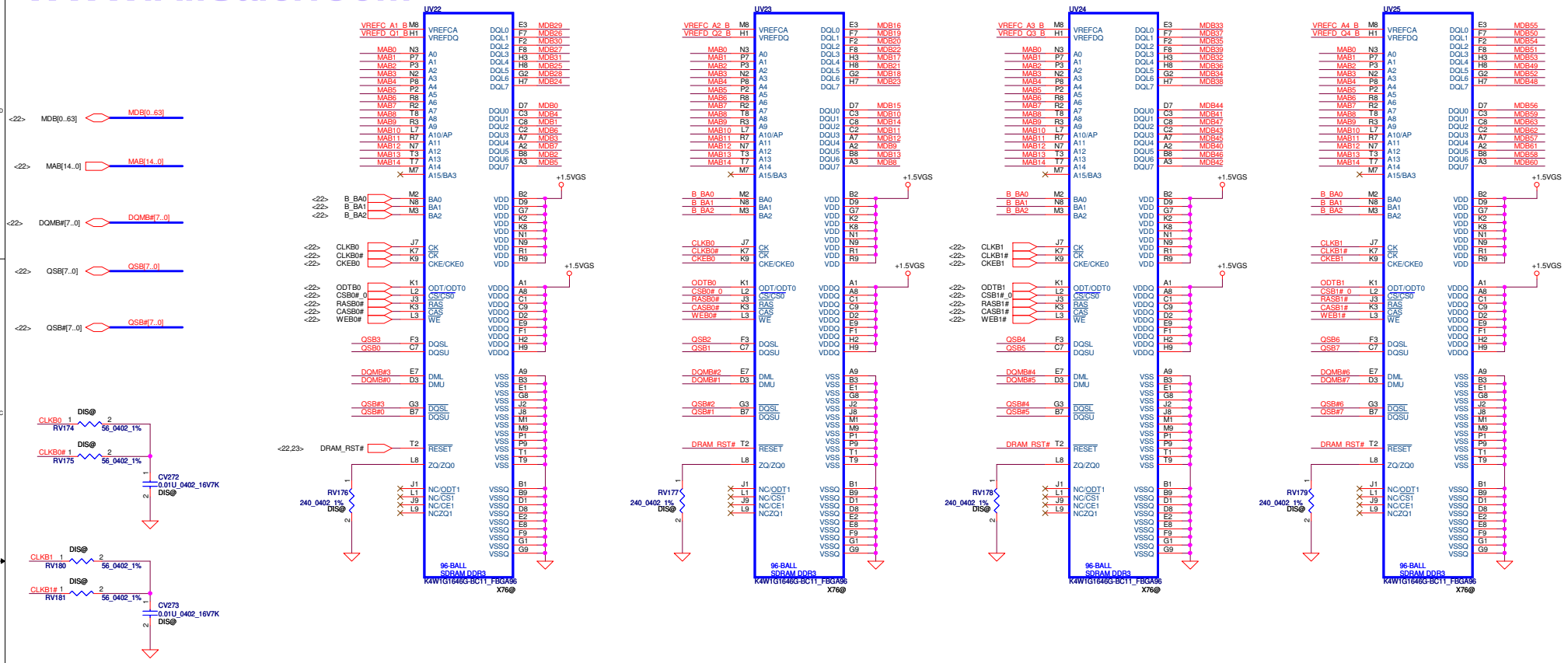
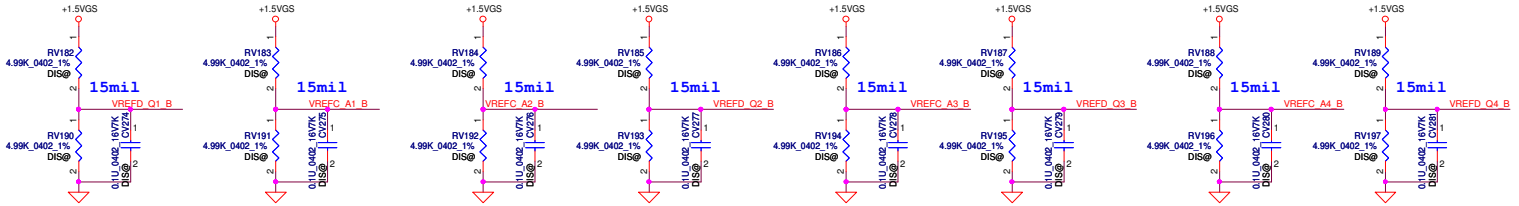
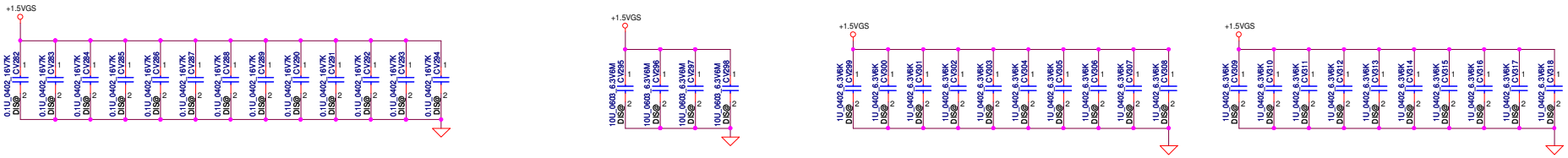
CHANNEL B: 256MB/512MB DDR3







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Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

Size	Document Number	Rev
C	LA8251P	1.0

Date: Monday, July 16, 2012 Sheet 24 of 50

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Power Consumption:

Pin5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA

+3VS 30mil 30mil +3VS_RT
1 ShortPad2 2
RV277 0_0805_5%

+AVCC33
10U_0603_6.3V6M CV343 0.1U_0402_16V4Z CV344 0.1U_0402_16V4Z CV321
Close to LV9 Close to 5 pin

+DVCC33
10U_0603_6.3V6M CV322 0.1U_0402_16V4Z CV323 22U_0805_6.3V6M CV324 0.1U_0402_16V4Z CV325 0.1U_0402_16V4Z CV326
Close to LV10 Close to 18 pin Close to 22 pin

60 mils
+SWR_V12
22U_0805_6.3V6M CV327 0.1U_0402_16V4Z CV328 0.1U_0402_16V4Z CV329 0.1U_0402_16V4Z CV330
Close to LV11 Close to 11 pin Close to 43 pin

+3VS_RT
RV293 100K_0402_5% @
DP0_AUXN_C
DP0_AUXP_C
RV294 100K_0402_5% @
AUX termination

UV27
RTD2136S

change footprint
+3VS_RT +DVCC33
LV25 FBMA-L11-201209-221LMA30T 0805 40 mils +DVCC33
LV24 FBMA-L11-201209-221LMA30T 0805 +AVCC33
+SWR_V12 LV26 4.7UH_PG031B-4R7MS_1.1A_20% 60 mils +SW_LX 60 mils

PWR: PVCC, SWR_VDD, DP_V33, SWR_LX, SWR_VCCK, VCCK, DP_V12
DP: LANE0P, LANE0N, LANE1P, LANE1N, AUX-CH_P, AUX-CH_N, DP_HPD
OTHERS: PWMIN, TESTMODE, DP_REXT, MIICSCL0, MIICSDA0, CIICSCL1, CIICSDA1
GND: DP_GND, GND, PAD

<7> DP0_TXP0_C DP0_TXP0_C
<7> DP0_TXN0_C DP0_TXN0_C
<7> DP0_TXP1_C DP0_TXP1_C
<7> DP0_TXN1_C DP0_TXN1_C
<7> DP0_AUXP_C DP0_AUXP_C
<7> DP0_AUXN_C DP0_AUXN_C
<9> LVDS_HPD RV227 1K_0402_5% LVDS_HPD_OUT
<9> APU_INVT_PWM TP2 RV280 12K_0402_1%
MIIC_SCL MIIC_SDA
CSCL RV284 ShortPad2 0_0402_5% CIICSCL
CSDA RV287 ShortPad2 0_0402_5% CIICSDA

LVDS: TXOC+/- TXO0+/- TXO1+/- TXO2+/- TXO3+/- TXEC+/- TXE0+/- TXE1+/- TXE2+/- TXE3+/-
LVDS_ACLK LVDS_ACLK# LVDS_A0 LVDS_A0# LVDS_A1 LVDS_A1# LVDS_A2 LVDS_A2# LVDS_BCLK LVDS_BCLK# LVDS_B0 LVDS_B0# LVDS_B1 LVDS_B1# LVDS_B2 LVDS_B2#
MIICSCL1 MIICSDA1 EDID_CLK EDID_DATA
PANEL_VCC PWMOUT BL_EN TL_ENVDD TL_INVT_PWM TL_BKOFF#_R
UTLGND1 ShortPad2 RV288 0_0402_5%
RTD2136S-CG_QFN48_6X6

+DVCC33 EERom
UV26
MIIC_SCL MIIC_SDA
VCC WP SCL SDA A0 A1 A2 GND
CAT24C64WI-GT3_SO8
Addr: A8 (1010 100X)

+DVCC33
RV278 4.7K_0402_5% EEPROM
MIIC_SCL
RV279 4.7K_0402_5% ROMLESS @

+DVCC33
EDID_DATA RV2811 4.7K_0402_5%
EDID_CLK RV2821 4.7K_0402_5%
MIIC_SDA RV2831 4.7K_0402_5%
CSCL RV2851 4.7K_0402_5%
CSDA RV2891 4.7K_0402_5%

Vendor advise reserve it

RV290 @ 0_0402_5% ENBAKL <34>
TL_BKOFF#_R RV291 0_0402_5% TL_BKOFF# <26>
+3VS_RT CV331 0.1U_0402_16V7K @
<26,34> BKOFF#
UV28 @ MC74VHC1G08DFT2G SC70 5P

+3VS_RT
CSDA QV28A DMN66D0LDW-7_SOT363-6 EC_SMB_DA2 EC_SMB_DA2 <18,34,7>
CSCL QV28B DMN66D0LDW-7_SOT363-6 EC_SMB_CK2 EC_SMB_CK2 <18,34,7>

LVDS_HPD
RV292 100K_0402_5%
Pull-Low 100K
TL_BKOFF#_R
RV295 100K_0402_5%

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Issued Date	2011/08/01	Deciphered Date 2013/01/01	Title: LVDS Translator - RTD2132S
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 25 of 50		

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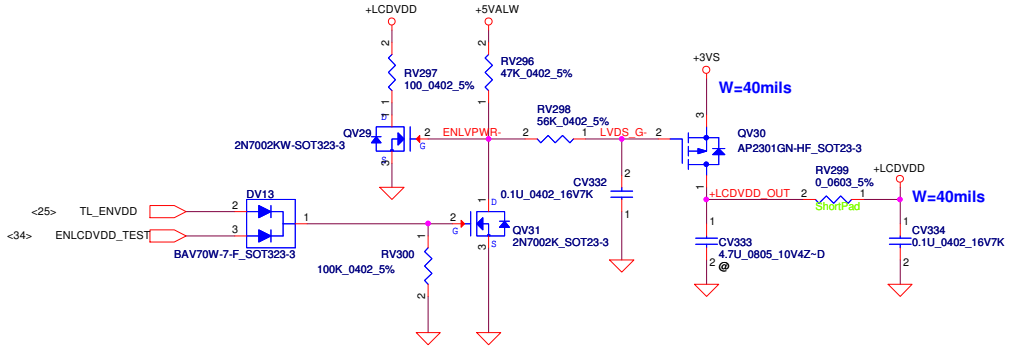
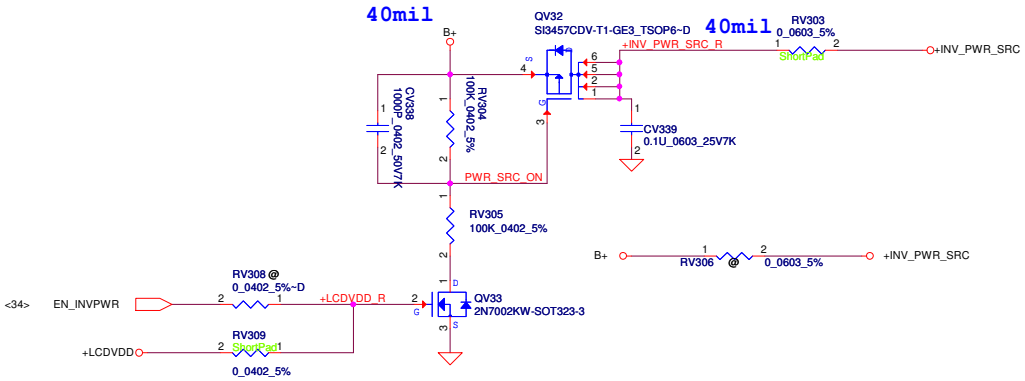
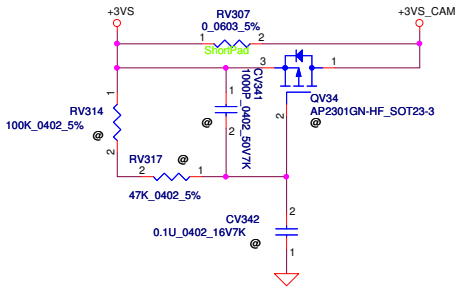
LCD PWR CTRL



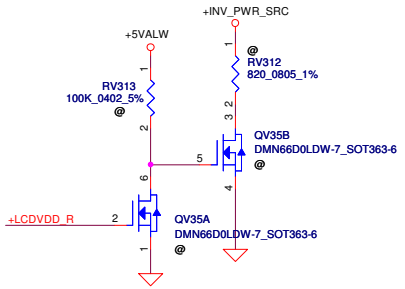
LCD backlight PWR CTRL



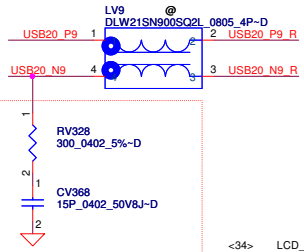
Wedcam PWR CTRL

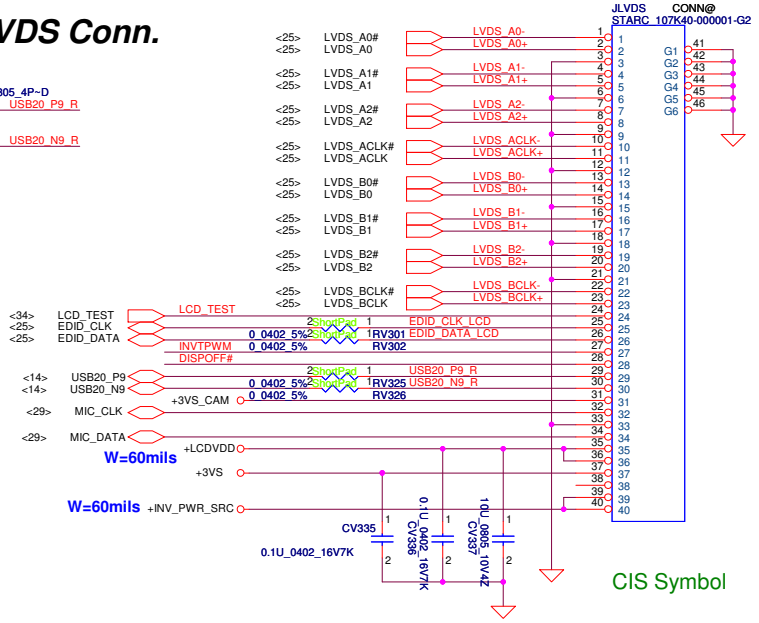


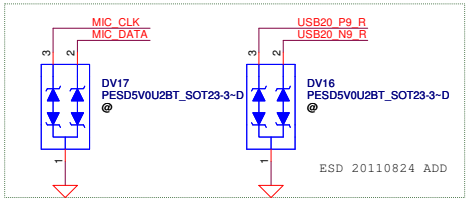
* Reserved for LCD sequence tuning

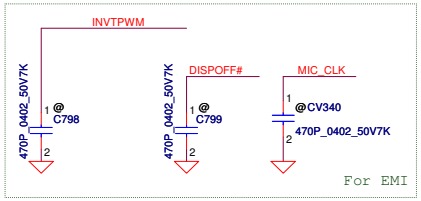


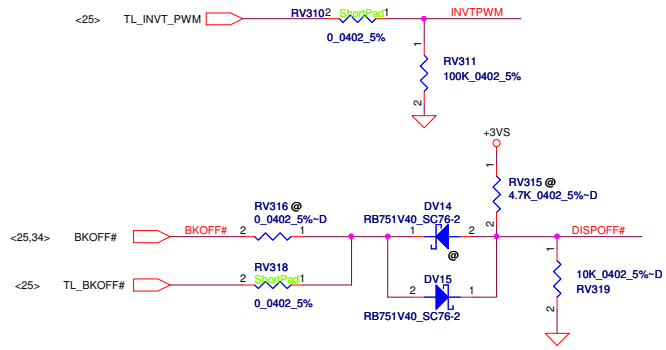
LVDS Conn.











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Compal Electronics, Inc.			
Title	LVDS/CAMERA		
Size B	Document Number LA8251P		Rev 1.0
Date: Monday, July 16, 2012	Sheet 26 of 50		

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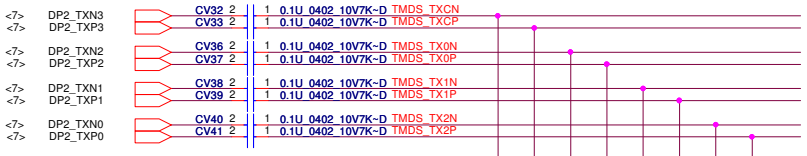
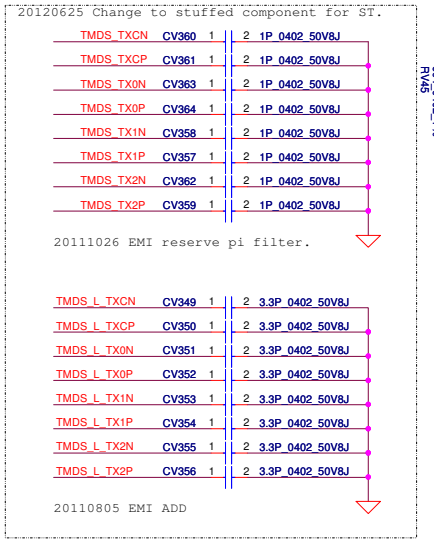
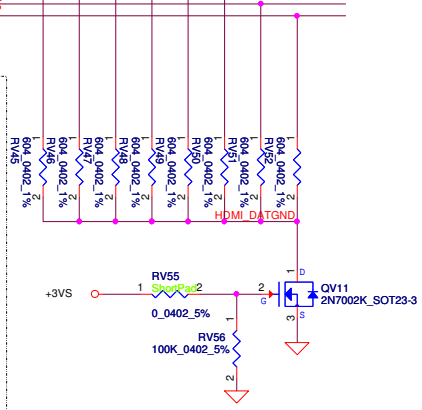
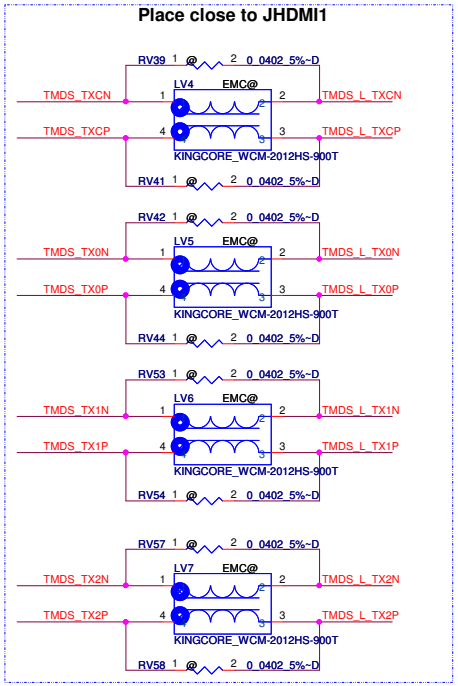
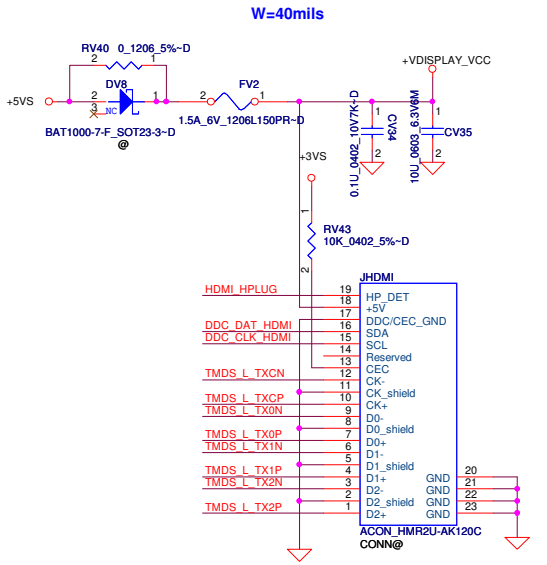




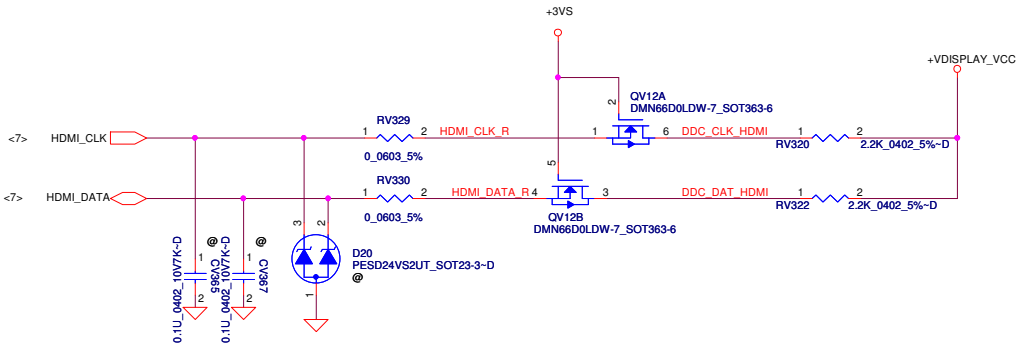


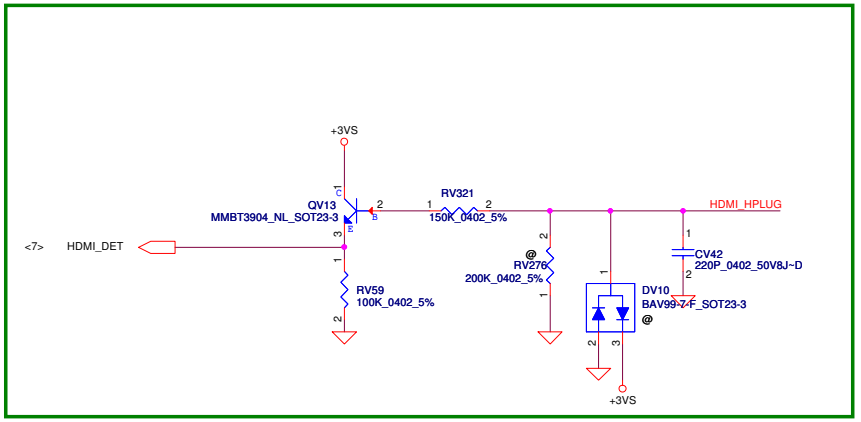




46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM





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Compal Electronics, Inc.

Title: HDMI

Size: Custom | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 27 of 50

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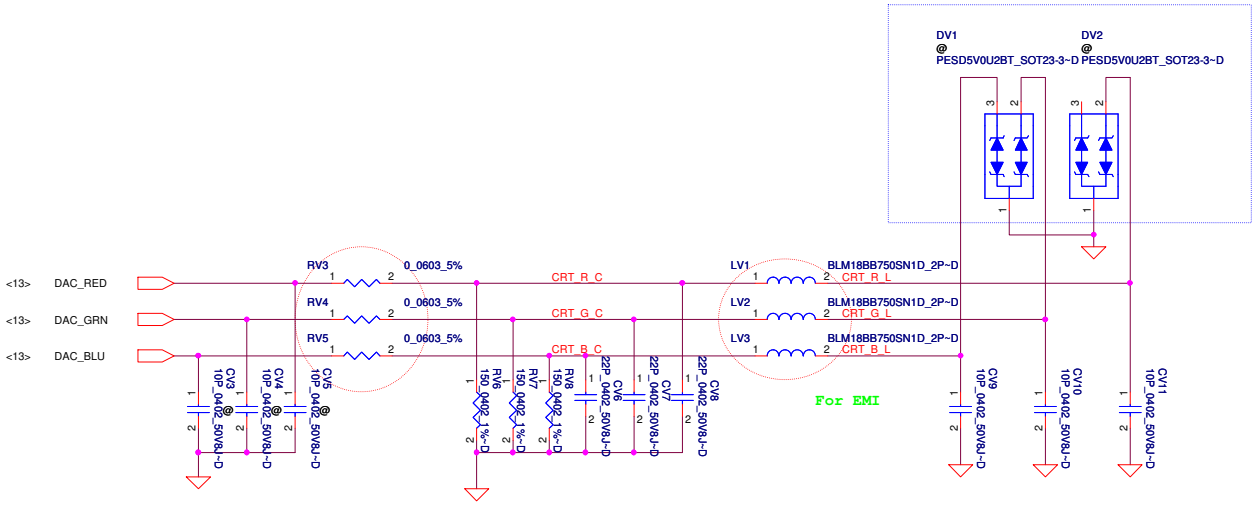

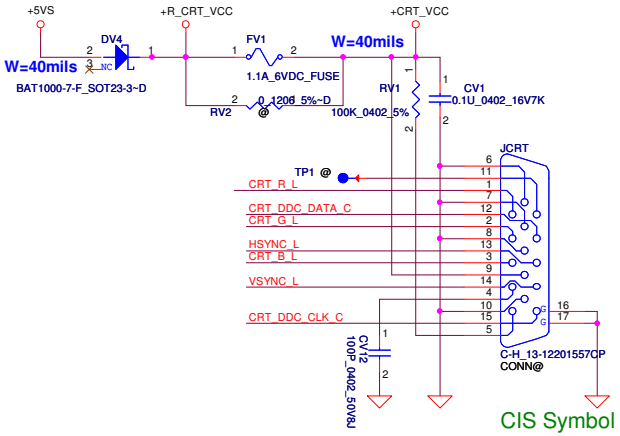

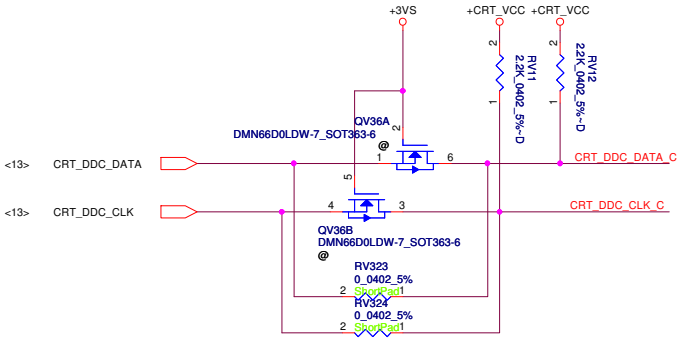

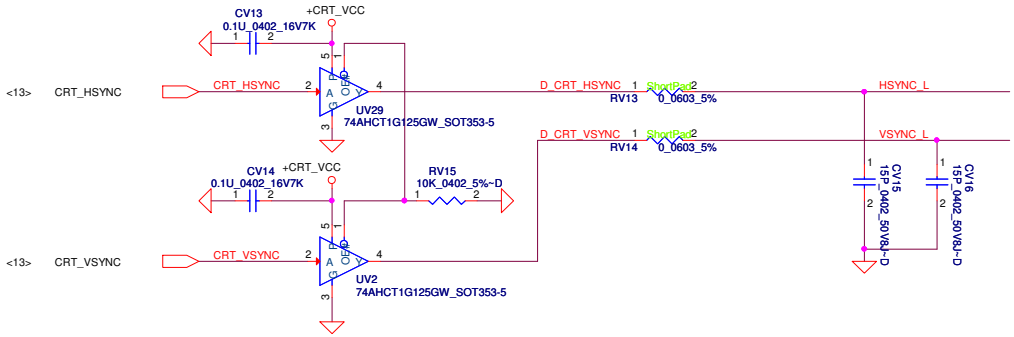

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Issued Date	2011/08/01	Deciphered Date 2013/01/01	Title: CRT Conn.
Size	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 28 of 50		

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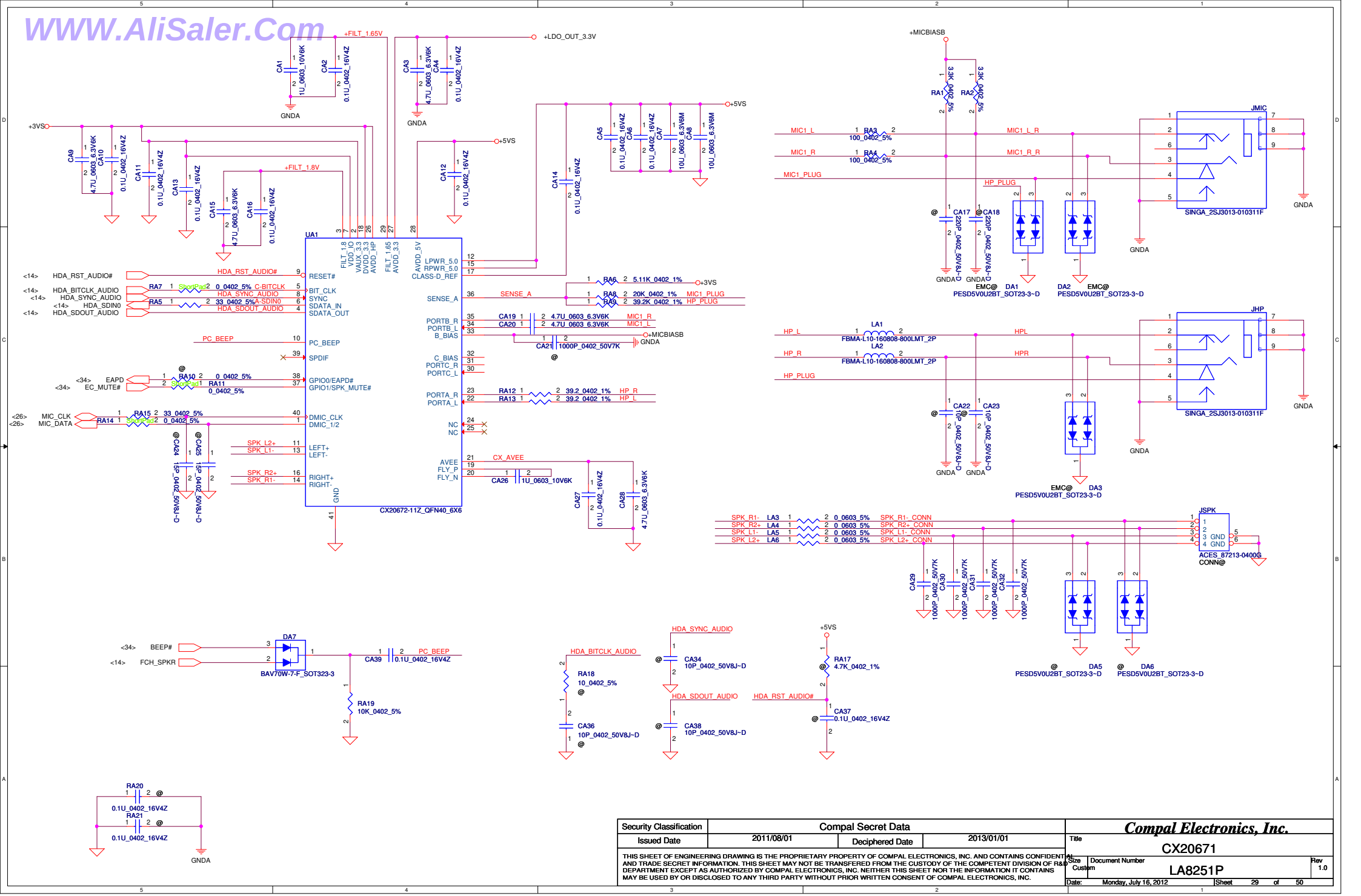

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Compal Electronics, Inc.			
Title	CX20671		
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 29 of 50		

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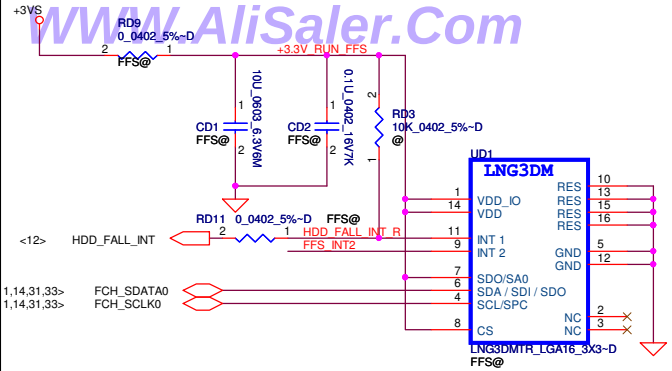

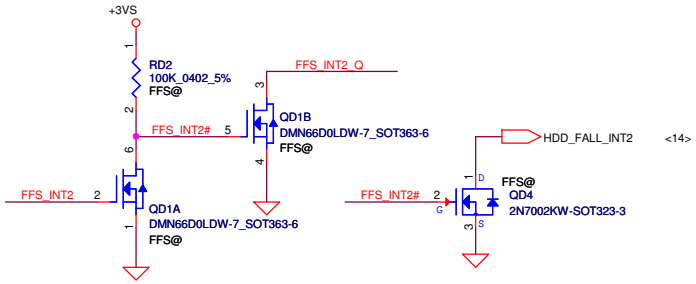

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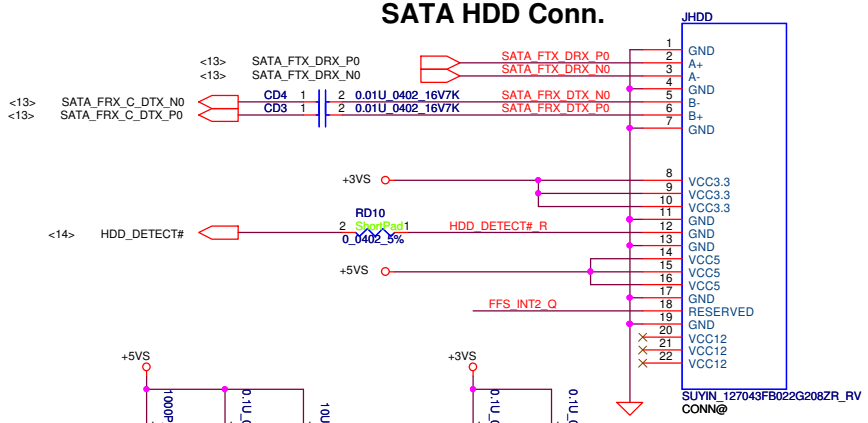
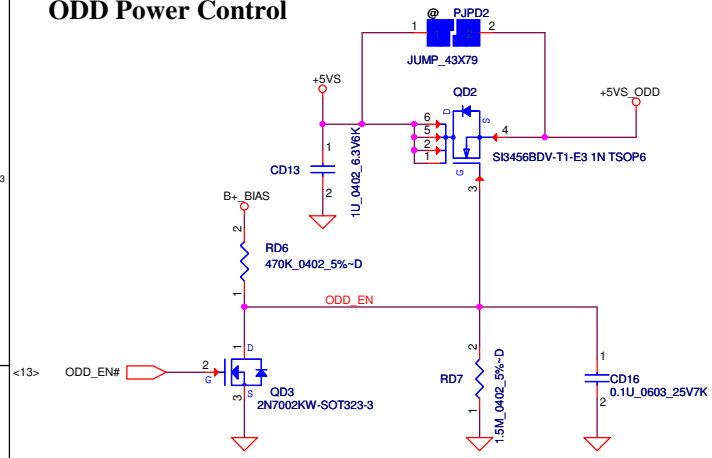
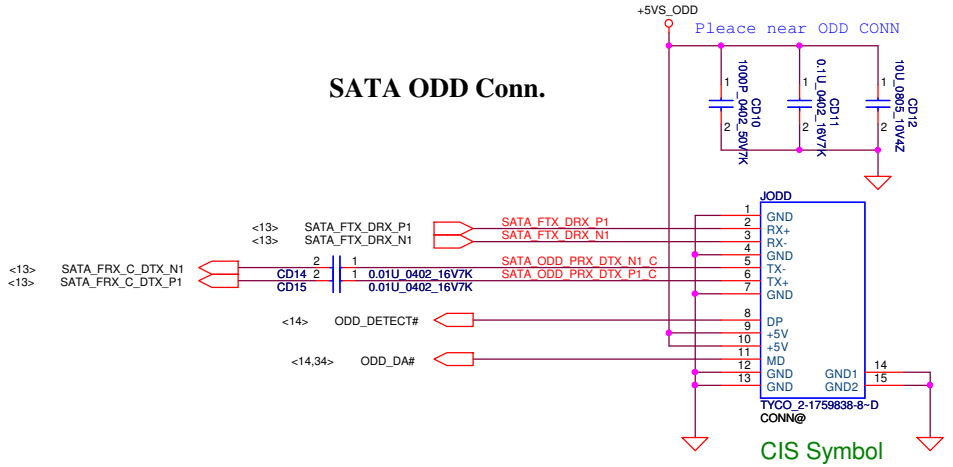


ODD Power Control



SATA ODD Conn.



CIS Symbol

Security Classification	Compal Secret Data		
Issued Date	2011/08/01	Deciphered Date	2013/01/01

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Compal Electronics, Inc.			
Title	HDD/ODD/FAN		
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 30 of 50		

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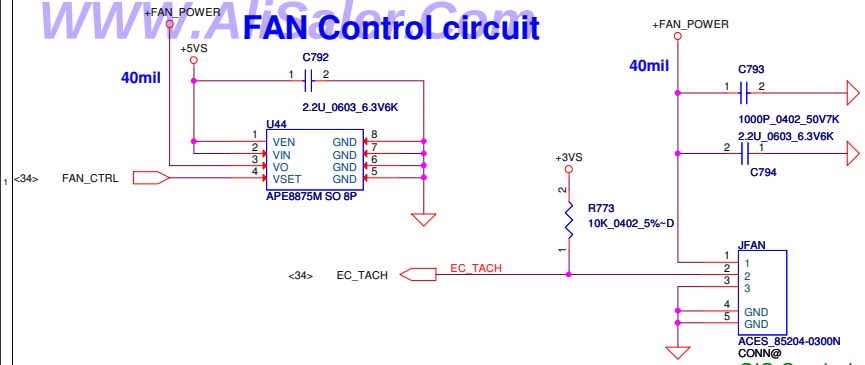
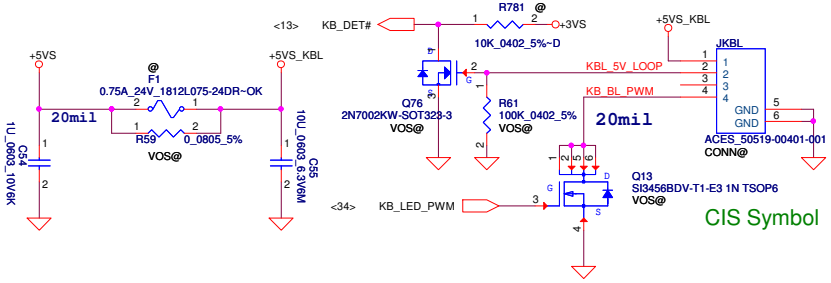
FAN Control circuit



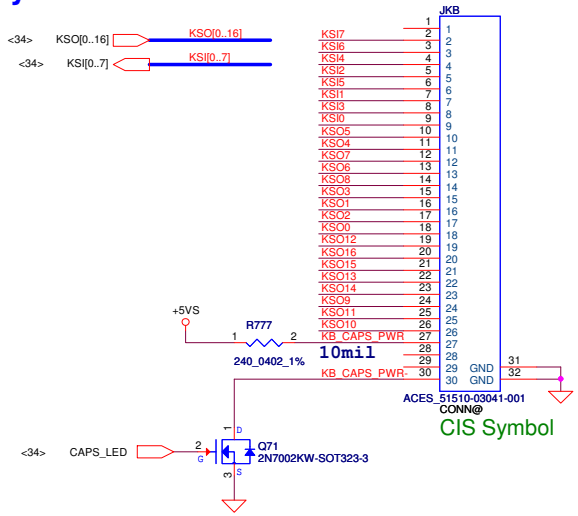
CIS Symbol

Keyboard back light



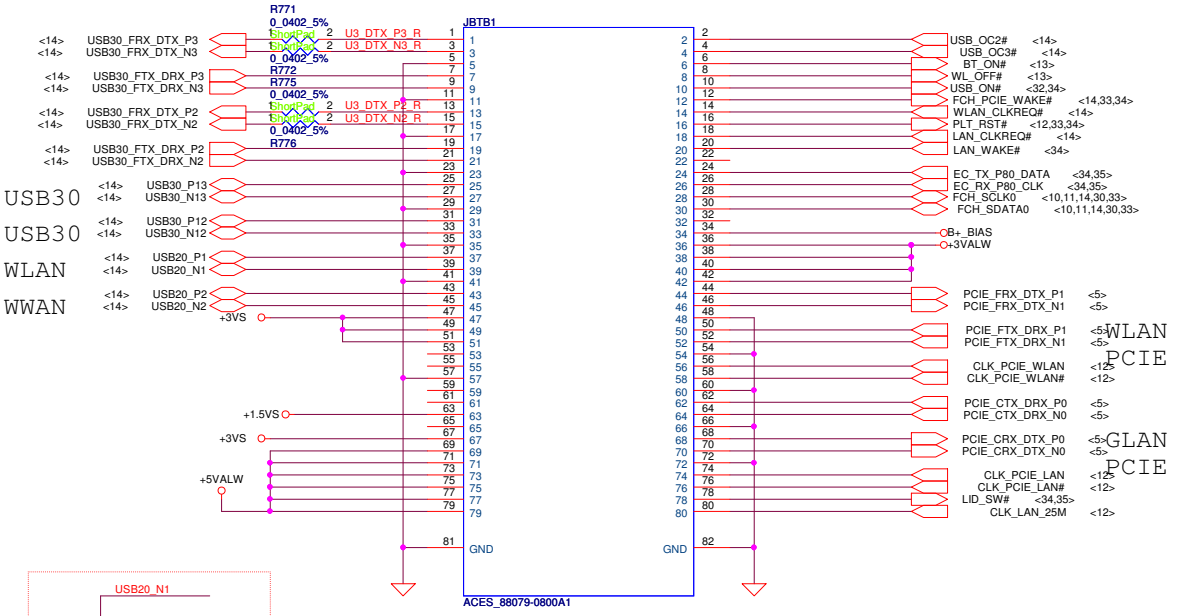
CIS Symbol

Keyboard Connector

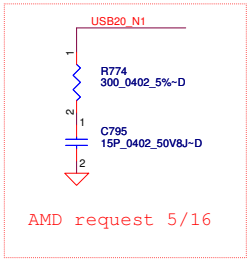


CIS Symbol

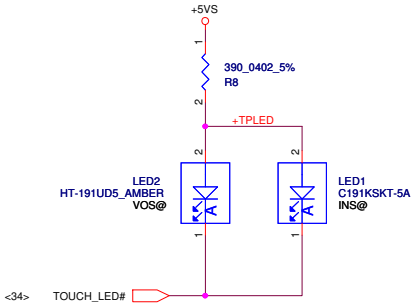
M/B to D/B BTB connector, LAN, FMC, HMC, USB3.0*2

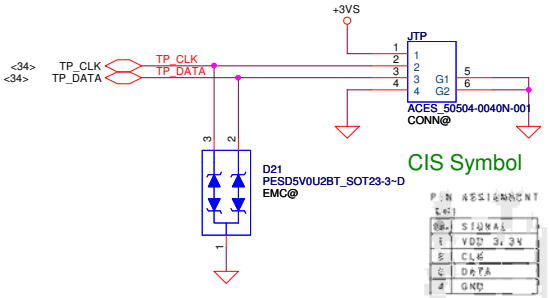


CIS Symbol, Receptacle.



Touch pad





CIS Symbol

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Issued Date	2011/08/01	Deciphered Date	2013/01/01

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Compal Electronics, Inc.

Title: IO brd Conn & FAN/KB/TP

Size: B | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 31 of 50

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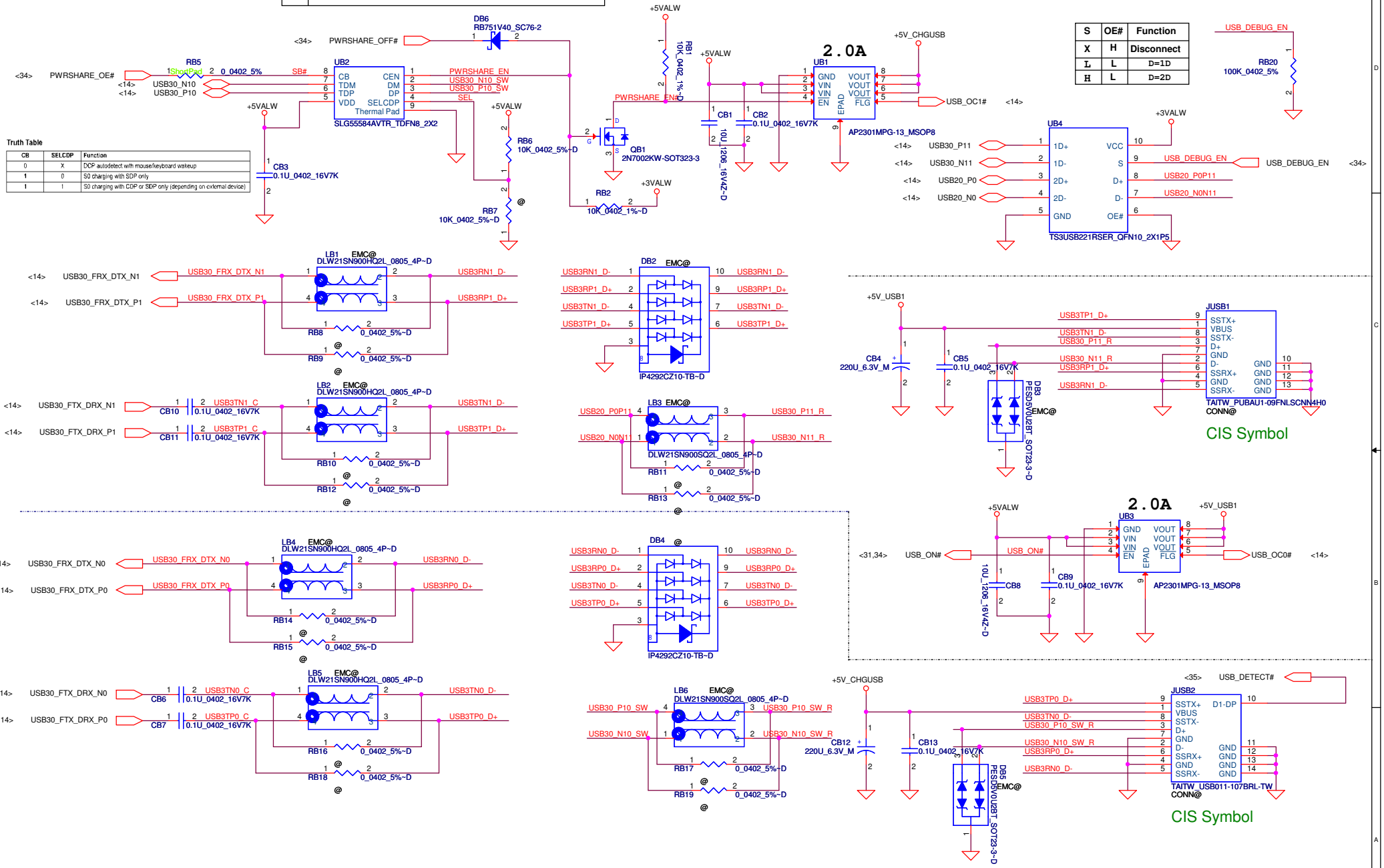
Power share

CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

Truth Table

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



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Compal Electronics, Inc.			
Title	USB LP1/2		
Size	Document Number		Rev
Custom	LA8251P		1.0
Date:	Monday, July 16, 2012	Sheet	32 of 50

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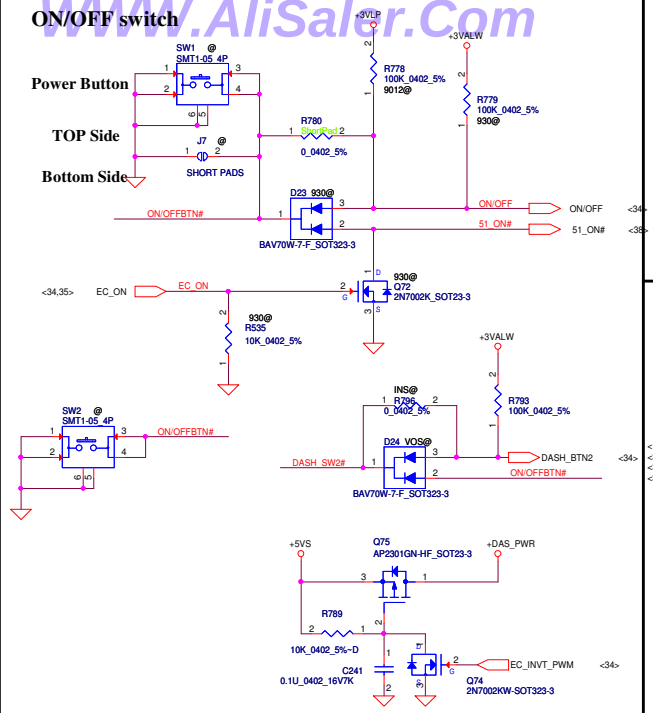
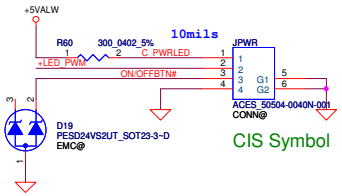
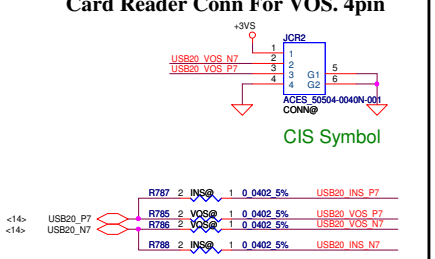
ON/OFF switch



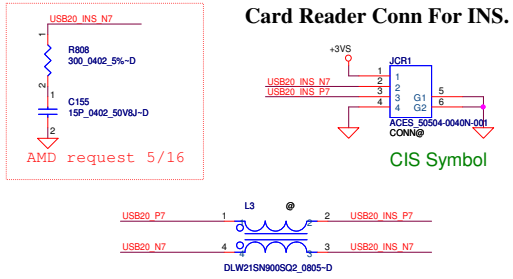
Power Button Board Conn. 4pin



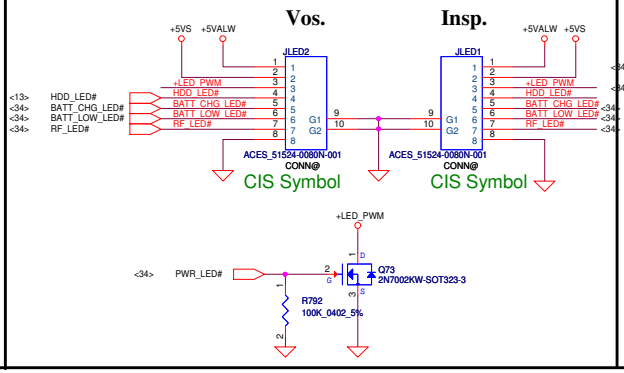
Card Reader Conn For VOS. 4pin



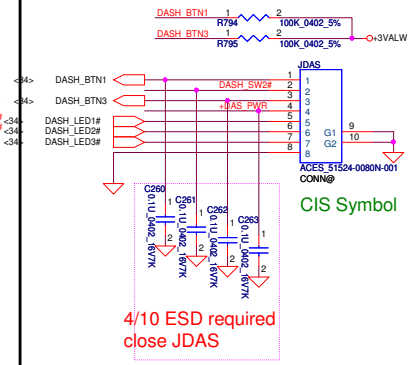
Card Reader Conn For INS.



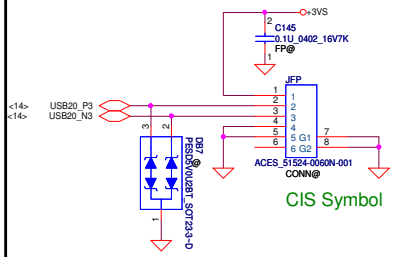
LED Board Conn, include LID SW. 10pin



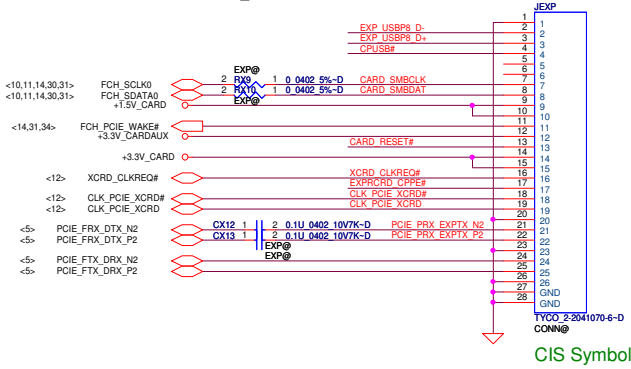
Dashboard Function Conn. 8pin



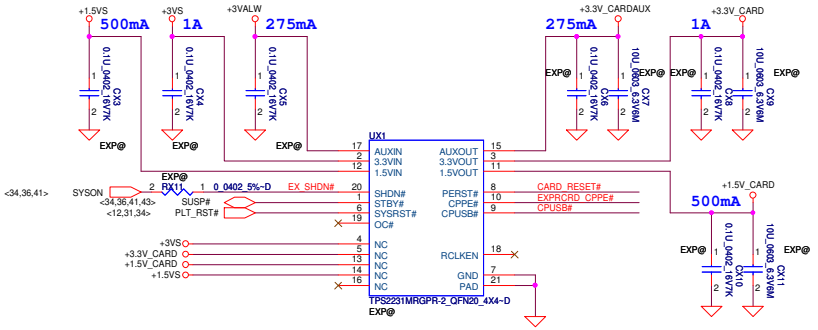
Finger Printer Conn. 6pin

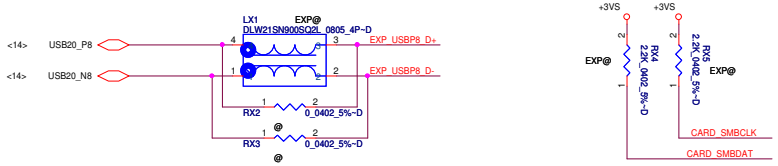


Express Card



Express Card PWR S/W





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Issued Date	2011/08/01	Deciphered Date	2013/01/01

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Compal Electronics, Inc.	
Title	Other IO Conn. ExCARD
Size: C	Document Number: LA8251P
Rev	1.0
Date: Monday, July 16, 2012	Sheet 33 of 50

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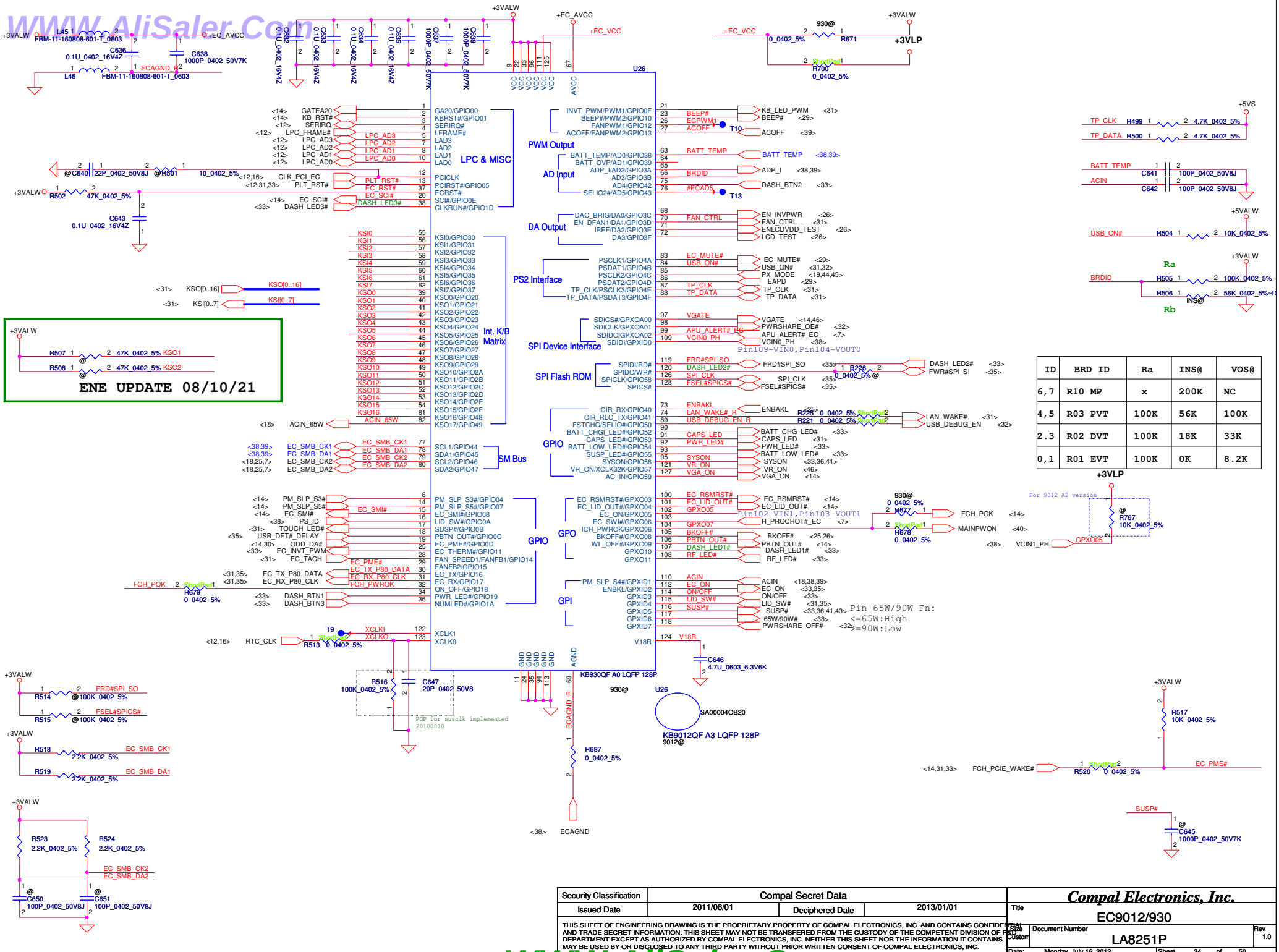

ID	BRD ID	Ra	INS@	VOS@
6,7	R10 MP	x	200K	NC
4,5	R03 PVT	100K	56K	100K
2.3	R02 DVT	100K	18K	33K
0,1	R01 EVT	100K	0K	8.2K

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Title: EC9012/930

Size: Custom | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 34 of 50

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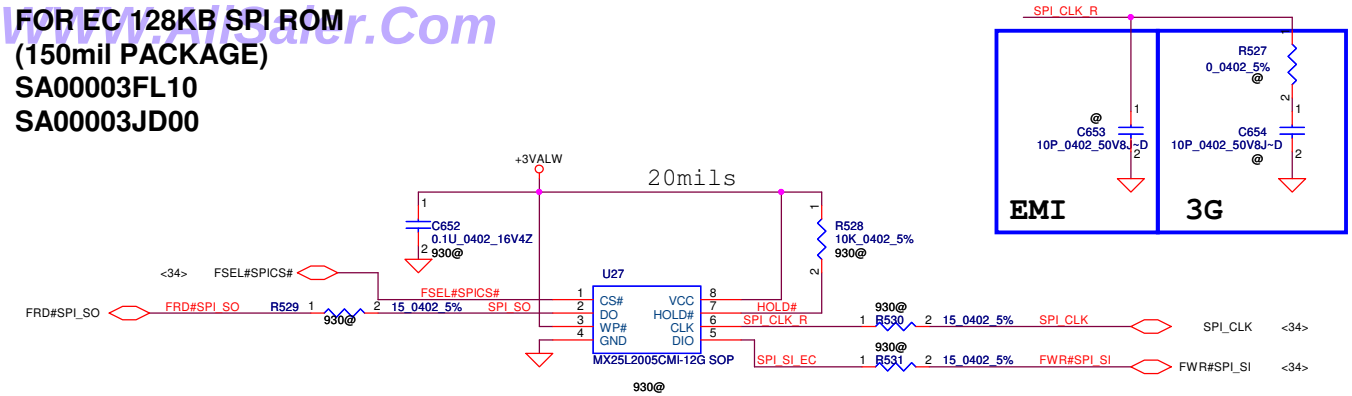
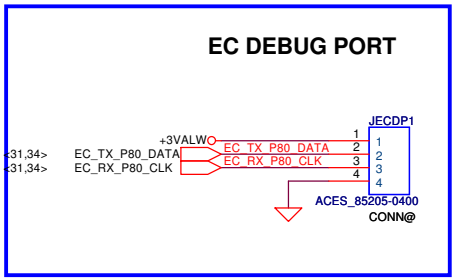
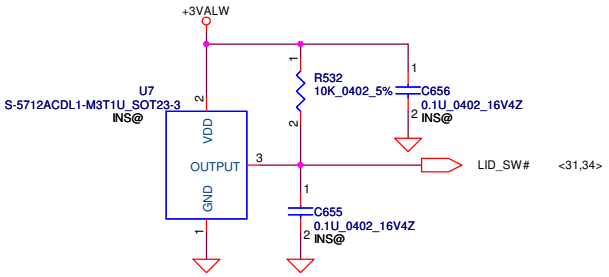
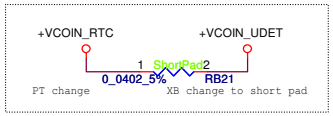
FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00



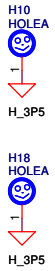


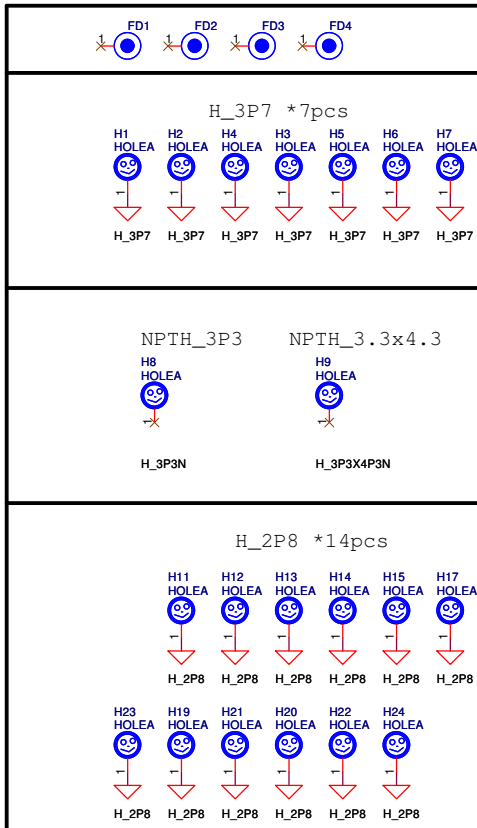
LID SWITCH FOR INS. ONLY





H_3P5 *2pcs





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Compal Electronics, Inc.

Title: EC ROM/Debug

Size: B | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 35 of 50

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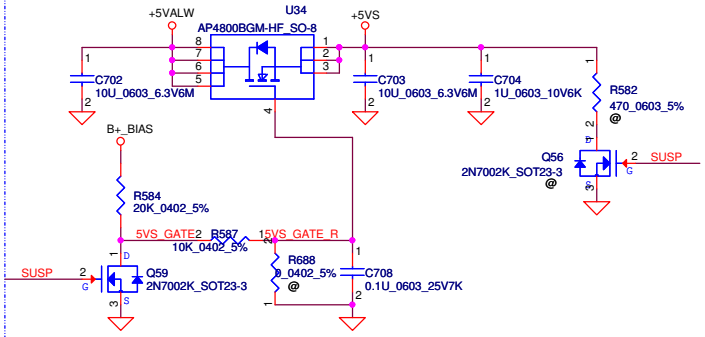
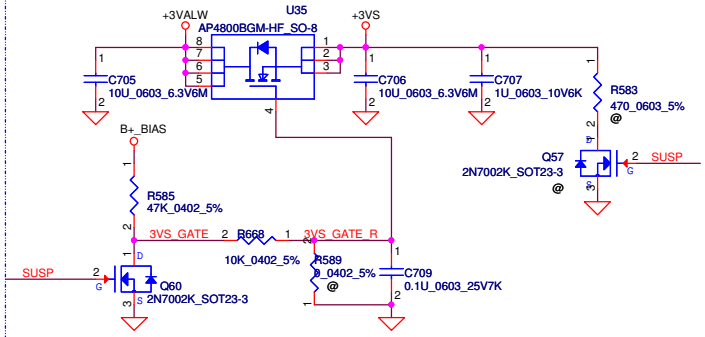
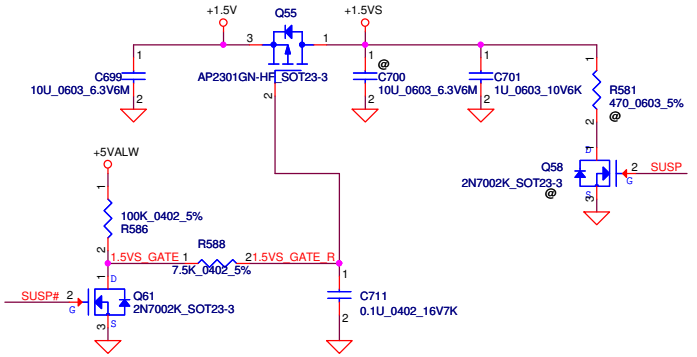
+5VALW TO +5VS



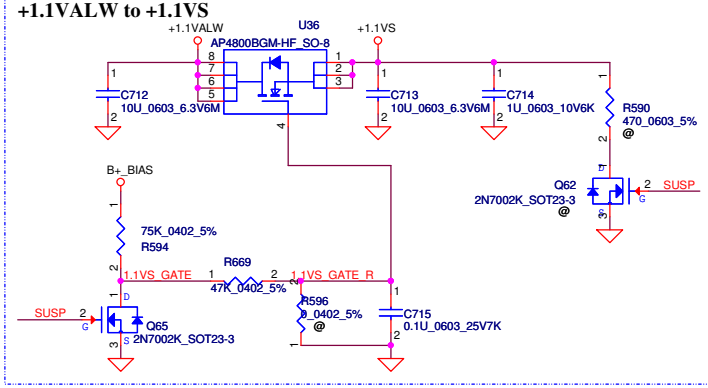
+3VALW TO +3VS

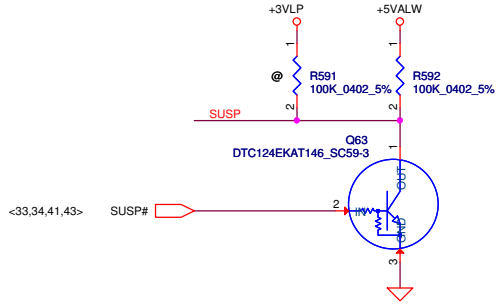


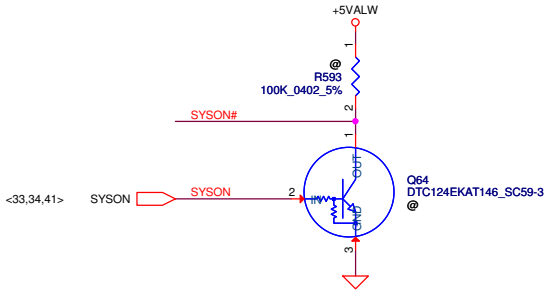
+1.5V to +1.5VS

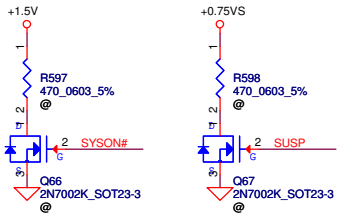


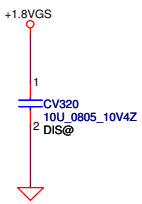
+1.1VALW to +1.1VS

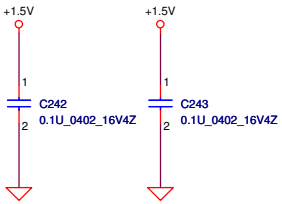




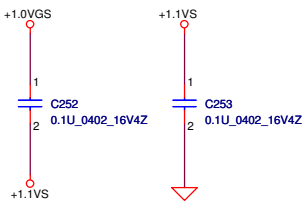




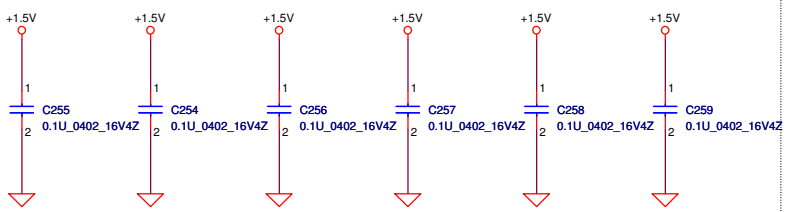




For USB3.0 Cross Moat On Bottom



ESD demand in PT



EMI Adding for PT, 2011/11/28

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 36 of 50

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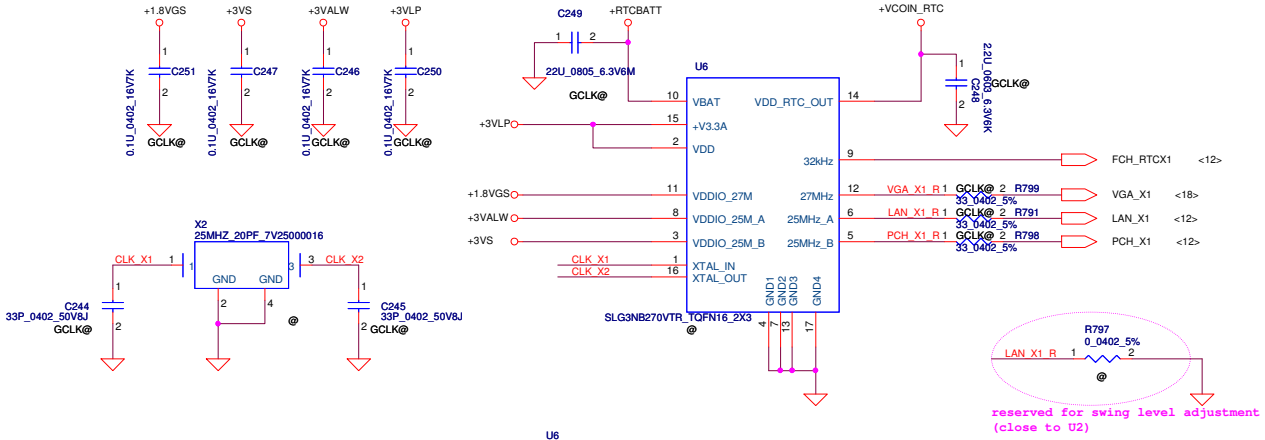

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Issued Date	2011/08/01	Deciphered Date	2013/01/01
Title	AMP & GCLK		
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 48 of 50		

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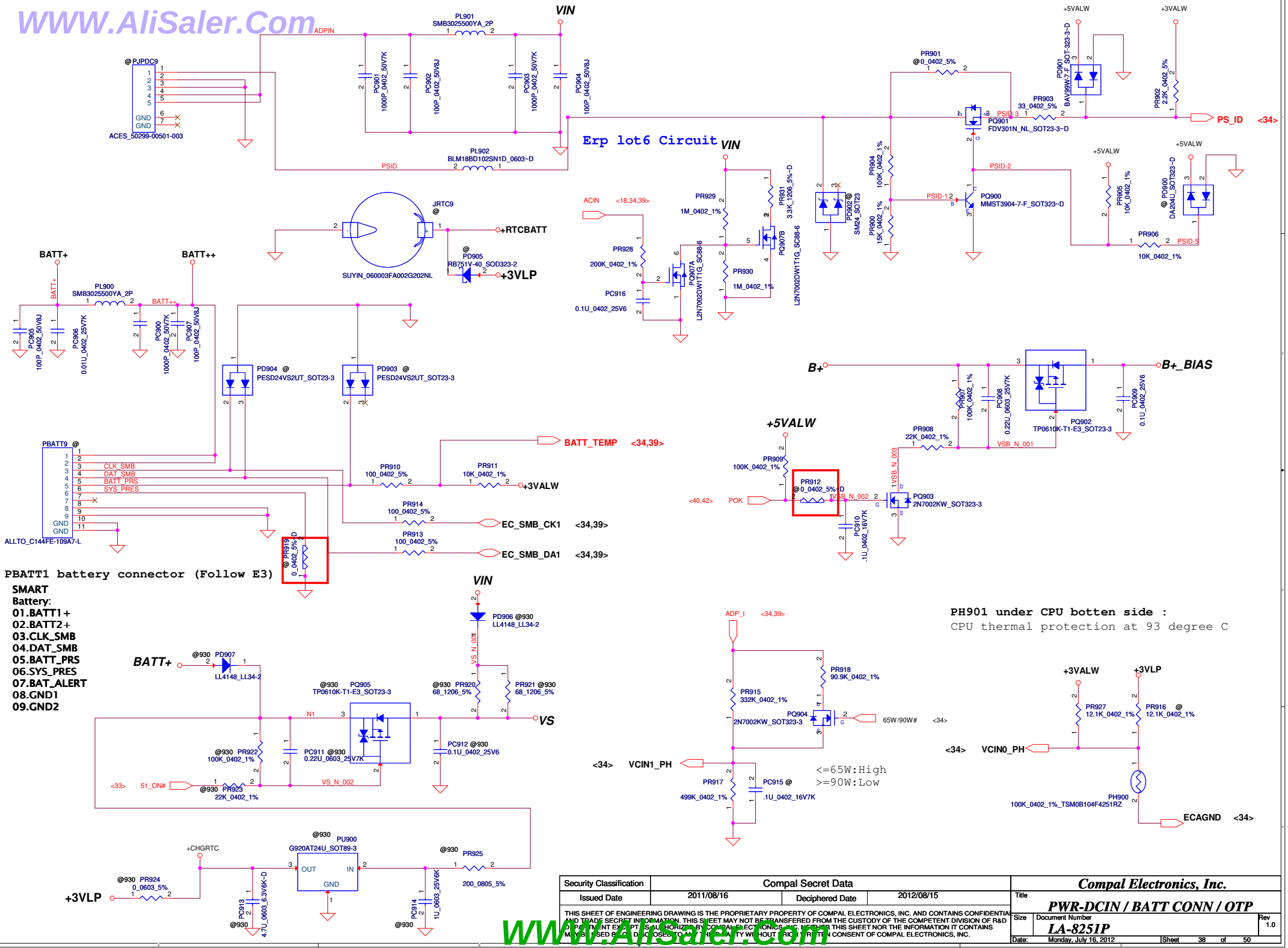

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

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Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size: | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 38 of 50

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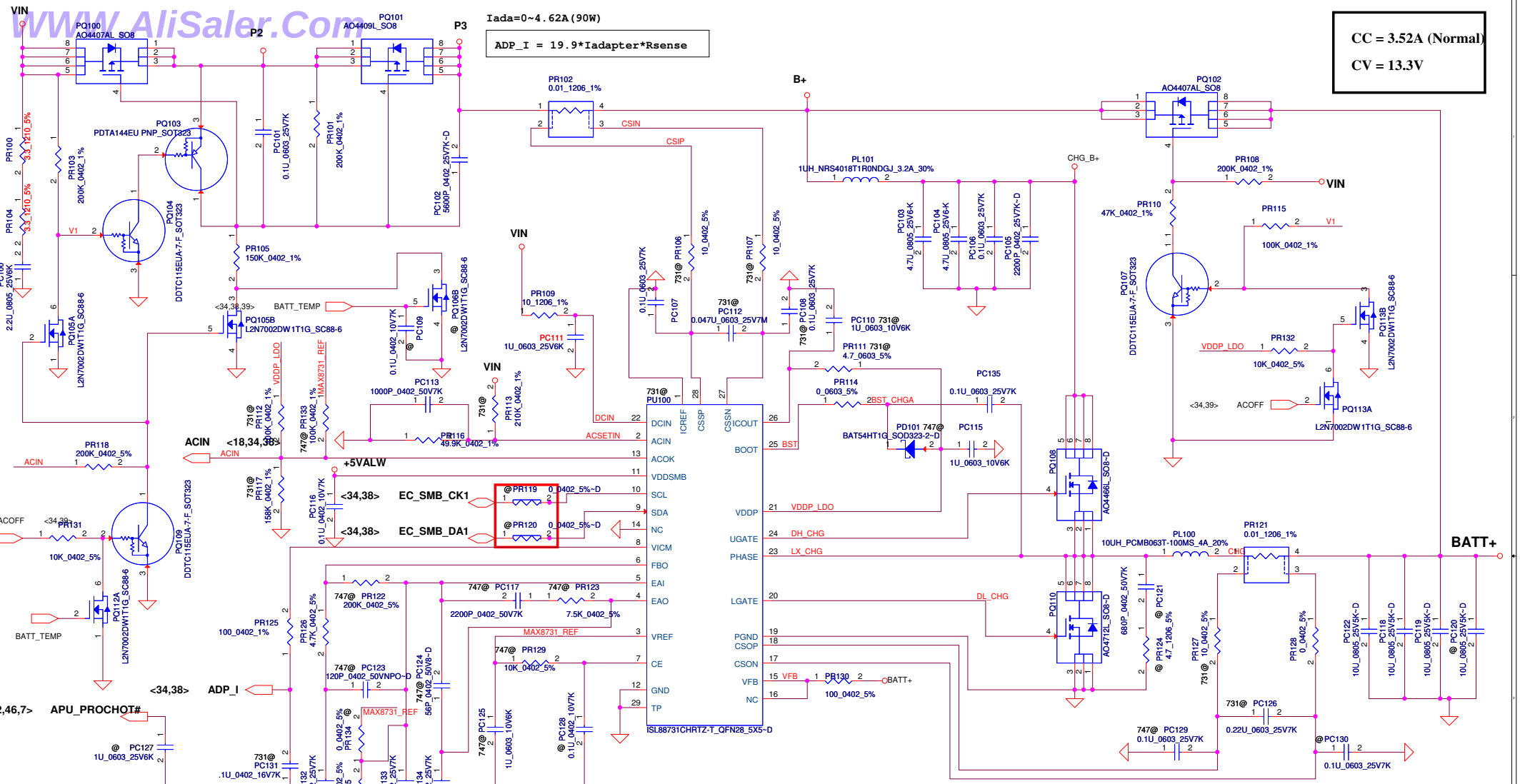
Iada=0~4.62A(90W)

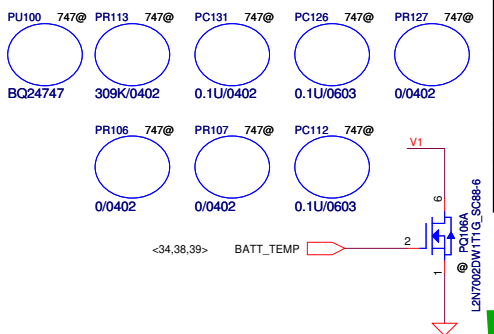
ADP_I = 19.9*Iadapter*Rsense

CC = 3.52A (Normal)

CV = 13.3V



For DT Mode



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PU100	ISL88731C	BQ24747
PR133	@	100k
PR112	100k	@
PR117	158k	@
PR113	210k	309k
PC131	0.1u	0.1u
PC132	0.01u	@

	ISL88731C	BQ24747
PR122	@	200k
PR123	@	7.5k
PR129	@	10k
PC117	@	2200p
PC124	@	56p
PC123	@	120p
PC125	@	1u

	ISL88731C	BQ24747
PC134	0.01u	@
PC129	@	0.1u
PC126	0.22u	0.1u
PR127	10	0
PC110	1u	@
PD101	@	BAT54HT1G

	ISL88731C	BQ24747
PC108	0.1u	@
PR106	10	0
PR107	10	0
PC112	0.047u	0.1u

731@ for ISL88731C
747@ for BQ24747

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

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Compal Electronics, Inc.

Title: PWR-Charger

Size: | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 39 of 50

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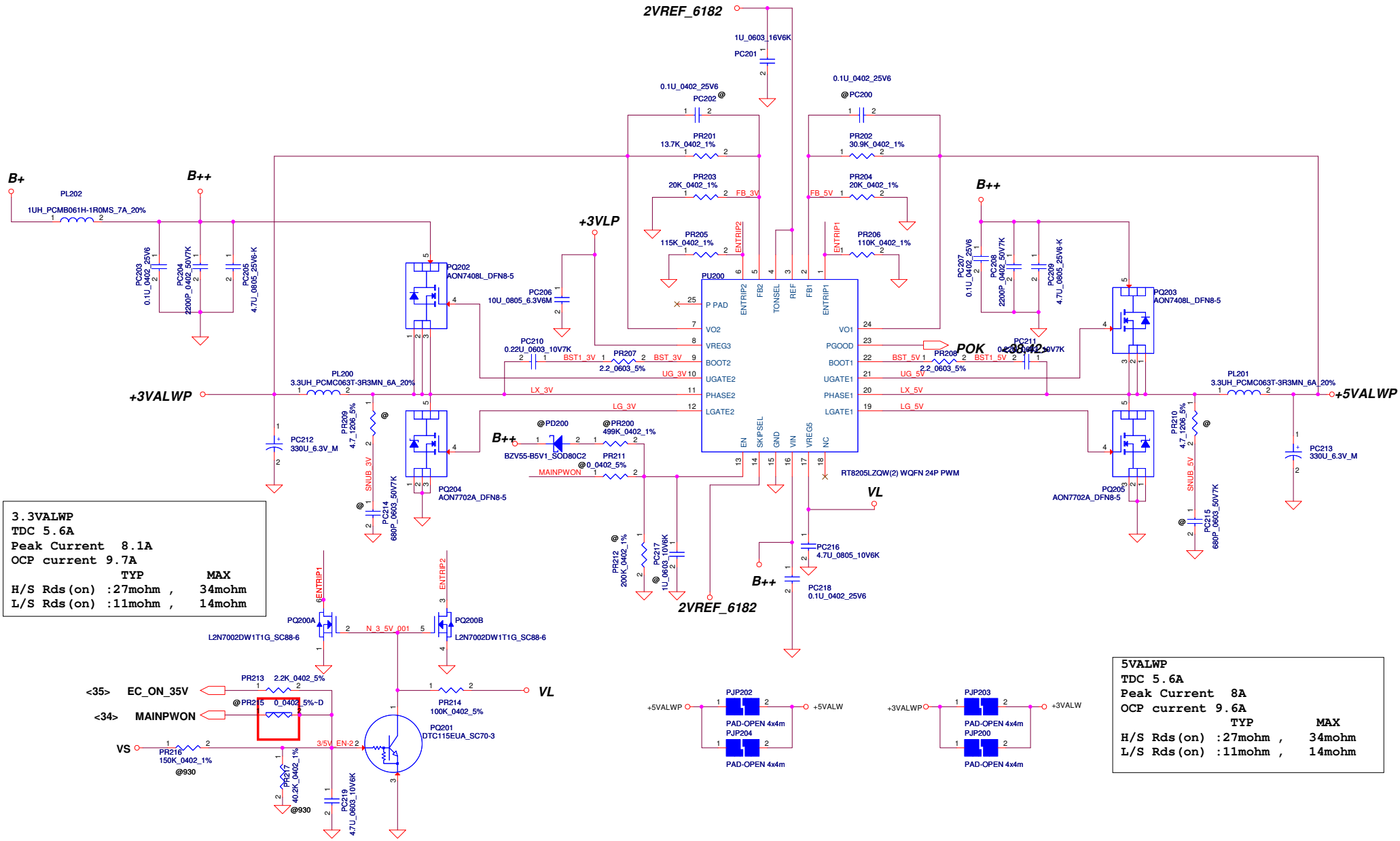

3.3VALWP
TDC 5.6A
Peak Current 8.1A
OCP current 9.7A

	TYP	MAX
H/S Rds(on) :	27mohm ,	34mohm
L/S Rds(on) :	11mohm ,	14mohm

5VALWP
TDC 5.6A
Peak Current 8A
OCP current 9.6A

	TYP	MAX
H/S Rds(on) :	27mohm ,	34mohm
L/S Rds(on) :	11mohm ,	14mohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/04	Deciphered Date 2012/08/03	Title PWR-3VALWP/5VALWP
			Size B Document Number LA-8251P Rev 1.0
			Date: Monday, July 16, 2012 Sheet 40 of 50

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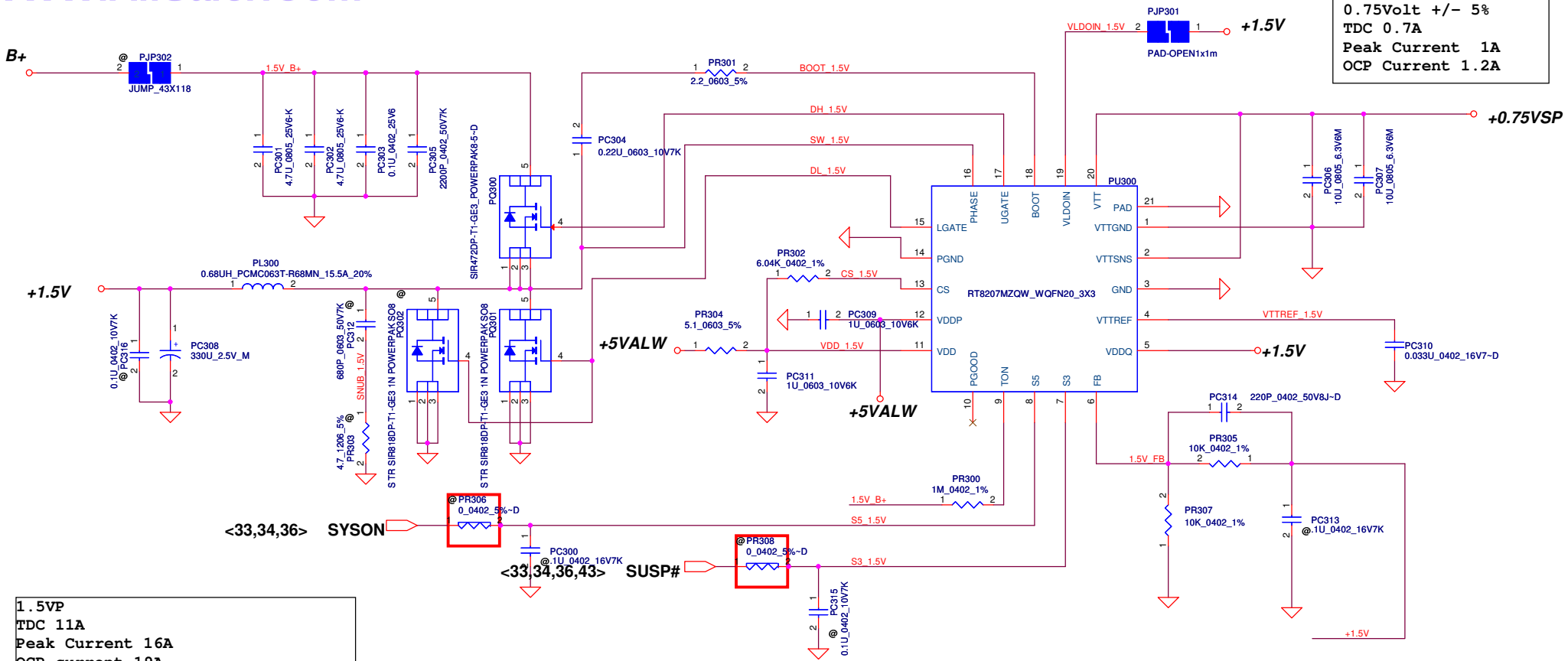

Security Classification	Compal Secret Data		
Issued Date	2011/08/04	Deciphered Date	2012/08/03

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Compal Electronics, Inc.			
Title: PWR-1.5V/0.75VSP			
Size	Document Number: LA-8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 41 of 50		

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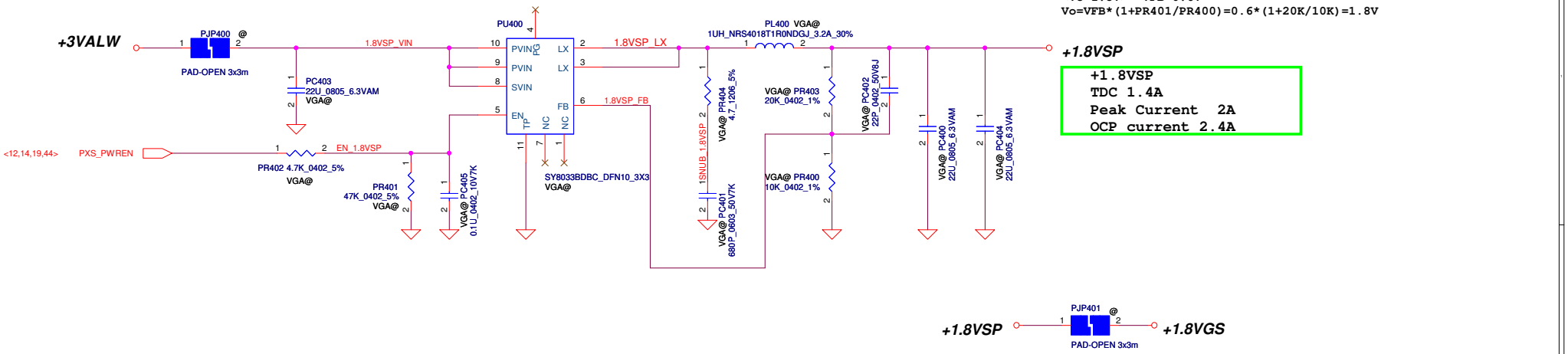

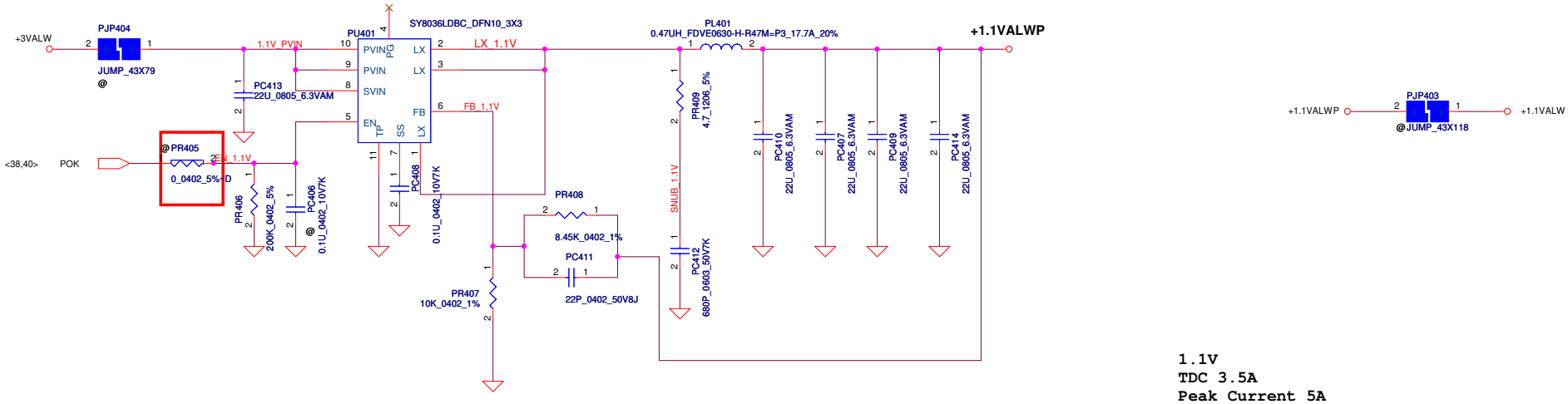

1.1V
TDC 3.5A
Peak Current 5A
OCP current 6A

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:11mohm ,	14mohm

Security Classification	Compal Secret Data		
Issued Date	2011/08/04	Deciphered Date	2012/08/03

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Compal Electronics, Inc.

Title: PWR-1.8VSP/1.1VALWP

Size | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 42 of 50

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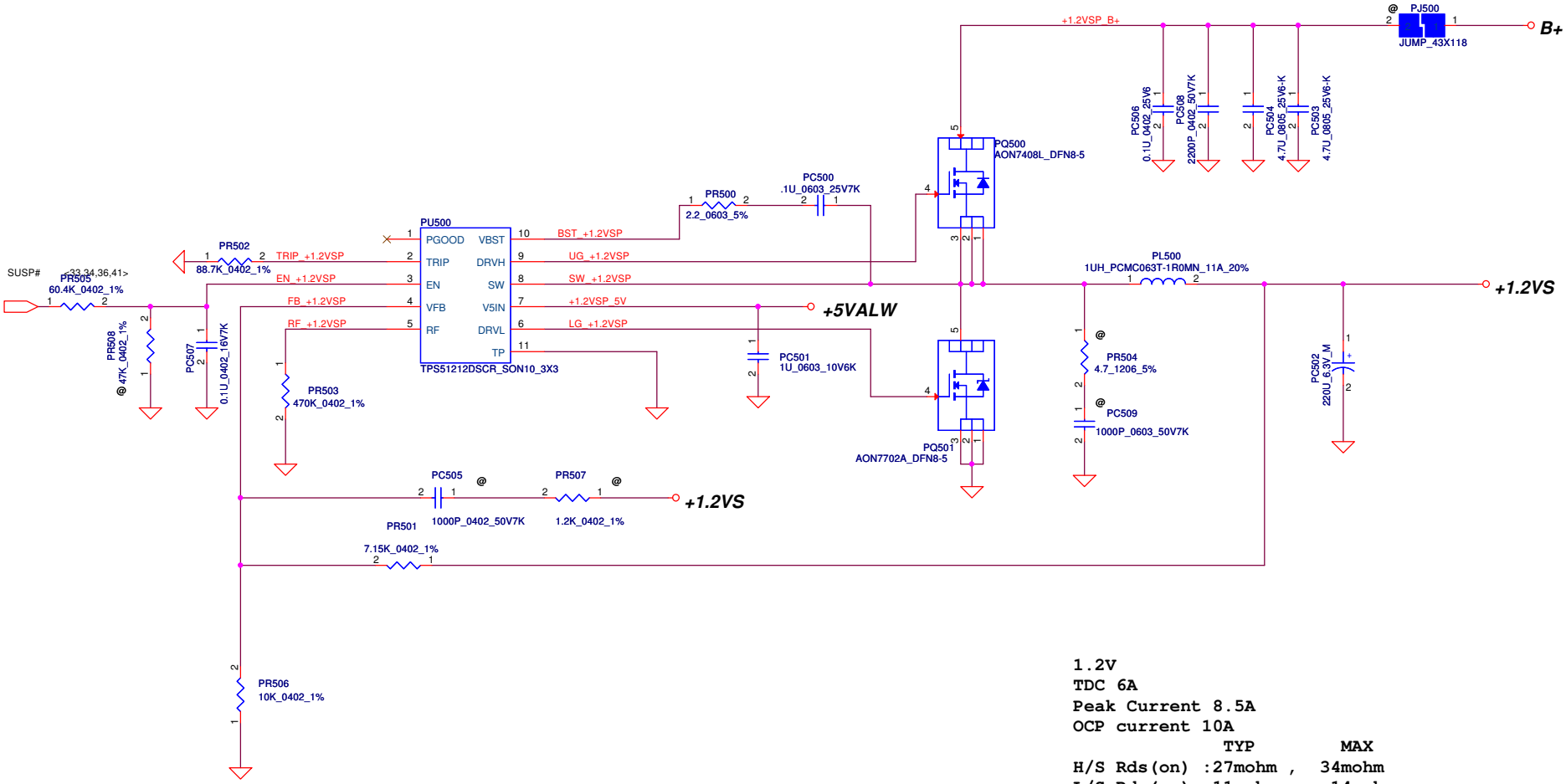
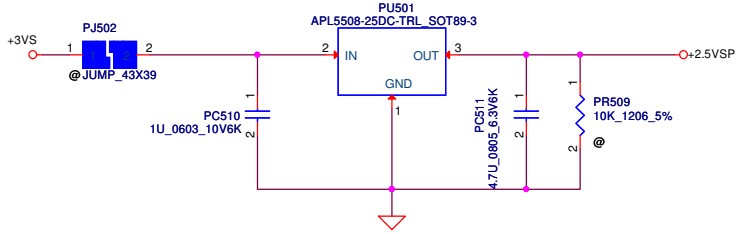


1.2V
TDC 6A
Peak Current 8.5A
OCP current 10A

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:11mohm ,	14mohm



(0.5A,20mils ,Via NO.=1)

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Compal Electronics, Inc.

Title: PWR-1.2VSP/2.5VSP

Size | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 43 of 50

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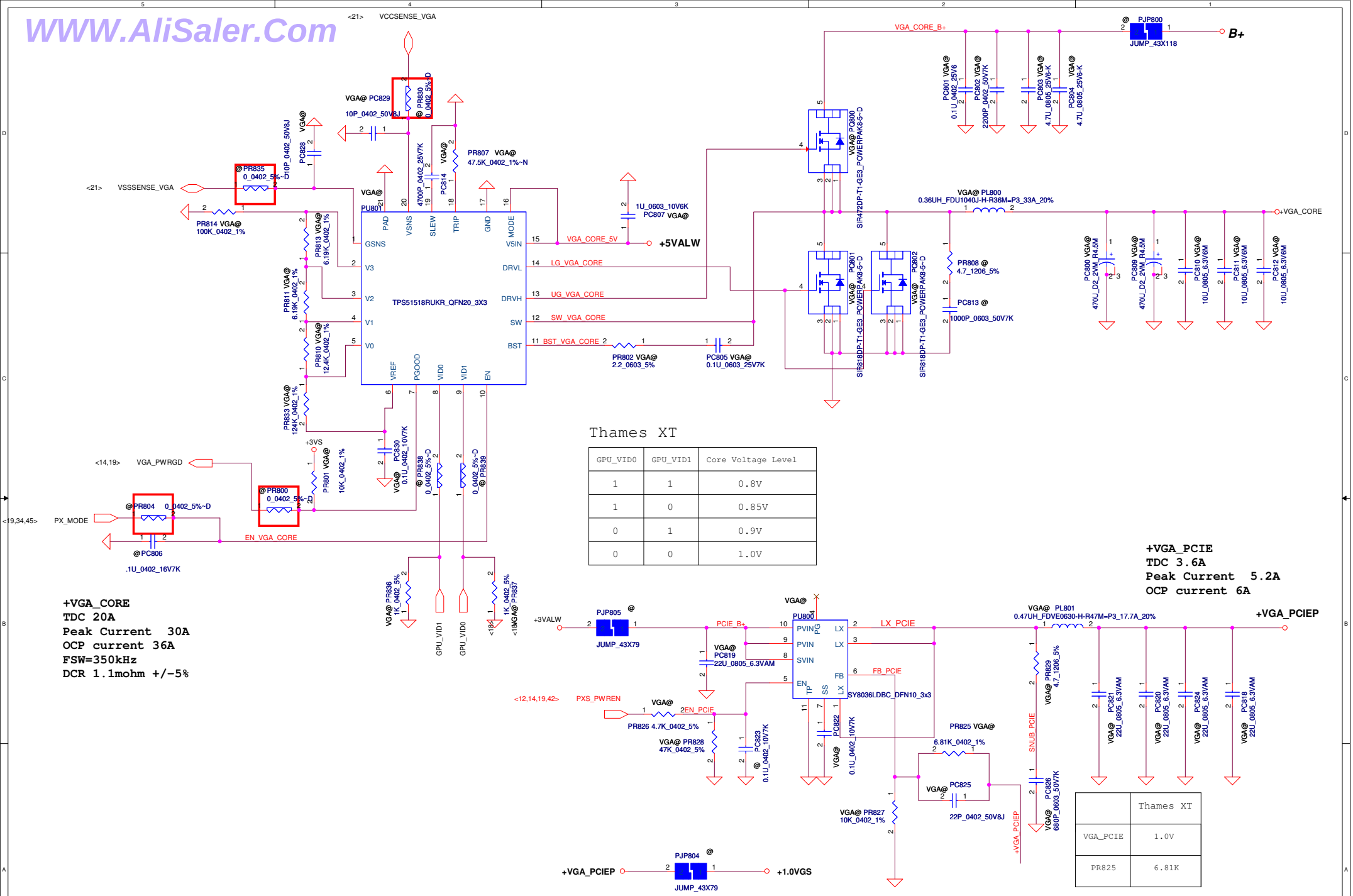

Thames XT

GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.8V
1	0	0.85V
0	1	0.9V
0	0	1.0V

	Thames XT
VGA_PCIE	1.0V
PR825	6.81K

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

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Compal Electronics, Inc.	
Title	PWR-VGA_CORE/VGA_PCIE
Size	Document Number: LA-8251P
Rev	1.0
Date:	Monday, July 16, 2012
Sheet	44 of 50

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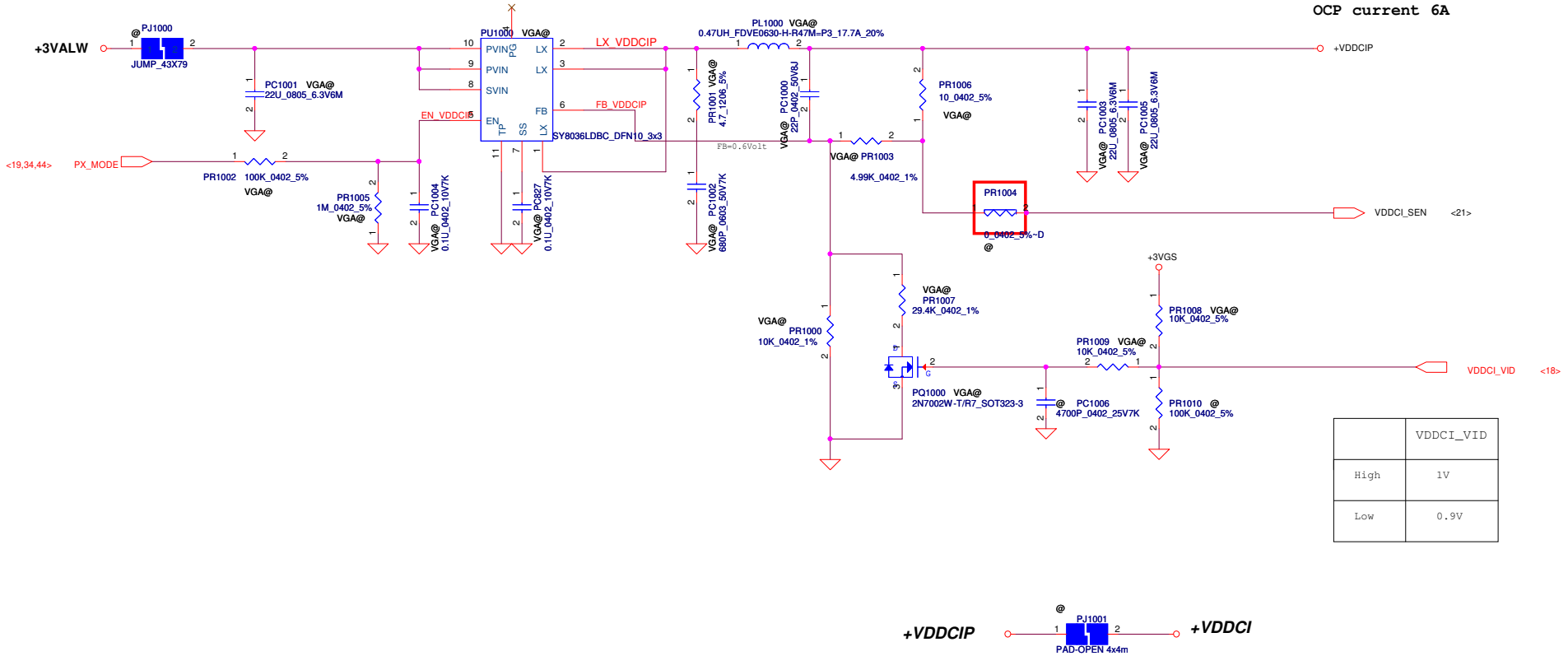
+VDDCI
TDC 2.8A
Peak Current 4A
OCP current 6A



	VDDCI_VID
High	1V
Low	0.9V

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

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Compal Electronics, Inc.

Title: +VDDCIP

Size | Document Number: LA-8251P | Rev: 1.0

Date: Monday, July 16, 2012 | Sheet 45 of 50

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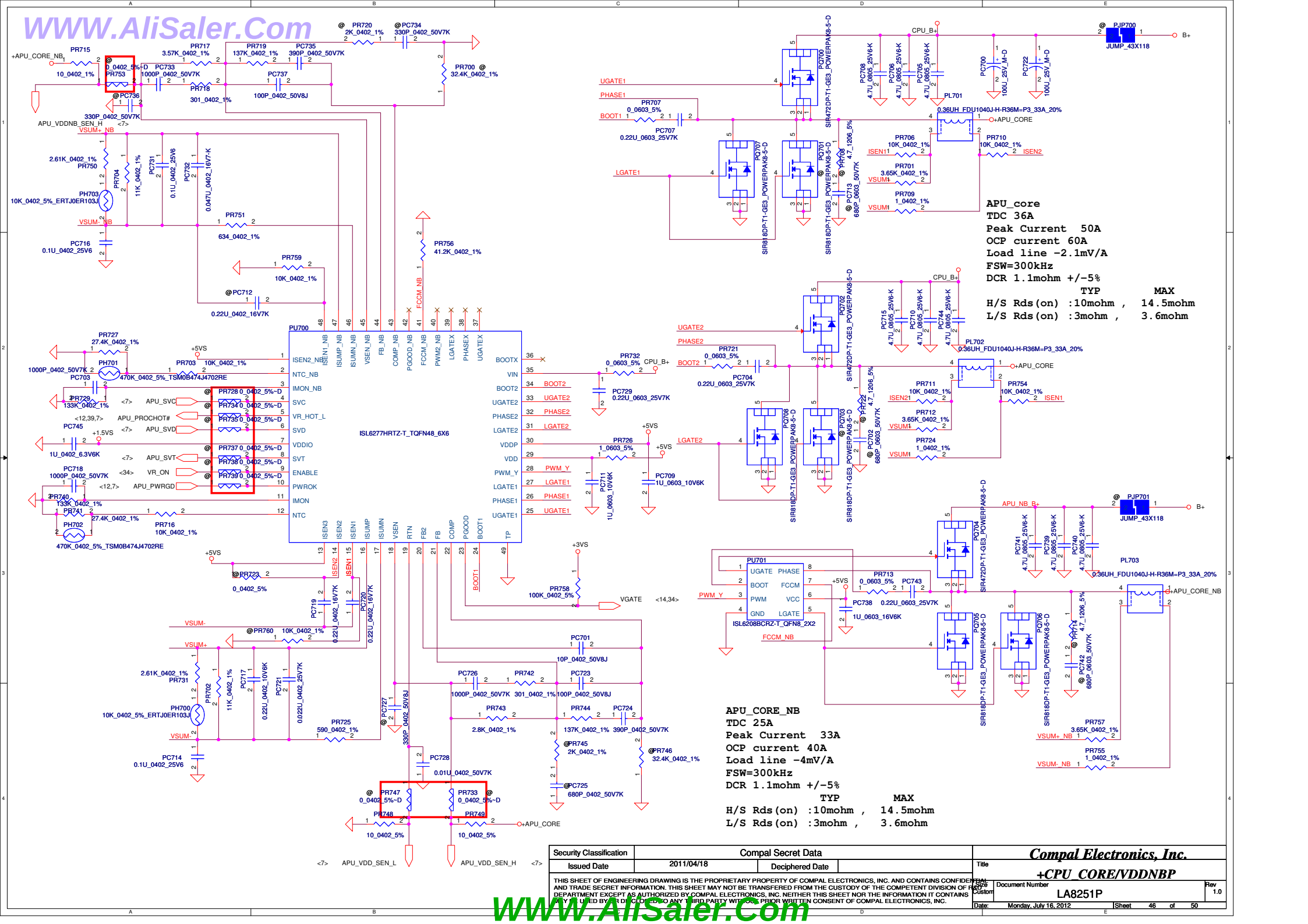

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Issued Date	2011/04/18	Deciphered Date	

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Title	Compal Electronics, Inc.
	+CPU_CORE/VDDNBP
Size: Custom	Document Number: LA8251P
Rev	1.0
Date: Monday, July 16, 2012	Sheet 46 of 50

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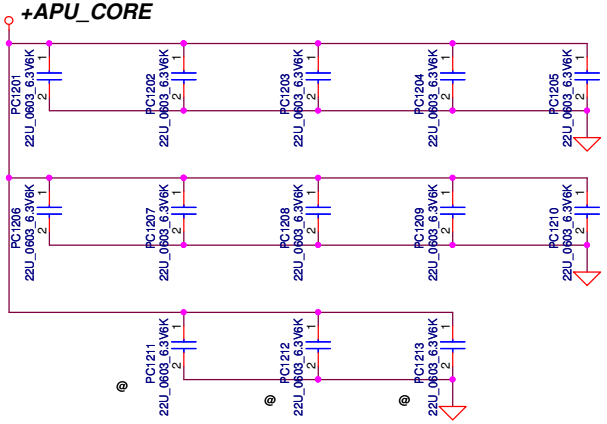
+APU_CORE

+APU_CORE



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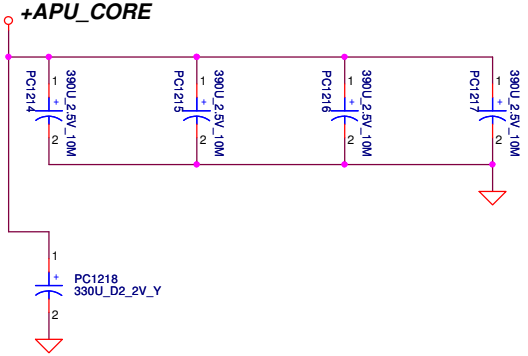
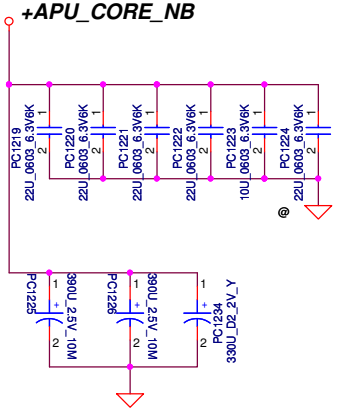
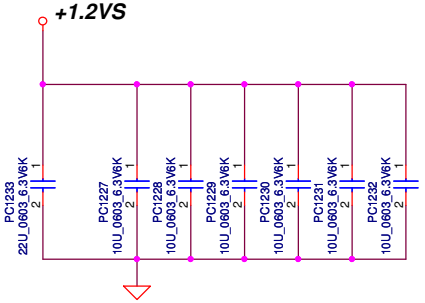


+APU_CORE_NB

+APU_CORE_NB



+1.2VS



+1.2VS

Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	

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Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
Custom	LA8251P	1.0

Date: Monday, July 16, 2012 Sheet 47 of 50

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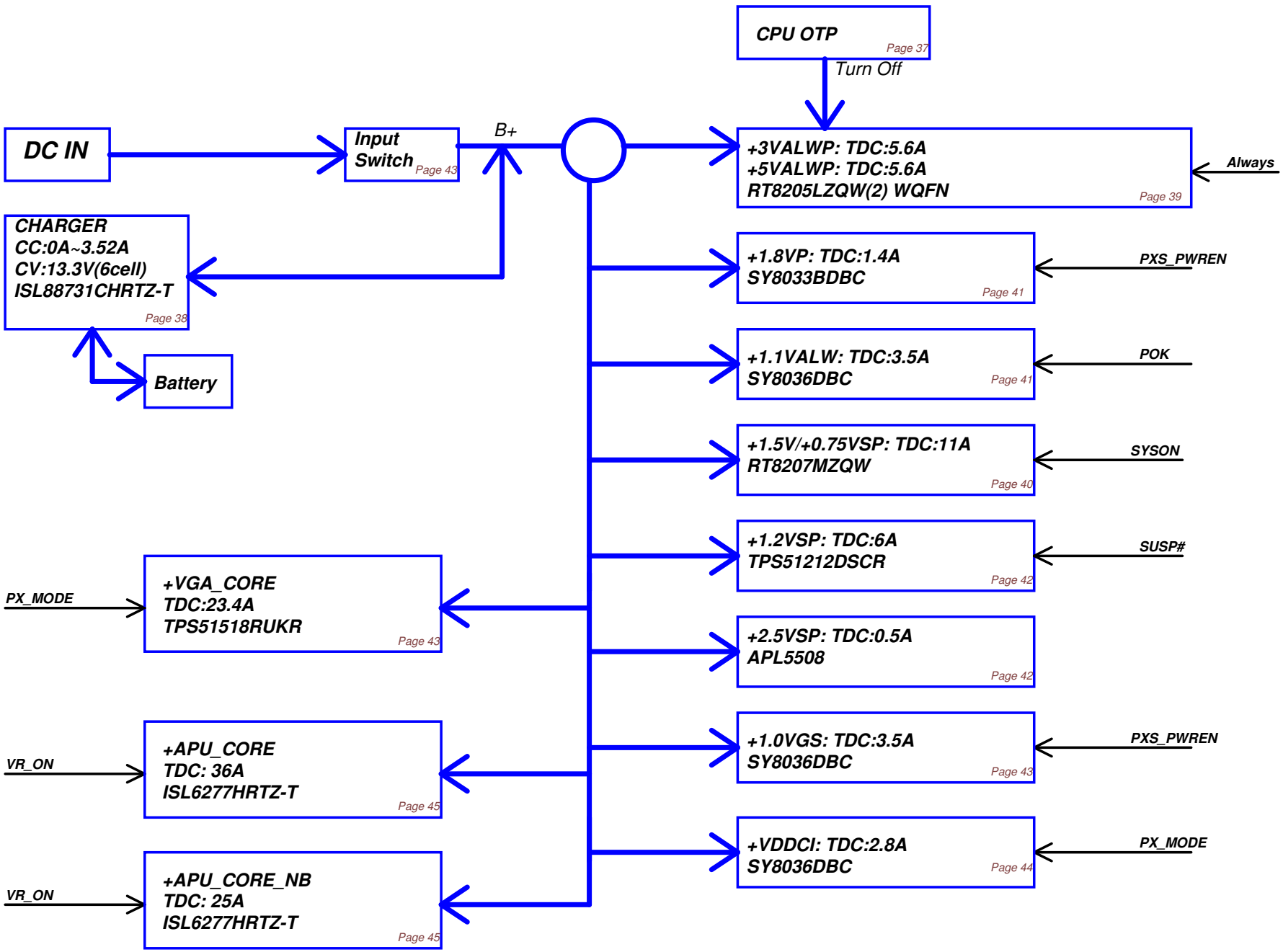
Power block



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	Title: PWR-POWER BLOCK DIAGRAM
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 48 of 50		

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/04/18	Deciphered Date	Title: PWR-PIR

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Size: C Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 49 of 50		

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	9	XXX	XX*XX/XX	Compal_XX	XXXXX	Change PRXX from Xohm to XXKohm.	X01

Design Change

Date	Page	Part reference	change description	Reason
10/17/2011	33	JLED2	Add JLED2 for Inspiron use only.	ME change drawing.
10/17/2011	30	UD1	Swap nets FCH_SDATA0/FCH_SCLK0	correct connection
10/17/2011	25	UV27.1	ADD RV327 for HPD	Vendor review
10/17/2011	25	RV268	DEL RV268	No need 1.2V from system.
10/17/2011	14	D6.D7	Change D6. D7 to Schottky for VGA PWR control	Original Diode. Vf too high.
10/17/2011	12	C159.C158	Change C159.C158 to 10pF	Vendor review
10/17/2011	12	D5.D8	Change D5. D8 to Schottky	Original Diode. Vf too high. Vendor review.
10/17/2011	27	DV8	Reserve DV8. use RV40 short.	HDMI Voltage issue.
10/17/2011	26	JLVDS	JLVDS Reverse Pin	LVDS connector location change.
10/17/2011	21	RV215	RV215 connect to net:+VDDCI	FB_VDDCI Should connect to +VDDCI
10/17/2011	37	AMP	Add an Audio AMP Circuit in page37	customer requires.
10/19/2011	33	DB7	Reserve DB7 for ESD	ESD request
10/19/2011	36	RB21	Adding RB21. change USB charge circuit power rail to +VC	USB charge sequence fine tune
10/19/2011	34	U26	Dashboard button change to U26 pin34.36.75	to meet customer spec.
10/19/2011	13	U2	KB_DET# Change to FCH GPIO56. add Q76	EC pin saving.
10/20/2011	34	R503	R503 DEL	Leakage form 3VALW to VS
10/20/2011	30	QD4	Add QD4	Leakage form 3VALW to VS
10/21/2011	33	R793.R794.R795.R796.D24	add R793.R794.R795 100K*3.R796 0ohm.D24 BAT54C	For Dashboard support 3 second boot up.
10/21/2011	37	U6	Reserve U6. C244~C251. R797~R799	Reserve GreenCLK
10/21/2011	31	JBTB1	change pin67 to +3VS. pin36.38.40.42 to +3VALW	LAN D/B design changes.
10/21/2011	27.32	JUSB2.JHDMI	update JUSB2 Footprint. JHDMI Footprint	ME change drawing.
10/25/2011	29	CA19.CA20	From 2.2UF to 4.7UF	Vendor review
10/25/2011	28	CV6.CV7.CV8	From 22pF to 10pF	CRT high resolution issue.
10/26/2011	33	R60.R8	Change to 300ohm	LED current need >5mA
10/26/2011	33	R792	Add 100Kohm to GND	Power LED issue.
10/26/2011	33	UX1	SYSON connect to UX1.20	Express Card not support S5 weakup.
10/28/2011	29	RA12.RA13	Change from 5.1ohm to 39.2ohm	Vendor review
11/21/2011	33	UX1	Connect pin4 to +3VS. pin14 to +1.5VS for 2nd GMT	2nd source required.
11/28/2011	7	Q6	Add Q6, Del Q1	ProcHot# change to High active. Common code for EC
11/28/2011	12	R109	10M reserved	Without RTC battery, system should not boot up issue
11/28/2011	36	EMI	Add C254,C255,C256,C257,C258,C259 0.1uF +1.5V	For EMI request
11/28/2011	32	UB4	AMD USB debug Port0 change to JUSB1	JUSB1 USB SI too margin. Due to switch serial resistor approx 10ohm

Design Change for PT

Date	Page	Part reference	change description	Reason
04/03/12	18	YV1	27MHz package change to small size	Sourcer's recommend for cost down
04/03/12	26	JLVDS	pin assignment change for 31,32,33,34,35,37	Sourcer's recommend for cost down
04/03/12	35	C657	add 0.1u_0402 on USB_DETECT#	ESD required
04/03/12	35	C658	add 0.1u_0402 on USB_DET#_DELAY	ESD required
04/03/12	18	RV205,RV206	add 10K_0402 reserved only.	AMD Chelsea required
04/03/12	18	R804,R805	add 0_0402 reserved only.	AMD Chelsea required
04/03/12	20	RV244,CV366,RV208	add 2K_0402 ,10P_0402, 0_0402, reserved	AMD Chelsea required
04/03/12	21	RV247,RV248	add 0_0402 reserved, RV247 stuffed.	AMD Chelsea required
04/03/12	18	RV250	add 0_0402 to GND for Thames, stuffed.	AMD Chelsea required
04/03/12	28	JCRT	footprint changed	DFB required
04/03/12	30	JHDD	footprint changed	DFB required
04/03/12	12	C158,C159,Y1	18p,18p,small size, 10P→18P	Sourcer's recommend for cost down
04/03/12	12	C155,C157,X1	12p,12p,small size, 27P→12P	Sourcer's recommend for cost down
04/12/12	19	RV104,RV101,QV21,CV96,RV103,RV109,QV25,RV99,RV100,QV18,QV19,QV20	Remove from BOM	These parts are PX4.0 supports. We support PX5.0 only.
04/12/12	19	RV112,RV113	RV113 Change 150K→240K, RV112 change 20K→240K.	Power rail +1.5VGS Timing fine tune.
04/12/12	18	R807,R806	Reserve 0ohm, R807 stuffed.	Reserve adaptor choice for dGPU GPIO5(net:AC_BATT)
04/12/12	29	R14, Q78	R14 10K, Q78 NMOS dual.	AMD recommend.
04/12/12	32	LB6, RB17, RB19	LB6 add to BOM.	EMI required.
04/12/12	13	R136	100K ohm stuffed.	Add PU for FCH GPIO171. (net:ODD_EN#)
04/12/12	14	R104	Reserve 0ohm.	Reserve for ODD_DA#
04/12/12	33	C260, C261, C262, C263	0.1uF stuffed.	ESD required
04/10/12	8	C100	Change to SGA00002280	ME Height limit. 4mm.
04/11/12	27	CV365,CV367	add 0.1U_0402_10V7K~D, reserve only.	EMI required, add caps in HDMI DDC
04/12/12	33	L3	add DLW21SN900SQ2_0805~D, reserve only.	EMI required, add CC in Cardreader
05/02/12	7	C71	pop 0.1U_0402_16V4Z	EE required, Shutdown issue, Leason learn from CGs

Design Change for ST

Date	Page	Part reference	change description	Reason
05/31/12	26,33,31	RV328,R808,R774	add 300_0402_5%~D	AMD required, USB20 D- add RC for device lose
05/31/12	26,33,31	CV368,C155,C795	add 15P_0402_50V8J~D	AMD required, USB20 D- add RC for device lose
05/31/12	18,28	RV220,RV223,RV217,RV226,RV222,RV225,RV221,RV224,RV216,RV227,RV218,RV228,RV219,RV229	delete CRT debug	AMD required, for VGA layout concern.
05/31/12	7	Q6	reverse Q6	EE required
05/31/12	27	RV329,RV330	add 0_0603_5%~D	EMI required, DDC EMI issue.
05/31/12	27	D20	add PESD24VS2UT_SOT23-3~D, reserve only.	ESD required, HDMI plug issue, Leason learn from CGs
06/22/12	18	R806	pop R806 0ohm	Fast Power reduce function
06/23/12	27	RV39, RV41, RV42, RV44, RV53, RV54, RV57, RV58	Remove these part	change to common mode chock
06/24/12	27	LV4, LV5, LV6,LV7	add these KINGCORE WCM-2012HS-900T common mode chock	EMI required for HDMI noise
06/25/12	27	CV351, CV352, CV349, CV350, CV353, CV354, CV355, CV356	add these 3.3pF 50V 0402	EMI required for HDMI noise
06/26/12	27	CV364, CV363, CV360, CV361, CV358, CV357, CV362, CV359	add these 1pF 50V 0402	EMI required for HDMI noise
06/22/12	32	DB4	Remove	USB detect issue

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Issued Date	2011/04/18	Deciphered Date	Title: HW-PIR
Size: Custom	Document Number: LA8251P		Rev: 1.0
Date: Monday, July 16, 2012	Sheet 50 of 50		

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