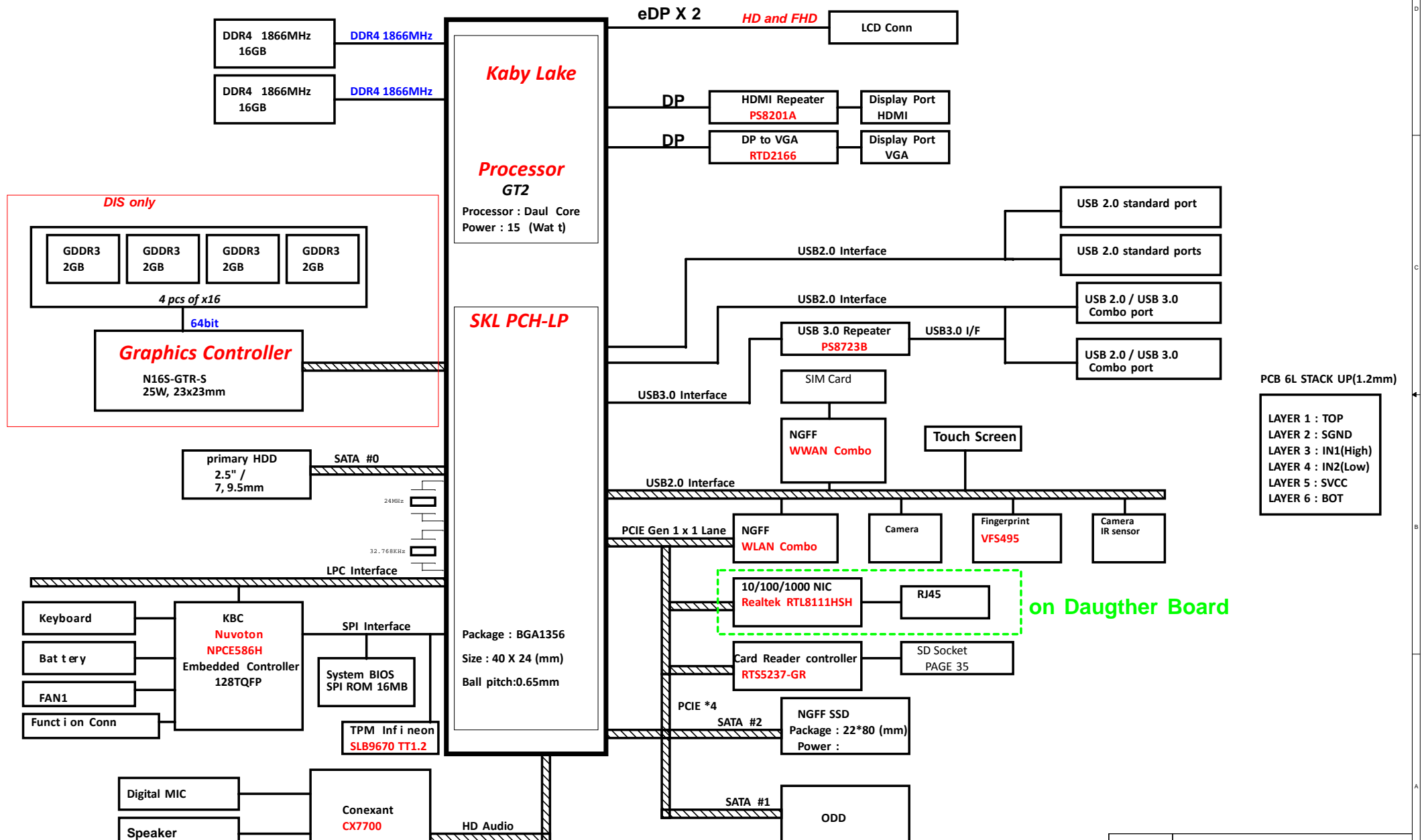
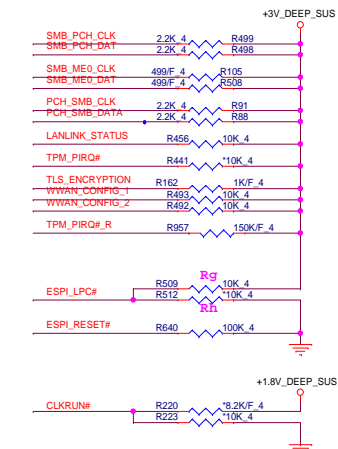


# 2015 400 series Kaby Lake 15"/ 17" (UMA/DIS) Block Diagram 01







LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R660	<b>Ra</b> 0Ω	15Ω
R662	<b>Rb</b> 0Ω	15Ω
R661	<b>Rc</b> 0Ω	15Ω
R646	<b>Rd</b> 0Ω	15Ω
R653	<b>Rf</b> UNINSTAL	INSTAL
R509	<b>Rg</b> UNINSTAL	INSTAL
R512	<b>Rh</b> INSTAL	UNINSTAL

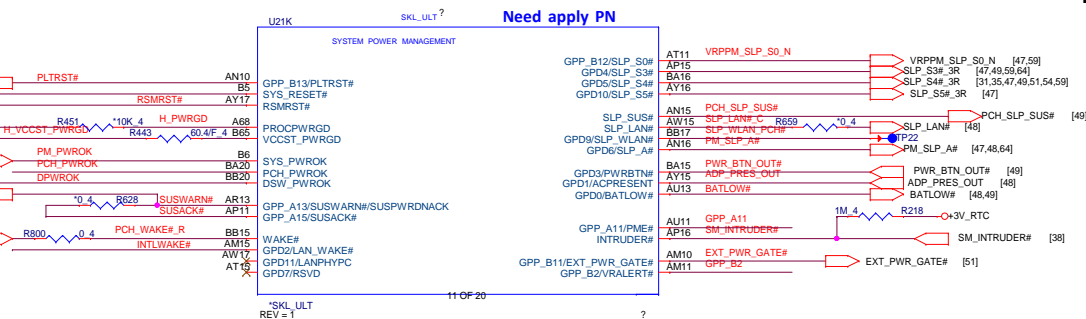
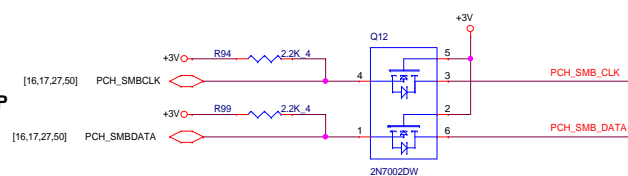
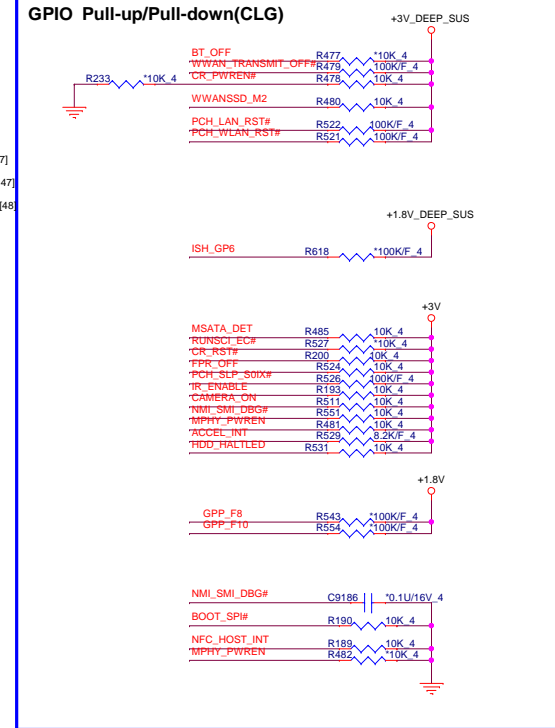


Figure 10 shows the I/O pin connections for the Intel Atom™ C3000 SoC. The diagram illustrates the following connections:

- BATLOW#** (R622) is connected to **+3VPCU**.
- TOP\_PRES#\_OUT** (R644) is connected to **+3VPCU**.
- INTLWAKE#** (R100) is connected to **+3VPCU**.
- PCH\_WAKE#** (R645) is connected to **+3VPCU**.
- PCH\_WAKE#\_R** (R801) is connected to **+3VPCU**.
- PCI\_3S\_SERIRQ** (R954) is connected to **+3V**.
- +1.8V\_DEEP\_SUS** is connected to **PCI\_3S\_SERIRQ** (R954).
- PCI\_3S\_SERIRQ** (R655) is connected to **+1.8V\_DEEP\_SUS**.
- GPP\_A11** (R282) is connected to **+1.8V\_DEEP\_SUS**.
- SUSWARM#** (R629) is connected to **+1.8V\_DEEP\_SUS**.
- GPP\_B2** (R547) is connected to **+3V\_DEEP\_SUS**.

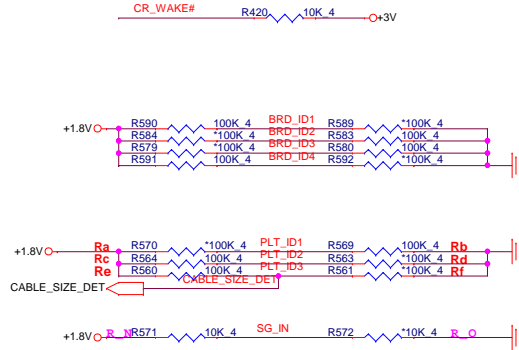
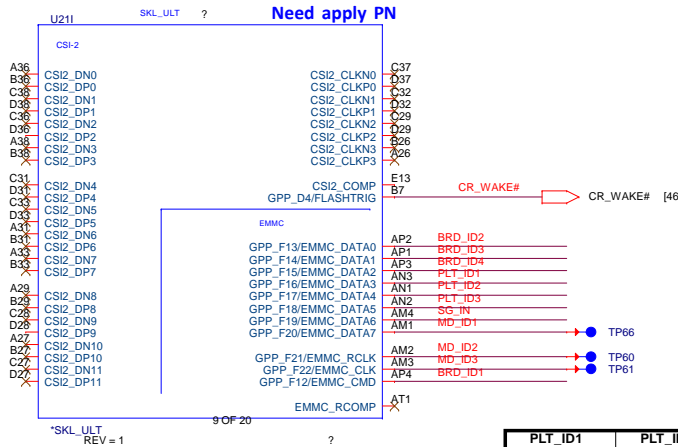




Conexant CX7501 & CX7700 TABLE (SI stage)		
	CX7501	CX7700
Rc	UNINSTALL	INSTALL
Rd	INSTALL	UNINSTALL

Pin	Function	Pin Numbers
1	+1.8V	[5,8,30,55,64]
2	+3VPCU	[3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
3	+3V_DEEP_SUS	[3,5,6,8,10,37,43,47,48,50,56,59,64]
4	+3V	[2,3,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

BOARD REVISION	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
Pre-PV	1	0	0	0	
PV	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



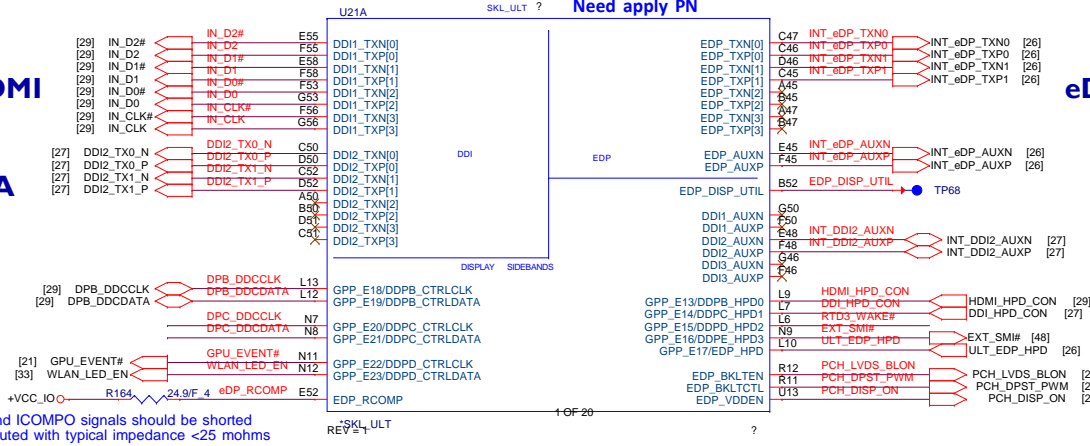
PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	1	15.6"
0	1	1	17.3"

SG_IN	Install	Un-Install
UMA	R572 R_O	R571 R_N
DIS	R571 R_N	R572 R_O

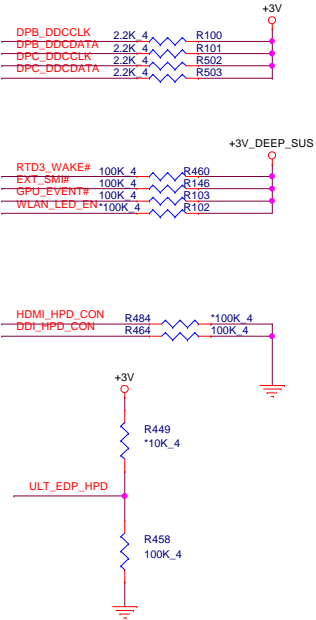
Cable detect

HDMI


VGA



eDP



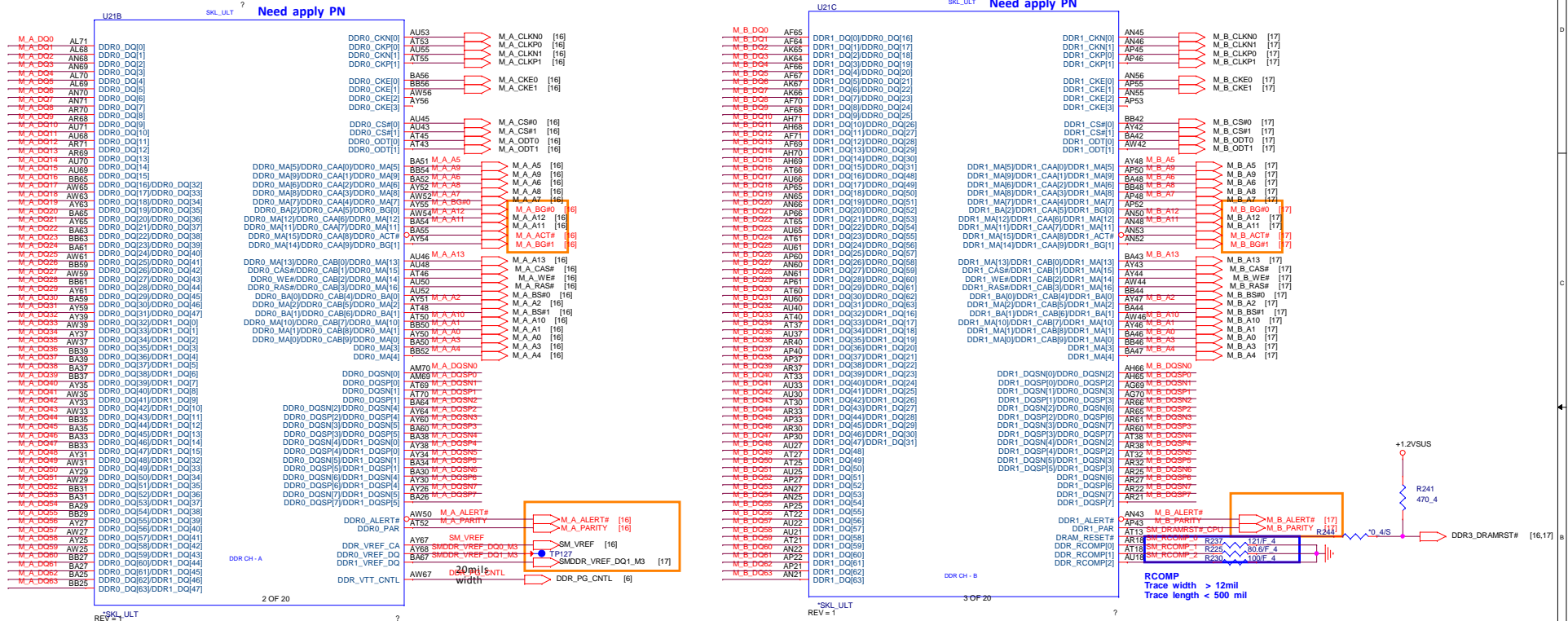
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

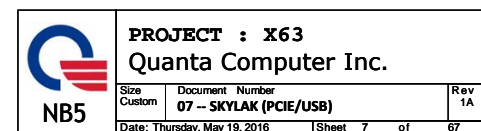


NB5

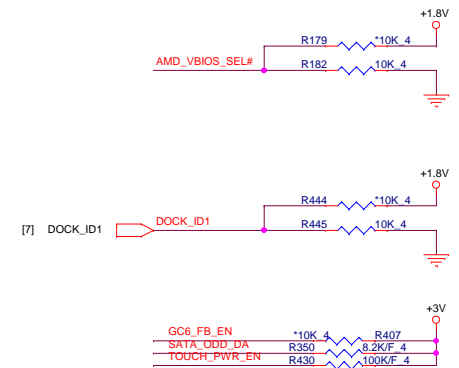
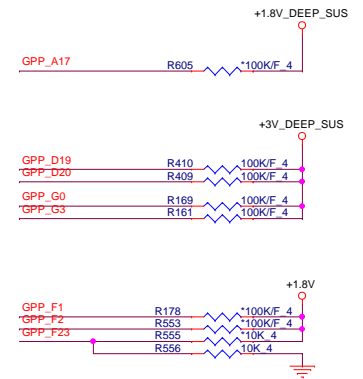
**PROJECT : X63**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>05 - SKYLAKE (eDP/DDI/Board ID)</b>	Rev 1A
Date: Thursday, May 19, 2016		Sheet 5 of 67



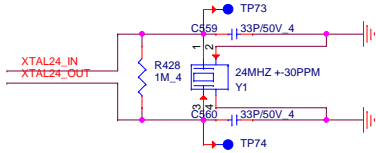






AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	





**Figure 1-1: Pinmux diagram**

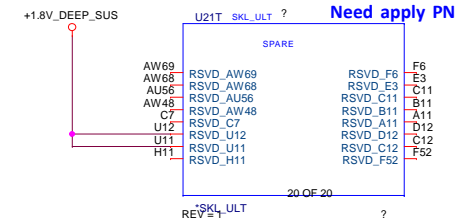
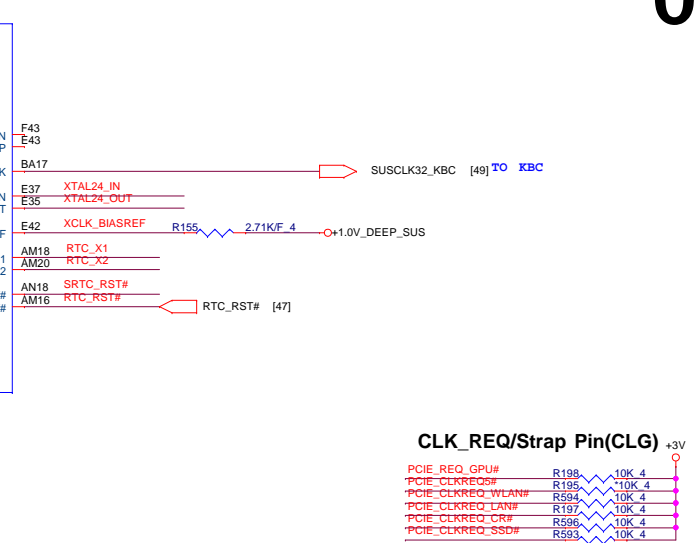
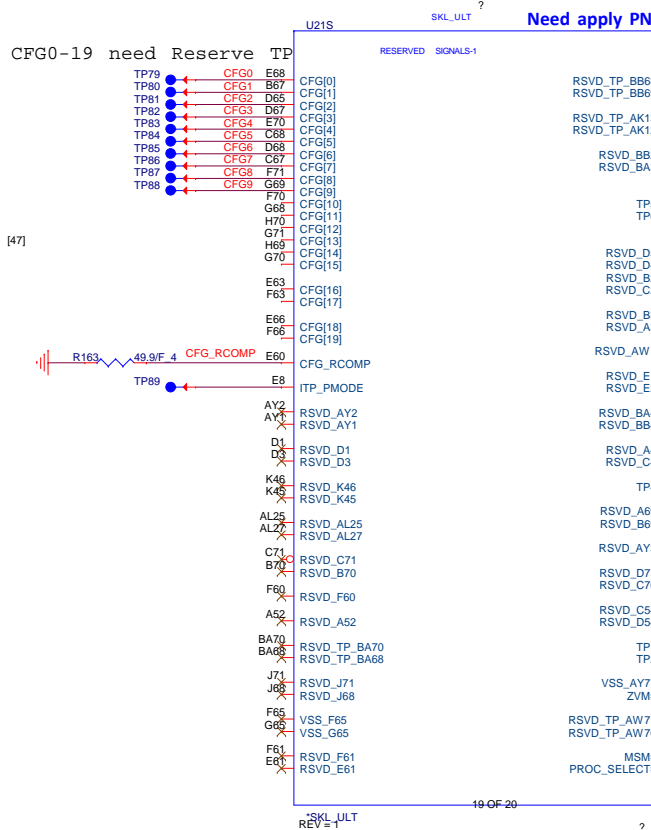
The diagram illustrates the pinmux configuration for the U21J device, showing the mapping of various peripheral signals to specific pins. The signals are grouped by peripheral type:

- SSD:**
  - CLK\_PCIE\_SSDN (D42)
  - CLK\_PCIE\_SSDP (C42)
  - PCIE\_CLKREQ\_SSD# (A10)
- Cardreader:**
  - CLK\_PCIE\_CRN (B42)
  - CLK\_PCIE\_CRP (A42)
  - PCIE\_CLKREQ\_CR# (A17)
- LAN:**
  - CLK\_PCIE\_LANN (D41)
  - CLK\_PCIE\_LANP (C41)
  - PCIE\_CLKREQ\_LAN# (A18)
- WLAN:**
  - CLK\_PCIE\_WLANN (D40)
  - CLK\_PCIE\_WLANP (C40)
  - PCIE\_CLKREQ\_WLAN# (A10)
- dGPU:**
  - CLK\_GFX\_N (B40)
  - CLK\_GFX\_P (A40)
  - PCIE\_REQ\_GPU# (A08)

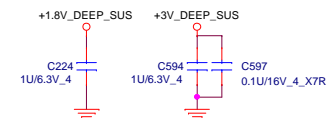
Additional signals shown include:


- CLKOUT\_PCIE\_N0
- CLKOUT\_PCIE\_P0
- GPP\_B5/SRCCCLKREQ0#
- CLKOUT\_PCIE\_N1
- CLKOUT\_PCIE\_P1
- GPP\_B6/SRCCCLKREQ1#
- CLKOUT\_PCIE\_N2
- CLKOUT\_PCIE\_P2
- GPP\_B7/SRCCCLKREQ2#
- CLKOUT\_PCIE\_N3
- CLKOUT\_PCIE\_P3
- GPP\_B8/SRCCCLKREQ3#
- CLKOUT\_PCIE\_N4
- CLKOUT\_PCIE\_P4
- GPP\_B9/SRCCCLKREQ4#
- CLKOUT\_PCIE\_N5
- CLKOUT\_PCIE\_P5
- GPP\_B10/SRCCCLKREQ5#

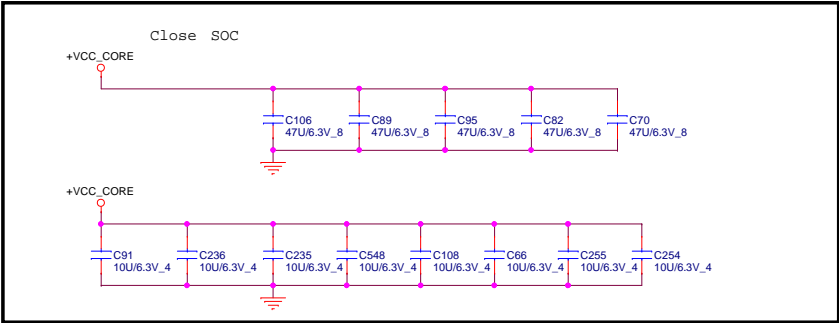
The diagram is divided into two main sections: **Need apply PN** (top) and **SKL\_UJT ?** (bottom). The bottom section includes a note: "10 OF 20".



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 <b>NB5</b>	<b>PROJECT : X63</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>10 -- SKYLAKE (PCH POWER)</b>	Rev <b>1A</b>
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Layout note: be routing together and ALERT need connection CLK and DATA.

**CLOSE TO CPU  
PLACE THE PU RESISTORS**

**SVID ALERT**

H\_CPU\_SVIDALRT# R90 220/F 4 VR\_SVID\_ALERT# [57]

**PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE**

**SVID CLK**


VR\_SVID\_CLK VR\_SVID\_CLK [57]

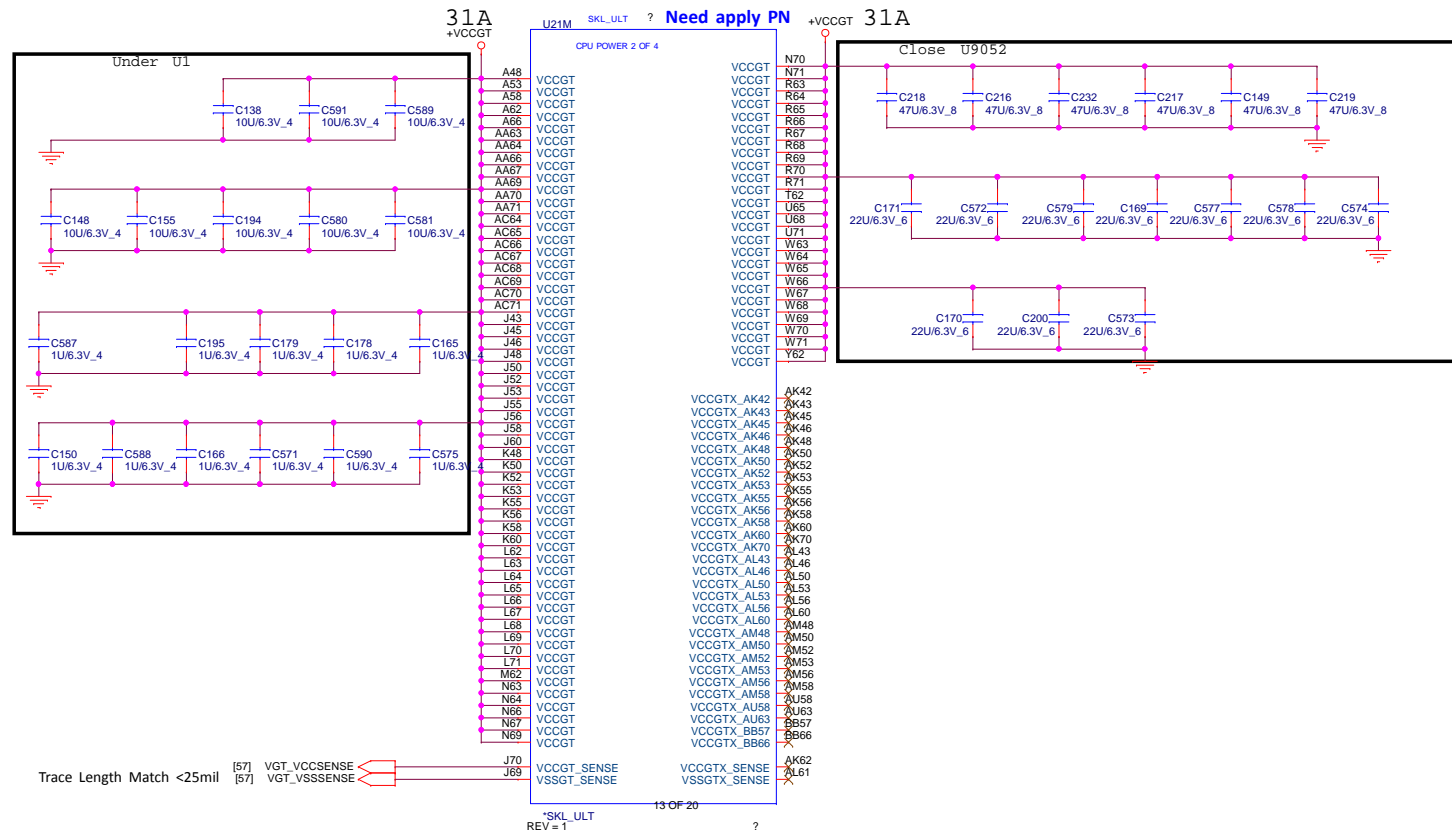
**CLOSE TO CPU  
PLACE THE PU RESISTORS**

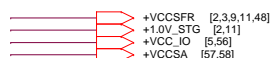
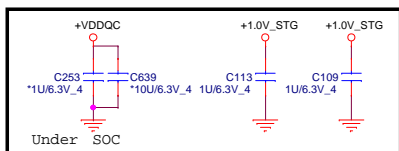
**SVID DATA**

VR\_SVID\_DATA VR\_SVID\_DATA [57]

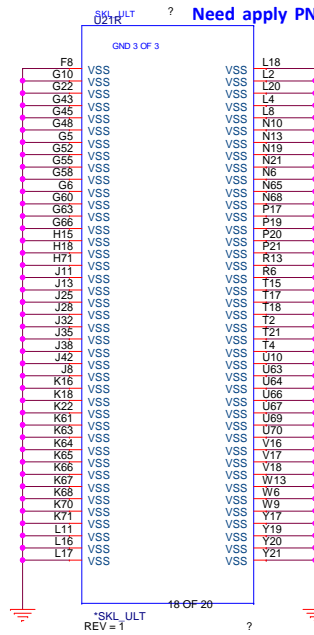


	<b>PROJECT : X63</b> <b>Quanta Computer Inc.</b>		
	<b>Size</b> Custom	<b>Document Number</b> <b>11 -- SKYLAKE (POWER-1)</b>	<b>Rev</b> 1A
	<b>Date:</b> Thursday, May 19, 2016		<b>Sheet</b> 11 <b>of</b> 67

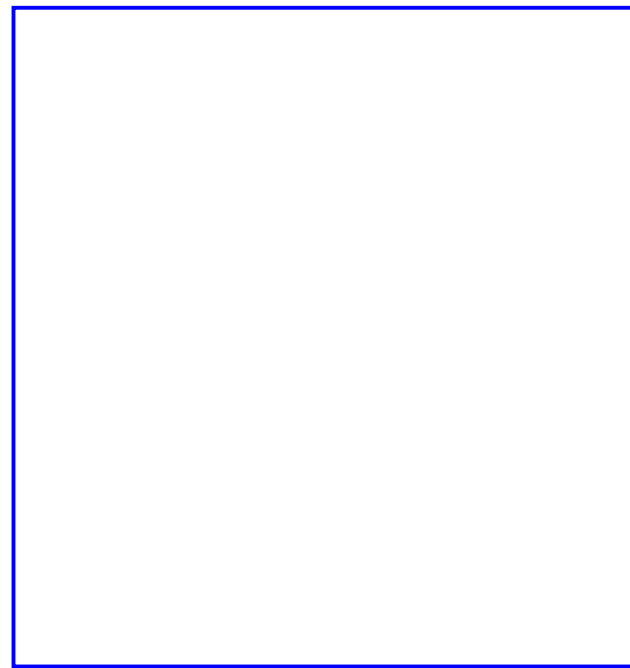




Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



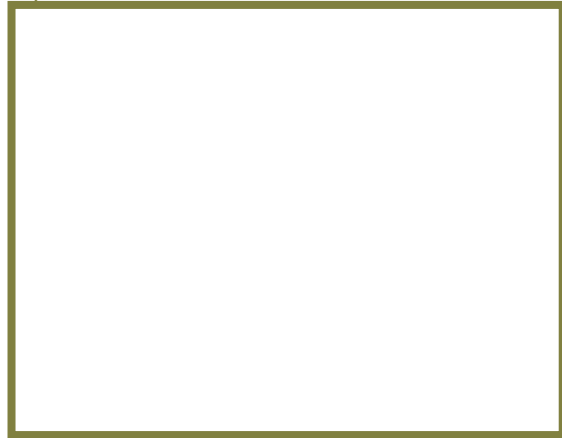
10/28 Del XDP



11/03 Del XDP



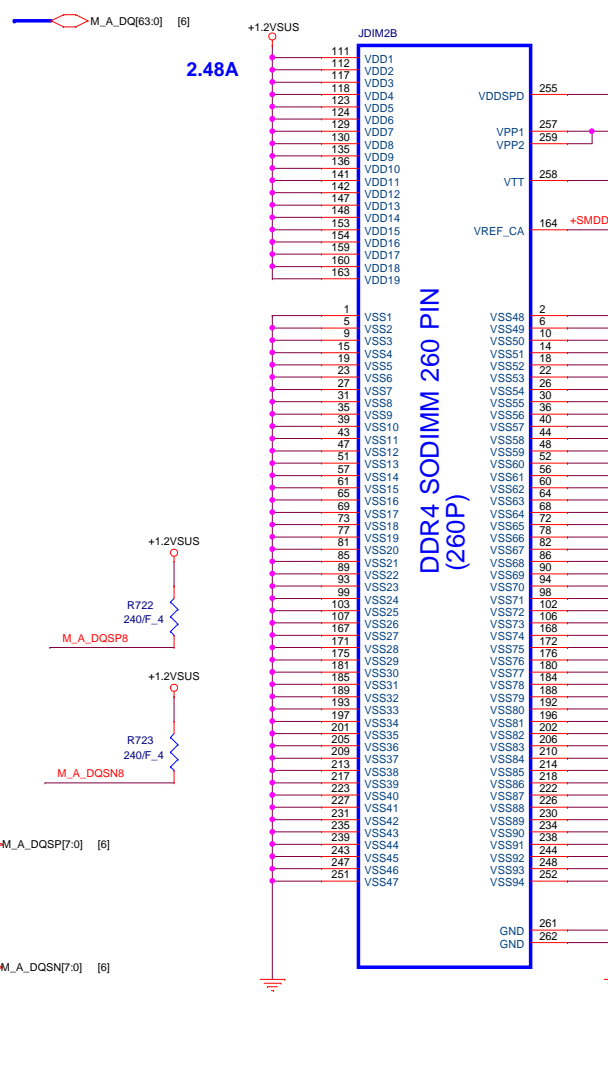
PV, 0421 Delete APS Connector



11/03 Del XDP







**For EMI RESERVE**

EC31 \*120P/50V\_4

EC32 \*120P/50V\_4

EC29 \*0.1U/16V\_4 X7R

EC26 \*0.1U/16V\_4 X7R

EC22 \*120P/50V\_4

EC18 \*120P/50V\_4

EC19 \*120P/50V\_4

EC17 \*120P/50V\_4

DDR\_VTT

EC27 \*120P/50V\_4

EC30 \*120P/50V\_4

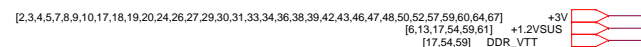
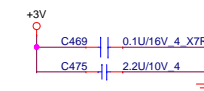
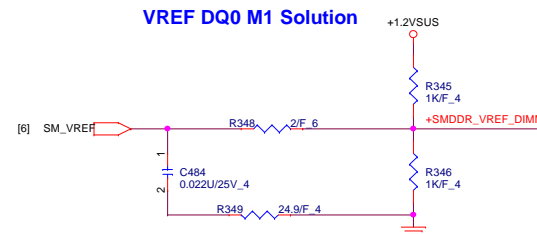
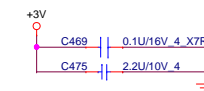
+SMDDR\_VREF\_DIMM

C498 0.1U/16V 4 X7R

C496 2.2U/10V 4

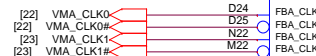
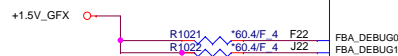
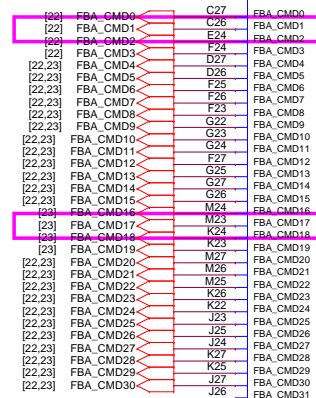
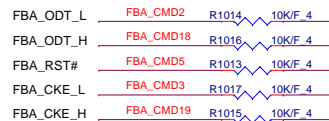
Place these Caps near So-Dimm0

For RF Reserved



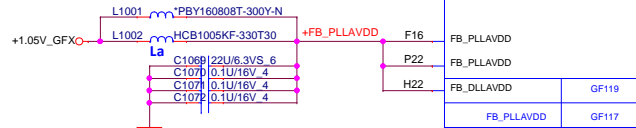




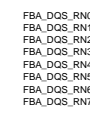
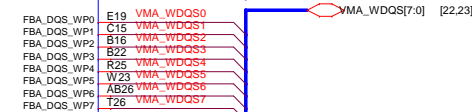
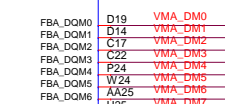
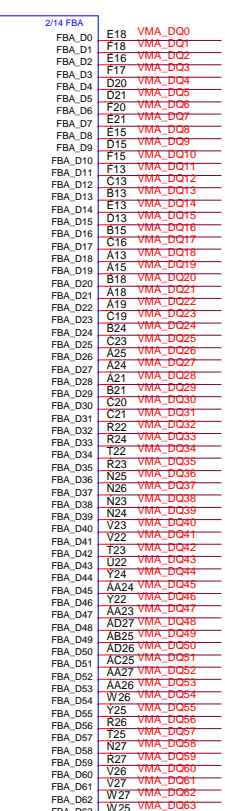


FB\_PLLAVDD = 55mA

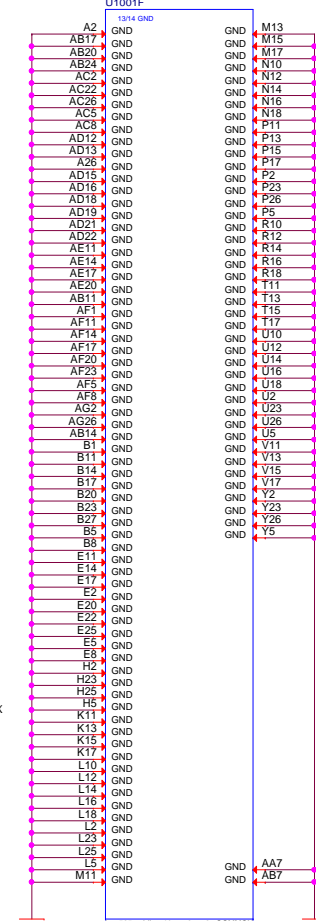
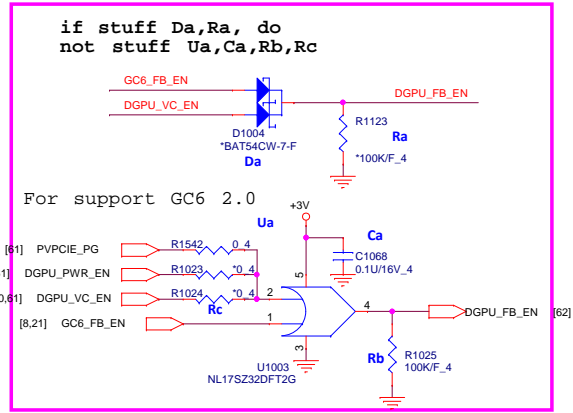
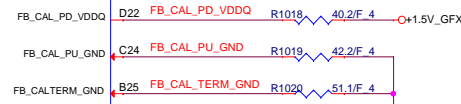
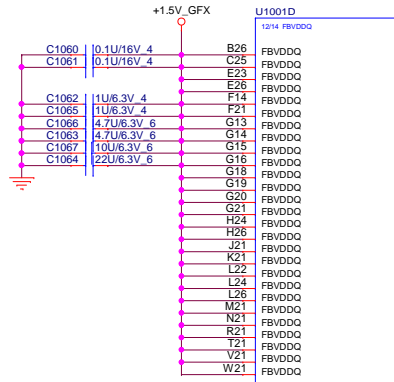
Add La (0402) for co-lay



FB\_DLLAVDD = 15mA



FBVDDQ + FBVDD = 3.116A



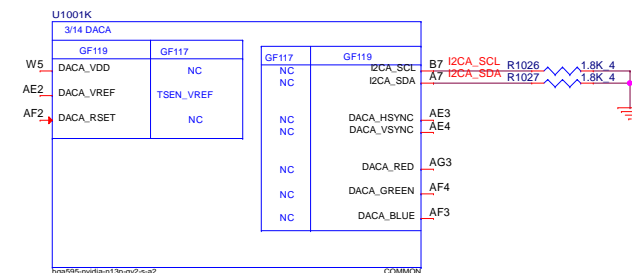
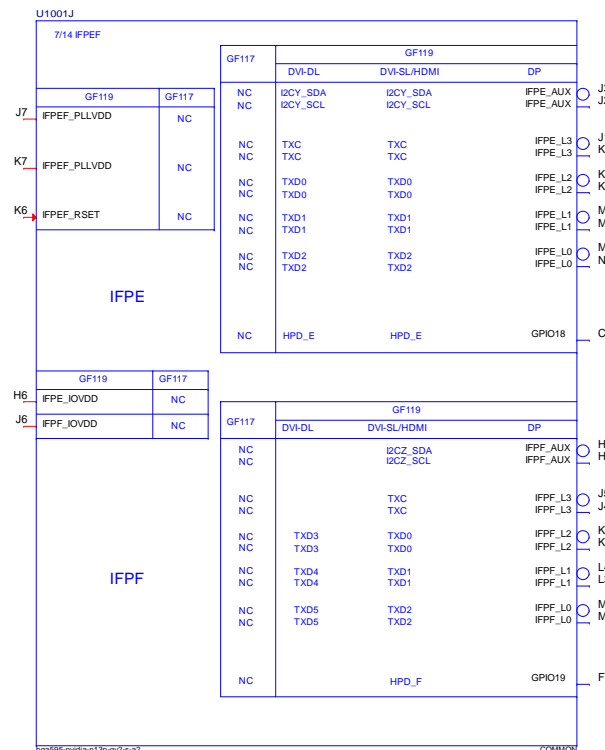
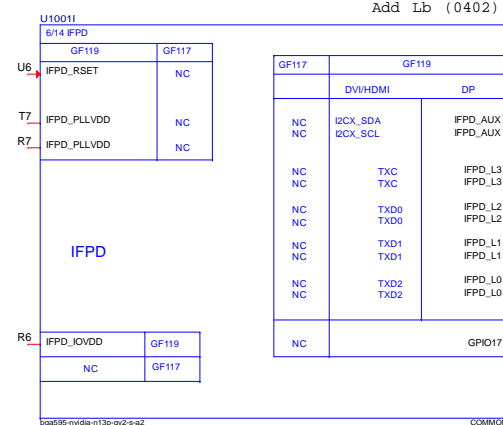
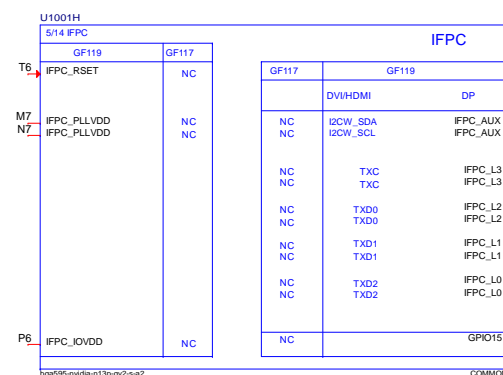
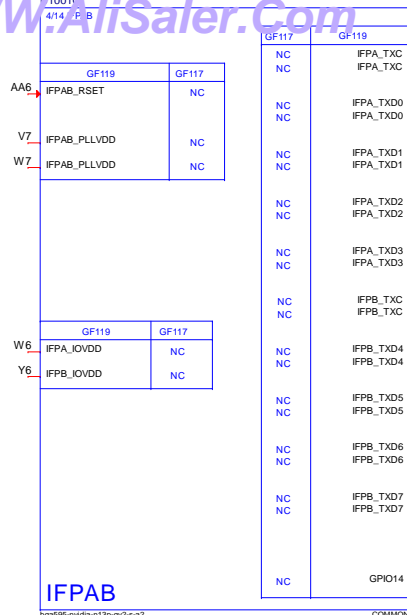
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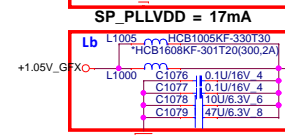
**NB5**

Size Custom Document Number **N16S-GMR (MEMORY/GND)** Rev 1A

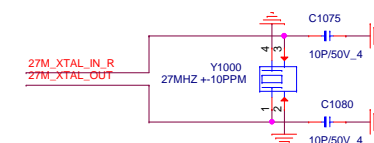
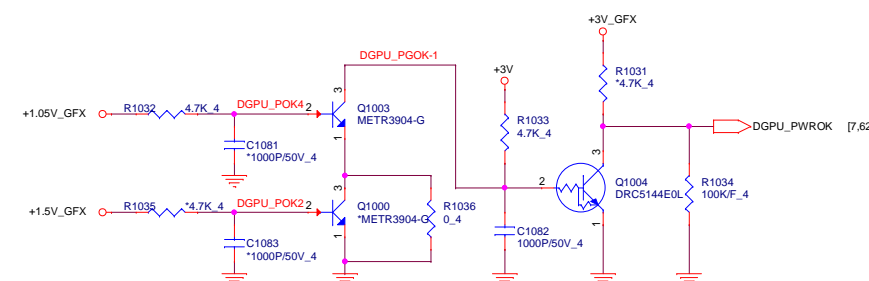
Date: Thursday, May 19, 2016 Sheet 19 of 67



PLLVD = 38mA Add La (0402) for co-lay



VID\_PLLVDD = 41mA



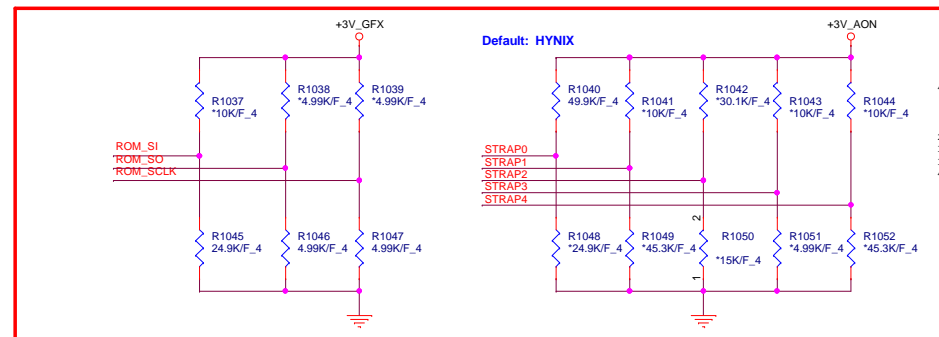
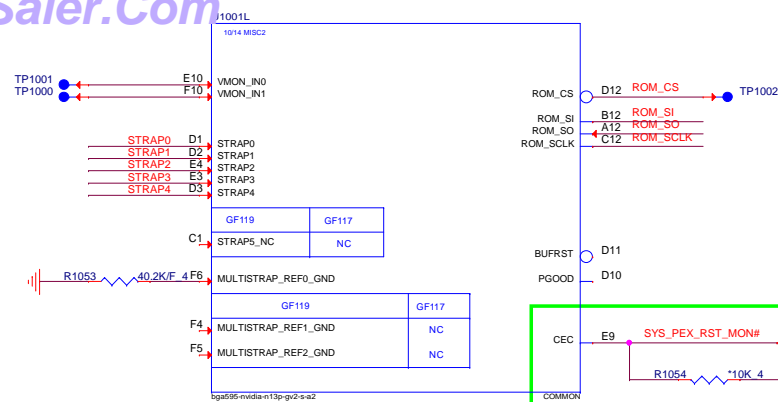


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5P2DWT01	AKD5P2DWT02
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59G8T11	AKD59G8T100
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

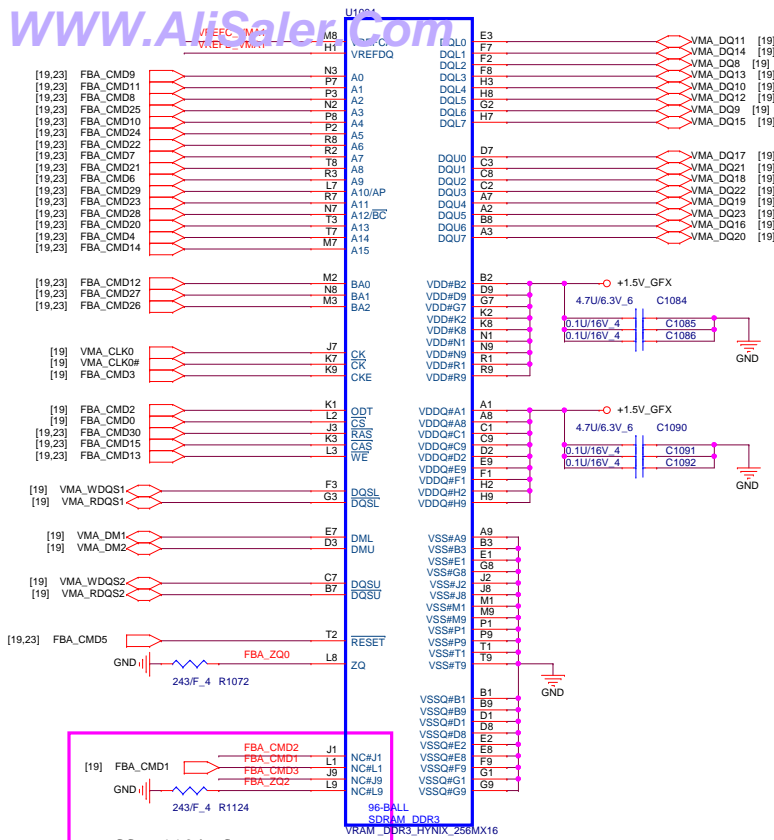
**PROJECT : X63**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev 1A
N16S-GMR (GPIO/STRAPS)		
Date: Thursday, May 19, 2016	Sheet 21 of 67	



Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
 MIC 256Mx16, MT41J256M16HA-093G:E QBC PN AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
 SAM 256Mx16, K4W4G1646D-BC1A QBC PN AKD5PGWT501---TOP B/S PN : AKD5PGWT502



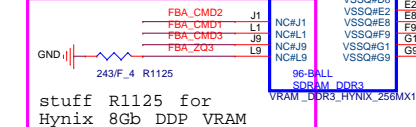
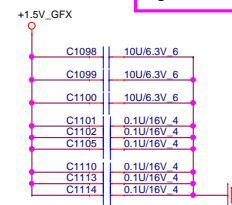
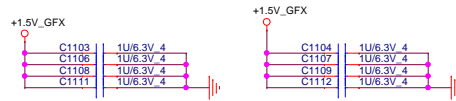
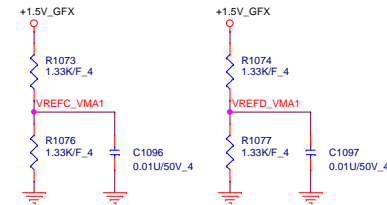
stuff R1124 for Hynix 8Gb DDP VRAM

reserve for Hynix 8Gb DDP VRAM

SDDR3\_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN FBAO ODT1	J1	NC/ODT1
SNN FBAO CKE1	J9	NC/CKE1
SNN FBAO CS1	L1	NC/CS1
SNN FBAO ZQ1	L9	NC/ZQ1

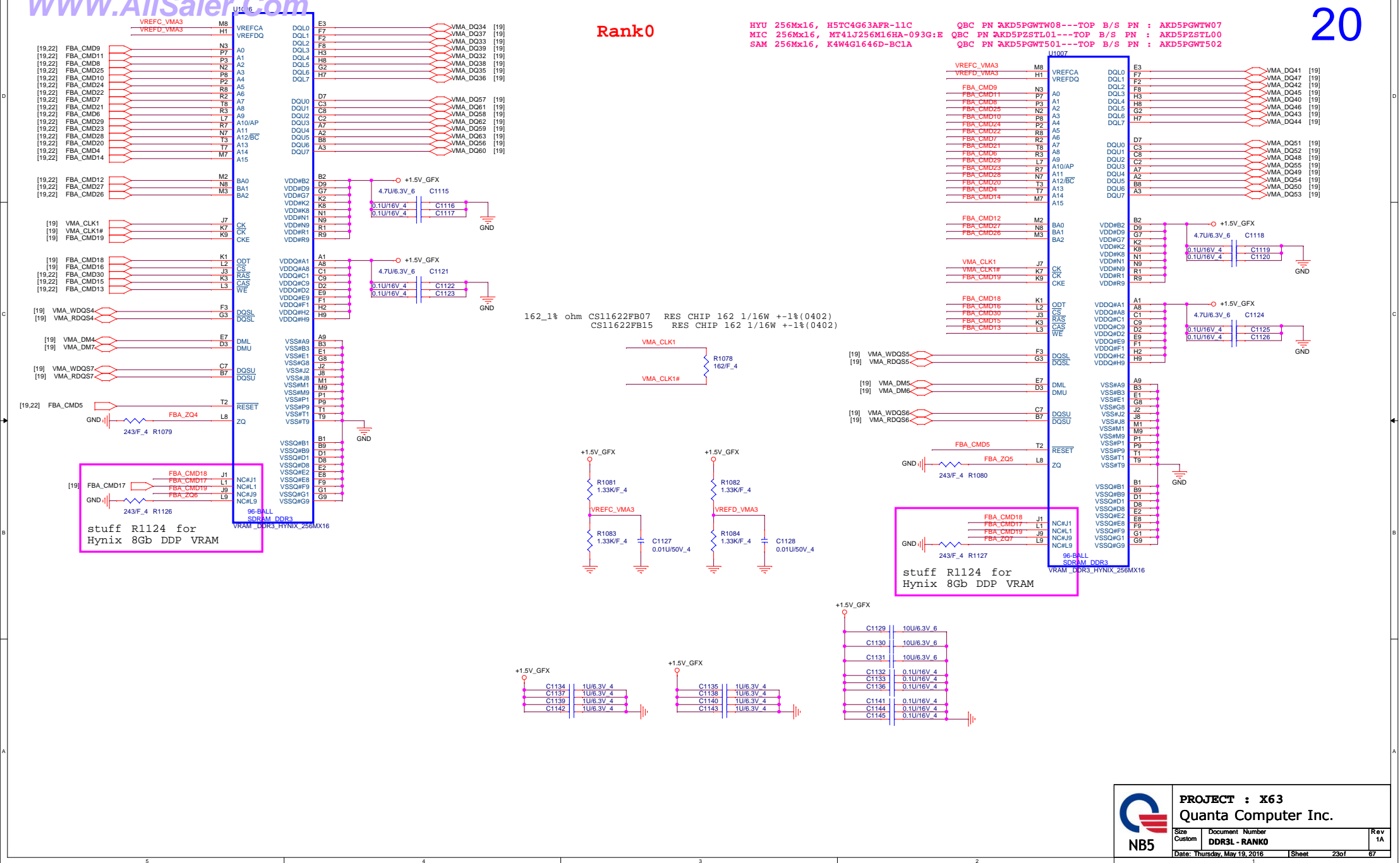


stuff R1125 for Hynix 8Gb DDP VRAM

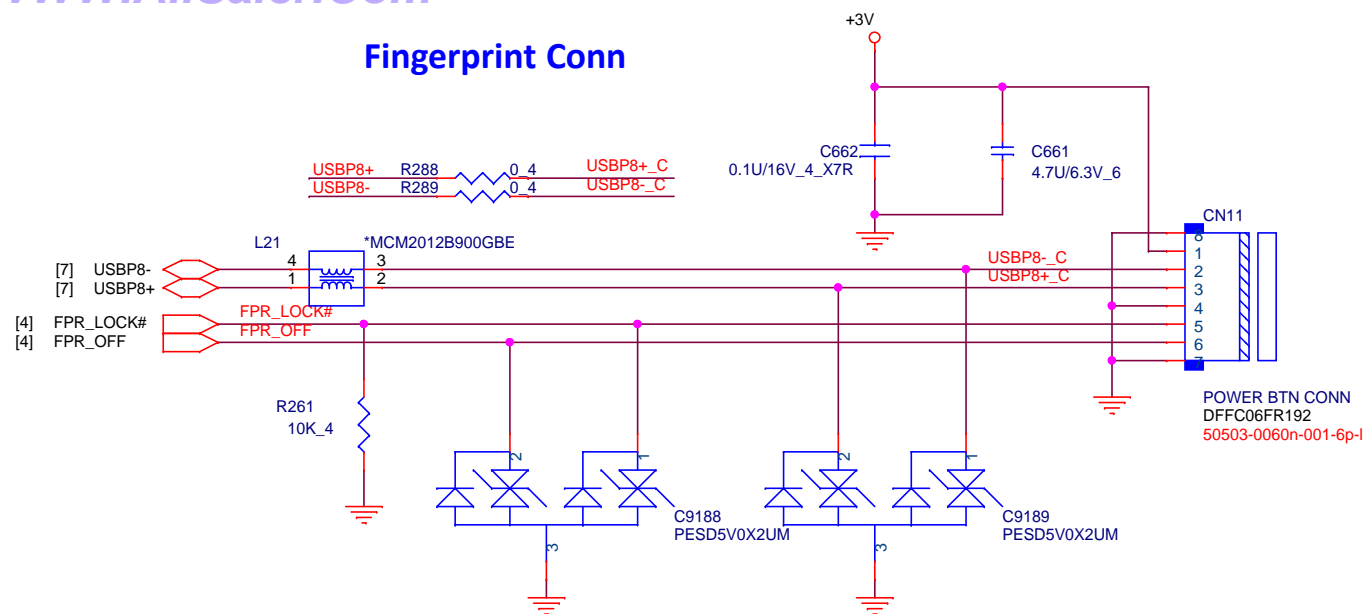
**PROJECT : X63**  
**Quanta Computer Inc.**


Size Custom Document Number **DDR3L - RANK0** Rev 1A  
 Date: Thursday, May 19, 2016 1 Sheet 22 of 67






# Fingerprint Conn



		PROJECT : S400 Series	
		Quanta Computer Inc.	
Size Custom	Document Number <b>24 -- FPR</b>	Rev 1A	
Date: Thursday, May 19, 2016	Sheet 24	of	67

ALF@1119:  
HP confir med to re move the eDP to LVDS convert α.

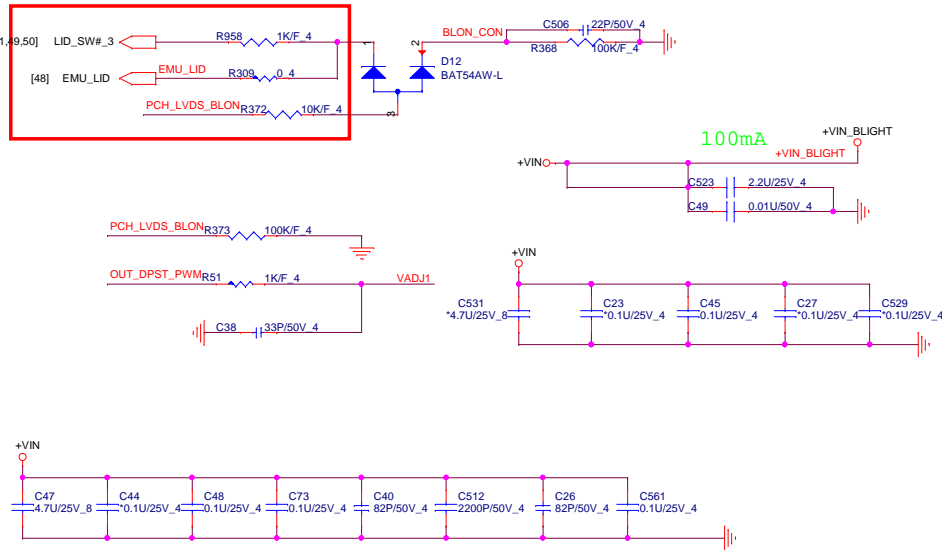
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V



PROJECT : X63

Quanta Computer Inc.

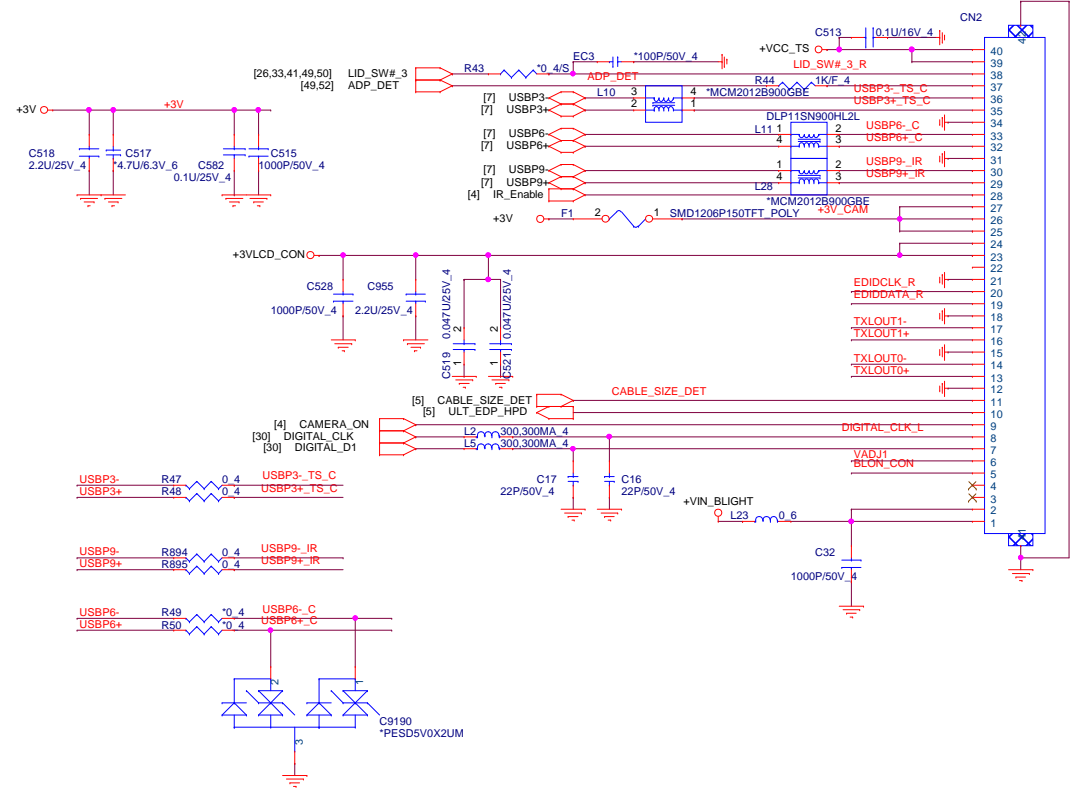
Size	Document	Number	Rev
Custom	25 -- LVDS converter	RTD2136	1A
Date: Thursday, May 19, 2016		Sheet 25 of 67	



LVDS Conn.

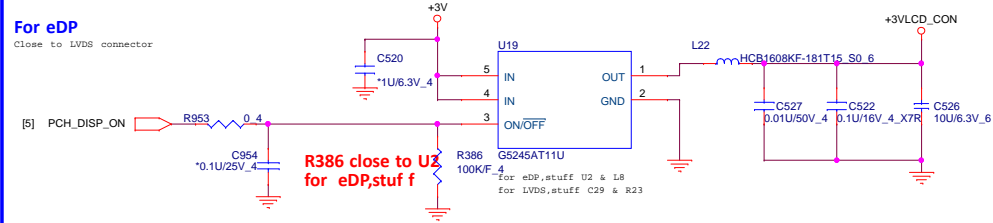
GS12401-1011-9H  
51519-0400-V02-40p-I

DFFC40FR081

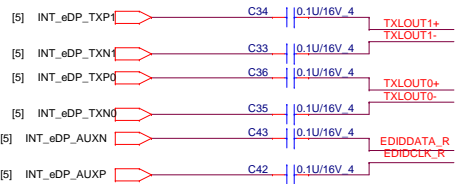


For eDP

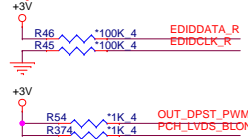
Close to LVDS connector



For EDP Only: stuff Cap  
For LVDS only stuff Resistor



For EDP Only: Reserved

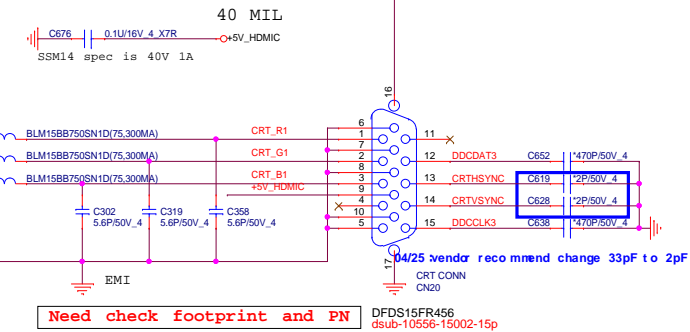
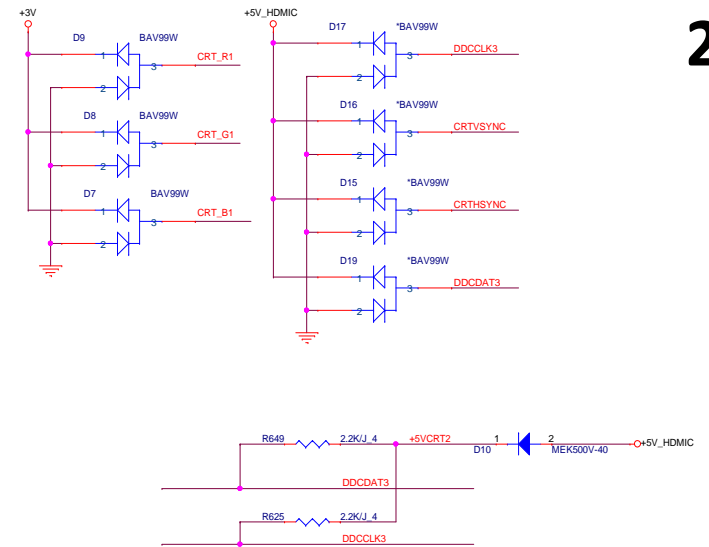


For eDP, close to CN2




PROJECT : X63  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 -- LCD CONN/LID/CAM/D-MIC	1A
Date: Thursday, May 19, 2016	Sheet 26 of 67	

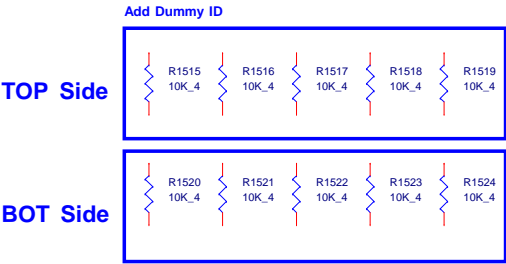


[3,16,17,50] PCH\_SMBDATA R627 0.4 FCH\_3S\_SMDATA


[3,16,17,50] PCH\_SMBCLK R623 0.4 FCH\_3S\_SMCLK

	<b>PROJECT : X63</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number 27 -- DP2VGA_converter	Rev 1A
Date: Thursday, May 19, 2016		Sheet 27 of 67	

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V <sub>DD</sub>	2 dB
short to V <sub>DD</sub>	short to GND	4 dB
short to V <sub>DD</sub>	short to V <sub>DD</sub>	6 dB



OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

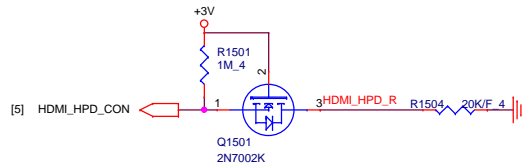
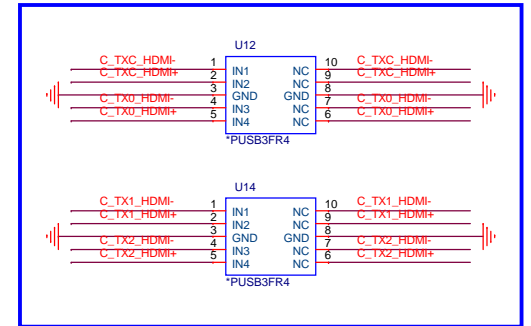
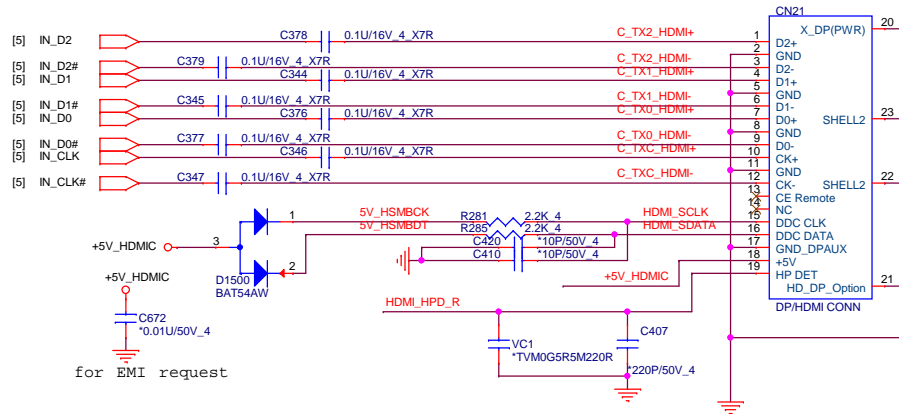
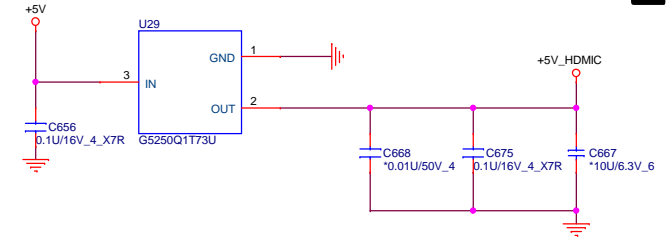
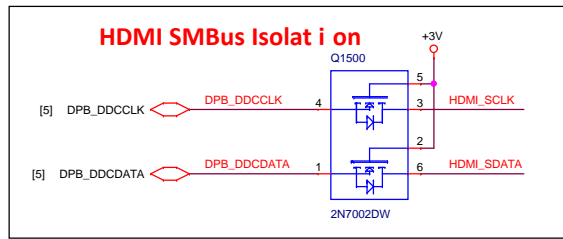


**PROJECT : X63**

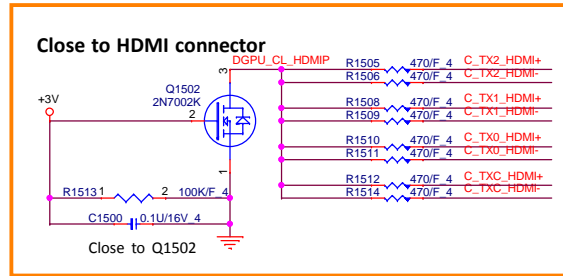
**Quanta Computer Inc.**

Size Custom	Document Number	Rev
	<b>28 – REPEATER PTN3366</b>	<b>1A</b>
Date: Thursday, May 19, 2016		Sheet 28 of 67

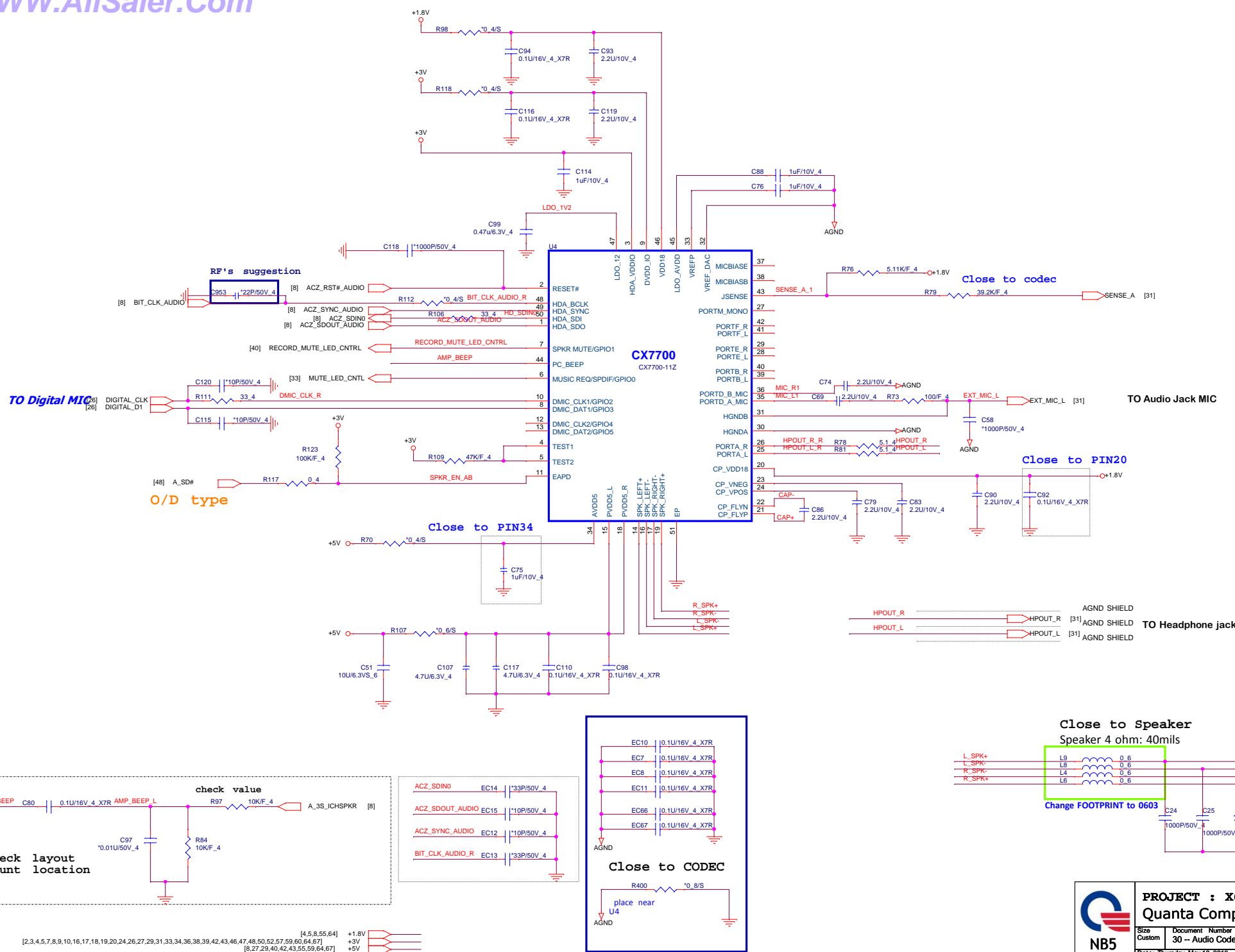
### HDMI SMBus Isolati on

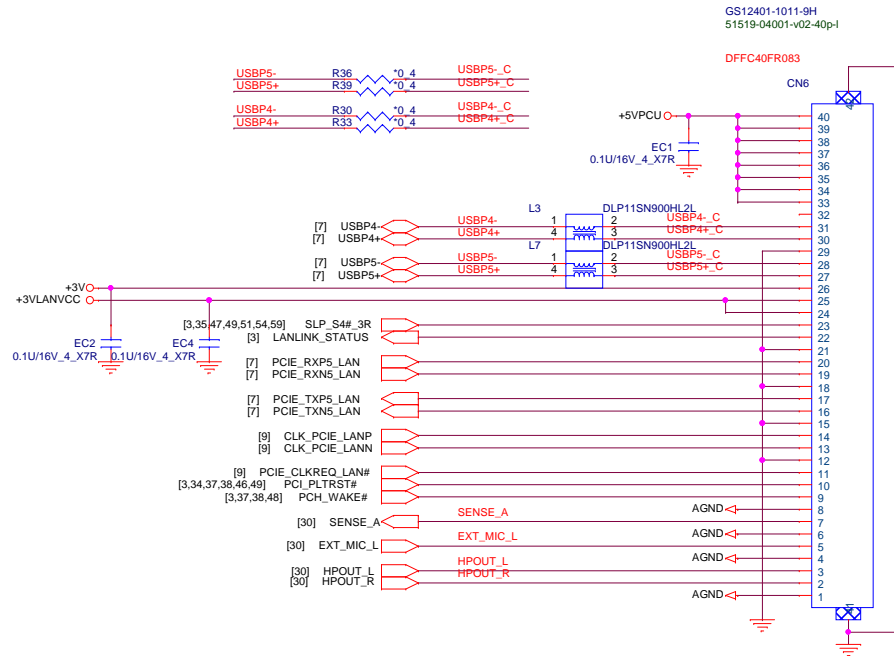



### Close to HDMI connector




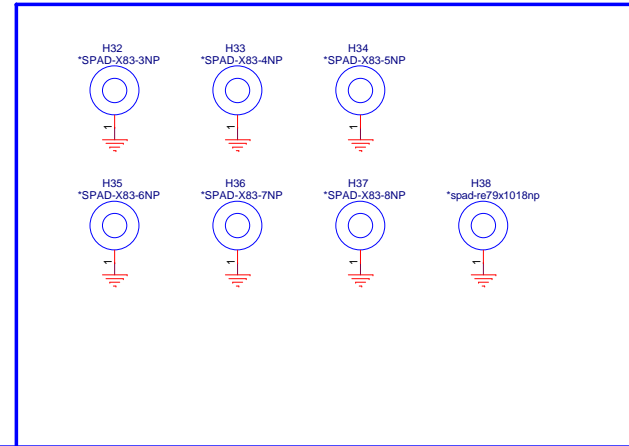
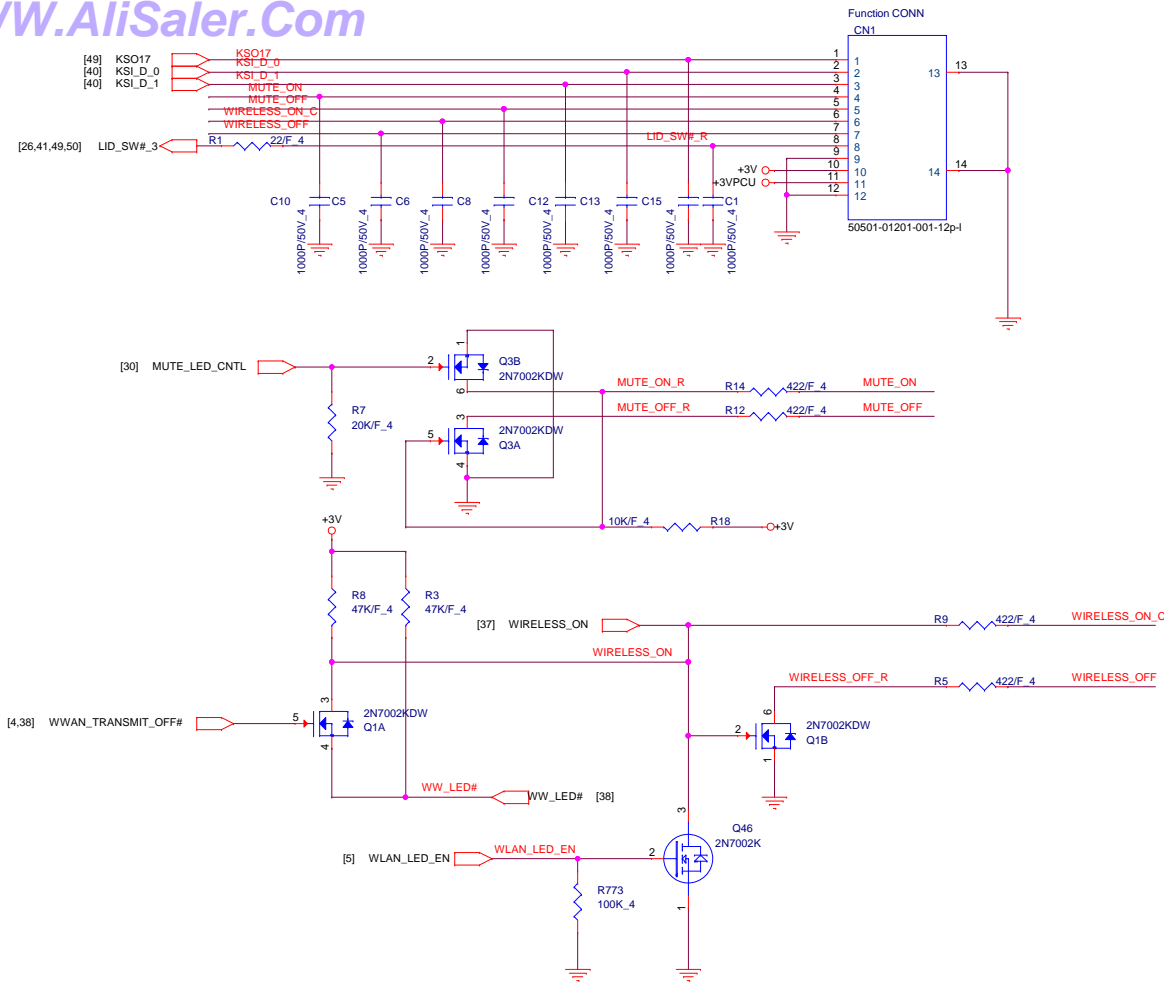




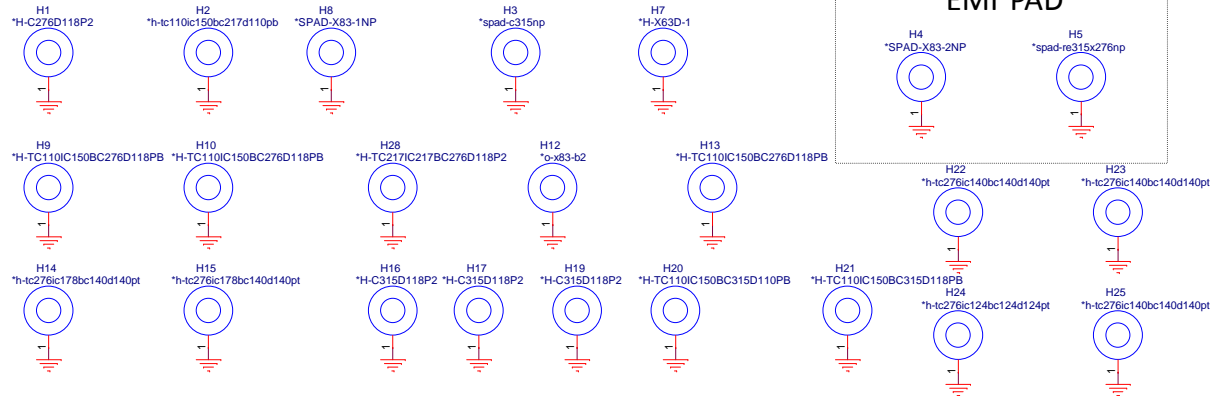


	<b>PROJECT : X63</b>			
	<b>Quanta Computer Inc.</b>			
	Size Custom	Document Number 31 -- DAUGHTER BOARD CONN.		Rev 1A
	Date: Thursday, May 19, 2016		Sheet 31 of 67	

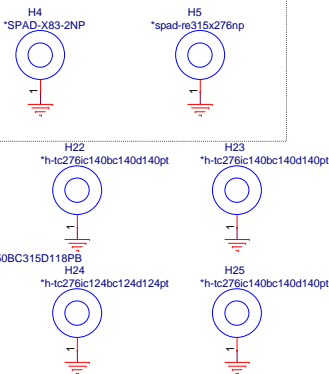
	<b>PROJECT : X63</b>		
	<b>Quanta Computer Inc.</b>		
	Size C	Document Number <b>32 -- Reserved</b>	Rev 1A
Date: Thursday, May 19, 2016		Sheet 32 of 67	



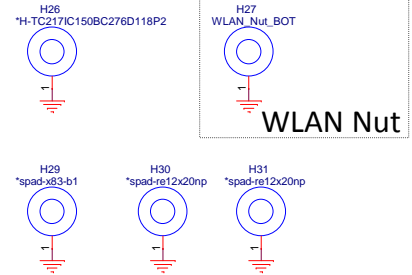
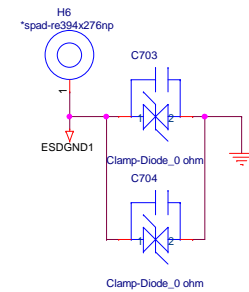
Hole



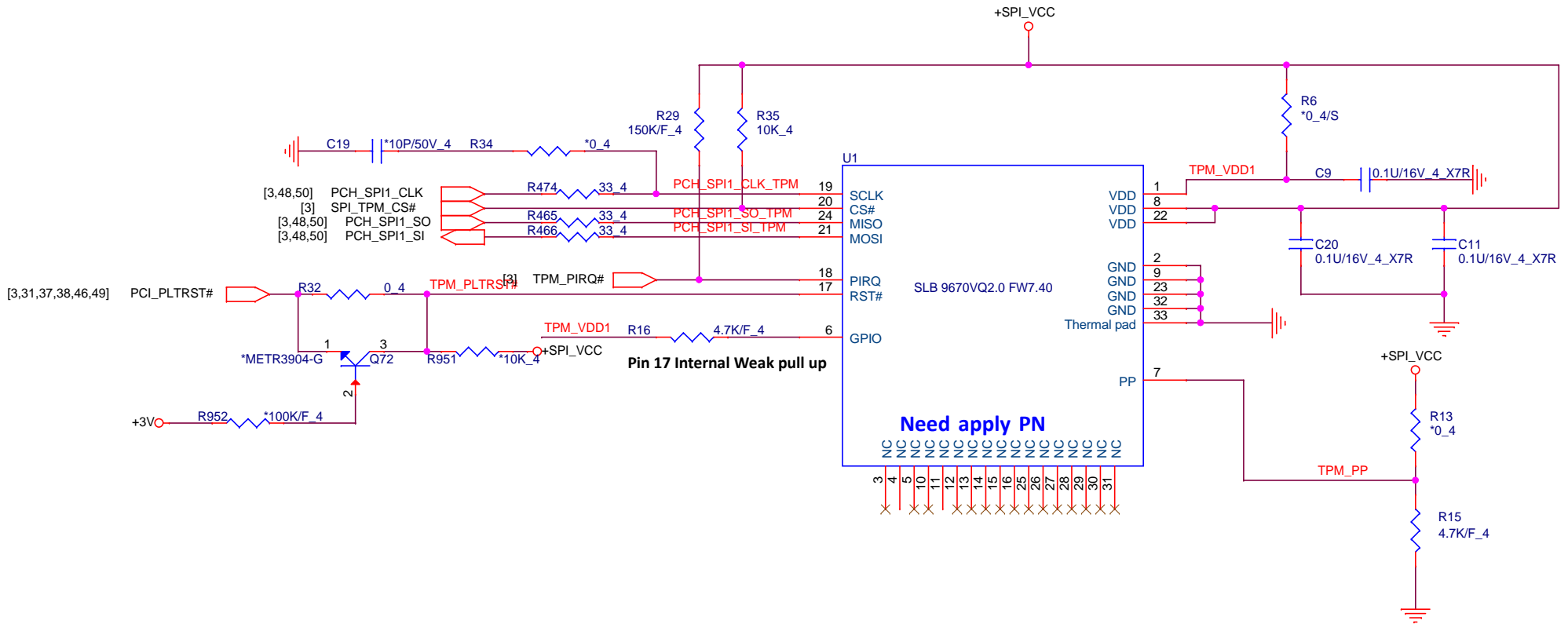
EMI PAD

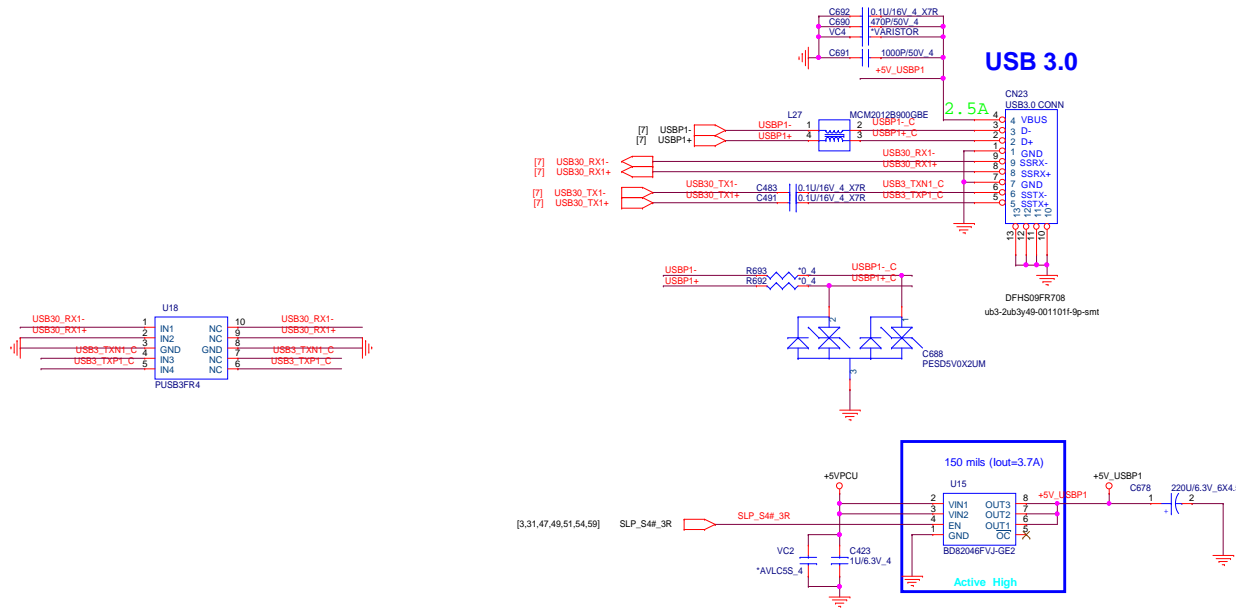


ESD PAD



NB5	<b>PROJECT : X63</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number	Rev 1A
	Date: Thursday, May 19, 2016	33 - Function Conn./Hole	Sheet 33 of 67





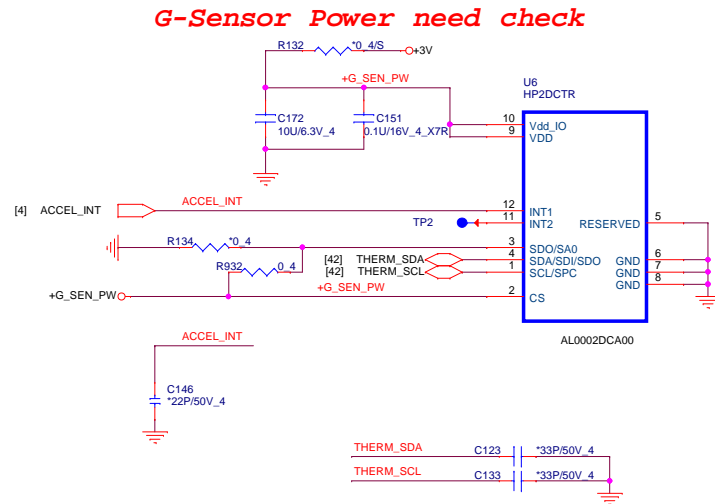
[31,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67]  
[9,41,51,52,53,59,63,64,67]

+5VPCU  
+3V\_ALW




PROJECT : X63  
Quanta Computer Inc.

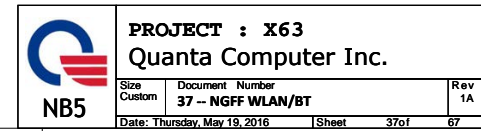
Size Custom	Document Number 35 -- USB3.0 x2	Rev 1A
Date: Thursday, Mar 19, 2016		Sheet 35 of 67

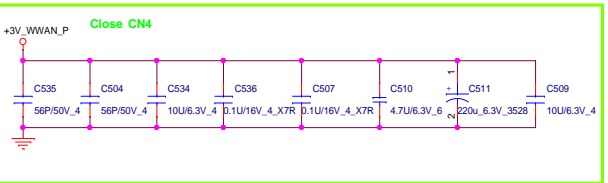


[31,35,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67] +5VPCU  
[9,41,51,52,53,59,63,64,67] +3V\_ALW

	<b>PROJECT : X63</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>36 -- TS and Accelerometer</b>	Rev 1A
Date: Thursday, May 19, 2016		Sheet 36 of 67	





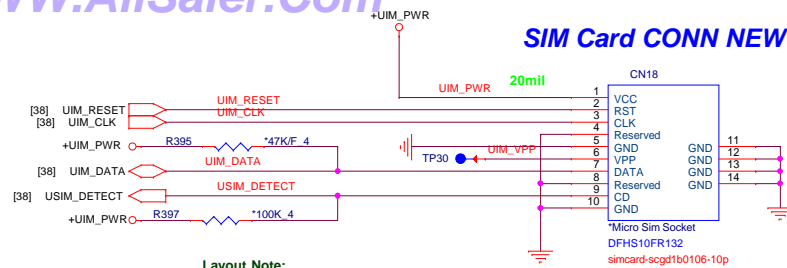


NOT  
Recommend

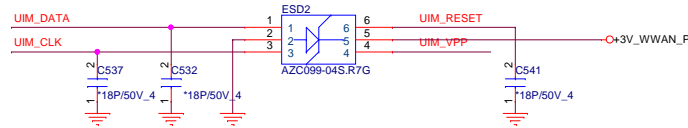
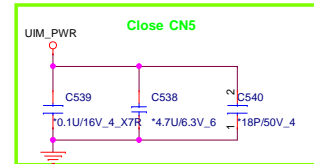
↰	<b>M.2 Pinout</b> ↰	S0↰	S3 – S5↰
WWAN 3.3V↰	2, 4, 70, 72, 74↰	On↰	Off↰

+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low





**Layout Note:**  
 1. UIM\_RESET, UIM\_CLK, UIM\_DATA routing as short as possible  
 Route into ESD then go out  
 2. Avoid routing the SIM\_CLK and SIM\_DATA lines in parallel over distances >= 2 cm  
 3. Position the SIM connector from the WWAN module <= 100mm if possible,  
 NOT exceed length is 150mm.

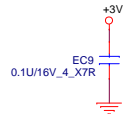


#### Trace Length and Routing<sup>↵</sup>

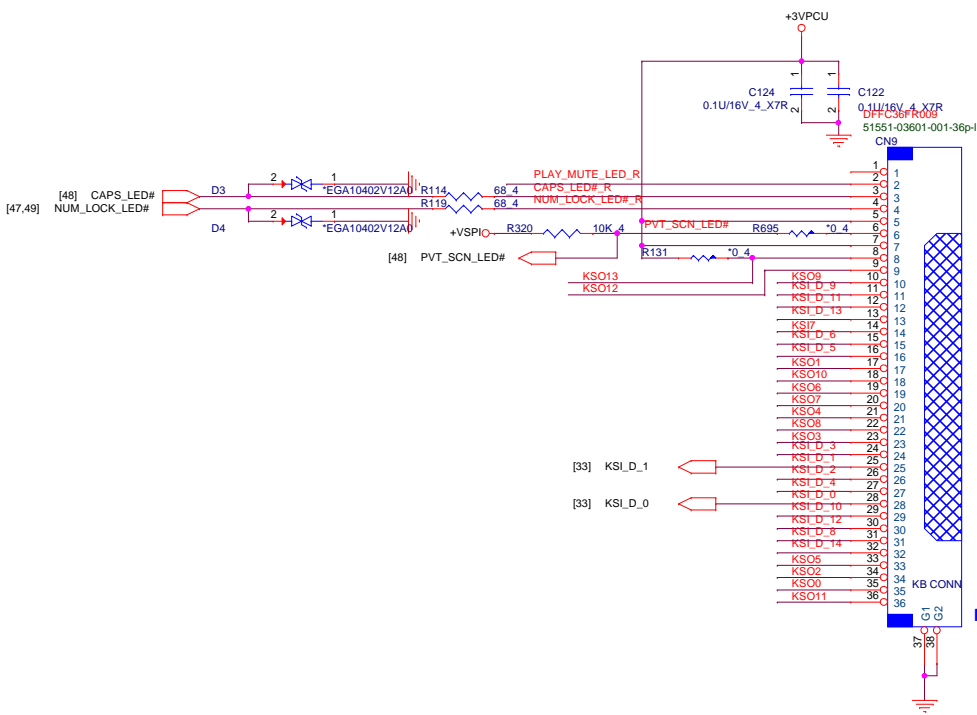
- Special attention should be paid to SIM traces (UIM\_CLK, UIM\_DATA and UIM\_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.<sup>↵</sup>
- Minimum distance between UIM\_CLK and UIM\_DATA should be 20 mils. Static signals such as UIM\_RST can be routed between UIM\_CLK and UIM\_DATA to conserve space if needed.<sup>↵</sup>
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM\_CLK, UIM\_DATA and any other high-speed switching signals.<sup>↵</sup>
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.<sup>↵</sup>

#### SIM Power<sup>↵</sup>

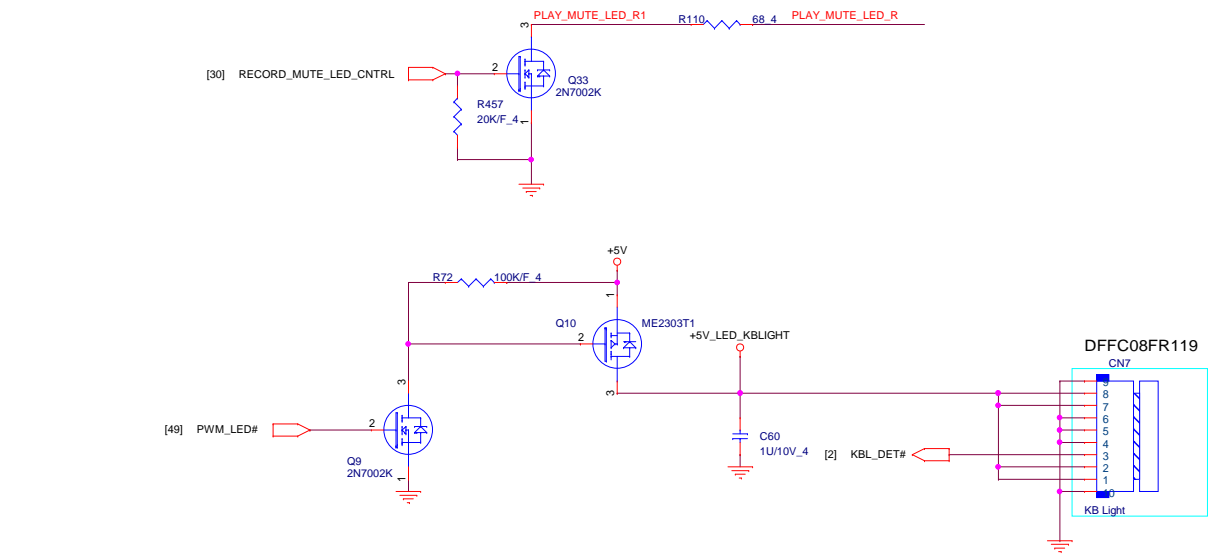
- The UIM\_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.<sup>↵</sup>
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM\_PWR supply and locate near the SIM connector.<sup>↵</sup>



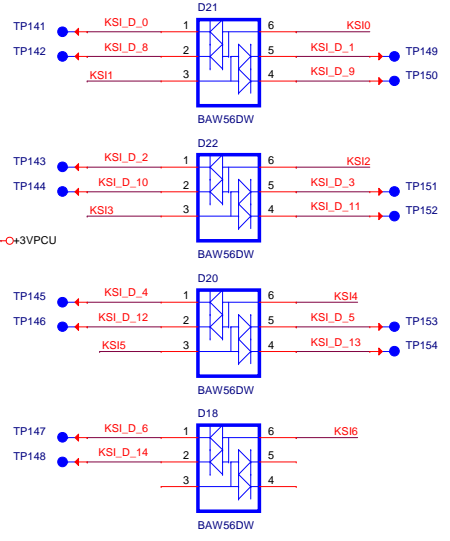
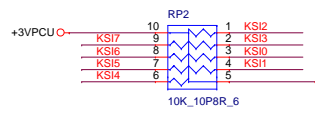
		<b>PROJECT : X63</b>	
		<b>Quanta Computer Inc.</b>	
Size Custom	Document Number 39 -- SIM CARD/ RF cap	Rev 1A	
Date: Thursday, May 19, 2016		Sheet 39 of 67	



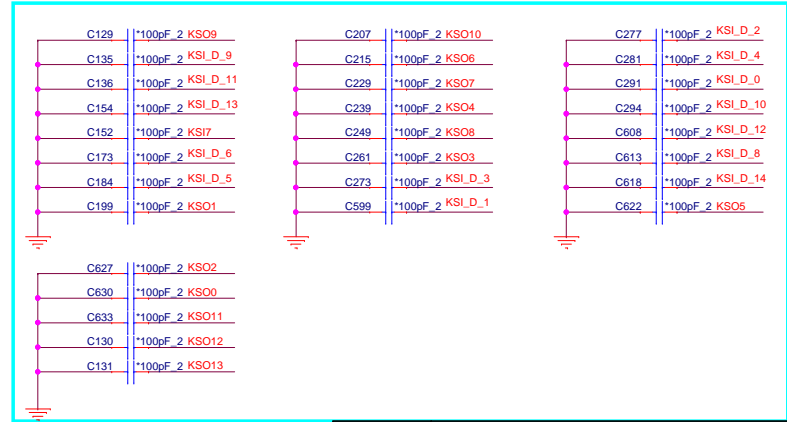
Need apply PN & FOOTPRINT



KEYBOARD PULL-UP



For EMI reserved




[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]  
[8,27,29,30,42,43,55,59,64,67]  
[9,41,51,52,53,59,63,64,67]

3+V

5+V

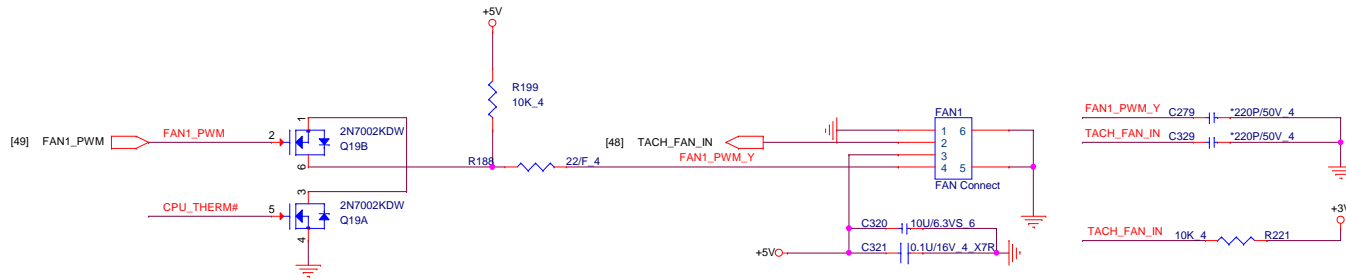
3+V\_ALW



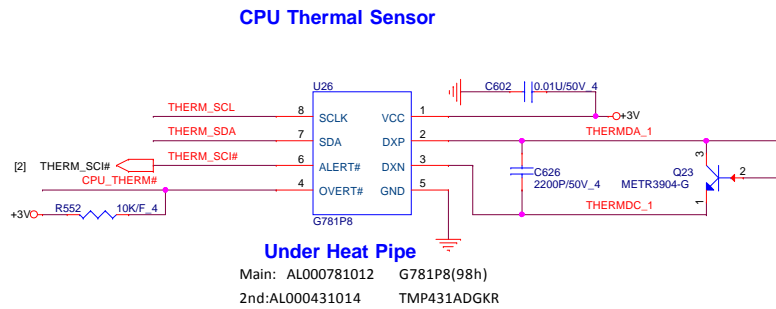
**PROJECT : X63**  
**Quanta Computer Inc.**

Size	Document	Number	Rev
Custom	40 -- KB/ KB light CONN		1A
Date: Thursday, May 19, 2016		Sheet 40 of 67	



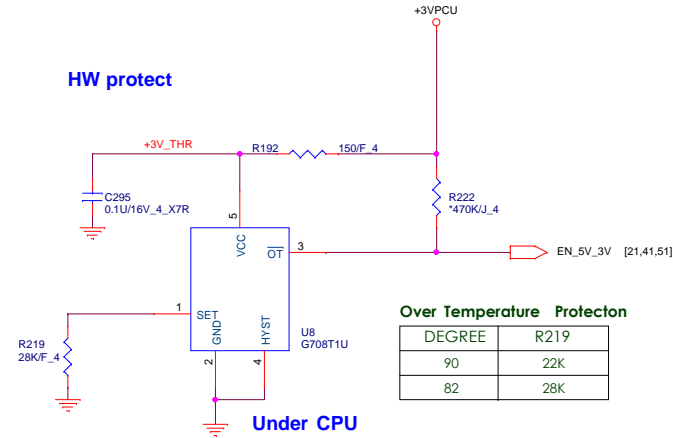


## Thermal sensor



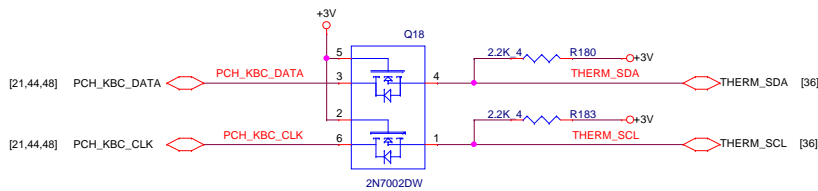
**Under Heat Pipe**  
Main: AL000781012 G781P8(98h)  
2nd:AL000431014 TMP431ADGKR

## HW protect



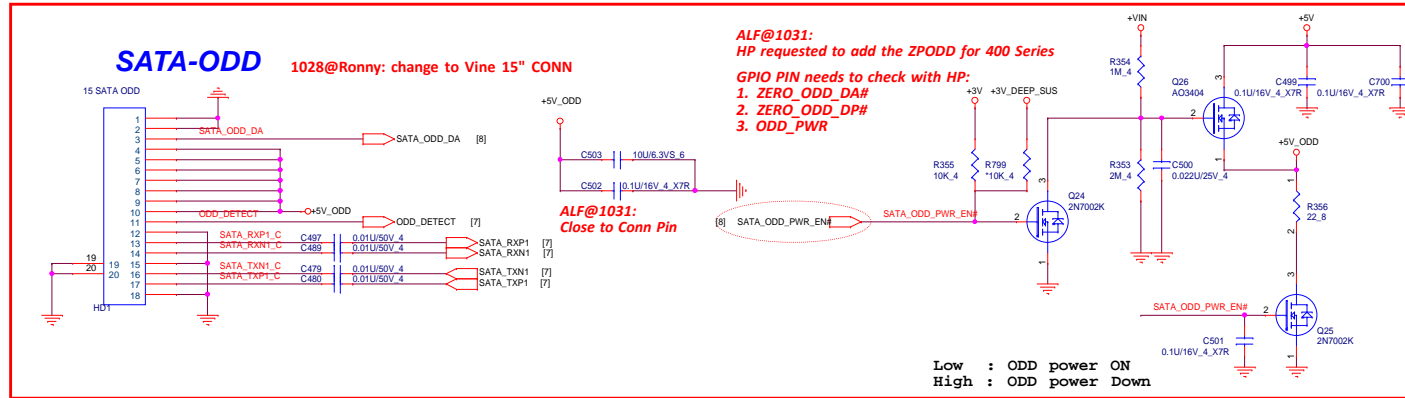
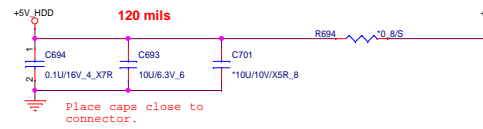
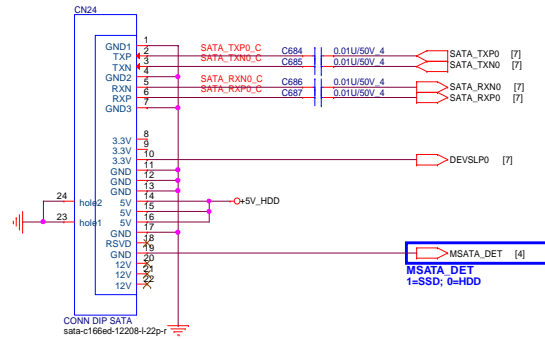
Over Temperature Protection	
DEGREE	R219
90	22K
82	28K

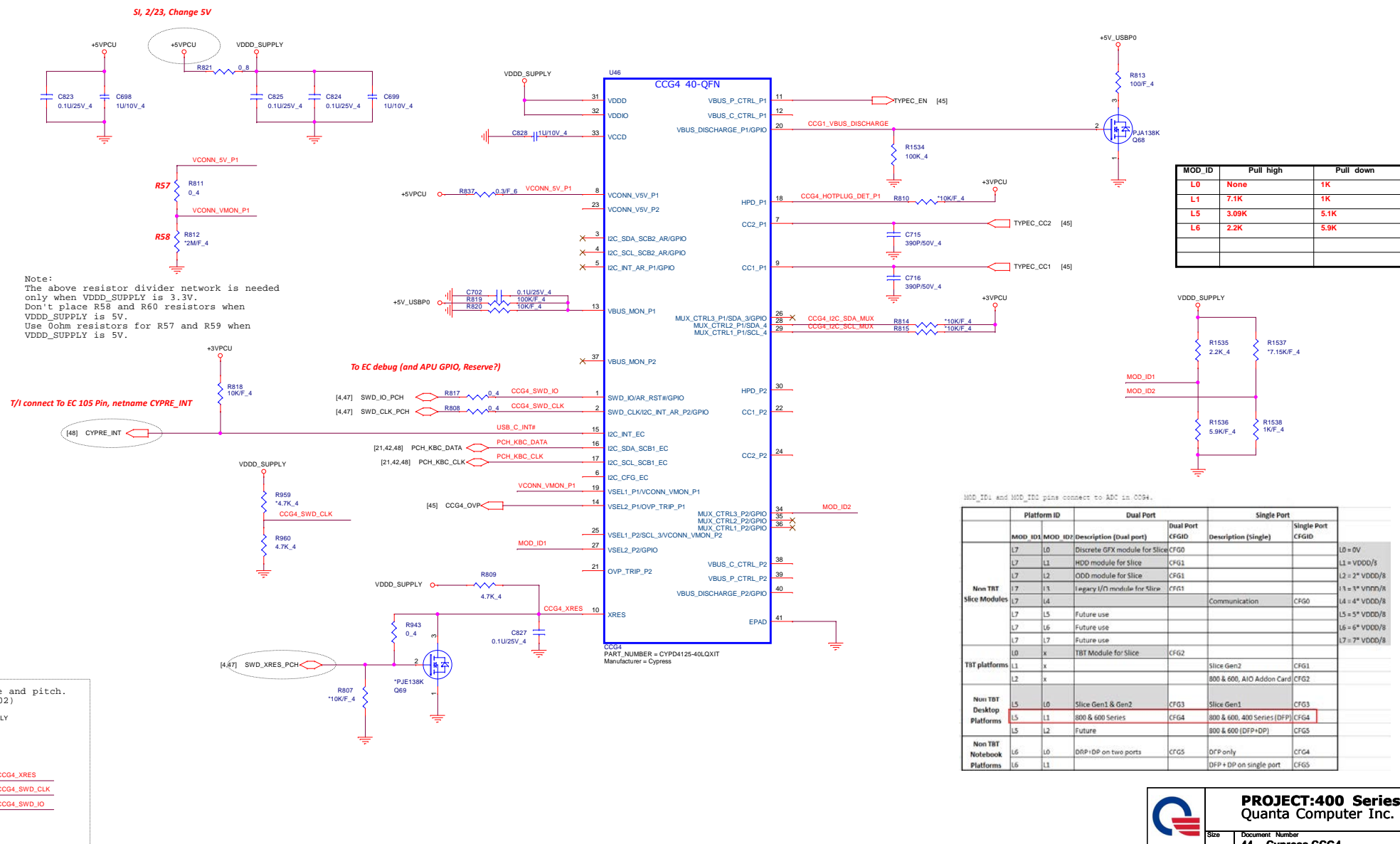
$$RSET \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,43,46,47,48,50,52,57,59,60,64,67]  
[9,41,51,52,53,59,63,64,67] +3V\_ALW

	<b>PROJECT : X63</b>		
	<b>Quanta Computer Inc.</b>		
	Size Custom	Document Number 42-- FAN and Thermal IC	Rev 1A
Date: Thursday, May 19, 2016		Sheet 42 of 67	



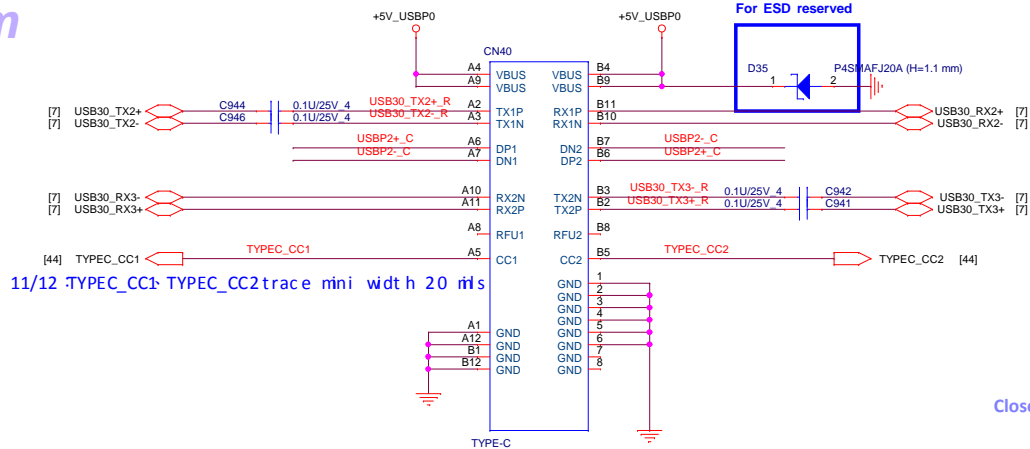


**PROJECT:400 Series**  
**Quanta Computer Inc.**

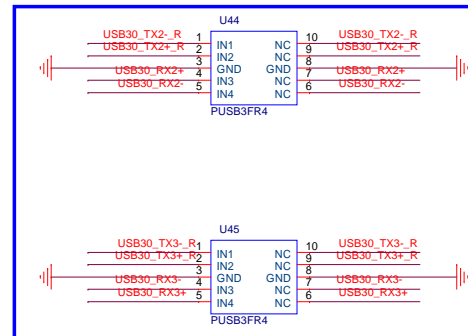
Size: Document Number  
**44 - Cypress CCG4**

Date: Thursday, May 19, 2016 Sheet 44 of 67

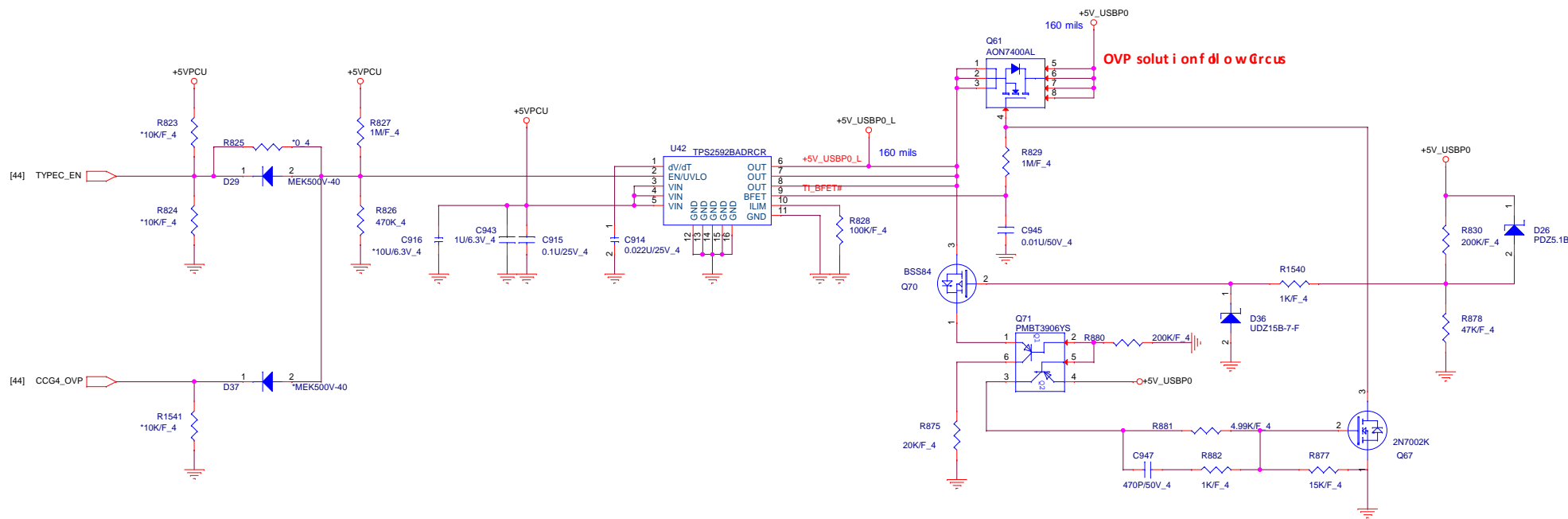
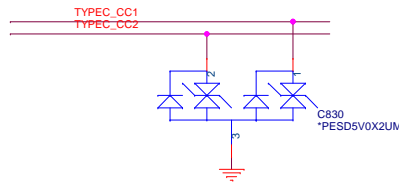
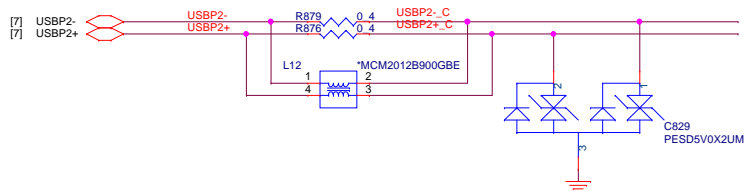
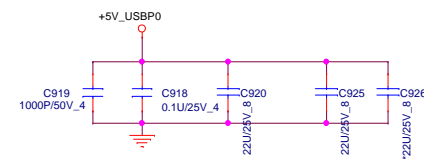


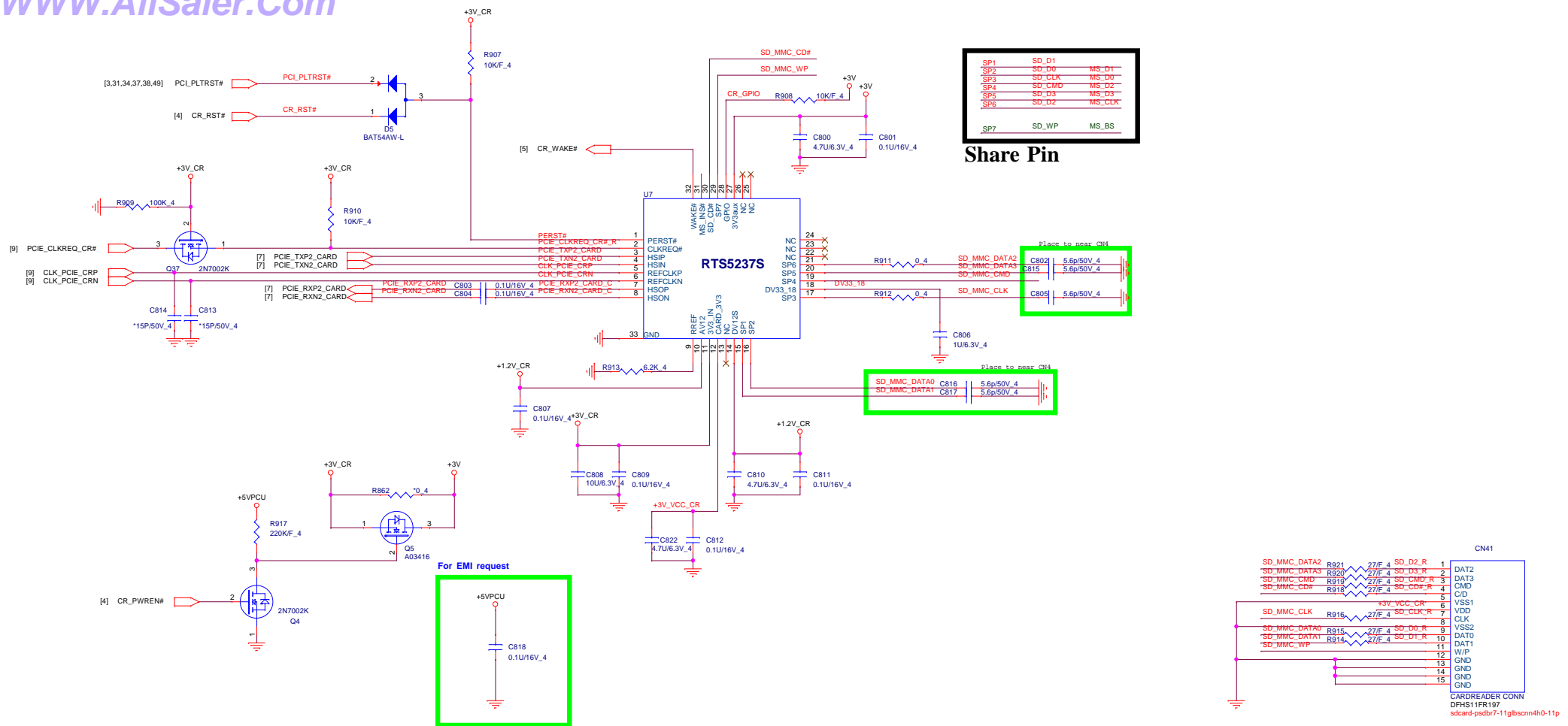


Reserve ESD chip



Close CN40

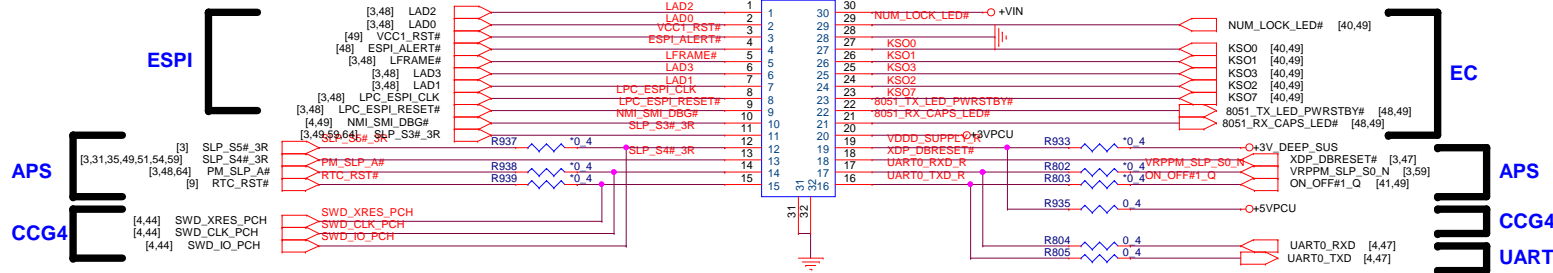




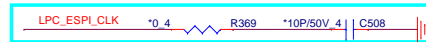
# ESPI+EC+APS debug conn on MB

debug\_CONN\_30P

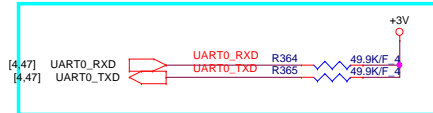
CN14




For EMI reserved

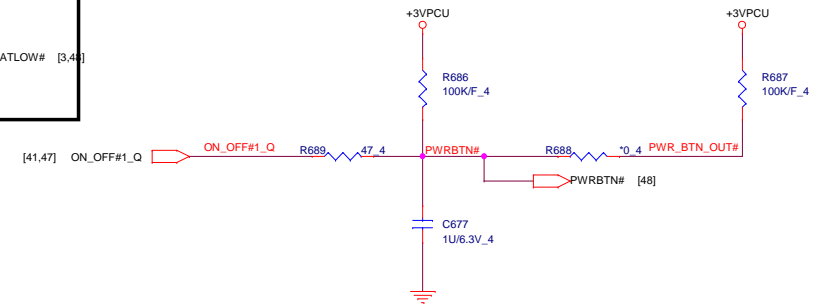
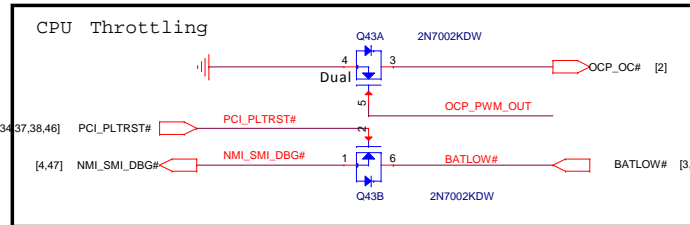


For check list



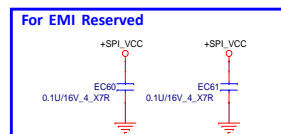
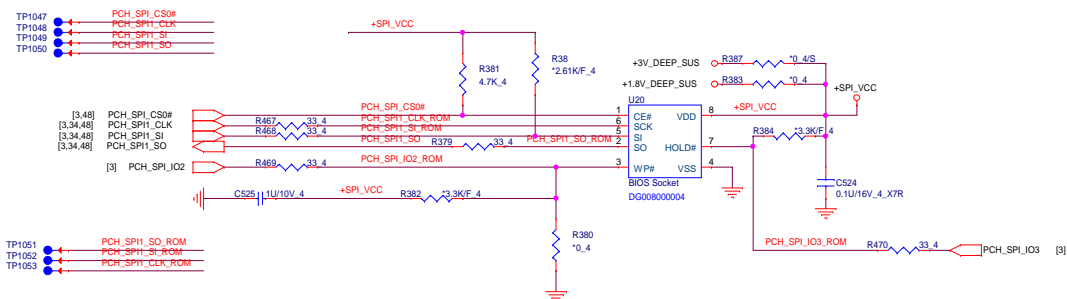
	PROJECT : X63		
	Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	44 - EC & eSPI/UART debug conn	1A
Date: Thursday, May 19, 2016		Sheet 47 of 67	



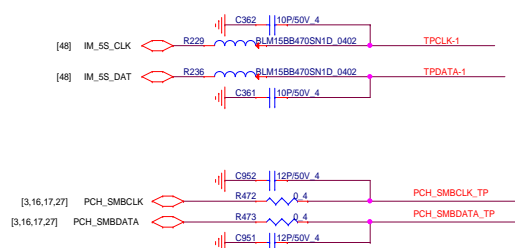


Vender	Size	P/N
Winbond	8MB	AKE3EFPKN01
Winbond	16MB	AKE3DZN0N01 SI : 02/ 02
Socket		DFHS08FS046

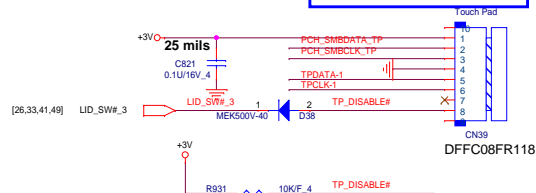
PCH 6\*5mm WSON 16M  
SPI ROM Socket



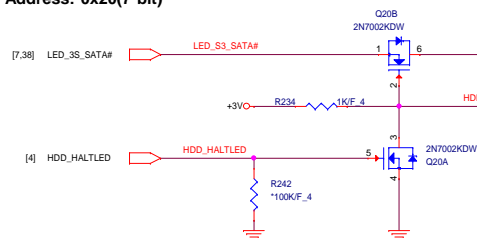
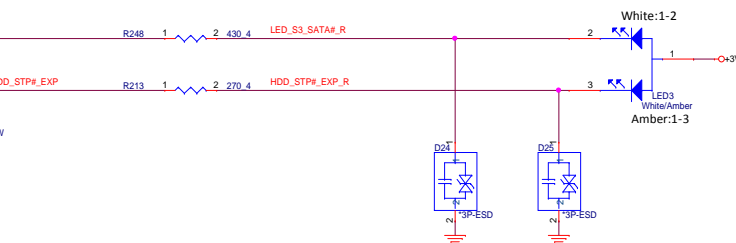
### Touch pad

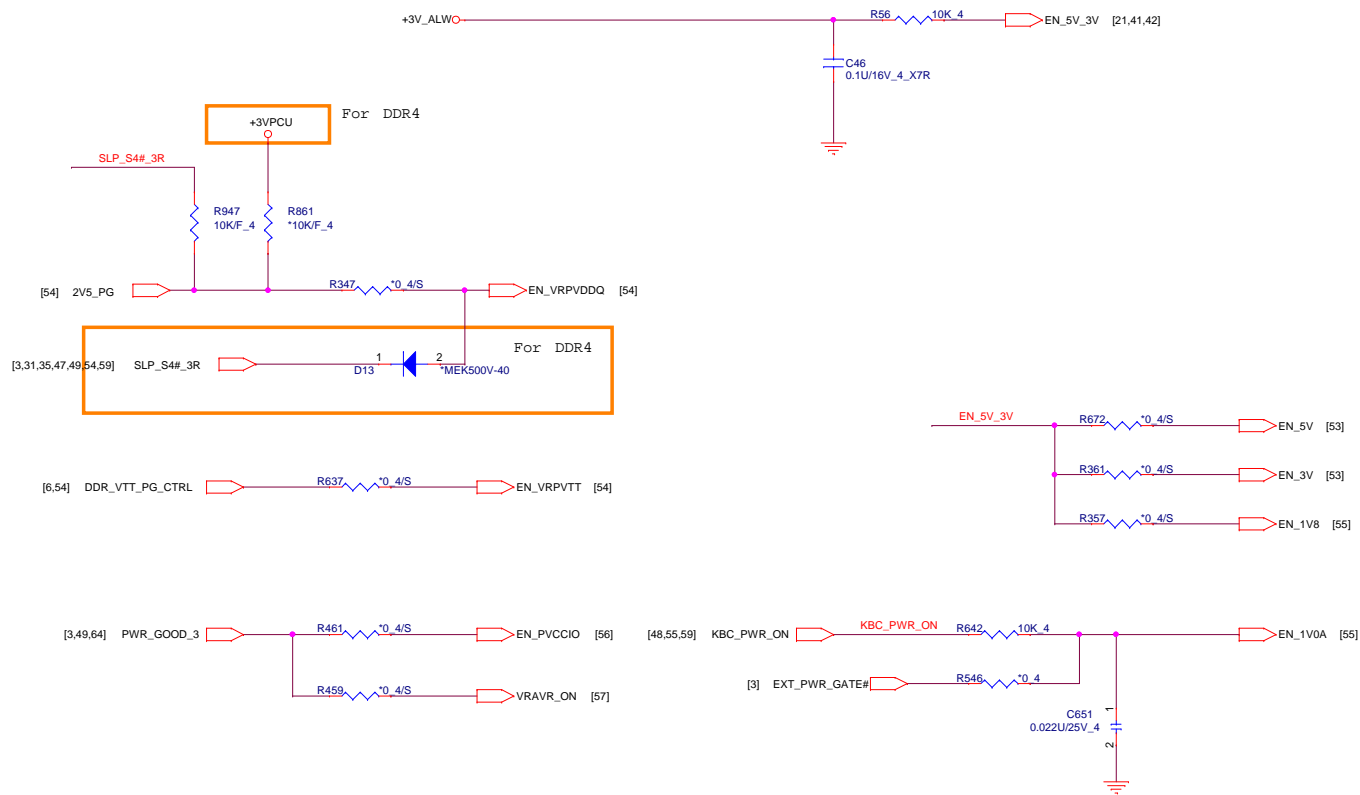


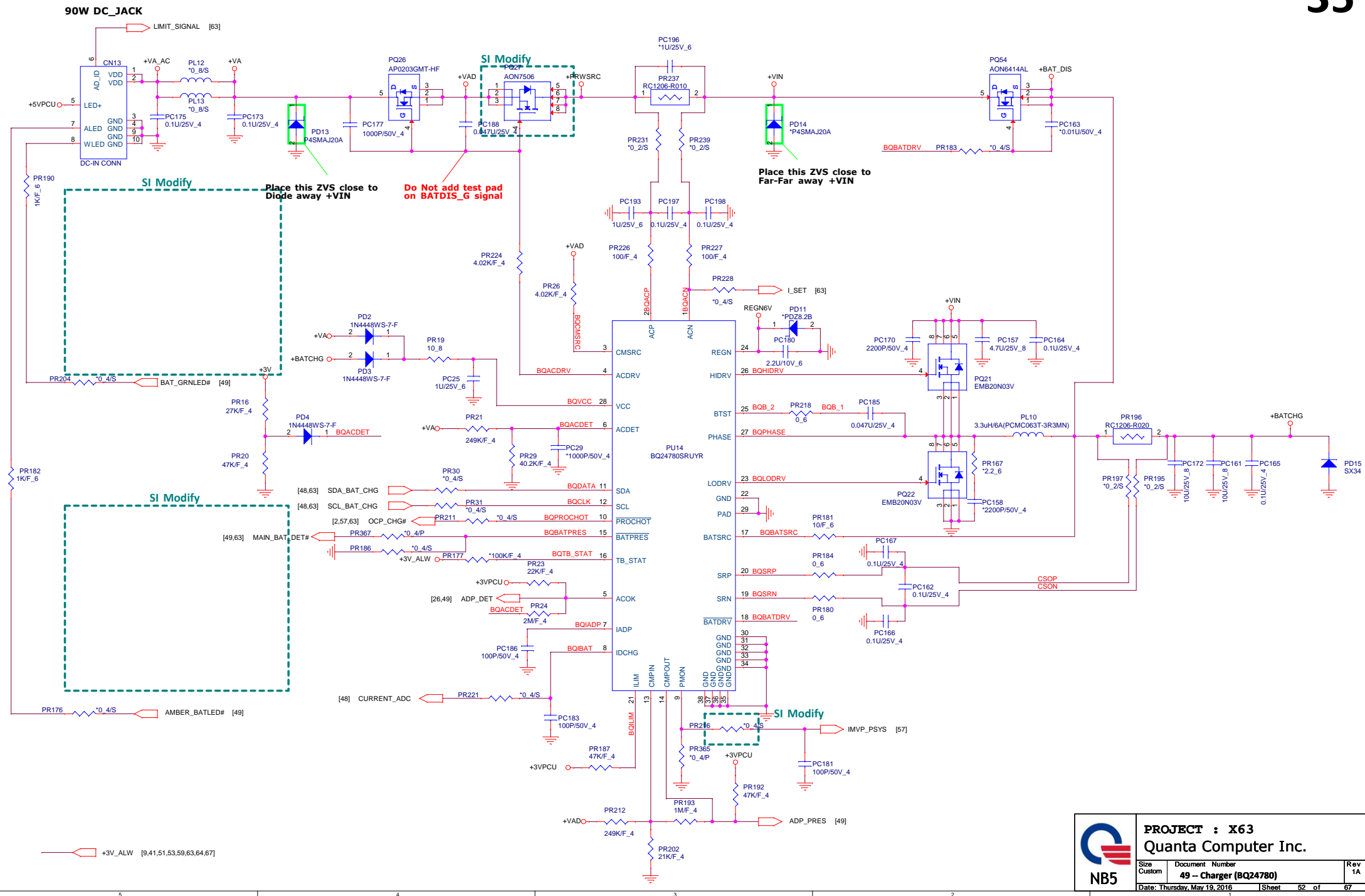
### Forced Pad Connector



**CLICK PAD**  
Address: 0x20(7 bit)

**HDD LED**



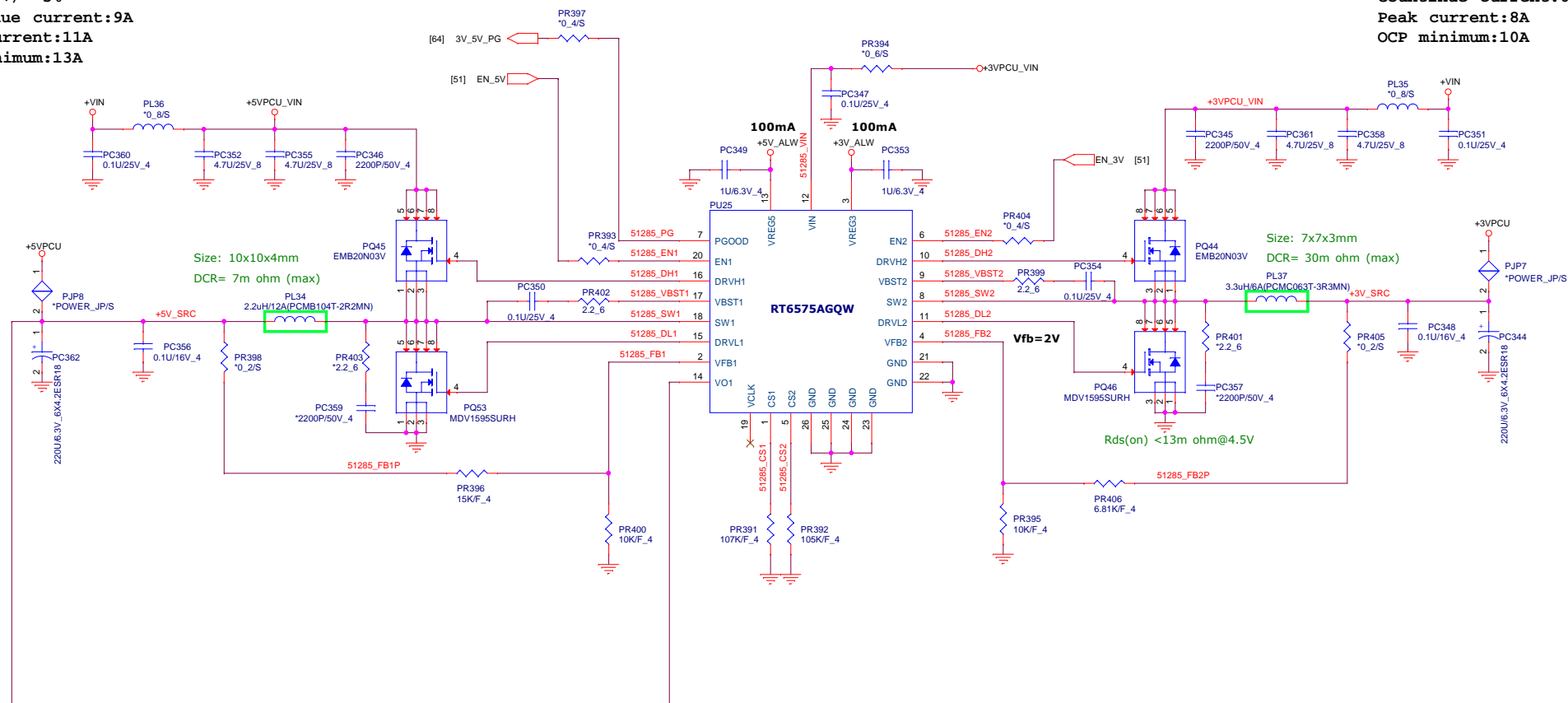




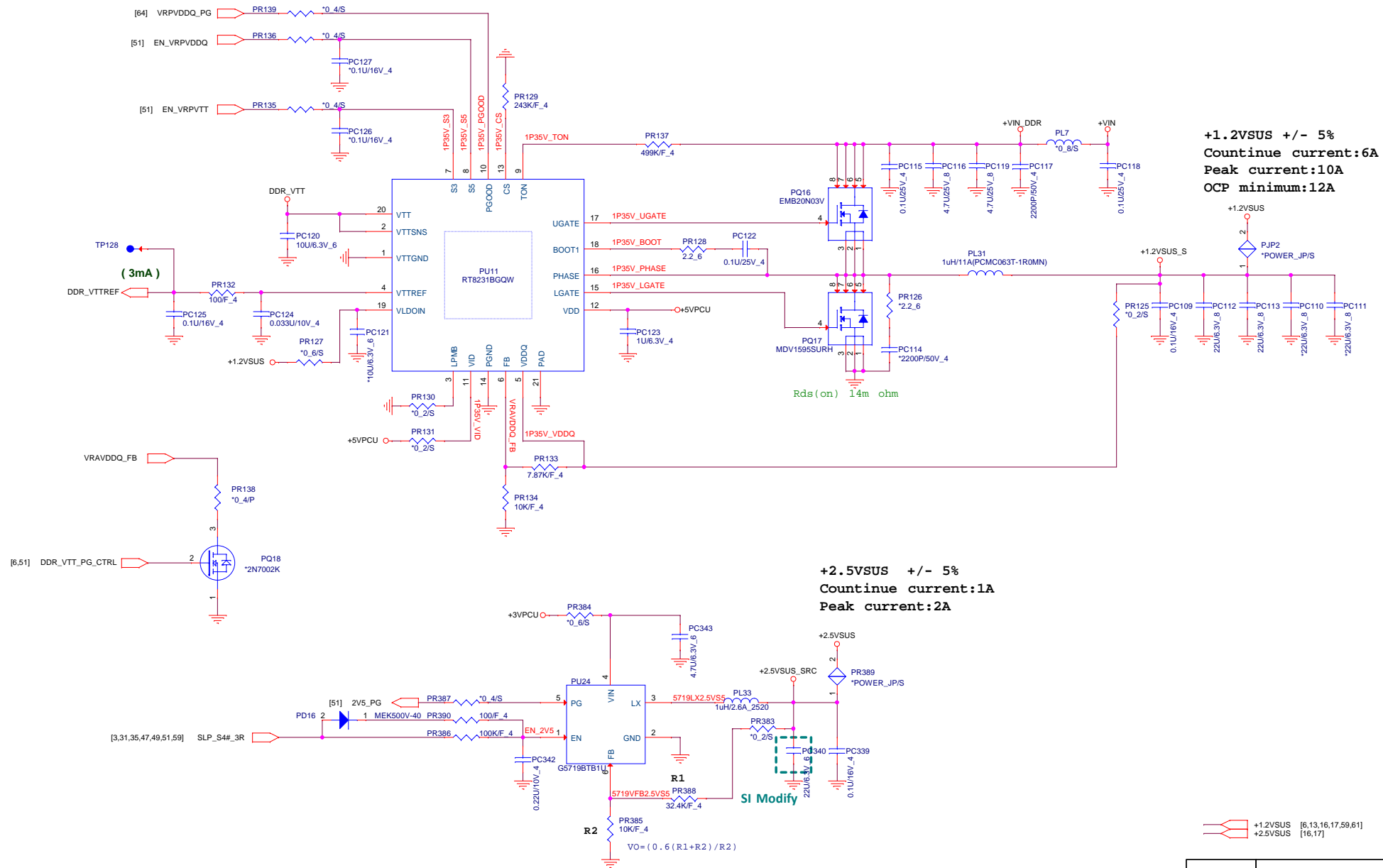
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,54,56,59,61,63,64,67]  
+5VPCU [31,35,44,45,46,47,52,54,55,57,58,59,60,61,62,64,67]


+5VPCU +/- 5%  
Countinue current:9A  
Peak current:11A  
OCP minimum:13A

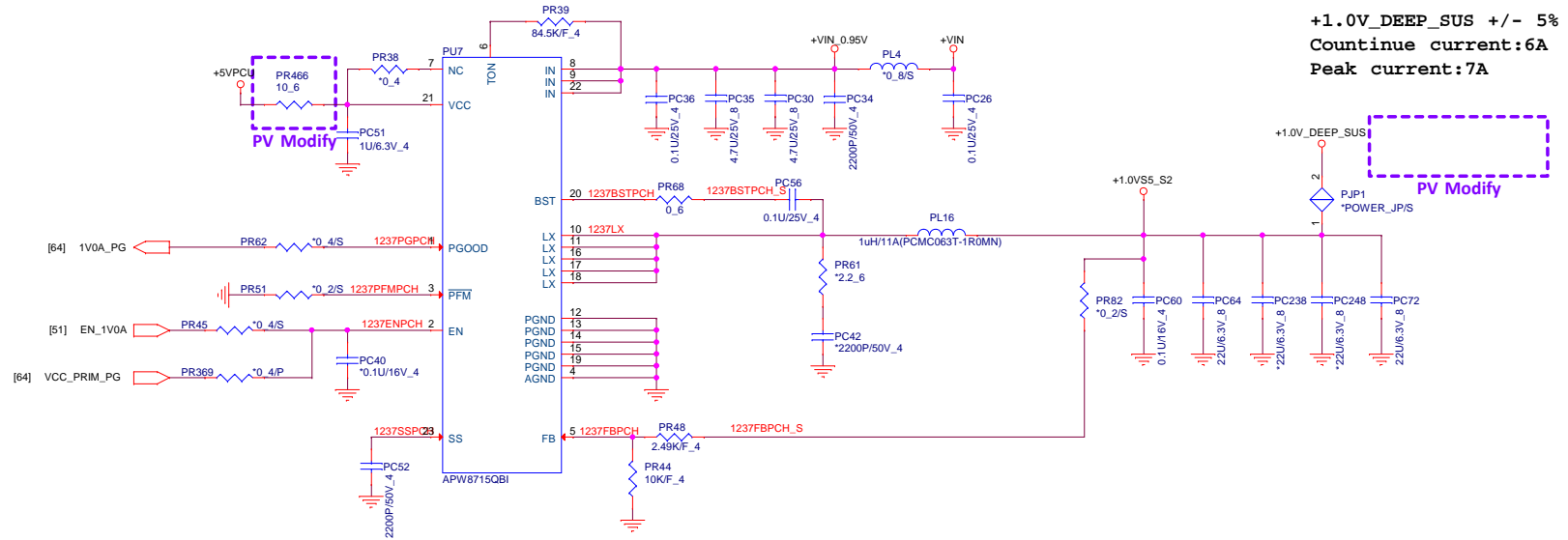
+3VPCU +/- 5%  
Countinue current:6A  
Peak current:8A  
OCP minimum:10A



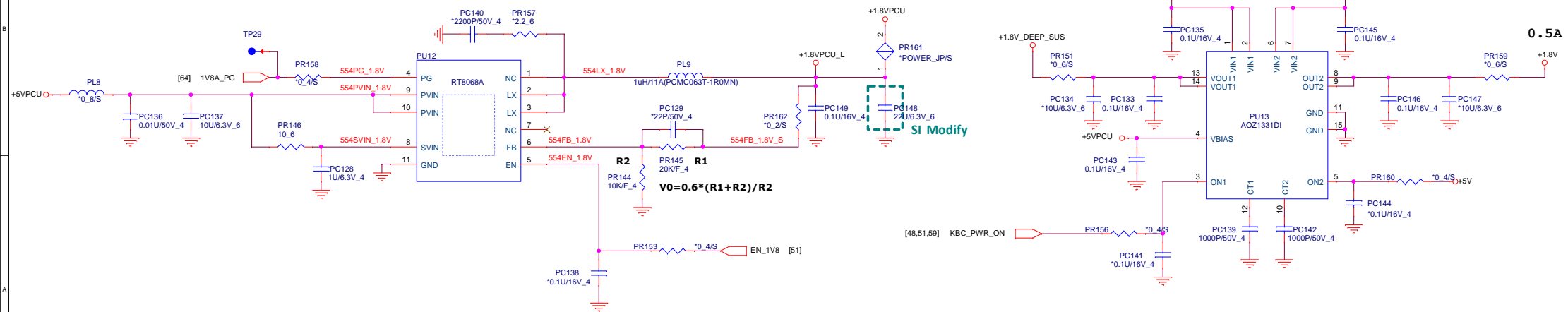
NB5	PROJECT : X63		
	Quanta Computer Inc.		
Size	Document Number	Rev	
	50 - 3/5VS5 (SY8208B/SY8208C)	1A	
Date:	Thursday, May 19, 2016	Sheet	53 of 67




		<b>PROJECT : X63</b>	
		<b>Quanta Computer Inc.</b>	
Size	Document Number	Rev	
	51 - DDR4 (RT8231B)	1A	
Date:	Thursday, May 19, 2016	Sheet	54 of 67



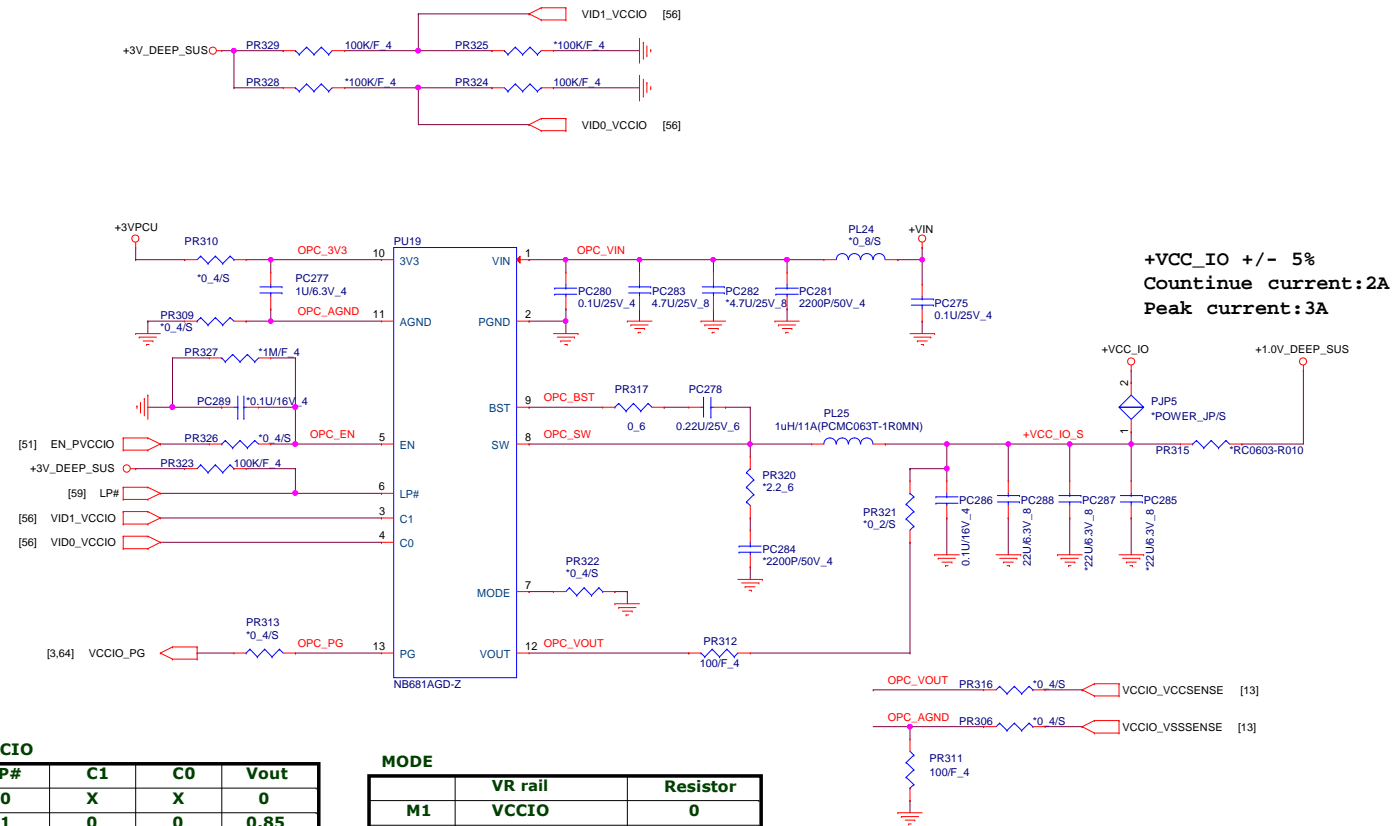
**+1.8VPCU +/- 5%**  
**Countinue current:2A**  
**Peak current:4A**



+VIN [26,43,47,52,53,54,56,57,58,59,60,62,67]  
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]  
+5VPCU [31,35,44,45,46,47,52,53,54,57,58,59,60,61,62,64,67]

		<b>PROJECT : X63</b>	
		<b>Quanta Computer Inc.</b>	
Size	Document Number	Rev	
	52 -- +1.0V5/1.8V5	1A	
Date:	Thursday, May 19, 2016	Sheet	55 of 67

[26,43,47,52,53,54,55,57,58,59,60,62,67] +VIN  
[9,41,51,52,53,59,63,64,67] +3V\_ALW  
[5,13] +VCC\_IO

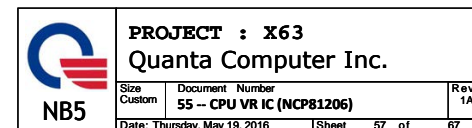


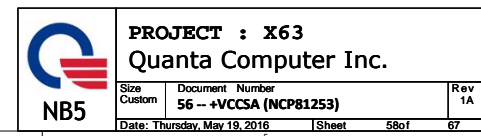
**VCCIO**

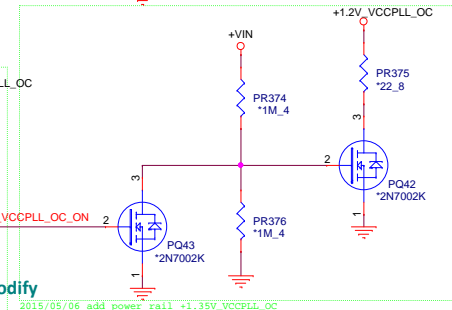
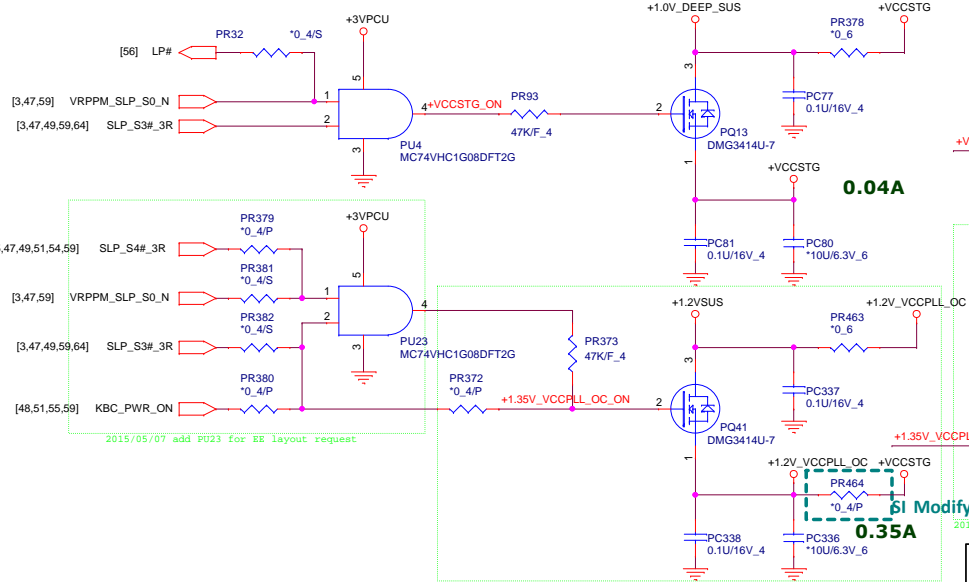
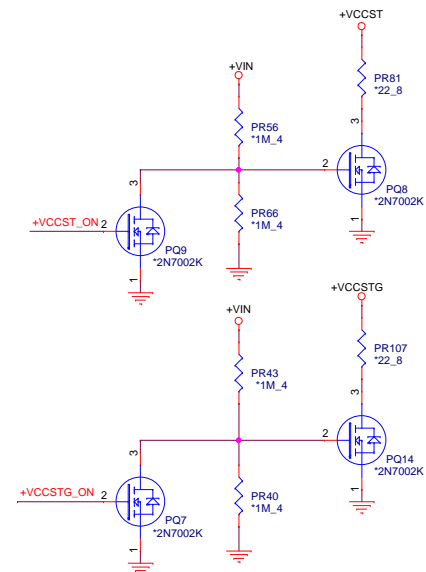
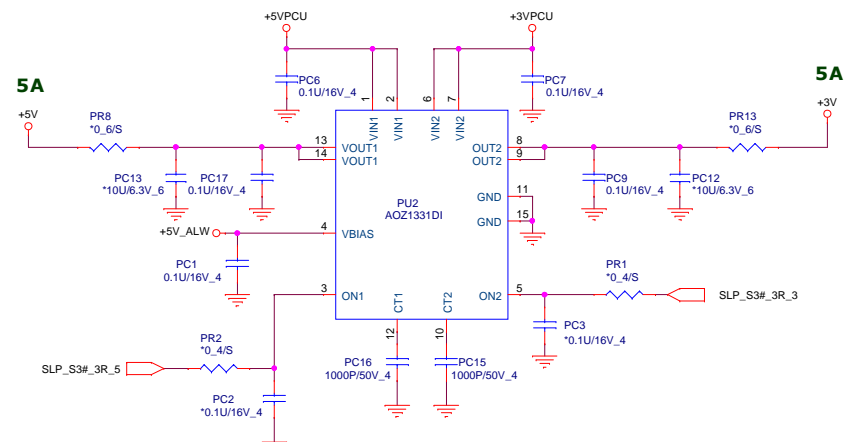
LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975


**MODE**

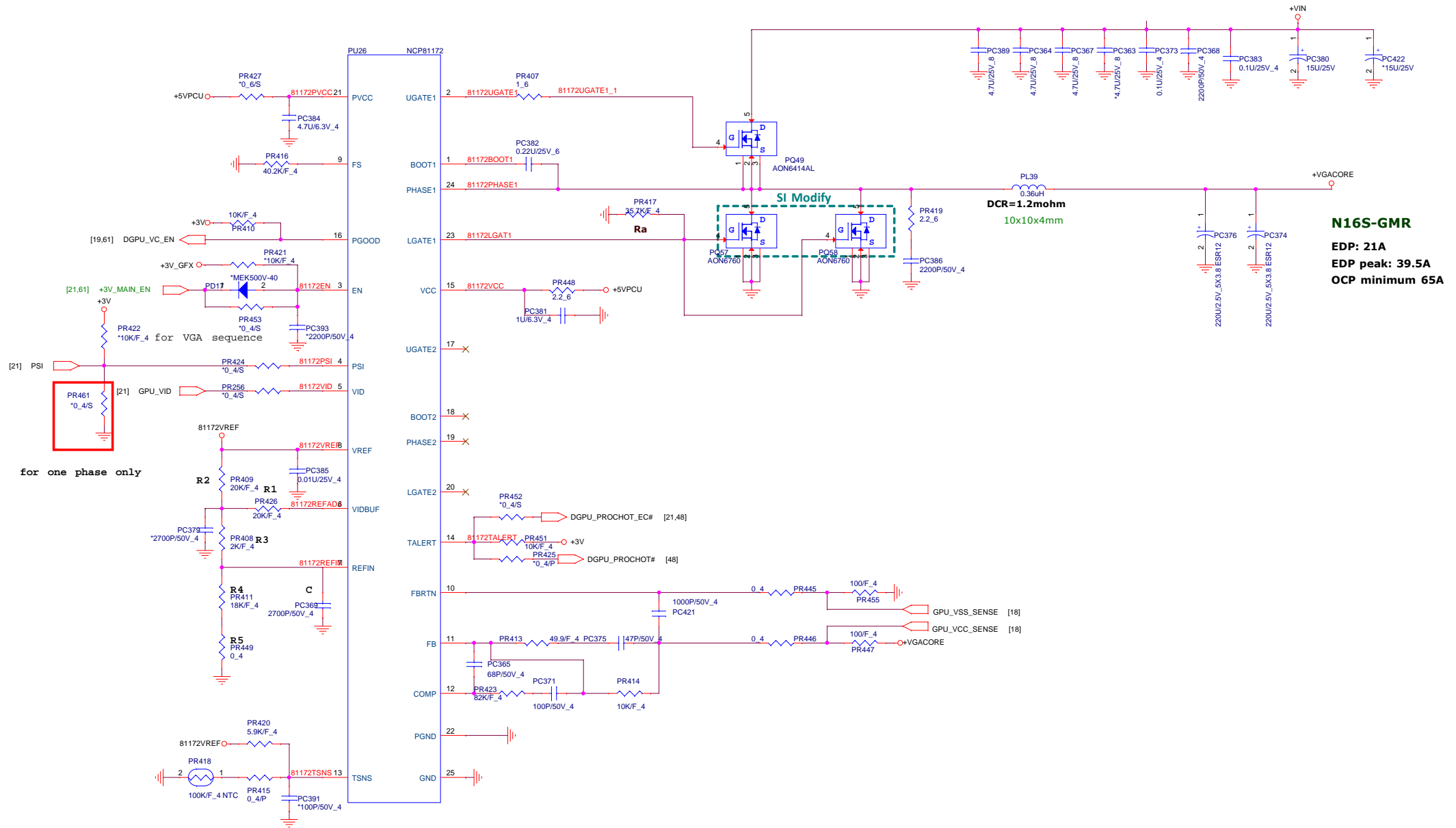
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EPIO	100K
M4	other	150K





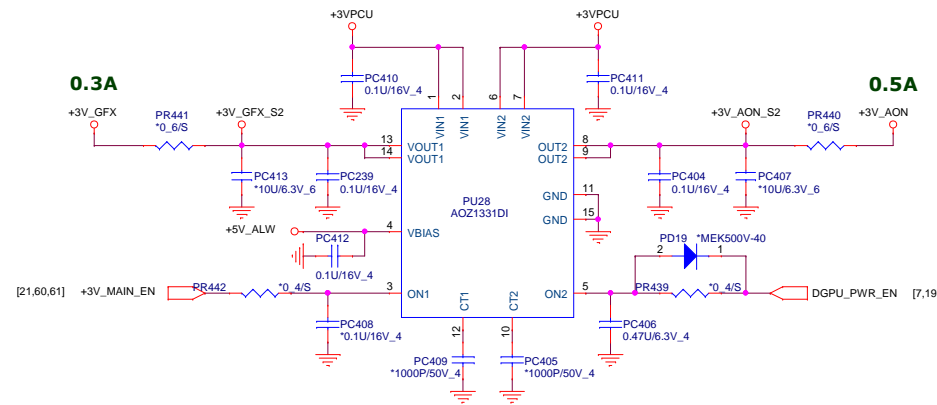
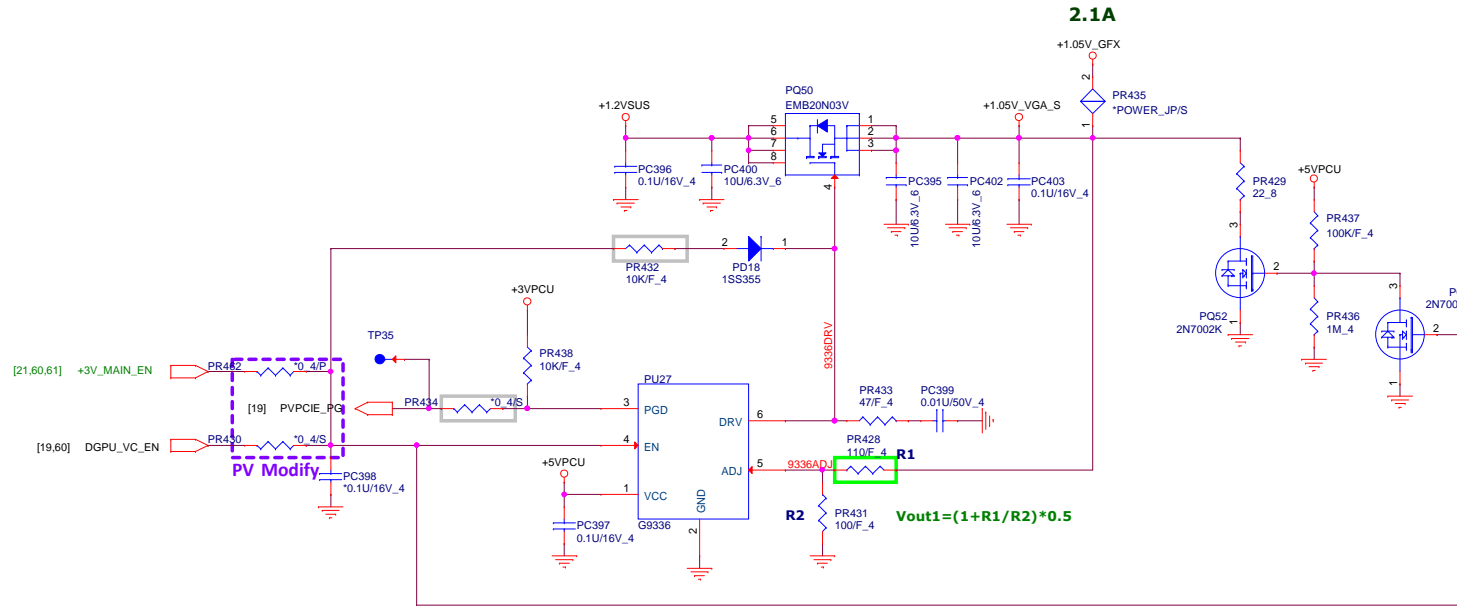


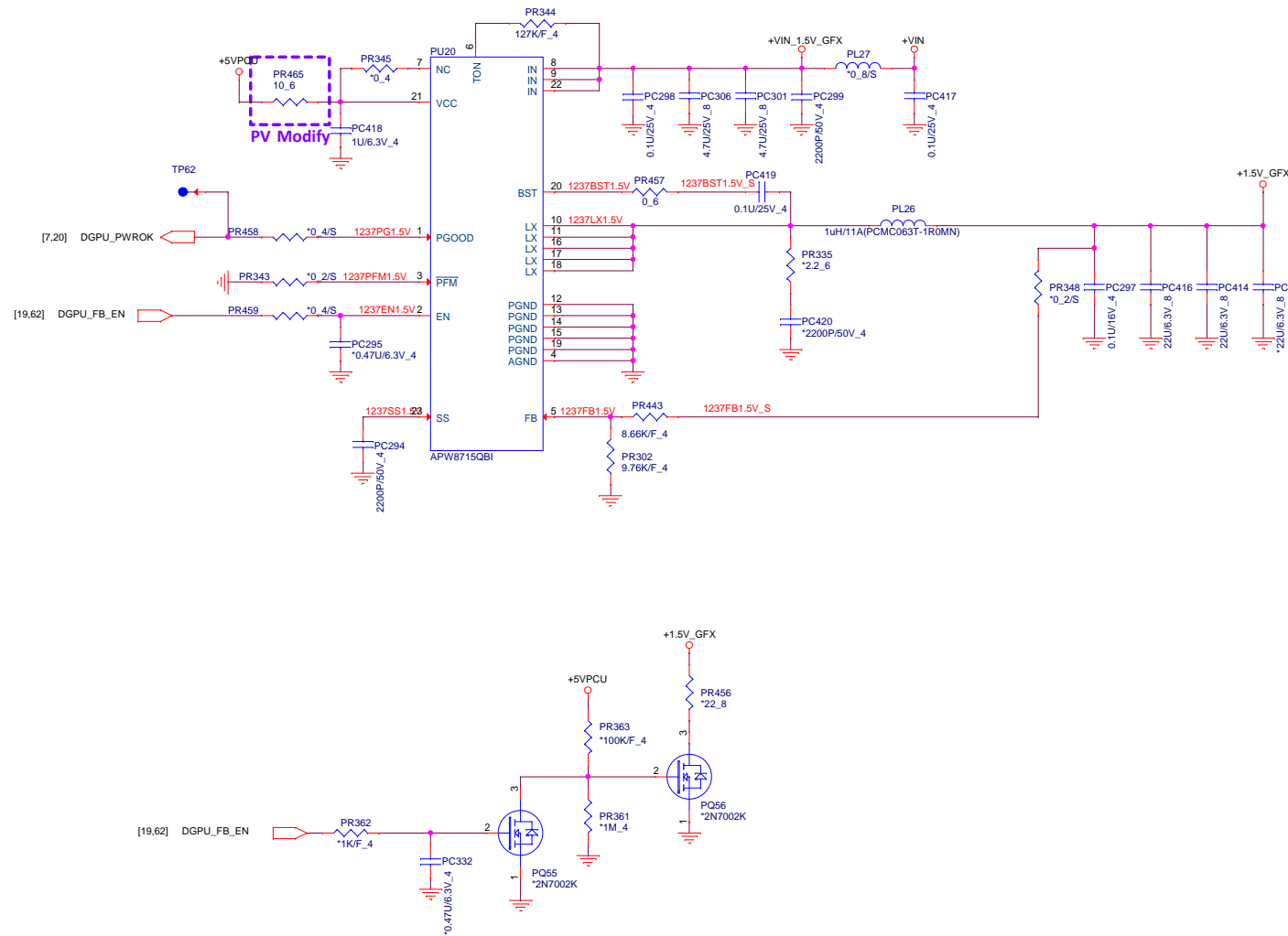
	<b>PROJECT : X63</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number 57 -- Load switch IC (APL3523A)	Rev 1A
	Date: Thursday, May 19, 2016	Sheet 59 of	67

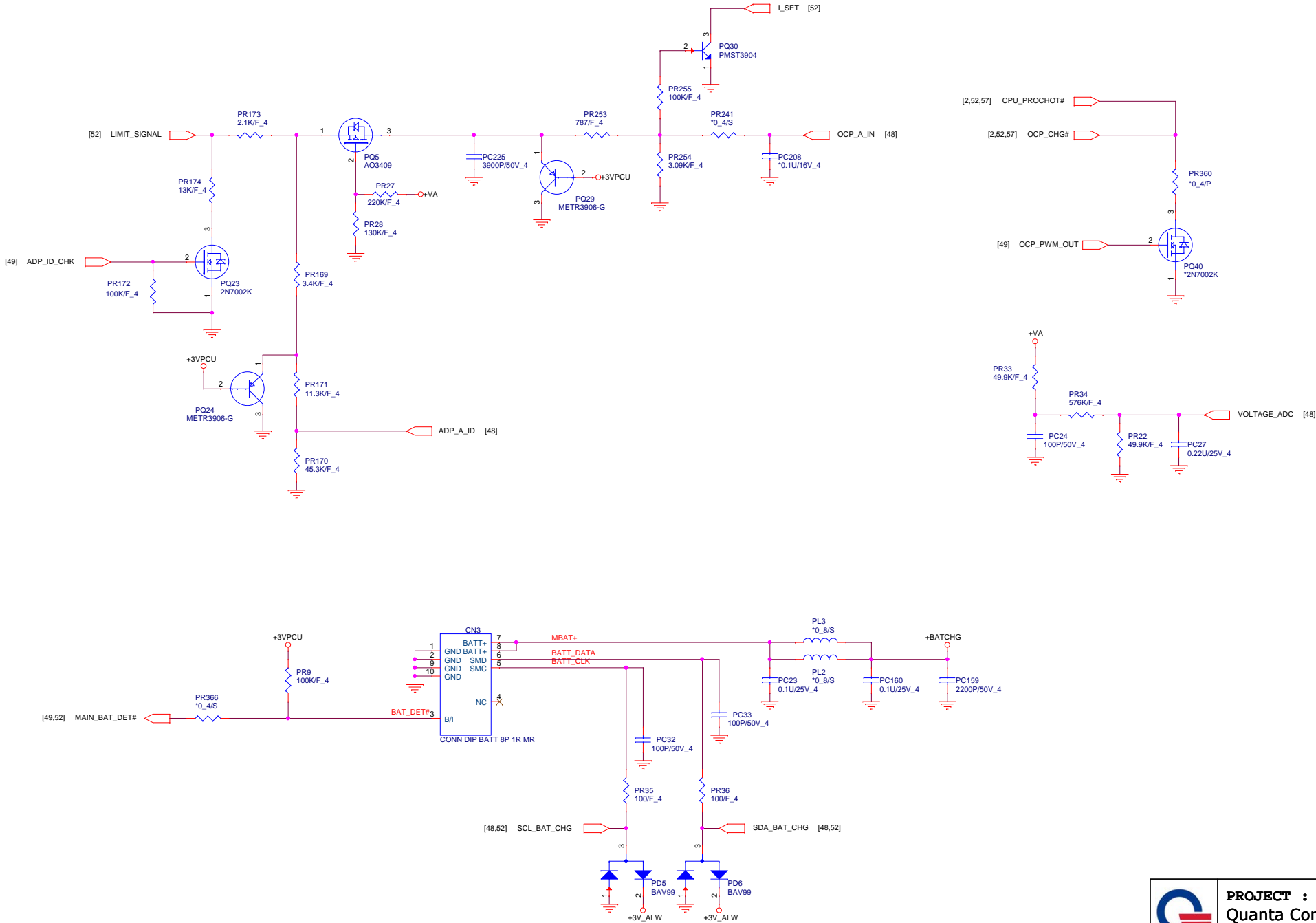


NB5	<b>PROJECT : X63</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number 58 - VGA Core1 (ISL62771)	Rev 1A
	Date: Thursday, May 19, 2016	Sheet 60 of 67	67









## POK CKT

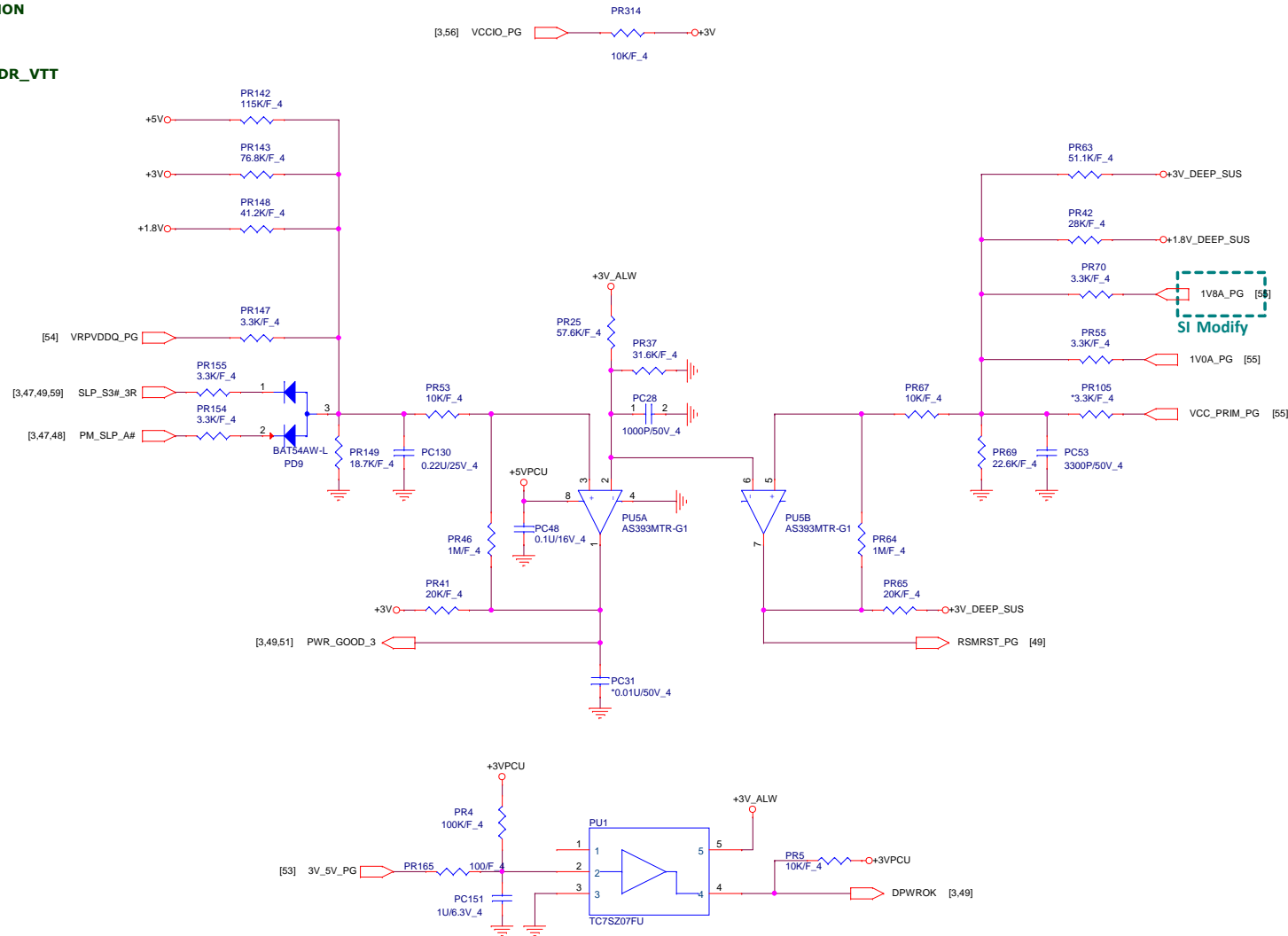
PM\_SLP\_S4# = SUSON

PM\_SLP\_S3# = MAINON

+V5S = +5V


+V3S = +3V

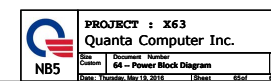
+V0.75S = +0.75V\_DDR\_VTT

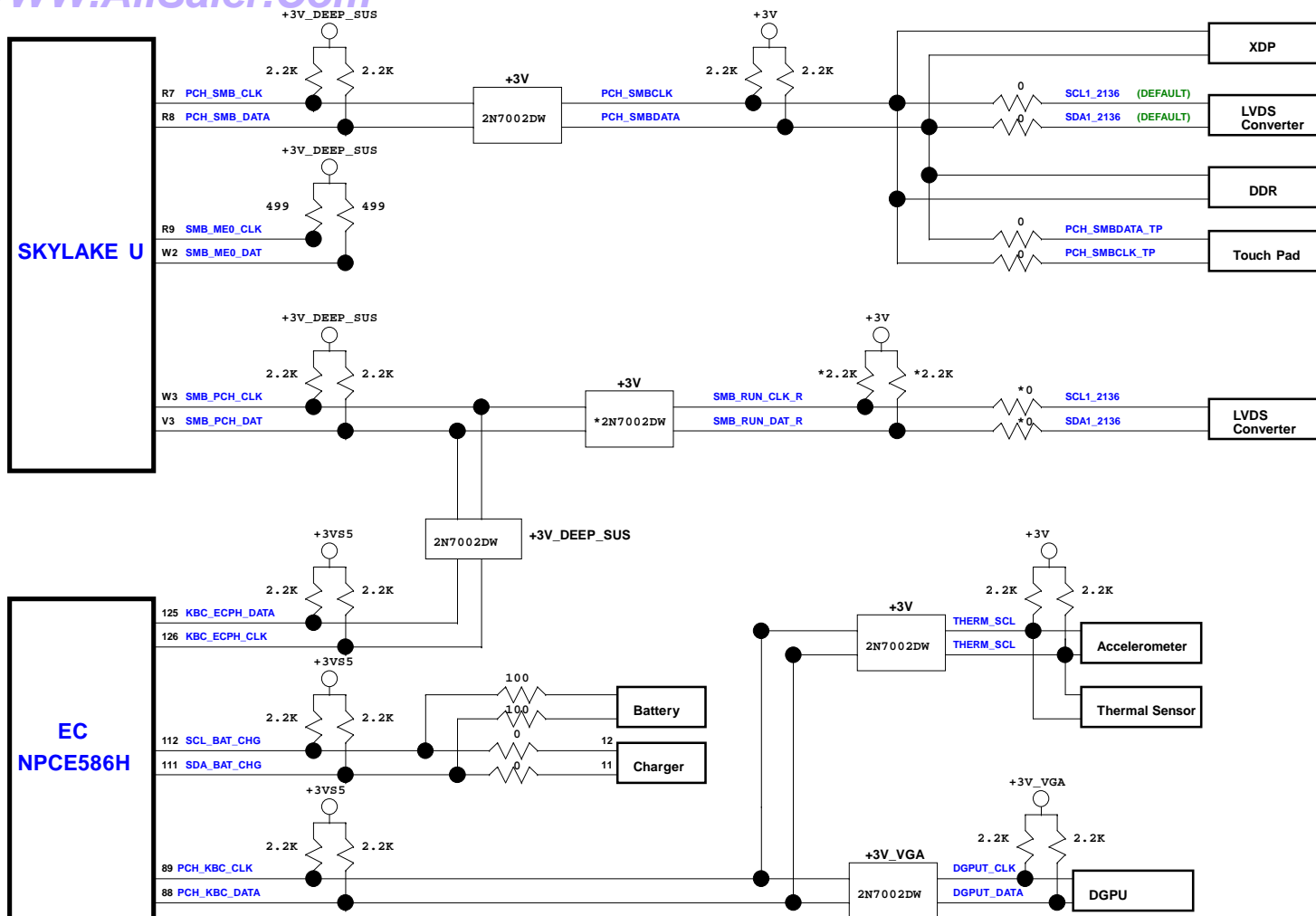


[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,67]  
 [6,27,29,30,40,42,43,55,59,67]  
 [9,41,51,52,53,59,63,67]

+3V  
 +5V  
 +3V\_ALW

	PROJECT : X63		
	Quanta Computer Inc.		
	Size Custom	Document Number 63 - PWROK	Rev 1A
	Date: Thursday, May 19, 2016	Sheet 64 of 67	

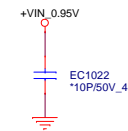
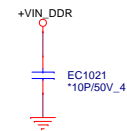
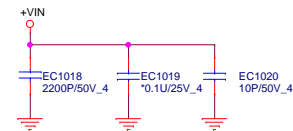
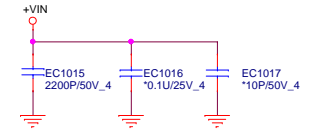
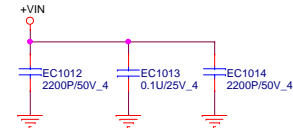
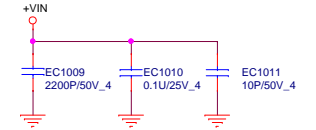
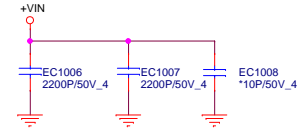
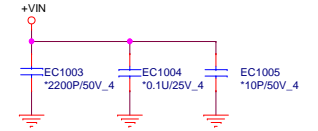
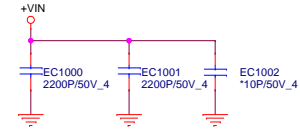
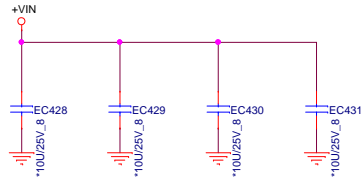
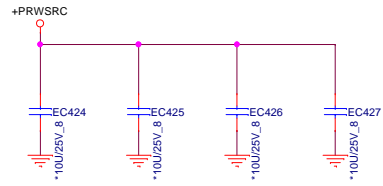




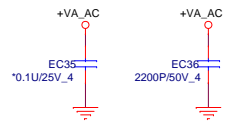
Example: \*499/F\_4 and \*0\_6/S  
 \* means none-installed  
 499 means value  
 F means 1%  
 \_4 means 0402 size  
 /S means short pad

Mult i plexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

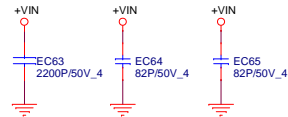
USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB2 #2	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC



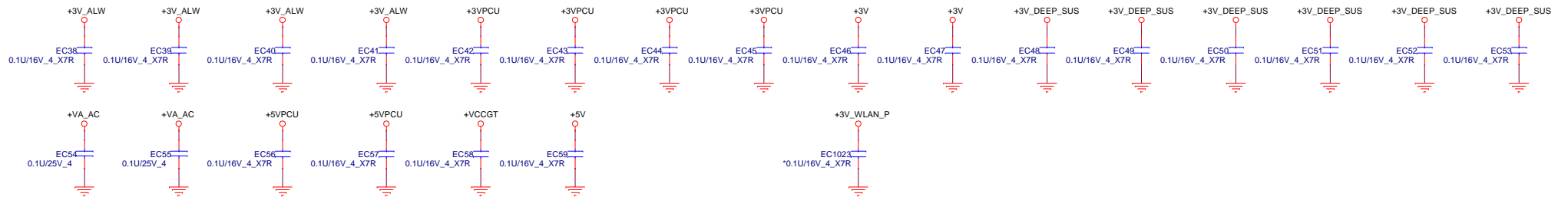
EMI cap



RF cap



EMI cap



Title				
<Title>				
Size	Document Number			Rev
Custom	<Doc>			<Rev>
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