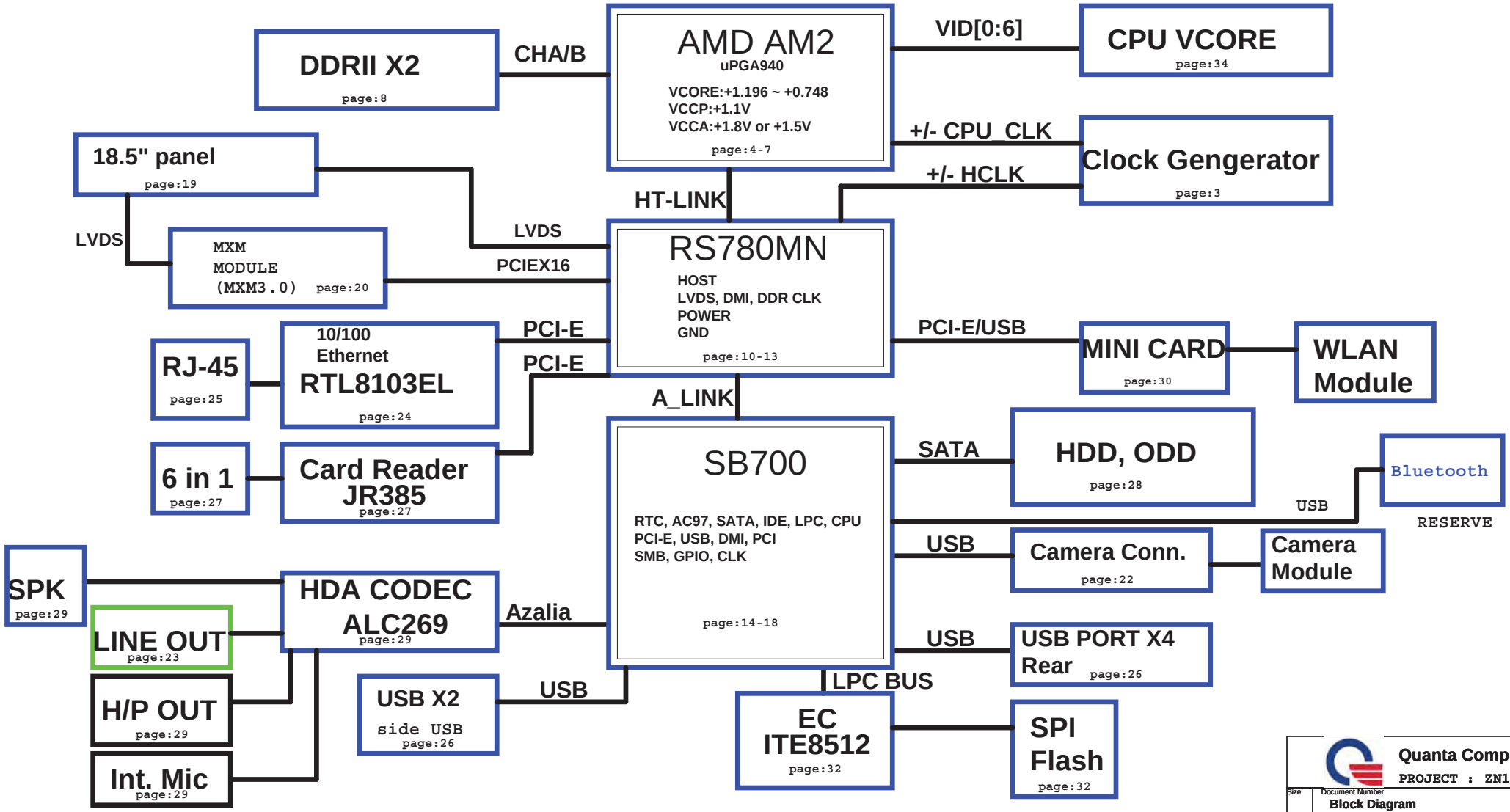
Amazon LCD PC Block Diagram

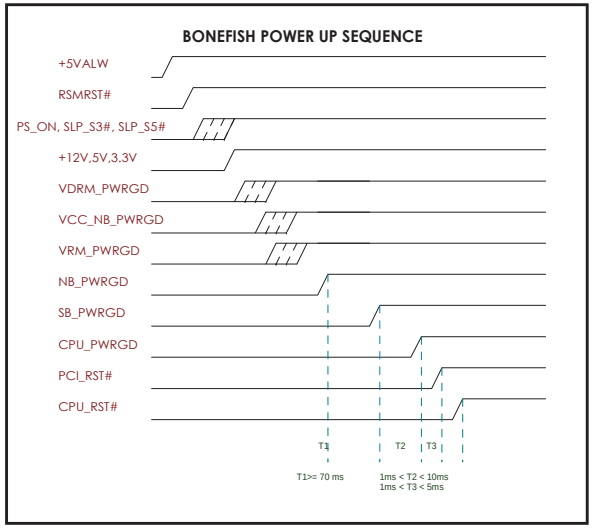


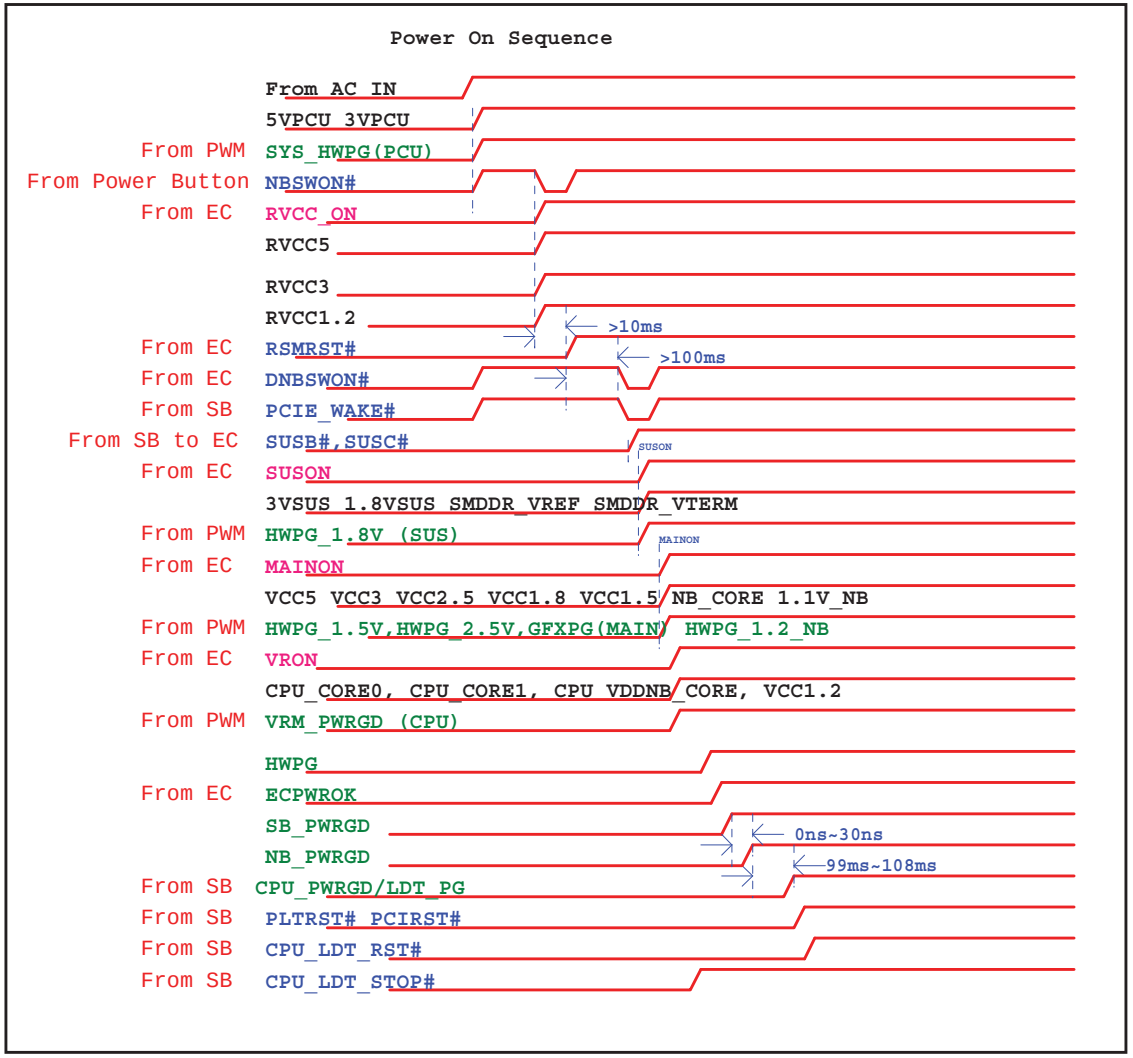
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

Voltage Rails

Power	Voltage	S0~S2	S3	S4	S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	VIN
3VPCU	3V	V	V	V	V	VIN
RVCC3	3V	V	V	V	V	RVCC_ON
RVCC1.2	1.2V	V	V	V	V	RVCC_ON
5VSUS	5V	V	V			SUSD
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAIND
VCC3	3V	V				MAIND
VCC1.8	1.8V	V				MAIND
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				VCC3
NB_CORE	1.2V	V				VRON
SMDDR_VTERM	0.9V	V				SUSON
CPU_CORE	By CPU	V				VR_ON





Quanta Computer Inc.
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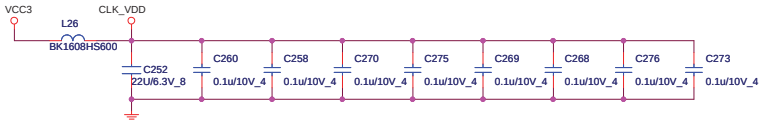
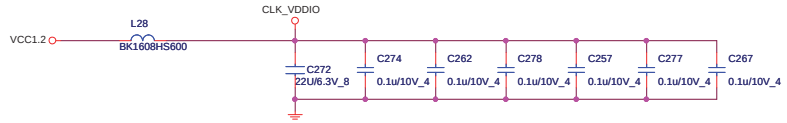
CLK_GEN_SLG8SP628





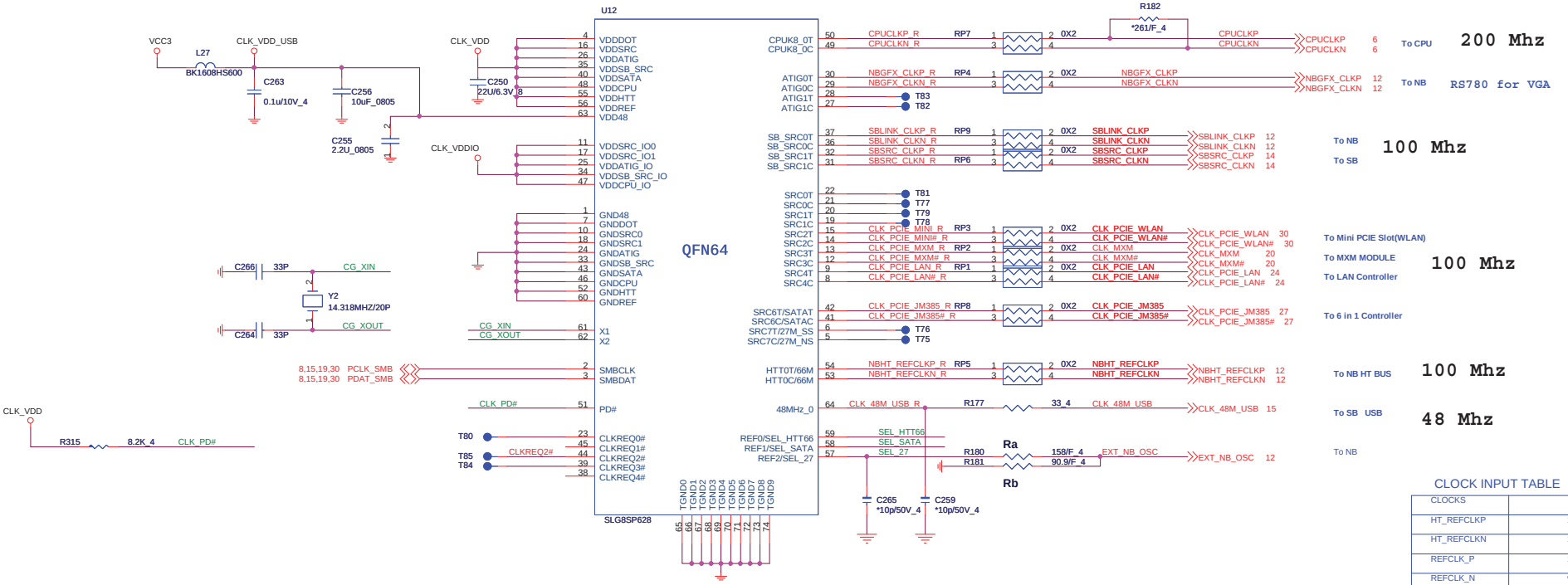
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

ICS9LPRS480 P/N : ALPRS480000

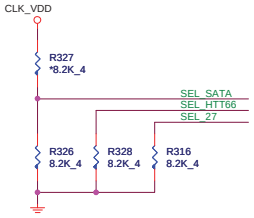
SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000



CLOCK INPUT TABLE

CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF



SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

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Size	Document Number	Rev
	Clock Generator	1A

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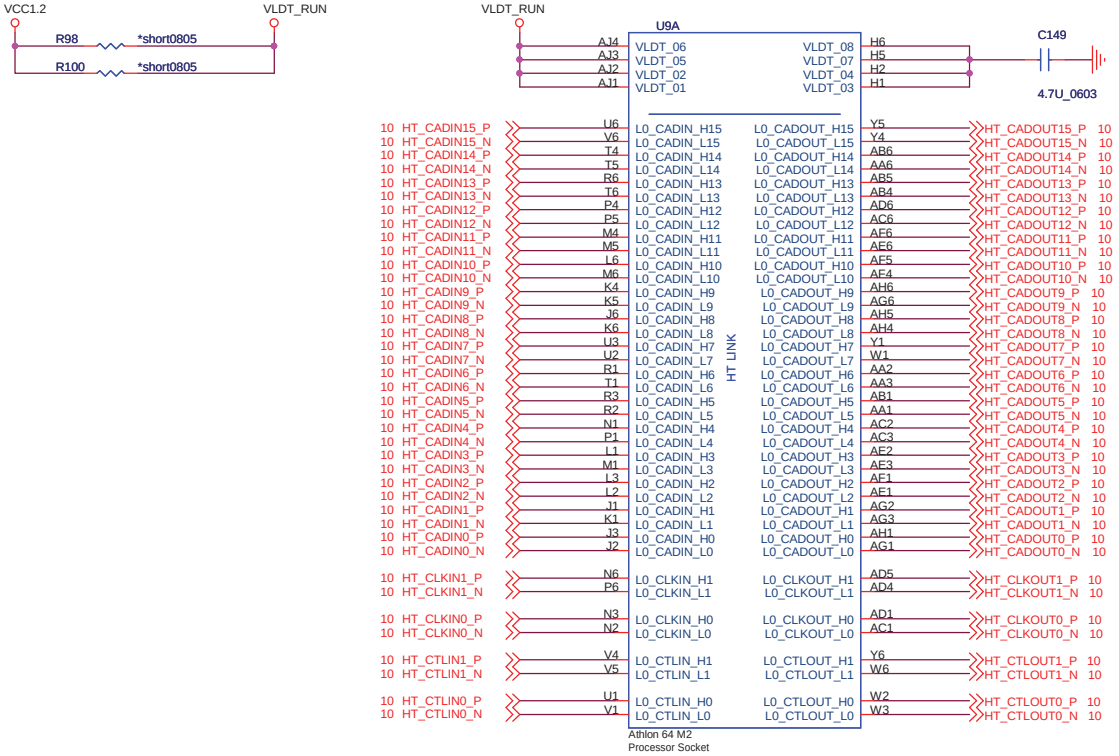
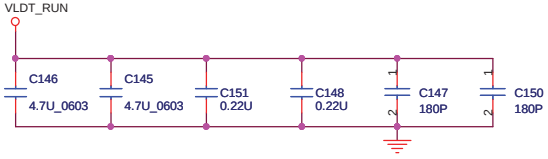
CPU HyperTransport Interface

VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.





Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	AMD AM2 HT I/F	1A
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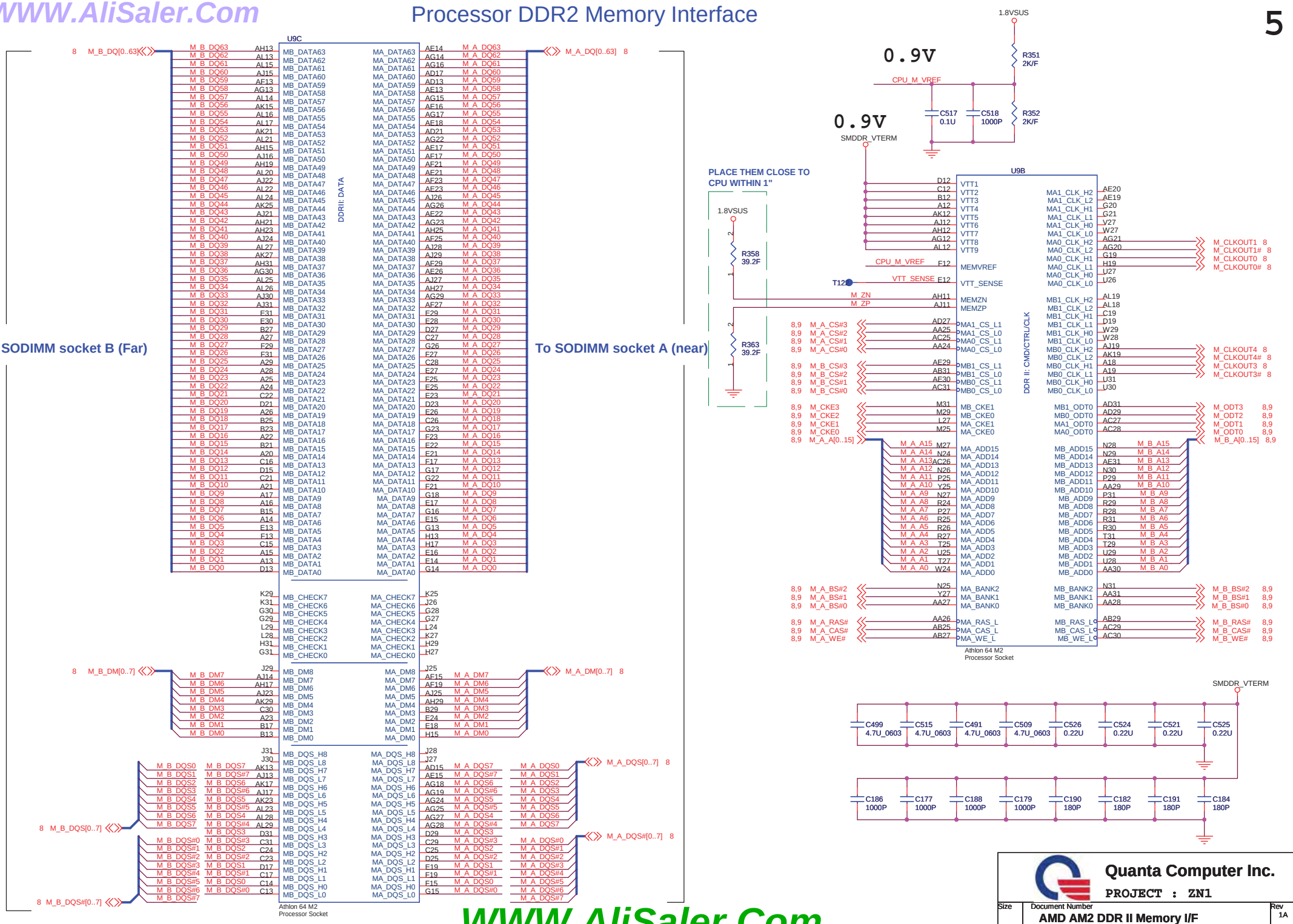
Processor DDR2 Memory Interface



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PROJECT : ZN1

Size	Document Number	Rev
	AMD AM2 DDR II Memory I/F	1A
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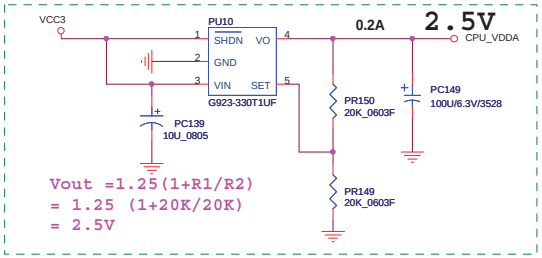
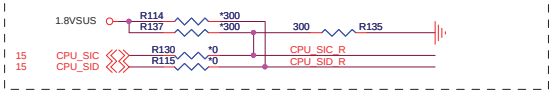
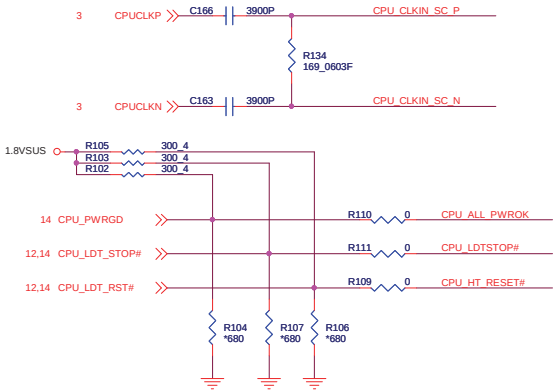
Add component to BOM
Vender suggest

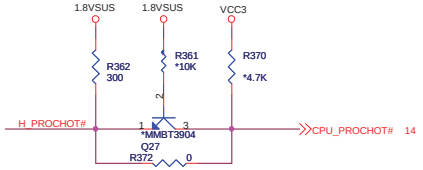
ATHLON Control and Debug

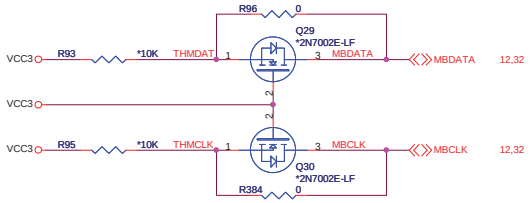


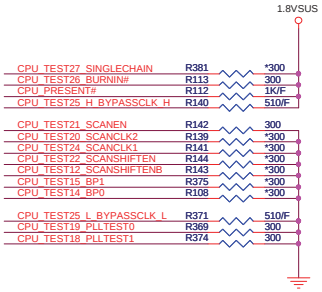
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

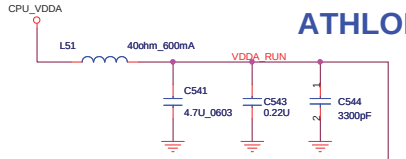


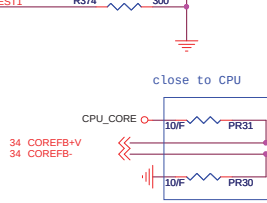


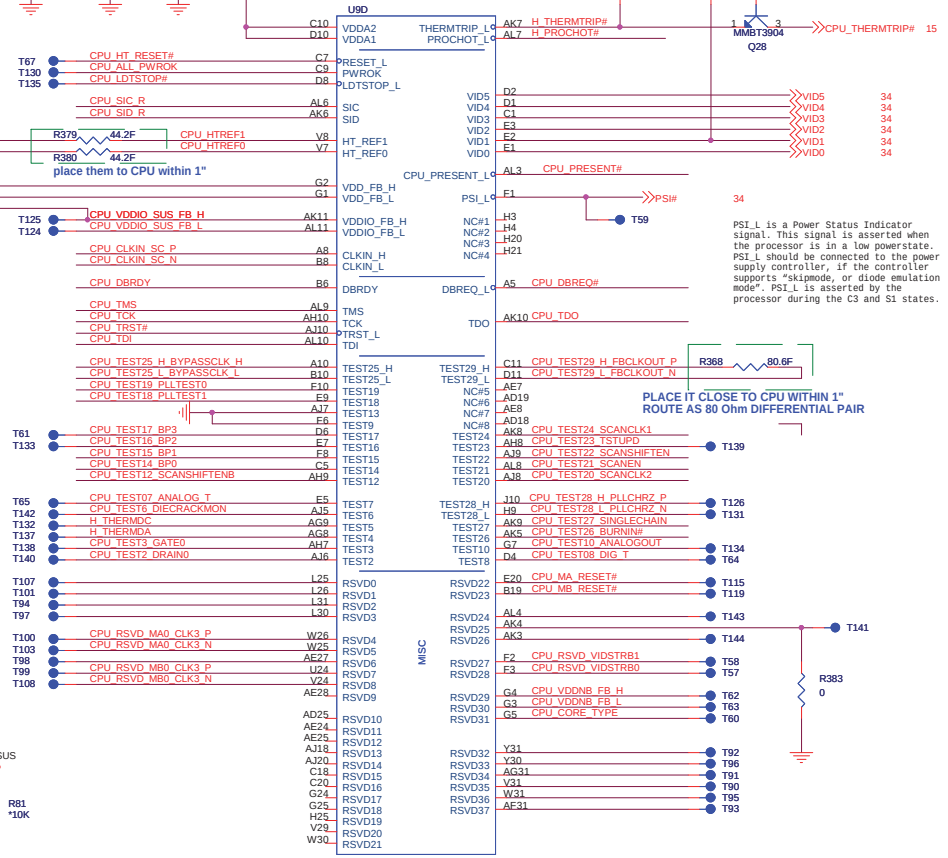


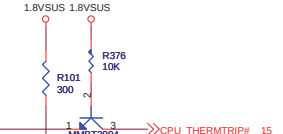








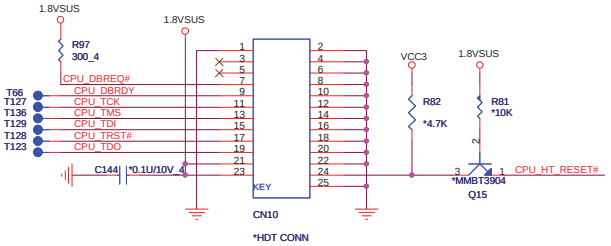




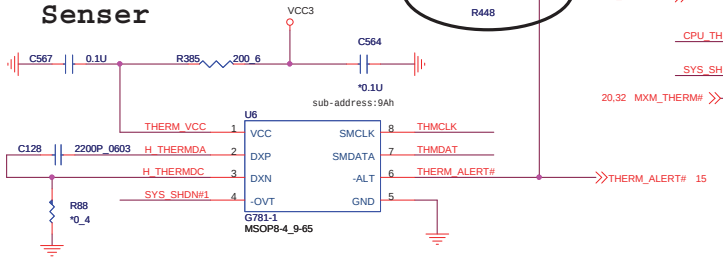
PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

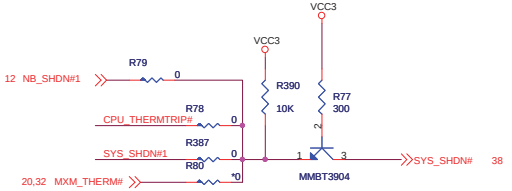
PLACE IT CLOSE TO CPU WITHIN 1"
ROUTE AS 80 Ohm DIFFERENTIAL PAIR

HDT Connector



CPU Thermal Senser





SMBUS SLAVE ADDRESS	
G781	98 (CPU)

Quanta Computer Inc.
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	AMD AM2 CTRL & DEBUG	1A
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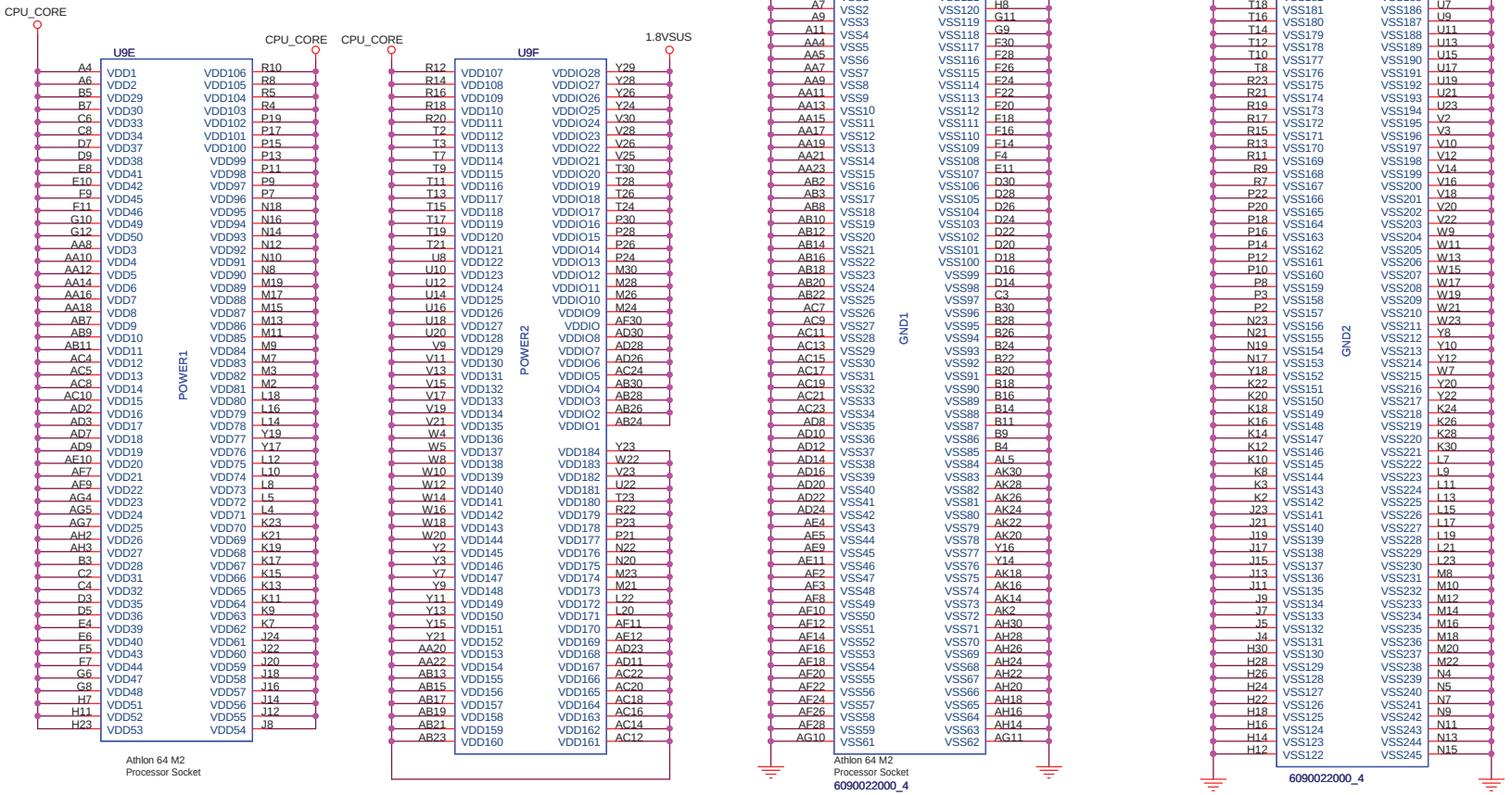
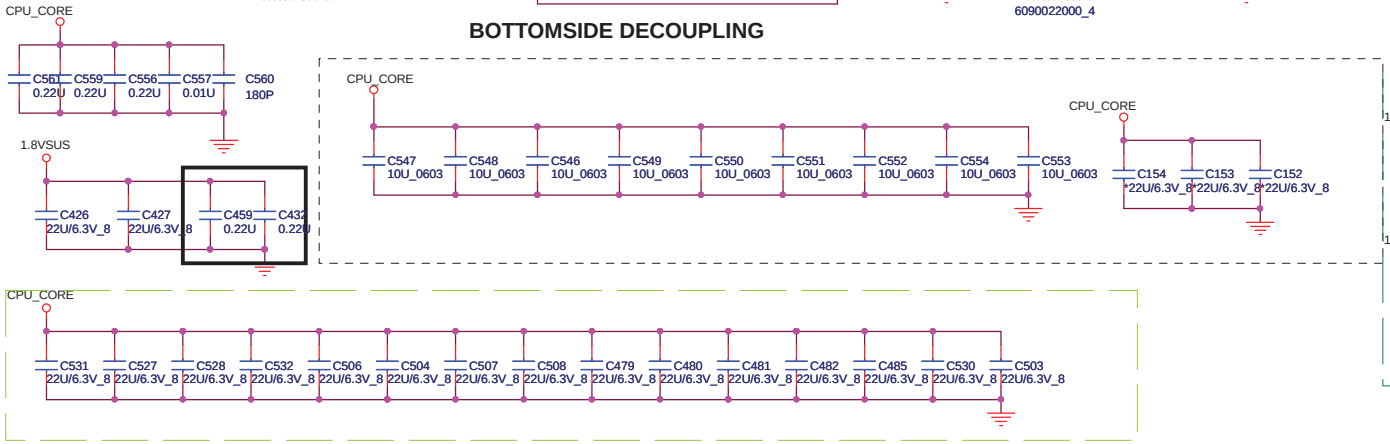
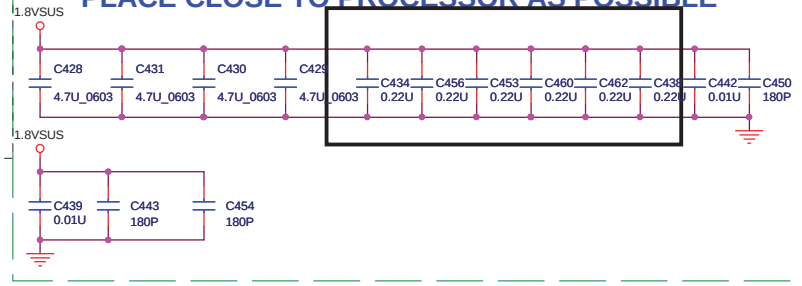
PROCESSOR POWER AND GROUND



BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



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Size	Document Number	Rev
	AMD AM2 PWR & GND	1A
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SA_A : 00

SA_B : 10

SO-DIMM (H=6.5)

SO-DIMM (H=11)

DDRII_SODIMM_H_6.5

DDRII_SODIMM_H_11

For EMI

0.9V

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PROJECT : ZN1

Size	Document Number	Rev
	DDRII SODIMM x2	1A
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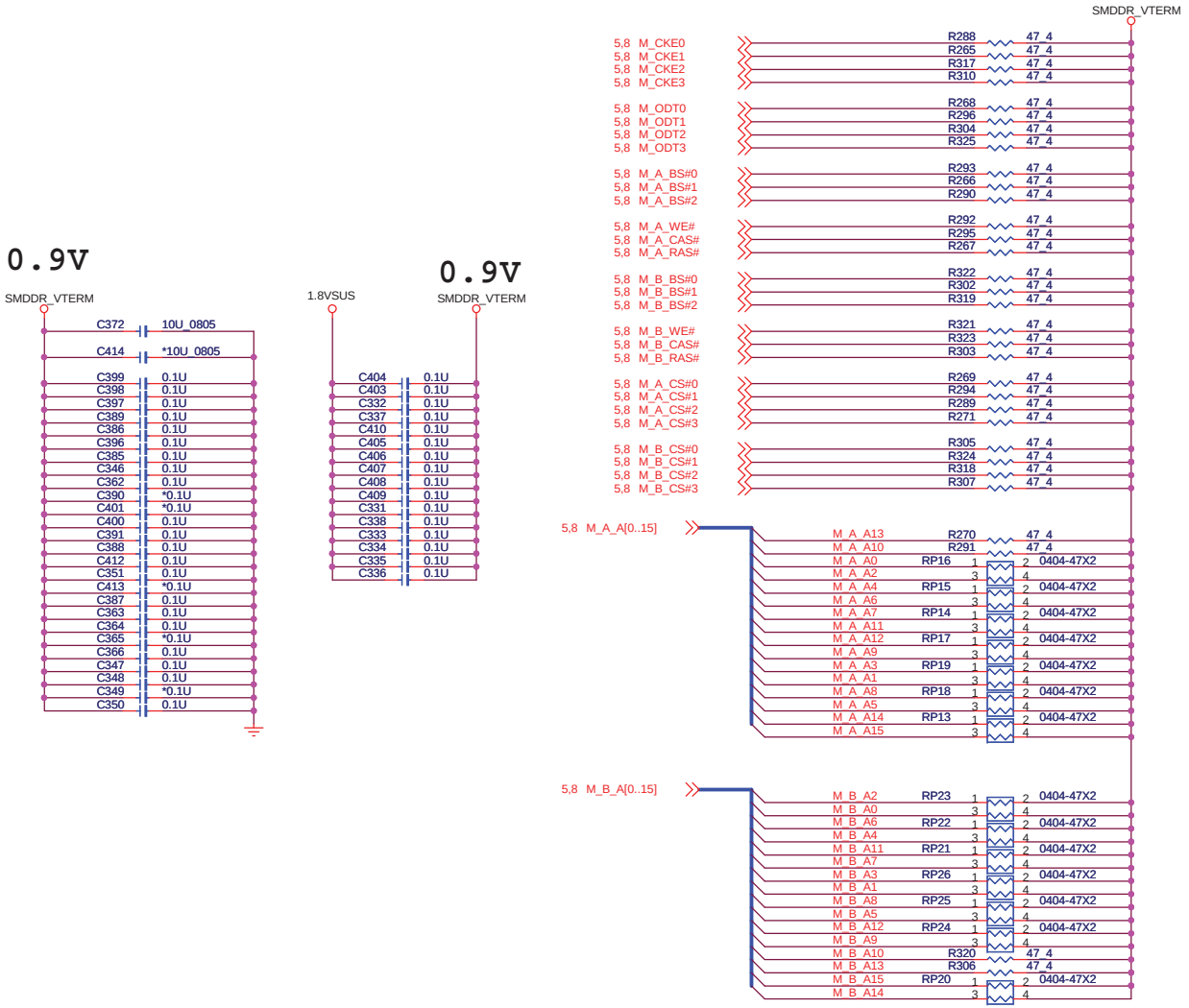

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PROJECT : ZN1

Size	Document Number	Rev
	DDRII TERMINATION	1A
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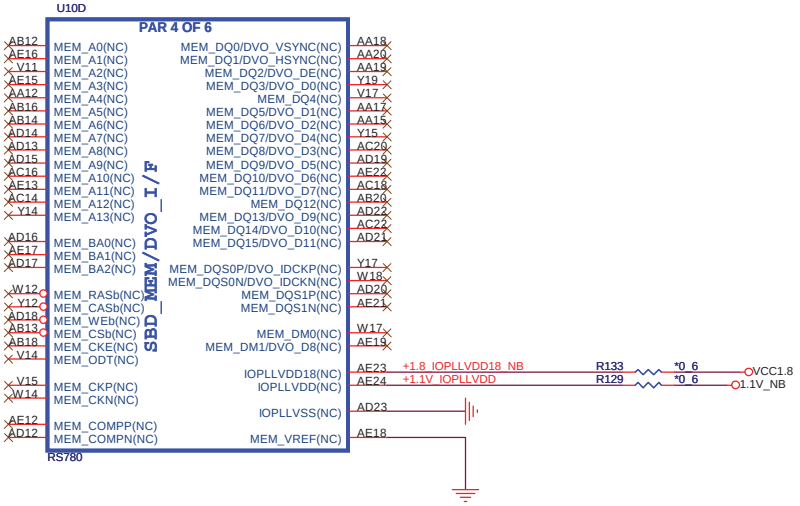
This block is for UMA RS780 only



Quanta Computer Inc.		
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Size	Document Number: RS780M HT LINK I/F 1/4	Rev: 1A
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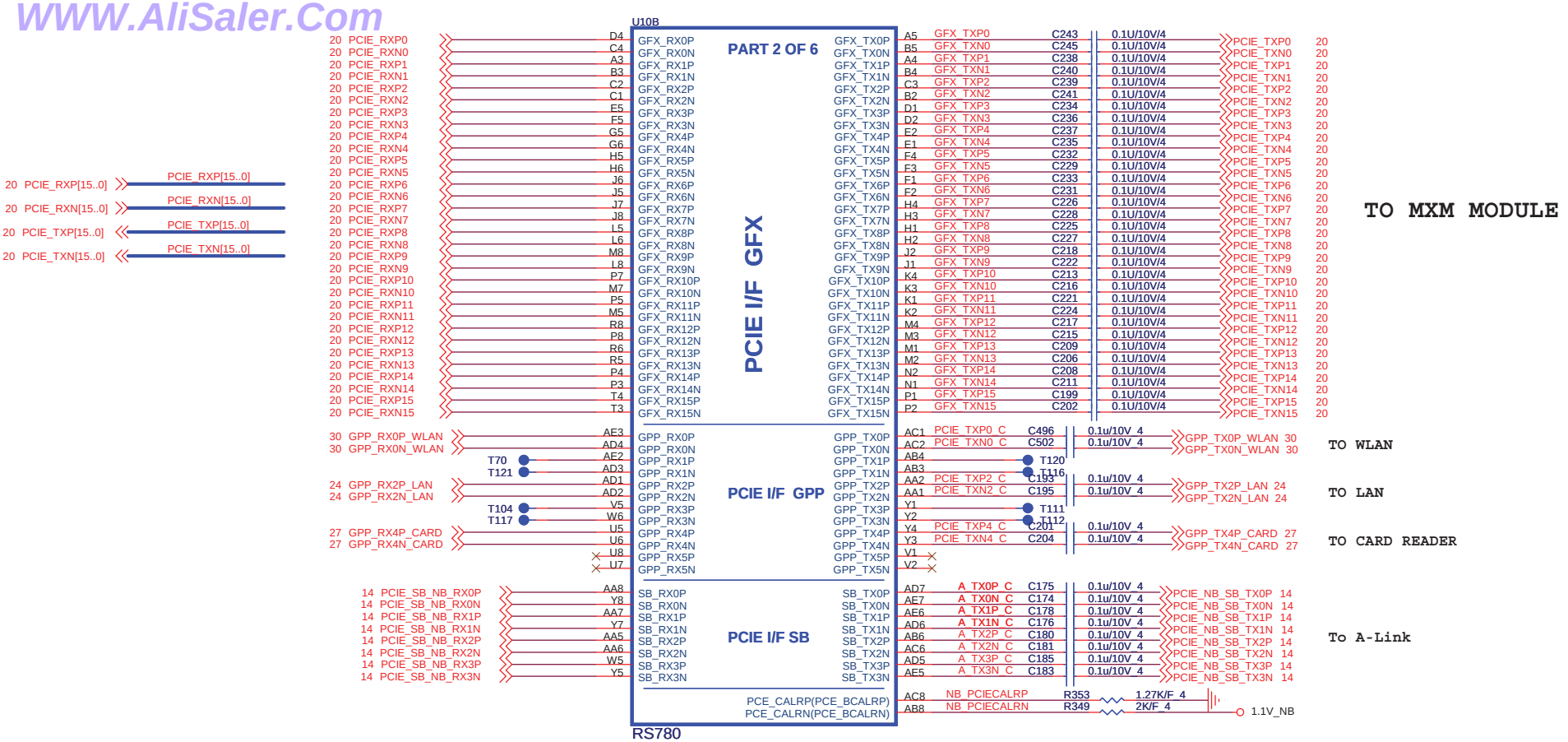

Quanta Computer Inc.	
PROJECT : ZN1	
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Thermal Senser

SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

U7 G781 MSOP8-4_9-65 — SMBUS Add. : 98h

C165 0.1U_4 · C162 *0.1U · R128 0R_6 · C171 2200P_0603 · R_NB_THRMDA · R_NB_THRMDC · 6 NB_SHDN#1

MBCLK 6,32 · MBDATA 6,32 · NB_TALERT# 15

VCC3 · R449 1K/F_4

Change BOM value

RX780 6,14 CPU_LDT_RST# R337 *0_4 NB_RST#_IN

RS780 14 NB_PLTRST# R336 0_4

North Bridge RESET

+NB_CORE_ON R162 *10K/F_4 VCC3 · R164 2.2K_4

CRT_RED · CRT_GRN · CRT_BLU · R205 150/F · R202 150/F · R197 140/F

RS780_AUX_CAL R166 *3K_4

CRT_VSYNC R160 3K_4 VCC3 · R161 *3K_4

CRT_HSYNC R159 3K_4 VCC3 · R158 *3K_4

U10C — RS780 — PART 3 OF 6

CRT/TVOUT: AVDD1(NC) F12 · AVDD2(NC) F12 · AVDD3(NC) F14 · AVSSDI(NC) G15 · AVDDQ(NC) H15 · AVSSQ(NC) H14 · C_Pr(DFT_GPIO5) F17 · Y(DFT_GPIO2) F17 · COMP_Pb(DFT_GPIO4) F15 · RED(DFT_GPIO0) G18 · REDb(NC) G17 · GREEN(DFT_GPIO1) F18 · GREENb(NC) F18 · BLUE(DFT_GPIO3) E19 · BLUEb(NC) F19 · DAC_HSYNC(PWM_GPIO4) A11 · DAC_VSYNC(PWM_GPIO6) B11 · DAC_SDA(PCE_TCALRN) E8 · DAC_SCL(PCE_RCALRN) F8 · DAC_RSET(PWM_GPIO1) G14

LVTM: PLLVDD(NC) A12 · PLLVDD18(NC) D14 · PLLVSS(NC) B12 · VDDA18HTPLL H17 · VDDA18PCIEPLL1 D7 · VDDA18PCIEPLL2 E7

PLL PWR: SYSRESETb D8 · POWERGOOD A10 · LDTSTOPb C10 · ALLOW_LDTSTOP C12

PM: HT_REFCLKP C25 · HT_REFCLKN C24

CLOCKs: REFCLK_P/OSCIN(OSCIN) E11 · REFCLK_N(PWM_GPIO3) F11 · GFX_REFCLKP T2 · GFX_REFCLKN T1 I/O · GPP_REFCLKP U1 · GPP_REFCLKN U2 I/O · GPPSB_REFCLKP(SB_REFCLKP) V4 · GPPSB_REFCLKN(SB_REFCLKN) V3

MIS.: I2C_DATA A9 · I2C_CLK B9 · DDC_DATA/AUX0N(NC) B8 · DDC_CLK/AUX0P(NC) A8 · AUX1P(NC) B7 · AUX1N(NC) A7 · STRP_DATA B10 · RSVD G11 · AUX_CAL(NC) C8

TXOUT_L0P(NC) A22 · TXOUT_L0N(NC) B22 · TXOUT_L1P(NC) A21 · TXOUT_L1N(NC) B21 · TXOUT_L2P(NC) B20 · TXOUT_L2N(DBG_GPIO0) A20 · TXOUT_L3P(NC) A19 · TXOUT_L3N(DBG_GPIO2) B19 · TXOUT_U0P(NC) B18 · TXOUT_U0N(NC) A18 · TXOUT_U1P(PCIE_RESET_GPIO3) A17 · TXOUT_U1N(PCIE_RESET_GPIO2) B17 · TXOUT_U2P(NC) D20 · TXOUT_U2N(NC) D21 · TXOUT_U3P(PCIE_RESET_GPIO5) D18 · TXOUT_U3N(NC) D19 · TXCLK_LP(DBG_GPIO1) B16 · TXCLK_LN(DBG_GPIO3) A16 · TXCLK_UP(PCIE_RESET_GPIO4) D16 · TXCLK_UN(PCIE_RESET_GPIO1) D17

VDDLTP18(NC) A13 · VSSLTP18(NC) B13 · VDDLT18_1(NC) A15 · VDDLT18_2(NC) B15 · VDDLT33_1(NC) A14 · VDDLT33_2(NC) B14 · VSSLT1(VSS) C14 · VSSLT2(VSS) D15 · VSSLT3(VSS) C16 · VSSLT4(VSS) C18 · VSSLT5(VSS) C20 · VSSLT6(VSS) E20 · VSSLT7(VSS) C22

LVDS_DIGON(PCE_TCALRP) E9 · LVDS_BLON(PCE_RCALRP) F7 · LVDS_ENA_BL(PWM_GPIO2) G12

TMDS_HPD(NC) D9 · HPD(NC) D10 · TVCLKIN(PWM_GPIO5) D12 · THERMALDIODE_P AE8 · THERMALDIODE_N AD8 · TESTMODE D13

To LVDS panel

LVDS POWER

+3V_AVDD_NB · +1.8V_AVDDDI_NB · +1.8V_AVDDQ_NB · +1.1V_PLLVDD · +1.8V_VDDA18HTPLL · +1.8V_VDDA18PCIEPLL · +1.8V_VDDLTP18_NB · +1.8V_VDDLT_18_NB · +3V_VDLT33_NB

INT_TV_C/R T109 · T118 · T114 · R346 IV@715/F_6 · DAC_RSET_NB

21 CRT_RED · 21 CRT_GRN · 21 CRT_BLU · R343 0_4 · R344 0_4 · R345 0_4

21 CRT_HSYNC · 21 CRT_VSYNC · 21 CRT_DDCDAT · 21 CRT_DDCCLK

18 NB_PWRGD_IN · 14 ALLOW_LDTSTOP · 3 NBHT_REFCLKP · 3 NBHT_REFCLKN · NB_RST#_IN · NB_PWRGD_IN · NB_LDT_STOP# · NB_ALLOW_LDTSTOP · NBHT_REFCLKP · NBHT_REFCLKN

3 EXT_NB_OSC · 1.1V_NB · R330 4.7K_4 · RS780 · R331 4.7K_4 · R332 0_4 NB_REFCLK_P · R333 0_4 NB_REFCLK_N

3 NBGFX_CLKP · 3 NBGFX_CLKN · NBGFX_CLKP · NBGFX_CLKN · T110 · T113 · NBGPP_CLKP · NBGPP_CLKN

3 SBLINK_CLKP · 3 SBLINK_CLKN · SBLINK_CLKP · SBLINK_CLKN

19,20 LVDS_DAT · 19,20 LVDS_CLK

T73 · T74 · RS740_DFT_GPIO1 · +NB_CORE_ON · T72 · RS780_AUX_CAL

TMDS_HPD0 T102 · TMDS_HPD1 T106 · SUS_STAT#_NB · R329 *0_4 · D48 1SS355 · SUS_STAT# 15 · PLTRST# 14,16,20,24,27,30 · R_NB_THRMDA T68 · R_NB_THRMDC T69 · TEST_EN · R334 1.82K/F_4

VCC3 · L48 BLM18PG201SN1D(200_1.4A)_6 · +3V_AVDD_NB · C461 2.2u/6.3V_6

1.1V_NB · BLM18PG201SN1D(200_1.4A)_6 L22 · +1.1V_PLLVDD · C219 2.2u/6.3V_6

VCC1.8 · L25 BLM18PG201SN1D(200_1.4A)_6 · +1.8V_PLLVDD18 · C230 10u/6.3V_8 · C474 2.2u/6.3V_6

VCC1.8 · R339 *short0603 · +1.8V_AVDDDI_NB · C466 0.1u/10V_4 · BLM18PG201SN1D(200_1.4A)_6 L43 · +1.8V_AVDDQ_NB · C433 2.2u/6.3V_6

VCC1.8 · L21 BLM18PG201SN1D(200_1.4A)_6 · +1.8V_VDDLTP18_NB · C455 2.2u/6.3V_6

L20 BLM21PG201SN1D(200_100M_2A)_8 · +1.8V_VDDLT_18_NB · C210 4.7u/6.3V_6 · C207 0.1u/10V_4

VCC1.8 · VDDA18PCIEPLL -PCIE PLL · L46 BLM18PG221SN1D(220_1.4A)_6 · 20mils width · +1.8V_VDDA18PCIEPLL · C440 2.2u/6.3V_6

VDDA18HTPLL -HT LINK PLL · L24 BLM18PG201SN1D(200_1.4A)_6 · 20mils width · +1.8V_VDDA18HTPLL · C223 2.2u/6.3V_6

VCC1.8 · R169 *300_4 · Q17 *BSS138_NL/SOT23 · VCC1.8 · +VDDG_NB · R165 *4.7K_4 · 6,14 CPU_LDT_STOP# · NB_LDT_STOP# · R167 0_4 · RS780

R163 0_6 · VCC3 · +VDDG_NB

VCC3 · L47 · +3V_VDLT33_NB · *BLM21PG221SN1D(220_100M_2A)_8 · C444 *2.2u/6.3V_6

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PROJECT : ZN1

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	RS780M-SYSTEM I/F 3/4	1A
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U10F

PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

RS780 POWER DIFFERENCE TABLE

PIN NAME	RS780	PIN NAME	RS780
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

VDDHT - HT LINK digital I/O for RS780

1.1V_NB

+1.1V 2A for RS780M

L53 BLM21PG221SN1D(220_100M_2A)_8 +1.1V_VDDHT

C538 4.7U/6.3V_6 C495 0.1u/10V_4 C510 0.1u/10V_4 C505 0.1u/10V_4

VDDHTRX - HT LINK RX I/O for RS780

L23 BLM21PG221SN1D(220_100M_2A)_8 +1.1V_VDDHTRX

C205 4.7U/6.3V_6 C490 0.1u/10V_4 C203 0.1u/10V_4 C200 0.1u/10V_4

+1.2V 2A for RS780M+SB700

VCC1.2 L17 BLM21PG221SN1D(220_100M_2A)_8 +1.2V_VDDHTTX

C161 4.7U/6.3V_6 C514 0.1u/10V_4 C535 0.1u/10V_4 C529 0.1u/10V_4 C555 0.1u/10V_4

VDDHTTX - HT LINK TX I/O for RS780

+1.8V 1A for RS780M+SB700

VCC1.8 L52 BLM21PG221SN1D(220_100M_2A)_8 +1.8V_VDDA18PCIE

VDDA18PCIE - PCIE TX stage I/O for RS780

C522 4.7U/6.3V_6 C486 4.7U/6.3V_6 C516 0.1u/10V_4 C500 0.1u/10V_4 C472 0.1u/10V_4 C492 0.1u/10V_4

VDD18 - RS780 I/O transform

VCC1.8 R338 *short0603 C458 1u/10V_4 +1.8V_VDDG18_NB

VCC1.8 R136 *short0603 C170 1u/10V_4 +1.8V_VDD18_MEM

VDD18_MEM For UMA RS780

U10E

PART 5/6

POWER

RS780

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7 → J17 K16 L16 M16 P16 R16 T16

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7 → H18 G19 F20 E21 D22 B23 A23

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13 → AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15 → J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) → F9 G9

VDD18_MEM1(NC) VDD18_MEM2(NC) → AE11 AD11

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17 → A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC) → AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC) → H11 H12

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 → K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE R348 *short0805 1.1V_NB

C476 0.1u/10V_4 C468 0.1u/10V_4 C489 1u/10V_4 C445 1u/10V_4 C497 4.7U/6.3V_6

VDDC - Core Logic power

NB_CORE

C513 0.1u/10V_4 C487 0.1u/10V_4 C519 0.1u/10V_4 C501 0.1u/10V_4 C449 10u/6.3V_8 C533 0.1u/10V_4 C467 0.1u/10V_4 C473 0.1u/10V_4 C470 *0.1u/10V_4 C483 10u/6.3V_8

C512 0.1u/10V_4 C493 0.1u/10V_4 C523 0.1u/10V_4 C457 10u/6.3V_8

+1.8V_VDD_MEM *BLM21PG221SN1D(220_100M_2A)_8 L50 VCC1.8 R356 0_6

VDD_MEM For UMA RS780

+3V_VDDG33 R335 RS780 *short0603 VCC3

C469 0.1u/10V_4 C477 0.1u/10V_4

VDD33 - 3.3V I/O

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	RS780M-POWER4/4	1A

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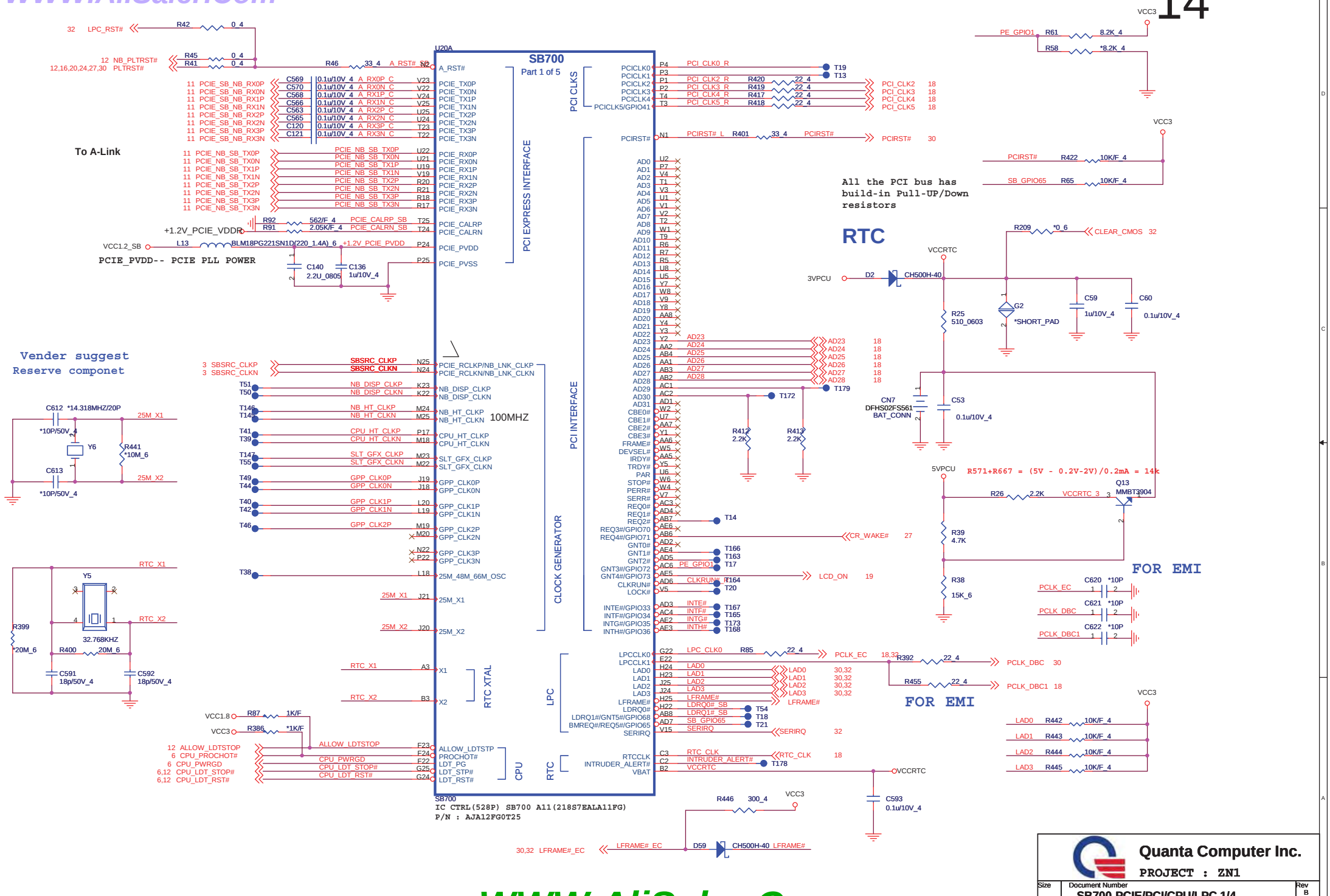

Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: SB700-PCIE/PCI/CPU/LPC 1/4	Rev B
Date: Friday, May 08, 2009	Sheet 14 of 41	

RVCC3
R408 *2.2K_4 SB_TEST0
R35 *2.2K_4 SB_TEST1
R34 *2.2K_4 SB_TEST2

RVCC3
R409 *10K/F_4 SWI#

VCC3 Clock gen /DDR2 /MINI CARD/NEW CARD
R83 2.2K_4 PCLK_SMB
R84 2.2K_4 PDAT_SMB

RVCC3
R406 2.2K_4 SB_SMBCLK1
R405 2.2K_4 SB_SMBDATA1
ADD for BIOS Write Protect

RVCC3
R391 2.2K_4 SB_SCLK2
R388 2.2K_4 SB_SDATA2

VCC3
R407 *3K_4 SUS_STAT#

To Azalia

29 ACZ_BITCLK_AUDIO — R404 33 AZ_BITCLK; C595 *10P/50V_4
29 ACZ_SDOUT_AUDIO — R402 33 AZ_SDOUT; C594 *10P/50V_4
29 ACZ_SYNC_AUDIO — R28 33 AZ_SYNC; C58 *10P/50V_4
29 ACZ_SDIN0 — R33 33 AZ_SDIN0; R31 *33 AZ_SDIN1
29 ACZ_RESET#_AUDIO — R30 33 AZ_RST#
R403 *10K_4
R32 *10K_4

32 SUSB# 32 SUSC# 32 DNBSWON# 18 SB_PWRGD_IN 12 SUS_STAT#
T175 RI# E1
T170 SLP_S2 H7
T27 SUSB# F5
SUSC# G1
DNBSWON# H2
SB_PWRGD_IN H1
SUS_STAT# K3
SB_TEST2 H5
SB_TEST1 H4
SB_TEST0 H3

32 GATEA20 32 RCIN# 32 SCI# 32 KBSMI#
GATEA20 Y15
RCIN# W15
SCI# K4
KBSMI# K24

T176 SYS_RST# J2
T181 PCIE_WAKE# H6
SWI# F2
CPU_THERMTRIP# J6
WD_PWRGD W14
24,30 PCIE_WAKE# 32 SWI# 6 CPU_THERMTRIP# 18 WD_PWRGD

32 RSMRST# — RSMRST# D3

del power control to MXM 12V&RST MXM

T183 — dGPU_PWR_EN# AE18
20 dGPU_PWR_EN# 32 BIOS_WP#
20 dGPU_RUNPWROK AD18
19 WRITE_EDID_ROM AA19
20,32 dGPU_PRSNT# W17
V17
W20

29 SPKR 3,8,19,30 PCLK_SMB 3,8,19,30 PDAT_SMB
R395 0_4 ACZ_SPKR W21
PCLK_SMB AA18
PDAT_SMB W18
SB_SMBCLK1 K1
SB_SMBDATA1 K2

24 ENERGY_DET — RT28 — AA20
Y18
C1
SES_INT Y19
T45 — R410 *0_4 CR_CPPE#R — 27 CR_CPPE# G5

T156 B9
26 USB_OCP5# B8
26 USB_OCP4# A8
26 USB_OCP3# A9
26 USB_OCP2# E5
26 USB_OCP1# F8
26 USB_OCP0# E4

AZ_BITCLK M1
AZ_SDOUT M2
AZ_SDIN0 J7
AZ_SDIN1 J8
6 THERM_ALERT# R27 0_4 SMBALERT#_1 L8
12 NB_TALERT# NB_TALERT# M3
AZ_SYNC L6
18 AZ_RST# AZ_RST# M4
L5

HD audio interface is 3.3V voltage

U20D

SB700 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7

INTEGRATED uC

USBCLK/14M_25M_48M_OSC
USB_RCOMP

USB MISC

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

USB 1.1

USB 2.0

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPIO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

INTEGRATED uC

SB700

C8 CLK_48M_USB — CLK_48M_USB 3
G8 USB_RCOMP_SB R67 11.8K/F_6

DELETE T159(E7)

E6 USB_FSD13P — T10
E7
F7 USB_FDS12P — T30
E8 USB_FSD12N — T24

DELETE T31(H11) and T35(J10)

H11
J10
E11 — T32
F11 — T33
A11 — T36
B11 — T34

C10 D10 USBP8+ USBP8- 22 — TO WEBCAM
G11 H12 USBP7+ USBP7- 30 — TO BLUETOOTH
E12 E14 USBP6+ USBP6- 30 — TO WLAN
C12 D12 USBP5+ USBP5- 26 — TO SIDE USB
B12 A12 USBP4+ USBP4- 26 — TO SIDE USB
G12 G14 USBP3+ USBP3- 26 — To M/B USB
H14 H15 USBP2+ USBP2- 26 — To M/B USB
A13 B13 USBP1+ USBP1- 26 — To M/B USB
B14 A14 USBP0+ USBP0- 26 — To M/B USB

A18
B18
F21
D21 SB_SCLK2
F19 SB_SDATA2
E20 CPU_SIC 6
E21 CPU_SID 6
E19 T182
D19 SB_GPIO16 18
E18 SB_GPIO17 18

SPI/LPC define

CLK_48M_USB
R64 *10_6
C72 *10p/50V_4
for EMI

Quanta Computer Inc.
PROJECT : ZN1
Size | Document Number: SB700-ACPI/GPIO/USB 2/4 | Rev 1A
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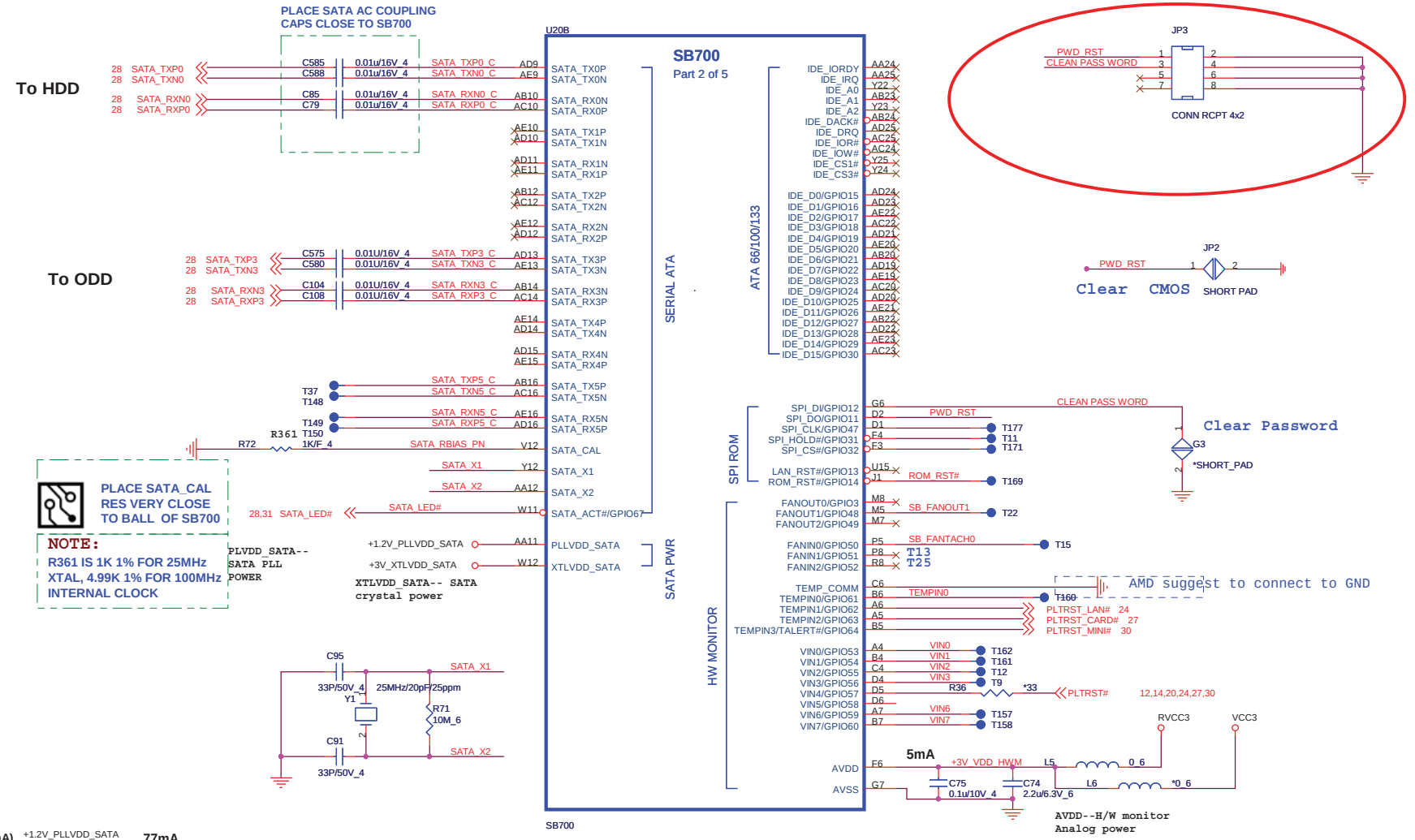

Quanta Computer Inc.			
PROJECT : ZN1			
Size	Document Number		Rev
	SB700-SATA/IDE/HWM/SPI 3/4		1A
Date: Friday, May 08, 2009		Sheet 16 of 41	

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

U20C
SB700
Part 3 of 5
POWER
SB700

U20E
SB700
GROUND
Part 5 of 5
SB700

VDDQ--3.3V I/O power
1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE
VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power
PCIE_VDDR--PCIE I/O power
AVDD_SATA--SATA phy power
For support USB wakeup-->3V_S5
AVDDTX--USB Phy
Analog I/O power
VDD-- S/B CORE power
CKVDD_1.2V-- Internal
clock Generator I/O
power
S5_3.3--3.3v standby power
S5_1.2V--1.2V standby power
V5_VREF--PCI 5V TOLERANCE
*:reserve
USB_PHY_1.2V--USB Phy
digital power
AVDDCK--USB Analog PLL power
AVDDCK_1.2--USB Phy
digital power
AVDDCK_3.3--Analog
system PLL power

Quanta Computer Inc.	
PROJECT : ZN1	
Size	Document Number: SB700-PWR/DECOUPLING 4/4
Rev	1A
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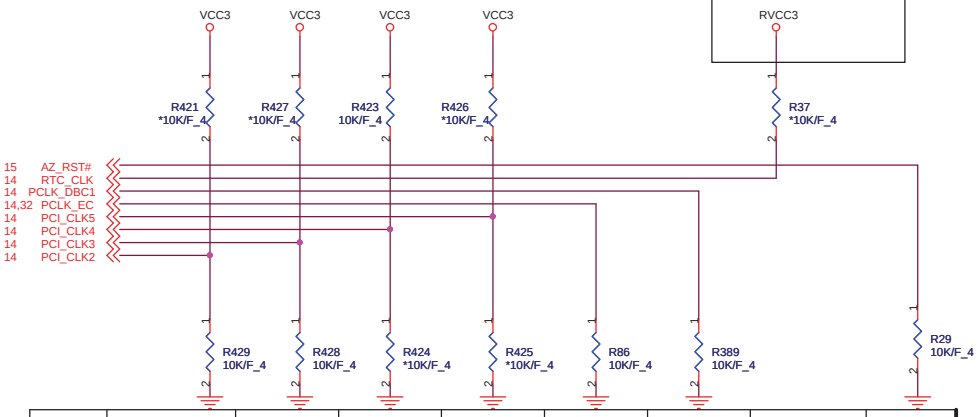
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

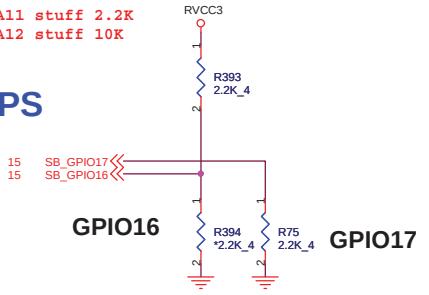
It must ready refore RSMRST#



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT
					EC ENABLED			ENABLE PCI MEM BOOT

REQUIRED STRAPS

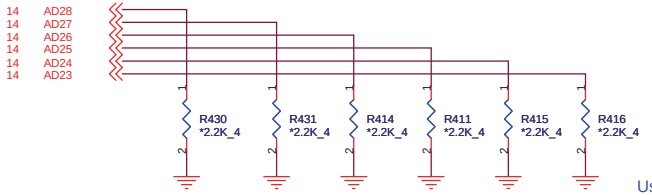
A11 stuff 2.2K
A12 stuff 10K



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

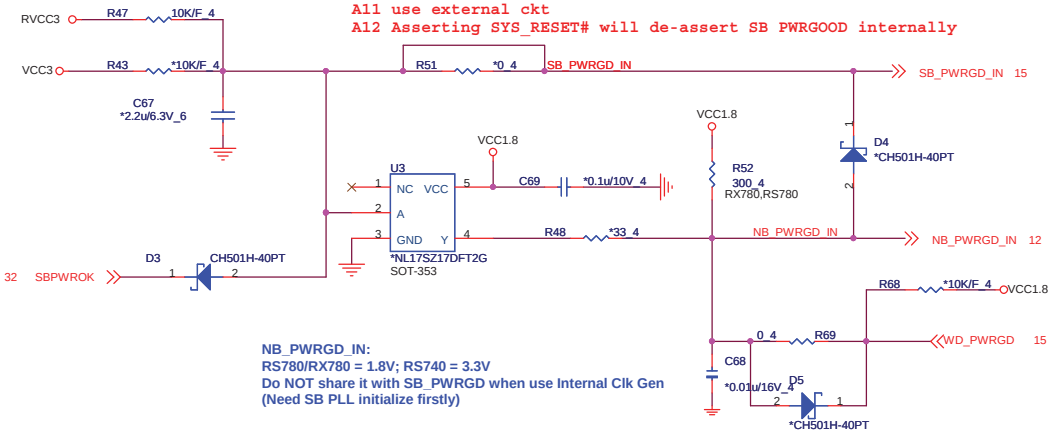
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally



NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

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PROJECT : ZN1

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	SB700-STRAPS	1A
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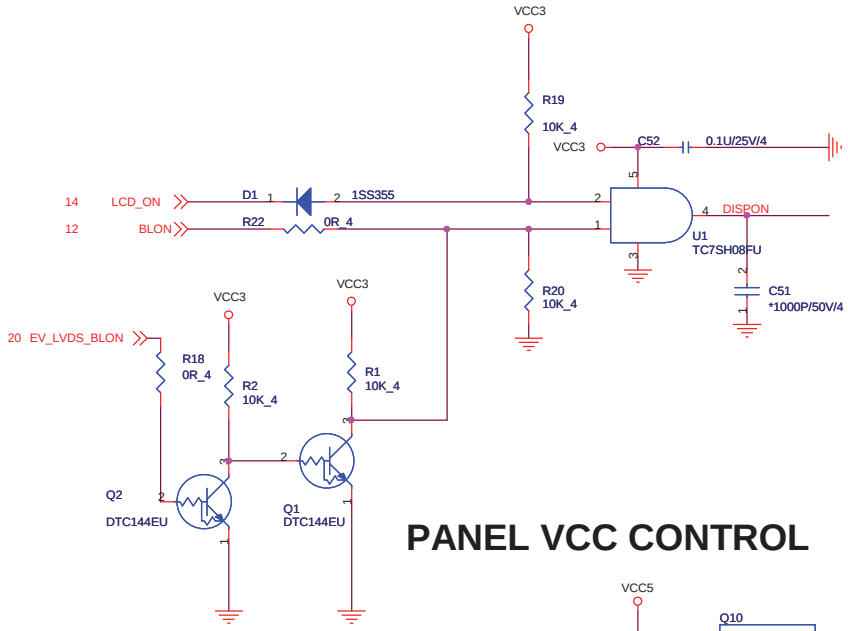
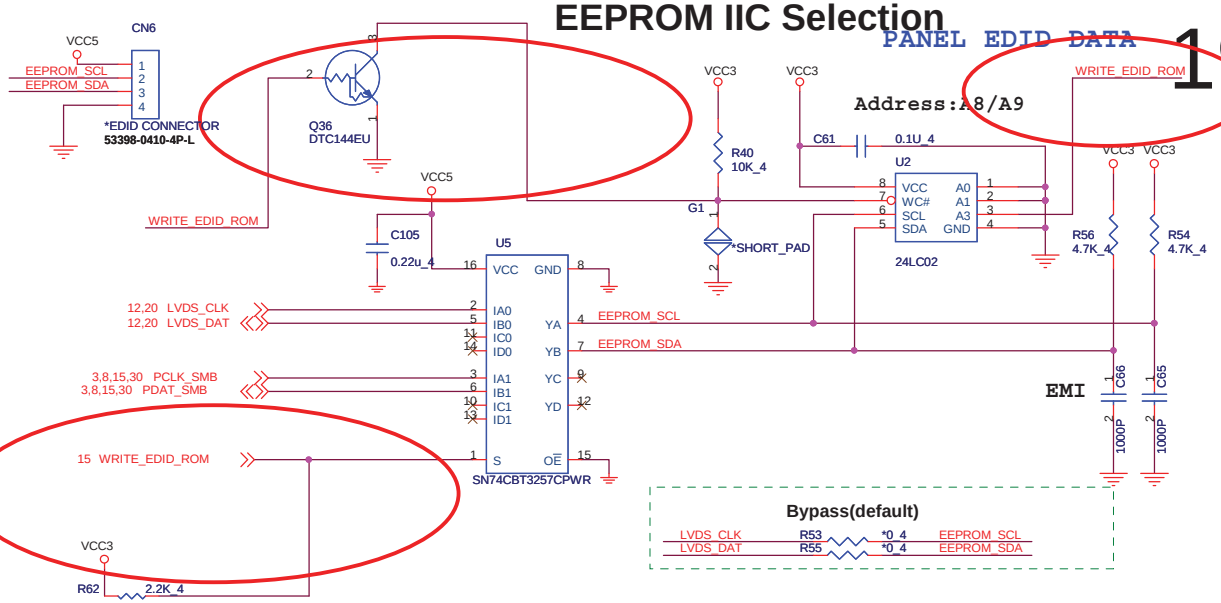
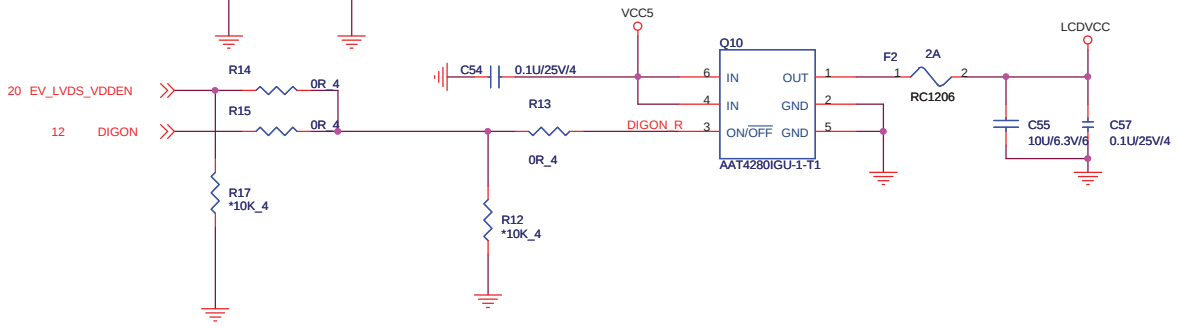
BACKLIGHT CONTROL



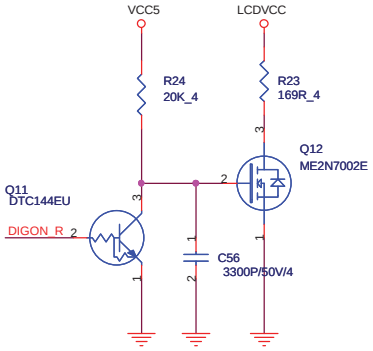
EEPROM IIC Selection



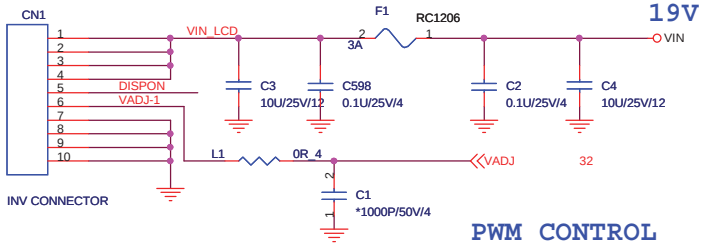
PANEL VCC CONTROL



Discharge panel power

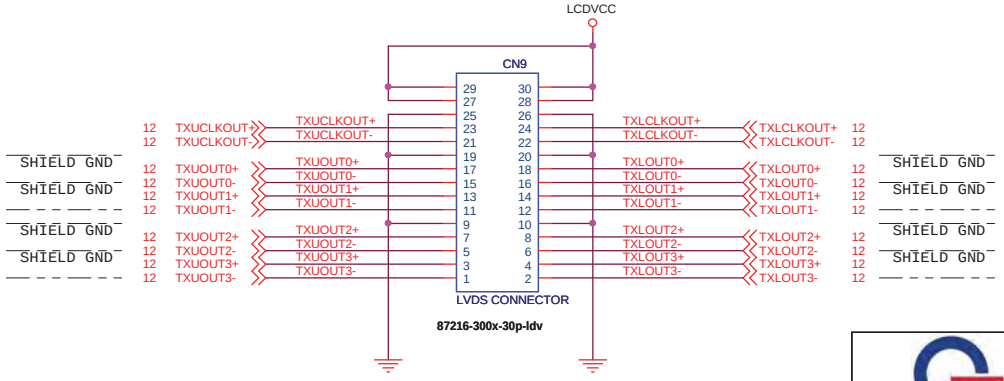


TO INVERTER POWER



PWM CONTROL

LCD PANEL CONNECTOR



Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	LCD PANEL/WEBCAM	A
Date: Friday, May 08, 2009	Sheet 19 of 41	

MXM Module

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

update MXM footprint to mxm-mm70-314-310b1-1-270p

MXM3.0 Signal Table

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

MXM Reset

SMBus

MXM VIN Power switch

MAINON	Behavior
Low	Enable dGPU PWR
High	Disable dGPU PWR

MXM 3V/5V Power switch

LCD PANEL CONNECTOR(WITH MXM)

pin28 connect to LCDVCC

Change BOM value

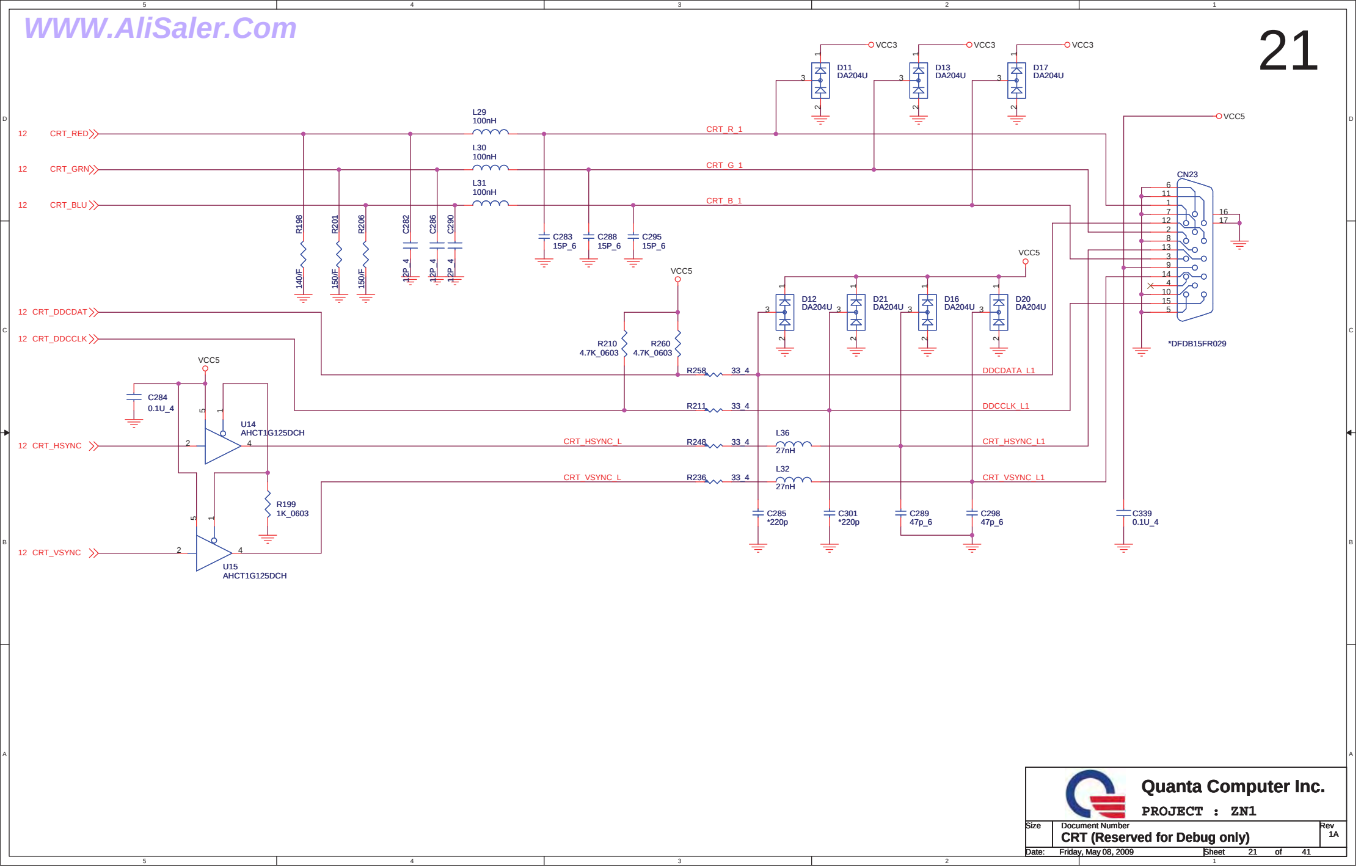
To low power status mode

Quanta Computer Inc.

PROJECT : ZN1

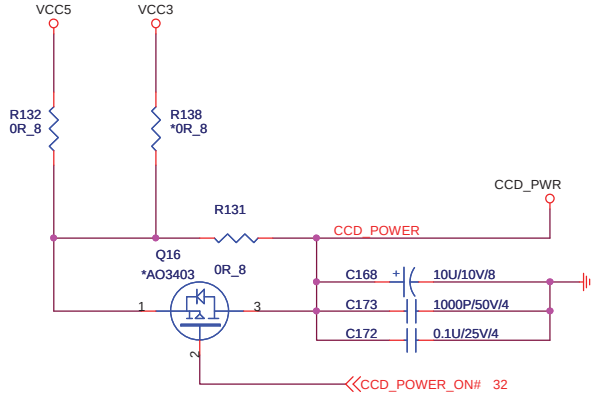
Size	Document Number	Rev
	MXM3.0	3B

Date: Friday, May 08, 2009 Sheet 20 of 41

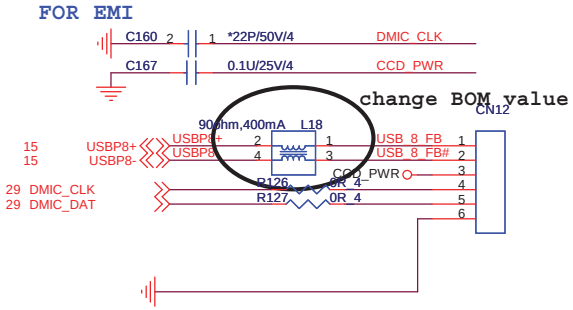


Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: CRT (Reserved for Debug only)	Rev: 1A
Date: Friday, May 08, 2009	Sheet 21 of 41	

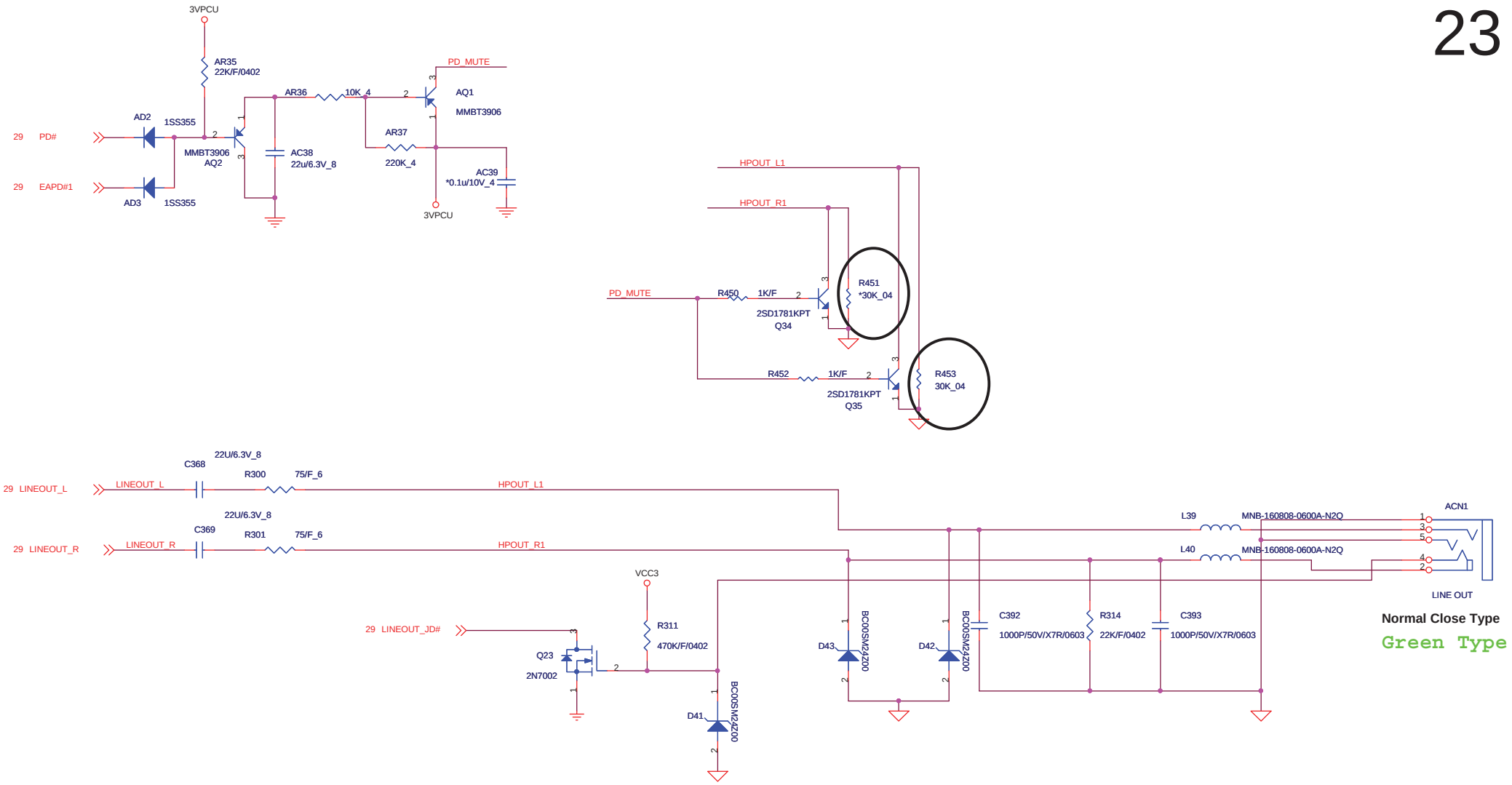
CAMERA POWER CONTROL



TO WEB CAM MODULE



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: WEBCAM	Rev: 1A
Date: Friday, May 08, 2009	Sheet 22 of 41	



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: Line Out	Rev: 1A
Date: Friday, May 08, 2009	Sheet 23 of 41	

LAN Power

RVCC3

Delete Q26,C475

R447
*short0603

LANVCC

WIDE TRACE

change L value to 0 in 8103EL

C192 .1U/10V/X5R_4
C194 22U/6.3V/X5R_8

LANVCC

R154 *0_8
R153 *0_8@NC

R341 2.49K/F_4

CTRL12A

XTAL25
XTAL25_R R340 0_4 XTAL25_1
Y4 25MHZ
C447 33P/50V_4
C448 33P/50V/_4

U18 EC-A-01 RTL8103EL

Vender suggest

for 8103EL

R382 1K_4
U19 *AT93C46A(3.3V)
EECS LED1/EESK LED2/EEDI LED3/EEDO
CS SK DI DO VCC DC ORG GND
C562 *0.1U/16V/Y5V_4@NC
R378 3.6K_6 LANVCC

LED0 D53 1SS355 LAN_ACT# 25
LED1/EESK D54 1SS355 LAN_LINK# 25
LED3/EEDO R458 *0_6 R459 *0_6 LAN_LINK1# 25
VCC3

L49 0_8
C451 22U/6.3V/X5R_8
C452 .1U/10V/X5R_4
GND

EVDD12_R R366 *0_8 EVDD12
C536 1U/6.3V/X5R_4
C542 1U/6.3V/X5R_4
R342 *0_8

DVDD12
C189 *.1U/10V/X5R_4
C537 .1U/10V/X5R_4
C488 .1U/10V/X5R_4
C465 .1U/10V/X5R_4
C498 .1U/10V/X5R_4

for 8103EL

LANVCC
C464 .1U/10V/X5R_4
C484 .1U/10V/X5R_4
C463 .1U/10V/X5R_4
C511 .1U/10V/X5R_4

LAN0_MDI0+ LAN0_MDI0-
LAN0_MDI1+ LAN0_MDI1-
LAN0_MDI2+ LAN0_MDI2-
LAN0_MDI3+ LAN0_MDI3-

R364 1K_4
D55 RB501V-40 RT28 15
R360 15K_4

R350 0_4 PLTRST# 12,14,16,20,27,30
PCIE_WAKE# 15,30

R357 10K/F_4 LANVCC

LAN_REST# R355 *0_4 PLTRST_LAN# 16

ENERGY_DET 15

11 GPP_TX2P_LAN
11 GPP_TX2N_LAN
C539 .1U/10V/X5R_4
C540 .1U/10V/X5R_4
GPP_RX2N_LAN 11
GPP_RX2P_LAN 11

CLK_PCIE_LAN# 3
CLK_PCIE_LAN 3

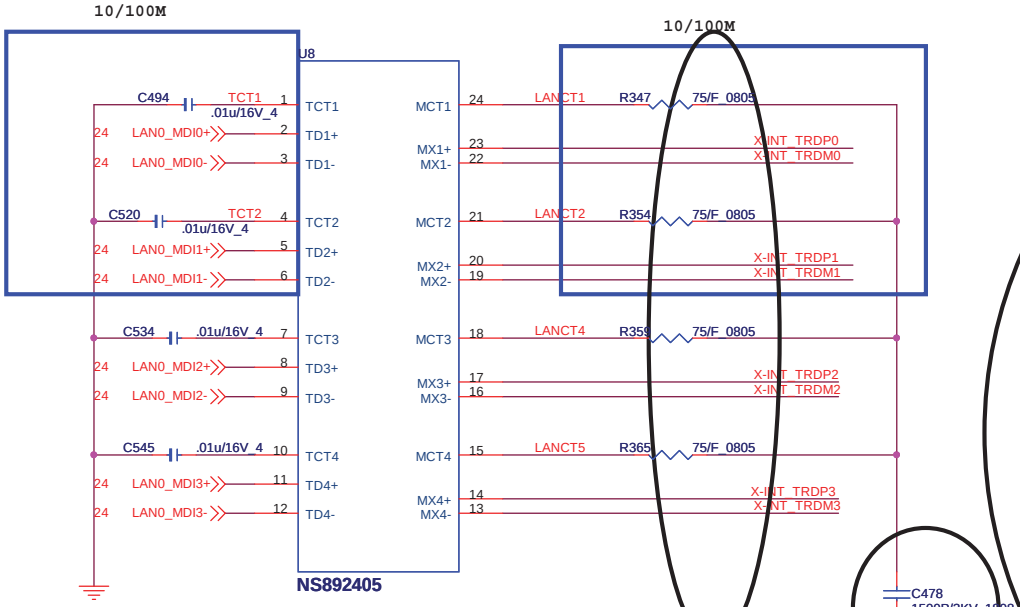
DVDD12
R148 0_8 CTRL12/VDD

Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	LAN RTL8111DL/RTL8103EL	1A

Date: Friday, May 08, 2009 Sheet 24 of 41

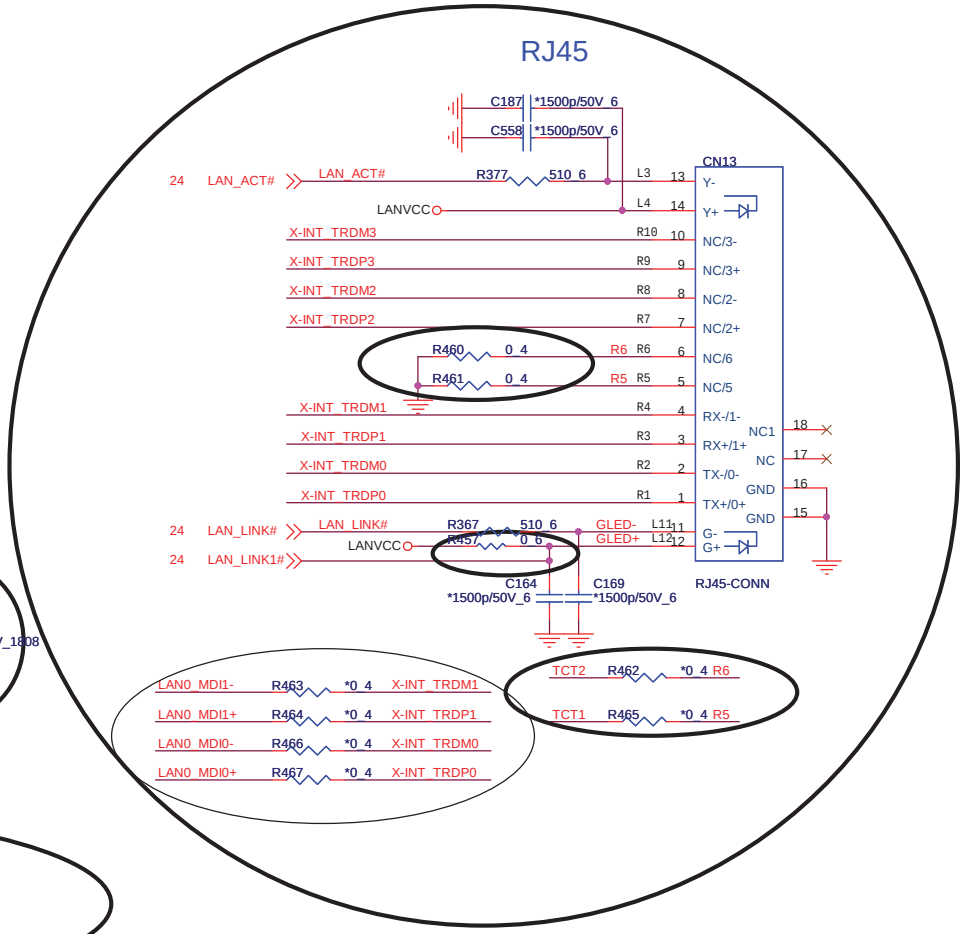
LAN Transformer & WIRE CONN to RJ45



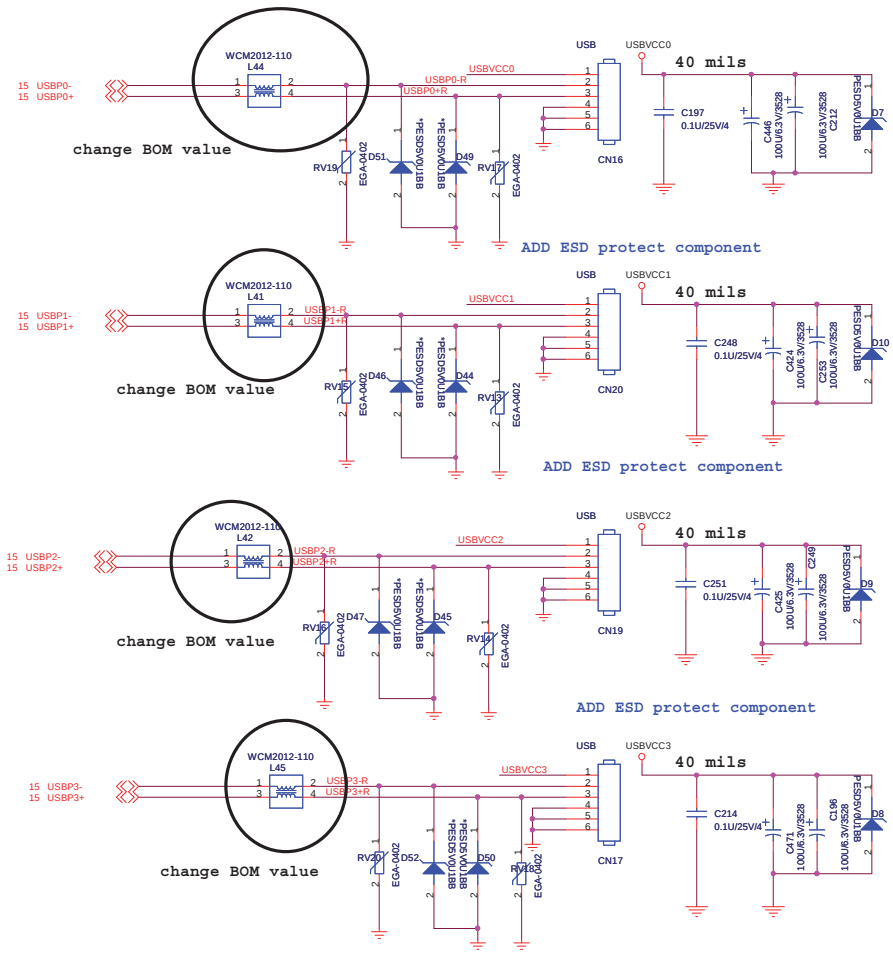
100/1000 Base T NS892402
10/100 Base T NS892405

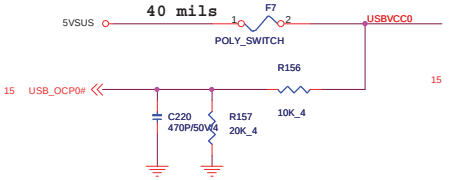
change the footprint and BOM

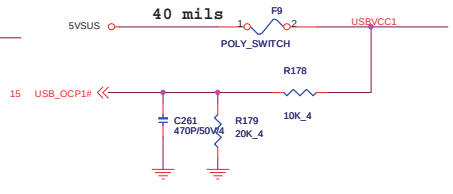
delete RV1-RV8

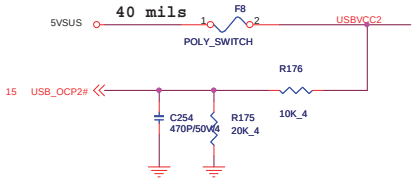


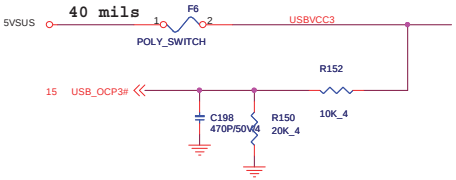
Quanta Computer Inc.	PROJECT : ZN1	
Size	Document Number: LAN Transformer & RJ45	Rev 1A
Date: Friday, May 08, 2009	Sheet 25 of 41	

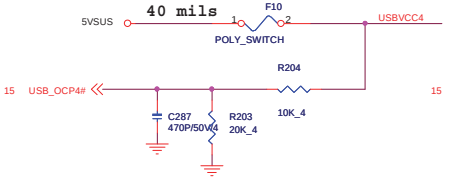


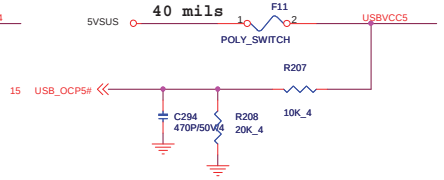


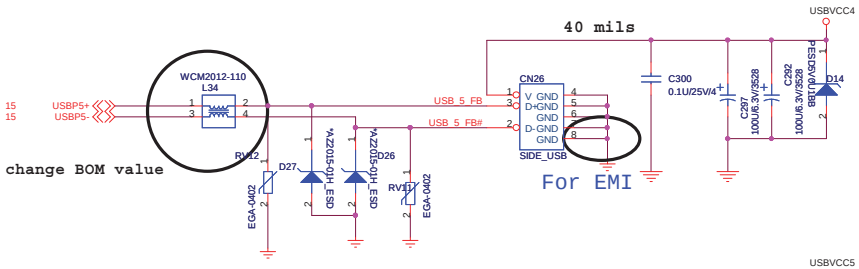


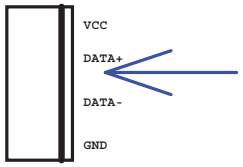


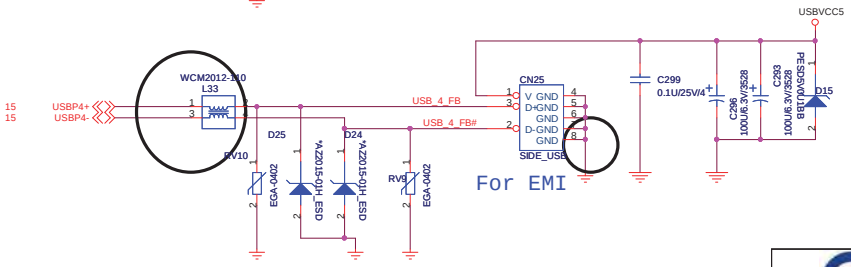












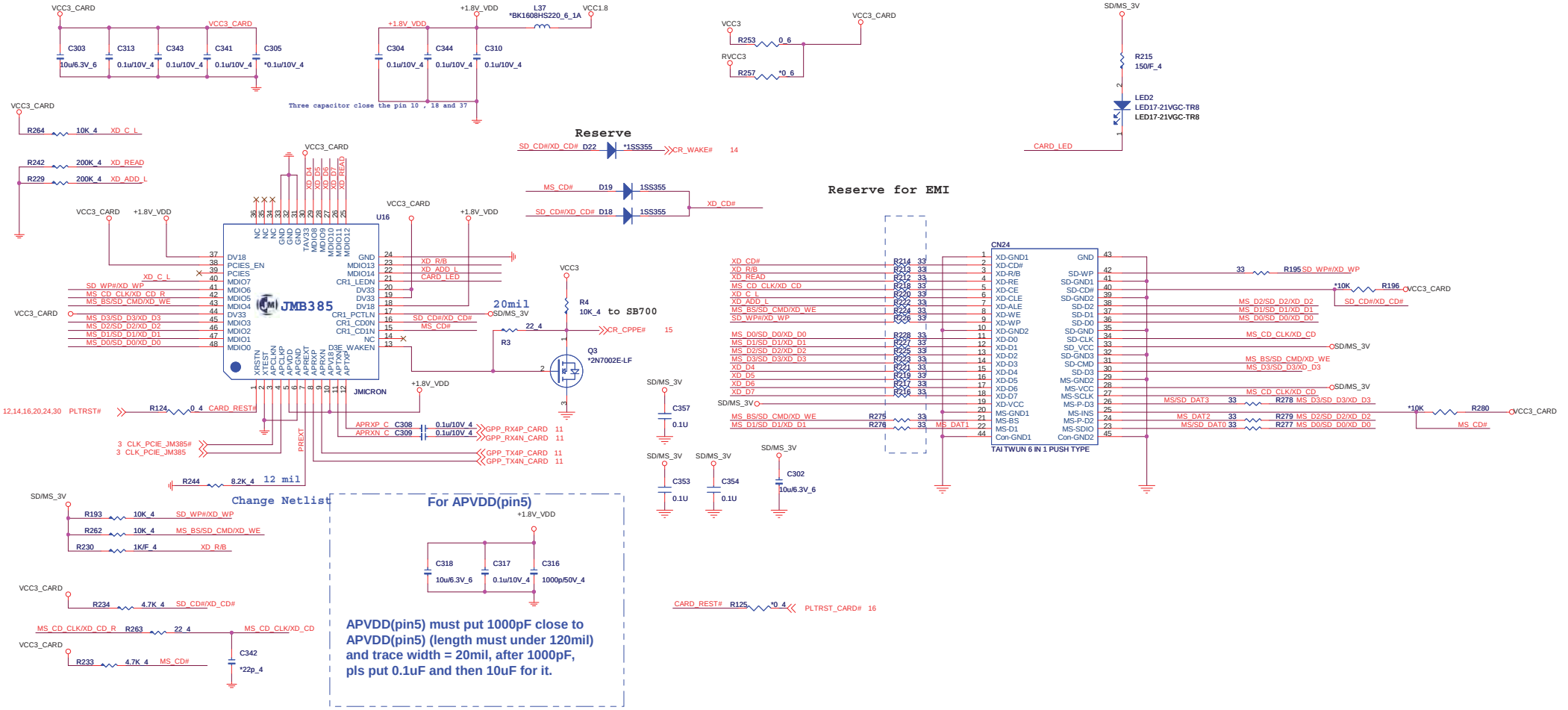
Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	USB Port X6	A

Date: Friday, May 08, 2009 Sheet 26 of 41

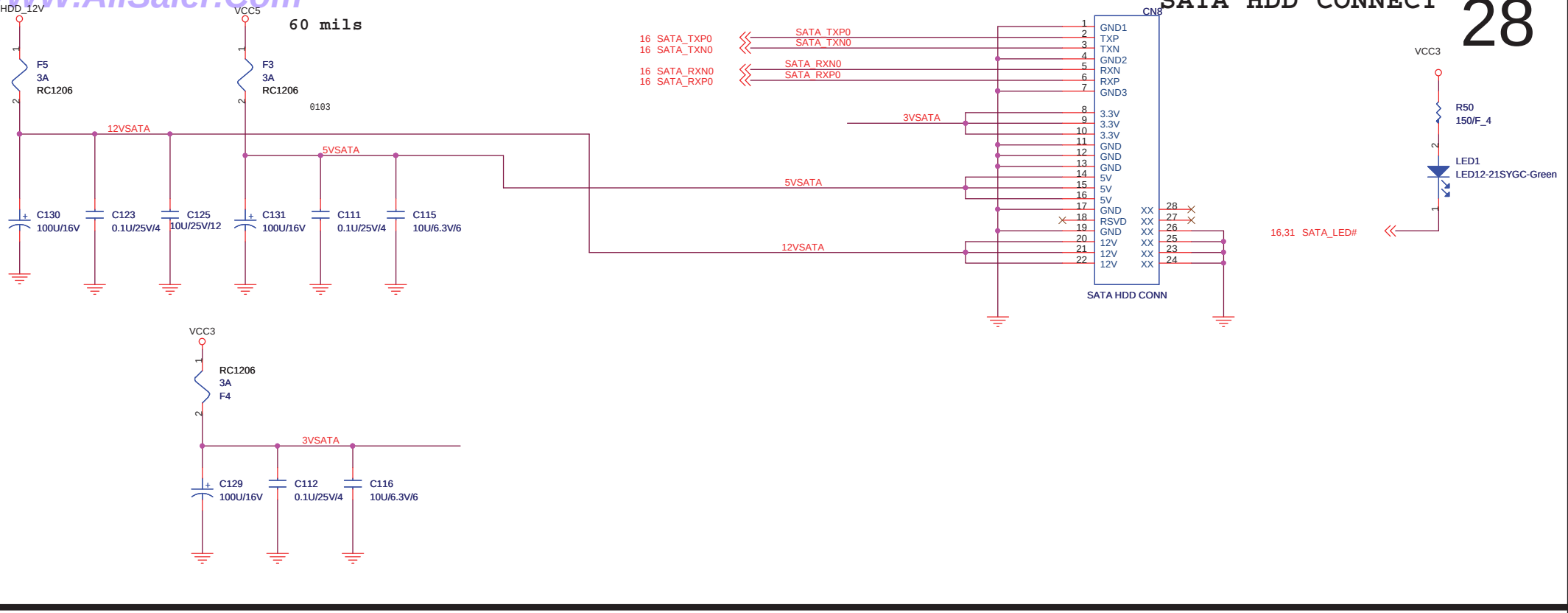
Memory Card Power Supply



Quanta Computer Inc.	PROJECT : ZN1	
Size	Document Number: Card Reader	Rev 1A
Date: Friday, May 08, 2009	Sheet 27 of 41	

SATA HDD CONNECT

28

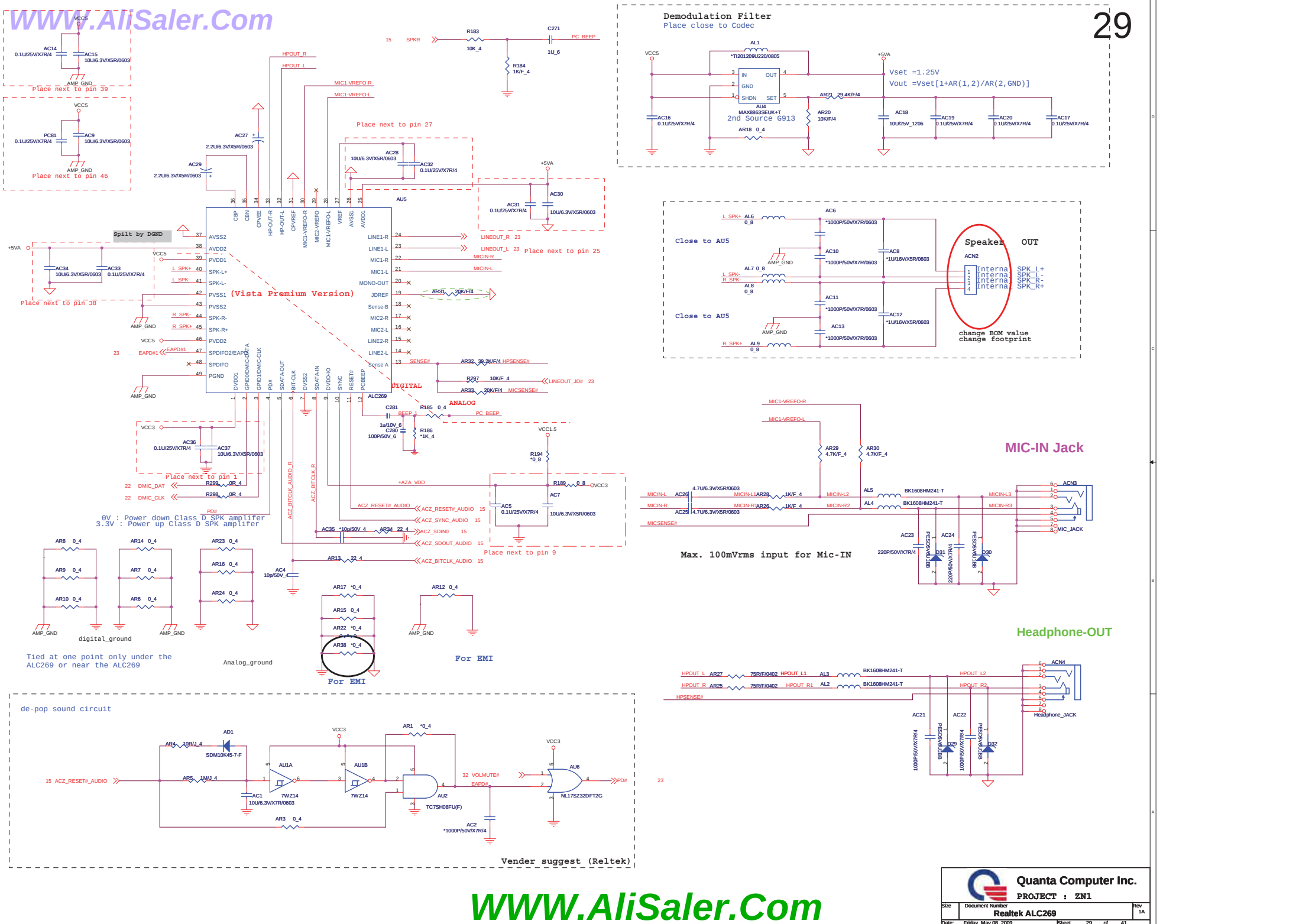


SATA ODD CONNECTOR

Quanta Computer Inc.

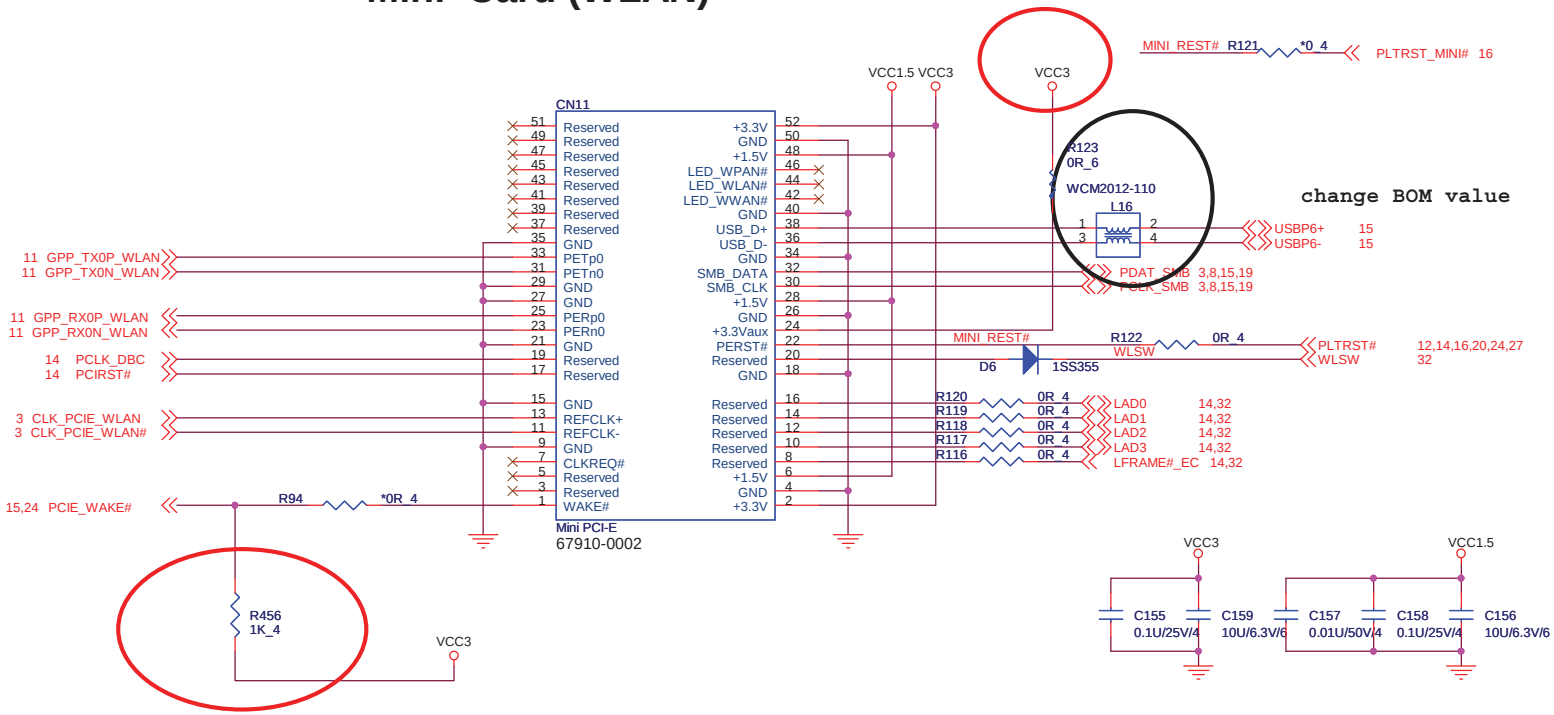
PROJECT : ZN1

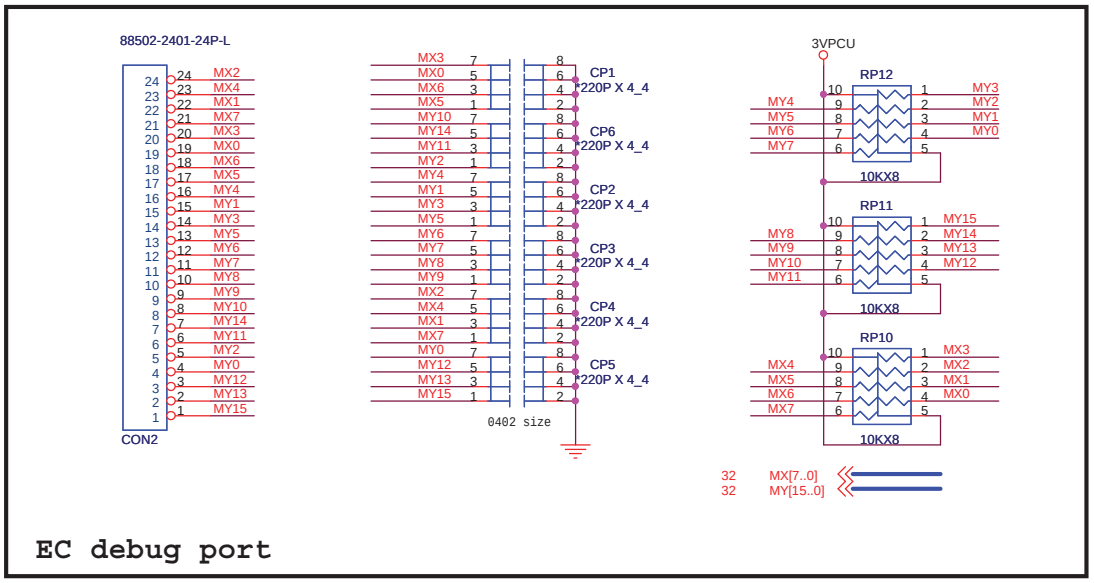
Size	Document Number	Rev
	SATA HDD/ODD	A
Date: Friday, May 08, 2009	Sheet 28 of 41	



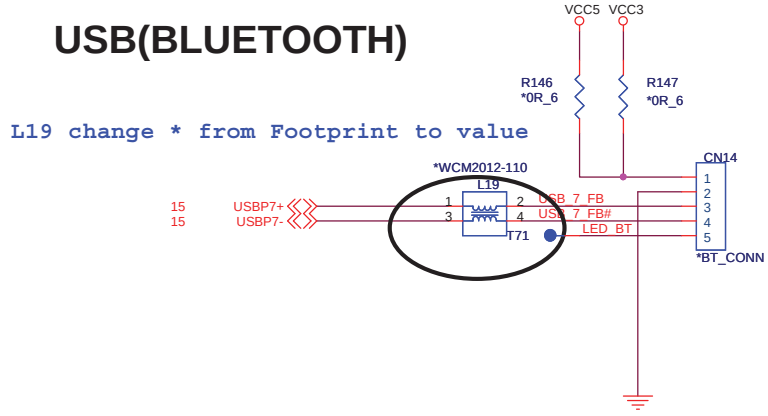
Quanta Computer Inc.			
PROJECT : ZN1			
Size	Document Number		Rev
	Realtek ALC269		1A
Date: Friday, May 08, 2009		Sheet 29 of 41	

Mini Card (WLAN)



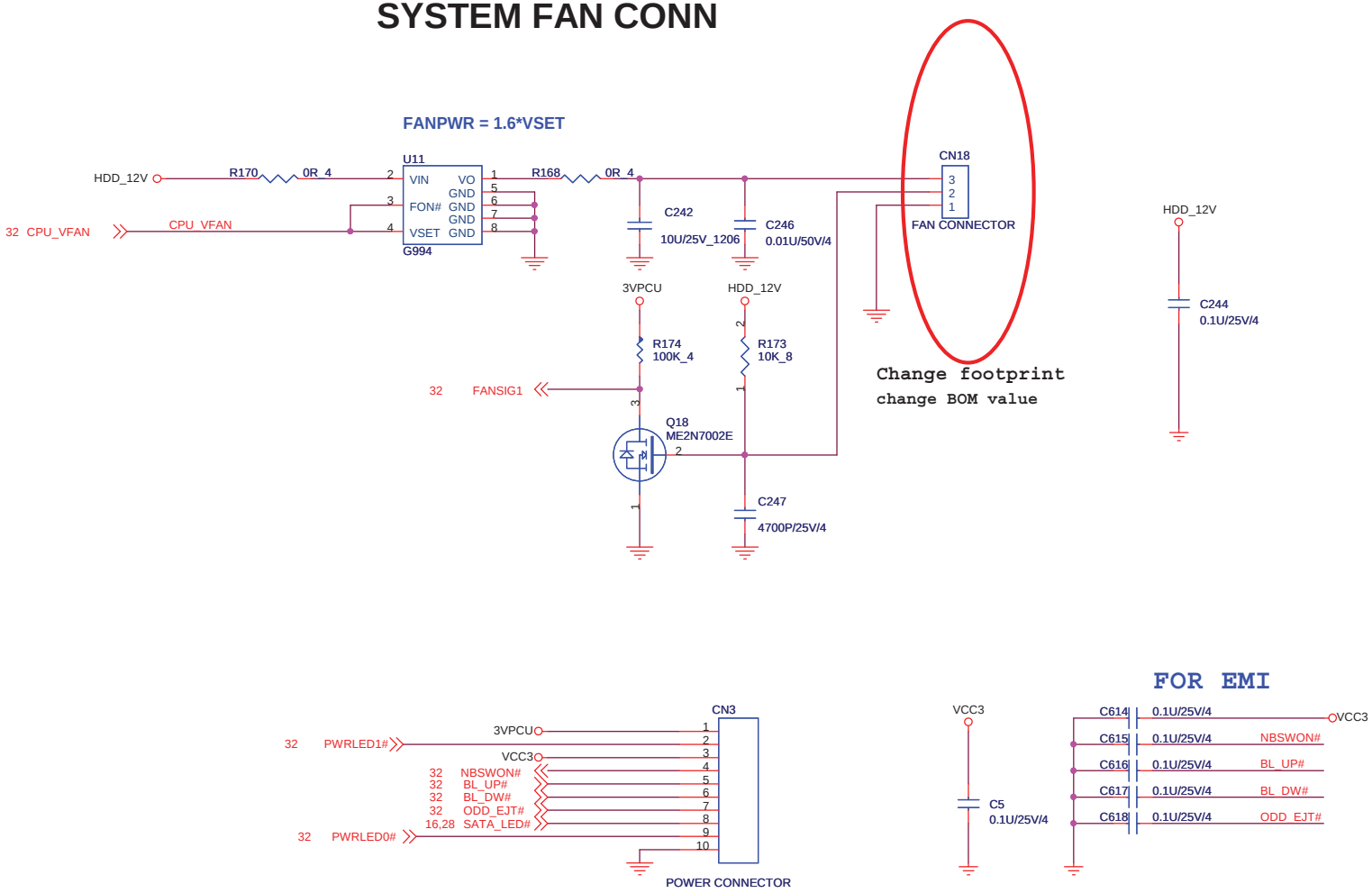


USB(BLUETOOTH)



Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: MINI CARD & BT	Rev: A
Date: Friday, May 08, 2009	Sheet 30 of 41	

SYSTEM FAN CONN



TO POWER BUTTON & LED LIGHT

Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: FAN	Rev: A
Date: Friday, May 08, 2009	Sheet 31 of 41	

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

(For PLL Power)

SMBUS

Pull Up for Low Active Pin

8Mbit , SPI

8M Winbond P/N:AKE3GZN0N00

SPI Socket P/N:DG008000031
A stage be use first

IT8512

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

IT8512 U17
AJ085120F03

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

Please reserve this connector for serial debug port & KBS download usage.

UART_TXD
UART_RXD

Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	EC ITE8512	1A

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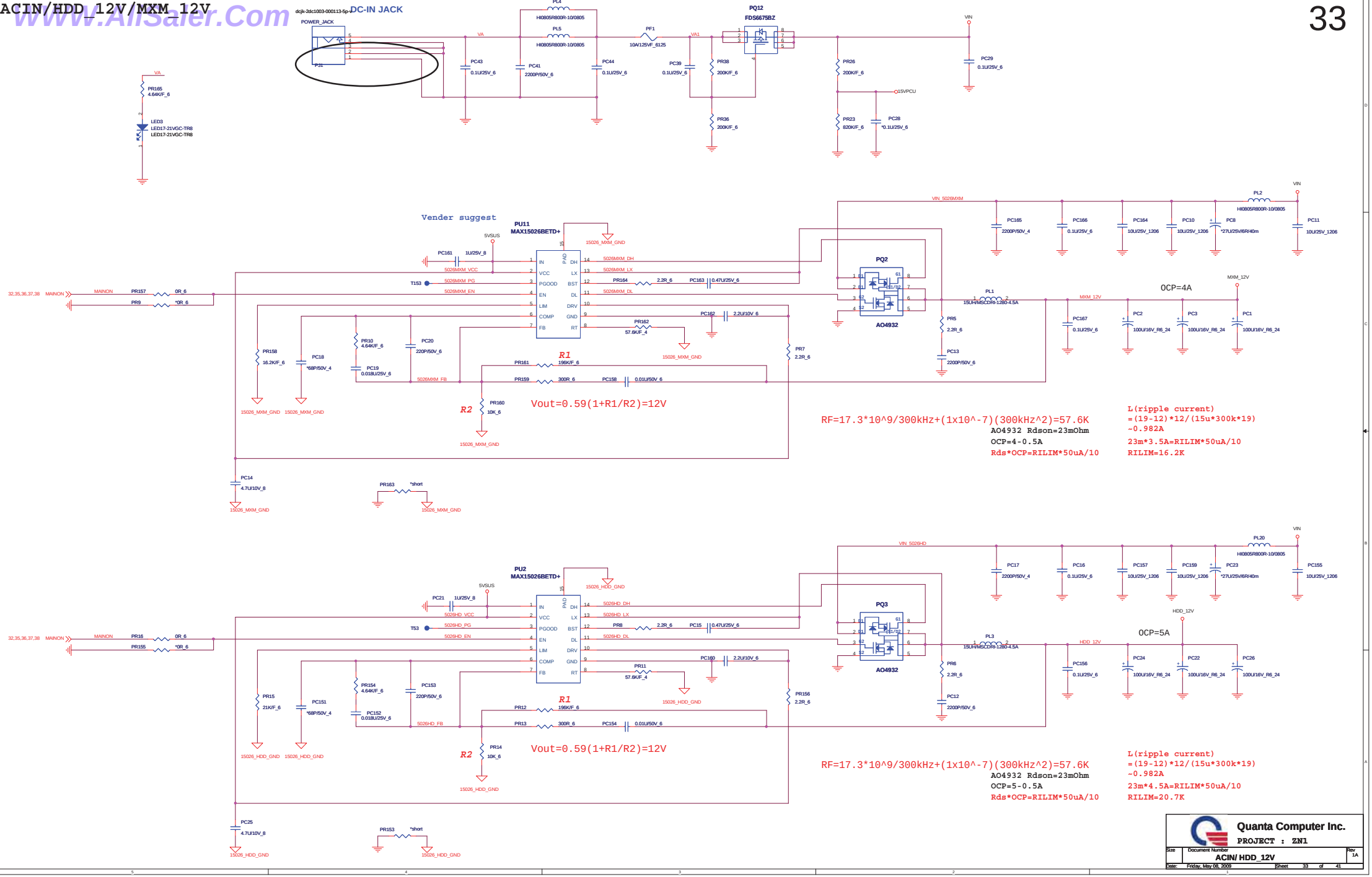
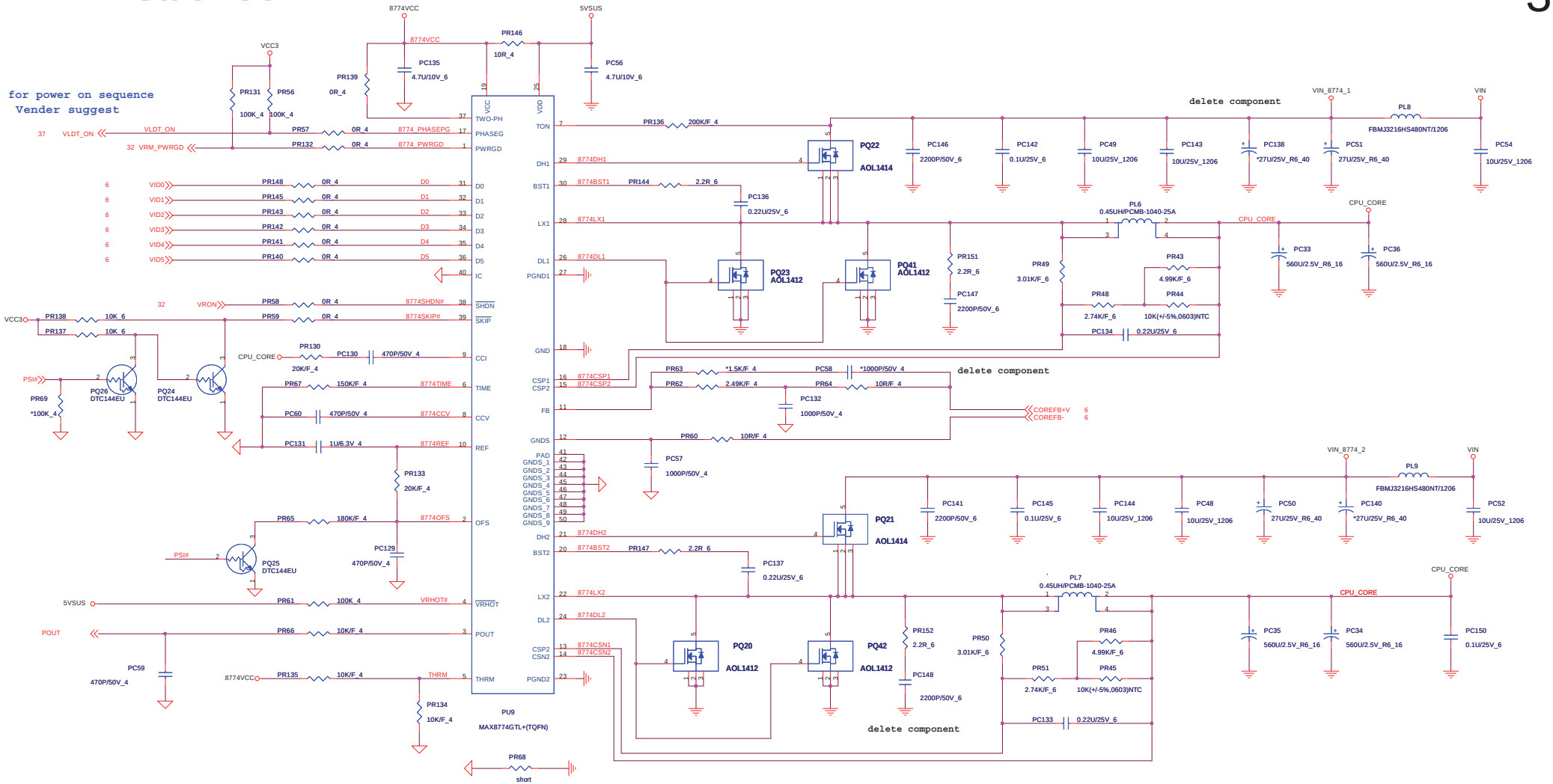


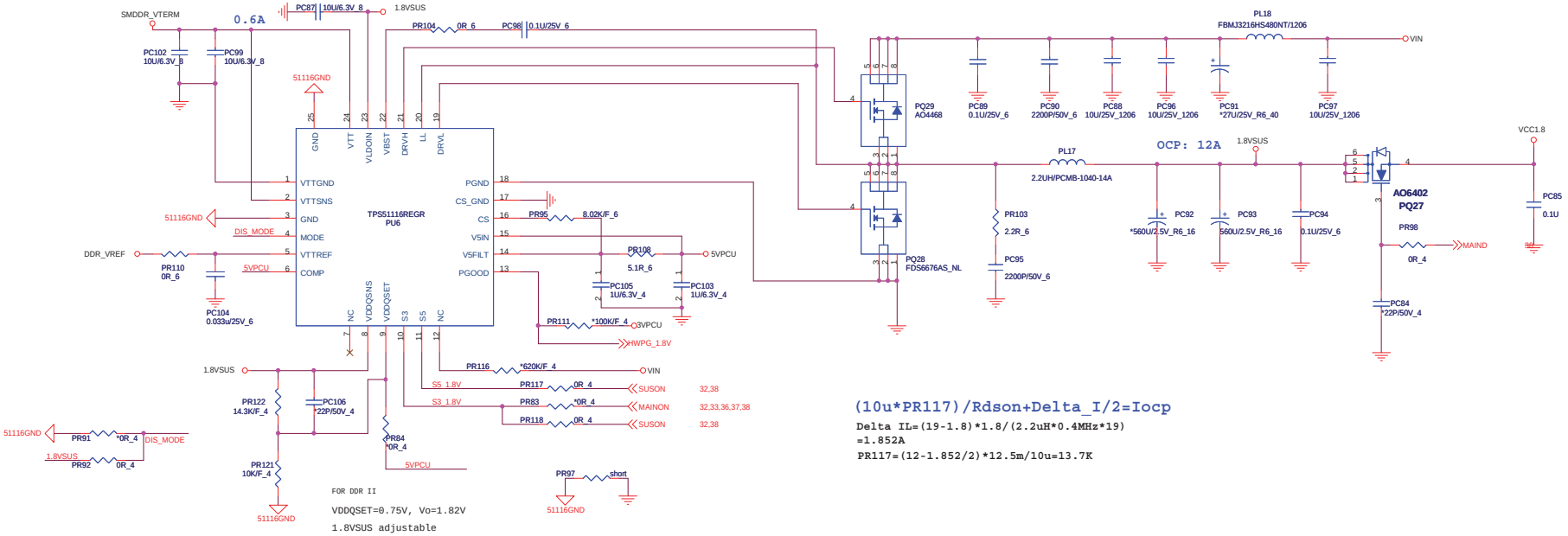
Quanta Computer Inc.		
PROJECT : ZN1		
Size	Document Number: ACIN/ HDD_12V	Rev: 1A
Date: Friday, May 08, 2009	Sheet 33 of 41	

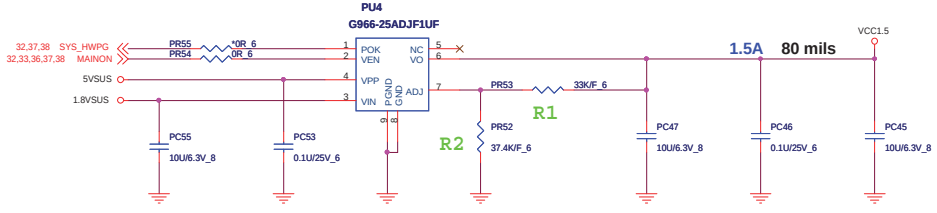
CPU_CORE and CPU_VDDNB_RUN



For AMD AM2 CORE

Quanta Computer Inc.	
PROJECT : ZN1	
Size	Document Number: CPU CORE(MAX8774) — Rev: 1A
Date: Friday, May 08, 2009	Sheet 34 of 41





Quanta Computer Inc.
PROJECT : ZN1

Size	Document Number	Rev
	DDR 1.8V(TPS51116&VTERM)	2B

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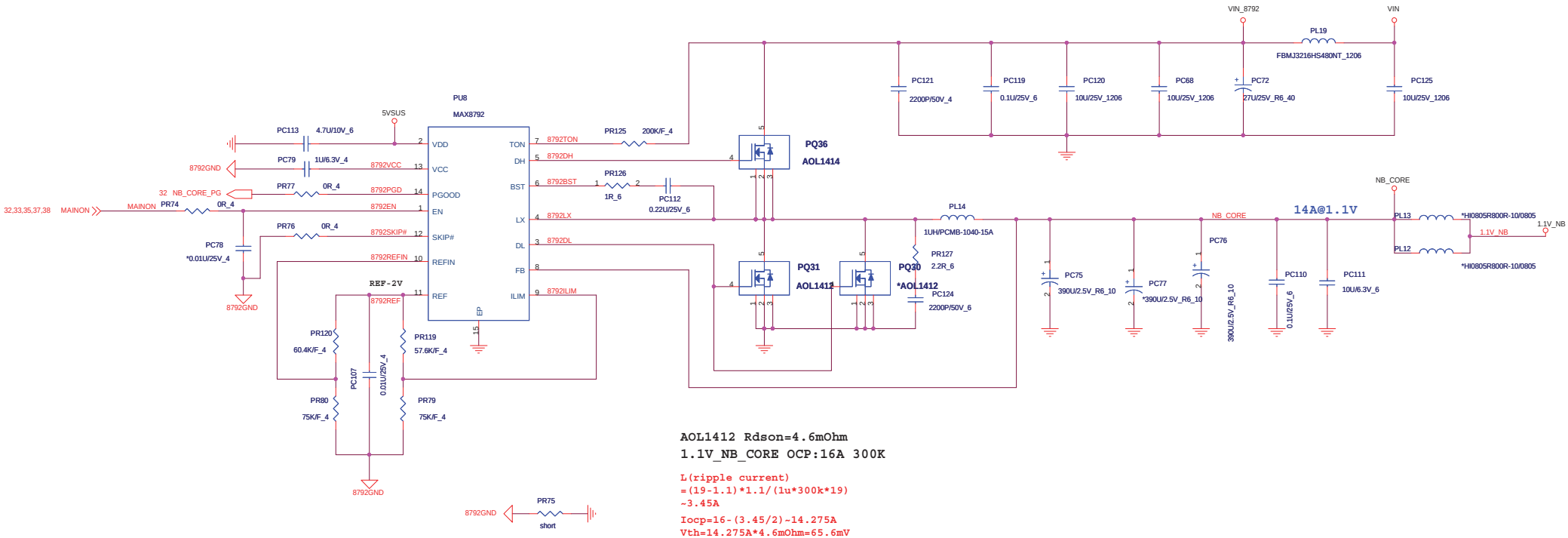


AOL1412 Rdson=4.6mOhm

1.1V_NB_CORE OCP:16A 300K

L(ripple current)
=(19-1.1)*1.1/(1u*300k*19)
~3.45A

Iocp=16-(3.45/2)~14.275A
Vth=14.275A*4.6mOhm=65.6mV

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	POWER_VGA_CORE	A

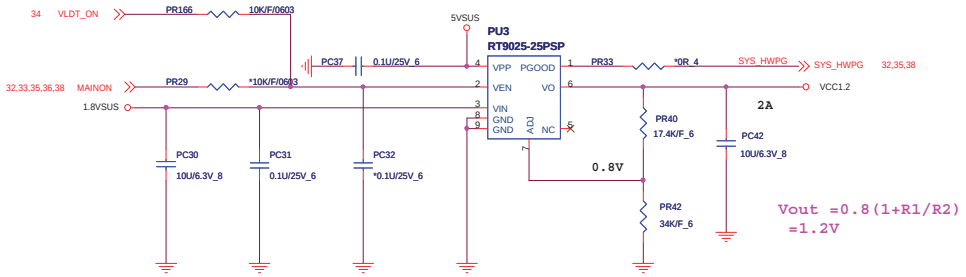
Date: Friday, May 08, 2009 Sheet 36 of 41

VCC1.2 & VCC1.2SB

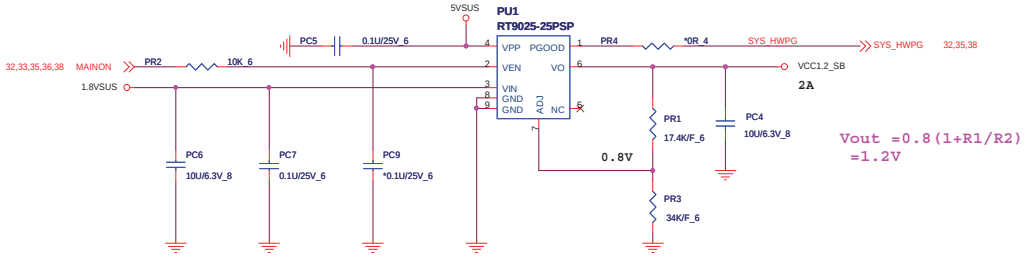
Change netlist for HT BUS power

Vender suggest

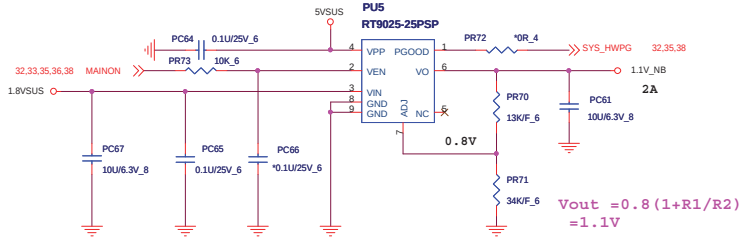
Colsed to CPU/NB



Colsed to SB



Colsed to NB



Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	VCC1.2	1A

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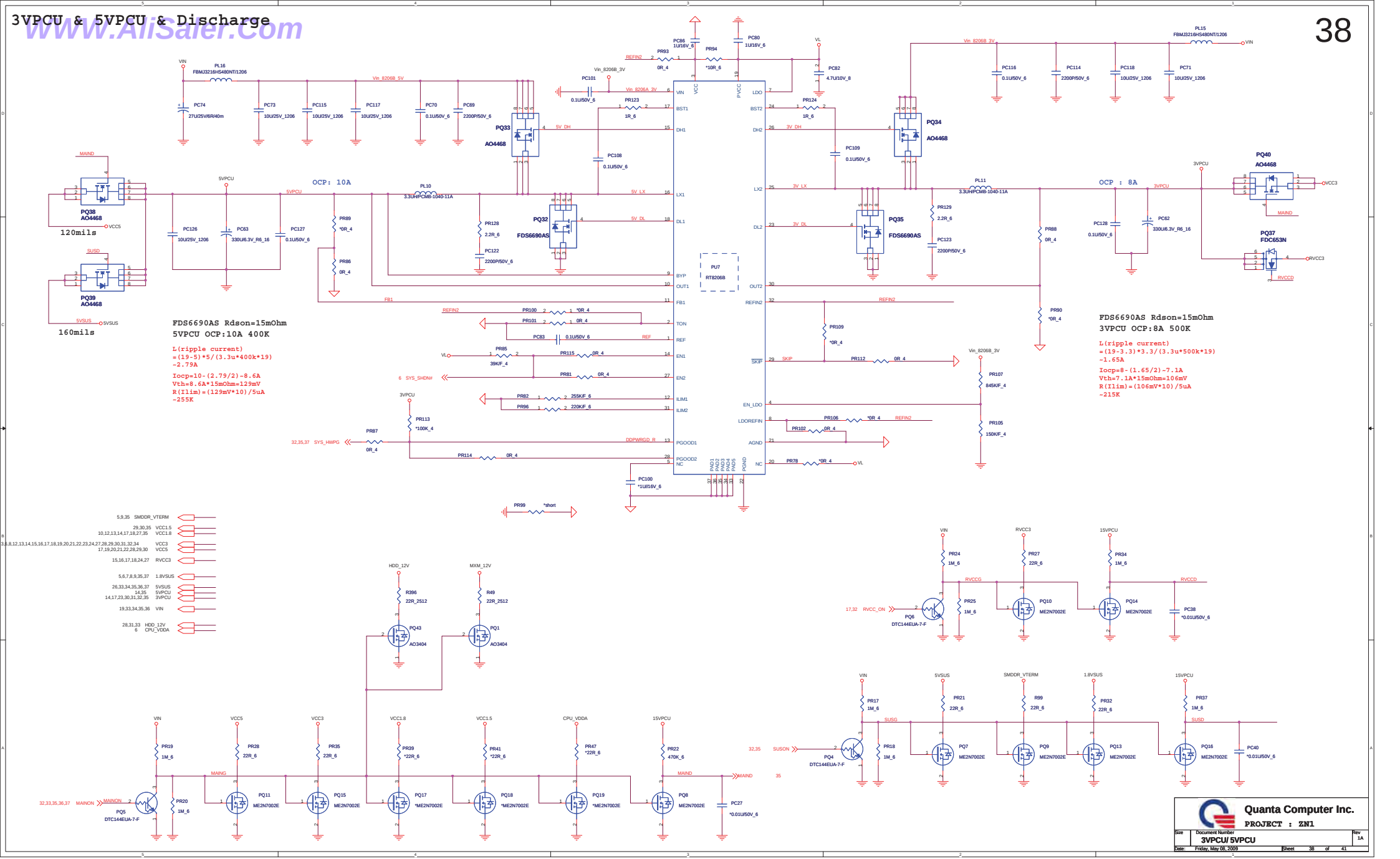
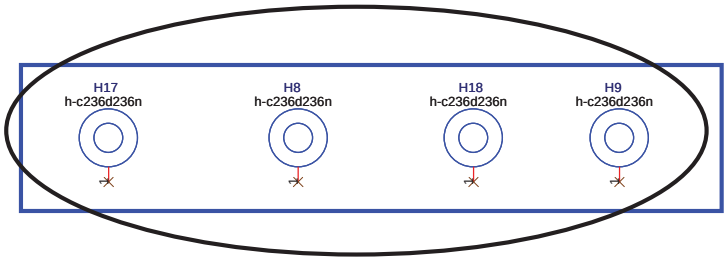
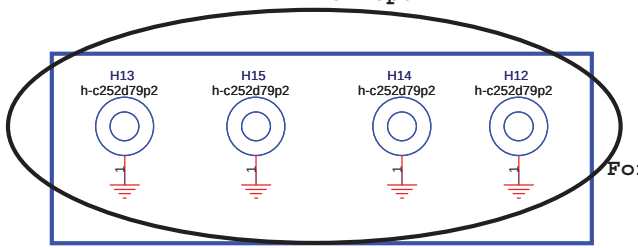
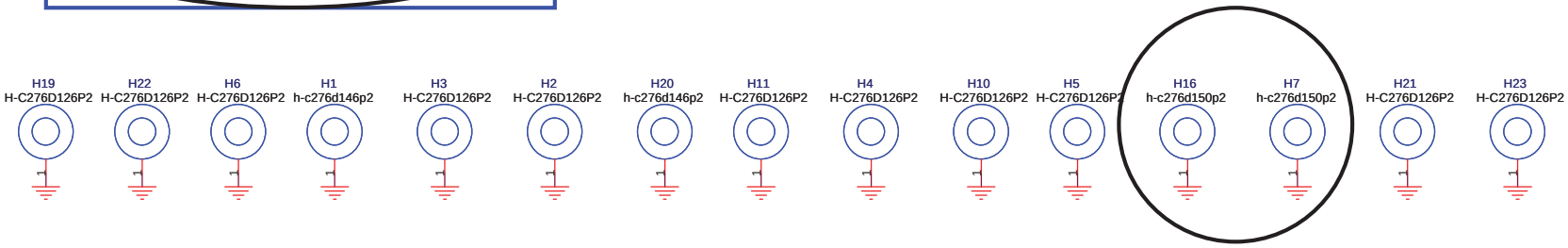




For cpu



For mini card



Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	SCREW HOLE & EMI	A
Date: Friday, May 08, 2009	Sheet 39 of 41	

DATE	Description	Note	Page
2009 0320	1.change RP1-RP9 to 47 ohm (AMD suggestion)----PAGE 3 2.add R448 10k to VCC3---PAGE 6 3.add R101 300ohm to 1.8VSUS---PAGE 6 4.add R449 10K ohm to VCC3---PAGE12 5.Reserve C612,C613,R441,Y6 to schmatic---page14 6.add D59 and R446 10k to VCC3---page14 7.add R455,C621,C622 to schmatic for EMI---page14 8.add write EDID rom net to control ---page15 9.delete R403 and R32 --page 15 10.change C91,c95 value to 33p---page 16 11.Add 2 short pin for clear cmos and clear password --page16 12.add R86 10k--page 18 13.delete D4,D5 ,C68 component and add R69 0ohm---page18 14.change netlist to SB control (write_edid _rom)and add R62 2.2k ohm--- page19 15.change Q8 control pin to main pin---page 20 16.change MXM reset from pltrst.---page20 17.add ine out mute function---page23 add component ar35,ar36,ar37,ac38,aq1,aq2,ad2,ad3,q34,q35,r450,r452--page23 18.delete Q26,c475 and change LANVCC net to RVCC3 to control ---page24 19.change C447,C448 to 33p---page 24 20.change CN13 footprint for LED pin change---page 25 21.add ESD protect RV17,RV19,RV13,RV15,RV14,RV16, RV18,RV20,RV9,RV10,RV11,RV12---PAGE 26 22.Change CN25,CN26 footprint for ME---page26 23.add D18,D19 for XD detect and change net SD_WP#/XD_WP for SD write protect ---page27 24.change LED2 to Green type---page 27 25.change CN8 to rightangle and change odd connect to vertical type for ME---page 28 26.change au6 to OR-gate from AND-gate for pop sound---page 29 27.change fan control net from Vender suggestion.---page 31 28.add c614--618 0.1u for EMI--- page 31 29.add pr165 ,led3 for power line in ---page33 30.change VLDT_ON net for power on sequence--PAGE 34 31.change pr137,pr138 type to BOM---page 34	B2B	
	33.LED RT value need to change		

Quanta Computer Inc.

PROJECT : ZN1

Size	Document Number	Rev
	CHANGE LIST	C

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DATE	ZN1 Board file	ZN1 Schematic
11th Mar. 2009	ZN1-0311-17-152.brd	AH1_A_FEB23_01.DSN
31th Mar. 2009	ZN1-0325-1830.brd	ZN1_B_HP_MAR31.DSN

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PROJECT : ZN1

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