

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

TV_OUT
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

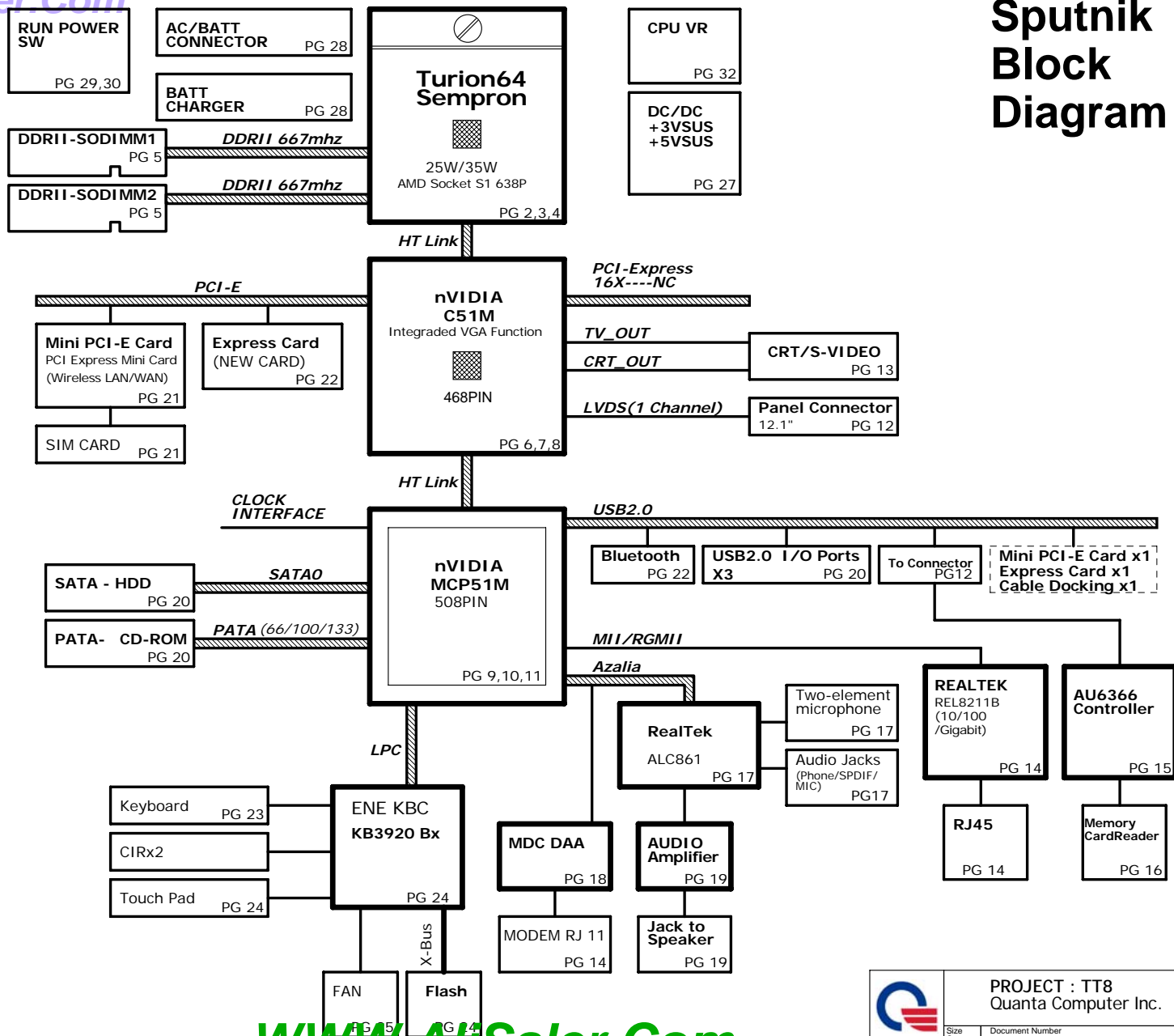
PG 25

VAULE DEFINE

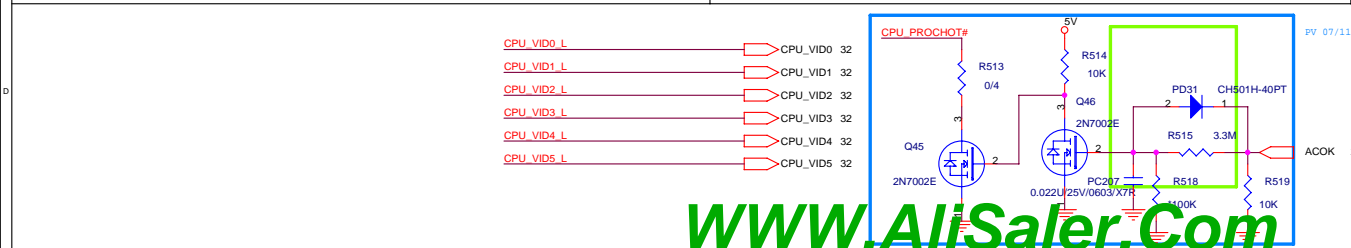
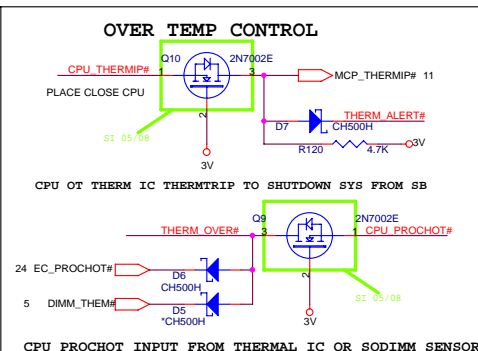
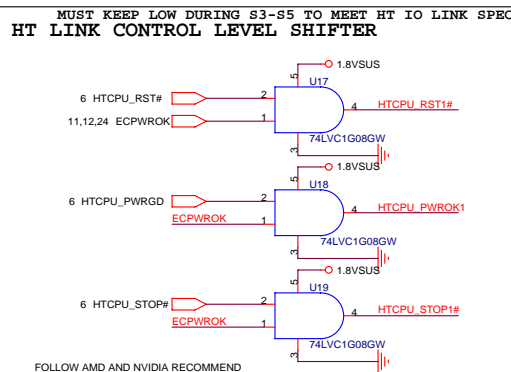
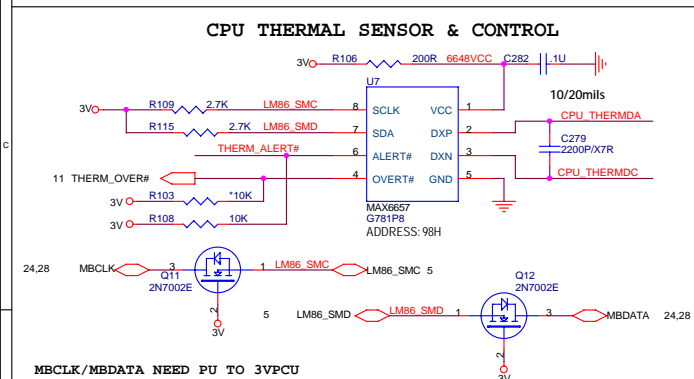
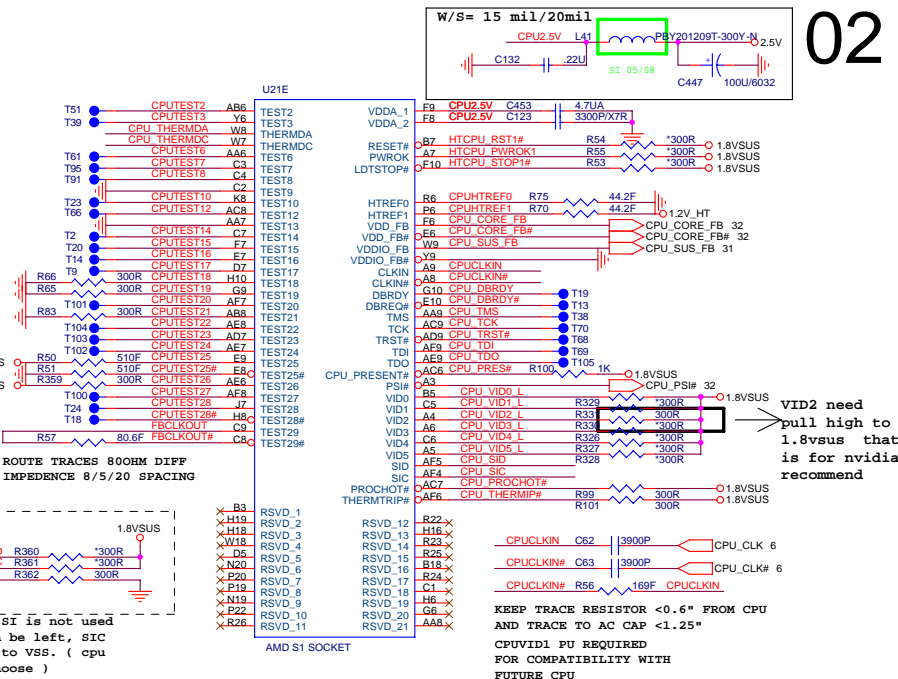
A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)



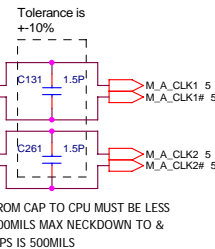
Sputnik Block Diagram



U21B	
M A D063 AA12	MA_DATA[63]
M A D062 AB12	MA_DATA[62]
M A D061 AA14	MA_DATA[61]
M A D060 AB14	MA_DATA[60]
M A D059 W11	MA_DATA[59]
M A D058 Y12	MA_DATA[58]
M A D057 AD13	MA_DATA[57]
M A D056 AB13	MA_DATA[56]
M A D055 AD15	MA_DATA[55]
M A D054 AB15	MA_DATA[54]
M A D053 Y17	MA_DATA[53]
M A D052 Y14	MA_DATA[52]
M A D051 W14	MA_DATA[51]
M A D049 W16	MA_DATA[50]
M A D048 AD17	MA_DATA[49]
M A D047 Y18	MA_DATA[48]
M A D046 AD19	MA_DATA[47]
M A D045 AD21	MA_DATA[46]
M A D044 AB21	MA_DATA[45]
M A D043 AB18	MA_DATA[44]
M A D042 AA18	MA_DATA[43]
M A D041 AA20	MA_DATA[42]
M A D040 Y20	MA_DATA[41]
M A D038 Y22	MA_DATA[40]
M A D037 W21	MA_DATA[39]
M A D036 W22	MA_DATA[38]
M A D035 AA21	MA_DATA[37]
M A D034 AB22	MA_DATA[36]
M A D033 AB24	MA_DATA[35]
M A D032 Y24	MA_DATA[34]
M A D031 H22	MA_DATA[33]
M A D030 H20	MA_DATA[32]
M A D029 E22	MA_DATA[31]
M A D028 E21	MA_DATA[30]
M A D027 H19	MA_DATA[29]
M A D026 H24	MA_DATA[28]
M A D025 E20	MA_DATA[27]
M A D024 F20	MA_DATA[26]
M A D023 C23	MA_DATA[25]
M A D022 B22	MA_DATA[24]
M A D021 E18	MA_DATA[23]
M A D020 E18	MA_DATA[22]
M A D019 E20	MA_DATA[21]
M A D018 D22	MA_DATA[20]
M A D017 C19	MA_DATA[19]
M A D016 G18	MA_DATA[18]
M A D015 G17	MA_DATA[17]
M A D014 C17	MA_DATA[16]
M A D013 F14	MA_DATA[15]
M A D012 E14	MA_DATA[14]
M A D011 H17	MA_DATA[13]
M A D010 H17	MA_DATA[12]
M A D09 E15	MA_DATA[11]
M A D08 H15	MA_DATA[10]
M A D07 E13	MA_DATA[9]
M A D06 C13	MA_DATA[8]
M A D05 H12	MA_DATA[7]
M A D04 H11	MA_DATA[6]
M A D03 G14	MA_DATA[5]
M A D02 H14	MA_DATA[4]
M A D01 F12	MA_DATA[3]
M A D00 G12	MA_DATA[2]
M A A15 K19	MA_ADD[15]
M A A14 K20	MA_ADD[14]
M A A13 V24	MA_ADD[13]
M A A12 K24	MA_ADD[12]
M A A11 L20	MA_ADD[11]
M A A10 R19	MA_ADD[10]
M A A9 L19	MA_ADD[9]
M A A8 L22	MA_ADD[8]
M A A7 L21	MA_ADD[7]
M A A6 M19	MA_ADD[6]
M A A5 M20	MA_ADD[5]
M A A4 M22	MA_ADD[4]
M A A3 M22	MA_ADD[3]
M A A2 N22	MA_ADD[2]
M A A1 N21	MA_ADD[1]
M A A0 R21	MA_ADD[0]

AMD S1 SOCKET

U21C	
Y13 M A DQM7	MA_DATA[63]
AB16 M A DQM6	MA_DATA[62]
Y19 M A DQM5	MA_DATA[61]
AC24 M A DQM4	MA_DATA[60]
F24 M A DQM3	MA_DATA[59]
E19 M A DQM2	MA_DATA[58]
C15 M A DQM1	MA_DATA[57]
E12 M A DQM0	MA_DATA[56]
W12 M A DQST7	MA_DATA[55]
Y15 M A DQST6	MA_DATA[54]
AB19 M A DQST5	MA_DATA[53]
AD23 M A DQST4	MA_DATA[52]
G22 M A DQST3	MA_DATA[51]
C22 M A DQST2	MA_DATA[50]
G16 M A DQST1	MA_DATA[49]
G13 M A DQST0	MA_DATA[48]
W13 M A DQST7	MA_DATA[47]
CW15 M A DQST6	MA_DATA[46]
CA20 M A DQST5	MA_DATA[45]
CA23 M A DQST4	MA_DATA[44]
G21 M A DQST3	MA_DATA[43]
C21 M A DQST2	MA_DATA[42]
G15 M A DQST1	MA_DATA[41]
H13 M A DQST0	MA_DATA[40]
E16 M A CK1	MAO_CLK[1]
E16 M A CK1#	MAO_CLK[1]
Y16 M A CK2	MAO_CLK[2]
AA16 M A CK2#	MAO_CLK[2]
K22 M A BA2	MA_BANK[2]
R20 M A BA1	MA_BANK[1]
T22 M A BA0	MA_BANK[0]
C220 M A RAS#	MA_RAS#
U220 M A CAS#	MA_CAS#
U221 M A WE#	MA_WE#
CY19 M A CS#0	MAO_CS#0
CJ22 M A CS#2	MAO_CS#2
V222 M A CS#1	MAO_CS#1
CY19 M A CS#0	MAO_CS#0
J20 M A CKE1	MA_CKE[1]
J21 M A CKE0	MA_CKE[0]
V20 M A ODT1	MAO_ODT[0]
U19 M A ODT0	MAO_ODT[0]

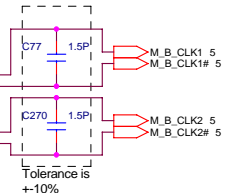


U21C	
M B D063 AD11	MB_DATA[63]
M B D062 AF11	MB_DATA[62]
M B D061 AF14	MB_DATA[61]
M B D060 AE14	MB_DATA[60]
M B D059 Y11	MB_DATA[59]
M B D058 AB11	MB_DATA[58]
M B D057 AC12	MB_DATA[57]
M B D056 AE13	MB_DATA[56]
M B D055 AF16	MB_DATA[55]
M B D054 AF16	MB_DATA[54]
M B D053 AC18	MB_DATA[53]
M B D052 AF19	MB_DATA[52]
M B D051 AD14	MB_DATA[51]
M B D050 AC14	MB_DATA[50]
M B D049 AE18	MB_DATA[49]
M B D048 AD18	MB_DATA[48]
M B D047 AD20	MB_DATA[47]
M B D046 AC20	MB_DATA[46]
M B D045 AF23	MB_DATA[45]
M B D044 AF24	MB_DATA[44]
M B D043 AF20	MB_DATA[43]
M B D042 AE20	MB_DATA[42]
M B D041 AD22	MB_DATA[41]
M B D040 AC22	MB_DATA[40]
M B D039 AE25	MB_DATA[39]
M B D038 AD26	MB_DATA[38]
M B D037 AA25	MB_DATA[37]
M B D036 AA26	MB_DATA[36]
M B D035 AE24	MB_DATA[35]
M B D034 AD24	MB_DATA[34]
M B D033 AA23	MB_DATA[33]
M B D032 AA24	MB_DATA[32]
M B D031 G23	MB_DATA[31]
M B D030 G23	MB_DATA[30]
M B D029 D26	MB_DATA[29]
M B D028 C26	MB_DATA[28]
M B D027 G26	MB_DATA[27]
M B D026 G25	MB_DATA[26]
M B D025 E24	MB_DATA[25]
M B D024 E23	MB_DATA[24]
M B D023 C24	MB_DATA[23]
M B D022 B24	MB_DATA[22]
M B D021 C20	MB_DATA[21]
M B D020 B00	MB_DATA[20]
M B D019 C25	MB_DATA[19]
M B D018 D24	MB_DATA[18]
M B D017 A21	MB_DATA[17]
M B D016 D20	MB_DATA[16]
M B D015 D18	MB_DATA[15]
M B D014 C18	MB_DATA[14]
M B D013 D14	MB_DATA[13]
M B D012 C14	MB_DATA[12]
M B D011 A20	MB_DATA[11]
M B D010 A16	MB_DATA[10]
M B D09 A16	MB_DATA[9]
M B D08 A15	MB_DATA[8]
M B D07 A13	MB_DATA[7]
M B D06 D12	MB_DATA[6]
M B D05 E11	MB_DATA[5]
M B D04 G11	MB_DATA[4]
M B D03 B14	MB_DATA[3]
M B D02 A14	MB_DATA[2]
M B D01 A11	MB_DATA[1]
M B D00 C11	MB_DATA[0]
M B A15 J25	MB_ADD[15]
M B A14 J26	MB_ADD[14]
M B A13 W25	MB_ADD[13]
M B A12 L23	MB_ADD[12]
M B A11 L25	MB_ADD[11]
M B A10 U25	MB_ADD[10]
M B A9 L24	MB_ADD[9]
M B A8 M26	MB_ADD[8]
M B A7 L26	MB_ADD[7]
M B A6 N23	MB_ADD[6]
M B A5 N24	MB_ADD[5]
M B A4 N26	MB_ADD[4]
M B A3 N26	MB_ADD[3]
M B A2 P24	MB_ADD[2]
M B A1 P26	MB_ADD[1]
M B A0 T24	MB_ADD[0]

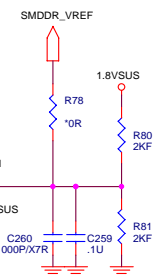
AMD S1 SOCKET

U21C	
AD12 M B DQM7	MB_DATA[63]
AC16 M B DQM6	MB_DATA[62]
AE22 M B DQM5	MB_DATA[61]
AB26 M B DQM4	MB_DATA[60]
E28 M B DQM3	MB_DATA[59]
A22 M B DQM2	MB_DATA[58]
B16 M B DQM1	MB_DATA[57]
A12 M B DQM0	MB_DATA[56]
AF12 M B DQST7	MB_DATA[55]
AE16 M B DQST6	MB_DATA[54]
AF21 M B DQST5	MB_DATA[53]
AC25 M B DQST4	MB_DATA[52]
F26 M B DQST3	MB_DATA[51]
A24 M B DQST2	MB_DATA[50]
D16 M B DQST1	MB_DATA[49]
C12 M B DQST0	MB_DATA[48]
AE12 M B DQST7	MB_DATA[47]
AD16 M B DQST6	MB_DATA[46]
AF22 M B DQST5	MB_DATA[45]
AC26 M B DQST4	MB_DATA[44]
E26 M B DQST3	MB_DATA[43]
AC24 M B DQST2	MB_DATA[42]
OC16 M B DQST1	MB_DATA[41]
OB12 M B DQST0	MB_DATA[40]
A17 M B CK1	MB0_CLK[1]
A18 M B CK1#	MB0_CLK[1]
AF18 M B CK2	MB0_CLK[2]
AF17 M B CK2#	MB0_CLK[2]
K26 M B BA2	MB_BANK[2]
T26 M B BA1	MB_BANK[1]
U26 M B BA0	MB_BANK[0]
OV24 M B RAS#	MB_RAS#
OV26 M B CAS#	MB_CAS#
U22 M B WE#	MB_WE#
Y26 M B CS#3	MB0_CS#3
U24 M B CS#2	MB0_CS#2
U24 M B CS#1	MB0_CS#1
U23 M B CS#0	MB0_CS#0
H26 M B CKE1	MB_CKE[1]
J23 M B CKE0	MB_CKE[0]
W23 M B ODT1	MB0_ODT[1]
W26 M B ODT0	MB0_ODT[0]
Y10 VTERM_FB	VTERM_FB 31
W17 CS1M_VREF	M_VREF
AE10 MEMZN R358	M_ZN
AF10 MEMZP	M_ZP

TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS



5,31



C51MVREF : W = 20MIL AND SPACE = 20MIL

5 M_A_DQ[63..0] M A DQ[63..0]
4.5 M_A_A[15..0] M A A15..0

M A DQM[7..0] M A DQ[7..0] 5
M A DQST[7..0] M A DQST[7..0] 5
M A BA[2..0] M A BA[2..0] 4.5
M A CS[63..0] M A CS[63..0] 4.5
M A RAS# 4.5
M A CAS# 4.5
M A WE# 4.5
M A CKE1 4.5
M A CKE0 4.5
M A ODT1 4.5
M A ODT0 4.5

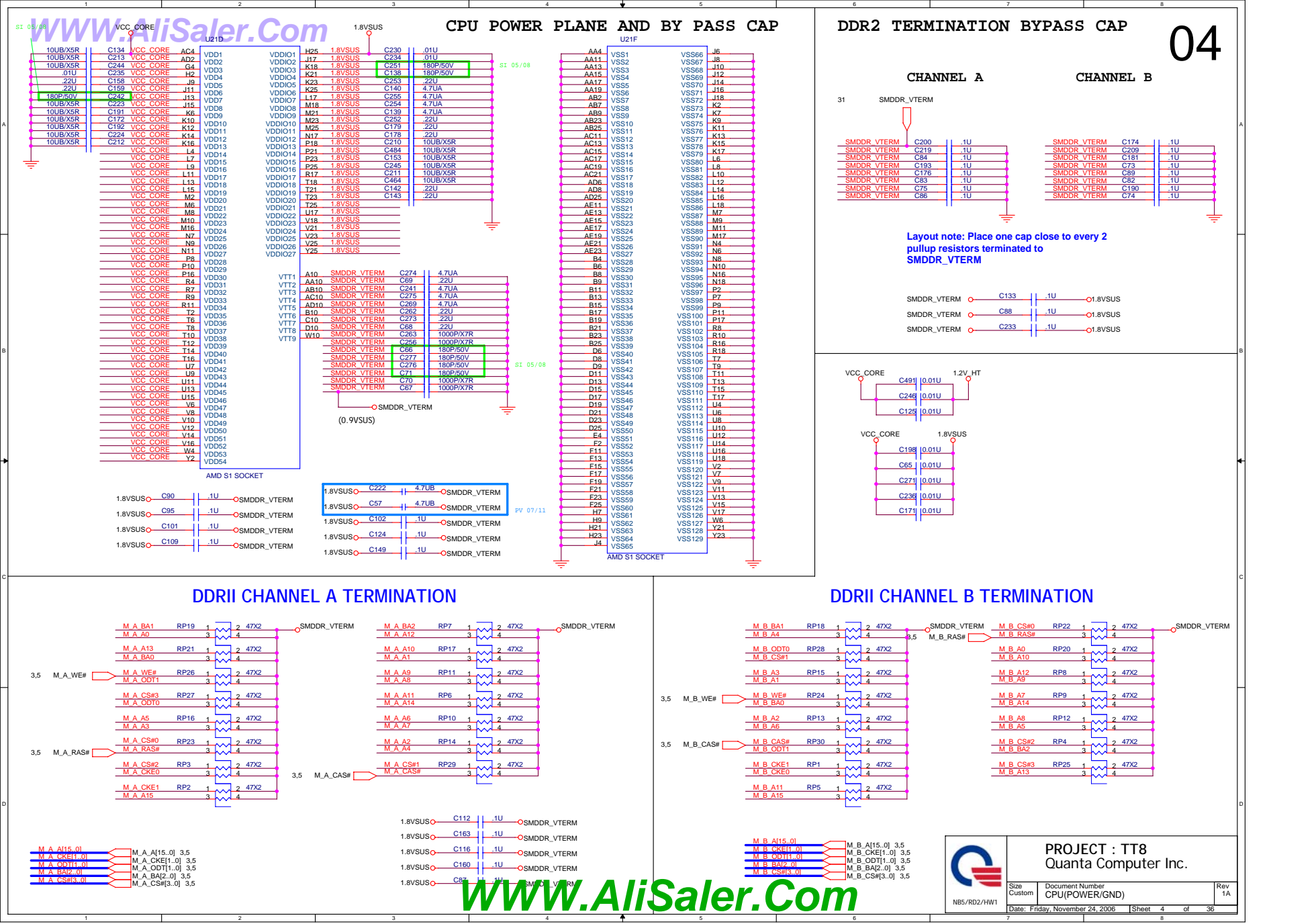
5 M_B_DQ[63..0] M B DQ[63..0]
4.5 M_B_A[15..0] M B A15..0

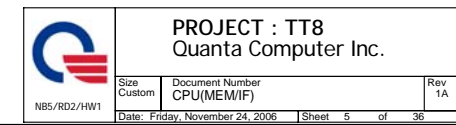
M B DQM[7..0] M B DQ[7..0] 5
M B DQST[7..0] M B DQST[7..0] 5
M B BA[2..0] M B BA[2..0] 4.5
M B CS[63..0] M B CS[63..0] 4.5
M B RAS# 4.5
M B CAS# 4.5
M B WE# 4.5
M B CKE1 4.5
M B CKE0 4.5
M B ODT1 4.5
M B ODT0 4.5

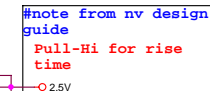


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Quanta Computer Inc.

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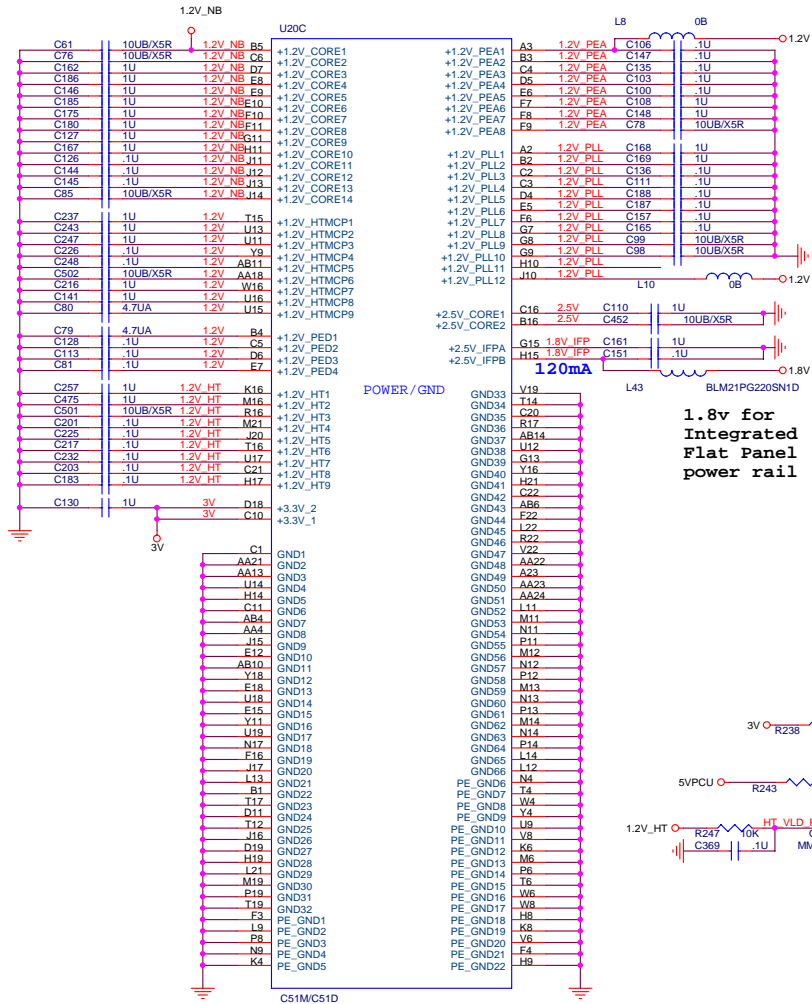


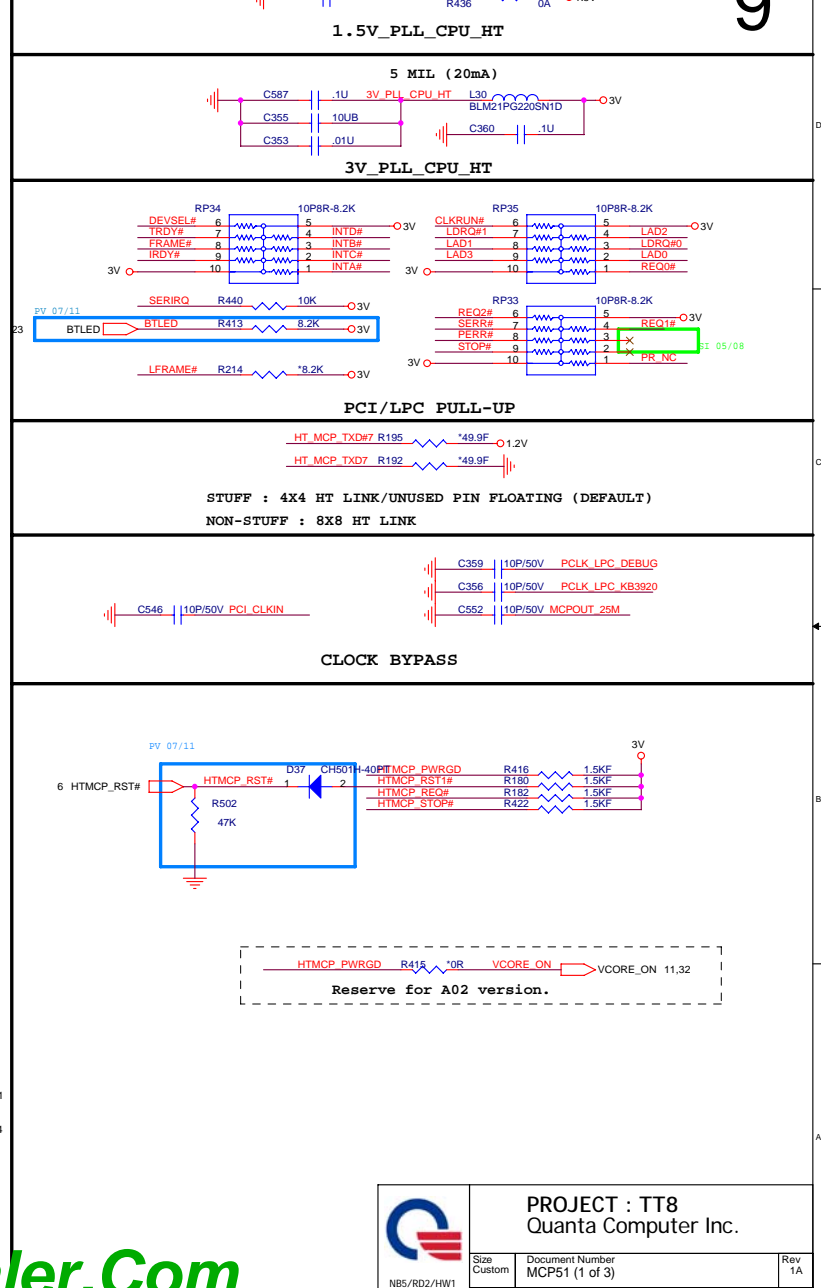
NB5/RD2/HW

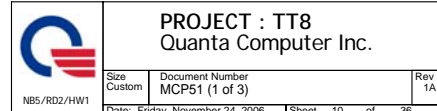
Size Custom	Document Number C51MV (HT LINK)	Rev 1A
Date: Friday, November 24, 2006	Sheet 6 of 36	

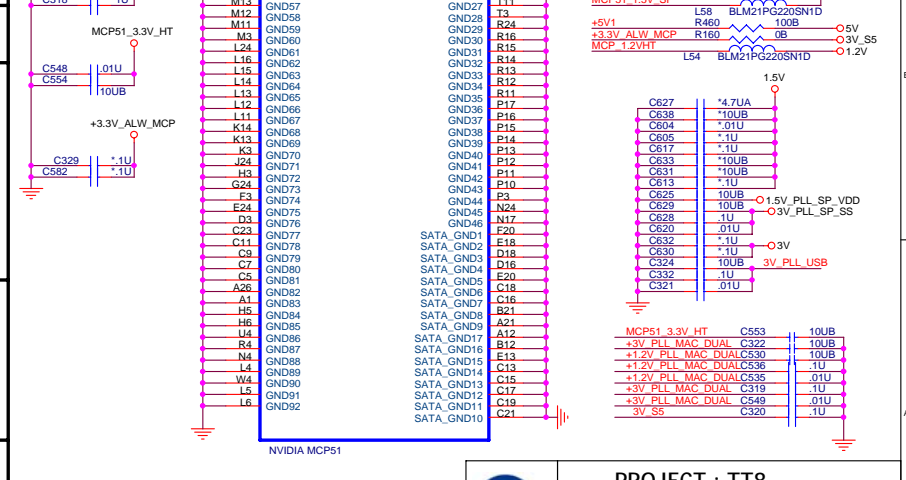
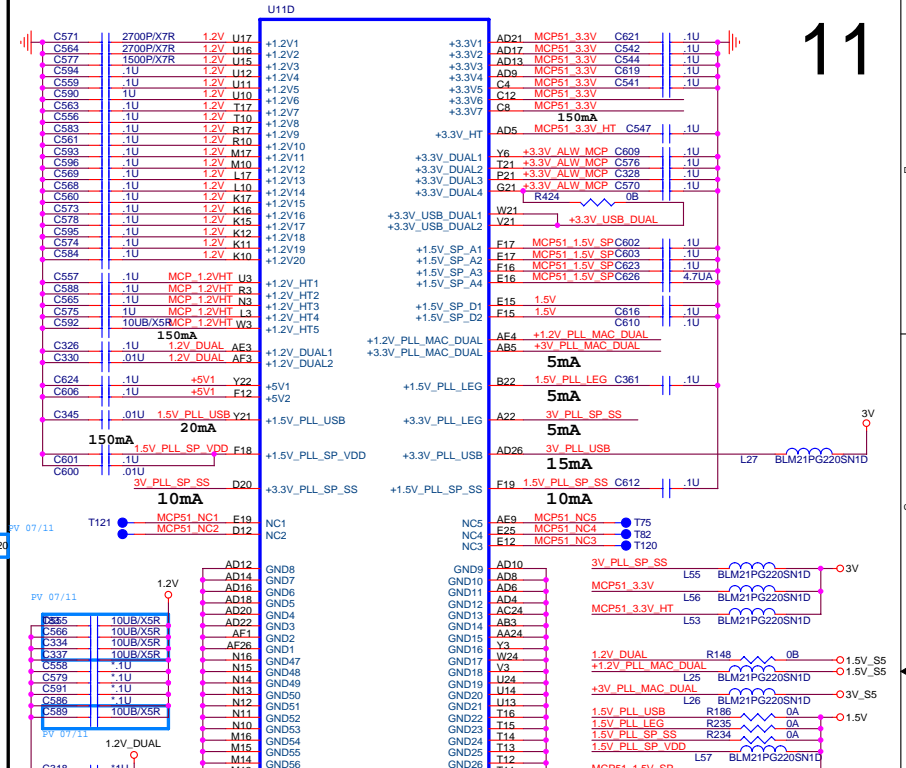


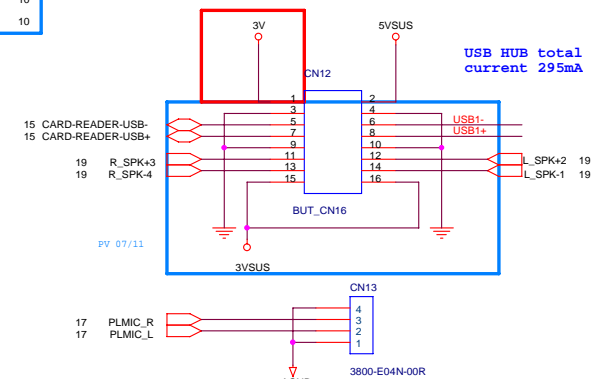
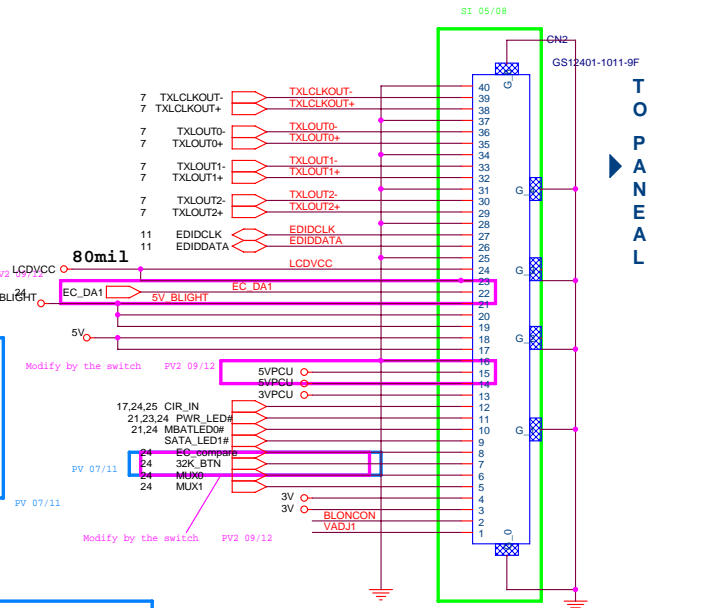
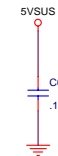
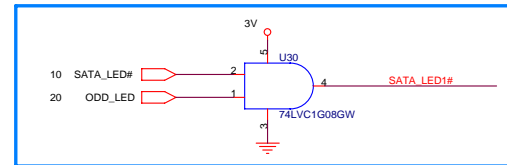
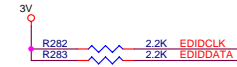
C51M POWER PLANE/GND & BYPASS







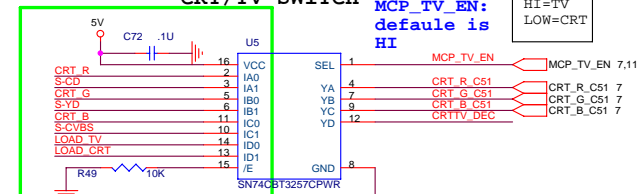




CRT/TV SWITCH

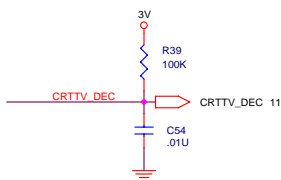
MCP_TV_EN:
default is
HI

HI=TV
LOW=CRT



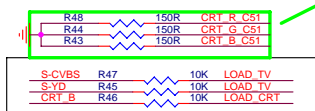
LOAD_CRT -- TV WORK
LOAD_TV -- CRT WORK

SI 05/08



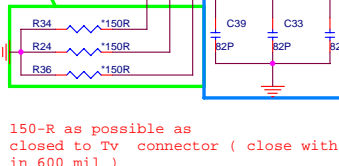
close within 600mils (
close data switch)

Change from nVIDIA for B-test



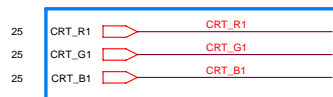
That is for CRT and TV choose..
used impedance and driver to
choose

Change from nVIDIA for B-test

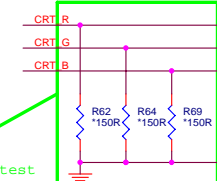


150-R as possible as
closed to Tv connector (close with
in 600 mil)

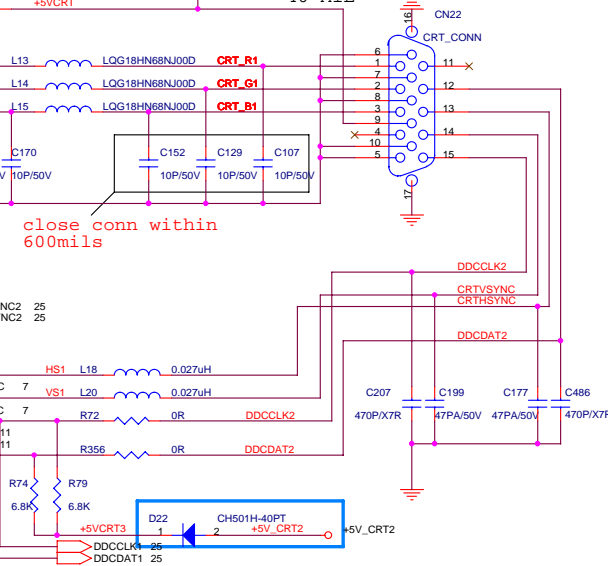
PV 07/11



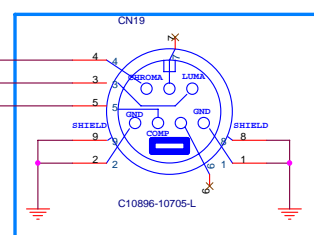
150-R as possible as
closed to CRT connector (
close with in 600 mil)



CRT PORT



TV_OUT



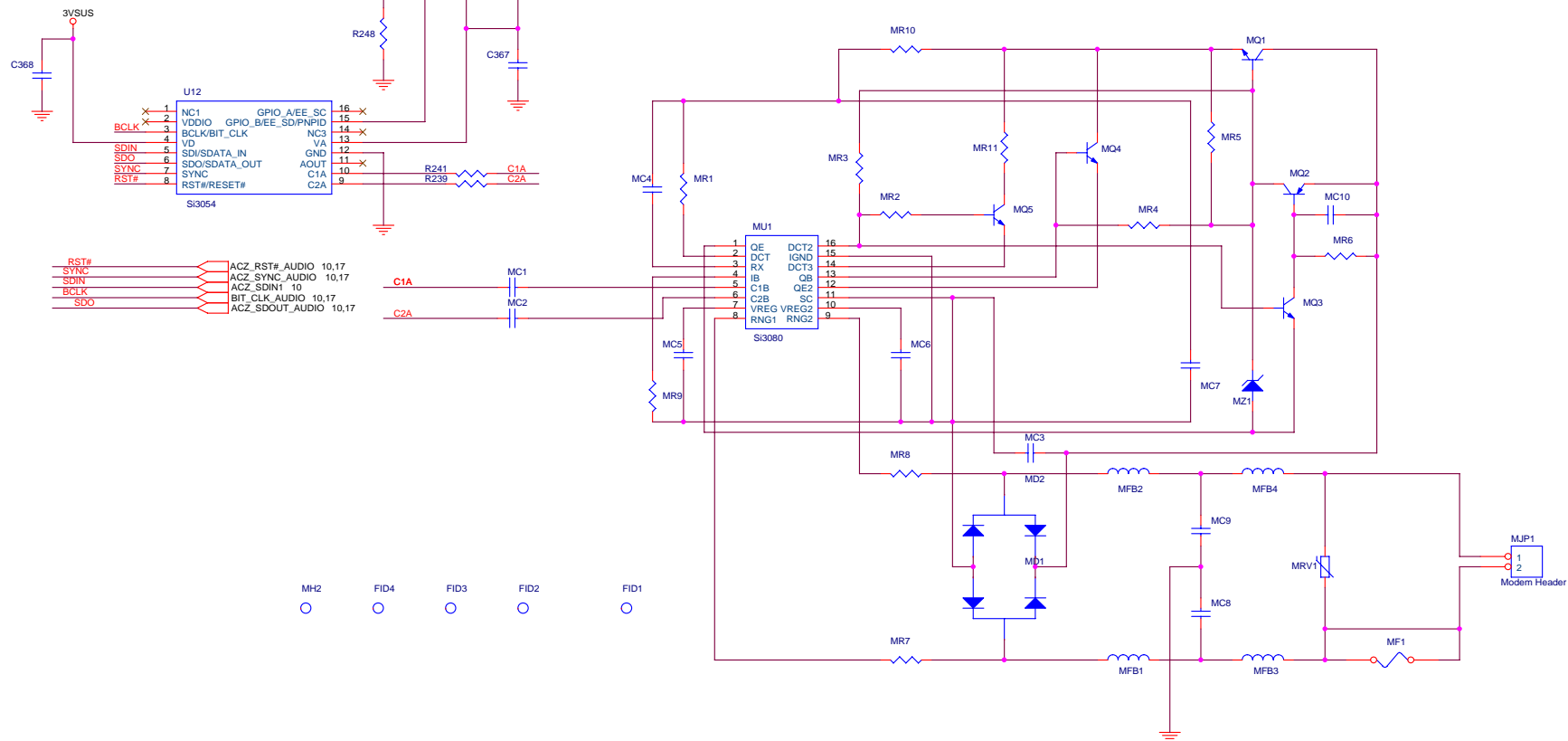
PROJECT : TT8
Quanta Computer Inc.

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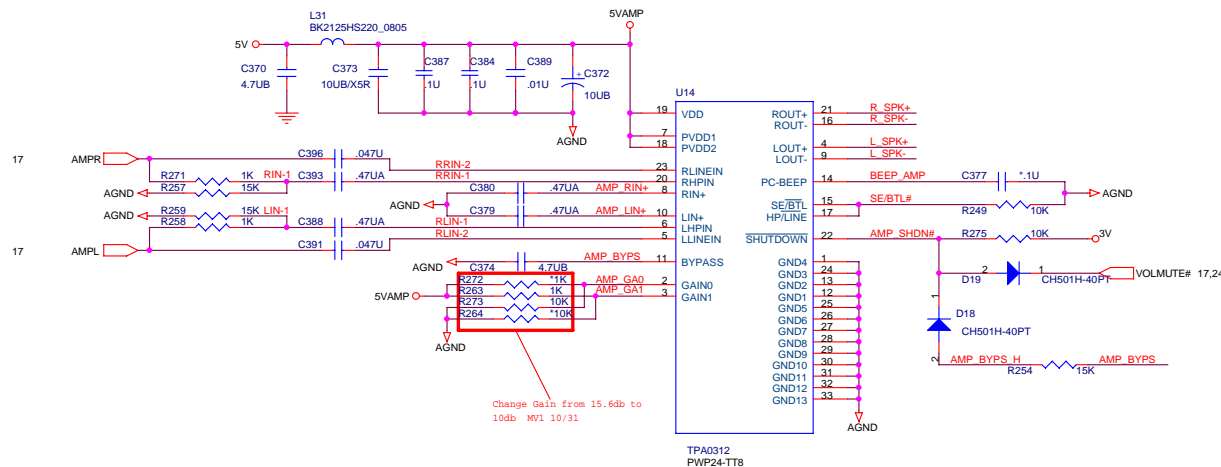
Size Custom	Document Number AU6366 controller	Rev 1A
Date: Friday, November 24, 2006		Sheet 15 of 36





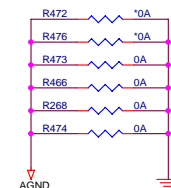
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL



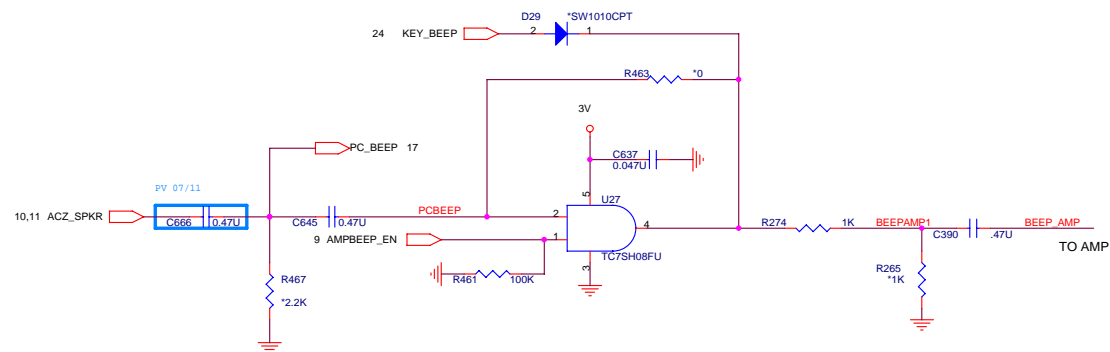
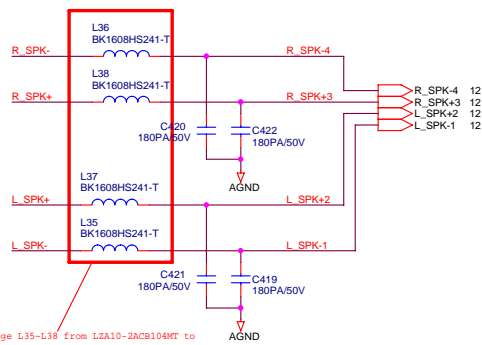
0312 Gain Table

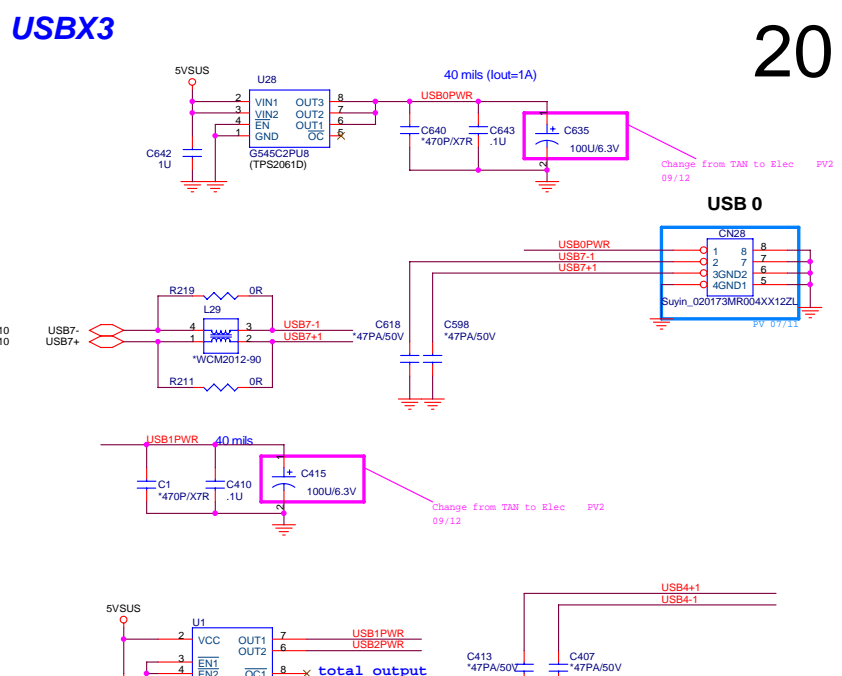
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



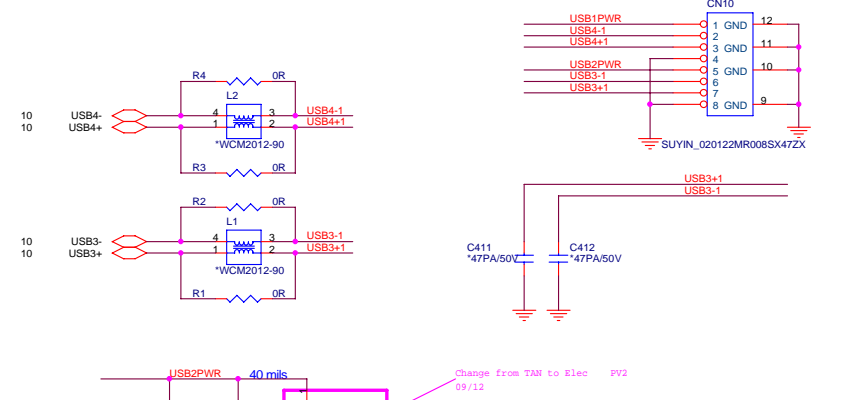
INT. SPEAKER

PCSPK BEEP





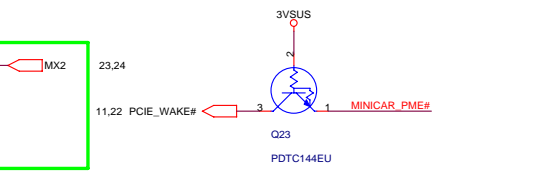
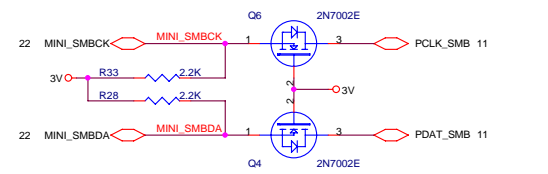
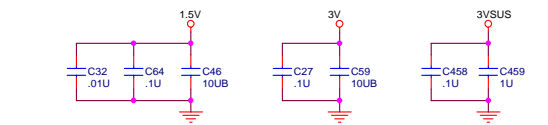
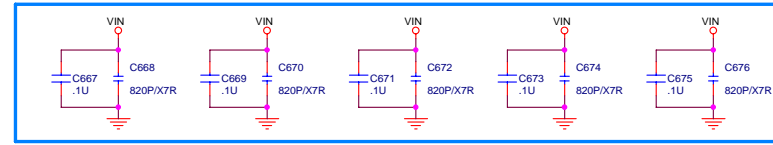
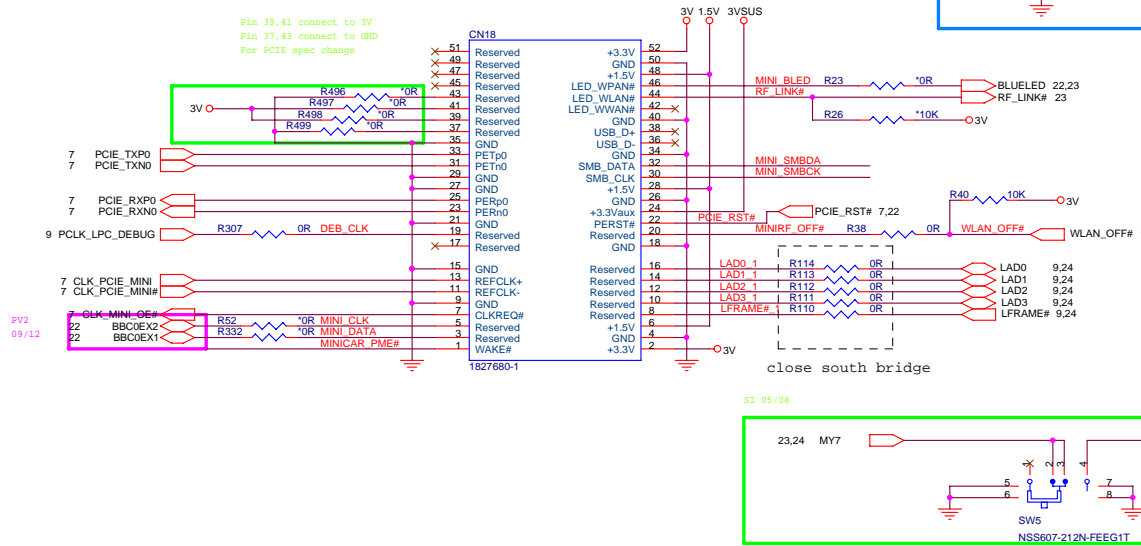
USB 1& 2



Mini PCI-E Card 1 WLAN

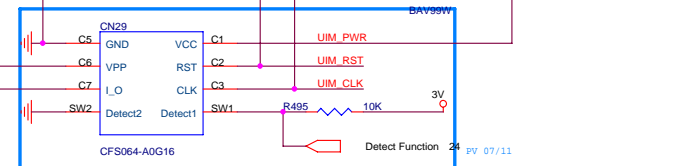
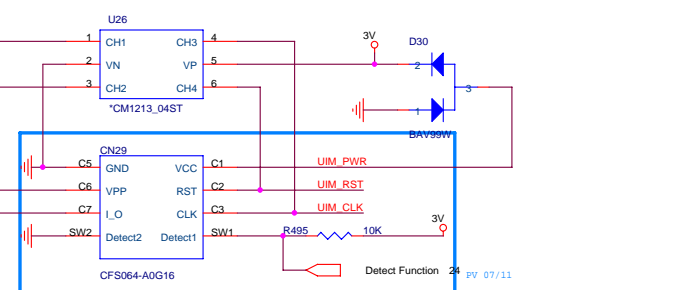
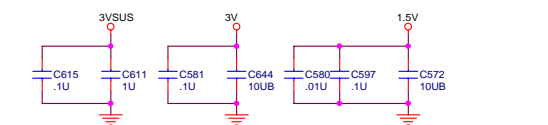
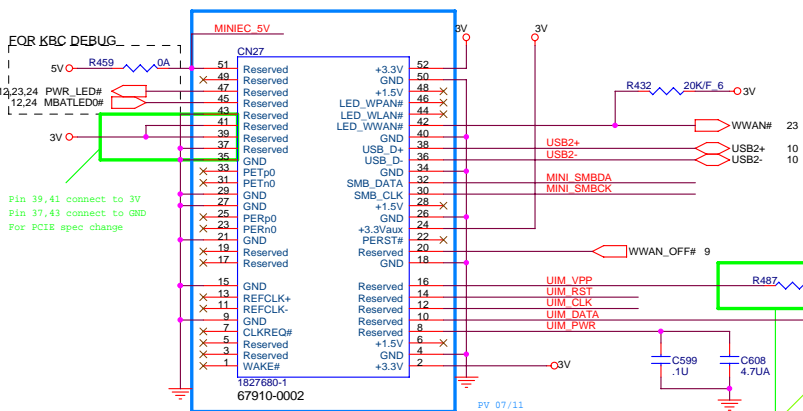
21

Pin 39,41 connect to 3V
Pin 37,43 connect to GND
For PCIe spec change



Mini PCI-E Card 2 WWAN(W/SIM)

FOR KBC DEBUG

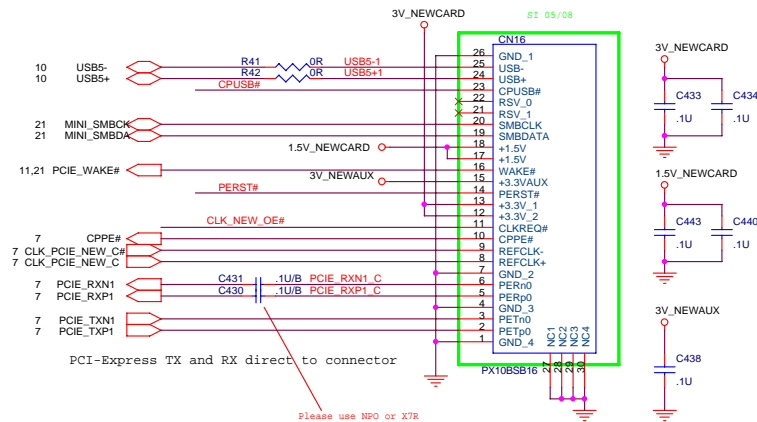


PROJECT : TT8
Quanta Computer Inc.

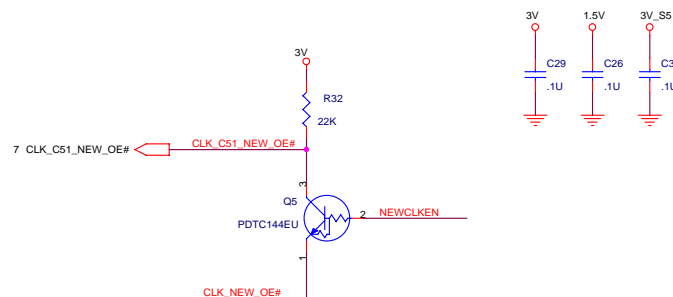
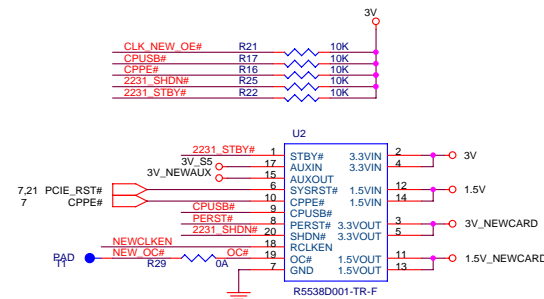
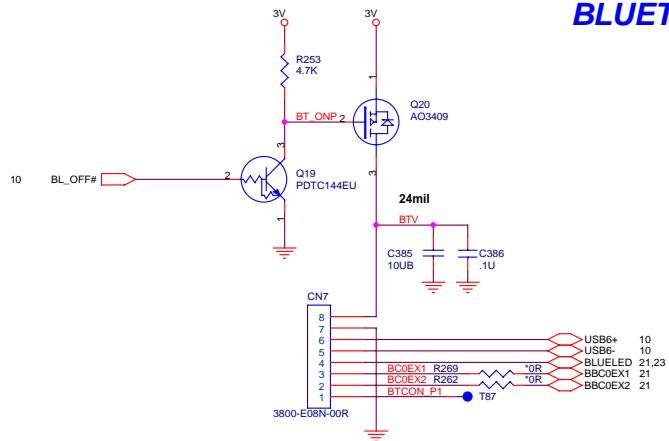
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NEWCARD

22

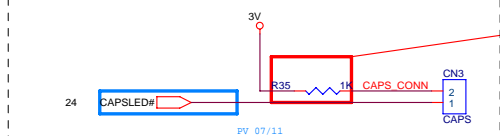


BLUETOOTH

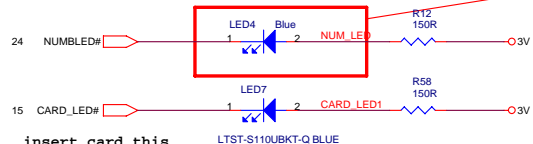
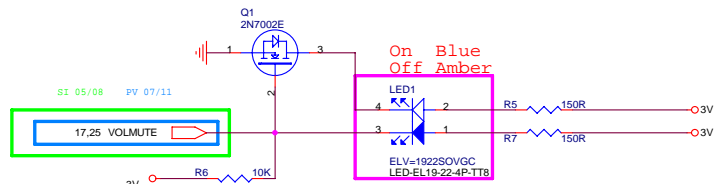
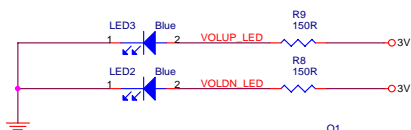




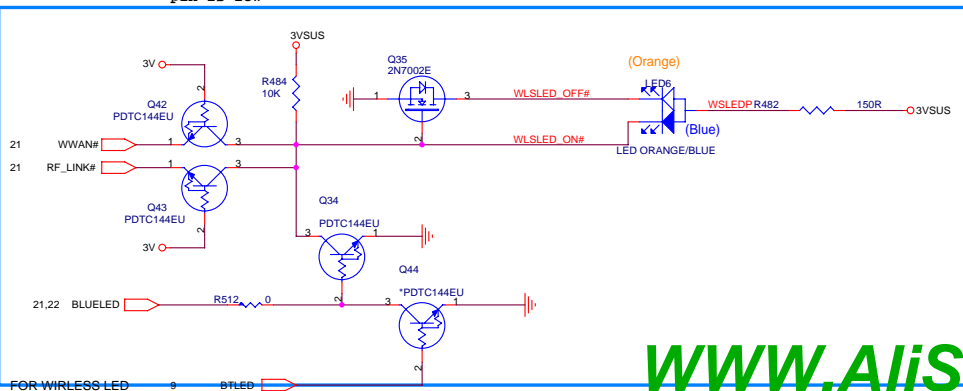
FOR POWER ON SW BOARD



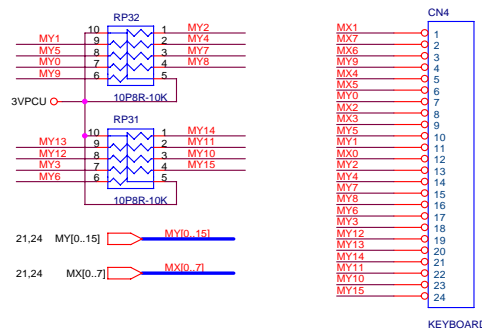
for caps lock LED board



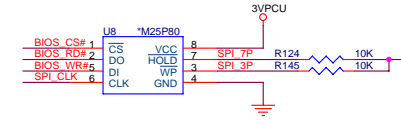
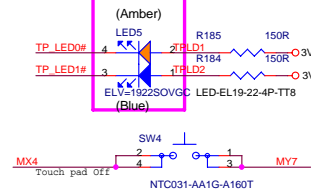
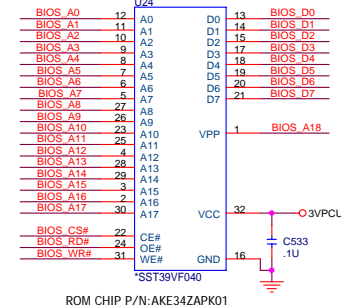
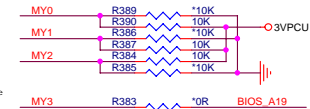
insert card this pin is low



KEYBOARD PULL-UP

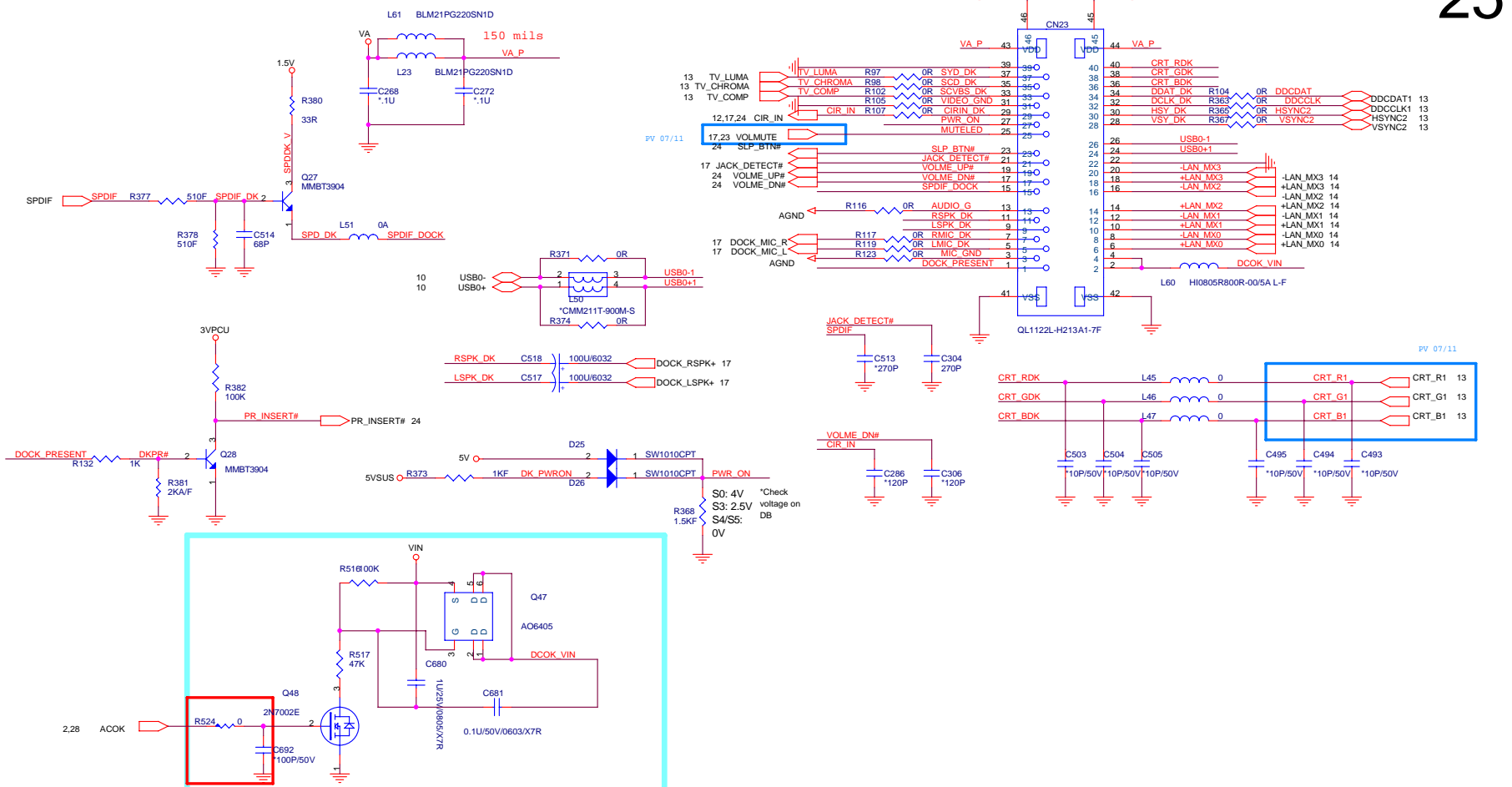


KEYBOARD

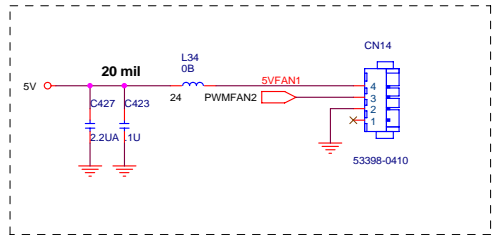


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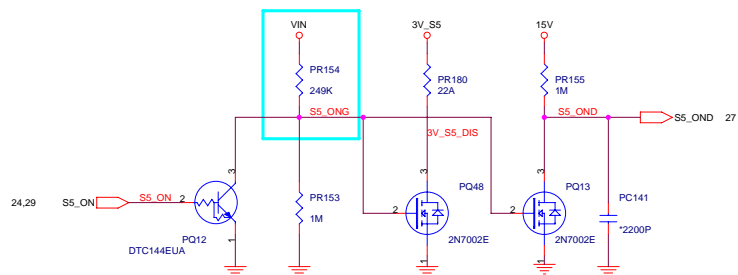
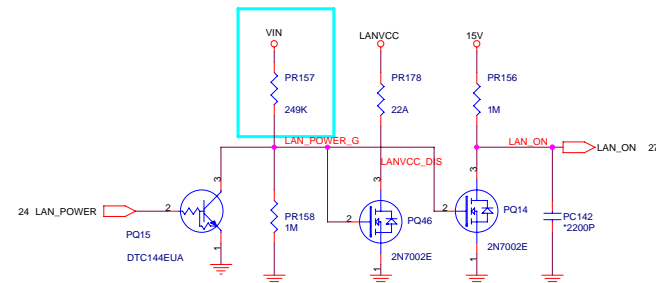
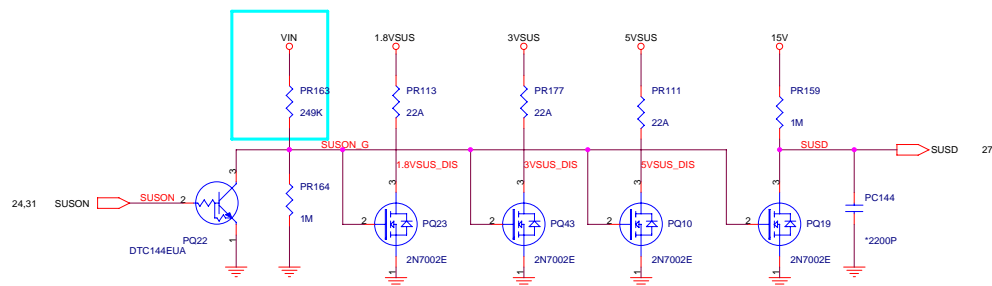
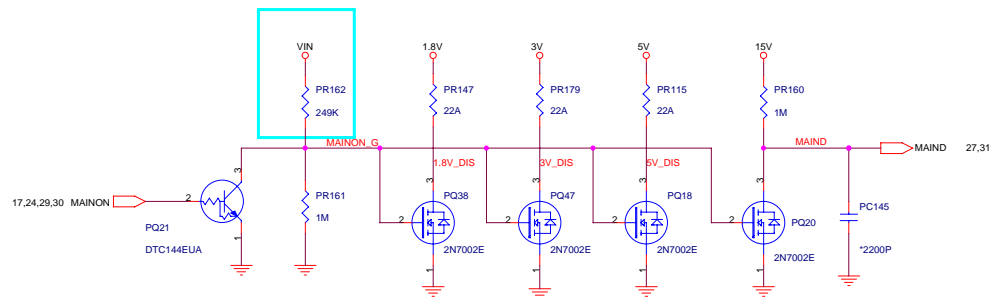
Size Custom	Document Number KB3920	Rev 1/
Date: Friday, November 24, 2006	Sheet 24 of 36	



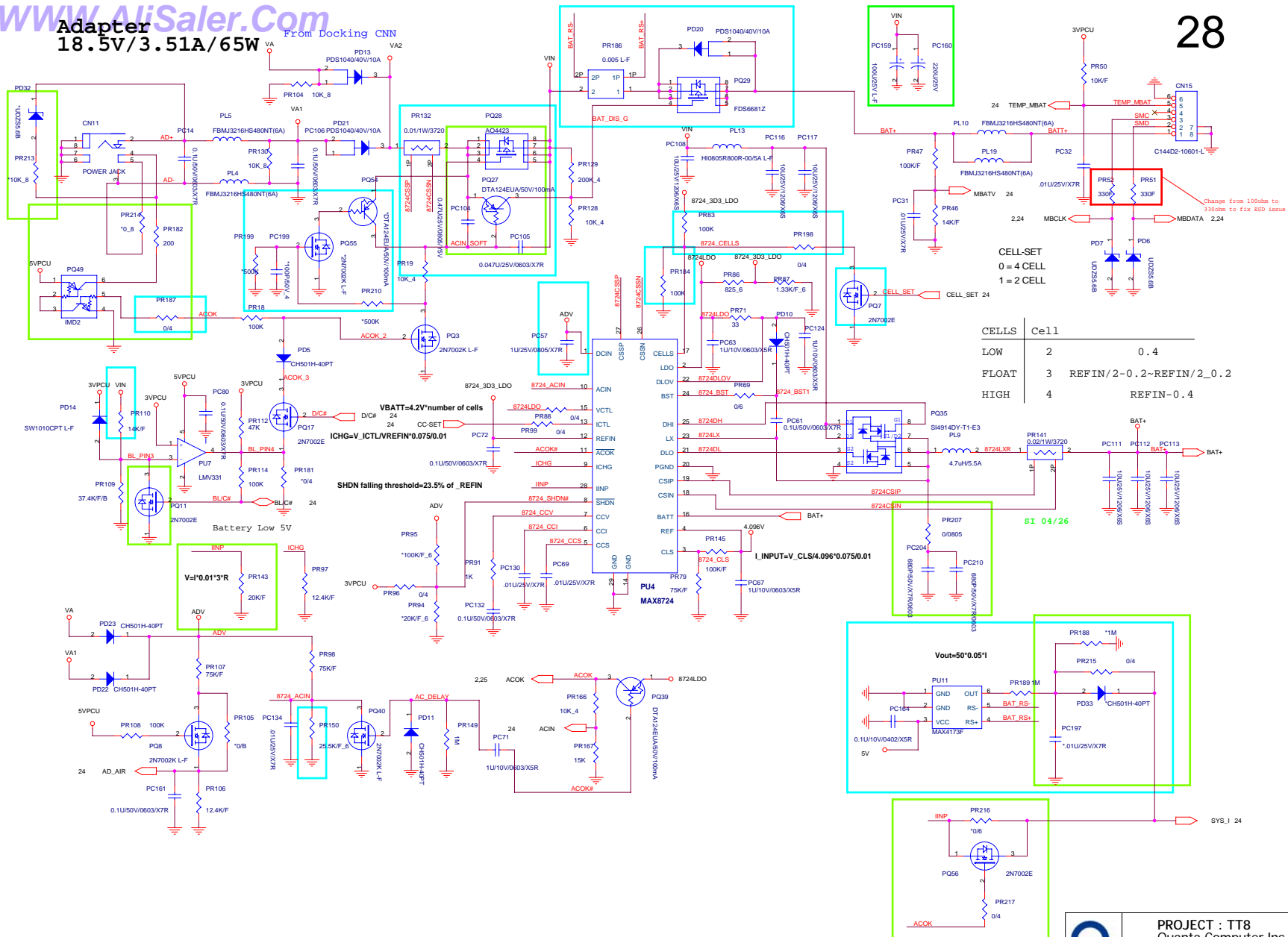
FAN

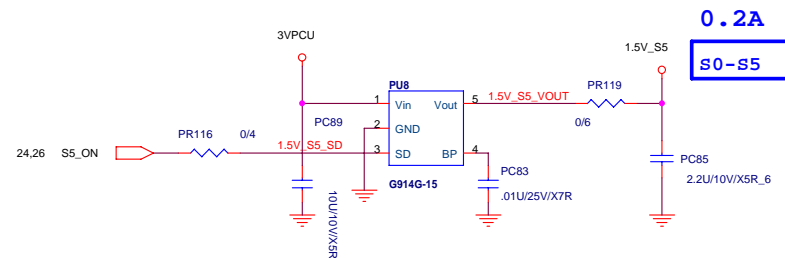
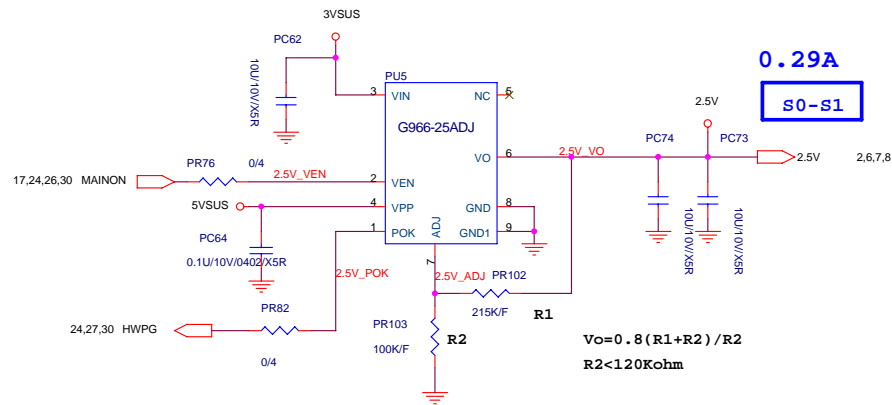


FAN1 PWM CONNECTOR

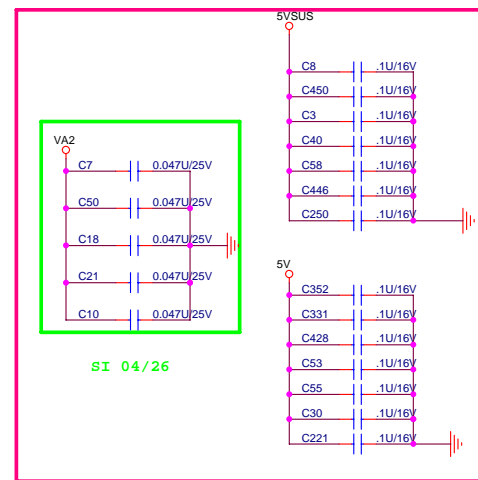
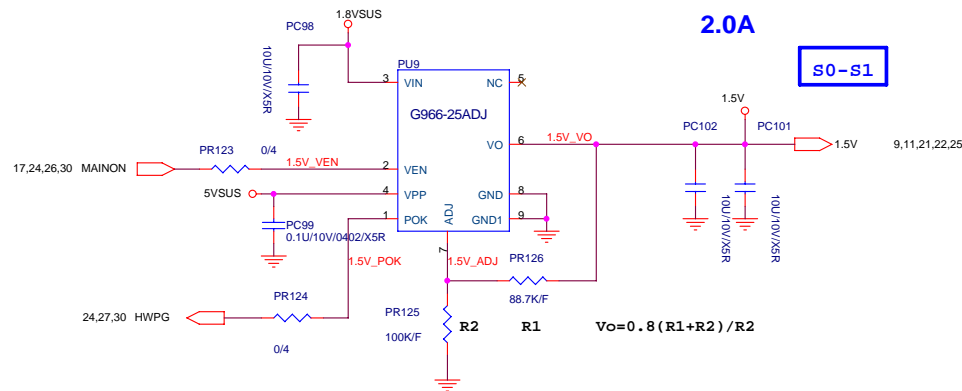








EMI



MAX1549

S0-S1

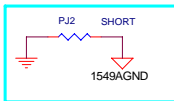
3A

$$V_{cs} = I_L(A) * L_DCR(m\Omega) = V_ILIM(mV) / 10$$

DCR 28m OHM

$$V_{out} = 0.5V(1 + R1/R2)$$

SI-2 modified



FBLANK			
VCC	OPEN	REF	GND
150us	100us	50us	blanking disabled
150us	100us	50us	100us

OUI fault protection and PG01 blanking
OUI forced-PWM transition operation

S0-S1

3.7A

$$V_{cs} = I_L(A) * L_DCR(m\Omega) = V_ILIM(mV) / 10$$

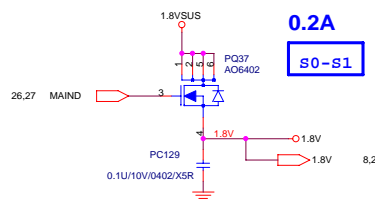
DCR 28m OHM

$$V_{out1} = 2.0V(REQ / (Rb + REQ))$$

INPUTS		OUTPUTS			REQ	VOUT1
G1	G0	OD1	OD2	OD3		
0	0	High-Z	High-Z	Hight-Z	Ra=150K	1.2V
1	0	0	High-Z	Hight-Z	Ra//ROD1=100.1K	1.0V
0	1	High-Z	0	Hight-Z	Ra//ROD2=122.4K	1.1V
1	1	High-Z	High-Z	0	Ra//ROD3=82.02K	



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Slew rate=(12.5mV/us)*(71.5K/R_TIME)
VFB=V_VID+0.125(VREF-V_OFS)
VRHOT is low when VTHRM below 1.5V
Tsw=16.26pF(R_TON+6.5K)ohm
CCV CAP=470pF*(2/total phase)*300KHz/fsw

VCC_CORE MAX8774

32

OCP=44A
VCC_CORE
35A / 1.05V

DCR=1.1m/+5%

DCR=1.1m/+5%

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.550V	1	0	0	0	0	0	0.7425V
0	0	0	0	0	1	1.520V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.500V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.475V	1	0	0	1	0	1	0.7250V
0	0	0	1	0	0	1.450V	1	0	0	1	0	0	0.7125V
0	0	0	1	0	1	1.425V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.400V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.375V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.350V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.325V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.300V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.275V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.250V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.225V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.200V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.175V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.150V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.125V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.100V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.075V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.050V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.025V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.975V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.950V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.925V	1	1	1	0	0	1	0.4500V
0	1	1	0	1	0	0.900V	1	1	1	1	0	0	0.4375V
0	1	1	0	1	1	0.875V	1	1	1	1	0	1	0.4250V
0	1	1	1	0	0	0.850V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.825V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.800V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.775V	1	1	1	1	1	1	0.3750V



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Quanta Computer Inc.

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CHANGE LIST

MODEL	DB1 --->S11		Model	OT1 MB BOARD	
				FROM	TO
TT8 MB 31TT8MB0006	4/17-4/20	1.Change Audio port and senser pin resistor. Internal MIC change from Pin14,15 to Pin16,17 Docking Mic Change from Pin16,17 to Pin14,15 Docking spk change from Pin23,24 to Pin 43,44 Swap Pin30 and Pin31 Change R486 from Pin 13 to Pin 34 and change from 5.1KK to 10K Change R251 10K to R485 5.1K 2.Change WWAN and WLAN Pin define Add R487 and R488 3.Change TEMP Control chip for leakage, Change Q9 and Q10 to BAM70020074 4.Change HDD connector type, RJ45/CRT connector footprint 5.Swap LCD connector signal from machine require 6.Swap U5 CRT/TV singnal from nVIDIA require 7.Change battery and D30 footprint 8.Change C251,C242,C138,C66,C71,C276,C277 footprint from 0603 to 0402 9.Add Q36,Q37,R489,C661,R490 for Docking MIC detect 10.Change SW5 and CN8 footprint for machinecal request 11.Change L41 to PBY201209T-300Y-N (Footprint : 0805) 12.Delect H3 and H4 for machinecal change 13.Change C20 from 0.1U to 1U (Fix LCD rise time) 14.Move Net "SLP_BTN# from pin99 to pin87 15.Modify Docking mute LED circuit 16.Modify U25 SCI# signal from BIOS request, AddR491,R492 17.Modify Buletooth switch and ODD BAYINS# to EC 18.Change caps lock connector footprint from machencal request 19.Add U30,R495,R494,R493,Q38 for reserve SIM card 20.Change 4-in-1 card footprint 21.Add R44,R43,R48 Remove R62,R64,R69,R34,R24,R36 22.Change L45,L46,L47 to 0 ohm Del C503,C504,C505,C493,C494,C495 for D-SUB function	Page		
			1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	



NBS/RD2/HW1

PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number --> S1** Change history	Rev 1A
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CHANGE LIST

MODEL	SI1 ---->PV1		Model	OT1 MB BOARD	
			Page	FROM	TO
TT8 MB 31TT8MB0006	5/17-7/11	1.Exchange Audio port External MIC Exchange Pin22 and Pin21 CD Line Exchange Pin18 and Pin20 Internal MIC Exchange Pin16 and Pin17 Docking Mic Exchange Pin14 and Pin15 3.Change R478 from 22ohm to 0ohm 4.Change R462 0ohm to C666 0.47u for Audio chip distortion 5.Exchange R272 and R263, R273 and R264 for amplifier gain change 6.Change Q8 from BAM51030Z15 to BAM23010Z30 for Rdson issue 7.Remove C439 for MS pro card can not detect 8.Add C667,C668,C669,C670,C671,C672,C673,C674,C675,C676 for WLAN con not detect issue 9.Add reverse circuit for LED issue 10.Delect Q7 for Cap lock LED 11.Add EMI Cap C93,C118,C496,C497,C499,C566,C589,C555,C334,C337 12.Change CN19,CN27,CN28,CN29 footprint 14.Change Sim connector (Add detect pin) 15.Move Docking CRT signal after PI circuit 16.Add R500, R501 for Audio chip function 17.Add D37 and R502 for nVIDIA solution 18.Move D22 from +5VCRT to +5VCRT3 19.Change Docking detect circuit 20.Delet H20 H21 21.Exchange MINI_DATA and MINI_CLK 22.Add Diode for SATA and ODD LED control 23.Add power controller for 5V shutdown 24.Change WLAN LED circuit 25.Add Res for ACZ signal 26.Delete H7 and H14 for ME change 27.Modify SB to Audio and Modem signal	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
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			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	

CHANGE LIST

MODEL			Page	OT1 MB BOARD	
				FROM	TO
TT8 MB 31TT8MB0006	PV1 --->PV2 9/8-10/17	1.Page17 change voltage from +3V to 3V fix the Mic can not work 2.Page17 change R14 from 4.7K to 5.6K to fix LCCVDD rise time 3.Page17 change LCD cable Pin22 and Pin15 for switch function, Pin7 change to 32K_BTN 4.Page24 add GPIO for switch function 5.Page10 Change cap from 18p to 22p 6.Page17 Change C392 and C395 from 10U to 1U to fix Docking noise 7.Page16 add PA11(EMI spring) 8.Page21 Exchange BBC0EX1 and BBC0EX2 9.Page20 remove C614, C607, C406, C414, C404, C405 10.Page20 Change C635, C415, C416 from TAN to ELEC 11.Page11 Del R205 and Add R207 for Bios check	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
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			13	1A	
			14	1A	
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			24	1A	
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			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	

CHANGE LIST

MODEL			Model	OT1 MB BOARD	
				FROM	TO
TT8 MB 31TT8MB0006	PV2 --->MV1 10/17-11/15	1.Page10 Exchange USB0+/- with USB3+/- signal 2.Page12 Change CN12 Pin1 from 5VSUS to 3V 3.Page17 Change C648 and C656 from 4.7U to 22U to fix Vista issue 4.Page19 Change L35-L38 from LZA10-2ACB104MT to BK1608HS241-T 5.Page19 Change Gain from 15.6db to 10db 6.Page17 Del R260,R267,D312,D322 for Docking MIC 7.Page17 ADD R520,R521,R522,R523 for Docking MIC 8.Page21 Change PR51 PR52 from 100ohm to 330ohm to fix ESD issue 9.Page20 unstuff R188 to fix ODD problem 10.Page11 Change the board ID1 from low to high 11.Page15 Change Cap (C60,C56,C441,C44,C45)from 0.1u to 1u 12.Page15 Change Res (R318,R313,R312)from 39K to 10K 13.Page17 Add 0.01u(C693, C694) to fix high frequency problem 14.Page14 remove the cap(C408,C409) from MV build 15.Page7 Reserve C696 for nVIDIA 16.Page15 Reserve R525 and C695 for 3VSUS drop 17.Page23 Change LED4 for ME requests	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
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			27	1A	
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			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	