# AT3U BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

**CPU Merom**
478P (uPGA)/35W
PAG 3,4

**CPU THERMAL SENSOR**
PAG 11

14.318MHz

**CLOCK GEN**
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

**NORTH BRIDGE**
Crestline
PAG 5,6,7,8,9,10,11

**DDRII-SODIMM1**
PAG 12,13
DDRII 533,667 MHz

**DDRII-SODIMM2**
PAG 12,13
DDRII 533,667 MHz

*TV_OUT*
*CRT_OUT*
*LVDS(2 Channel)*

**CRT/S-VIDEO**
PAG 18

**Panel Connector**
PAG 19

**Cable Docking**
PAG 31
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

NBSRCCLK, NBSRCCLK#

**DMI LINK**

**SOUTH BRIDGE**
ICH-8M
PAG 14,15,16,17

*USB2.0*
5 | 0 | 3 | 4,6,7

**Bluetooth** PAG 27

**USB2.0 I/O Ports X1** PAG 24

**Camera X1** PAG 24

**Mini PCI-E Card x1**
**Express Card x1**
**Cable Docking x1** PAG 31

*PCI BUS / 33MHz*
PCI-E
*Azalia*

**SATA - HDD1** PAG 24 — *SATA2*
**SATA - HDD2** PAG 27 — *SATA0*
**PATA- CD-ROM** PAG 24 — *PATA (66/100/133)*

*LPC*

**Mini PCI-E Card**
PCI Express Mini Card (Wireless LAN)
PAG 30

**LAN**
Realtek PCIE-LAN RTL8101 (10/100)
PAG 25,26

**Express Card 34**
(NEW CARD)
PAG 27

**RICOH**
RICOH 832
PAG 20,21

**Realtek**
ALC 268
PAG 22

Two-element microphone PAG 28

Audio Jacks (Phone/ MIC) PAG 22

**ENE KBC**
KB3926QF A2
PAG 32

Keyboard Touch Pad PAG 28
CIR PAG 22
Capacitive Sense SW PAG 28

**RJ45** PAG 25

**IEEE1394 CONN** PAG 21

**Memory CardReader** PAG 20

**AUDIO Amplifier** PAG 23

**Jack to Speaker** PAG 28

**FAN** PAG 31

**SPI** PAG 32

**SYSTEM CHARGER(MAX8724)** PAG 33

**SYSTEM POWER MAX8778** PAG 34

**VCCP +1.5V AND GMCH 1.05V(MAX8717)** PAG 35

**CPU CORE MAX8771** PAG 36

**DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR)** PAG 37

**DISCHARGE/3VS/5VS/LANVCC** PAG 38

| PCI ROUTING TABLE | IDSEL | INTERUPT | DEVICE |
|---|---|---|---|
| REQ0# / GNT0# | AD25 | INTE#,INTF# | RICOH832 |
| REQ1# / GNT1# | AD22 | INTC#,INTD# | MINI PCI for debug |

**PROJECT : AT3U**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | BLOCK DIAGRAM | 2A |

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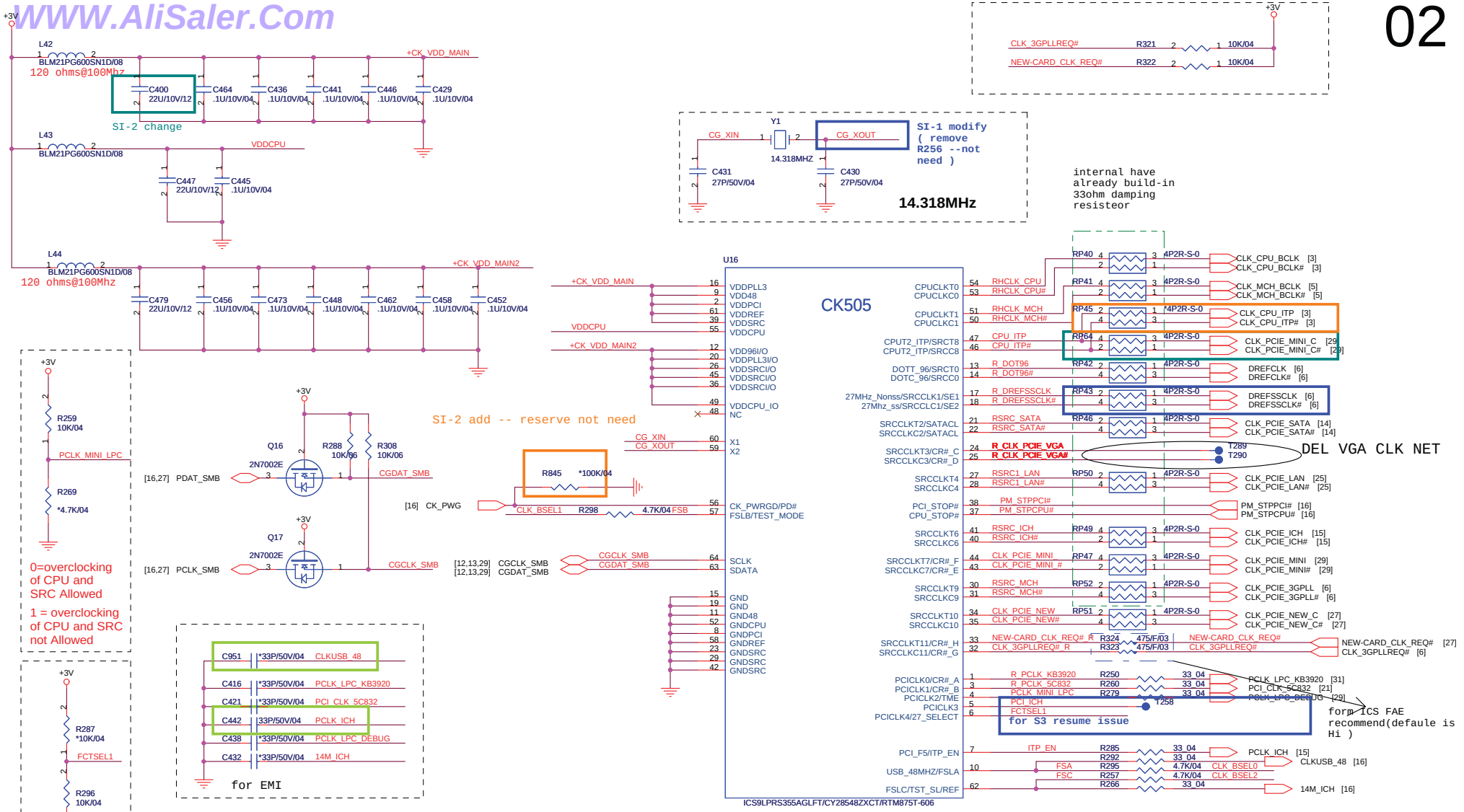
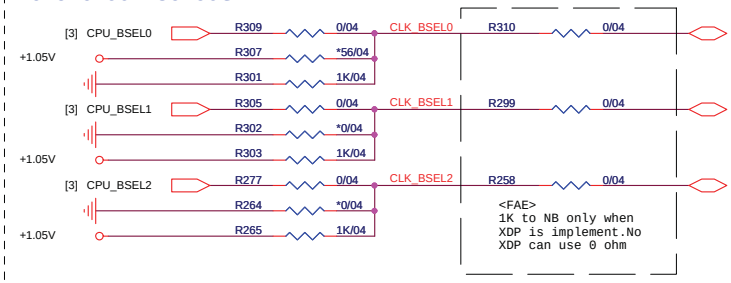
NB5/RD1/HW2




## CPU Clock select




| FSC | FSB | FSA | CPU | SRC | PCI |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 100 | 100 | 33 |
| 0 | 0 | 1 | 133 | 100 | 33 |
| 0 | 1 | 1 | 166 | 100 | 33 |
| 0 | 1 | 0 | 200 | 100 | 33 |
| 0 | 0 | 0 | 266 | 100 | 33 |
| 1 | 0 | 0 | 333 | 100 | 33 |
| 1 | 1 | 0 | 400 | 100 | 33 |
| 1 | 1 | 1 | RSVD | 100 | 33 |

**GCLK_SEL = FCTSEL1**

| FCTSEL1 (PIN13) | PIN20 | PIN21 | PIN24 | PIN25 |
|---|---|---|---|---|
| 0=UMA | DOT96T | DOT96C | SRCT1/LCDT_100 | SRCT1/LCDT_100 |
| 1 = External VGA | SRCT0 | SRCC0 | 27Mout-NSS | 27Mout-SS |

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| Size | Document Number | Rev |
|---|---|---|
| Custom | CLOCK GENERATOR | 2A |
| Date: Wednesday, May 02, 2007 | Sheet 2 of 37 | |

NB5/RD1/HW2

for power noise

Layout Note: Place voltage divider within 0.5" of GTLREF pin

modified --remove R72

SI-2 modified for fix run TAT hang

Note: H_DPRSTP need to daisy chain from ICH8 to IMVP6 to CPU.

Reserved for EMI.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Populate ITP700Flex for bringup

ITP debug signals

Layout Note: Place R8 close ITP.

Layout Note: Place R4,R361,R346 & R7 close to CPU.

| FSB | BCLK | BSEL2 | BSEL1 | BSEL0 |
|---|---|---|---|---|
| 533 | 133 | 0 | 0 | 1 |
| 667 | 166 | 0 | 1 | 1 |
| 800 | 200 | 0 | 1 | 0 |

ITP disable guidelines

| Signal | Resistor Value | Connect To | Resistor Placement |
|---|---|---|---|
| TDI | 150 ohm +/- 5% | VTT | Within 2.0" of the ITP |
| TMS | 39 ohm +/- 1% | VTT | Within 2.0" of the ITP |
| TRST# | 500-680ohm +/- 5% | GND | Within 2.0" of the ITP |
| TCK | 27 ohm +/- 1% | GND | Within 2.0" of the ITP |
| TDO | 150 ohm +/- 5% | VTT | Within 2.0" of the ITP |
| | | | |

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

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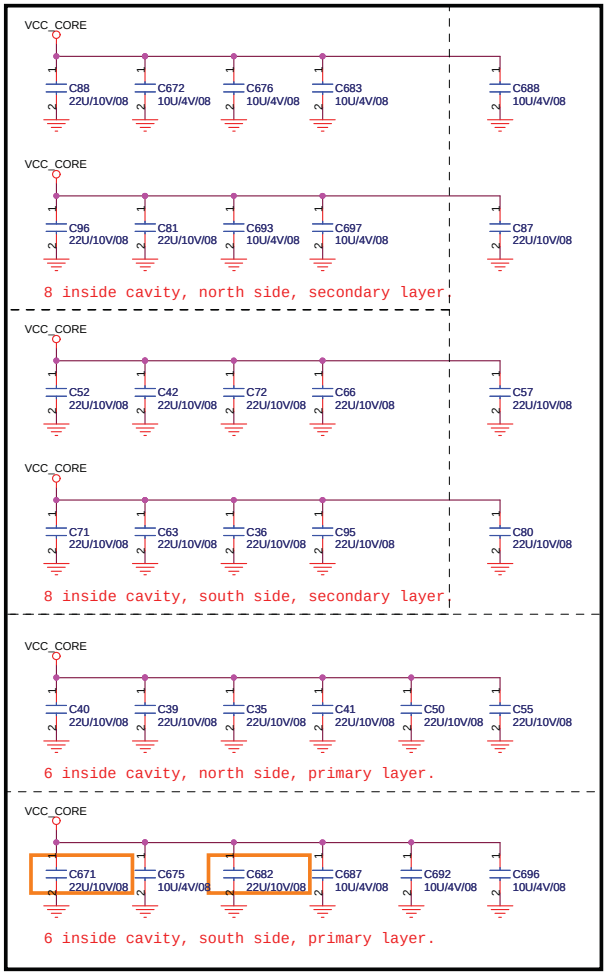
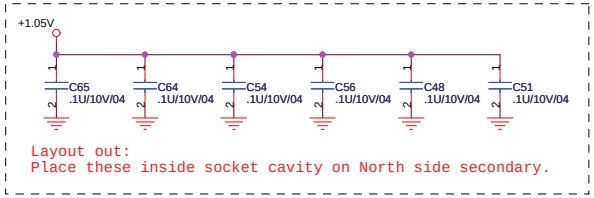
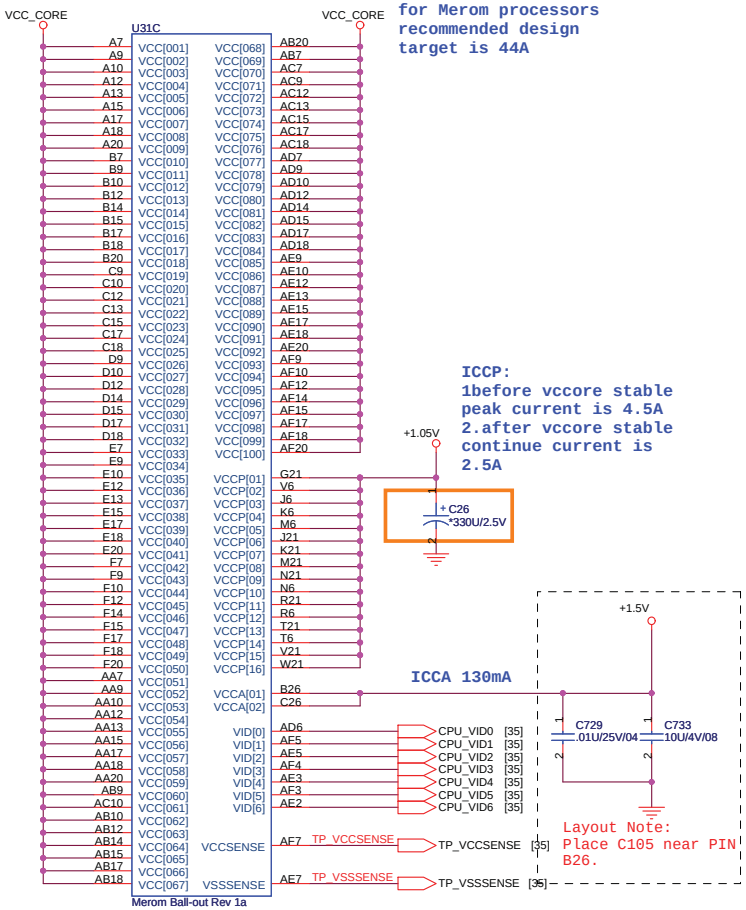
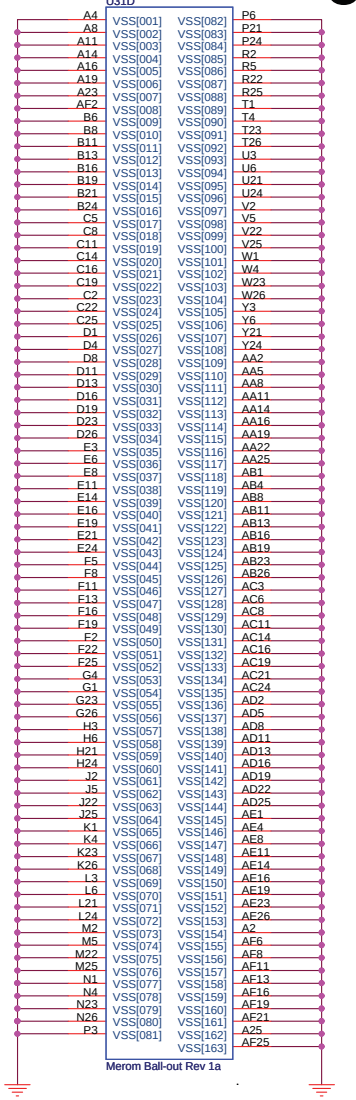
| Size | Document Number | Rev |
|---|---|---|
| Custom | CLOCK GENERATOR | 2A |
| Date: Wednesday, May 02, 2007 | Sheet 3 of 37 | |

NB5/RD1/HW2

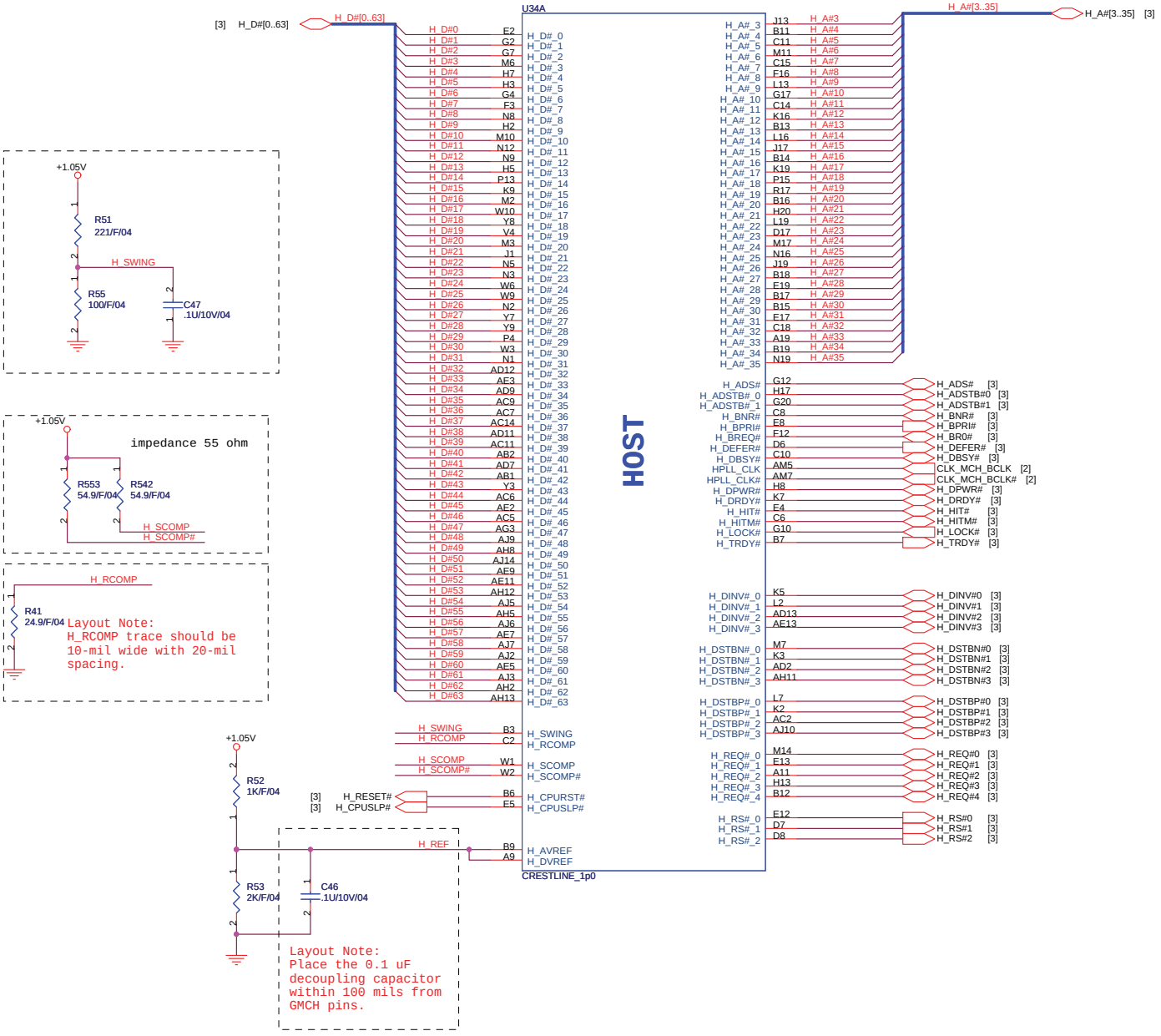



| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| | Size: Custom<br>Document Number: Merom Processor (POWER) | Rev: 2A |
| | Date: Wednesday, May 02, 2007 | Sheet 4 of 37 |




| | |
|---|---|
| PROJECT : | AT3U |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: Crestline (HOST) |
| Rev: 2A | |
| NB5/RD1/HW2 | |
| Date: Wednesday, May 02, 2007 | Sheet 5 of 37 |

U34B

U34C

WW22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs

CRESTLINE new pin define

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

<check list & CRB>
For Calero : 1.5K
For Cresstline:2.4K

modified add 470P

Dis/Enable setting

<FAE>
If no use can be NC

<check lisr & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0 ohm

<FAE> Flexible and safe

IV&EV Dis/Enable setting

<check list> HSYNC/VSYNC serial R place close to NB

In Crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)

only resever AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC

CLKREQ# ( MCH drives CLK_REQ# to control the PCI-E diff clk input itself )

GMCH pwrok is 3.3v tolerant

<FAE>
If no use DREFCLK PU and DREFCLK# PD

IV&EV Dis/Enable setting

<design guide>
If no use
DREFCLK PU and
DREFCLK# PD

<check list>
For EV@
Connect to GND
CRT R/G/B
TV A/B/C
HSYNC/VSYNC

<check list>
For IV@
Connect to 150ohm
CRT R/G/B
TV A/B/C
Connect to 39ohm
HSYNC/VSYNC

SI-2 change

close to chip

CRESTLINE_1p0

CRESTLINE_1p0



PROJECT : AT3U
Quanta Computer Inc.

N85/RD1/HW2

Size: Custom | Document Number: Crestline (VGA,DMI) | Rev: 2A

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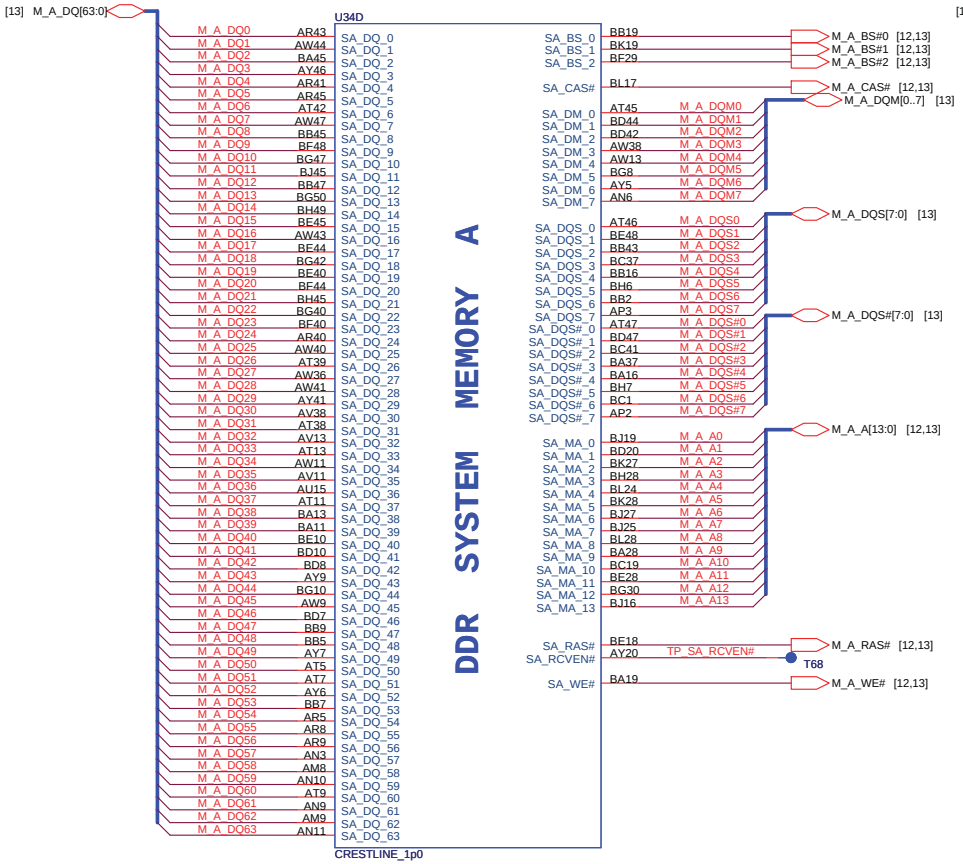
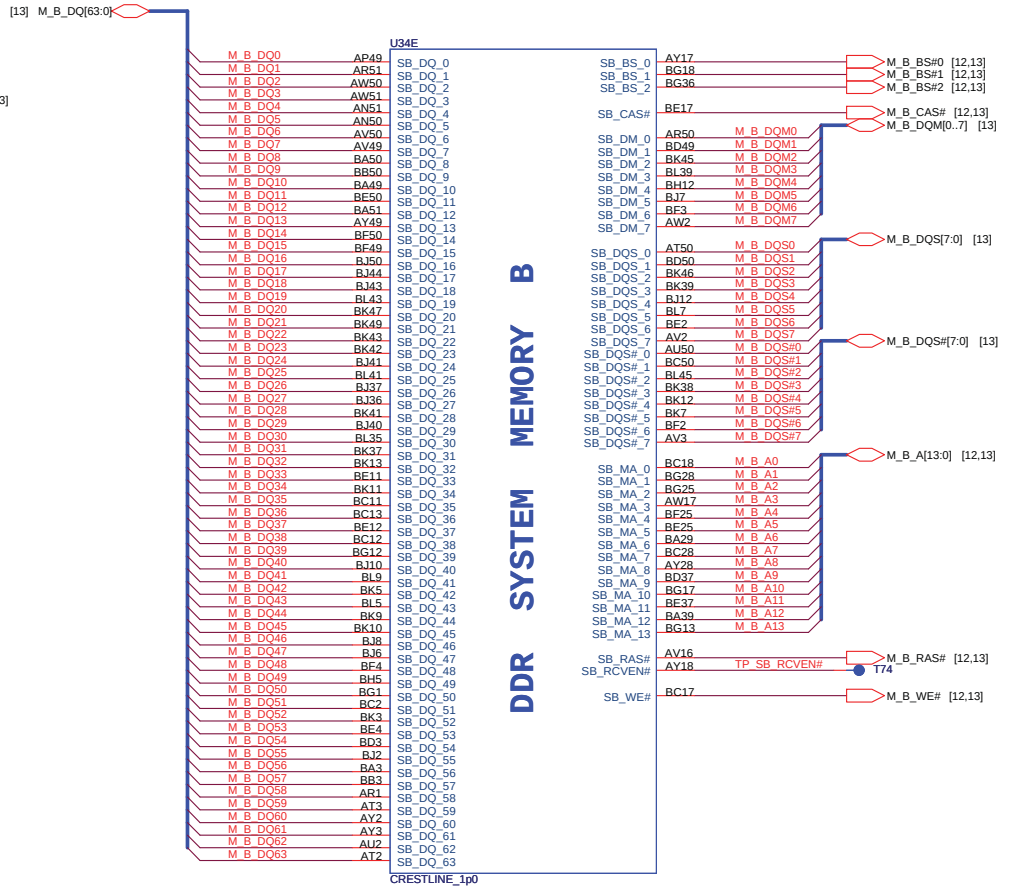



| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: Crestline (DDR) | Rev: 2A |
| Date: Wednesday, May 02, 2007 | Sheet 7 of 37 | |

U34G

VCC CORE

VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13

AT35 AT34 AH28 AC32 AC31 AK32 AJ31 AJ28 AH32 AH31 AH29 AF32 R30

+1.05V

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

+1.8VSUS_GMCH

POWER

VCC SM

VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35 VCC_SM_36

AU32 AU33 AU35 AV33 AW33 AW35 AY35 BA32 BA33 BA35 BB33 BC32 BC33 BC35 BD32 BD35 BE32 BE33 BE35 BF33 BF34 BG32 BG33 BG35 BH32 BH34 BH35 BJ32 BJ33 BJ34 BK32 BK33 BK34 BK35 BL33 AU30

+VCC_AXG

+1.05V

VCC GFX

VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34

R20 T14 W13 W14 Y12 AA20 AA23 AA26 AA28 AB21 AB24 AB29 AC20 AC21 AC23 AC24 AC26 AC28 AD20 AD23 AD24 AD28 AF21 AF26 AA31 AH20 AH21 AH23 AH24 AH26 AD31 AJ20 AN14

VCC GFX NCTF

VCC_AXG_NCTF_1 VCC_AXG_NCTF_2 VCC_AXG_NCTF_3 VCC_AXG_NCTF_4 VCC_AXG_NCTF_5 VCC_AXG_NCTF_6 VCC_AXG_NCTF_7 VCC_AXG_NCTF_8 VCC_AXG_NCTF_9 VCC_AXG_NCTF_10 VCC_AXG_NCTF_11 VCC_AXG_NCTF_12 VCC_AXG_NCTF_13 VCC_AXG_NCTF_14 VCC_AXG_NCTF_15 VCC_AXG_NCTF_16 VCC_AXG_NCTF_17 VCC_AXG_NCTF_18 VCC_AXG_NCTF_19 VCC_AXG_NCTF_20 VCC_AXG_NCTF_21 VCC_AXG_NCTF_22 VCC_AXG_NCTF_23 VCC_AXG_NCTF_24 VCC_AXG_NCTF_25 VCC_AXG_NCTF_26 VCC_AXG_NCTF_27 VCC_AXG_NCTF_28 VCC_AXG_NCTF_29 VCC_AXG_NCTF_30 VCC_AXG_NCTF_31 VCC_AXG_NCTF_32 VCC_AXG_NCTF_33 VCC_AXG_NCTF_34 VCC_AXG_NCTF_35 VCC_AXG_NCTF_36 VCC_AXG_NCTF_37 VCC_AXG_NCTF_38 VCC_AXG_NCTF_39 VCC_AXG_NCTF_40 VCC_AXG_NCTF_41 VCC_AXG_NCTF_42 VCC_AXG_NCTF_43 VCC_AXG_NCTF_44 VCC_AXG_NCTF_45 VCC_AXG_NCTF_46 VCC_AXG_NCTF_47 VCC_AXG_NCTF_48 VCC_AXG_NCTF_49 VCC_AXG_NCTF_50 VCC_AXG_NCTF_51 VCC_AXG_NCTF_52 VCC_AXG_NCTF_53 VCC_AXG_NCTF_54 VCC_AXG_NCTF_55 VCC_AXG_NCTF_56 VCC_AXG_NCTF_57 VCC_AXG_NCTF_58 VCC_AXG_NCTF_59 VCC_AXG_NCTF_60 VCC_AXG_NCTF_61 VCC_AXG_NCTF_62 VCC_AXG_NCTF_63 VCC_AXG_NCTF_64 VCC_AXG_NCTF_65 VCC_AXG_NCTF_66 VCC_AXG_NCTF_67 VCC_AXG_NCTF_68 VCC_AXG_NCTF_69 VCC_AXG_NCTF_70 VCC_AXG_NCTF_71 VCC_AXG_NCTF_72 VCC_AXG_NCTF_73 VCC_AXG_NCTF_74 VCC_AXG_NCTF_75 VCC_AXG_NCTF_76 VCC_AXG_NCTF_77 VCC_AXG_NCTF_78 VCC_AXG_NCTF_79 VCC_AXG_NCTF_80 VCC_AXG_NCTF_81 VCC_AXG_NCTF_82 VCC_AXG_NCTF_83

T17 T18 T19 T21 T22 T23 T25 U15 U16 U17 U19 U20 U21 U23 U26 V16 V17 V19 V20 V21 V23 V24 Y15 Y16 Y17 Y19 Y20 Y21 Y23 Y24 Y26 Y28 Y29 AA16 AA17 AB16 AB19 AC16 AC17 AC19 AD15 AD16 AD17 AF16 AF19 AH15 AH16 AH17 AH19 AJ16 AJ17 AJ19 AK16 AK19 AL16 AL17 AL19 AL20 AL21 AL23 AM15 AM16 AM19 AM20 AM21 AM23 AP15 AP16 AP17 AP19 AP20 AP21 AP23 AP24 AR20 AR21 AR23 AR24 AR26 V26 V28 V29 Y31

VCC SM LF

VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7

AW45 BC39 BE39 BD17 BD4 AW8 AT6

VCCSM_LF1 VCCSM_LF2 VCCSM_LF3 VCCSM_LF4 VCCSM_LF5 VCCSM_LF6 VCCSM_LF7

C129 .1U/10V/04 C172 .1U/10V/04 C222 0.22U/10V/06 C174 0.22U/10V/06 C212 0.47U/10V/06 C155 1U/10V/06 C145 1U/10V/06

CRESTLINE_1p0

+3V

R500 10_04 +VCC_GMCH_L D32 CH751H-40PT

Ivcc (External GFX 1.310 A, integrate 1.572 A)

+1.05V

C670 220U/2.5V C663 22U/4V/08 C115 0.22U/10V/06 C90 0.22U/10V/06 C106 .1U/10V/04

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

+VCC_AXG +1.05V

C91 *330U/6.3V C108 *330U/6.3V

SI-2 modified --remove ~~C91&C108~~

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

C118 .1U/10V/04 C110 .1U/10V/04 C116 0.47U/10V/06 C79 1U/10V/06 C68 10U/6.3V/08 C73 22U/4V/08

for IAMT power if not support need to connection to S0 power

| GMCH 1.05V | current(A) | Remark |
|---|---|---|
| VCC Core | 1.573 | ( 1.3A for external GFX ) |
| VCC_AXG | 7.7 | for integrated Gfx |
| VCC_AXD | 0.2 | |
| VTT | 0.85 | FSB VCCP |
| VCC_PEG | 1.2 | for PCIEG |
| VCC_AXM | 0.54 | for IAMT function |
| VCCR_RX_DMI | 0.25 | DMI |
| SUM | 12.313 | |

+1.05V

Ivcc_AXM Controller supply current 540mA

C105 .1U/10V/04 C94 .1U/10V/04 C113 .1U/10V/04

Layout Note: Inside GMCH cavity.

C124 22U/4V/08 C123 0.22U/10V/06 C99 0.22U/10V/06

Layout Note: Place close to GMCH edge.

U34F

VCC NCTF

VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38 VCC_NCTF_39 VCC_NCTF_40 VCC_NCTF_41 VCC_NCTF_42 VCC_NCTF_43 VCC_NCTF_44 VCC_NCTF_45 VCC_NCTF_46 VCC_NCTF_47 VCC_NCTF_48 VCC_NCTF_49 VCC_NCTF_50

AB33 AB36 AB37 AC33 AC35 AC36 AD35 AD36 AF33 AF36 AH33 AH35 AH36 AH37 AJ33 AJ35 AK33 AK35 AK36 AK37 AD33 AJ36 AM35 AL33 AL35 AA33 AA35 AA36 AP35 AP36 AR35 AR36 Y32 Y33 Y35 Y36 Y37 T30 T34 T35 U29 U31 U32 U33 U35 U36 V32 V33 V36 V37

VSS NCTF

VSS_NCTF_1 VSS_NCTF_2 VSS_NCTF_3 VSS_NCTF_4 VSS_NCTF_5 VSS_NCTF_6 VSS_NCTF_7 VSS_NCTF_8 VSS_NCTF_9 VSS_NCTF_10 VSS_NCTF_11 VSS_NCTF_12 VSS_NCTF_13 VSS_NCTF_14 VSS_NCTF_15 VSS_NCTF_16 VSS_NCTF_17 VSS_NCTF_18 VSS_NCTF_19 VSS_NCTF_20 VSS_NCTF_21

T27 T37 U24 U28 V31 V35 AA19 AB17 AB35 AD19 AD37 AF17 AF35 AK17 AM17 AM24 AP26 AP28 AR15 AR19 AR28

POWER

VSS SCB

VSS_SCB1 VSS_SCB2 VSS_SCB3 VSS_SCB4 VSS_SCB5 VSS_SCB6

A3 B2 C1 BL1 BL51 A51

+1.05V

VCC AXM

VCC_AXM_1 VCC_AXM_2 VCC_AXM_3 VCC_AXM_4 VCC_AXM_5 VCC_AXM_6 VCC_AXM_7

AT33 AT31 AK29 AK24 AK23 AJ26 AJ23

VCC AXM NCTF

VCC_AXM_NCTF_1 VCC_AXM_NCTF_2 VCC_AXM_NCTF_3 VCC_AXM_NCTF_4 VCC_AXM_NCTF_5 VCC_AXM_NCTF_6 VCC_AXM_NCTF_7 VCC_AXM_NCTF_8 VCC_AXM_NCTF_9 VCC_AXM_NCTF_10 VCC_AXM_NCTF_11 VCC_AXM_NCTF_12 VCC_AXM_NCTF_13 VCC_AXM_NCTF_14 VCC_AXM_NCTF_15 VCC_AXM_NCTF_16 VCC_AXM_NCTF_17 VCC_AXM_NCTF_18 VCC_AXM_NCTF_19

AL24 AL26 AL28 AM26 AM28 AM29 AM31 AM32 AM33 AP29 AP31 AP32 AP33 AL29 AL31 AL32 AR31 AR32 AR33

CRESTLINE_1p0

1.8VSUS

C267 .1U/10V/04 C744 330U/6.3V

Layout Note: Place C901 where LVDS and DDR2 taps.

+1.8VSUS_GMCH

C265 22U/4V/08 C266 22U/4V/08

Layout Note: Place on the edge.

NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Crestline (VCC, NCTF) | 2A |

Date: Monday, April 30, 2007 Sheet 8 of 37

## CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

| Ball | Enable | Disable | Ball | Enable | Disable |
|---|---|---|---|---|---|
| VCCA_CRT_DAC | 3.3V | GND | VCCA_TVC_DAC | 3.3V | GND |
| VCCD_CRT | 1.5V | GND | VCCD_TVDAC | 1.5V | 1.5V |
| VCCD_QDAC | 1.5V | GND | VCCA_DAC_BG | 3.3V | GND |
| VCCA_TVA_DAC | 3.3V | GND | VSS_DAC_BG | GND | GND |
| VCCA_TVB_DAC | 3.3V | GND | VCCSYNC | 3.3V | GND |

## LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

| Signal | If SDVO Disable LVDS Disable | If LVDS enable |
|---|---|---|
| VCCD_LVDS | GND | 1.8V |
| VCCA_LVDS | GND | 1.8V |
| VCC_TX_LVDS | GND | 1.8V |

9

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_180ohm+-25%
_100mHz_1500mA
_0.09ohm DC

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

10uH+-20%_100mA

0.1Caps should be placed 200 mils with in its pins.

SI-1 modify
( NET name
wrong )

POWER

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXF

Ivcca_PEG_BG supply current 100mA

Ivcc_PEG supply current 1.2A

SI-1 modified change

Ivcc_RX_DMI supply current 250mA

1uH+-20%_300mA

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

+3V_VCC_HV

40 mil wide

CRESTLINE_1p0

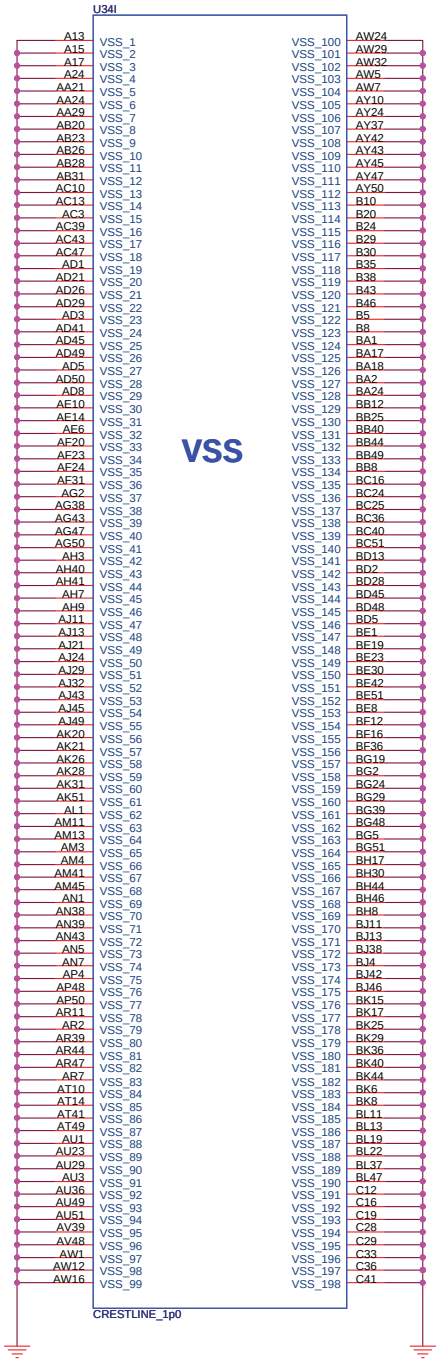


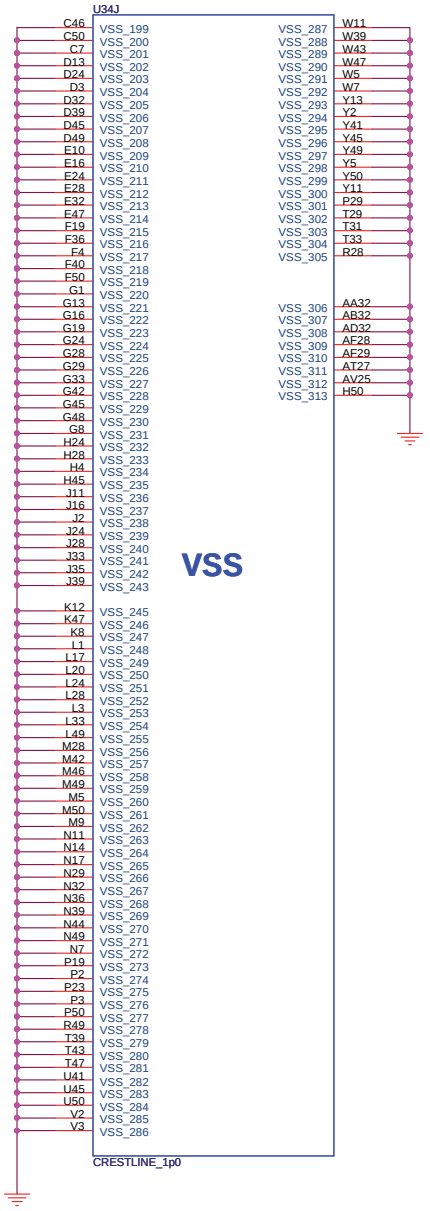
PROJECT : AT3U
Quanta Computer Inc.

Size: Custom | Document Number: Crestline (POWER) | Rev: 2A

Date: Monday, April 30, 2007 | Sheet 9 of 37

N85/RD1/HW2



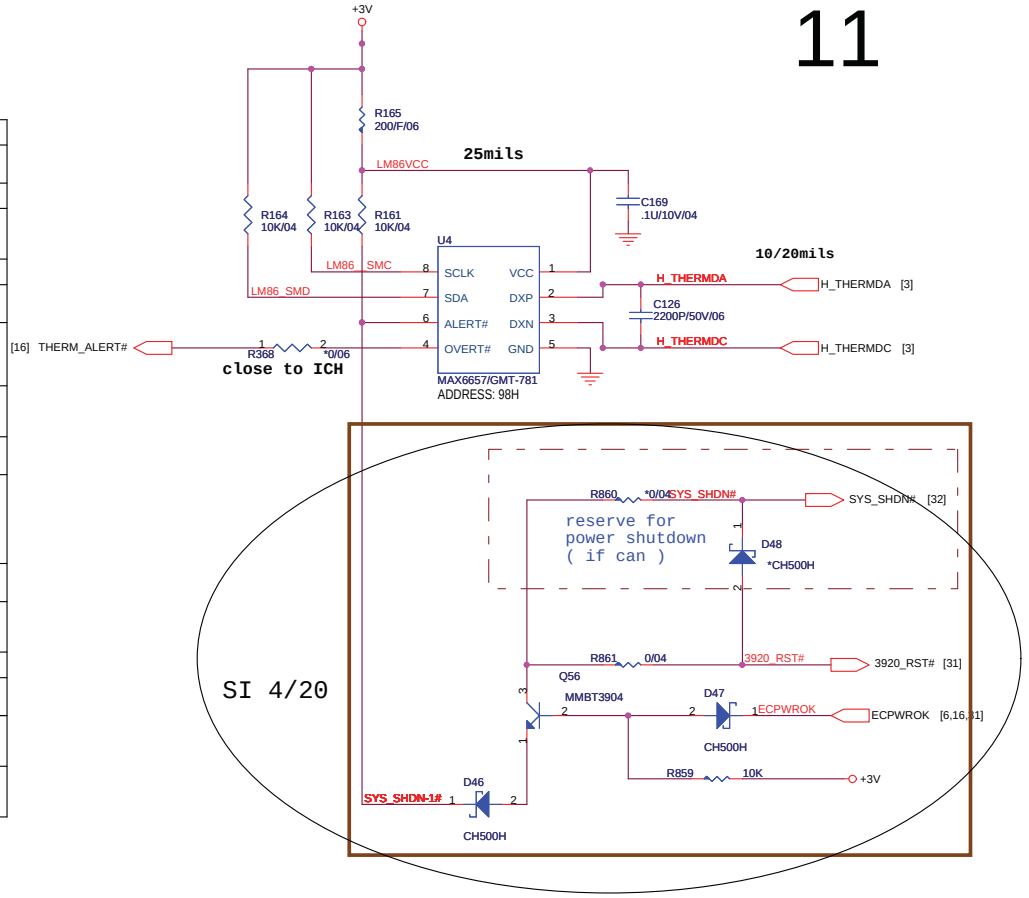




| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: Crestline (VSS) | Rev: 2A |
| Date: Monday, April 30, 2007 | Sheet 10 of 37 | |

## Strap table

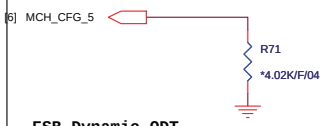
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

| Pin Name | Strap description | Configuration |
|---|---|---|
| CFG[2:0] | FSB Frequency Select | 010 = FSB 800MHz<br>011 = FSB 667MHz |
| CFG[4:3] | Reserved | |
| CFG5 | DMI X2 Select | 0 = DMI X2<br>1 = DMI X4(Default) |
| CFG6 | Reserved | |
| CFG7 | CPU Strap | 0 = Reserved<br>1 = Mobile CPU(Default) |
| CFG8 | Low power PCI Express | 0 = Normal mode<br>1 = Low Power mode |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reverse Lanes<br>1 = Normal operation(Default) |
| CFG[11:10] | Reserved | |
| CFG[13:12] | XOR/ALLZ | 00 = Reserved<br>01 = XOR Mode Enable<br>10 = All-Z Mode Enabled<br>11 = Normal operation(Default) |
| CFG[15:14] | Reserved | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT disable<br>1 = Dynamic ODT Enable(Default) |
| CFG[18:17] | Reserved | |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card present(Default)<br>1 = SDVO Card Present |
| CFG19 | DMI Lane Reversal | 0 = Normal operation(Default)<br>1 = Reverse Lanes |
| CFG20 | SDVO/PCIe concurrent | 0 = Only SDVO or PCIE x1 is operation(Default)<br>1 = SDVO and PCIE x1 are operating simultaneously via the PEG port |



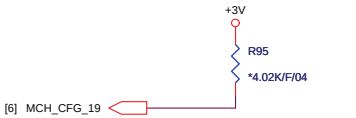

### DMI X2 Select

| | |
|---|---|
| MCH_CFG_5 | Low = DMIX2<br>High = IDMIX4(Default) |



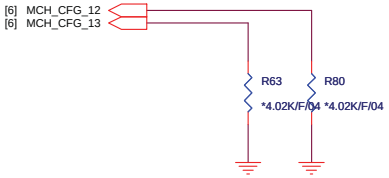

### DMI Lane Reversal

| | |
|---|---|
| MCH_CFG_19 | Low = Normal operation(Default)<br>High = Reverse Lane |



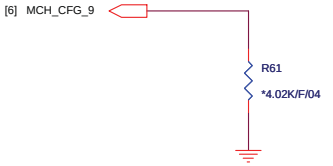

### XOR /ALLz /Clock Un-gating

| MCH_CFG_12 | MCH_CFG_13 | Configuration |
|---|---|---|
| 0 | 0 | Clock gating disable |
| 0 | 1 | XOR Mode Enable |
| 1 | 0 | ALL-z Mode Enable |
| 1 | 1 | Normal operation(Default) |



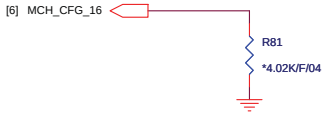

### PCI Express Graphics

| | |
|---|---|
| MCH_CFG_9 | Low = Reverse Lane<br>High = Normal operation(Default) |



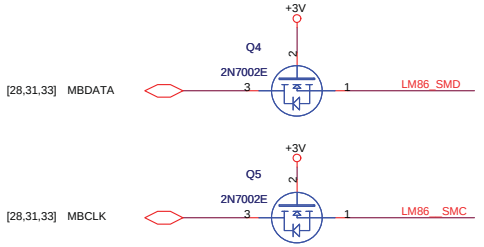

### FSB Dynamic ODT

| | |
|---|---|
| MCH_CFG_16 | Low = ODT Disable<br>High = ODT Enable(Default) |




### SDVO/PCIE Concurrent operation

| | |
|---|---|
| MCH_CFG_20 | Low = Only SDVO or PCIE X1 is operational(Default)<br>High = SDVO andPCIE X1 are operating simultaneously via the PEG port |


**SDVO Present**

**Strap define at External DVI control page**

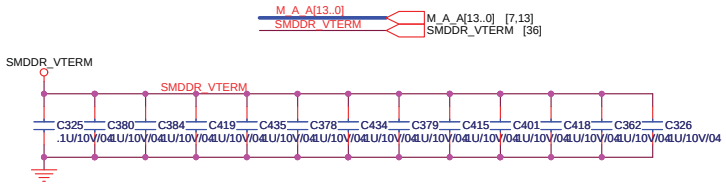
**PROJECT : AT3U**
Quanta Computer Inc.

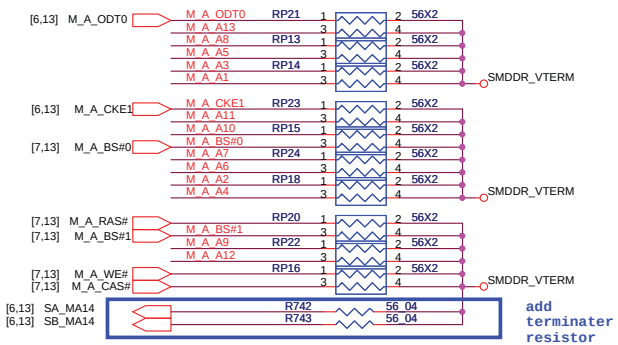
| Size | Document Number | Rev |
|---|---|---|
| Custom | 10 -- GMCH STRAP-3(6 of 6) | 2A |
| NB5/RD1/HW2 | Date: Wednesday, May 02, 2007 | Sheet 11 of 37 |

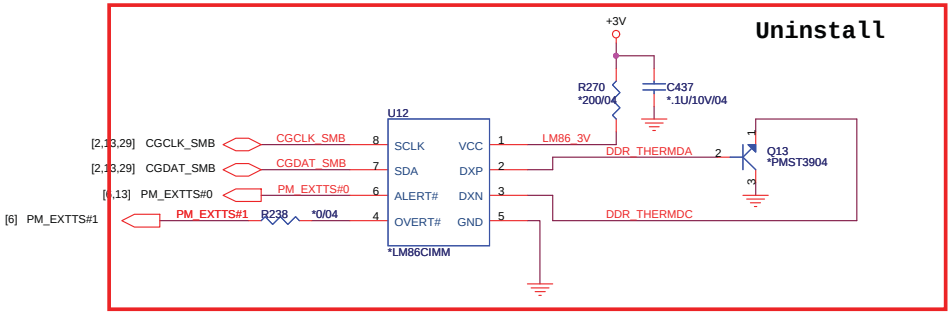
# DDRII DUAL CHANNEL A,B.



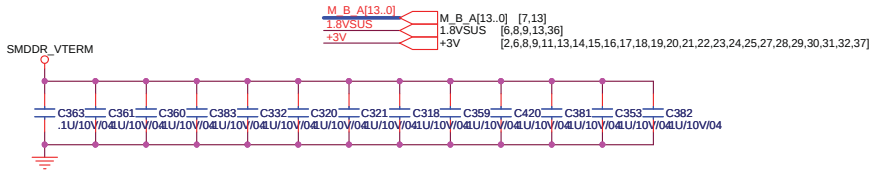
## DDRII A CHANNEL



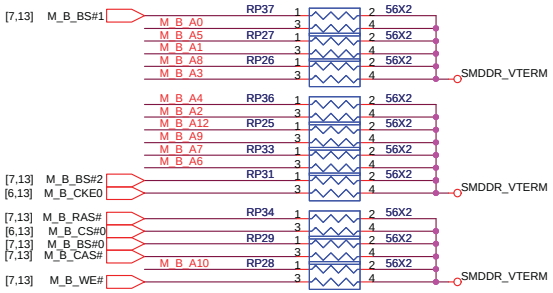



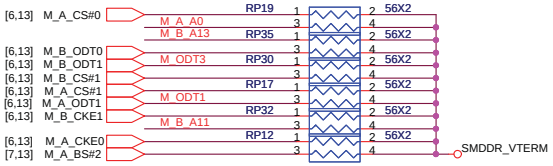




## DDRII B CHANNEL




Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM




| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| | Size: Custom<br>Document Number: DDRII RES.ARRAY | Rev: 2A |
| | Date: Wednesday, May 02, 2007 | Sheet 12 of 37 |

CGCLK_SMB [2,12,29]
CGDAT_SMB [2,12,29]

M_A_CKE[0..1] [6,12]
M_A_CS#[0..1] [6,12]
M_A_RAS# [7,12]
M_A_CAS# [7,12]
M_A_WE# [7,12]
M_A_CLK0 [6]
M_A_CLK0# [6]
M_A_CLK1 [6]
M_A_CLK1# [6]
M_A_BS#[0..2] [7,12]
M_A_ODT[0..1] [6,12]
M_A_DQM[0..7] [7]
M_A_DQ[0..63] [7]
M_A_DQS[0..7] [7]
M_A_DQS#[0..7] [7]
M_A_A[13..0] [7,12]

+3V [2,6,8,9,11,12,14,15,16,17,18,19,20,21,22,23,24,25,27,28,29,30,31,32,37]
1.8VSUS [6,8,9,36]

M_B_CKE[0..1] [6,12]
M_B_CS#[0..1] [6,12]
M_B_RAS# [7,12]
M_B_CAS# [7,12]
M_B_WE# [7,12]
M_B_CLK0 [6]
M_B_CLK0# [6]
M_B_CLK1 [6]
M_B_CLK1# [6]
M_B_BS#[0..2] [7,12]
M_B_ODT[0..1] [6,12]
M_B_DQM[0..7] [7]
M_B_DQ[0..63] [7]
M_B_DQS[0..7] [7]
M_B_DQS#[0..7] [7]
M_B_A[13..0] [7,12]

## CKEA 0,1

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26A

H 9.2

## CKEB 0,1

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR
CN24A

H 5.2

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM
SB_MA14 [6,12]
PM_EXTTS#0 [6,12]

FOX=AS0A426-M2S-TR
CN26B

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM
SA_MA14 [6,12]
PM_EXTTS#0

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
R226 0/06 SMDDR_VREF [6,36]
R227 1.8VSUS
R603 *10K/F/06
*10K/F/06

DIM2_SA0 R267 10K/04
DIM2_SA1 R268 10K/04 +3V
SMbus address A4

R216 10K/04 DIM1_SA0
R217 10K/04 DIM1_SA1
SMbus address A0

### Place these Caps near So-Dimm1.

1.8VSUS
C773 2.2U/6.3V/06 C775 2.2U/6.3V/06 C785 2.2U/6.3V/06 C444 2.2U/6.3V/06 C764 2.2U/6.3V/06 C770 .1U/10V/04 C788 .1U/10V/04 C439 .1U/10V/04 C433 .1U/10V/04 C769 .1U/10V/04 C767 .1U/10V/04

SMDDR_VREF_DIMM
C772 .1U/10V/04 C768 2.2U/6.3V/06

+3V
C317 2.2U/6.3V/06 C316 .1U/10V/04

**SO-DIMM BYPASS PLACEMENT :**
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

### Place these Caps near So-Dimm2.

1.8VSUS
C774 2.2U/6.3V/06 C786 2.2U/6.3V/06 C784 2.2U/6.3V/06 C759 2.2U/6.3V/06 C760 .1U/10V/04 C776 .1U/10V/04 C789 .1U/10V/04 C787 .1U/10V/04 C443 .1U/10V/04 C765 .1U/10V/04 C766 .1U/10V/04

SMDDR_VREF_DIMM
C371 .1U/10V/04 C373 2.2U/6.3V/06

+3V
C372 2.2U/6.3V/06 C385 .1U/10V/04

**SO-DIMM BYPASS PLACEMENT :**
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

**PROJECT : AT3U**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDRII SO-DIMM(200P) | 2A |
| Date: Wednesday, May 02, 2007 | Sheet 13 of 37 | |

# RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

change to battery conn

add RTC Bat rechargeable circuit

20MIL 20MIL

U42A

ICH8M REV 1.0

for fix ESD issue

Should be 2" close ICH7

Place within 500 mils of ICH7

25mils/15mils

intel check list define to stuff 33ohm

## SB Strap

**ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)**

| | |
|---|---|
| INTVRMEN | Low = Internal VR disable<br>High = Internal VR enable(Default) |

**ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)**

| | |
|---|---|
| LAN100_SLP | Low = Internal VR disable<br>High = Internal VR enable(Default) |

**XOR Chain Entrance Strap**

| ICH_RSV0 | HDA_SDOUT | Description |
|---|---|---|
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal opration(Default) |
| 1 | 1 | Set PCIE port config bit 1 |

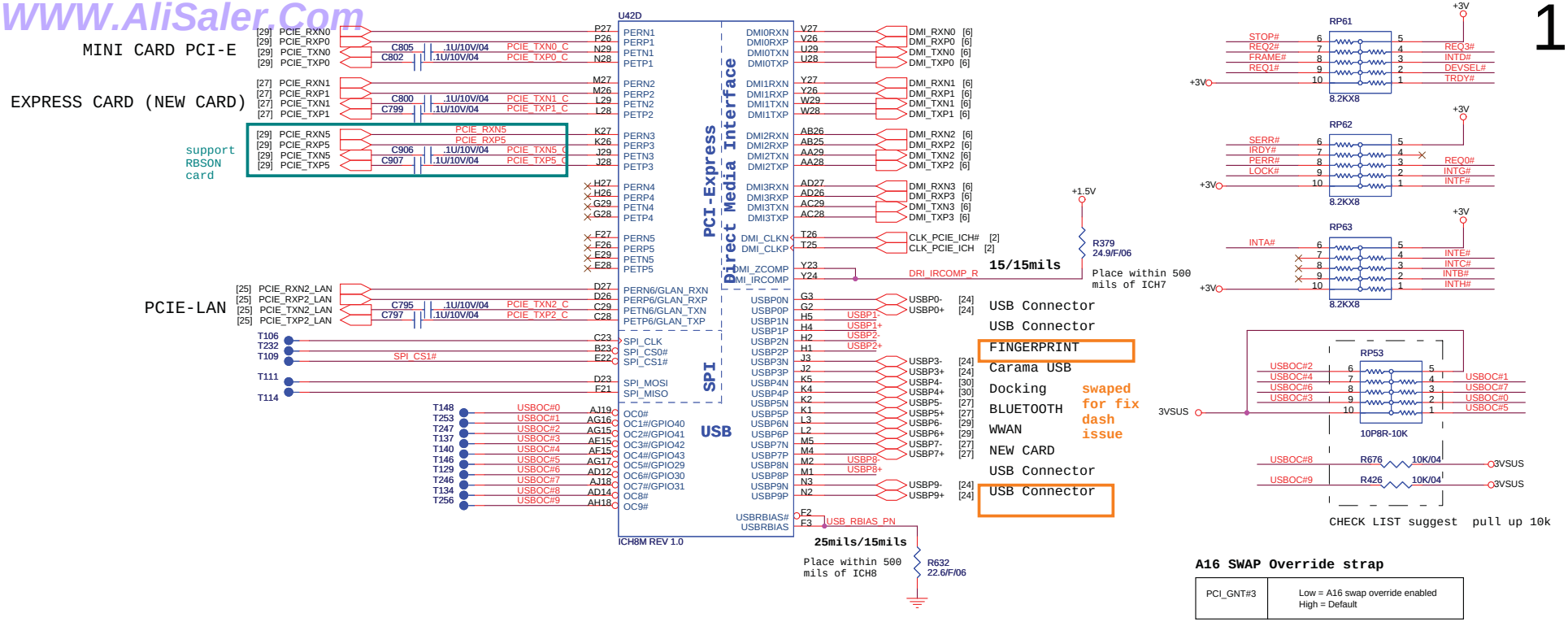
| | |
|---|---|
| PROJECT : | AT3U |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: ICH7-M HOST(1/4) Rev: 2A |
| NB5/RD1/HW2 | Date: Wednesday, May 02, 2007 Sheet 14 of 37 |

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

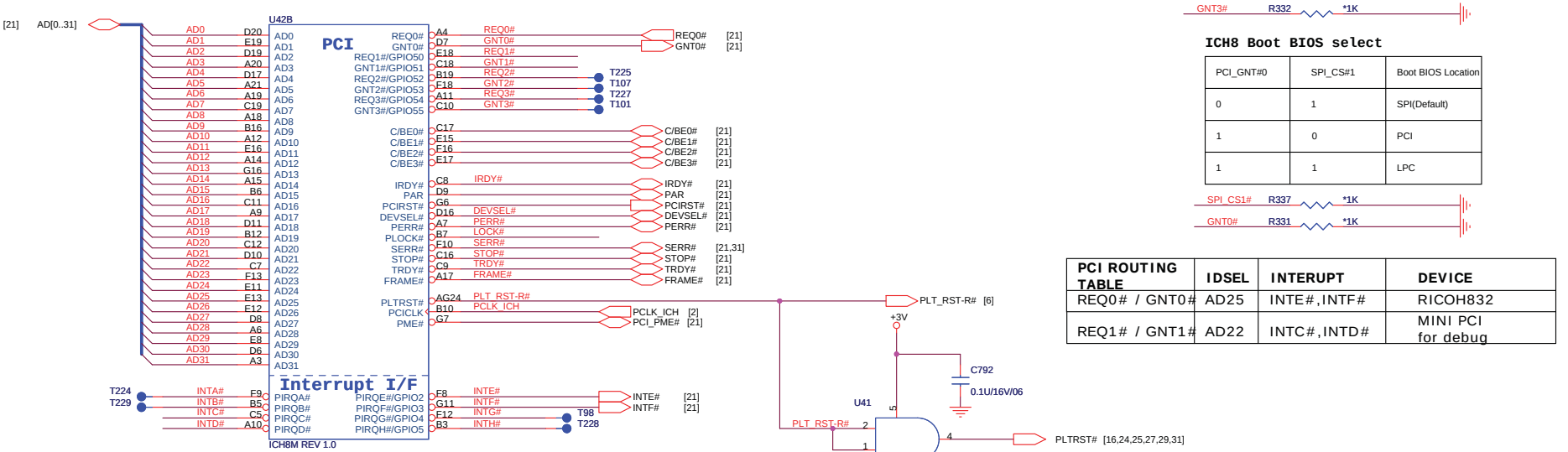
support RBSON card

PCIE-LAN










**A16 SWAP Override strap**

| | |
|---|---|
| PCI_GNT#3 | Low = A16 swap override enabled<br>High = Default |

GNT3# R332 *1K

**ICH8 Boot BIOS select**

| PCI_GNT#0 | SPI_CS#1 | Boot BIOS Location |
|---|---|---|
| 0 | 1 | SPI(Default) |
| 1 | 0 | PCI |
| 1 | 1 | LPC |

SPI_CS1# R337 *1K

GNT0# R331 *1K

| PCI ROUTING TABLE | IDSEL | INTERUPT | DEVICE |
|---|---|---|---|
| REQ0# / GNT0# | AD25 | INTE#,INTF# | RICOH832 |
| REQ1# / GNT1# | AD22 | INTC#,INTD# | MINI PCI for debug |

NB5/RD1/HW2

**PROJECT : AT3U**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | ICH7-M M PCI E(2/4) | 2A |
| Date: Wednesday, May 02, 2007 | Sheet 15 of 37 | |

fix re-boot fail

R833 2K/F/04 — [35] VR_PWRGD_CK410# — U26 NL17SZ14DFT2G — C608 1U/16V/04 — VR_PWRGD_CK410

R809 100K/04

PCLK_SMB R617 2.2K/06 — PDAT_SMB R272 2.2K/06 — PCIE_WAKE# R399 1K/06 — PM_BATLOW# R R387 8.2K/06

SMB_LINK_ALERT# R621 10K/06 — SMLINK0 R619 10K/06 — SMLINK1 R618 10K/06

RI# R624 8.2K/06 — DNBSWON# R271 10K/06 — SYS_RST#-1 R615 10K/06 — SMB_ALERT# R273 10K/06

KBSMI# R R281 10K/06

SWI# R R280 10K/06

CLKRUN# R433 8.2K/06 — SERIRQ R656 8.2K/06 — SCI# R R662 10K/06

PM_RSMRST# R R658 10K/06

these pin if unused require 8.2k to 10k pull-up to +3v

SI-1 add

U42C ICH8M REV 1.0

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1

SYS GPIO: RI#, SUS_STAT#/LPCPD#, SYS_RESET#, BMBUSY#/GPIO0, SMBALERT#/GPIO11, STP_PCI#/GPIO15, STP_CPU#/GPIO25, CLKRUN#/GPIO32, WAKE#, SERIRQ, THRM#, VRMPWRGD, TP7

GPIO: TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, GPIO12, TACH0/GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SPKR, MCH_SYNC#, TP3

Controller Link: MEM_LED/GPIO24, ME_EC_ALERT/GPIO10, EC_ME_ALERT/GPIO14, WOL_EN/GPIO9

SATA GPIO: SATA0GP/GPIO21, SATA1GP/GPIO19, SATA2GP/GPIO36, SATA3GP/GPIO37

Clocks: CLK14, CLK48, SUSCLK

Power MGT: SLP_S3#, SLP_S4#, SLP_S5#, S4_STATE#/GPIO26, PWROK, DPRSLPVR/GPIO16, BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, CK_PWRGD, CLPWROK, SLP_M#, CL_CLK0, CL_CLK1, CL_DATA0, CL_DATA1, CL_VREF0, CL_VREF1, CL_RST#

BOARD_ID1 T108 — BOARD_ID0 T130 — BOARD_ID3 T249 — BOARD_ID4 T251

14M_ICH R856 *33/04 — CLKUSB_48 R857 33_04 — C953 10P/04 — C952 *10P/04

SUSB# [31] — SUSC# [31] — R616 100/F/06 — R326 100/F/06

100ohm to 499 ohm check list -- series 500ohm to IMVP6+

R620 499/F — DPRSLPVR [6,35]

PM_BATLOW# [31] — DNBSWON# [31] — R642 0/04

C819 *1U/16V/04 — R665 *100/F/06 — R666 100/F/06 — LAN_REST [25,31] — PLTRST# [15,24,25,27,29,31]

R659 100/F/06 RSMRST# — RSMRST# [31]

CK_PWG [2] — R623 0/04

ECPWROK [6,11,31] — R622 0/04

CL_CLK0 [6] — CL_CLK1 [29]

CL_DATA0 [6] — CL_DATA1 [29]

CL_VREF0 SB — CL_VREF1 SB

CL_RST#0 [6,29]

BT_OFF# [27] — R284 0/04

LAN_RST pin : 1.if used pci LAN please tie to PLTRST# 2.if used PHY LAN please tie to RSMRST#

3V_S5 — R631 3.24K/F/06 — R633 453/F/04 — C798 1U/10V/04

Controller Link 1 VREF for IAMT support only

+3V — R338 3.24K/F/06 — R344 453/F/04 — C511 1U/10V/04

Controller Link 0 VREF for IAMT support only

R819 10K/04 — 3VSUS

ADD (ww36 request )

3/22

No Reboot strap

| | |
|---|---|
| HDA_SPKR | Low = Default<br>High = No Reboot |

ACZ_SPKR R411 *10K — +3V

SI-2 Change

CRB STUFF 2K%1 — R657 2K/F/04 — 3VSUS — C818 .047U/10V/04

[6,35] DELAY_VR_PWRGOOD — ECPWROK — U43 TC7SH08FU — ICH_PWROK — R667 10K/06 — R661 100K/06

| Board ID | 15 " AT3U 965GM DUAL HDD (0:0:1:1:1) BOARD ID 7 | |
|---|---|---|
| ID0 | R692 Stuff | R693 not Stuff |
| ID1 | R688 Stuff | R448 not Stuff |
| ID2 | R690 Stuff | R689 not Stuff |
| ID3 | R760 Stuff | R660 not Stuff |
| ID4 | R761 Stuff | R652 not Stuff |

R660 *10K/06 — BOARD_ID3 — R760 10K/06

R652 *10K/06 — BOARD_ID4 — R761 10K/06

R692 10K/06 — BOARD_ID0 — R693 *10K/06

R688 10K/06 — BOARD_ID1 — R448 *10K/06

R690 10K/06 — BOARD_ID2 — R689 *10K/06

NB5/RD1/HW2

**PROJECT : AT3U**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | ICH7-M GPIO(3/4) | 2A |

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1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A

V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCCHDA 32mA
VCC_SUSHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)

U42E — ICH8M REV 1.0
U42F — ICH8M REV 1.0

PROJECT : AT3U
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | ICH7-M POWER(4/4) | 2A |

Date: Monday, April 30, 2007 | Sheet 17 of 37

N85/RD1/HW2

# CRT PORT

fix CRT rise time issue

close conn within 600mils

EMI

## CRT SWITCH

fix CRT rise time issue

U51 74CBT3257

EMI

| inputs | | function |
|---|---|---|
| /E | SET | |
| L | L | Y - port 0 |
| L | H | Y - port 1 |
| H | X | Disconnect |

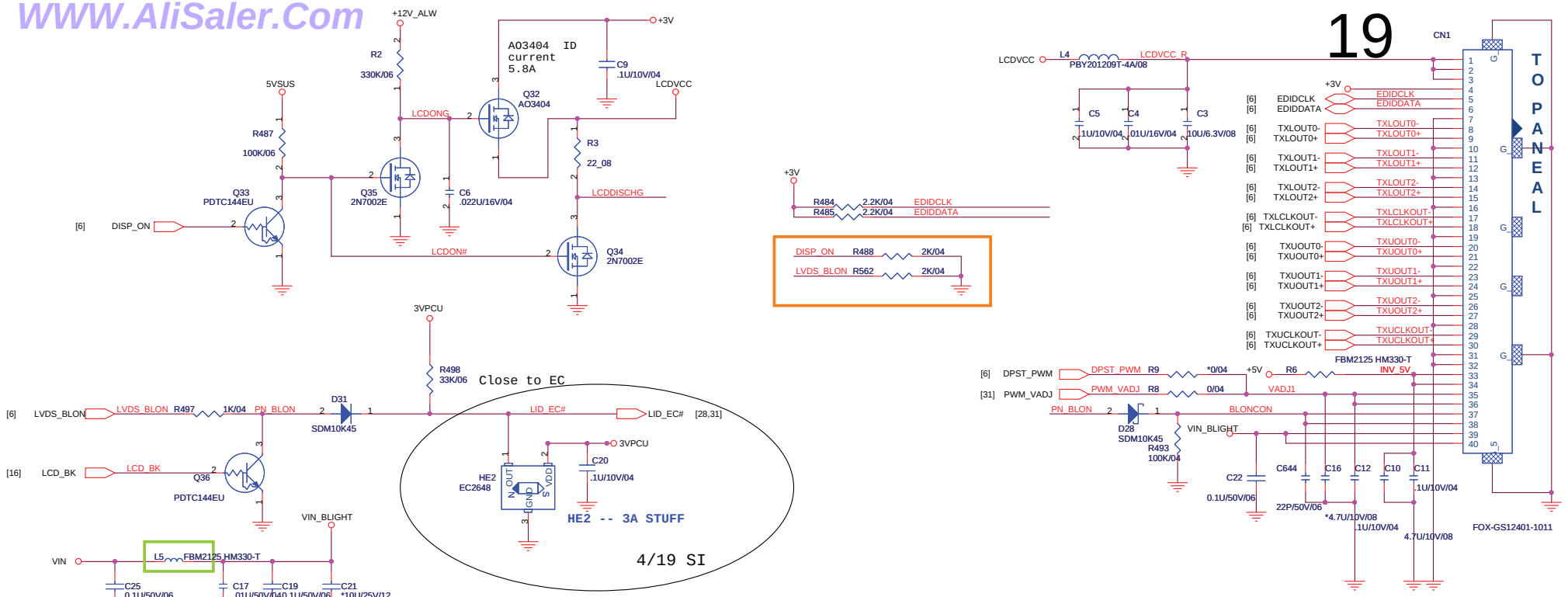
filter for HDTV

SI-1 MODIFY

## TV_OUT

SUY-030005FR007S102FU

| | |
|---|---|
| PROJECT : AT3U | |
| Quanta Computer Inc. | |
| Size: Custom | Document Number: CRT/TV_OUT |
| Rev: 2A | |
| NB5/RD1/HW2 | |
| Date: Wednesday, May 02, 2007 | Sheet 18 of 37 |





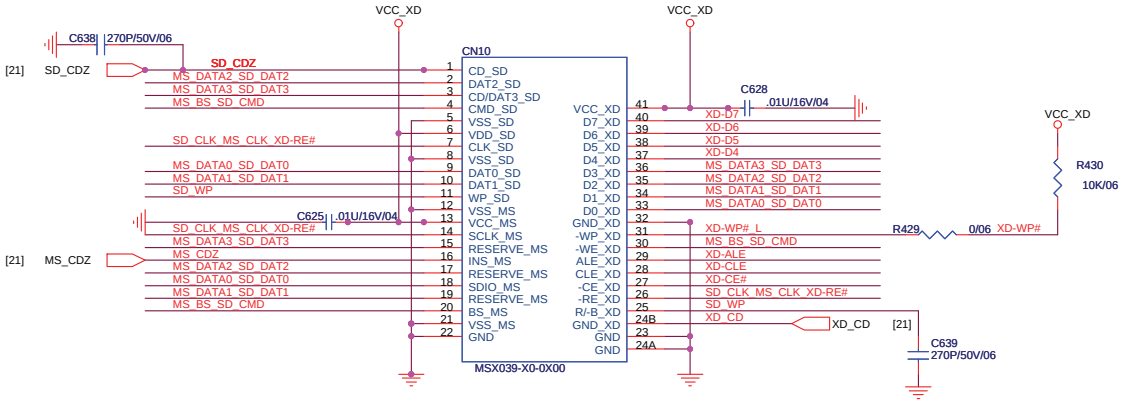


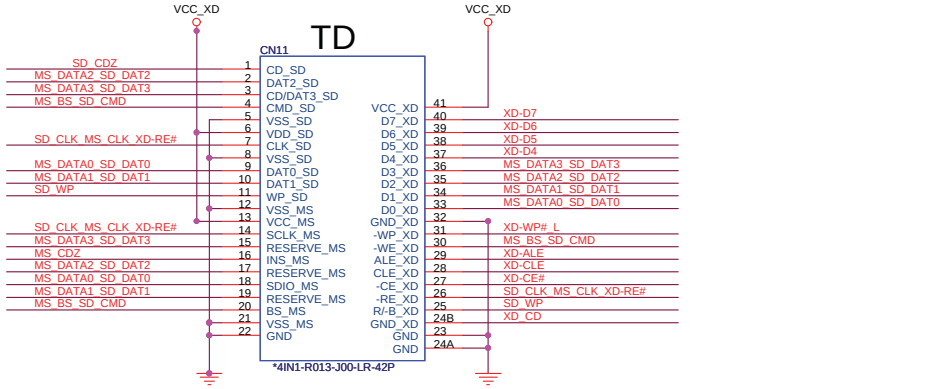



| | | | |
|---|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: LCD CONN | Rev: 2A |
| | Date: Wednesday, May 02, 2007 | Sheet 19 of 37 | |

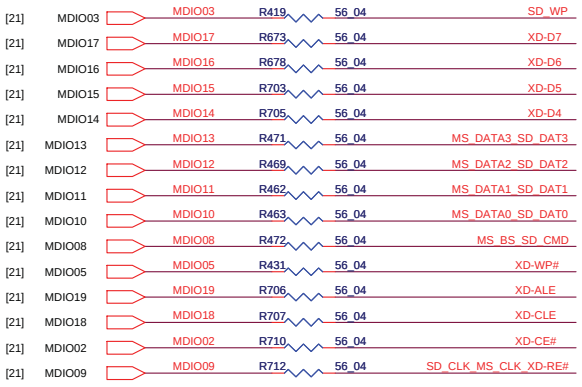
# 5 IN1 CARD READER
## XD,MMC/SD,MS/MSP

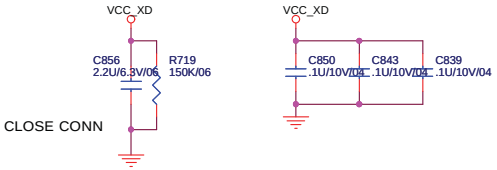


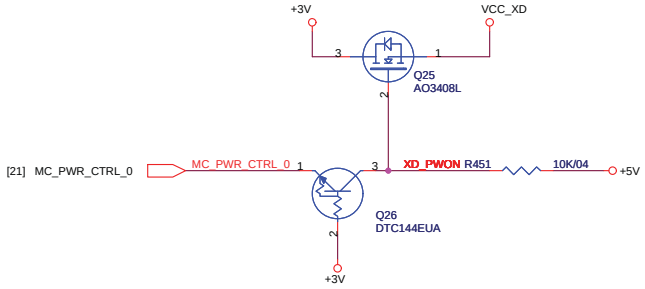


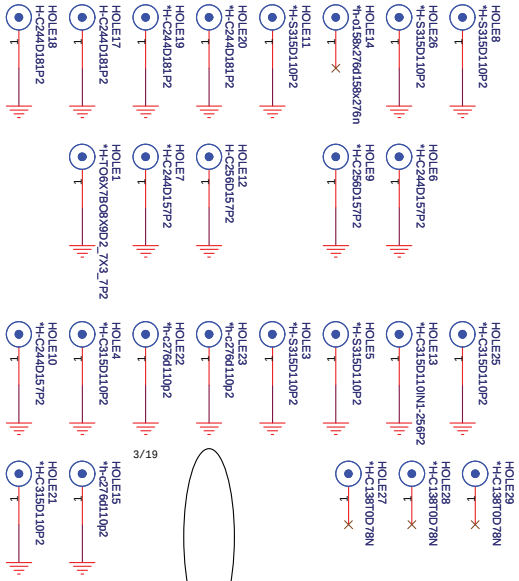

bom create 2'nd source



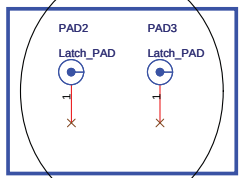

## SCREW HOLE

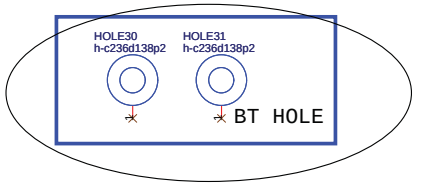


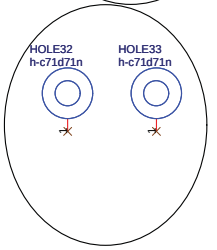

SI 4/20 del hole16

SI 4/30 del PAD1,9,10,13,16

BT PAD



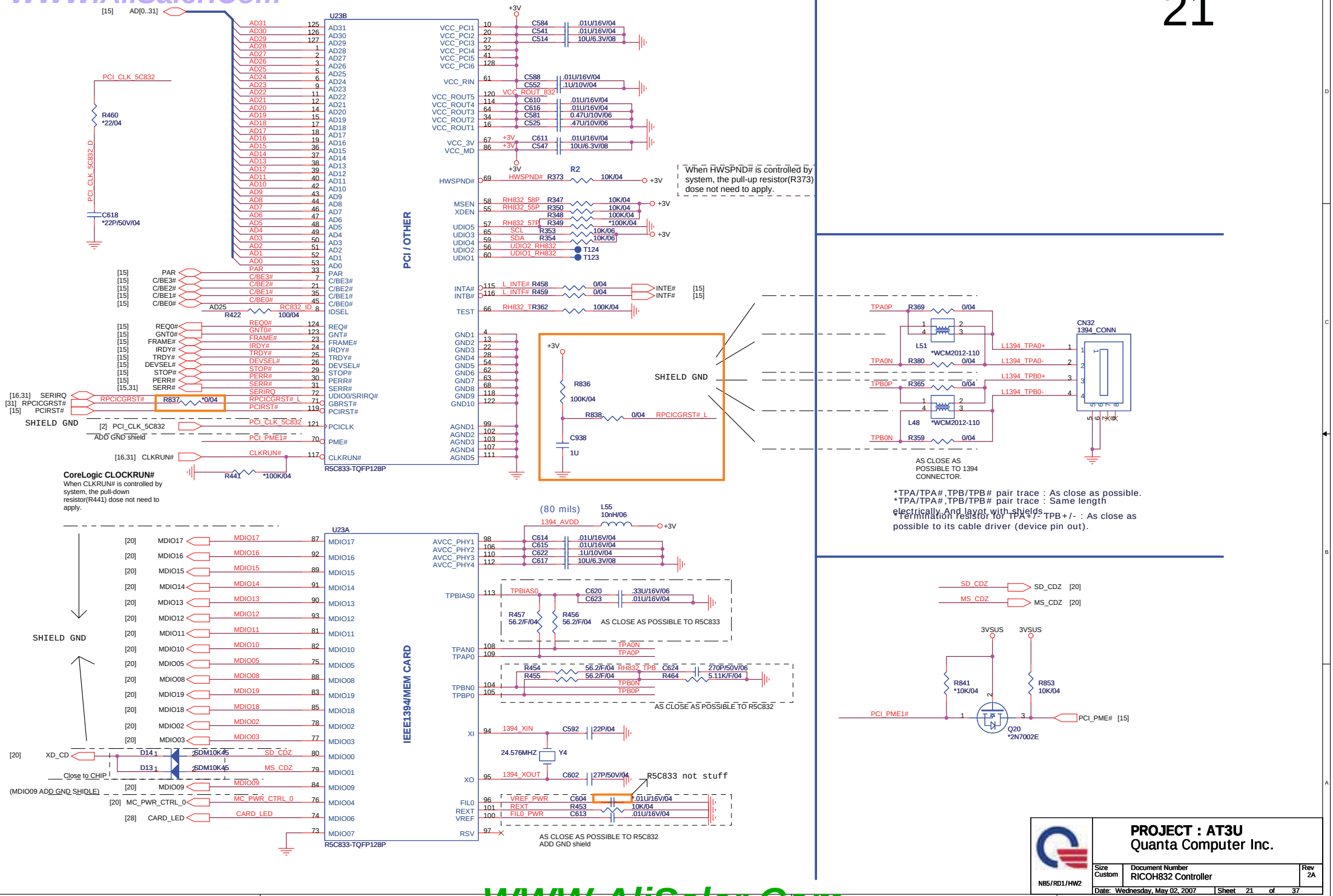




**PROJECT : AT3U**
Quanta Computer Inc.

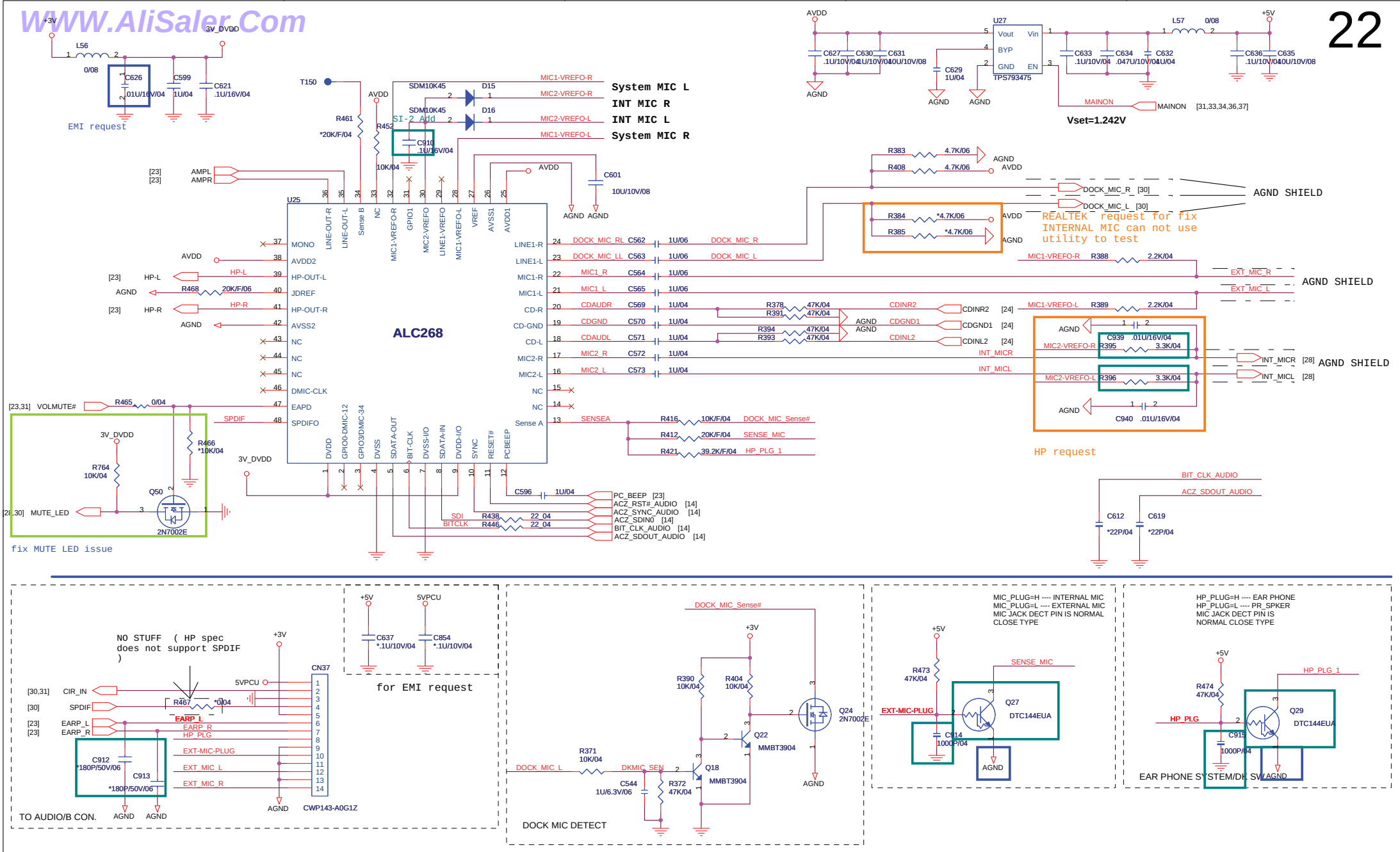
| Size | Document Number | Rev |
|---|---|---|
| Custom | CARD READER/HOLE | 1A |
| Date: Wednesday, May 02, 2007 | Sheet 20 of 37 | |

NB5/RD1/HW2




**PROJECT : AT3U**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | RICOH832 Controller | 2A |
| NB5/RD1/HW2 | Date: Wednesday, May 02, 2007 | Sheet 21 of 37 |



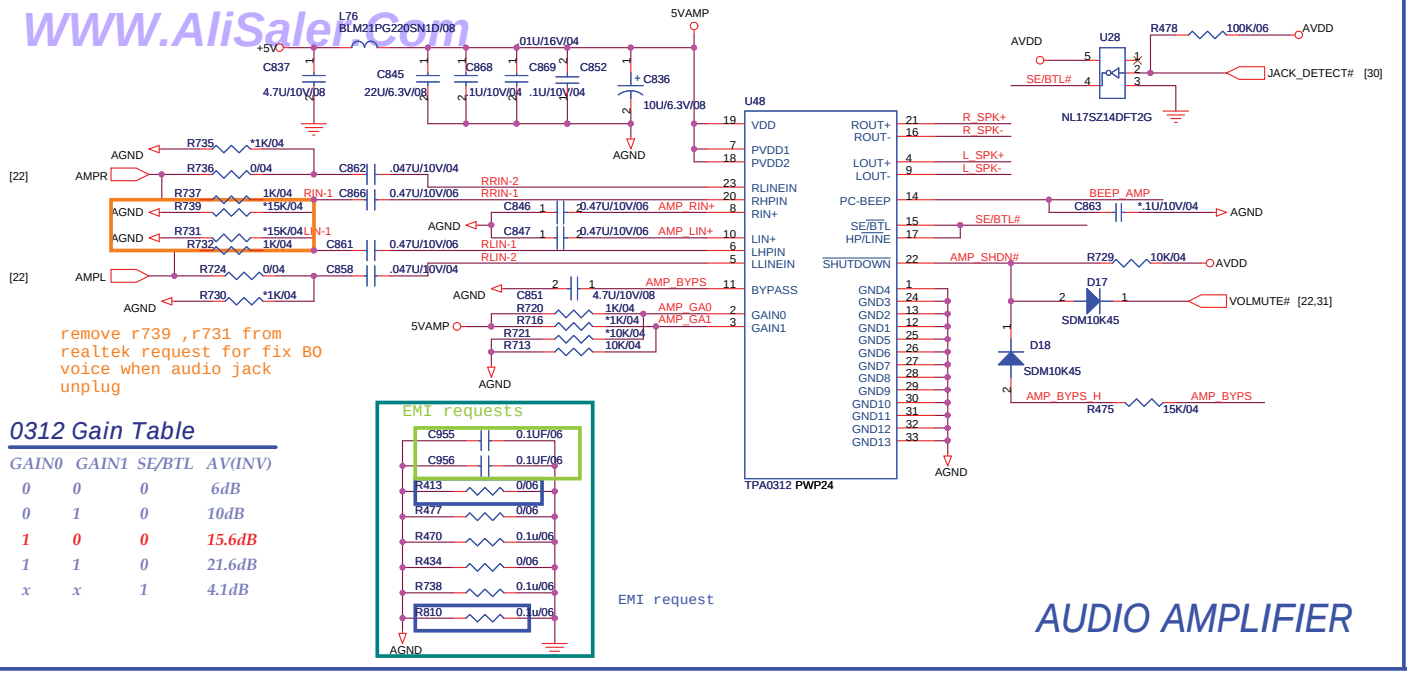

**PROJECT : AT3U**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Azalia CONEXANT20549-12 | 2A |

NB5/RD1/HW2

Date: Wednesday, May 02, 2007 Sheet 22 of 37

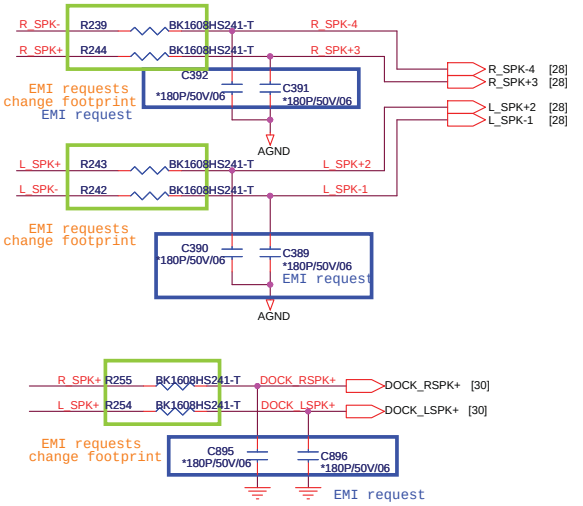
# AUDIO AMPLIFIER



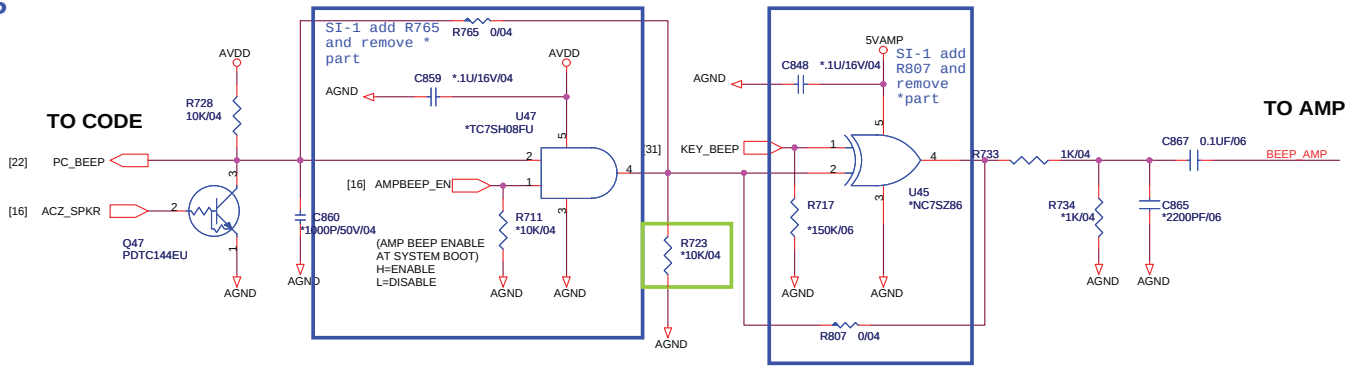

## 0312 Gain Table

| GAIN0 | GAIN1 | SE/BTL | AV(INV) |
|---|---|---|---|
| 0 | 0 | 0 | 6dB |
| 0 | 1 | 0 | 10dB |
| **1** | **0** | **0** | **15.6dB** |
| 1 | 1 | 0 | 21.6dB |
| x | x | 1 | 4.1dB |

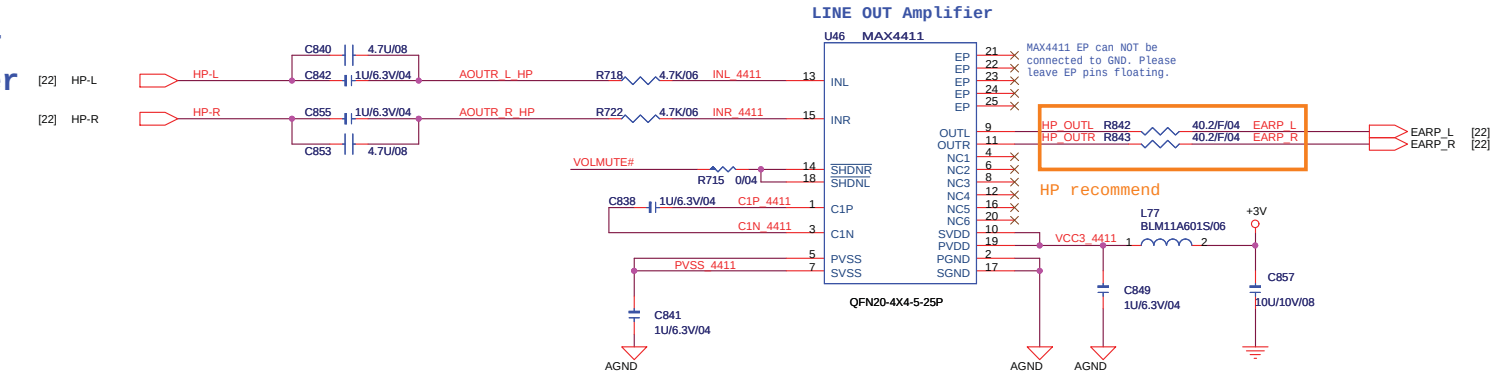
## INT. SPEAKER




## PCSPK BEEP

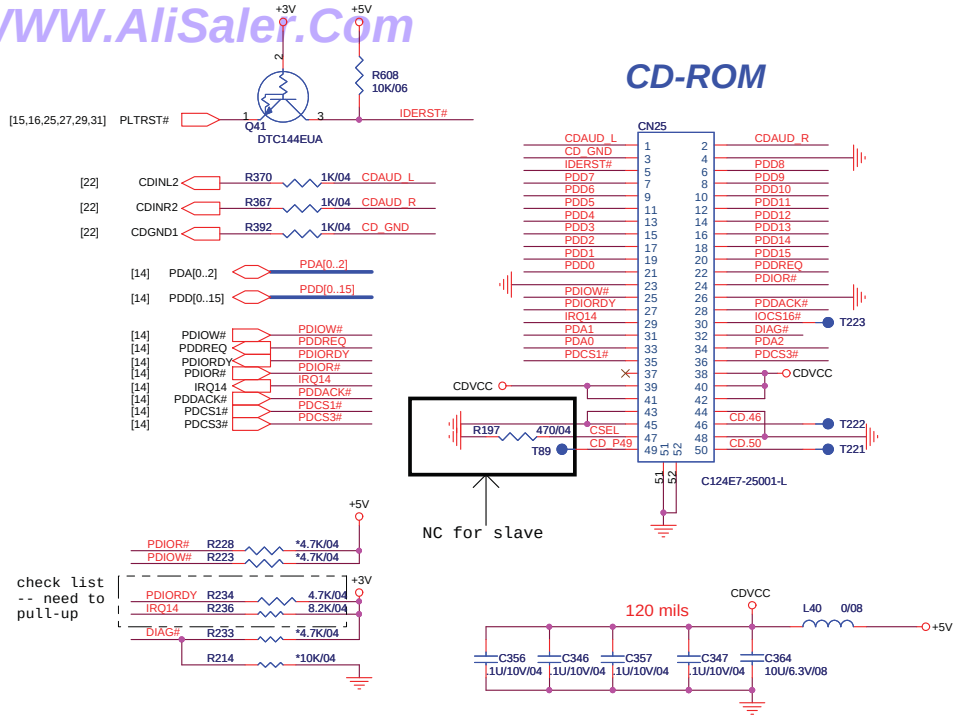



## LINE OUT Amplifier

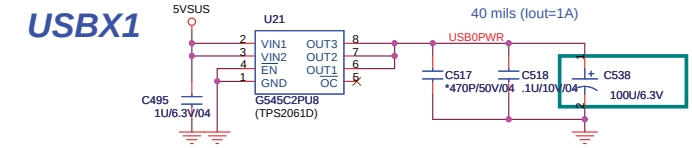



| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: JACK/AMP_TAP0312 | Rev: 2A |
| Date: Wednesday, May 02, 2007 | Sheet 23 of 37 | |

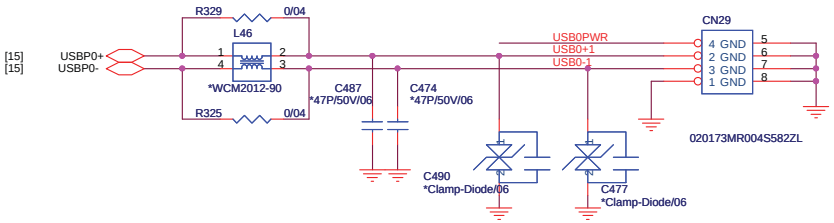
## CD-ROM



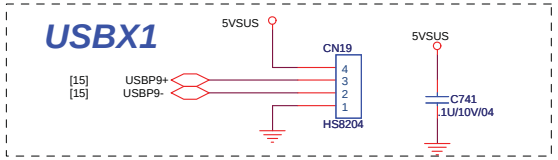

## USBX1



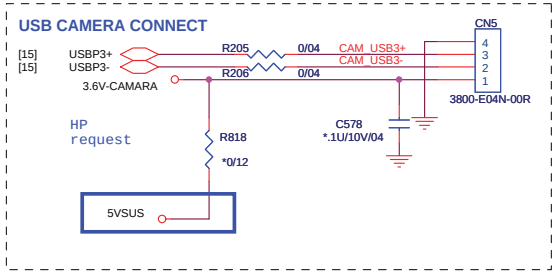

## USB 0

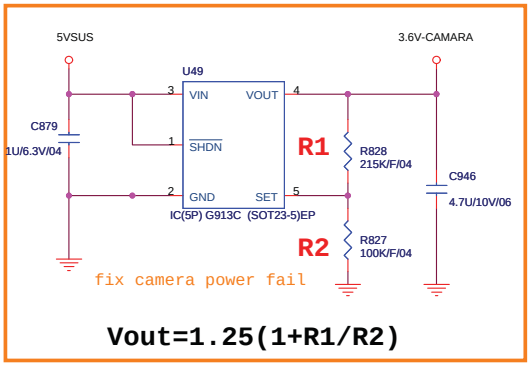



## USBX1

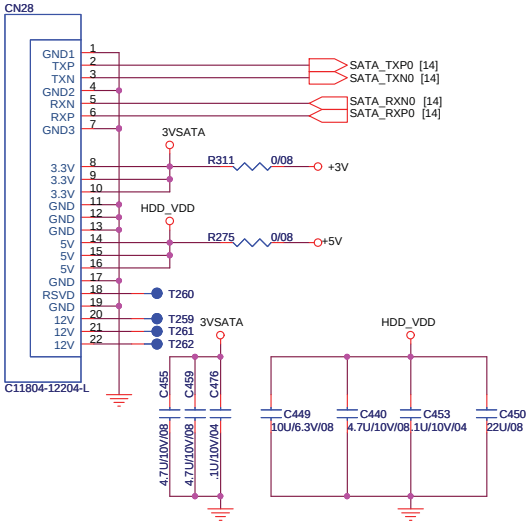



## USB CAMERA CONNECT




## SATA_2 CONNECTOR




| | | | |
|---|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: SATA HDD/CD-ROM/USBX2 | Rev: 2A |
| | Date: Wednesday, May 02, 2007 | Sheet 24 of 37 | |

E : Stuffed for 8101E(10/100)

fix 10/100 LAN LED issue

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

**BLOCK A is only for RTL8101E application.**

Block A

SI 4/20

RJ45

Remove R70 for 8111B and 8111C

for 93C56 used. NC if 93C46 is used.

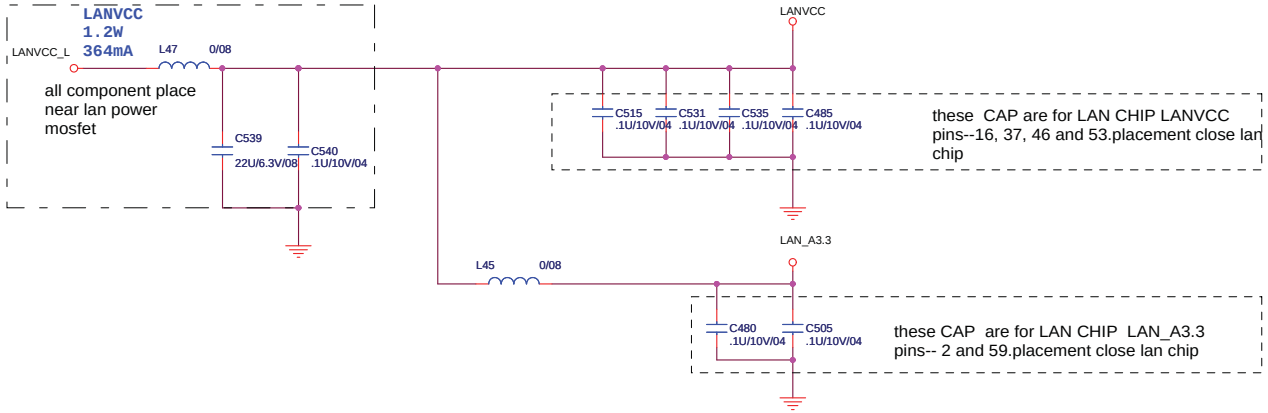
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs ( excluding PCIE_WAKE# pin )

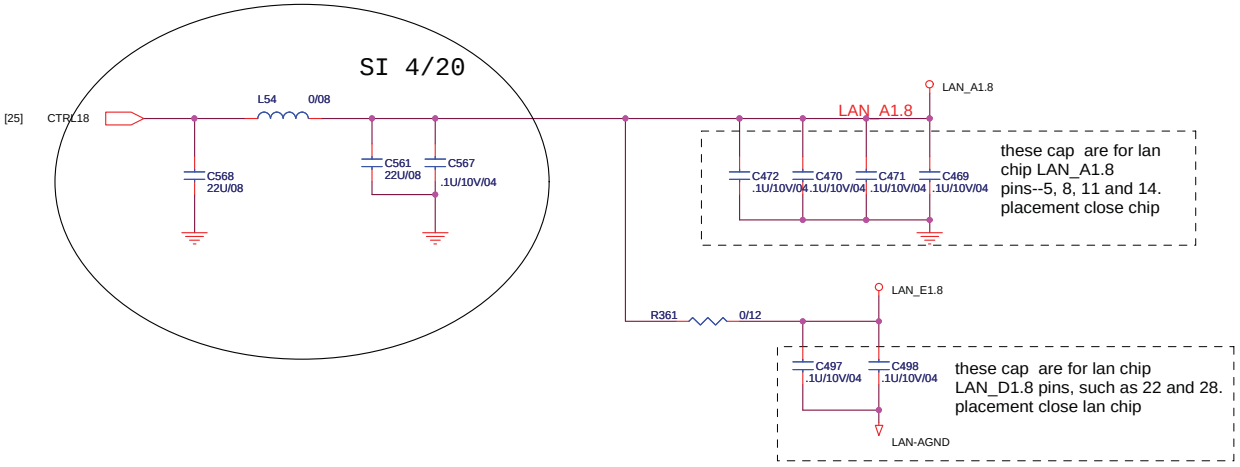
close U6



| | | |
|---|---|---|
| PROJECT : AT3U<br>Quanta Computer Inc. | | |
| Size: Custom | Document Number: RTL8101E | Rev: 2A |
| NB5/RD1/HW2 | Date: Wednesday, May 02, 2007 | Sheet 25 of 37 |

E : Stuffed for 8101E(10/100)

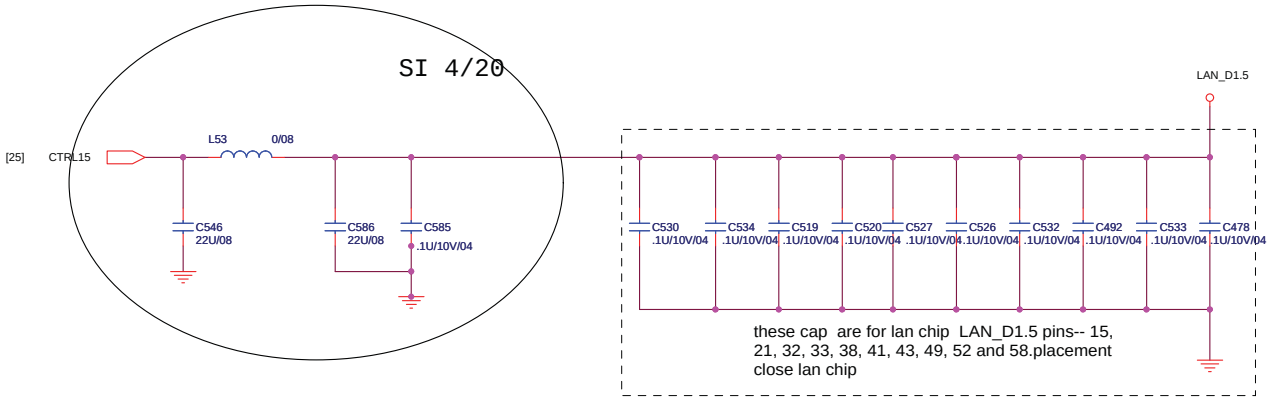



## Power domain chart

| | RTL8111B / RTL8101E | |
|---|---|---|
| LANVCC | 3.3V | |
| LAN_D1.8 | 1.8V | |
| LAN_A1.8 | 1.8V | |
| LAN_D1.5 | 1.5V | |

| | Q19 | Q21 |
|---|---|---|
| RTL8111B | Need | Need |
| RTL8101E | N/A | N/A |



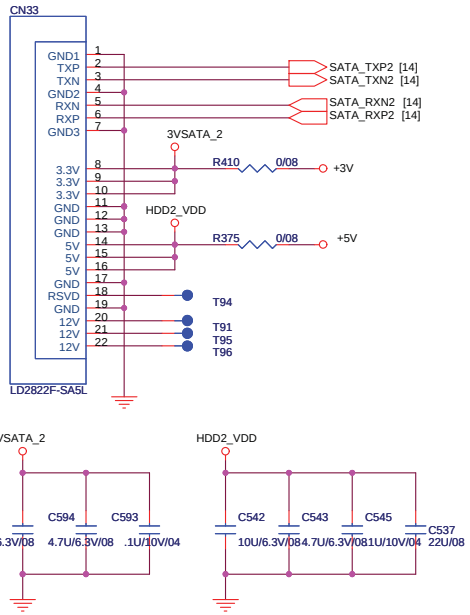

NB5/RD1/HW2

**PROJECT : AT3U**
Quanta Computer Inc.

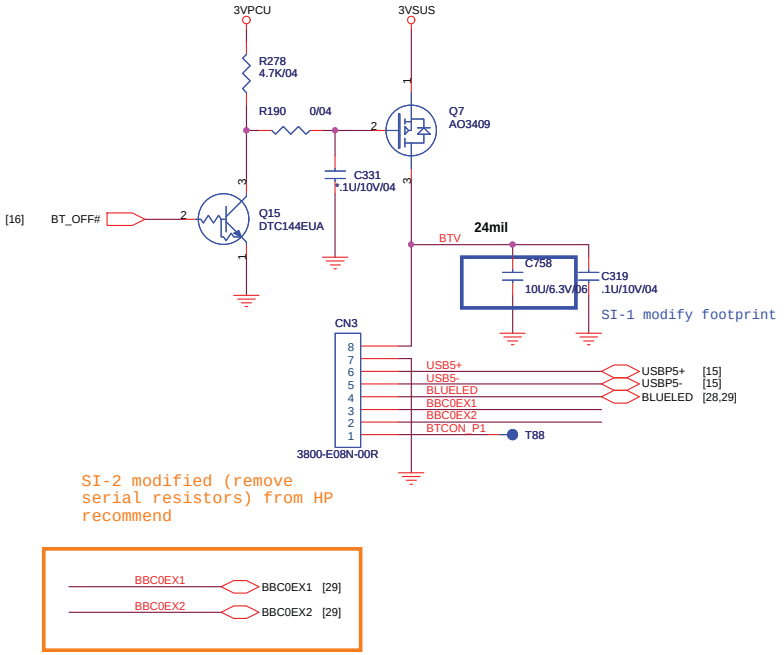
| Size | Document Number | Rev |
|---|---|---|
| Custom | LAN POWER | 2A |

Date: Wednesday, May 02, 2007 Sheet 26 of 37

# SATA_1 CONNECTOR



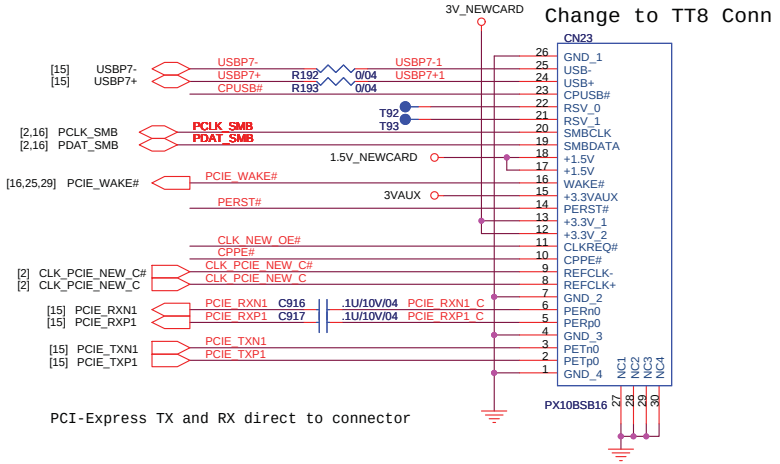

# BLUETOOTH



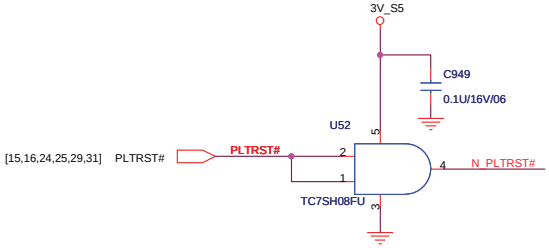

# NEWCARD

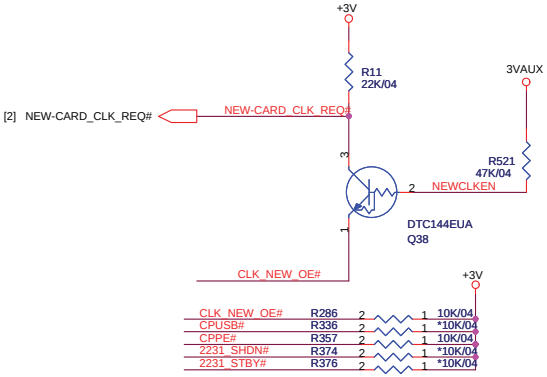


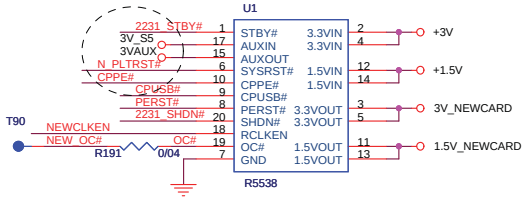
Change to TT8 Conn

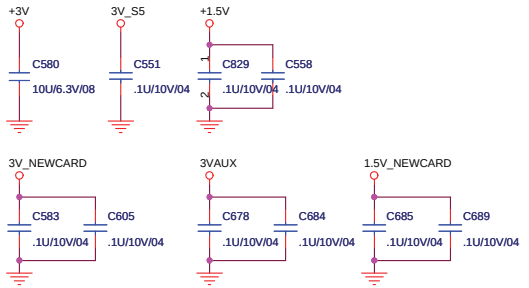



PCI-Express TX and RX direct to connector



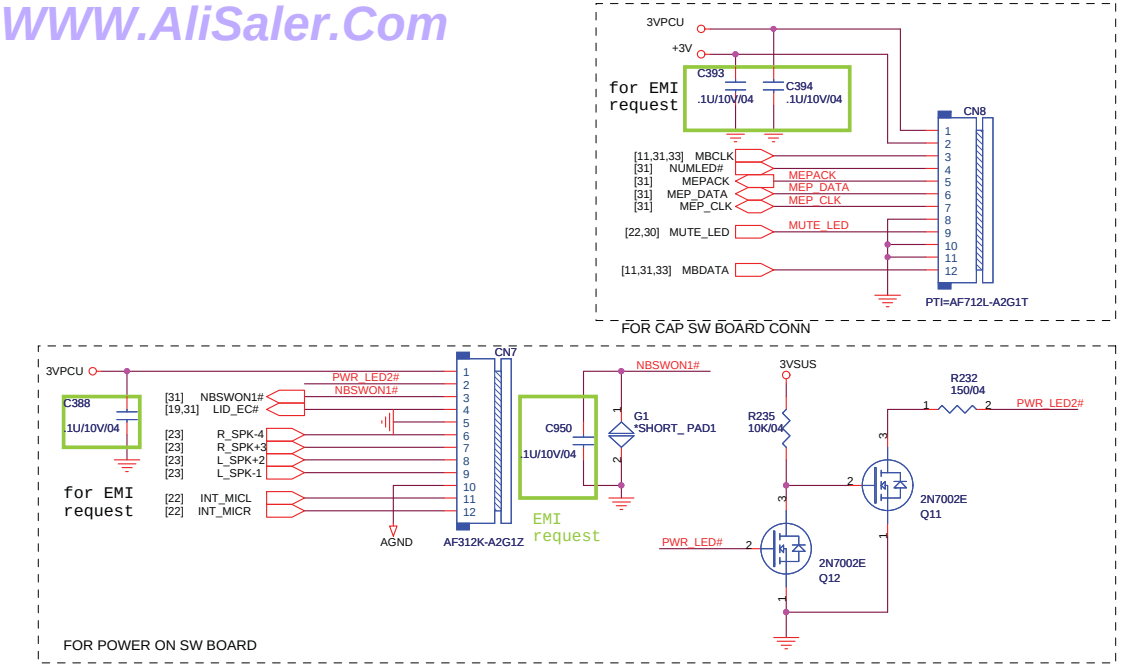



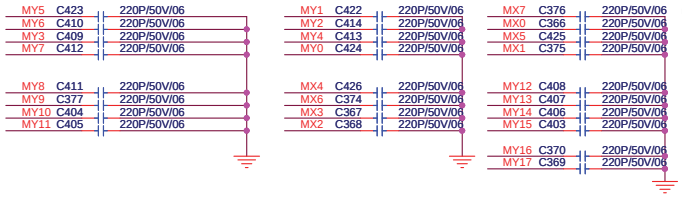

**PROJECT : AT3U**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | NEW CARD/BT | 2A |

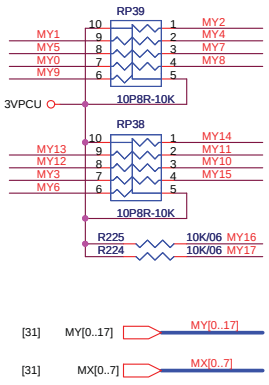
NB5/RD1/HW2

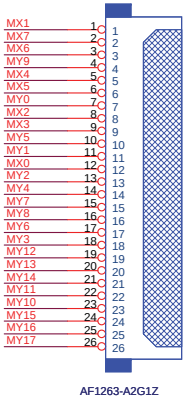
Date: Wednesday, May 02, 2007 Sheet 27 of 37

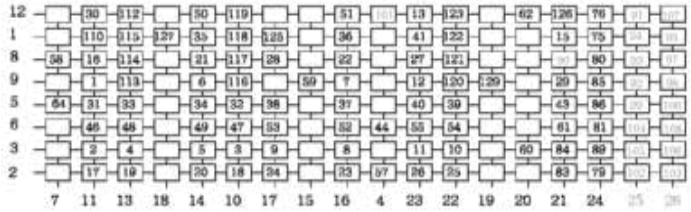



## KEYBOARD PULL-UP



**PROJECT : AT3U**
Quanta Computer Inc.

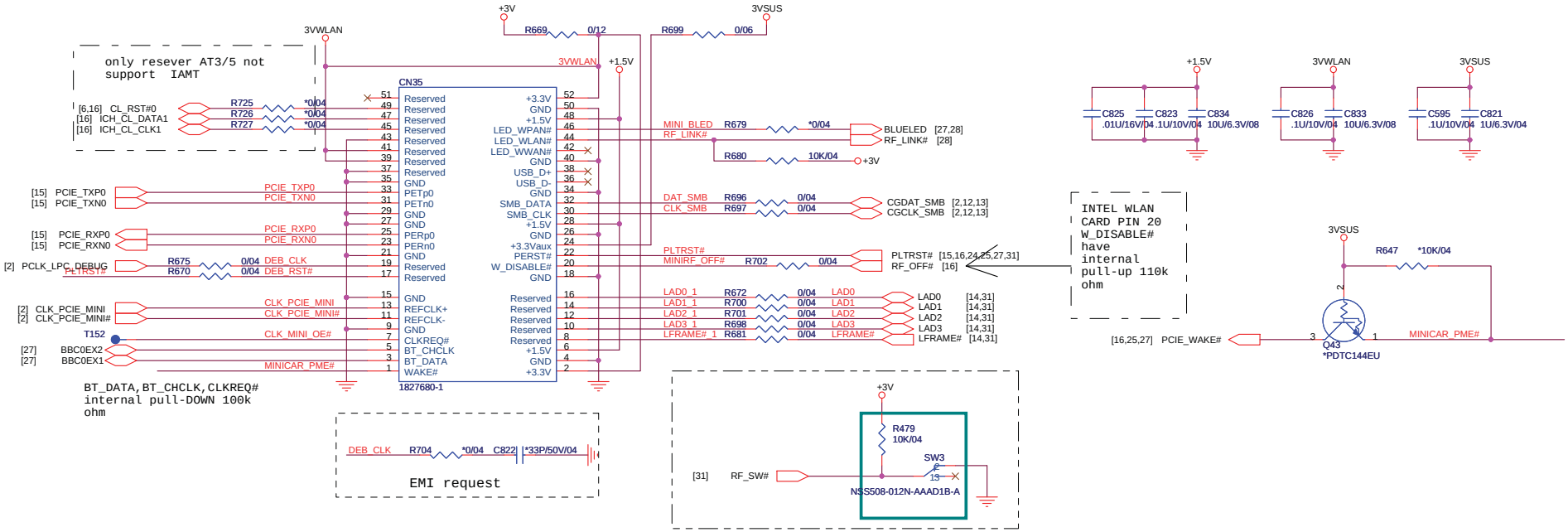
| Size | Document Number | Rev |
|---|---|---|
| Custom | LED/KEYBOARD/SW | 2A |

NB5/RD1/HW2

Date: Wednesday, May 02, 2007 Sheet 28 of 37

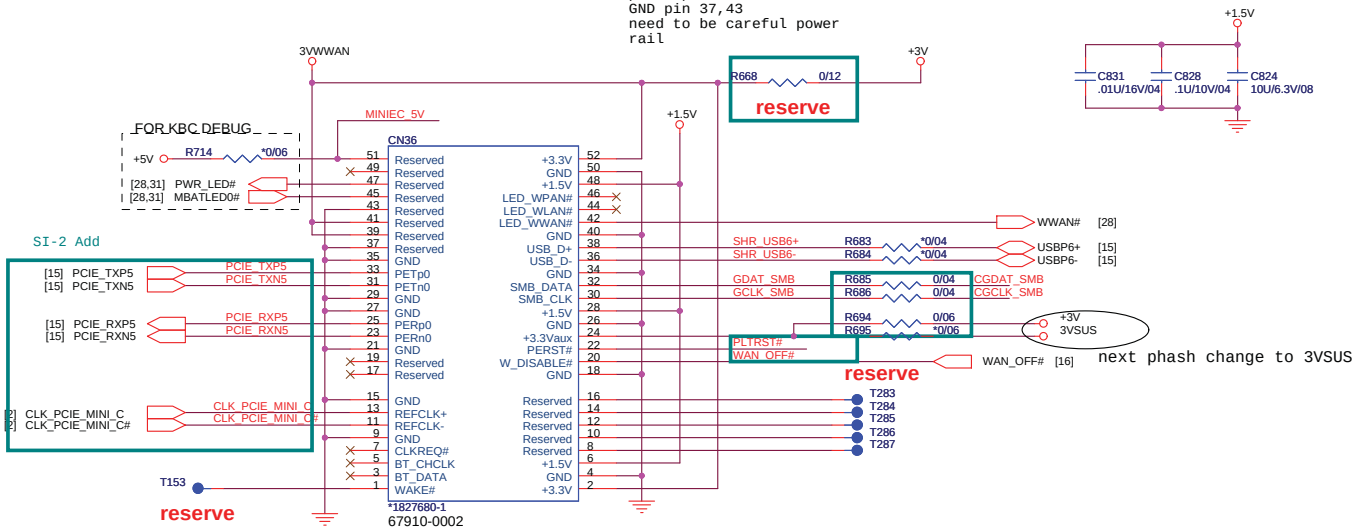
# Mini PCI-E Card 1
## WLAN






# Mini PCI-E Card 2

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail






PROJECT : AT3U
Quanta Computer Inc.

NB5/RD1/HW2

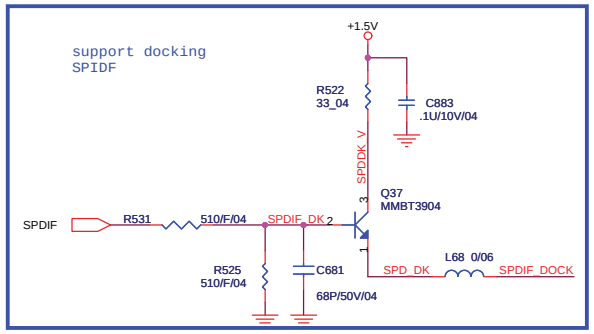
| Size | Document Number | Rev |
|---|---|---|
| Custom | MINI CARD X2 | 2A |

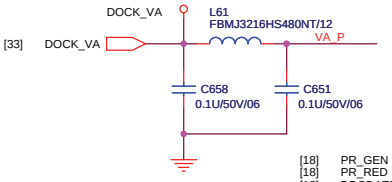
Date: Wednesday, May 02, 2007 Sheet 29 of 37

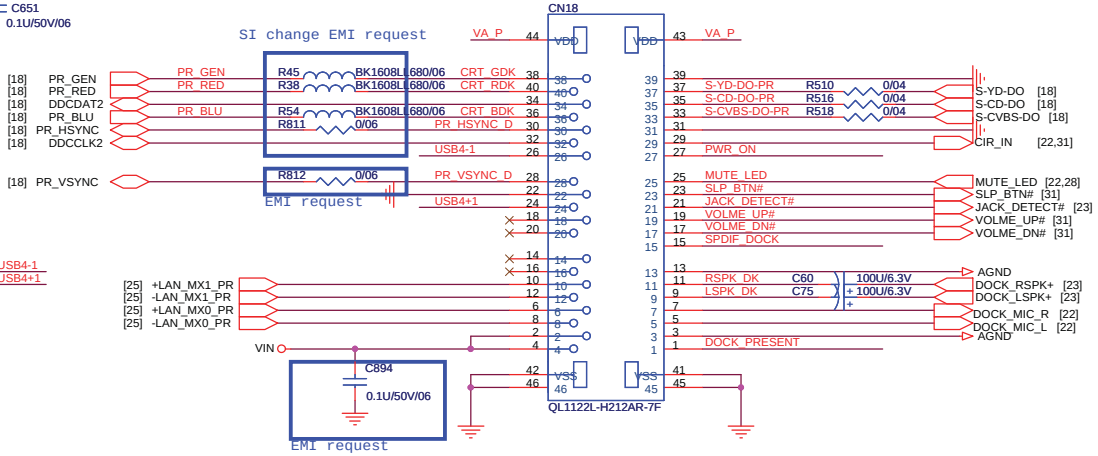
# CABLE DOCK

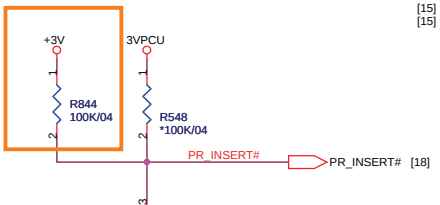
support 6A 200mils
CX000480005

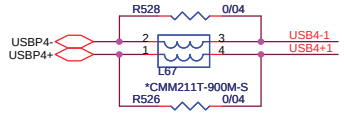


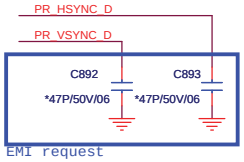


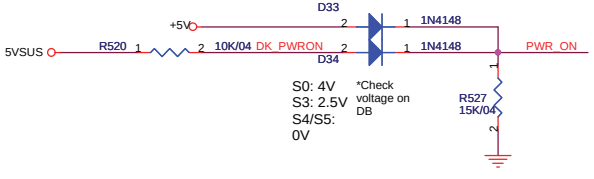



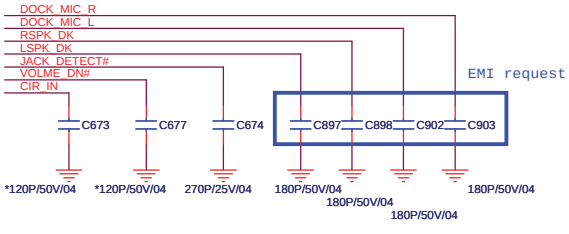



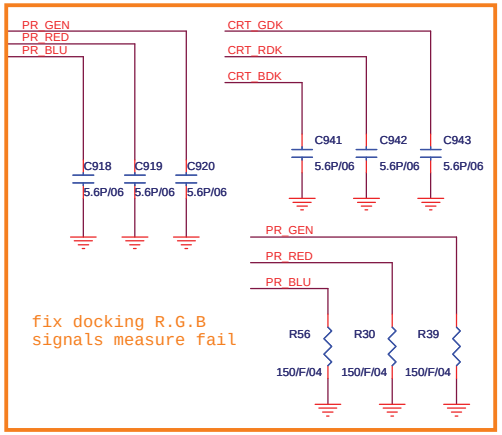



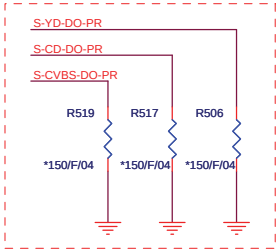



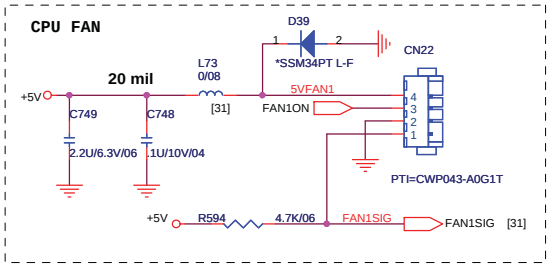




## FAN




FAN1 PWM CONNECTOR

| | | |
|---|---|---|
| N85/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| | Size: Custom<br>Document Number: CABLE DOCKING/FAN | Rev: 2A |
| | Date: Wednesday, May 02, 2007 | Sheet 30 of 37 |

## STRAP PIN

| | | |
|---|---|---|
| MY2 | 49 | TP_SPI: Default flash access<br>Low: Boot from SPI flash part<br>HIGH: Boot from ISA flash part |
| MY3 | 50 | TP_ISP: In System Programming Mode<br>Low: ISP mode<br>HIGH: Normal Mode |

DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

## SELECT KBC TPYE

| PIN NAME | USE KBC3920 | USE KBC3926 |
|---|---|---|
| MY2 | R208 | REMOVE R208 |
| BIOS_A0 | REMOVE R808 | R808 |

SI 4/30

remove R245 and add R241

SLPBTN# R241 0/04

NBSWON1# R245 *0/04

SLP_BTN# [30]

U50 KB3926

3VPCU

SCI1# D9 1N4148 SCI# [16]

PM_BATLOW1# D11 1N4148 PM_BATLOW# [16]

DNBSWON1# D10 1N4148 DNBSWON# [16]

KBSMI#1 D7 1N4148 KBSMI# [16]

SWI#1 D8 1SS355 SWI# [16]

[11] 3920_RST#

SERIRQ LFRAME# LAD0 LAD1 LAD2 LAD3 PCLK_LPC_KB3920 PLTRST# CLKRUN# SCI1# GATEA20 RCIN#

MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7

MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15 MY16 MY17

MEP_CLK MEP_DATA MEPACK ACIN TPCLK TPDATA

BIOS_RD# BIOS_WR# BIOS_CS# SERR# ECPWROK VOLME_UP# VOLME_DN# BIOS_D2 BIOS_D3 BIOS_D4 BIOS_D5 SIM_DETECT RF_SW#

10K/04 R808 BIOS_A0

SUSON MAINON LAN_POWER S5_ON BIOS_A5 BIOS_A6 BIOS_A7 BIOS_A8 BIOS_A9 BIOS_A10 BIOS_A11

T263 V18R

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 AVCC — C451 C395 C463 C465 C396 C454 C402 .1U/10V/04 1U/10V/04 10U/6.3V/08

AD0/GPI38 AD1/GPI39 AD2/GPI3A AD3/GPI3B — TEMP_MBAT MBATV AD_AIR SYS_I

DA0/GPO3C DA1/GPO3D DA2/GPO3E DA3/GPO3F — CC-SET CELL_SLT DA_VADJ D/C#

PWM1/GPIOE PWM2/GPIO10 — PWM_VADJ KEY_BEEP (1KHz)

FANPWM1/GPIO12 FANPWM2/GPIO13 FANFB1/GPIO14 FANFB2/GPIO15 — FAN1ON FAN2ON FANSIG CIR_IN

SCL1/GPIO44 SDA1/GPIO45 SCL2/GPIO46 SDA2/GPIO47 — MBCLK MBDATA T303 T304

GPIO4 SUSB# — GPIO7 GPIO8 HWPG PM_BATLOW1# T305 — GPIOA GPIOB GPIOC GPIOD GPIO11 GPIO16 GPIO17 GPIO18 SUSC# LAN_REST SWI#1 NBSWON1# BL/C# MBATLED0# PWR_LED# KBSMI#1 T306 — GPIO19 GPIO1A VRON NUMLED#

GPIO40 GPIO41 GPIO42 GPIO52 GPIO53 GPIO54 GPIO55 GPIO56 GPIO57 GPIO58 GPIO59 — SLPBTN# RPCICGRST# DNBSWON1# ALERT CAPSLED# TP_LED1# TP_LED2# RSMRST# VOLMUTE# SPI_CLK LID_EC# T307 T308 T309 T310 T311 T312

XCLKO CRY2 C489 18P/04 — XCLKI CRY1 Y2 32.768KHZ C488 18P/04

GND1 GND2 GND3 GND4 GND5 AGND

+3V R274 *10K/04 HWPG

3VPCU R204 100K/04 CIR_IN; R222 10K/04 NBSWON1#; R215 10K/04 VOLME_UP#; R207 10K/04 VOLME_DN#; R297 10K/04 SLPBTN#; R248 4.7K/04 MBCLK; R261 4.7K/04 MBDATA; R247 *8.2K/04 PM_BATLOW#; R262 10K/04 MEP_CLK; R276 10K/04 MEP_DATA

ICH8 has internal pull-up

+3V R289 *470K/04 LAD0; R294 *470K/04 LAD1; R300 *470K/04 LAD2; R304 *470K/04 LAD3; R306 *470K/04 LFRAME#

SI-1 ADD

PV-2 Add

3VPCU C954 1U/10V/04

R346 10K/04

BIOS_CS# SPI_CLK R813 33_0/4 BIOS_WR# R814 0/04 BIOS_RD# R815 0/04

U17 CE# SCK SI SO WP# VSS HOLD# VDD

SPI_3P SPI_7P

MX25L8005

R314 10K/04

1M byte SPI BIOS

(Amber) LED3 (Blue) LED BLUE/AMBER

TP_LED1# R609 150/04 TPLD1 +3V

TP_LED2# R610 150/04 TPLD2 +3V

## TOUCH PAD CONNECTOR

25 mils

5VSUS L30 BK1608HS800-T/06 5VTP C330 1U/10V/04

TPCLK L28 SBK160808T-221/06 TPCLK-1

TPDATA L31 SBK160808T-221/06 TPDATA-1

C323 *10P/50V/04 C327 *10P/50V/04

CN4 AF1043-A2G1Z

PCLK_LPC_KB3920 R249 *0/04 C428 *33P/50V/04

for EMI request

5VSUS R290 4.7K/04 TPCLK; R291 4.7K/04 TPDATA

SW1 MY7 MX4 NTC031-AA1G-A160T

| | | |
|---|---|---|
| PROJECT : AT3U<br>Quanta Computer Inc. | | |
| Size: Custom | Document Number: KB3920/ROM/TP | Rev: 2A |
| NB5/RD1/HW2 | Date: Wednesday, May 02, 2007 | Sheet 31 of 37 |

# DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

**5 Volt +/- 5%**
**Countinue current:8A**
**Peak current:11A**
**OCP minimum 13A**

**3.3 Volt +/- 5%**
**Countinue current:5A**
**Peak current:7.5A**
**OCP minimum 10A**

VIN
5V_AL
+5V_VCC1
5VPCU
3VPCU
+12V_ALW
PU10 ISL6236IRZA-T
PQ55 Si4800BDY
PQ59 SI4420DY
PQ50 Si4800BDY
PQ48 ME4410
PQ49 ME4410
PQ56 ME4410
PQ60 ME4410
PQ63 ME3424
PD7 BAT54S
PD8 BAT54S
PL14 1.5uH_MPL73-1R5
PL12 2.2uH_MPL73-2R2
Rds(on) 13m ohm
Rds(on) 15m ohm
PGOOD1
PGOOD2
3V_DH
5V_DH
5V_DL
3V_LX
3V_DL
SYS_SHDN#
MAIND
SUSD
HWPG
5.92A
3.8A
3.4A
2A
SI-1 MODIFY



| | | |
|---|---|---|
| N85/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: 3v/5v | Rev: 2A |
| Date: Wednesday, May 02, 2007 | Sheet 32 of 37 | |

C30: Add PD22 for 12cell battery issue

TOP DC JACK
65W/90W

SI power

SI-2 modify

SI-2 ADD

SI-1-2 Add

SI-1-2 MODIFY

Setting the Vin min to 8V

CELL_SLT = 1 -- 3 S
CELL_SLT = 0 -- 4 S

Iinput=Vcls/Vref * 0.075/RS1
Vref=4.096V,RS1=10m-ohm

| ADP TYPE | VALUE | P/N |
|---|---|---|
| 65W | 39.2K/F | CS33922FB15 |
| 90W | 20K/F | CS32002FB29 |

Battery Low = 8V

| BL/C# | D/C# | M/A# | Status |
|---|---|---|---|
| 0 | 0 | 0 | Chareg A batt |
| 0 | 0 | 1 | Charge M batt |
| 0 | 1 | 0 | Discharge A batt |
| 0 | 1 | 1 | Discharge M batt |
| 1 | 0 | 0 | Free Dicharge |
| 1 | 0 | 1 | Free Dicharge |
| 1 | 1 | 0 | Free Dicharge |
| 1 | 1 | 1 | Free Dicharge |

PROJECT : AT3U
Quanta Computer Inc.

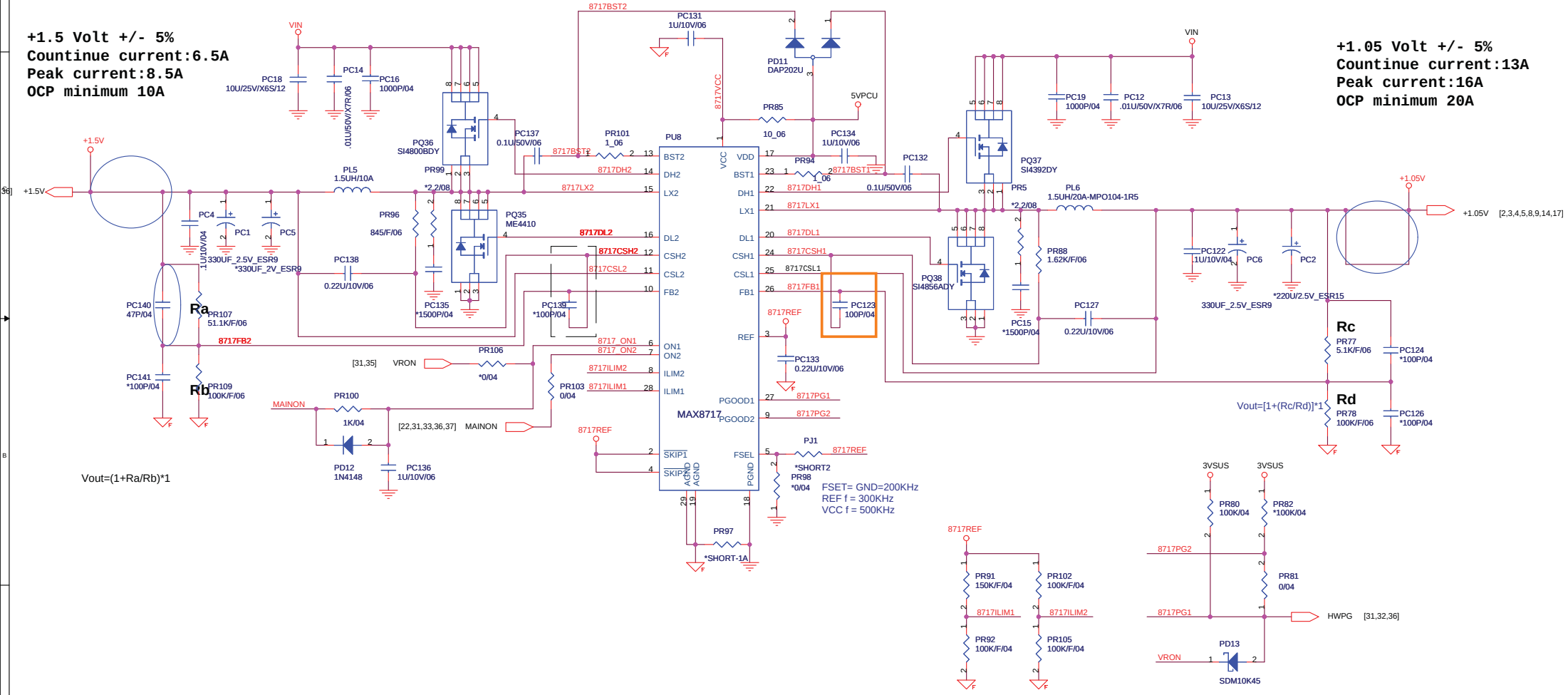
NB5/RD1/HW2

Size: Custom | Document Number: SYSTEM CHARGER(MAX8724) | Rev: 2A

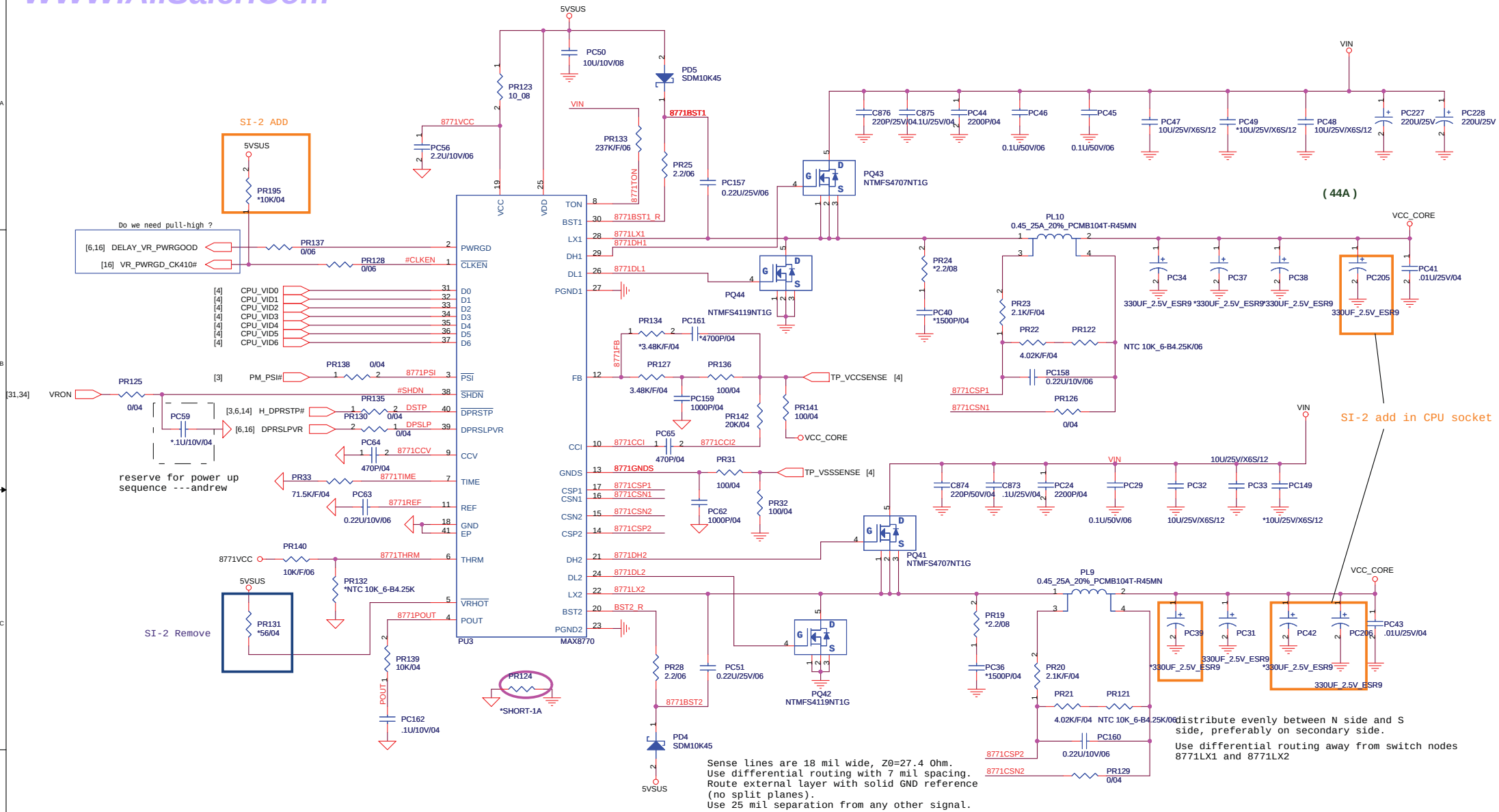
Date: Wednesday, May 02, 2007 | Sheet 33 of 37

**+1.5 Volt +/- 5%**
**Countinue current:6.5A**
**Peak current:8.5A**
**OCP minimum 10A**

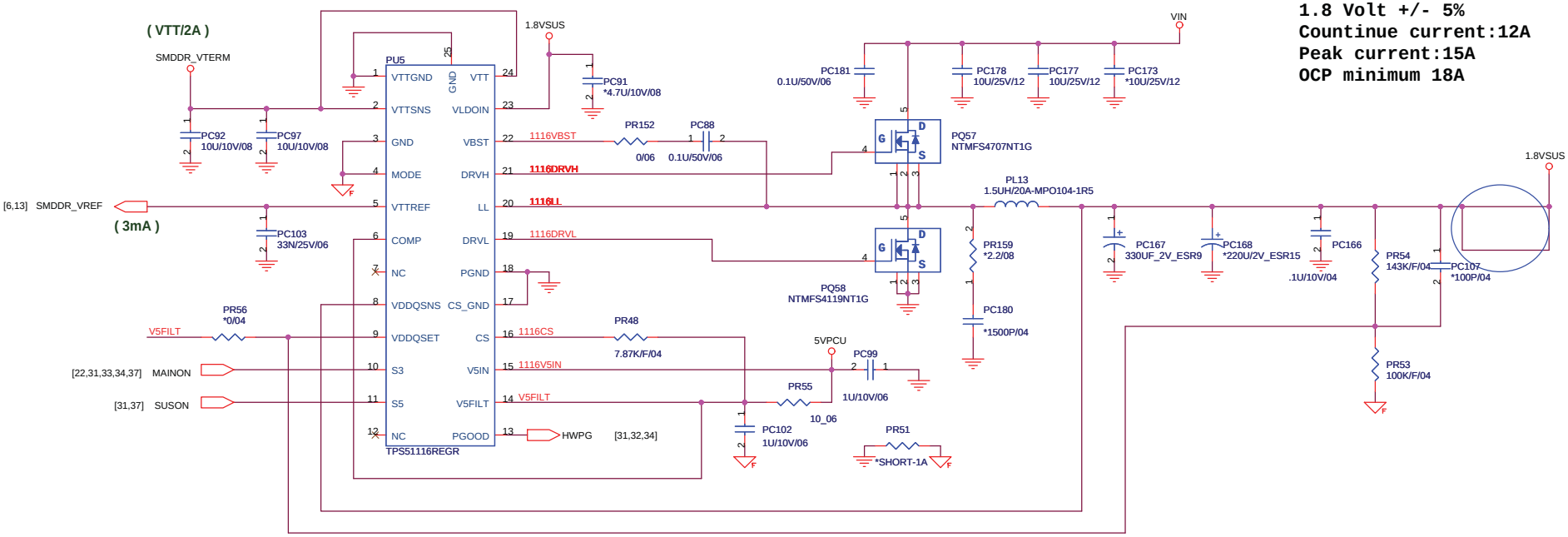
**+1.05 Volt +/- 5%**
**Countinue current:13A**
**Peak current:16A**
**OCP minimum 20A**



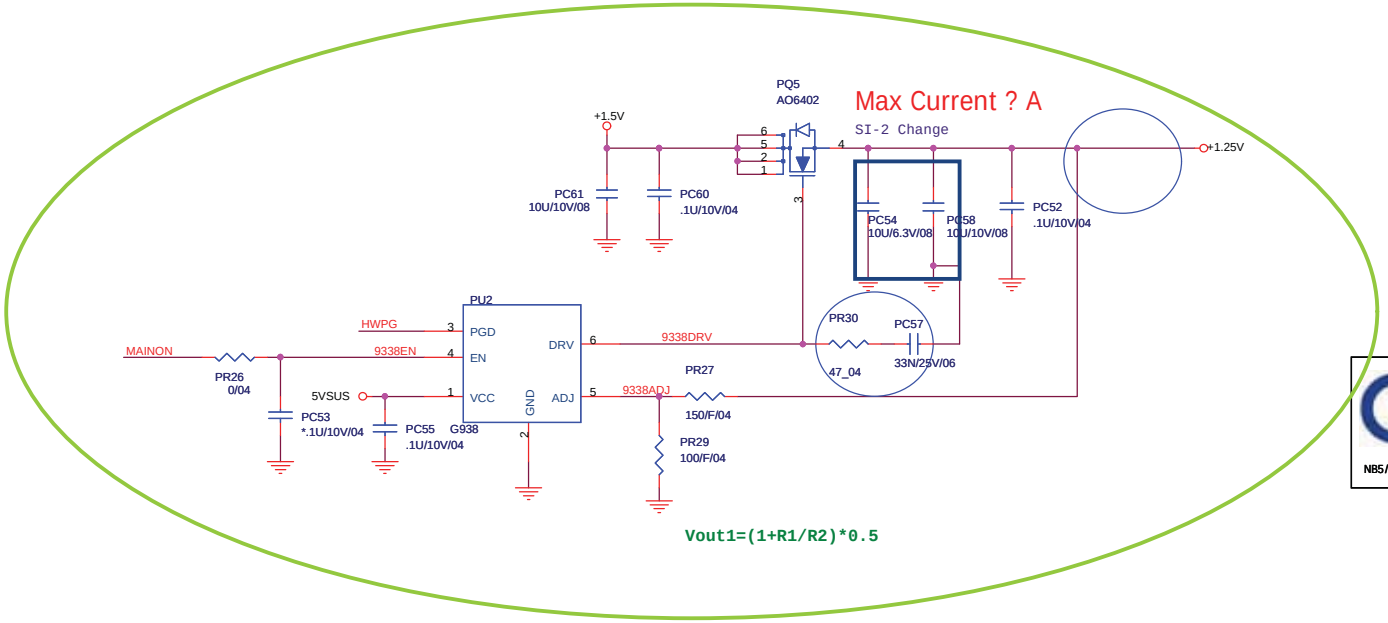

| | | |
|---|---|---|
| NB5/RD1/HW2 | **PROJECT : AT3U**<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: +-1.5V &VCCP+1.05V(MAX8743) | Rev: 2A |
| Date: Wednesday, May 02, 2007 | Sheet 34 of 37 | |



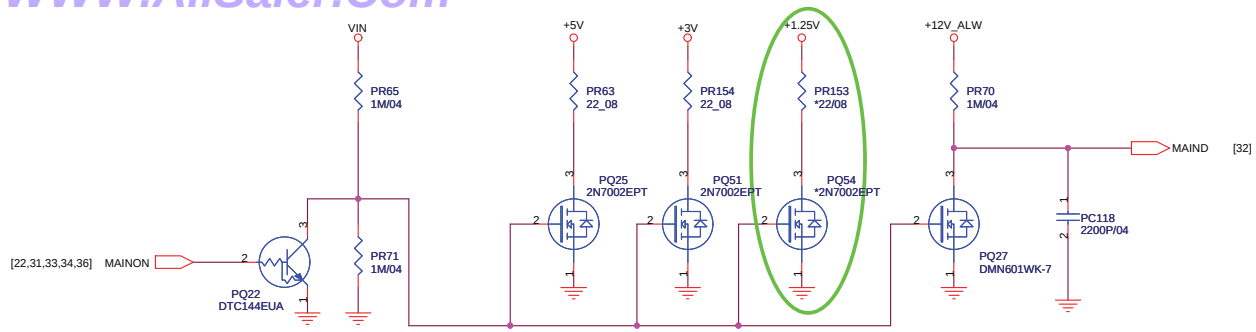

| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: CPU_CORE(MAX8771) | Rev: 2A |
| Date: Wednesday, May 02, 2007 | Sheet 35 of 37 | |

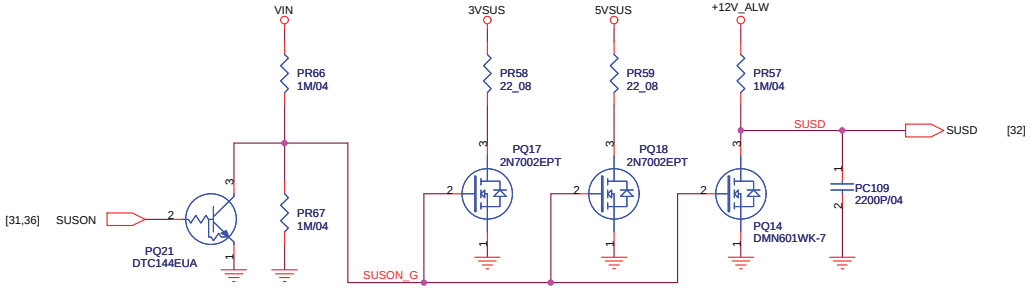


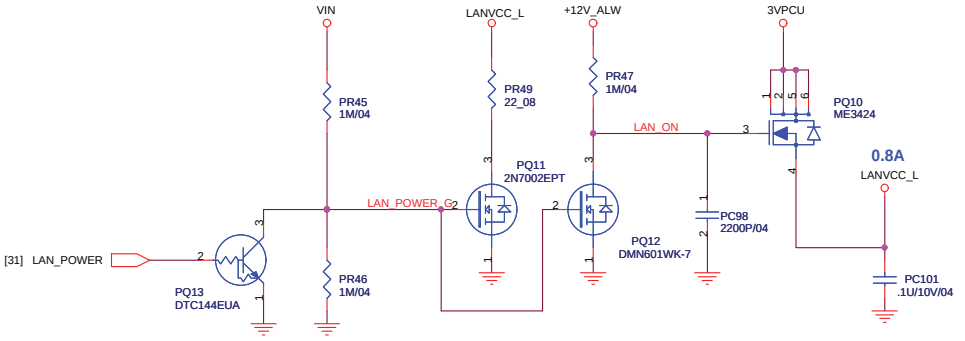

1.8 Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

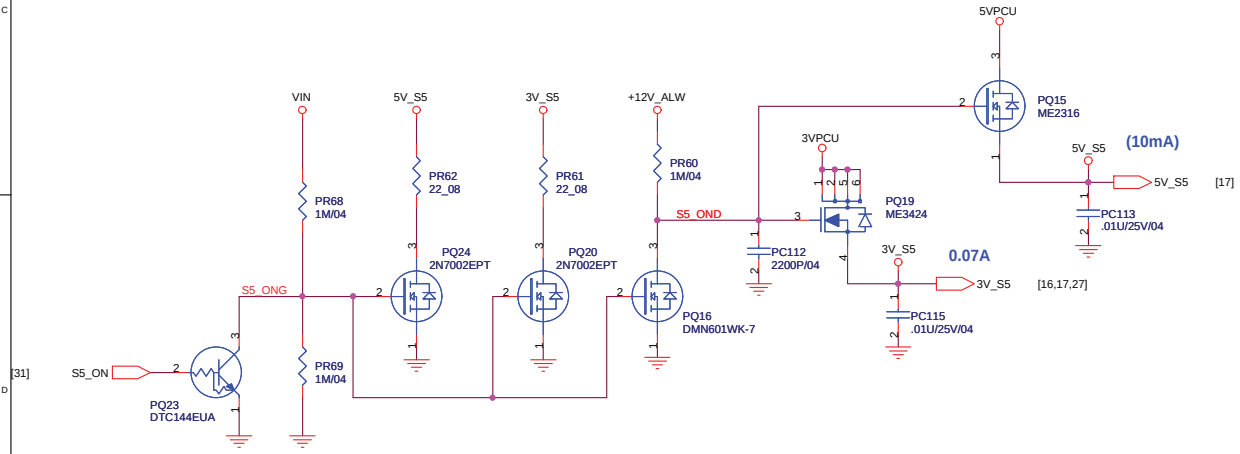



| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: DDRII 1.8VSUS/SMDDR_VTERM | Rev: 2A |
| Date: Wednesday, May 02, 2007 | Sheet 36 of 37 | |




| | | |
|---|---|---|
| NB5/RD1/HW2 | PROJECT : AT3U<br>Quanta Computer Inc. | |
| | Size: Custom — Document Number: DISCHARGE | Rev: 2A |
| | Date: Wednesday, May 02, 2007 — Sheet 37 of 37 | |