

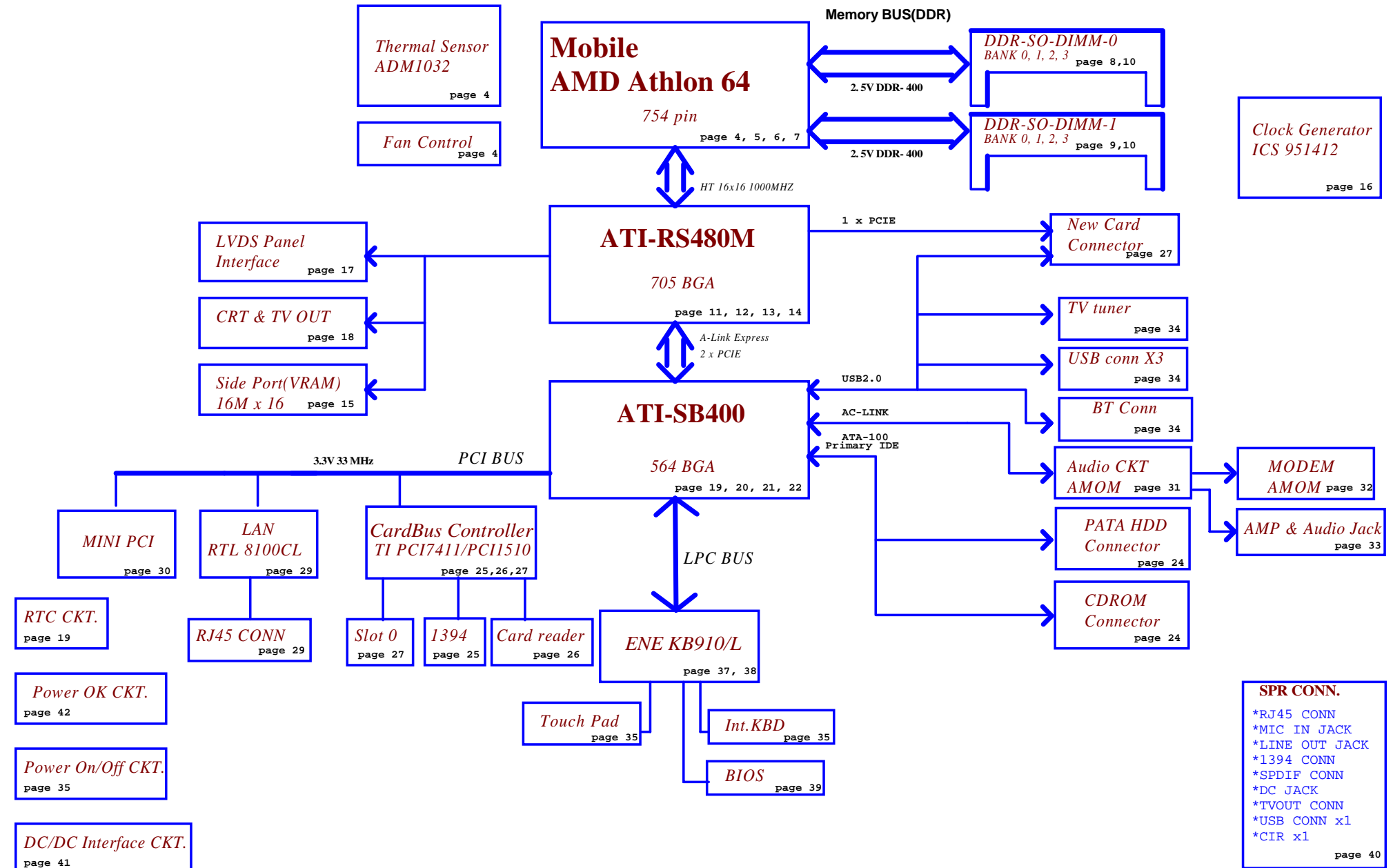
# Compal confidential

## Schematics Document

### AMD K8 with ATI RS480M+ATI SB400

2005-08-29  
REV:0.8

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Issued Date	2005/03/01	Deciphered Date	2005/04/06	Cover Page	
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## Voltage Rails

power plane State	+12VALW +5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT
S0	O	O	O
S1	O	O	O
S3	O	O	X
S5 S4/AC	O	X	X
S5 S4/AC don't exist	X	X	X

O MEANS ON

X MEANS OFF

## BOM STATUS :

VRAM@ , VRAMIC@, SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17\_EXP@ ,15\_EXO@,CIR@ ,D@, C@, 15.4@, DOCK@, WL\_LED@

45@ ( for 45 level RTC battery )

HAL10 17"      VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17\_EXP@ ,CIR@ ,D@ ,DOCK@,WL\_LED@

HAL20 FF 15.4"      VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,15\_EXP@ ,CIR@ ,C@ ,DOCK@,WL\_LED@, 15.4@(LED)

HAL20 DF 15.4"      EXP@, C@ ,DOCK@ ,15.4@(LED), CIR@, WLAN@, 15\_EXP@

## PCI Devices

INTERNAL DEVICE	IDSEL #	REQ/GNT #	PIRQ
SMBUS			
IDE			A
LPC I/F			
PCI to PCI			
AC97 AUDIO			B
AC97 MODEM			B
OHCI#1 USB			D
OHCI#1 USB			D
EHCI USB			D
SATA#1			A
SATA#2			A

EXTERNAL			
Wireless LAN	AD18	3	F
LAN	AD22	1	G
CARD BUS & 1394	AD20	2	E,H

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H\_CADOP[0..15] H\_CADOP[0..15] <11>  
H\_CADON[0..15] H\_CADON[0..15] <11>

JP1A

Claw Hammer-DTR

HTT Interface

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H\_CADIN15 R25 L0\_CADIN\_L15  
H\_CADIP14 U27 L0\_CADIN\_H14  
H\_CADIN14 U26 L0\_CADIN\_L14  
H\_CADIP13 V25 L0\_CADIN\_H13  
H\_CADIN13 U25 L0\_CADIN\_L13  
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H\_CADIN12 W26 L0\_CADIN\_L12  
H\_CADIP11 AA27 L0\_CADIN\_H11  
H\_CADIN11 AA26 L0\_CADIN\_L11  
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H\_CADIN10 AA25 L0\_CADIN\_L10  
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H\_CADIN9 AC26 L0\_CADIN\_L9  
H\_CADIP8 AD25 L0\_CADIN\_H8  
H\_CADIN8 AC25 L0\_CADIN\_L8  
H\_CADIP7 T27 L0\_CADIN\_H7  
H\_CADIN7 T28 L0\_CADIN\_L7  
H\_CADIP6 V29 L0\_CADIN\_H6  
H\_CADIN6 U29 L0\_CADIN\_L6  
H\_CADIP5 V27 L0\_CADIN\_H5  
H\_CADIN5 V28 L0\_CADIN\_L5  
H\_CADIP4 W29 L0\_CADIN\_H4  
H\_CADIN4 W29 L0\_CADIN\_L4  
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H\_CADIN3 AA29 L0\_CADIN\_L3  
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H\_CADIN2 AB28 L0\_CADIN\_L2  
H\_CADIP1 AD29 L0\_CADIN\_H1  
H\_CADIN1 AC29 L0\_CADIN\_L1  
H\_CADIP0 AD27 L0\_CADIN\_H0  
H\_CADIN0 AD28 L0\_CADIN\_L0

L0\_CADOUT\_H15  
L0\_CADOUT\_L15  
L0\_CADOUT\_H14  
L0\_CADOUT\_L14  
L0\_CADOUT\_H13  
L0\_CADOUT\_L13  
L0\_CADOUT\_H12  
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N26 H\_CADOP15  
N27 H\_CADON15  
L26 H\_CADOP14  
M25 H\_CADON14  
L26 H\_CADOP13  
L27 H\_CADON13  
J25 H\_CADOP12  
K25 H\_CADON12  
G25 H\_CADOP11  
H25 H\_CADON11  
G26 H\_CADOP10  
G27 H\_CADON10  
E25 H\_CADOP9  
F25 H\_CADON9  
E26 H\_CADOP8  
E27 H\_CADON8  
N29 H\_CADOP7  
P29 H\_CADON7  
M29 H\_CADOP6  
M27 H\_CADON6  
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M29 H\_CADON5  
K27 H\_CADOP4  
K28 H\_CADON4  
H28 H\_CADOP3  
H27 H\_CADON3  
G29 H\_CADOP2  
H29 H\_CADON2  
F28 H\_CADOP1  
F27 H\_CADON1  
E29 H\_CADOP0  
F29 H\_CADON0

J26 H\_CLKOP1  
J27 H\_CLKON1  
J29 H\_CLKOP0  
K29 H\_CLKON0

L0\_CLKOUT\_H1  
L0\_CLKOUT\_L1  
L0\_CLKOUT\_H0  
L0\_CLKOUT\_L0

N25  
P25  
P28  
P27  
AJ27

L0\_CTLIN\_H1  
L0\_CTLIN\_L1  
L0\_CTLIN\_H0  
L0\_CTLIN\_L0

L0\_CTLOUT\_H1  
L0\_CTLOUT\_L1  
L0\_CTLOUT\_H0  
L0\_CTLOUT\_L0

LDTSTOP#

L0\_REF1  
L0\_REF0

FOX\_PZ75403-2941-42

R8 680\_0402\_5%

+2.5VS

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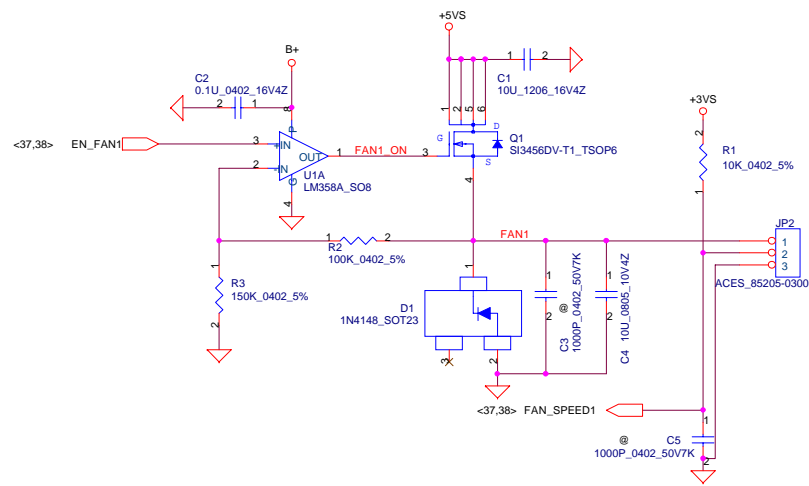
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LVREF1  
LVREF0

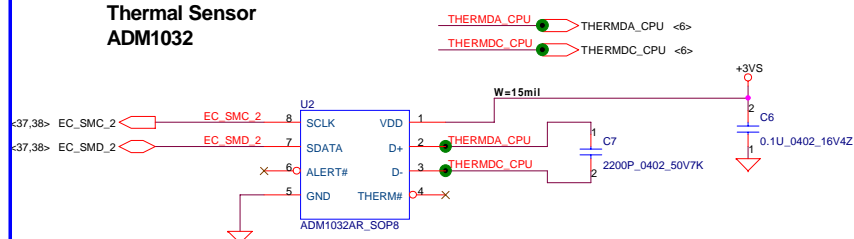
R4 49.9\_0402\_1%  
R5 49.9\_0402\_1%  
R6 44.2\_0603\_1%  
R7 44.2\_0603\_1%

+1.2V\_HT  
+1.2V\_HT

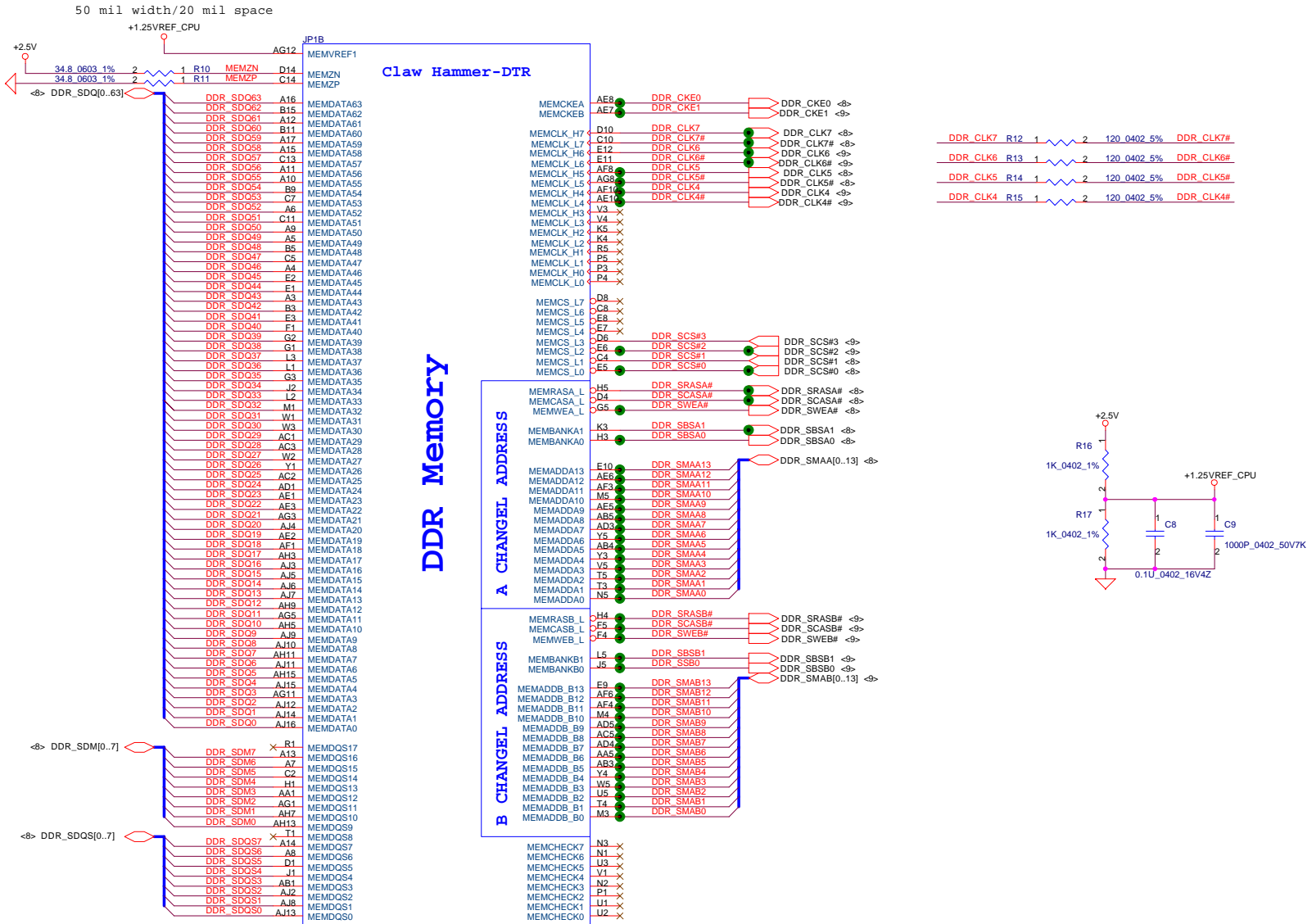
Fan Control Circuit



Thermal Sensor ADM1032

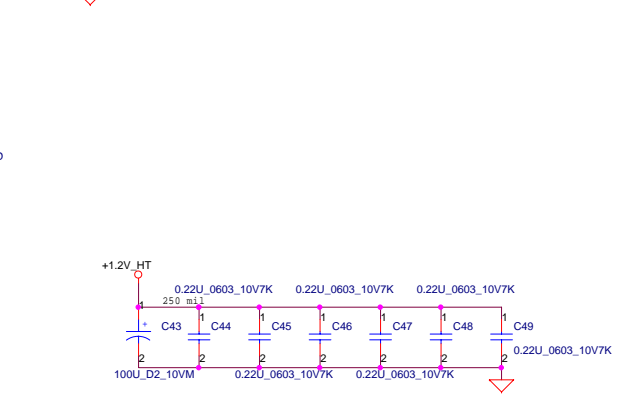
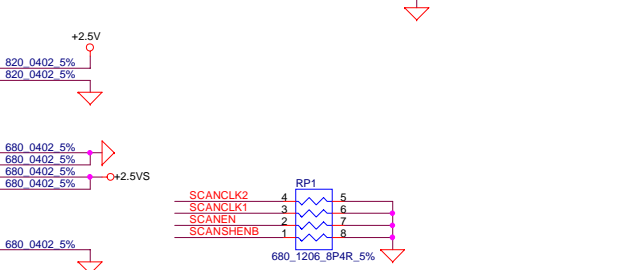
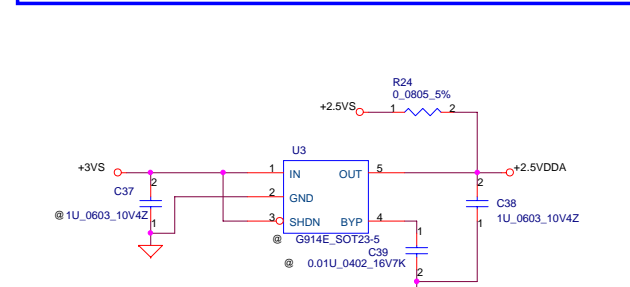
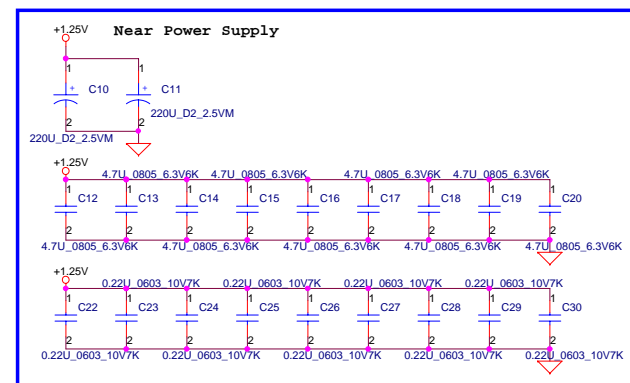
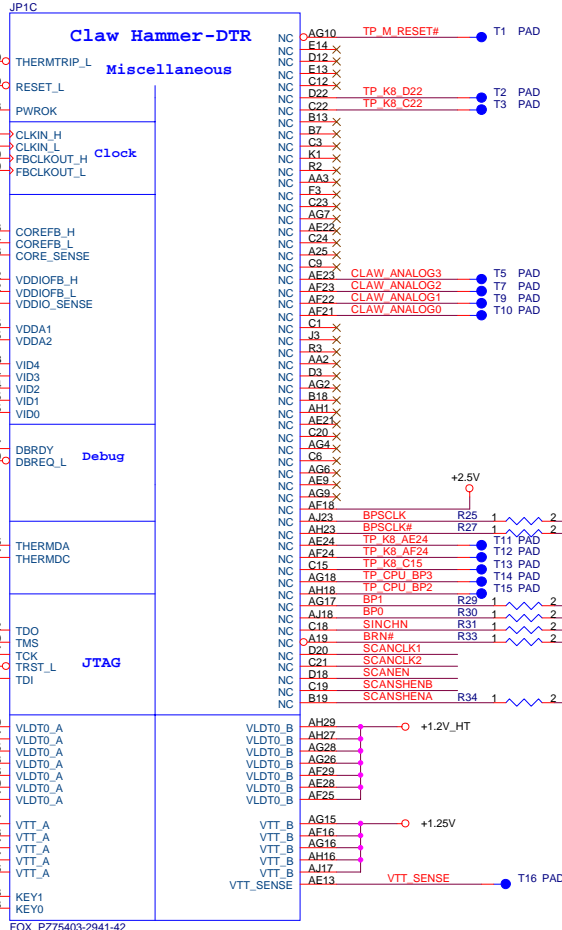
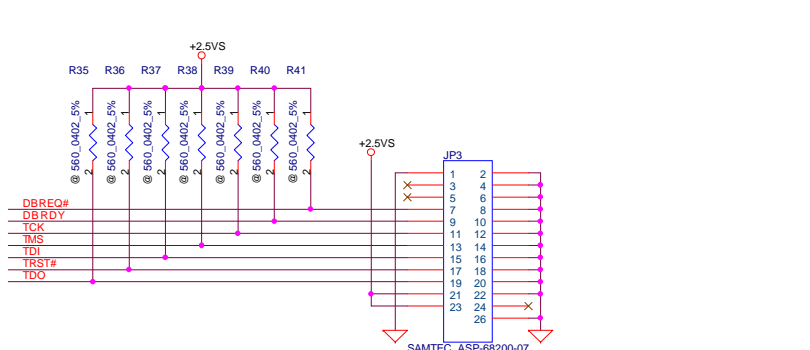
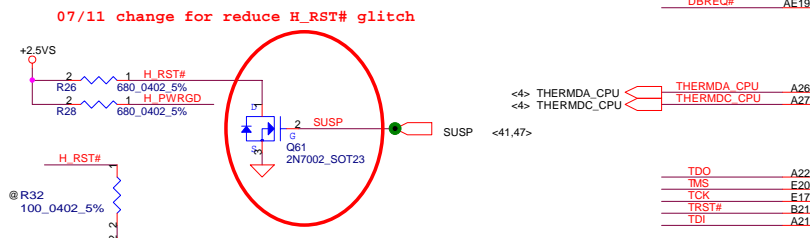
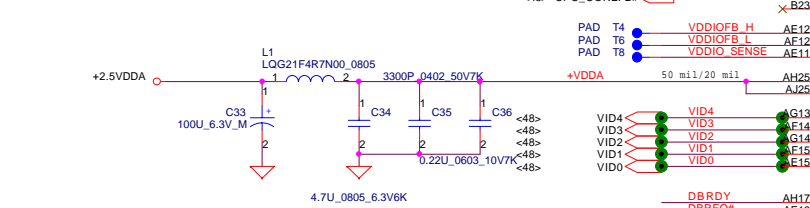
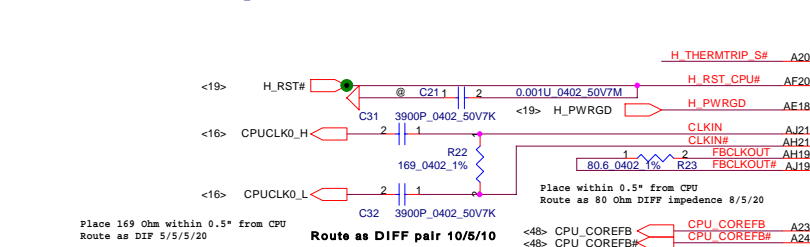
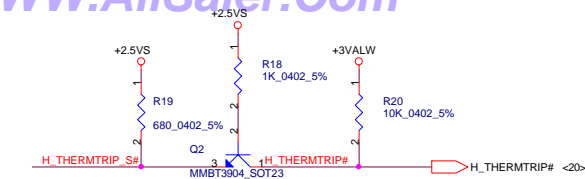


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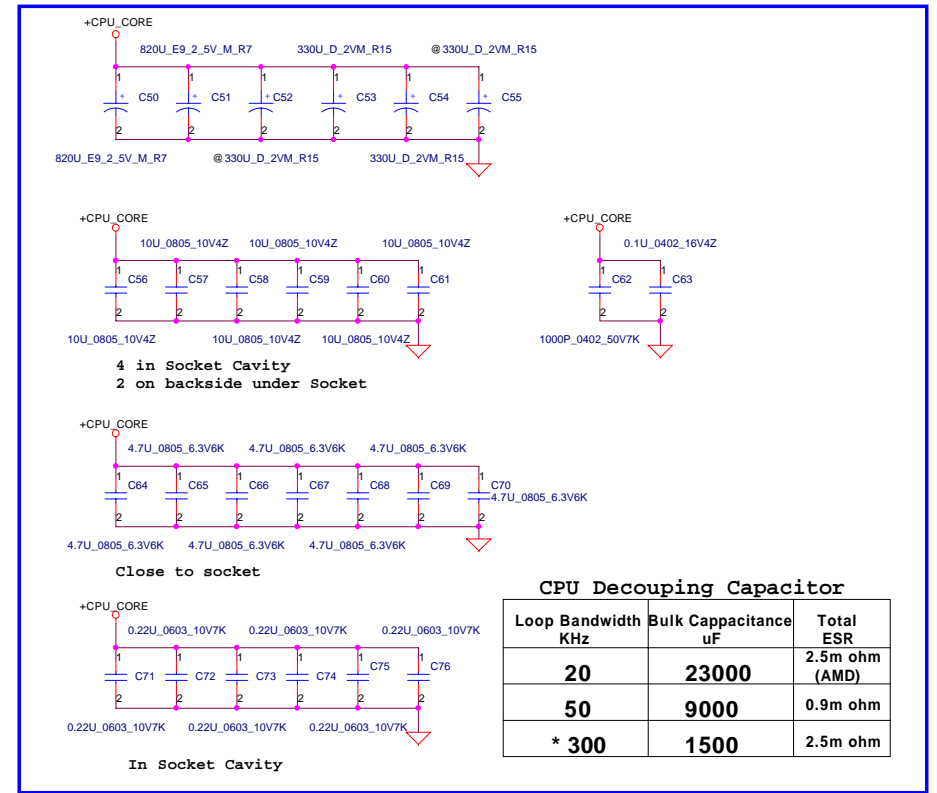
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W22	VSS	W28	VSS
M23	VSS	AC28	VSS
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AG25	VSS	C29	VSS
AG27	VSS	F2	VSS
D2	VSS	H2	VSS
W6	VSS	K2	VSS
Y7	VSS	M2	VSS
AA8	VSS	P2	VSS
AB9	VSS	T2	VSS
AA10	VSS	V2	VSS
J12	VSS	Y2	VSS
B14	VSS	AB2	VSS
Y15	VSS	AD2	VSS
AE16	VSS	AH2	VSS
H18	VSS	B4	VSS
G20	VSS	AA15	VSS
R20	VSS	H16	VSS
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W20	VSS	G6	VSS
AA20	VSS	J6	VSS
AC20	VSS	LR	VSS
AC20	VSS	N6	VSS
AC20	VSS	R6	VSS
AC20	VSS	U6	VSS
AC20	VSS	AE17	VSS
AJ20	VSS	AC6	VSS
D21	VSS	AH6	VSS
F21	VSS	F7	VSS
H21	VSS	H7	VSS
K21	VSS	K7	VSS
M21	VSS	M7	VSS
P21	VSS	P7	VSS
T21	VSS	T7	VSS
V21	VSS	V7	VSS
Y21	VSS	AB7	VSS
AD21	VSS	AD7	VSS
AC21	VSS	B8	VSS
B22	VSS	G8	VSS
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G22	VSS	L8	VSS
J22	VSS	N8	VSS
L22	VSS	R8	VSS
N22	VSS	T20	VSS
R22	VSS	U8	VSS
U22	VSS	W8	VSS
AC22	VSS	AC8	VSS
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AC22	VSS	AH8	VSS
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J24	VSS	AC10	VSS
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R24	VSS	F11	VSS
U24	VSS	H11	VSS
W24	VSS	K11	VSS
AA24	VSS	Y11	VSS
AC24	VSS	AB11	VSS
AC24	VSS	AD11	VSS
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AC24	VSS	G12	VSS
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AA18	VSS	K15	VSS
AC18	VSS	AB15	VSS
D18	VSS	AD15	VSS
F19	VSS	AE15	VSS
H19	VSS	AH14	VSS
K19	VSS	E16	VSS
Y19	VSS	J16	VSS
AB19	VSS	AA16	VSS
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L20	VSS	AJ26	VSS
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		Y17	VSS

POWER

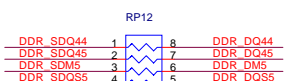
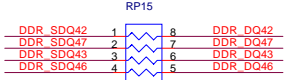
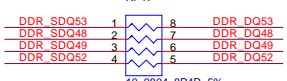
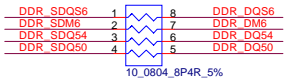
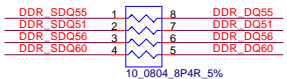
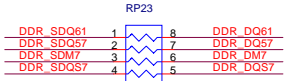
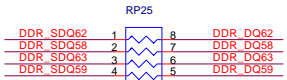
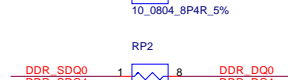
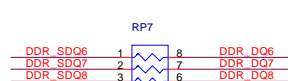
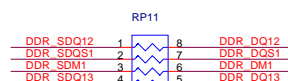
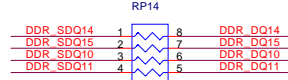
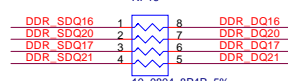
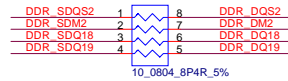
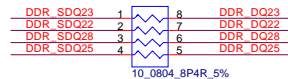
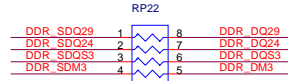
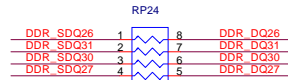
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		R23	VDD
		U23	VDD
		W23	VDD
		AA23	VDD
		AC23	VDD
		B24	VDD
		D24	VDD
		F24	VDD
		K24	VDD
		M24	VDD
		P24	VDD
		T24	VDD
		V24	VDD
		Y24	VDD
		AB24	VDD
		AD24	VDD
		AH24	VDD
		AE25	VDD
		K26	VDD
		AE14	VDD
		D16	VDD
		V26	VDD

FOX\_PZ75403-2941-42

E4	VDDIO
D4	VDDIO
J4	VDDIO
N4	VDDIO
U4	VDDIO
AA4	VDDIO
AC4	VDDIO
AE4	VDDIO
D5	VDDIO
AF5	VDDIO
F6	VDDIO
H6	VDDIO
K6	VDDIO
M6	VDDIO
P6	VDDIO
T6	VDDIO
V6	VDDIO
Y6	VDDIO
AB6	VDDIO
AD6	VDDIO
D7	VDDIO
G7	VDDIO
J7	VDDIO
AA7	VDDIO
AC7	VDDIO
AE7	VDDIO
F8	VDDIO
H8	VDDIO
AB8	VDDIO
AD8	VDDIO
D9	VDDIO
G9	VDDIO
AC9	VDDIO
AE9	VDDIO
F10	VDDIO
AD10	VDDIO
D11	VDDIO
AE11	VDDIO
F12	VDDIO
AD12	VDDIO
D13	VDDIO
AE13	VDDIO
F14	VDDIO
AD14	VDDIO
F16	VDDIO
AD16	VDDIO
D15	VDDIO
R4	VDDIO
N28	VDD
U28	VDD
AA28	VDD
AE27	VDD
R7	VDD
U7	VDD
W7	VDD
K8	VDD
M8	VDD
P8	VDD
T8	VDD
V8	VDD
Y8	VDD
J8	VDD
N8	VDD
R9	VDD
U9	VDD
W9	VDD
AA9	VDD
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K10	VDD
M10	VDD
P10	VDD
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AB10	VDD
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J11	VDD
AA11	VDD
AC11	VDD
H12	VDD
K12	VDD
Y12	VDD
AB12	VDD
J13	VDD
G14	VDD
AC13	VDD
H14	VDD
AB26	VDD
E28	VDD
J28	VDD



<-> DDR\_SDQS[0..7] <-> DDR\_DQ[0..63] <-> DDR\_DQS[0..7] <-> DDR\_DM[0..7] <-> DDR\_SMAA[0..13]

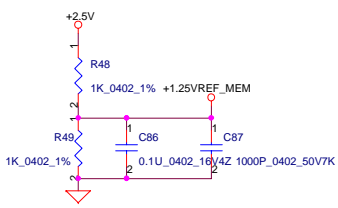
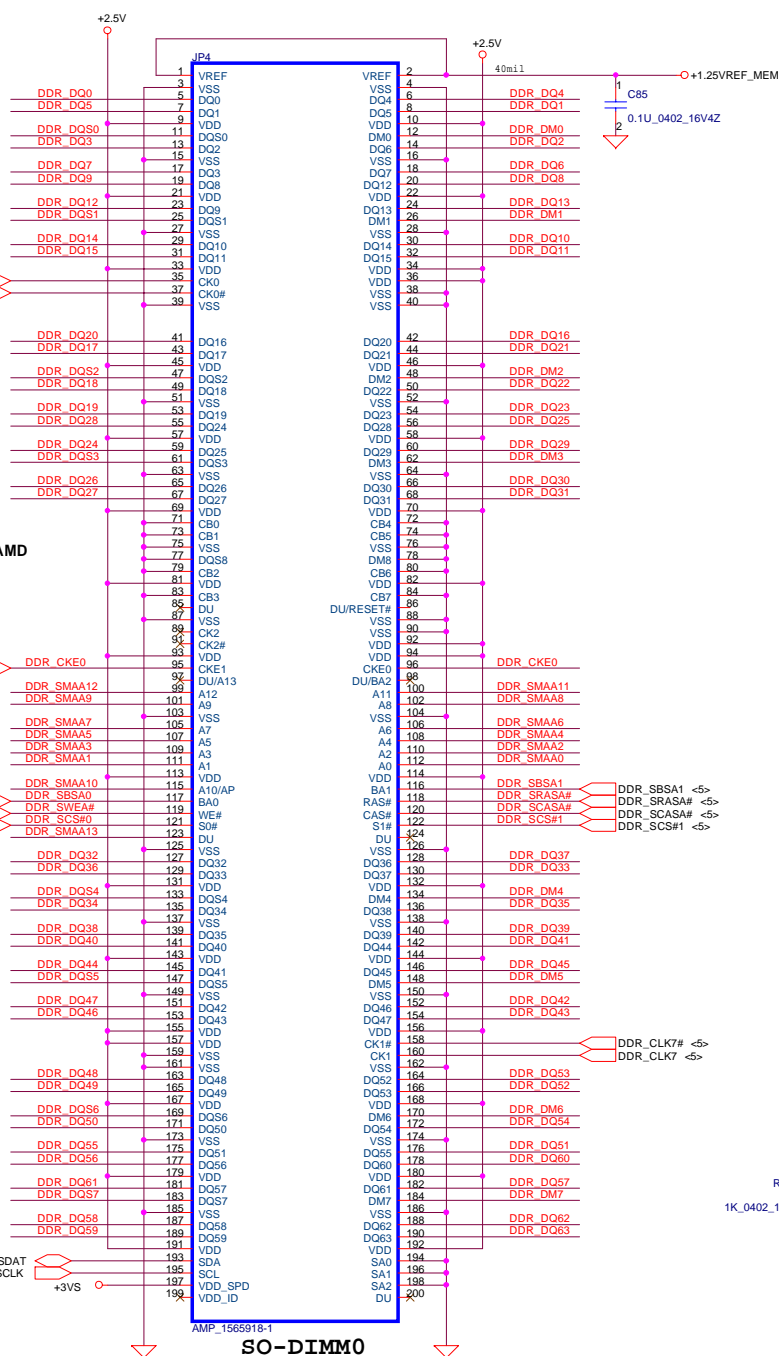


Note:  
DDR\_SMAA13 Recommend for AMD

Layout note


Place these resistors  
close to DIMM0,  
all trace length<500 mil

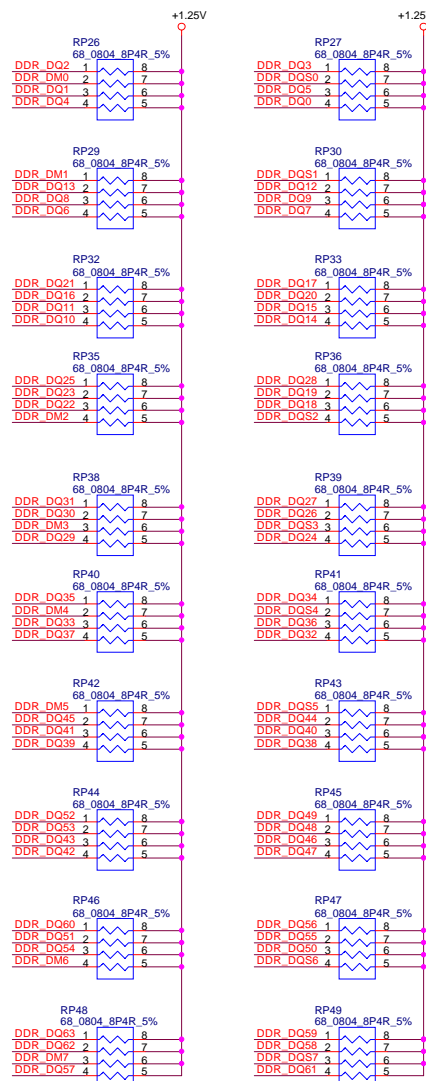
<9,16,20,28> SB\_DAT  
<9,16,20,28> SB\_SCLK  
+3VS







Security Classification				Compal Secret Data				Title			
Issued Date				Deciphered Date				DDR-SODIMM0			
2005/03/01				2005/04/06				LA-2771			
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Date				Tuesday, August 30, 2005				Sheet 8 of 53			





<B> DDR\_DQS[0..7]  DDR\_DQS[0..7]  
 <B> DDR\_DQ[0..63]  DDR\_DQ[0..63]  
 <B> DDR\_DM[0..7]  DDR\_DM[0..7]  
 <S> DDR\_SMA[0..13]  DDR\_SMA[0..13]

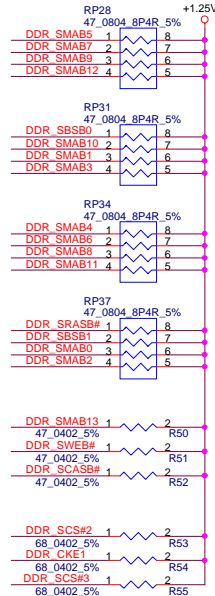
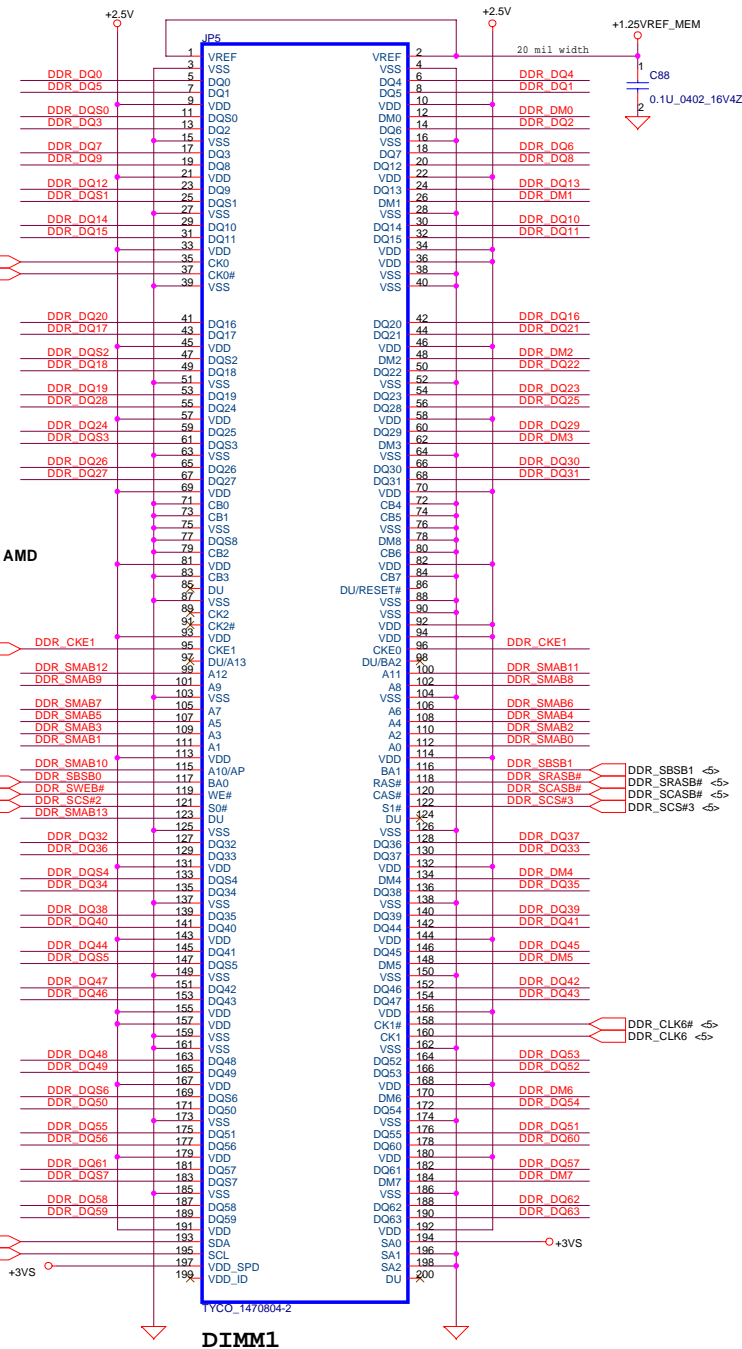


Note:  
DDR\_SMAA13 Recommend for AMD

<S> DDR\_CKE1  DDR\_CKE1  
 <S> DDR\_SBSB0  DDR\_SBSB0  
 <S> DDR\_SWEB#  DDR\_SWEB#  
 <S> DDR\_SCS#2  DDR\_SCS#2

Layout note  
Place these resistor  
closely DIMM1,  
all trace  
length<=800mil

<B,16,20,28> SB\_SDAT  SB\_SDAT  
 <B,16,20,28> SB\_SCLK  SB\_SCLK

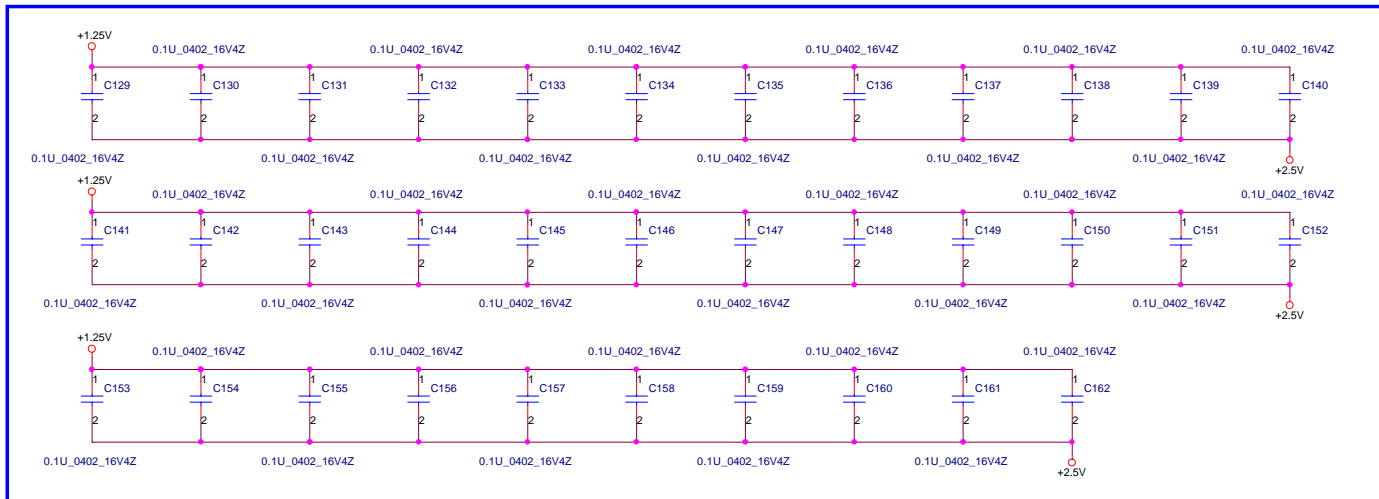
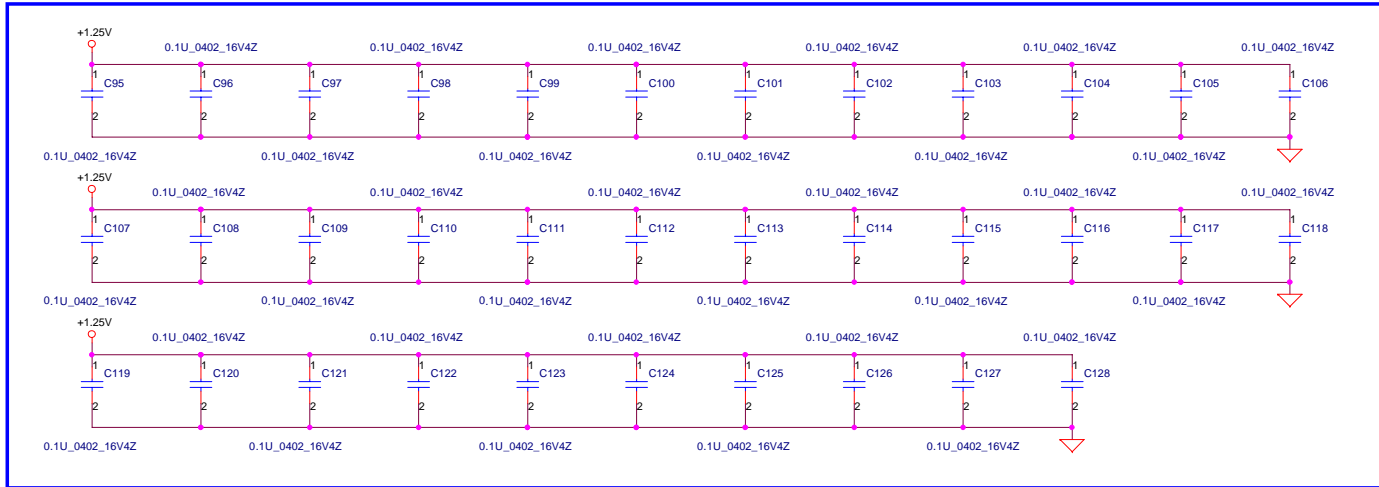
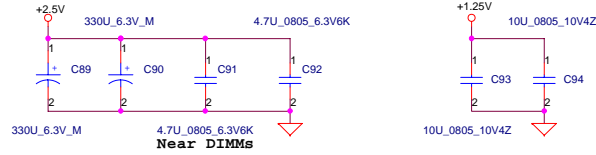


Layout note  
Place these resistor  
close by DIMM1,  
all trace length  
Max=0.8"

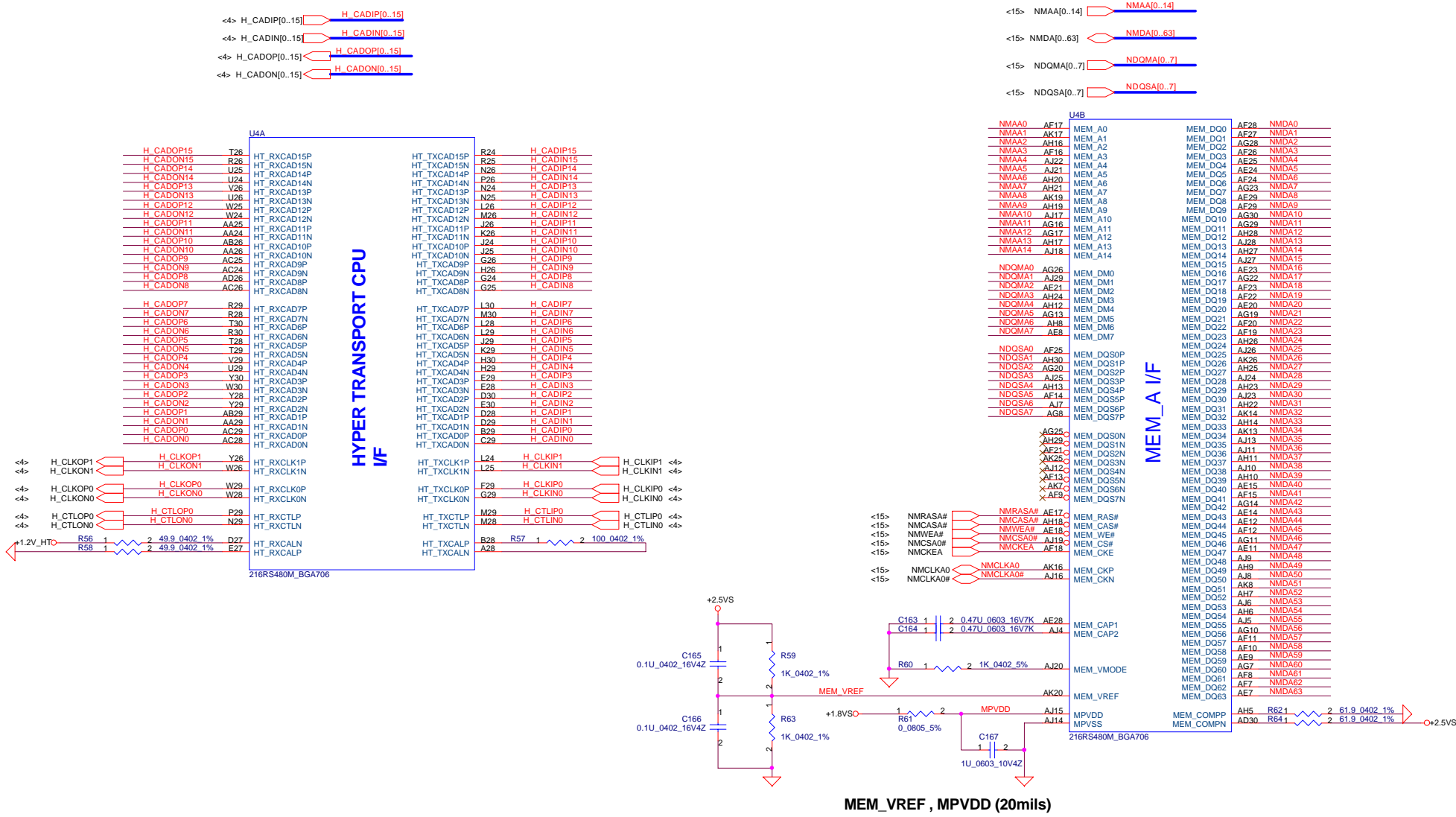
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	DDR-SODIMM1	
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				Custom	LA-2771
				Date	Tuesday, August 30, 2005
				Sheet	9 of 53

**Layout note :**

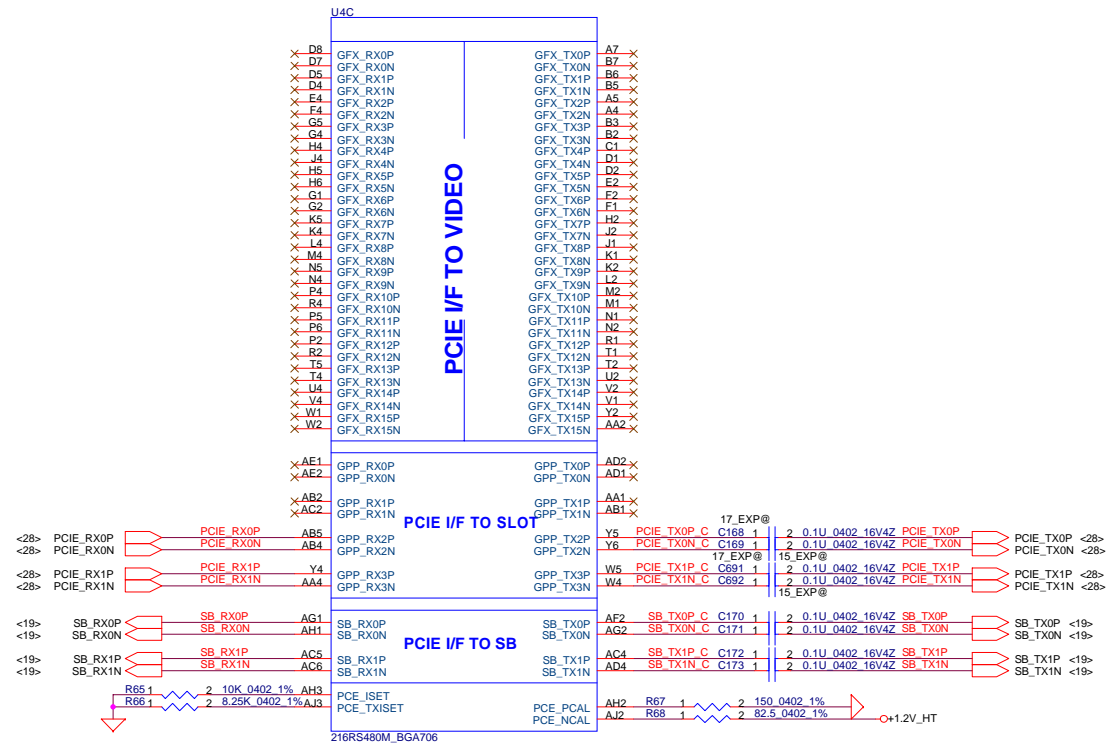
Place one cap close to every 2 pull up resistors termination to +1.25V



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Issued Date	2005/03/01	Deciphered Date	2005/04/06	DDR Decoupling	
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				Custom	LA-2771
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				Rev	0.8

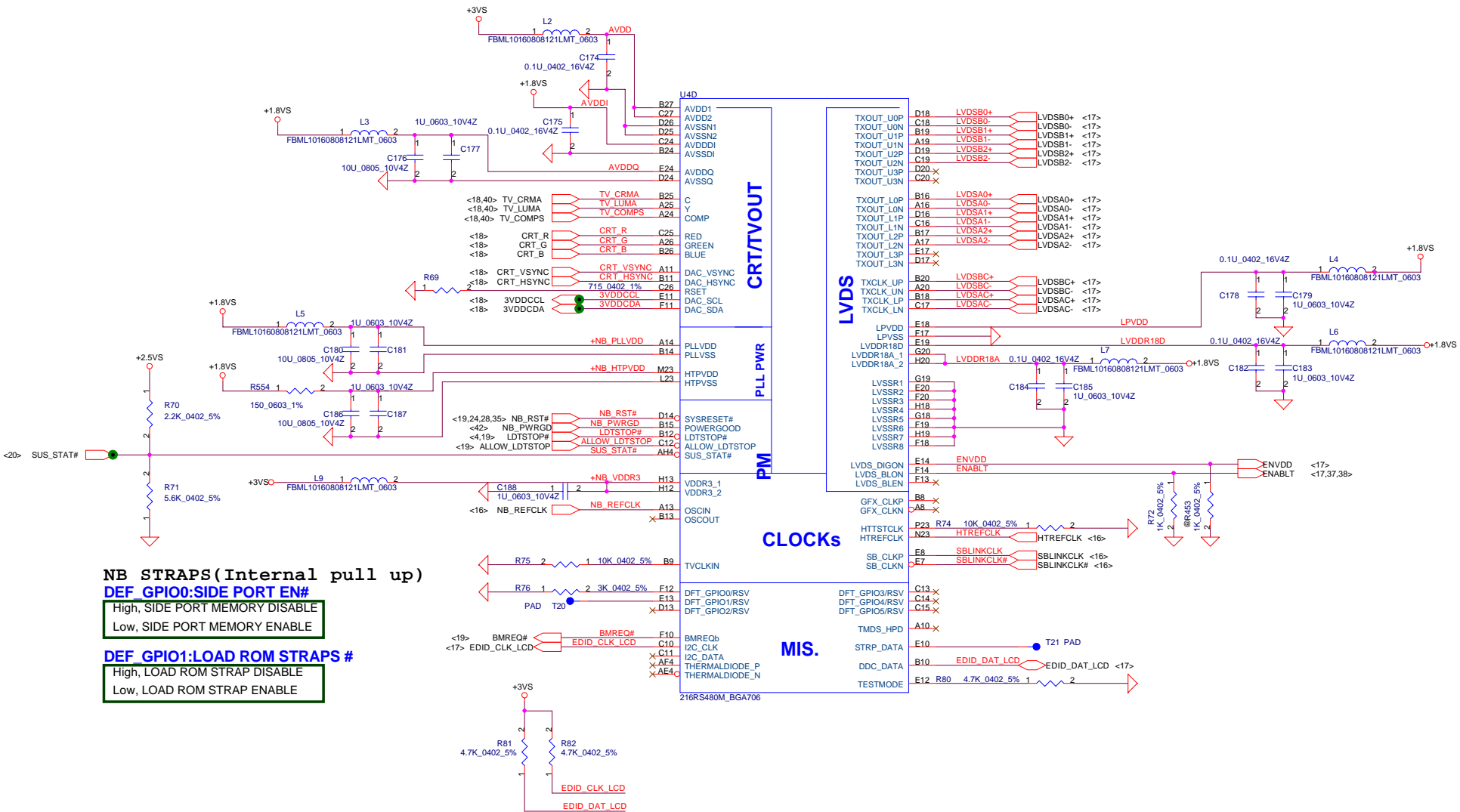


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Issued Date	2005/03/01	Deciphered Date	2005/04/06	Title		
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				Size	Document Number	Rev
				Custom	LA-2771	0.8
				Date:	Tuesday, August 30, 2005	Sheet 11 of 53

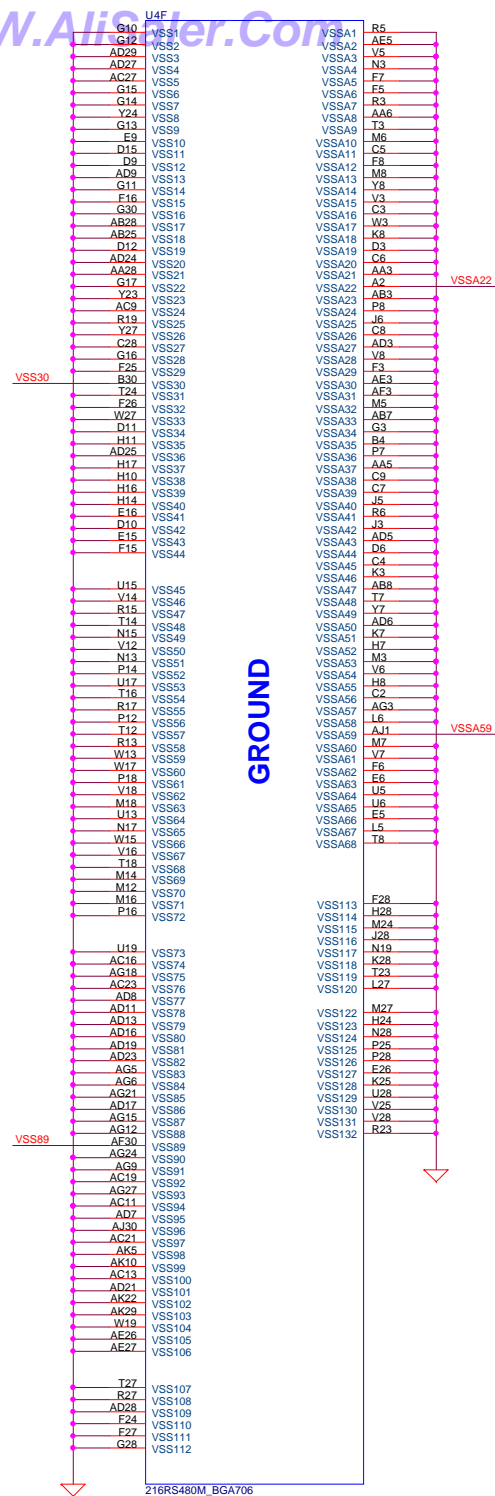


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	RS480M PCIE/DVI Controller	
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				Custom	LA-2771
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				Rev	0.8

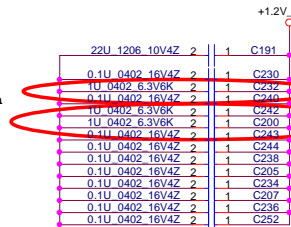
AVDD , AVDDI , AVDDQ , +NB\_PLLVDD , +NB\_HTPVDD  
+NB\_VDDR3 , LPVDD , LVDDR18D , LVDDR18A (20mils)



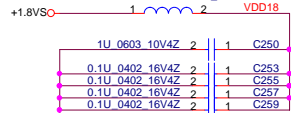
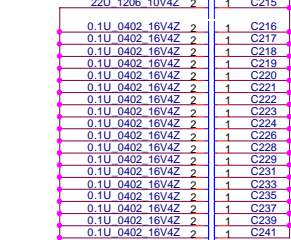
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Issued Date		2005/03/01		Deciphered Date				
		2005/04/06		Title				
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				Size	Document Number		Rev	
				Custom	LA-2771		0.8	
				Date:	Tuesday, August 30, 2005		Sheet 13 of 53	



2005.08.11 for ATI Suggestion



+2.5VS



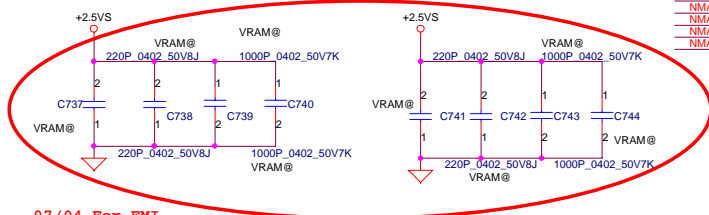
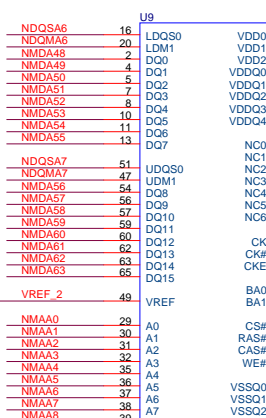
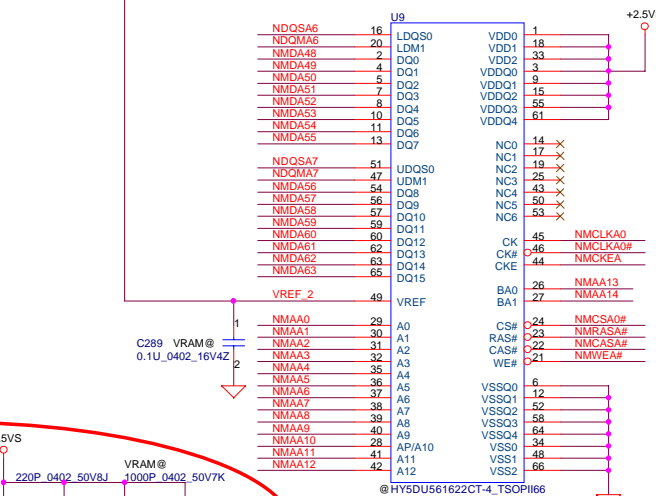
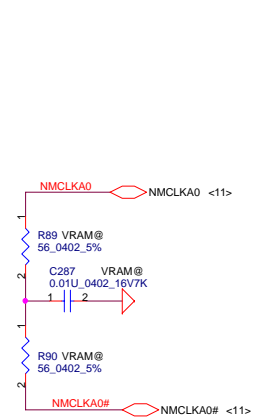
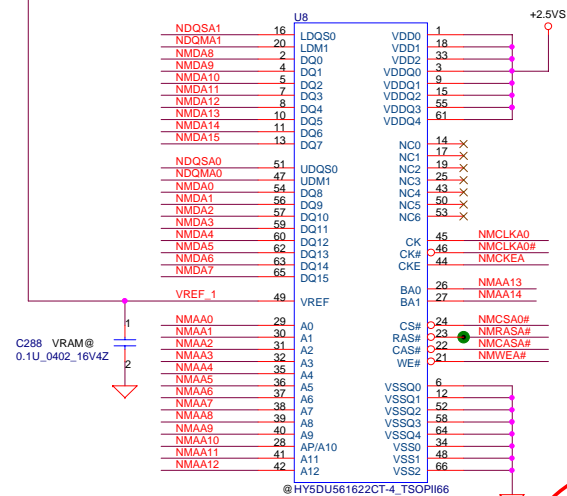
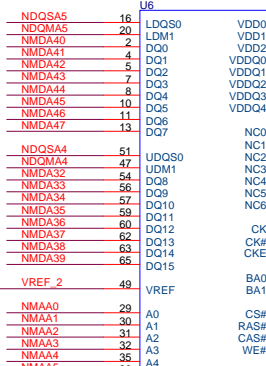
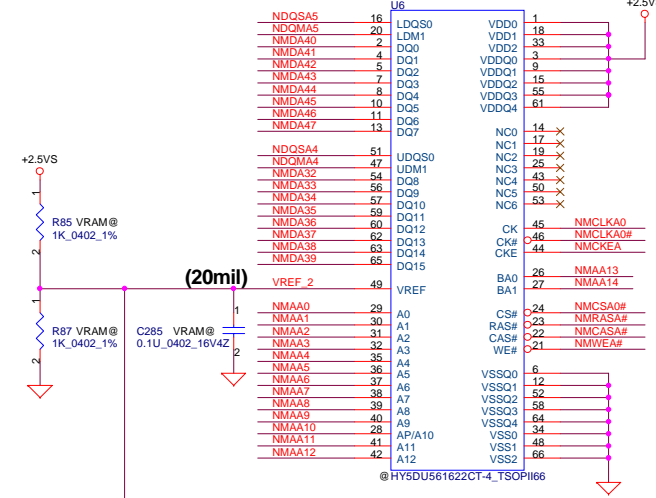
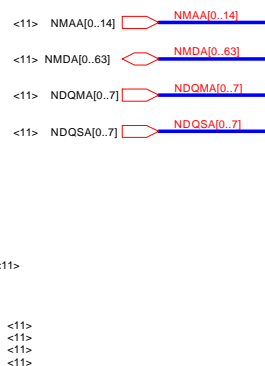
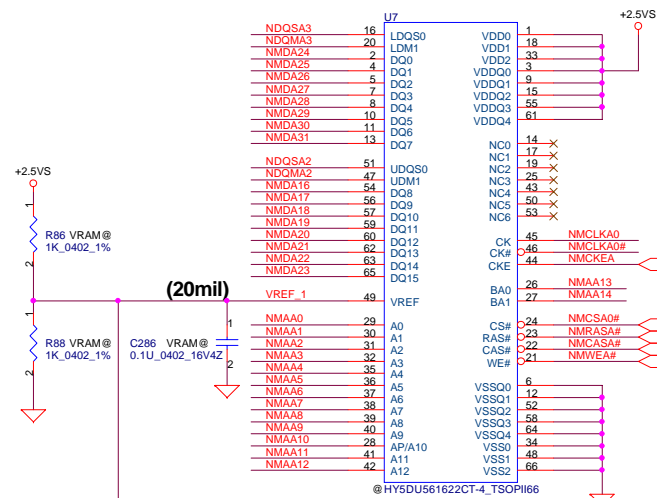
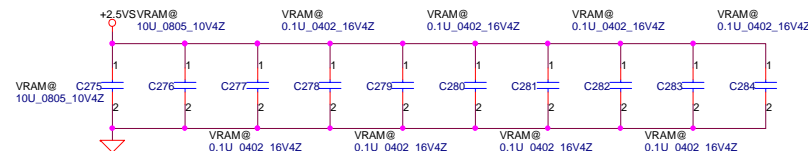
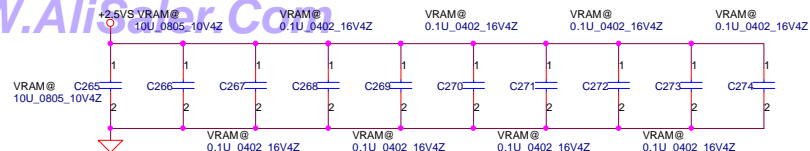
+1.8VS

VDD18

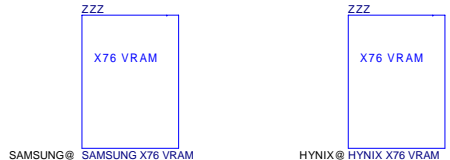
VDD18\_2

VDD18\_3

VDD18\_4

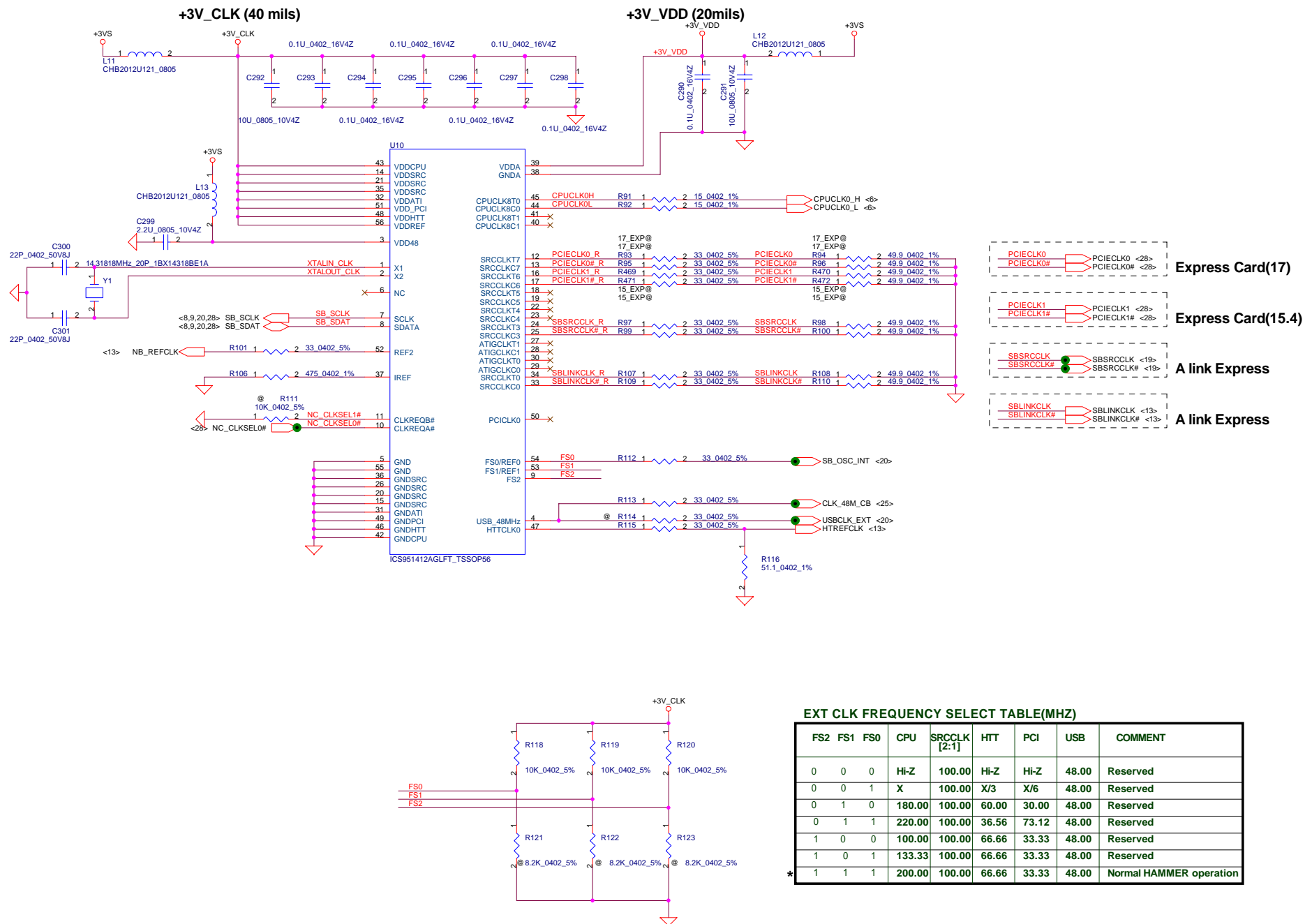


07/04 For EMI



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Size Custom		Document Number		LA-2771		Rev 0.8	
Date:		Tuesday, August 30, 2005		Sheet 15 of 53			

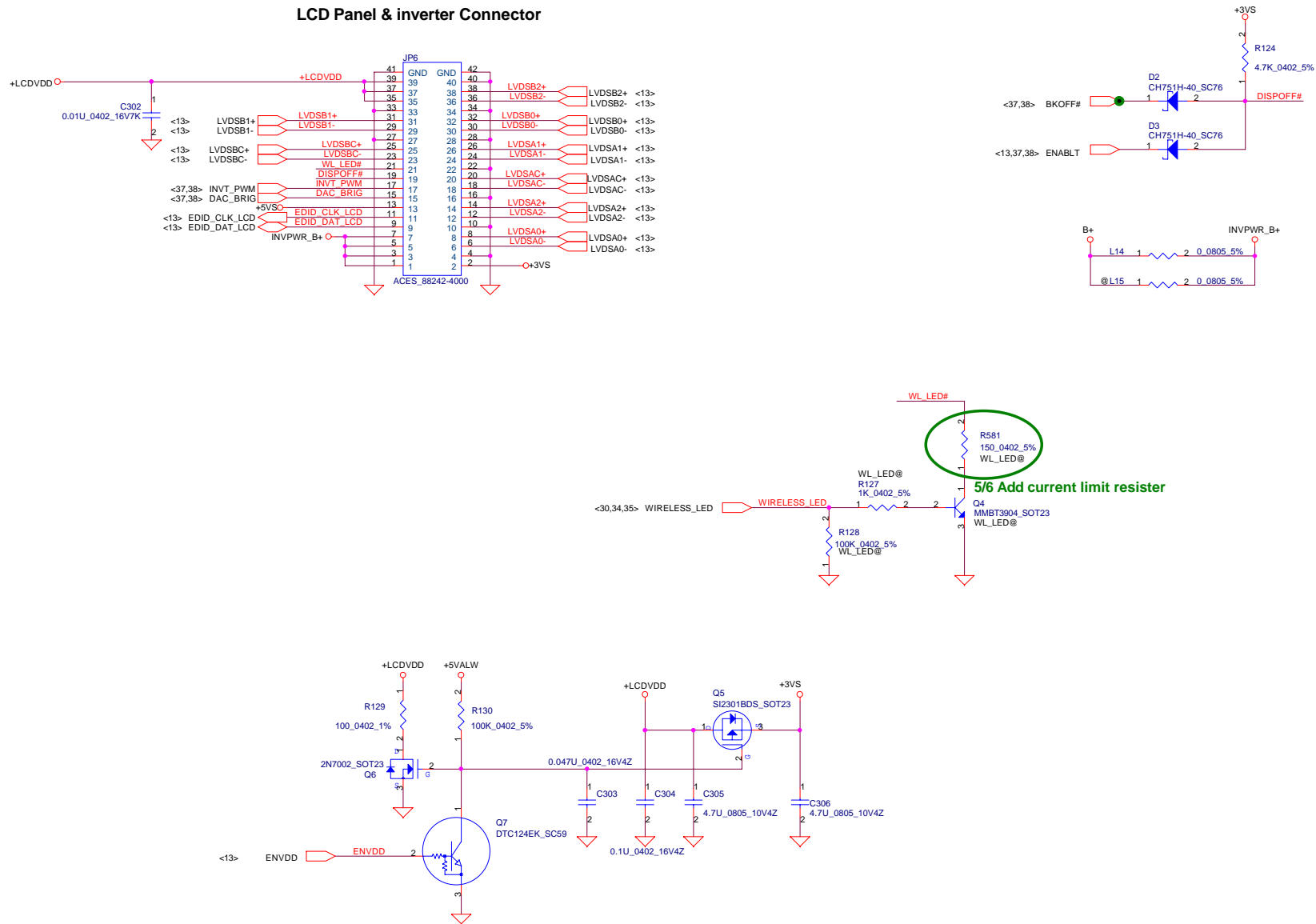




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				Custom	LA-2771	0.8
				Date	Tuesday, August 30, 2005	Sheet 16 of 53

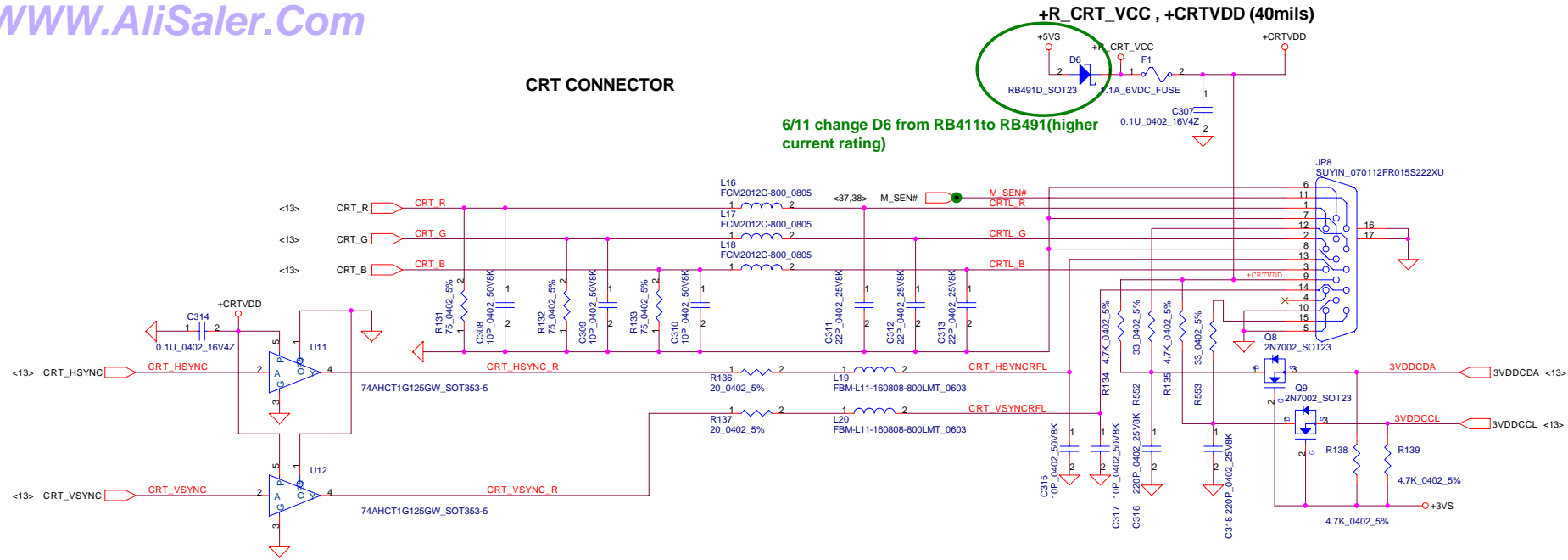
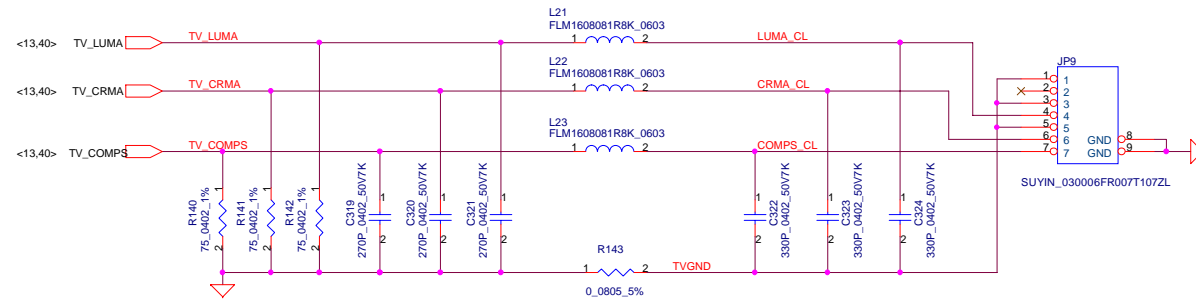


## LCD Panel &amp; inverter Connector

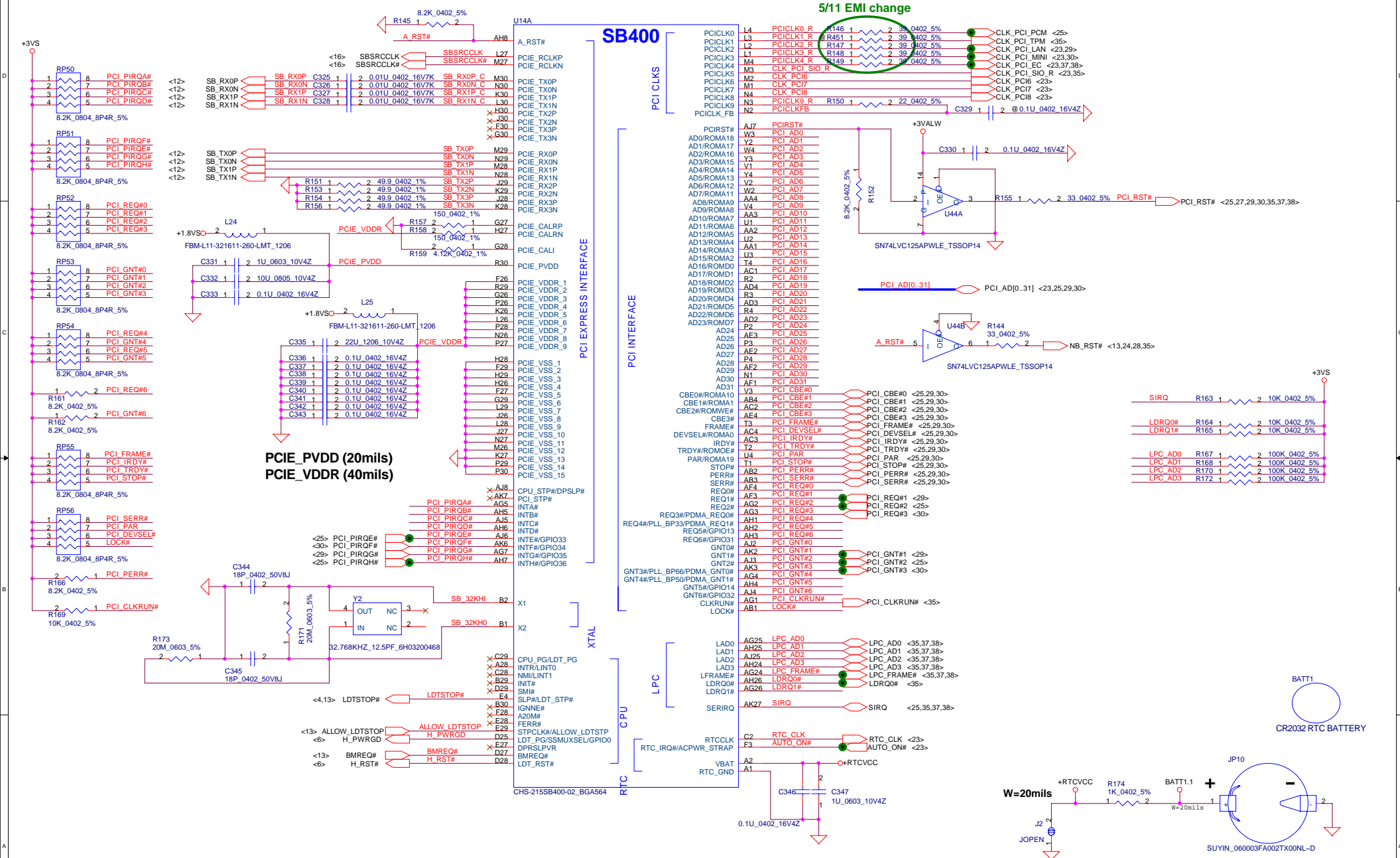


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Issued Date	2005/03/01	Deciphered Date	2005/04/06	LVDS Panel Interface	
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				Custom	LA-2771
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				Tuesday, August 30, 2005	0.8
				Sheet	17 of 53

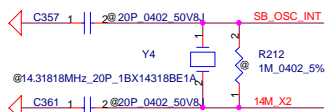
## CRT CONNECTOR

TV-Out Connector  
S-Video

Security Classification	Compal Secret Data			Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	CRT Connector & TV-OUT CONN	
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				Custom	LA-2771
				Date	Tuesday, August 30, 2005
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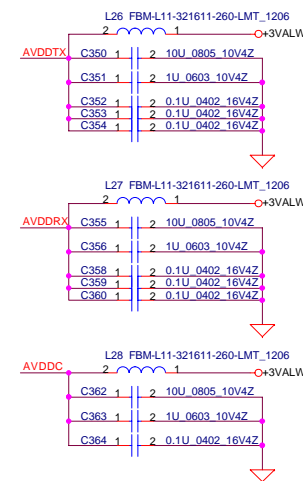
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Issued Date	2005/03/01	Deciphered Date	2005/04/06
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Title		SB400-PCI_EXP/PCI/LPC/RTC	
Size	Document Number	Rev	0.8
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Date	Tuesday, August 30, 2005	Sheet	19 of 53

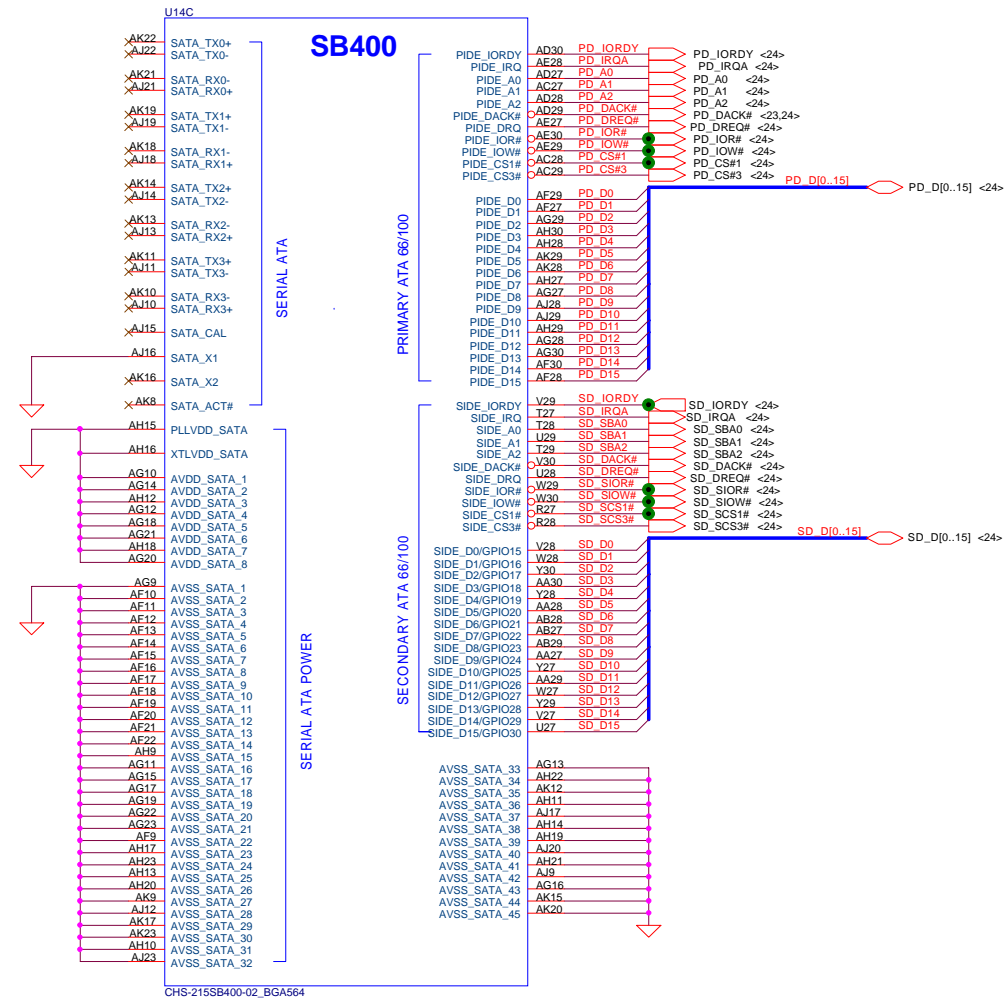


Security Classification	Compal Secret Data			Title		
Issued Date	2005/03/01	Deciphered Date	2005/04/06	SB400-USB/ACPI/AC97/GPIO		
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				LA-2771		
				Date:	Tuesday, August 30, 2005	Sheet 20 of 53



**Left side USB**

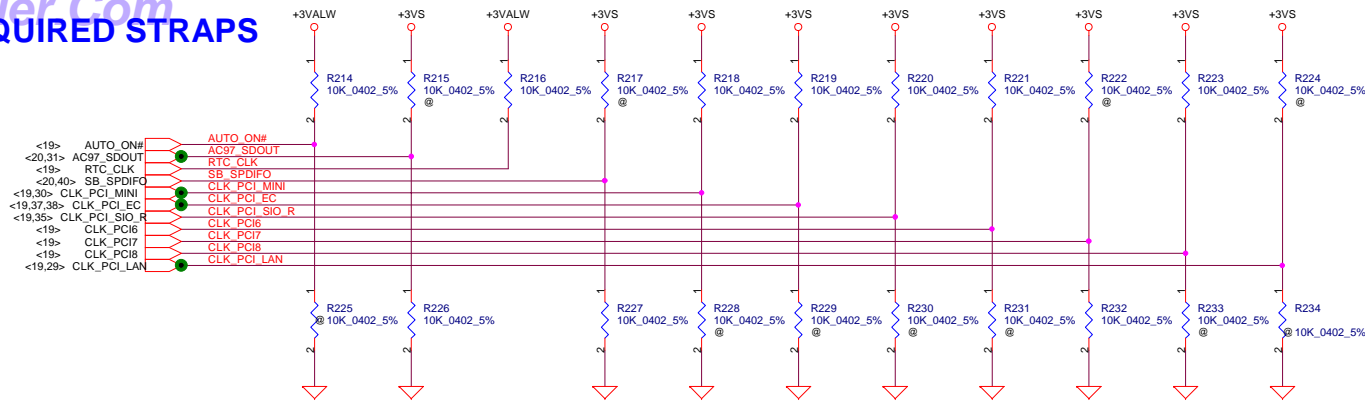




Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	SB400-IDE/SATA	
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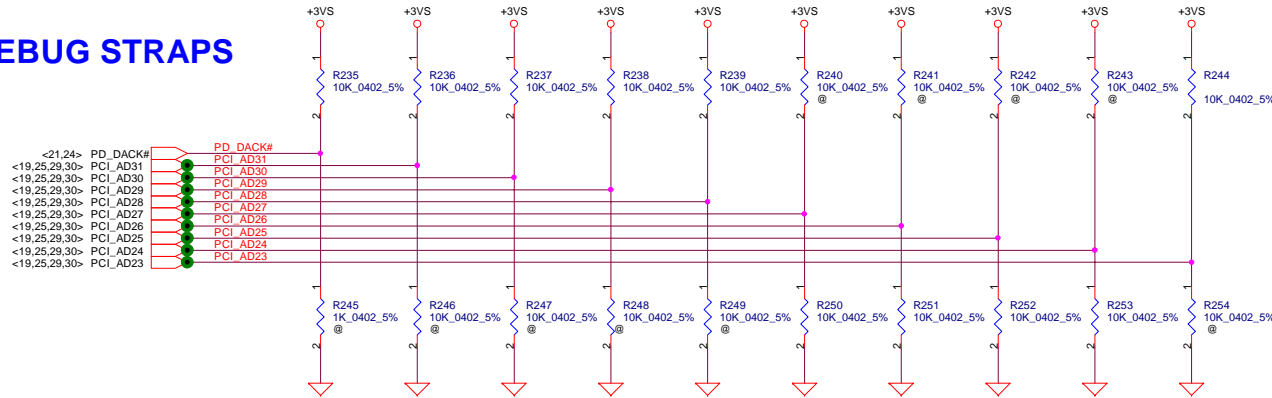


Security Classification	Compal Secret Data					
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Title		
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Size	Document Number				Rev	
Custom	LA-2771				0.8	
Date:	Tuesday, August 30, 2005	Sheet	22	of	53	



	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7	CLK_PCI8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	PCIE_CM_SET LOW DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712 )	SIO 48MHz DEFAULT	48MHz XTAL MODE	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	PCIE_CM_SET High	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM DEFAULT	

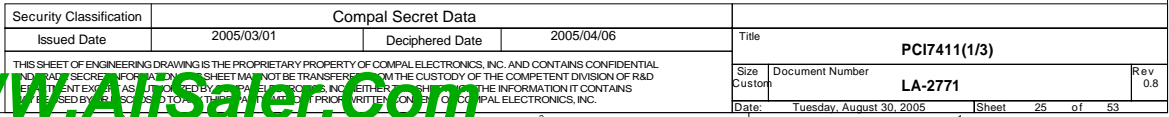
## DEBUG STRAPS

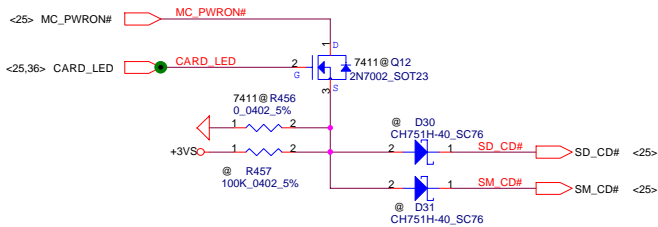


	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

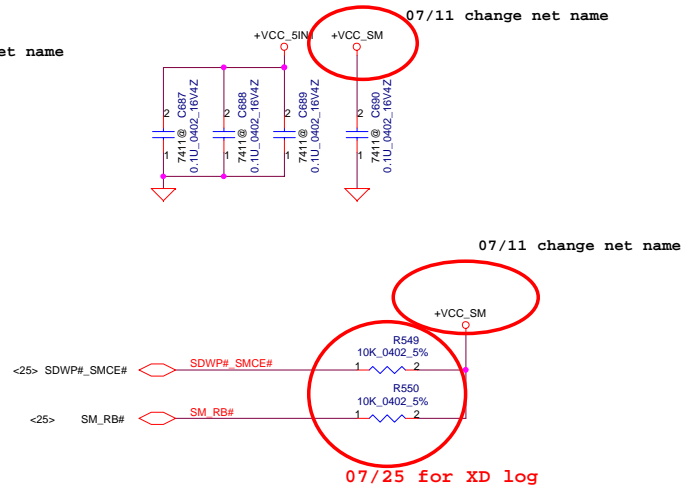
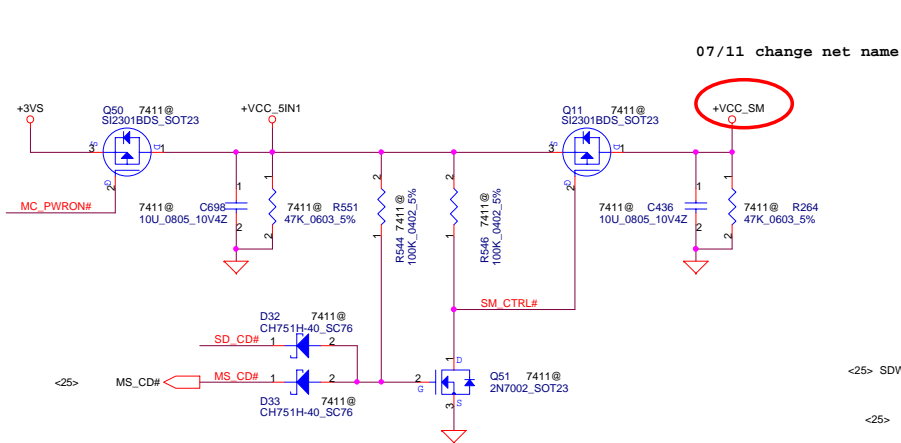
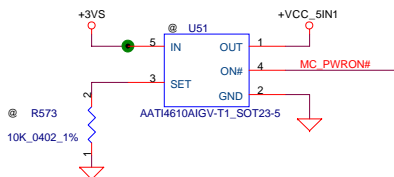
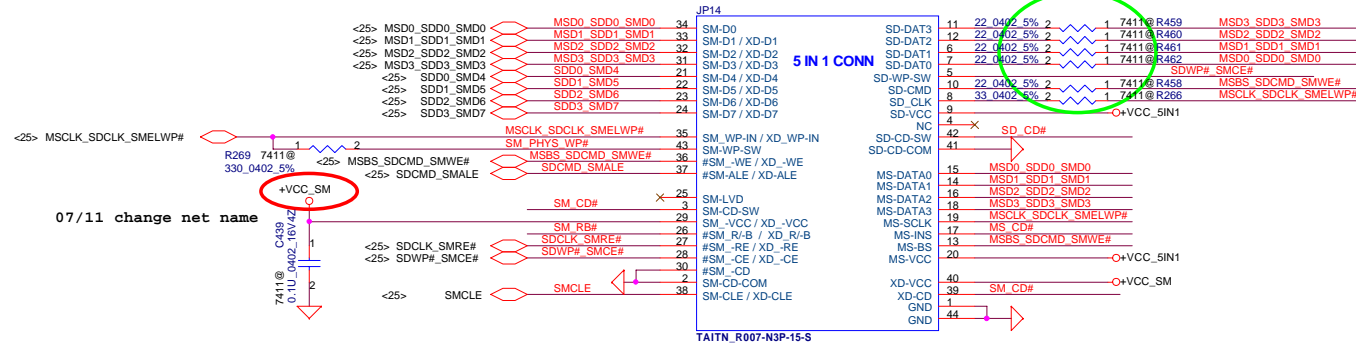




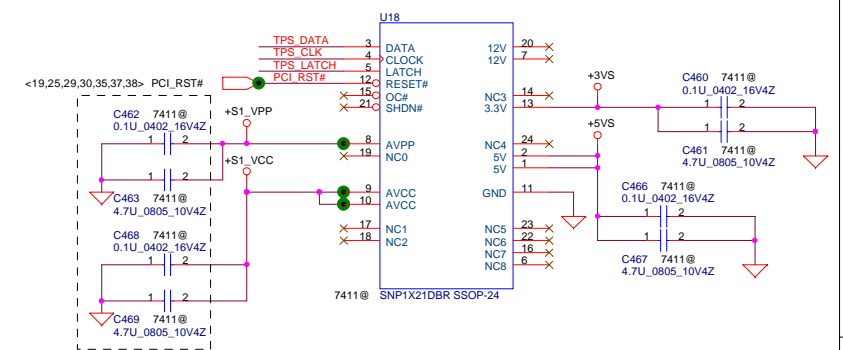




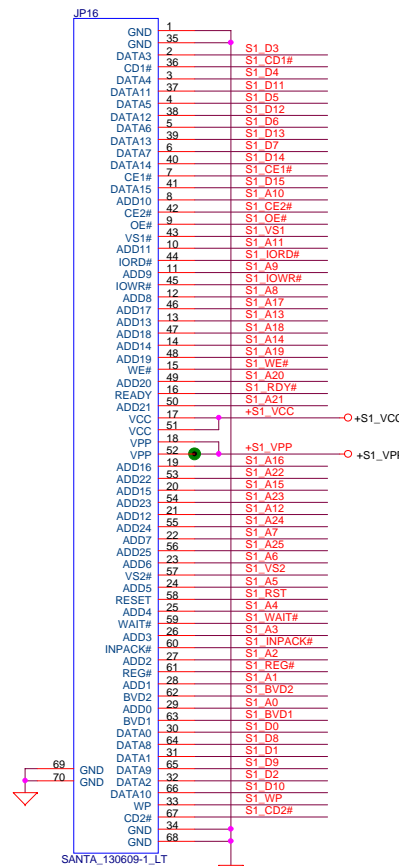
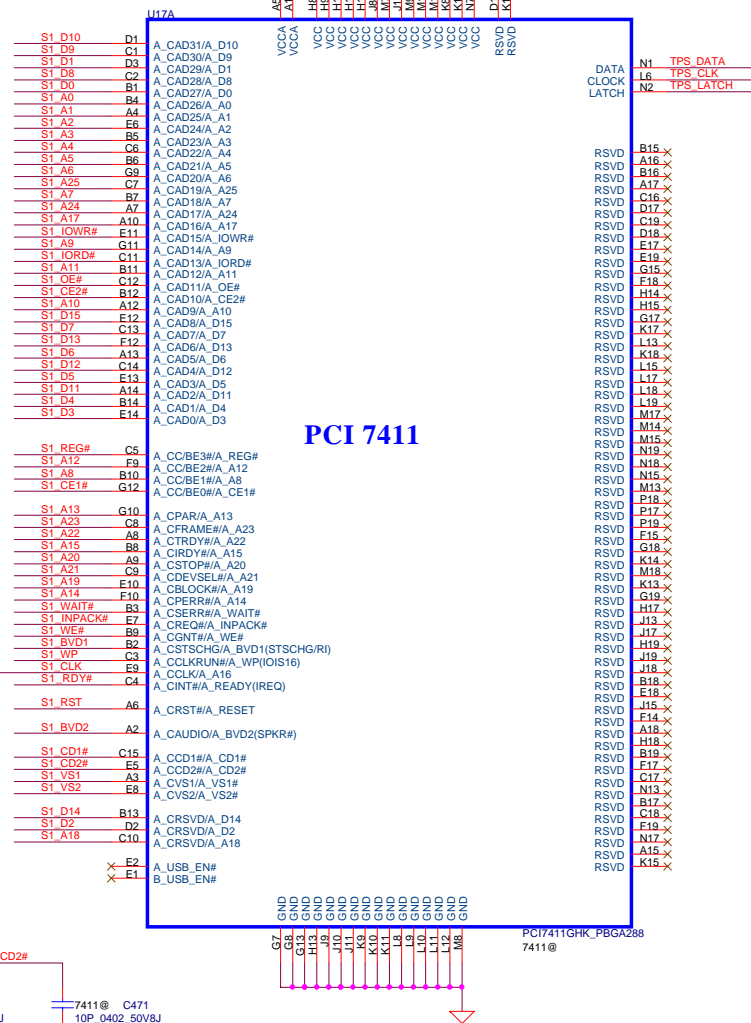
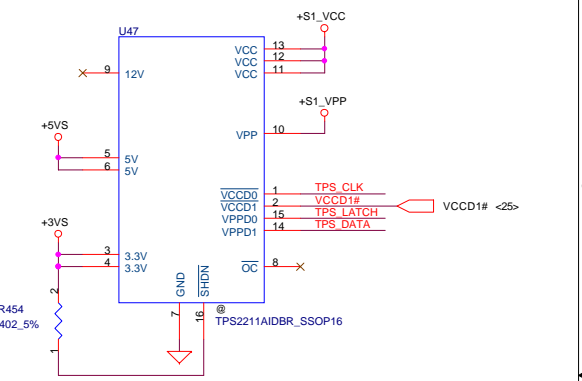
8/23 Relocate Damping resistor to solve Sandisk Card issue



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Issued Date	2005/03/01	Deciphered Date	2005/04/06	PCI7411(2/3)	
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				Custom	LA-2771
				Date	Tuesday, August 30, 2005
				Sheet	26 of 53
				Rev	0.8

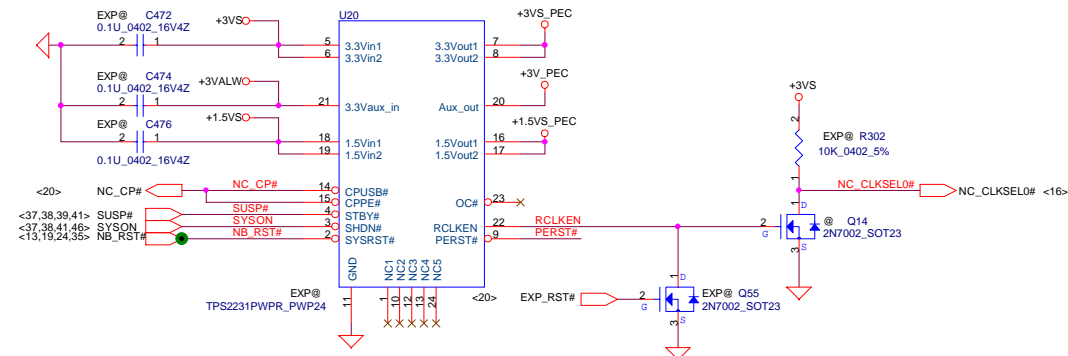


close to card bus conn

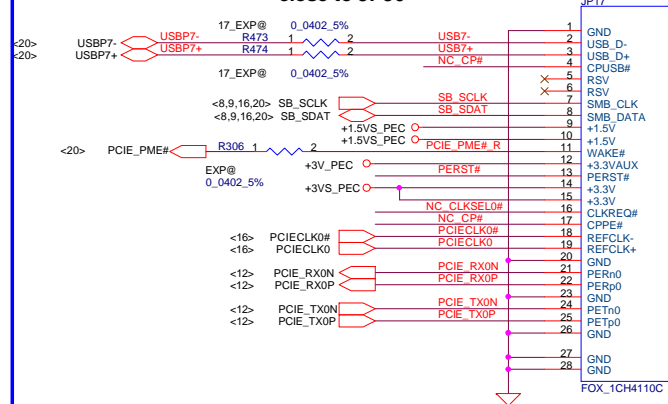


Security Classification		Compal Secret Data			
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Title	PCI7411(3/3)
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				Date:	Tuesday, August 30, 2005
				Sheet	27 of 53

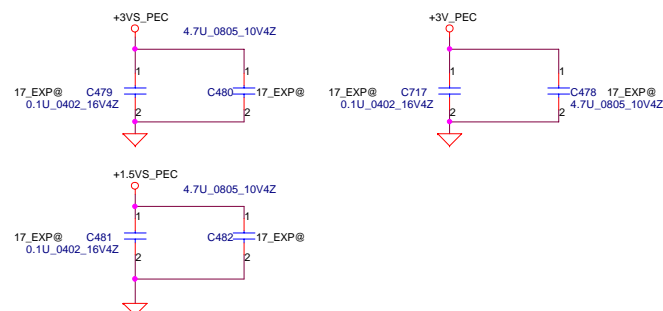
## Express Card Power Switch



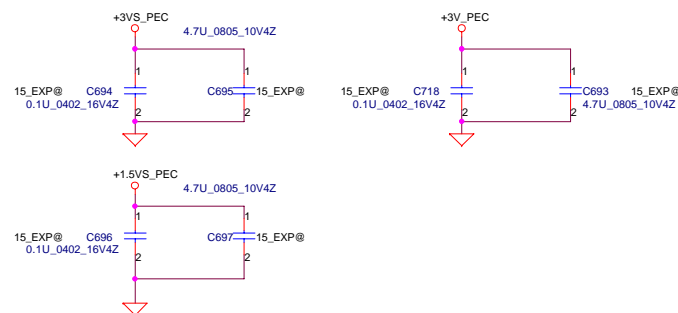
## close to JP36



## Near to Express Card slot. 17

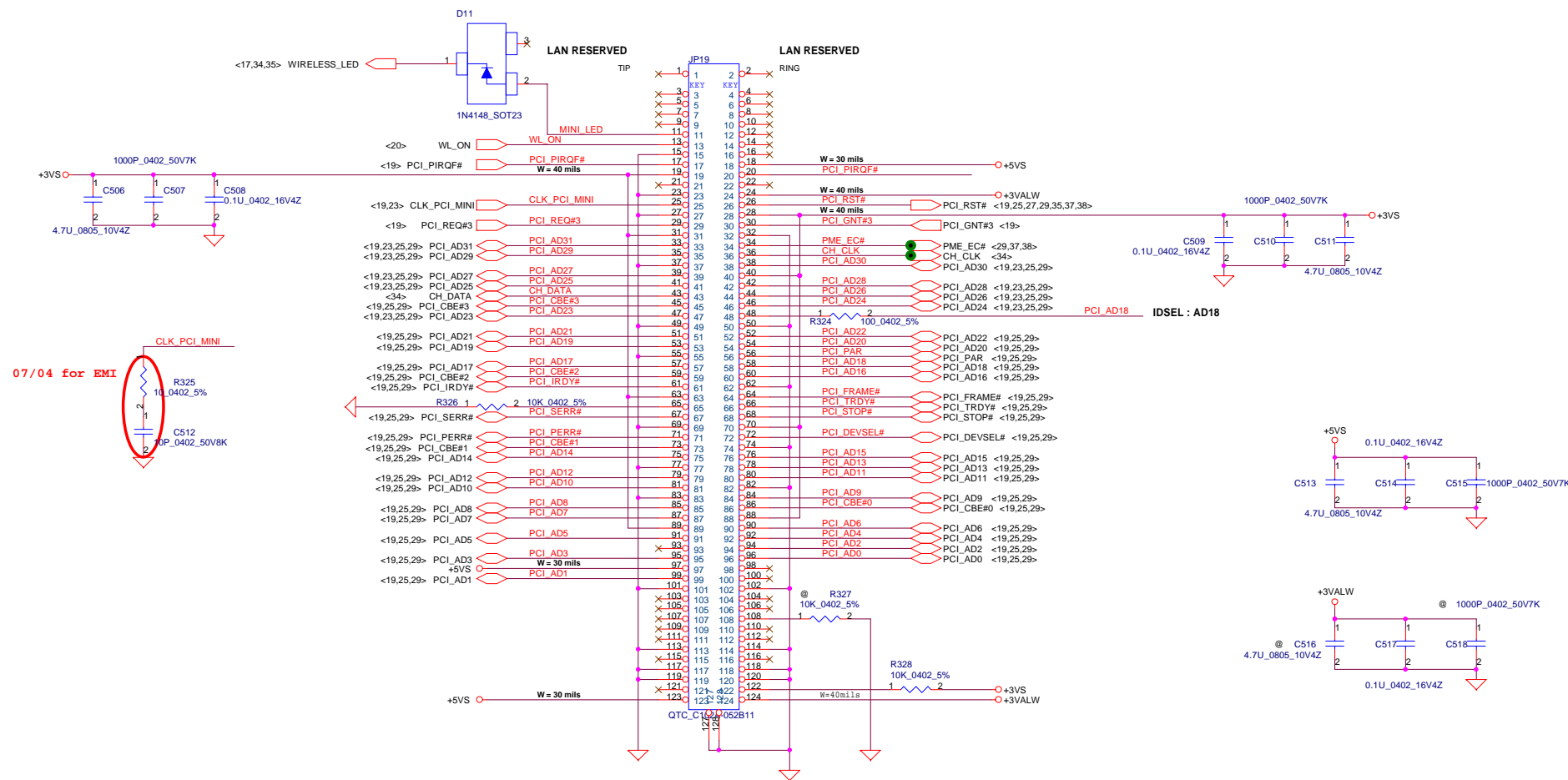


## Near to Express Card slot. 15.4

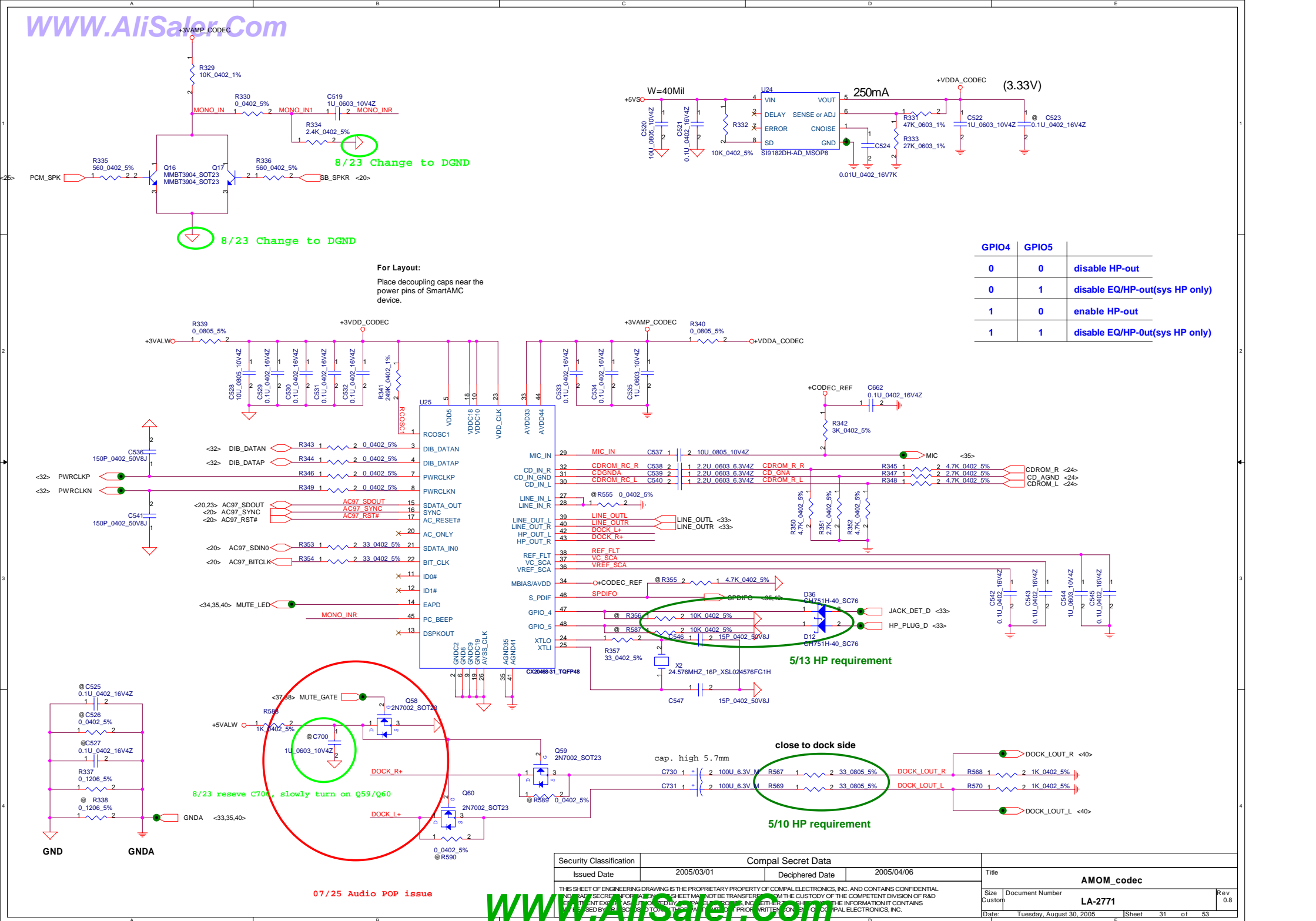


Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	Express Card	
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				Custom	LA-2771
				Date	Tuesday, August 30, 2005
				Sheet	28 of 53
				Rev	0.8



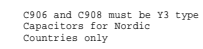


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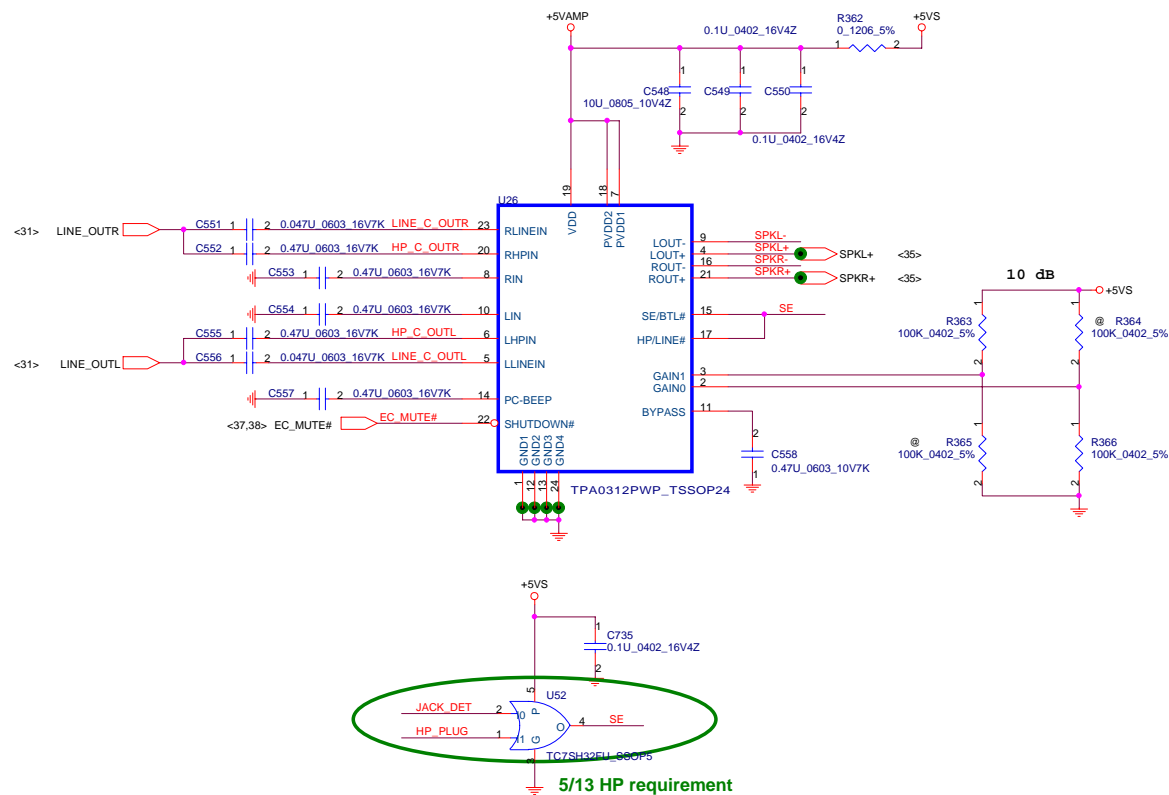
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	AMOM_codec	
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				Custom	0.8
				LA-2771	
				Date	Rev
				Tuesday, August 30, 2005	31 of 53



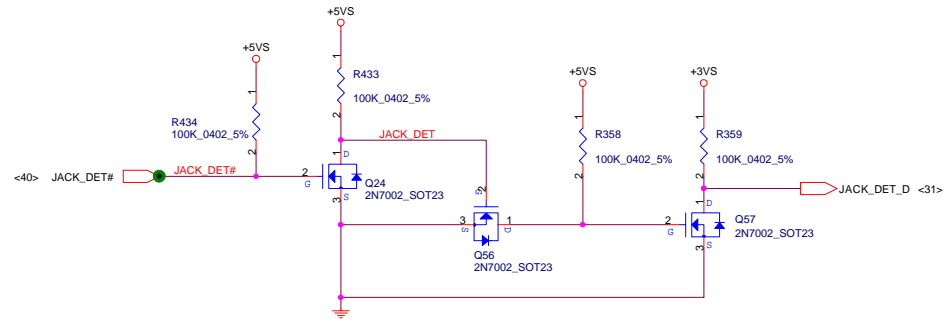
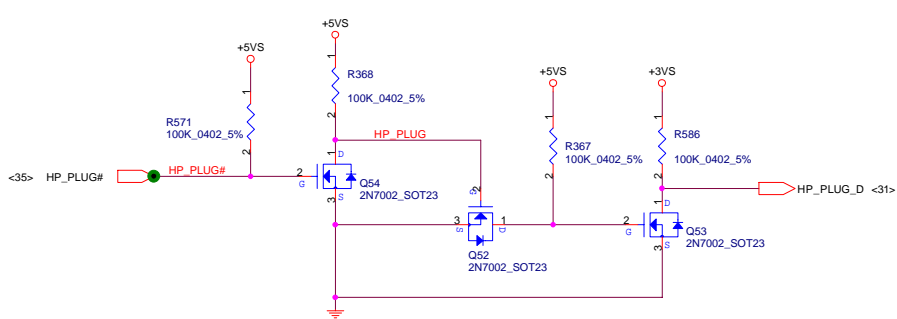
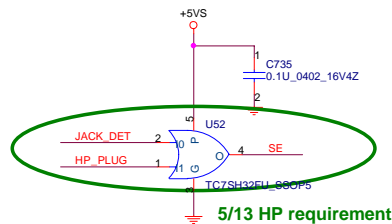
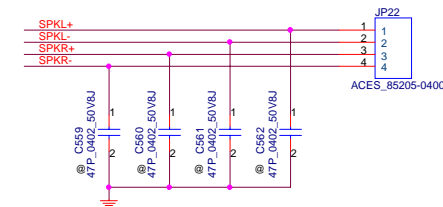


Size Custom	Document Number <b>LA-2771</b>	Rev 0.8
Date:	Tuesday, August 30, 2005	Sheet 32 of 53

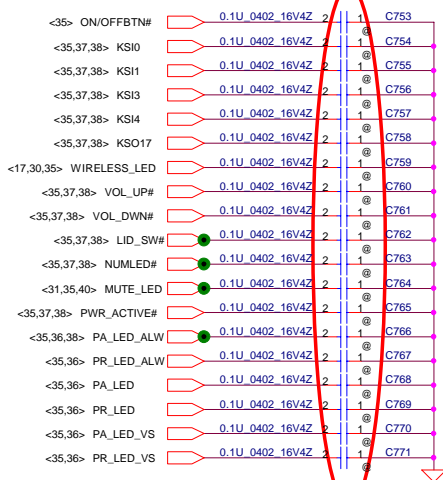
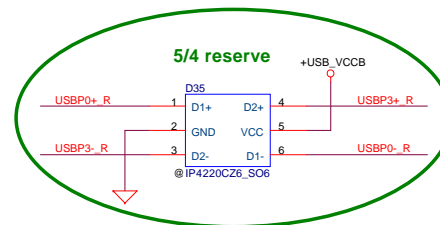
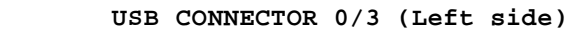




HEADPHONE OUT/LINE OUT			
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



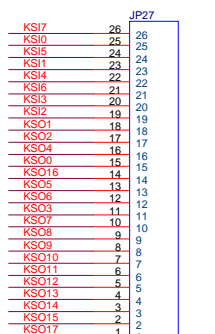
Security Classification				Compal Secret Data				Title			
Issued Date				Deciphered Date				AMP & Audio jack			
2005/03/01				2005/04/06				LA-2771			
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CUSTOMER EXTERNAL USE ONLY				Document Number				0.8			
Date				Tuesday, August 30, 2005				Sheet 33 of 53			



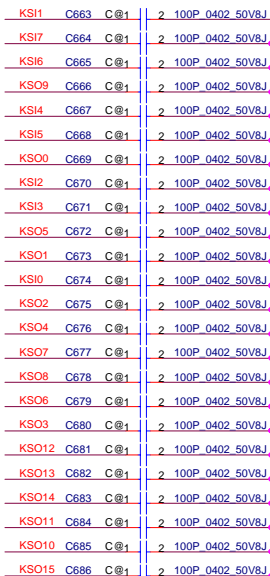
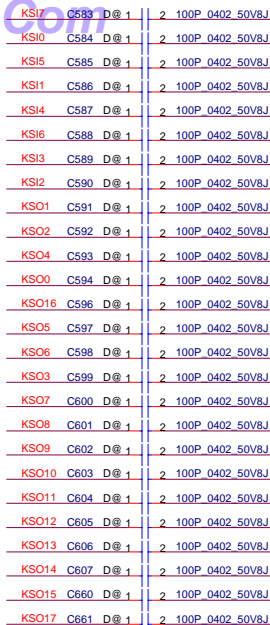
2005.08.11 for EMI solution

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					Size Custom	Document Number	
Date:		Tuesday, August 30, 2005			Sheet	34	of 53

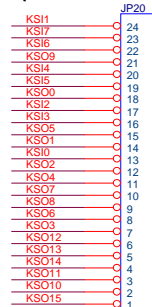
## INT\_KBD CONN.( TYPE "D" KB)



ACES 85201-2605

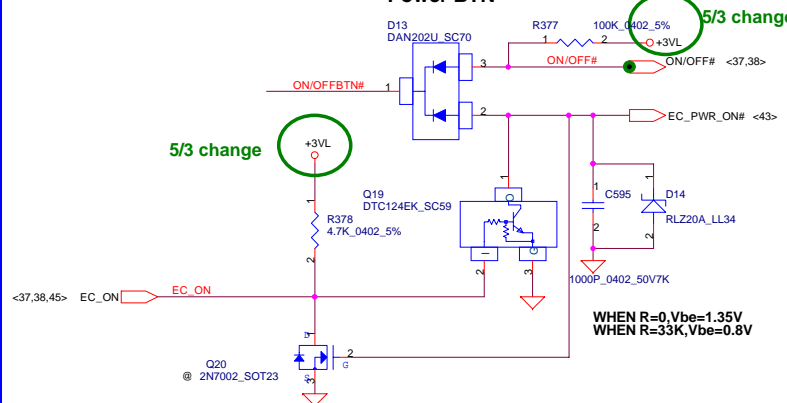


#### 15.4 ( TYPE "C" KB)

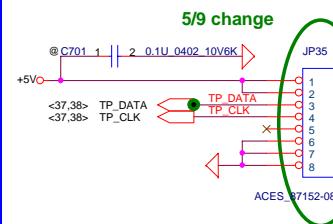


ACES 85201-2405

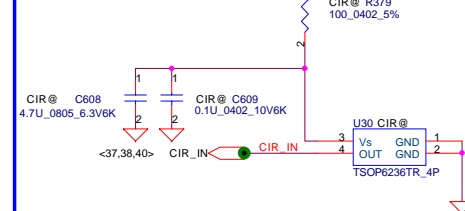
**Power BTN**



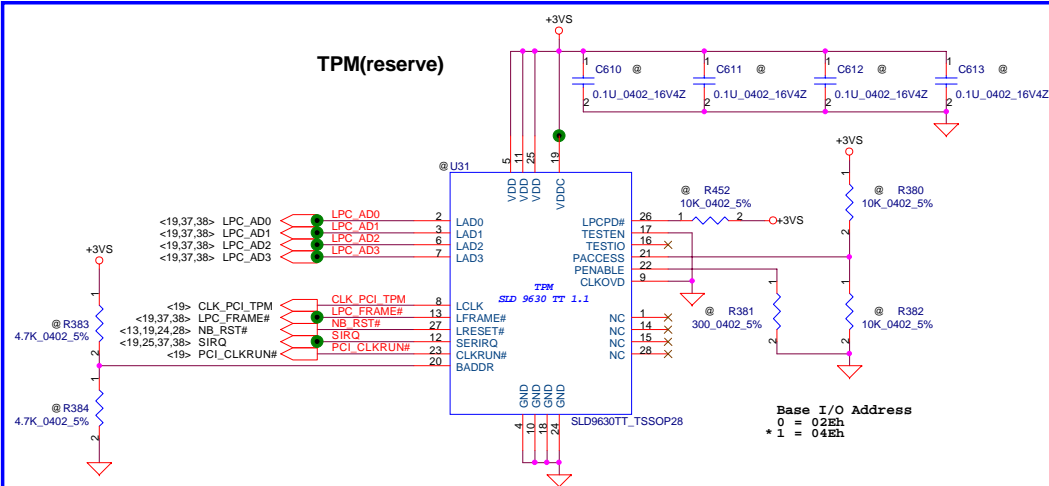
## TP to MB CONN



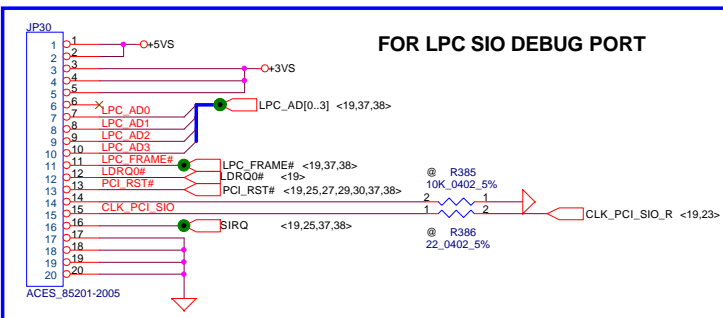
## Consumer IR



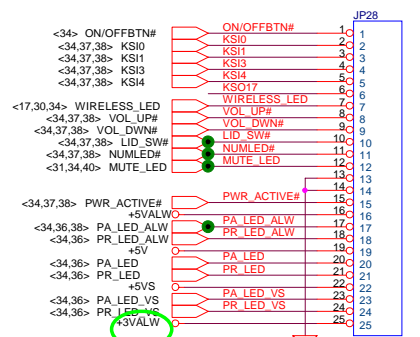
## TPM(reserve)



FOR LPC SIO DEBUG PORT

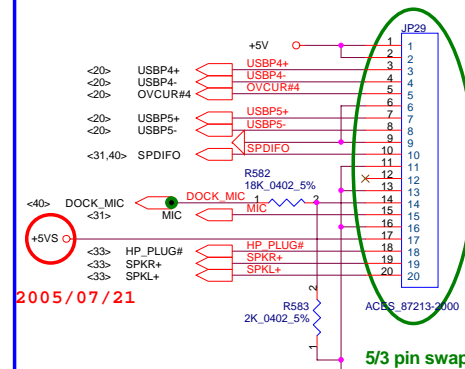


### Switch board conn



## 8/23 Add +3VALW power rail for Boxster lid Switch

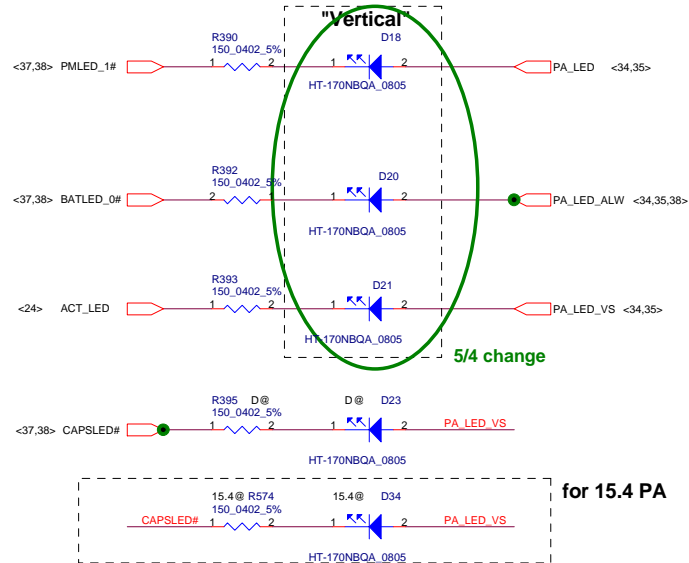
### Audio board conn



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				2005/04/06	
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				KBD,ON/OFF,T/P,LED/B,DEBUG	
				Size Custom	Document Number
				LA-2771	
				Date:	Tuesday, August 30, 2005
				Sheet	35 of 53

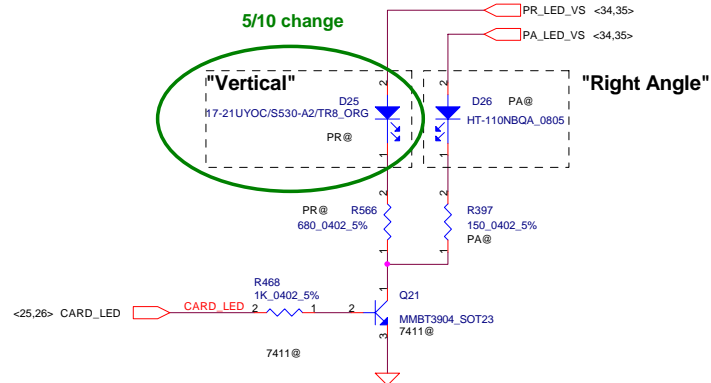
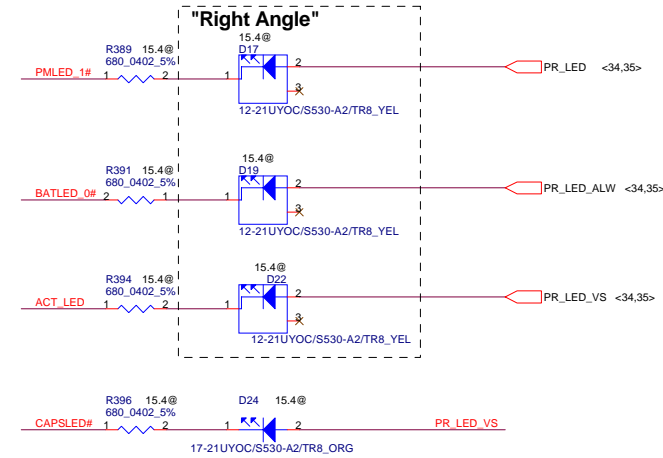
For PA

FOR POWER BUTTON BACKLIGHT SYSTEM POWER

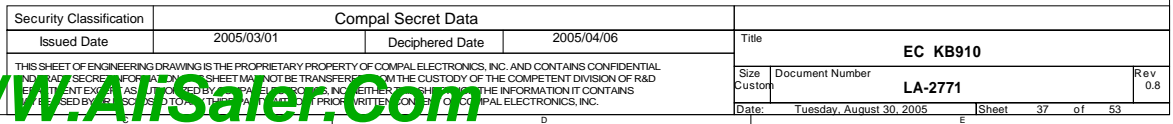


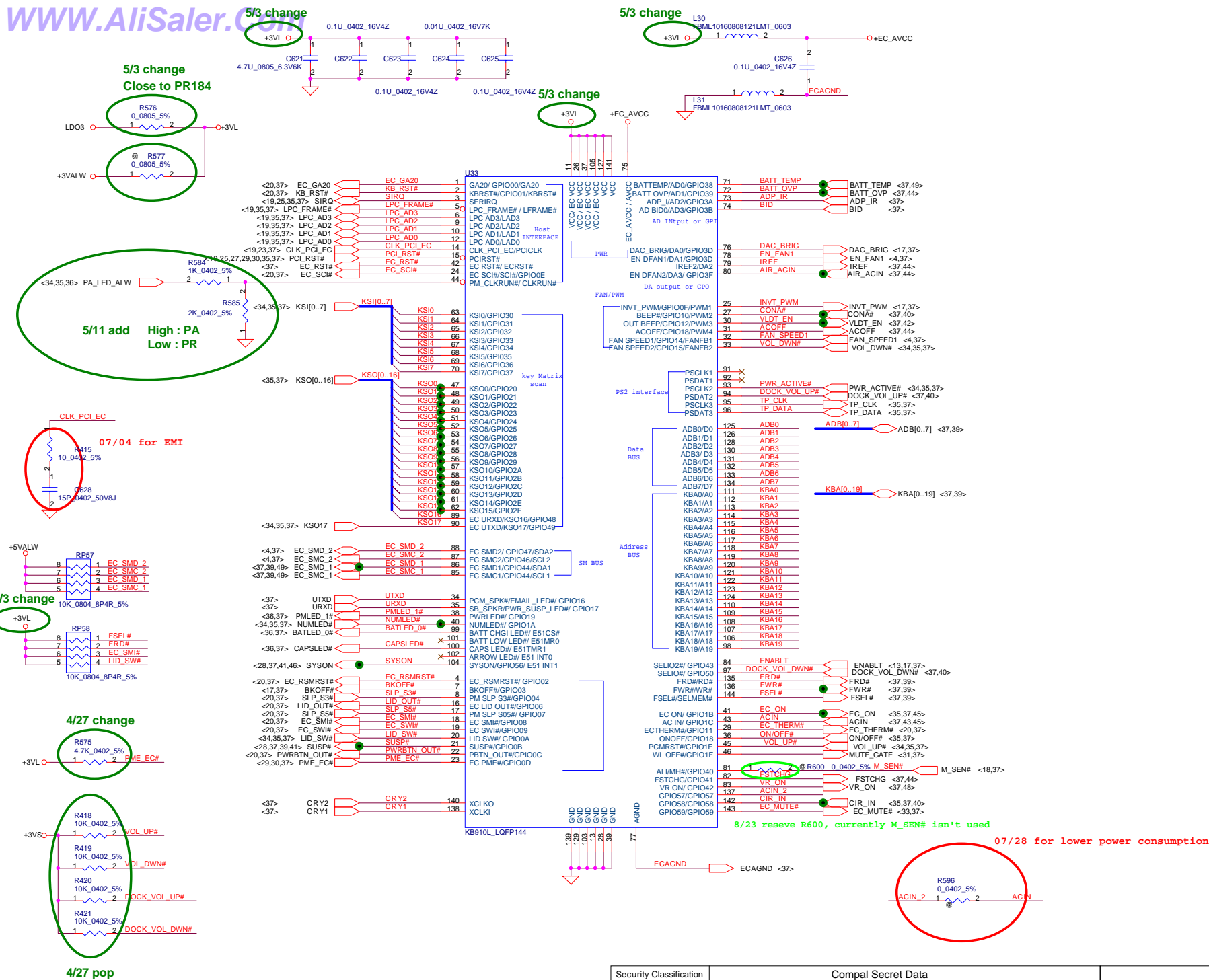
For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER



Security Classification	Compal Secret Data			Title		
Issued Date	2005/03/01	Deciphered Date	2005/04/06	INDICATE LED		
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				Custom	LA-2771	0.8
				Date	Tuesday, August 30, 2005	Sheet 36 of 53



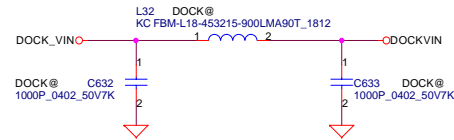


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Title		EC KB910L	
Size	Document Number	Rev	
Custom	LA-2771	0.8	
Date	Tuesday, August 30, 2005	Sheet	38 of 53

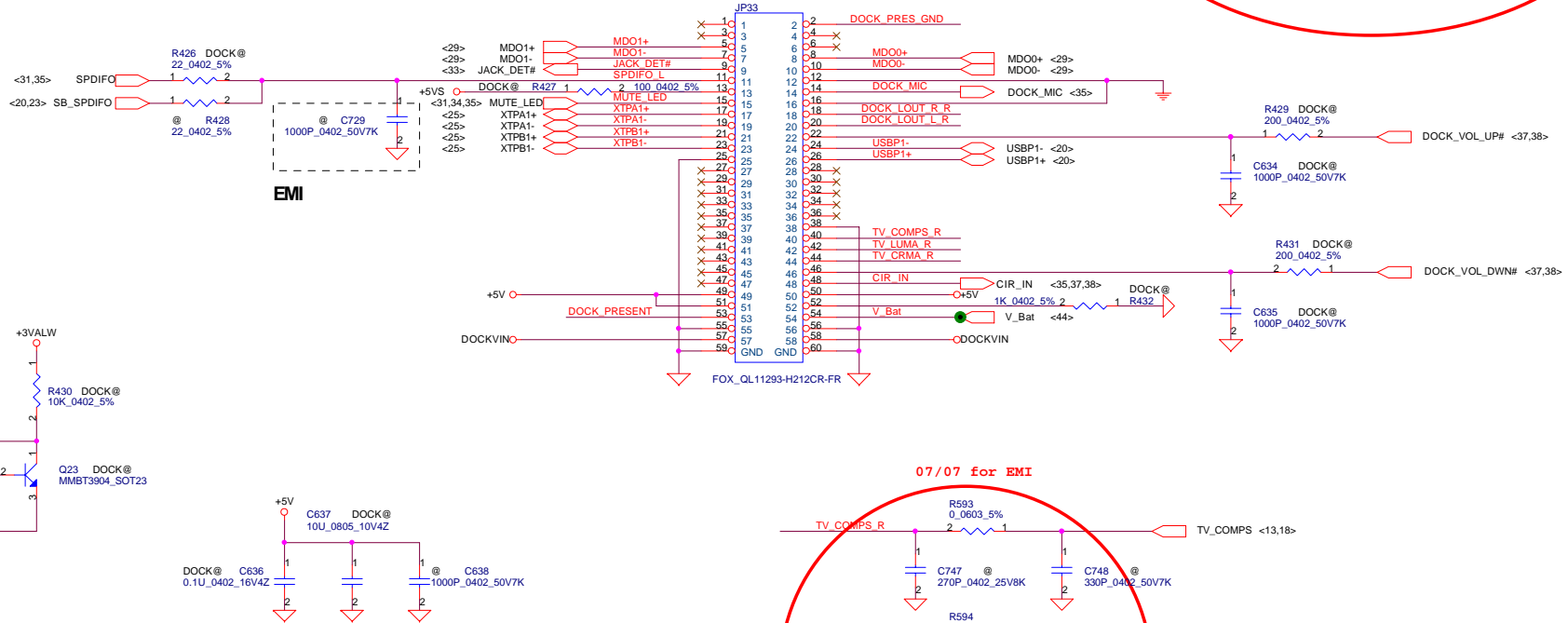


**WWW.AliSaler.Com**

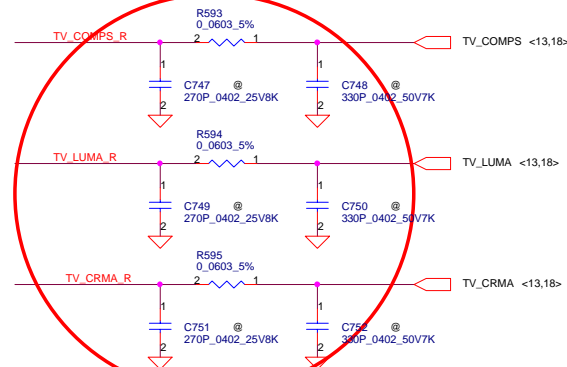




Tampa 2

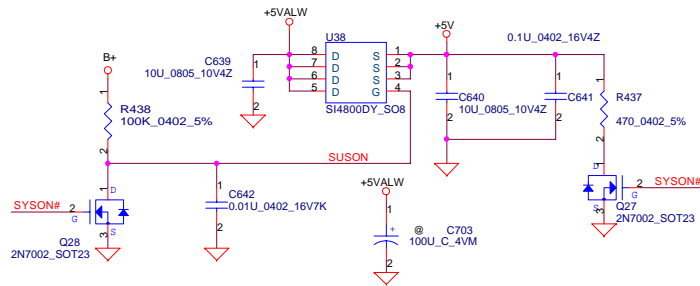


07/07 for EMI

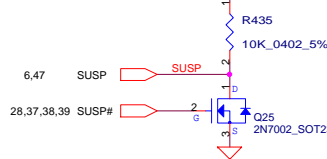




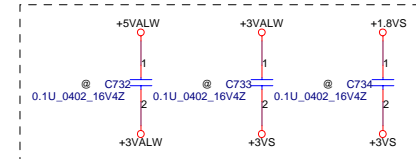
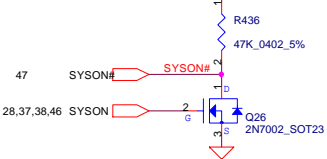
### +5VALW to +5V Transfer



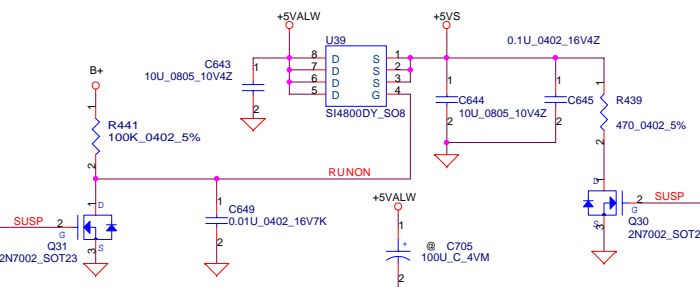
### +5VALW to +5V Transfer



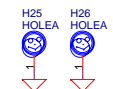
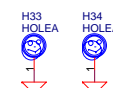
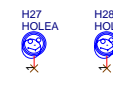
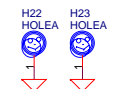
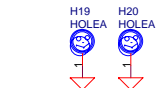
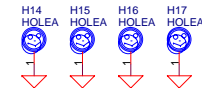
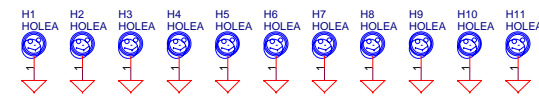
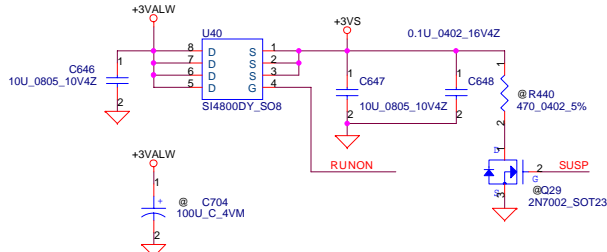
### +5VALW to +5V Transfer



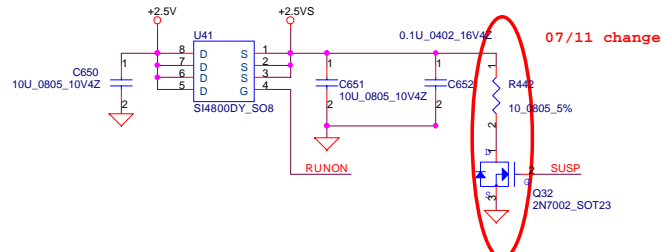
### +5VALW to +5VS Transfer



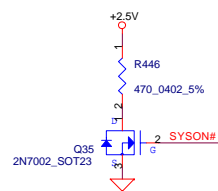
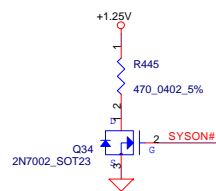
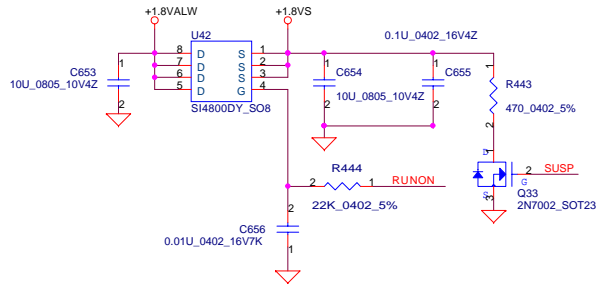
### +3VALW to +3VS Transfer



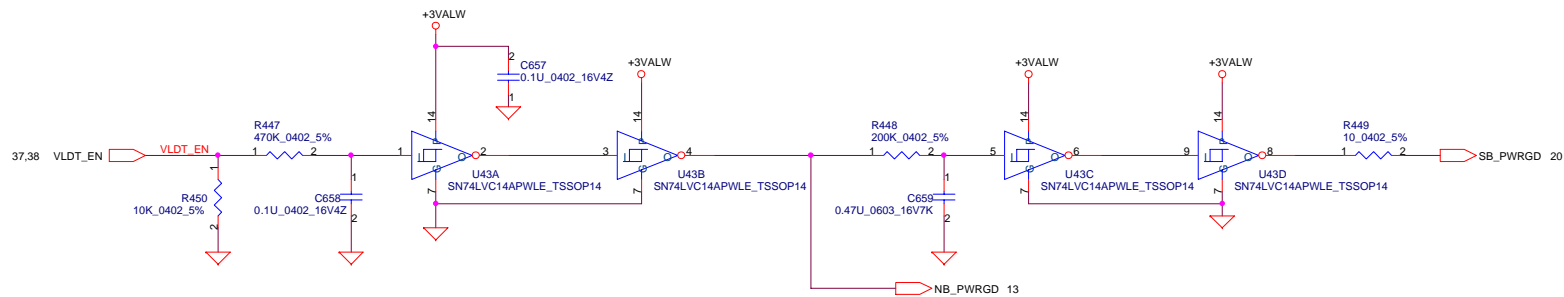
### +2.5V to +2.5VS Transfer



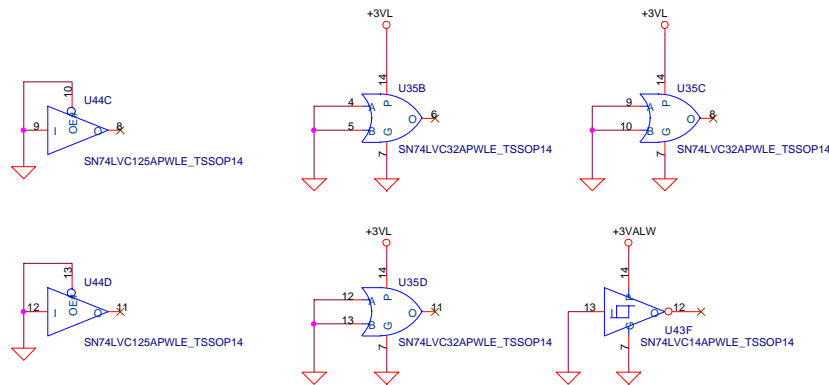
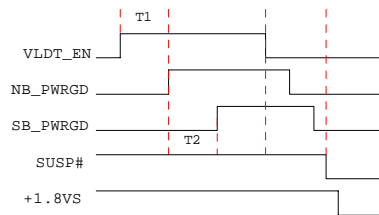
### +1.8VALW to +1.8VS Transfer



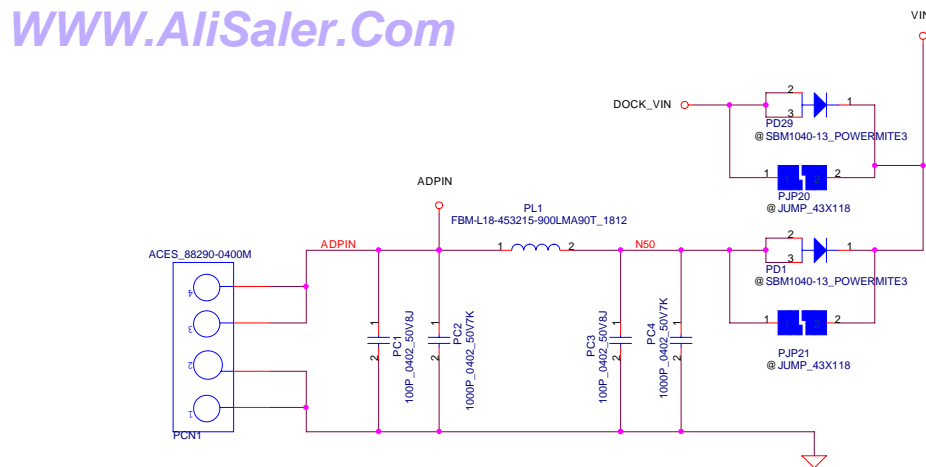
Security Classification		Compal Secret Data					
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				DC/DC Interface & Hole			
Size		Document Number		LA-2771		Rev	
Custom						0.8	
				Date: Tuesday, August 30, 2005			
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note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,  
SUSP# goes to low after SB\_PWRGD goes to low for power  
down.



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				Custom	LA-2771
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				Rev	0.8

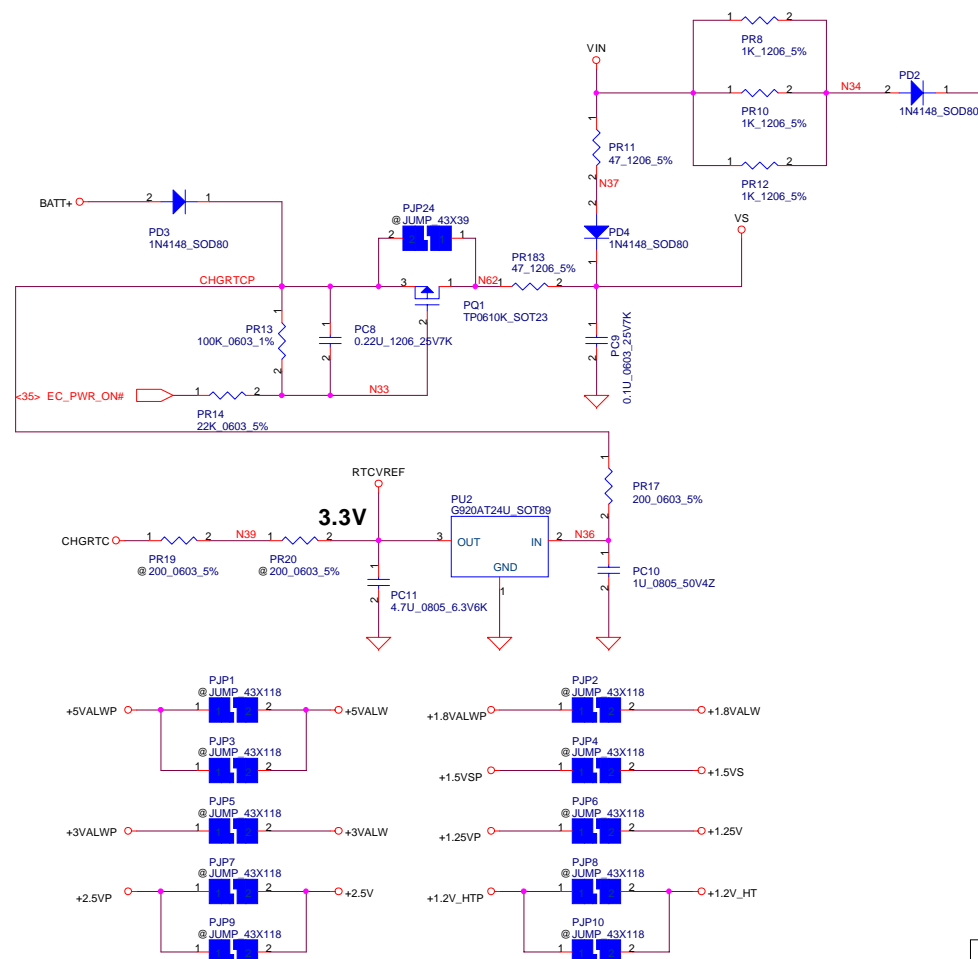


Vin Detector : Cayenne		
18.234	17.841	17.449
17.597	17.210	16.813

Vin Detector : Boxster		
14.352	13.950	13.555
13.818	13.411	13.000

8/29 Change to 0.022uF for AC Off issue

Cayenne : PR5=22K; PR6=19.6K
Boxster : PR5=47K; PR6=27K



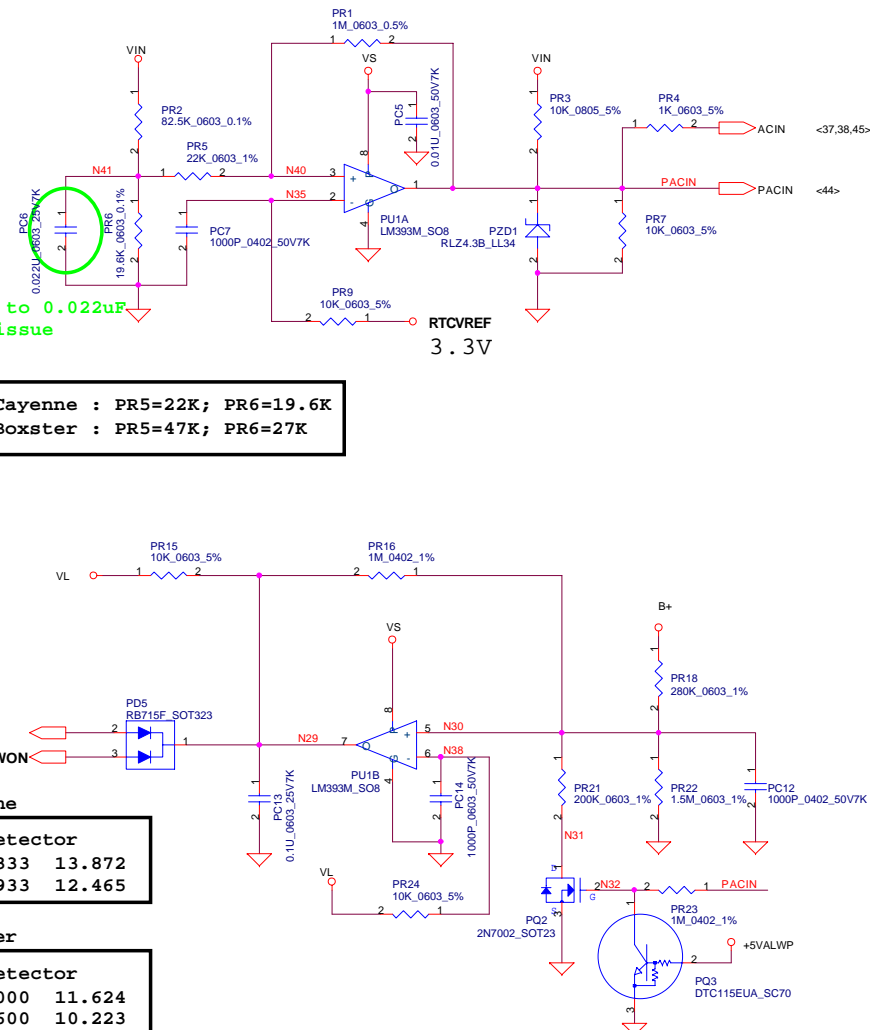
Cayenne : PR5=22K; PR6=19.6K
Boxster : PR5=47K; PR6=27K

ACIN : Cayenne		
Precharge detector		
14.805	14.333	13.872
13.355	12.933	12.465

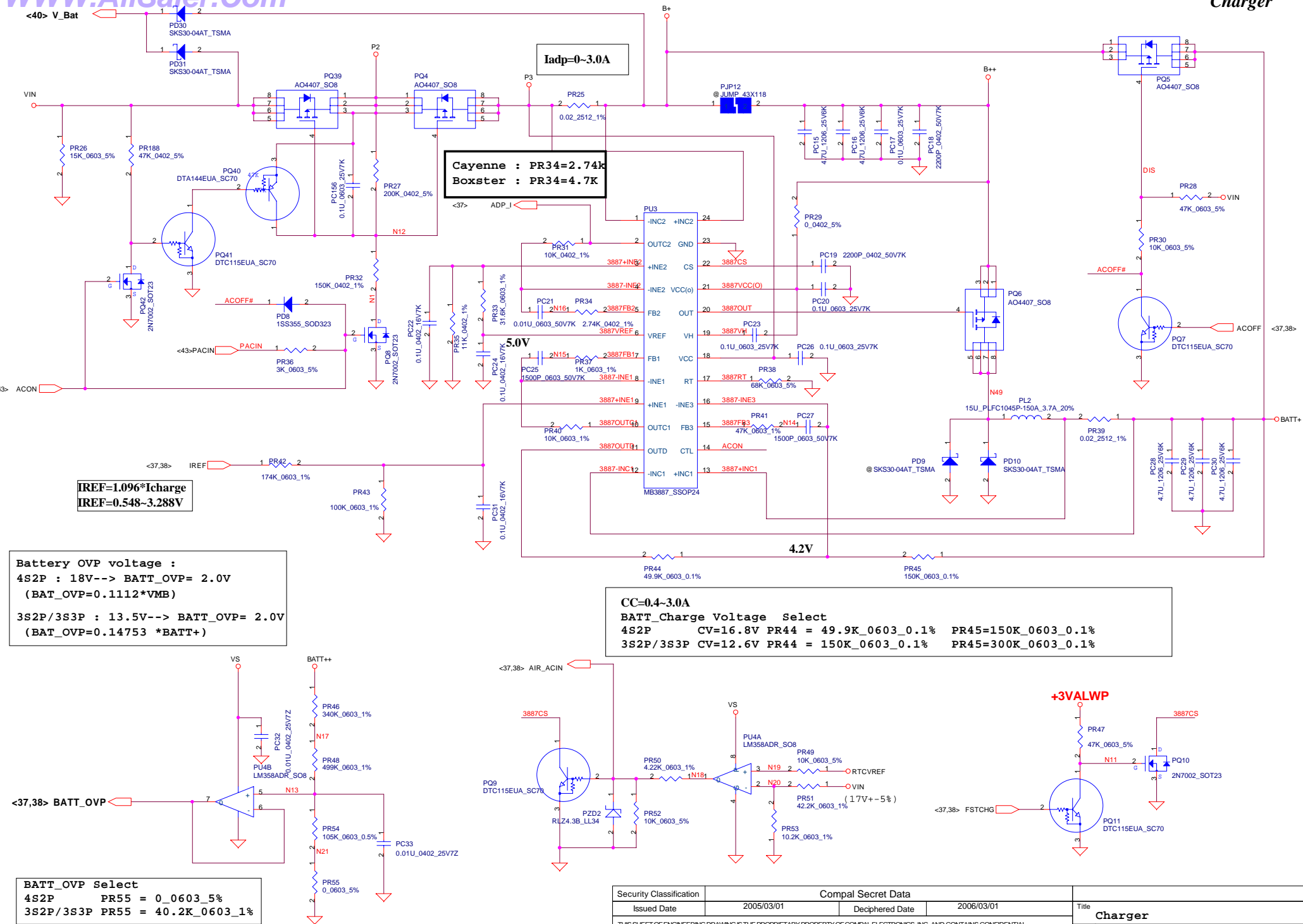
ACIN : Boxster		
Precharge detector		
12.384	12.000	11.624
10.927	10.600	10.223

BATT		
Detector		
7.558	7.333	7.112
6.108	5.933	5.704

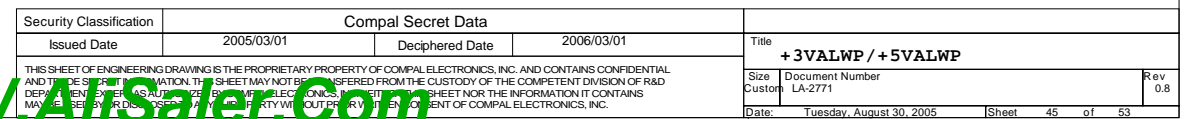
Cayenne : PR21=200K
Boxster : PR21=300K



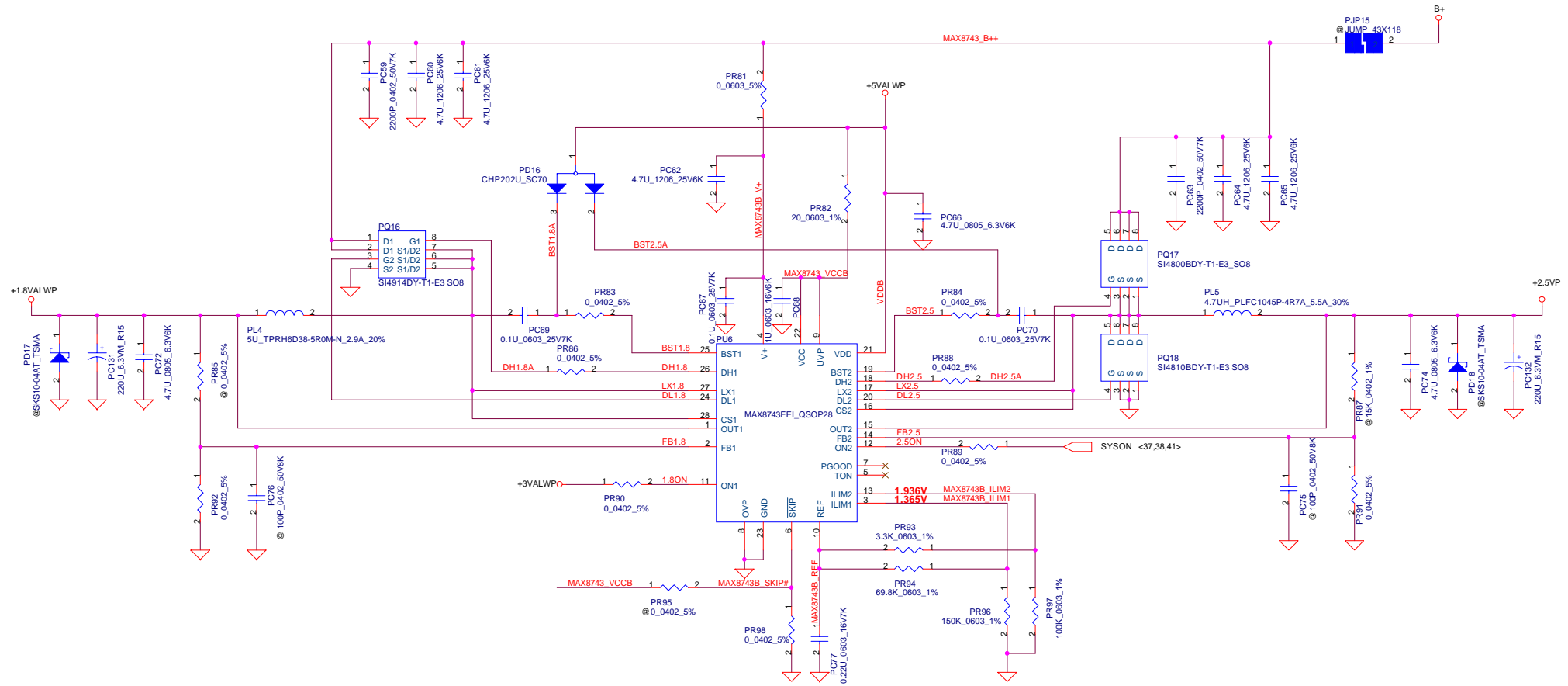
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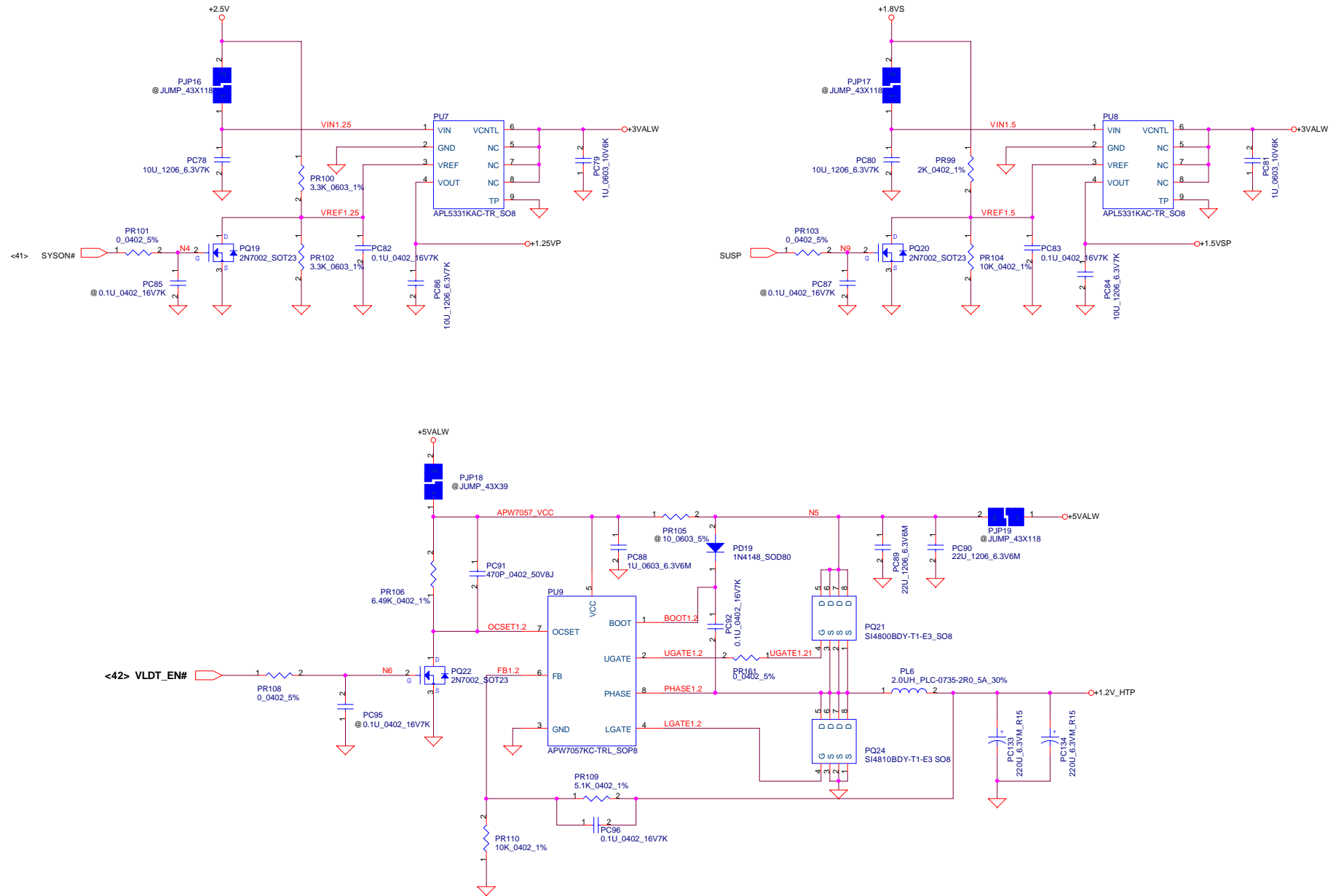
Security Classification				Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Size	Document Number	Rev	
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+1.8VALWP/+2.5VP

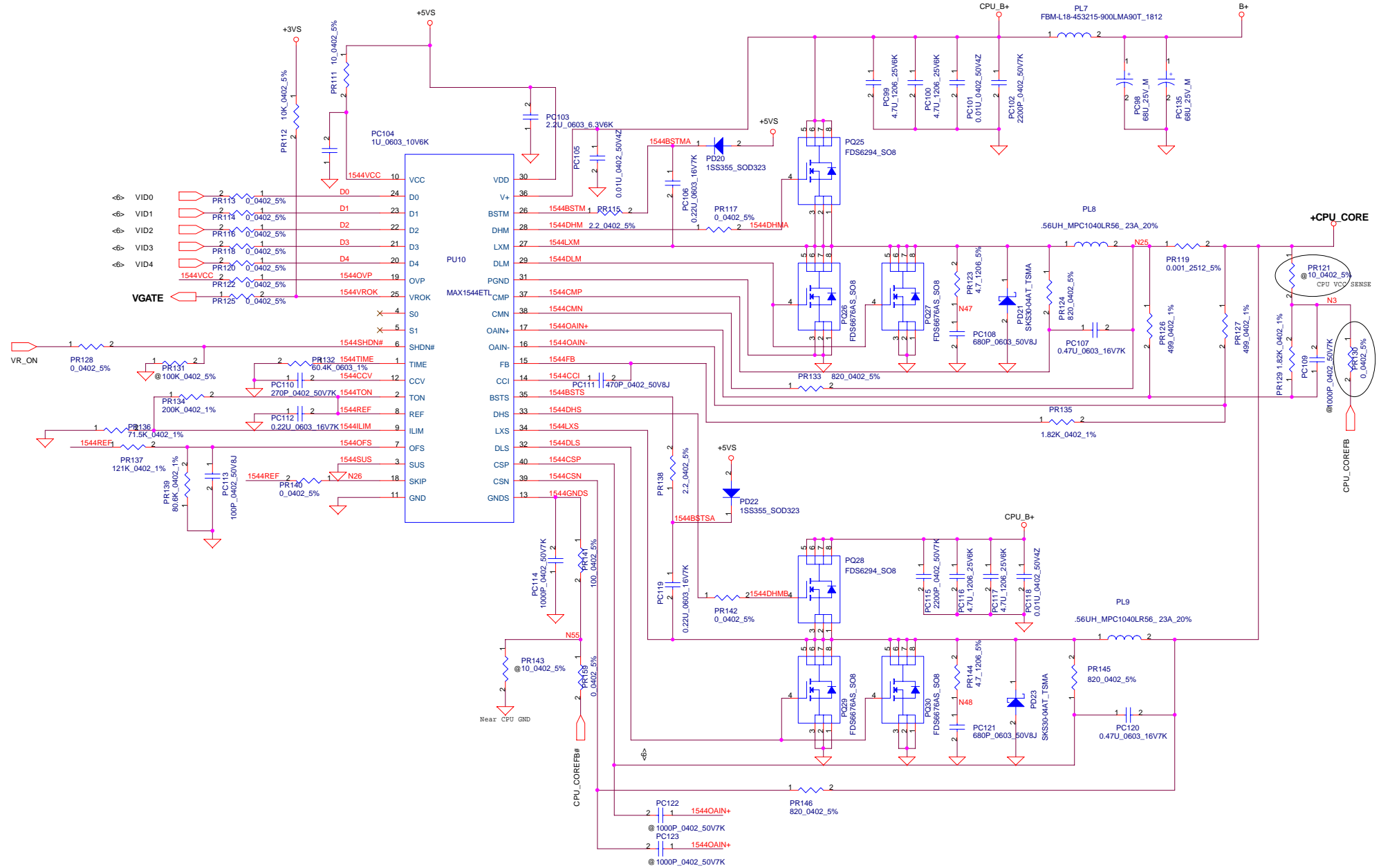


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Issued Date	2005/03/01	Deciphered Date	2006/03/01	+1.8VALWP/+2.5VP
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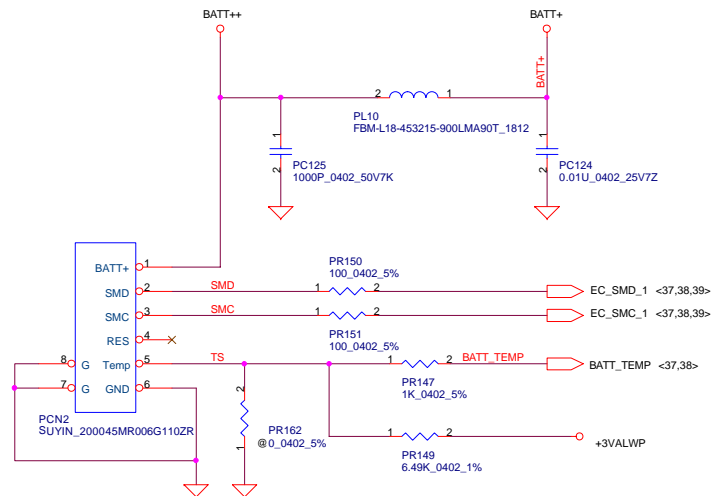
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				+CPU_CORE					
				Size		Document Number		Rev	
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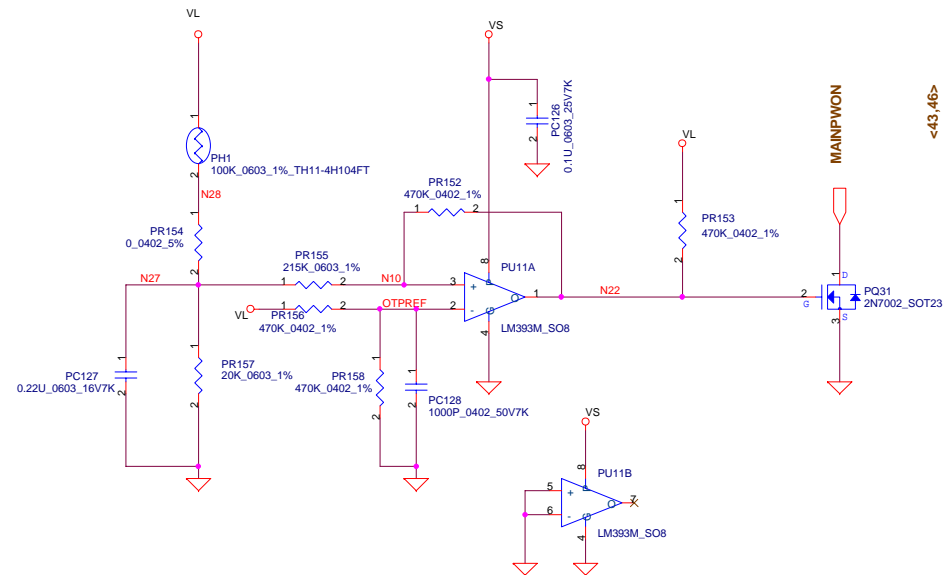
# Battery Connect/OTP



**PJPB1 battery connector**  
**SMART**  
**Battery:**  
**1.BATT+**  
**2.SMBD**  
**3.SMBC**  
**4.Res**  
**5.Temp**  
**6.GND**

CPU

**PH1 under CPU botten side :**  
 CPU thermal protection at 90 +-3 degree C  
 Recovery at 50 +-3 degree C



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Item	Reason for change	PG#	Modify List	Date	B.Ver#
1	Add the functionality to turn on the system on from Off and S4 with the consumer IR.	45	Change 3/5VALWP regulator from MAX1902 to MAX1999	2005.04.08	
2	Change PCN1 from SP020022200 to SP020024800.	49	Change PCN1 from SP02000AO00 to DC040001P00.	2005.04.08	
3	Because EMI test fail	48	Change CPU_CORE HI-SIDE MOS from AO4408 to FDS6294, LOW-SIDE from AO4410 to FDS6676AS	2005.05.18	
4	Because V_bat to Calgary havn a leakage current, cause precharge can't finish.	44	Add PD30 and PD31 to supply the V_bat power.	2005.06.09	
5	Add air-adapter detector	44	Add PU4 to detector air-adapter in.	2005.07.02	
6	Adjust the MB3887 CC to CP response cause the adapter OCP.	44	Change the PR31 from 100k_0402_1% to 10k_0402_1% Change the PR34 from 10k_0402_1% to 2.74k_0402_1% Change the PC21 from 4700p_0603_50V to 0.01u_0603_50v	2005.07.29	

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Compal Electronics, Inc.		
Title		
PWR PIR		
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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2005.06.27>	1	For clear H_RST# glitch	41	Add Q61	0.5
<2005.07.04>	1	For +1.8VS EMI	11	Change R61, R84 value from 0 ohm to 120 ohm	0.5
	2	For +1.2V_HT power ripple	14	Change C197, C209, C254, C248, C251, C256, C258 value from 0.1U 16V4Z 0402 to 1U 6.3V4Z 0402	0.5
	3	For +2.5VS EMI	15	Add C737, C738, C741, C742 220P 50V8J 0402	0.5
	4	For +2.5VS EMI	15	Add C739, C740, C743, C744 1000P 50V7K 0402	0.5
	5	For Mini-PCI_CLK EMI	30	Mount R325 and C512	
	6	For CardBus chip PCI_CLK EMI	25	mount R279 and C442	0.5
	7	For LAN chip PCI_CLK EMI	29	Mount R322 and C504	0.5
	8	For EC K/B chip PCI_CLK EMI	30	Mount R415 and C628	
<2005.07.05>	1	For USB EMI	34	Add L33, L34	
	2	For USB EMI	34	change R561,R559,R562,R560 size from 0603 to 0402	
<2005.07.07>	1	For dock Docking audio noise	31	Add Q58, R589, Q60, R590, Q59, R589	
	2	For Dock_LOUTR/L EMI	40	Add R591, C745, R592, C746	
	3	For Docking TV_out signals EMI	40	Add R593, C747, R594, C748,C749, C750, R595, C751, C752	
<2005.07.11>	1	For accelerate +2.5VS discharge speed	40	change R442 size and value from 470_0402 to 10_0805	
	2	For LAN lamp	29	Swap Activity and Link Lamp	
<2005.07.25>	1	For SanDisk SD 256M card could not work issue	25	delete U48 Quick switch reserve schematics	
	2	For SanDisk SD 256M card could not work issue	25	Delete R463, R465, R466, R476, R268	
	3	For SanDisk SD 256M card could not work issue	26	Delete R270, R267, R547, R548	
	4	For SanDisk SD 256M card could not work issue	26	Mount R550 and R549	
<2005.07.28>	1	For lower power consumption	38	Add and un-mount R596	
	2	For CRT Assy	18	change CRT footprint	

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<2005.08.11>

<2005.08.23>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Delect all reserve 0 ohm resistors.	41	Delete R24, R125, R21 , R73 , R263, R565	0.5
2		For EMI solution on switch connector	11	Add C753~C771 total 19 pcs	0.5
3		For ATI suggestion on RS480	14	Change C200, C202, C242, C232 from 0.1U 16V4Z 0402 to 1U 6.3V4K 0402	0.5
4		Relocate damping resistor to solve Sandisk issue	26	Relocate R266, R458, R459, R460, R461, R462	0.8
5		Change from AGND to DGND for Codec precision improvement	31	Change Q16/Q17 pin3 and R334 pin2 to DGND	0.8
6		Add +3VALW power rail for Boxster lid switch use	35	Add +3VALW to JP28 pin25	0.8
7		Reserve C700, for soft start if necessary	31	Reserve C700	0.8
8		Reserve R600 M_SEN#, currently this signal isn't used	38	Reserve R600	0.8
1					
2					
1					
2					
3					
1					
2					
1					
2					
3					
4					
1					
2					

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