R63 INTEL SYSTEM DIAGRAM

01

+3V/+5V S5 PG.36

+1.05V PG.37

CPU Core PG.40~41

DDR3L PG.38

Charge PG.35

Dis-Charge PG.39

+VGACORE PG.42

+1.5 VGA PG.43

+1.0V/+1.8/ +3 VGA PG.44

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A

SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

INTEL Haswell
Processor : Daul / Quad Core
Power : 37 / 47 (Watt)
Package : rPGA947
Size : 37.5 x 37.5 (mm)
PG.2~5

PCI-E x8 — AMD Mars / SUN XT 29mm X 29mm TDP 35W / 25W PG.14~20

eDP (5.4Gb/s)

DDI (5.4Gb/s)

DDR3 900MHz — VRAM 128Mx16x8,128bit PG.21~22

FDI DMI

HDD PG.33 — SATA0

ODD PG.33 — SATA1

INTEL PCH
Lynx Point
Power : 3.5 Watt
Package : FCBGA695
Size : 20 x 20 (mm)
PG.6~11

eDP — RTD 2136 S/R DP to LVDS Converter PAGE 23 — LVDS Interface — LVDS PG.25

DP Port B — HDMI PG.26

CRT — CRT PG.25

PCI-E x 1 — LANE2 / LANE1

LAN RTL8166EH 10/100 PG.30

WLAN BT COMBO PG.34 — USB 2.0 PORT10

PCI-E x 1 — LANE3

Accelerometer PG.34 — SMBUS

Card Reader RTS5237 PG.27

KBC EnE KB3940QF A1 PG.31 — LPC

KB PG.32 | TP PG.32 | ROM PG.31 | FAN PG.32

USB 3.0 — USB3.0 Ports X2 PG.29 | Webcam PG.25

USB 2.0 — PORT1,2 / PORT4 / PORT0,1

USB2.0 Ports PG.29

AUDIO CODEC ALC 3227 PG.28

Speaker PG.28

HP/MIC PG.29

Analog MIC PG.29

Stackup

TOP
GND
IN1
IN2
VCC
BOT

for HP

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Friday, December 21, 2012 Sheet 1 of 44

Haswell Processor (DMI,PEG,FDI)

Haswell Processor (CLK,MISC,JTAG)

02

U24A

DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 → DMI_RX#[0..3]
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 → DMI_RX[0..3]
DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 → DMI_TX#[0..3]
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 → DMI_TX[0..3]

DMI

FDI_TXN0 FDI_TXN1 FDI_TXP0 FDI_TXP1 → FDI_TX#[0..1], FDI_TX[0..1]
FDI_INT → FDI_INT
FDI_CSYNC (R71 *0_4/S FDI_CSYNC_R) → FDI_CSYNC

FDI

IN_D2# IN_D1# IN_D0# IN_CLK# IN_D2 IN_D1 IN_D0 IN_CLK
DPB_LANE0_N DPB_LANE1_N DPB_LANE2_N DPB_LANE3_N DPB_LANE0_P DPB_LANE1_P DPB_LANE2_P DPB_LANE3_P
→ DDIB_TX#[0..3], DDIB_TX[0..3]

DDIC_TX#[0..3], DDIC_TX[0..3]
DDID_TX#[0..3], DDID_TX[0..3]

Intel(R) DDI

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

eDP_RCOMP (R59 *0_4 INT_eDP_HPD_Q) EDP_DISP_UTIL → eDP_RCOMP, eDP_DISP_UTIL, eDP_HPD
EDP_AUXP EDP_AUXN → eDP_AUX, eDP_AUX#
EDP_TXP0 EDP_TXP1 → eDP_TX[0..1]
EDP_TXN0 EDP_TXN1 → eDP_TX[0..1]#

eDP

PCI EXPRESS* - GRAPHICS

PEG_COMP (E23) PEG_RCOMPO
PEG_RX#[0..15] → M29 K28 M31 L30 M33 L32 M35 L34 E29 D28 E31 D30 E35 D34 E33 E32
PEG_RX[0..15] → L29 L28 L31 K30 L33 K32 L35 K34 F29 E28 F31 E30 F35 E34 F33 D32
PEG_TX#[0..15] → H35 H34 J33 H32 J31 G30 C33 B32 B31 A30 B29 A28 B27 A26 B25 A24
PEG_TX[0..15] → J35 G34 H33 G32 H31 H30 B33 A32 C31 B30 C29 B28 C27 B26 C25 B24

HSW_RPGA_EDS_PGA

PEG_RX#[0..7] 14
PEG_RX[0..7] 14

H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

TP50 SKTOCC# → AP32 SKTOCC#
TP46 TP_CATERR# → AN32 CATERR#

HPECI Ra,Ca need placement close to EC.
9,31 EC_PECI — R537 43_4 — H_PECI
Ra
Ca C770 *47P/50V_4
4/30 CRB 1.0 Add
+VCCST
AR27 PECI
AK31 FC_AK31

PROCHOT# (50ohm)
Trace Length <11 inches
31,40 H_PROCHOT# — R263 56.2/F_4 — H_PROCHOT#_R → AM30 PROCHOT#
C38 Cb
Cb need placment near VR
47P/50V_4

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
9,31 PM_THRMTRIP#R — PM_THRMTRIP#_R → AM35 THERMTRIP#

Rb need placment near PCH
4/30 CRB 1.0 Add
+1.05V — R354 *100/F_4 — Rb

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
6 PM_SYNC — R533 *0_4/S — PM_SYNC_R → AT28 PM_SYNC
C729 *0.1U/10V_4

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
9 H_PWRGOOD — R502 *0_4/S — H_PWRGOOD_R → AL34 UNCOREPWRGOOD
R503 10K_4

PM_DRAM_PWRGD_R → AC10 SM_DRAMPWROK

CPU RESET#
8,14,27,30,31,34 PLTRST# — R531 *1.5K/F_4 — R532 *750/F_4 → AT26 RESET#
9,31 CPU_PLTRST#R
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
7/26: DB phase modify

HSW_RPGA_EDS_PGA

U24B

MISC
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
THERMAL
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
PWR MANAGEMENT

CLOCKS
BCLK BCLK# → CLK_CPU_BCLKP CLK_CPU_BCLKN
SSC_DPLL_REF_CLK SSC_DPLL_REF_CLK# → CLK_DPLL_SSCLKP CLK_DPLL_SSCLKN
DPLL_REF_CLK DPLL_REF_CLK# → CLK_DPLL_NSCCLKP CLK_DPLL_NSCCLKN

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

DDR3 MISC
SM_DRAMRST# → AN3 CPU_DRAMRST#
SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] → AP3 AR3 AP2 SM_RCOMP_0 SM_RCOMP_1 SM_RCOMP_2
R250 100/F_4
R526 75/F_4
R525 100/F_4

SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,

JTAG & BPM
PRDY# PREQ# → AR29 XDP_PRDY# AT29 XDP_PREQ# — TP100 TP57 CPU XDP
TCK TMS TRST# → AM34 XDP_TCLK AN33 XDP_TMS AM33 XDP_TRST# — TP42 TP41 TP94
TDI TDO → AM31 XDP_TDI_R AL33 XDP_TDO — TP36 TP39
DBR# → AP33 XDP_DBRST# — R524 *1K_4 +3V — XDP_DBRST# 6
BPM#[0..7] → AR30 AN31 AN29 AP31 AP30 AN28 AP29 AP28 XDP_BPM0..XDP_BPM7 — TP101 TP53 TP59 TP99 TP95 TP56 TP97 TP58

HSW_RPGA_EDS_PGA

SM_DRAMPWROK Processor Input.

To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

+3VS5
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
C44 0.1U/10V_4
+1.35V_CPU
R80 1.8K/F_4
DG 498556 -> 1.8K

10/22: SI modify
R75 100K_4 R66 100K_4
U2
38 51216PG — R65 *0_4/S
4PM_DRAM_PWRGD_C
R78 0_4 PM_DRAM_PWRGD_R
10/12: SI modify
74AHC1G09GW
C929 0.047U/10V_4
D15 *MEK500V-40
10/15: SI Del
R79 3.3K_4
C930 *0.047U/10V_4
DG 498556 -> 3.3K

PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches

DDR3 DRAM RESET

DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches
+1.35VSUS — R471 *1K_4 — R785 *0_4/S
12,13 DDR3_DRAMRST# — R472 *0_4/S — CPU_DRAMRST#
10/18: SI modify
CPU_DRAMRST#_R
Q29 *ME2N7002E
8 DRAMRST_CNTRL_PCH — *0_4 R468
31 DRAMRST_CNTRL_EC — *0_4 R467 — C628 *0.047U/10V_4
8,12,13 DRAMRST_CNTRL_DDR — R464 *4.99K/F_4
FOR DS3
0529 remove R825 pull hi due to EC is output pin

+VCCIO_OUT 4,40
+VCCIOA_OUT 4
+1.05V 4,9,10,11,31,34,37
+1.35V_CPU 3,4,12,13,38
+1.35VSUS 3,4,12,13,38
+3VS5 6,7,9,10,34,36,38,39,42,44
+3V 6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44

4/30 CRB V1.0 -> 10K

+VCCIO_OUT — R218 10K_4
INT_eDP_HPD_Q — Q12 ME2N7002E — EDP_HPD 24,25
R219 100K_4

PEG x8 disable (UMA only remove)

14 PEG_TX[0..7]

C_PEG_TX0	C688	0.22U/10V_4	PEG_TX0
C_PEG_TX1	C705	0.22U/10V_4	PEG_TX1
C_PEG_TX2	C698	0.22U/10V_4	PEG_TX2
C_PEG_TX3	C708	0.22U/10V_4	PEG_TX3
C_PEG_TX4	C699	0.22U/10V_4	PEG_TX4
C_PEG_TX5	C690	0.22U/10V_4	PEG_TX5
C_PEG_TX6	C715	0.22U/10V_4	PEG_TX6
C_PEG_TX7	C730	0.22U/10V_4	PEG_TX7

0.22uF AC coupling Caps for PCIE GEN1/2/3

14 PEG_TX#[0..7]

C_PEG_TX#0	C697	0.22U/10V_4	PEG_TX#0
C_PEG_TX#1	C707	0.22U/10V_4	PEG_TX#1
C_PEG_TX#2	C703	0.22U/10V_4	PEG_TX#2
C_PEG_TX#3	C714	0.22U/10V_4	PEG_TX#3
C_PEG_TX#4	C704	0.22U/10V_4	PEG_TX#4
C_PEG_TX#5	C700	0.22U/10V_4	PEG_TX#5
C_PEG_TX#6	C716	0.22U/10V_4	PEG_TX#6
C_PEG_TX#7	C733	0.22U/10V_4	PEG_TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

+VCCIOA_OUT — R138 24.9/F_4 — eDP_RCOMP

eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

+VCCIOA_OUT — R132 24.9/F_4 — PEG_COMP

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Processor pull-up (CPU)

H_PROCHOT# R257 62_4 +VCCIO_OUT
CLK_DPLL_SSCLKP R128 *10K_4
CLK_DPLL_SSCLKN R129 *10K_4

XDP_TDO R234 51_4
XDP_TMS R239 *51_4
XDP_TDI_R R226 *51_4
XDP_PREQ# R269 *51_4 +1.05V
XDP_TCLK R246 51_4
XDP_TRST# R519 51_4
check

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

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Haswell Processor (DDR3)

03

U24C

DDR SYSTEM MEMORY A

U24D

DDR SYSTEM MEMORY B

for HP

RSVD_V10 must be grounded

RSVD_R10 must be grounded

HSW_RPGA_EDS_PGA

HSW_RPGA_EDS_PGA

CPU SM_VREF

8/31: Intel suggestion

+SM_VREF R260 *0_6/S R285 *0_6/S R282 *1K_4 Q16 *ME2N7002E +VREF_CA_CPU

DRAMRST_CNTRL DRAMRST_CNTRL_DDR 2,12,13

+1.35V_CPU R278 *1K/F_4 R283 *0_6 +SM_VREF R261 *0_6 C400 *0.1U/10V_4 R279 *1K/F_4 Q17 *ME2N7002E DDR_VTTREF 12,38 MAIND MAIND 10,39

+1.35V_CPU 2,4,12,13,38

+VREF_CA_CPU 12

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

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Haswell Processor (POWER)

04

POWER

U24F

+VCCIN 95A

+VCC_CORE

+1.35V_CPU 4.2A

+1.35V_CPU

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

HSW_RPGA_EDS_PGA

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

+VCCIOA_OUT 2
+VCCIO_OUT 2,40
+VCCIO_PCH 10
+1.5V 6,7,8,10,28,34,38,44
+1.35V_CPU 2,3,12,13,38
+1.05V 2,9,10,11,31,34,37
+VCC_CORE 40,41
+VCCST 2
+1.35VSUS 2,3,12,13,38

IO Thrm Protect

+3VPCU

For 65 degree, 1.8v limit, (SW)

R774 16.5K/F_4

THRM_MOINTOR 31

C62 0.1U/10V_4

R775 3.3K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 31

R776 100K_4 NTC

C54 0.1U/10V_4

4/30: CRB 1.0 add

+1.05V R256 *0_8 +VCCST

C392 *22U/6.3VS_8

C381 *22U/6.3VS_8

Power Test Propose

+1.05V R60 150/F_4 PWR_DEBUG_R R62 *10K_4

+1.05V R510 *0_8 +VCCIO_OUT C753 10U/6.3V_6

+1.05V R462 0_6 +VCCIO_PCH

CRB 1.0 stuff C631 *4.7U/6.3V_6

4/30: DG 498550

Haswell PWR_DEBUG requires a 150-Ohm pull-up resistor to PCH 1.05-V VCC Core when routed to XDP

VCCIO_OUT AN35 +VCCIO_OUT_R *0_1206/S R513 +VCCIO_OUT 300mA

VCCIO2PCH A23 +VCCIO_PCH_R *0/F_1206 R466 +VCCIO_PCH 300mA

VCOMP_OUT F22 +VCCIOA_OUT_R *0_1206/S R87 +VCCIOA_OUT

VSS_AP35 AP35

VIDALERT# AM28 H_CPU_SVIDALRT#
VIDSCLK AM29 H_CPU_SVIDCLK
VIDSOUT AL28 H_CPU_SVIDDAT

PWR_DEBUG H27 PWR_DEBUG_R 0_4 R61 TP1

0_4 R518

VCC_SENSE AL35 R223 100_4 +VCC_CORE

VSS_SENSE AK35 VCC_SENSE 40

VSS_SENSE 40 R222 100_4

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

SVID CLK

H_CPU_SVIDCLK VR_SVID_CLK 40

7/26: DB sch modify, Del R23

SVID DATA

+VCCIO_OUT

Place PU resistor close to CPU

R253 130/F_4

Place PU resistor close to VR

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

H_CPU_SVIDDAT VR_SVID_DATA 40

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

SVID ALERT

C337 0.1U/10V_4

+VCCIO_OUT R247 75/F_4

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

H_CPU_SVIDALRT# R248 43_4 VR_SVID_ALERT# 40

CPU VDDQ

+1.35V_CPU +1.35VSUS

Placement close to CPU.

C235 0.1U/10V_4

C225 *0.1U/10V_4

Note: please keep plane is enough for VDDQ 4.2A

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

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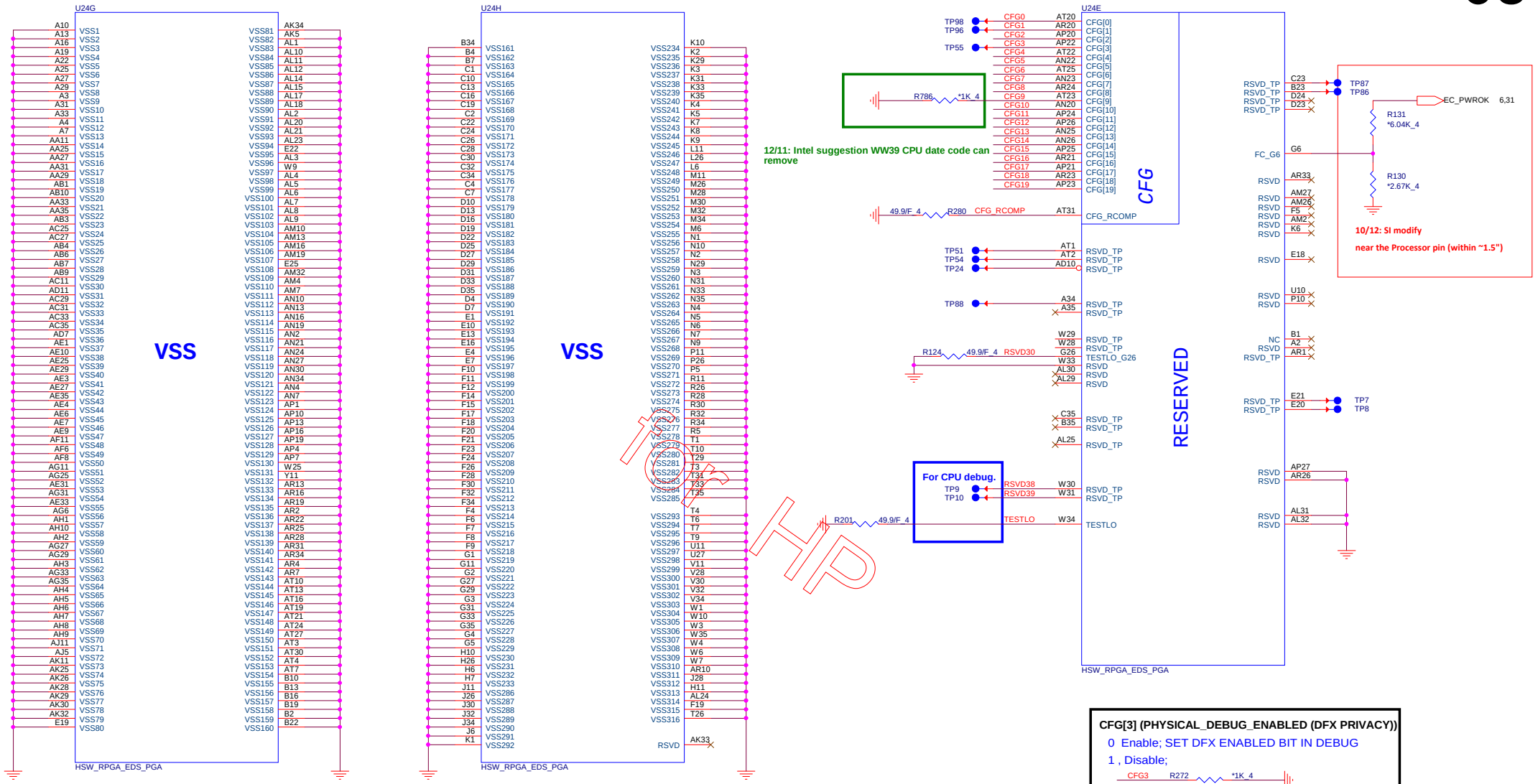
Haswell Processor (GND)

Haswell Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG3 R272 *1K_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG2 R275 *1K_4
CFG4 R271 1K_4
CFG7 R273 *1K_4
CFG5 R274 1K_4
CFG6 R270 *1K_4

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

Date: Friday, December 21, 2012 Sheet 5 of 44

Lynx Point (DMI,FDI,PM)

Lynx Point (DDI)

06

U33C

U33D

DMI

FDI

System Power Management

LVDS

CRT

Digital Display Interface

INT. HDMI

5/16 for DS3

12/17 PV modify

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance.

DG V0.7 -> 33 ohm
SCH V0.7 -> 0 ohm

DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS

Reserve from EMI request

Reserve for power on sequence

LPT_PCH_M_EDS/BGA

PCH Pull-high/low(CLG)

10/14: SI phase modify

10/12: SI phase modify

INT HDMI Detect Function

System PWR_OK(CLG)

7/26 DB Modify

10/17: SI Modify change to 10 Kohm

7/26 DB Modify

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PROJECT : R63
Quanta Computer Inc.

NB5

Size: Custom | Document Number: PCH 1/6 (DMI/FDI/VIDEO) | Rev: 1A

Date: Monday, December 24, 2012 | Sheet 6 of 44

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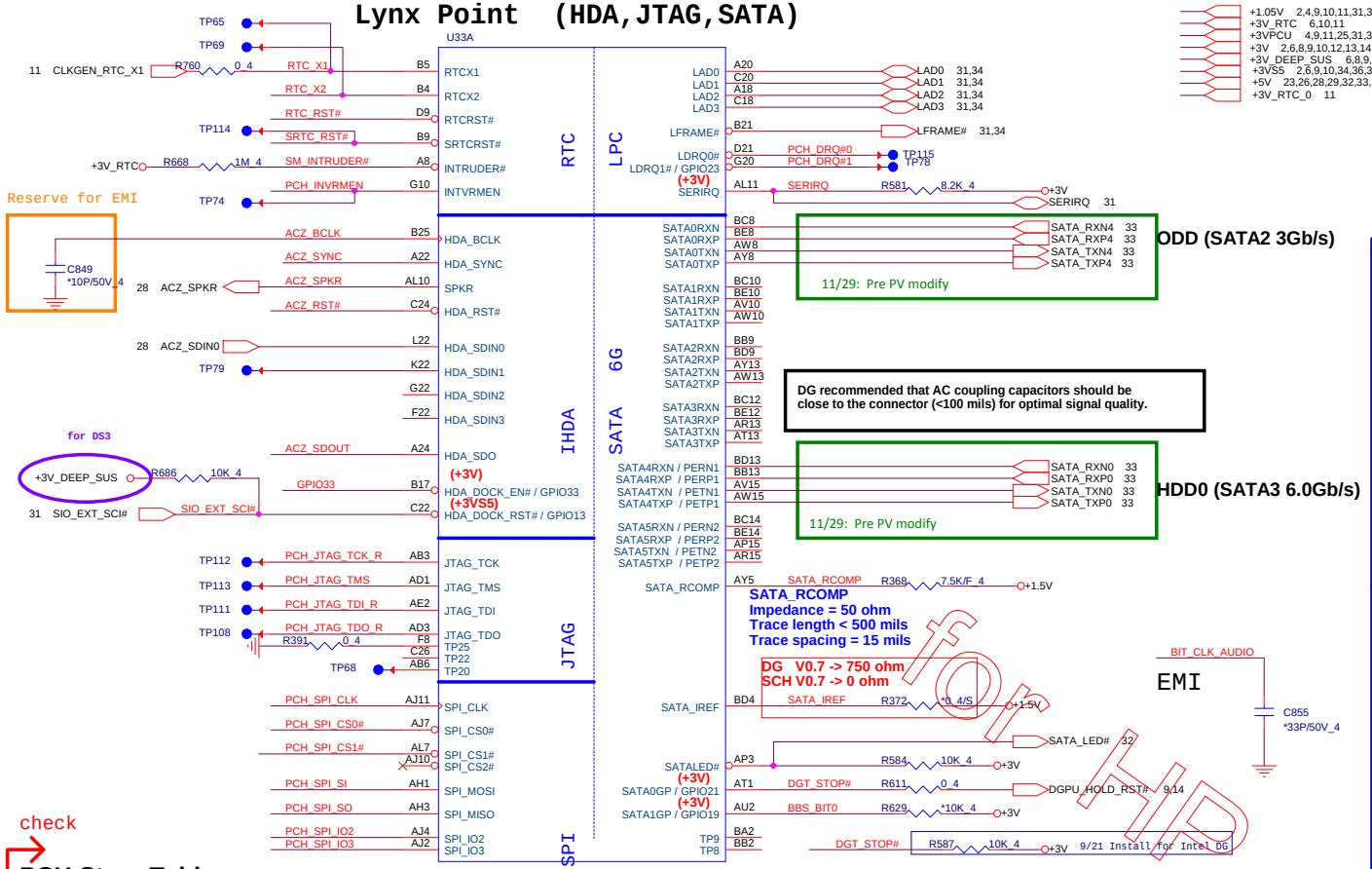
Lynx Point (HDA,JTAG,SATA)



check

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R569 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R563 *1K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R389 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R680 *0_4 +3V 10/18: SI Modify [Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0; GNT0# 1 0; Boot Location SPI LPC	R613 *1K_4 BBS_BIT0 R390 *1K_4 BBS_BIT1 8
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R684 *1K_4 ACZ_SYNC 12/13: PV modify
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	31 GPIO33_E ACZ_SDOUT R693 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R621 *1K_4 BT_OFF# 9,34
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R571 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R374 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	R564 *1K_4 PCH_SUSCLK 6,31

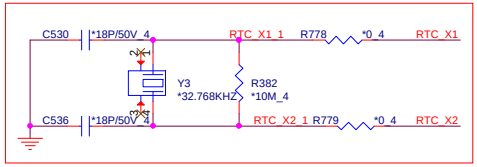
LPT_PCH_M_EDS/BGA

+1.05V 2,4,9,10,11,31,34,37
+3V_RTC 6,10,11
+3VPCU 4,9,11,25,31,32,34,35,36
+3V 2,6,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+3V_DEEP_SUS 6,8,9,10,39
+3VS5 2,5,9,10,34,36,38,39,42,44
+5V 23,26,28,29,32,33,34,39
+3V_RTC_0 11

10/18: SI Modify

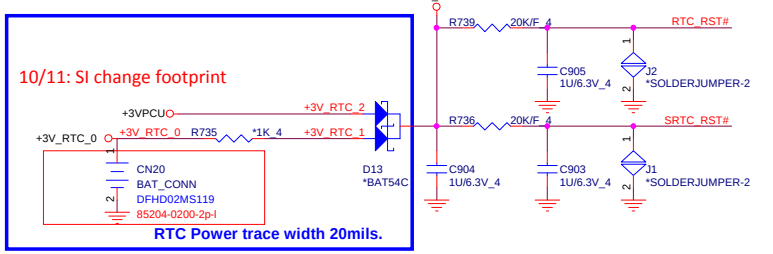
RTC Clock 32.768KHz

07

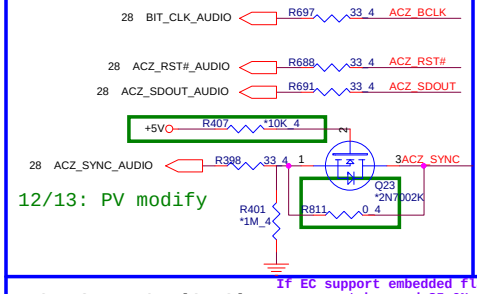


RTC Circuitry(RTC)

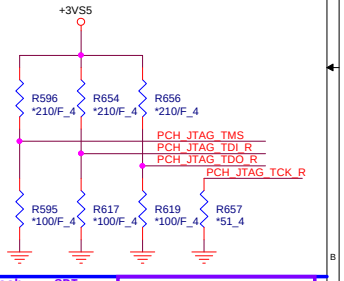
30mils



HDA Bus(CLG)

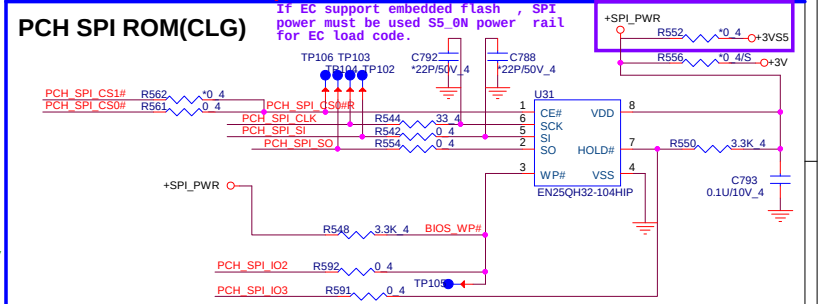


PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

If EC support embedded flash , SPI power must be used S5_ON power rail for EC load code.



10/18: Del R350 , R344

Vender	Size	P/N
EON	4MB	AKE39ZN0Q03 EON EN25QH32-104HIP
AMIC	4MB	AKE39ZN0800 AMIC A25QE32M-F (QE)
Socket		DFHS08FS023

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)

7/26 DB modify

PEG Clock detect (SG only)

7/26 DB modify

SMBus/Pull-up(CLG)

12/18 PV modify

CLK_REQ/Strap Pin(CLG)

PCIE Clock

SMBus/Pull-up(CLG)

check

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

USB2.0

USB2.0/USB3.0 COMBO 1st

USB2.0/USB3.0 COMBO 2nd

Webcam

Touch screen

12/11: PV modify

Right_USB

WLAN

USB3.0

WLAN

LAN

Cardreader

SMBUS

PCI-E*

CLOCKS

FLEX CLOCKS

RF

10/12: SI modify

10/18: SI modify

change 25M to small size

GPU

Remove for UMA only.

CLOCK TERMINATION for FCIM

for DS3

4/30: CRB 1.0 =>rename PCH_TP26

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PROJECT :	R63
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Size: Custom	Document Number: PCH 3/6 (PCIE/USB/CLK)
Rev: 1A	
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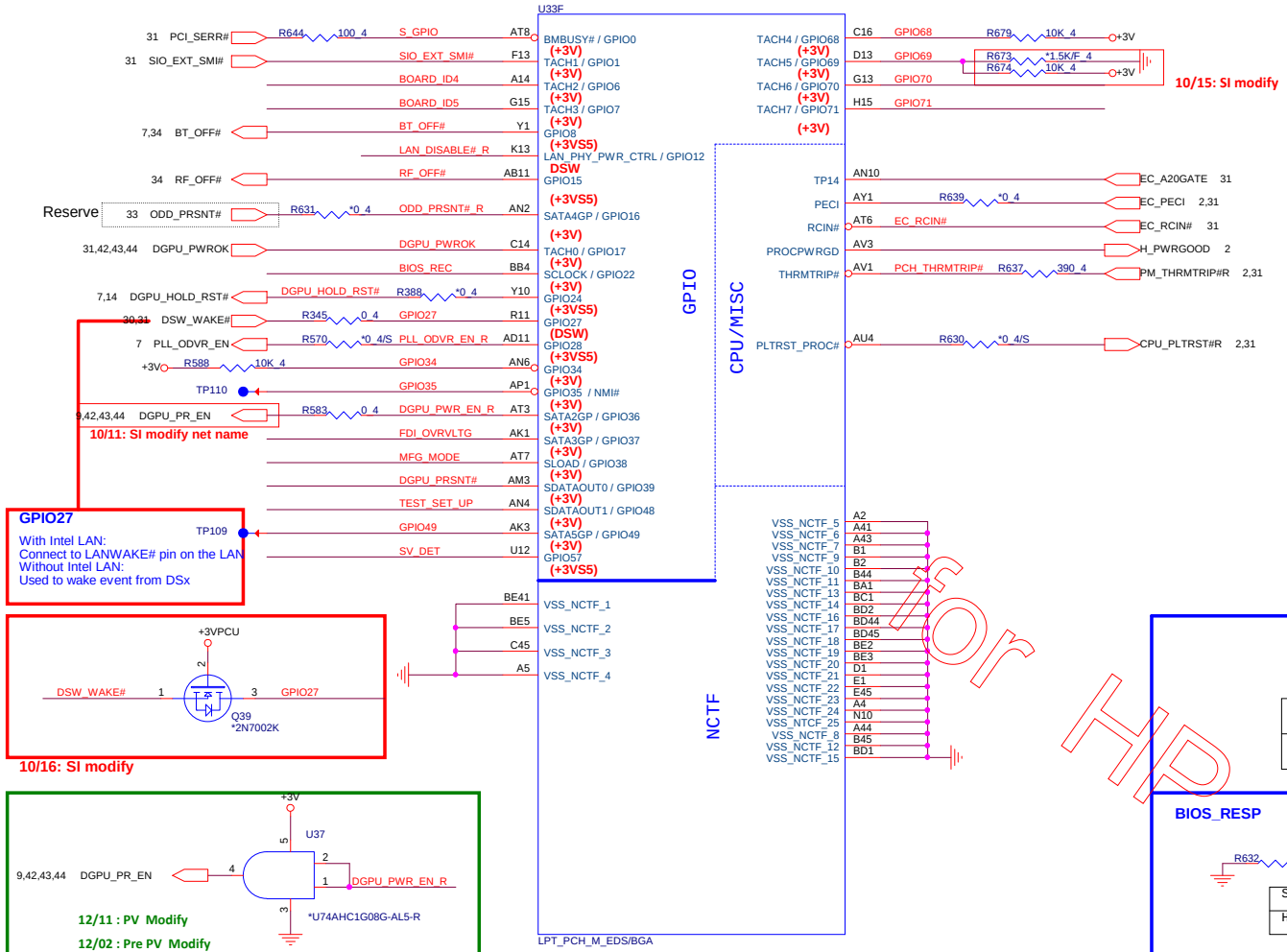
Lynx Point (GPIO,VSS_NCTF,RSVD)



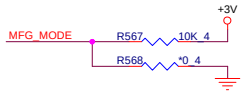
Clock Gen Power OK (CLG)

+3V_DEEP_SUS 6,7,8,10,39
+3VS5 2,6,7,10,34,36,38,39,42,44
+3V 2,6,7,8,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+5VS5 23,29,30,34,36,37,38,39,40,41,42,43,44

09

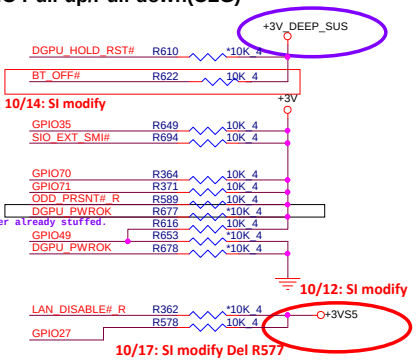
PCH MISC PU /PD

MFG-TEST



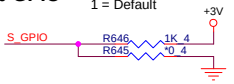
GPIO Pull-up/Pull-down(CLG)

for DS3

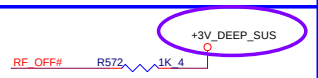


Swap GPIO

0 = SGPIO
1 = Default



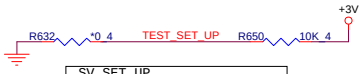
for DS3



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

BIOS RECOVERY	High = Disable (Default) Low = Enable

BIOS_RESP

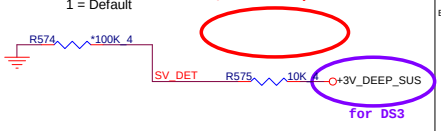


SV_SET_UP
High = Strong (Default)

SV Detect

0 = SV Detect
1 = Default

10/17: SI modify



GPIO36

Internal PD

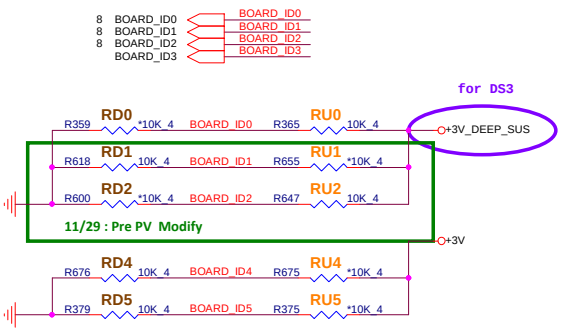
SATA3GP/GPIO37

TLS Confidentiality

0 = TLS no confidentiality (Int PD)
1 = TLS with confidentiality

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4		BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R63 UMA				0	0	0
DB R63 DIS				0	0	1
SI R63 UMA				0	0	0
SI R63 DIS				0	0	1
PV R63 UMA				1	0	0
PV R63 DIS				1	0	1



GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

NB5

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Quanta Computer Inc.

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Custom	PCH 4/6 (GPIO/MISC)	1A
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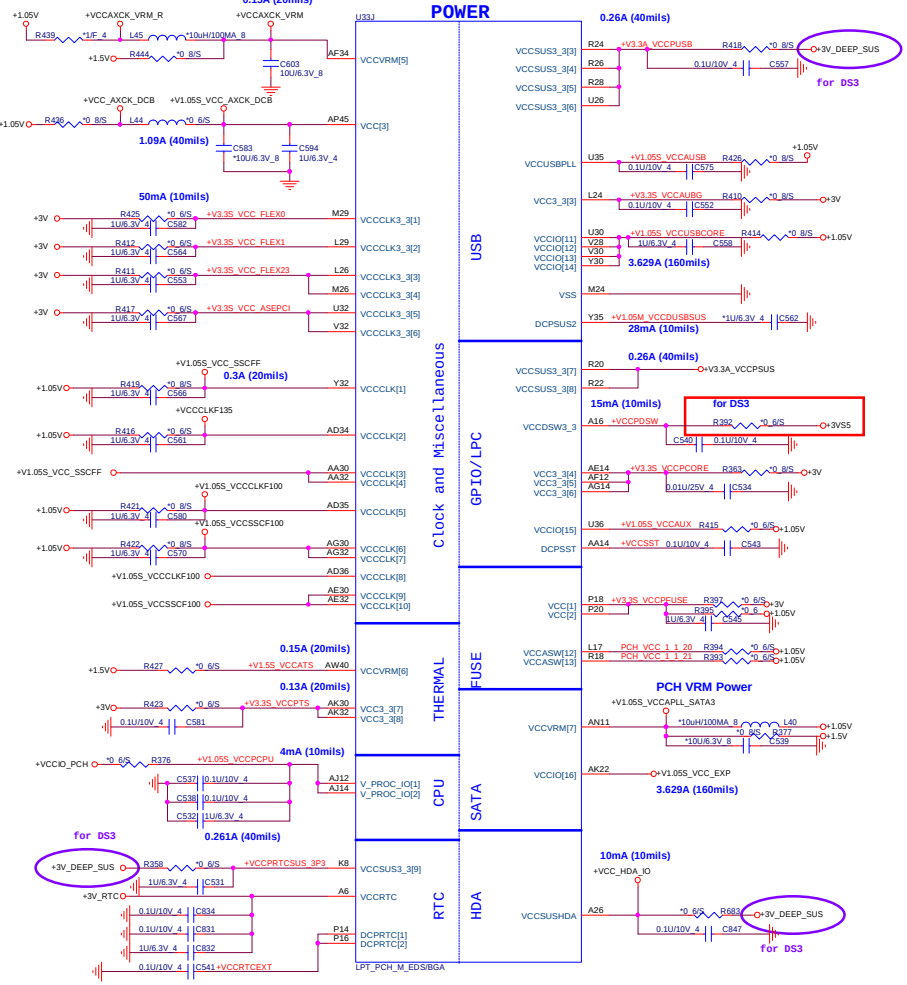
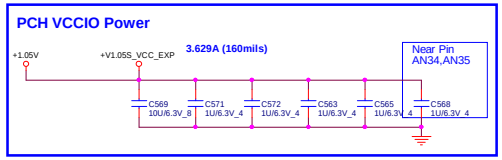
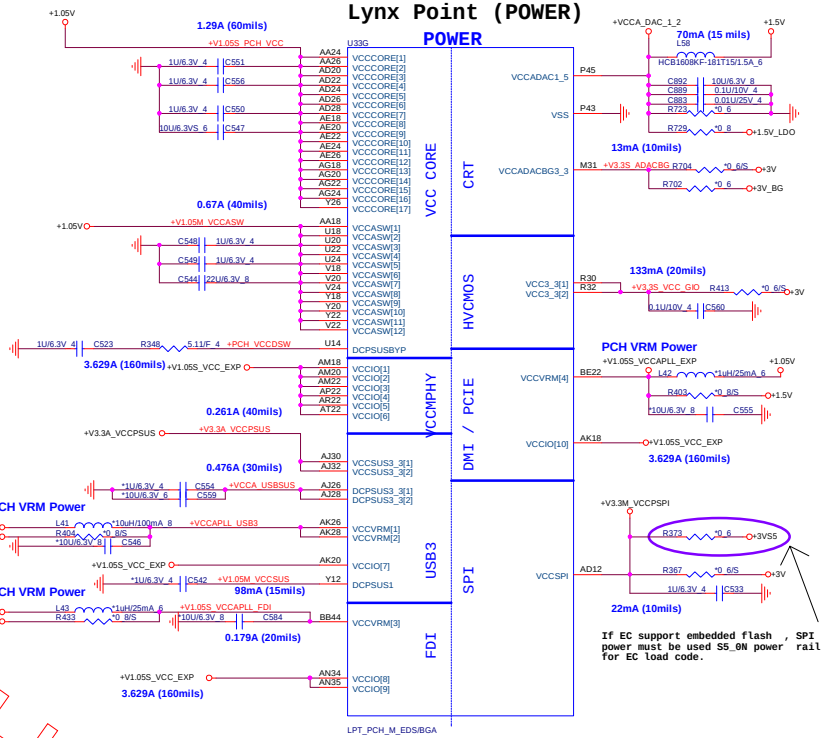
for HP

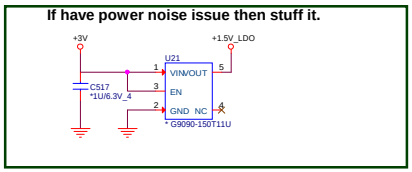
Lynx Point (POWER)

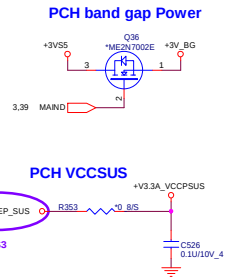


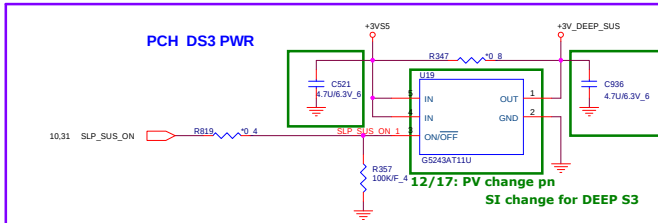


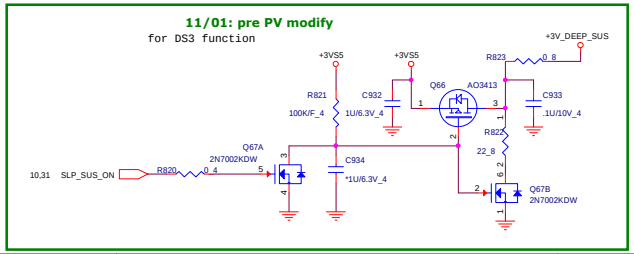
Lynx Point (POWER)











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Quanta Computer Inc.

NB5

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for HP

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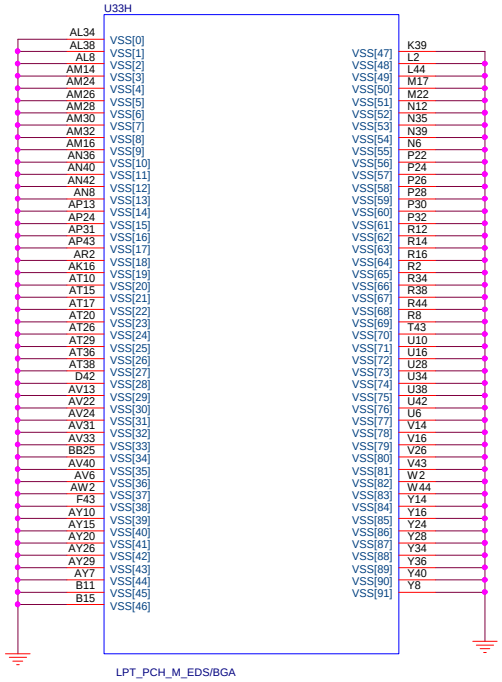
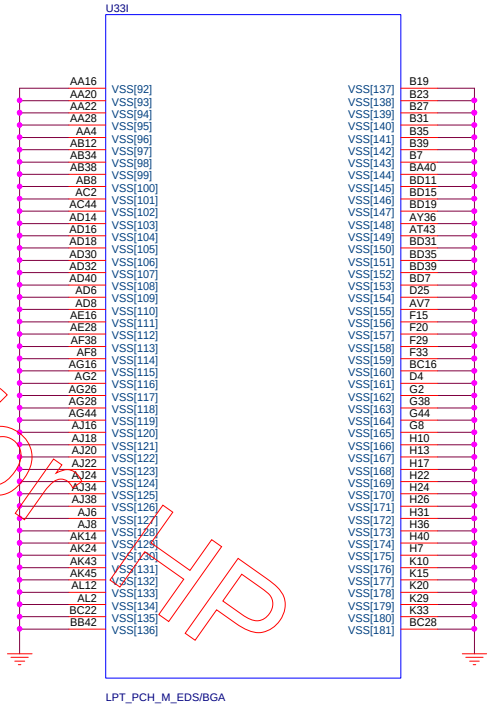
Lynx Point (GND)



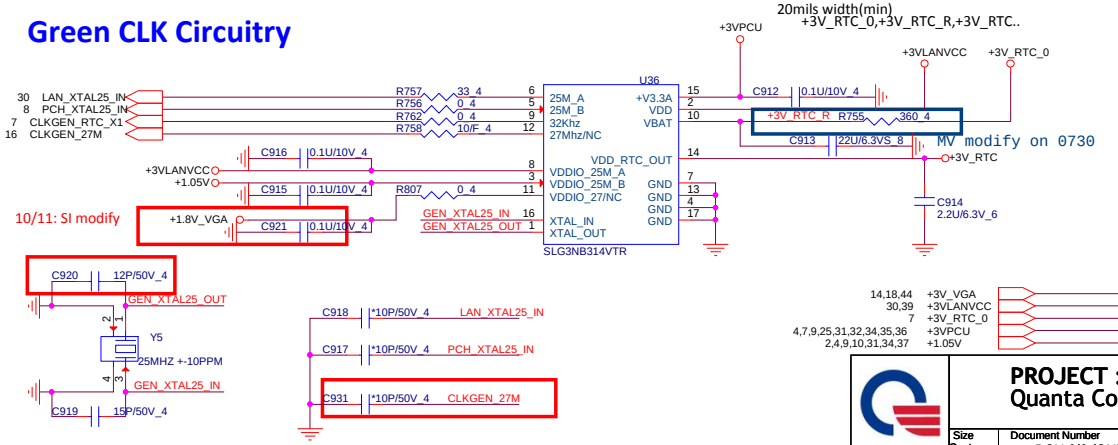
Lynx Point (GND)



for ZIP

	U36 P/N
UMA	AL3NB244000
DIS	AL000314000

Green CLK Circuitry



PROJECT :	R63
Quanta Computer Inc.	
Size: Custom	Document Number: PCH 6/6 (GND)
Rev: 1A	
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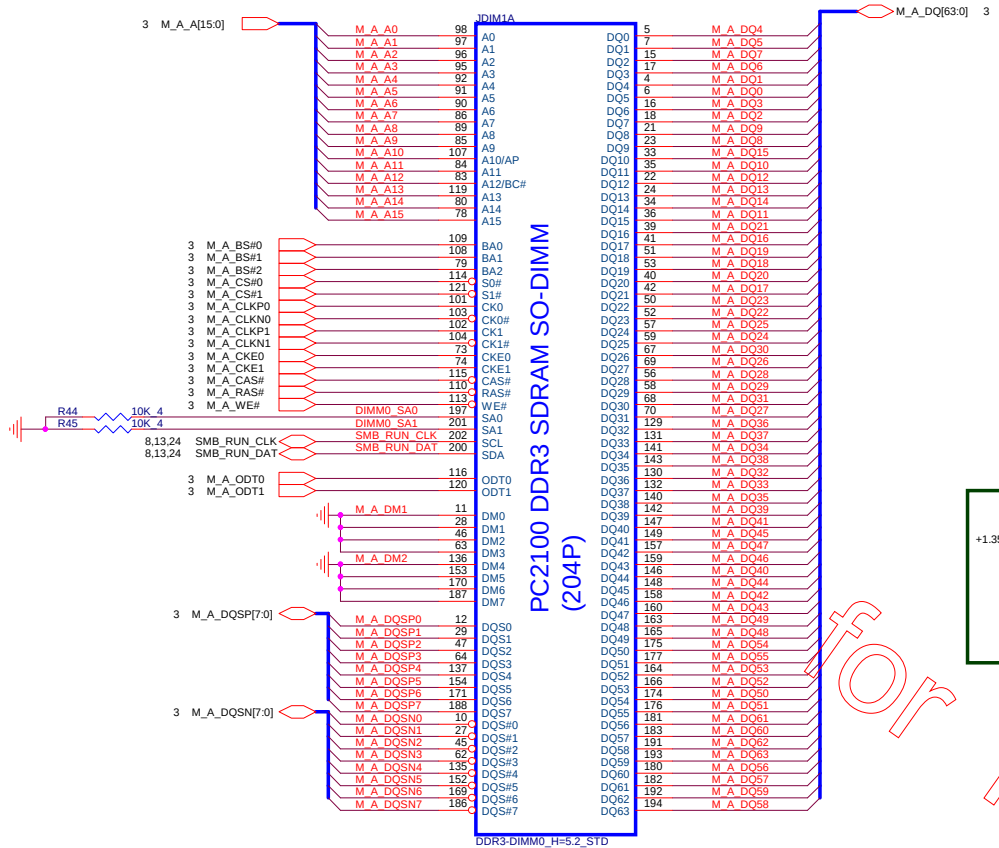
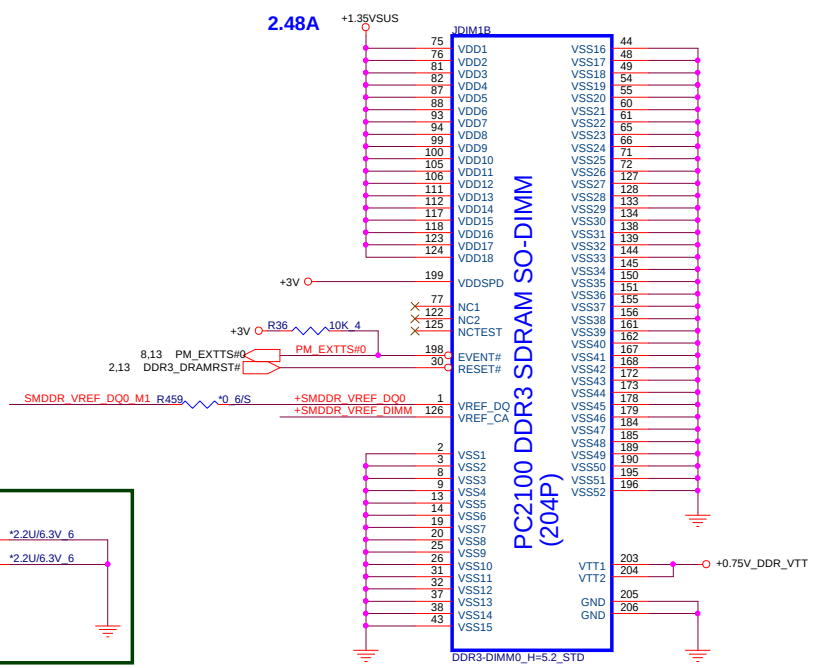
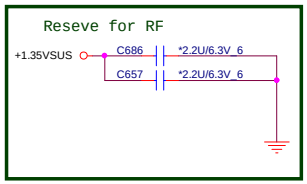
NB5

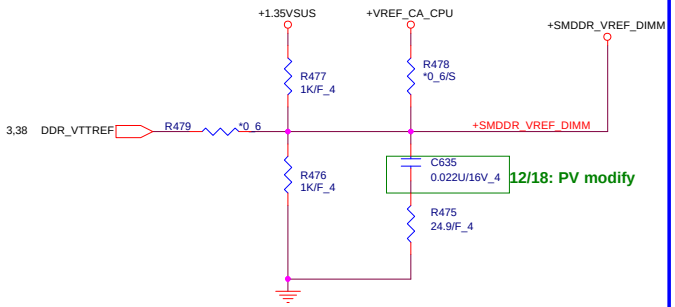




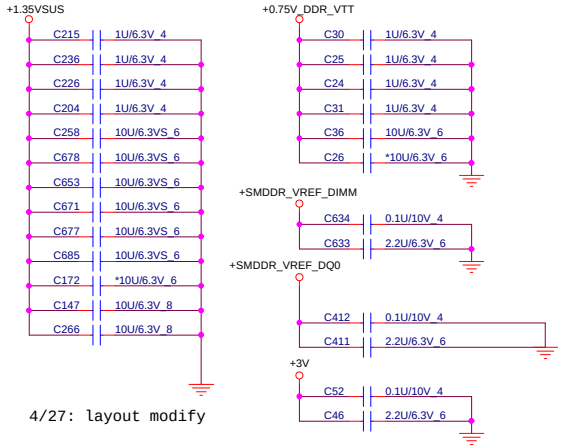


for HP

+SMDDR_VREF_DIMM 13
+VREF_CA_CPU 3
+0.75V_DDR_VTT 13,38,39
+1.35VSUS 2,3,4,13,38
+3V 2,6,7,8,9,10,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44



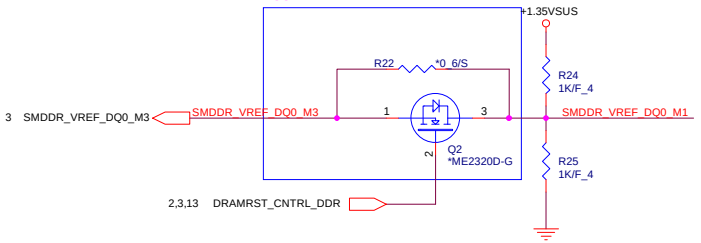
Place these Caps near So-Dimm0.



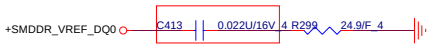
4/27: layout modify

VREF DQ0 M1 Solution

8/31: Intel suggestion



10/17: SI modify



NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM0-RVS (5.2H)	Rev: 1A
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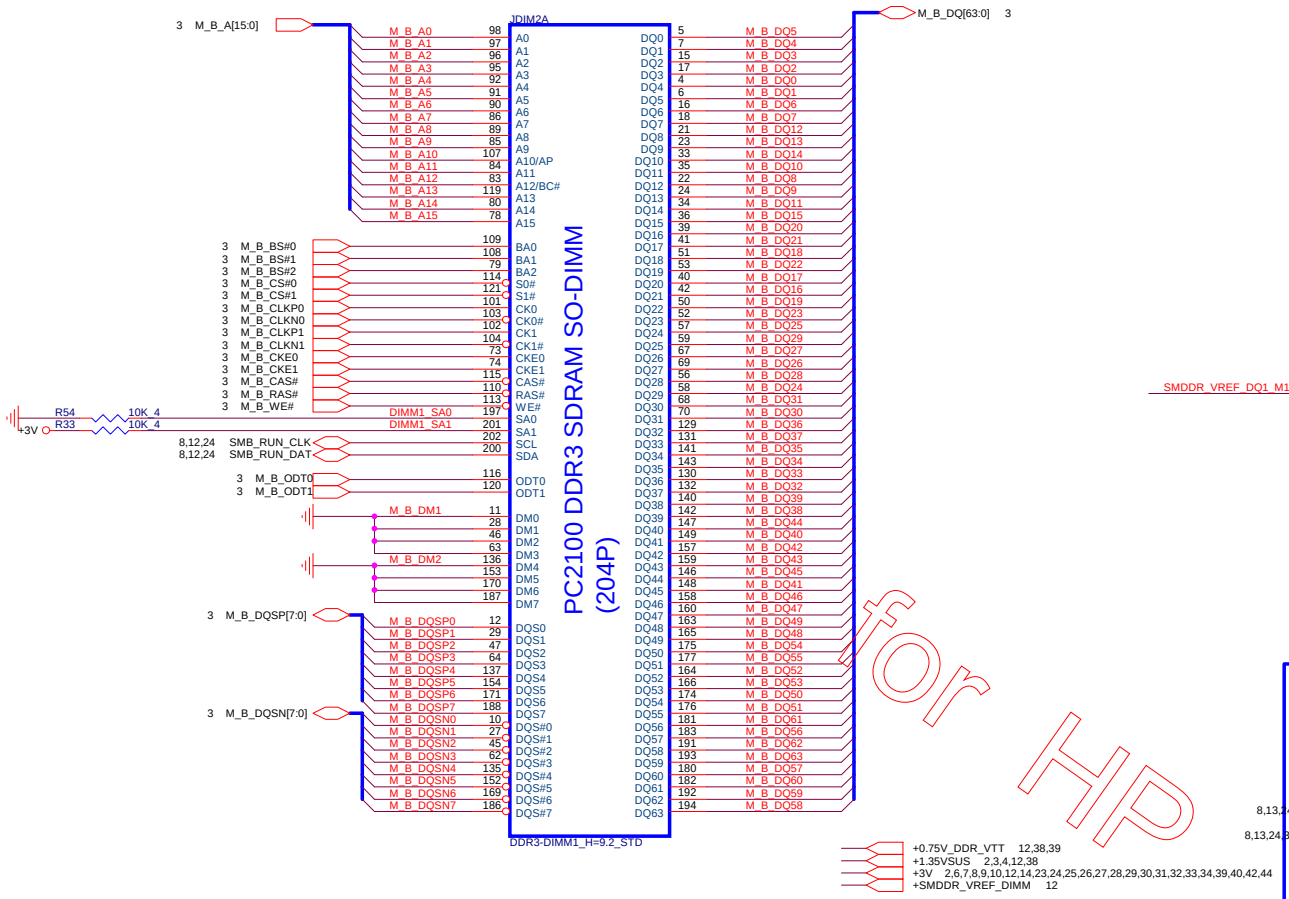
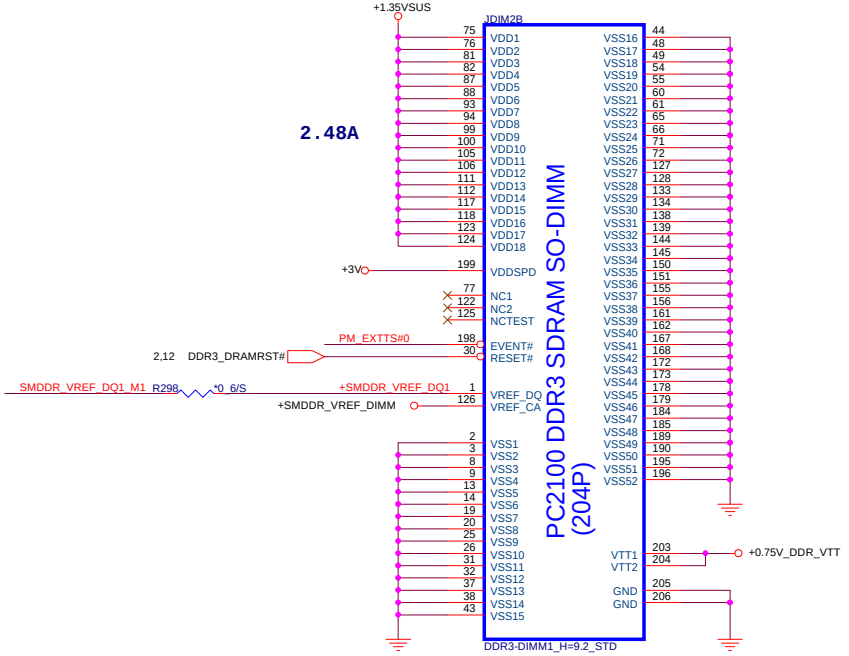
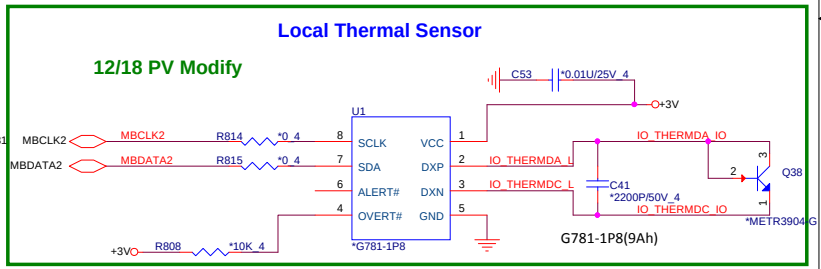


for HP

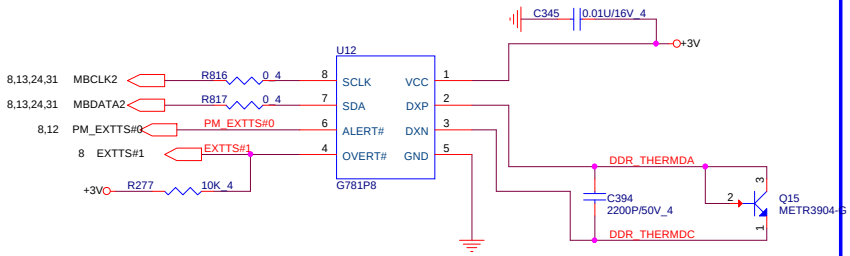


Local Thermal Sensor

12/18 PV Modify

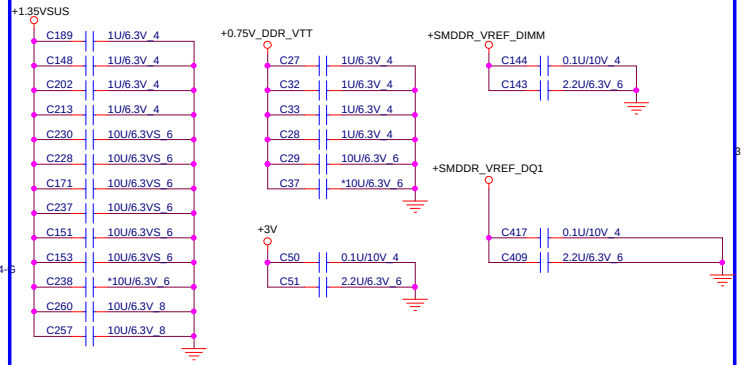


DDR Thermal Sensor



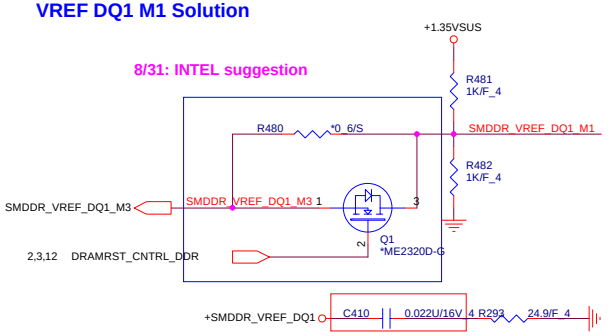
Address: G781P8(98h)

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution

8/31: INTEL suggestion



NB5

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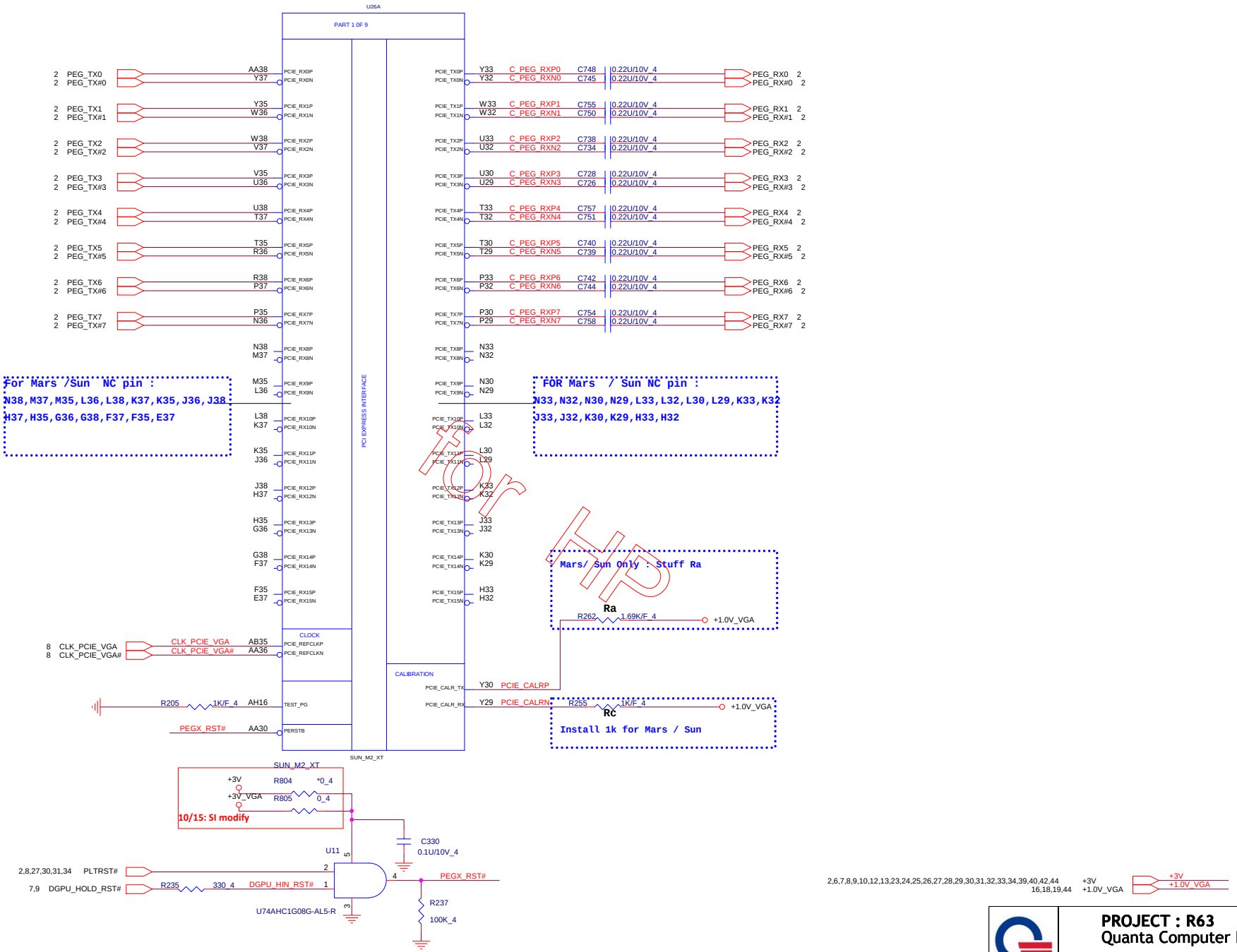
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A
Date: Friday, December 21, 2012	Sheet 13 of 44	



PROJECT : R63
Quanta Computer Inc.

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Custom	THAMES_PCIE_Interface	1A
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For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

For Sun only : AD28 /AC28 /AJ21 /AR21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

10/17: SI modify

12/13: PV modify

8/24: DB Modify

A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.

FOR SUN GPIO NC PIN : AJ19/ AK19 / AK24 / AM14 / AN14 / AJ24/ AH26 / AH24 / AJ20
AK20/ AH18 / AN16 / AK17 / AK16 / AL16/ AM16

Mars: stuff
For Sun Nc: R167, R141, C155
10/14: SI modify

FOR MARS: AD37/ AE38 / AD35 AVSSN to GND
FOR SUN : AD37/ AE38 / AD35 NC pin

8/15 DB Modify

10/14 SI Modify
DEL R747 R748 R749

10/14: SI modify , DEL R751, R753

FOR SUN NC PIN : AD34/ AE34 / AC33 / AC34 / AD39 / AE36
AF37/ AC36 / AC38 / AB34 /

8/15 Modify

PV, change to 0ohm
DAC1 Analog Power
AVDD : 1.8V @ 18mA
DAC1 Digital Power
VDD1D1 : 1.8V @ 117mA
PV, change to 0ohm
PV, change to DNI

Thermal Solution(Close to GPU)

12/13: PV modify

Address: G781-1P8(9Ah)

Reserve for Power Play

For Mars: Stuff Ra, Rc=> VDDC 1.1V

For Mars / Sun:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :NC pin
AL27, AM27, AN20, AN26, AM26, AL19, ,
AM19, AJ30, AJ31

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	00001
PS2	=>	00000
PS3	=>	11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K

PS3 BIT3=>BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	256Mx16 *4 pces	AKD5PGWTW08 IC SDRAM(96P)H5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M16HA-093G:E	256Mx16 *4 pces	AKD5PZSTL01 IC SDRAM(96P)MT41J256M16HA-093G:E	2G
010	2	Samsung	K4W4G1646B-HC1A	256Mx16 *4 pces	AKD5PZDT501 IC SDRAM(96P)K4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FRR-11C	128Mx16 *4 pces	AKD5MZDTW03 IC SDRAM(96P)H5TC2G63FRR-11C	1G
100	4	Micron	MT41J128M16JT-093G:E	128Mx16 *4 pces		1G
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pces	AKD5MGGT535 IC SDRAM(96P)K4W2G1646E-BC1A	1G

14,16,18,19,44 +1.0V_VGA → +1.0V_VGA
11,16,18,19,44 +1.8V_VGA → +1.8V_VGA
17,18 +3V_DELAY → +3V_DELAY

NB5

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Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

La
+1.8V_VGA — L23 *0_6/S — +1.8V_DPLL_PVDD
C259 10U/6.3V_8, C264 1U/6.3V_4, C265 0.1U/10V_4
Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

Lb
+1.0V_VGA — L21 *0_6/S — +1.0V_DPLL_VDDC
C253 10U/6.3V_8, C268 1U/6.3V_4, C267 0.1U/10V_4
1.0V(125mA DPLL_VDDC)
DPLL_VDDC : 0.935V @ 140mA
DPLL_PVSS

+1.8V_VGA — HCB1608KF-471T10 L35 — +1.8V_MPLL_PVDD
C441 10U/6.3V_8, C437 1U/6.3V_4, C438 0.1U/10V_4
MPLL_PVDD : 1.8V @ 150mA

+1.8V_VGA — L16 FCM1005KF-121T03 — +1.8V_SPLL_PVDD
C167 10U/6.3V_8, C176 1U/6.3V_4, C191 0.1U/10V_4
SPLL_PVDD : 1.8V @ 75mA

+1.0V_VGA — L19 HCB1608KF-471T10 — +1.0V_SPLL_VDDC
C181 10U/6.3V_8, C222 1U/6.3V_4, C216 0.1U/10V_4
1.0V(125mA DPLL_VDDC)
SPLL_VDDC : 0.935V @ 150mA
SPLL_PVSS

DPEF_VDD18
R212 Ra *0_4
R249 Rb *0_4
reserve Ra, Rb for future ASIC
10/14: SI modify

U26I
PART 9 OF 9
AM32 DPLL_PVDD
AN31 DPLL_VDDC
AN32 DPLL_PVSS
H7 H8 MPLL_PVDD
AM10 SPLL_PVDD
AN9 SPLL_VDDC
AN10 SPLL_PVSS
AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS
PLL5XTAL
SUN_M2_XT

XTALIN AV33 — 0_4 R759 — CLKGEN_27M 11
XTALIN AV33 — *0_4 R792 — EVGA-XTALI — *22P/50V_4 C244
R207 *10M_4
Y2 *7A27000010
XTALOUT AU34 — *0_4 R793 — EVGA-XTALO — *22P/50V_4 C245
11/29: Pre PV modify
XO_IN AW34 — TP129
12/13: PV modify del
XO_IN2 AW35 — R487 *0_4
CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB
C193 *0.1U/10V_4, C227 *0.1U/10V_4
R171 *51.1/F_4, R191 *51.1/F_4
Debug only,
for clock observation,
if not needed, DNI
route 50ohms
single-ended/
100ohms diff and keep short
for ASIC

U26F
PART 6 OF 9
PCIE_VSS: AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U31 U34 V34 V39 W31 W34 Y34 Y39
GND: F15 F17 F19 F21 F23 F25 F27 F29 F31 F33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L2 L22 L24 L6 M17 M22 M24 N16 N18 N2 N21 N23 N26 N6 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27
GND: A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20 AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13
VSS_MECH: A39 AW1 AW39
SUN_M2_XT
AG22 is nc pin

14,18,19,44 +1.0V_VGA → +1.0V_VGA
11,15,18,19,44 +1.8V_VGA → +1.8V_VGA

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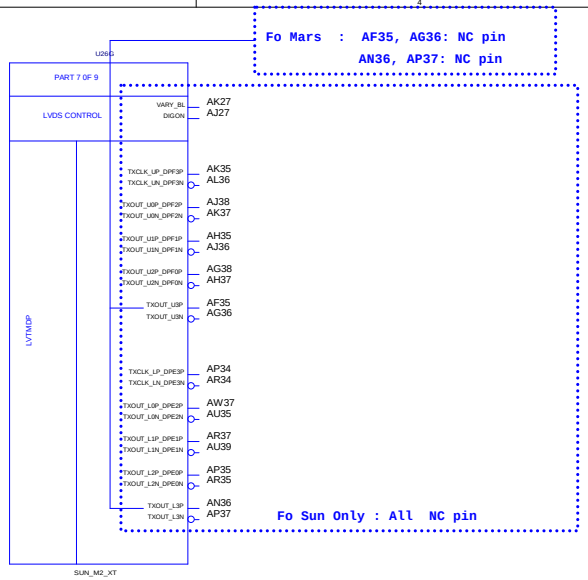
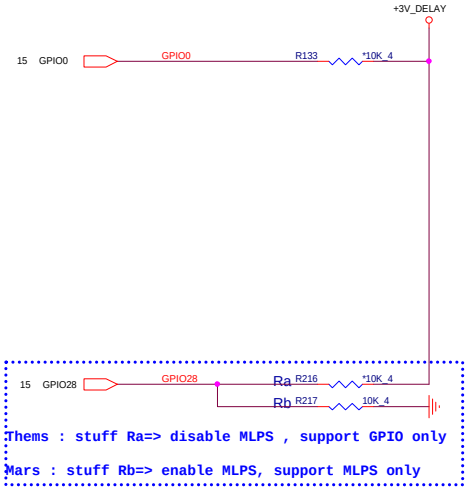




CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50%_Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

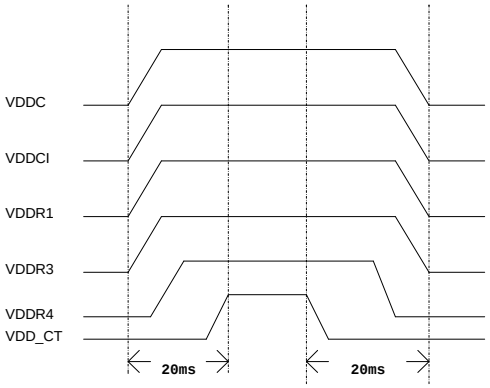
for HD

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	+3.3V_Delay
0	512M	1	0	0	+1.8V_VGA
0	1G	1	0	1	+1.8V_VGA
0	2G	1	1	0	
0	4G	1	1	1	

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



NB5

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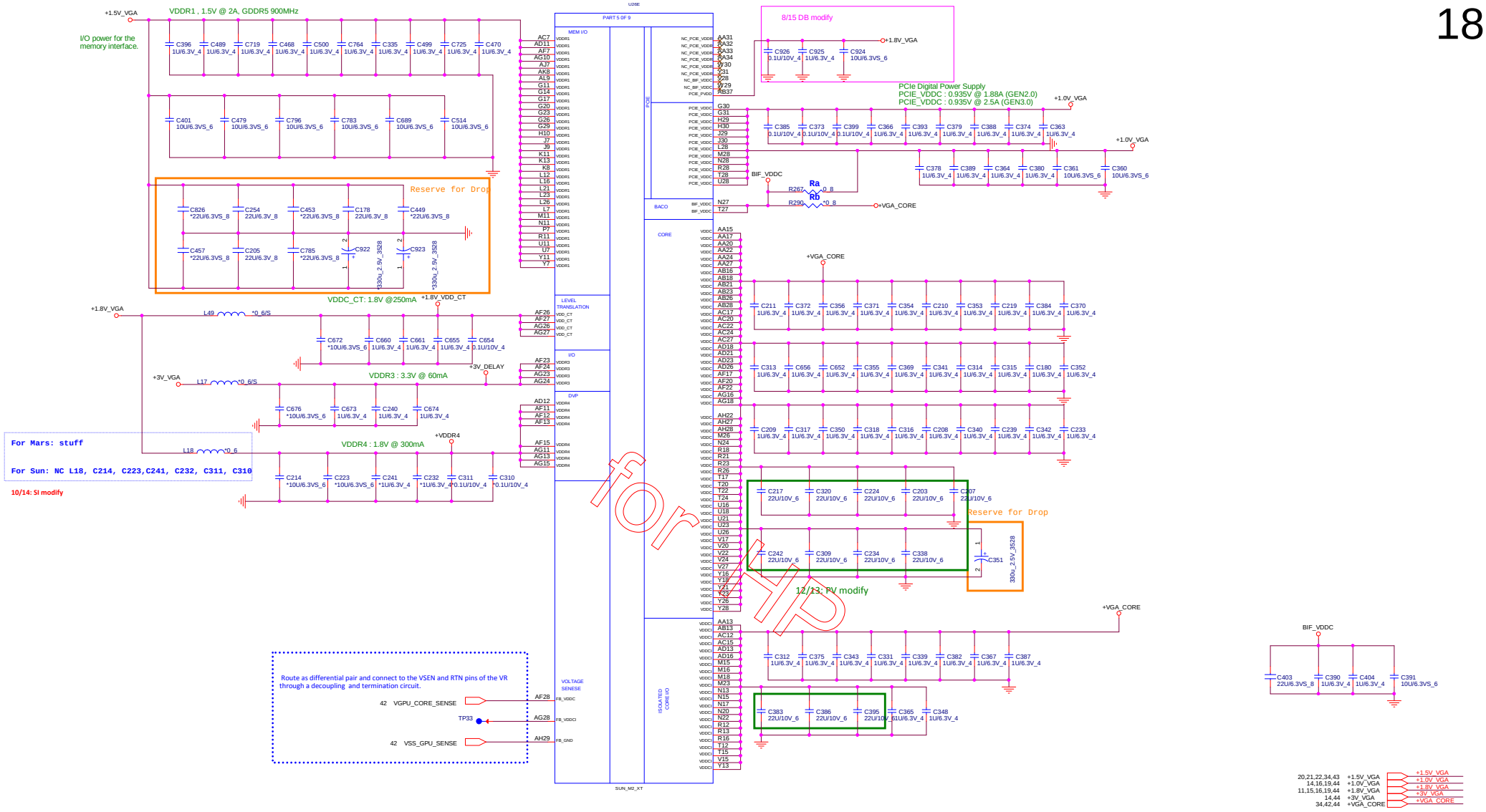

Support BACO Mode

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

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For Mars : L20 sutff
For Sun: L20 , C247 , C246 , C252 NC

+1.0V_VGA
DPAB_VDD10
L20 *0_6
C247 *0.1U/10V_4
C246 *1U/6.3V_4
C252 *10U/6.3VS_6

10/14: SI modify

U26H
PART 8 0F 9
DP_VDDR
DP_VDDC
DP GND
CALIBRATION

DP_VDDC: AP31, AP32, AN33, AP33
DP_VDDC: AP13, AT13, AP14, AP15
DP_VDDC: AL33, AM33, AK33, AK34

DP_VDDR: AN24, AP24, AP25, AP26, AU28, AV29
DP_VDDR: AP20, AP21, AP22, AP23, AU18, AV19
DP_VDDR: AH34, AJ34, AF34, AG34, AM37, AL38

10/14: SI modify

For Mars : L26 sutff
For Sun: L26 , C279 , C281 , C282 NC

+1.8V_VGA
L26 *0_6
DPEF_VDD18
C279 *10U/6.3VS_6
C281 *1U/6.3V_4
C282 *0.1U/10V_4

10/14: SI modify

DPEF_VDD10
L25 *0_6
+1.0V_VGA
C291 *0.1U/10V_4
C290 *1U/6.3V_4
C293 *10U/6.3VS_6

For Mars : L25 sutff
For Sun : L25/ C293/C290/C291 NC

DP_VSSR: AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, AM35

AW28 DPAB_CALR
AW18 DPCD_CALR
AM39 DPEF_CALR

10/14: SI modify

R495 *150/F_4

For Mars : R495 sutff
For Sun : R495 NC

10/14: SI modify DEL R754

For Mars : R754 sutff
For Sun : R754 NC

SUN_M2_XT

14,16,18,44 +1.0V_VGA
11,15,16,18,44 +1.8V_VGA

+1.0V_VGA
+1.8V_VGA

for PDQ

NB5

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Custom	THAMES_DP Powers	1A
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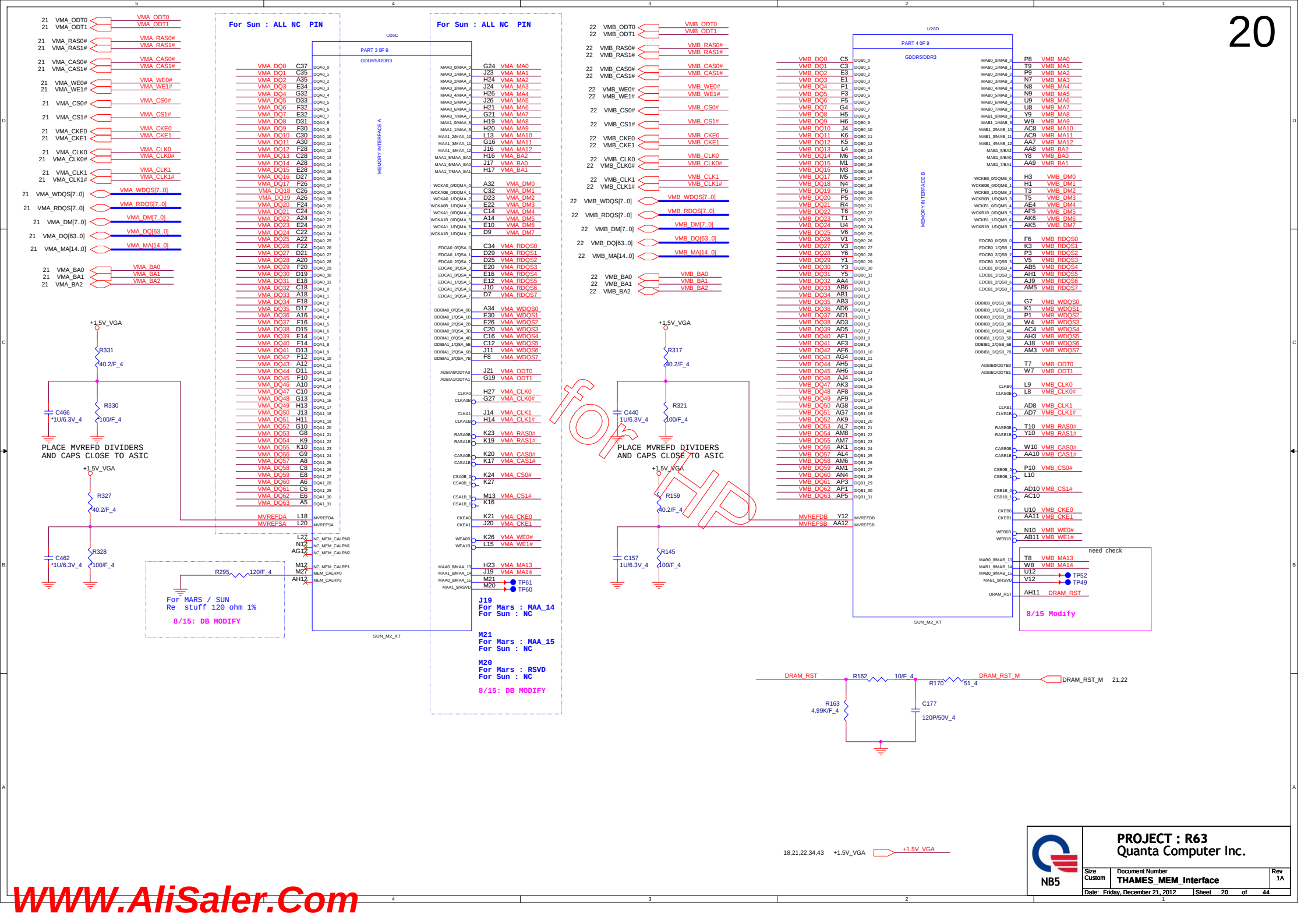

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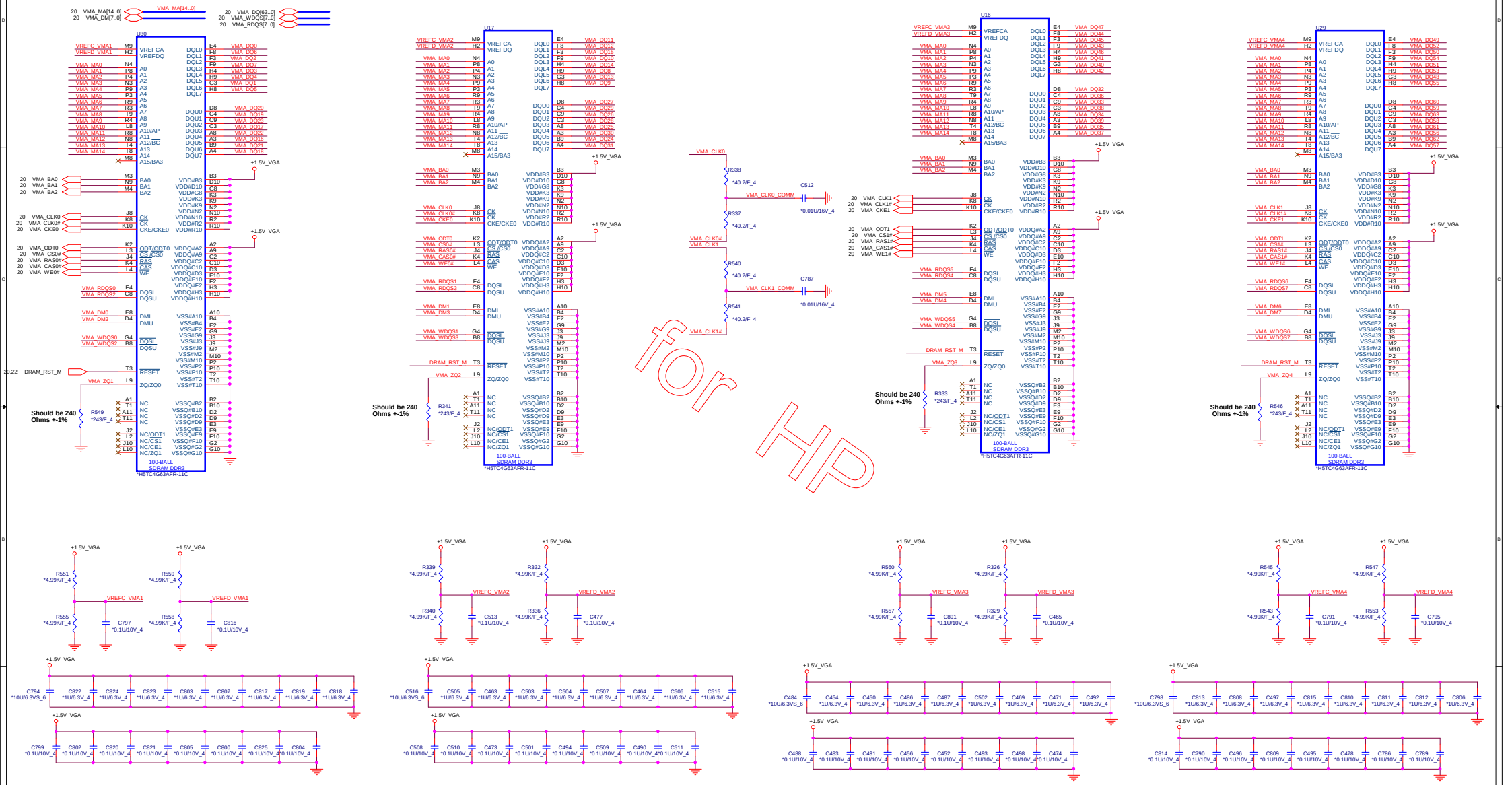
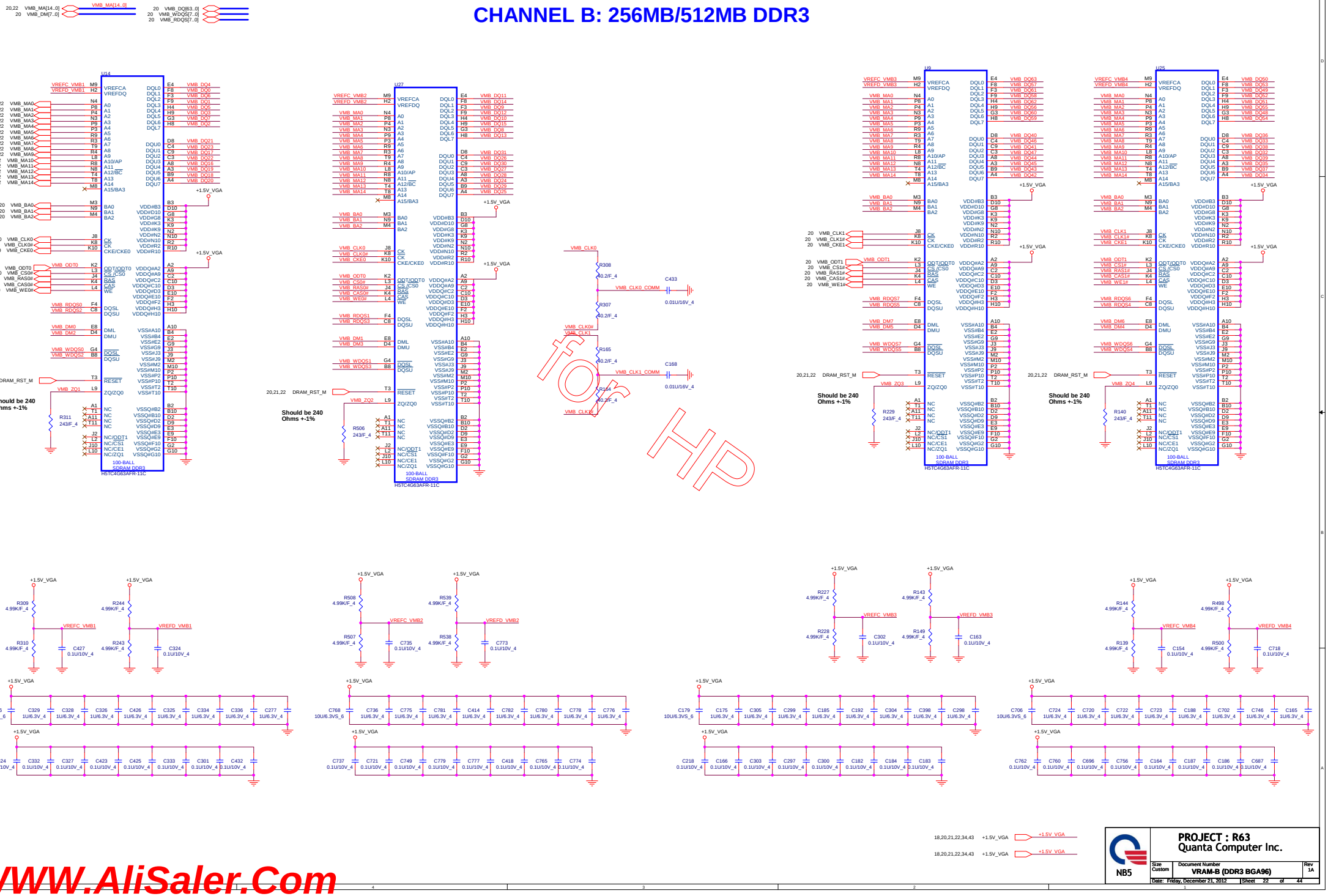
CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3



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7,26,28,29,32,33,34,39 +5V
2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
29,30,34,36,37,38,39,40,41,42,43,44 +5VS5
26 +5V_HDMIC

CRT PORT

10/24: SI modify

12/13: PV modify

6 CRT_R
6 CRT_G
6 CRT_B
CRT_R
CRT_G
CRT_B
L15 BLM18BB470
L14 BLM18BB470
L13 BLM18BB470
CRT_R1
CRT_G1
CRT_B1
R112 150/F_4
R104 150/F_4
R100 150/F_4
C131 22P/50V_4
C115 22P/50V_4
C125 22P/50V_4
C101 22P/50V_4
C102 22P/50V_4
C138 22P/50V_4
EMI

+5V_HDMIC
CRTDDCDAT2 C170 *470P/50V_4
CRTHSYNC C199 10P/50V_4
CRTVSYNC C200 10P/50V_4
CRTDDCCLK2 C174 *470P/50V_4
CRT CONN
CN9
DFDS15FR362
dsub-dsd-15atxb-15p

6 HSYNC_COM
6 VSYNC_COM
6 DDCCLK
6 DDCDATA
HSYNC_COM
VSYNC_COM
DDCCLK
DDCDATA

+5V
+3V
U7
+5V_CRT2
C134 0.22U/25V_6
CRT_BYP
VCC_SYNC
VCC_DDC
BYP
VCC_VIDEO
VIDEO_1
VIDEO_2
VIDEO_3
GND
SYNC_OUT2
SYNC_OUT1
SYNC_IN2
SYNC_IN1
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
TPD7S019
CRT_VSYNC1 R157 22_4 CRTVSYNC
CRT_HSYNC1 R156 22_4 CRTHSYNC
VSYNC_COM
HSYNC_COM
DDCCLK
DDCDATA
VGA_DDC_CLK_RT
VGA_DDC_DAT_RT
R148 2.2K_4
R160 2.2K_4
CRTDDCCLK2
CRTDDCDAT2

DDCCLK R168 2.7K_4
DDCDATA R169 2.7K_4

+5V_HDMIC
+5V_HDMIC
MEK500V-40 D3
+5V_CRT2
C146 0.1U/10V_4

9/29 EMI request
+5VS5
C609 0.1U/10V_4
C64 0.1U/10V_4
C71 0.1U/10V_4

9/27 EMI request

for test

HOLE

H27 *spad-r63-8np
H16 *h-tc354bc315ic150d110p2
H5 *h-c354ic150d110p2
H6 *h-c354ic150d110p2
H4 *h-c354ic150d110p2

12/20: PV add
H20 *H-C315IC150D110P2
H22 *h-c197d110p2
H21 *h-c315ic150d110p2
H3 *H-C197D110P2
H17 *h-tc276bc315d236p2
H26 *H-C87D87N
H25 *spad-re197x79np

10/17: SI modify add H25

11/30: Pre PV modify add H26

12/13: PV modify H26 Del gnd

FAN hole
H2 *O-LX9-1

PCH BKT
H19 h-tc177bc276ic162d122p2
H18 h-tc177bc276ic162d122p2
Nut PN:MBUL1001010

CPU BKT
H11 *intel-cpu-bkt2

VGA BKT
H15 *H-TC248BC197D150P2
H14 *H-TC248BC197D150P2
H10 *H-TC248BC197D150P2

THERMAL BKT
H9 h-tc177bc276ic162d122p2
H1 *h-tc256bc276d168x155p2
H24 *h-e315x278d110p2

KB lock
H13 *H-TC354BC315IC150D110P2
H8 *H-TC354BC315IC150D110P2

NB5

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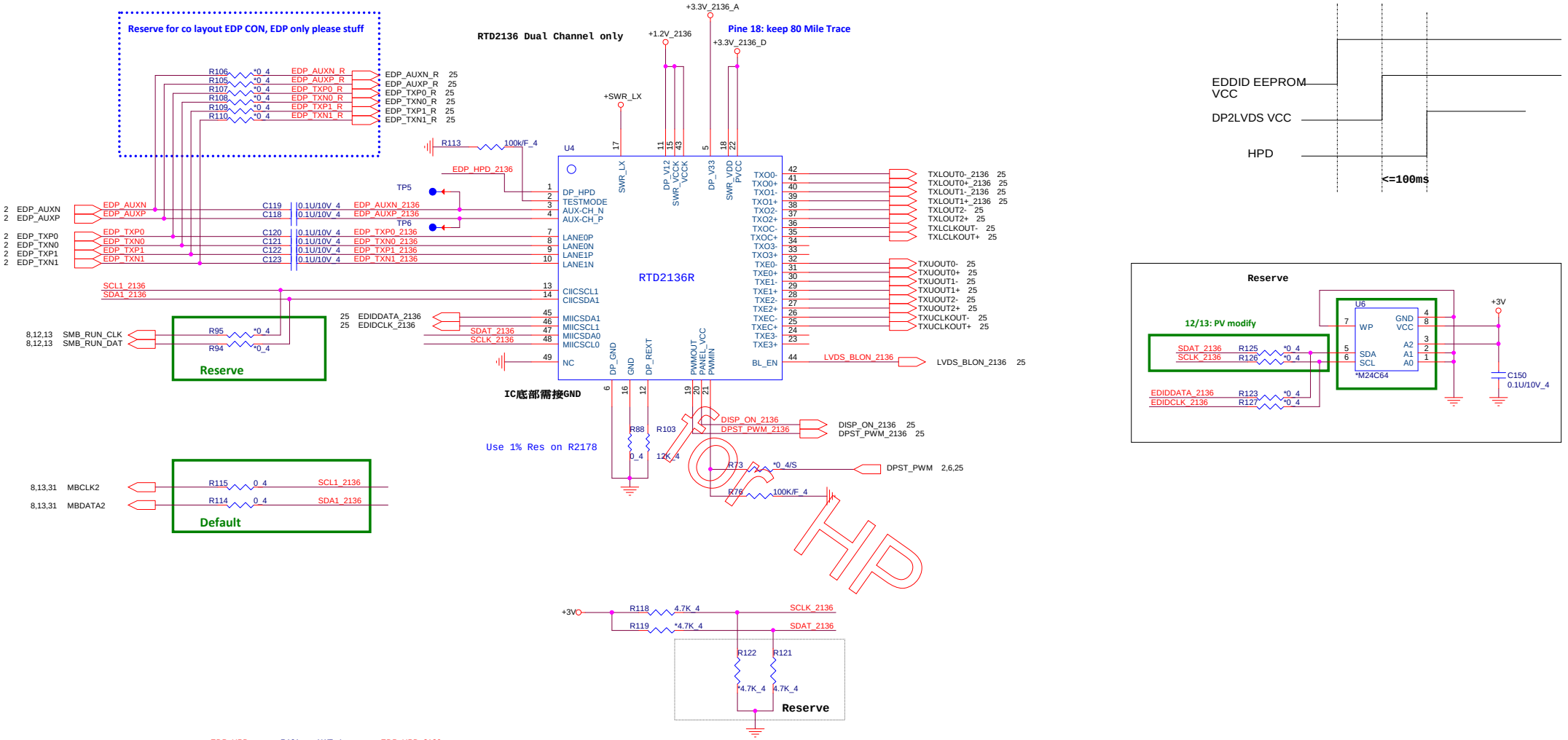

SWR MODE	LDO MODE
Stuff L8	Stuff R86

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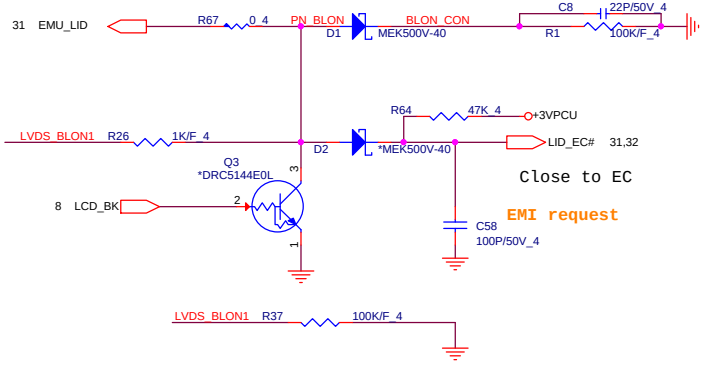
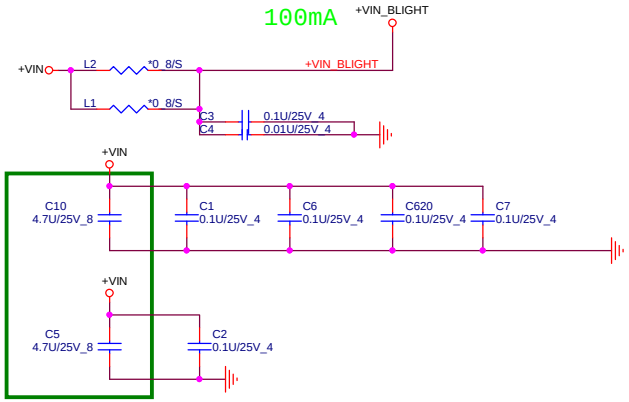
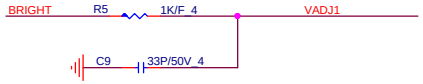
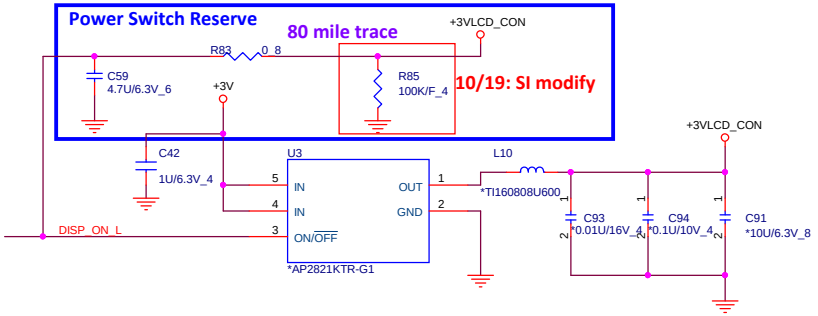
LID Switch

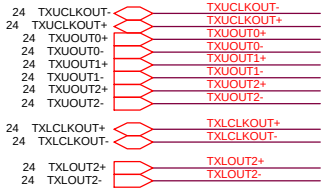


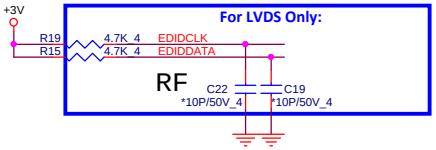


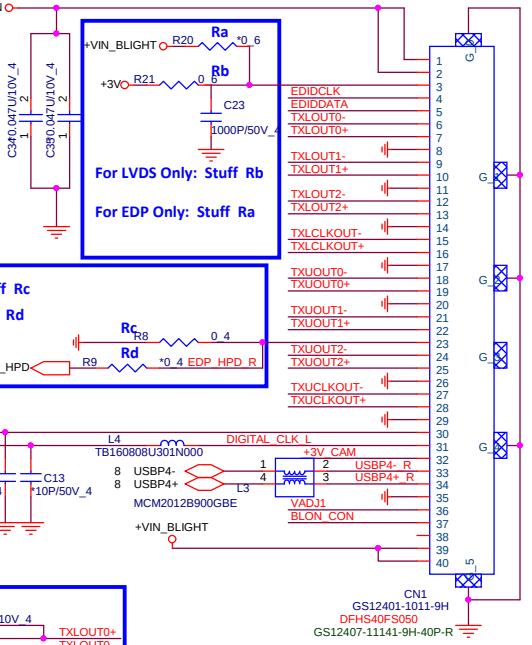
12/17: PV modify pn for 0.85 height

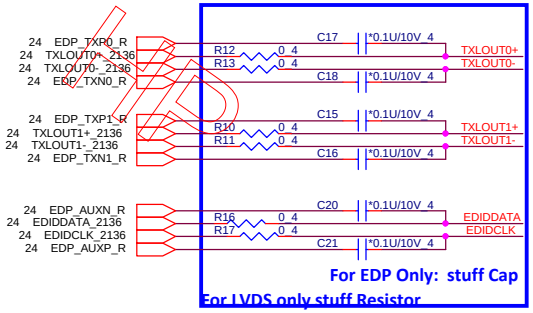


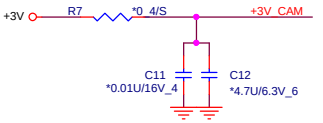


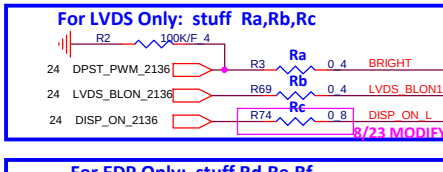


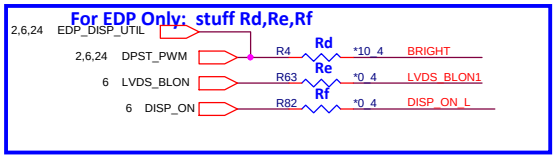


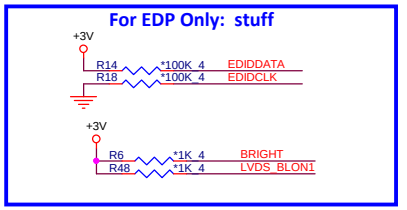


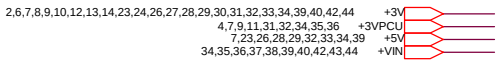












for

NB5

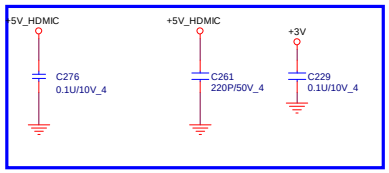
PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

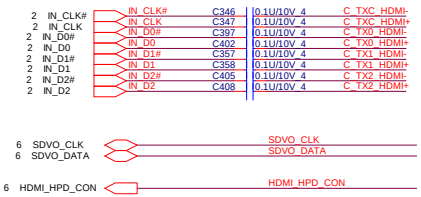
Date: Friday, December 21, 2012 Sheet 25 of 44

7,23,28,29,32,33,34,39 +5V
23 +5V_HDMIC
2,6,7,8,9,10,12,13,14,23,24,25,27,28,29,30,31,32,33,34,39,40,42,44 +3V

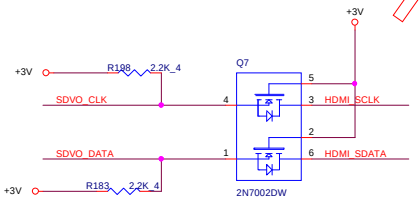
EMI request

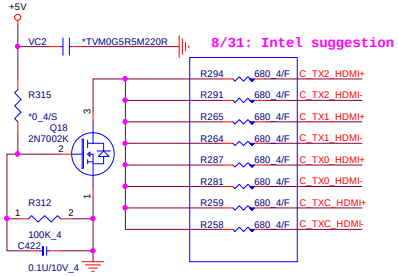


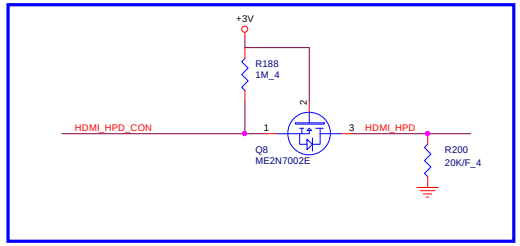
close to HDMI conn



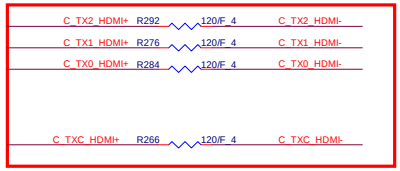
Close to HDMI Connector

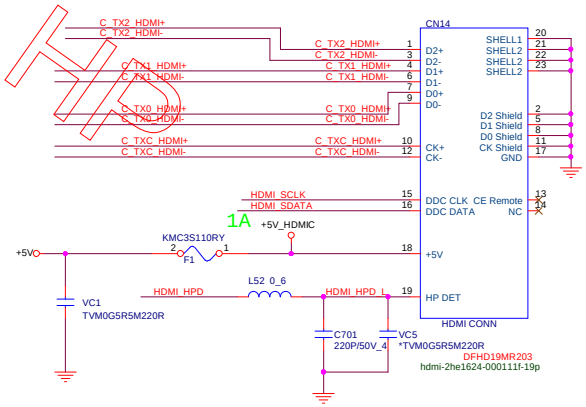


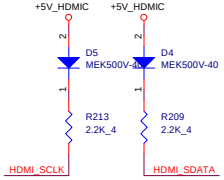




10/14: SI for EMI request







for KT

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A
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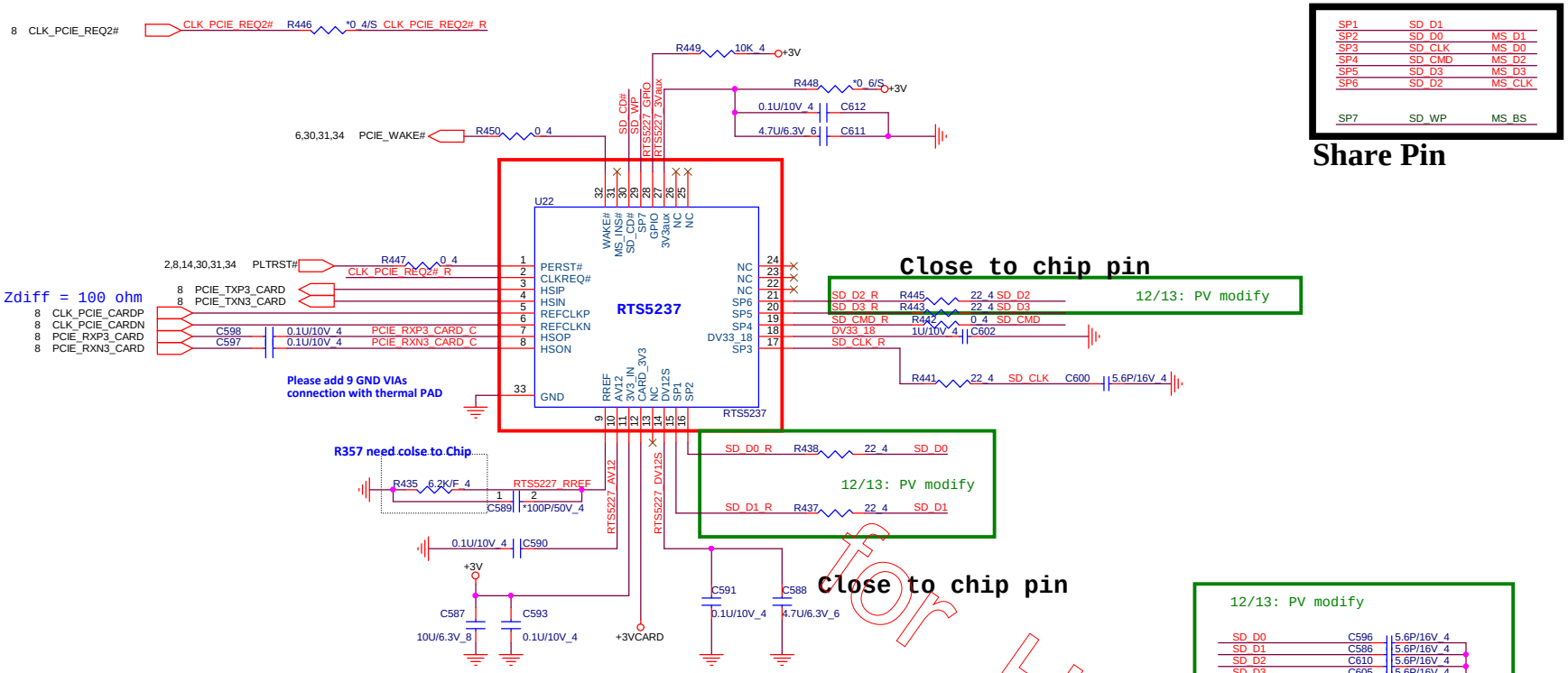
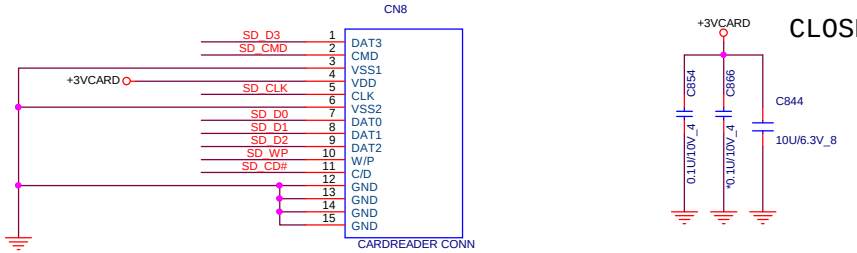


Share Pin

for HP

SD / MMC CARD READER



Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p

2,6,7,9,10,34,36,38,39,42,44 +3VS5
2,6,7,8,9,10,12,13,14,23,24,25,26,28,29,30,31,32,33,34,39,40,42,44 +3V
+3VCARD

NB5	PROJECT : R63 Quanta Computer Inc.	
Size Custom	Document Number RTS5229 & CR SOCKET	Rev 1A
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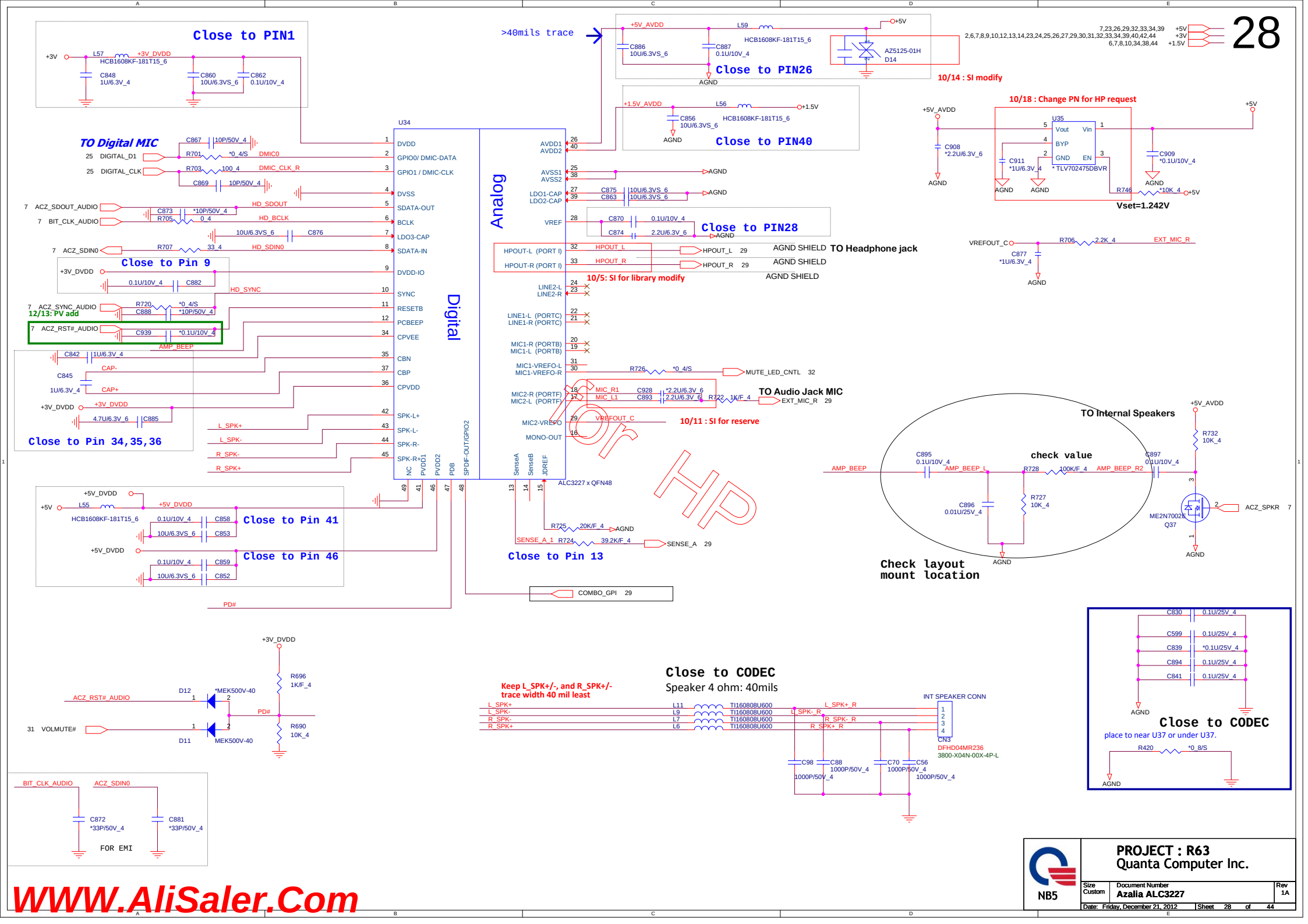

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NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC3227	1A

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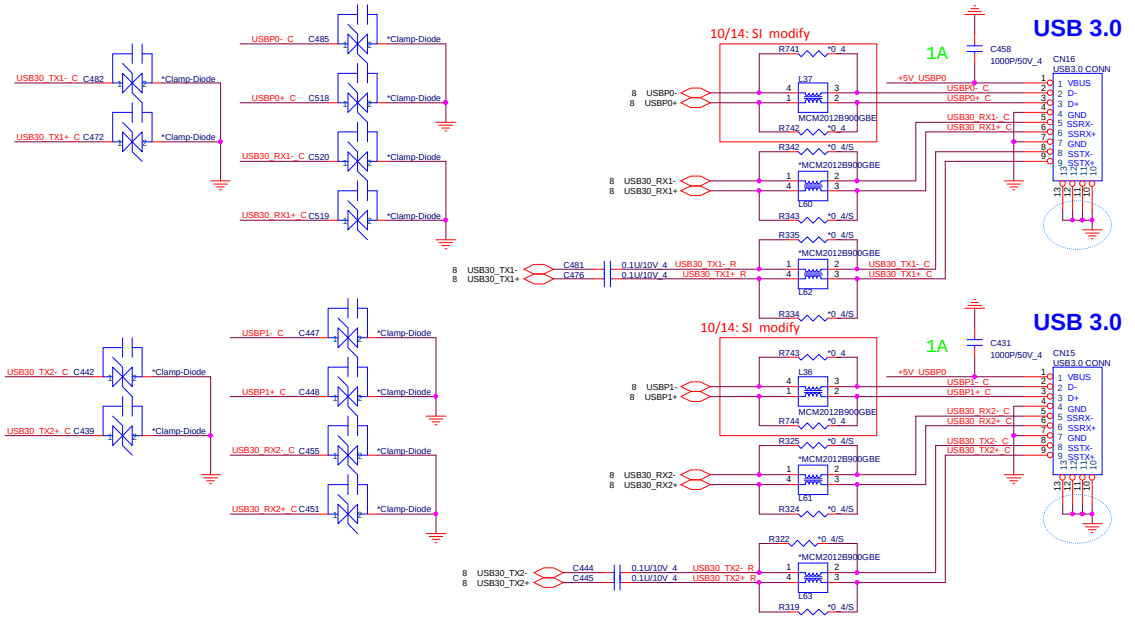
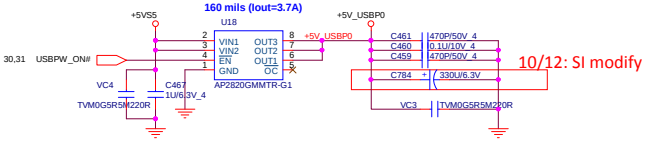
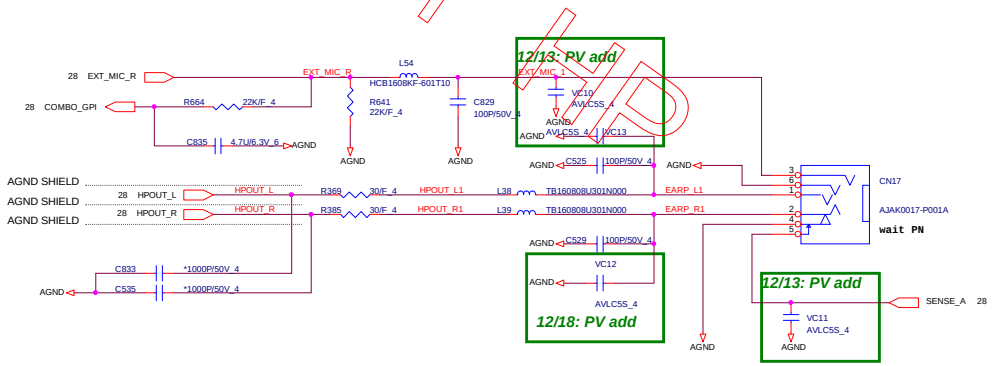


USB3.0 X 2/USB2.0 COMBO



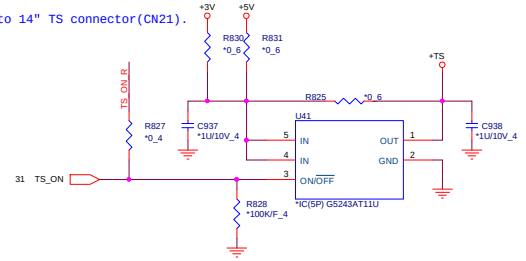
for COMBO JACK

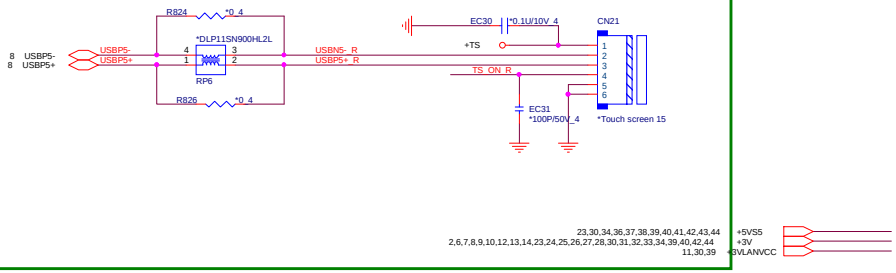


12/11: PV add

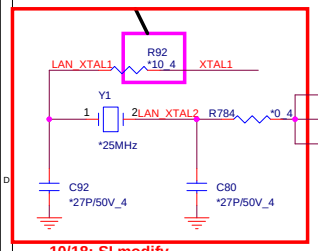
Touch Screen Connector

close to 14" TS connector(CN21).





For EMI 0 ~ 22 ohm



10/18: SI modify

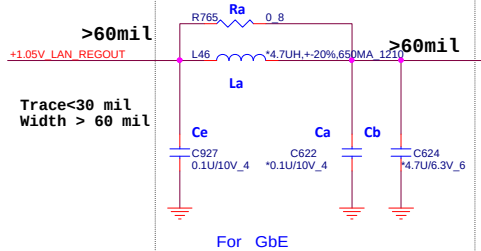
Power trace Layout 寬度> 60mil

>60mil

>60mil

+1.05V_LAN_REGOUT

Trace<30 mil
Width > 60 mil

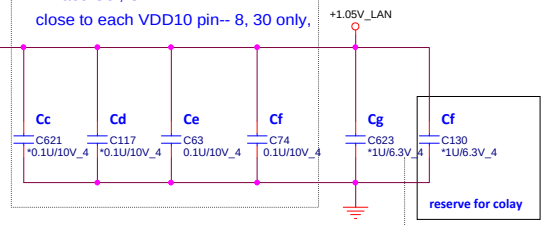


For GbE
Stuff La, Ca ,Cb

For 10/100
NA: La, Ca ,Cb
STUFF : Ra, Ce

For GbE
* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf
* Place Ce , Cf
close to each VDD10 pin-- 8, 30 only,



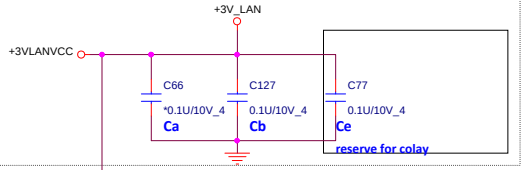
For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

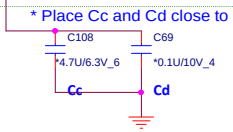
for ref

For 10/100
* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



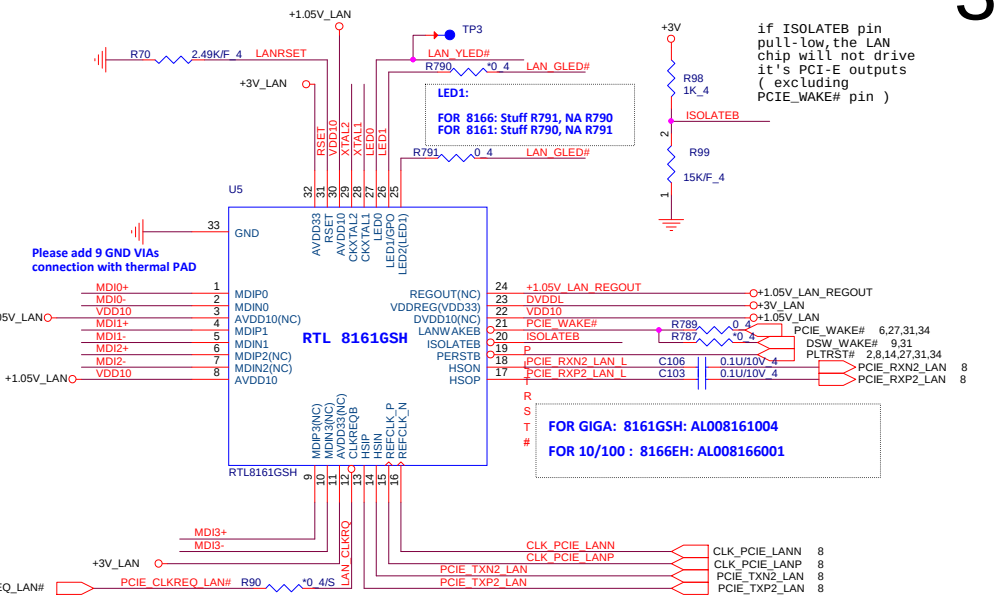
* Place Cc and Cd close to each VDD33 pin-- 23



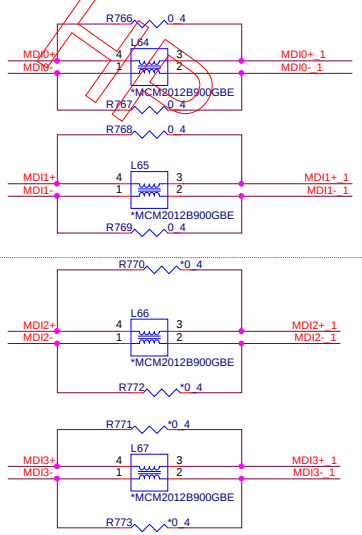
For GIGA
Stuff Cc ,Cd

For 10/100
NA: Cc, Cd

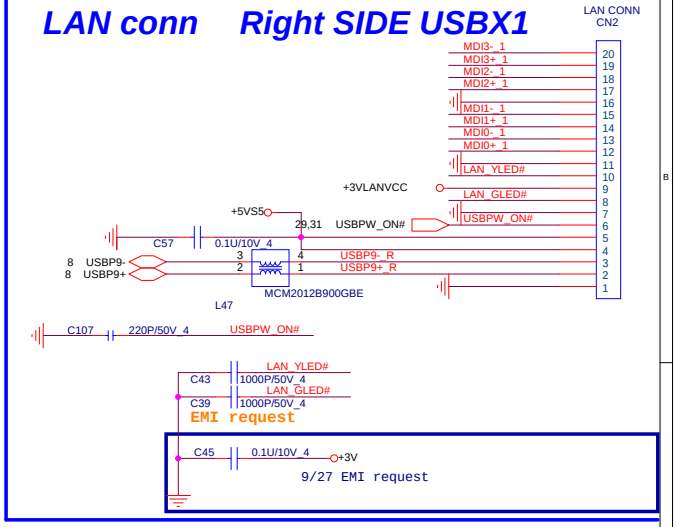
Remove For Not Using SWR mode



For 10/100 only



LAN conn Right SIDE USBX1



For GiGA

BOT:GST5009B LF,DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

For 10/100

BOT: TST1284R LF DB0EL5LAN00

FCE :NS892408 ,DB0EF7LAN01

2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,31,32,33,34,39,40,42,44 +3V
11,39 +3VLANVCC

NB5	PROJECT : R63 Quanta Computer Inc.	
Size Custom	Document Number RTL 8105E/RJ45	Rev 1A
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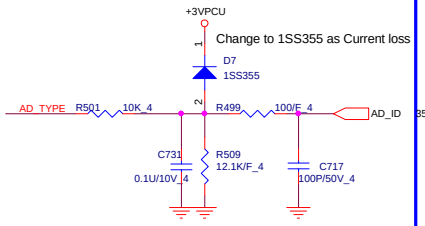
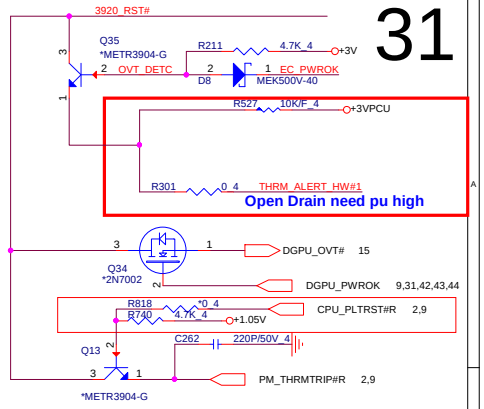
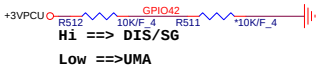
adapter Type check





adapter select for EC

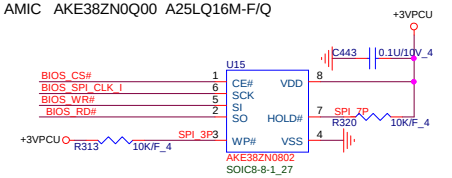


2M byte SPI EC ROM

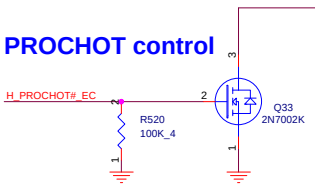
Socket: DFHS08FS023

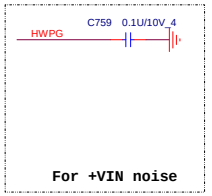
EON AKE38ZN0802 EN25QH16-104HIP

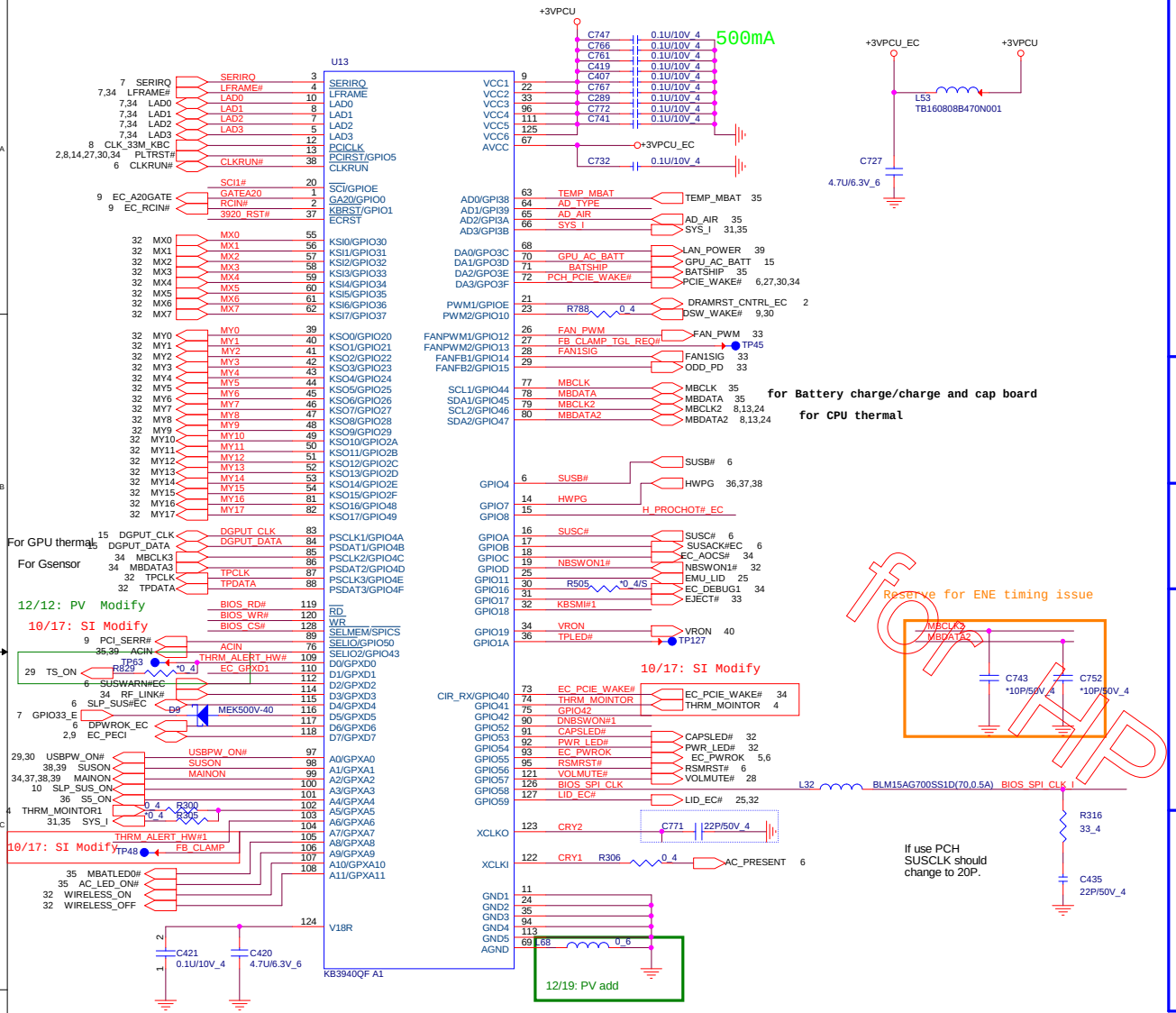
AMIC AKE38ZN0Q00 A25LQ16M-F/Q

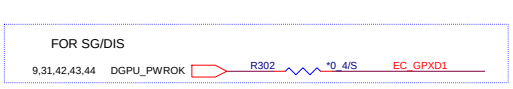


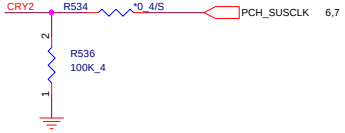
PROCHOT control

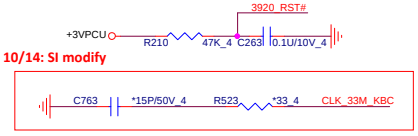


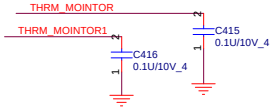


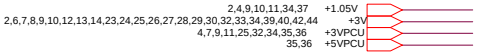












NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3940 A1)/ROM	1A
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KEYBOARD Con.

31 MY[0..17] MY[0..17]
31 MX[0..7] MX[0..7]

KB CONN 50698-03201-001-32p-l
DFFC32FR035
CN6

SATA_LED

C902 *AVLC 5S
7 SATA_LED# SATA_LED#
8 ACC_LED# SATA_R_LED1
R734 39_6 +3V
LED2 LED 3P WHITE/AMBER
R733 200/F_6
(Amber)
C899 *AVLC 5S

KEYBOARD PULL-UP

RP2 *10P8R-8.2K
RP1 *10P8R-8.2K
R173 *8.2K_4 MY16
R176 *8.2K_4 MY17

MY5 C109 *220P/50V_4
MY6 C142 *220P/50V_4
MY3 C145 *220P/50V_4
MY7 C140 *220P/50V_4
MY8 C141 *220P/50V_4
MY9 C76 *220P/50V_4
MY10 C173 *220P/50V_4
MY11 C169 *220P/50V_4
MY1 C128 *220P/50V_4
MY2 C136 *220P/50V_4
MY4 C139 *220P/50V_4
MY0 C96 *220P/50V_4
MX4 C82 *220P/50V_4
MX6 C73 *220P/50V_4
MX3 C104 *220P/50V_4
MX2 C97 *220P/50V_4
MX7 C67 *220P/50V_4
MX0 C133 *220P/50V_4
MX5 C90 *220P/50V_4
MX1 C61 *220P/50V_4
MY12 C149 *220P/50V_4
MY13 C152 *220P/50V_4
MY14 C156 *220P/50V_4
MY15 C190 *220P/50V_4
MY16 C201 *220P/50V_4
MY17 C206 *220P/50V_4

31 CAPSLED# R185 200/F_6 CAPSLED#_R
R191 200/F_6 MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R

28 MUTE_LED_CNTL Q6 2N7002K
R147 10K/F_4

SI, add Mute LED feature

EC KB3930 has included K/B pull-up resistor and function

9/15 SI for H/W.

R196 1K/F_4
R777 *200/F_6
R195 *200/F_6
Q10 DRC5144E0L
31 WIRELESS_ON
WIRELESS_ON_R

R199 1K/F_4
R208 *200/F_6
Q9 DRC5144E0L
31 WIRELESS_OFF
WIRELESS_OFF_R

PWR_LED

12/20 PV modify

R440 39_6
LED1 3P WHITE LED
C601 *AVLC 5S DEEP_PWRLED#
C607 1000P/50V_4 SATA_LED#
C604 1000P/50V_4 DEEP_PWRLED#

POWER BOTTON CONNECT

100mA

C116 *4.7U/6.3V_6
C114 1U/10V_4
C113 0.1U/10V_4
CN4
25,31 LID_EC#
31 NBSWON1#
31,32 PWR_LED#
R116 *0_4
DEEP_PWRLED# R117 *0_4/S
PWR BTN CONN
DFFC06MR001
88513-0601-6P-L-SMT

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

C110 PWR_LED# *0.1U/10V_4
C112 LID_EC# 0.1U/10V_4
C111 NBSWON1# 0.1U/10V_4

+3VPCU
R120 10K/F_4
Q5 DRC5144E0L
31,32 PWR_LED#
C135 0.1U/10V_4
DEEP_PWRLED#
for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.

+3VSUS R318 4.7K_4 TP_SMB_CLK
R323 4.7K_4 TP_SMB_DATA

change to +3VSUS
close conn

R304 4.7K_4 TPCLK
R303 4.7K_4 TPDATA

88513-0601-6P-L-SMT
DFFC06MR001
PWR BTN CONN
C429 10P/50V_4
31 TPCLK L34 TB160808B470N001
31 TPDATA L33 TB160808B470N001
C428 10P/50V_4
TPCLK-1
TPDATA-1
TP_SMB_DATA
TP_SMB_CLK
CN7

25 mils

C430 0.1U/10V_4

+3VSUS
Q19 *2N7002DW
TP_SMB_CLK SMB_PCH_CLK 8
TP_SMB_DATA SMB_PCH_DAT 8

PV , HP request Image sensor
SMBUS reserve to PCH

4,7,9,11,25,31,34,35,36 +3VPCU
7,23,26,28,29,33,34,39 +5V
39 +3VSUS
2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,33,34,39,40,42,44 +3V

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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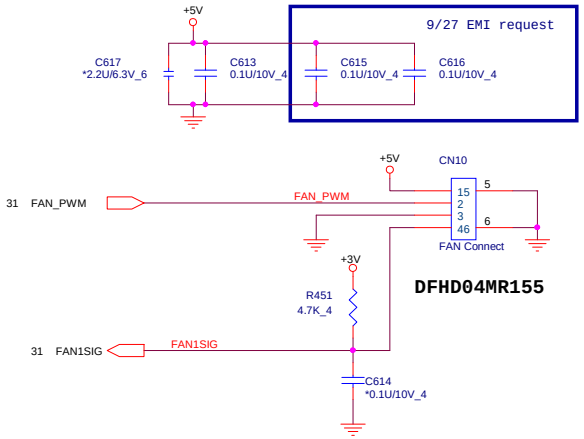
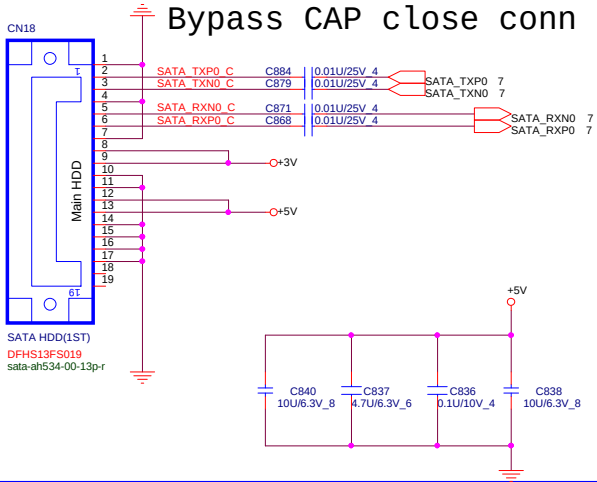
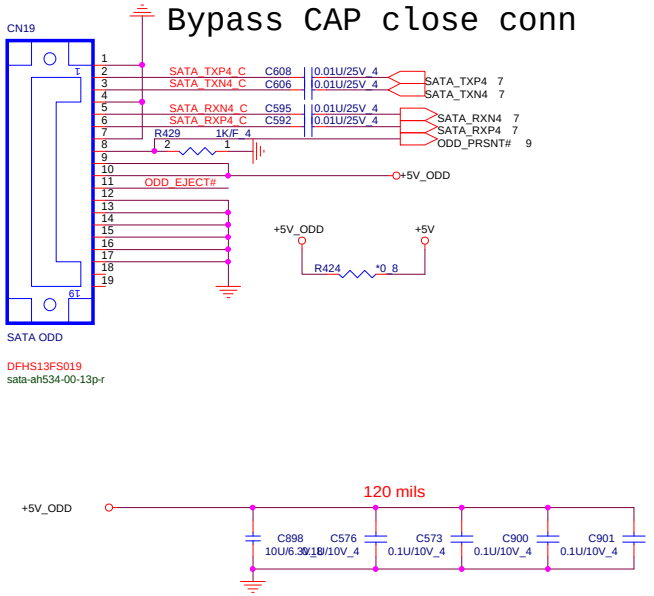
CPU FAN



SATA HDD CONNECTOR

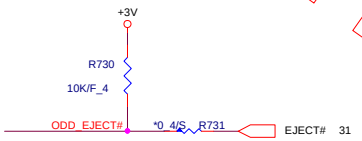


SATA ODD CONNECTOR

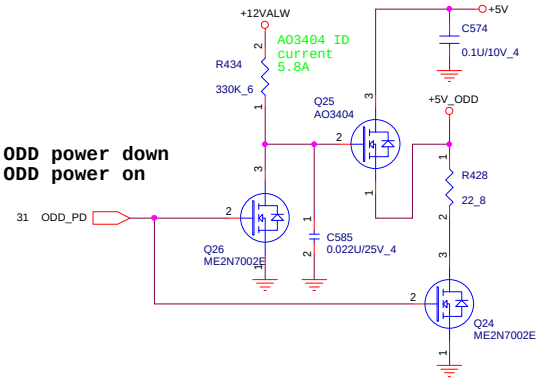


for HP

follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,34,39,40,42,44 +3V
4,7,9,11,25,31,32,34,35,36 +3VPCU
7,23,26,28,29,32,34,39 +5V
35,39,44 +12VALW

NB5

PROJECT : R63
Quanta Computer Inc.

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Mini PCI-E Card 1
WLAN

7,9 BT_OFF# D6 MEK500V-40

7/26 DB modify

+3V_AOAC R465 4.7K_4 FOR KBC DEBUG

+5V R463 *0_6 +MINIEC_5V

EC debug pin

31 EC_DEBUG1

CN13

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	LED_WPAN#	46
43	Reserved	LED_WLAN#	44
41	Reserved	LED_WWAN#	42
39	Reserved	GND	40
37	Reserved	USB_D+	38
35	Reserved	USB_D-	36
33	GND	GND	34
31	PETp0	SMB_DATA	32
29	PETn0	SMB_CLK	30
27	GND	+1.5V	28
25	GND	GND	26
23	PERp0	+3.3Vaux	24
21	PERn0	PERST#	22
19	GND	W_DISABLE#	20
17	Reserved	GND	18
15	Reserved	Reserved	16
13	GND	Reserved	14
11	REFCLK+	Reserved	12
9	REFCLK-	Reserved	10
7	GND	Reserved	8
5	CLKREQ#	Reserved	6
3	BT_CHCLK	+1.5V	4
1	BT_DATA	GND	2
	WAKE#	+3.3V	

MINI PCIE H=11
DFHS52FR097
MIPCI-C-1759513-52P-LDV-SMT

8 PCIE_TXP1 PCIE_TXP1
8 PCIE_TXN1 PCIE_TXN1
8 PCIE_RXP1 PCIE_RXP1
8 PCIE_RXN1 PCIE_RXN1
8 CLK_33M_DEBUG
PLTRST#
8 CLK_PCIE_WLAN CLK_PCIE_WLAN
8 CLK_PCIE_WLAN# CLK_PCIE_WLAN#
8 PCIE_CLKREQ_WLAN# R461 *0_4 BT_COMBO_EN_R#
8 BT_COMBO_EN#
MINICAR_PME#

BT_DATA,BT_CHCLK,CLKREQ#
internal pull-DOWN 100k
ohm

+3V_AOAC
+1.5V

7/26 DB modify
R96 *4.7K_4 +3V_AOAC
R111 0_4 RF_LINK#
MINI_BLED
RF_LINK#
10/12: SI reserve
R801 0_4 RF_LINK# 31
R97 4.7K_4 +3V_AOAC
7/26 DB modify
USBP10+ 8
USBP10- 8

10/12: SI reserve
R802 0_4
PLTRST# 2,8,14,27,30,31
RF_OFF# 9

INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm

LAD0 LAD0 7,31
LAD1 LAD1 7,31
LAD2 LAD2 7,31
LAD3 LAD3 7,31
LFRAME# LFRAME# 7,31

C126 0.01U/16V_4
C129 0.1U/10V_4
C132 10U/6.3VS_6

R473 0_8 +3V
+3V_AOAC
C86 0.1U/10V_4
C632 0.1U/10V_4
C639 0.1U/10V_4
C638 10U/6.3VS_6

+3V_AOAC
6,27,30,31 PCIE_WAKE#
*DRC5144E0L Q31
MINICAR_PME#

+3V_AOAC
R474 *10K/F_4
31 EC_PCIE_WAKE#
*DRC5144E0L Q30

12/21: PV modify

CLK_33M_DEBUG R84 *51_4 C78 *15P/50V_4

10/14: SI for EMI request

Reserve for AOAC function

+3VPCU +3VS5 +3V_AOAC
R68 *10K/F_4
C935 *0.022U/25V_4
R456 *100K/F_4
Q28 *ME2303T1
24mil
Q27 *ME2N7002E
+3V_AOAC
C81 *10U/6.3V_8
C87 *.1U/10V_4
8 PCH_AOCS# R457 *0_4
31 EC_AOCS# R458 *0_4
Q68 *2N7002E
31,37,38,39 MAINON

6,7,8,10,28,34,38,44 +1.5V
2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
4,7,9,11,25,31,32,35,36 +3VPCU
7,23,26,28,29,32,33,39 +5V
2,6,7,9,10,36,38,39,42,44 +3VS5

Accelerometer Sensor

R245 *0_6/S +3V
R225 *0_6 +3V_AOAC
+G_SEN_PW
U10
HP3DC2TR
C319 0.1U/10V_4
C308 0.1U/10V_4
Vdd_IO
VDD
NC
NC
8 ACCEL_INTH#
D10 MEK500V-40
ACCEL_INTH#1
TP22
INT1
INT2
RESERVED
RESERVED
RESERVED
RESERVED
R224 *0_4/S
31 MBDATA3
31 MBCLK3
SDO
SDA
SCL
GND
GND
+G_SEN_PW R221 *0_4/S
CS
AL003DC2A00

+G_SEN_PW R496 4.7K_4 R497 4.7K_4
ACCEL_INTH#1
MBDATA3 C323 33P/50V_4
MBCLK3 C322 *33P/50V_4
C288 22P/50V_4

9/27 EMI request

+3VS5
+3V
C524 0.1U/10V_4
C640 0.1U/10V_4
C522 0.1U/10V_4
C641 0.1U/10V_4
C625 0.1U/10V_4
C83 0.1U/10V_4
C84 0.1U/10V_4
C630 0.1U/10V_4
C626 0.1U/10V_4
C527 0.1U/10V_4
C636 0.1U/10V_4
C637 0.1U/10V_4
C627 0.1U/10V_4
C629 0.1U/10V_4

SI for +VIN noise issue

+5VS5
EC4 0.01U/50V_4
EC2 0.01U/50V_4
EC3 0.01U/50V_4
EC5 0.01U/50V_4
+VIN
+3V
EC18 0.01U/50V_4
EC1 0.01U/50V_4
EC13 0.01U/50V_4

EC23
10.14: SI modify.
+5VS5
+VIN
*0.01U/25V_4 EC24
*0.01U/25V_4 EC25
*0.01U/25V_4 EC26
*0.01U/25V_4
EC28
*0.01U/25V_4 EC29
*0.01U/25V_4
+3VPCU
C446 *0.1U/10V_4
+5V
C49 0.1U/10V_4
C48 0.1U/10V_4
+5VS5
C475 0.1U/10V_4
C480 0.1U/10V_4
+VGA_CORE
C406 0.1U/10V_4

+5V EC7 0.01U/50V_4 +3V
+3V EC22 0.01U/50V_4 +1.5V_VGA
+5V EC6 0.01U/50V_4 +5VS5
+1.05V EC9 0.01U/50V_4 +5VS5
+3V EC8 0.01U/50V_4 +1.05V

2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
32,39 +3VSUS
6,7,8,10,28,34,38,44 +1.5V
23,29,30,36,37,38,39,40,41,42,43,44 +5VS5

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN & G-sensor	1A
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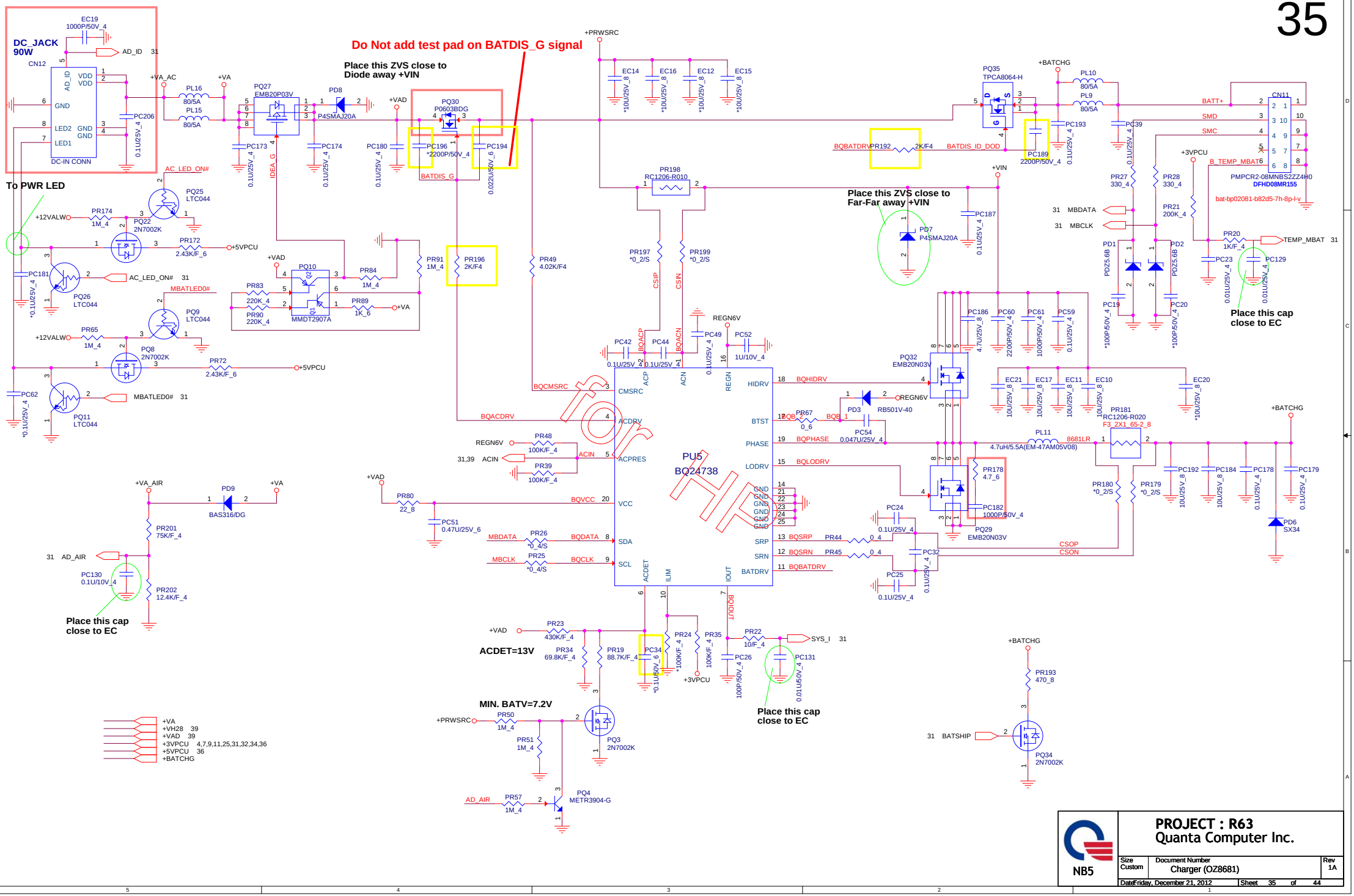
DC_JACK 90W
DC-IN CONN
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
ACDET=13V
MIN. BATV=7.2V
PU5 BQ24738
+PRWSRC
+BATCHG
+VIN
+VA
+VAD
+5VPCU
+3VPCU
+12VALW
REGN6V
SYS_I 31
BATSHIP 31
AD_AIR 31
AC_LED_ON# 31
MBATLED0# 31
MBDATA 31
MBCLK 31
TEMP_MBAT 31
ACIN 31,39
+VA 39
+VH28 39
+VAD 39
+3VPCU 4,7,9,11,25,31,32,34,36
+5VPCU 36
+BATCHG
NB5
PROJECT : R63
Quanta Computer Inc.
Size Custom
Document Number Charger (OZ8681)
Rev 1A
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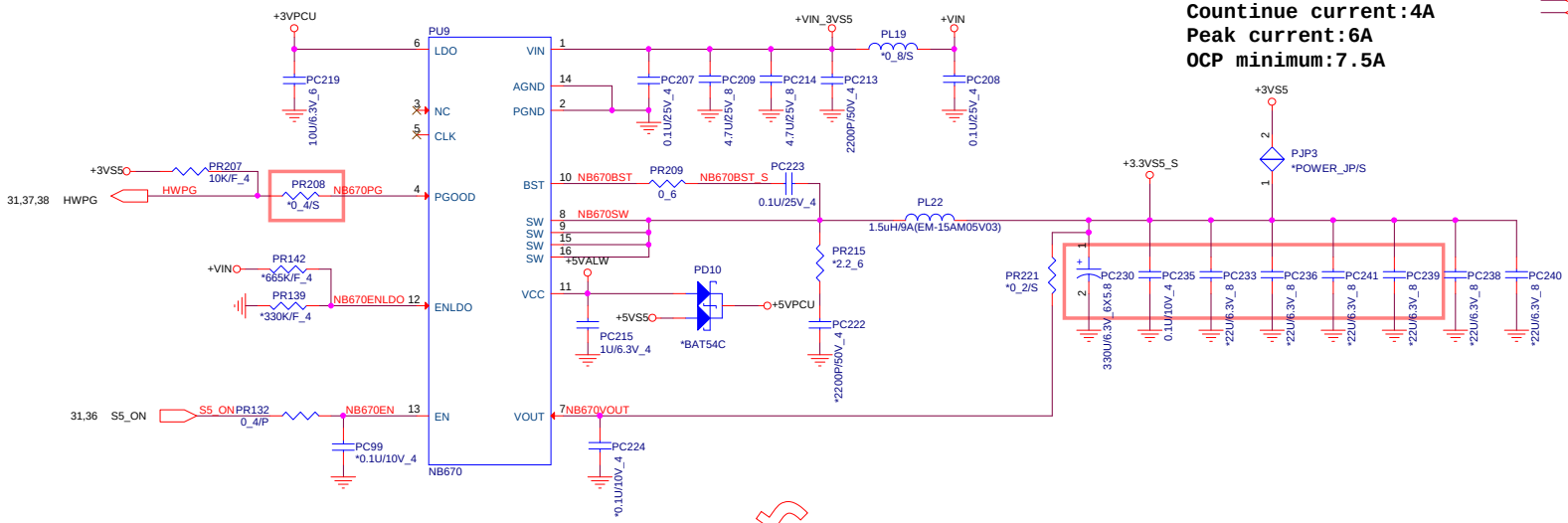
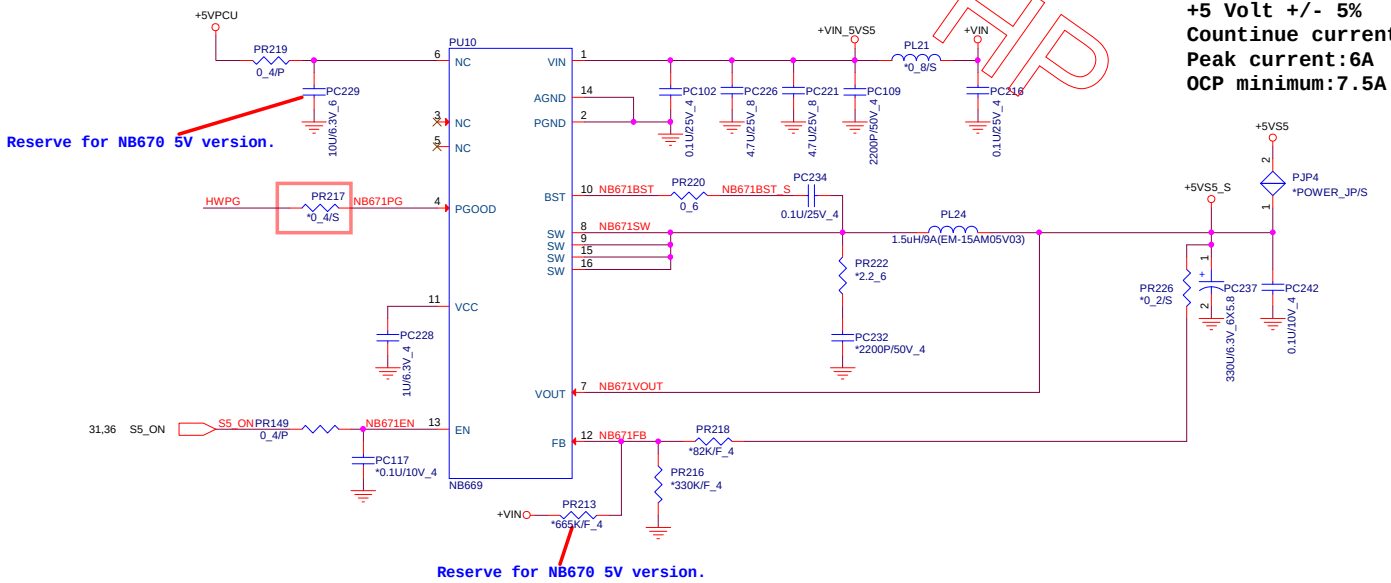
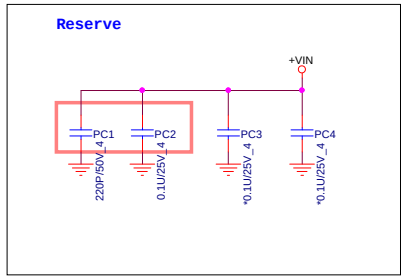




for HP



NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VPCU(RT8243A)	Rev: 1A
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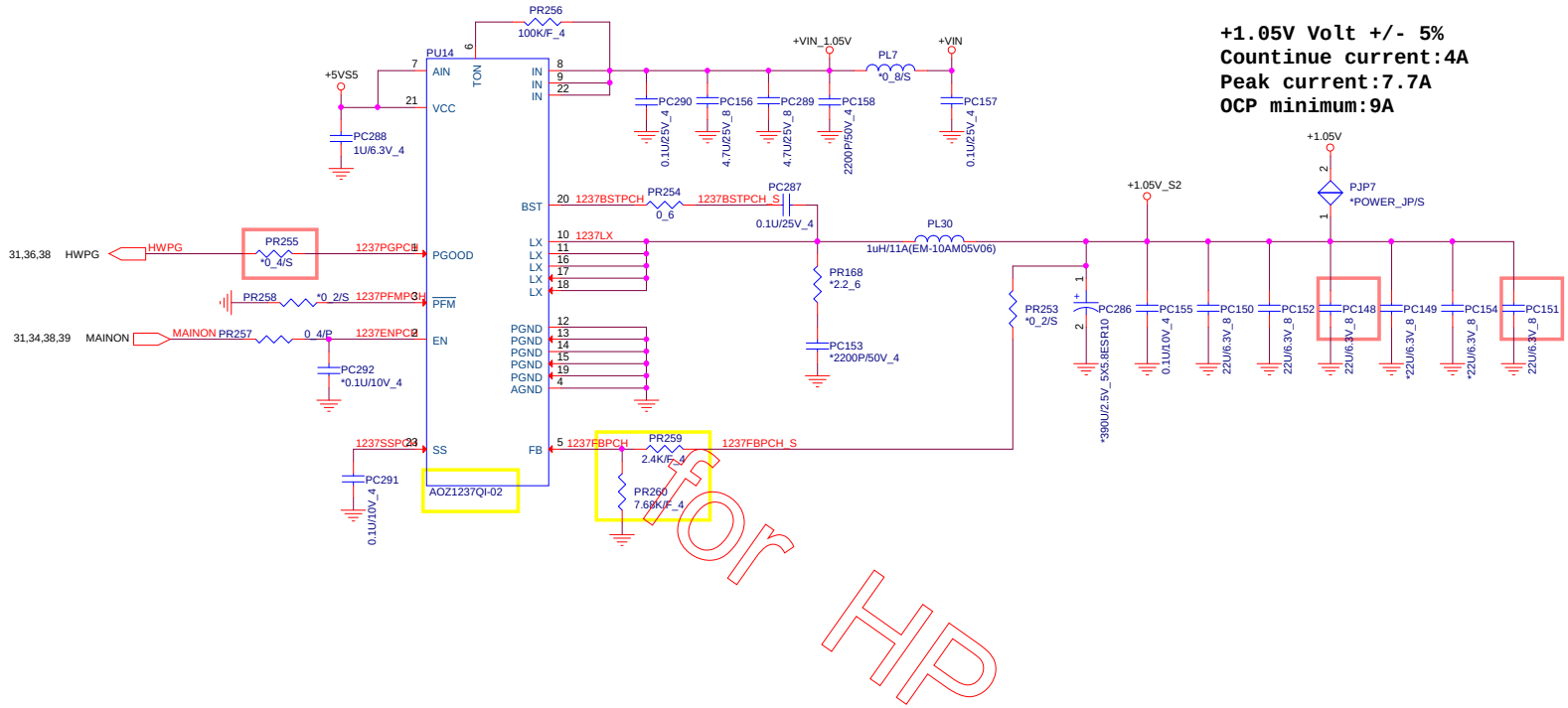

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: 1.05V(RT8228BZ)	Rev: 1A
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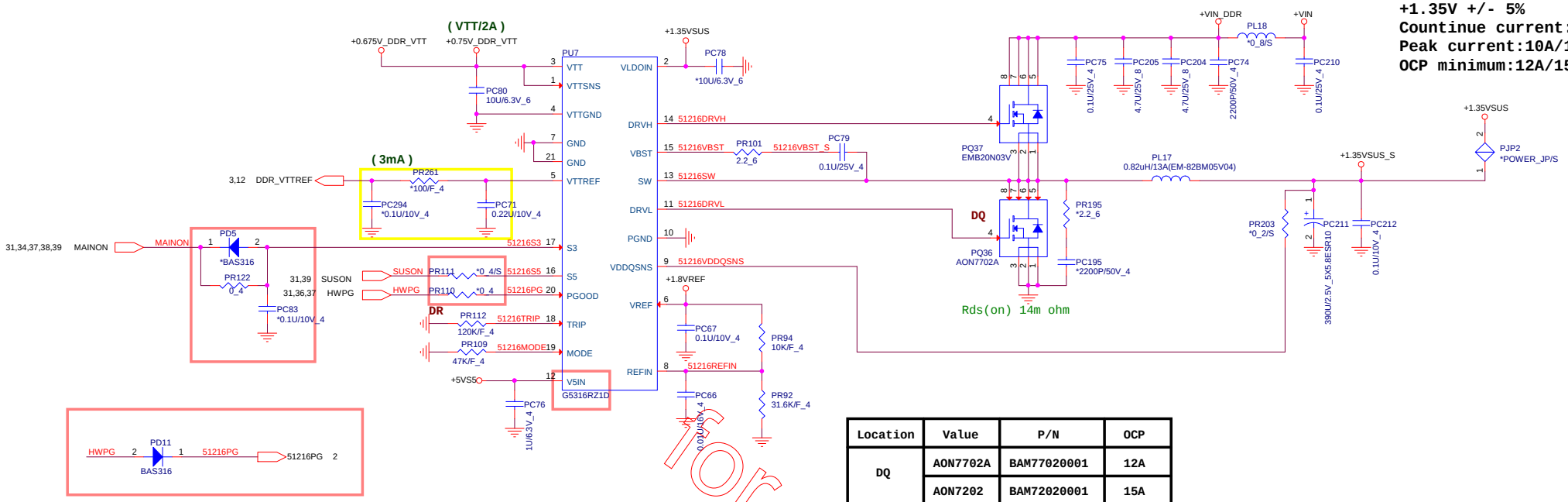
+1.35VSUS 2,3,4,12,13
+1.5V 6,7,8,10,28,34,44

+1.35V +/- 5%
Countinue current:6A/8A
Peak current:10A/12A
OCP minimum:12A/15A

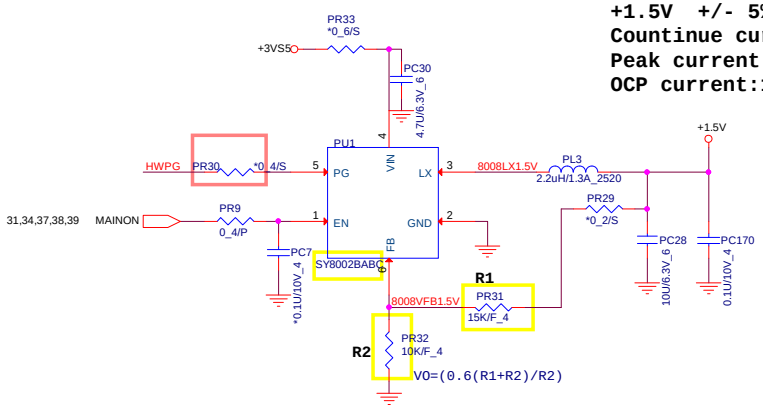


HWPG 2 PD11 1 51216PG → 51216PG 2
BAS316

Location	Value	P/N	OCP
DQ	AON7702A	BAM77020001	12A
	AON7202	BAM72020001	15A

Location	Value	P/N	OCP
DR	120K	CS41202FB17	12A
	76.8K	CS37682FB00	15A

+1.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A
OCP current:1.2A



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L(APW8819)	1A
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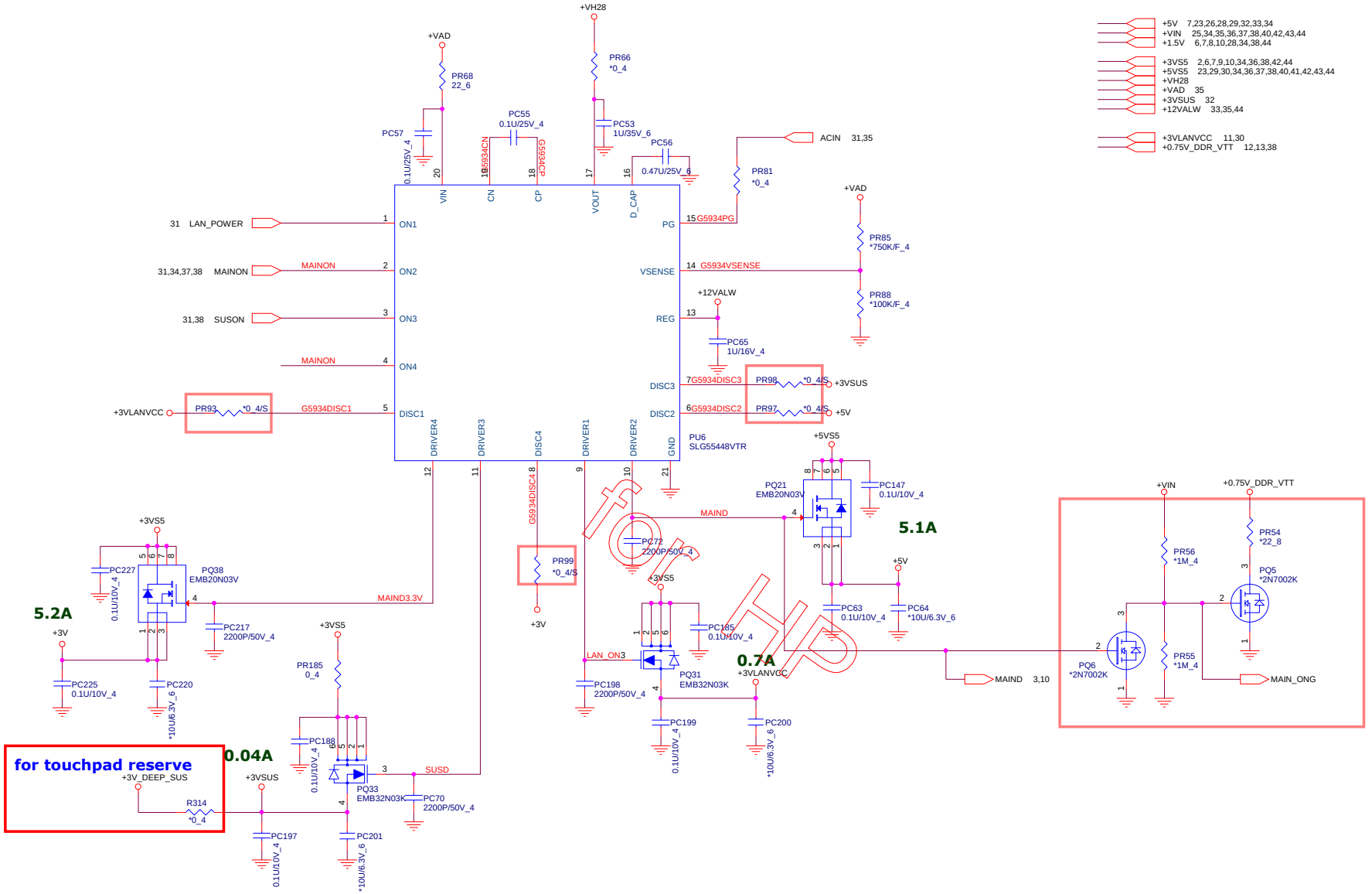

NB5	PROJECT : R63 Quanta Computer Inc.		
	Size: Custom	Document Number: Dis-charge IC (G5934)	Rev: 1A
	Date: Friday, December 21, 2012	Sheet 39 of 44	

CPU	Re	PR18
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14

PUT COLSE TO VCORE Phase 1 Inductor

Dummy Rc For 2 phase

Rc

Dummy Ra and Ca For 2 phase

Ca

Ra

Rb

POP Rb for 2 phase

CPU	Rd	PR14
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16

Re

Rd

SV 37W CPU
VID1=1.8V
IccMax=55A
Icc_Dyn=35A
Icc_TDC=26A
R_LL=1.5m ohm
OCP~60A

CPU	Ra	Ca	Rb	Rc	Rd	Re		
37W	Dummy	Dummy	POP	Dummy	CS34322FB00	CS29092FB27	CH733RY8802	Dummy Page 41
47W	POP	POP	Dummy	POP	CS36652FB16	CS31472FB14	CH756RM8802	POP Page 41
R63 Location	PR10	PC6	PR4	PR8	PR14	PR18	PC128	

PUT COLSE TO VCORE HOT SPOT

For 37W CPU ; PC128 Placed 330uF_9 mohm
For 47W CPU ; PC128 Placed 560uF_4.5 mohm

CPU	PC128
37W	CH733RY8802
47W	CH756RM8802

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NB5

Size: Custom | Document Number: CPUCORE (NCP81103) | Rev: 1A
Date: Friday, December 21, 2012 | Sheet 40 of 44

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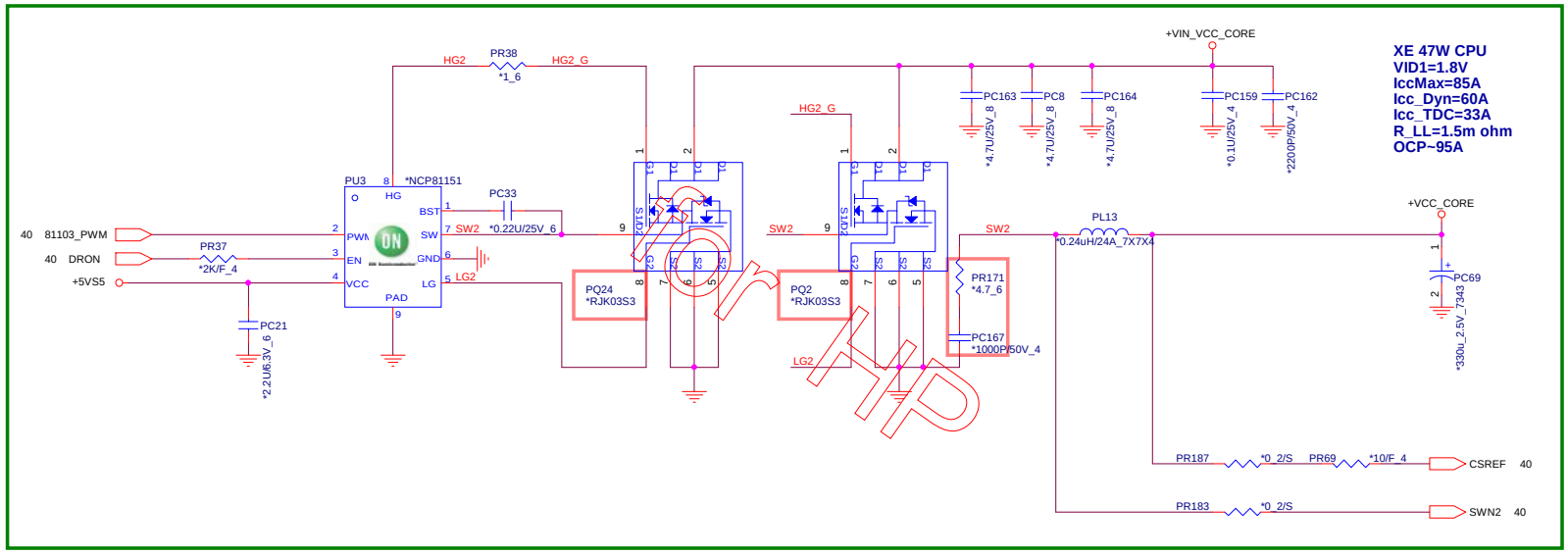

For 37W CPU
Dummy these components

+VCC_CORE 4,40

NB5

PROJECT : R63
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Size	Document Number	Rev
Custom	NCP81151	1A

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VGA Core

+VGA_CORE 18,34,44

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V Default
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

GPIO12 GPIO16 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE
0	1	0	1.0V Default
1	0	0	0.9V
1	0	1	0.875V

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L=0mV/A

DCR_1.4m ohm

DCR_1.4m ohm

PU8
NCP3218G

This NTC Close to Phase 1 MOSFET

Close to Phase 1 Inductor

Shortest the net trace

for ref

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NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE NCP3218G)	Rev: 1A
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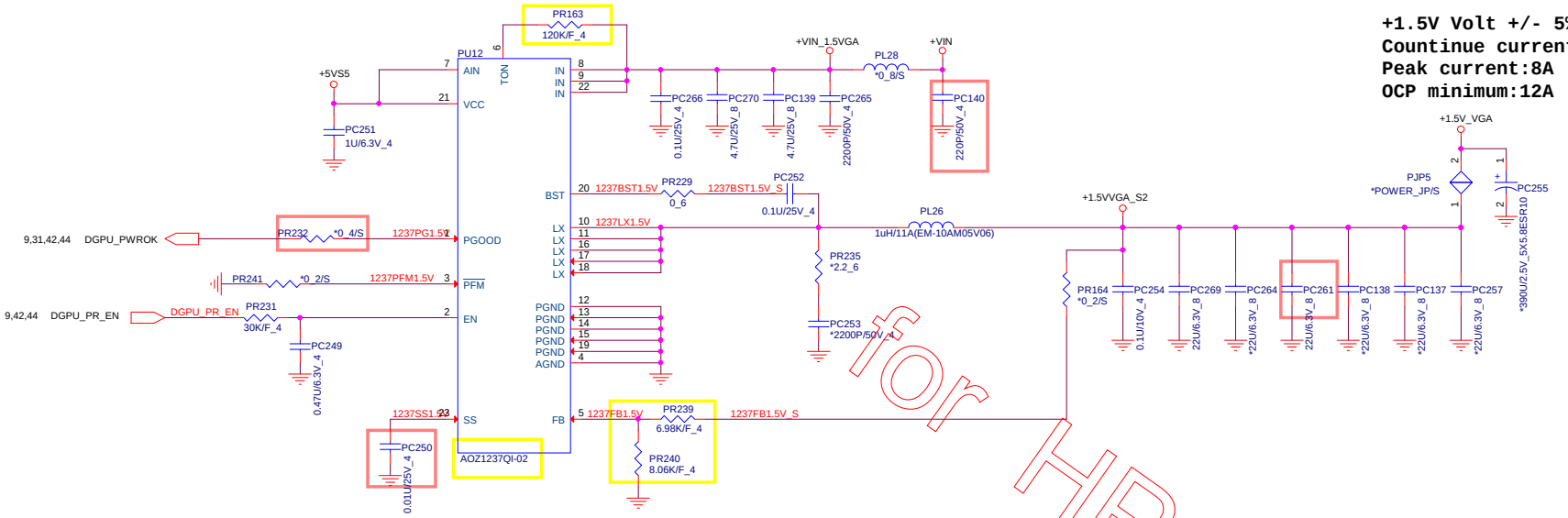
+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



for HP

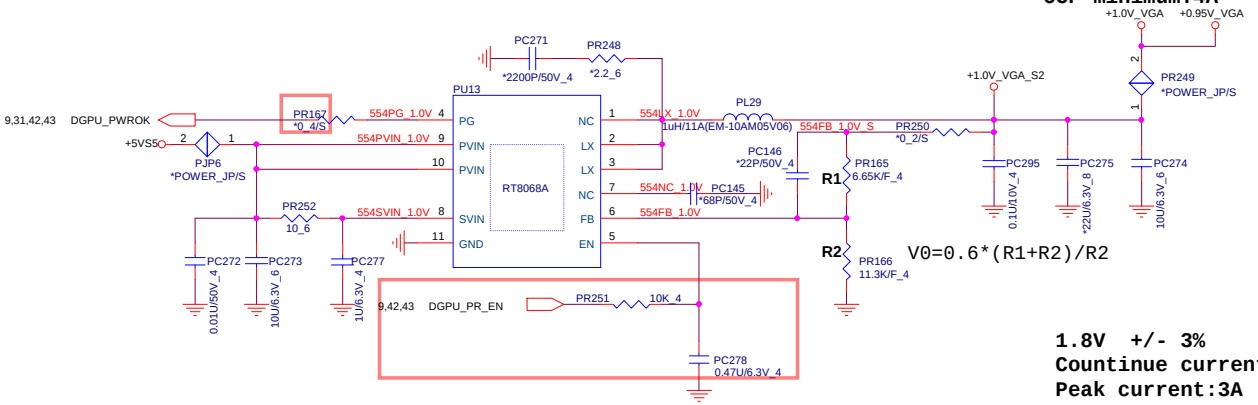
NB5

PROJECT : R63
Quanta Computer Inc.

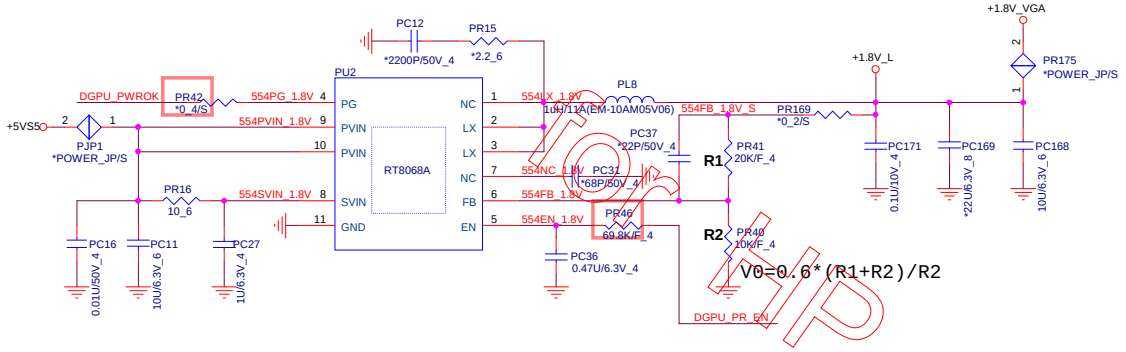
Size	Document Number	Rev
Custom	**+VGA POWER**	A
Date: Friday, December 21, 2012	Sheet 43 of 44	

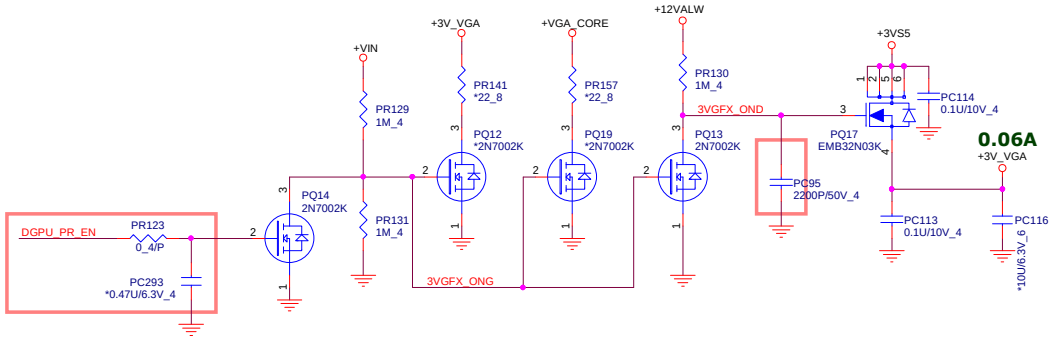
VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

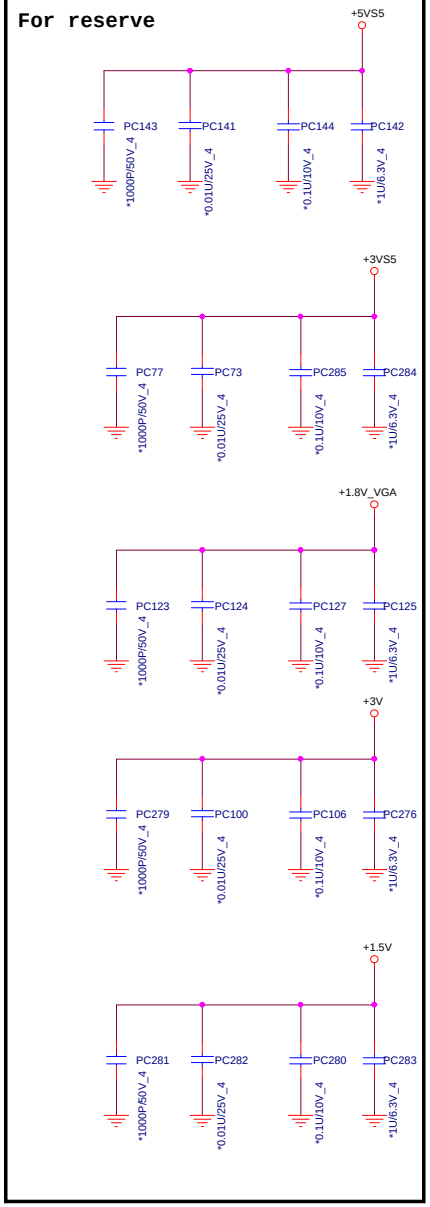


1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A





For reserve



+1.8V_VGA 11,15,16,18,19
+1.0V_VGA 14,16,18,19
+3V_VGA 14,18

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A
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