MODEL: RT2

REV	DATE	CHANGE LIST
3B	2001/05/29	**C2 Test (PCB P/N: DA0RT2MBAD1)** 31. To Decrease volume of PC Beep, Page25: Change R319 to 22K, R312 to 680 Page26: Change R288 to 22K, R303 to 680 32. Page47: For machenism interference, change C509, C510 to no-loading; C511,C512 to 270U. 33. Page14: For USB signals quality, change C415, C366, C391, C386, C429, C421 to no-loading. 34.Page15: Add 2'nd source for eeprom of Lan 35.Page8: Pull-up & pull-down already built in GMCH, so change R242, R38-40, R46-49, R52, R53, R60, R62-67, R72, R73 to no-loading. 36. Page42: Change spring to FDRT1010019(5mm): PAD100, PAD102, PAD106-108, 110-112.
3C	2001/06/20	**Ramp (PCB P/N: DA0RT2MBAE0)** 1.Page12: For ICH3 (B0 stepping, QB62), change R547 to 18.2_1%. 2.Page42: Hole1, Hole2 are NPTH, so change pin1 to NC. 3.Page34: To awake EC, change D32.2 to <SUSB#> from <SUSA#>. 4.Page17: Add discharge circuits for CD_VCC: Q116, R676. 5.Page44: Change PC69, PC71 footprint to TC1206. 6.Page22: Change Q48 to 2N7002. 7.Page14: Change R20 to 0805 for USB GND. 8.Page46: To avoid interference with Lan cable, move PFL2 to TOP side. 9. For EMI, Page27: Change C858, C860 to 180P. Page42: Load PAD107, PAD29, PAD37. Change PAD110 to no-loading. Change PAD37 to FDSS2002019. 10.Page15: For lan, change R385 to 124_1%. Reserve C967,C757. Add 2'nd source for U59:ATP119(this config can pass the lan test in intel lab). Change C968,C969 to 1000P_2KV_1206(footprint is compatible with 1808 size). 11. Change U47(ATI M6-P) P/N to AJAFA120T03 for TOP. 12.Page16: Change CON18(HDD conn) to DFHS44FR096. 13.Page12: Change RTC cap: C797, C796 to 15P. 14.Page36: To avoid mechanism interference, change CON15(stick conn) to 5.5mm(ACS). 15.Page30: To avoid conflict with wireless card, change R318.2 (USB_DISCONN) to CON24.4; R622.2 (USB_RESET) to CON24.6 16.Page22: Change C483 from 10U/25V_4532 to 10U/25V_1210. 17. For ESD, Page42: Change Hole1 to <GND_DC1> and connected gnd by R678, R680. Change Hole2, PAD100 to <GND_DC2> and connected gnd by R677, R679. Page41: Change CON5.243,244 to NC from GND. 18. Change PCB to DA0RT2MBAE0, Rev E.
	2001/06/22	19.Page47: Change D5 footprint to DSMA. 20.Page8: Because of external graphic, pull down <DREF_CLK>: delete C963, change R666 to 10K. 21.Page26: Change R165 to 0603; add R681, but reserved. 22.Page41: U5,U6,U7 cghange foot print to APIC16861-RT2. 23.Page42: Change PAD37 to FDSS2002019 to avoid interference.
	2001/06/28	24.Page8: Reserve R666.
	2001/07/04	25.Page45: Deeper sleep voltage change to 0.85V, so reserve R12,R170,R219; change R220, R169, R13 to loading.
	2001/07/10	26. Add jumper wire(AWG26) to connect PQ43 pin3 and L124 pin2 on PCB top side, to avoid VGA core power <+1.8V_VGA> drop down.

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11	1A		43	1A	2A
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13	1A		45	1A	
14	1A	2A	46	1A	2A
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PROJECT : RT2.0
Quanta Computer Inc.

Project : RT2 MB	MB Assy' P/N: 31RT2MBAB5	Document No.: 204	Rev: 3C	Cover Sheet: 6 of 6
Project Manager : Jacky Lee	Project Leader : T.S. Wan	Drawing by : Allan Yu	Approved by : Jacky Lee	

MODEL: RT2

REV	DATE	CHANGE LIST
3B	2001/04/25	**C2 Test (PCB P/N: DA0RT2MBAD1)** 6. Page12: Move R600, C874, R609 close to ICH3. 7. Page28: To avoid floating, add pull-up R669 at <PCICSPK>. 8. Page47: For machenism interference, exchange the parts loaded on C510-512 with C81-83. 9. Page44: Change PQ47 from <1.8V_S5> to <+1.8V>.
	2001/05/07	10. Page46: Reserved PAD101. 11. Page47: Delete R299. Change PU9.18 to GND. Delete <S0>, <S1>, R80, R81, R70, R68, R69, R77. 12. Page46: Add PC101 470P, PC102 1000P for EMI. 13. Page15: For LAN performance, (1) Delete L101-L104, short directly. (2) Delete <GND_LAN>, R407. (3) C745, C730 change to GND. (4) Change R376 to 0805. (5) Add LAN termination plane <GND_LAN_TERM >. Add C967-C969 1000P. (6) Change U59 to Pulse H0022.
	2001/05/09	14. Page44: Delete PR71, PR75 short directly. Change PC82 to 1U_0805. 15. To avoid ICH3 SM bus leakage, Page37: Change U21 to FST 3253. Page12: Change R454, R445 to <3V_S5> from <+3V>. Page3: Add Q114, Q115, R671, R672, R673. 16. Page44: Delete PFL3, short directly. Delete PD27 and PD24. Change PR72 to 240K, PC95 to 220P, PR80 to 20K_1%, PR74 to 200K. 17. Page42: Delete PAD103, 104, 105. 18. Page15: For LAN, add R674, R675 0_0805. 19. Page28: Add C970, C971 0.1u_0402 at L100.
	2001/05/10	20. Page15: Change R397 to BK2125HM121. Change CON23.15 to GND. 21. Page42: Delete PAD13, PAD32, PAD38.
	2001/05/15	22. Page23: Change the trace width or CRT RGB to 4 mil from 10 mil to approach the recommended impedance 75 ohm. 23. Page15: Add C972, C973 by intel recommendation for LAN.
	2001/05/17	24. For EMI Page18: Add C974, L134. Page24: Add C975, C976. Page46: Change PL6, PL10 to FBMJ3216HS800-T. Page47: Add L135 FBMJ3216HS800-T. Page23: Delete TV_GND, change to GND. Delete R144. 25. To reduce Audio noise, Page41: Change CON5.182 to AUDGND from GND. Page26: Change Q62, Q60, C610, C64 to AUDGND. Page30: Delete C65. Page22: Delete C399-C403, C53, C464. Page26,27: Change footprint of CON20,CON19,CON22. Delete R525, R550, R521, R523, R158, R568. Page25: Delete R314, R313.
	2001/05/18	26. To Add regulator for VGA PLL power, Page24: Delete C149, C121, C79. Add U89, C988, C985, C986, C989, C987, C978, C984, C982. 27. To fix VAUXPCIC leakage under Suspend to Disk, Page12: Add U87(NC7SZ32), C977, <SUSCLK_ICH>. 28. Page42: For ICT test tool, change HOLE4,20,15,21,16 to NPTH.
	2001/05/19	29. Page23: Move C8 from TOP to BOT.
	2001/05/24	30. BOM changes: Page42: PAD109 no loading; Page18: Y1 change part to BG627000106; Page3: Update U24 to rev E; Page23: Change CON12 to Yellow, and C803,C804,C808,C809,C811,C812 to 82P, and L34-36 to 1.8UH; Page27: Change CON19 to Blue, CON20 to Pink; Page36: Change CON15 to vendor ACES; Page38: Change CON28 to vendor ACES; Page15: Change U59 from H0022 to H0029 (it's same as the former but lower cost for asia market). Page6: Change U17 to new ver, QC32.

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PROJECT : RT2.0
Quanta Computer Inc.

Project : RT2 MB	MB Assy' P/N: 31RT2MBAB5	Document No.: 204	Rev: 3C	Cover Sheet: 5 of 6
Project Manager : Jacky Lee	Project Leader : T.S. Wan	Drawing by : Allan Yu	Approved by : Jacky Lee	

MODEL: RT2

REV	DATE	CHANGE LIST
3A	2001/04/02	48. Page35: For interference, change U58 to NC7SZ58. 49. Page38: Change R614 to 680 ohm; CON28.1,R614 to be powered by +5V. 50. Page18: For ATI P6 D3 cold, add R659 to interconnect <PCIRST#> and P6. Change R518,Q80,U68,C841 to no-loading. 51. Page47: To interconnect pwrgood of MAX1718 and <HPWG> to EC, add D46, R660. 52. Page18: Change the gate of Q33,Q41 from <5VSUS> to <+5V>. 53. Page47: Change R299 to no-loading.
	2001/04/03	54. Page16: For<- HDDRESET>, change U83 to NAND(TC7SH00FU), add DTC144EU,10K to isolate different powers. 55. For ATI P6 D3 cold, delete <2.5VSUS>, Page44: Delete <2.5VSUS>, PQ48,PR77, change PQ46 to no load and nets. Add R661,R662(no load). Change the control of U16.11 to <MAINON> but option to <SUSON> by R662. Page24: Delete L131,<2.5VSUS>. 56. Page24: Add regulators for DAC powers of CRT & TVout. Add U85,U86,C949-958. Delete L21,L93,C133,C515. 57. Page24, 44 ATI P6 power source options about D3 cold and D3 hot:
	2001/04/09	58. To decrease volume of pc beep, Page26: Change R288 to 6.8K. Page25: Change R319 to 6.8K. 59. Page47: To fine tune CPU core voltage (VTT), change R89 to 1.82K_1%.
	2001/04/16	60. Page15: To improve Lan performance, change R385 to 110_1% from 100_1%, C757 to 1000P_2KV from 68P_2KV.
3B	2001/04/23	**C2 Test (PCB P/N: DA0RT2MBAD1)** 1. To fix wrong pins' definitions of ZV port buffer, Page29: swap net names between U56.3 and U56.9; U56.17 and U56.11. Page18: Change net name of U47.AA3 to <ZV_PCLK>. Page25: Change net name of U43.50 to <ZV_SCLK>. 2. For EMI, Page3: Add R668, R664 0 ohm to connect GND planes. Page6: Add R665, C960, but reserved. Page7: Add C961, C962, C965, C966. Page8: Add R666, C963, but reserved. Page12: Add R667, C964, but reserved. Change R475 to 22 ohm from 68; C817 to 5P from 15P.
	2001/04/24	3. Page44: Change PC96 to 10U/10V/TAN. 4. Page15: Change C757 to 1000P_X7R_4520_3KV for LAN. 5. Page29: Change C723 to 0603 from 0402. Page30: Change C733 to 0603 to 0402.

Power source option for ATI P6 power states selection		
ATI P6 power states	D3 cold	D3 hot
Control signals	MAINON	SUSON
Location	Components options	
R661 Q110 L133 L130 R659	Load	No load
R662 PQ46 L129 L22 U68 Q80 R518 C841	No load	Load

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MODEL: RT2

REV	DATE	CHANGE LIST
3A	2001/03/15	15. Page47: Delete R644.
	2001/03/16	16. Page44: Change PQ48 to SI4800DY for larger current rating. 17. Page16: Change Q102, Q103 to DTC144EU to fix the problem that high level driven by 3.3V is lower than <HDD_VCC>.
	2001/03/22	18. Page44: Change PU16 pin20, 21 to 5VPCU. 19. Page47: Change D3 to EC31QS03L. 20. For Intel recommended on GMCH QS stepping, Page6: Modify C430 and change value to 0.01U Page3: Add R649 240K at U24.24. 21. Change part 1U_0805 to 1U_0603: C59-62, C521, C463, C545, C462, C533, C564, C559, C625, C624. 22. Page11: Add R658 pull-up for <RC> but reserved. 23. Page7: Change <SM_CLK> layout for Intel design change. 24. Page39: Change U30 power to <+5VA>, add C941 to reduce noise of <BEEP>. 25. For audio noise, Page26: Change the power to <+5VA> and gnd to <AUDGND> for U12, Q47, C64, R54,R225, R256. Page41: CON5 pin1,2,61,62,183,65 to <AUDGND> from <GND>. Page27: Delete R292, R204, R269 and short the nets directly. Page26: Delete R232. 26. Page41: Change R27 to <AUDGND> from <GND>, CON5 pin243, 244 to <GND> from <CHASIS_DOCK_1>(chasis gnd).
	2001/03/28	27. To prevent <HDD_VCC> and <CD_VCC> from power down during <PCIRST#> acting in warm-boot, Page12: Delete the GPIO41, GPIO42 at U67(ICH3) pin G21, D23. Add <HDDVCC_EN> at pin W4(GPIO27), <CDVCC_EN> at pin Y3(GPIO28). Page16: Add <HDDVCC_EN>, R653, R654(reserved), and <HDDVCC_ON> from EC. Change Q106 to 2N7002E. Page17: Add <CDVCC_EN>, R655, R656(reserved), and <CDVCC_ON> from EC. Page35: Add <HDDVCC_ON>,<CDVCC_ON> at U82 pin2, 5, controlled by EC (reserved). 28. Page12: Add R652 pull-low <PWROK>. 29. For RTC leakage, implement the design changes from Intel(WW08), Page12: Add R652 pull-low <PWROK>. Add U84, C948, R651. The rest changes have been done. 30. Page12: Move the RTC short pad G2 near CON29 under ninipci door. 31. Page16: For <-HDRESET>, Add U83, C942; delete Q102,103105, R630, R632. 32. Page16: Add C943. Change R629 to 1M. 33. Page17: Change R143 to 1M. 34. Page11: Add R657 10K at <APICD1>. Change R510 to 10K. 35. Page12 Change R547 to 22.6_1% for uab bias. 36. Page 24: For ATI P6 D3 cold, Change L131,L129,L22 to no-loading; L132,L130,L133 to loading. 37. For EC to control RF ON or OFF, Page38: Add Q112, <RF_ON_OFF>. Page35: Add <RF_ON_OFF> at U78.19. 38. Page36: For FAN driving current, change R458 to 1K; D41to loading; C895 to 4700P for <FANSIG>. 39. To prevent interference from wireless card, Page30: Change C590,711,748 to 1U_0603. Page25: Change C552 to 1U_0603. Page28: Change C684 to 1U_0603. 40. Page46: To save power, change PR49,50,12,13 from 100K to 1M. 41. Page42: Add EMI Spring: PAD100-109. 42. Page5: Add C944-C947 for VTT. 43. For interference, move Q56,R380 away from CON29. 44. Page34: For interference, change C844 to 1U-0603.
	2001/03/29	45. Page33: Add IRGND plane under the ir module. 46. Page36: Move R458, Q73 to top side. 47. For impedance control, Change USB diffrrencial pairs to 7.5/7.5 mil (width/space).

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PROJECT : RT2.0
Quanta Computer Inc.

Project : RT2 MB	MB Assy' P/N: 31RT2MBAB5	Document No.: 204	Rev: 3C	Cover Sheet: 3 of 6
Project Manager : Jacky Lee	Project Leader : T.S. Wan	Drawing by : Allan Yu	Approved by : Jacky Lee	

MODEL: RT2 MB 16M

REV	DATE	CHANGE LIST
2A	2001/02/26	**B Test (PCB P/N: DA0RT2MBAB5)** 40. Page46: For power on squence, change PC36, PC38 to 1000P. 41. Page4: Change R108 to 0603 size. 42. Page24,44: Change C149, C167, C171, C793 foot print to TC1206 43. Page38: Change R362 to 10K. 44. Page43: Change R516, R520 to no-loading for ITP. 45. Page25, 12, 15: ChangeY3 to Epson SG-710ECK, Y6 to MC-306, add 2nd source BG625000508.
	2001/02/27	46. Page12: Add L122 on <VCCRTC> for EMI. 47. Page46: Change R300 to 0603 size. 48. Page3: For EMI, add C900-C905(10P, reserved) and place near the destinations. 49. Page5: Add bypass cap 0.1U_0402 on VTT (C906-C926) and VCCT(C927-C936). 50. Page24: Modify power circuit for <VGA_PLL1.8>,<VGA_PNLPLL1.8>. 51. Page3: For EMI, modify GND of CLK generator. Add <CLK_GND>, R642, R643. 52. Page30, 35: Change the control of <-RF_ON_LED>, R633 from miniPCI to EC. 53. Page23, 38: To save power, change power plane from <5VPCU> to <+5V> on U39.8, R176, R3; from <3VSUS> to <3.3VAUX> on R369, R362. 54. Page47: Change Q6, Q12 to IRF7811A; Q5, Q10, Q11 to FDS7764A because of better characteristics.
	2001/03/02	55. Page20: Change L23 to no-loading, L24 to loading for Hyundai DDR. And change part to FCM2012V131DC10 for larger current rating. 56. Page36: Change R628 from 180K to 100K for part available.
	2001/03/06	57. Page12: For RTC leakage, change R455 to 22K at U67.Y6 (INTRUDER#).
3A	2001/03/07	**C1 Test (PCB P/N: DA0RT2MBAC3)** 1. Page22: Change R210 from 22_1206 to 22R_0805.
	2001/03/08	2. Modify 3V power circuits to simplify 3V resources and components. Delete <3V_ALWAYS> in entire schematics because it doesn't need ALWAYS 3V. Page49: Change PU15.28 from <VL> to <RVCC_ON>, change <3V_ALWAYS> to <3V_S5>.Change parts of PL4, PR63. Delete PC36, PC47. NC PD19. 3. Page21: Change memory I/O power of VGA chip, VDDR1, from <VDD_SDRAM> to <VDDQ_2.5V>. Because it must be same as VDDQ of VGA SDRAM(U23, U60). Change VDDRH(U47.C5) to <VDDQ_2.5V> thru L123. 4. Page44, 46: Change net name from <MAINON_0> to <-MAIN_ON>, from <SUSON_0> to <-SUS_ON>. 5. Page47: Add L127, R644 but reserved for second source. 6. Page13: Change R432 from 0805 to 0603. 7. Page46: Delete fuse L33, L44. Change PL6 to FBM3216HS480NT(6 Amp) and add PL10 the same part.
	2001/03/12	8. Page 44: Modify 1.8 and 2.5 voltage circuits to switching power circuits for efficiency, change the source of <+1.5V> to be from <+1.8V>. 9. As the changes of item 8, modify the VGA power circuits, Page24: Delete regulators circuits: PU1, R98, R99 for <+1.8_VGA>; Q21, Q72, PU11, C285, C787-788, R447 for <VDDQ_2.5V>; U20, C173, C146, R337-338 for <VGA_MEMPLL1.8>, and the relative discharging circuits. Then power them thru beads. 10. Page25, 35: Change <-M3_RST_EN> to <M3_RST_EN> for high-active. 11. Page47: Add discharge circuits for <VCCT>: R647, Q109; <VTT>: R645-646, Q107-108. 12. Page6: Change R324 footprint from 0603 to 0805.
	2001/03/13	13. Page17: Change Q78 from SI4800DY to SI3456 for small size.
	2001/03/15	14. For VGA D3-cold, Page44: Add <+2.5V> power, PQ48, Q110, R648. Page24: Add <2.5_VGA>, L131(reserved), L132 for option of power. Page20: Change L24 to be powered with <2.5_VGA>. Page24: Add <1.8_VGA>, L129(reserved), L130 for option of power. Page24: Add L133(reserve L22) for option of power between <3VSUS> and <+3V>.

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PROJECT : RT2.0
Quanta Computer Inc.

Project : RT2 MB 16M	MB Assy' P/N: 31RT2MB0019	Document No.: 204	Rev: 3C	Cover Sheet: 2 of 6
Project Manager : Jacky Lee	Project Leader : T.S. Wan	Drawing by : Allan Yu	Approved by : Jacky Lee	

MODEL: RT2 MB 16M

REV	DATE	CHANGE LIST
1A	2000/01/04	**A Test** First Release (PCB P/N: DA0RT2MBA7)
2A	2001/01/12	**B Test (PCB P/N: DA0RT2MBAB5)** 1. Change R103, R107, R61, R92, R97, R122, R123, R75, R379, R581, R582 from 22_1206 to 22_0805. 2. Page24: Modify footprint (UMAX8) of U19,U42. 3. For NS87570 strap pin, Page34: Change R584 from 10K to no-loading, R585 from no-loading to 10K. 4. For Super I/O (PC87393) strap pin, Page 31 Delete R463 at <TXD1>. 5. Page 5: Change R439 from 0805 to 0603. 6. The NMOS turn-on voltage (Q84, Q18) for 3V_S5, 3.3VAUX is not high enough, Page44: Add Q98, Q97, R613, R612, <3V_S5_EN>, <3VAUX_EN>. 7. The voltage level of VGA_PLL1.8 and VGA_PNLPLL1.8 is not correct Page24: Change R283, R51 to 44.2K_1%. 8. Spring arm ground contact Page30, 10, 51: CON27.125.126; CON24.125.126; CON25.147.148; CON26.125.126. 9. Page15: Change U57(LAN PHY) to 82562EP(Kinnereth-M). 10. Simplify RI# circuits: Page38: Delete U53, U54, C694, C695, R372, R373. Short D21.2, D22.2, D23.2, Q64.2. 11. Page 3: Exhange clock generator U24 66MHz output pin 22 & 23 for power down mode sequence. 12. Page 12: Delete USB pull low 1.5K: R559-R564, R541-R546. 13. Modify <DISPON> circuits : Page22: Delete U35,U11, add D39, D40. 14.To prevent interference, Page34, 51: change C789, C878, C810, C843 to 1U_0603_X5R. 15. To eliminate ground noise, Page47: Change PU9.15 from inverter ground to system ground(GND). 16. Page15: Add one 4-pin lan pass through connector(CON29) for docking. 17. Page15: Add bypass cap C885-C889 for U56 (86562EP). 18. Page47: Delete SW2, add R618, change R272 from 0 to 15K_1%. 19. Page14: Change pin assignment of USB connector(CON6) and del U10. Change C422, C423 from 4.7Uf to 100uF 20. Page 16: Add reset and power control circuit for HDD. 21. Page 20: Pin 28 of U60 changes net name from VMCS1# to VMCS0# 22. Page 25: Add L120, L121for 49.152MHz oscillator for EMI. 23. Page 26: To increase the volume gain. Change R330 from 20K to 33K and R331 from 2.49K to 0. 24. Page 30: Add BlueTooth USB signals to 1st mini PCI connector. 25. Page 34: MY11 pin name is duplicated on BP4, pin5 and CON10, pin15. Change the net name to MY1_1. 26. Page 34,35: Add additional GPI and GPO for 87570. 27. Page 36: Add new fan drive circuit. 28. Page 36: Modify power LED control circuit for single color support, but reserved <-PWRLED1>. 29. Page 38: Add wireless LAN enable/disable circuit and add CON28 for antenna support. 30. Page 30: Route the AC-link signals to 1st mini PCI connector. 31. Page 14: Add two power control signals to USB ports and <USBOC0#>,<USBOC1#>. 32. Page 5: VID pullup resistor changes from 10K to 1K. 33. Page7, 9: New pin definition were added for GMCH-A3 silicon. 34. Page 7: Del R345 and make the length equals to 150+-50 mil.
	2001/02/26	35. Page 22: Modify <DIPON> circfuits, it controled by VGA(<-BLON>), ICH3(<DISP_ON>); simplify LCDVCC control circuits(<DIGON>). 36. Page46: Add spring (PAD101) under power jack(PJ1). 37. For EMI, Page25: Add L120, L121. Page6: Add R639, C899(reserved), <CLK66_GBIN_1>. 38. Page6: R300 change to 0603 size. 39. Page25: Change R313 to noloading to disable modem auto detect by ES1988.

RT2 MB 16M

Page	From	To	Page	From	To
1	1A		33	1A	
2	1A		34	1A	2A
3	1A	2A	35	1A	
4	1A	2A	36	1A	2A
5	1A	2A	37	1A	
6	1A	2A	38	1A	2A
7	1A	2A	39	1A	
8	1A		40	1A	
9	1A	2A	41	1A	
10	1A	2A	42	1A	
11	1A		43	1A	2A
12	1A	2A	44	1A	2A
13	1A		45	1A	
14	1A	2A	46	1A	2A
15	1A	2A	47	1A	2A
16	1A	2A	48	1A	
17	1A	2A	49	1A	
18	1A		50	1A	
19	1A		51	1A	2A
20	1A	2A			
21	1A				
22	1A	2A			
23	1A	2A			
24	1A	2A			
25	1A	2A			
26	1A	2A			
27	1A				
28	1A				
29	1A				
30	1A	2A			
31	1A	2A			
32	1A				

PROJECT : RT2.0
Quanta Computer Inc.

Project : RT2 MB 16M	MB Assy' P/N: 31RT2MB0019	Document No.: 204	Rev: 3C	Cover Sheet: 1 of 6
Project Manager : Jacky Lee	Project Leader : T.S. Wan	Drawing by : Allan Yu	Approved by :	

0711 modify
RT2 MB: PCB Rev E , Schematics Rev 3C

Schematics Page Index

Pg#	Description	DNI LIST	Pg#	Description	DNI LIST
1	Schematic Block Diagram		27	line in/mic in/CD audio in	
2	PAGE INDEX		28	TI1420 CARDBUS CONTROLLER	
3	Clock Generator		29	CARDBUS interface	
4	TUALATIN CPU(HOST BUS)-1		30	MINI PCI-1 interface	
5	TUALATIN CPU(POWER/NC)-2		31	super I/O (PC87393F)	
6	GMCH-M(HOST)-1		32	LPT/FDD interface	
7	GMCH-M(DRAM)-2		33	COM/IR interface	
8	GMCH-M(AGP)-3		34	PC87570F	
9	GMCH-M(VCC,GND)-4		35	570 I/O & RF/B CONN	
10	SDRAM,SODIMMX2		36	570 access BUS/PS2/FAN/touch PAD	
11	ICH3-M (CPU,PCI,IDE)-1		37	ICH SMBus	
12	ICH3-M (USB,HUB,LPC)-2		38	RING INDICATOR	
13	ICH3-M (POWER&GND)-3		39	1K Hz BEEP	
14	USBx2		40	upper,volume interface	
15	LAN interface		41	FULL DOCK	
16	Primary IDE (HDD interface)		42	hole PAD and EMI PAD	
17	Secondary IDE/FDD interface		43	ITP interface	
18	ATI P6 (HOST,VIDEO O/P)-1		44	system special power	
19	ATI P6 (VRAM)-2		45	VID selector	
20	Video DDR SDRAM		46	power JACK/BATTERY CONN.	
21	ATI M6 (PWR/GND)-3		47	CPU power-VCCT/VTT	
22	LCD interface		48	CHARGER & DISCHARGER	
23	S Video/Composite,CRT		49	POWER CIRCUIT(MAX1632)	
24	VGA power		50	BATTERY SELECTOR	
25	ESS1988		51	MINI PCI second interface	
26	AMP/line out				

10-LAYERS
STACKUP

Layer 1 TOP
Layer 2 GND
Layer 3 IN1
Layer 4 IN4
Layer 5 GND1
Layer 6 IN5
Layer 7 IN2
Layer 8 IN3
Layer 9 VCC
Layer 10 BOT

Modified on C1 test

PROJECT : RT2.0
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Custom	FRONT-PAGE	1A
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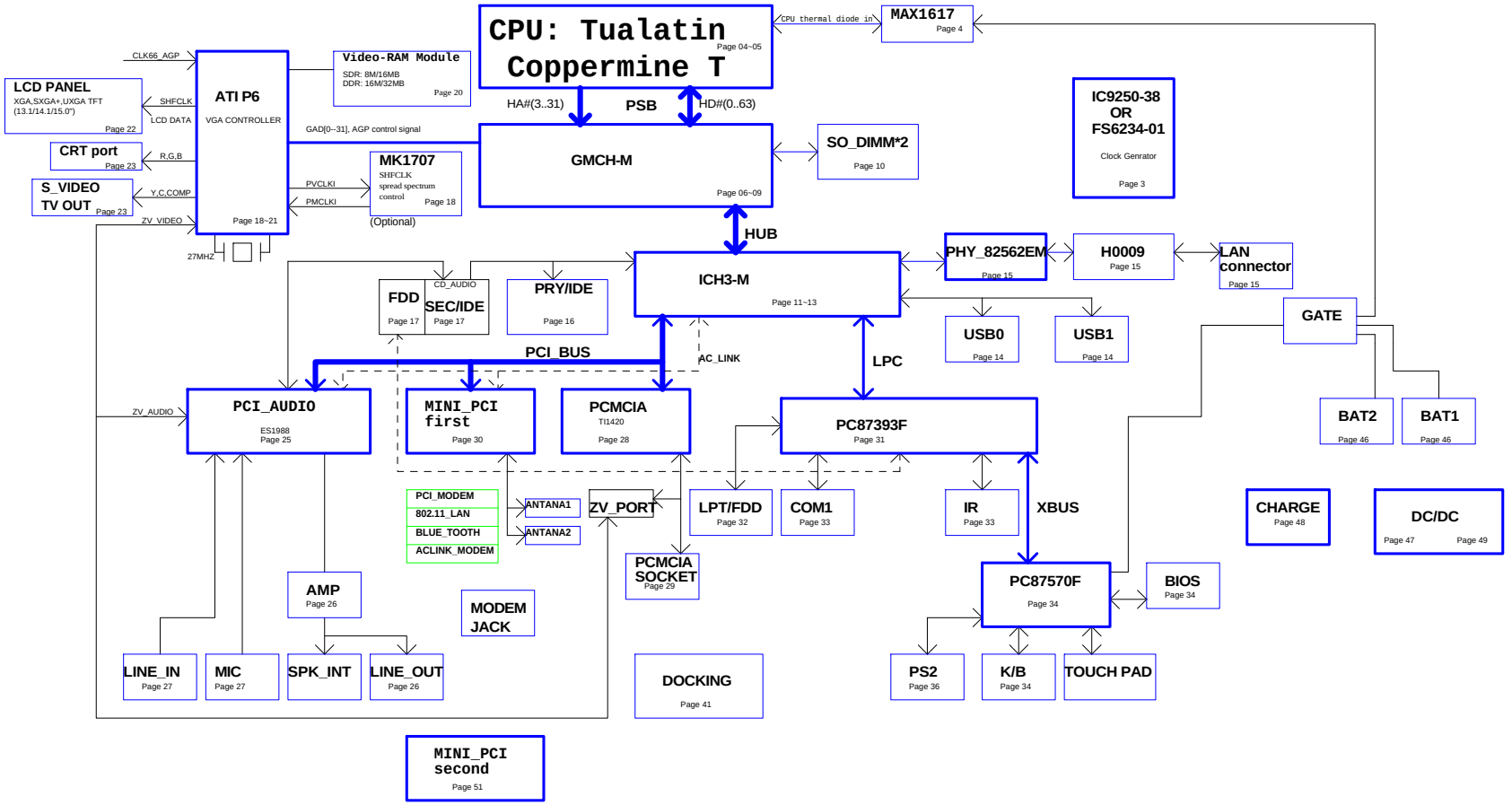
RT2.0



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
C	BLOCK DIAGRAM	1A

Date: Tuesday, September 11, 2001 Sheet 2 of 57

BSEL[1:0]		STSEM BUS FREQUENCY
1	1	133MHZ
0	1	100MHZ

Ramp_0704: Update

Clock Generator

Add

Place near destination

C900 C901 C902 C903 C904 C905 *10P

CLK66_GBOUT — R128 33 — C267 5P

+3V — R400 330 — R399 330 — R124 10K — R402 *0

C237 10P — C236 10P — R116 2M — Y2 14.318MHz — CLK_XIN — CLK_XOUT

U24 — CK-TITAN

XTAL_IN 2 — XTAL_OUT 3

[12,18,25] SUSA# — PWR_DWN# 25
[12] PCI_STP# — PCI_STP# 34
[12] CPU_STP# — CPU_STP# 53
[5] VTT_PWRGD# — PWRGD# 28

CK_SMCLK — SCLK 30
CK_SMDATA — SDATA 29

[4] BSEL1 — BSEL2 40 — BSEL1 55
[4] BSEL0 — BSEL0 54

SEL2 40 — SEL1 55 — SEL0 54

+3V — BK2125HM471 L25 — C241 0.1u_0402 — C250 1000P — CK_VDD_REF
C256 0.1u_0402 — C246 0.1u_0402 — C244 0.1u_0402

VDD_REF 1 — VDD_PCI_1 8 — VDD_PCI_2 14

+3V — BK2125HM471 L28 — C275 0.1u_0402 — C268 1000P — C269 0.1u_0402 — C263 0.1u_0402 — CK_VDD_3

VDD_3V66_1 19 — VDD_3V66_2 32

+3V — BK2125HM471 L105 — C242 0.1u_0402 — C239 10U/25V_1206 — CK_VDD_CPU
1000P C252 — 0.1u_0402 C254 — 0.1u_0402 C247

VDD_CPU_1 46 — VDD_CPU_2 50

+3V — BK2125HM471 L118 — C881 10U/25V_1206 — CK_VDD_48MHZ
C264 0.1u_0402 — R411 221_1% — R120 10K

VDD_48MHZ 37 — IREF 42 — MULT0 43

+3V — BK2125HM471 L29 — C959 0.1u_0402 — C277 10U/25V_1206 — CK_VDDA
C274 0.1u_0402

VDD_CORE 26 — GND_CORE 27 — CLK_GND

GND_REF 4 — GND_PCI_1 9 — GND_PCI_2 15 — GND_3V66_1 20 — GND_3V66_2 32 — GND_48MHz 36 — GND_IREF 41 — GND_CPU 47 — CLK_GND

CK-TITAN-A

14M_S — R395 33 — R391 33 — C744 *10P — C749 *10P — 14M_SIO [31] — 14M_ICH [12]

REF 56

CPU0 52 — CPU0# 51 — HCLK_CPU [4] — HCLK_CPU# [4]

CPU1 49 — CPU1# 48 — HCLK_GMCH [6] — HCLK_GMCH# [6]

CPU2 45 — CPU2# 44 — HCLK_ITP [43] — HCLK_ITP# [43]

3V66_0 33 — 3V66_1/VCH 35 — T201 *PAD — T200 *PAD

R649 240K — 0322: Add for QS stepping.

CLK66_GBOUT 24 — CLK66_ICHHUB_S 23 — R434 33 — CLK66_GBIN_S 22 — R431 33 — CLK66_AGP_S 21 — R417 33

66IN/3V66_5 — 66B2/3V66_4 — 66B1/3V66_3 — 66B0/3V66_2

CLK66_GBOUT [6] — CLK66_ICHHUB [12] — CLK66_GBIN [6] — CLK66_AGP [18]

PCI_F2 7 — PCI_F1 6 — PCI_F0 5 — T198 *PAD

PCLK_ICH_S — R398 33 — PCLK_CPUAPIC_S — R118 33

PCLK_ICH [11] — PCLK_CPUAPIC [4]

PCI6 18 — PCI5 17 — PCI4 16 — PCI3 13 — PCI2 12 — PCI1 11 — PCI0 10 — T199 *PAD

PCLK_SIO_S — R121 33 — PCLK_PCIC_S — R413 33 — PCLK_AUD_S — R410 33 — PCLK_MINI2_S — R409 33 — PCLK_MINI_S — R119 33 — PCLK_DK_S — R401 33

PCLK_SIO [31] — PCLK_PCIC [28] — PCLK_AUD [25] — PCLK_MINI2 [51] — PCLK_MINI [30] — PCLK_DK [41]

48M_USB 39 — 48M_DOT 38 — CLK48_USB_S — R414 33 — CLK48_DREF_S — R426 22

CLK48_USB [12] — CLK48_DREF [8]

C778 C768 C253 C755 C767 C257 C756 C243 C750 C775 C780 C782 C762 *10P

0_0805 R668 — 0_0805 R664 — 0_0805 R642 — CLK_GND

C2_0423: Add

0_0805 R643 — CLK_GND

C2_0423: Add

+3V — R671 10K — Q114 2N7002E — [12,37] ICH_SMCLK — CK_SMCLK

+3V — R672 10K — Q115 2N7002E — [12,37] ICH_SMDATA — CK_SMDATA

12V — R673 100K

FOR GMCH A3
ICS: ICS9250EG-38 *** Used in C2 test, P/N:AL009250K17
Cypress: W320-03X

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	2B
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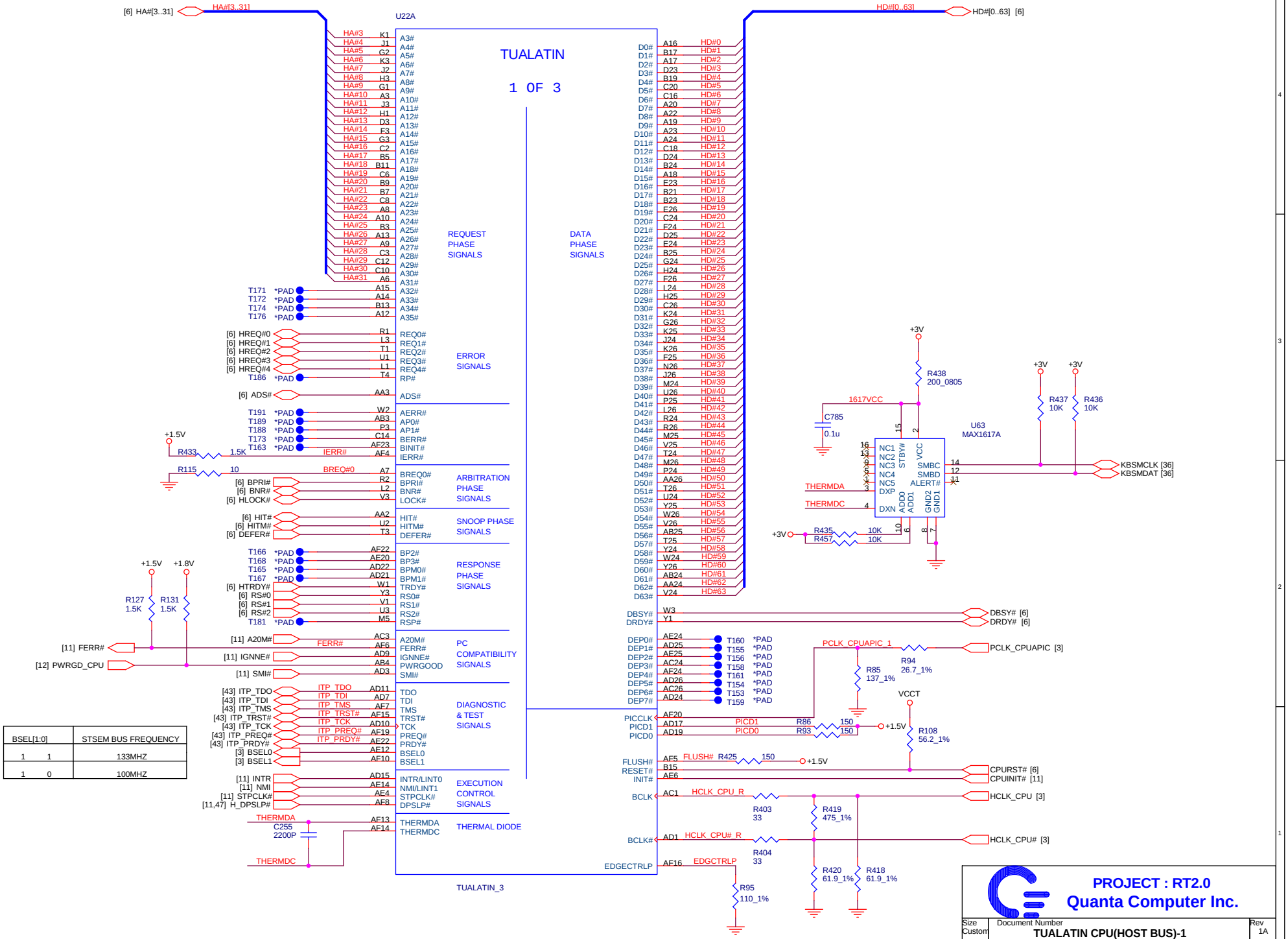
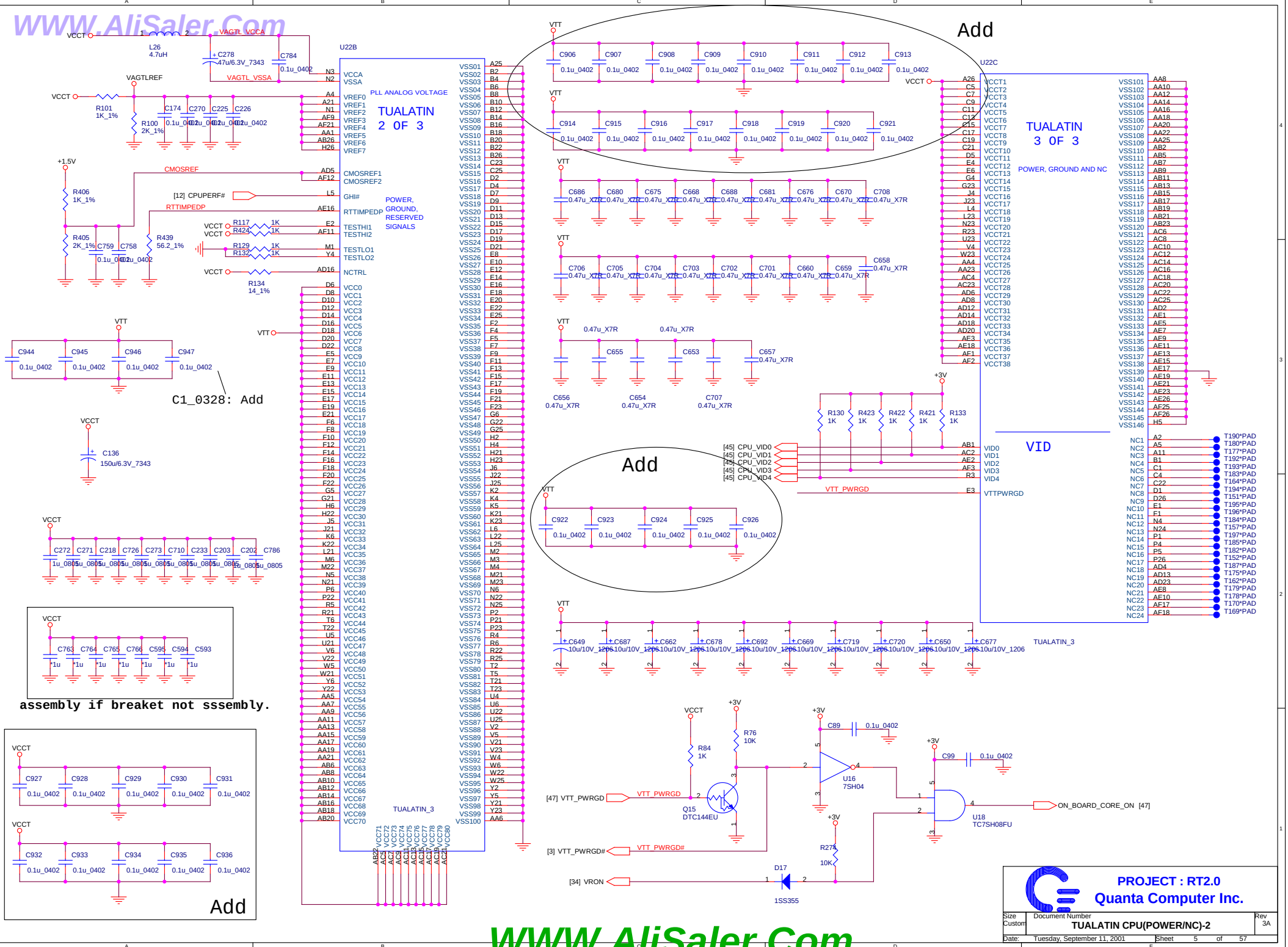


BSEL[1:0]		STSEM BUS FREQUENCY
1	1	133MHZ
1	0	100MHZ

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TUALATIN CPU(HOST BUS)-1	1A
Date: Tuesday, September 11, 2001	Sheet 4 of 57	



GMCH-M

[12] HL[0..10] — HL[0..10]
[4] HD#[0..63] — HD#[0..63]
[4] HA#[3..31] — HA#[3..31]
[11,16,18,25,28,30,31,41,51] PCIRST# — R231 0 — PCIRST# 1
[4] ADS# — ADS#
[4] HREQ#0 — HREQ#0
[4] HREQ#1 — HREQ#1
[4] HREQ#2 — HREQ#2
[4] HREQ#3 — HREQ#3
[4] HREQ#4 — HREQ#4
[4] BPRI# — BPRI#
[4] BNR# — BNR#
[4] HLOCK# — HLOCK#
[4] HIT# — HIT#
[4] HITM# — HITM#
[4] DEFER# — DEFER#
[4] DBSY# — DBSY#
[4] DRDY# — DRDY#
[4] HTRDY# — HTRDY#
[4] RS#0 — RS#0
[4] RS#1 — RS#1
[4] RS#2 — RS#2
[43] ITP_CPURST# — R270 0 — CPURST#
[4] CPURST#

[3] CLK66_GBIN — CLK66_GBIN — R639 0 — CLK66_GBIN_1
C899 *10P
[12] HLSTRB — HLSTRB
[12] HLSTRB# — HLSTRB#
[3] CLK66_GBOUT — CLK66_GBOUT — C430 0.01u — CLK66_GBOUT_S — R201 49.9_1%

EMI

0322: Change

[3] HCLK_GMCH — R18 33 — HCLK_GMCH_R
R25 475_1%
[3] HCLK_GMCH# — R24 33 — HCLK_GMCH#_R
R19 61.9_1%
R28 61.9_1%

+1.8V — C582 *470P — HUBREF_CV
R298 301_1%
R315 *56.2_1%
[12] VHUBREF — VHUBREF
R307 301_1%
R321 0
C588 0.1u_0402 — HUBREF_CG
C568 0.01u

HUBREF = 0.5 * VCC1_8
Place divider in the middle of the bus

U17A

HOST BUS INTERFACE (Processor System Bus)

HD#0	U4	HD0#	
HD#1	P1	HD1#	
HD#2	W6	HD2#	
HD#3	U2	HD3#	
HD#4	U6	HD4#	
HD#5	R1	HD5#	
HD#6	N3	HD6#	
HD#7	W5	HD7#	
HD#8	V4	HD8#	
HD#9	P3	HD9#	
HD#10	R3	HD10#	
HD#11	U1	HD11#	
HD#12	V6	HD12#	
HD#13	W4	HD13#	
HD#14	T3	HD14#	
HD#15	P2	HD15#	
HD#16	V3	HD16#	
HD#17	R2	HD17#	
HD#18	T1	HD18#	
HD#19	W3	HD19#	
HD#20	U3	HD20#	
HD#21	Y4	HD21#	
HD#22	AA3	HD22#	
HD#23	W1	HD23#	
HD#24	V1	HD24#	
HD#25	Y1	HD25#	
HD#26	Y6	HD26#	
HD#27	AD3	HD27#	
HD#28	AB4	HD28#	
HD#29	AB5	HD29#	
HD#30	V2	HD30#	
HD#31	Y3	HD31#	
HD#32	Y2	HD32#	
HD#33	AA4	HD33#	
HD#34	AA1	HD34#	
HD#35	AA6	HD35#	
HD#36	AB1	HD36#	
HD#37	AC4	HD37#	
HD#38	AA2	HD38#	
HD#39	AB3	HD39#	
HD#40	AD2	HD40#	
HD#41	AD1	HD41#	
HD#42	AC2	HD42#	
HD#43	AB6	HD43#	
HD#44	AC6	HD44#	
HD#45	AC1	HD45#	
HD#46	AF3	HD46#	
HD#47	AD4	HD47#	
HD#48	AD6	HD48#	
HD#49	AC3	HD49#	
HD#50	AH3	HD50#	
HD#51	AE5	HD51#	
HD#52	AE3	HD52#	
HD#53	AG2	HD53#	
HD#54	AF4	HD54#	
HD#55	AF2	HD55#	
HD#56	AJ3	HD56#	
HD#57	AE4	HD57#	
HD#58	AG1	HD58#	
HD#59	AE1	HD59#	
HD#60	AG4	HD60#	
HD#61	AH4	HD61#	
HD#62	AG3	HD62#	
HD#63	AF1	HD63#	
PCIRST# 1	AB24	RESET#	

HA3#	H2	HA#3	
HA4#	E3	HA#4	
HA5#	G3	HA#5	
HA6#	N4	HA#6	
HA7#	M6	HA#7	
HA8#	F1	HA#8	
HA9#	F2	HA#9	
HA10#	J3	HA#10	
HA11#	F3	HA#11	
HA12#	P6	HA#12	
HA13#	G1	HA#13	
HA14#	N5	HA#14	
HA15#	H1	HA#15	
HA16#	P4	HA#16	
HA17#	T4	HA#17	
HA18#	M2	HA#18	
HA19#	J2	HA#19	
HA20#	L2	HA#20	
HA21#	R4	HA#21	
HA22#	K1	HA#22	
HA23#	L3	HA#23	
HA24#	L1	HA#24	
HA25#	J1	HA#25	
HA26#	N1	HA#26	
HA27#	T5	HA#27	
HA28#	H3	HA#28	
HA29#	M3	HA#29	
HA30#	M1	HA#30	
HA31#	K3	HA#31	
ADS#	C1	ADS#	
HREQ0#	K6	HREQ#0	
HREQ1#	M4	HREQ#1	
HREQ2#	K5	HREQ#2	
HREQ3#	K4	HREQ#3	
HREQ4#	L6	HREQ#4	
BPRI#	L4	BPRI#	
BNR#	E1	BNR#	
HLOCK#	J6	HLOCK#	
HIT#	D3	HIT#	
HITM#	D1	HITM#	
DEFER#	J4	DEFER#	
DBSY#	G5	DBSY#	
DRDY#	F4	DRDY#	
HTRDY#	G4	HTRDY#	
RS0#	H6	RS#0	
RS1#	H4	RS#1	
RS2#	G6	RS#2	
CPURST#	R6	CPURST#	
HTCLK	AJ4	HCLK_GMCH_R	
HTCLK#	AH5	HCLK_GMCH#_R	
GTL_RCOMP	C2		
GTL_REFA	J7	R324 80.6_1%_0805	
GTL_REFB	AA7		
GBOUT	AD24	CLK66_GBOUT_S	
GBIN	AG26	CLK66_GBIN_1	
HL0	G26	HL0	
HL1	H28	HL1	
HL2	H29	HL2	
HL3	H27	HL3	
HL4	F29	HL4	
HL5	F27	HL5	
HL6	E29	HL6	
HL7	E28	HL7	
HL8	G25	HL8	
HL9	G27	HL9	
HL10	H26	HL10	
HLREF	H24	VHUBREF	
HLSTRB	G29	HLSTRB	
HLSTRB#	F28	HLSTRB#	
HL_RCOMP	J23	HL_RCOMP	

GMCH3-M

R300 54.9_1%

B2_0313: Change to 0805

VAGTLREF
C460 0.1u_0402
C561 0.1u_0402

CLK66_GBIN_1 — R665 *22 — C960 *5P

C2_0423: Add, reserved Close to GMCH

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	GMCH-M (HOST)-1	2B
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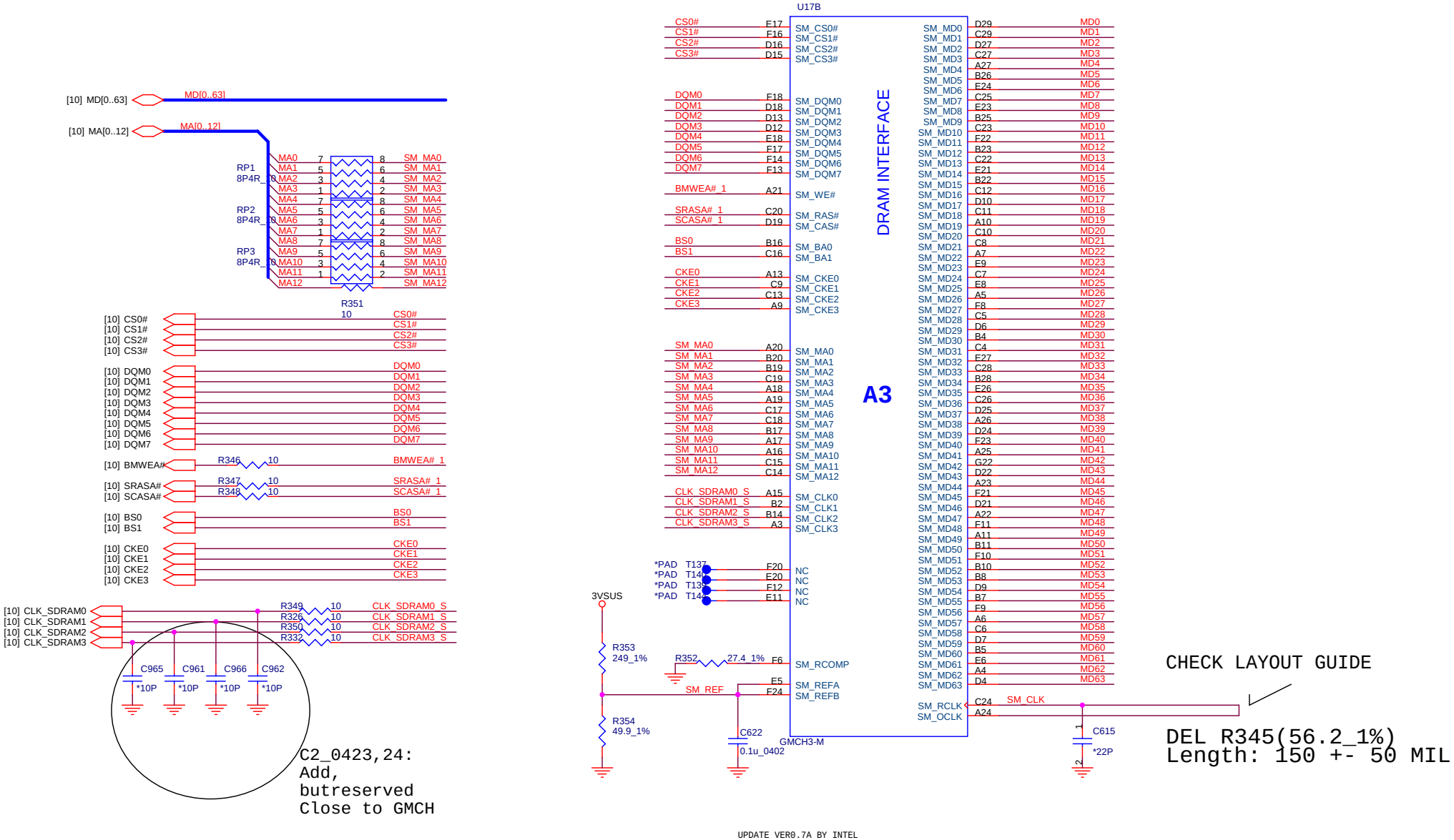
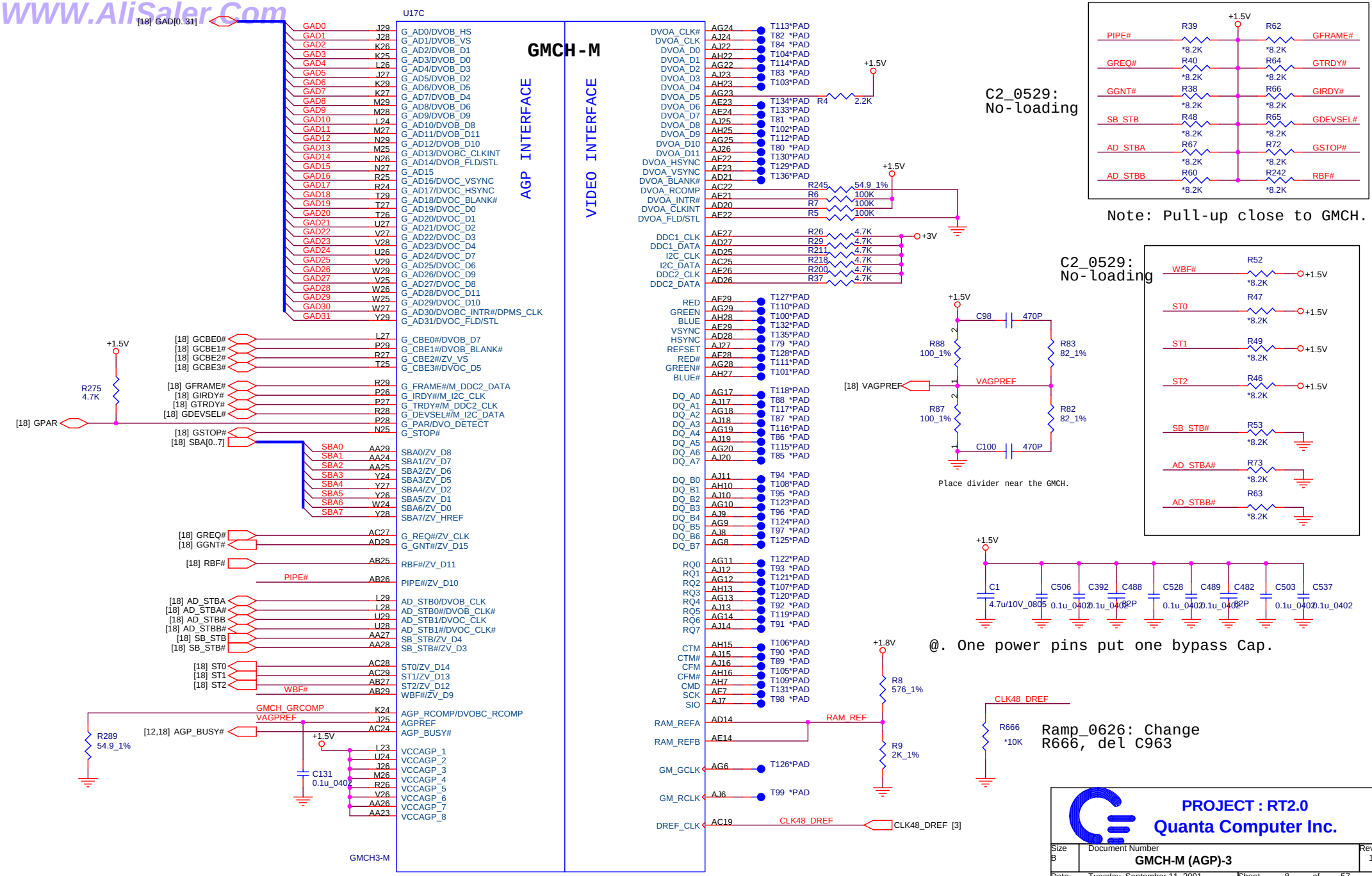
GMCH-M



UPDATE VER0.7A BY INTEL

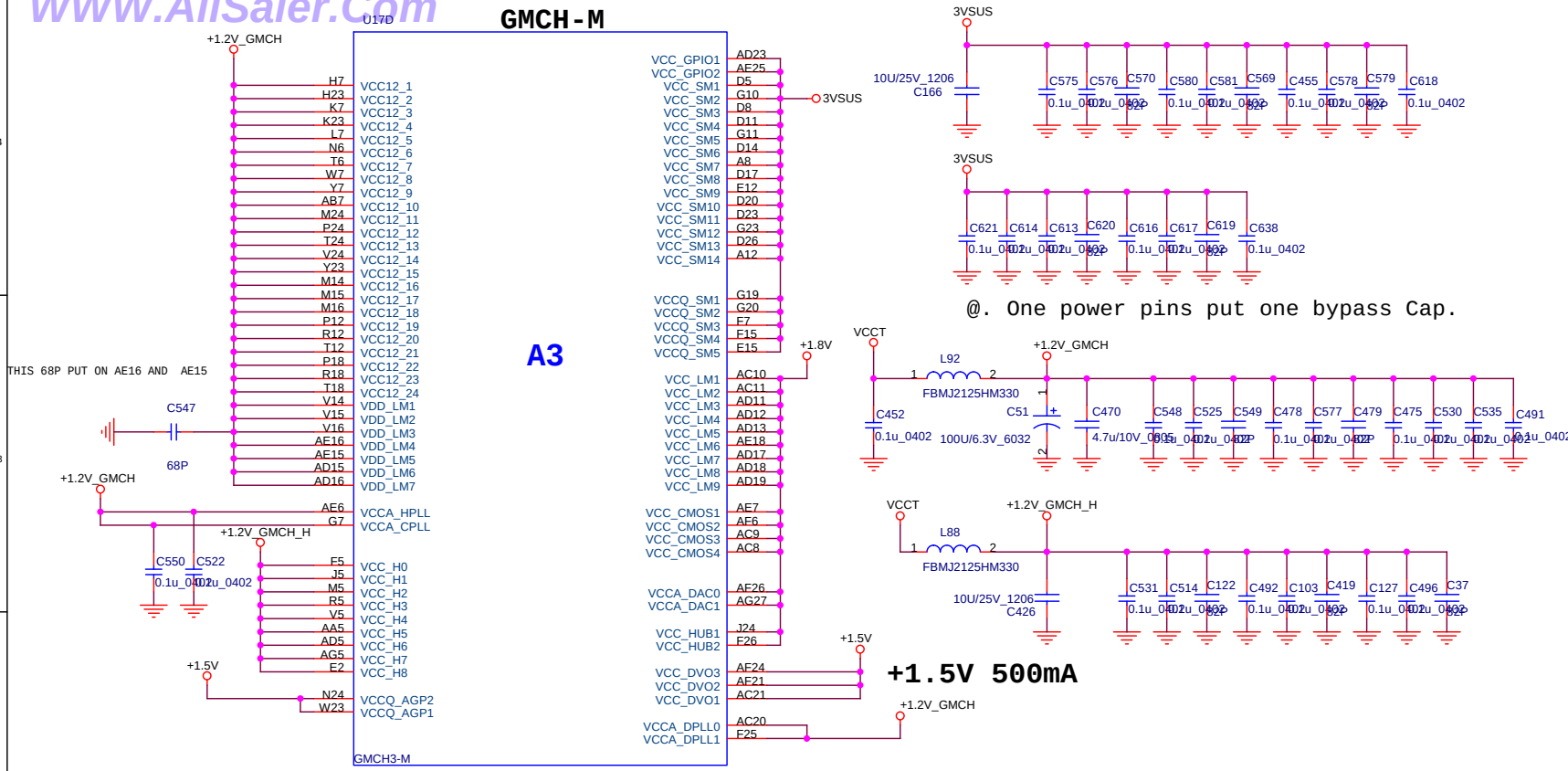
LAYOUT 2'' AND 6'' FOR EACH LINE

PROJECT : RT2.0		
Quanta Computer Inc.		
Size: B	Document Number: GMCH-M (DRAM)-2	Rev: 2A
Date: Tuesday, September 11, 2001	Sheet 7 of 57	



GMCH-M

U17D



3VSUS

10U/25V_1206 C166

C575 C576 C570 C580 C581 C569 C455 C578 C579 C618 0.1u_0402 82P

C621 C614 C613 C620 C616 C617 C619 C638 0.1u_0402

@. One power pins put one bypass Cap.

VCCT

L92 FBMJ2125HM330

C452 0.1u_0402

+1.2V_GMCH

C51 100U/6.3V_6032

C470 4.7u/10V_0805

C548 C525 C549 C478 C577 C479 C475 C530 C535 C491 0.1u_0402 82P

VCCT

L88 FBMJ2125HM330

+1.2V_GMCH_H

10U/25V_1206 C426

C531 C514 C122 C492 C103 C419 C127 C496 C37 0.1u_0402 82P

+1.5V 500mA

+1.2V_GMCH

C550 C522 0.1u_0402

+1.5V

+1.2V_GMCH

C507 C502 C534 C480 C457 C518 C447 C446 0.1u_0402 82P

+1.2V_GMCH

C556 C562 C513 C476 C471 C504 C450 C477 0.1u_0402 82P

+1.8V +1.8V 250mA

C169 10U/25V_1206

C445 C448 C459 C449 C474 C458 C444 C2 C3 C591 0.1u_0402 82P

@. One power pins put one bypass Cap.

+1.2V_GMCH

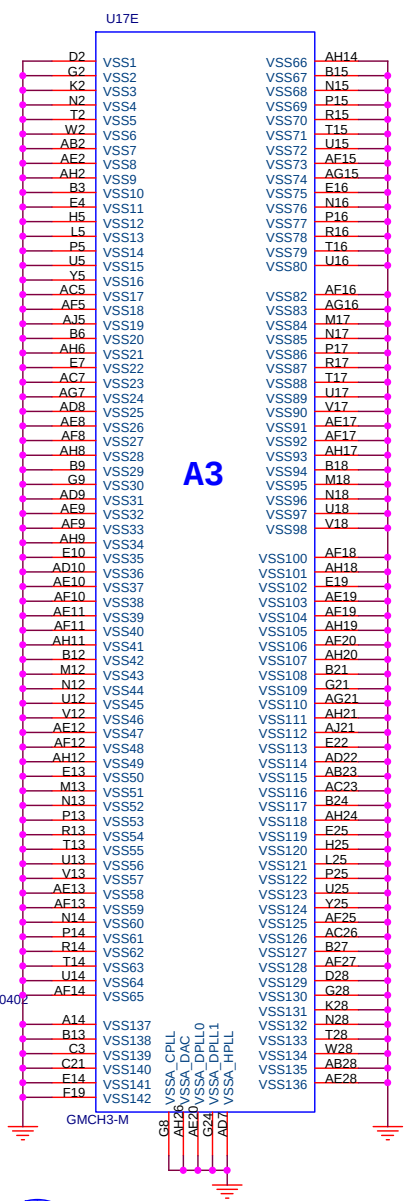
C553 C554 C519 C539 C523 C508 C505 C484 0.1u_0402 82P

+1.5V

C168 10U/25V_1206

C558 C456 C543 C524 0.1u_0402 82P

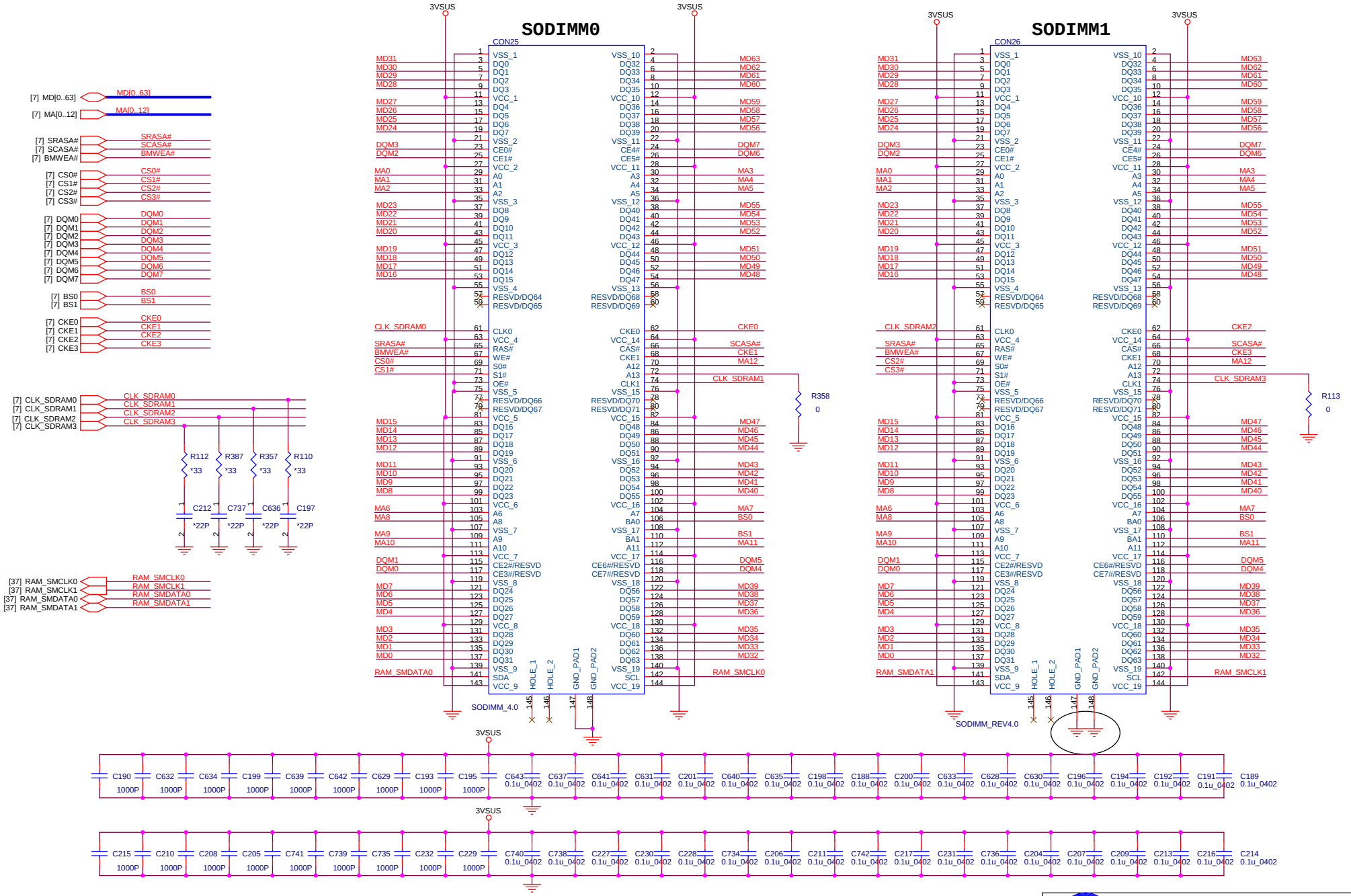
U17E



PROJECT : RT2.0

Quanta Computer Inc.

Size	Document Number	Rev
B	GMCH-M (VCC,GND)-4	1A
Date: Tuesday, September 11, 2001	Sheet 9 of 57	



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SDRAM,SODIMMx2	2A
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ICH HUB

U67A

CPU

[4] NMI → NMI (Y21)
[4] A20M# → A20M# (V23)
[4] FERR# → FERR# (J22)
[4] IGNNE# → IGNNE# (AA21)
[4] INTR → INTR (AA23)
[4] CPUINIT# → INIT# (AB23)
[34] RC# → RCIN# (U22)
[34] KGA20 → A20GATE (Y22)

R658 *10K: +3V → A20GATE

APICD0 (J20), APICD1 (J21), APICCLK (J19) → R510 10K, 10K, R657

SMI# (Y23) → SMI# [4]
STPCLK# (U23) → STPCLK# [4]
CPU_SLP# (W21) → T65 *PAD
DPSLP# (AB22) → H_DPSLP# [4,47]

C1_0328: Modify

C1_0328: Add but reserved.

PCI

AD0 (J2), AD1 (K1), AD2 (J4), AD3 (K3), AD4 (H5), AD5 (K4), AD6 (H3), AD7 (L1), AD8 (L2), AD9 (G2), AD10 (L4), AD11 (H4), AD12 (M4), AD13 (J3), AD14 (M5), AD15 (J1), AD16 (F5), AD17 (N2), AD18 (G4), AD19 (P2), AD20 (G1), AD21 (P1), AD22 (F2), AD23 (P3), AD24 (F3), AD25 (R1), AD26 (E2), AD27 (N4), AD28 (D1), AD29 (P4), AD30 (E1), AD31 (P5)
[25,28,30,41,51] AD[0..31]

C/BE0# (K2), C/BE1# (K5), C/BE2# (N1), C/BE3# (R2) → C/BE0# [25,28,30,41,51] … C/BE3# [25,28,30,41,51]

FRAME# (F1), IRDY# (N3), TRDY# (H1), DEVSEL# (M3), STOP# (H2), PAR (G5), SERR# (L5), PERR# (M2), PLOCK# (M1)
FRAME# [25,28,30,41,51], IRDY# [25,28,30,41,51], TRDY# [25,28,30,41,51], DEVSEL# [25,28,30,41,51], STOP# [25,28,30,41,51], PAR [25,28,30,41,51], SERR# [28,30,41,51], PERR# [28,30,41,51], PLOCK# [41]
PAR → *100 R511
for A0 version must be pull low 100 Ohm.

REQ0# (D3), REQ1# (F4), REQ2# (A3), REQ3# (R4), REQ4# (E4), GNT0# (A4), GNT1# (E3), GNT2# (D2), GNT3# (D5), GNT4# (B4)
REQ0# [41], REQ1# [30], REQ2# [28], REQ3# [25], REQ4# [51], GNT0# [41], GNT1# [30], GNT2# [28], GNT3# [25], GNT4# [51]

PIRQA# (B1), PIRQB# (C1), PIRQC# (B2), PIRQD# (A2), PIRQE# (A6)
PIRQA# [28,41], PIRQB# [18,30,41,51], PIRQC# [25,41], PIRQD# [30,41,51]
+3V → R553 100K, R533 100K, R534 100K

GPIO2/PIRQE#, GPIO3/PIRQF#, GPIO4/PIRQG#, GPIO5/PIRQH# (B5, C5, A5)
IDE_ID0 [17], IDE_ID1 [17], IDE_ID2 [17]

PCLK_ICH → R484 *68, C827 *15P

[6,16,18,25,28,30,31,41,51] PCIRST# (Y1)
[25,28,30,41,51] PME# (W1)
[28,31,41] SERIRQ (H22)
[25,28,30,31,41,51] CLKRUN# (AC2)
[3] PCLK_ICH (T5)
PCIRST#, PME#, SERIRQ, CLKRUN#/GPIO24, PCICLK

GPIO0/REQA# (C4), GPIO1/REQB#/REQ5# (D4), GPIO16/GNTA# (B6), GPIO17/GNTB#/GNT5# (B3)
REQA# [41], REQB# [28], GNTA# [41], GNTB# [28]

GNTA# → R569 *1K

IDE

[16] PDD0 … [16] PDD15 (W12, AB11, AA10, AC10, W11, Y9, AB9, AA9, AC9, Y10, W9, Y11, AB10, AC11, AA11, AC12)
PDD0 … PDD15

[16] PDCS1# (AC15), [16] PDCS3# (AB15), [16] PDA0 (AA14), [16] PDA1 (AC14), [16] PDA2 (AA15), [16] PDIOR# (AC13), [16] PDIOW# (Y12), [16] PIORDY (AB13), [16] IRQ14 (AB14), [16] PDDREQ (AB12), [16] PDDACK# (Y13)
PDCS1#, PDCS3#, PDA0, PDA1, PDA2, PDIOR#, PDIOW#, PIORDY, IRQ14, PDDREQ, PDDACK#

SDD0 (Y17) … SDD15 (AC18)
SDD0 [17] … SDD15 [17]

SDCS1# (AC21), SDCS3# (AC22), SDA0 (AC20), SDA1 (AA19), SDA2 (AB20), SDIOR# (AC19), SDIOW# (AA18), SIORDY (AB19), IRQ15 (W19), SDDREQ (AB18), SDDACK# (Y19)
SDCS1# [17], SDCS3# [17], SDA0 [17], SDA1 [17], SDA2 [17], SDIOR# [17], SDIOW# [17], SIORDY [17], IRQ15 [17], SDDREQ [17], SDDACK# [17]

ICH3_F

PCI Pullups

RP39 10P8R_8.2K: REQ0# REQ1# REQ2# REQ3# → GNT0# GNT1# GNT2# GNT3#, +3V
RP36 10P8R_8.2K: STOP# TRDY# FRAME# IRDY# → SERR# DEVSEL# PERR# PLOCK#, +3V
RP41 10P8R_8.2K: PIRQA# PIRQB# PIRQC# PIRQD# → REQ4# GNT4# IRQ14 IRQ15, +3V

CLKRUN# R452 10K +3V
REQA# R552 8.2K +3V
REQB# R532 8.2K +3V
GNTA# R554 100K +3V
GNTB# R531 100K +3V
SERIRQ R512 8.2K +3V
PME# R467 10K 3V_S5
PIRQE# R535 10K +3V

Device ID	AD19	AD21	---	---	AD20	AD18
PIRQA#		TI1420		DOCKING		
PIRQB#			ATI P6	DOCKING	MINI PCI 1	MINI PCI 2
PIRQC#	ES1988			DOCKING		
PIRQD#				DOCKING	MINI PCI 1	MINI PCI 2
PIRQE#						
REQ0# GNT0#				DOCKING		
REQ1# GNT1#					MINI PCI 1	
REQ2# GNT2#		TI1420				
REQ3# GNT3#	ES1988					
REQ4# GNT4#						MINI PCI 2
REQA# GNTA#				DOCKING		
REQB# GNTB#		TI1420				
SERIRQ		TI1420		DOCKING		

SERIRQ PC87393F

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	ICH3-M (CPU,PCI,IDE)-1	3A

Date: Tuesday, September 11, 2001 Sheet 11 of 57

@. G1 put in the SODIMM area.

ICH HUB

0322: Del GPIO41-42

EPSON MC-306 (12.5pF 10PPM)

RTC

BATT_AHL03014003(ML1220)
BATT_CONN_DFHS02FS021

C2_0425: Change size

C2_0425: Move & close U67

Ramp_0620: Change for B0 stepping QB62

Ramp_0620: Change

C1_0402: Add for RTC leakage.Cover page3 item 29(0328).

C2_0423: Add

C2_0423: Change value

C2_0509: Change pwr

AC_shut bit set to 1

Add for EMI

For RTC leakage

0322: Add

C2_0518: For leakage

C1_0323: Add for RTC leakage.

DEL USB PULL LOW 1.5K R559-R564, R541-R546

HUBVSWING = 0.5 * VCC1_8

Place divider in the middle of the bus

ICH3_F

PROJECT : RT2.0	Quanta Computer Inc.
Size: Custom	Document Number: ICH3-M (USB,HUB,LPC)-2
Rev: 3A	
Date: Tuesday, September 11, 2001	Sheet 12 of 57

ICH3

U67C

VCC

ICH3_F

B2: Change size from 0805 to 0603

R432 1K

D25 RB500

5VREF_RUN

+1.8V 500mA

@. One power pins put one bypass Cap.

+1.5V 45mA

1.8VAUX

3.3VAUX

+1.8V_ICH3_LAN1

+3V_ICH3_LAN3

ICH3

U67D

GND

ICH3_F

T75 *PAD

T67 *PAD

T73 *PAD

T68 *PAD

T72 *PAD

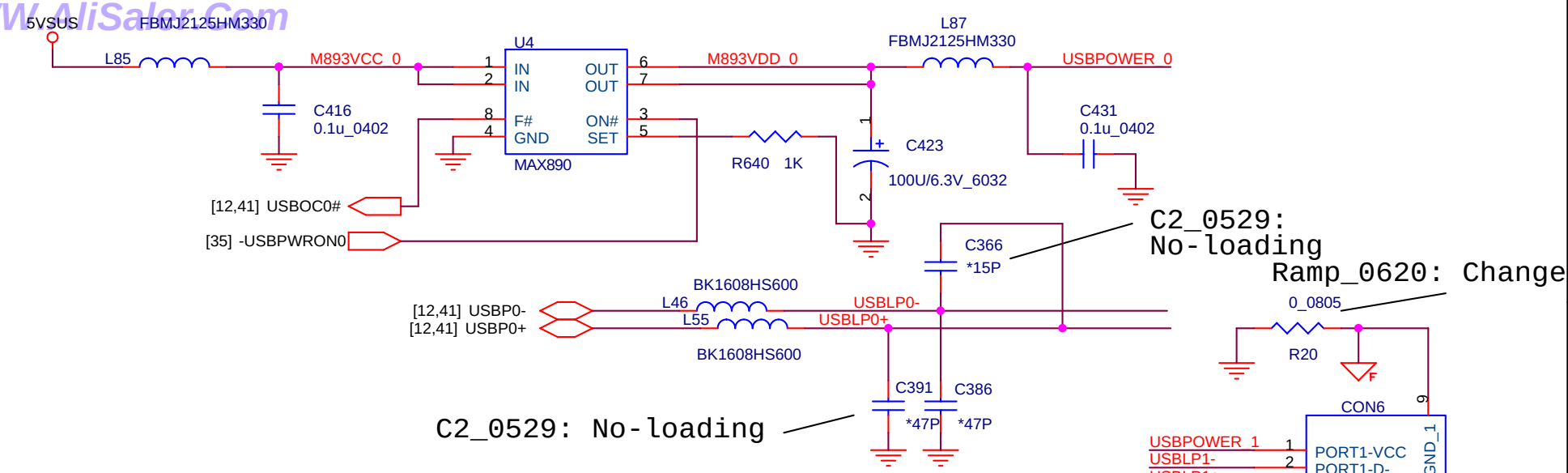
@. One power pins put one bypass Cap.

@. One power pins put one bypass Cap.

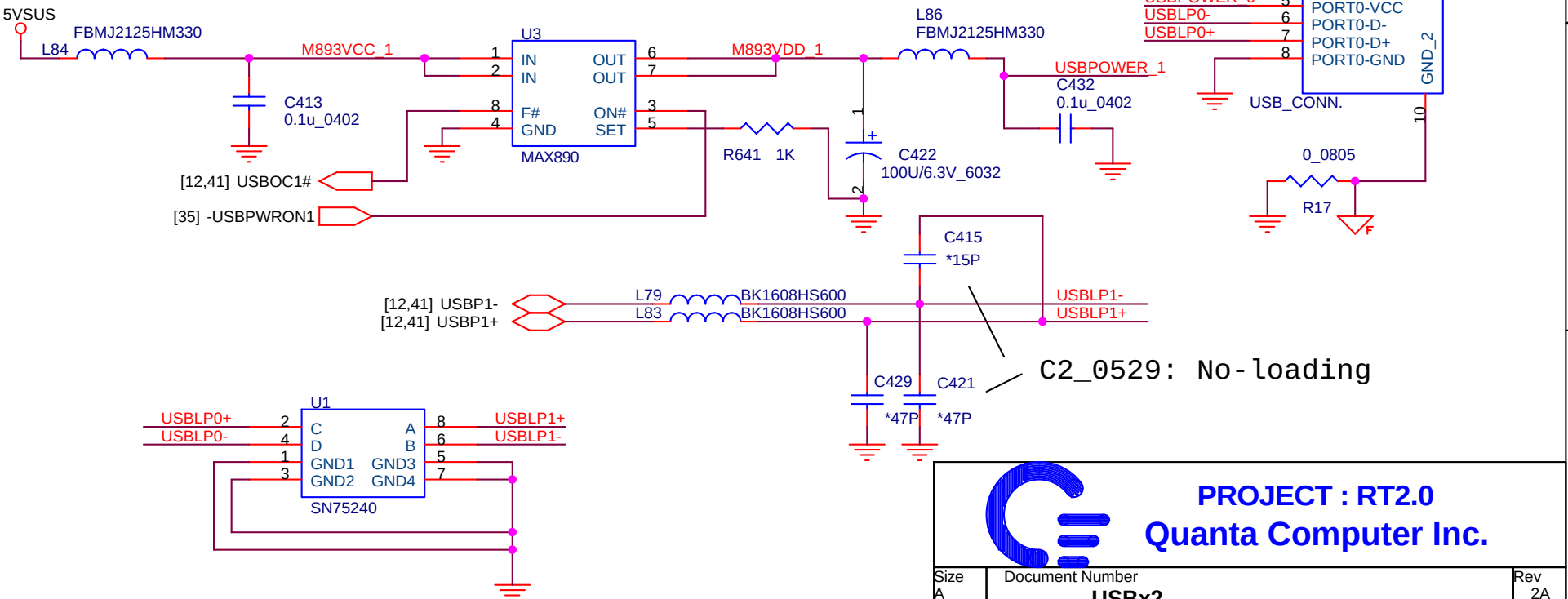
PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH3-M (POWER&GND)-3	2B

Date: Tuesday, September 11, 2001 Sheet 13 of 57



USB CONNECTOR



PROJECT : RT2.0		
Quanta Computer Inc.		
Size A	Document Number USBx2	Rev 2A
Date: Tuesday, September 11, 2001	Sheet 14 of 57	

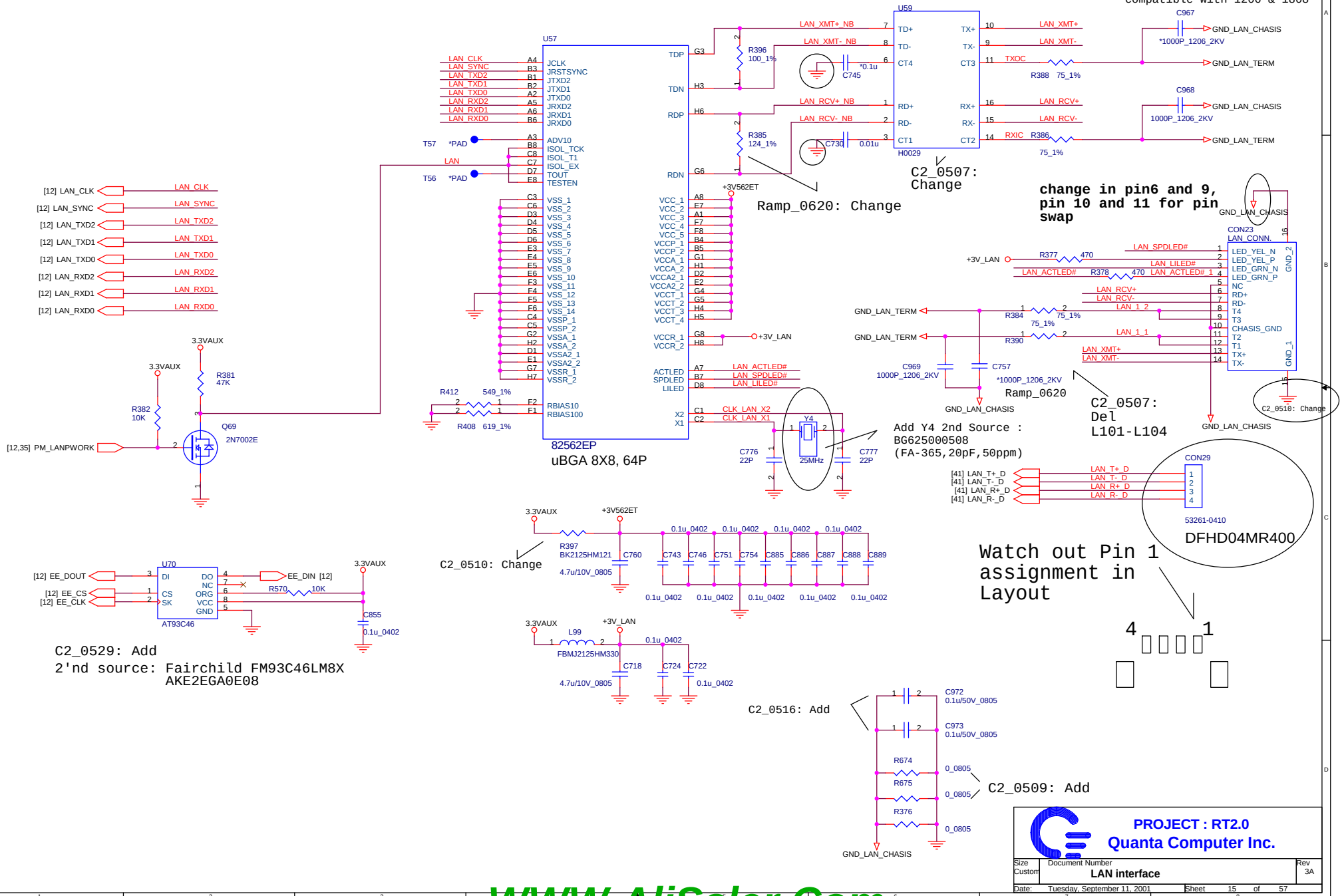
C2_0507: Del

LAN PHY

2nd Source ATP119: DB0TM7LAN22

Pulse H0029 (Same as H0022, but lower cost)

Ramp_0620:
C967-969,C757: foot print is compatible with 1206 & 1808



PROJECT : RT2.0	Quanta Computer Inc.
Size: Custom	Document Number: LAN interface
Rev: 3A	
Date: Tuesday, September 11, 2001	Sheet 15 of 57

Change pullup power plane

Ramp_0620: Change to new part number

HDD connector

C1_0328: Change to 1M from 100K

2A: ADD

0322

C1_0403: Change to NAND, add DTC144EU,10K.

C1_0328: Add

C1_0323: Add

RP34 8P4R_33: [11] PDD7 → IDEPD7; [11] PDD6 → IDEPD6; [11] PDD5 → IDEPD5; [11] PDD4 → IDEPD4

RP37 8P4R_33: [11] PDD3 → IDEPD3; [11] PDD2 → IDEPD2; [11] PDD1 → IDEPD1; [11] PDD0 → IDEPD0

RP42 8P4R_33: [11] PDA2 → R_PDA2; [11] PDA1 → R_PDA1; [11] IRQ14 → R_IRQ14; [11] PDDACK# → -R_PDDACK

RP11 8P4R_33: [11] PDD8 → IDEPD8; [11] PDD9 → IDEPD9; [11] PDD10 → IDEPD10; [11] PDD11 → IDEPD11

RP12 8P4R_33: [11] PDD15 → IDEPD15; [11] PDD14 → IDEPD14; [11] PDD13 → IDEPD13; [11] PDD12 → IDEPD12

RP43 8P4R_33: [11] PDA0 → R_PDA0; [11] PDCS3# → -R_PDCS3; [11] PDCS1# → -R_PDCS1

[11] PDDREQ → PDDREQ R155 33 R_PDDREQ
[11] PDIOW# → PDIOW# R156 33 -R_PDIOW
[11] PDIOR# → PDIOR# R157 33 -R_PDIOR
[11] PIORDY → PIORDY R160 33 R_PIORDY
[36] -HDDLED → -HDDLED

HDD_VCC
R_PIORDY R161 1K
PDDREQ R154 5.6K
PDD7 R147 10K

CON18 (HDD_CONN.)
-HDRESET 1 | IDEPD7 3 | IDEPD6 5 | IDEPD5 7 | IDEPD4 9 | IDEPD3 11 | IDEPD2 13 | IDEPD1 15 | IDEPD0 17 | 19
R_PDDREQ 21 | -R_PDIOW 23 | -R_PDIOR 25 | R_PIORDY 27 | -R_PDDACK 29 | R_IRQ14 31 | R_PDA1 33 | R_PDA0 35 | -R_PDCS1 37 | 39 | 41 | 43
2 | IDEPD8 4 | IDEPD9 6 | IDEPD10 8 | IDEPD11 10 | IDEPD12 12 | IDEPD13 14 | IDEPD14 16 | IDEPD15 18 | 20 | 22 | 24 | 26 | PSEL 28 | 30 | 32 | 34 | R_PDA2 36 | -R_PDCS3 38 | 40 | 42 | 44
-HDDLED
HDD_VCC
C864 100P
C349 0.1u_0402
0.1u_0402 C350
R159 470

HDD_VCC
R663 10K
-HDRESET
C942 0.1u_0402
C295 100P
+3V
[12] RST_HDD#
[6,11,18,25,28,30,31,41,51] PCIRST#
U83 TC7SH00FU
Q113 DTC144EU

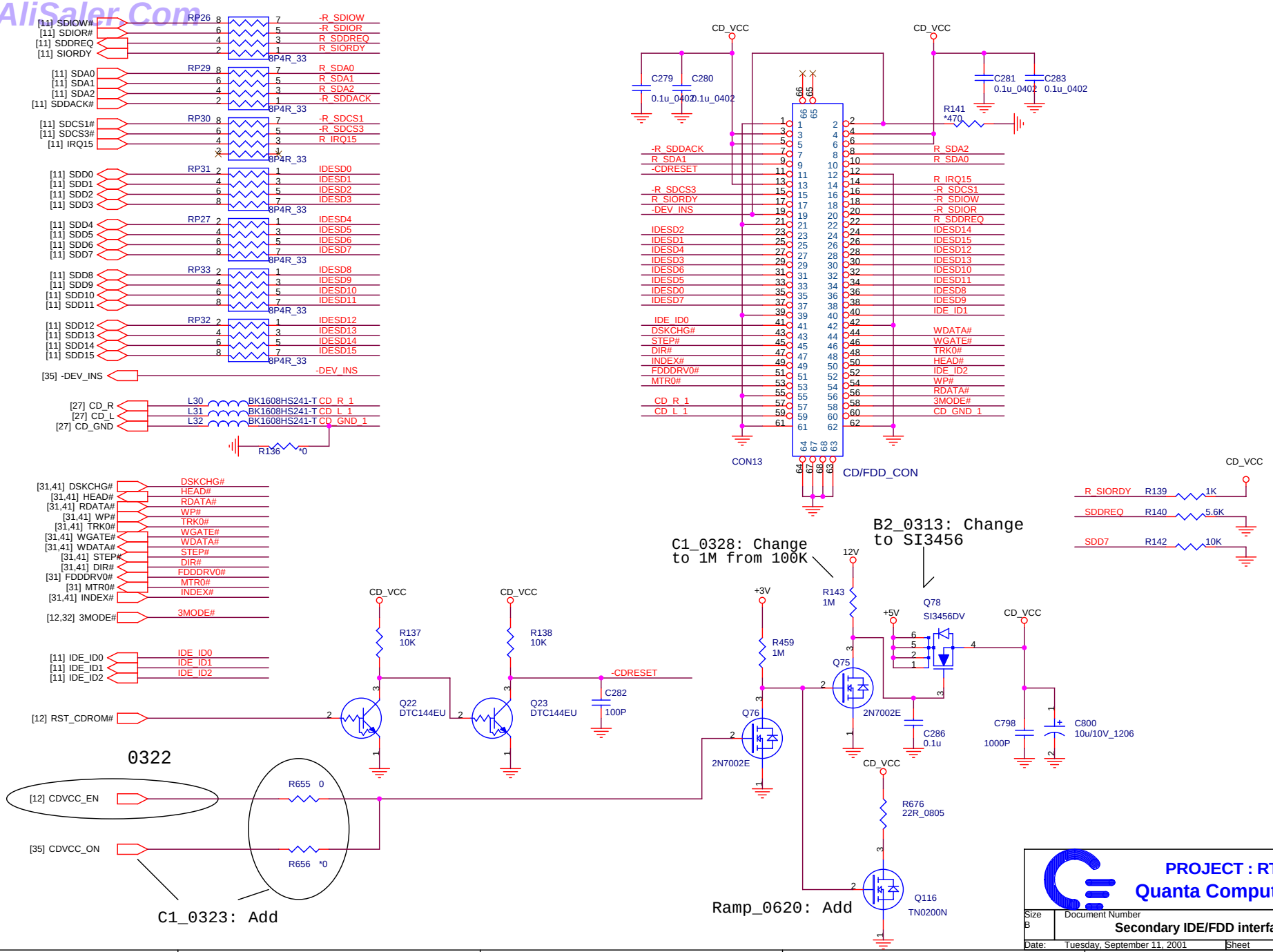
+3V
R629 1M
12V
+5V
Q101 SI3456DV
HDD_VCC
R631 1M
Q104 2N7002E
C897 0.1u_0402
C896 10u/10V/Tan_1206
C943 0.1u_0402

Q106 2N7002E
R653 0
R654 *0
[12] HDDVCC_EN
[35] HDDVCC_ON

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
A	Primary IDE (HDD interface)	3A

Date: Tuesday, September 11, 2001 Sheet 16 of 57



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	Secondary IDE/FDD interface	3A
Date: Tuesday, September 11, 2001	Sheet 17 of 57	

ATI P6

U47A

C2_0517: Add L,C for EMI

C1 Test_0402: Add for D3 cold, but reserved.

C2_0423: Change net name from<ZV_SCLK>

C1 Test_0402: Change

C1 Test_0402: Change

(Optional) SHFCLK spread spectrum control

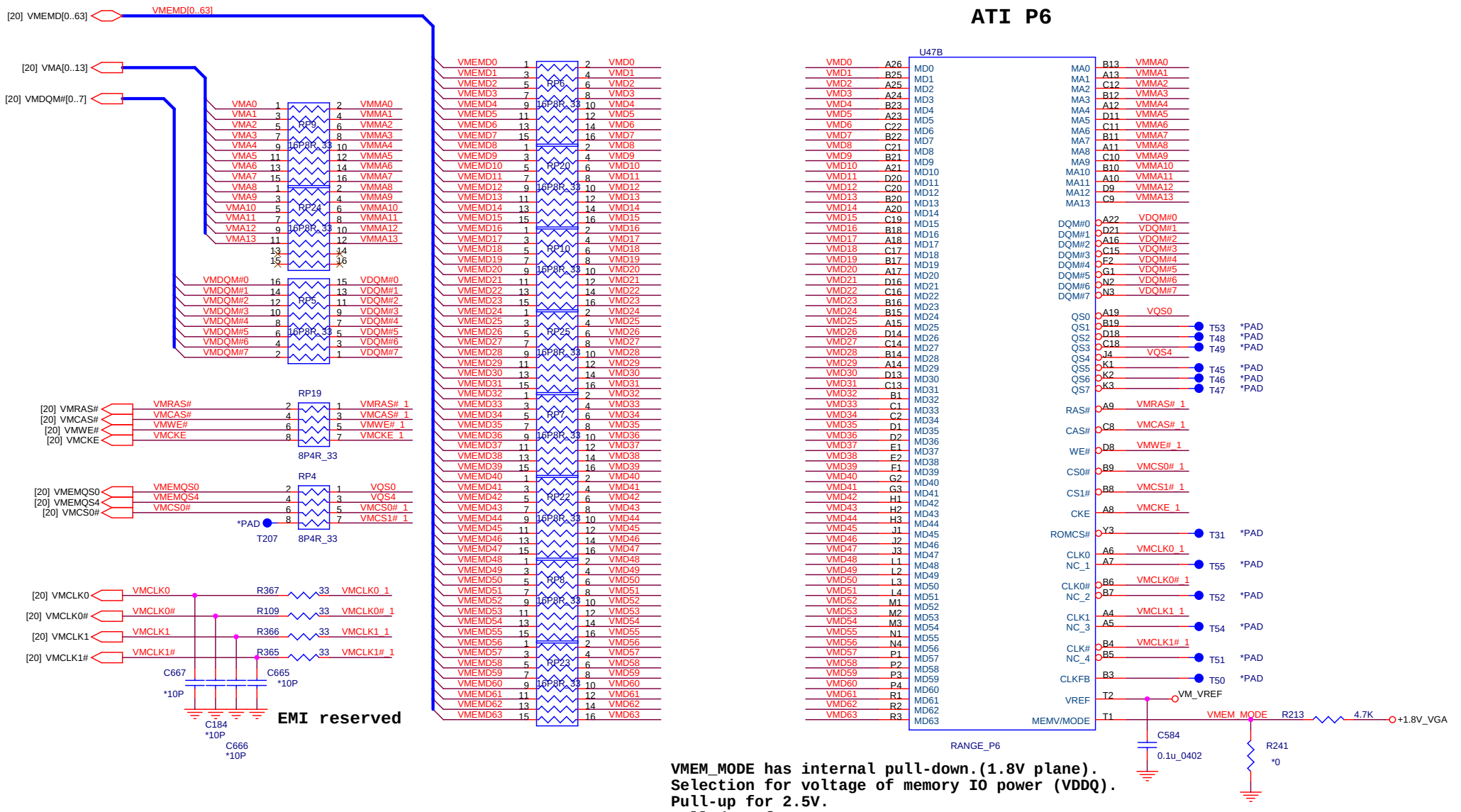
LEE is internal pull high. high for enable EMI function

PIRQB#

TXC 6P27000019

RANGE_P6

PROJECT : RT2.0	Quanta Computer Inc.
Size C	Document Number: ATI P6 (HOST, VIDEO O/P)-1
Rev 3A	
Date: Tuesday, September 11, 2001	Sheet 18 of 57



VMEM_MODE has internal pull-down.(1.8V plane).
Selection for voltage of memory IO power (VDDQ).
Pull-up for 2.5V.
pull-down for 3.3V.

Both samsung's and hyundai's sdram are 2.5V on VDDQ.

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	ATI P6 (VRAM)-2	1A

Date: Tuesday, September 11, 2001 Sheet 19 of 57

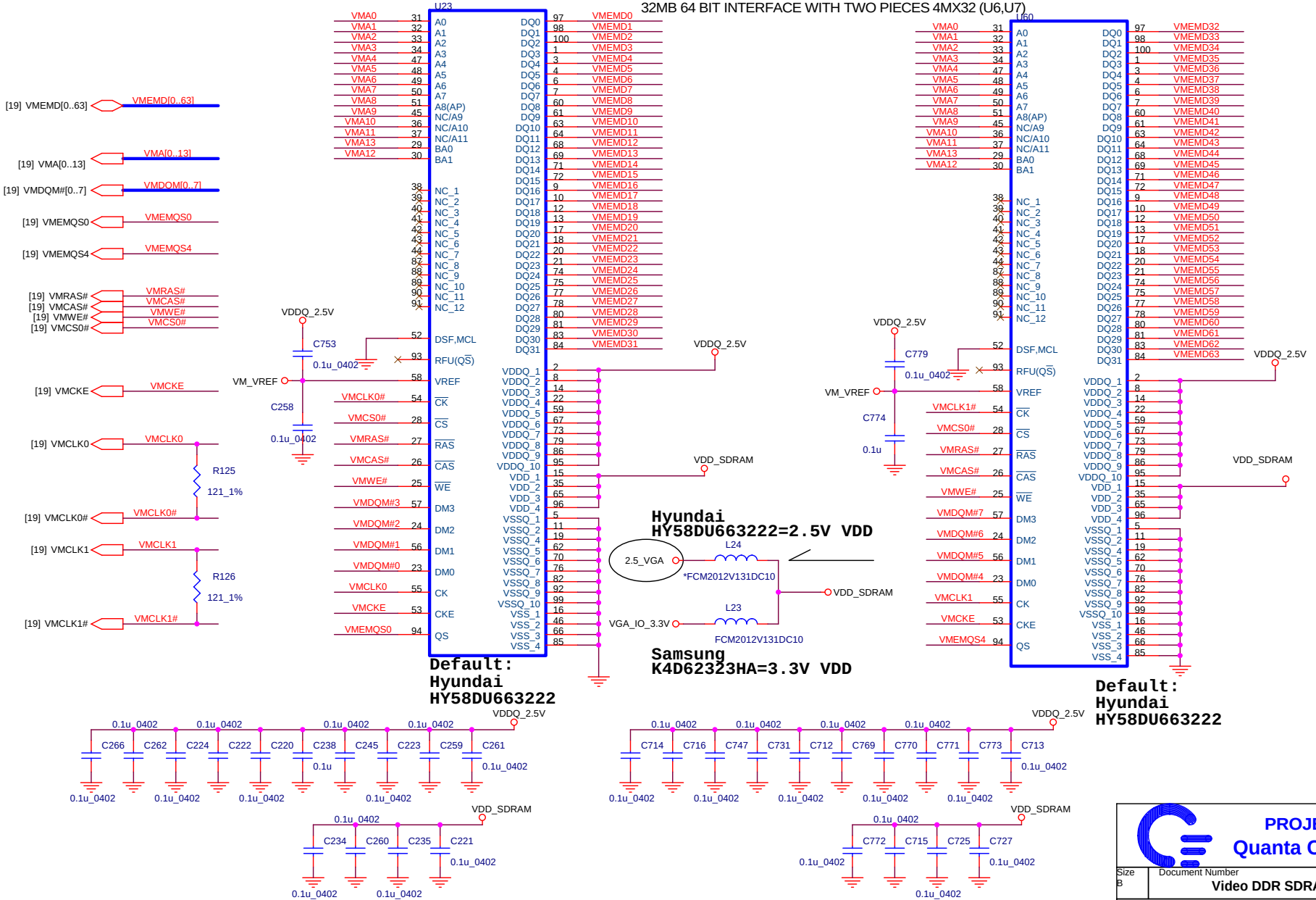
8/16/32MB DDR 2/4MX32 SDRAM

8MB 32 BIT INTERFACE WITH ONE PIECE 2MX32 (U6)

8MB 64 BIT INTERFACE WITH TWO PIECES 2MX32 (U6,U7)

16MB 32 BIT INTERFACE WITH ONE PIECE 4MX32 (U6)

32MB 64 BIT INTERFACE WITH TWO PIECES 4MX32 (U6,U7)

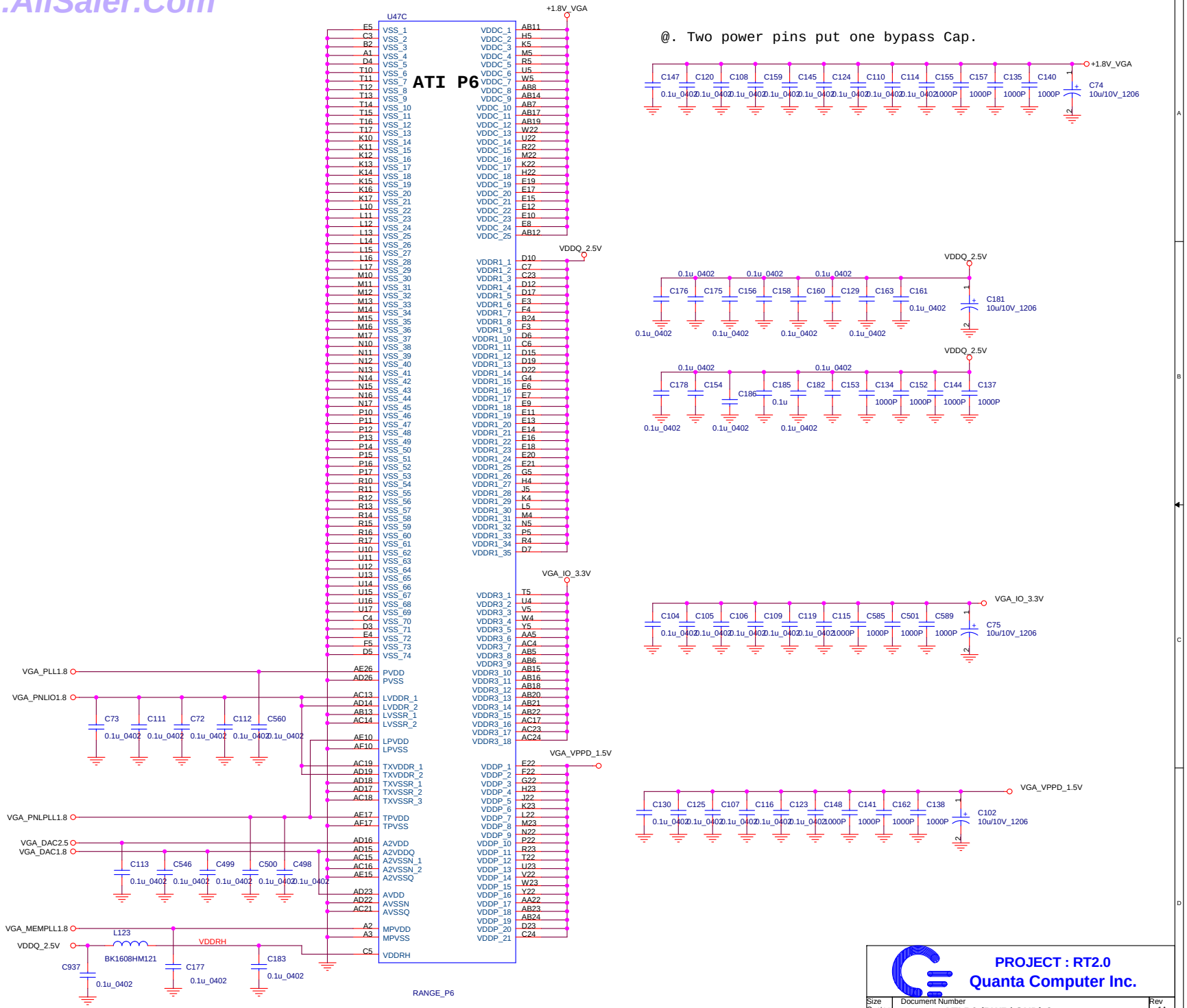


PROJECT : RT2.0

Quanta Computer Inc.

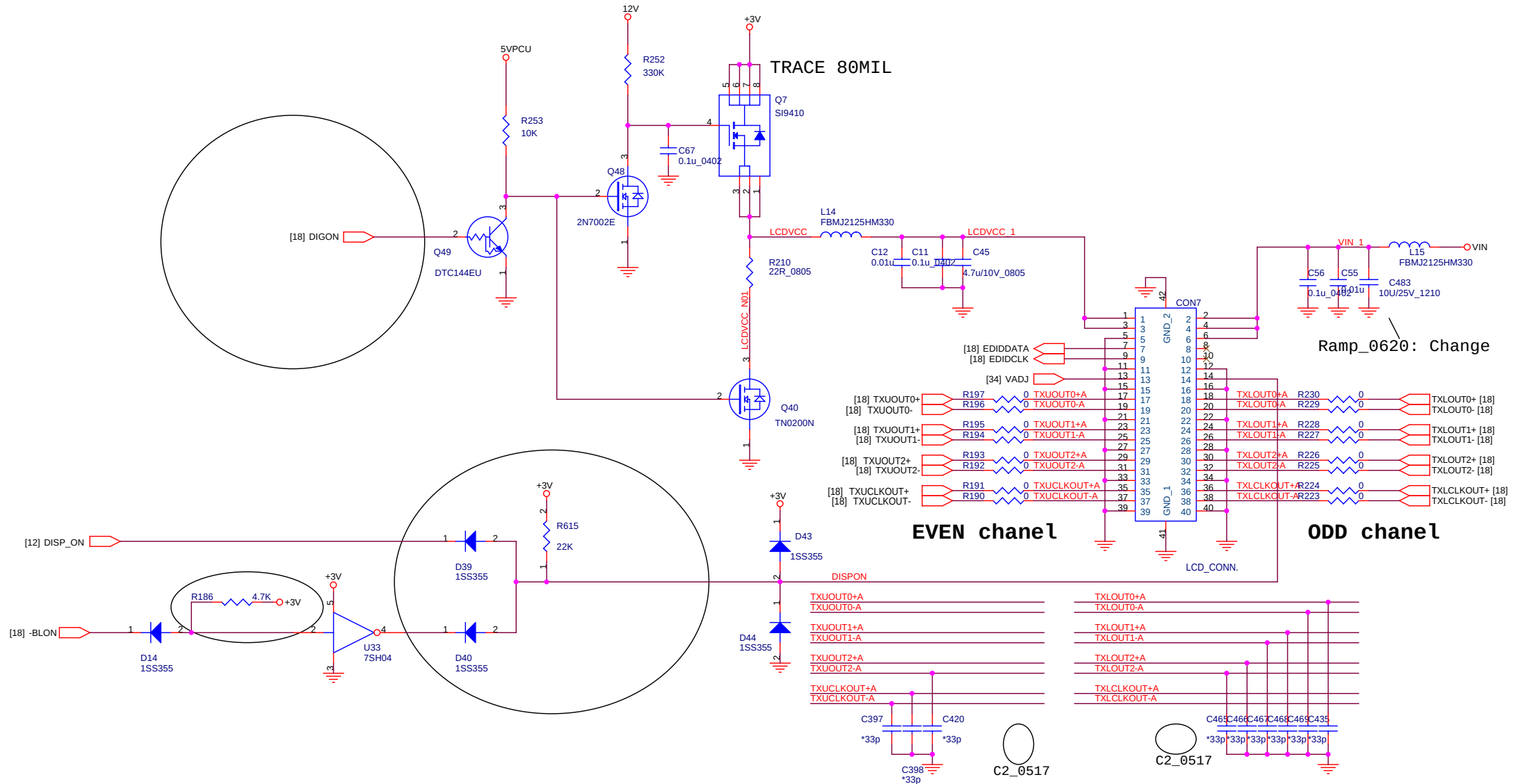
Size	Document Number	Rev
B	Video DDR SDRAM	2B

Date: Tuesday, September 11, 2001 Sheet 20 of 57



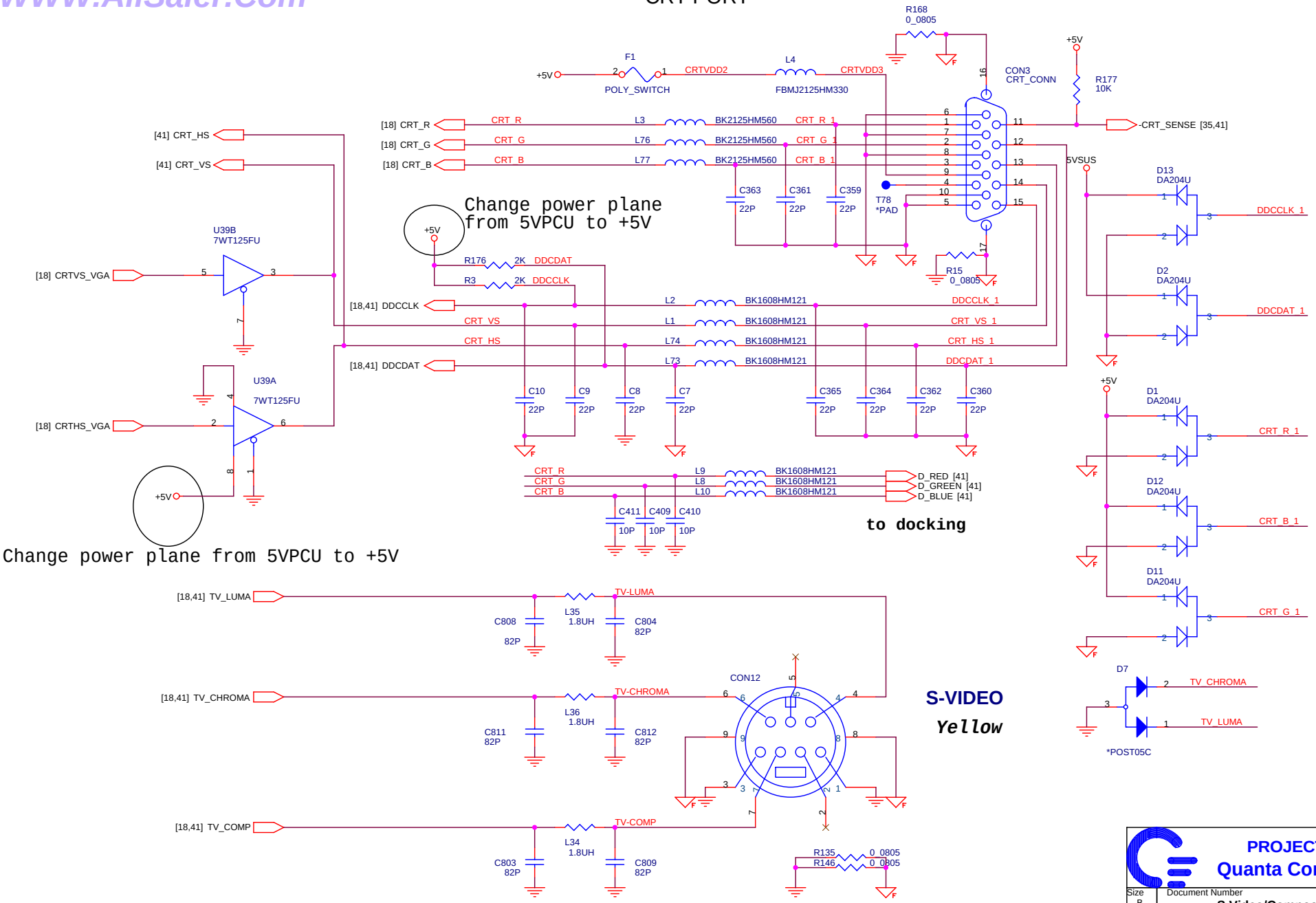
@. Two power pins put one bypass Cap.

PROJECT : RT2.0		
Quanta Computer Inc.		
Size: Custom	Document Number: ATI P6 (PWR/ GND)-3	Rev: 1A
Date: Tuesday, September 11, 2001	Sheet 21 of 57	



PROJECT : RT2.0		
Quanta Computer Inc.		
Size: B	Document Number: LCD interface	Rev: 2A
Date: Tuesday, September 11, 2001	Sheet 22 of 57	

CRT PORT



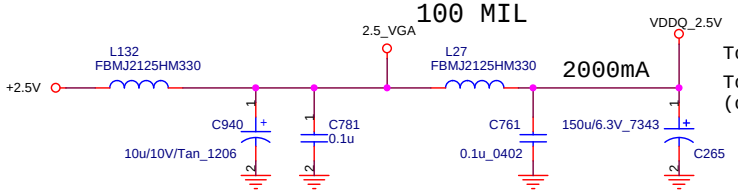
PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	S Video/Composite,CRT	1A

Date: Tuesday, September 11, 2001 Sheet 23 of 57

For DDR SDRAM VDDQ & P6 VDDR1

B2_0324: 100 MIL



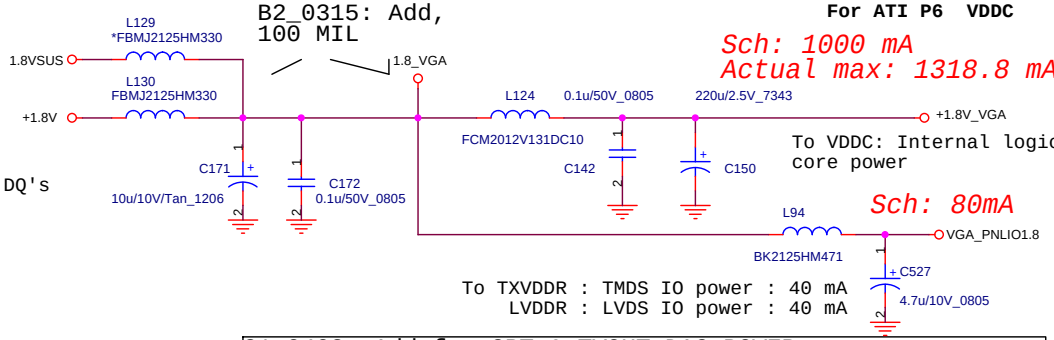
To VDDR1: Memory IO power

To VDDQ of DDR SRRAM: Power for DQ's (output buffers)

B2_0315: Add, 100 MIL

For ATI P6 VDDC

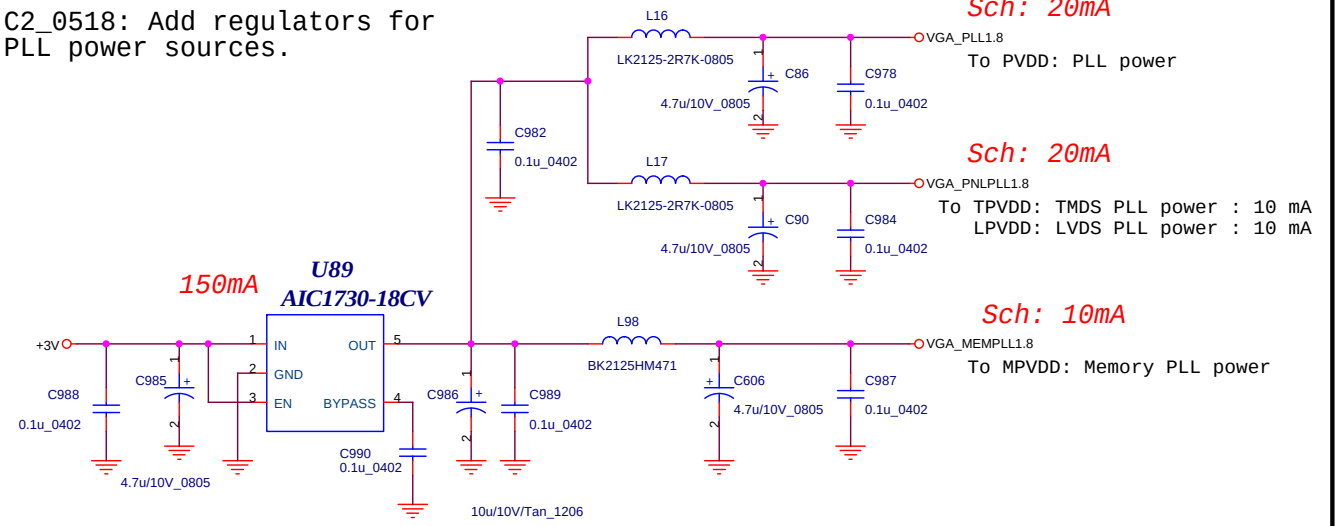
Sch: 1000 mA
Actual max: 1318.8 mA



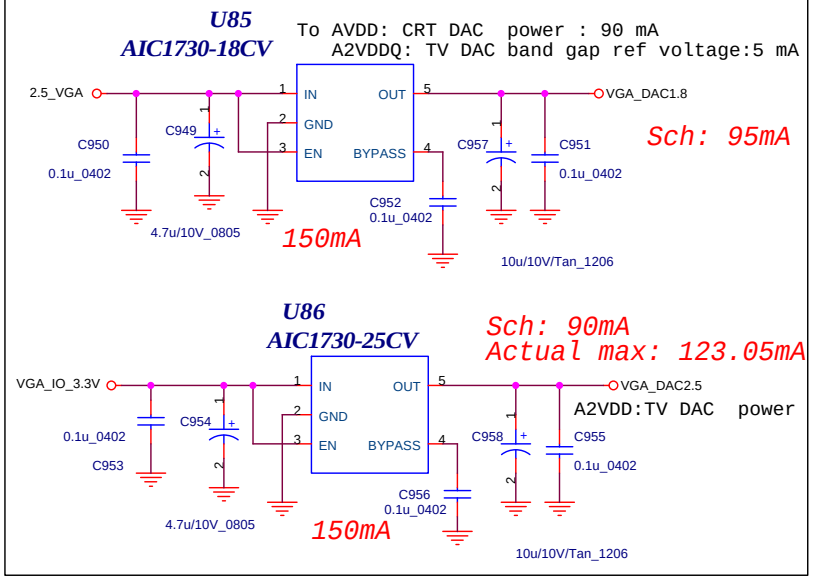
To VDDC: Internal logic core power

To TXVDDR : TMDS IO power : 40 mA
LVDDR : LVDS IO power : 40 mA

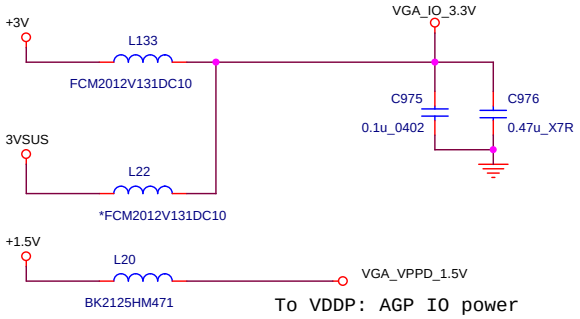
C2_0518: Add regulators for PLL power sources.



C1_0403: Add for CRT & TVOUT DAC POWER

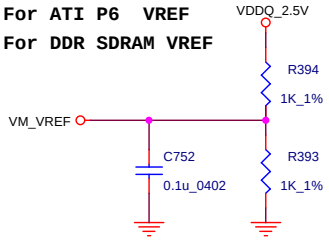


C2_0517: Add cap for EMI



To VDDP: AGP IO power

For ATI P6 VREF
For DDR SDRAM VREF

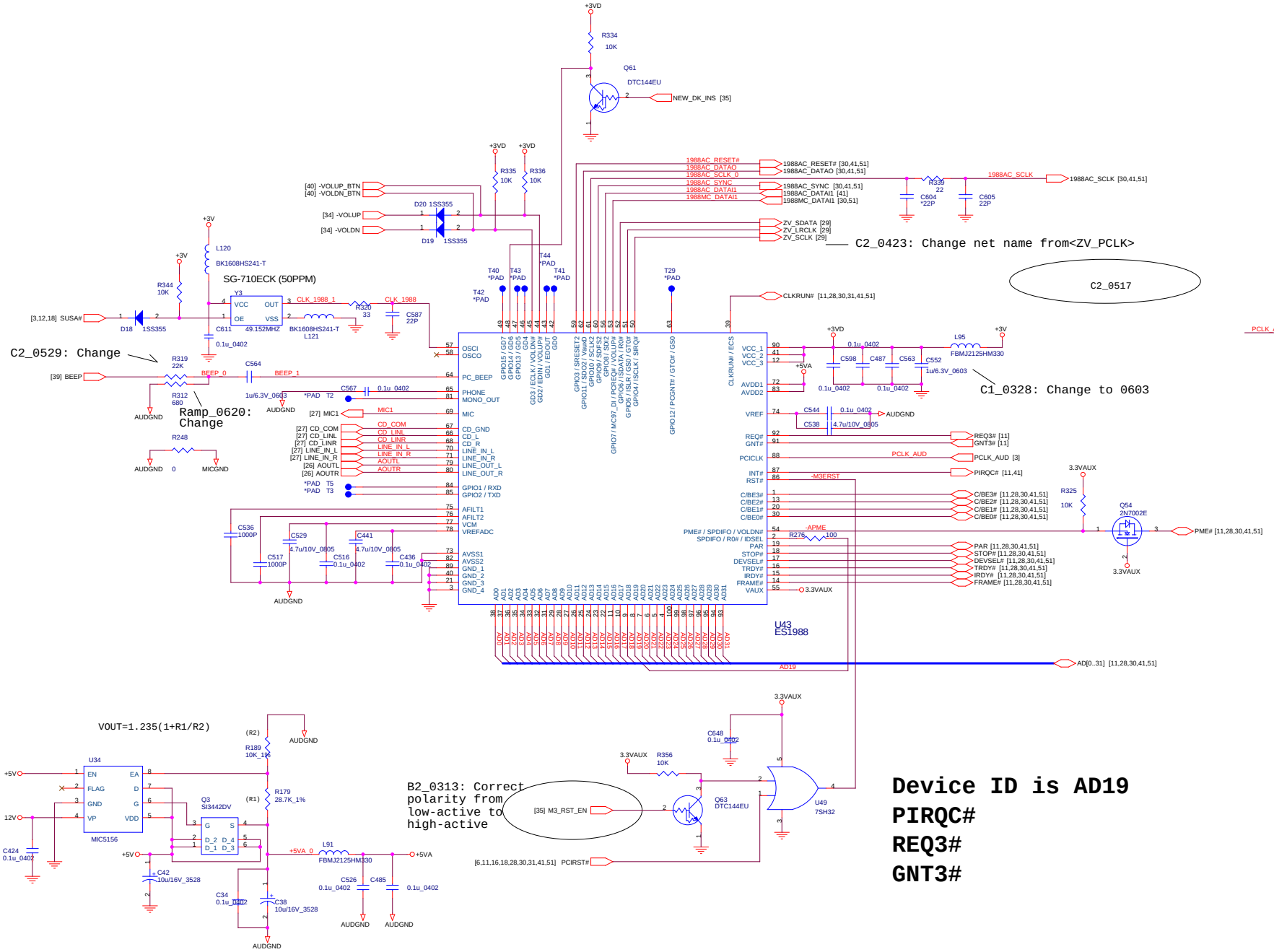


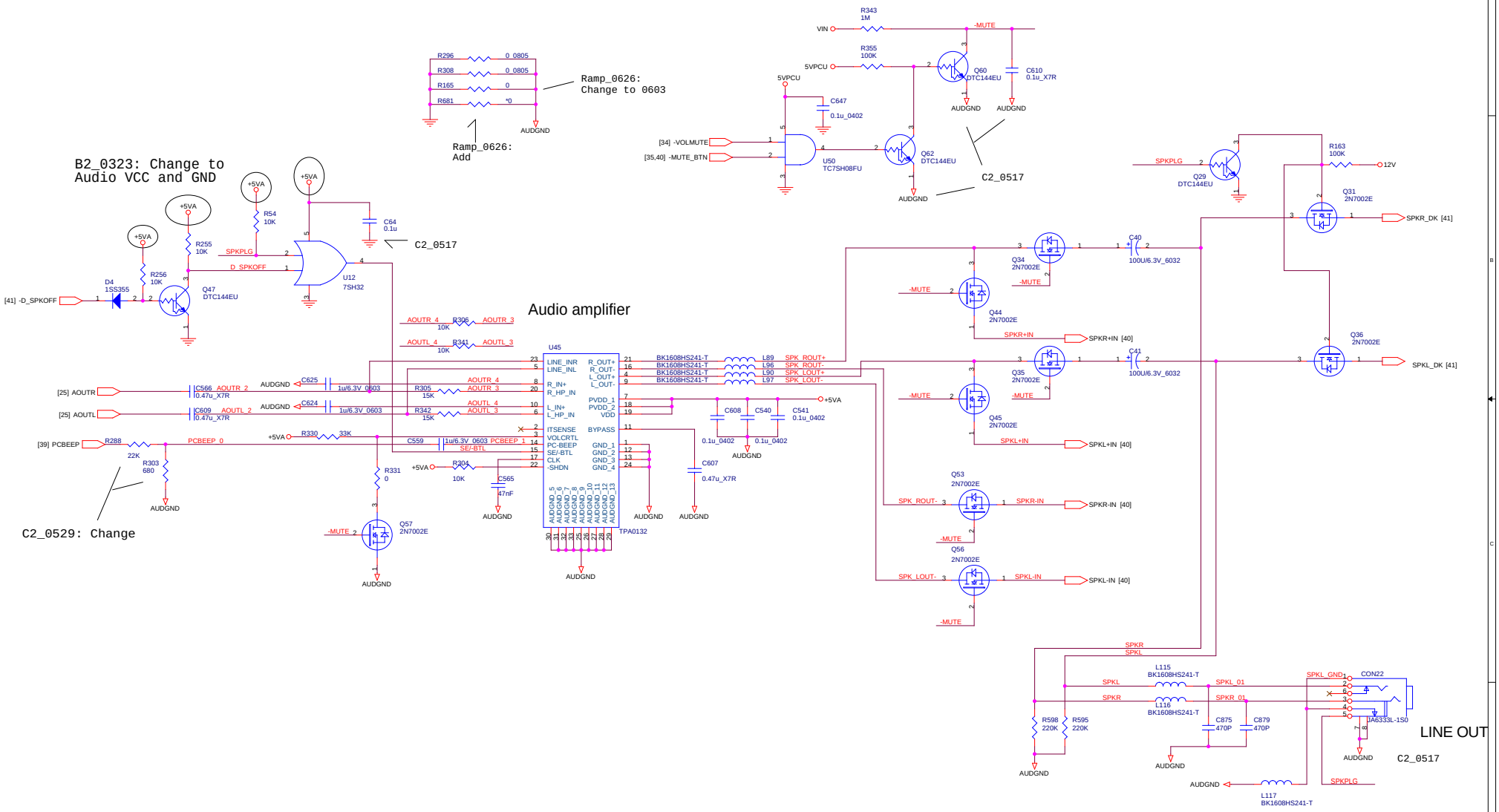
Power source option for ATI P6 power states selection		
ATI P6 power states	D3 cold	D3 hot
Control signals	MAINON	SUSON
Location \ Components options		
L133 L130 Page44: R661 Q110	Load	No load
L22 L129 Page44: PQ46 R662	No load	Load

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	VGA power	3A

Date: Tuesday, September 11, 2001 Sheet 24 of 57

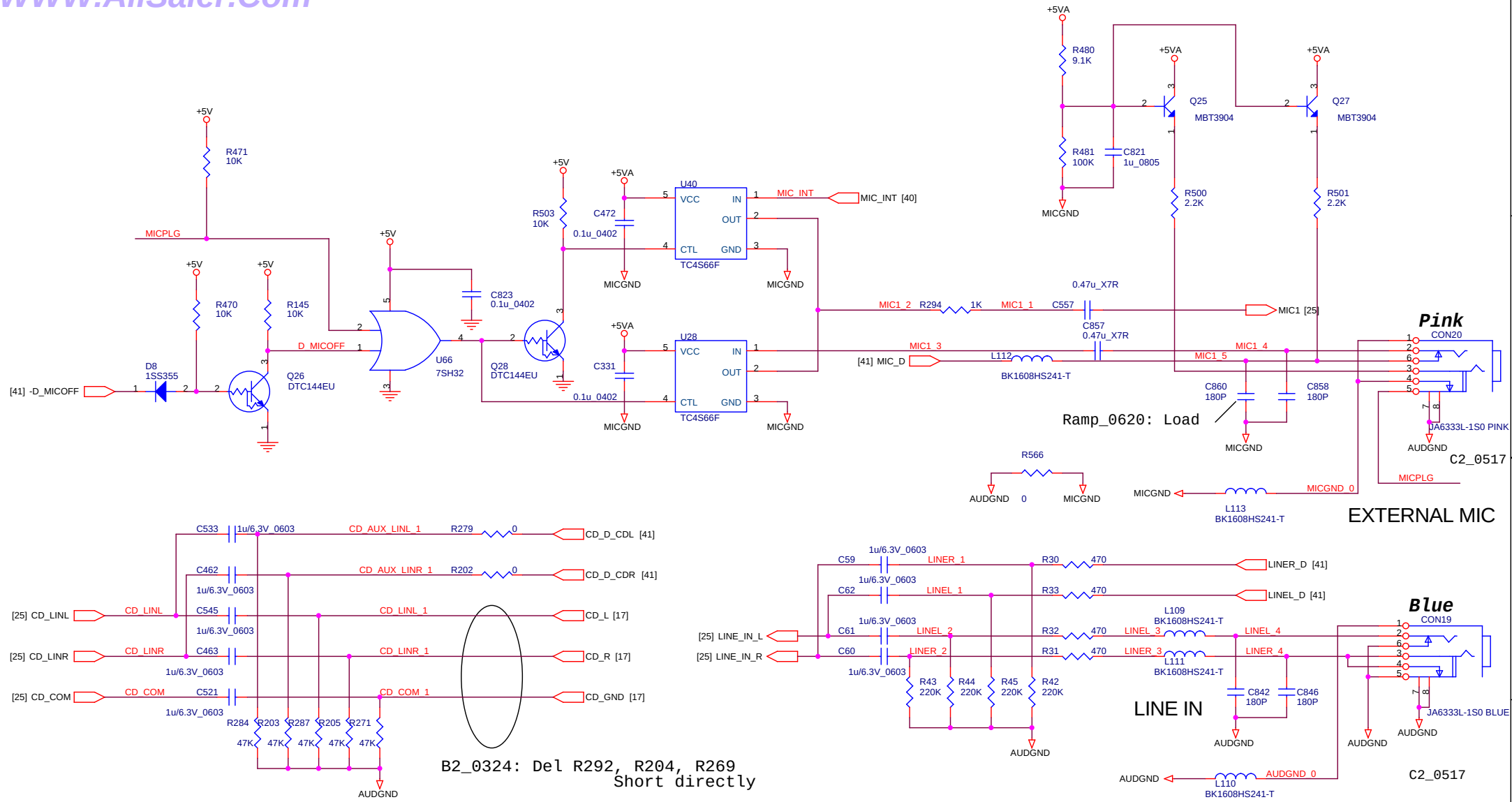




PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
C	AMP/line out	3A

Date: Tuesday, September 11, 2001 Sheet 26 of 57



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	line in/mic in/CD audio in	2B

Date: Tuesday, September 11, 2001 Sheet 27 of 57

C2_0425: Add

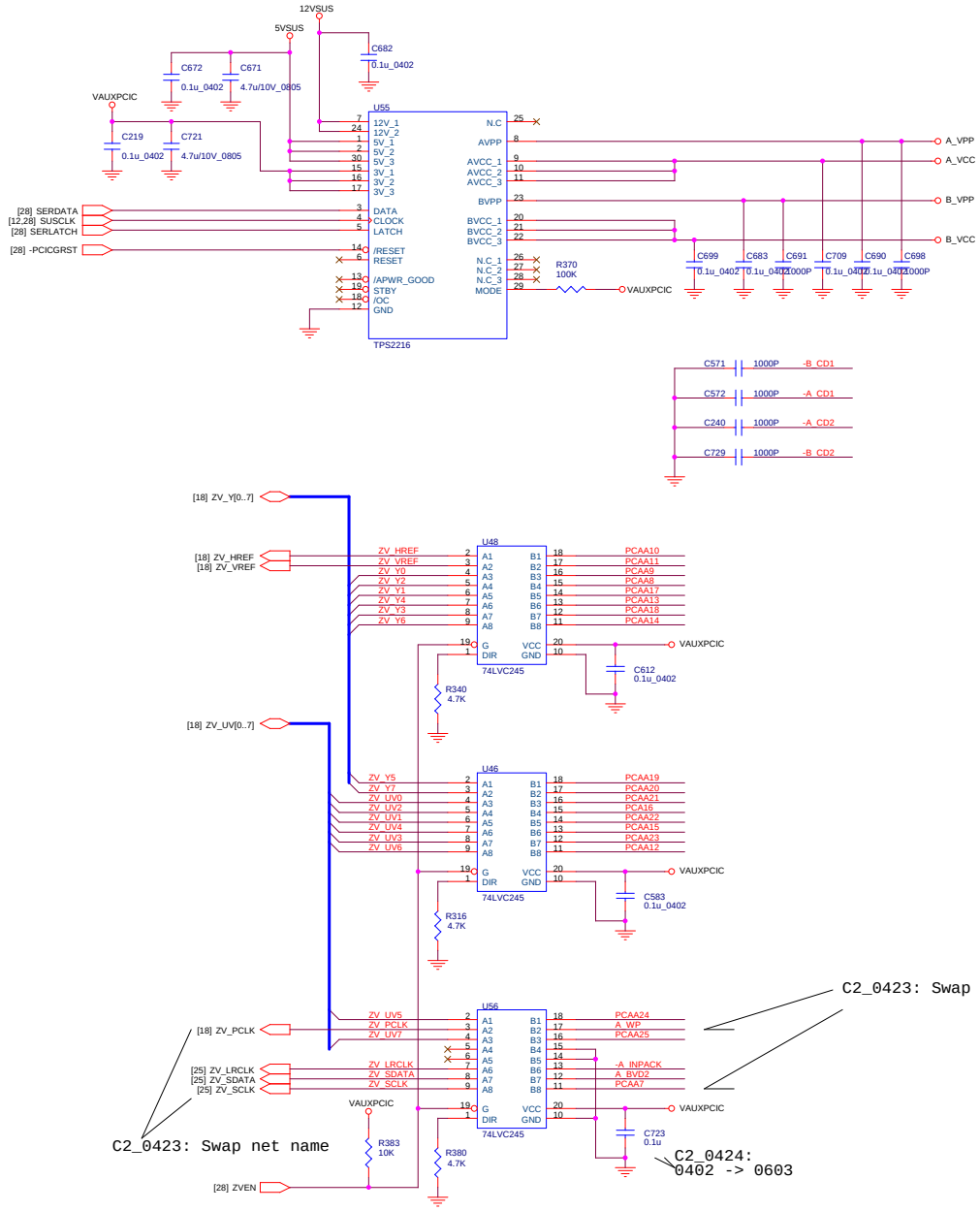
C2_0510: Add

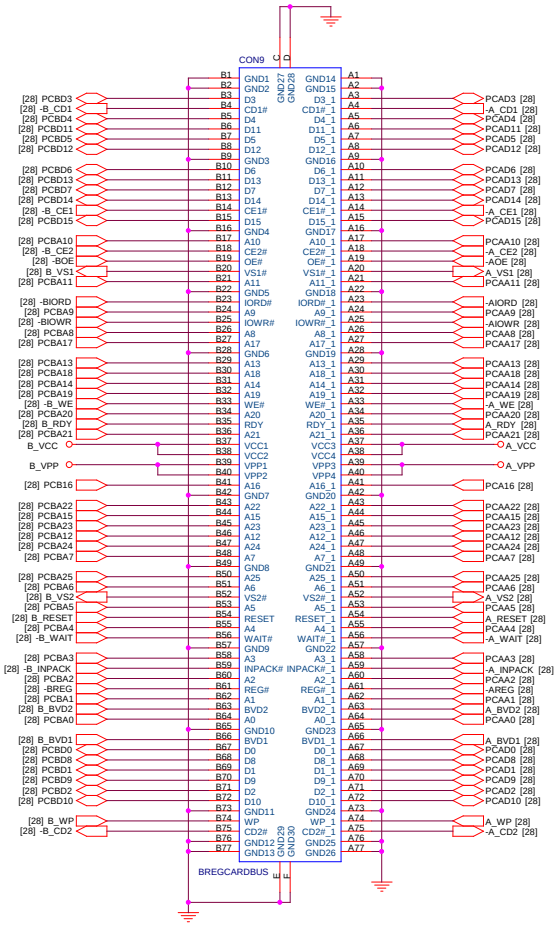
C1_0328: Change to 0603

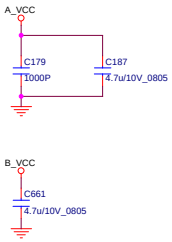
Device ID is AD21
SERIRQ
PIRQA#
REQ2#
GNT2#
REQB#
GNTB#

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
C	TI1420 CARDBUS CONTROLLER	3A
Date: Tuesday, September 11, 2001	Sheet 28 of 57	

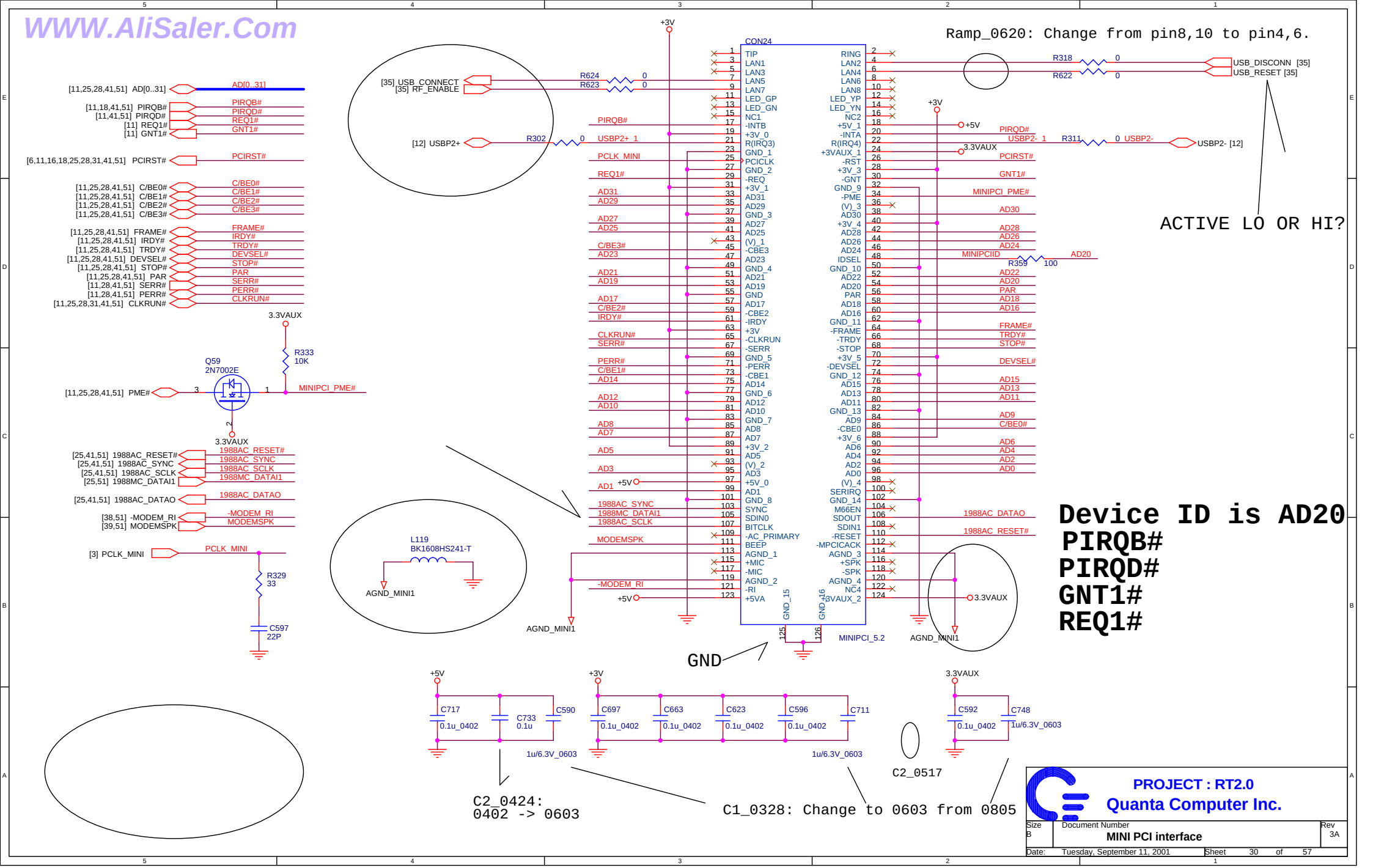




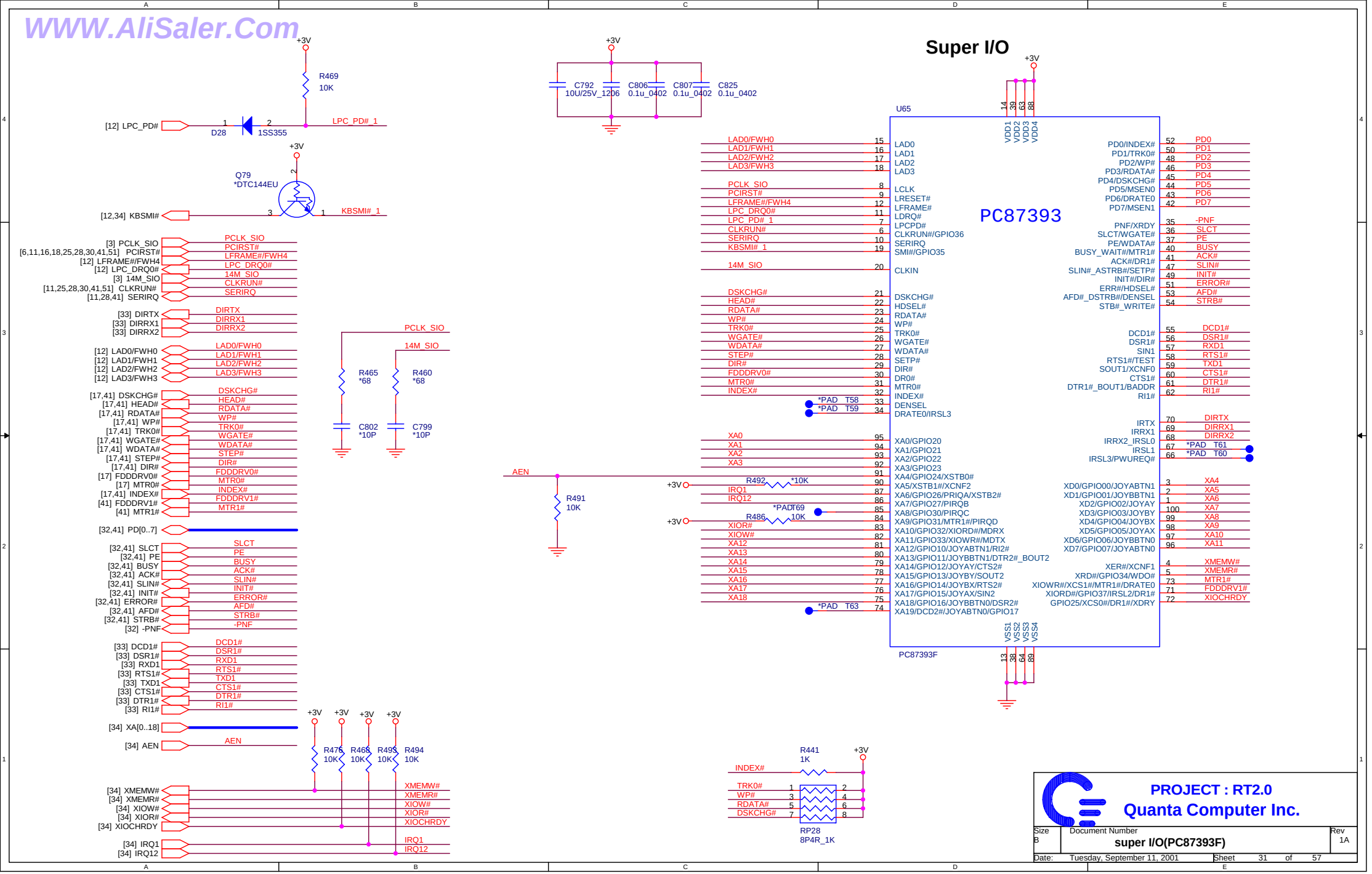


PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
C	CARDBUS interface	1A
Date: Tuesday, September 11, 2001	Sheet 29 of 57	



Super I/O



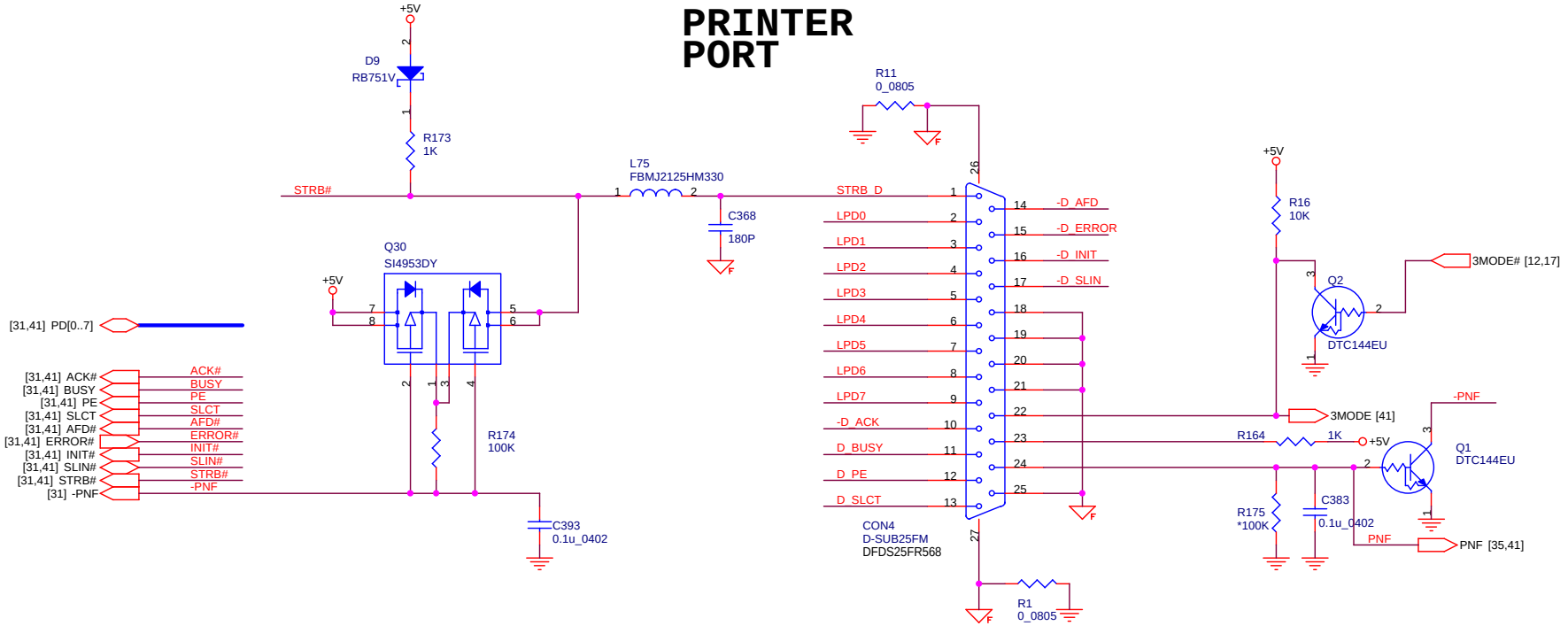
Size	Document Number	Rev
B	super I/O(PC87393F)	1A

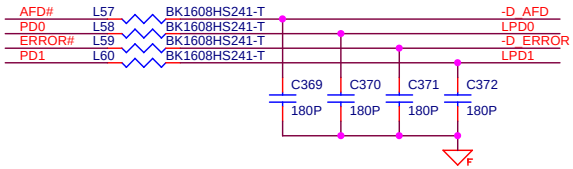
PROJECT : RT2.0

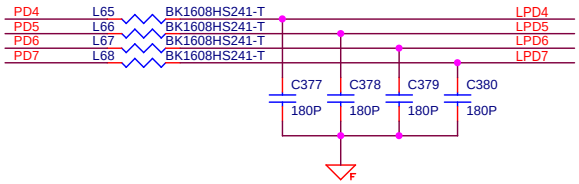
Quanta Computer Inc.

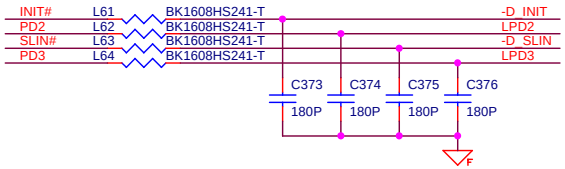
Date: Tuesday, September 11, 2001 Sheet 31 of 57

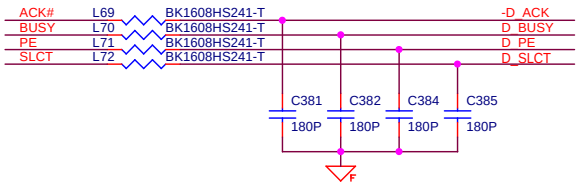
PRINTER PORT

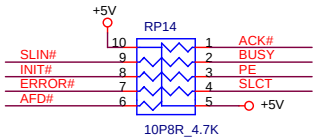


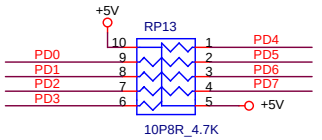








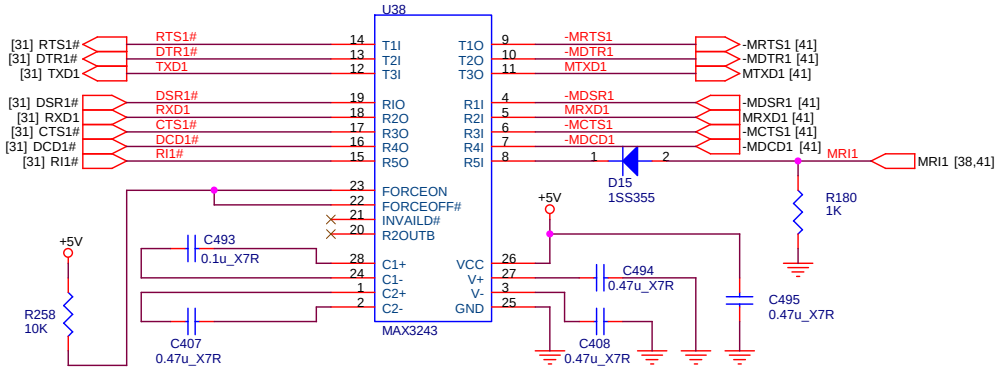


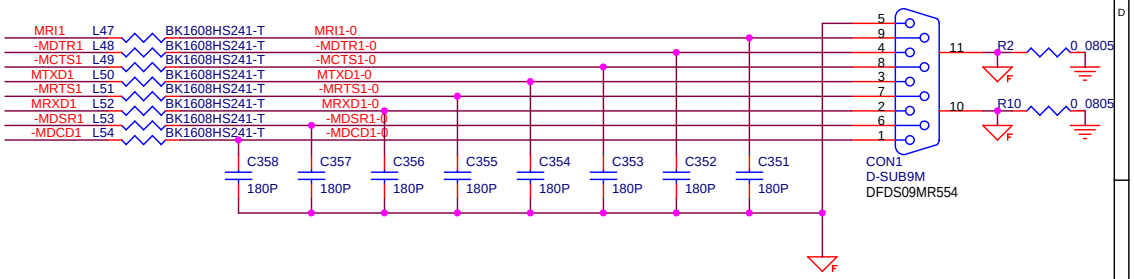


PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	LPT1/FDD interface	1A

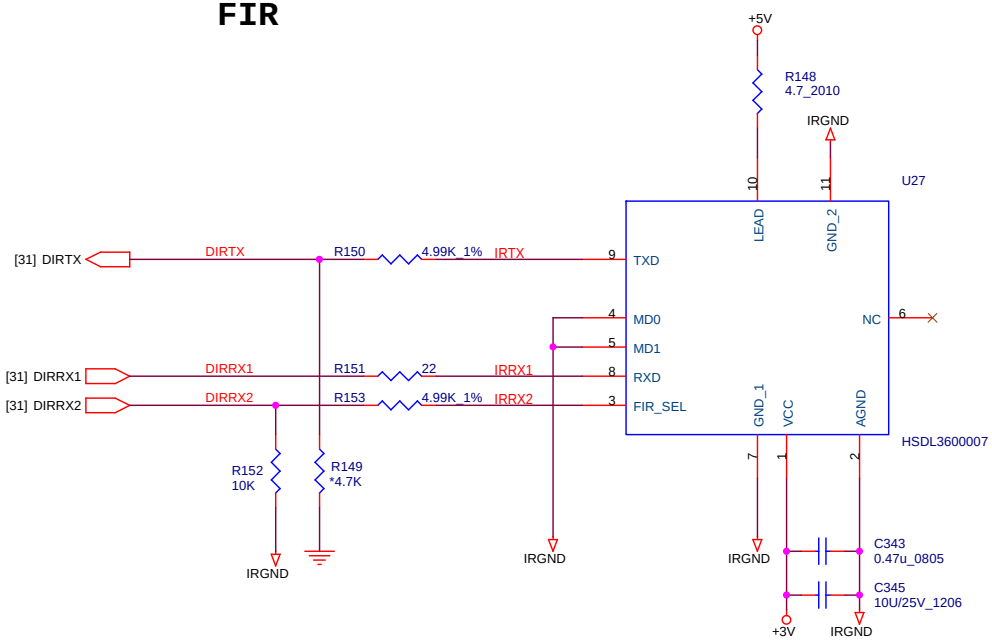
Date: Tuesday, September 11, 2001 Sheet 32 of 57



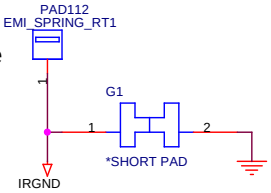


COM PORT

FIR



C2_0529: Change



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	COM/IR interface	3A
Date: Tuesday, September 11, 2001	Sheet 33 of 57	

NS87570 Version : C4, code:05

C1_0328: Change to 0603

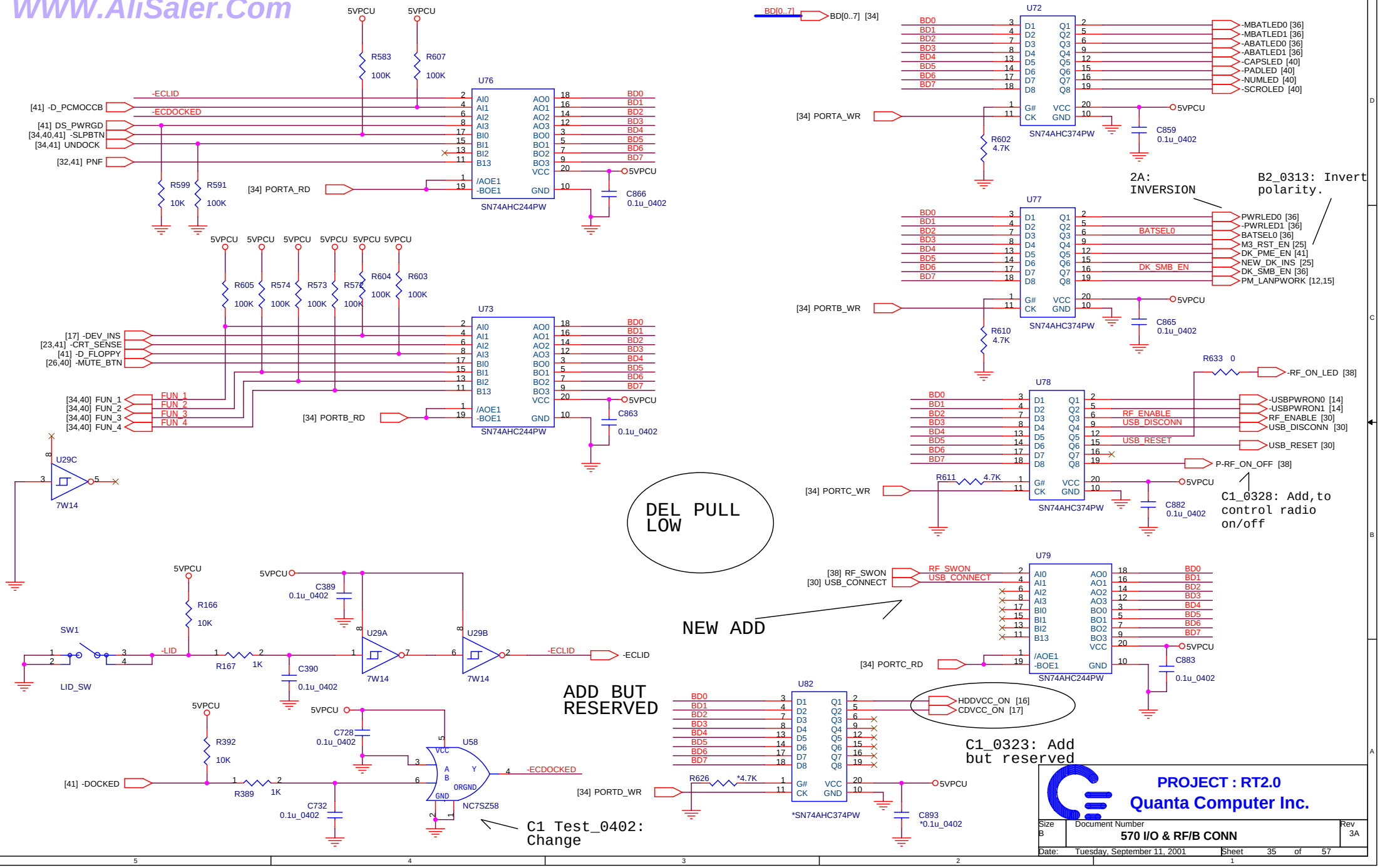
CLOSE TO NS570

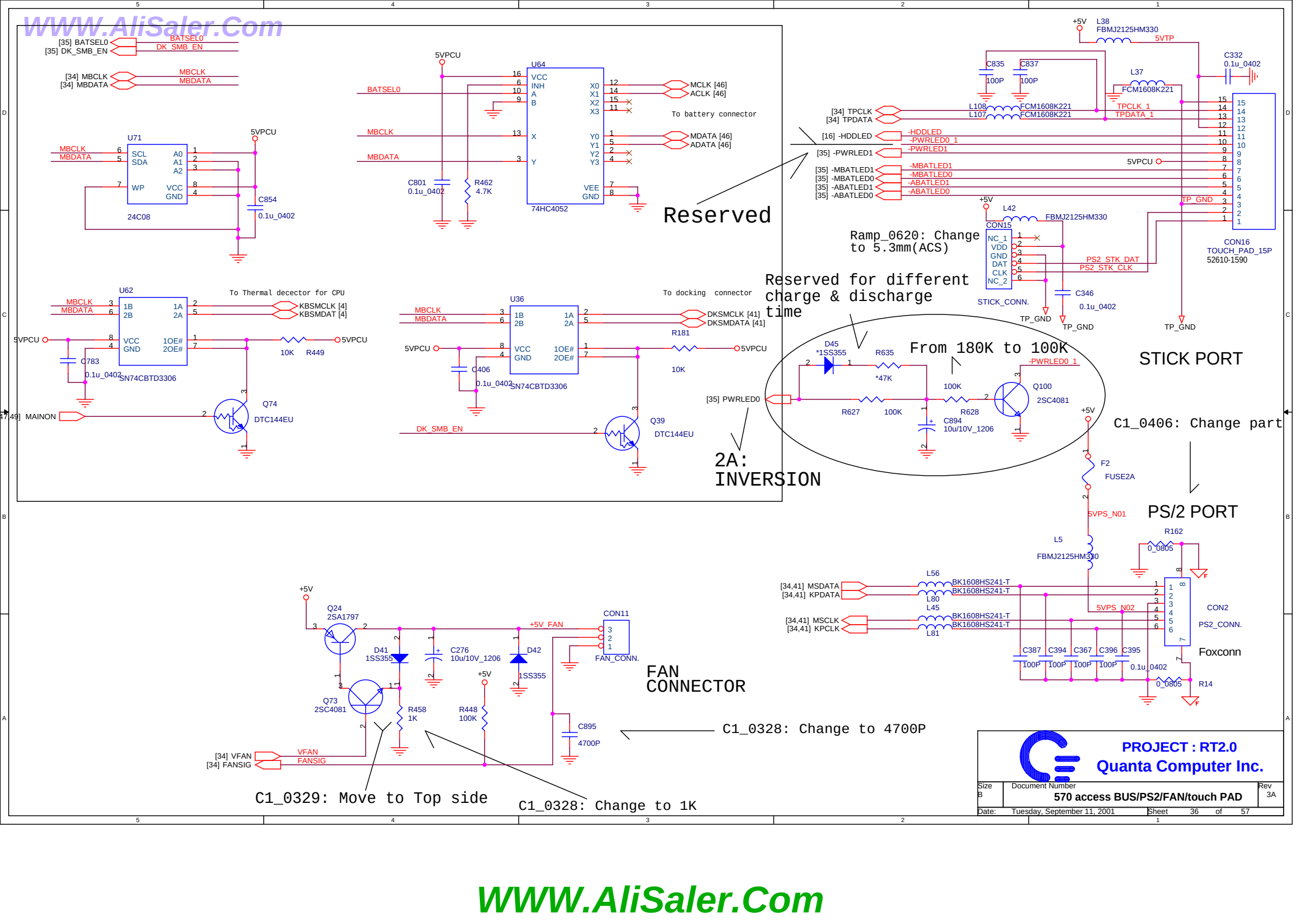
NEW ADD

Ramp_0620

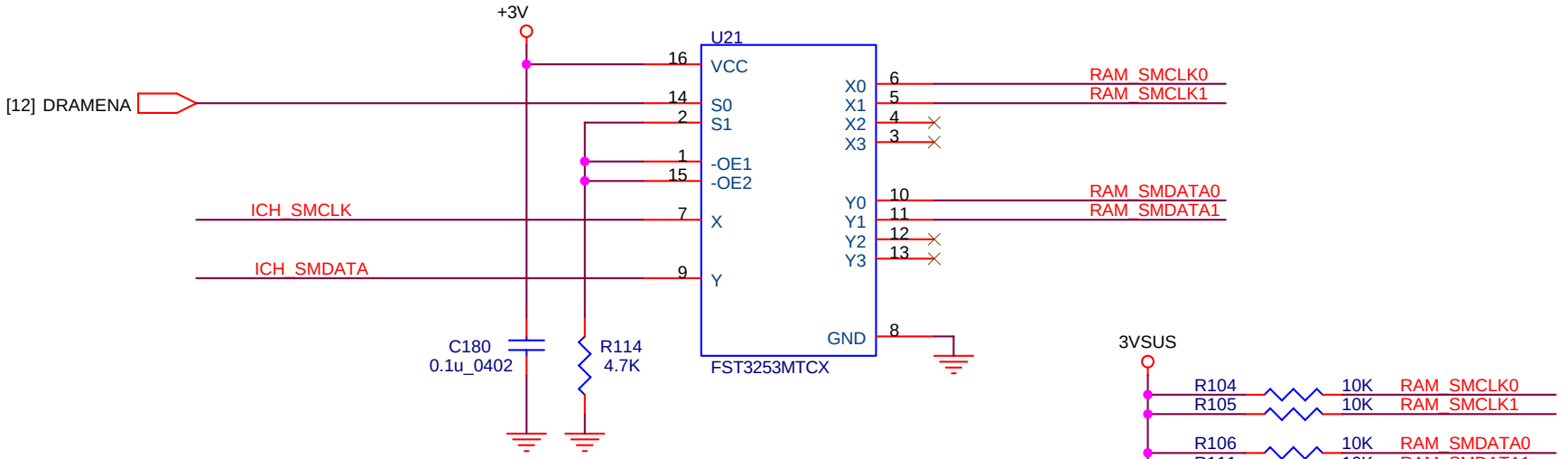
STERLING 1.0 : INSTALL R13,R101/10K
STERLING 1.5 : INSTAL R101/0 ,
REMOVE R13

PROJECT : RT2.0		
Quanta Computer Inc.		
Size: C	Document Number: PC87570F	Rev: 3A
Date: Tuesday, September 11, 2001	Sheet 34 of 57	





C2_0509: Modify



[3,12] ICH_SMCLK — ICH_SMCLK

[3,12] ICH_SMDATA — ICH_SMDATA

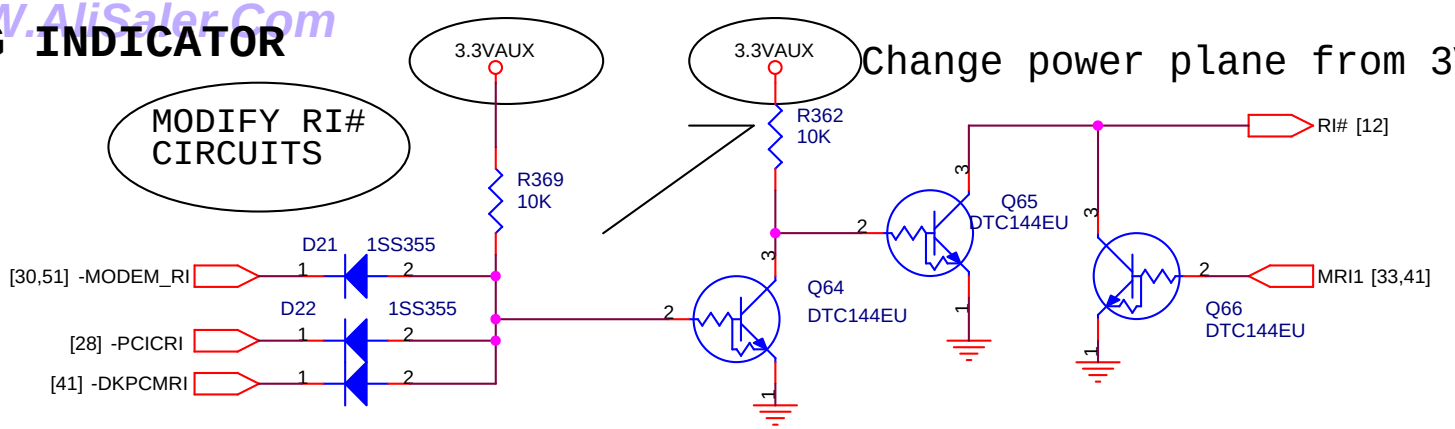
[10] RAM_SMCLK0 — RAM_SMCLK0
[10] RAM_SMCLK1 — RAM_SMCLK1
[10] RAM_SMDATA0 — RAM_SMDATA0
[10] RAM_SMDATA1 — RAM_SMDATA1

PROJECT : RT2.0

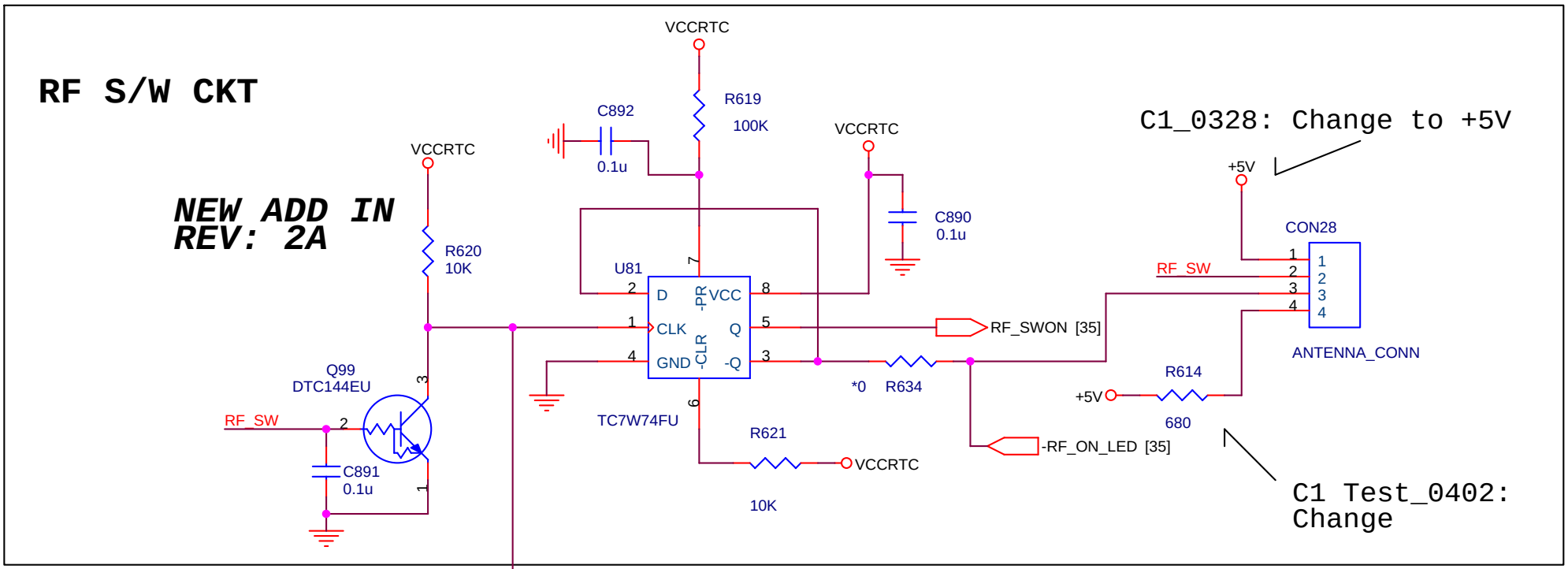
Quanta Computer Inc.

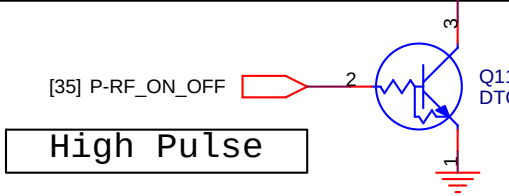
Size	Document Number	Rev
A	**ICH SMBus**	1A
Date: Tuesday, September 11, 2001	Sheet 37 of 57	

RING INDICATOR

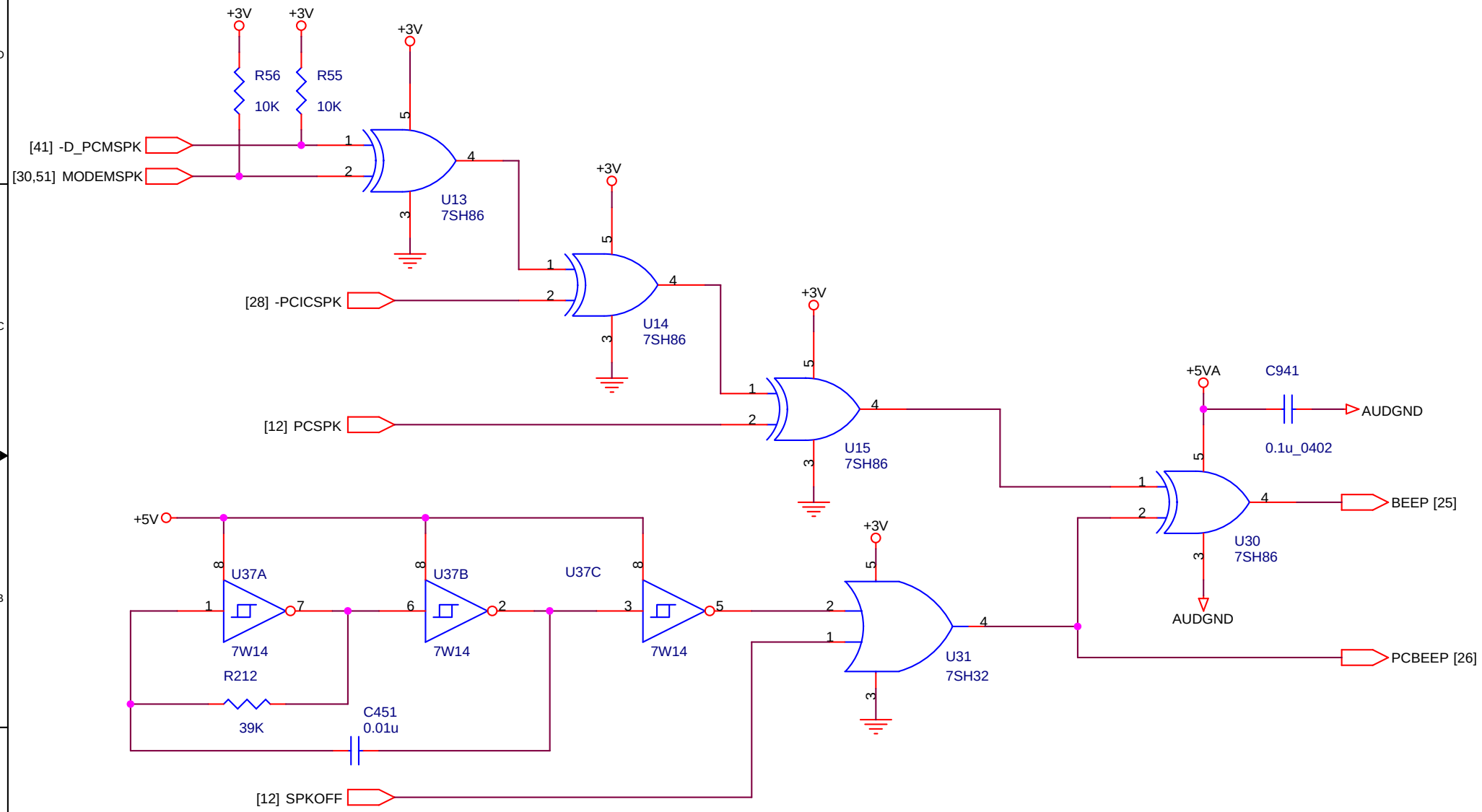


RF S/W CKT





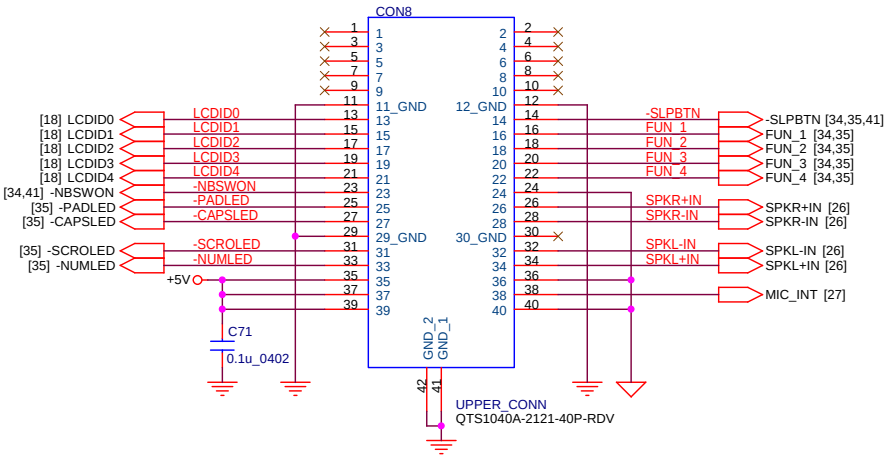
PROJECT : RT2.0		
Quanta Computer Inc.		
Size A	Document Number RING INDICATOR & RF S/W CKT	Rev 3A
Date: Tuesday, September 11, 2001	Sheet 38 of 57	

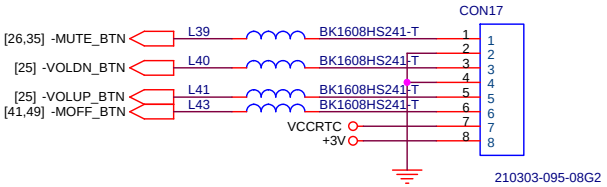


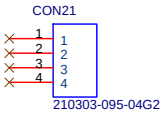
PROJECT : RT2.0

Quanta Computer Inc.

Size	Document Number	Rev
A	**IK BEEP**	2B
Date: Tuesday, September 11, 2001	Sheet 39 of 57	





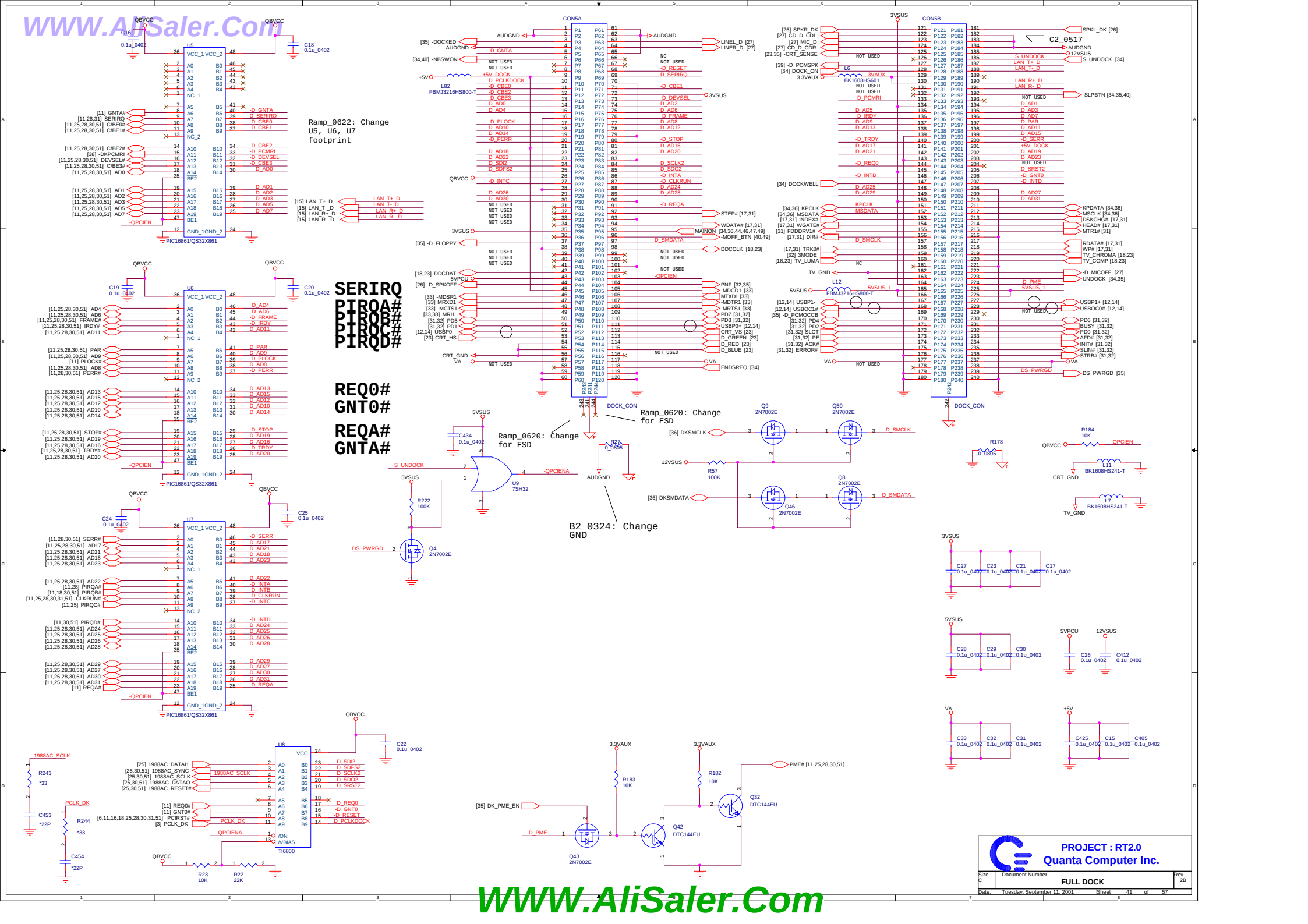


PROJECT : RT2.0

Quanta Computer Inc.

Size	Document Number	Rev
B	upper,volume interface	1A

Date: Tuesday, September 11, 2001 Sheet 40 of 57



Ramp_0620: NPTH

PAD108 EMI_SPRING_RT1
PAD109 *EMI_SPRING_RT1
PAD110 EMI_SPRING_RT1
PAD111 EMI_SPRING_RT1

C2_0529: Change

PAD102 EMI_SPRING_RT1
PAD29 EMI_SPRING_RT1
PAD37 SPRING_2.0X3.0X4.5

Ramp_0622: Change

Ramp_0620: Load

PAD106 EMI_SPRING_RT1
PAD107 EMI_SPRING_RT1

HOLE1 *SCREW HOLE HOLE-S315D110N-8
HOLE2 *SCREW HOLE HOLE-S315D110N-8

GND_DC1
GND_DC2

Ramp_0620: Change for ESD

HOLE14 SCREW_HOLE_01011 HOLE-C315D236P2

C2_0510: Del

PAD100 EMI_SPRING_RT1
0_0805 R677
R679 0_0805
GND_DC2

0_0805 R680
R678 0_0805
GND_DC1

HOLE3 *SCREW HOLE HOLE-TC236BS315D102P2
HOLE7 *SCREW_HOLE HOLE-TC354BC315D197PB
C2_0507
HOLE23 SCREW_HOLE_01011 HOLE-C315D236P2
HOLE11 *HDD_PAD HOLE-OB128X58D98X28P2

HOLE5 *SCREW_HOLE HOLE-TC354BS315D197PB
C2_0507

HOLE4 *SCREW HOLE HOLE-TC315BS394D118NP2-4

C2_0517: For ICT

HOLE13 *SCREW HOLE HOLE-C315D146P2
HOLE21 *SCREW HOLE HOLE-TC236BC315D118NP2

NPTH

C2_0425: Change drill size

Ramp_0620: Add for ESD

PAD4 PAD5 PAD6 PAD7 PAD8 *SHORT
PAD14 PAD16 PAD19 PAD23 *SHORT
PAD25 PAD21 *SHORT
C2_0517
PAD26 *SHORT
C2_0510: Del
PAD17 *SHORT
PAD11 *SHORT
C2_0517
PAD12 *SHORT
C2_0510: Del
PAD20 *SHORT AUDGND AUDGND
PAD2 PAD3 *SHORT
PAD1 PAD30 PAD31 *SHORT
C2_0510: Del
PAD33 *SHORT
PAD39 PAD41 PAD44 PAD48 *SHORT
PAD50 PAD46 *SHORT
C2_0517
PAD51 PAD43 *SHORT
PAD42 *SHORT
PAD36 *SHORT
C2_0517
PAD38 PAD45 PAD28 *SHORT AUDGND AUDGND

HOLE12 *HEATSINK_HOLE HOLE-S315D118P2
HOLE8 *HEATSINK_HOLE HOLE-S315D118P2
HOLE16 *SCREW HOLE HOLE-S157D118NP2

C2_0510: Del

HOLE15 *SCREW HOLE HOLE-S394D118NP2-4

HOLE9 *HEATSINK_HOLE HOLE-S315D118P2

C2_0517: For ICT

HOLE18 *SCREW HOLE HOLE-S394D110P2
HOLE25 *HDD_PAD HOLE-OB207X58D177X28P2

C2_0508: Change size

HOLE20 *SCREW HOLE HOLE-TC354BS315D118NP2-4

C2_0517: For ICT

HOLE22 *SCREW HOLE HOLE-S315D102P2
HOLE17 SCREW_HOLE_16017 HOLE-C236D158P2
HOLE19 *SCREW HOLE HOLE-S394D118P2
AUDGND
HOLE6 SCREW_HOLE_83014 HOLE-TC276BC197D158P2
AUDGND

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	hole PAD and EMIPAD	3A

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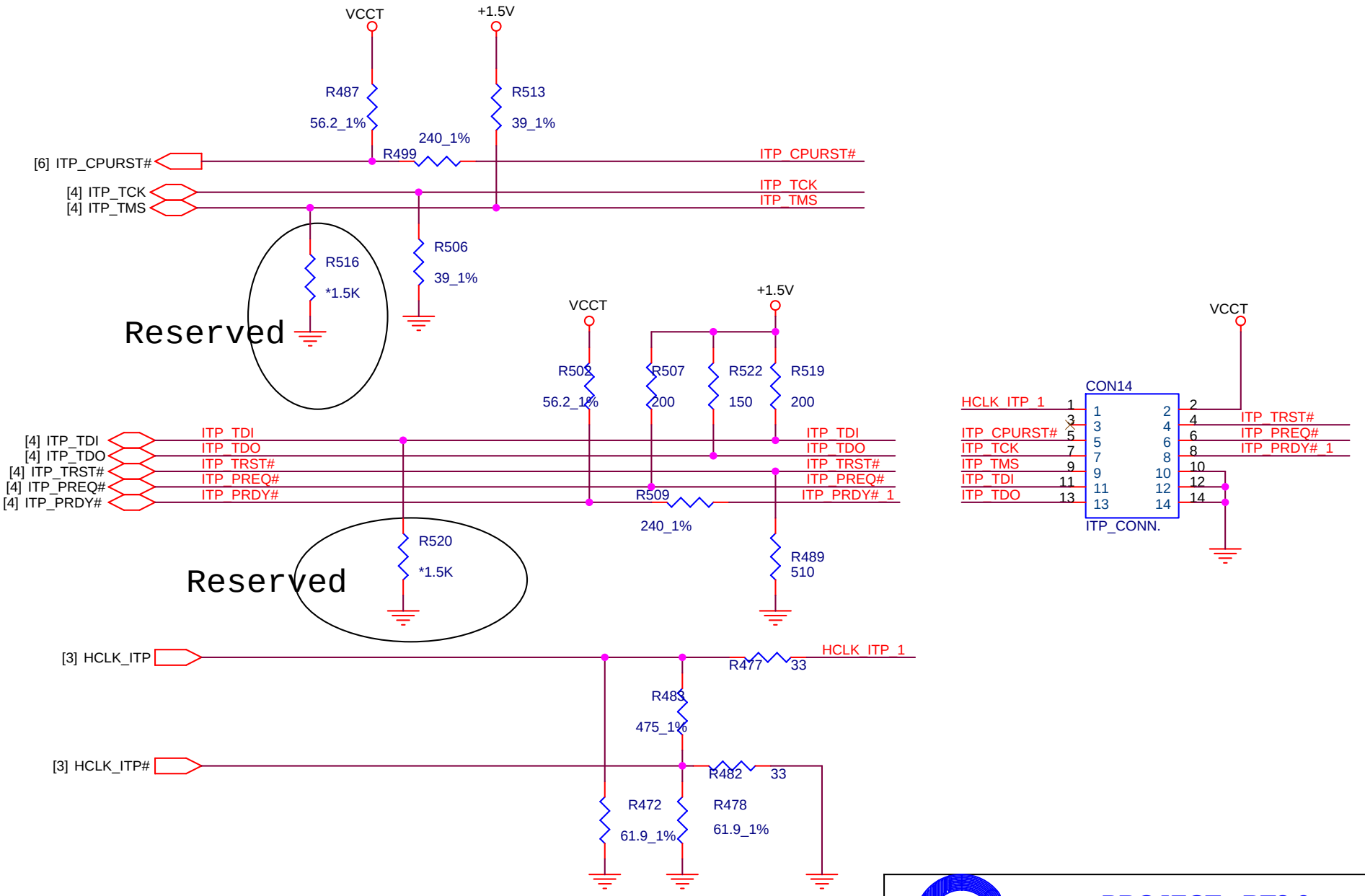
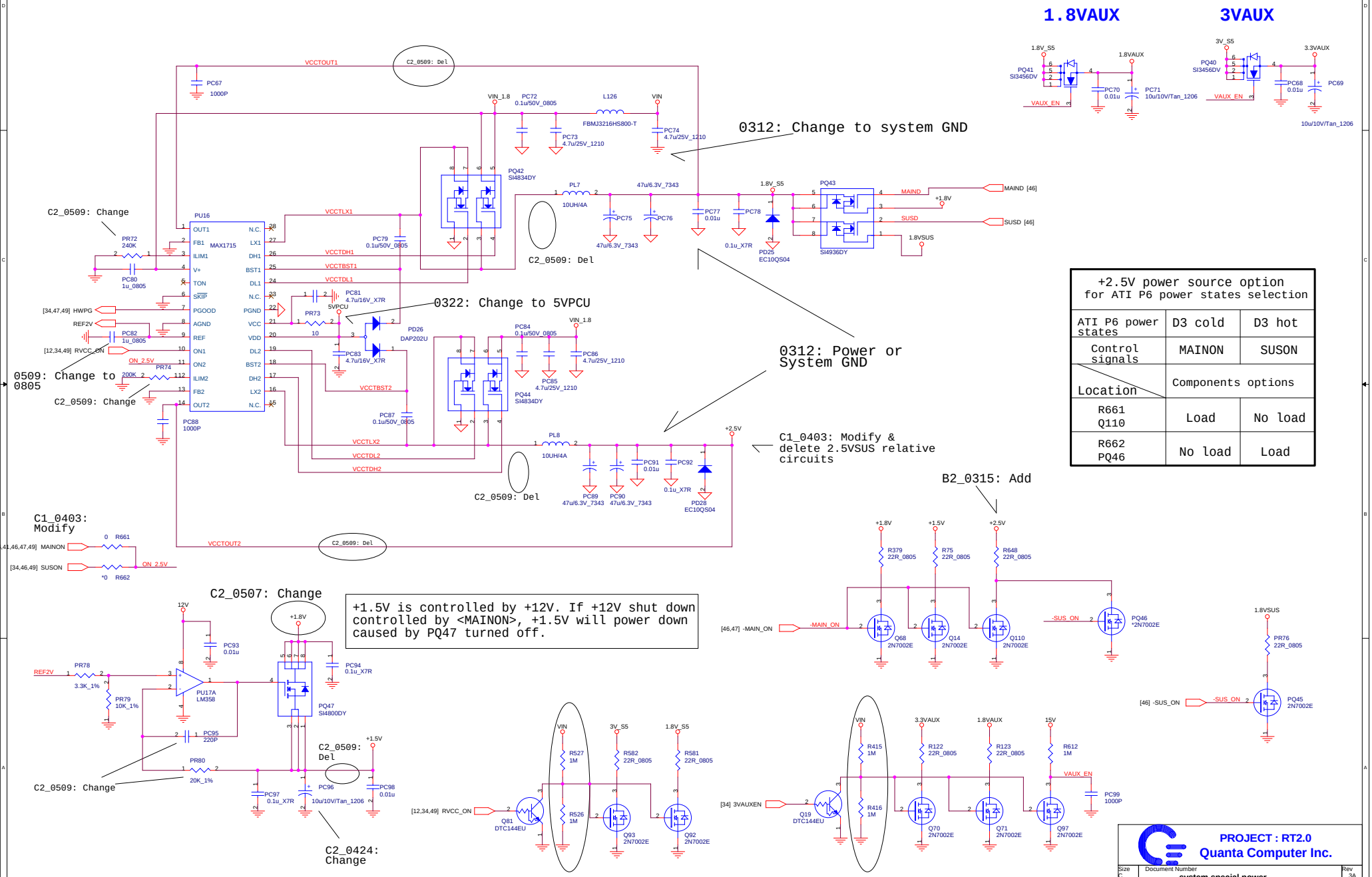


PROJECT : RT2.0

Quanta Computer Inc.

Size	Document Number	Rev
A	**ITP interface**	2A
Date: Tuesday, September 11, 2001	Sheet 43 of 57	

B2 Test change the power circuits

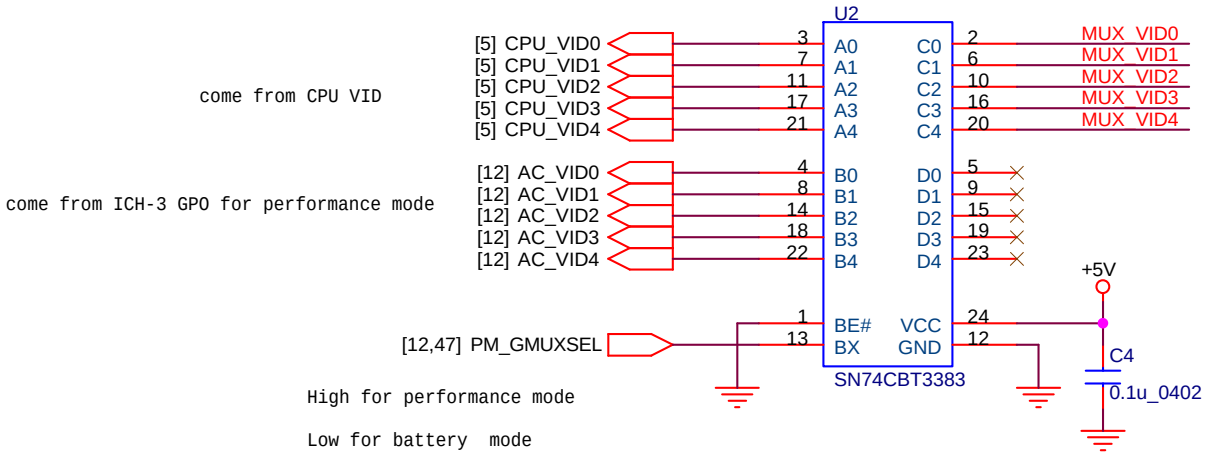


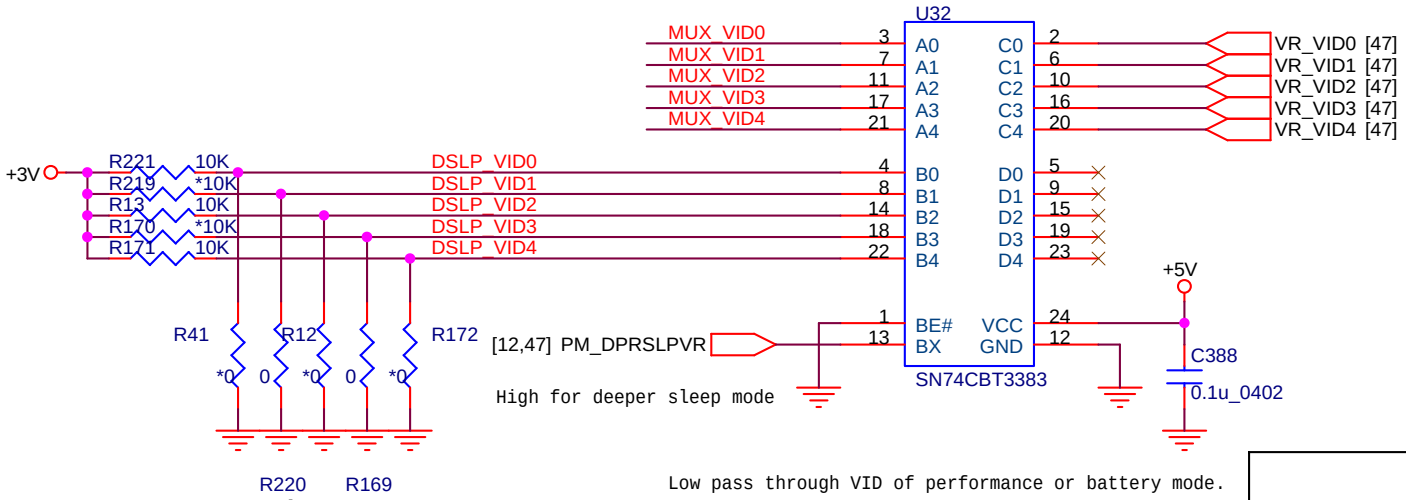
+2.5V power source option for ATI P6 power states selection		
ATI P6 power states	D3 cold	D3 hot
Control signals	MAINON	SUSON
Location	Components options	
R661 Q110	Load	No load
R662 PQ46	No load	Load

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
C	system special power	3A
Date: Tuesday, September 11, 2001	Sheet 44 of 57	

CPU VID selector





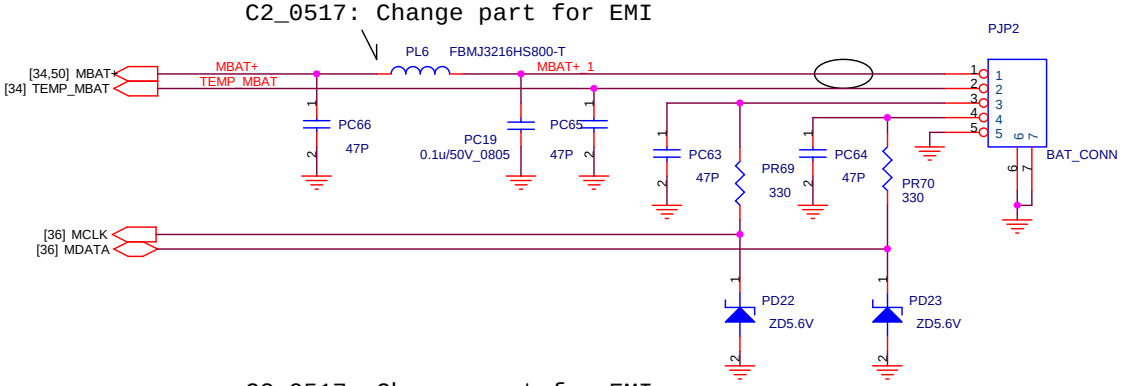
Low pass through VID of performance or battery mode.

Ramp_0704: Change to 0.85V

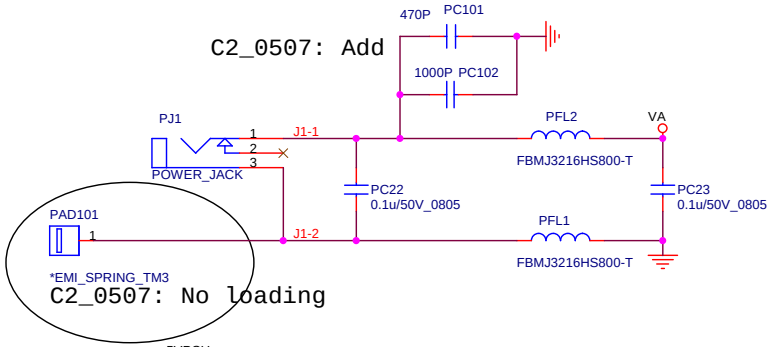
	ID4	ID3	ID2	ID1	ID0
0.85V:	1	0	1	0	1

Size	Document Number	Rev
A	VID selector	1A
Date: Tuesday, September 11, 2001	Sheet 45 of 57	

C2_0517: Change part for EMI

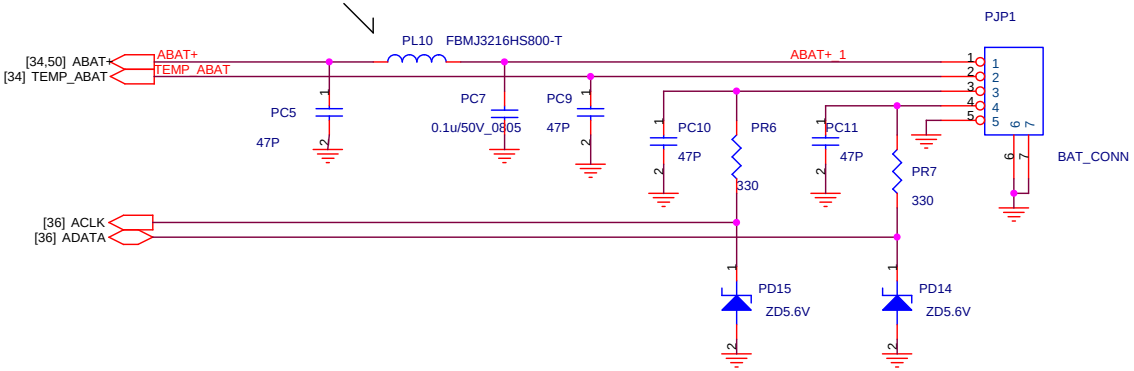


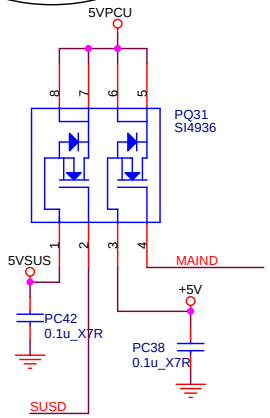
C2_0507: Add

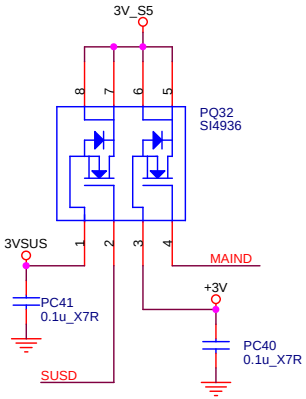


C2_0507: No loading

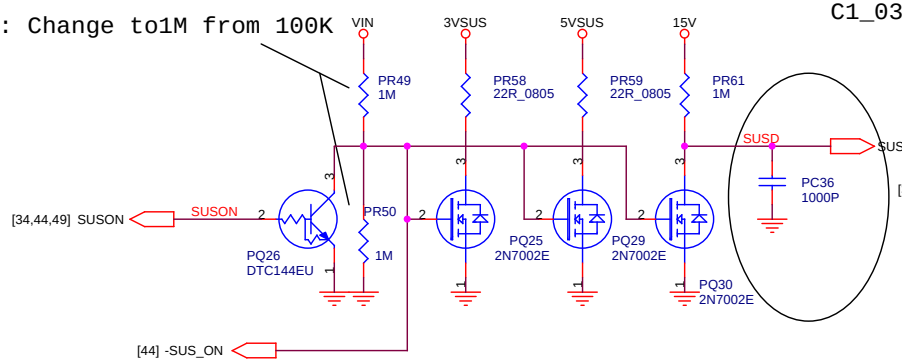
C2_0517: Change part for EMI



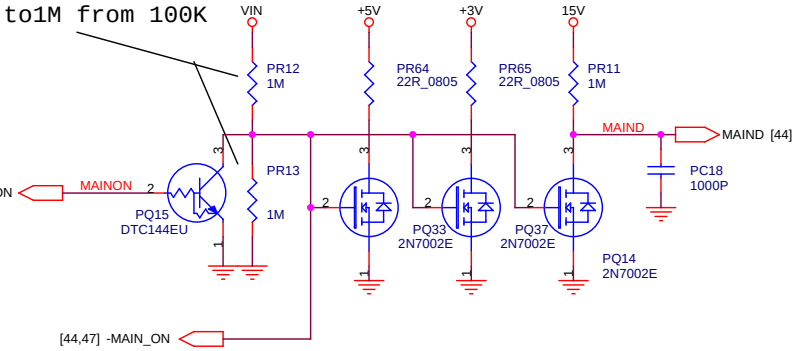




C1_0328: Change to1M from 100K



C1_0328: Change to1M from 100K



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	POWER JACK / BATTERY conn.	3A

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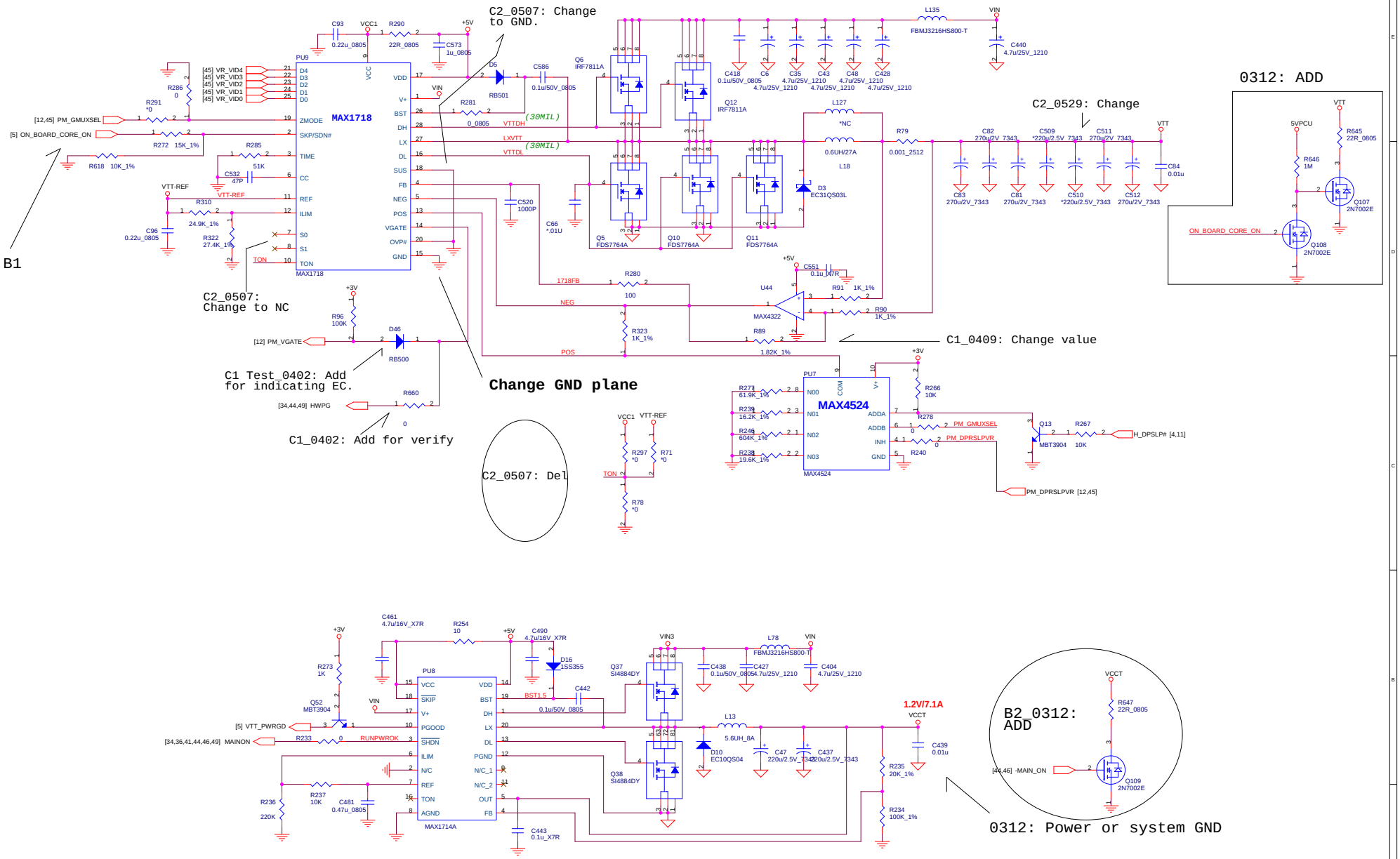
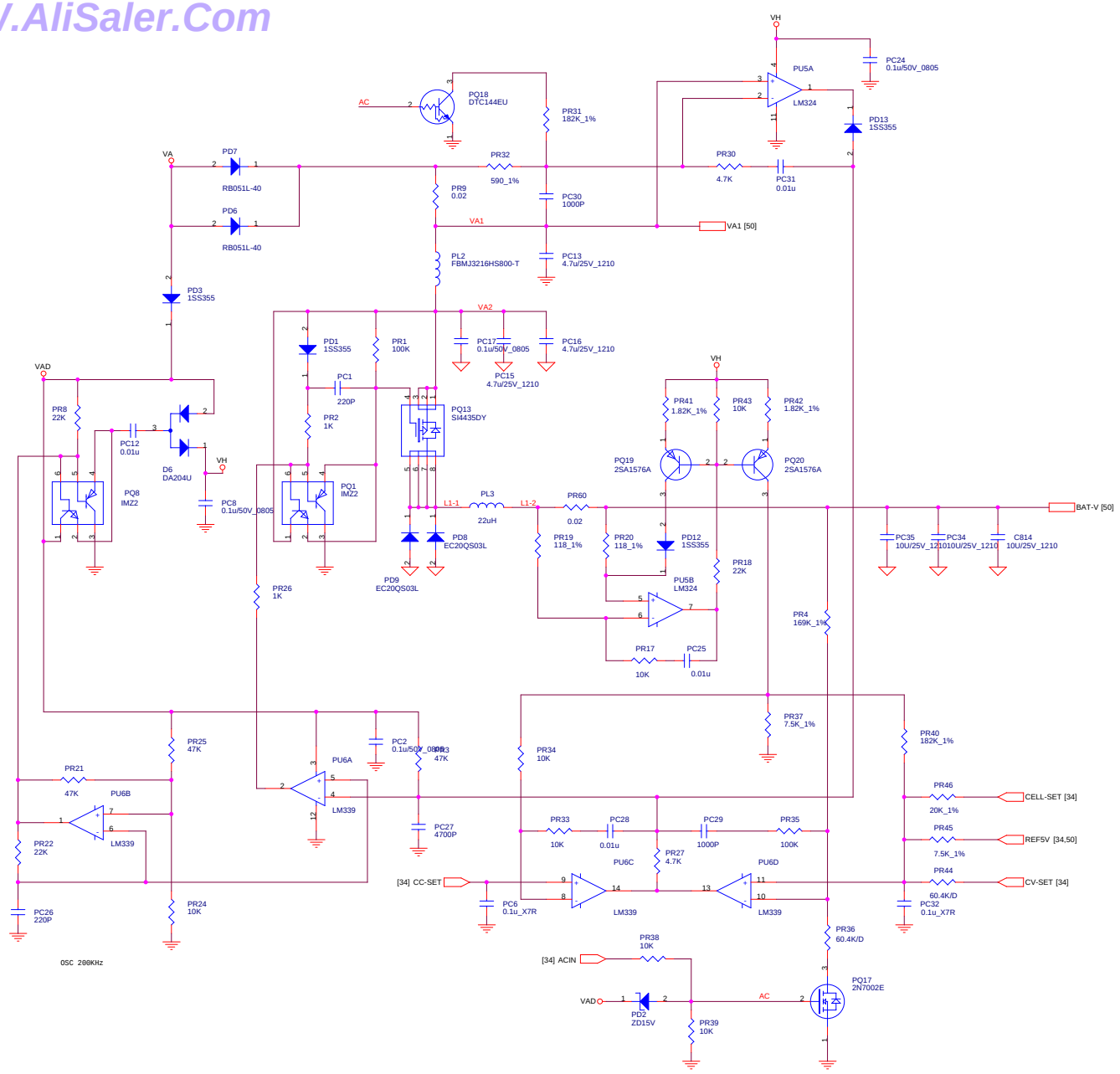


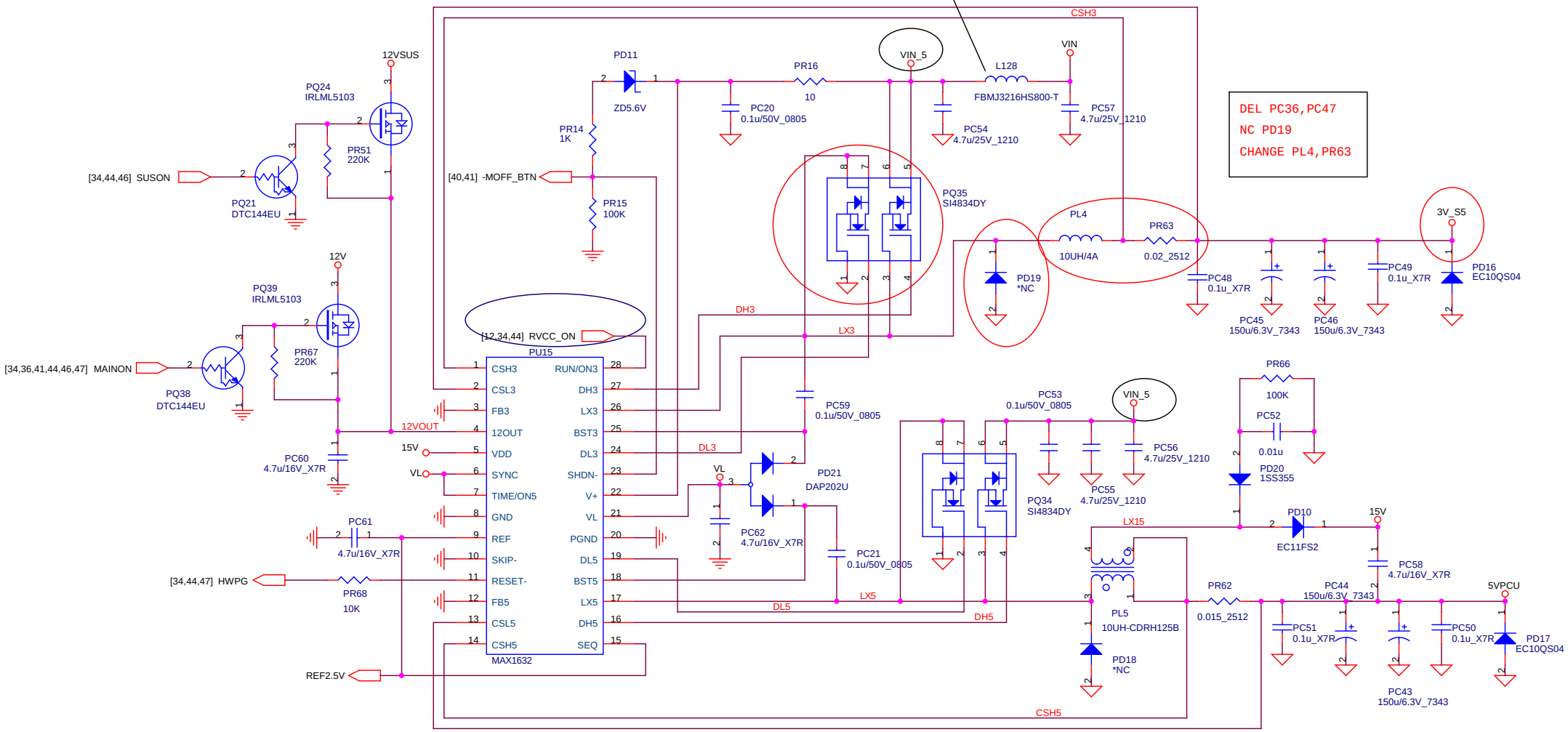
PROJECT : RT2.0		
Quanta Computer Inc.		
Size: C	Document Number: CPU power - VCC/VTT	Rev: 3A
Date: Tuesday, September 11, 2001	Sheet 47 of 57	



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
C	CHARGER & DISCHARGER	1A
Date: Tuesday, September 11, 2001	Sheet 48 of 57	

B2 Test: ADD



PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	POWER CIRCUIT(MAX1632)	2B

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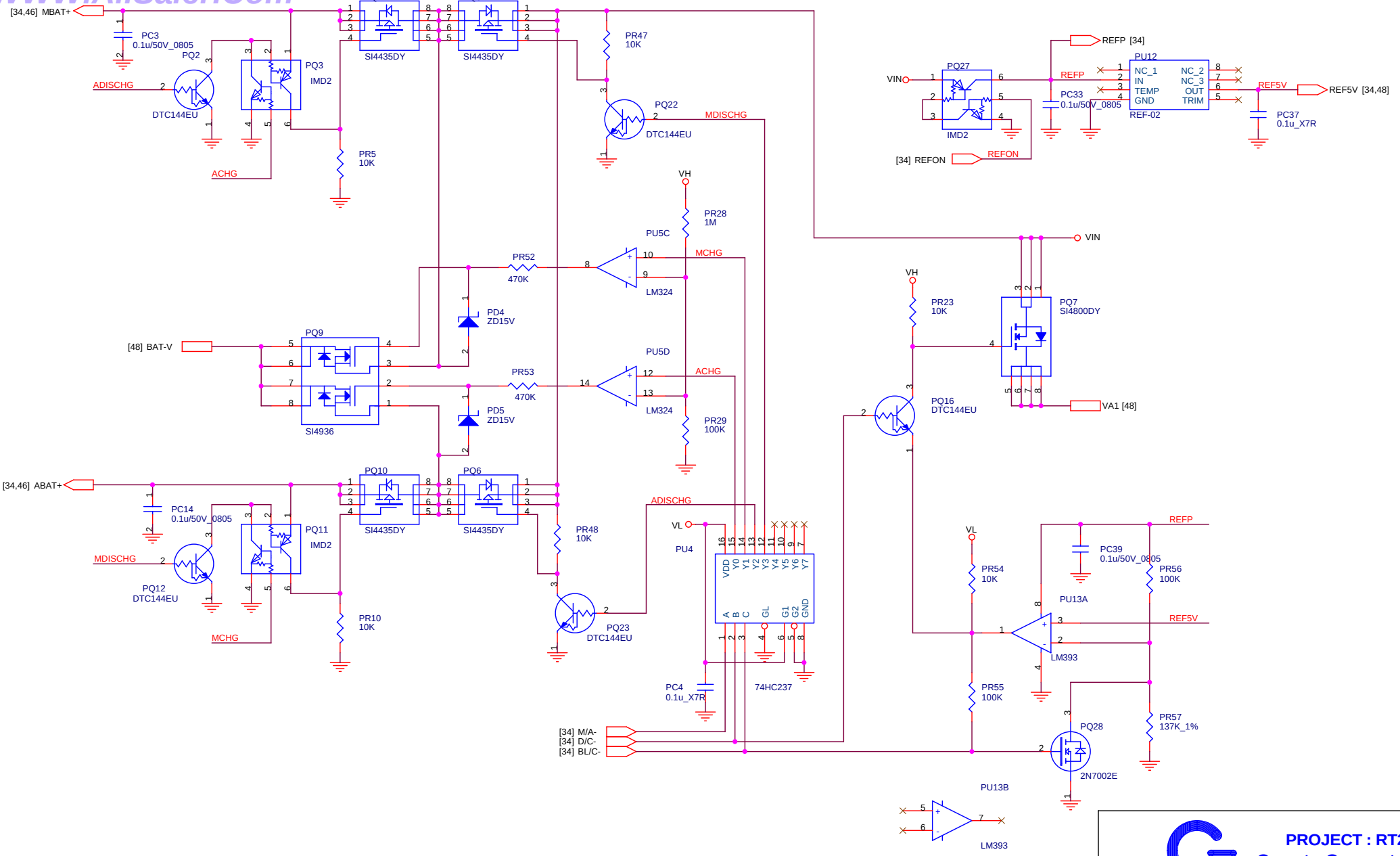
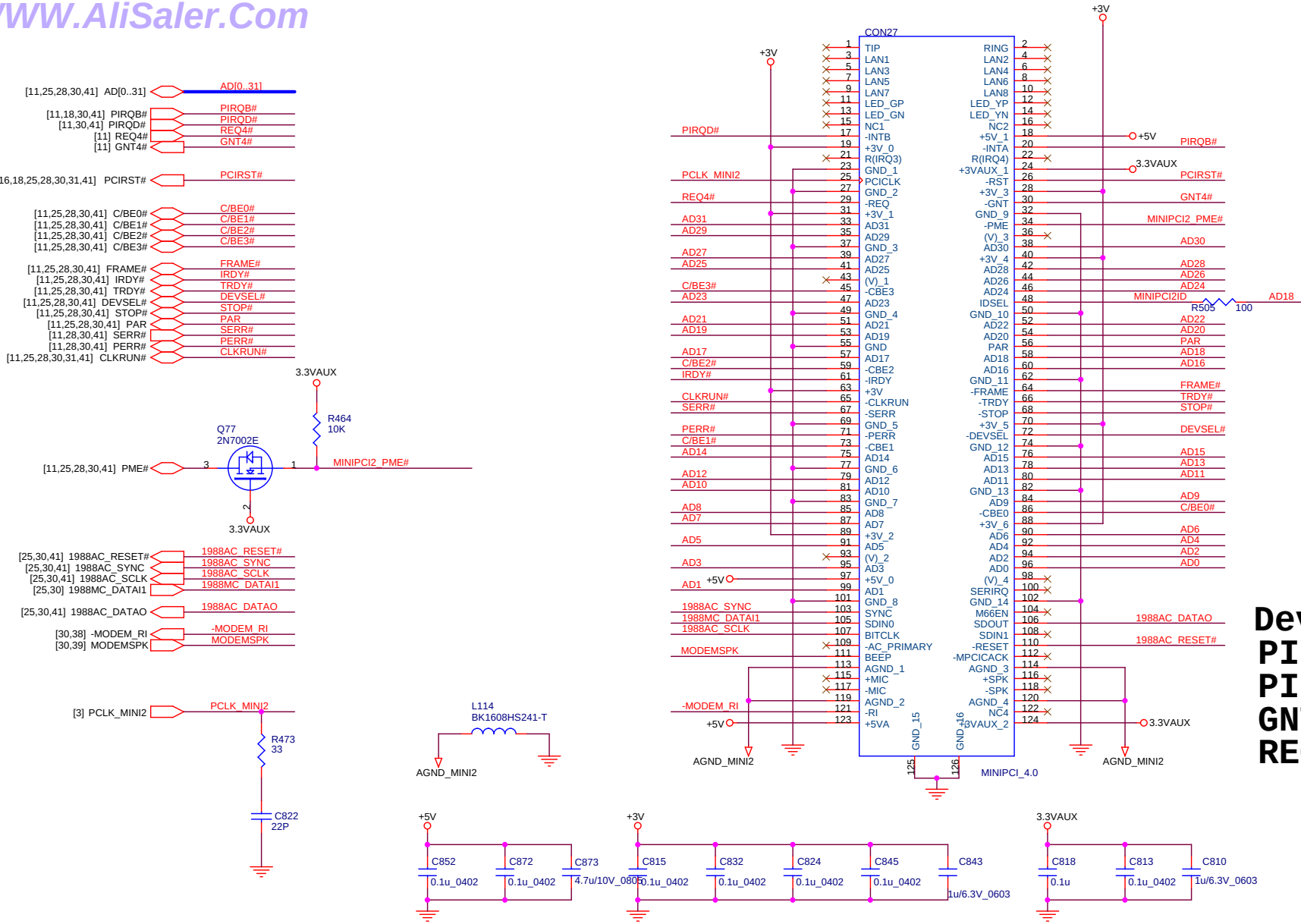


PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	BATTERY SELECTOR	1A
Date: Tuesday, September 11, 2001	Sheet 50 of 57	



Device ID is AD18
PIRQD#
PIRQB#
GNT4#
REQ4#

PROJECT : RT2.0
Quanta Computer Inc.

Size	Document Number	Rev
B	MINI PCI second interface	1A

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