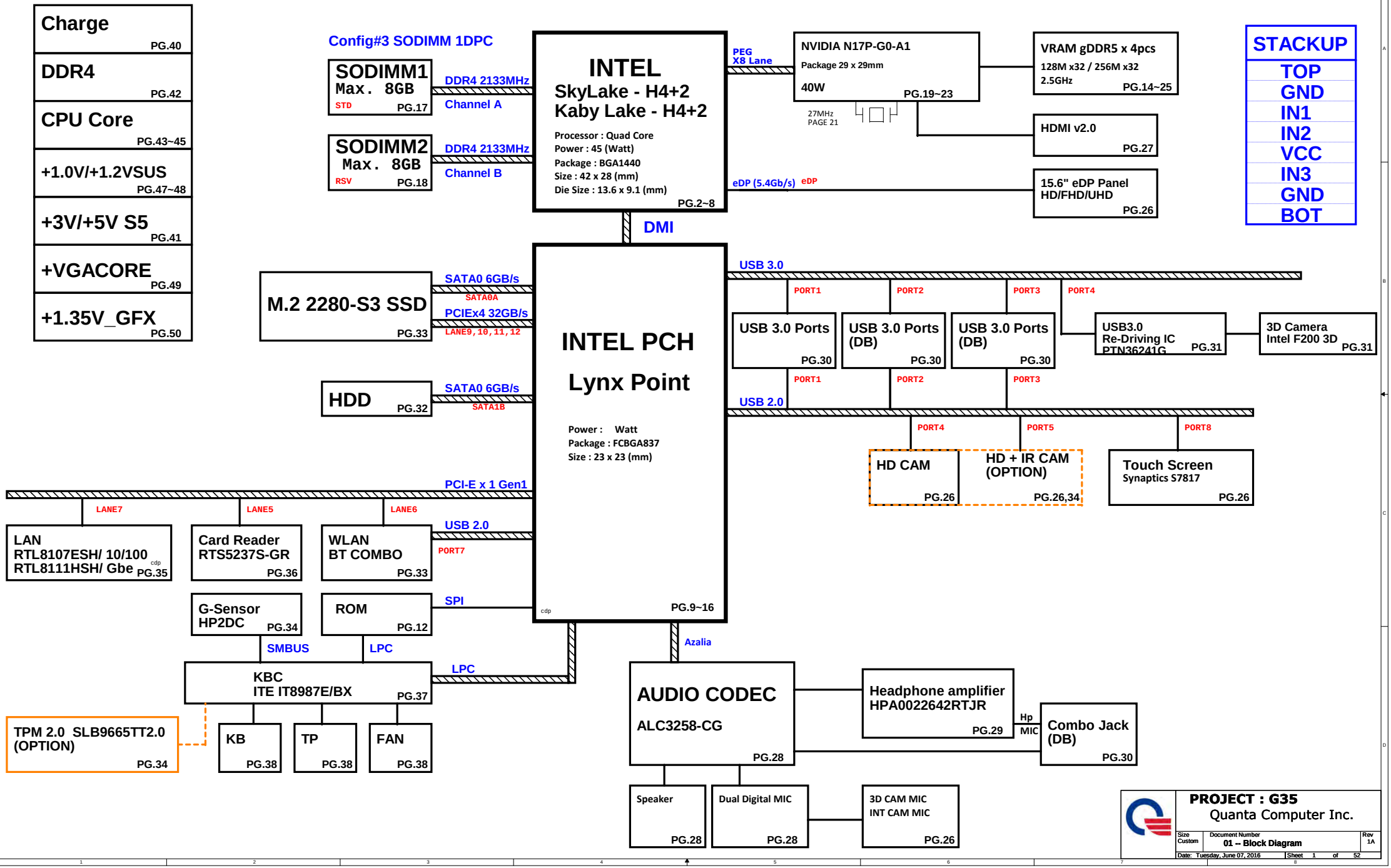
POWER PAVILION Trifle INTEL SKL / KABY -H SYSTEM DIAGRAM

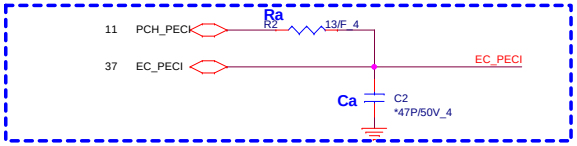
01



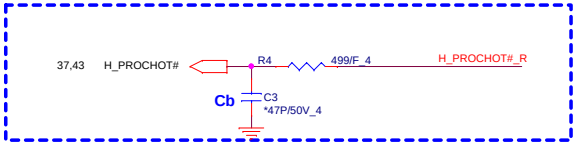
SKYLAKE Processor (CLK,MISC,JTAG)

02

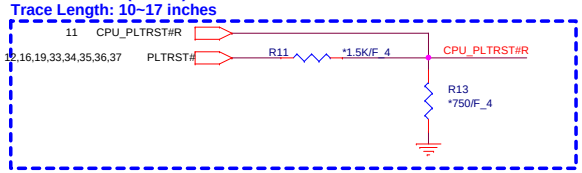
H_PECI (50ohm)
Trace Length: <0.5 iches
Ra,Ca need placement close to PCH.



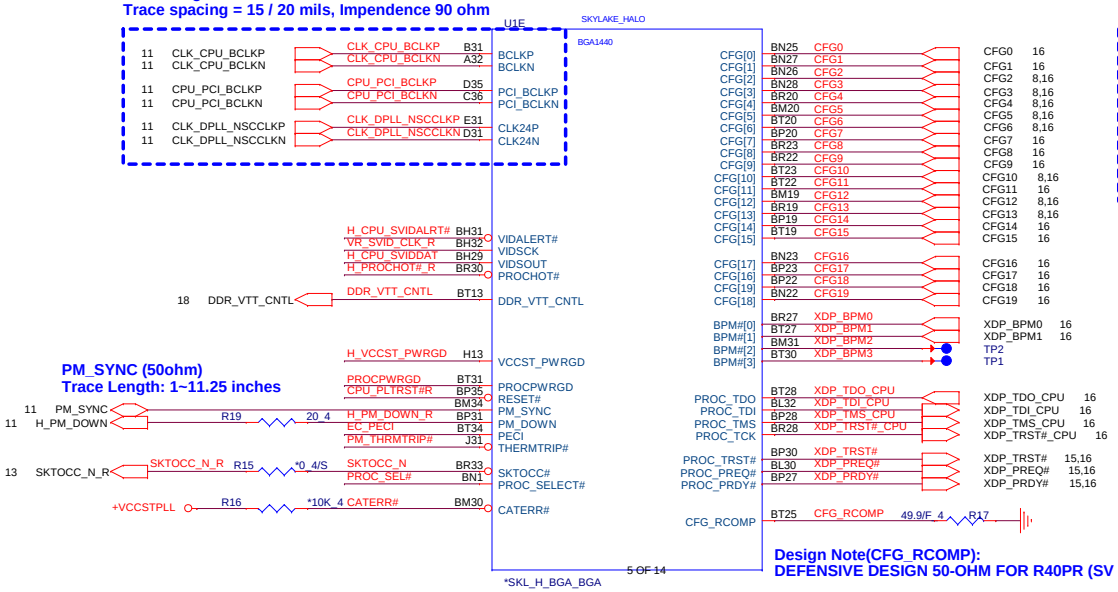
PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR



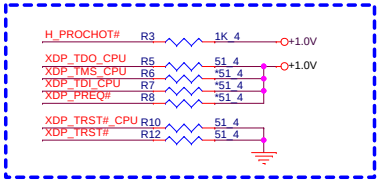
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 90 ohm



Processor pull-up (CPU)



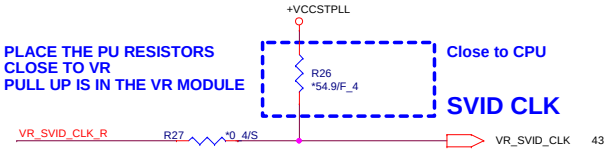
PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

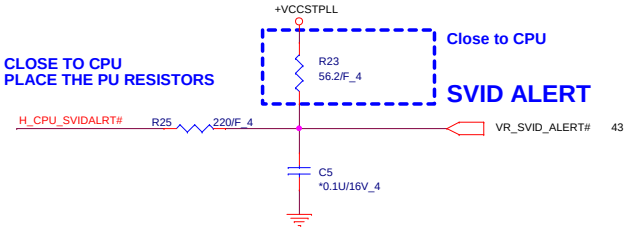
CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

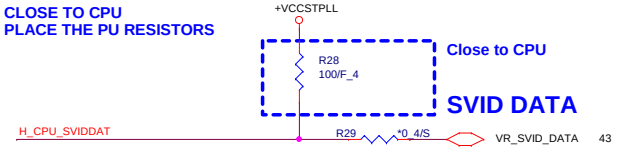
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



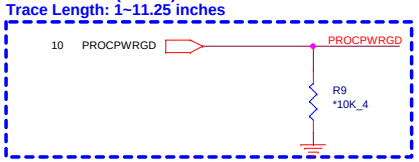
CLOSE TO CPU
PLACE THE PU RESISTORS



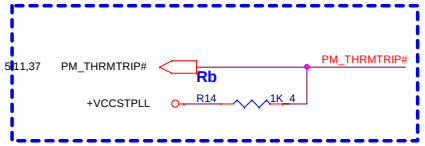
CLOSE TO CPU
PLACE THE PU RESISTORS



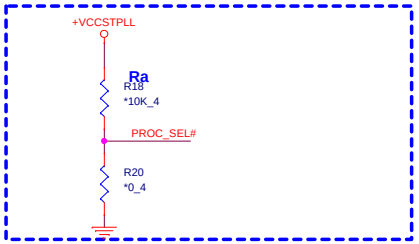
PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches



THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placment near PCH

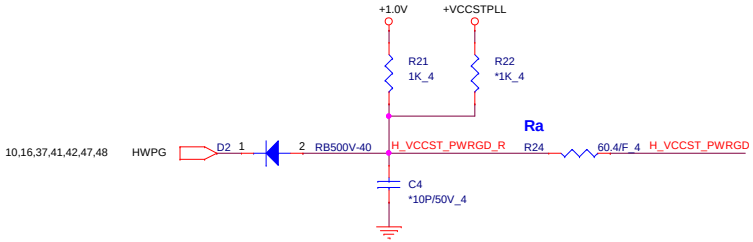


Ra(R10804) Not install in SKL-H



HWPD

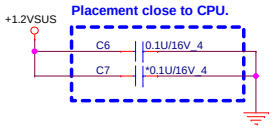
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

Placement close to CPU.



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKL 1/7 (JTAG/MISC)	1A

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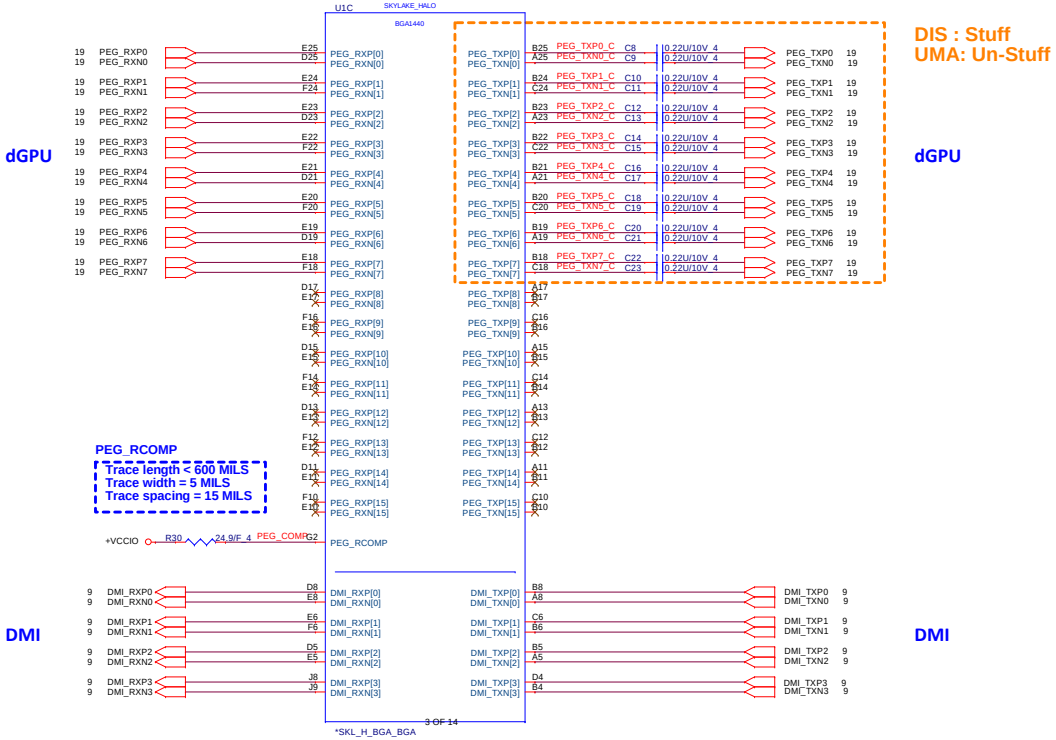
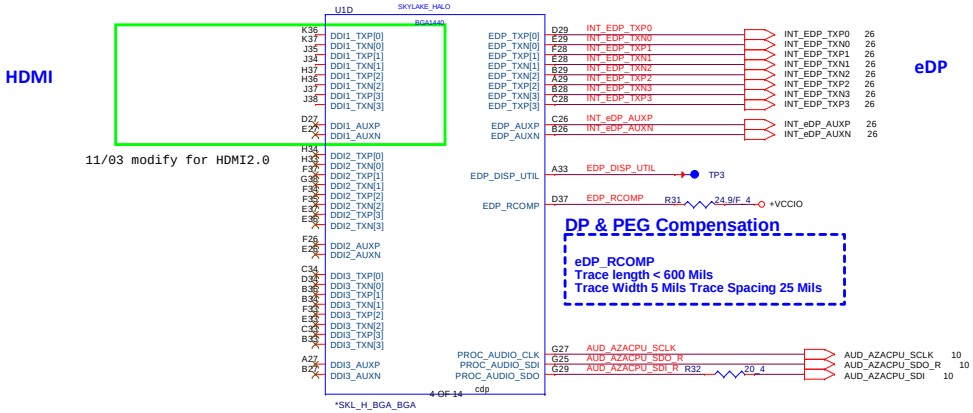
SKYLAKE Processor (DMI,PEG,FDI)

03





+1.2VSUS 2,6,10,17,18,42,48,51
+3VS5 10,12,14,16,33,37,41,42,46,47,4
+3V 5,9,10,11,12,13,14,16,17,18,22,26,2

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 – SKL 2/7 (DMI/EDP/PEG)	1A

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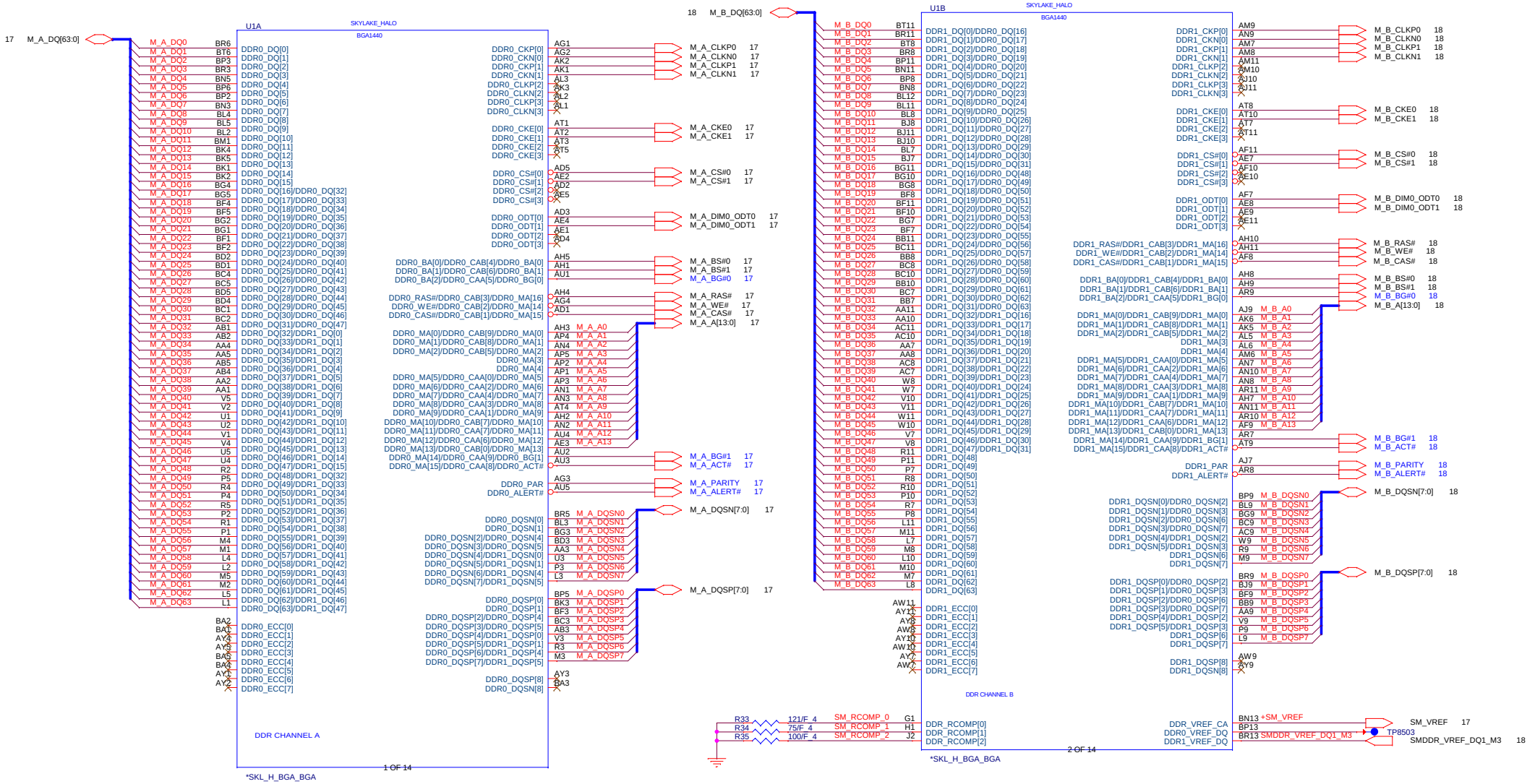
SKYLAKE Processor (DDR4)

04



PROJECT : G35	
Quanta Computer Inc.	
Size: Custom	Document Number: 04 -- SKL 3/7 (DDR4 I/F)
Rev: 1A	
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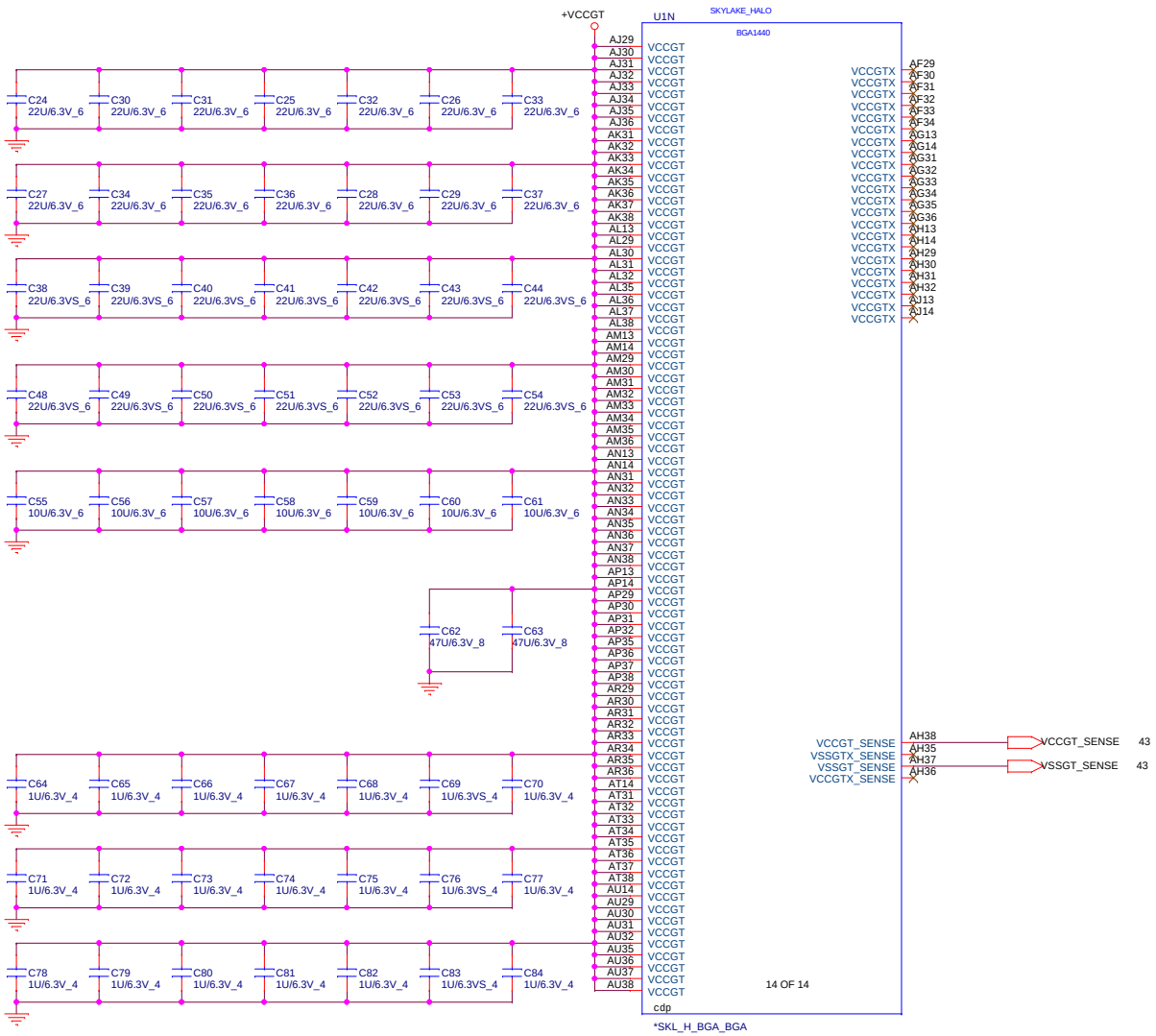
SKYLAKE Processor (POWER)

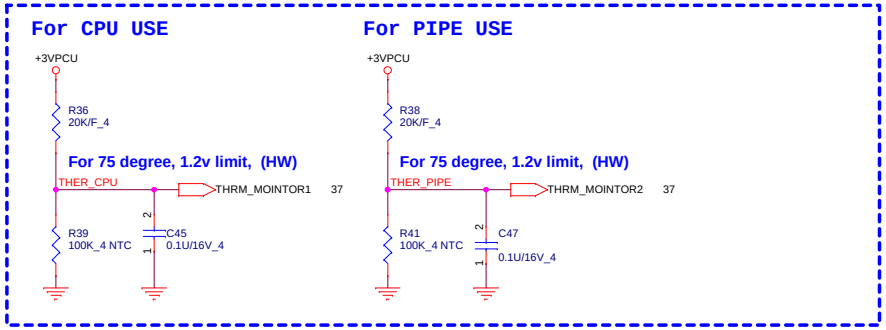
05

Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A



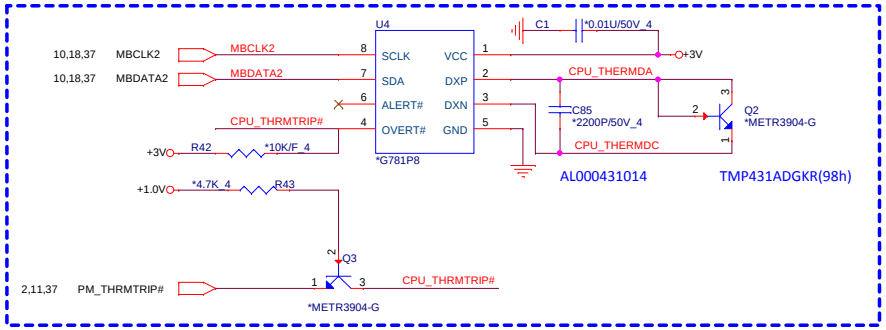
IO Thrm Protect

Location need thermal confirm



CPU Thermal Sensor

Location need thermal confirm



PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKL 4/7 (POWER)	1A

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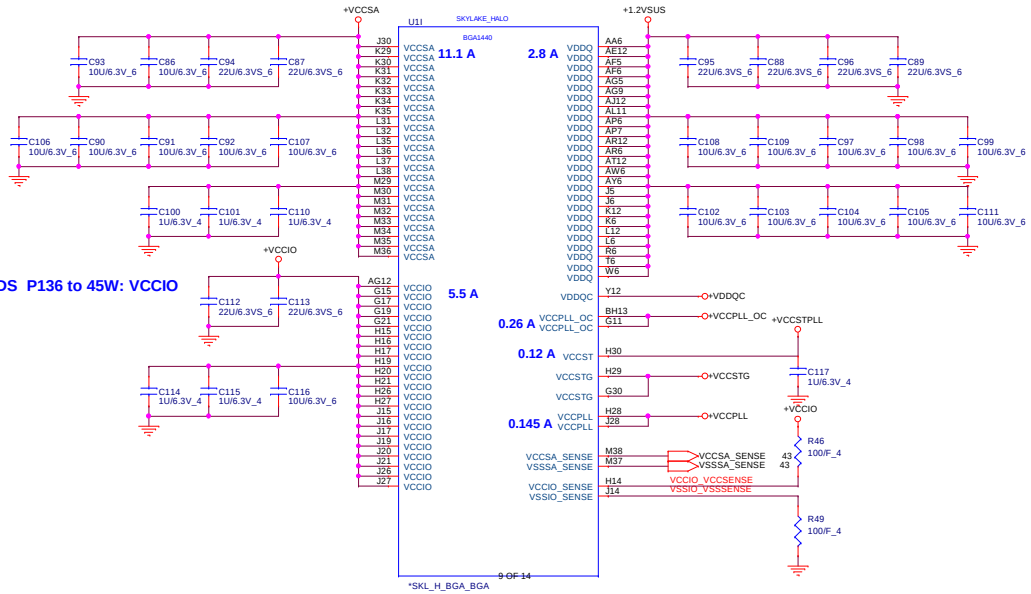
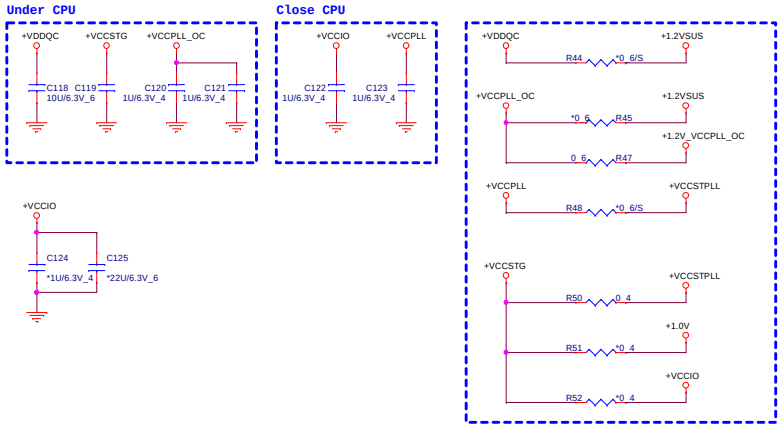
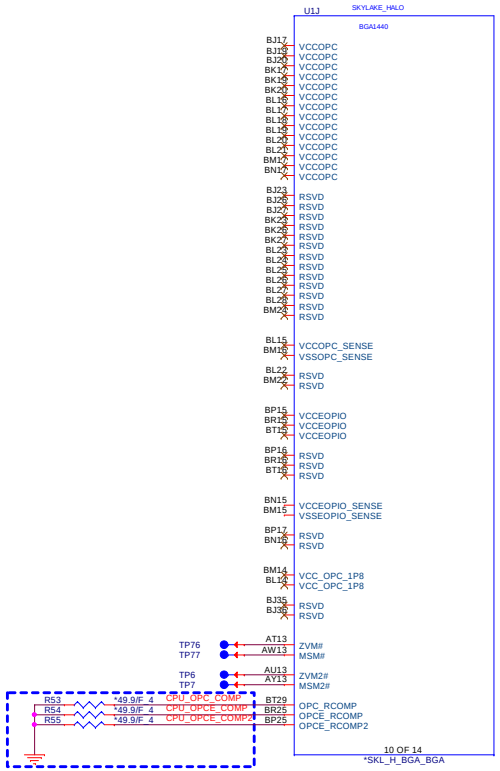
Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow SKL H EDS page 135 45W: VDDQ=2.8A



Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V





Unconnected for Processors without OPC.

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Custom	06 -- SKL 5/7 (POWER&GND)	1A

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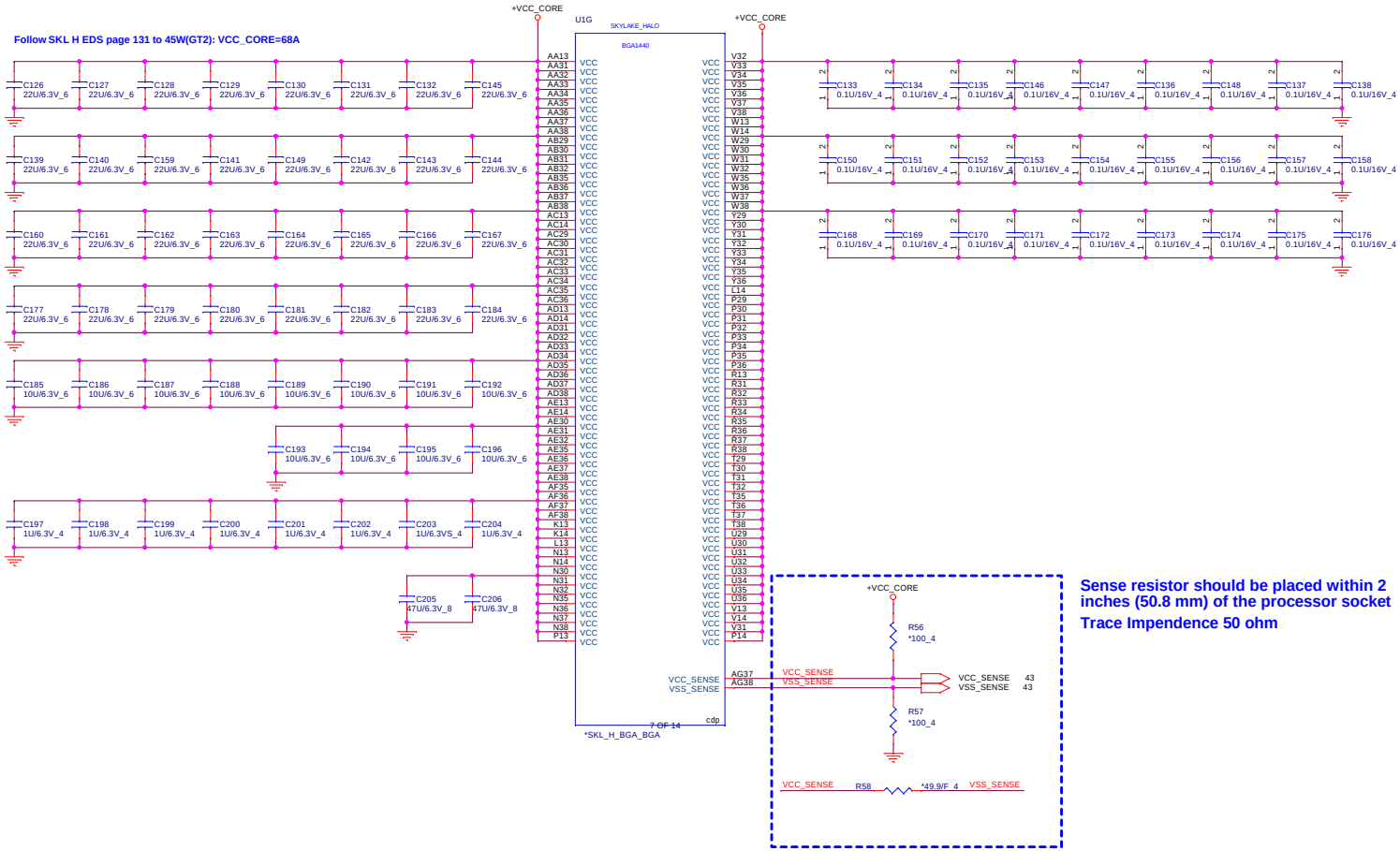
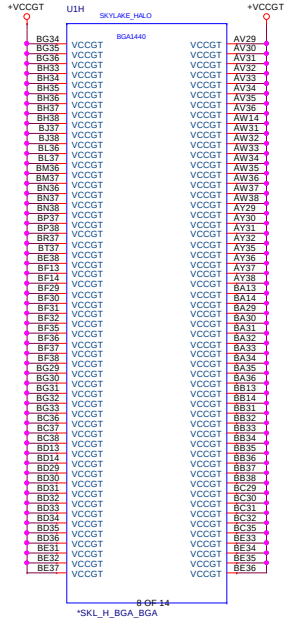
Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm



+VCC_CORE 43,44

PROJECT : G35

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Size	Document Number	Rev
Custom	07 -- SKL 6/7 (POWER&GND)	1A

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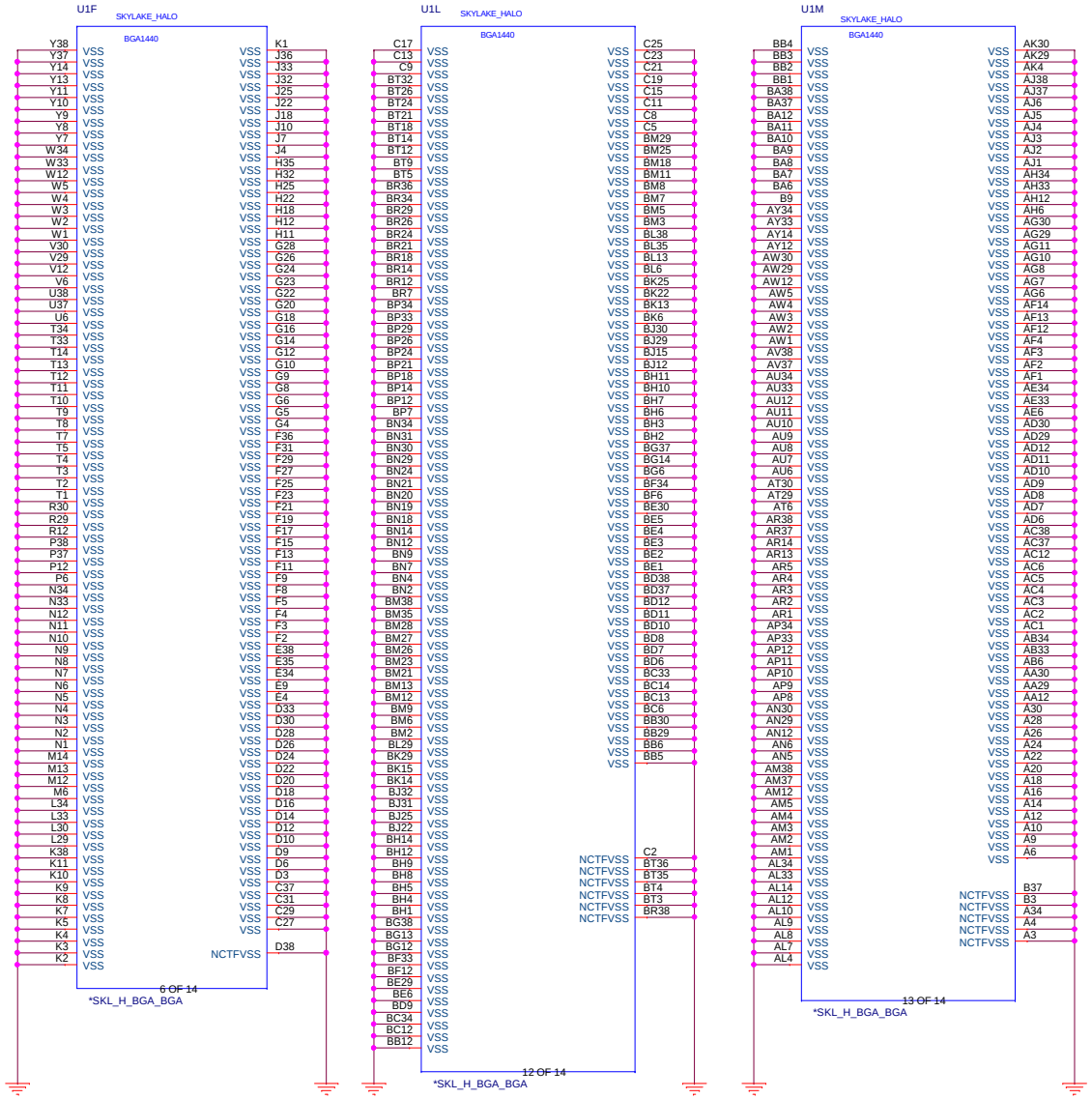
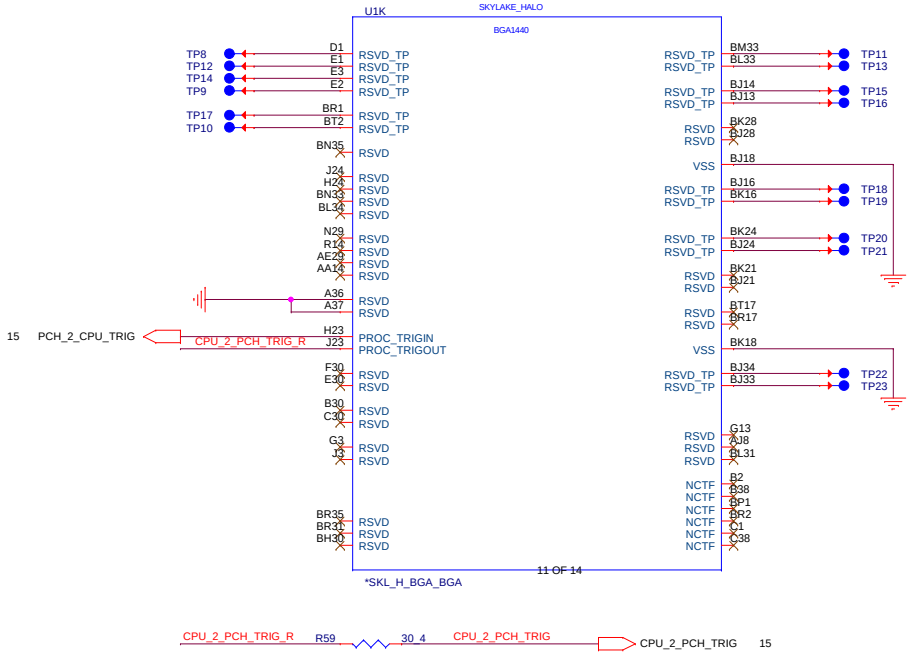
SKL-HProcessor (GND)



SKL-H Processor (RESERVED, CFG)

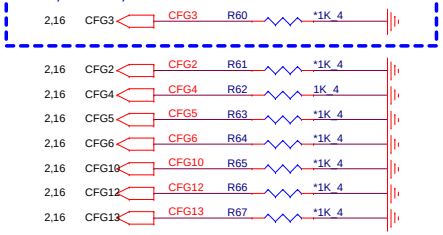


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;



PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKL 7/7 (GND)	1A

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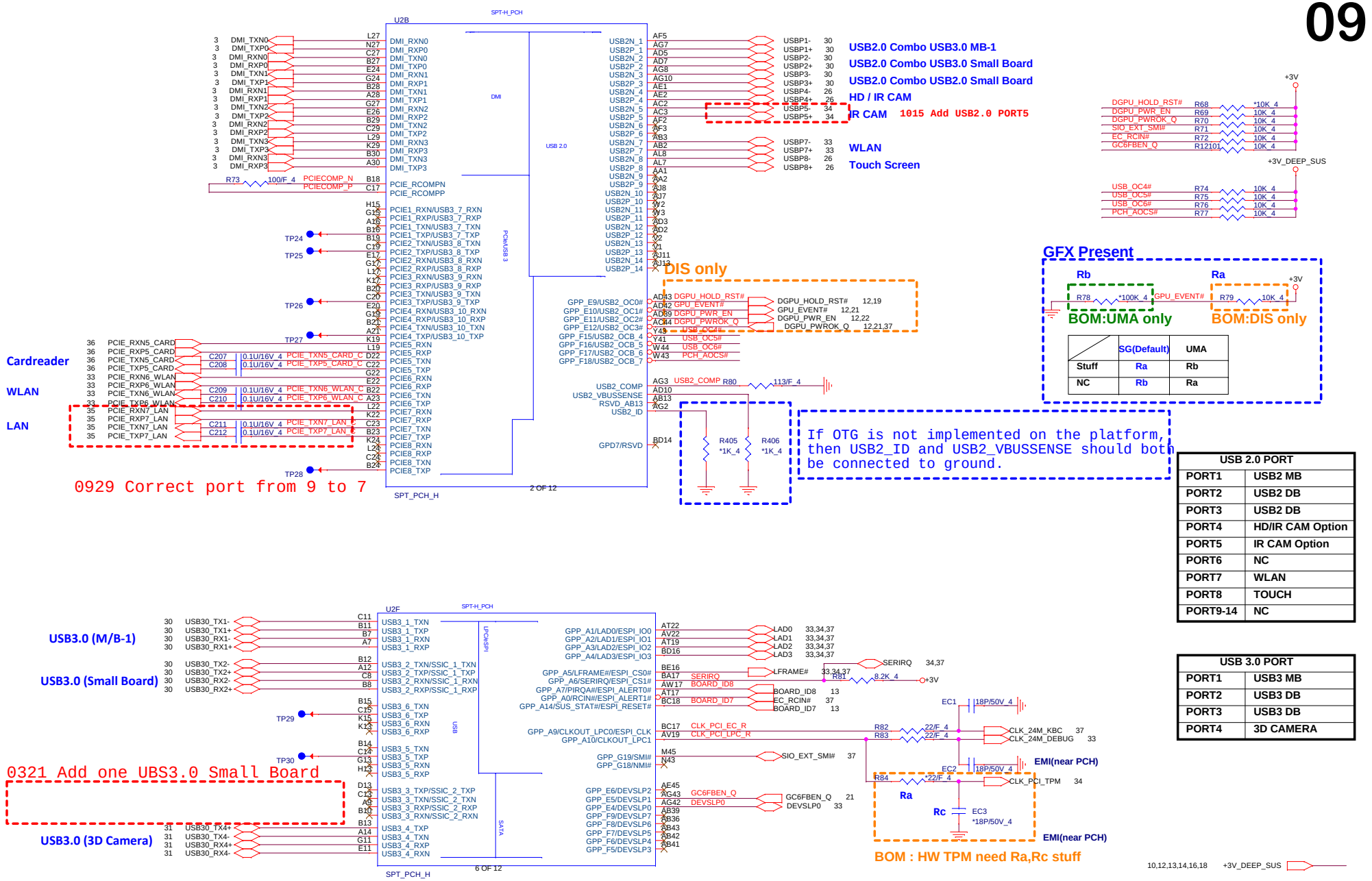

	SG(Default)	UMA
Stuff	Ra	Rb
NC	Rb	Ra

USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB
PORT3	USB2 DB
PORT4	HD/IR CAM Option
PORT5	IR CAM Option
PORT6	NC
PORT7	WLAN
PORT8	TOUCH
PORT9-14	NC

USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	USB3 DB
PORT4	3D CAMERA

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- PCH 1/7 (DMI/USB/PCIE)	1A

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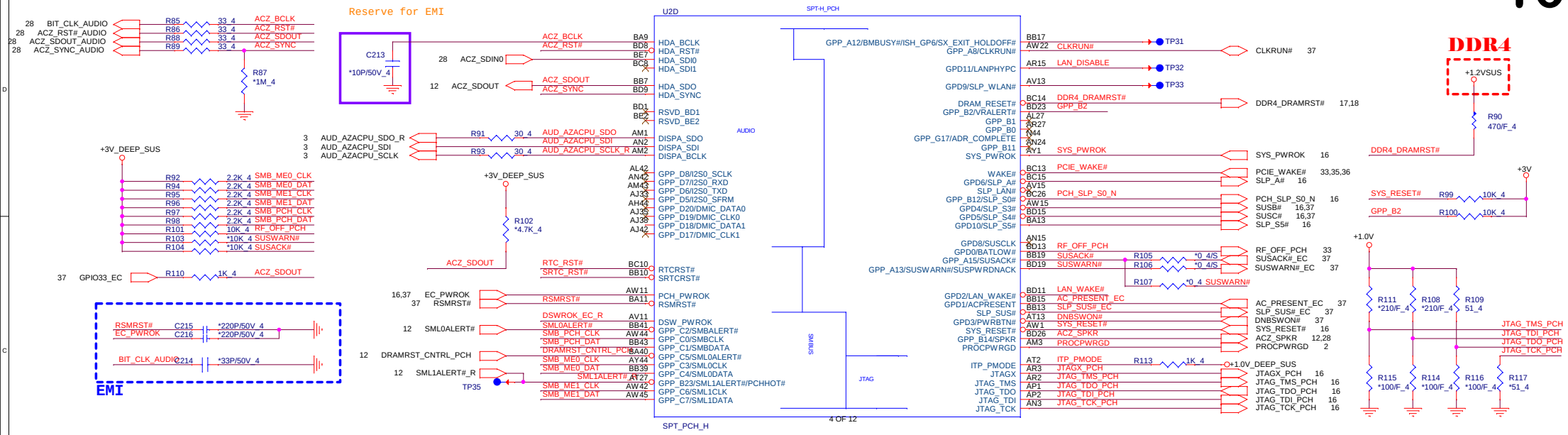
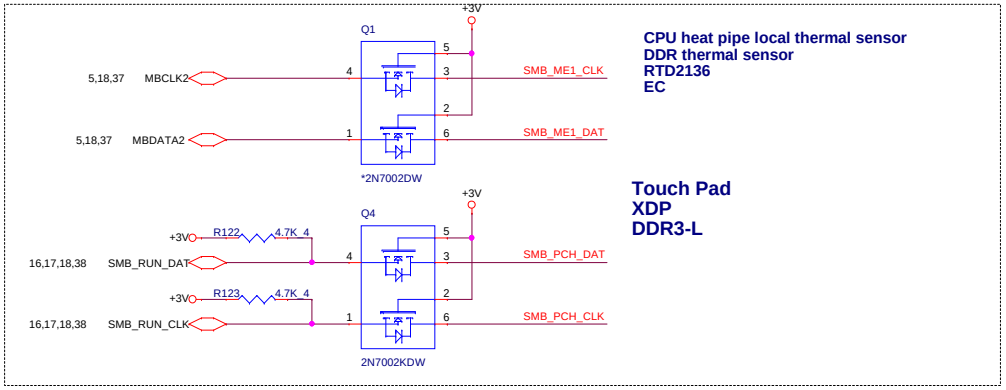
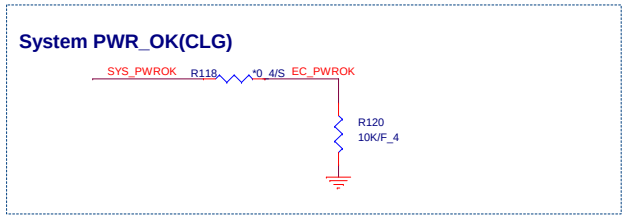
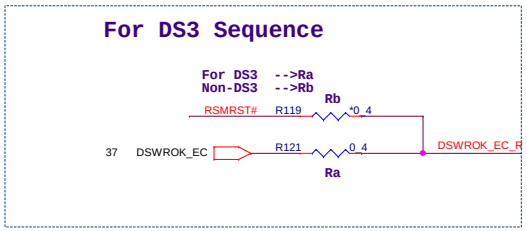
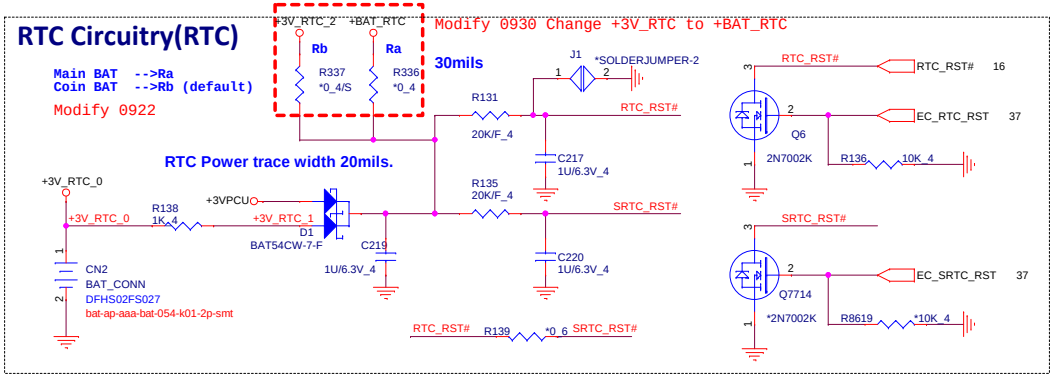
HDA Bus(CLG)

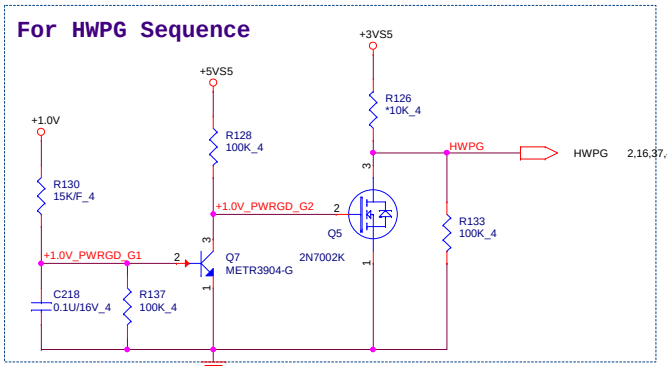


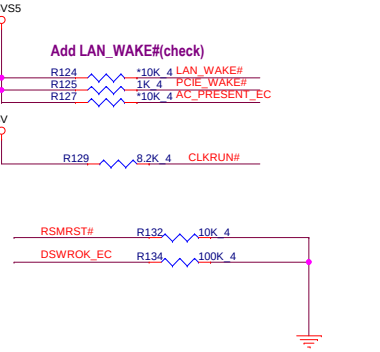












PROJECT : G35
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Size	Document Number	Rev
Custom	10 -- PCH 2/7 (HDA/SMBUS)	1A

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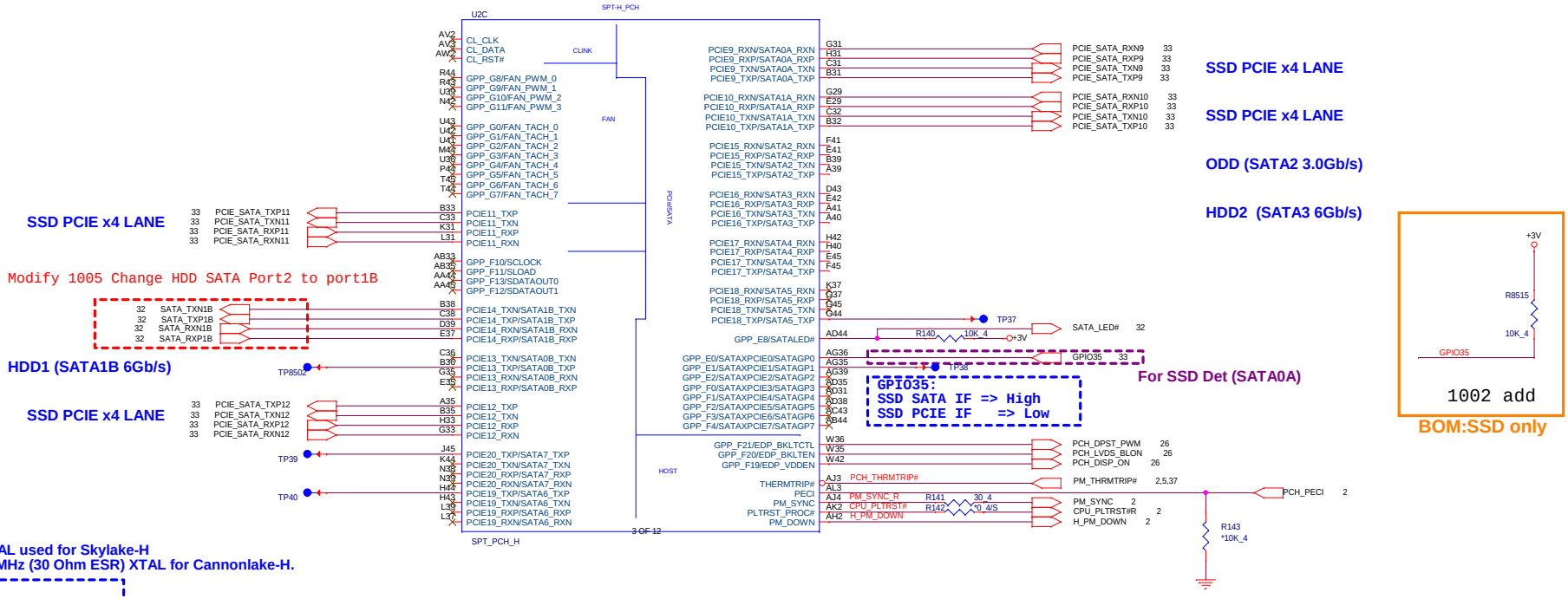
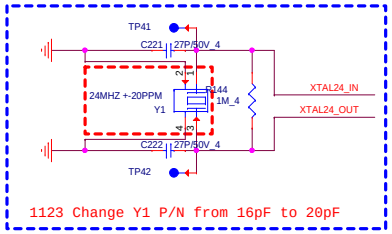
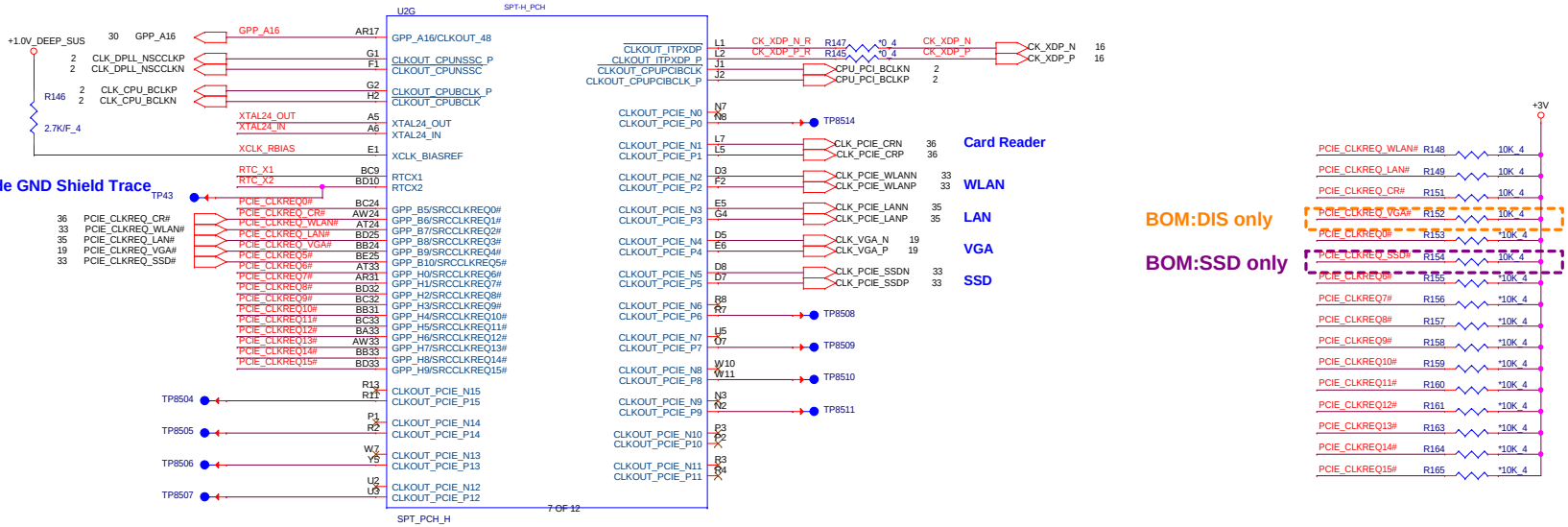
HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	NC
PCIE17	NC
PCIE18-20	NC



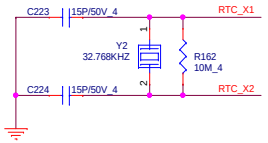
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H
needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.



Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace



RTC Clock 32.768KHz



32.768KHz
BG332768453 CRYSTAL SMD 32.768KHZ(+-20PPM,12.5PF)
footprint: xtl-3_2X1_5-2_5-0_8h

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 – PCH 3/7 (SATA/LPC/CLK)	1A

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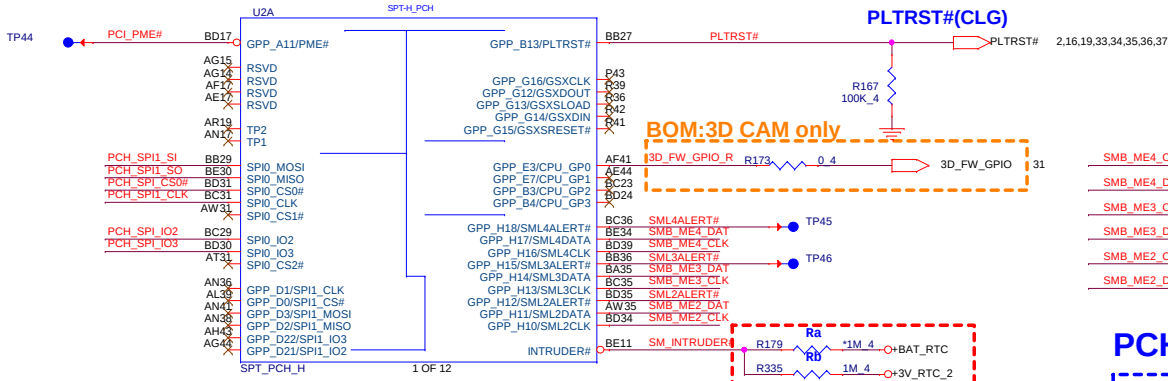
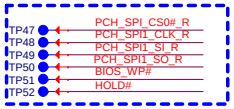


BOM:3D CAM only

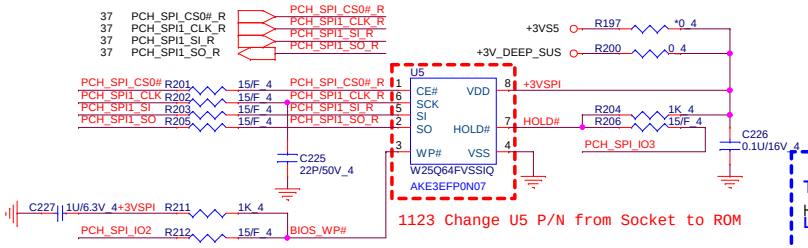
support HW TPM -->Ra
support SW TPM -->Rb (default)

Modify 0930 Change +3V_RTC to +BAT_RTC

PCH SPI ROM(CLG)



Place to TOP



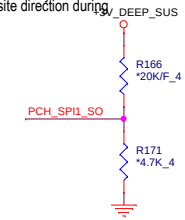
1123 Change U5 P/N from Socket to ROM

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

PCH Strap Pin

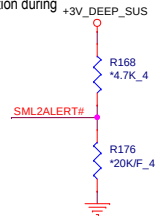
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



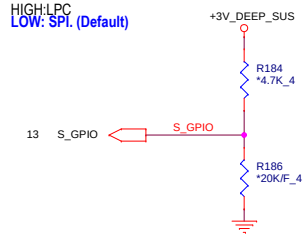
ESPI FLASH SHARING MODE

HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



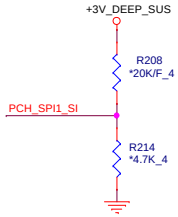
BOOT SELECT STRAP

HIGH:LPC
LOW: SPI. (Default)

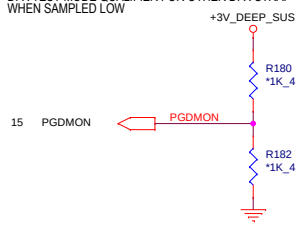


RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

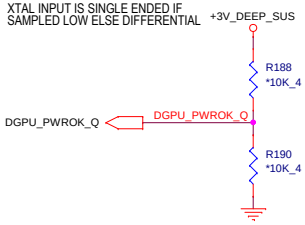


DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW



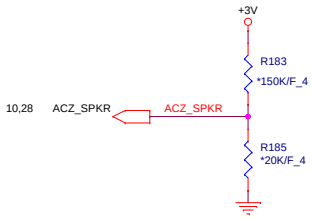
DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



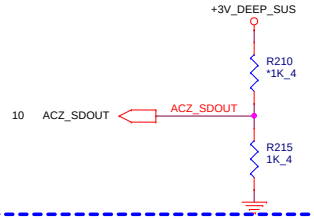
TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)



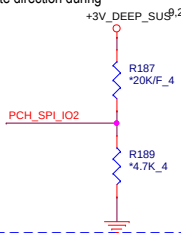
TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)
LOW: security measures defined in the Flash Descriptor. (Default)

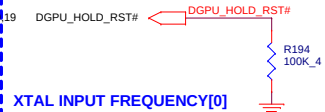


RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

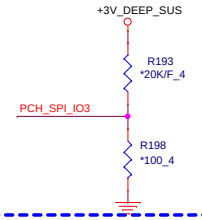


RING OSCILLATOR BYPASS

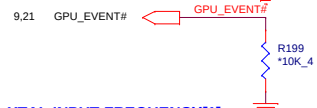


RESERVED

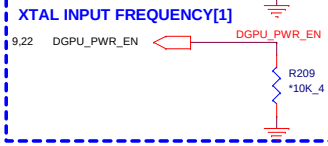
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



XTAL INPUT FREQUENCY[0]

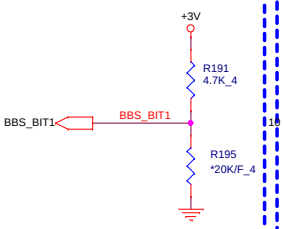


XTAL INPUT FREQUENCY[1]



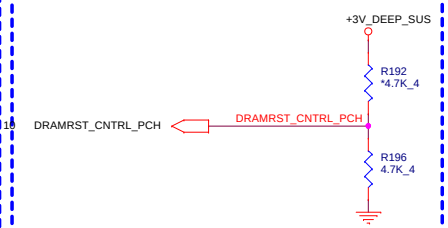
NO REBOOT IF SAMPLED HIGH

HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)



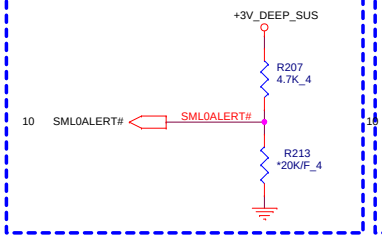
ESPI/LPC SELECT STRAP

HIGH:eSPI Is selected for EC.
LOW: LPC Is selected for EC. (Default)



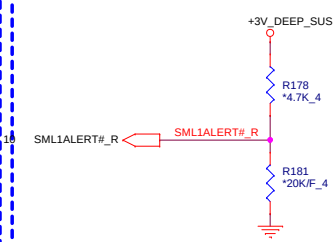
TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



RESERVED

This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- PCH 4/7 (GPIO/MISC)	1A

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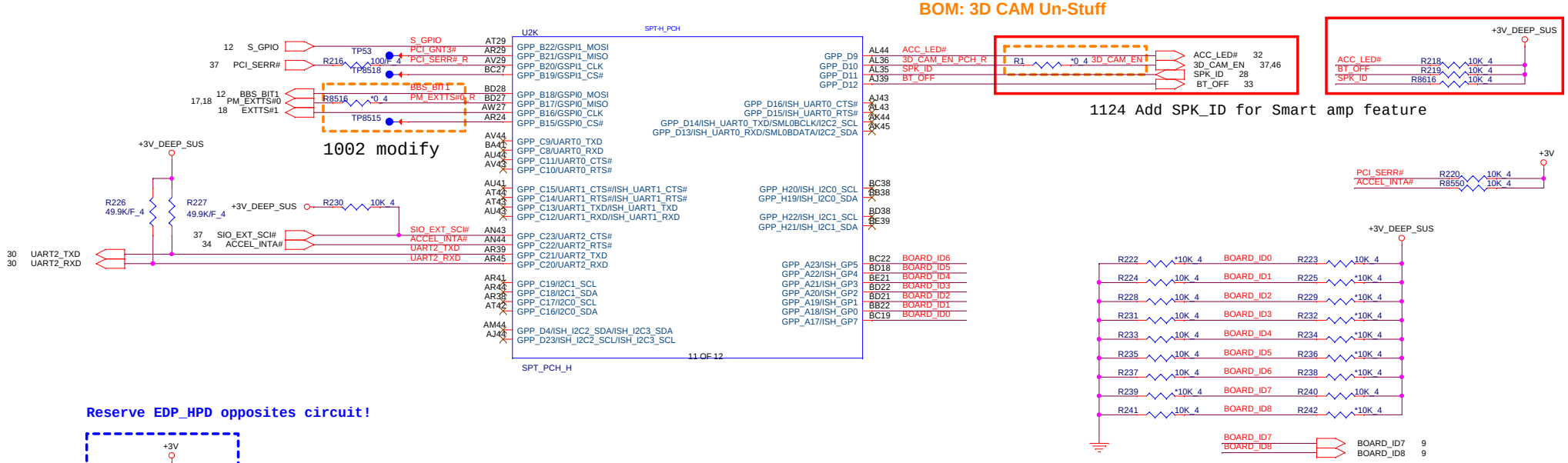
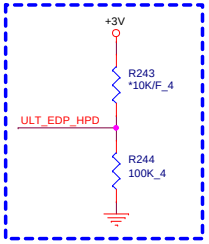
9,10,12,14,16,18 +3V_DEEP_SUS

3D CAMERA
BOM: 3D CAM Un-Stuff

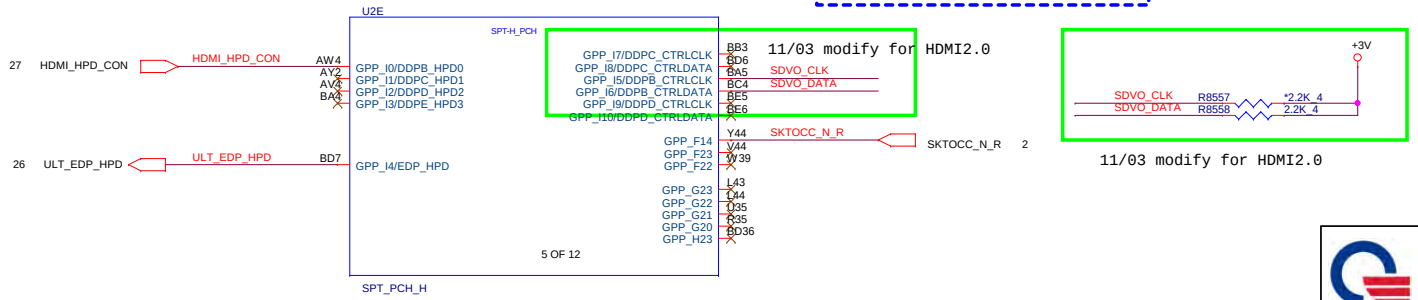


Reserve EDP_HPD opposites circuit!



Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3		BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	01 SKL H 10 KBL H *RSV	00 Reserve	ID4 Reserve	ID3 0 Nvidia 1 AMD	00 15" 01 17" 10 17" SP	0 : UMA 1 : DIS

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- PCH 5/7 (GPIO)	1A

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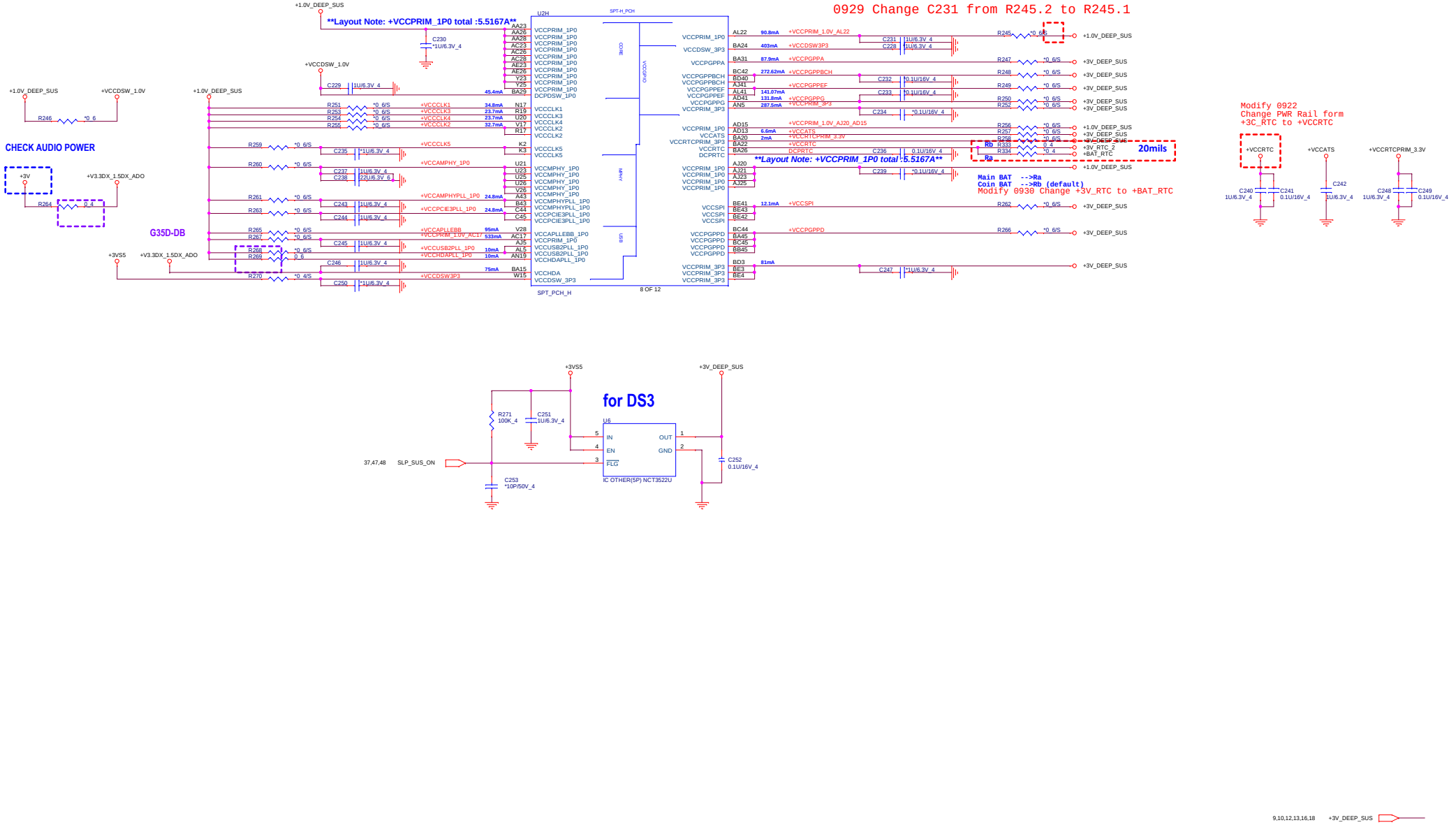

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 -- PCH 6/7 (POWER)	1A

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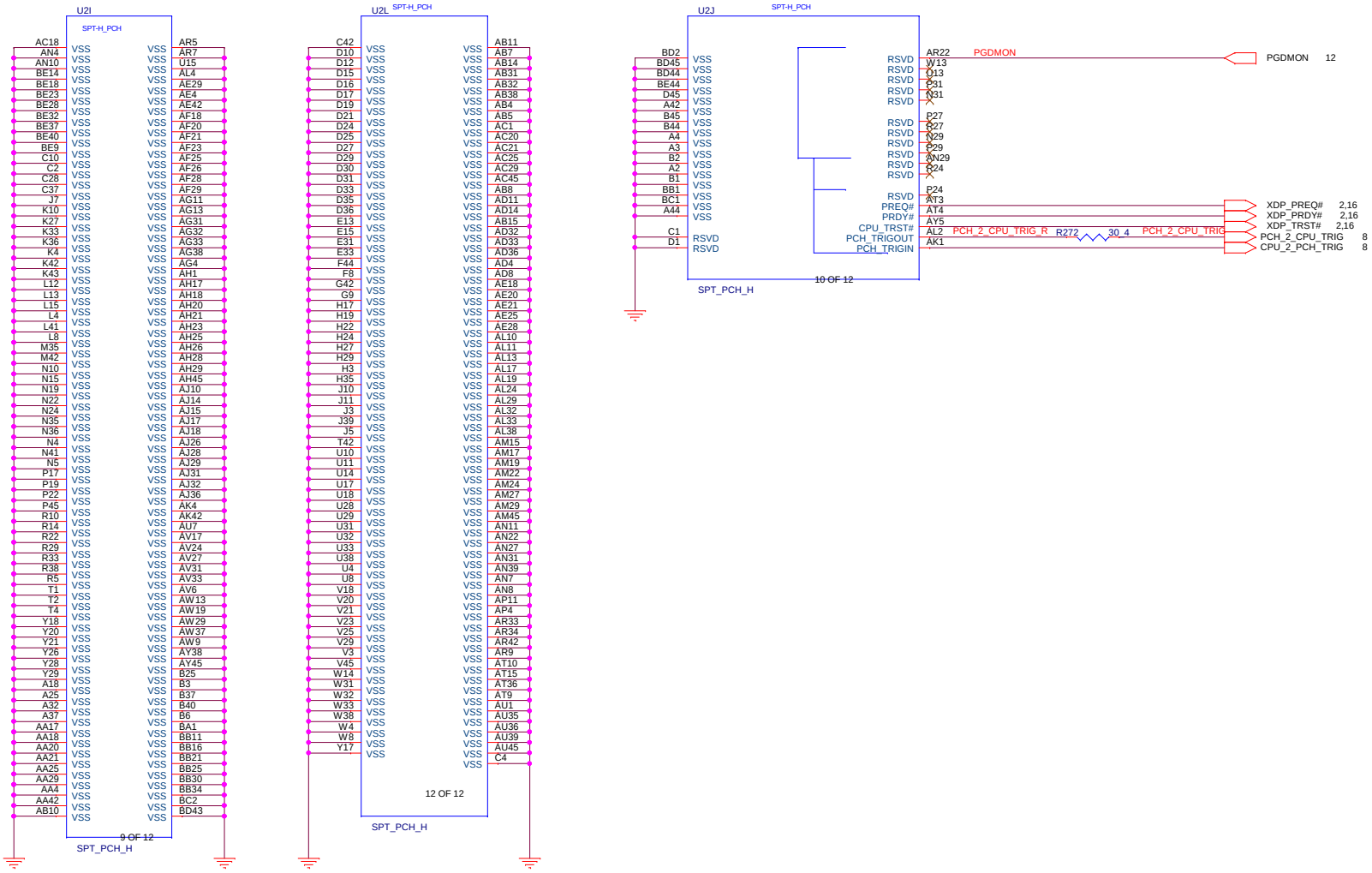

PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	15 -- PCH 7/7 (GND)	1A

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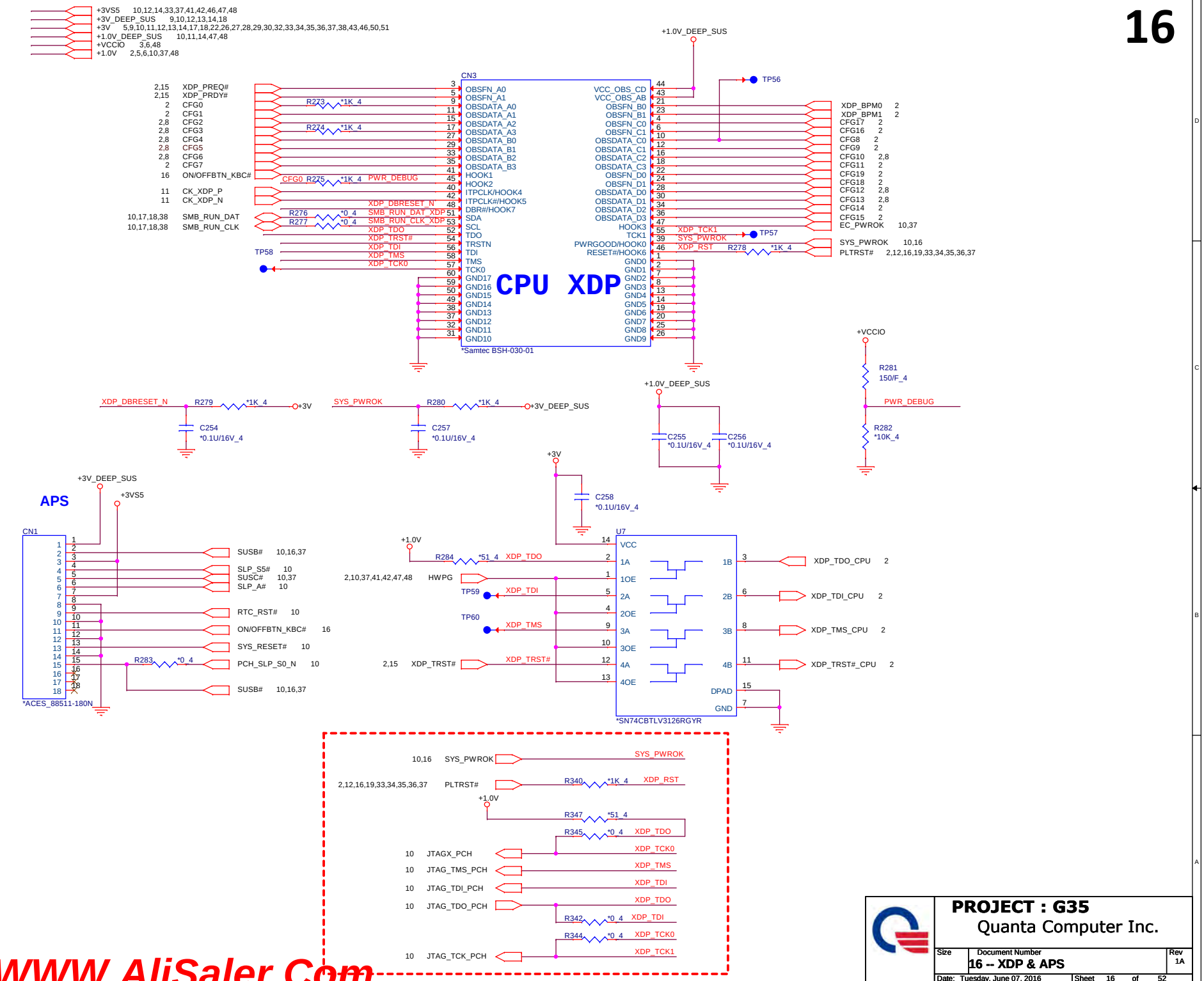

PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
	16 -- XDP & APS	1A

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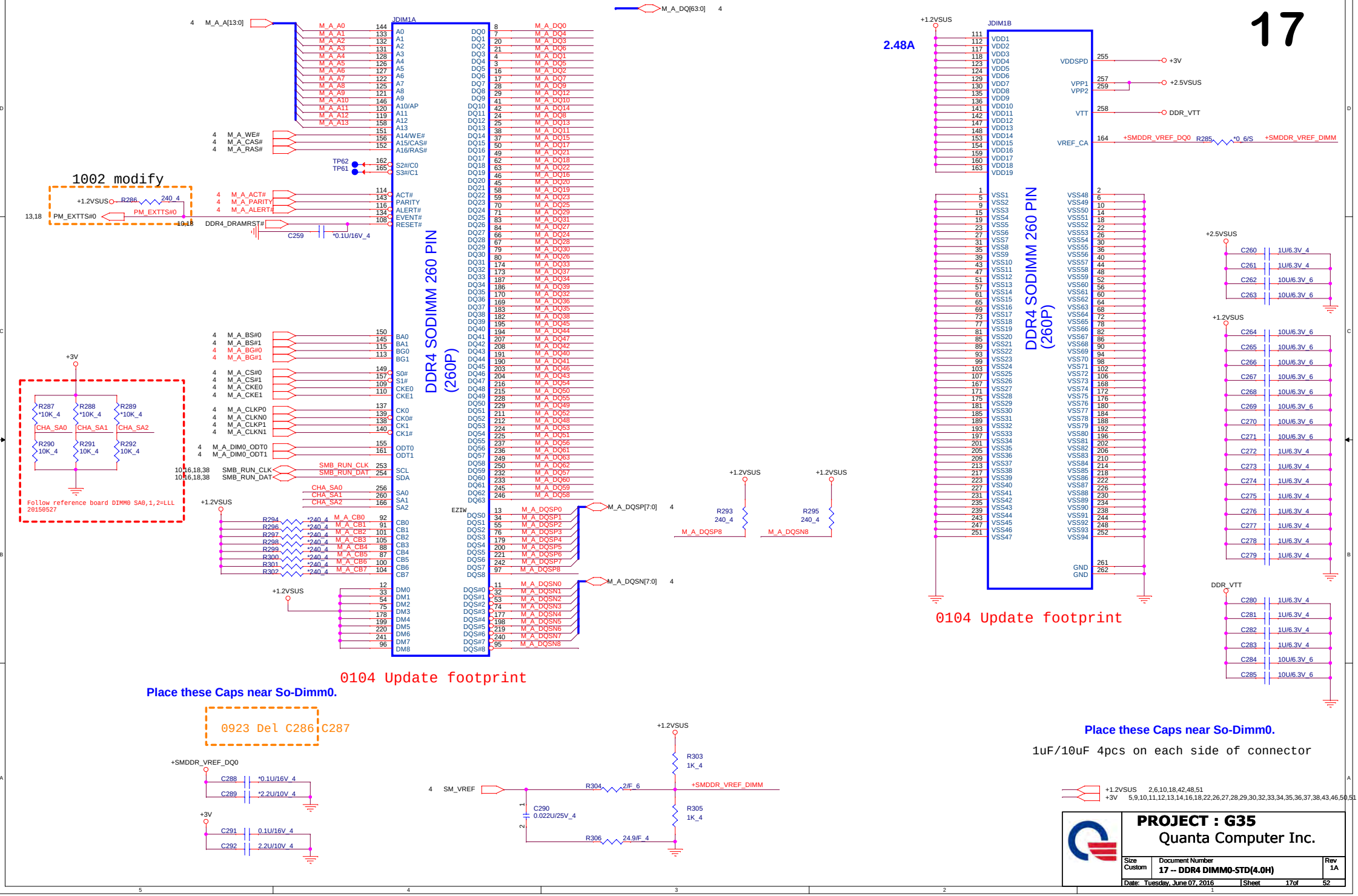
JDIM1A
DDR4 SODIMM 260 PIN (260P)
M_A_A[13:0]
M_A_DQ[63:0]
M_A_DQSP[7:0]
M_A_DQSN[7:0]
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_ACT#
M_A_PARITY
M_A_ALERT#
DDR4_DRAMRST#
C259
*0.1U/16V_4
1002 modify
+1.2VSUS
R286
240_4
PM_EXTTS#0
13,18
10,18
M_A_BS#0
M_A_BS#1
M_A_BG#0
M_A_BG#1
M_A_CS#0
M_A_CS#1
M_A_CKE0
M_A_CKE1
M_A_CLKP0
M_A_CLKN0
M_A_CLKP1
M_A_CLKN1
M_A_DIM0_ODT0
M_A_DIM0_ODT1
SMB_RUN_CLK
SMB_RUN_DAT
10,16,18,38
CHA_SA0
CHA_SA1
CHA_SA2
+3V
R287 *10K_4
R288 *10K_4
R289 *10K_4
R290 10K_4
R291 10K_4
R292 10K_4
Follow reference board DIMM0 SA0,1,2=LLL 20150527
R294 *240_4
R296 *240_4
R297 *240_4
R298 *240_4
R299 *240_4
R300 *240_4
R301 *240_4
R302 *240_4
M_A_CB0
M_A_CB1
M_A_CB2
M_A_CB3
M_A_CB4
M_A_CB5
M_A_CB6
M_A_CB7
TP62
TP61
EZIW
R293 240_4
R295 240_4
M_A_DQSP8
M_A_DQSN8
JDIM1B
DDR4 SODIMM 260 PIN (260P)
2.48A
VDDSPD
+3V
VPP1
VPP2
+2.5VSUS
VTT
DDR_VTT
VREF_CA
+SMDDR_VREF_DQ0
R285
*0_6/S
+SMDDR_VREF_DIMM
C260 1U/6.3V_4
C261 1U/6.3V_4
C262 10U/6.3V_6
C263 10U/6.3V_6
C264 10U/6.3V_6
C265 10U/6.3V_6
C266 10U/6.3V_6
C267 10U/6.3V_6
C268 10U/6.3V_6
C269 10U/6.3V_6
C270 10U/6.3V_6
C271 10U/6.3V_6
C272 1U/6.3V_4
C273 1U/6.3V_4
C274 1U/6.3V_4
C275 1U/6.3V_4
C276 1U/6.3V_4
C277 1U/6.3V_4
C278 1U/6.3V_4
C279 1U/6.3V_4
C280 1U/6.3V_4
C281 1U/6.3V_4
C282 1U/6.3V_4
C283 1U/6.3V_4
C284 10U/6.3V_6
C285 10U/6.3V_6
0104 Update footprint
0104 Update footprint
Place these Caps near So-Dimm0.
0923 Del C286 C287
+SMDDR_VREF_DQ0
C288 *0.1U/16V_4
C289 *2.2U/10V_4
C291 0.1U/16V_4
C292 2.2U/10V_4
SM_VREF
R303 1K_4
R304 2/F_6
R305 1K_4
R306 24.9/F_4
C290 0.022U/25V_4
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
+1.2VSUS 2,6,10,18,42,48,51
+3V 5,9,10,11,12,13,14,16,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
PROJECT : G35
Quanta Computer Inc.
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
Date: Tuesday, June 07, 2016
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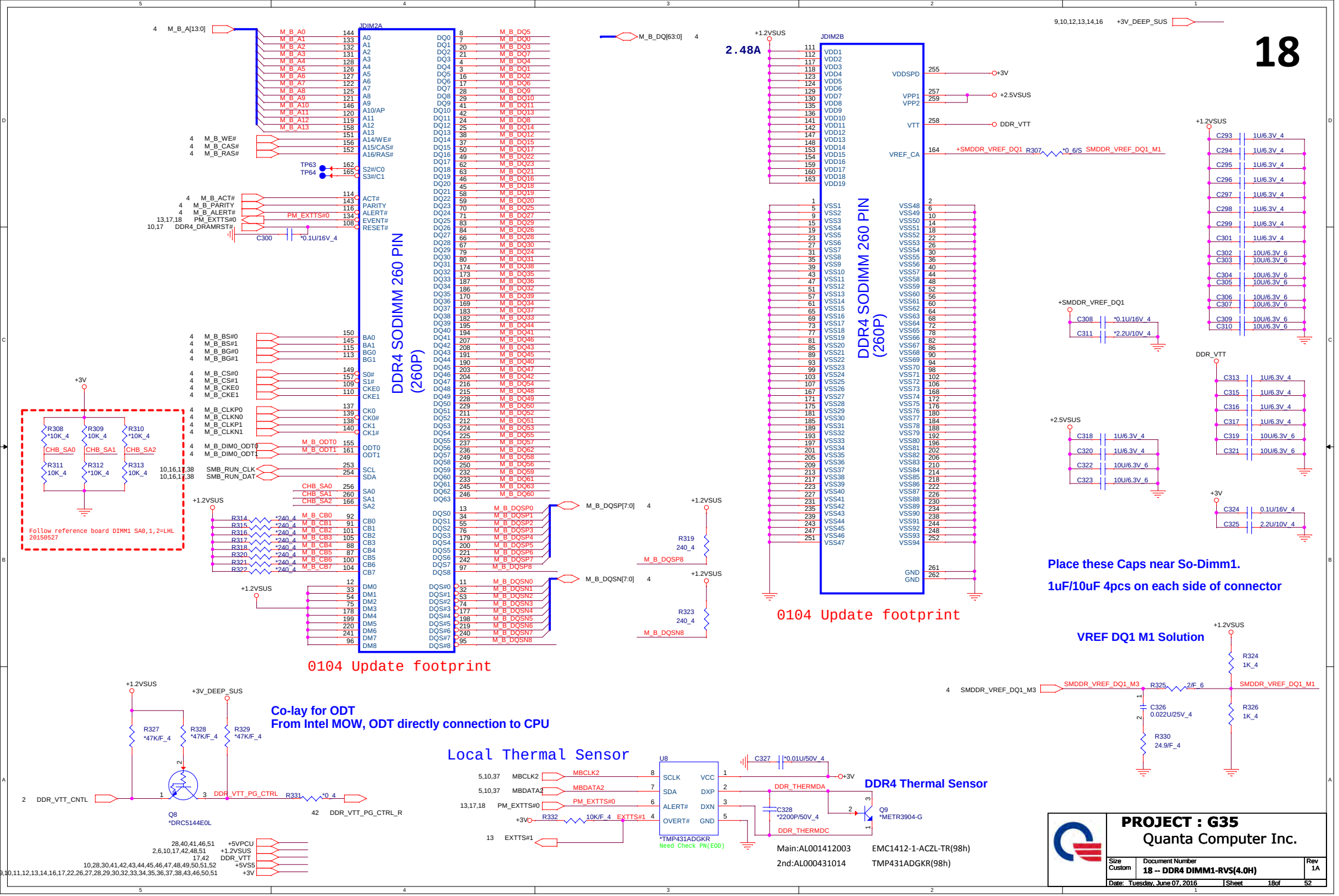

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	18 -- DDR4 DIMM1-RVS(4.0H)	1A

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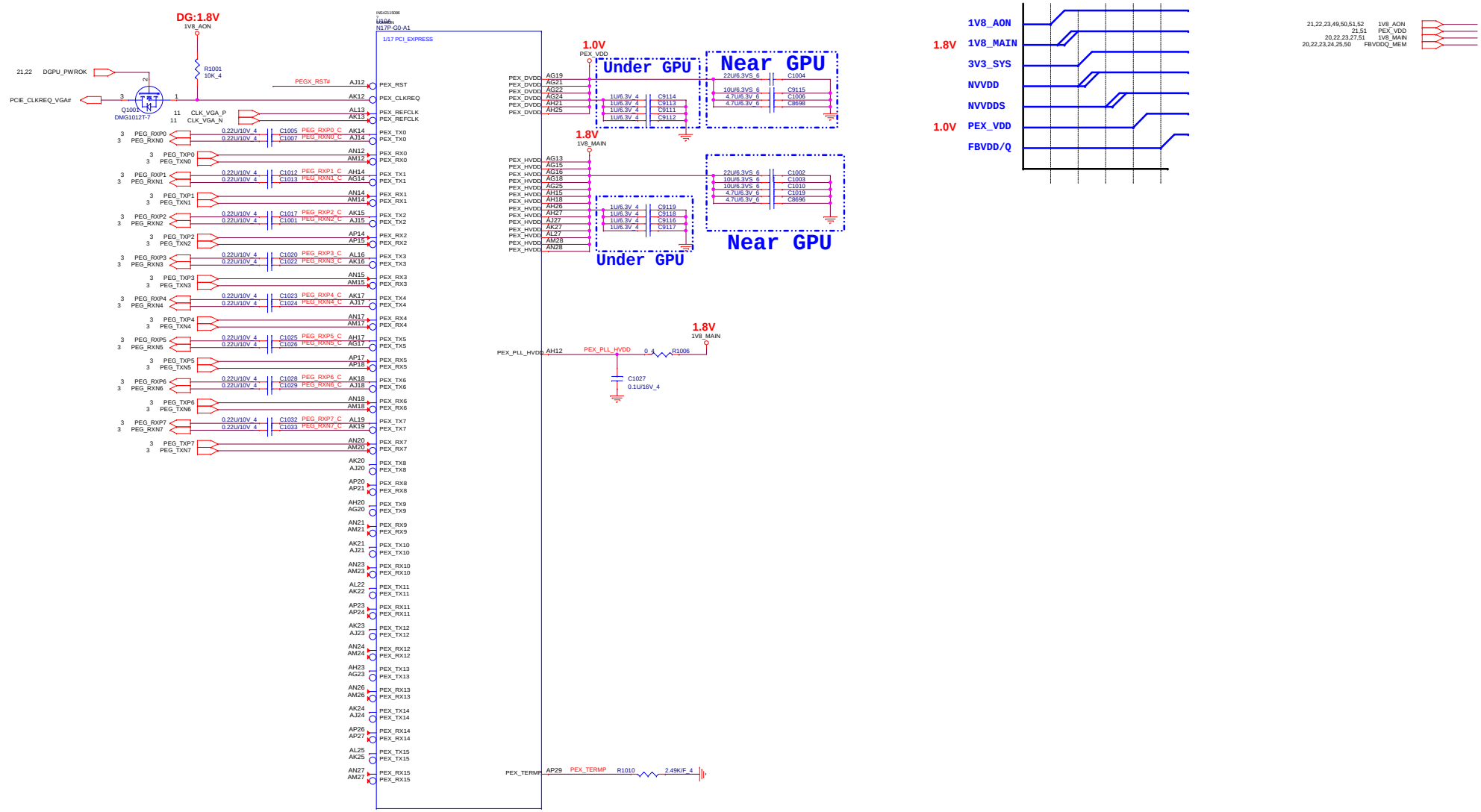
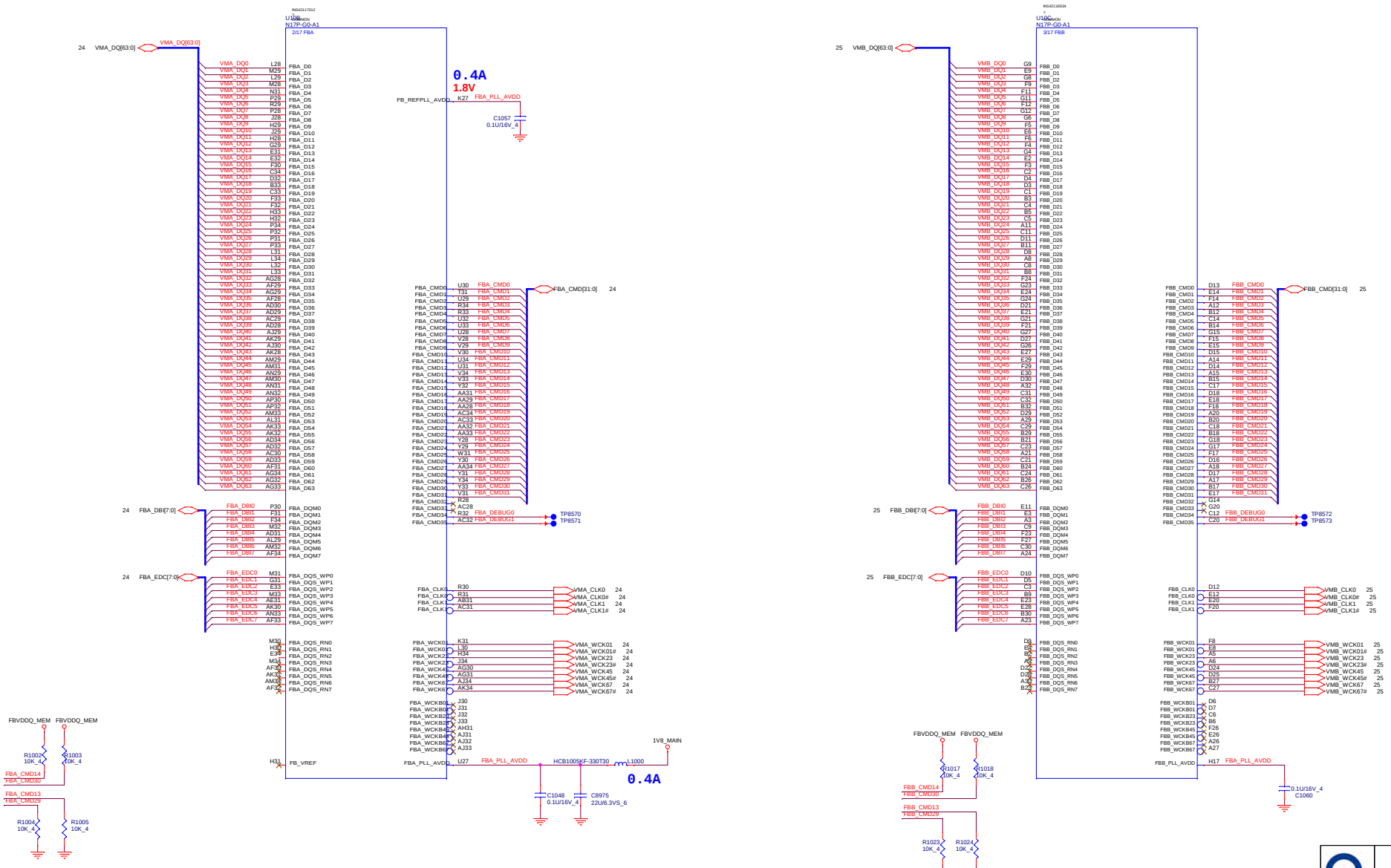


NB5 Custom	**PROJECT : G38A** Quanta Computer Inc.		
Size	Document Number N17P-G0-A1-1/9		Rev 1A
Date: Tuesday, June 07, 2016	Sheet 19 of 52		

19,22,23,27,51 1V8_MAIN
22,23,24,25,50 FBVDDQ_MEM



PROJECT : G38A
Quanta Computer Inc.

Size	Document Number	Rev
NB5 Custom	N17P-G0-A1-2/9	1A

Date: Tuesday, June 07, 2016 Sheet 20 of 52

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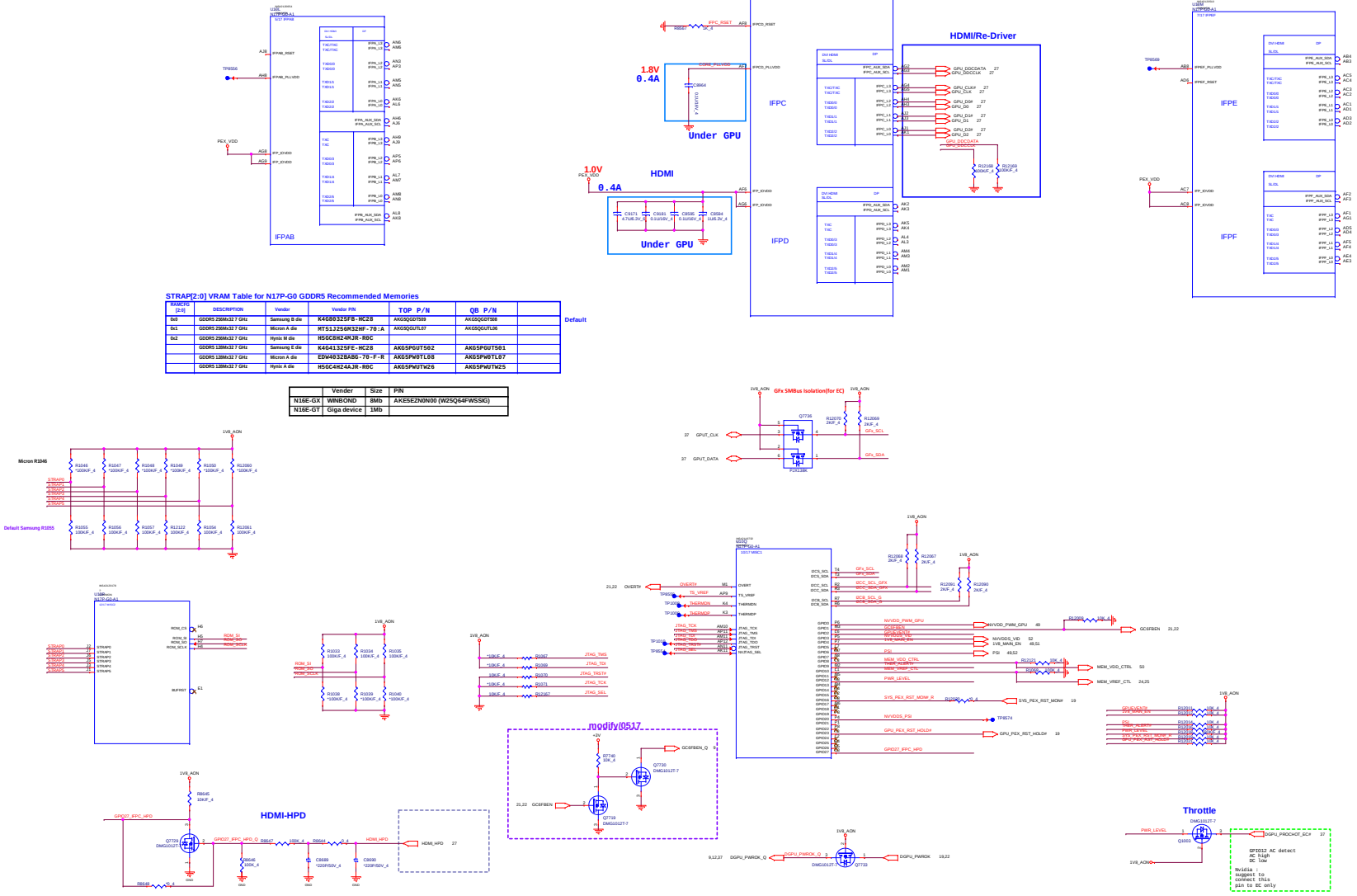


STRAP[2:0] VRAM Table for N17P-G0 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor PIN	TOP P/N	QB P/N	
0x0	GDDR5 256Mx32 7 GHz	Samsung B die	K4G80325FB-HC28	AKG5QGDT509	AKG5QGDT508	Default
0x1	GDDR5 256Mx32 7 GHz	Micron A die	MT51J256M32HF-70:A	AKG5QGUTL07	AKG5QGUTL06	
0x2	GDDR5 256Mx32 7 GHz	Hynix M die	H5GC8H24MJR-R0C			
	GDDR5 128Mx32 7 GHz	Samsung E die	K4G41325FE-HC28	AKG5PGUTS02	AKG5PGUTS01	
	GDDR5 128Mx32 7 GHz	Micron A die	EDW4032BABG-70-F-R	AKG5PWUTL08	AKG5PWUTL07	
	GDDR5 128Mx32 7 GHz	Hynix A die	H5GC4H24AJR-R0C	AKG5PWUTW26	AKG5PWUTW25	

	Vender	Size	P/N
N16E-GX	WINBOND	8Mb	AKE5EZN0N00 (W25Q64FWSSIG)
N16E-GT	Giga device	1Mb	

Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GCM: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 kΩ pull-down
GPIO2	GCM: GPU_EVENT#/ WAKE*	I	GPU wake signal for GC6 2.1	10kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GCM:1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10kΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

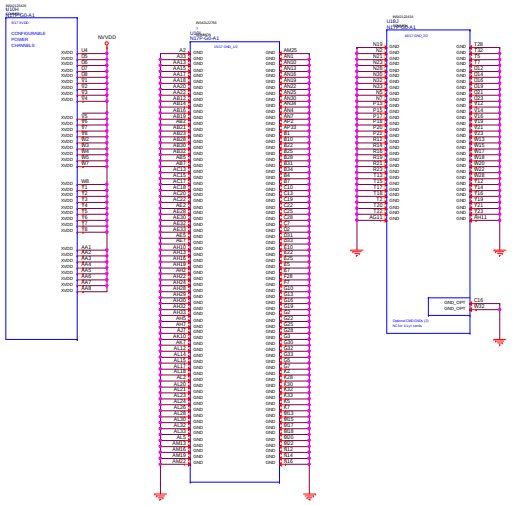
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.1.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBPWM power-on strap
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory Vref Control	10 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	3.3 power detect or power supply monitor input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted Input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted Input. See Figure 14.3
GPIO16	GCM: GPU_PEX_RST_MONI#	I/O	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted Input. See Figure 14.3
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted Input. See Figure 14.5
GPIO19	3D_VISION	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	MUX_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

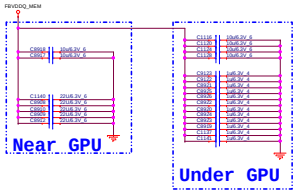
Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

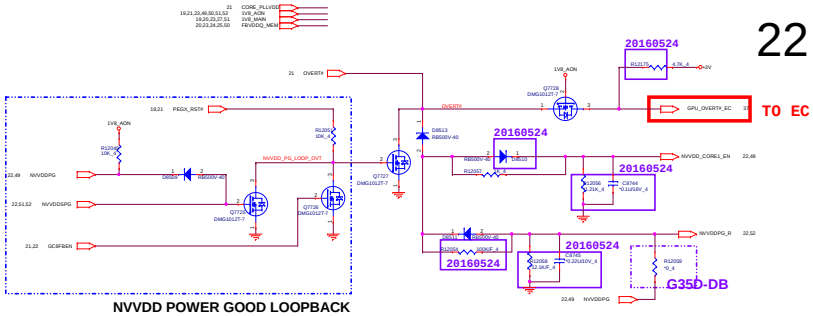
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GCM: GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to 3V3_AON
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted Input. See Figure 14.5
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted Input. See Figure 14.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

Morgan Chang NVIDIA Confidential
Quanta HP Notebook 2012-12-22
Quanta HP Notebook 2012-12-22



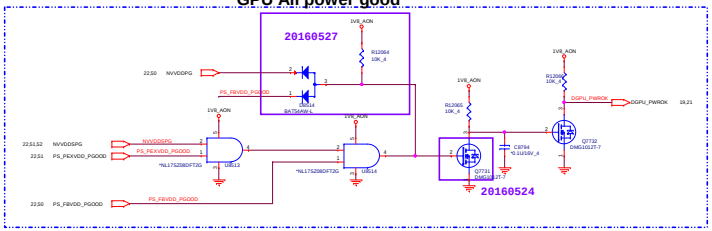




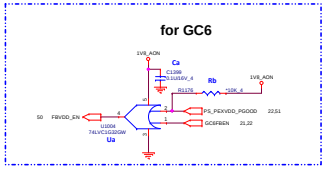
NVVDD POWER GOOD LOOPBACK

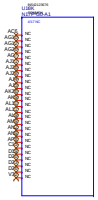
Overt temp ckt for NVVDD and NVVDDS

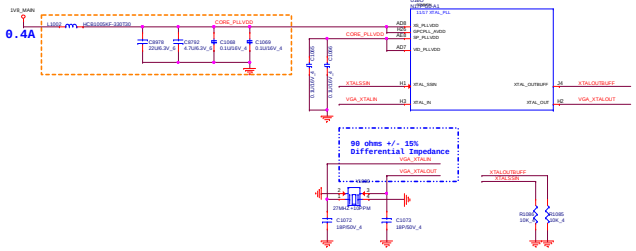
GPU All power good



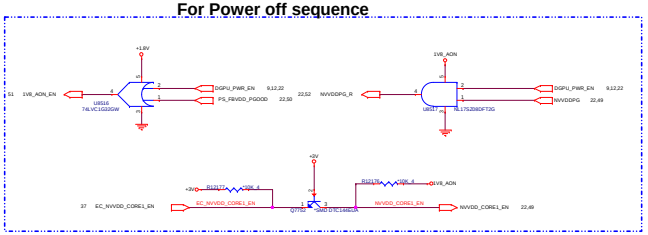
for GC6







For Power off sequence



NB5	PROJECT : G38A Quanta Computer Inc.
Size	Document Number: N17P-G0-A1-4/9
Rev	1A
Date: Tuesday, June 07, 2016	Sheet 9 of 59

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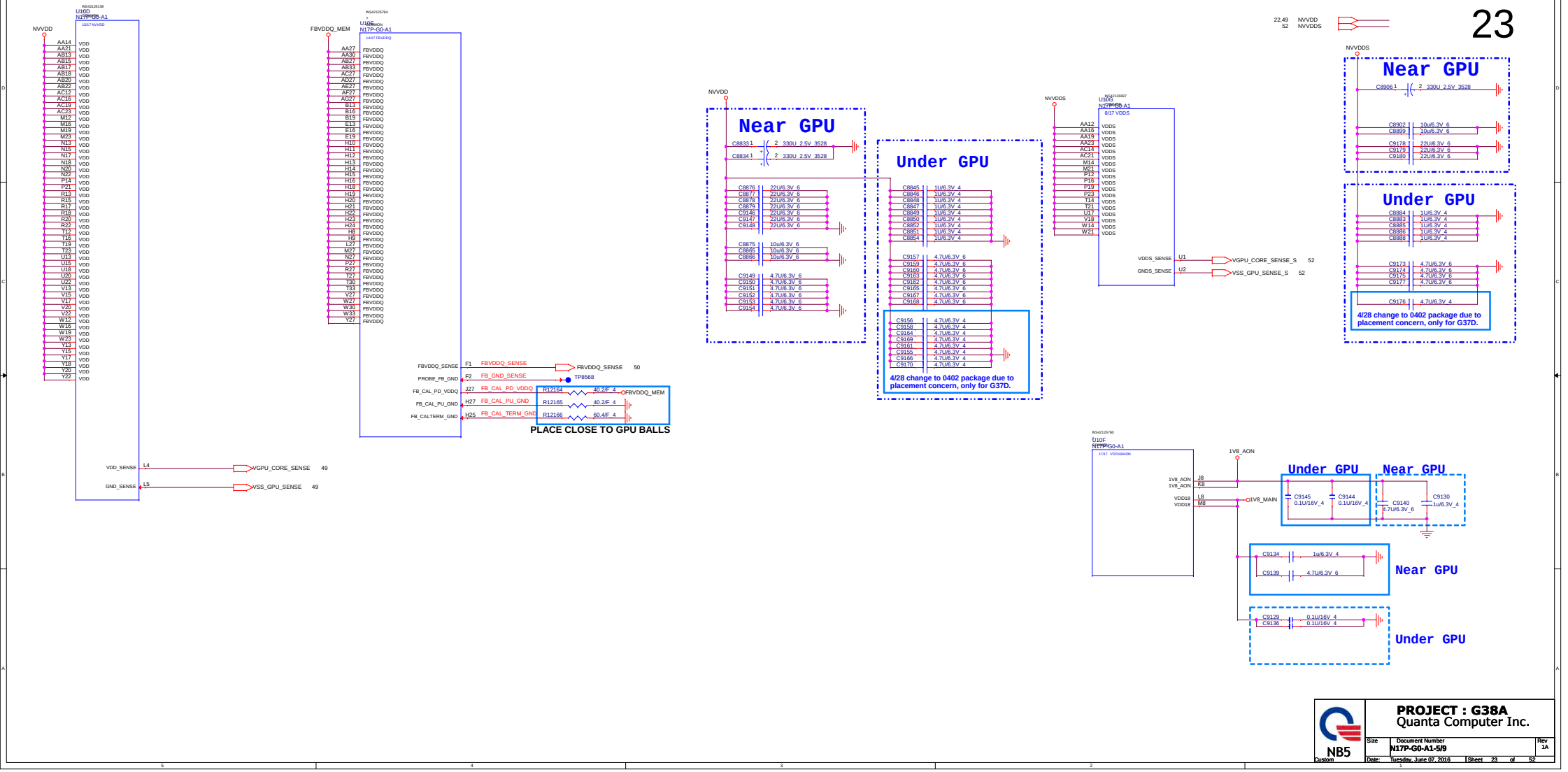

NB5 Custom	PROJECT : G38A Quanta Computer Inc.		
	Size	Document Number N17P-G0-A1-5/9	Rev 1A
	Date: Tuesday, June 07, 2016	Sheet 23 of 52	

CHANNEL A: 2G/4G GDDR5

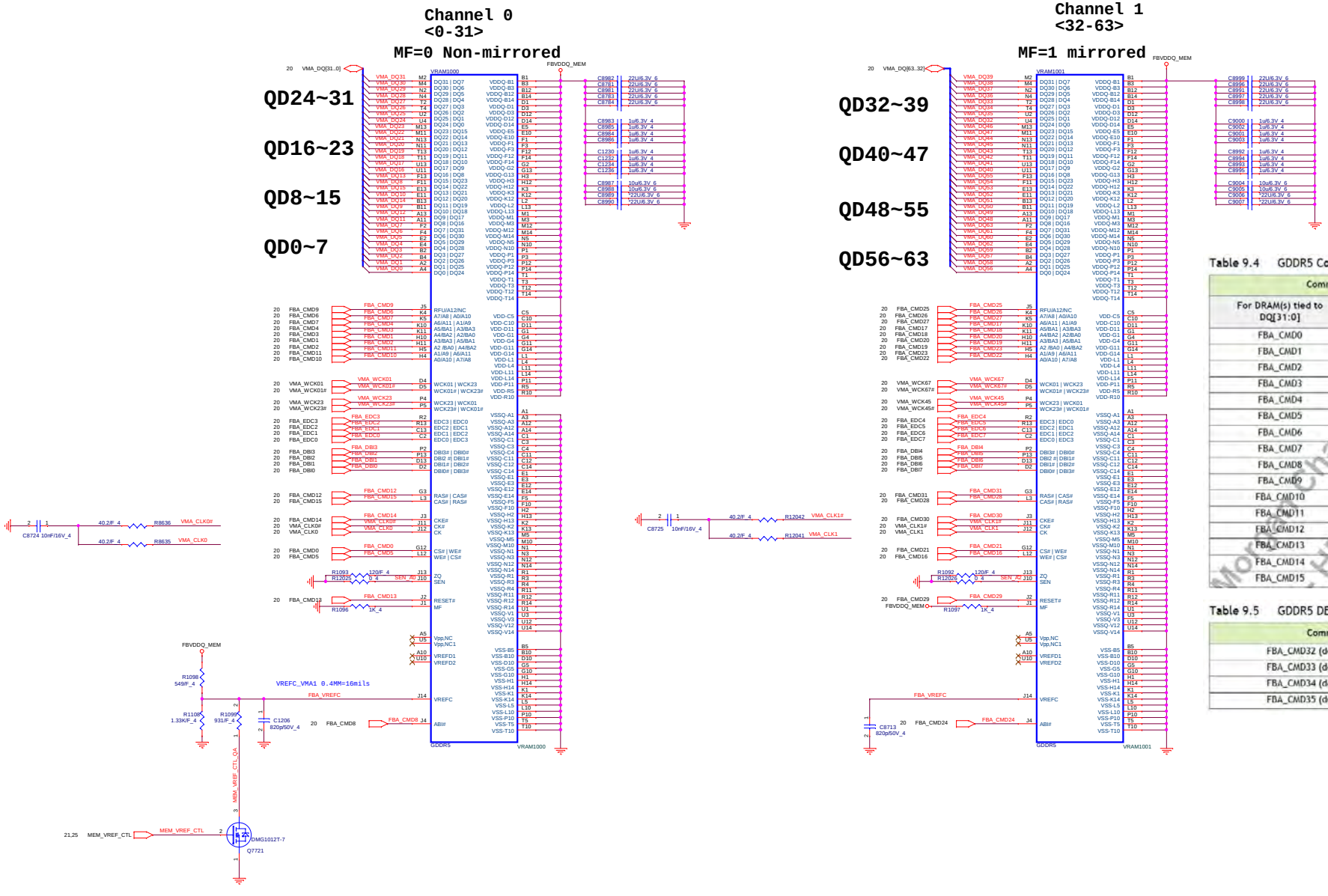

Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

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CHANNEL B: 2G/4G GDDR5

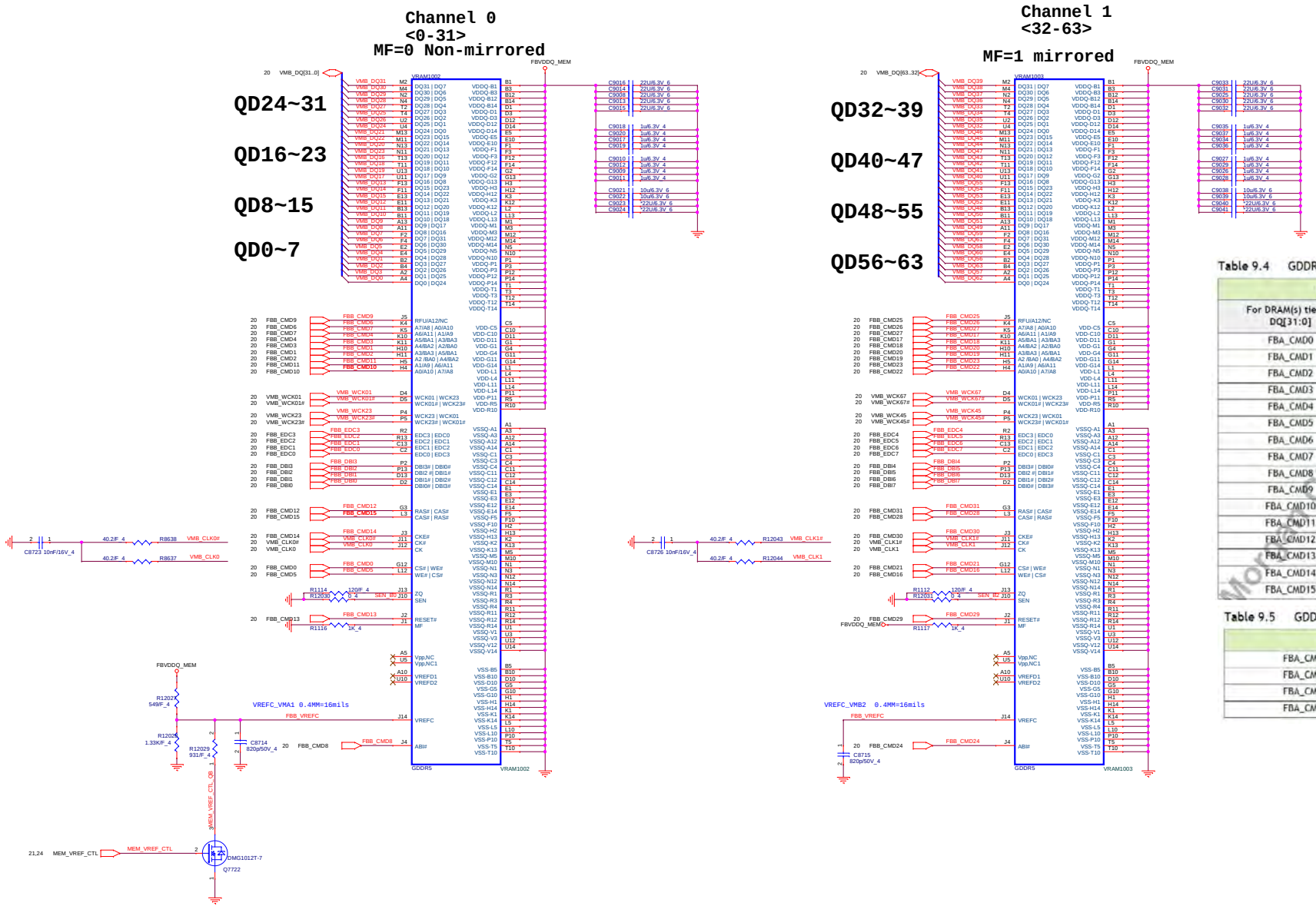


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

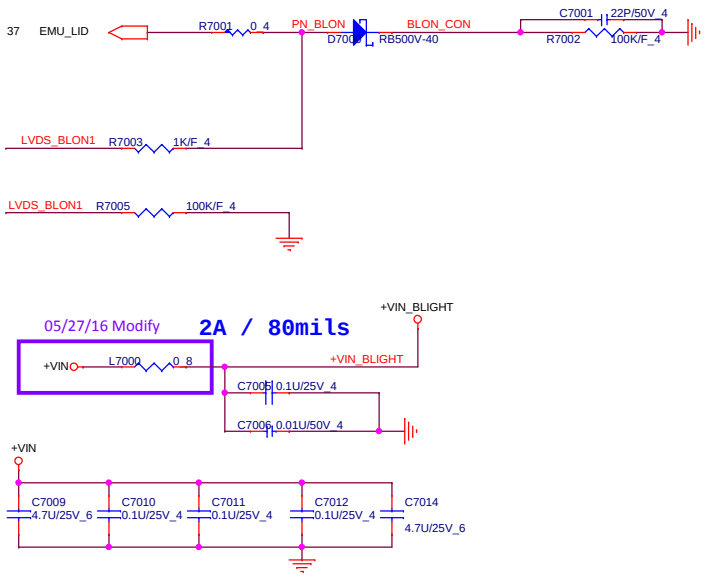
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

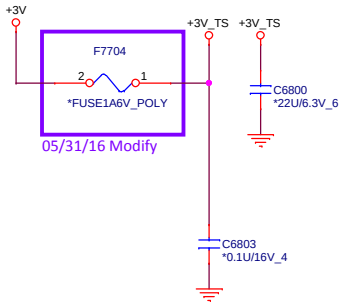
Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

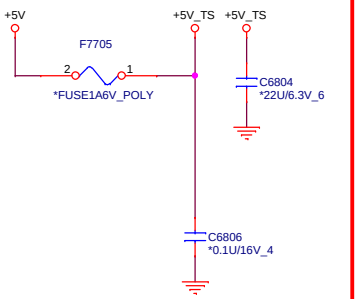
Morris Chang NB5 HP Notebook 2016-02-29
2016-02-29

LID Switch

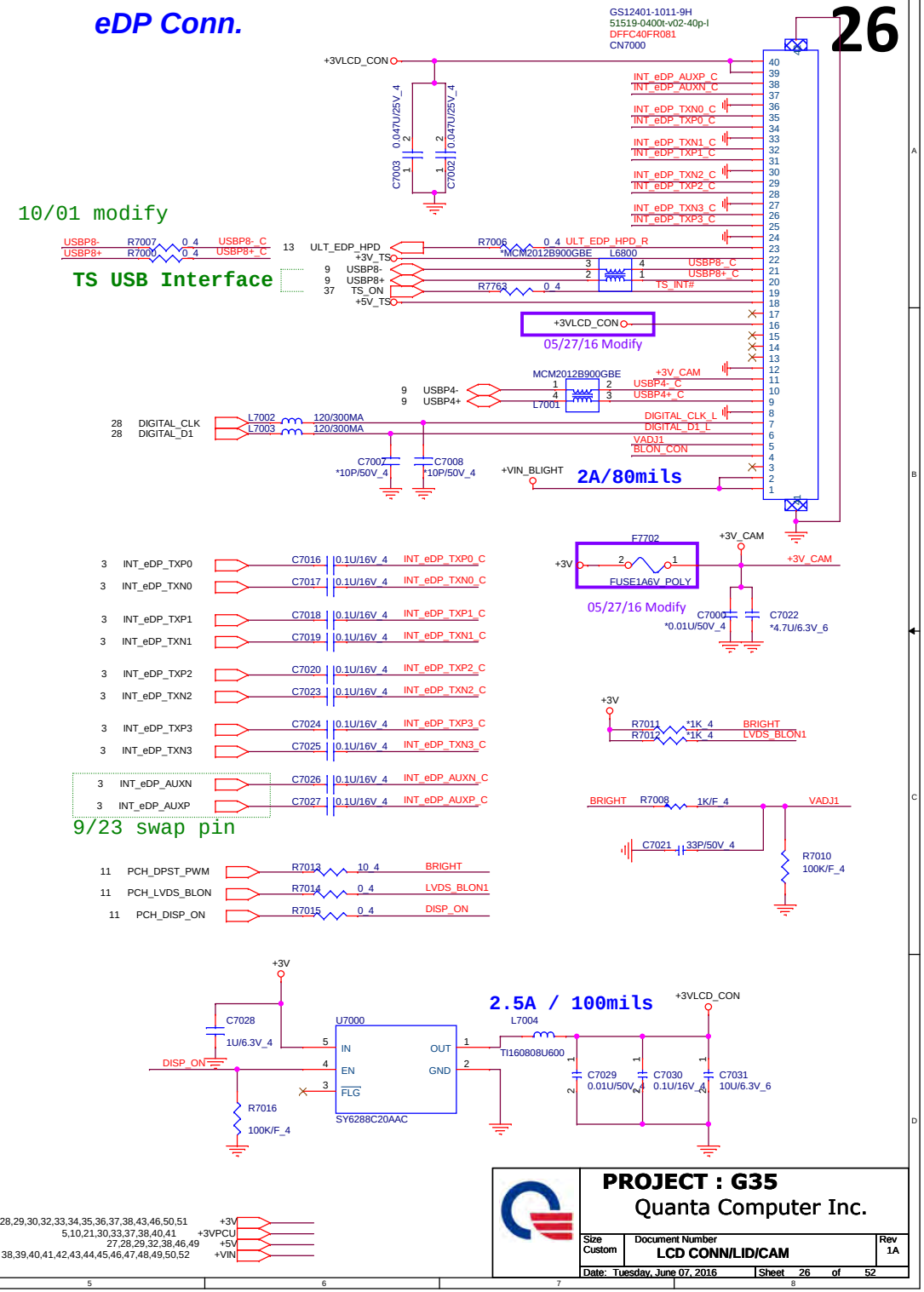


Touch screen





eDP Conn.



5,9,10,11,12,13,14,16,17,18,22,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51 +3V
5,10,21,30,33,37,38,40,41 +3VPCU
27,28,29,32,38,46,49 +5V
38,39,40,41,42,43,44,45,46,47,48,49,50,52 +VIN

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Quanta Computer Inc.

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Custom	LCD CONN/LID/CAM	1A

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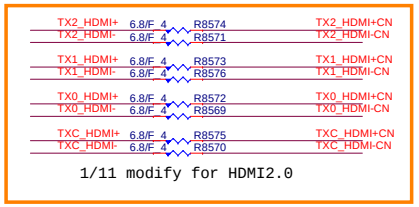
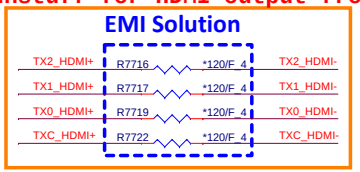
5,9,10,11,12,13,14,16,17,18,22,26,28,29,30,32,33,34,35,36,37,38,43,46,50,51 +3V

26,28,29,32,38,46,49 +5V

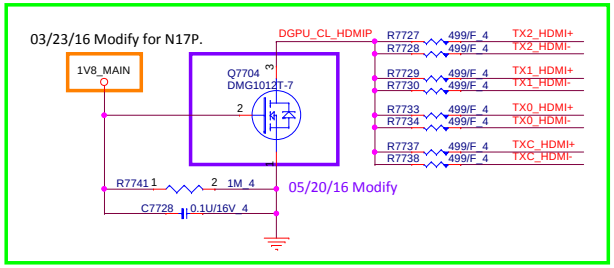
01/11 change to 0 ohm for NV suggest



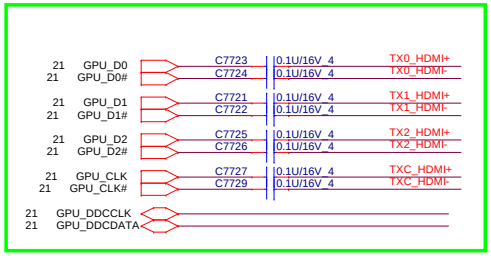
01/11 unstuff for HDMI output from GPU



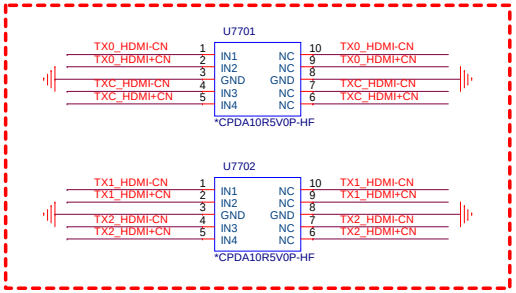
11/04 modify for HDMI2.0



11/03 modify for HDMI2.0



ESD

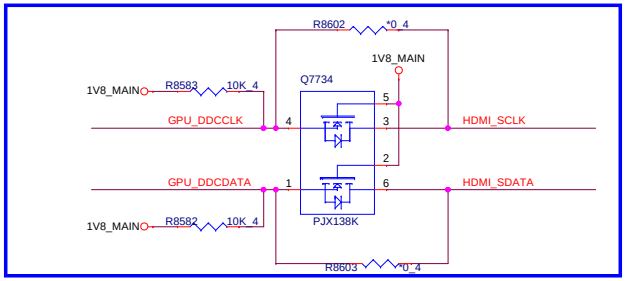


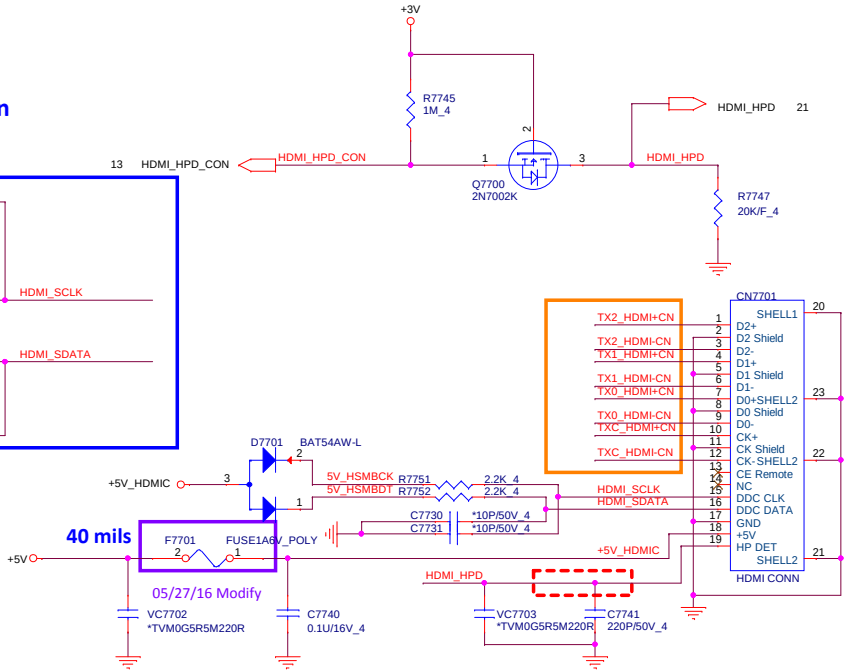
1125 Reserve ESD protection component

1125 SWAP

HDMI SMBus Isolation

Close to HDMI connector





0925 Del Net HDMI_DET_C

PROJECT : G35

Quanta Computer Inc.

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Custom	27 -- HDMI/HDMI REDRIVER	1A

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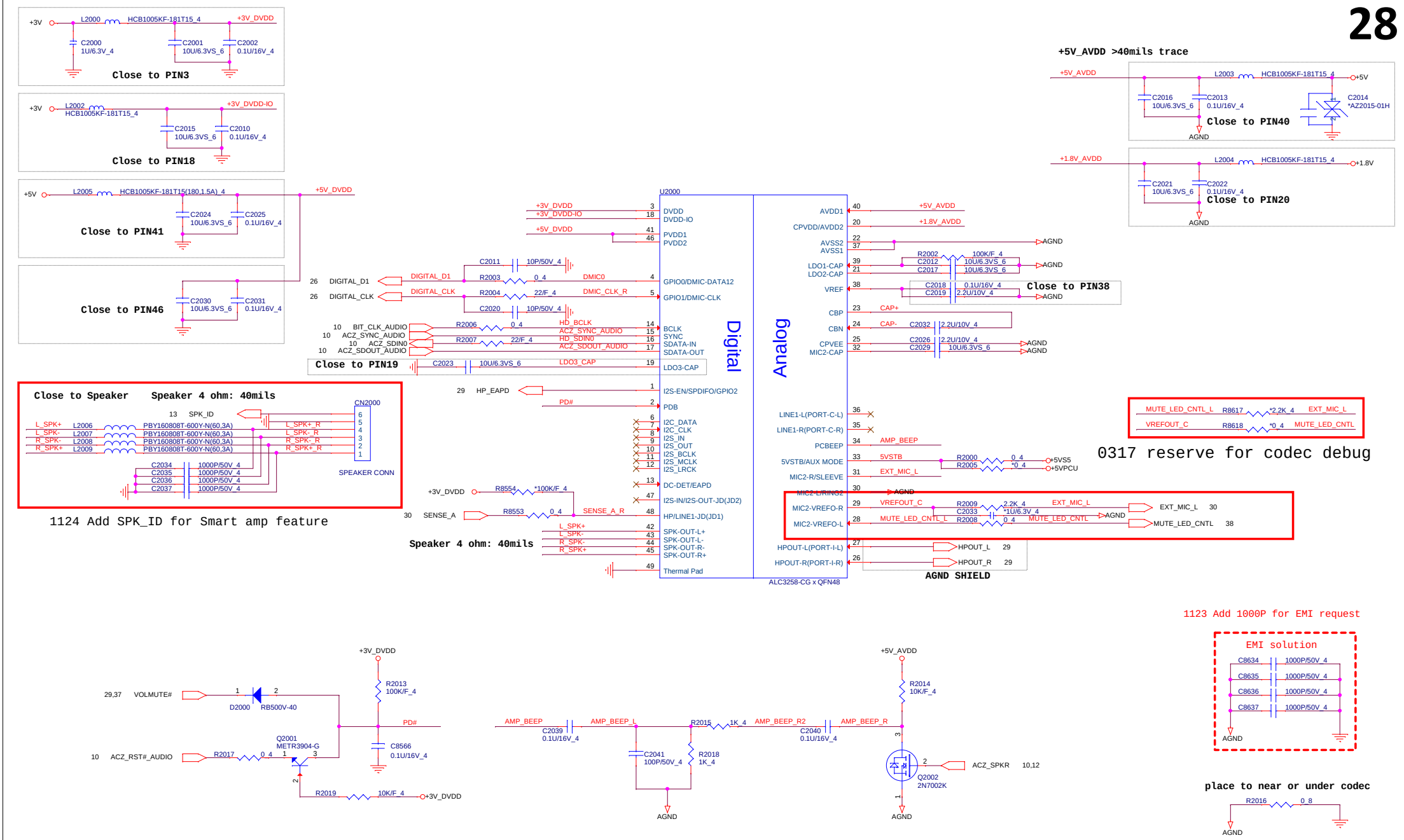

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 -- AUDIO CODEC ALC3258-CG	

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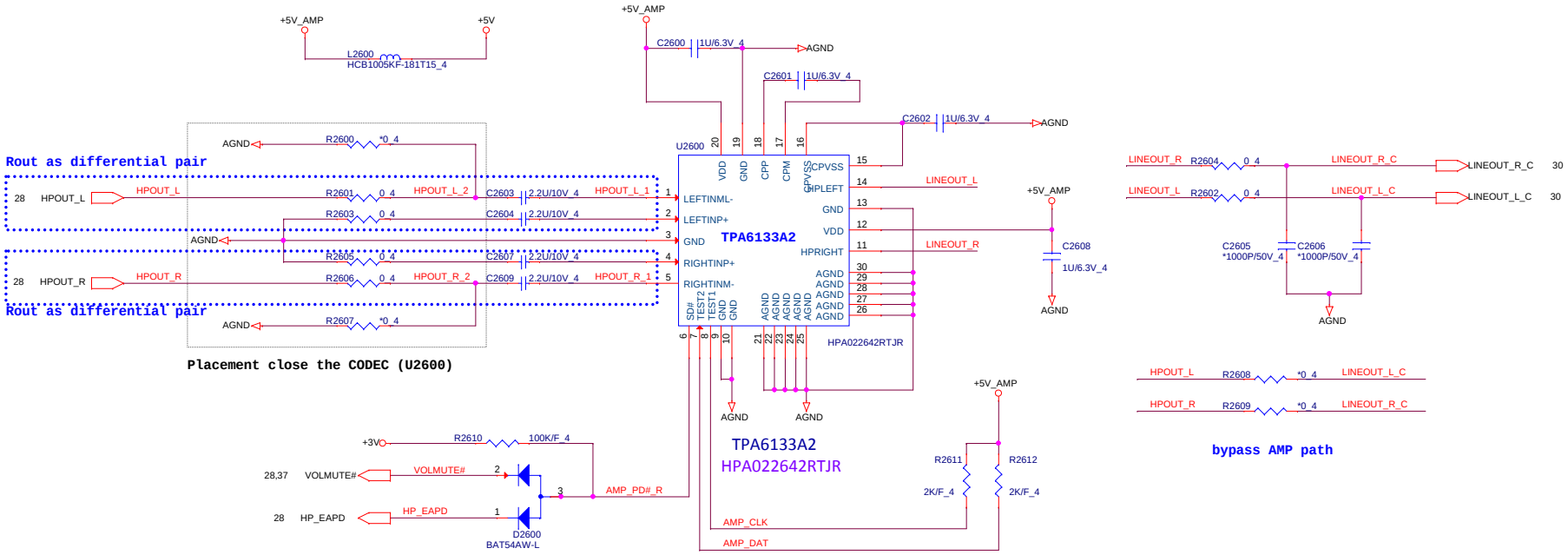
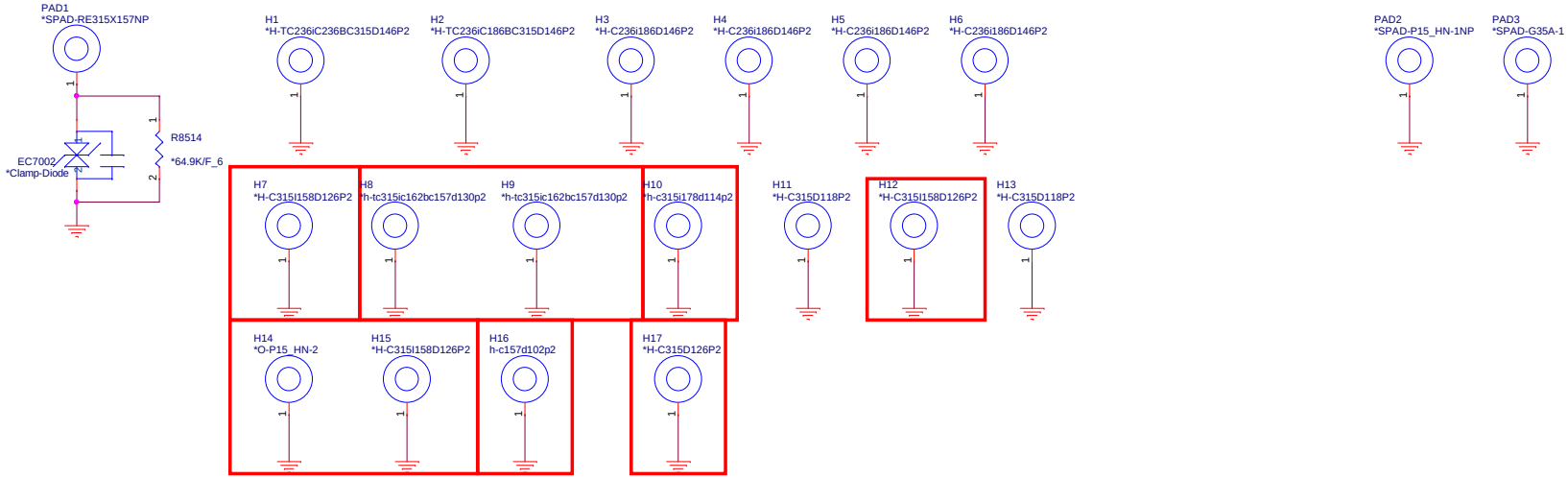
Head Phone out



HOLE



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	29-- HP AMP HPA022642RTJR	1A

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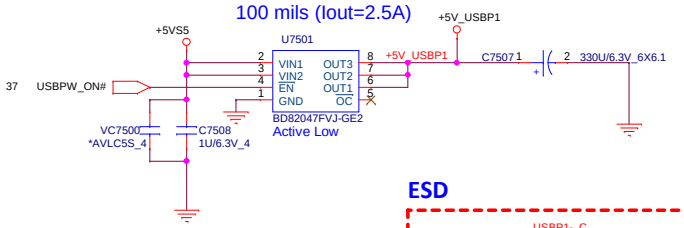
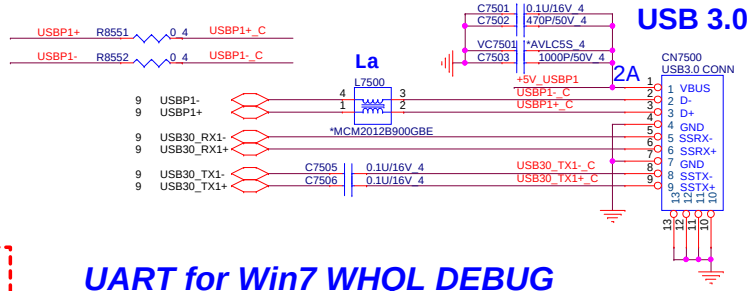
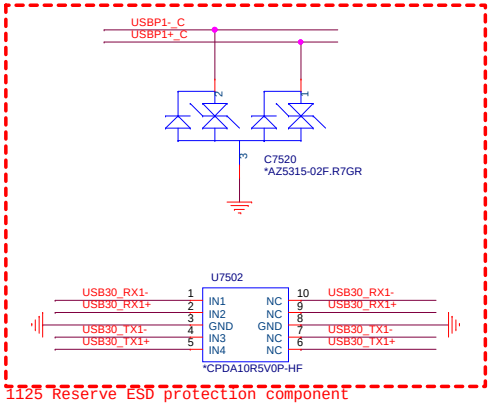
USB 2.0/3.0 Combo



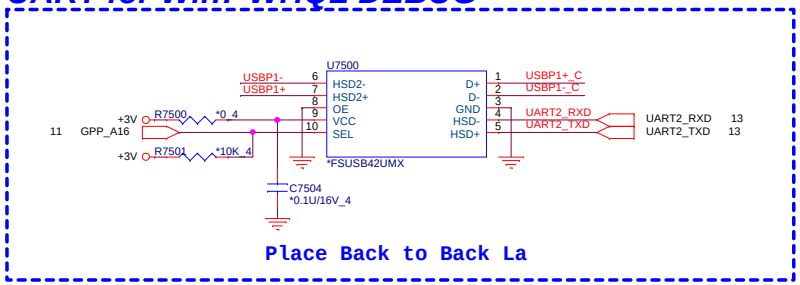


ESD



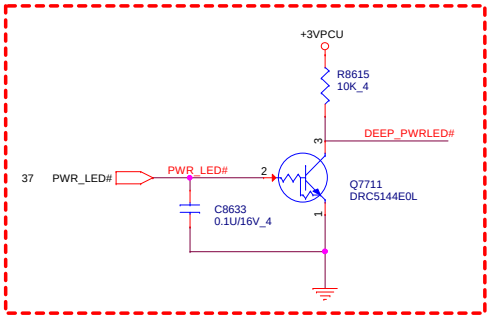
1125 Reserve ESD protection component

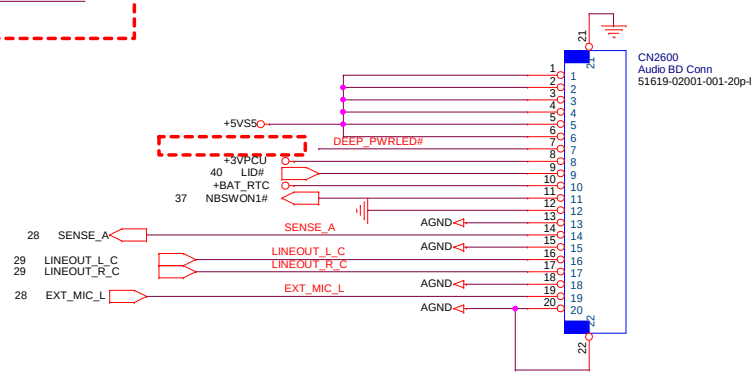
UART for Win7 WHQL DEBUG

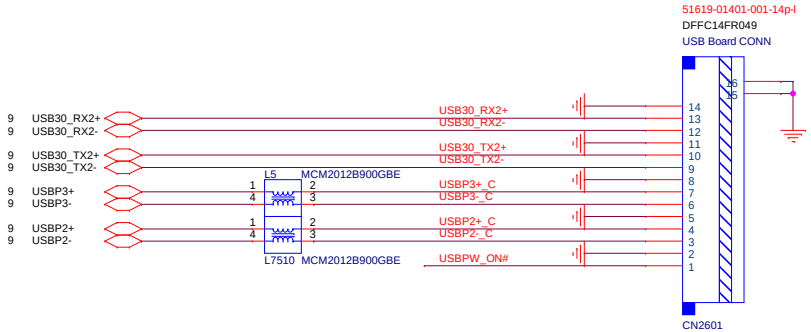


Daughter Board

1123 Add PWR LED MOS Circuit







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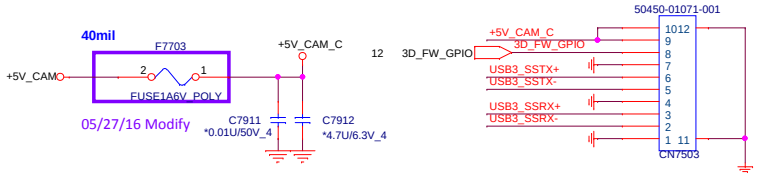
3D CAMERA

10/08 3D Camera MIC combine in LCD CONN

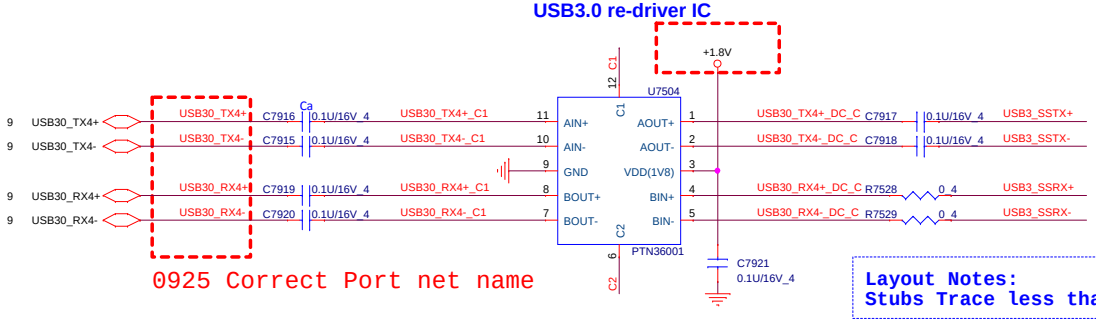
3D Camera Conn.



USB3.0

USB3.0 Re-driver IC

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V



0925 Correct Port net name

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V

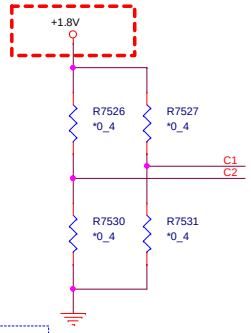


Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Layout Notes:
Stubs Trace less than 150mil

28,40,41,46,51 +5VPCU
5,10,21,30,33,37,38,40,41 +3VPCU
22,28,47,51 +1.8V

PROJECT : G35
Quanta Computer Inc.

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Custom	31 – 3D CAM/REDRIVER	1A

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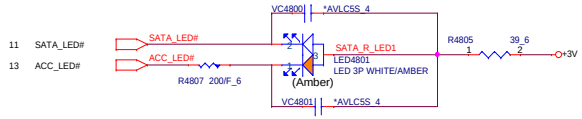
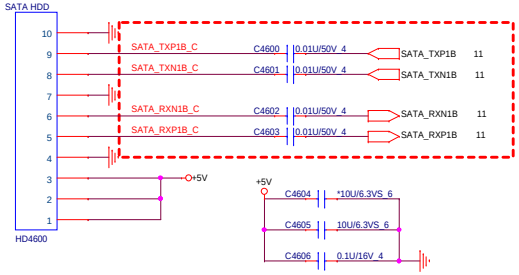
SATA LED



HDD



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PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
C	32 -- HDD/ODD	1A

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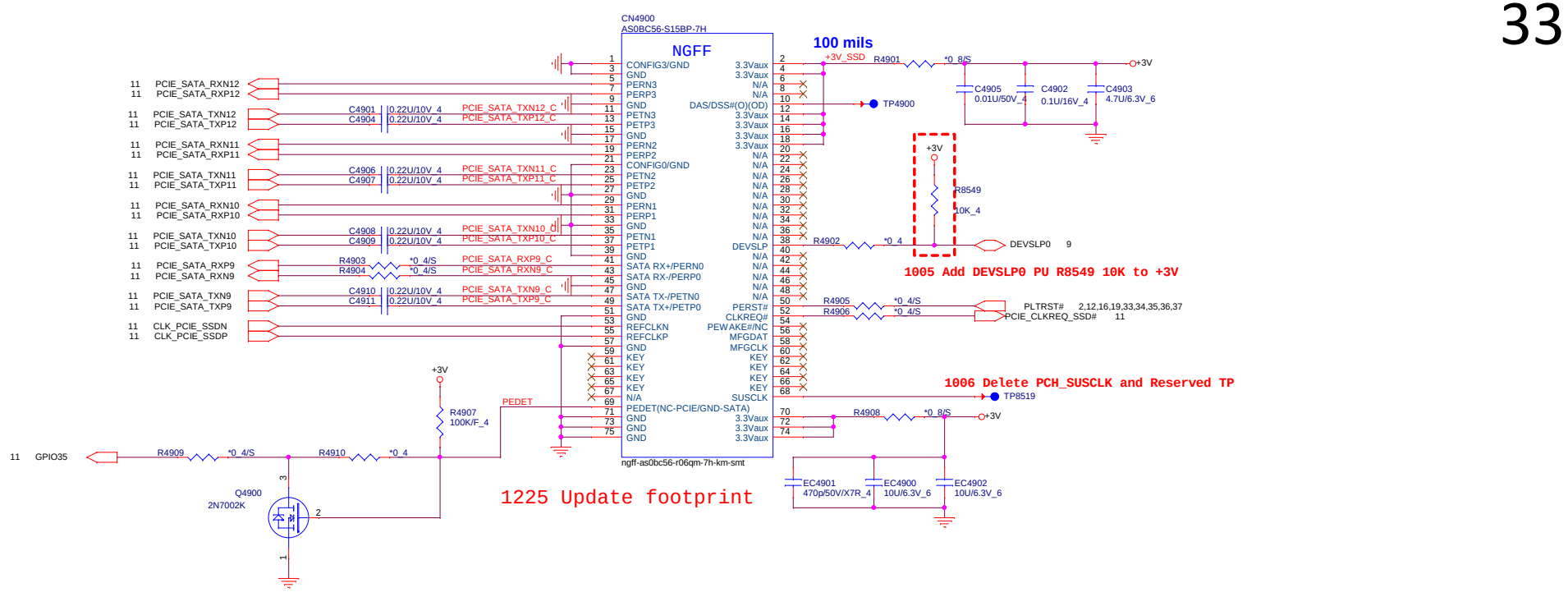
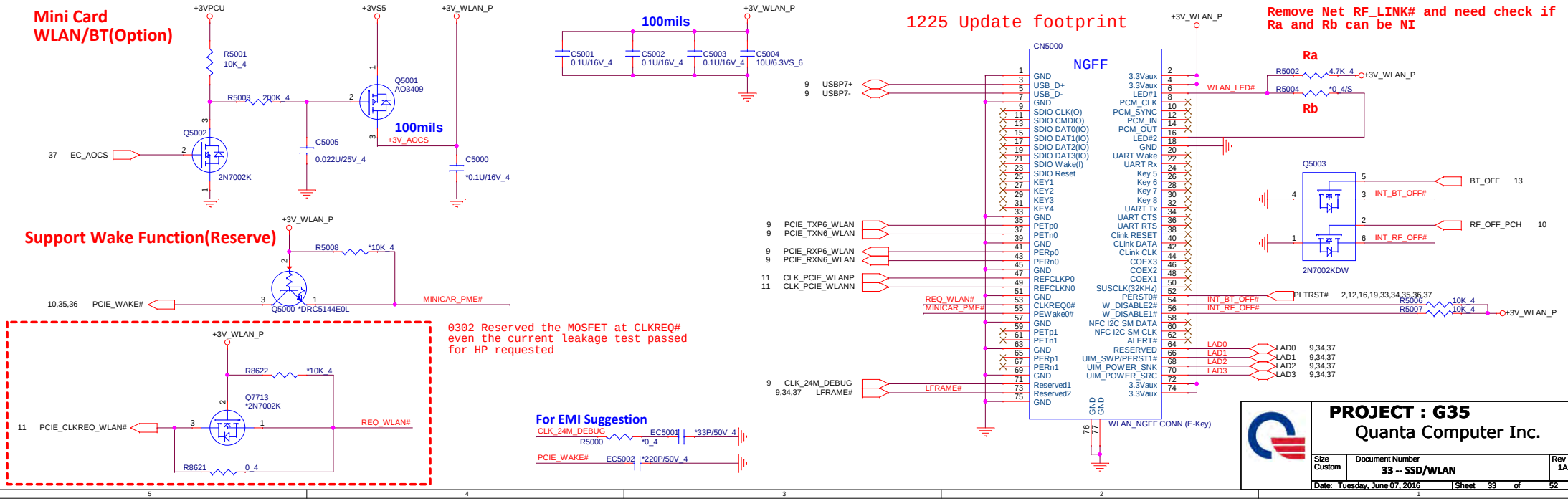
SSD





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Quanta Computer Inc.			
Size Custom	Document Number 33 -- SSD/WLAN		Rev 1A
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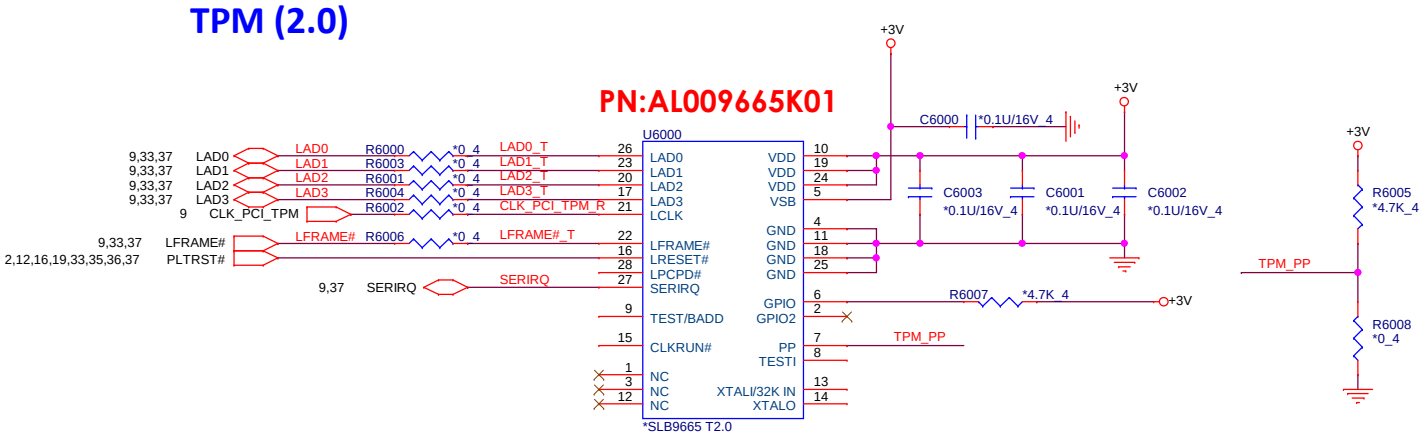
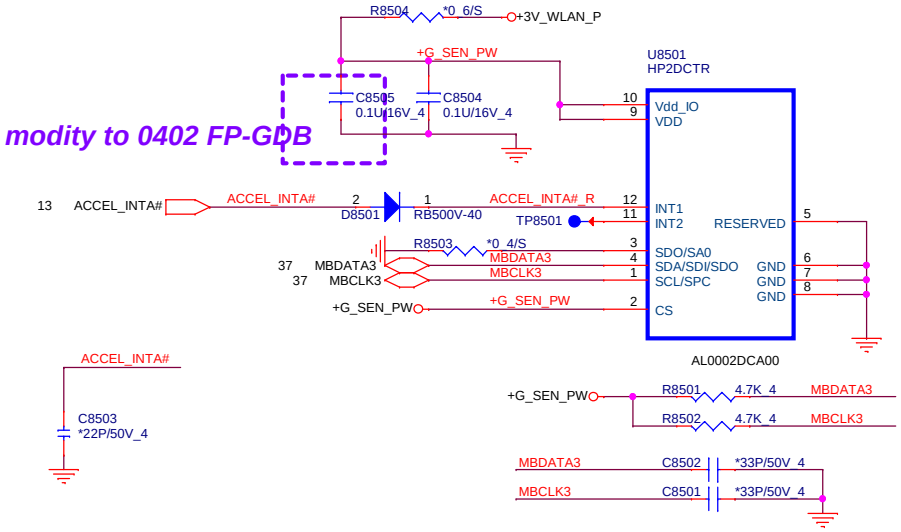
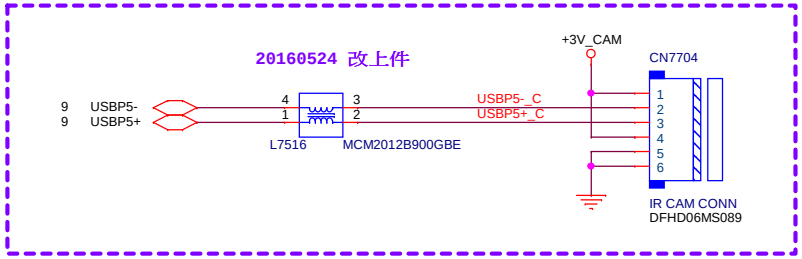
TPM (2.0)



Accelerometer Sensor



IR CAM



PROJECT : G35
Quanta Computer Inc.

B	34 - TPM/G-Sensor	Document Number	1A Rev
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Date:		Sheet	of

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LAN & RJ45

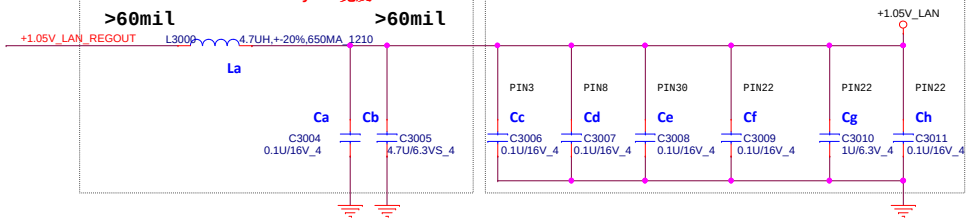
For SWR mode support RTL8111HSH/RTL8107ESH

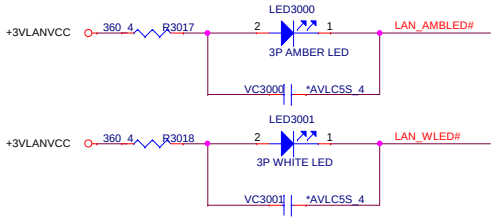
Stuff La, Ca ,Cb

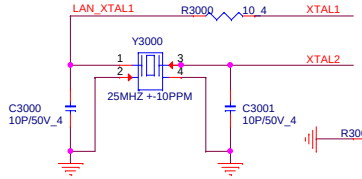
* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)

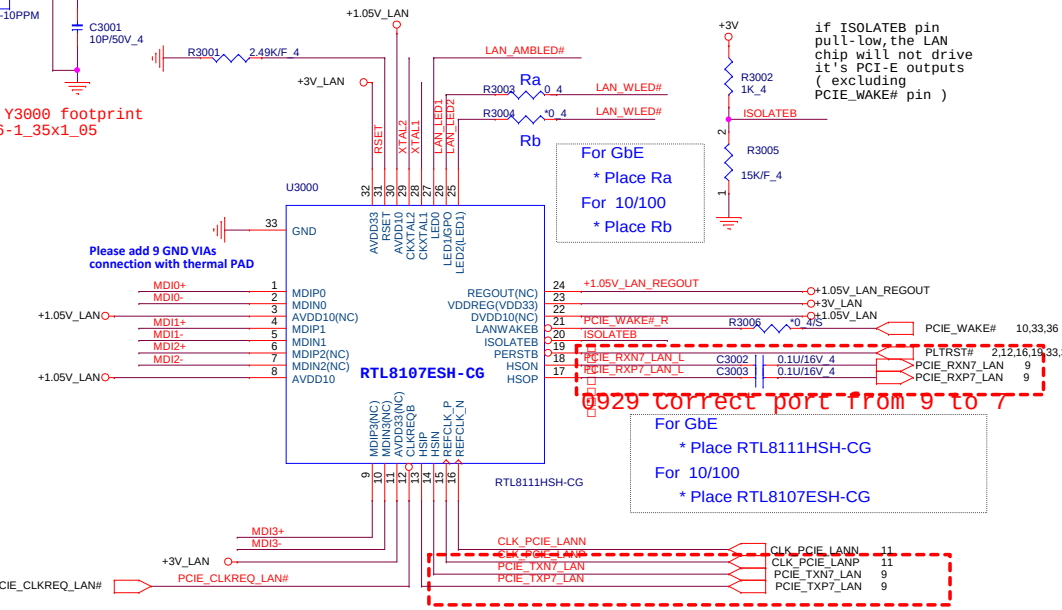
Power trace Layout 寬度> 60mil







1028 Change Y3000 footprint to xtl-2x1_6-1_35x1_05



if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

For GbE
* Place Ra
For 10/100
* Place Rb

For GbE
* Place RTL8111HSH-CG
For 10/100
* Place RTL8107ESH-CG

0929 correct port from 9 to 7

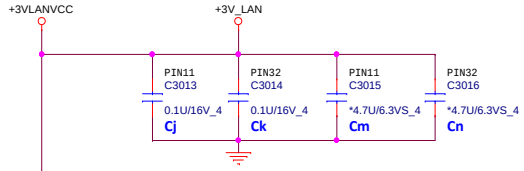
0929 Correct port from 9 to 7

For 10/100 stuff only

Close RJ45

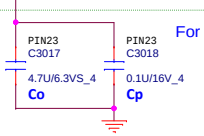
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

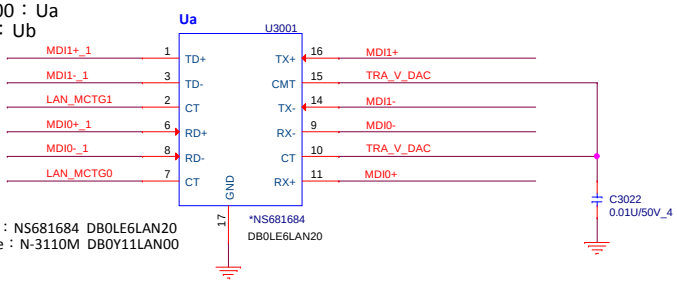


For SWR mode support RTL8111HSH/RTL8107ESH

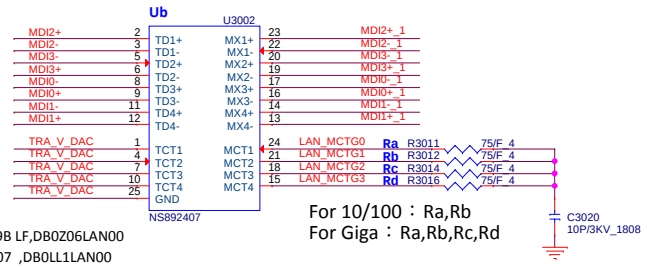
Stuff Co, Cp



For 10/100：Ua
For Giga：Ub



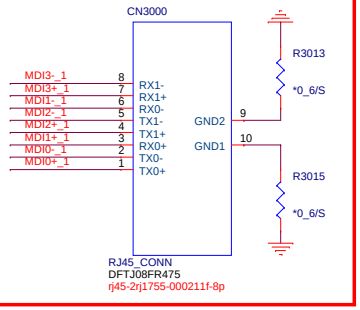
1st source：NS681684 DB0LE6LAN20
2nd source：N-3110M DB0Y11LAN00



For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd

RJ45



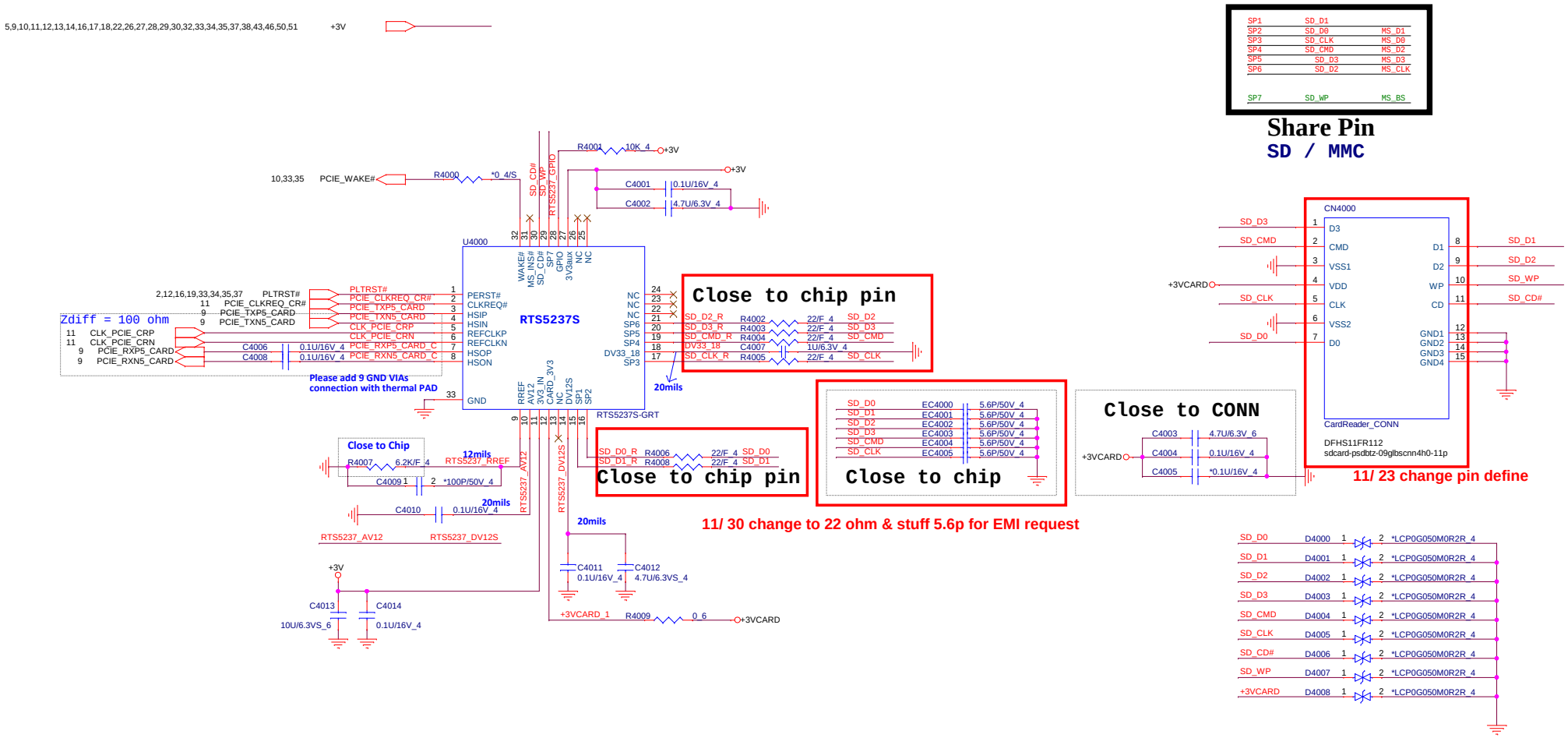
0104 Update footprint

5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,36,37,38,43,46,50,51

46 +3V +3VLANVCC

PROJECT : G35		
Quanta Computer Inc.		
Size Custom	Document Number 35 – LAN RTL8107ESH-CG/RJ45	Rev 1A
Date: Tuesday, June 07, 2016	Sheet 35 of 52	

RTS5237S PCIE CARD READER Controller



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 – CR RTS5237S/CR SOCKET	1A

Date: Tuesday, June 07, 2016 Sheet 36 of 52

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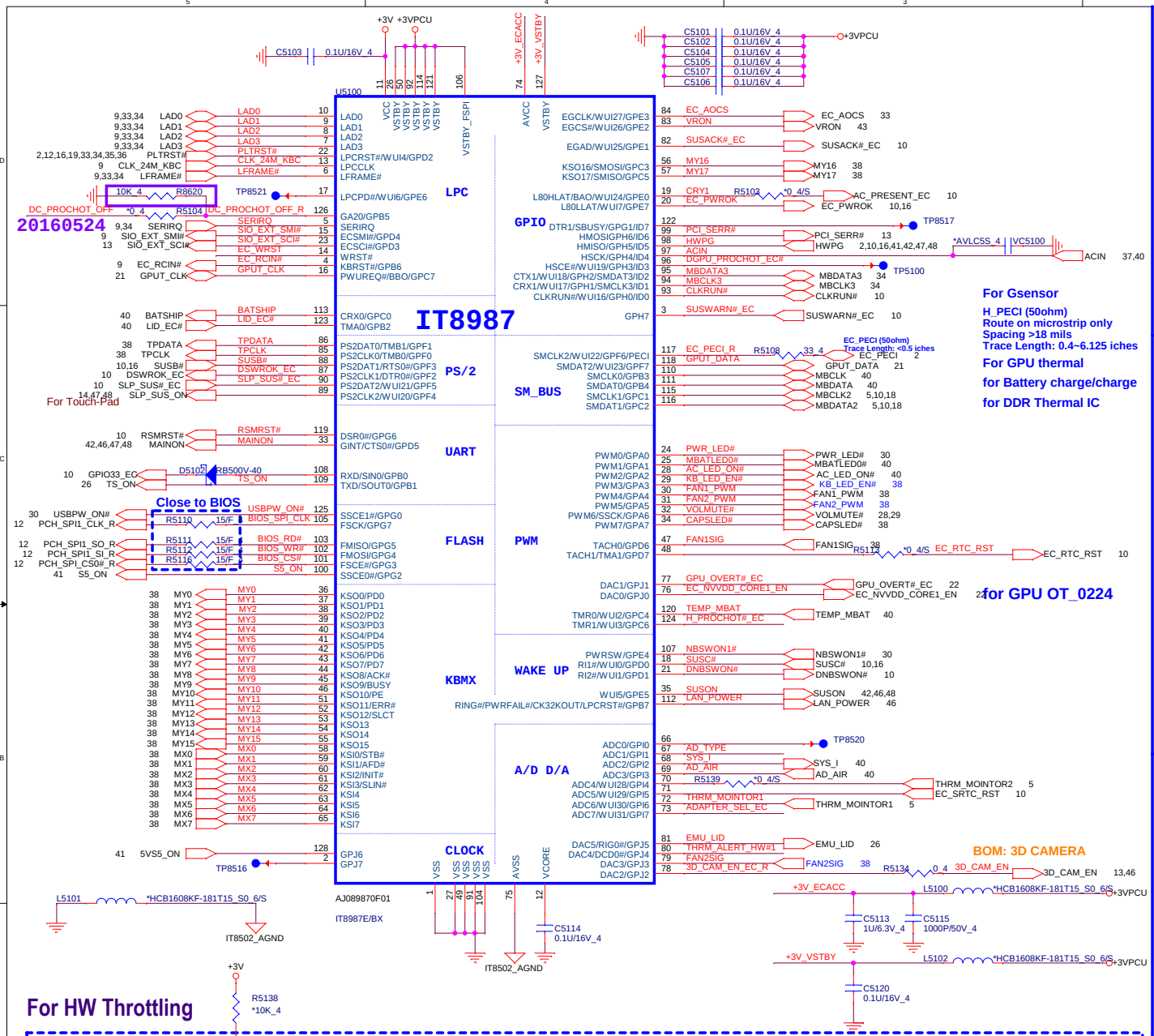
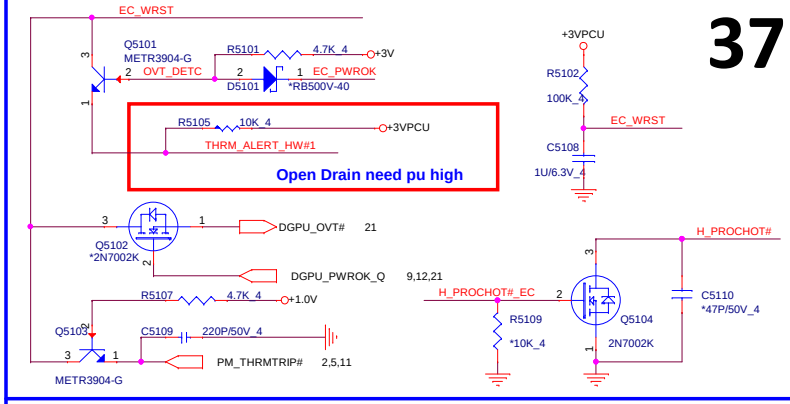
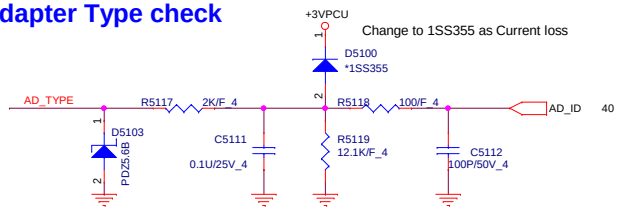


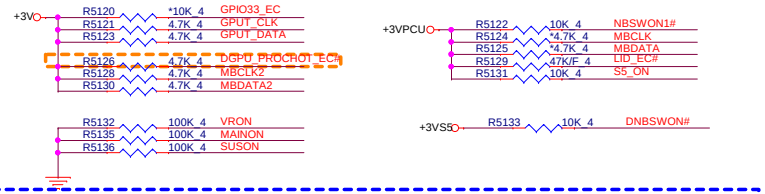


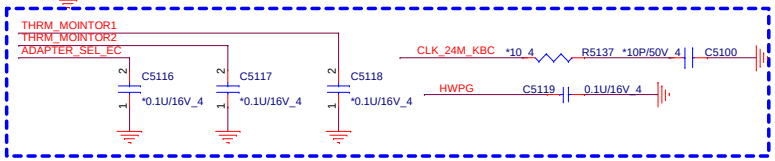
Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	DIS
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	UMA
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check







CLOSE to EC Pin

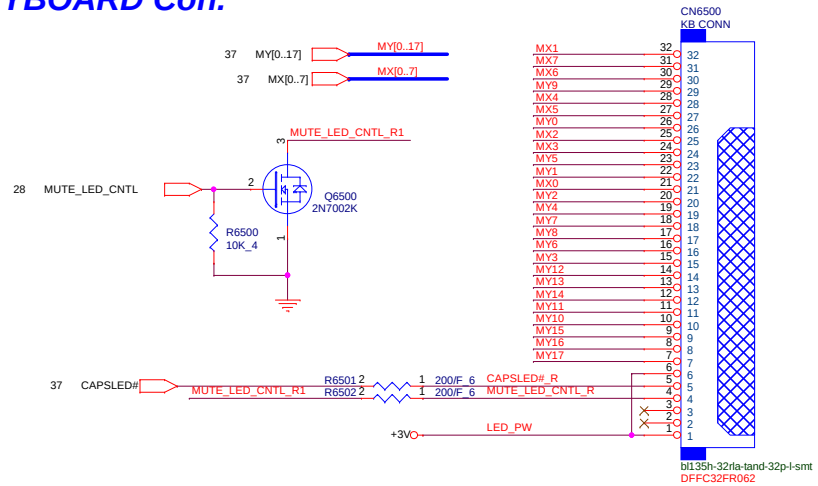
5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,38,43,46,50,51 +3V
10,12,14,16,33,41,42,46,47,48 +3VS5
5,10,21,30,33,38,40,41 +3VPCU

PROJECT : G35
Quanta Computer Inc.

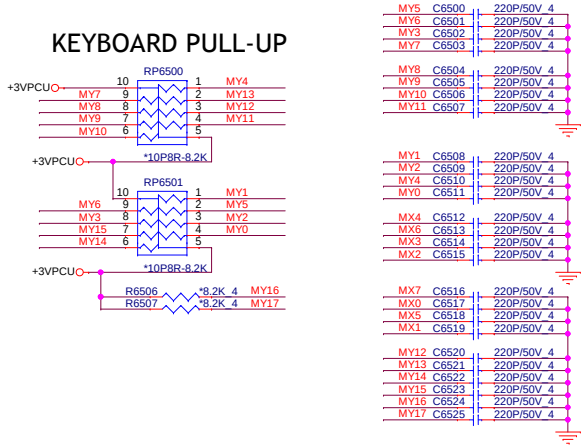
Size	Document Number	Rev
Custom	37 -- EC (IT8987)	1A

Date: Tuesday, June 07, 2016 Sheet 37of 52

KEYBOARD Con.

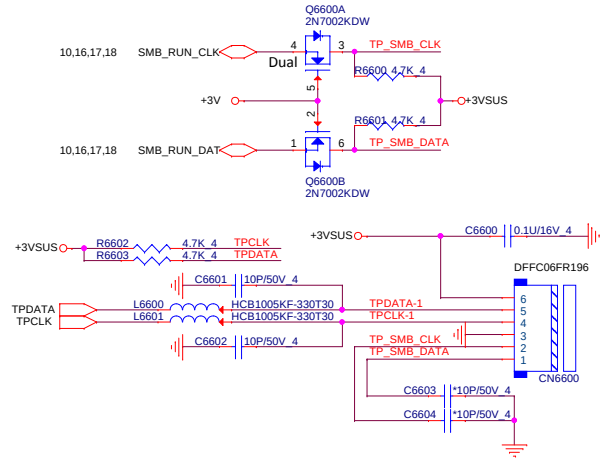


KEYBOARD PULL-UP

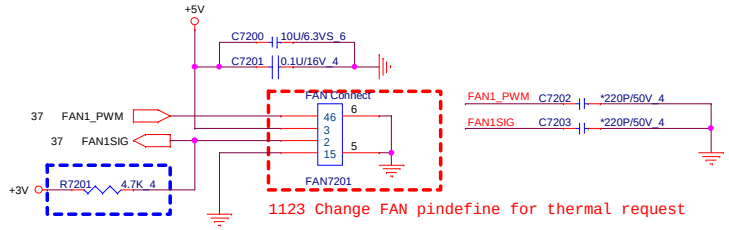


Touch Pad Connector

38

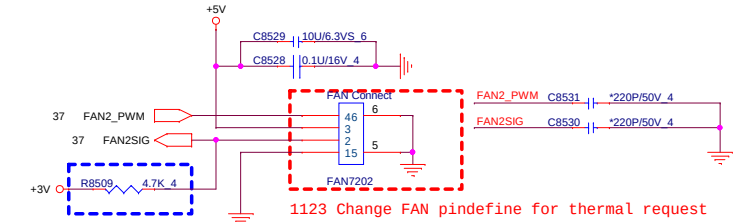


FAN



1123 Change FAN pindefine for thermal request

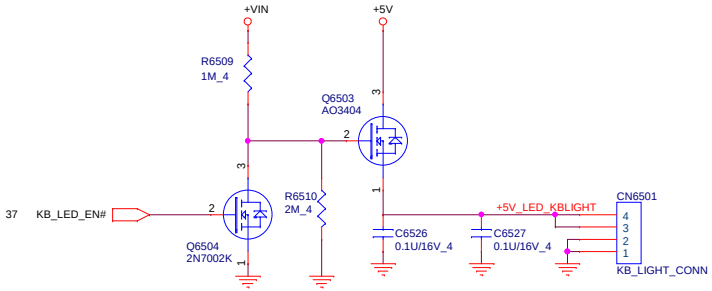
Close to EC Side



1123 Change FAN pindefine for thermal request

Close to EC Side

KB LIGHT CONN



PROJECT : G35 Quanta Computer Inc.		
Size Custom	Document Number 38 -- KB/TP/FAN/HOLE	Rev 1A
Date: Tuesday, June 07, 2016	Sheet 38 of 52	

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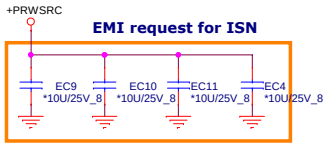
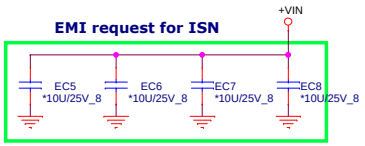
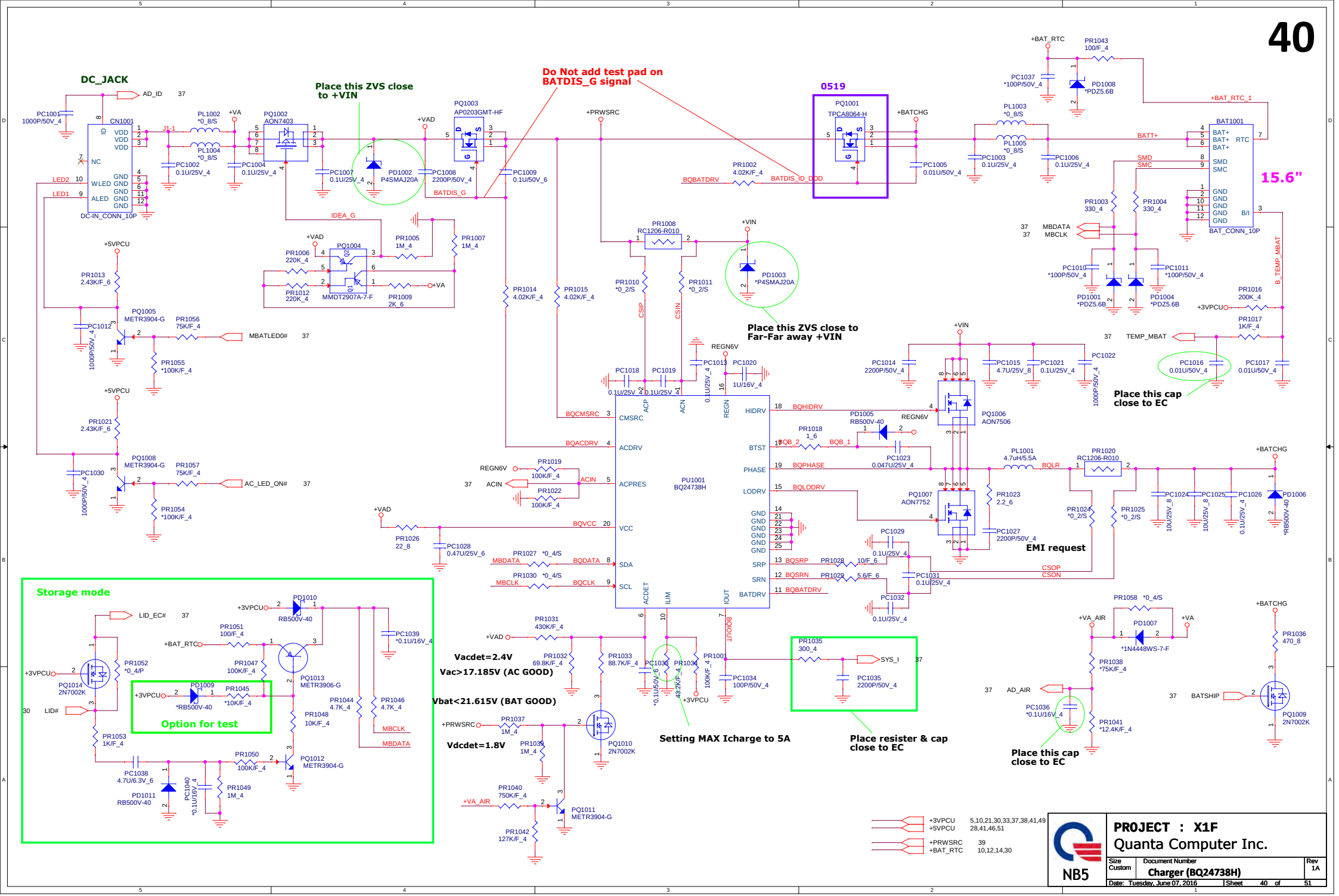




NB5	**PROJECT : X1F** Quanta Computer Inc.	
Size Custom	Document Number **RF Solution**	Rev 1A
Date: Tuesday, June 07, 2016	Sheet 39of 52	



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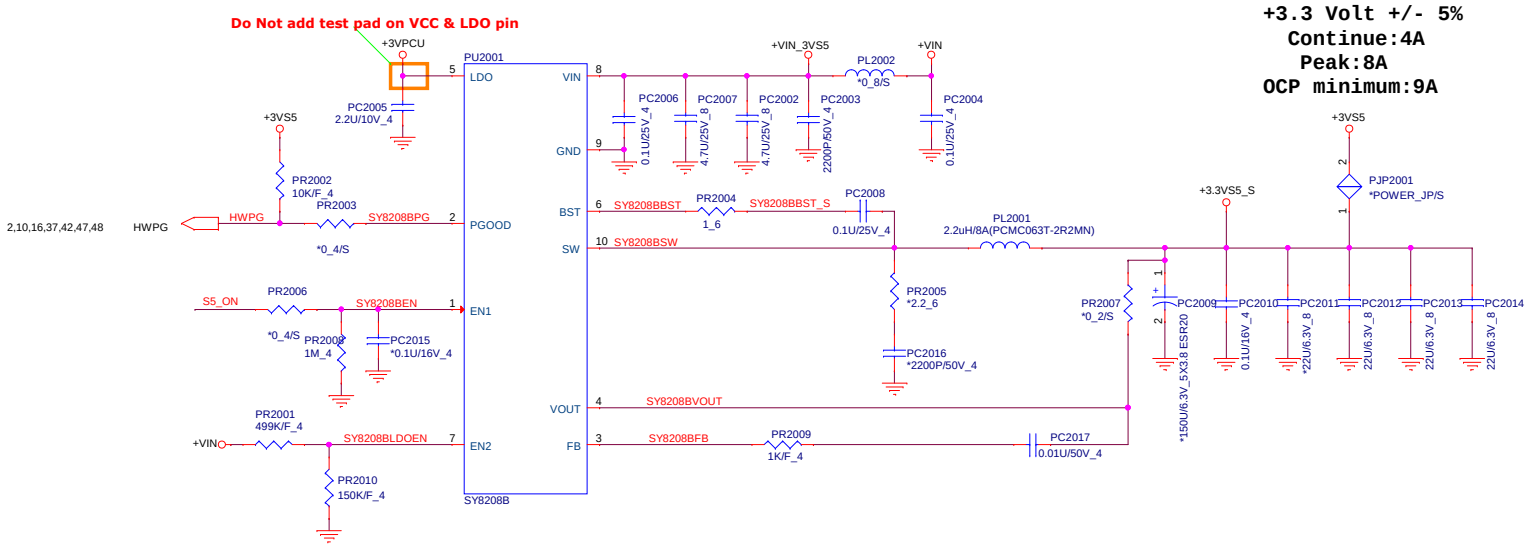

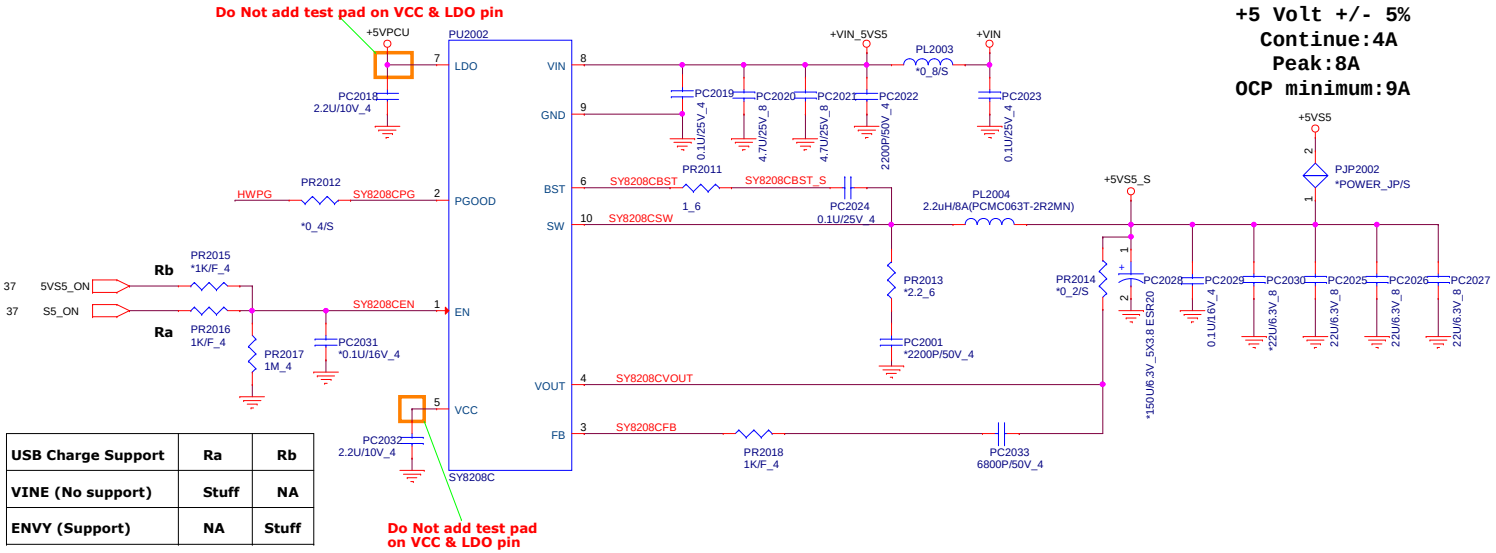

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

+VIN	26,38,39,40,42,43,44,45,46,47,48,49,53,54
+3VS5	10,12,14,16,33,37,42,46,47,48
+5VS5	10,28,30,42,43,44,45,46,47,48,49,51,53,54
+3VPCU	5,10,21,30,33,37,38,40,49
+5VPCU	28,40,46,51

NB5

PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A

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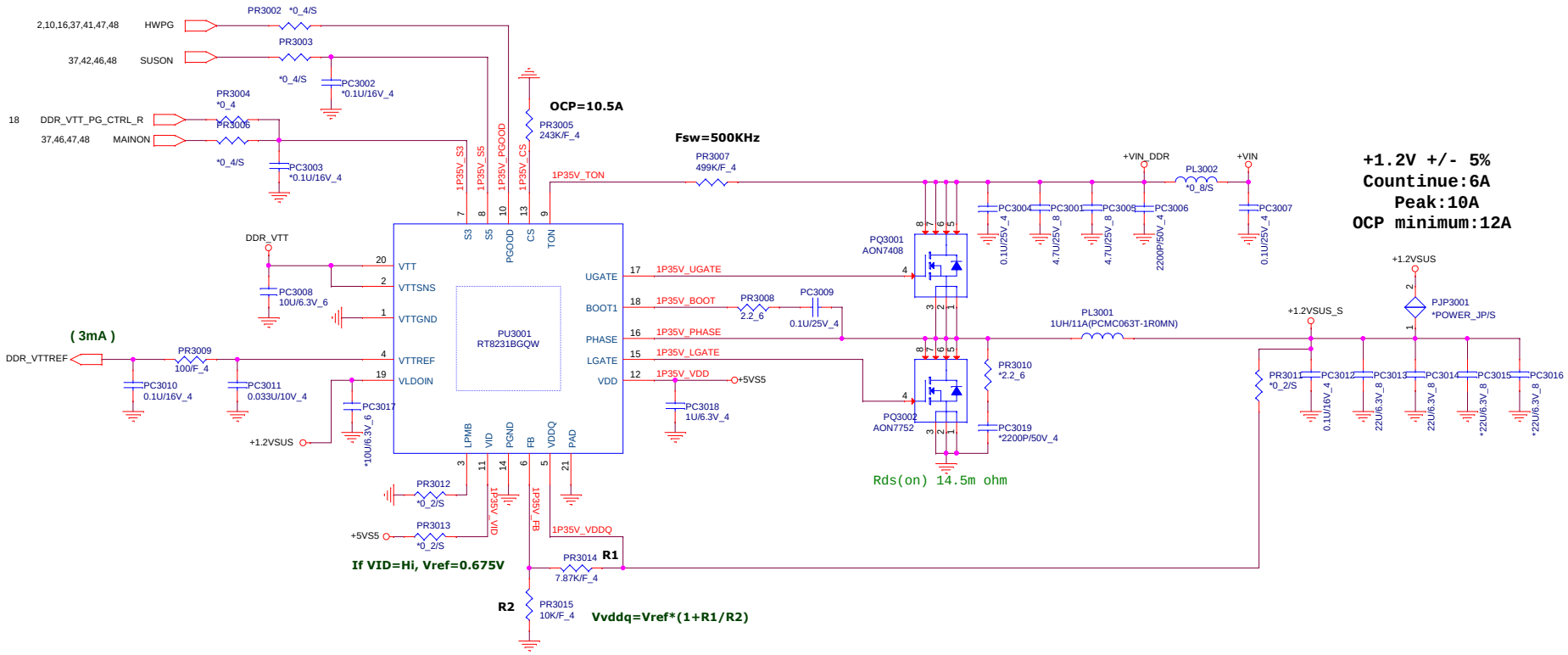
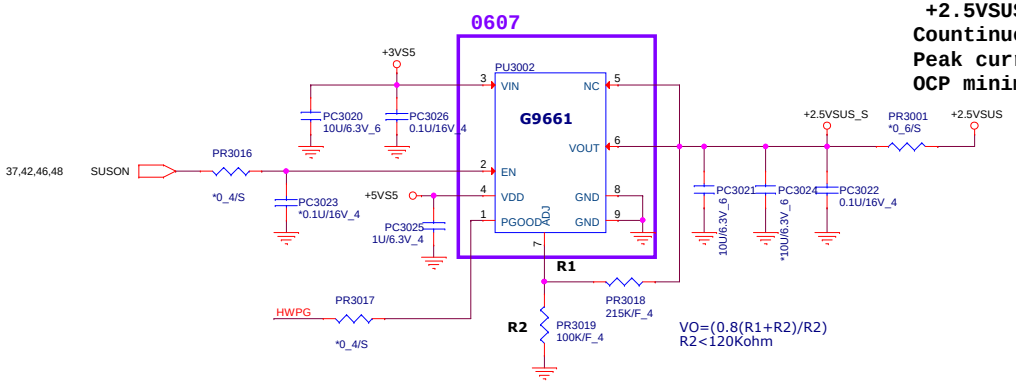


+1.2V +/- 5%
Countinue:6A
Peak:10A
OCP minimum:12A



+2.5VSUS +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum:3A

+VIN	26,38,39,40,41,43,44,45,46,47,48,49,53,54
+5VS5	10,28,30,41,43,44,45,46,47,48,49,51,53,54
+1.2VSUS	2,6,10,17,18,48,51
DDR_VTT	17,18
+2.5VSUS	17,18

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 (RT8231B)	1A

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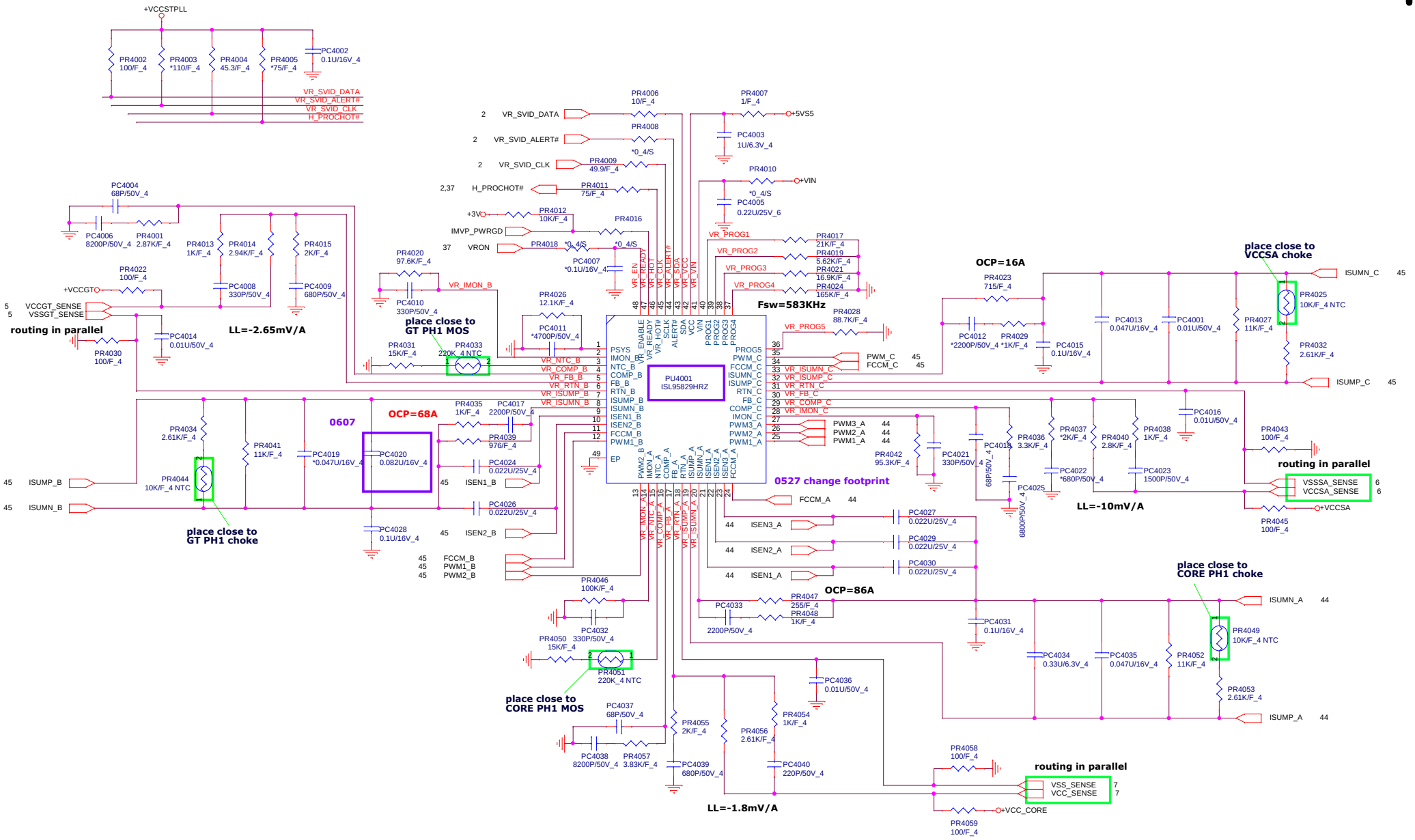
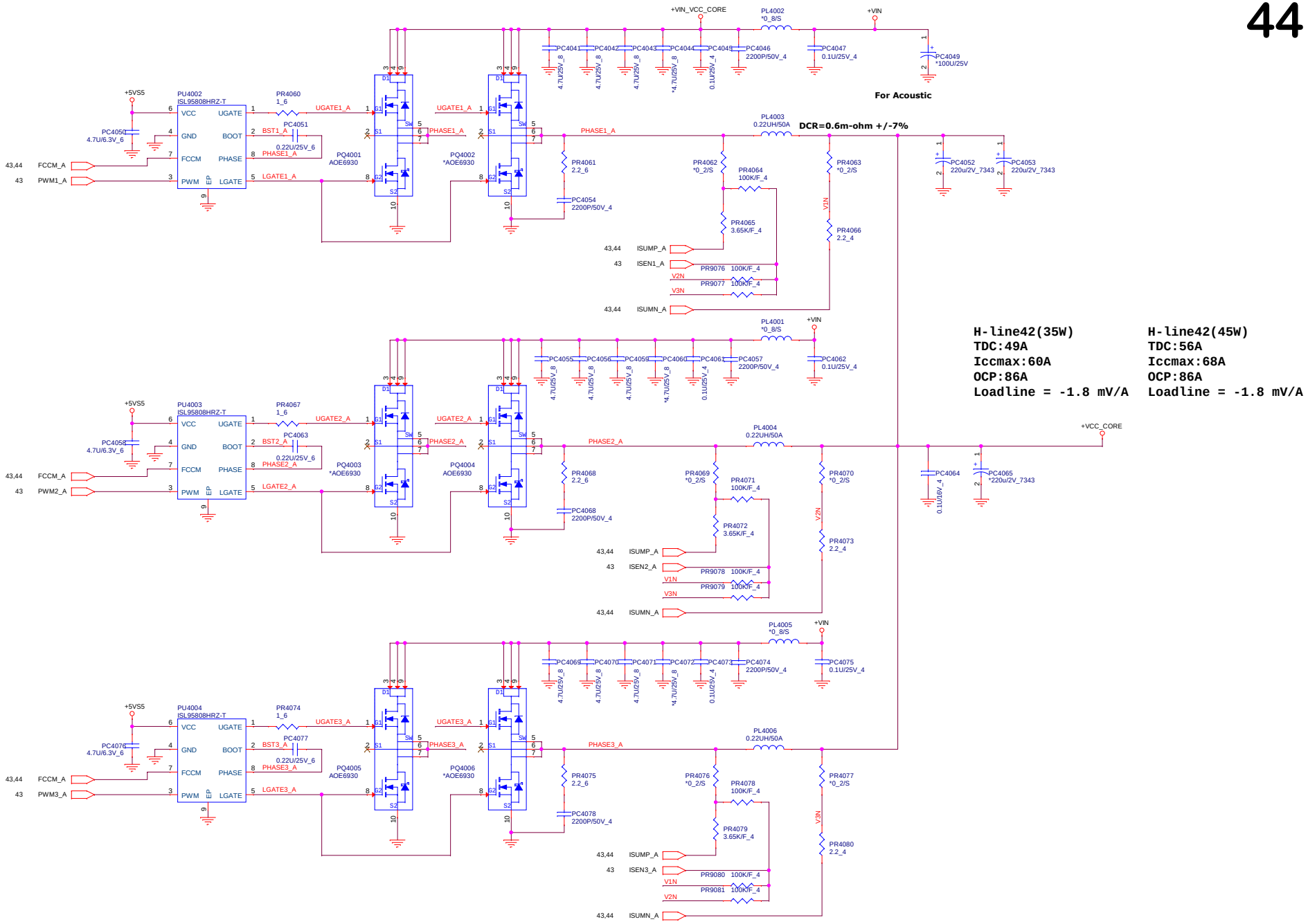


NB5	PROJECT : X1F Quanta Computer Inc.		
Size Custom	Document Number CPU VR IC (ISL95829HRZ)		Rev 1A
Date: Tuesday, June 07, 2016	Sheet 43 of 51		



H-line42(35W)	H-line42(45W)
TDC:49A	TDC:56A
Iccmax:60A	Iccmax:68A
OCP:86A	OCP:86A
Loadline = -1.8 mV/A	Loadline = -1.8 mV/A

NB5

PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCC_CORE (ISL95808HRZ-T)	1A

Date: Tuesday, June 07, 2016 | Sheet 44 of 51

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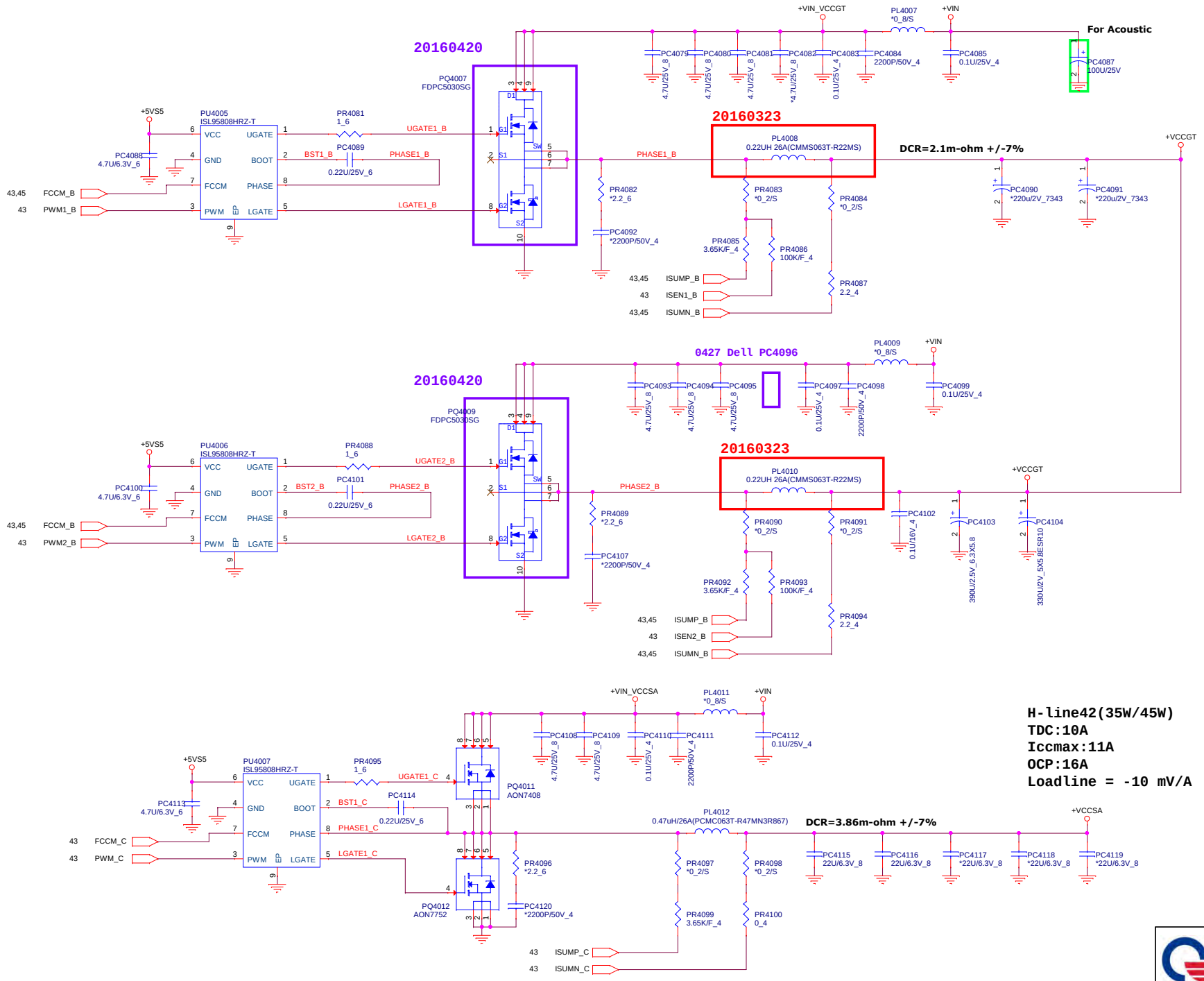


H-line42(35W)
TDC:41A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

H-line42(45W)
TDC:39A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

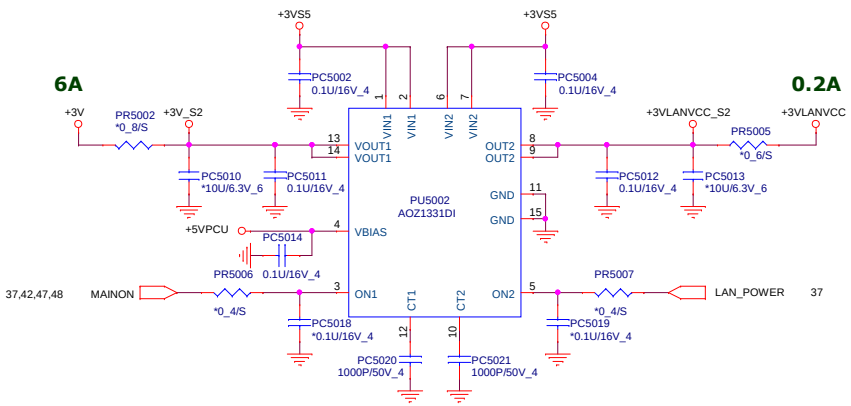
H-line42(35W/45W)
TDC:10A
Iccmax:11A
OCP:16A
Loadline = -10 mV/A

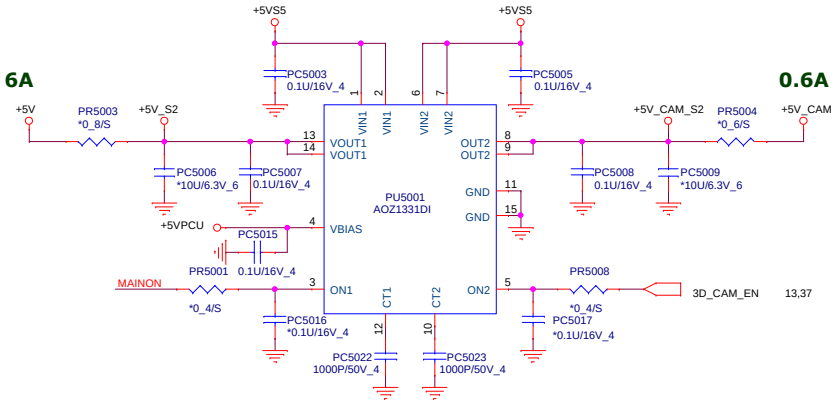
NB5

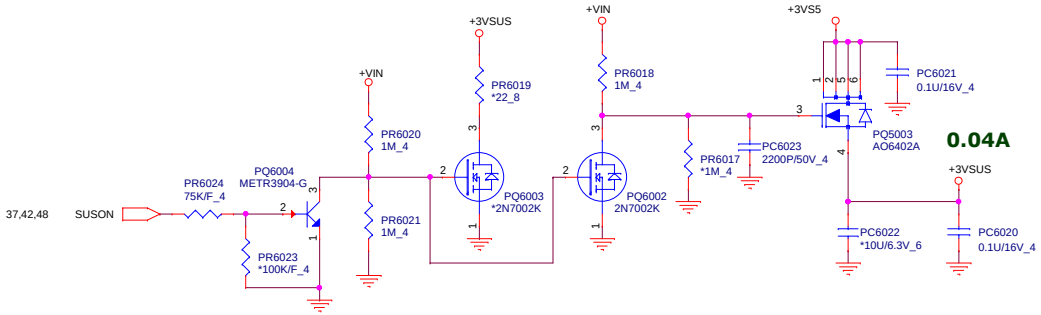
PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCGT/SA (ISL95808HRZ-T)	1A

Date: Tuesday, June 07, 2016 Sheet 45 of 51







+3V	5,9,10,11,12,13,14,16,17,18,26,27,28,29,30,32,33,34,35,36,37,38,43,54
+5V	26,27,28,29,31,32,38,49
+3VS5	10,12,14,16,33,37,41,42,47,48
+5VS5	10,28,30,41,42,43,44,45,47,48,49,51,53,54
+3VSUS	38
+3VLANVCC	35
+5V_CAM	31
+3V_DEEP_SUS	9,10,12,13,14,16,18

NB5

PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Load switch IC (AOZ1331D)**	1A

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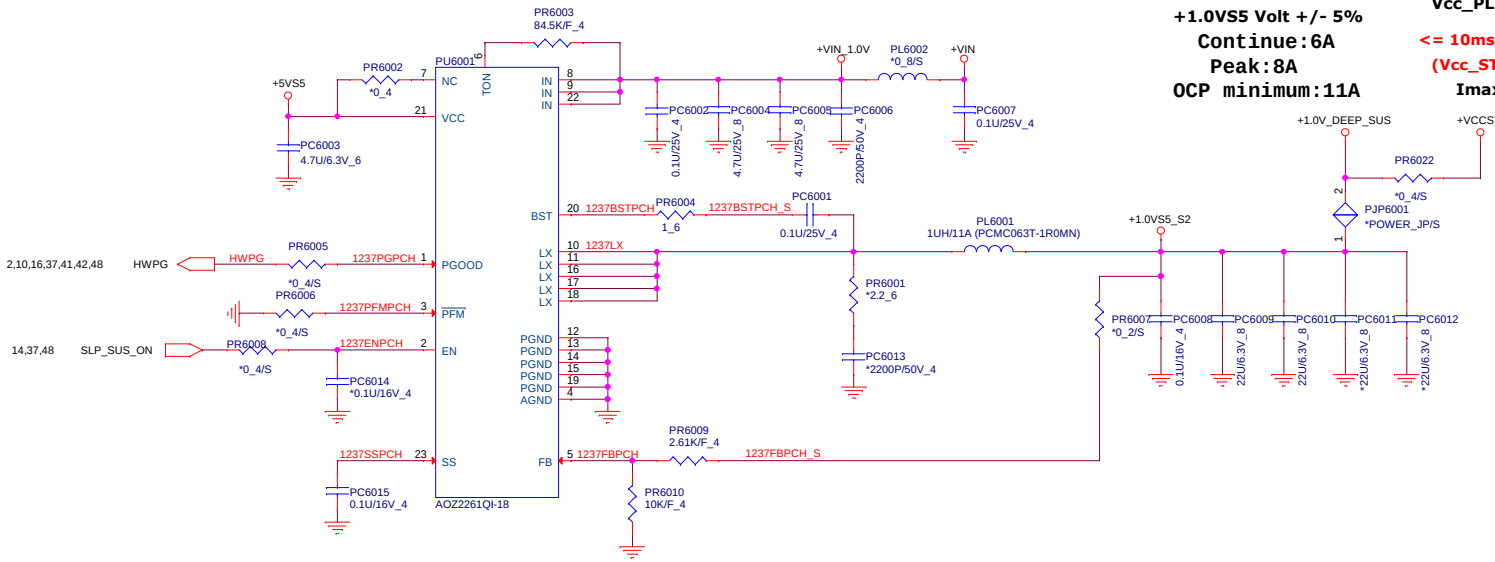
(V1.00A+V1.00_MODPHY+VccPRIM_CORE)

+1.0VS5 Volt +/- 5%
Continue:6A
Peak:8A
OCP minimum:11A

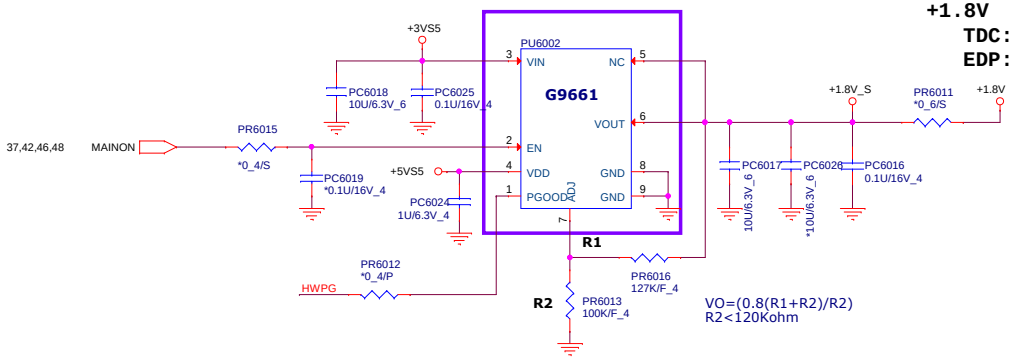
Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)
Imax:0.24A



0607

+1.8V +/- 5%
TDC:1A
EDP:2A



+VIN	26,38,39,40,41,42,43,44,45,46,48,49,53,54
+3VS5	10,12,14,16,33,37,41,42,46,48
+5VS5	10,28,30,41,42,43,44,45,46,48,49,51,53,54
+1.0V_DEEP_SUS	10,11,14,16,48
+1.8V	22,28,31,51
+VCCSTPLL	2,6,43

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0_DEEP_SUS	1A

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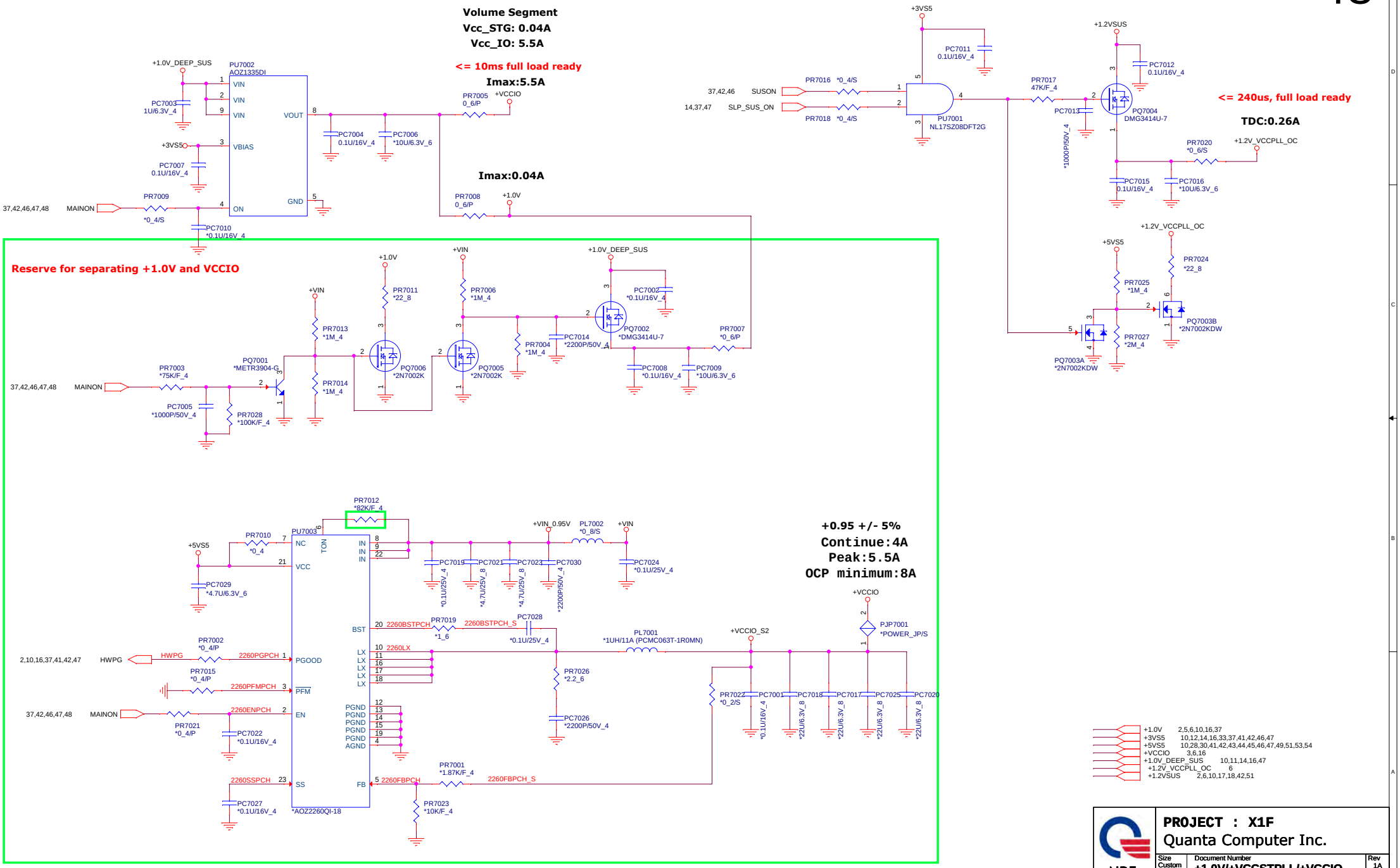

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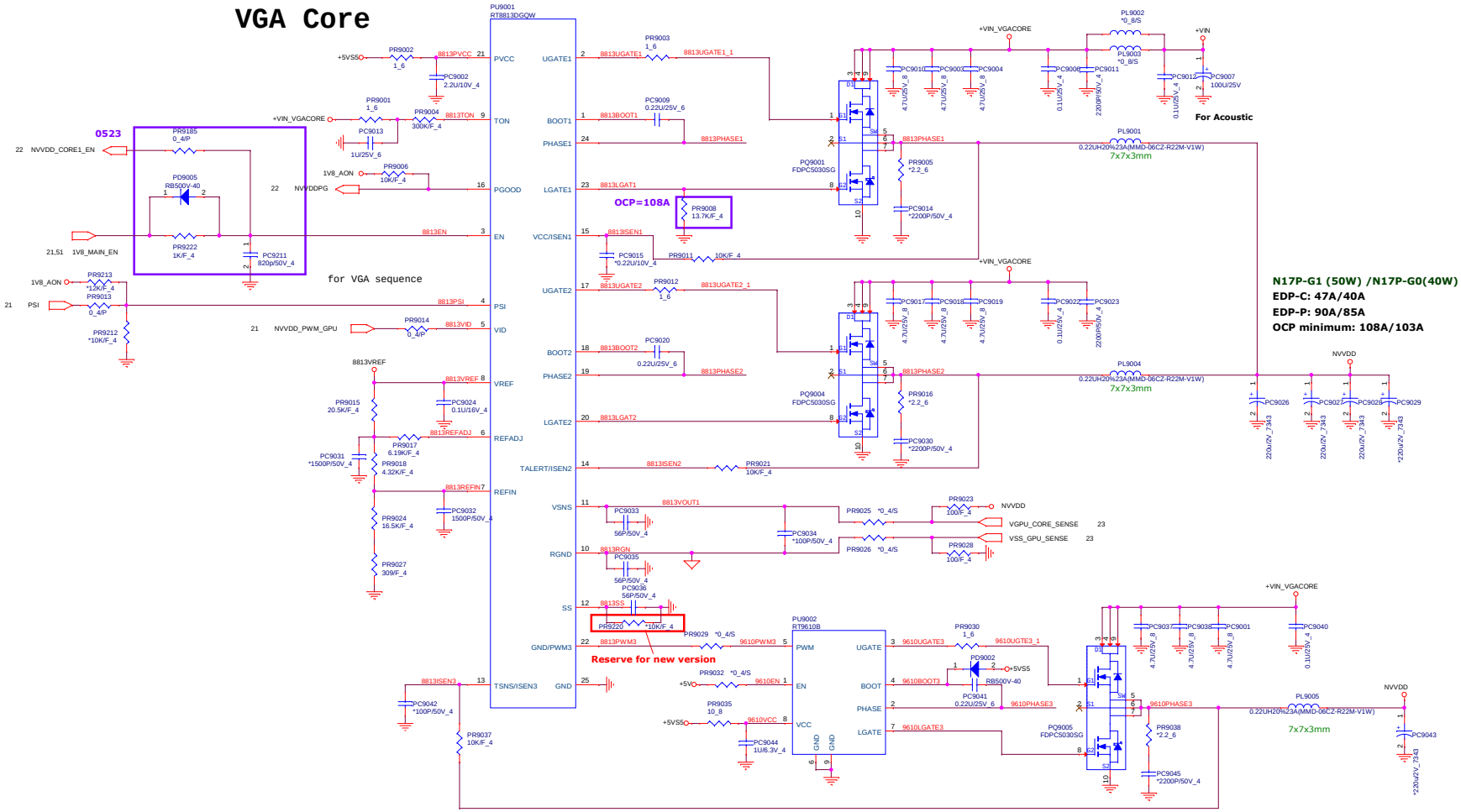
VGA Core



NVDDS

1. Ripple Current:
   Irip=7.79A
2. Ripple Voltage:
   ESR/1=9mohm
   Vrip=70.11mV
3. MOSFET Spec:
   L-side MOSFET: FDPC5030
   Rds(ON)=3mohm (Vgs=4.5 V)
   I cont = 25A (T =25 ℃)
   I pulse=503A
4. Frequency:
   F=500KHz (PR9224=300k ohm)
5. OCP:
   Set = PR9008 to 13.7K
   Vtrip= PR9008*10uA-40mV=97V
   Iocp=(Vtrip/Rdson) + Iripple/2
   = 36.23A (1 phase)

Total OCP=36.23*3=108.6A (3 phase)

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A

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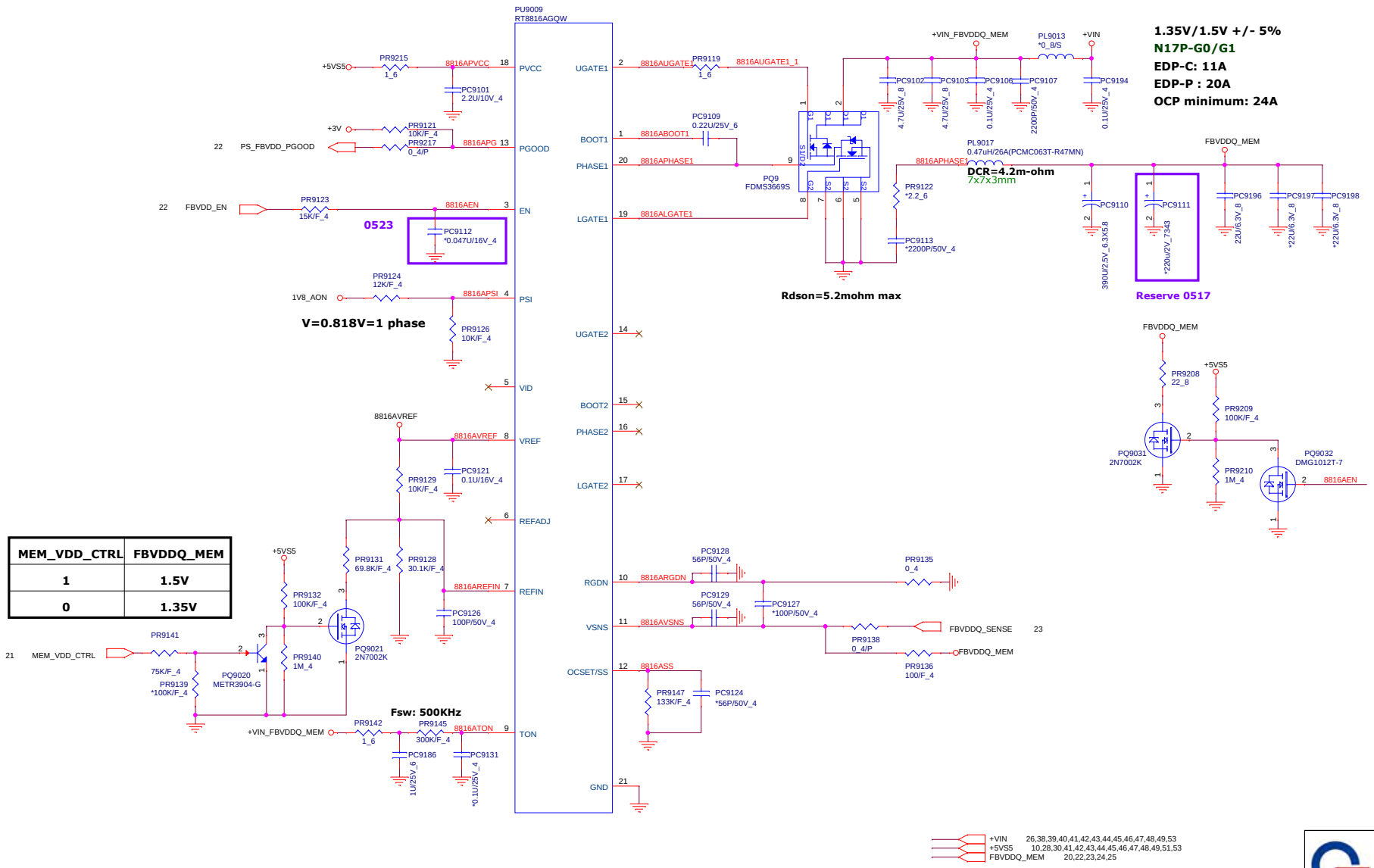

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.5V
0	1.35V

1.35V/1.5V +/- 5%
N17P-G0/G1
EDP-C: 11A
EDP-P : 20A
OCP minimum: 24A

FBVDDQ

1. Ripple Current:
Irip=5.34A Vo=1.35V
Irip=5.88A Vo=1.5V

2. Ripple Voltage:
ESR/1=9mohm
Vrip=48.06mV Vo=1.35
Vrip=53mV Vo=1.5

3.MOSFET Spec:
L-side MOSFET: FDMS3669S
Rds(ON)=5.2mohm (Vgs=4.5 V)
I cont = 18A (T =25 ℃)
I pulse=60A

4. Frequency:
F=500KHz (PR9145=300k ohm)

5. OCP:
Set = PR9147 to 133K Vo=1.35
Vtrip= PR9147*10uA/12=110.83mV
Iocp=(Vtrip/Rdson) + Iripple/2 = 24A

NB5

PROJECT : G38A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_GFX (AOZ2263QI-18)	1A

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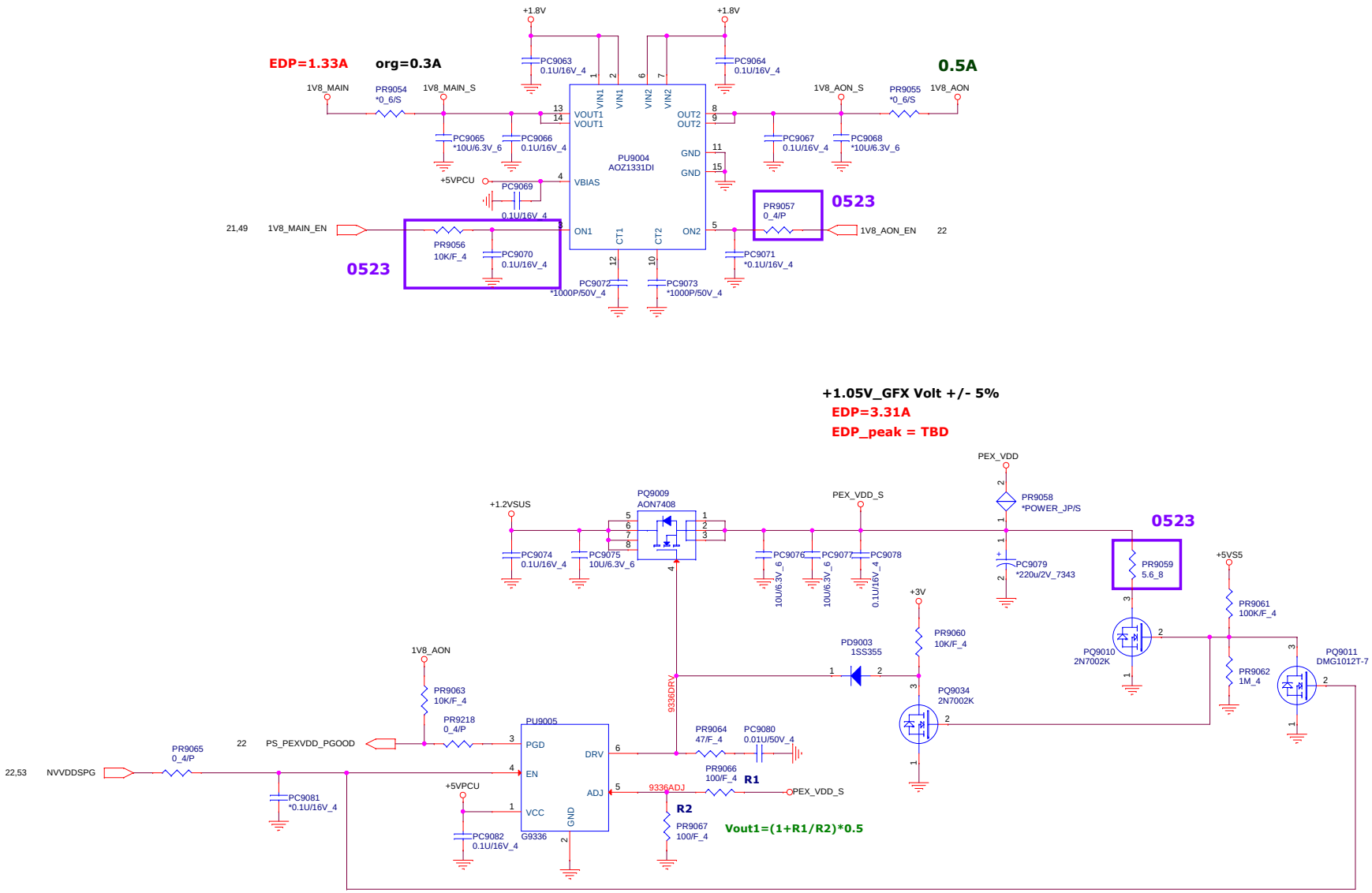

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(AOZ1331DI)	1A

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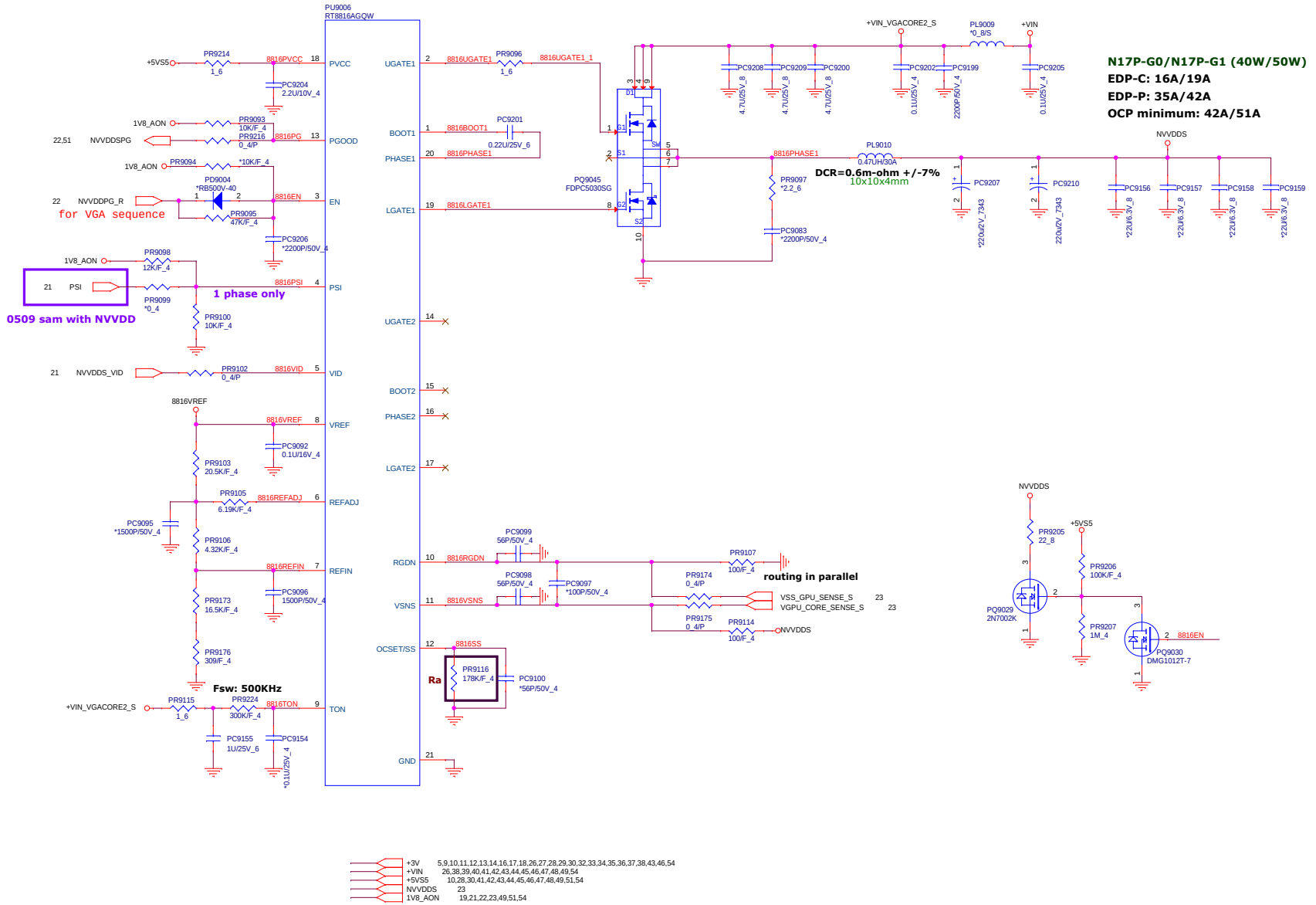

NVDDS

1. Ripple Current:

Irip=3.65A

2. Ripple Voltage:

ESR/1=9mohm
Vrip=32.85mV

3. Inductor Spec:

Isat=40A
Idc=30A
DCR=1.68mohm

4.MOSFET Spec:

H-side MOSFET: FDPC5030
Rds(ON)=6.5mohm (Vgs=4.5 V)
I cont = 17A (T =25 ℃)

L-side MOSFET: FDPC5030
Rds(ON)=3mohm (Vgs=4.5 V)
I cont = 25A (T =25 ℃)
I pulse=503A

5. Frequency:

F=500KHz (PR9224=300k ohm)

6. OCP:

Set = PR9116 to 178K
Vtrip= PR9116*10uA/12=148.3mV
Iocp=(Vtrip/Rdson) + Iripple/2 = 51.2A

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A

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