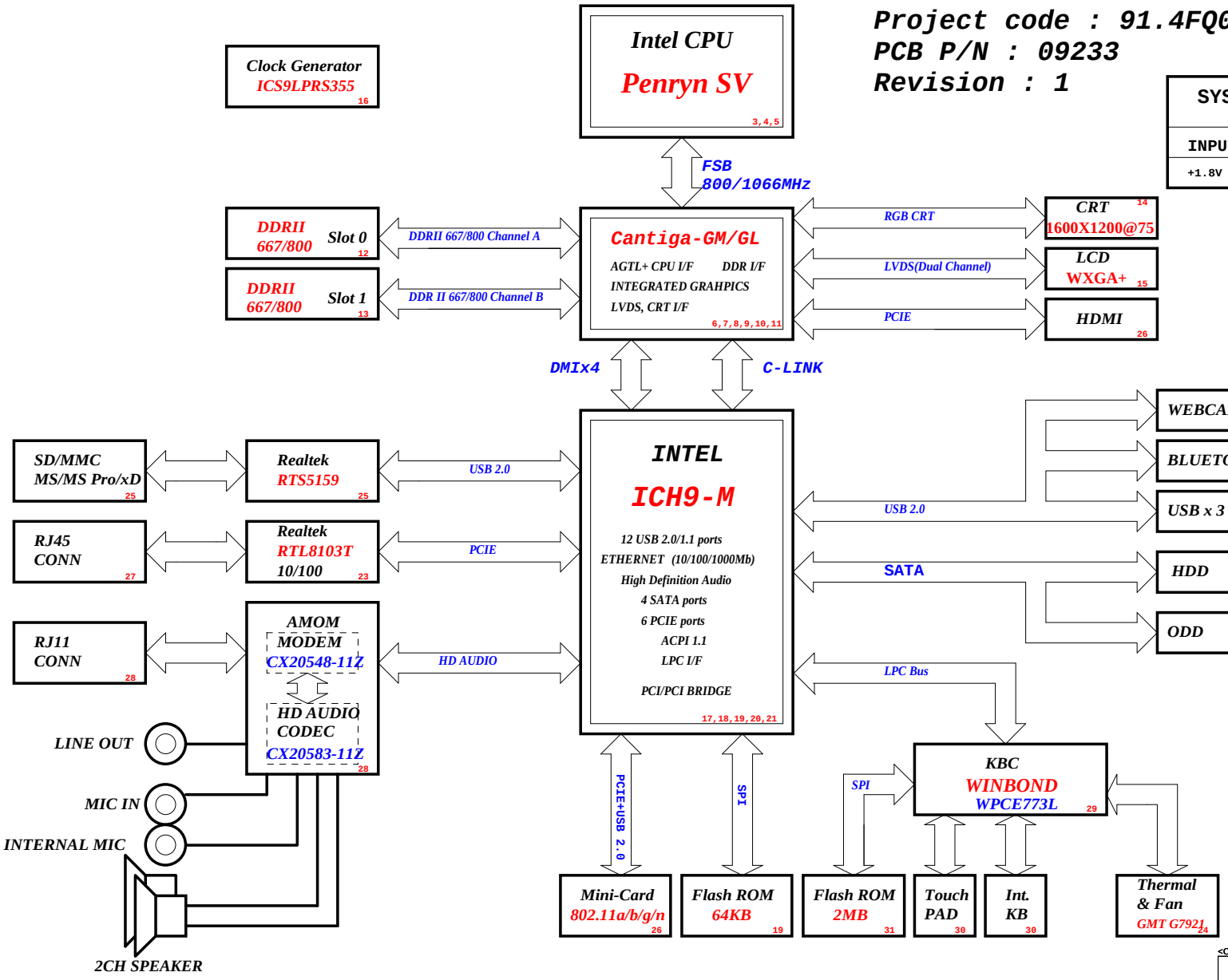
HBU16-1.2 Intel UMA Block Diagram

Project code : 91.4FQ01.001
PCB P/N : 09233
Revision : 1



SYSTEM DC/DC APL5912	
INPUTS	OUTPUTS
+1.8V	+1.5VS 40

SYSTEM DC/DC TPS51125	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 37

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 38

SYSTEM DC/DC RT8209	
INPUTS	OUTPUTS
+5VALW	+1.05V 39

MAXIM CHARGER MAX8731	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 33

CPU DC/DC ISL6269CCRZ	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 35,36

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 4
L5: VCC
L6: Signal 4

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

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LANE1	LAN
LANE2	MiniCard WLAN

USB Table

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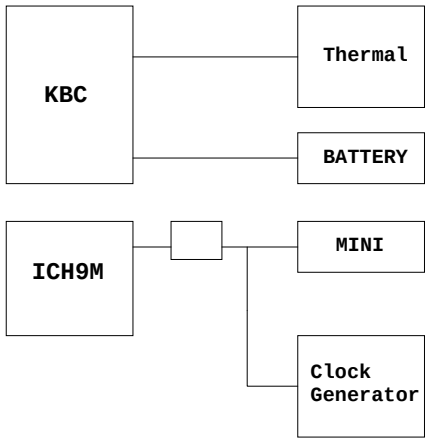
USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



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Title: Table of Content

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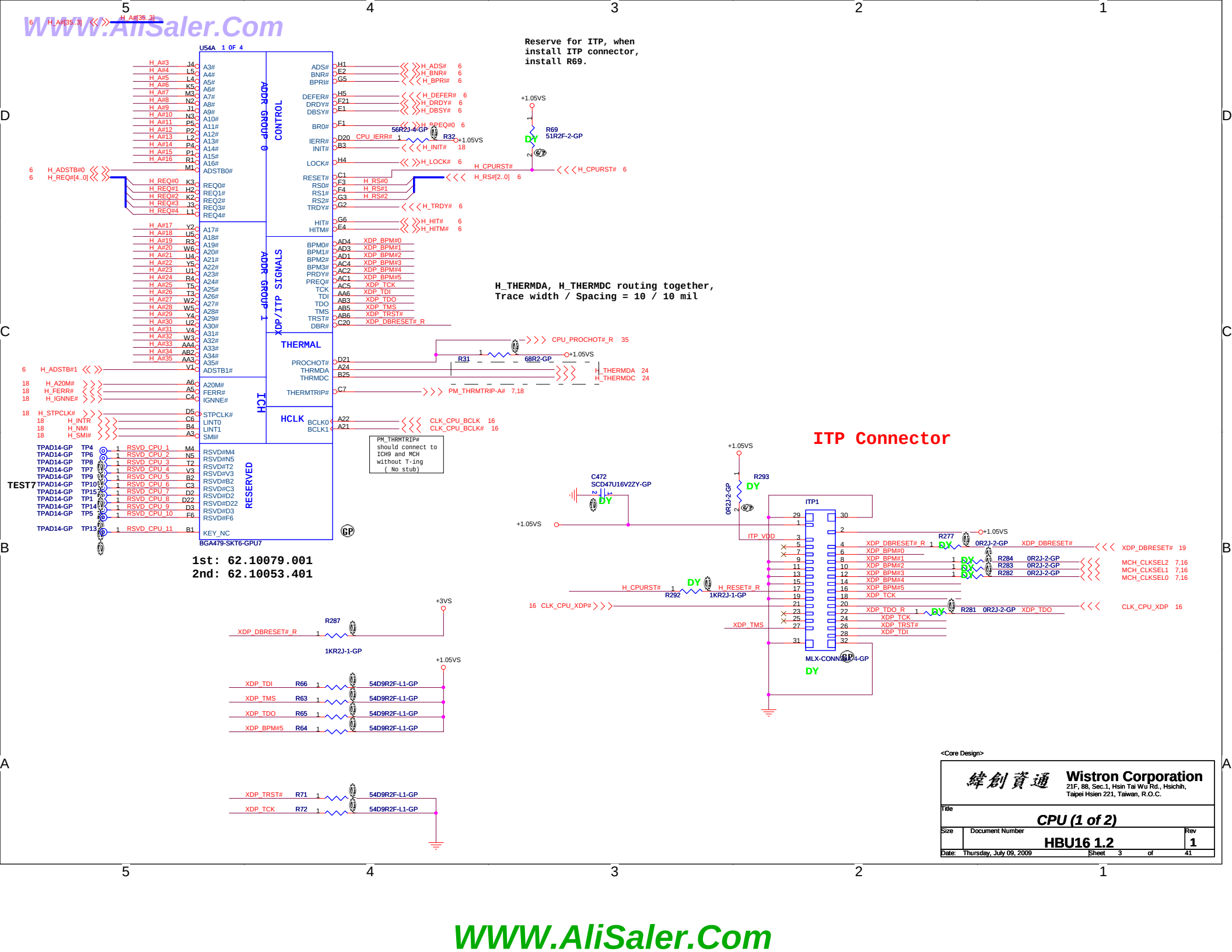
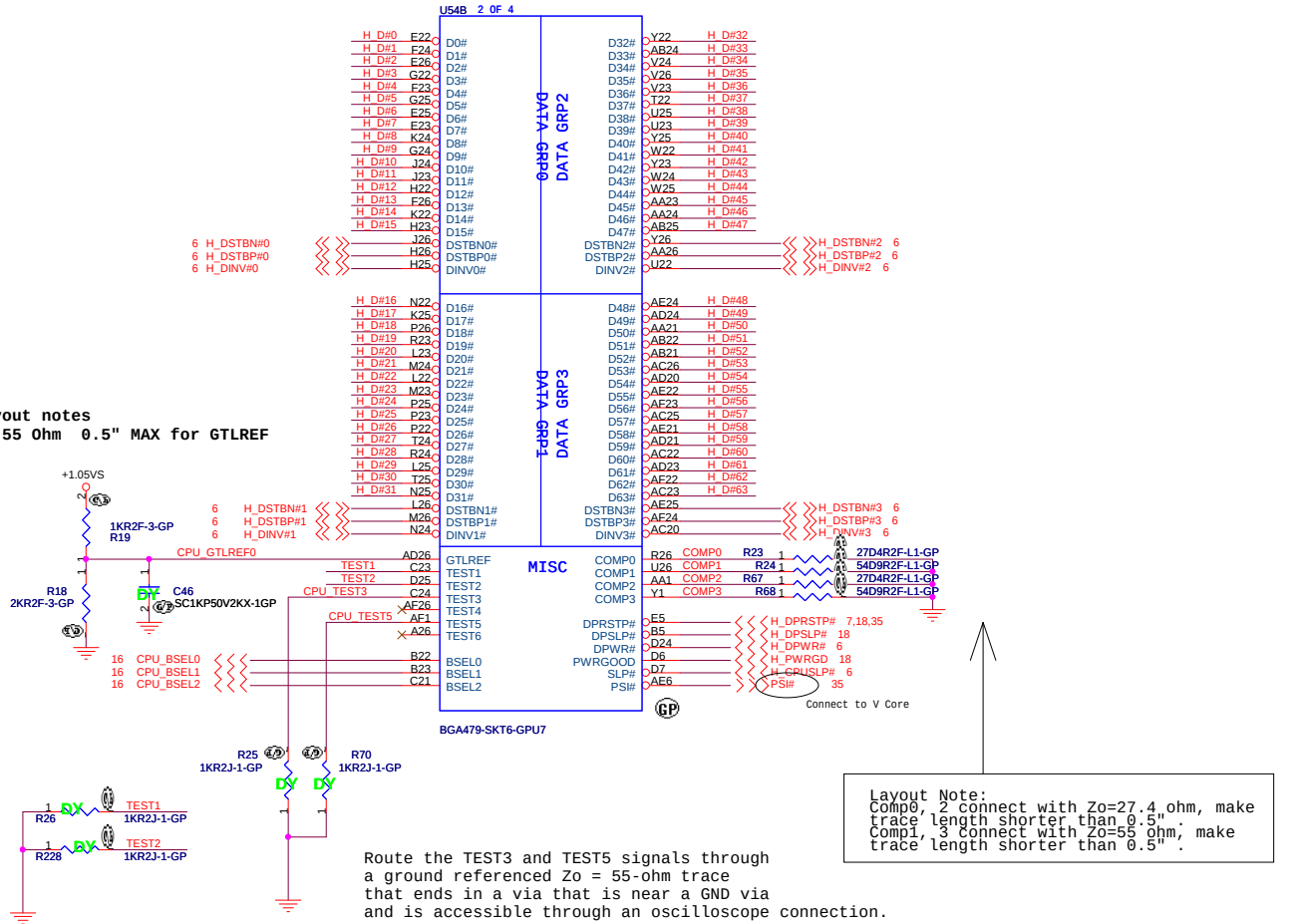


H_DINV#[3..0] H_DINV#[3..0] 6
H_DSTBN#[3..0] H_DSTBN#[3..0] 6
H_DSTBP#[3..0] H_DSTBP#[3..0] 6
H_D#[63..0] H_D#[63..0] 6



Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

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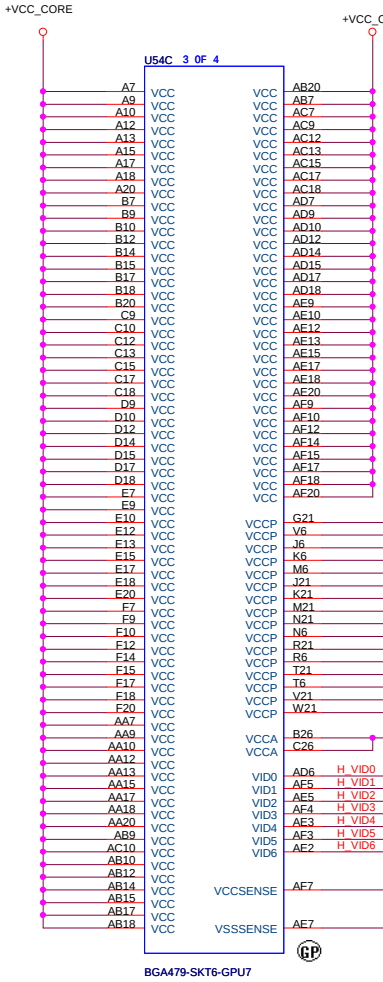
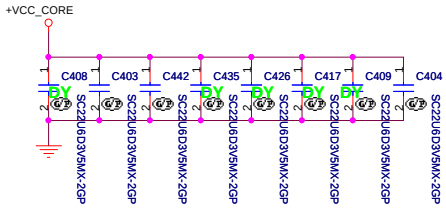
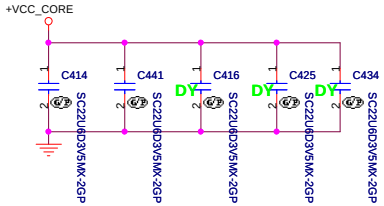
Please these inside socket cavity on L8(North side Secondary)

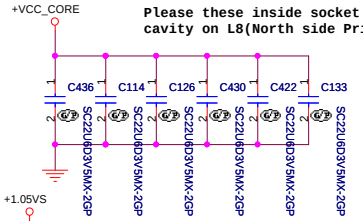


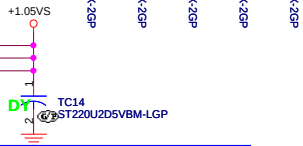


Please these inside socket cavity on L8(South side Secondary)

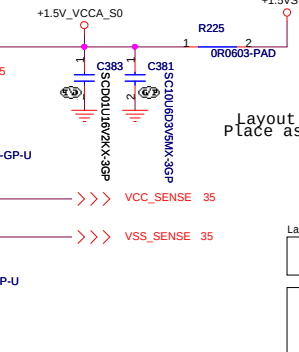


Please these inside socket cavity on L8(North side Primary)





layout note: "1D5V_VCCA_S0" as short as possible



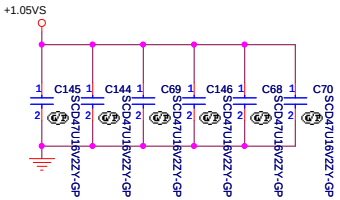
Layout Note:
Place as close as possible to the CPU VCCA pin.

Connect to V Core

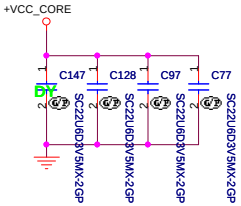
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

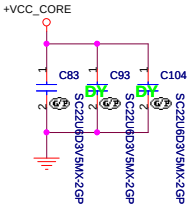
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket cavity on L8(North side Secondary)



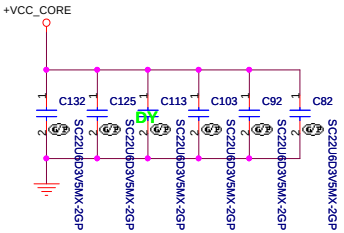
Please these outside socket cavity on L8(North side Secondary)

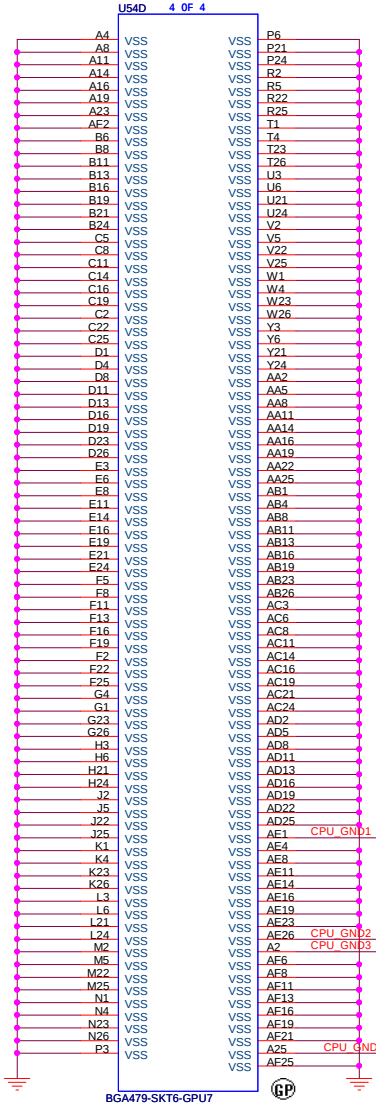


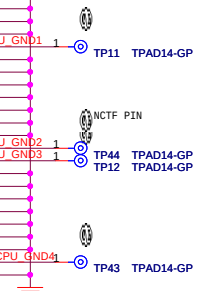


Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)







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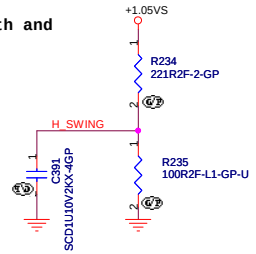
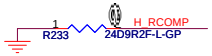
H_SWING routing Trace width and Spacing use 10 / 20 mil

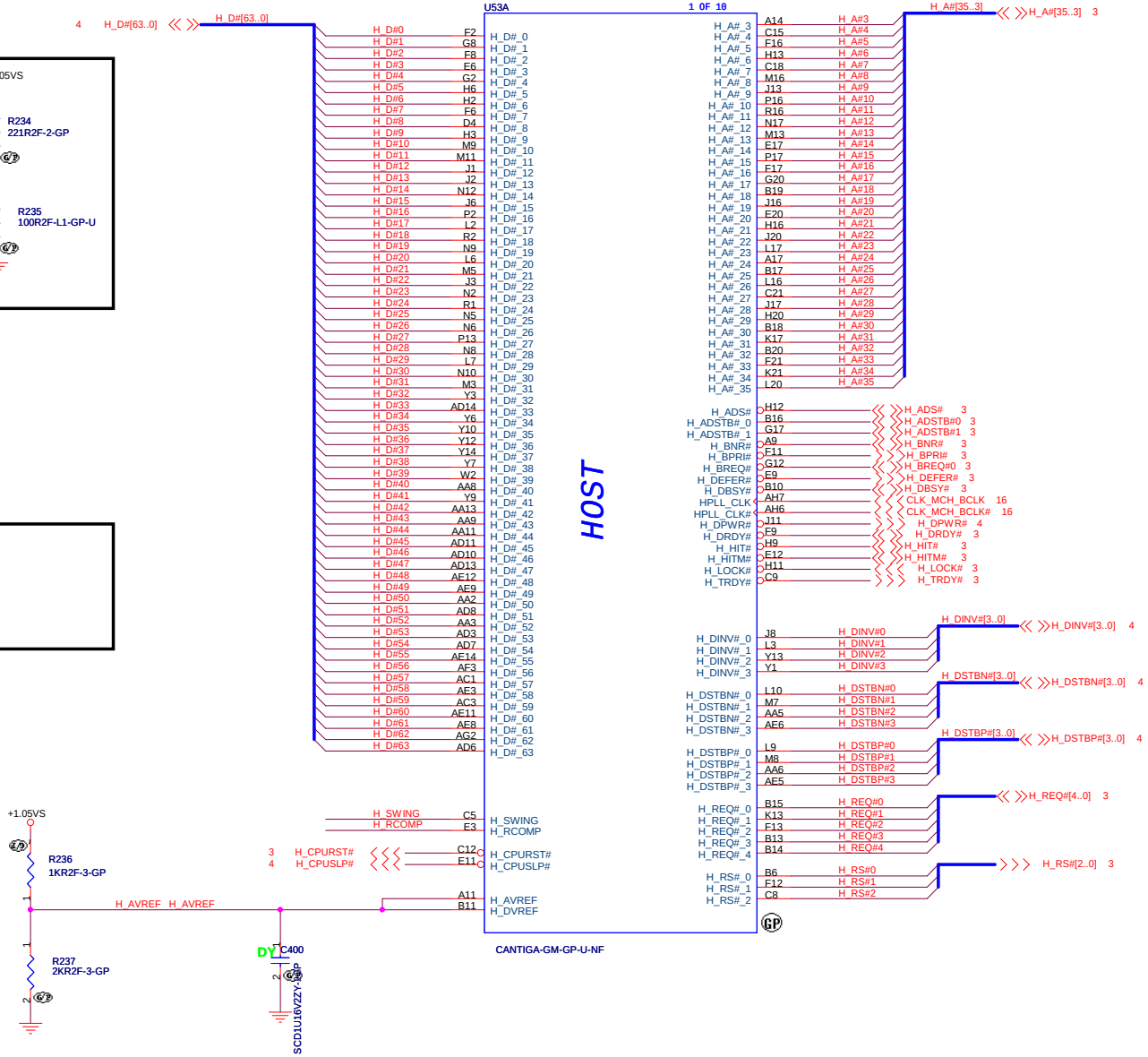
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

FSB setting

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

FOR Cantiga: 1.02k_1% ohm
CRT_IREF routing Trace width use 20 mil

DDPC/SDVO for HDMI used

CL_VREF ~= 0.35V

CRT Termination/EMI Filter

Place Close GMCH

Place Close Connector

Please Close GMCH

Please Close to U22

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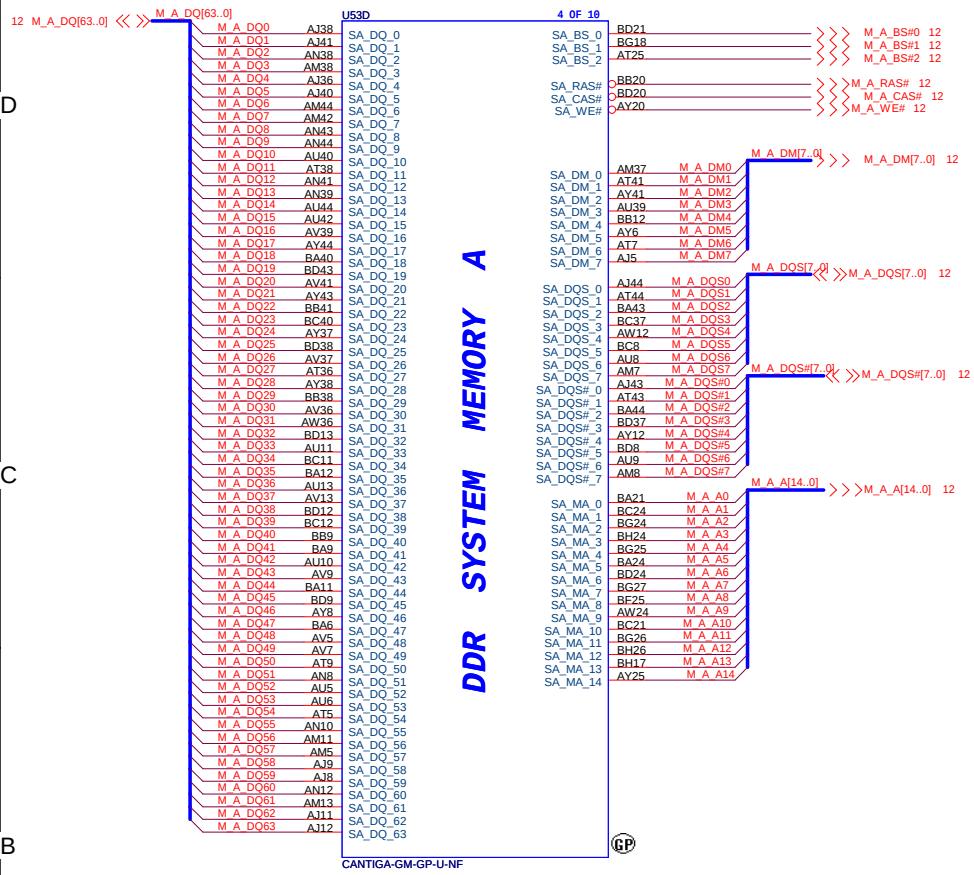

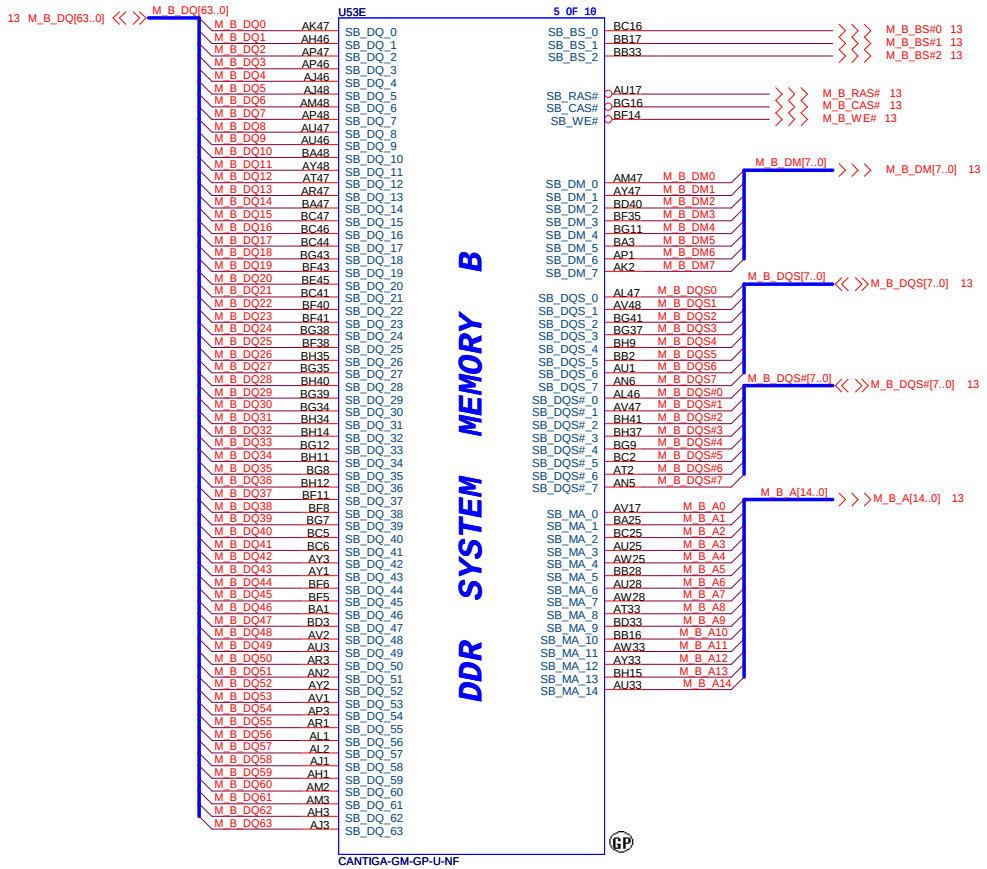

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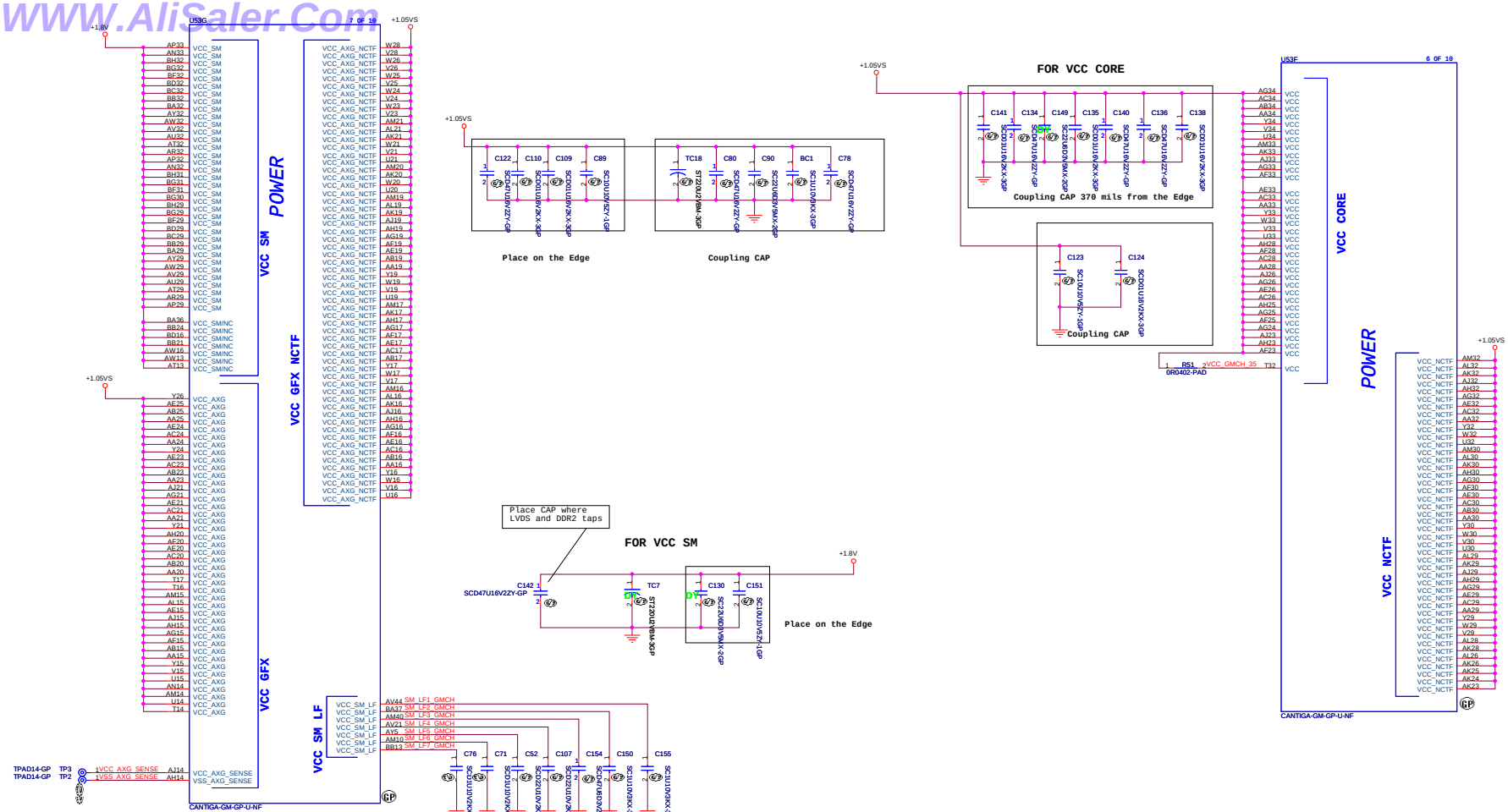

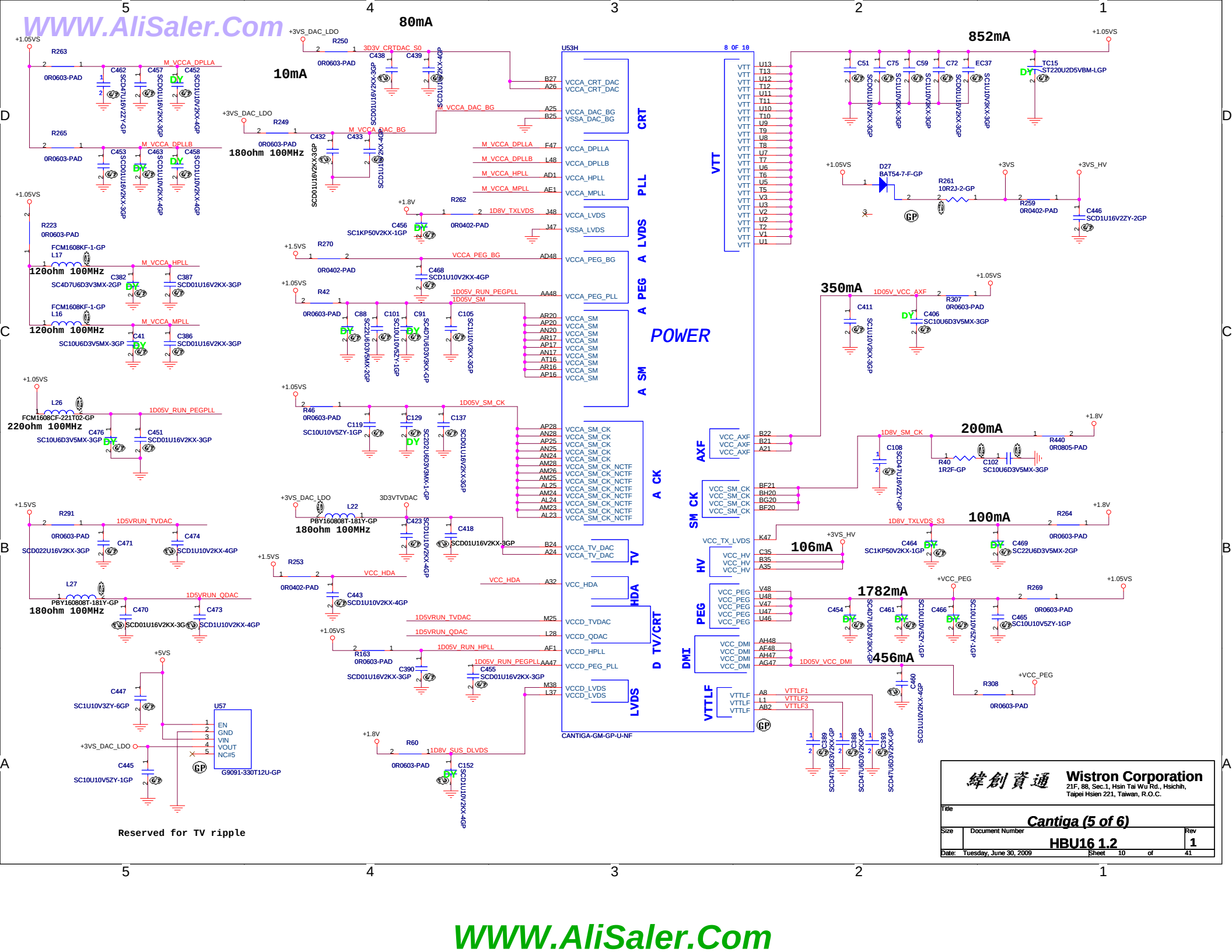

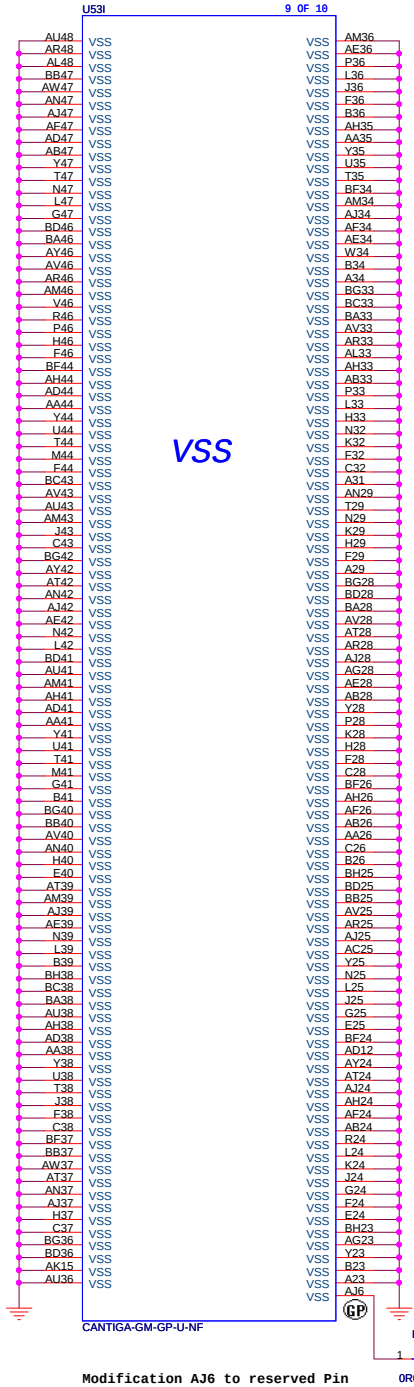

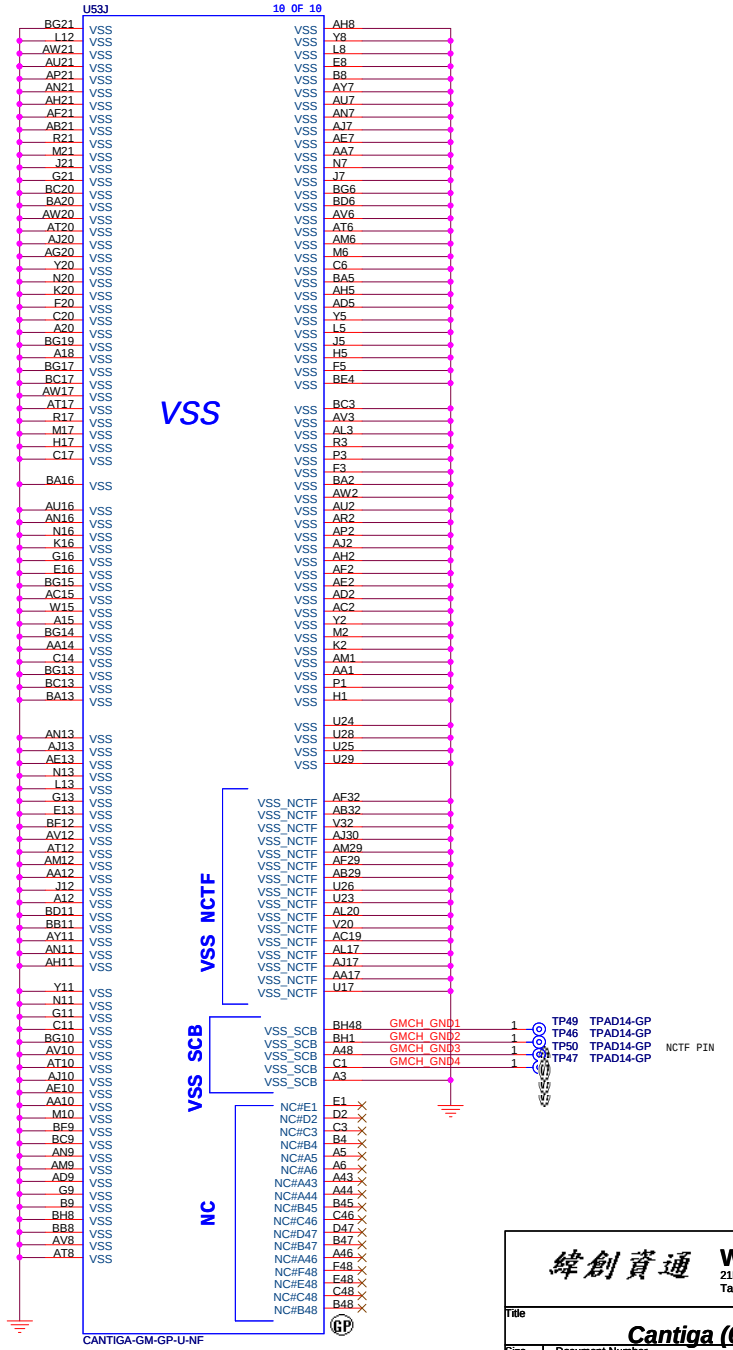

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8 M_A_DQS#[7..0]
8 M_A_DQ[63..0]
8 M_A_DM[7..0]
8 M_A_DQS[7..0]
8 M_A_A[14..0]

Layout Note:
Place near DM1

+1.8V
C118 SC4D7U6D3V8KX-GP
C74 SC4D7U6D3V8KX-GP
C94 DY SC2D2U10V2ZY-1GP
C53 DY SC2D2U10V2ZY-1GP
C87 SC4D7U6D3V8KX-GP
C106 DY SCD1U16V2ZY-2GP
C111 SCD47U16V2ZY-GP
C63 SCD1U16V2ZY-2GP
C58 DY SCD1U16V2ZY-2GP
TC2 DY ST220U2D5VBM-L-GP

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS
C84 DY SCD1U16V2ZY-2GP
C65 DY SCD1U16V2ZY-2GP
C55 SCD1U16V2ZY-2GP
C48 DY SCD1U16V2ZY-2GP
C98 SCD1U16V2ZY-2GP
C405 DY SCD1U16V2ZY-2GP
C398 SCD1U16V2ZY-2GP
C397 DY SCD1U16V2ZY-2GP
C410 DY SCD1U16V2ZY-2GP
C419 SCD1U16V2ZY-2GP
C427 SCD1U16V2ZY-2GP
C115 SCD1U16V2ZY-2GP
C392 SCD1U16V2ZY-2GP

+0.9VS
RN44 SRN56J-4-GP: M_A_A12, M_A_BS#2
RN45 SRN56J-4-GP: M_CKE0
RN41 SRN56J-4-GP: M_A_BS#0, M_A_A10
RN43 SRN56J-4-GP: M_A_A8, M_A_A9
RN6 SRN56J-4-GP: M_ODT0, M_CS0#
RN15 SRN56J-4-GP: M_A_A6, M_A_A5
RN18 SRN56J-4-GP: M_A_A14, M_A_A11
RN42 SRN56J-4-GP: M_A_A1, M_A_A3
RN40 SRN56J-4-GP: M_A_CAS#, M_A_WE#
RN9 SRN56J-4-GP: M_A_A2, M_A_A13
RN39 SRN56J-4-GP: M_ODT1, M_CS1#
RN3 SRN56J-4-GP: M_A_BS#1, M_A_RAS#
RN21 SRN56J-4-GP: M_CKE1, M_A_A7
RN12 SRN56J-4-GP: M_A_A4, M_A_A0

Layout Note:
Place these resistors closely DM1,all trace length Max=1.5"

DM2
M_A_A0 102 … M_A_A14 86
M_A_BS#2 85
M_A_BS#0 107
M_A_BS#1 106
M_A_DQ0 5 … M_A_DQ63 194
M_A_DQS#0 11 … M_A_DQS#7 186
M_A_DQS0 13 … M_A_DQS7 188
M_ODT0 114
M_ODT1 119
DDR_VREF_S3 → SC2D2U10V3ZY-1GP 1, 2
C467 SCD1U16V2ZY-2GP
C448
202
DDR2-200P-36-GP-U1

/RAS 108 → M_A_RAS# 8
/WE 109 → M_A_WE# 8
/CAS 113 → M_A_CAS# 8
/CS0 110 → M_CS0# 7
/CS1 115 → M_CS1# 7
CKE0 79 → M_CKE0 7
CKE1 80 → M_CKE1 7
CK0 30 → M_CLK_DDR0 7
/CK0 32 → M_CLK_DDR#0 7
CK1 164 → M_CLK_DDR1 7
/CK1 166 → M_CLK_DDR#1 7
DM0 10 → M_A_DM0
DM1 26 → M_A_DM1
DM2 52 → M_A_DM2
DM3 67 → M_A_DM3
DM4 130 → M_A_DM4
DM5 147 → M_A_DM5
DM6 170 → M_A_DM6
DM7 185 → M_A_DM7
SDA 195 → ICH_SMBDATA 13,16,21,26
SCL 197 → ICH_SMBCLK 13,16,21,26
VDDSPD 199 → +3VS
SA0 198, SA1 200 → RN2 SRN10KJ-11-GP-U
NC#50 69, NC#69 83, NC#83 120, NC#120 163, NC#163/TEST
50 → PM_EXTTS#0 7
C18 SCD1U16V2ZY-2GP
C15 DY SC2D2U10V3ZY-1GP
VDD: 81, 82, 87, 88, 95, 96, 103, 104, 111, 112, 117, 118 ← +1.8V
VSS: 3, 8, 9, 12, 15, 18, 21, 24, 27, 28, 33, 34, 39, 40, 41, 42, 47, 48, 53, 54, 59, 60, 65, 66, 71, 72, 77, 78, 121, 122, 127, 128, 132, 133, 138, 139, 144, 145, 149, 150, 155, 156, 161, 162, 165, 168, 171, 172, 177, 178, 183, 184, 187, 190, 193, 196

M_CLK_DDR0
M_CLK_DDR#0
C153 DUMMY-C2
C156 DUMMY-C2
put near connector
C37 DUMMY-C2
C36 DUMMY-C2

DM2	1st:	62.10017.E11
	2nd:	62.10017.691
	3nd:	62.10017.891

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1
Size: Custom | Document Number: HBU16 1.2 | Rev: 1
Date: Thursday, July 09, 2009 | Sheet 12 of 41

8 M_B_DQS#[7..0]
8 M_B_DQ[63..0]
8 M_B_DM[7..0]
8 M_B_DQS[7..0]
8 M_B_A[14..0]

Layout Note:
Place near DM2

+1.8V
C54 SC4D7U6D3V3KX-6P
C399 DIY SC2D2U10N3ZY-1GP
C407 SC4D7U6D3V3KX-6P
C79 SC4D7U6D3V3KX-6P
C112 SC4D7U6D3V9KX-GP
C95 SCD1U16V4ZY-2GP
C394 DIY SCD1U16V4ZY-2GP
C421 SCD1U16V4ZY-2GP
C64 SCD1U16V4ZY-2GP
C8 DIY ST220U2D5VBM-L6P

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS
C45 DIY SCD1U16V2ZY-2GP
C49 SCD1U16V2ZY-2GP
C56 SCD1U16V2ZY-2GP
C66 DIY SCD1U16V2ZY-2GP
C85 SCD1U16V2ZY-2GP
C99 SCD1U16V2ZY-2GP
C116 SCD1U16V2ZY-2GP
C67 SCD1U16V2ZY-2GP
C50 SCD1U16V2ZY-2GP
C57 DIY SCD1U16V2ZY-2GP
C86 SCD1U16V2ZY-2GP
C100 DIY SCD1U16V2ZY-2GP
C117 SCD1U16V2ZY-2GP

+0.9VS
RN4 SRN56J-4-GP: M_B_CAS#, M_B_WE#
RN22 SRN56J-4-GP: M_B_A9, M_CKE2
RN16 SRN56J-4-GP: M_B_A8, M_B_A5
RN11 SRN56J-4-GP: M_B_A0, M_B_BS#1
RN10 SRN56J-4-GP: M_B_A3, M_B_A1
RN7 SRN56J-4-GP: M_CS3#, M_ODT3
RN23 SRN56J-4-GP: M_CKE3
RN5 SRN56J-4-GP: M_B_RAS#, M_B_A13
RN20 SRN56J-4-GP: M_B_A14, M_B_A11
RN17 SRN56J-4-GP: M_B_A6, M_B_A7
RN14 SRN56J-4-GP: M_B_A2, M_B_A4
RN13 SRN56J-4-GP: M_B_A10, M_B_BS#0
RN8 SRN56J-4-GP: M_CS2#, M_ODT2
RN19 SRN56J-4-GP: M_B_BS#2, M_B_A12

Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"

DM1 DDR2-200P-25-GP-U2

M_B_A0	102	A0	
M_B_A1	101	A1	
M_B_A2	100	A2	
M_B_A3	99	A3	
M_B_A4	98	A4	
M_B_A5	97	A5	
M_B_A6	94	A6	
M_B_A7	92	A7	
M_B_A8	93	A8	
M_B_A9	91	A9	
M_B_A10	105	A10/AP	
M_B_A11	90	A11	
M_B_A12	89	A12	
M_B_A13	116	A13	
M_B_A14	86	A14	
	84	A15	
M_B_BS#2	85	A16/BA2	
M_B_BS#0	107	BA0	
M_B_BS#1	106	BA1	
M_B_DQ0	5	DQ0	
M_B_DQ1	7	DQ1	
M_B_DQ2	17	DQ2	
M_B_DQ3	19	DQ3	
M_B_DQ4	4	DQ4	
M_B_DQ5	6	DQ5	
M_B_DQ6	14	DQ6	
M_B_DQ7	16	DQ7	
M_B_DQ8	23	DQ8	
M_B_DQ9	25	DQ9	
M_B_DQ10	35	DQ10	
M_B_DQ11	37	DQ11	
M_B_DQ12	20	DQ12	
M_B_DQ13	22	DQ13	
M_B_DQ14	36	DQ14	
M_B_DQ15	38	DQ15	
M_B_DQ16	43	DQ16	
M_B_DQ17	45	DQ17	
M_B_DQ18	55	DQ18	
M_B_DQ19	57	DQ19	
M_B_DQ20	44	DQ20	
M_B_DQ21	46	DQ21	
M_B_DQ22	56	DQ22	
M_B_DQ23	58	DQ23	
M_B_DQ24	61	DQ24	
M_B_DQ25	63	DQ25	
M_B_DQ26	73	DQ26	
M_B_DQ27	75	DQ27	
M_B_DQ28	62	DQ28	
M_B_DQ29	64	DQ29	
M_B_DQ30	74	DQ30	
M_B_DQ31	76	DQ31	
M_B_DQ32	123	DQ32	
M_B_DQ33	125	DQ33	
M_B_DQ34	135	DQ34	
M_B_DQ35	137	DQ35	
M_B_DQ36	124	DQ36	
M_B_DQ37	126	DQ37	
M_B_DQ38	134	DQ38	
M_B_DQ39	136	DQ39	
M_B_DQ40	141	DQ40	
M_B_DQ41	143	DQ41	
M_B_DQ42	151	DQ42	
M_B_DQ43	153	DQ43	
M_B_DQ44	140	DQ44	
M_B_DQ45	142	DQ45	
M_B_DQ46	152	DQ46	
M_B_DQ47	154	DQ47	
M_B_DQ48	157	DQ48	
M_B_DQ49	159	DQ49	
M_B_DQ50	173	DQ50	
M_B_DQ51	175	DQ51	
M_B_DQ52	158	DQ52	
M_B_DQ53	160	DQ53	
M_B_DQ54	174	DQ54	
M_B_DQ55	176	DQ55	
M_B_DQ56	179	DQ56	
M_B_DQ57	181	DQ57	
M_B_DQ58	189	DQ58	
M_B_DQ59	191	DQ59	
M_B_DQ60	180	DQ60	
M_B_DQ61	182	DQ61	
M_B_DQ62	192	DQ62	
M_B_DQ63	194	DQ63	
M_B_DQS#0	11	/DQS0	
M_B_DQS#1	29	/DQS1	
M_B_DQS#2	49	/DQS2	
M_B_DQS#3	68	/DQS3	
M_B_DQS#4	129	/DQS4	
M_B_DQS#5	146	/DQS5	
M_B_DQS#6	167	/DQS6	
M_B_DQS#7	186	/DQS7	
M_B_DQS0	13	DQS0	
M_B_DQS1	31	DQS1	
M_B_DQS2	51	DQS2	
M_B_DQS3	70	DQS3	
M_B_DQS4	131	DQS4	
M_B_DQS5	148	DQS5	
M_B_DQS6	169	DQS6	
M_B_DQS7	188	DQS7	
M_ODT2	114	ODT0	
M_ODT3	119	ODT1	
	1	VREF	
	2	VSS	
	202	GND	
	108	/RAS	M_B_RAS# 8
	109	/WE	M_B_WE# 8
	113	/CAS	M_B_CAS# 8
	110	/CS0	M_CS2# 7
	115	/CS1	M_CS3# 7
	79	CKE0	M_CKE2 7
	80	CKE1	M_CKE3 7
	30	CK0	M_CLK_DDR2 7
	32	/CK0	M_CLK_DDR#2 7
	164	CK1	M_CLK_DDR3 7
	166	/CK1	M_CLK_DDR#3 7
M_B_DM0	10	DM0	
M_B_DM1	26	DM1	
M_B_DM2	52	DM2	
M_B_DM3	67	DM3	
M_B_DM4	130	DM4	
M_B_DM5	147	DM5	
M_B_DM6	170	DM6	
M_B_DM7	185	DM7	
ICH_SMBDATA	195	SDA	ICH_SMBDATA 12,16,21,26
ICH_SMBCLK	197	SCL	ICH_SMBCLK 12,16,21,26
	199	VDDSPD	+3VS
	198	SA0	R12 10KR2J-3-GP
	200	SA1	R11 10KR2J-3-GP
	50	NC#50	
	69	NC#69	PM_EXTTS#1 7
	83	NC#83	
	120	NC#120	
	163	NC#163/TEST	
	81	VDD	
	82	VDD	
	87	VDD	
	88	VDD	
	95	VDD	
	96	VDD	
	103	VDD	
	104	VDD	
	111	VDD	
	112	VDD	
	117	VDD	
	118	VDD	
	3	VSS	
	8	VSS	
	9	VSS	
	12	VSS	
	15	VSS	
	18	VSS	
	21	VSS	
	24	VSS	
	27	VSS	
	28	VSS	
	33	VSS	
	34	VSS	
	39	VSS	
	40	VSS	
	41	VSS	
	42	VSS	
	47	VSS	
	48	VSS	
	53	VSS	
	54	VSS	
	59	VSS	
	60	VSS	
	65	VSS	
	66	VSS	
	71	VSS	
	72	VSS	
	77	VSS	
	78	VSS	
	121	VSS	
	122	VSS	
	127	VSS	
	128	VSS	
	132	VSS	
	133	VSS	
	138	VSS	
	139	VSS	
	144	VSS	
	145	VSS	
	149	VSS	
	150	VSS	
	155	VSS	
	156	VSS	
	161	VSS	
	162	VSS	
	165	VSS	
	168	VSS	
	171	VSS	
	172	VSS	
	177	VSS	
	178	VSS	
	183	VSS	
	184	VSS	
	187	VSS	
	190	VSS	
	193	VSS	
	196	VSS	
	201	GND	

M_CLK_DDR2
M_CLK_DDR#2
C157 DUMMY-C2
C158 DUMMY-C2
put near connector
C33 DUMMY-C2
C32 DUMMY-C2
+3VS
EC45 SCD1U25V2KY-1GP
C17 SCD1U16V2ZY-2GP
C14 DIY SC2D2U10V3ZY-1GP

DDR_VREF_S3
7 M_ODT2
7 M_ODT3
SC2D2U10V3ZY-1GP
C163 SCD1U16V2ZY-2GP
C162 DIY

DM1 1st: 62.10017.B51
DM1 2nd: 62.10017.E81

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2
Size: Custom
Document Number: HBU16 1.2
Rev: 1
Date: Thursday, July 09, 2009
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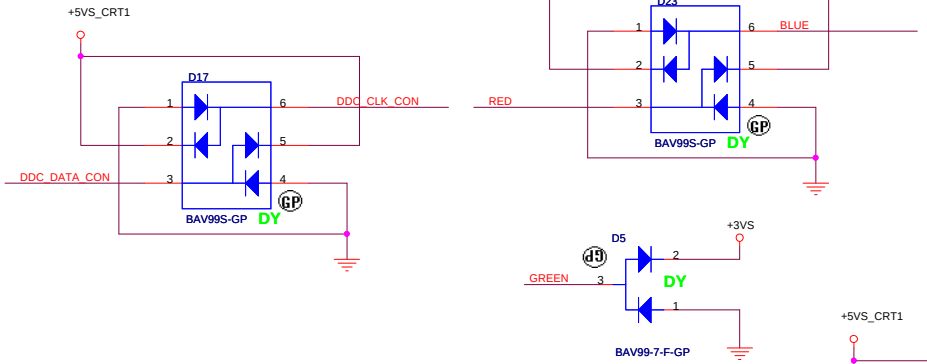
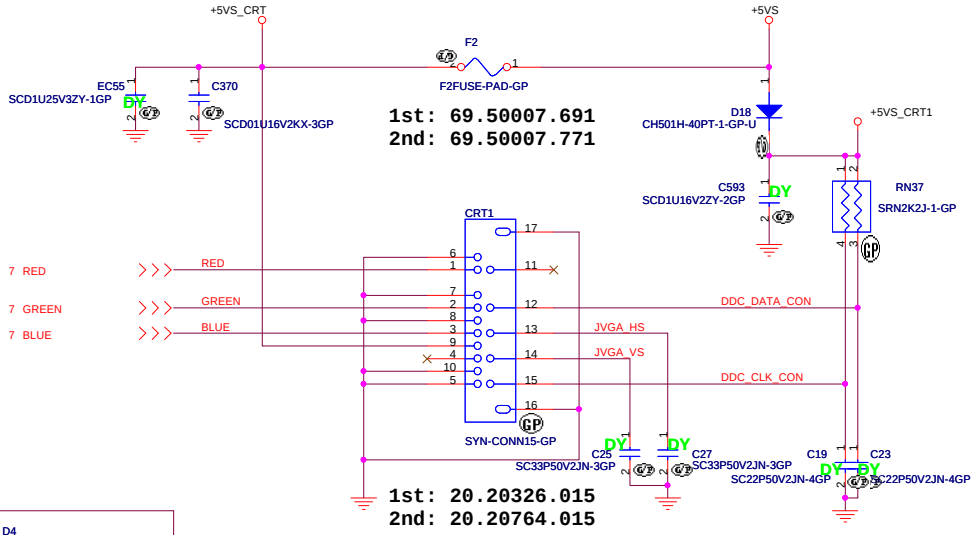
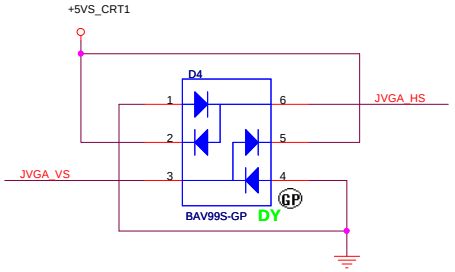
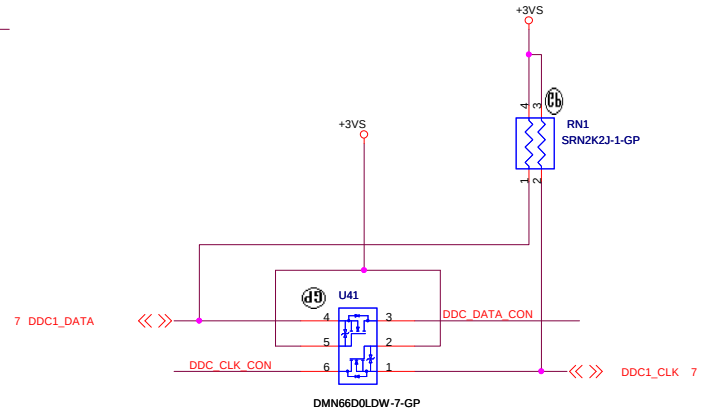
CRT I/F & CONNECTOR



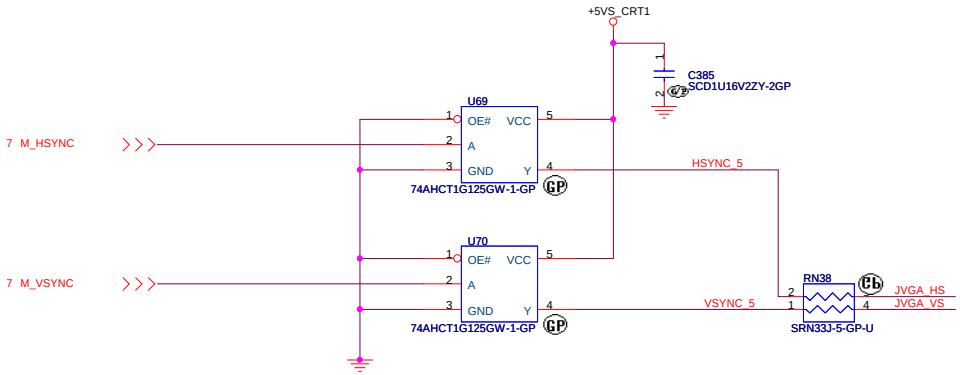




Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



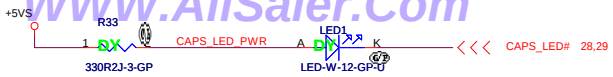
5V @ ext. CRT side



<Core Design>

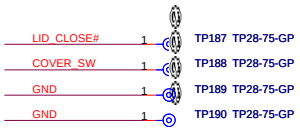
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CRT Connector***
Size: A3	Document Number: **HBU16 1.2** Rev: **1**
Date: Thursday, July 09, 2009	Sheet 14 of 41

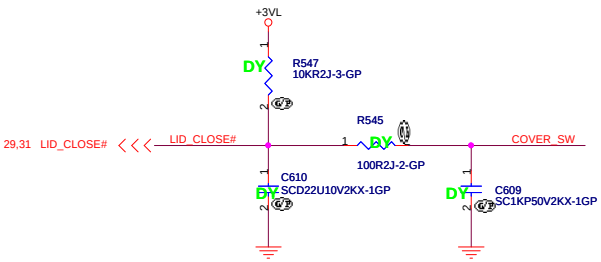
LCD / INVERTER INTERFACE / CAMERA

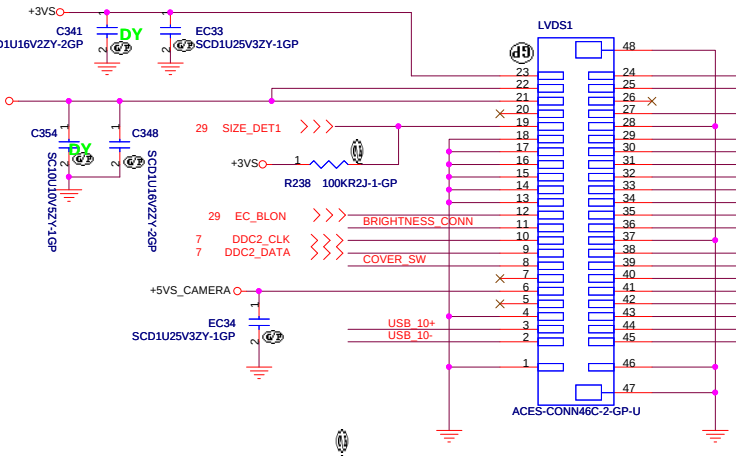


White LED:

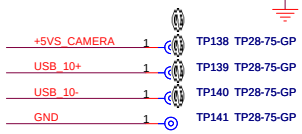
Lite-On	83.00191.D70
Everlight	83.19217.F70



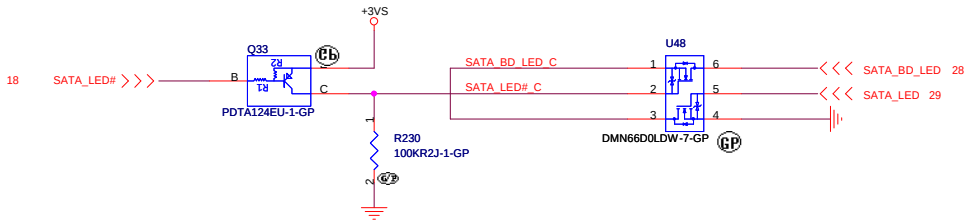


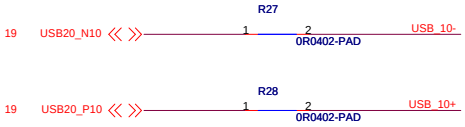


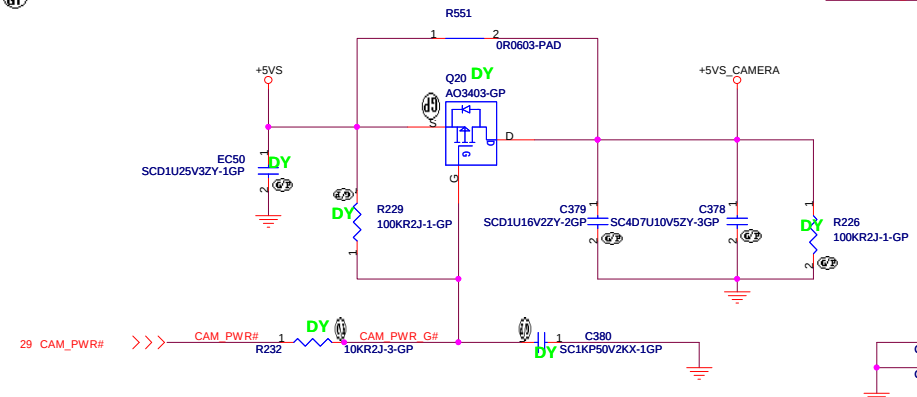
	SIZE_DET0 (Pin27)	SIZE_DET1 (Pin19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0

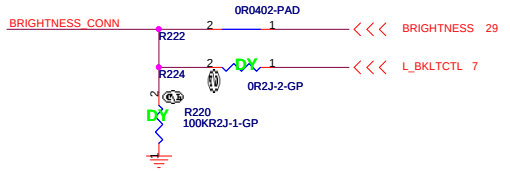


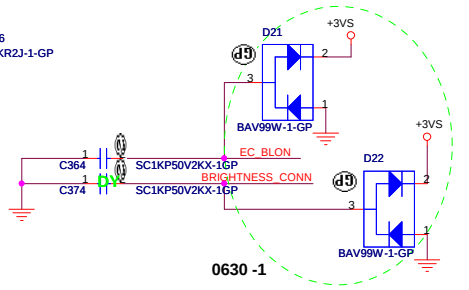
1st: 20.F1296.046
2nd: 20.F1270.046

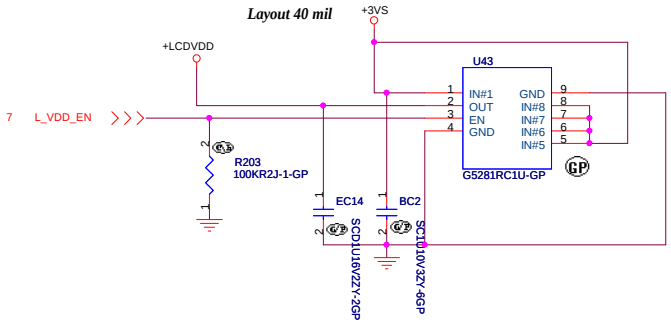


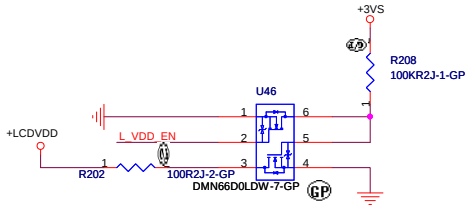












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector/CAM/LED**

Size	Document Number	Rev
A3	HBU16 1.2	1

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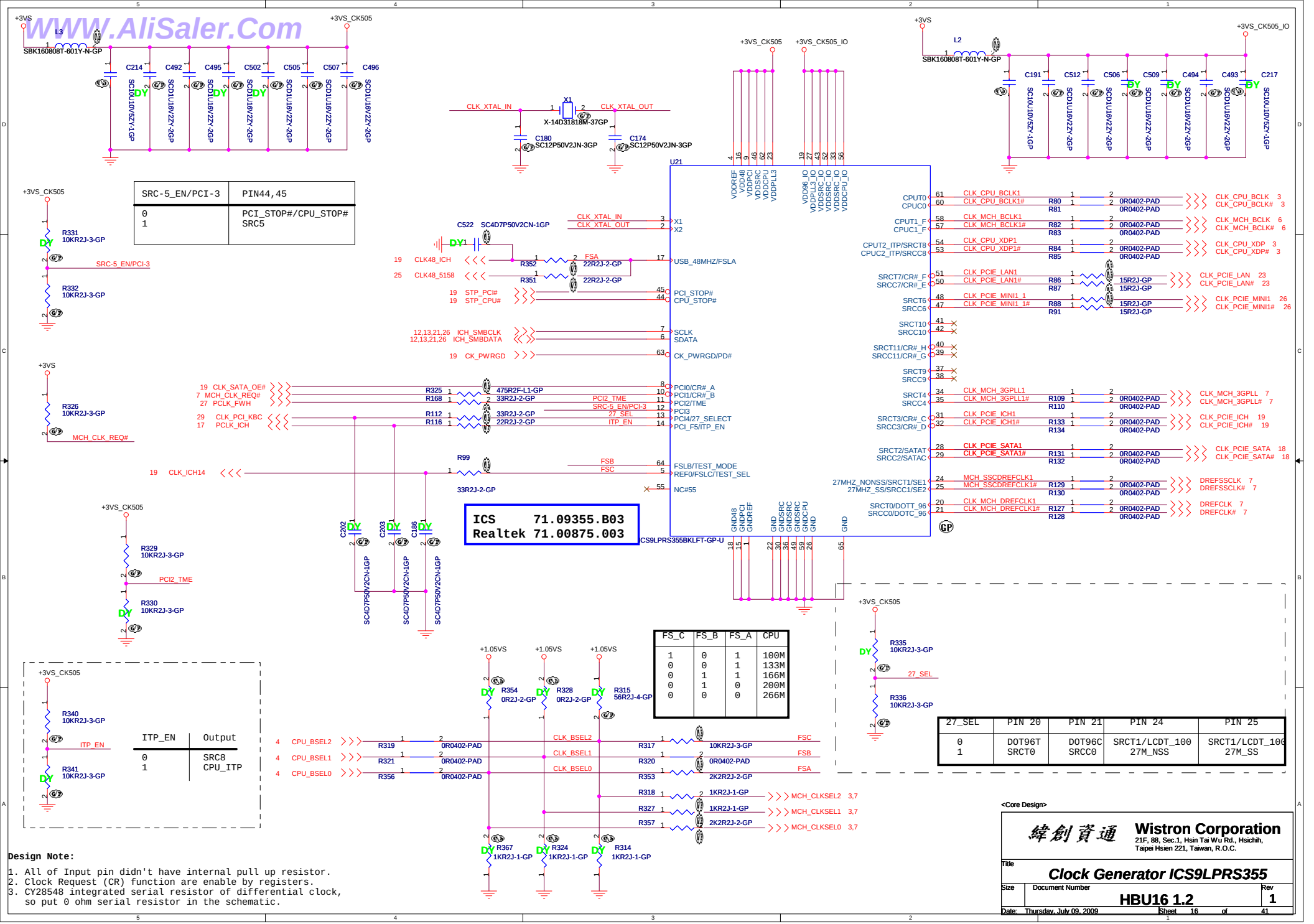

SRC-5_EN/PCI-3	PIN44,45
0	PCI_STOP#/CPU_STOP#
1	SRC5

ICS 71.09355.B03
Realtek 71.00875.003

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M
0	0	0	266M

ITP_EN	Output
0	SRC8
1	CPU_ITP

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator ICS9LPRS355**

Size: | Document Number: HBU16 1.2 | Rev: 1

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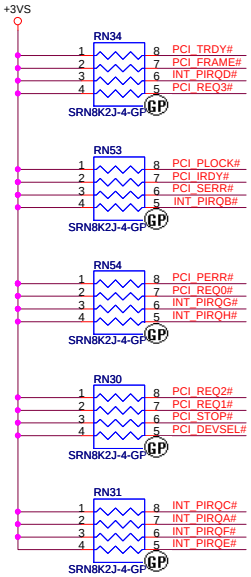
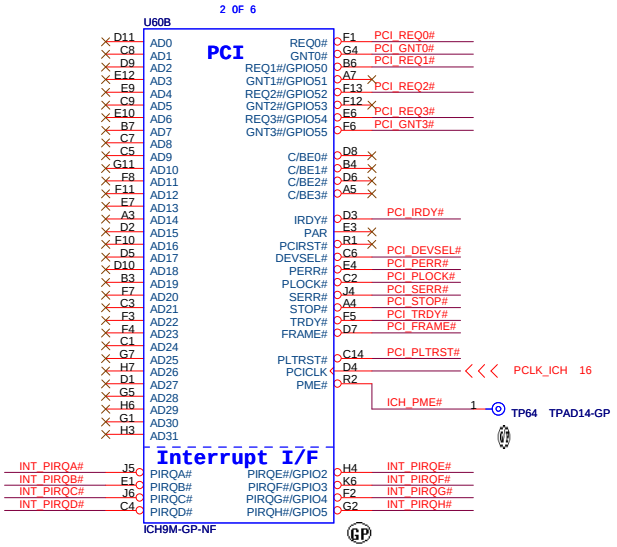
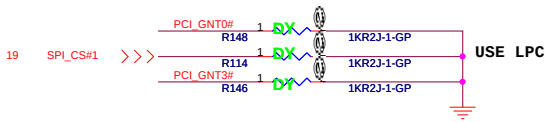
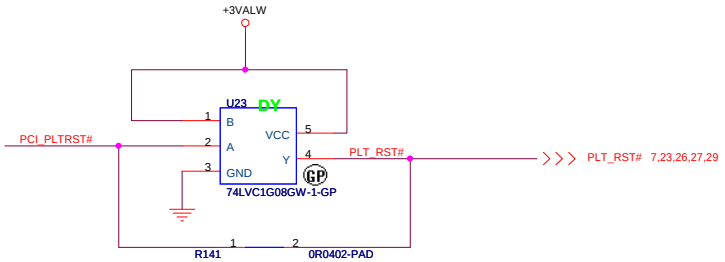






BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



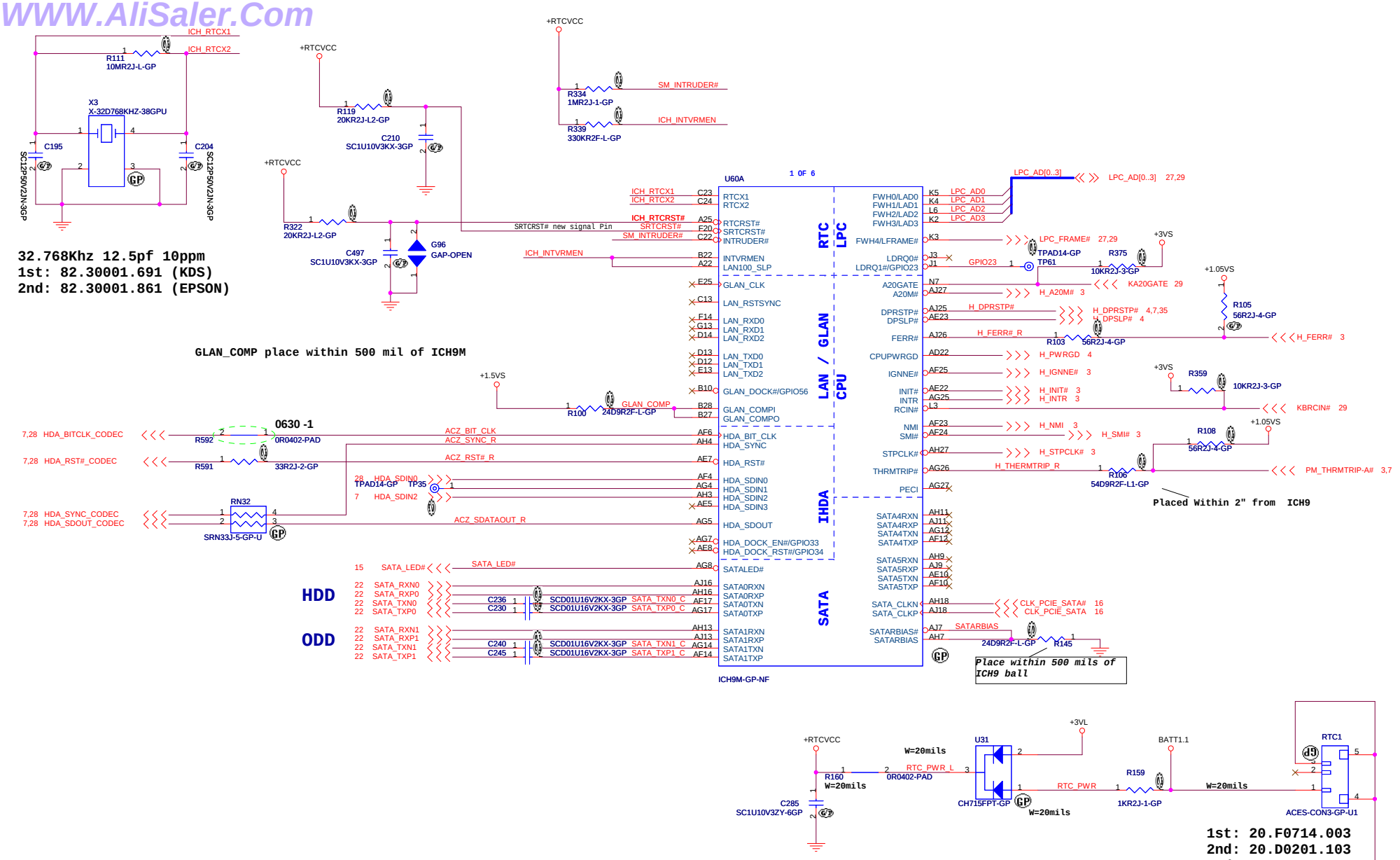
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 5)

Size | Document Number: HBU16 1.2 | Rev: 1

Date: Thursday, July 09, 2009 | Sheet 17 of 41



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

<Core Design>

緯創資通 Wistron Corporation
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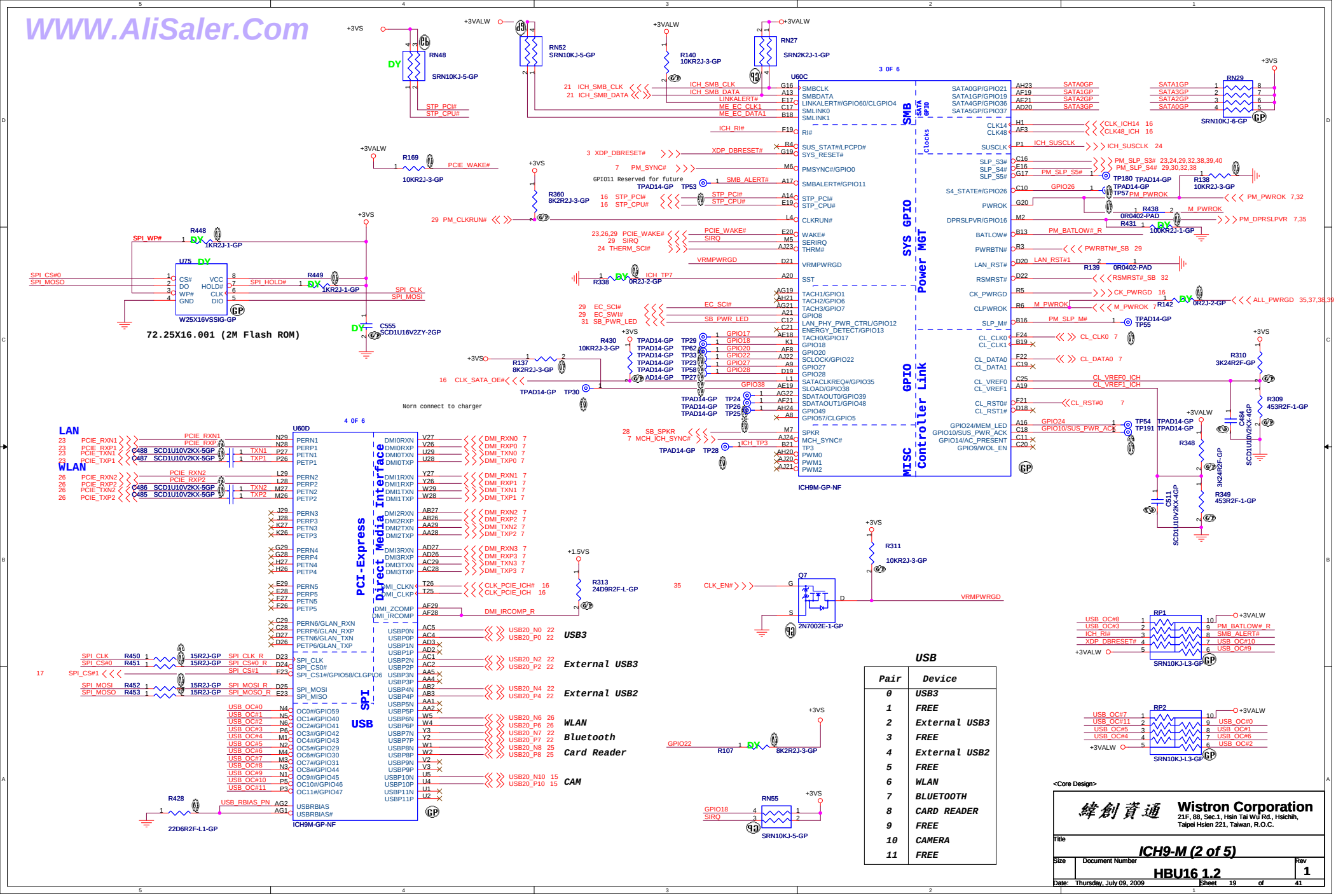
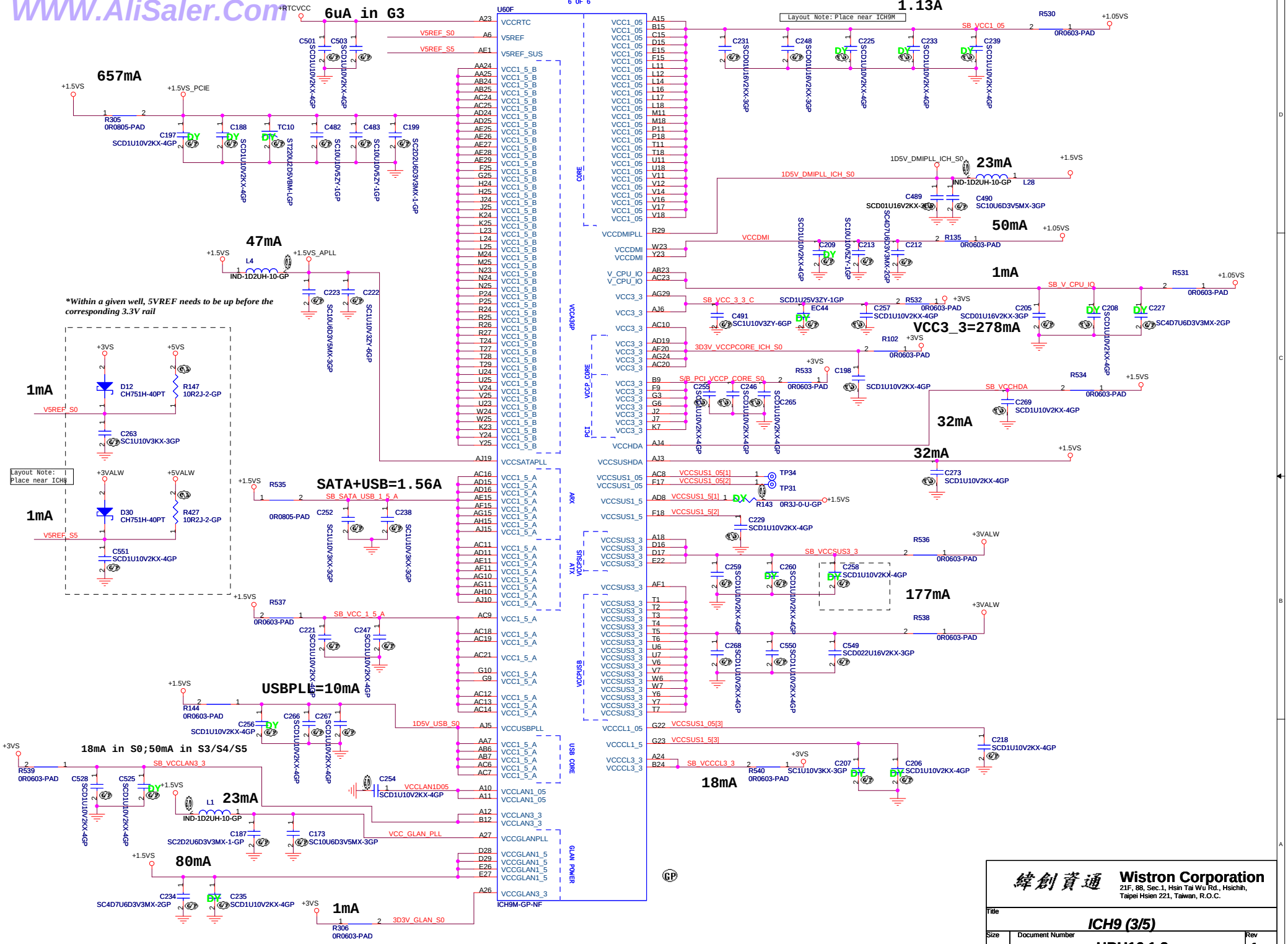
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (2 of 5)

Size	Document Number	Rev
	HBU16 1.2	1

Date: Thursday, July 09, 2009 Sheet 18 of 41

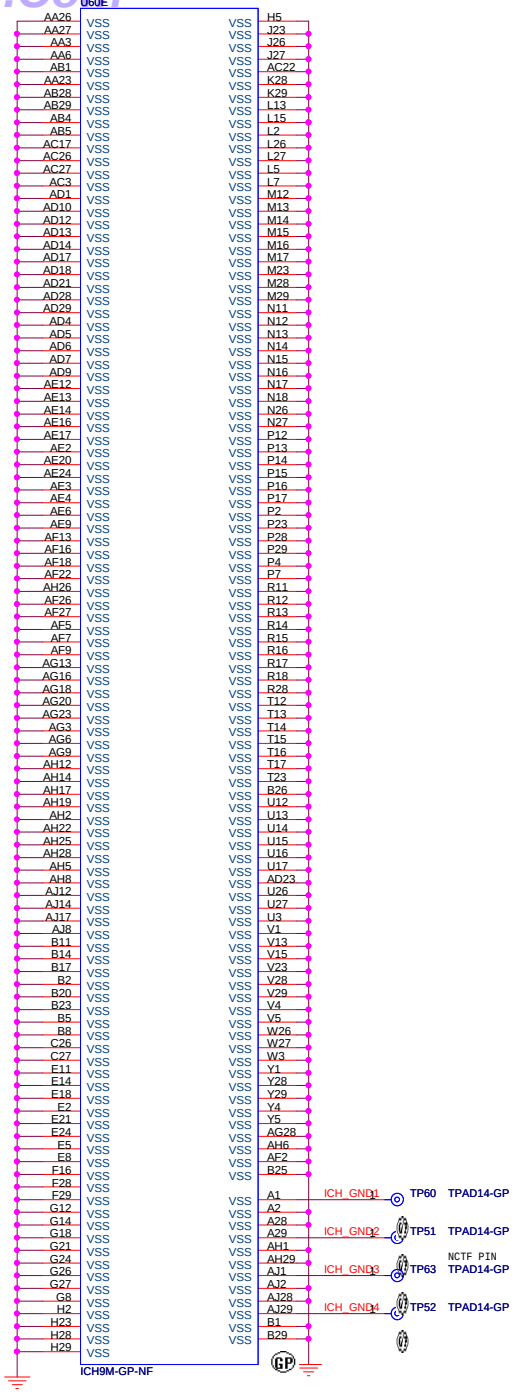


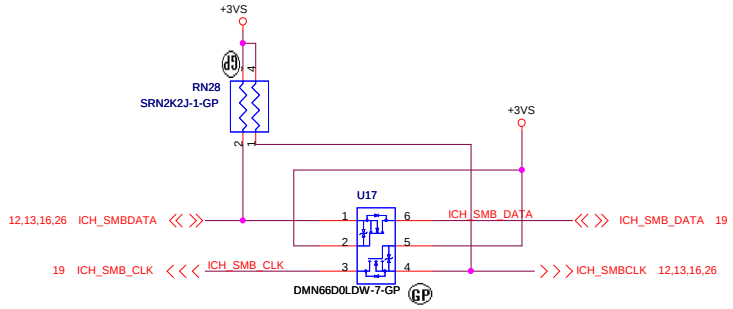


5 OF 6

U60E

ICH9M-GP-NF





SMBUS

緯創資通 **Wistron Corporation**
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Title: *ICH9-M (4 of 4)*

Size	Document Number	Rev
	HBU16 1.2	1

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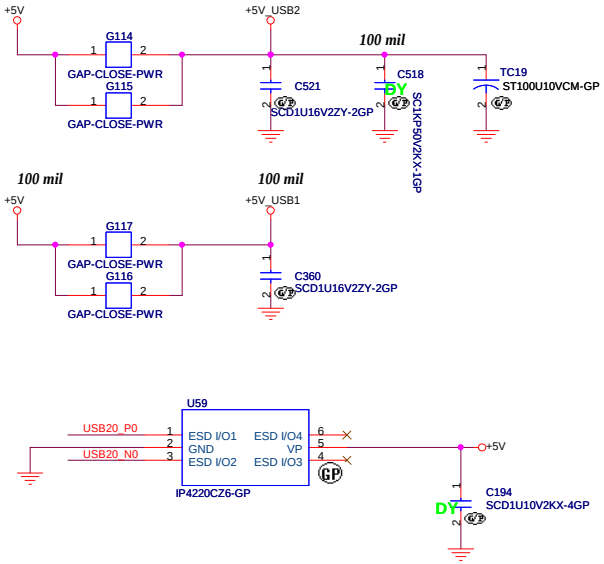
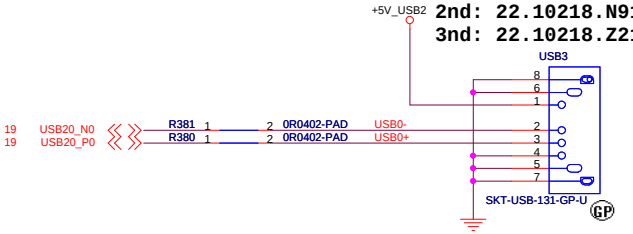
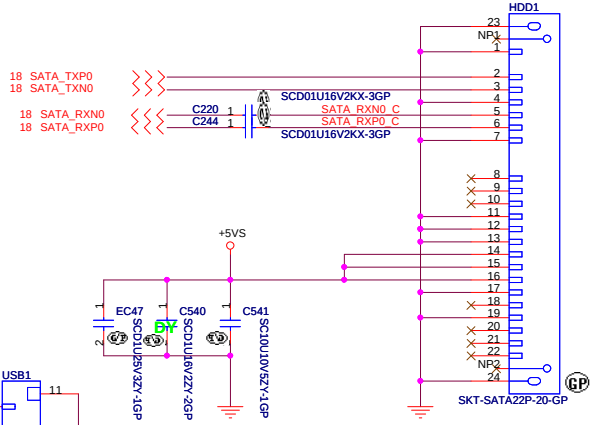
USB PORT



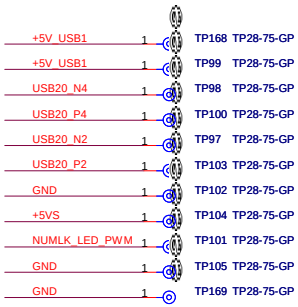
1st: 22.10218.N21
2nd: 22.10218.N91
3nd: 22.10218.Z21

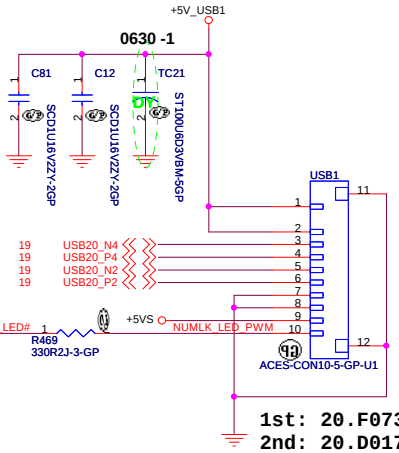


SATA HDD Connector

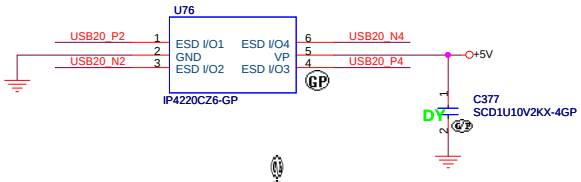


1st: 62.10065.261
2nd: 62.10065.511

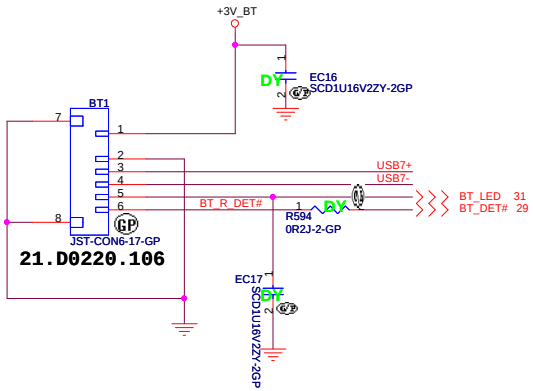


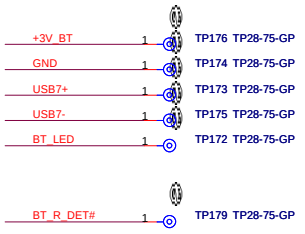


1st: 20.F0735.010
2nd: 20.D0174.110
3nd: 20.F0984.010



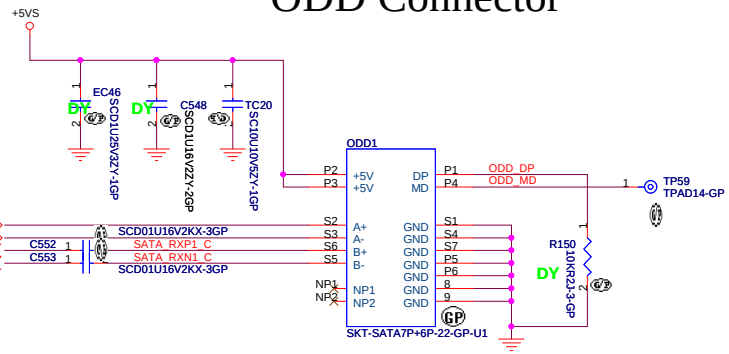
BLUETOOTH





MAX 150mA

ODD Connector



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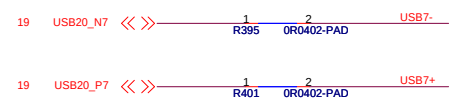
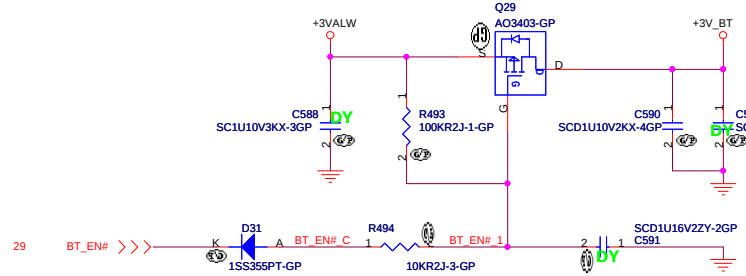
2nd: 62.10065.421
3nd: 62.10065.521





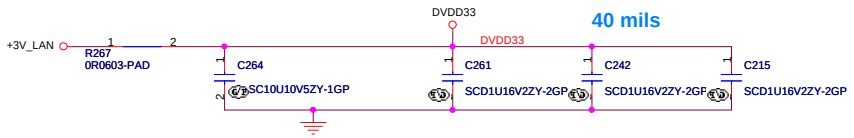
<Core Design>

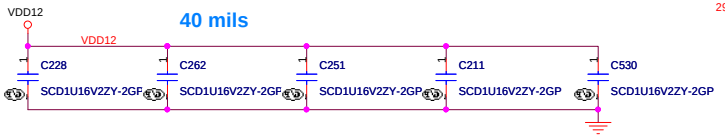
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

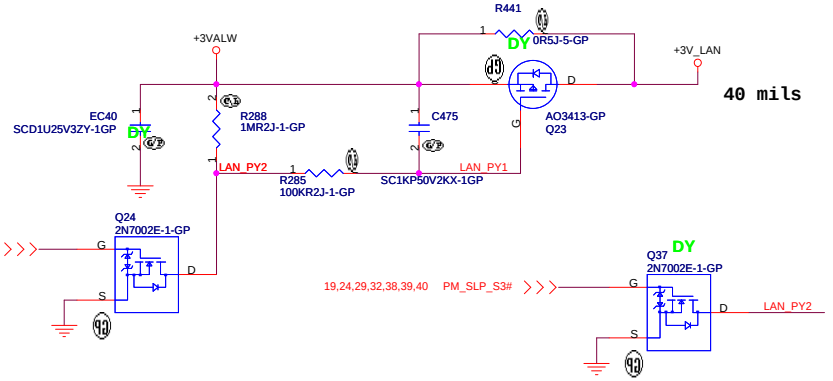
Title: HDD/CDROM/USB/BT

Size	Document Number	Rev
A3	HBU16 1.2	1

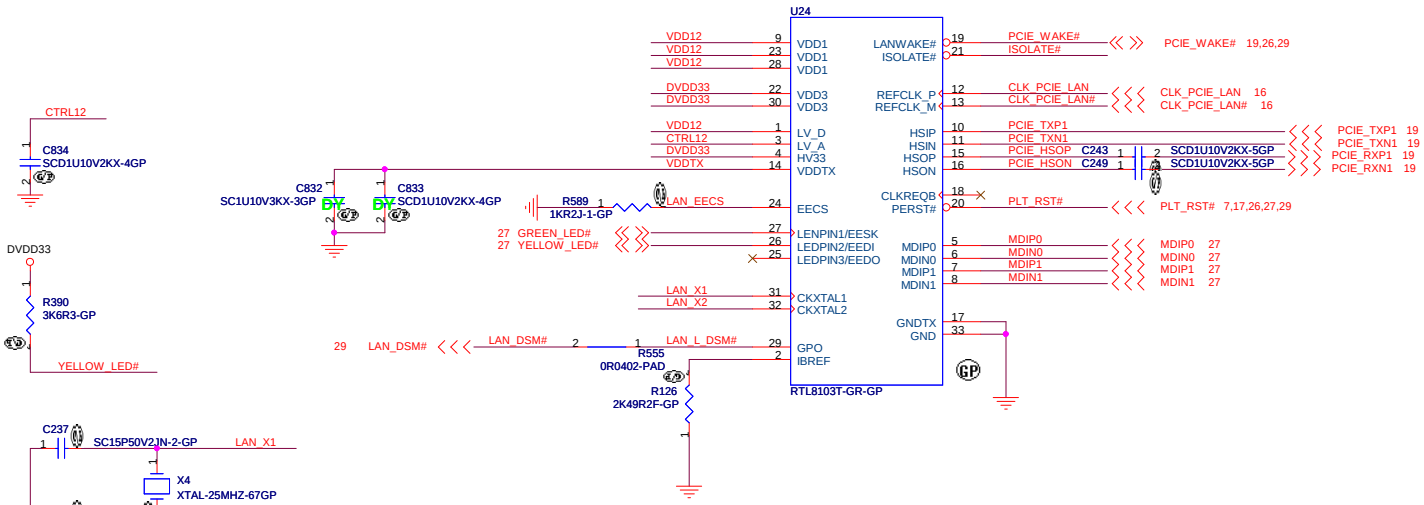
Date: Thursday, July 09, 2009 Sheet 22 of 41







EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED1 : LINK (Green)
=> LED2 : ACT (Yellow)
(BOTH 10/100 AND GIGA CHIP)



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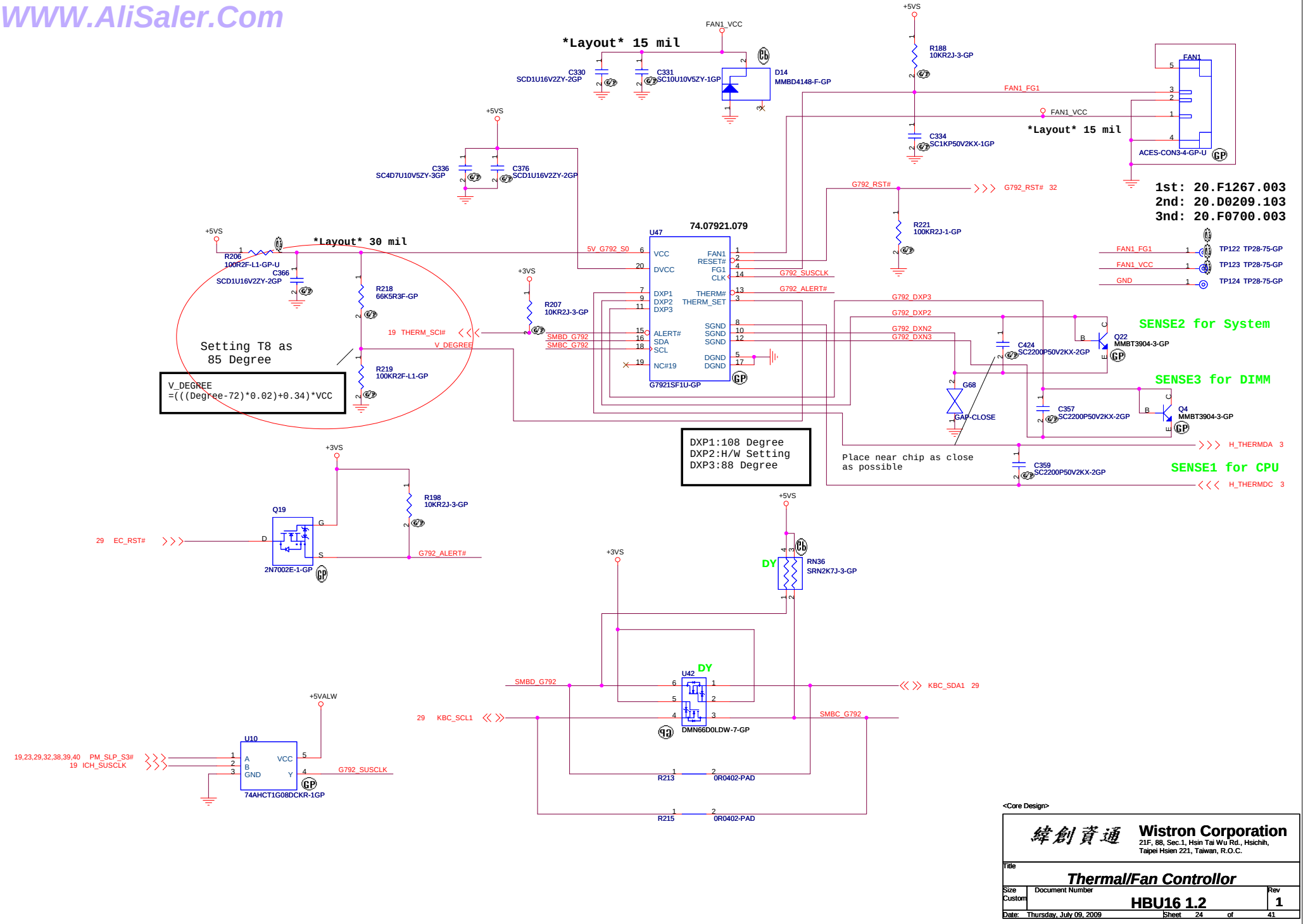
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RTL8103T***
Size: A3 / Document Number	**HBU16 1.2** / Rev: **1**
Date: Thursday, July 09, 2009	Sheet 23 of 41



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

Size	Document Number	Rev
Custom	HBU16 1.2	1

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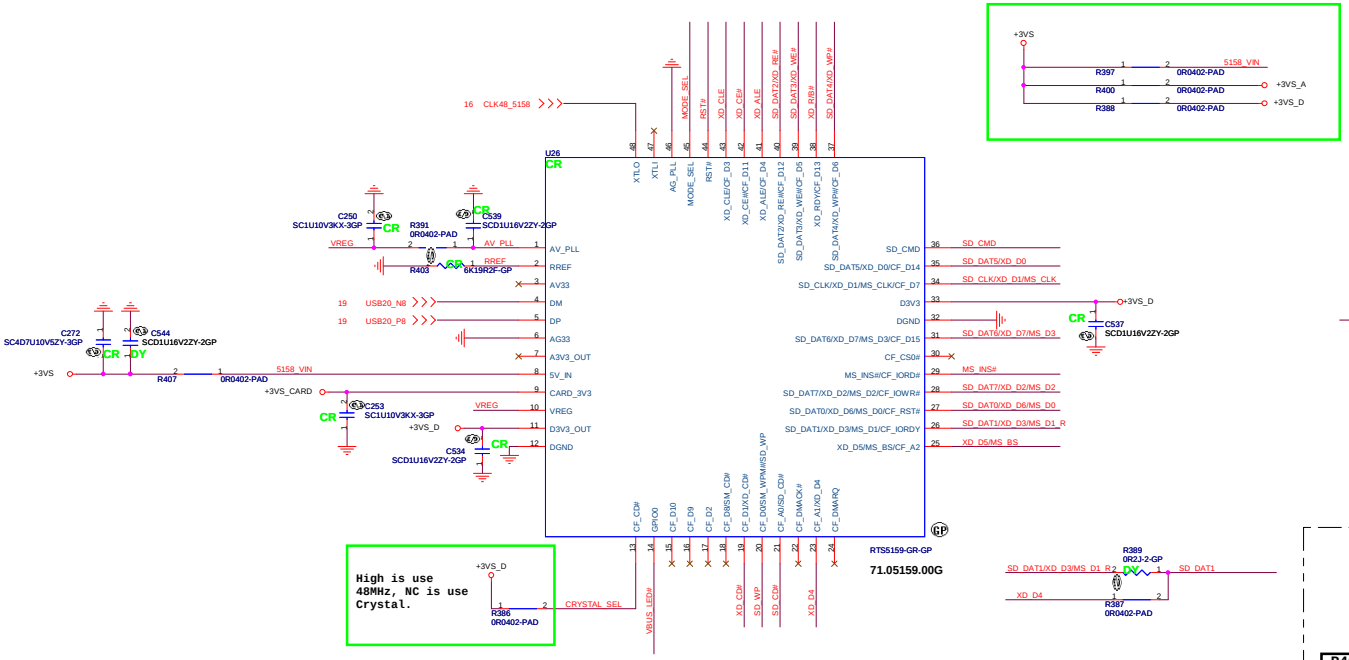
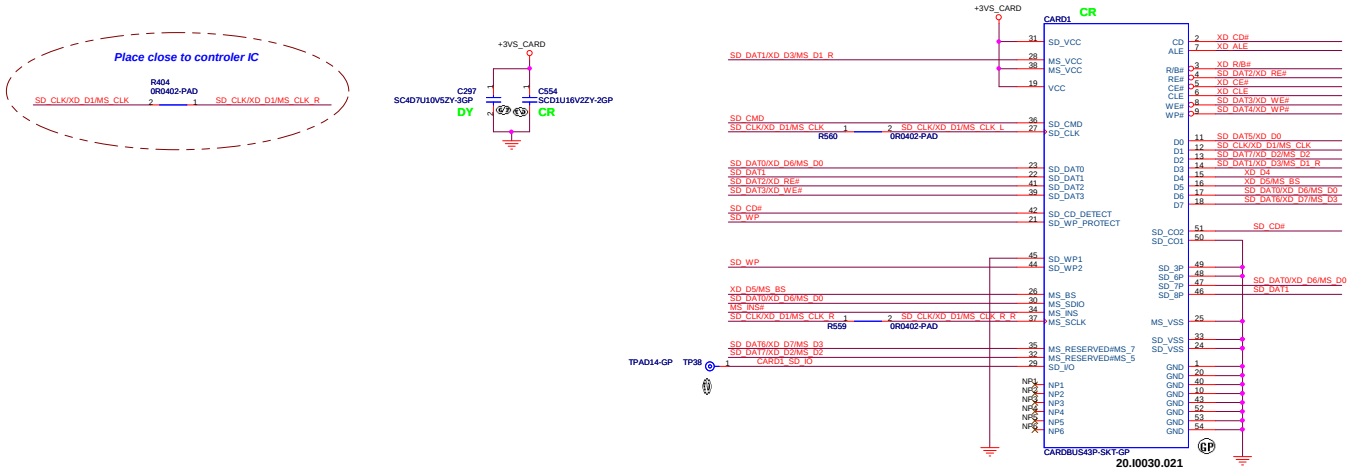


R405	C542	USB Auto De-link (*1)	MS Formatter (*2)	Description
0	NC	Yes	No	Recommended
NC	Install	Yes	Yes	
NC	NC	No	No	Compatible with RTS5158E

***1. USB Auto De-link mode:** If user remove memory card from socket, RTS5159 will terminate USB bus connection and enter power saving state.

***2. MS Formatter:** MSPRO, MSPRO DUO, MSPRO-HG or MSPRO-HG DUO card will be formatted as factory default setting if user formatted these card types under "Vista" OS.

4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



<Core Design>
緯創資通 Wistron Corporation
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Title: USB CardReader Controller-RTS5159

Size | Document Number: HBU16 1.2 | Rev: 1

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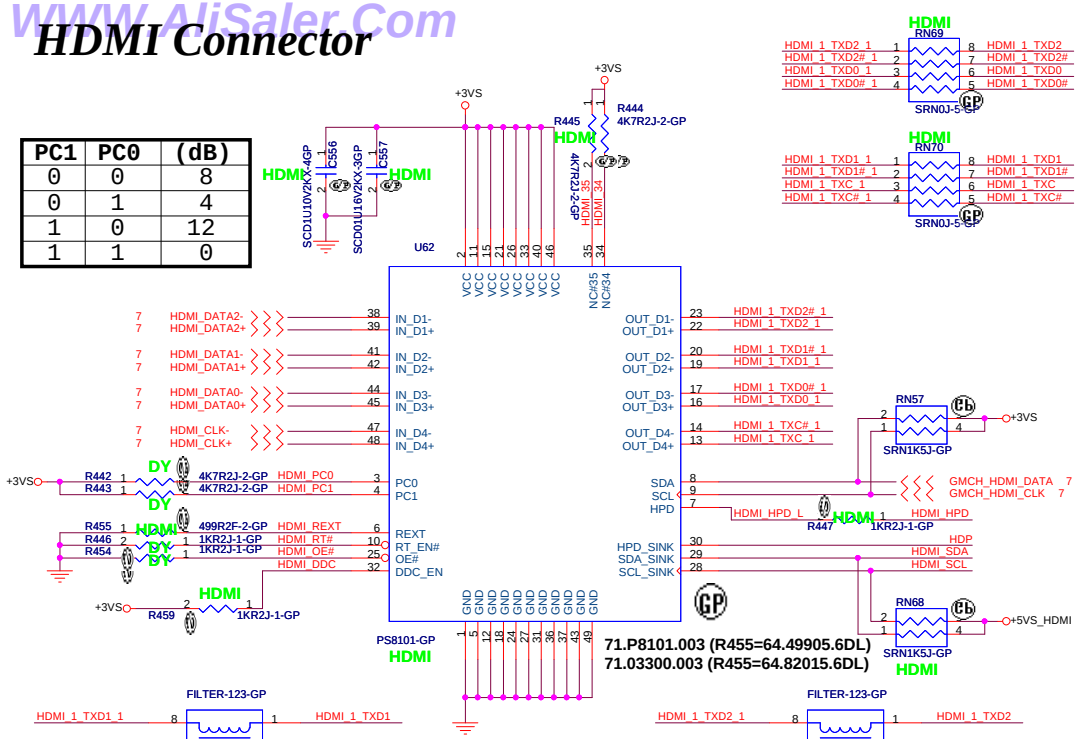
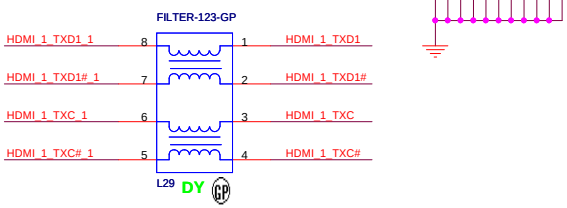
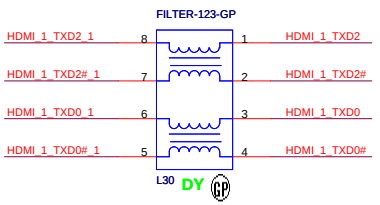
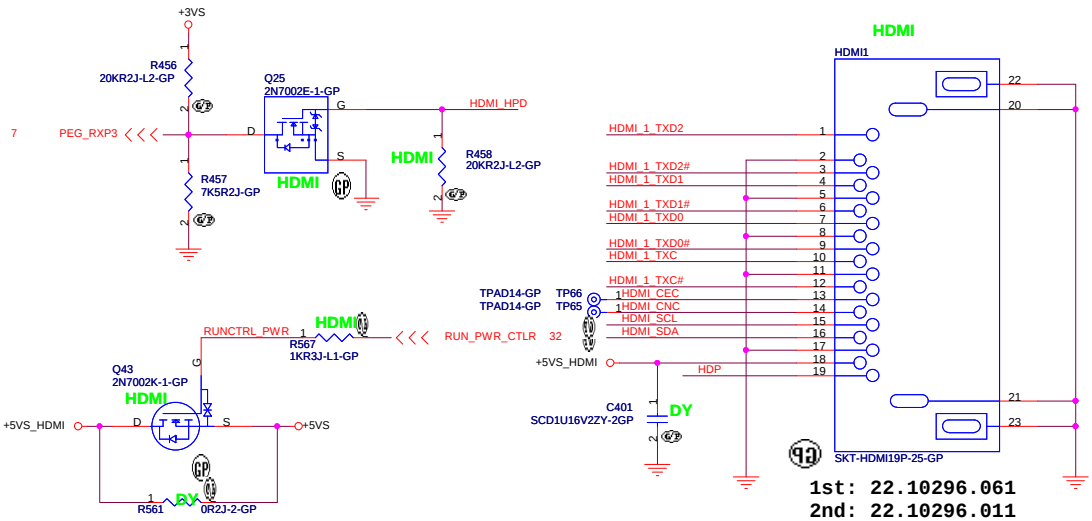
HDMI Connector

PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0

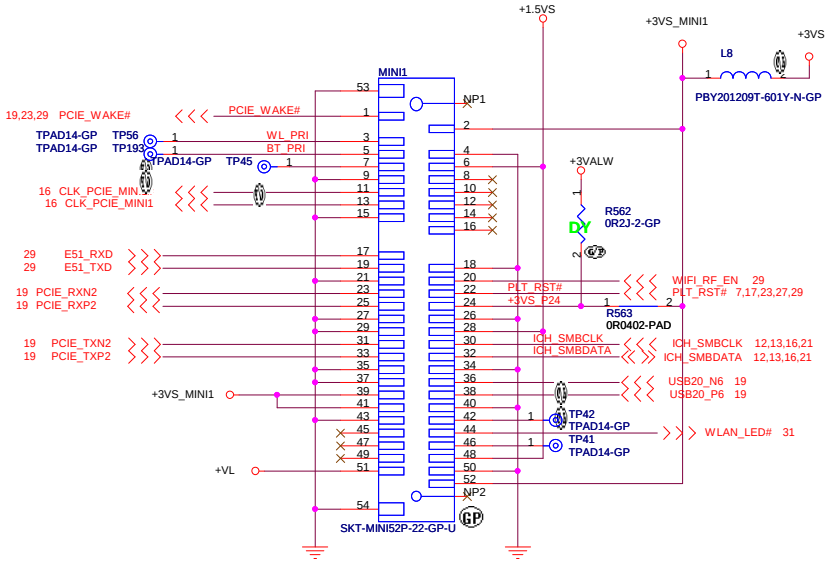


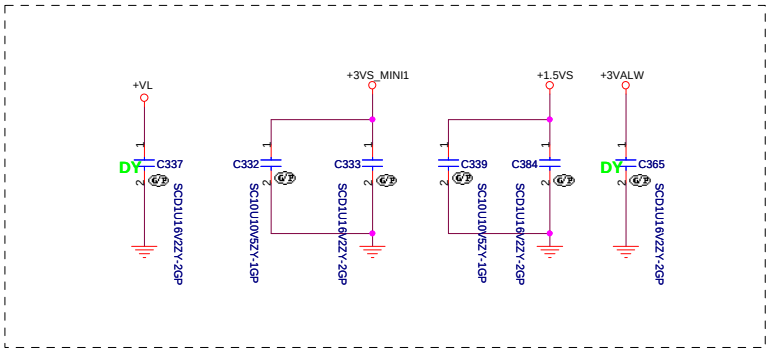






Mini Card Connector1(802.11a/b/g)





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: MINI CARD/HDMI CONN .

Size	Document Number	Rev
A3	HBU16 1.2	1

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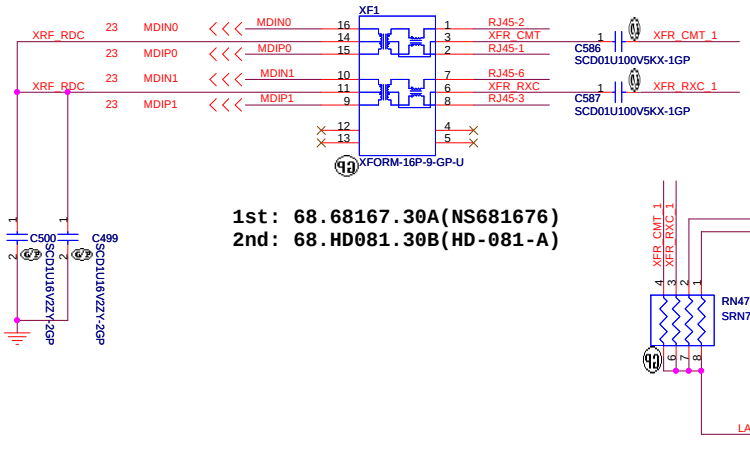
LAN Connector

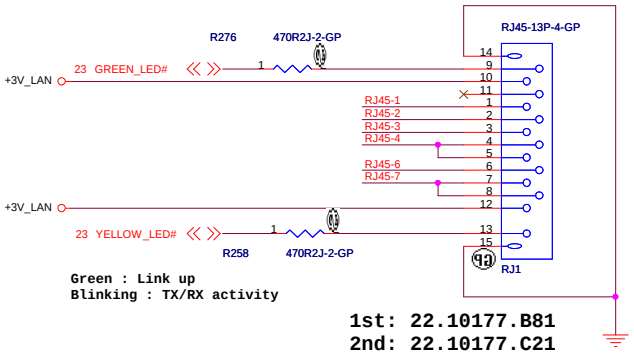
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW

10/100M Lan Transformer



1st: 68.68167.30A(NS681676)
2nd: 68.HD081.30B(HD-081-A)



Green : Link up
Blinking : TX/RX activity

1st: 22.10177.B81
2nd: 22.10177.C21

Remark:
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

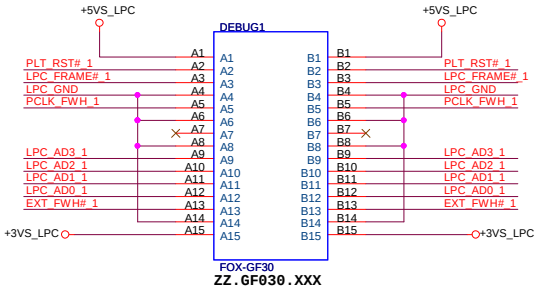
Golden Finger for Debug Board

TOP VIEW (A)

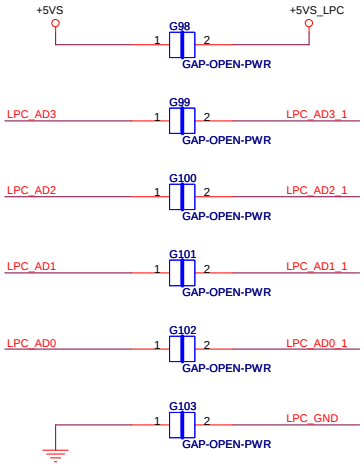
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)

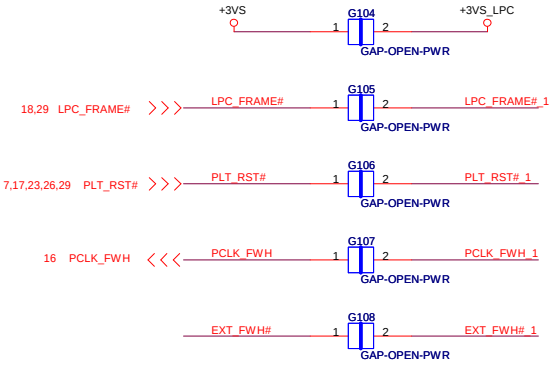
BOTTOM VIEW (B)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

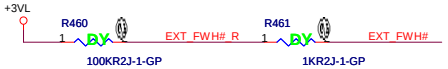


Please put near board edge.





LPC_AD[0..3] 18,29



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN/Debug
Size: A3
Document Number: HBU16 1.2
Rev: 1
Date: Thursday, July 09, 2009
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CLOSE TO TRANSFORMER

PC BEEP GAIN CONTROL

GAIN	R568
-46 dB	DY
-18 dB	Install

SPDIF/BEEPGAIN is an input used to set the PC Beep gain while the device is in reset.

Default gain is -46 dB without populating the 10-Kohm pull-up resistor.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5VS_AUD to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

2.5A (100mils)

Note:
In order for the audio codec to Wake on Jack, the CODEC VAUX pin (VAUX_3.3, pin2&6) must be powered by a rail that is not removed unless AC power is removed.

Close to Modem

Close to U32.

Close to U32.

Close to SPKR1.

0703 -1

0630 -1

0709 -1

1st: 83.R2003.E81
2nd: 83.BAT54.081
3nd: 83.00054.Q81

1st: 20.K0320.015
2nd: 20.K0343.015

Speaker

1st: 20.D0197.104
2nd: 20.F0984.004
3nd: 20.D0209.104

MIC

1st: 20.D0197.104
2nd: 20.F0984.004
3nd: 20.F0689.004

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC CX20583-11Z

Size: Custom | Document Number: HBU16 1.2 | Rev: 1

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CAP close to VCC-GND pin pair

CAP near ADC

TP near KB connector

32.768Khz 12.5pf 10ppm
1st: 82.30001.691 (KDS)
2nd: 82.30001.861 (EPSON)

2 GND connect at one point

Planar ID[2,1,0]
SA: 0,0,0
SB: 0,1,0
SC: 0,1,0
-1: 0,1,0

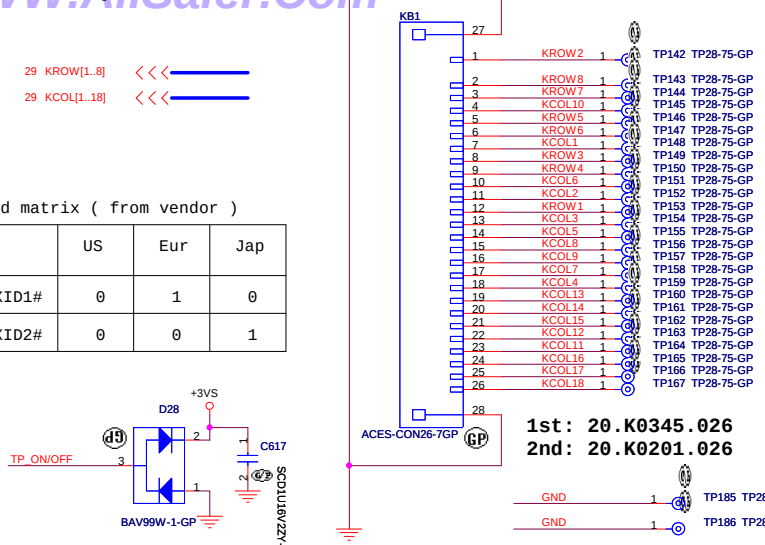
Core Design	緯創資通 Wistron Corporation, 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC WPCE773L
Size	A3
Document Number	HBU16 1.2
Rev	1
Date	Thursday, July 09, 2009
Sheet	29 of 41

Internal KeyBoard Connector

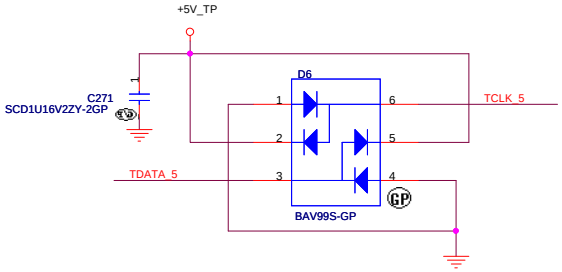
29 KROW[1..8]
29 KCOL[1..18]

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

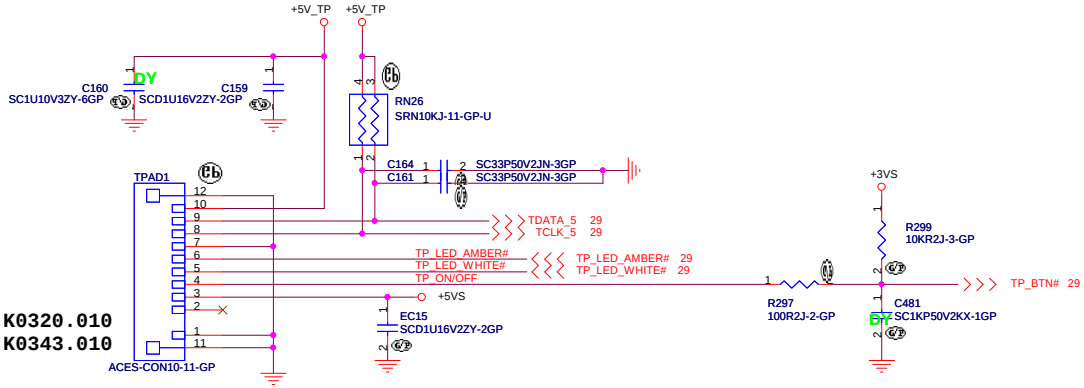


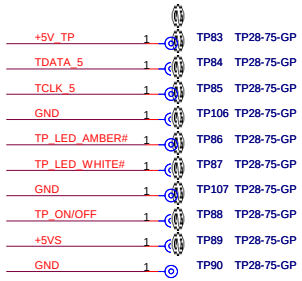
1st: 20.K0345.026
2nd: 20.K0201.026



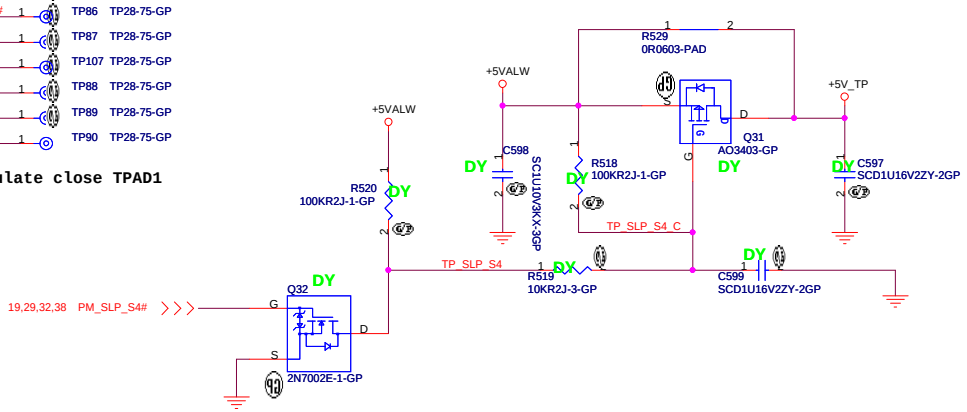
TouchPad Connector

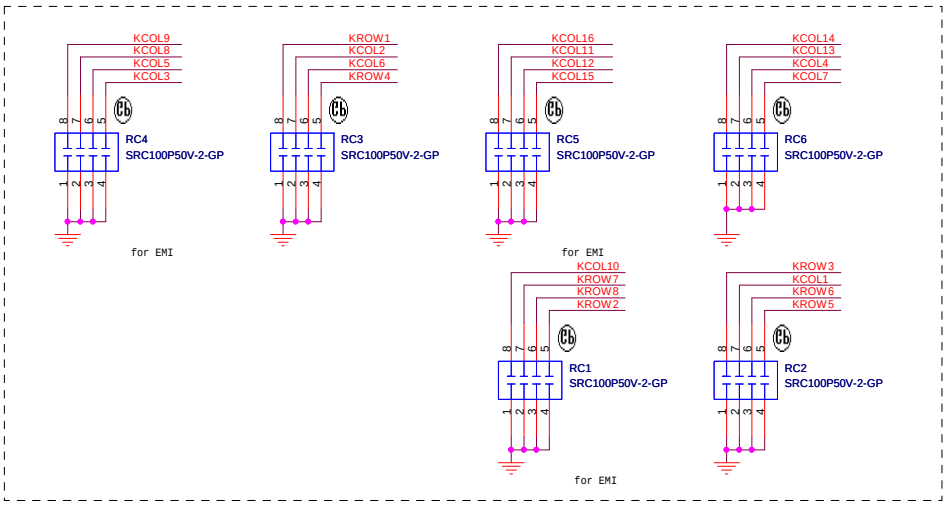
1st: 20.K0320.010
2nd: 20.K0343.010





Please populate close TPAD1





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: KeyBoard-CONN
Size: A3
Document Number: HBU16 1.2
Rev: 1
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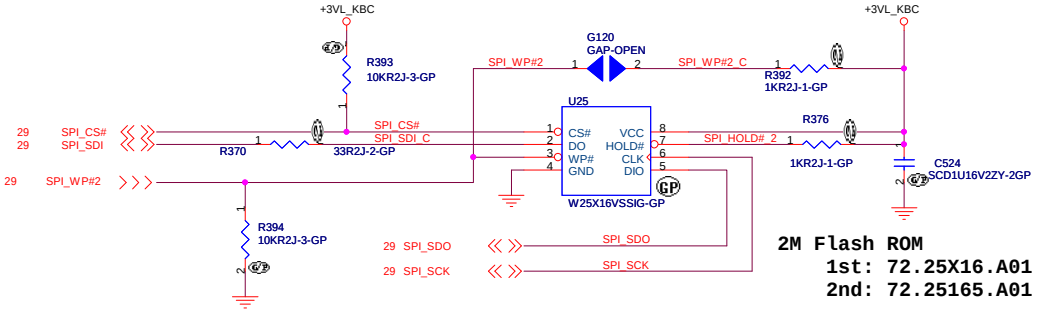

2M Flash ROM
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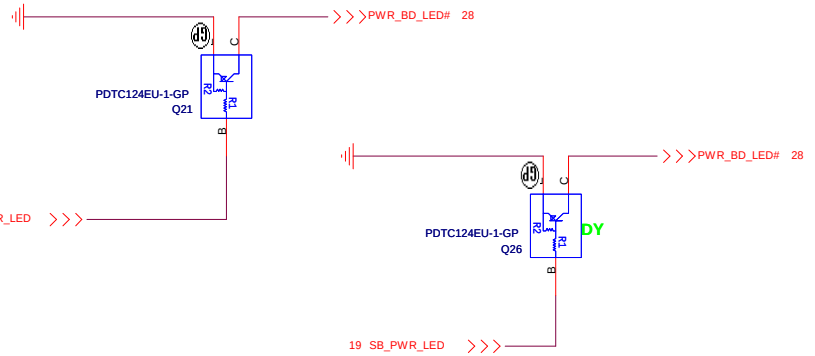
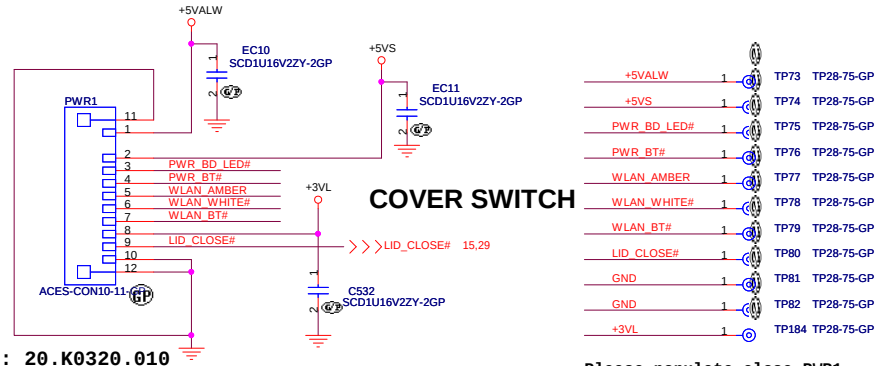
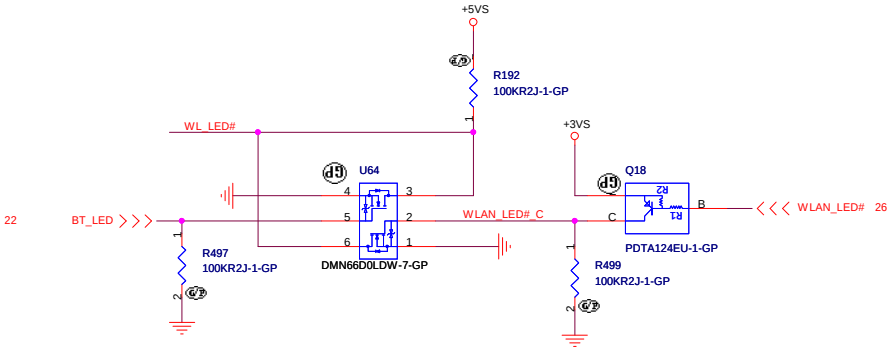




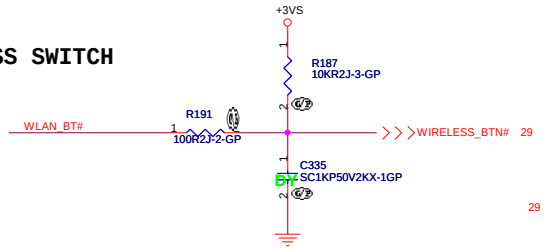
COVER SWITCH

1st: 20.K0320.010
2nd: 20.K0343.010

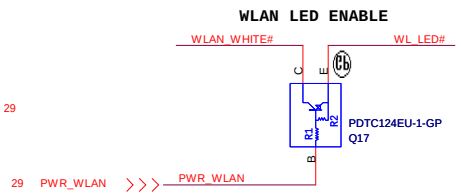
Please populate close PWR1



WIRELESS SWITCH



WLAN LED ENABLE



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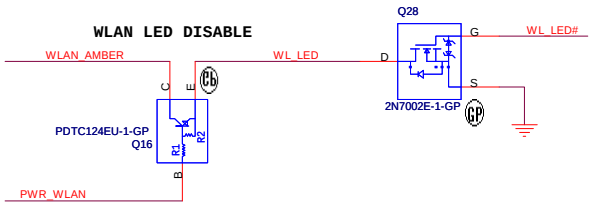
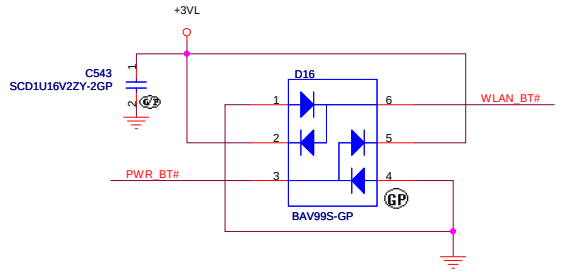
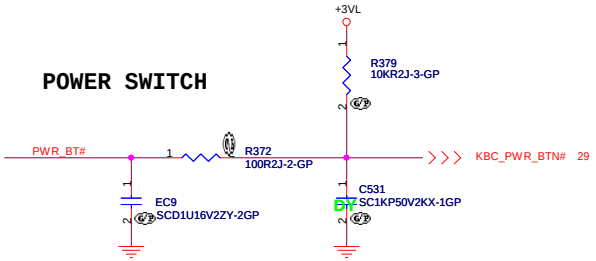




POWER SWITCH



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Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH and CONN.

Size: A3 | Document Number: HBU16 1.2 | Rev: 1

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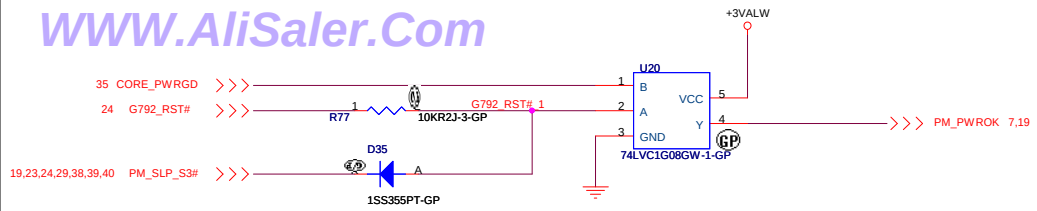
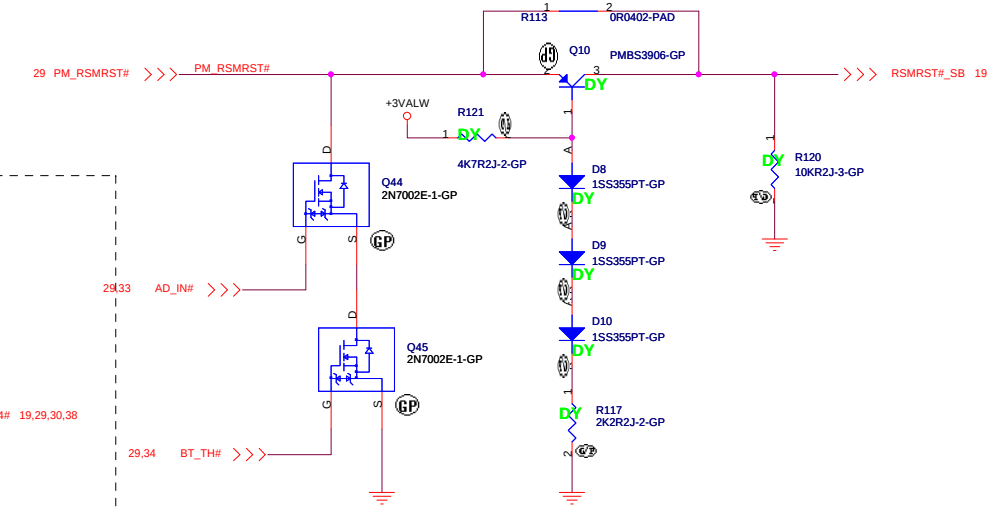
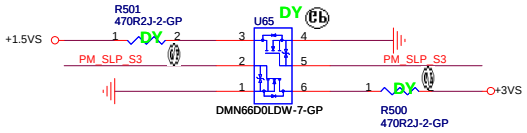
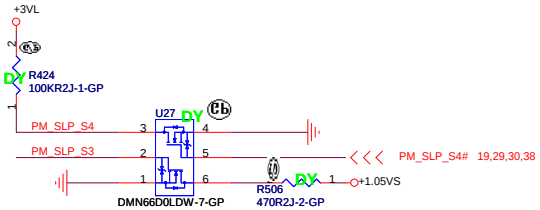


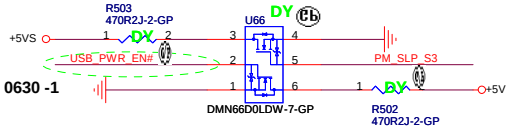


0523 SF

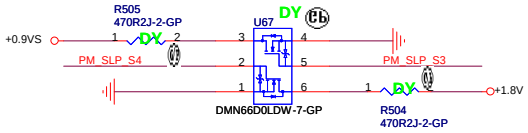
Discharge Circuit





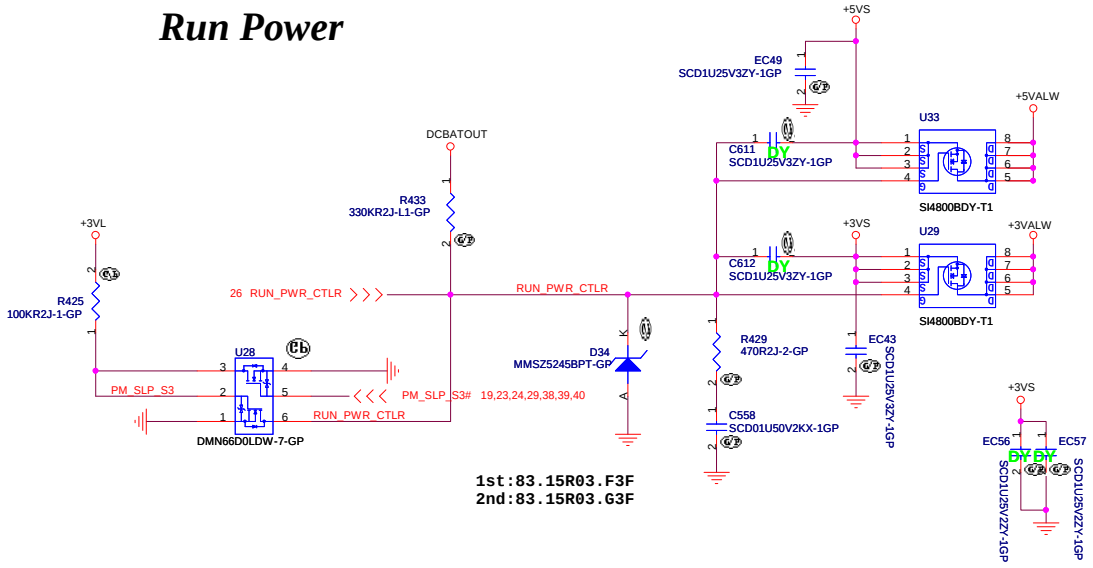


0630 -1



+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

Run Power



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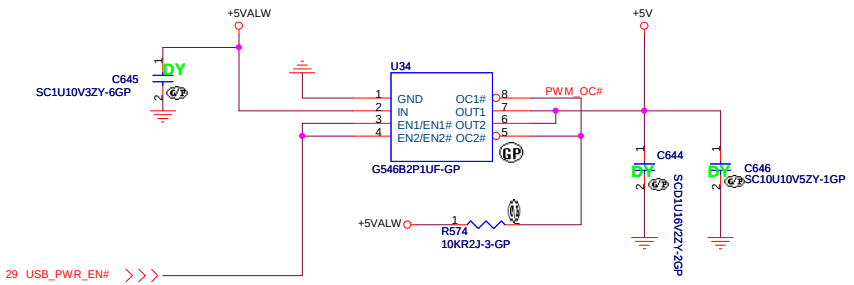
+5VALW to +5V Transfer

G546B2P1 Low active, 1.5A per channel



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWRPLANE		
Size: A3	Document Number: HBU16 1.2	Rev: 1
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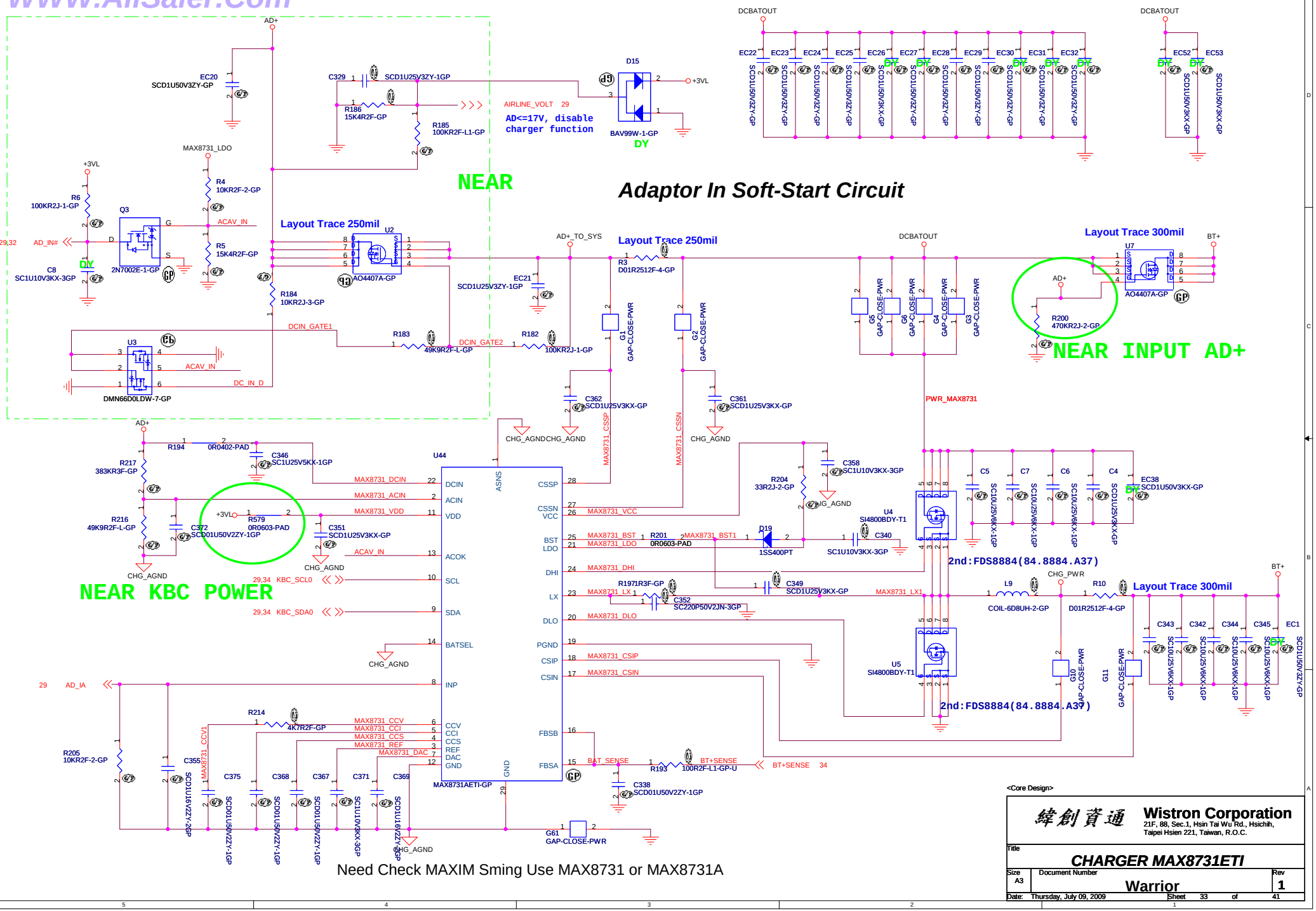
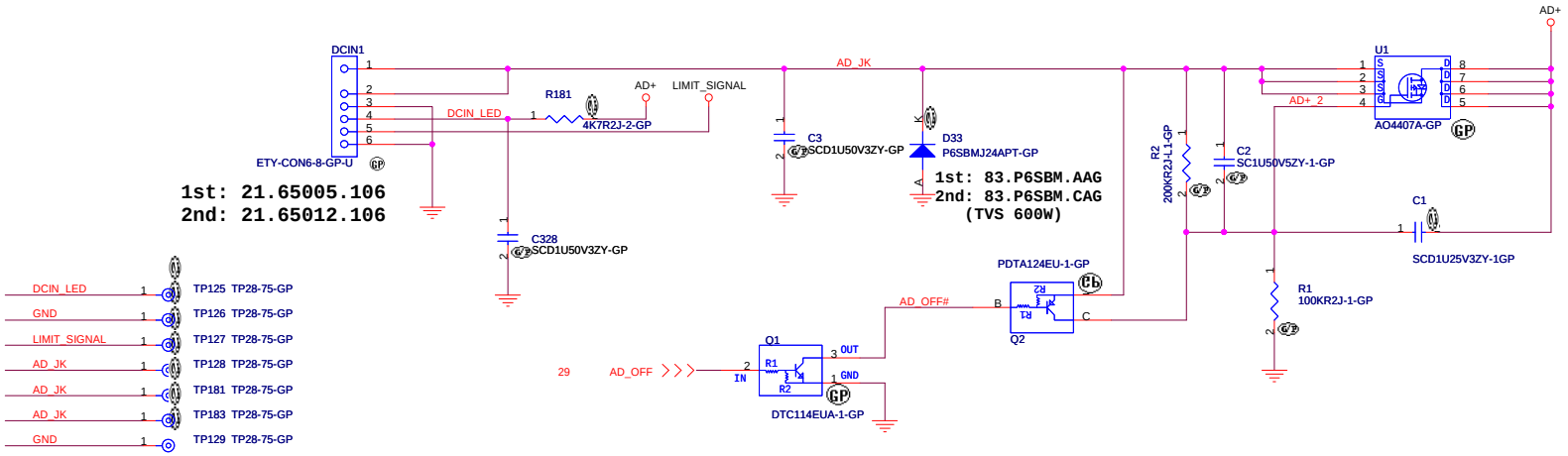
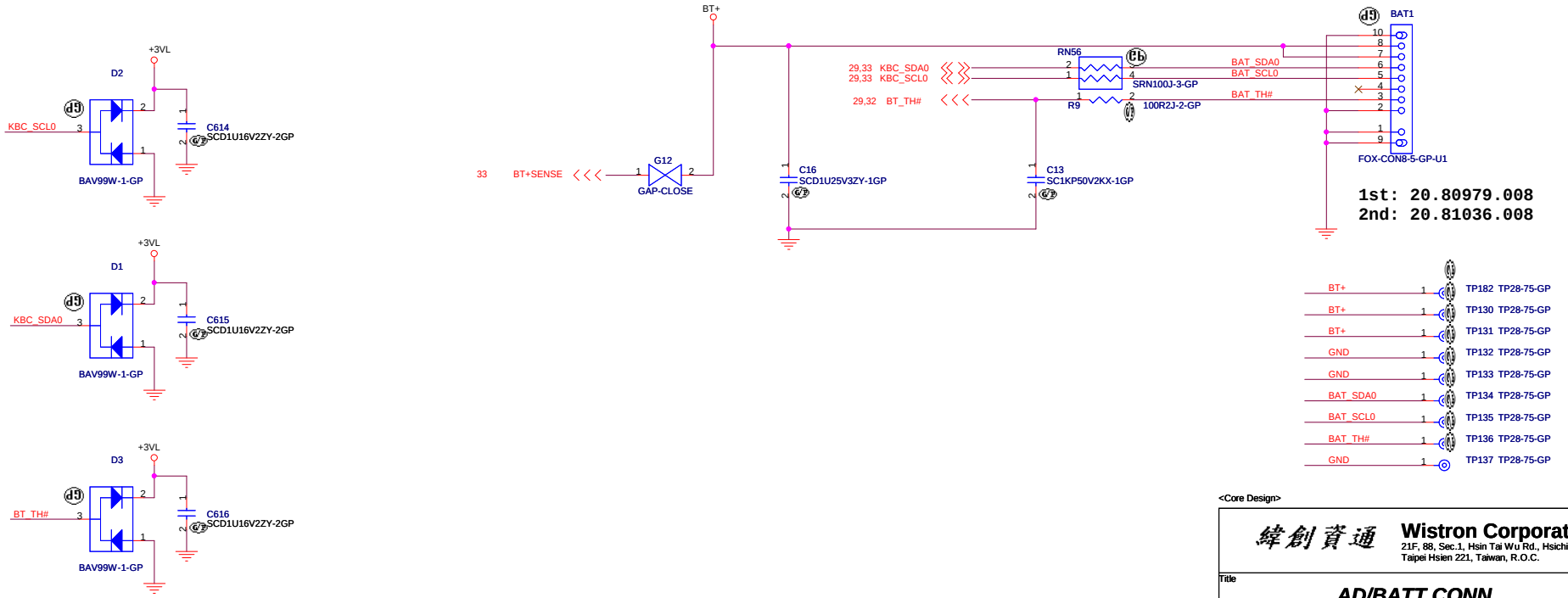


Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
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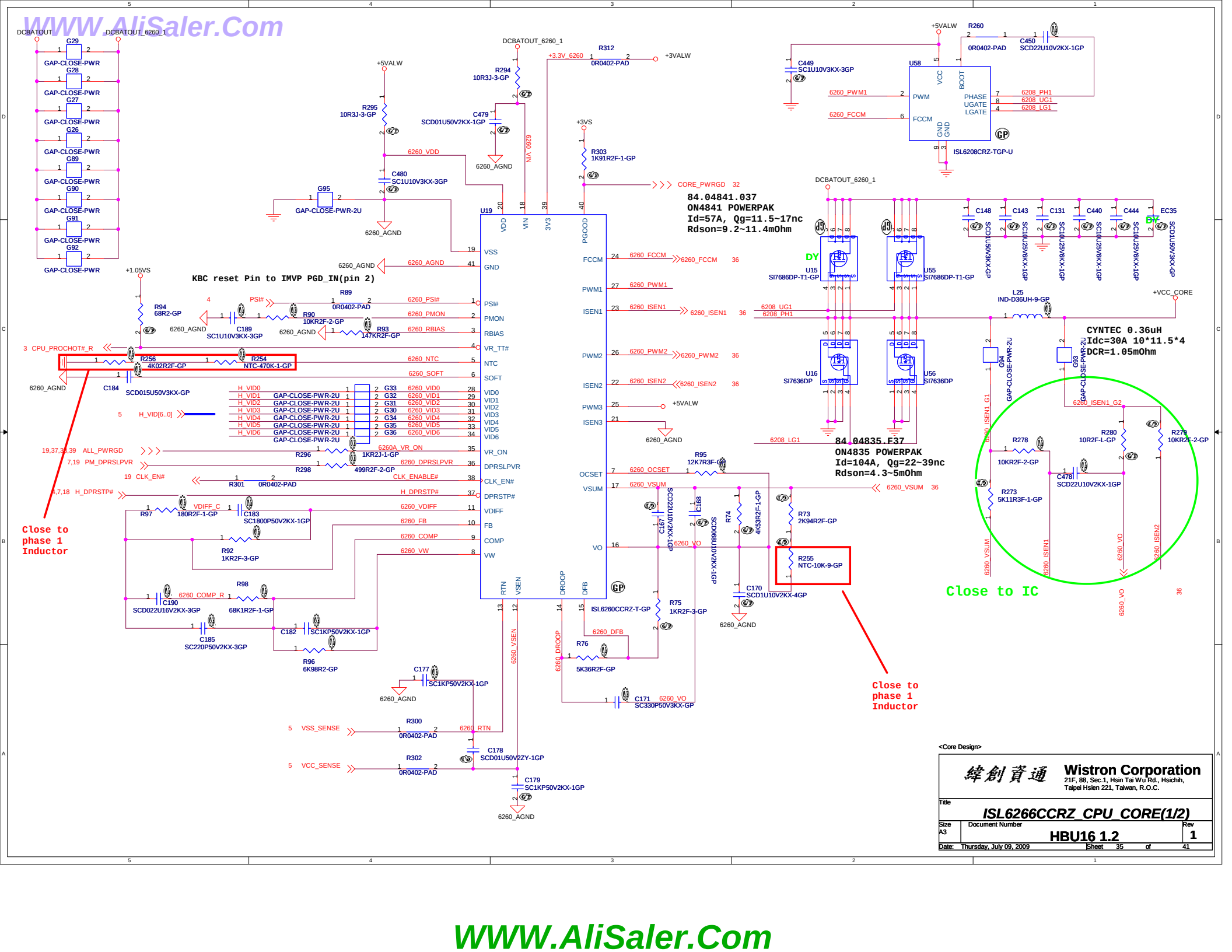
Date: Thursday, July 09, 2009 Sheet 34 of 41



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6266CCRZ_CPU_CORE(1/2)

Size	Document Number	Rev
A3	HBU16 1.2	1

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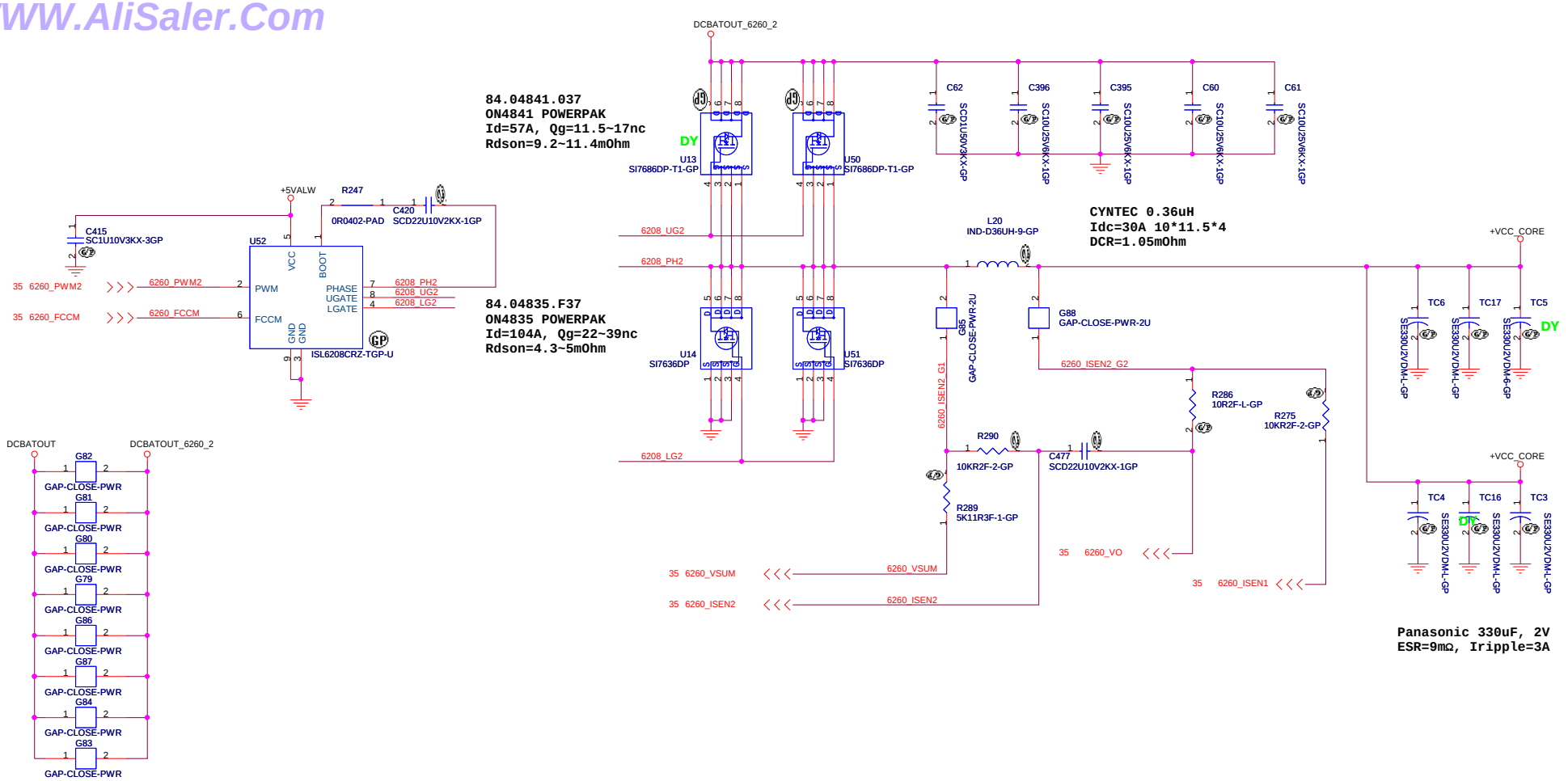

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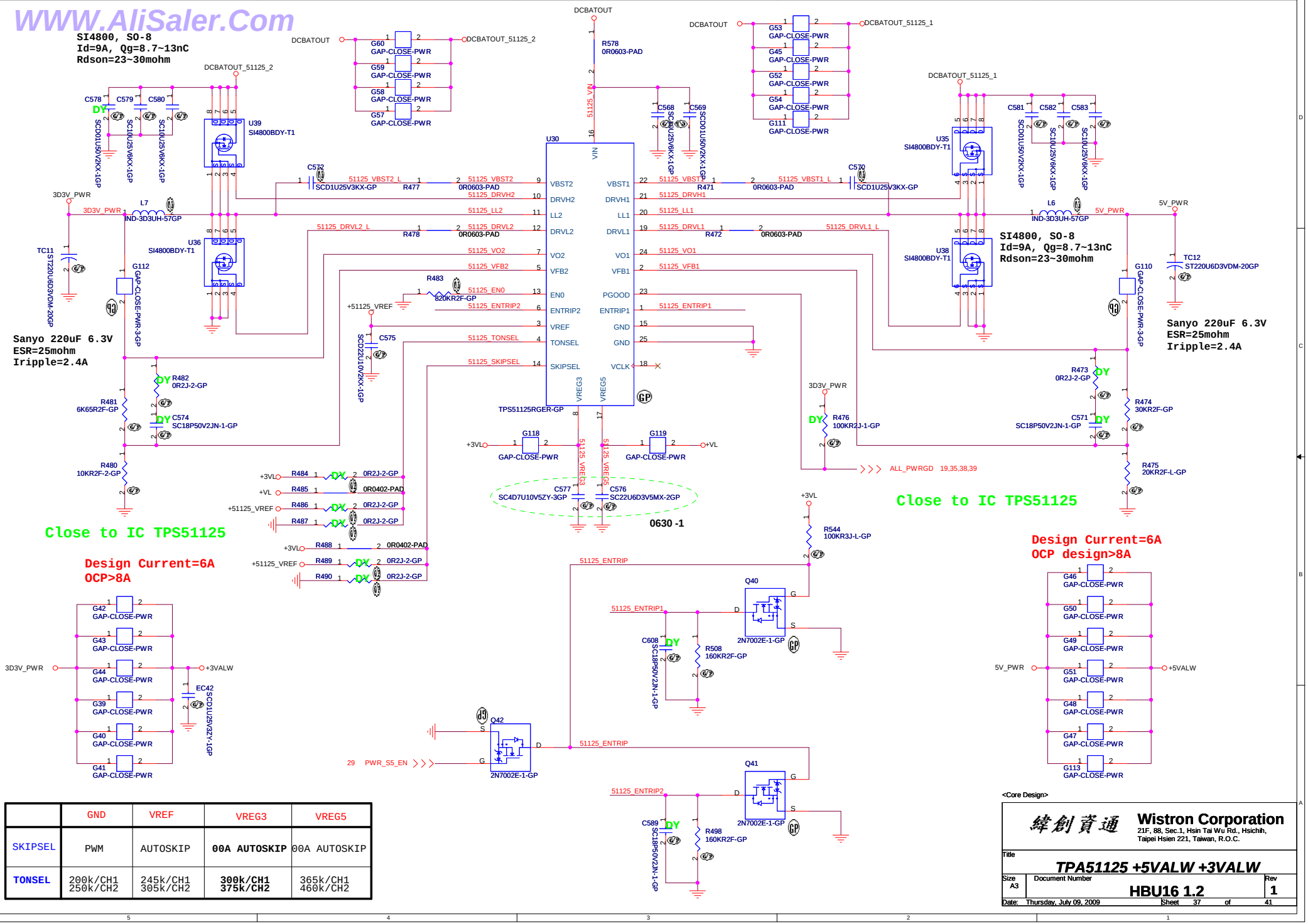
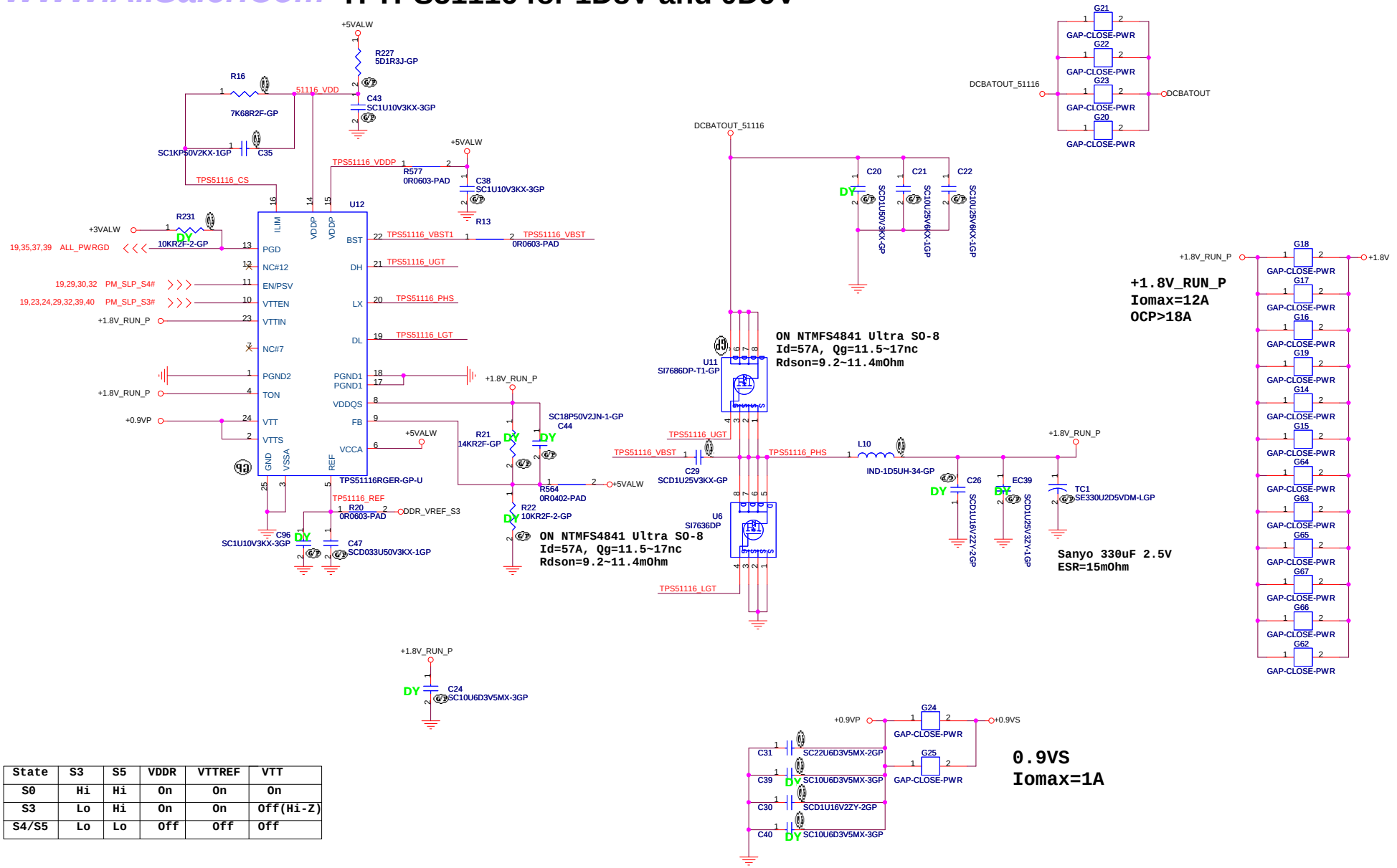
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*ISL6260CCRZ_CPU_CORE(2/2)*
Size: A3	Document Number: HBU16 1.2
Rev: 1	
Date: Thursday, July 09, 2009	Sheet 36 of 41



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	**00A AUTOSKIP**	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	**300k/CH1** **375k/CH2**	365k/CH1 460k/CH2

TI TPS51116 for 1D8V and 0D9V



ON NTMFS4841 Ultra SO-8
Id=57A, Qg=11.5~17nc
Rdson=9.2~11.4mOhm

ON NTMFS4841 Ultra SO-8
Id=57A, Qg=11.5~17nc
Rdson=9.2~11.4mOhm

+1.8V_RUN_P
Iomax=12A
OCP>18A

Sanyo 330uF 2.5V
ESR=15mOhm

0.9VS
Iomax=1A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: HBU16 1.2 | Rev: 1

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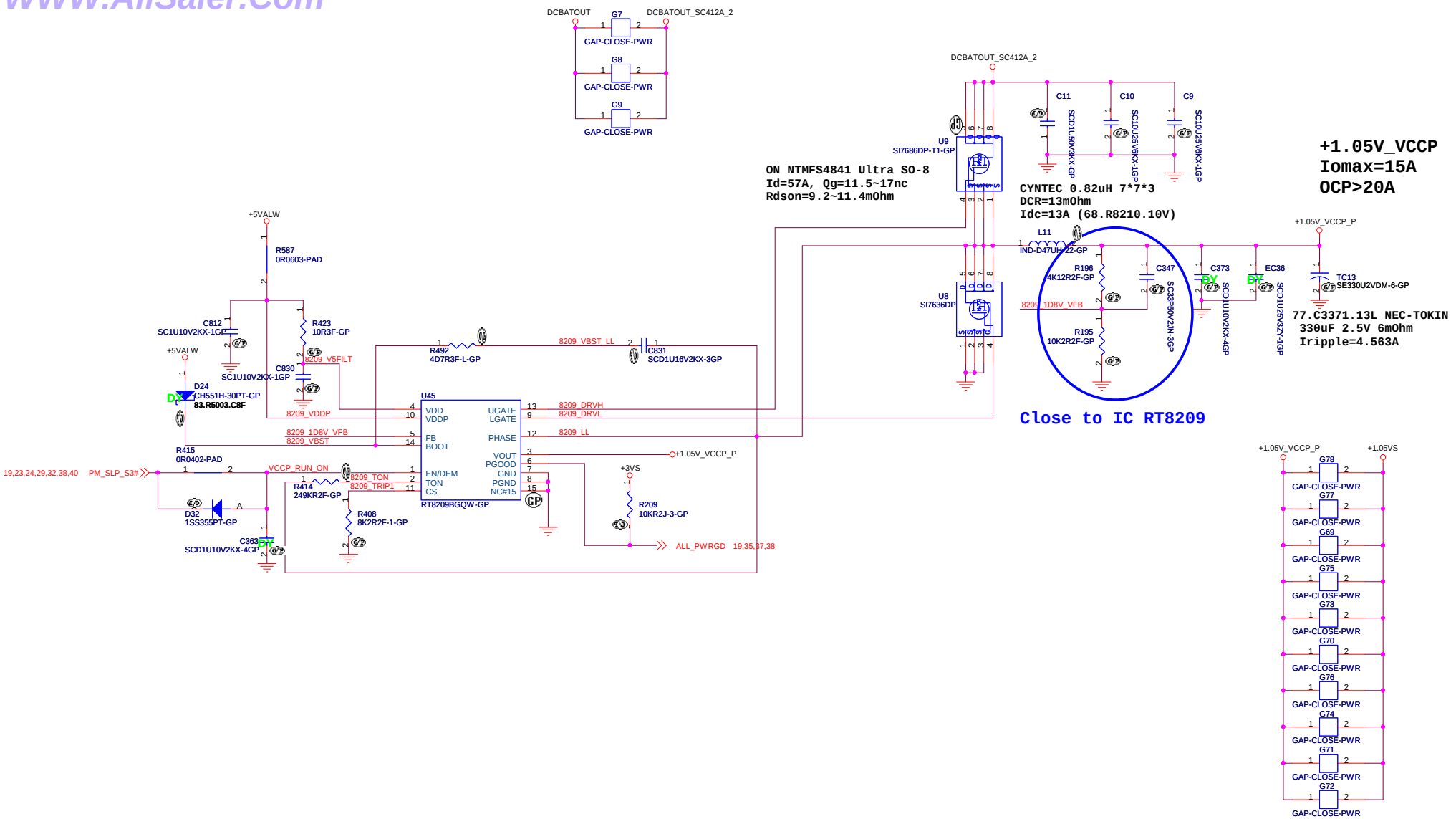

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Title	RT8209 +1.05VS	
Size A3	Document Number HBU16 1.2	Rev 1
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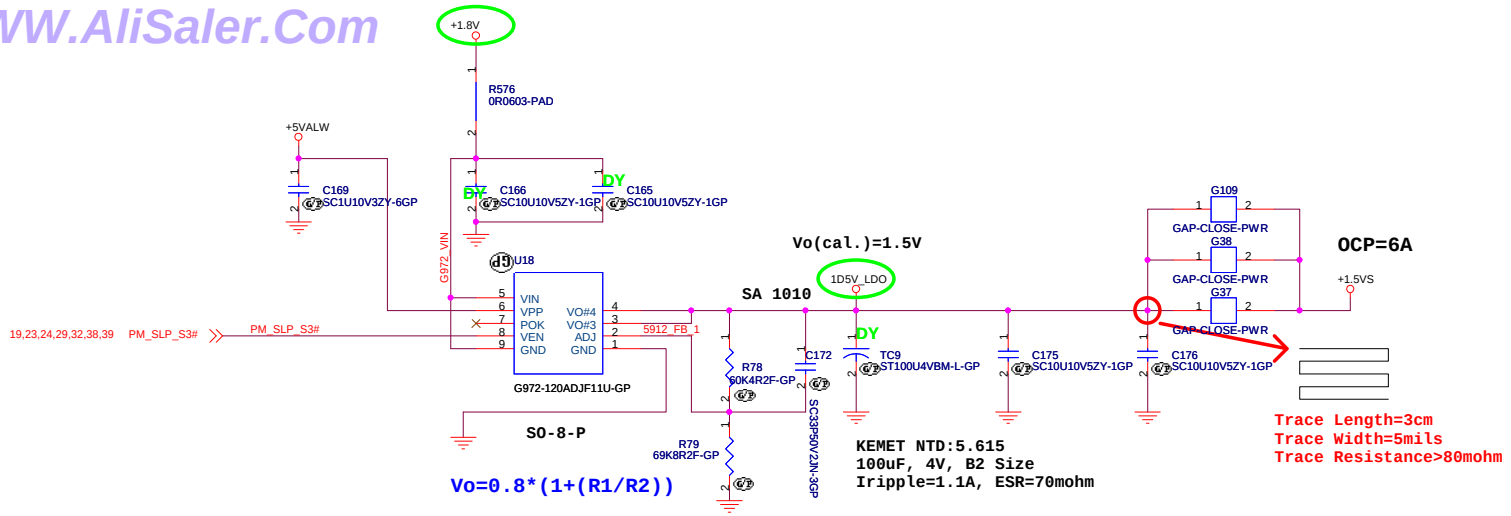

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2nd: 74.05912.A71(Anpac)

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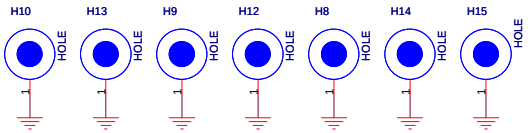
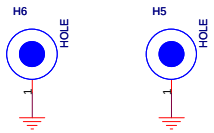
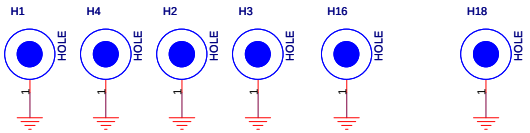
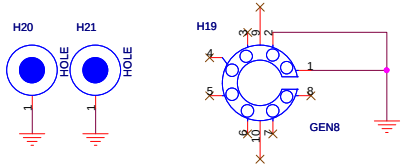
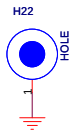
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GMT_1D5V_LDO		
Size: A3	Document Number: HBU16 1.2	Rev: 1
Date: Thursday, July 09, 2009	Sheet 40 of 41	

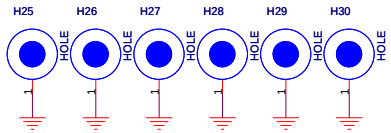


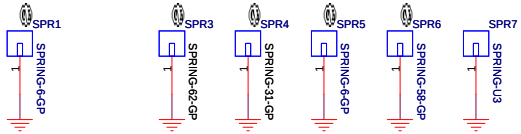












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SPR6: 34.4B312.002, 34.4B312.101
SPR7: 34.40U07.001, 34.40U07.101

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Title: ***MISC***

Size	Document Number	Rev
A3	HBU16 1.2	1

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