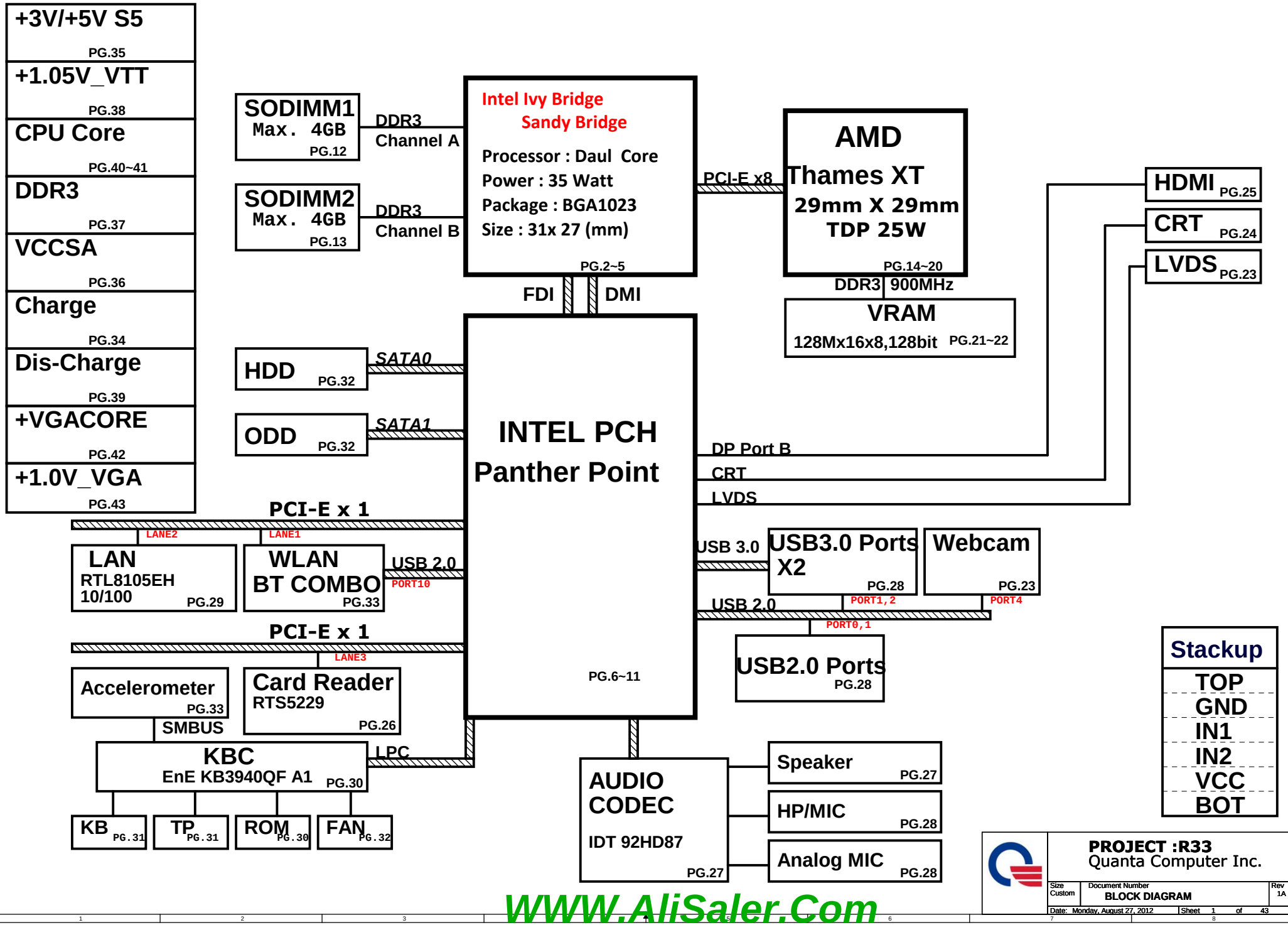
R33 INTEL UMA/DISCRETE SYSTEM DIAGRAM 01



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Quanta Computer Inc.

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Custom	BLOCK DIAGRAM	1A

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Ivy Bridge Processor (DMI,PEG,FDI)

PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

U7022A

DMI_TXN0 M2 DMI_RX#[0]
DMI_TXN1 P6 DMI_RX#[1]
DMI_TXN2 P1 DMI_RX#[2]
DMI_TXN3 P10 DMI_RX#[3]
DMI_TXP0 N3 DMI_RX[0]
DMI_TXP1 P7 DMI_RX[1]
DMI_TXP2 P3 DMI_RX[2]
DMI_TXP3 P11 DMI_RX[3]
DMI_RXN0 K1 DMI_TX#[0]
DMI_RXN1 M8 DMI_TX#[1]
DMI_RXN2 N4 DMI_TX#[2]
DMI_RXN3 R2 DMI_TX#[3]
DMI_RXP0 K3 DMI_TX[0]
DMI_RXP1 M7 DMI_TX[1]
DMI_RXP2 P4 DMI_TX[2]
DMI_RXP3 T3 DMI_TX[3]

DMI

FDI_TXN0 U7 FDI0_TX#[0]
FDI_TXN1 W11 FDI0_TX#[1]
FDI_TXN2 W1 FDI0_TX#[2]
FDI_TXN3 AA6 FDI0_TX#[3]
FDI_TXN4 W6 FDI1_TX#[0]
FDI_TXN5 V4 FDI1_TX#[1]
FDI_TXN6 Y2 FDI1_TX#[2]
FDI_TXN7 AC9 FDI1_TX#[3]
FDI_TXP0 U6 FDI0_TX[0]
FDI_TXP1 W10 FDI0_TX[1]
FDI_TXP2 W3 FDI0_TX[2]
FDI_TXP3 AA7 FDI0_TX[3]
FDI_TXP4 W7 FDI1_TX[0]
FDI_TXP5 T4 FDI1_TX[1]
FDI_TXP6 AA3 FDI1_TX[2]
FDI_TXP7 AC8 FDI1_TX[3]
FDI_FSYNC0 AA11 FDI0_FSYNC
FDI_FSYNC1 AC12 FDI1_FSYNC
FDI_INT U11 FDI_INT
FDI_LSYNC0 AA10 FDI0_LSYNC
FDI_LSYNC1 AG8 FDI1_LSYNC

Intel(R) FDI

eDP_COMP AF3 eDP_COMPIO 4mils
AD2 eDP_ICOMPO 12mils
INT_eDP_HPD_Q AG11 eDP_HPD#
AG4 eDP_AUX#
AF4 eDP_AUX
AC3 eDP_TX[0]
AC4 eDP_TX[1]
AE11 eDP_TX[2]
AE7 eDP_TX[3]
AC1 eDP_TX[0]
AA4 eDP_TX[1]
AE10 eDP_TX[2]
AE6 eDP_TX[3]

eDP

IC,IVB_2CBGA,0P7

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI G3 PEG_COMP
PEG_ICOMPO G1
PEG_RCOMPO G4

PEG_RX#[0..7] <14>
PEG_RX#0 H22 PEG_RX[0]
PEG_RX#1 J21 PEG_RX[1]
PEG_RX#2 B22 PEG_RX[2]
PEG_RX#3 D21 PEG_RX[3]
PEG_RX#4 A19 PEG_RX[4]
PEG_RX#5 D17 PEG_RX[5]
PEG_RX#6 B14 PEG_RX[6]
PEG_RX#7 D13 PEG_RX[7]
PEG_RX[0..7] <14>
PEG_RX0 K22 PEG_RX[8]
PEG_RX1 K19 PEG_RX[9]
PEG_RX2 C21 PEG_RX[10]
PEG_RX3 D19 PEG_RX[11]
PEG_RX4 C19 PEG_RX[12]
PEG_RX5 D16 PEG_RX[13]
PEG_RX6 C13 PEG_RX[14]
PEG_RX7 D12 PEG_RX[15]

<14> PEG_TX#[0..7]
C_PEG_TX#0 C7193 0.1U/10V_4 PEG_TX#0 G22 PEG_TX[0]
C_PEG_TX#1 C7187 0.1U/10V_4 PEG_TX#1 C23 PEG_TX[1]
C_PEG_TX#2 C7189 0.1U/10V_4 PEG_TX#2 D23 PEG_TX[2]
C_PEG_TX#3 C7179 0.1U/10V_4 PEG_TX#3 F21 PEG_TX[3]
C_PEG_TX#4 C7175 0.1U/10V_4 PEG_TX#4 H19 PEG_TX[4]
C_PEG_TX#5 C7177 0.1U/10V_4 PEG_TX#5 C17 PEG_TX[5]
C_PEG_TX#6 C7164 0.1U/10V_4 PEG_TX#6 K15 PEG_TX[6]
C_PEG_TX#7 C7172 0.1U/10V_4 PEG_TX#7 E17 PEG_TX[7]

<14> PEG_TX[0..7]
C_PEG_TX0 C7184 0.1U/10V_4 PEG_TX0 F22 PEG_TX[8]
C_PEG_TX1 C7186 0.1U/10V_4 PEG_TX1 A23 PEG_TX[9]
C_PEG_TX2 C7188 0.1U/10V_4 PEG_TX2 D24 PEG_TX[10]
C_PEG_TX3 C7178 0.1U/10V_4 PEG_TX3 E21 PEG_TX[11]
C_PEG_TX4 C7173 0.1U/10V_4 PEG_TX4 G19 PEG_TX[12]
C_PEG_TX5 C7176 0.1U/10V_4 PEG_TX5 B18 PEG_TX[13]
C_PEG_TX6 C7170 0.1U/10V_4 PEG_TX6 K17 PEG_TX[14]
C_PEG_TX7 C7171 0.1U/10V_4 PEG_TX7 G17 PEG_TX[15]

PEG x8 disable (UMA only remove)

<8,14,26,29,30,33> PLTRST#
R7410 1.5K/F_4
CPU_RESET# D44 RESET#
R7427 750/F_4
C7603 *43P/50V_4

CPU RESET#

U7022B

<7> H_SNB_IVB# F49 PROC_SELECT#
TP7006 SKTOCC# C57 PROC_DETECT#
TP7002 TP_CATERR# C49 CATERR#
Placement close to EC.
<30> EC_PECI R217 43_4 H_PECI A48 PECI
47P/50V_4 C7602
<30,40> H_PROCHOT# R7409 56.2/F_4 H_PROCHOT#_R C45 PROCHOT#
<9,30> PM_THRMTRIP# D45 THERMTRIP#

MISC
THERMAL

<6> PM_SYNC C48 PM_SYNC
R7407 10K/F_4
<9> H_PWRGOOD B46 UNCOREPWRGOOD
C7601 *43P/50V_4
PM_DRAM_PWRGD_R BE45 SM_DRAMPWROK
Intel DG request

PWR MANAGEMENT

BCLK J3 CLK_CPU_BCLKP <8>
BCLK# H2 CLK_CPU_BCLKN <8>
DPLL_REF_CLK AG3 R7450 1K/F_4
DPLL_REF_CLK# AG1 R7447 1K/F_4 +1.05V

CLOCKS

SM_DRAMRST# AT30 CPU_DRAMRST# C7634 *43P/50V_4
SM_RCOMP[0] BF44 SM_RCOMP_0 R7214 140/F_4
SM_RCOMP[1] BE43 SM_RCOMP_1 R7215 25.5/F_4
SM_RCOMP[2] BG43 SM_RCOMP_2 R7216 200/F_4
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

DDR3 MISC

PRDY# N53 XDP_PRDY#
PREQ# N55 XDP_PREQ# TP7005 CPU XDP
TCK L56 XDP_TCLK
TMS L55 XDP_TMS
TRST# J58 XDP_TRST#
TDI M60 XDP_TDI_R
TDO L59 XDP_TDO
DBR# K58 XDP_DBRST# XDP_DBRST# <6>
BPM[0] G58
BPM[1] E55
BPM[2] E59
BPM[3] G55
BPM[4] G59
BPM[5] H60
BPM[6] J59 XDP_BPM6
BPM[7] J61 XDP_BPM7

JTAG & BPM

IC,IVB_2CBGA,0P7

DDR3 DRAM RESET

+1.5VSUS
R7492 1K/F_4
R7493 1K/F_4 DDR3_DRAMRST# <12,13>
Q7034 2N7002K
CPU_DRAMRST#_R
<8,12,13> DRAMRST_CNTRL_PCH R7457 0_4
C7636 0.047U/10V_4
CPU_DRAMRST#
R7489 4.99K/F_4

SM_DRAMPWROK Processor Input.

+1.5V_CPU
R7503 200/F_4
<6> PM_DRAM_PWRGD
PM_DRAM_PWRGD R7505 130/F_4 PM_DRAM_PWRGD_R
R7506 *39_4
R7504 *3K/F_4
Q7037 *2N7002K
MAIN_ONG <4,39>

Processor pull-up (CPU)

+1.05V
H_PROCHOT# R7408 62_4
XDP_TDO R7418 51_4
XDP_TMS R7421 51_4
XDP_TDI_R R7417 51_4
XDP_PREQ# R7422 *51_4
XDP_TCLK R7420 51_4
XDP_TRST# R7419 51_4

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V R7446 24.9/F_4 eDP_COMP
+1.05V R7431 24.9/F_4 PEG_COMP
+1.05V R7444 *10K/F_4 INT_eDP_HPD_Q

XDP_BPM6 TP7007 TP7025
XDP_BPM7 TP7004 TP7036

For iFDIM Trigger Point

Connect a Test Point on BPM# 6 signal, very close to processor.

Connect a Test Point on BPM# 7 signal, very close to processor.

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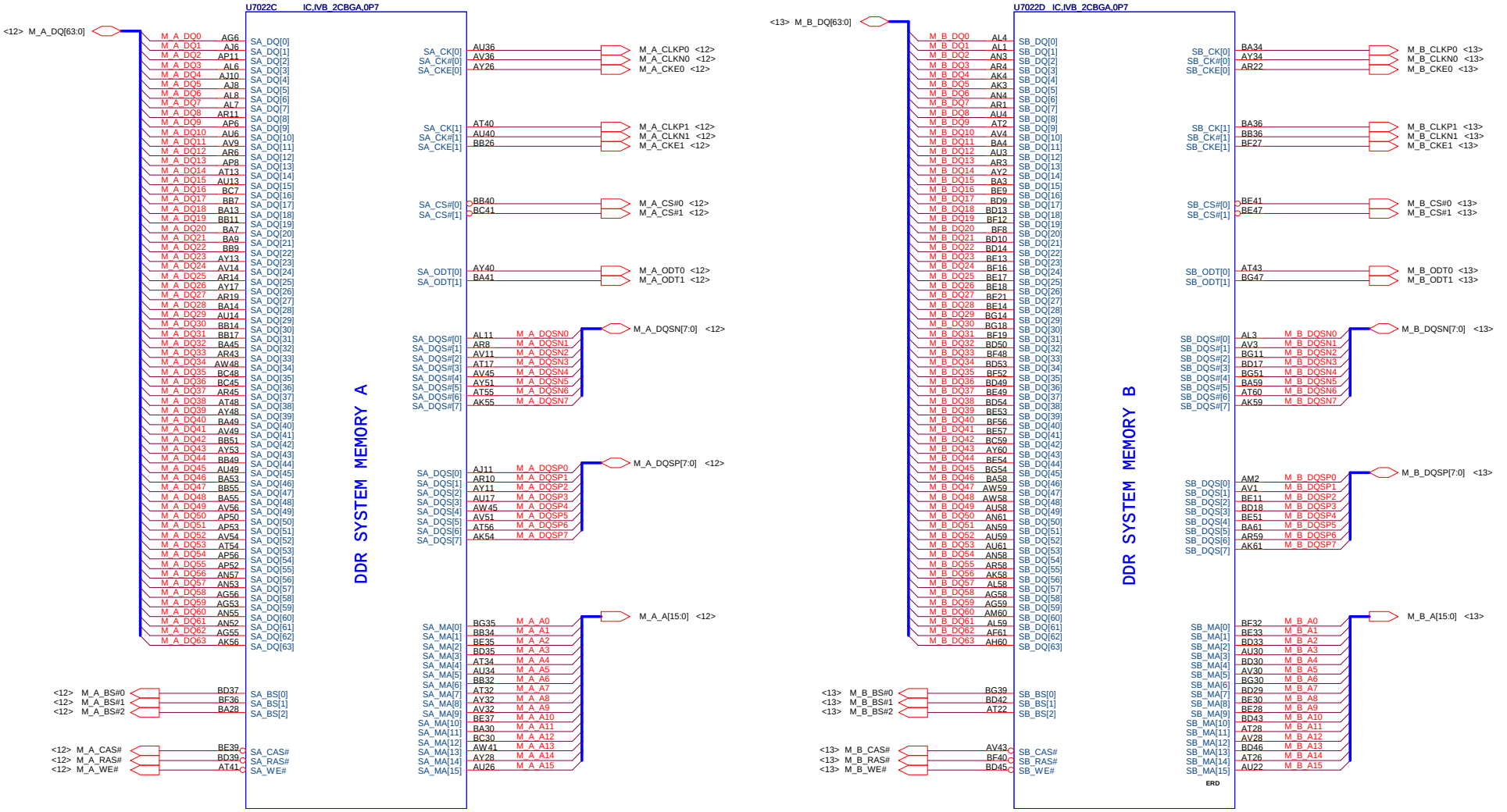
Ivy Bridge Processor (DDR3)



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POWER

U7022F

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

IC,IVB_2CBGA,0P7

+VCC_CORE

C7593 C7589 C7606 C7587 C7592 C7600 C7607 C7598 C7604 C7599 C7608 C7597 C7605 C7596 C7610 C7609 — 22U/6.3VS_6 / *22U/6.3VS_6

C7254 C7245 C7258 C7284 C7270 C7278 C7279 C7280 C7281 C7275 C7276 C7277 C7243 C7256 C7259 C7246 — 2.2U/6.3VS_4

330uFx3pcs bulk BOT
22uFx14pcs cavity BOT
2.2uFx16pcs BGA TOP

VCC[1] … VCC[76]

IVB:8.5A

+1.05V

C7324 C7315 C7316 — 1U/6.3V_4

C7619 C7620 C7621 C7326 C7330 C7622 C7615 C7617 — 22U/6.3VS_6

C7623 C7624 — *22U/6.3VS_6

330uFx2pcs bulk BOT
22uFx10pcs cavity BOT
2.2uFx13pcs BGA TOP

C7310 C7302 C7303 C7304 C7305 C7306 C7308 C7329 C7328 C7334 C7325 C7307 C7335 C7336 C7337 C7338 C7339 C7340 — 1U/6.3V_4 / *1U/6.3V_4

VCCIO_SEL — BC22 — H_VTTVID1 <38> — R7217 *1K/F_4

VCCPQE[1] VCCPQE[2] — AM25 AN22 — +1.05V — C7313 1U/6.3V_4

VIDALERT# A44 H_CPU_SVIDALRT#
VIDSCLK B43 VR_SVID_CLK
VIDSOUT C44 VR_SVID_DATA

100- ±1% pull-up to VC near processor.

VCC_SENSE F43 — R7415 100/F_4 — +VCC_CORE — VCC_SENSE <40>
VSS_SENSE G43 — R7414 100/F_4 — R7219 10/F_4 — +1.05V — VSS_SENSE <40>

Zo impedance: 27.4ohm

VCCIO_SENSE AN16 VCCP_SENSE — VCCP_SENSE <38>
VSS_SENSE_VCCIO AN17 VSSP_SENSE — VSSP_SENSE <38> — R7218 10/F_4

Zo:55 ohm

R close to CPU

H_CPU_SVIDALRT# — R7428 43_4 — R7412 75/F_4 — +1.05V — VR_SVID_ALERT# <40>
VR_SVID_DATA — VR_SVID_DATA <40>
VR_SVID_CLK — R7411 130/F_4 — +1.05V — VR_SVID_CLK <40>

+VCC_GFX

330uFx2pcs bulk BOT
22uFx12pcs cavity BOT
1uFx12pcs BGA TOP

C7298 C7300 C7215 C7267 C7299 C7317 C7217 C7268 C7301 C7216 C7218 C7269 C7295 C7219 C7296 C7273 C7312 C7297 C7220 C7271 C7272 — 22U/6.3VS_6 / 1U/6.3V_4

VAXG[1] … VAXG[56]

GRAPHICS

TP7034 — +VCC_GFX — 10/F_4 — R7416

<40> VCC_AXG_SENSE
<40> VSS_AXG_SENSE

VAXG_SENSE F45
VSSAXG_SENSE G45

SENSE LINES

Zo impedance: 27.4ohm

10/F_4 — R7413 — TP7035

+1.8V

IVB: 1.5A

C7627 C7628 C7629 — 1U/6.3V_4 / 10U/6.3V_6

330uF x1, 10uF_8 x1, 1uF_4 x2

VCCPLL[1] BB3
VCCPLL[2] BC1
VCCPLL[3] BC4

1.8V RAIL

+VCCSA

IVB: 6A

C7247 C7292 C7288 C7309 — 10U/6.3V_6

330uFx1, 10uFx4

VCCSA[1] L17
VCCSA[2] L21
VCCSA[3] N16
VCCSA[4] N20
VCCSA[5] N22
VCCSA[6] P17
VCCSA[7] P20
VCCSA[8] R16
VCCSA[9] R18
VCCSA[10] R21
VCCSA[11] U15
VCCSA[12] V16
VCCSA[13] V17
VCCSA[14] V18
VCCSA[15] V21
VCCSA[16] W20

SA RAIL

IC,IVB_2CBGA,0P7

Q7013 AON7410 — +1.5VSUS — +1.5V_CPU — R7507 220_8 — MAIND — C7638 *470P/50V_4 — Q7036 2N7002K — MAIN_ONG <2,39>

CPU VDDQ

U7022G

VREF

SM_VREF AY43
SA_DIMM_VREFDQ BE7 SMDDR_VREF_DQ0_M3
SB_DIMM_VREFDQ BG7 SMDDR_VREF_DQ1_M3

20mils width

+VDDR_REF_CPU — C7637 0.1U/10V_4 — R7494 1K/F_4 — +1.5V_CPU — R7499 1K/F_4

Q7035 2N7002K — DDR_VTTREF <12,13,37>

R7500 3.3K/F_4 — MAIND <39>

C7639 470P/50V_4

+VDDR_REF_CPU and DDR_VTTREF must use 10mils width

DDR3 - 1.5V RAILS

VDDQ[1] … VDDQ[26]

IVB: 5A

C7331 C7320 C7318 C7322 — 10U/6.3V_6

C7333 C7321 C7332 C7319 — 10U/6.3V_6

QUIET RAILS

CPU center

CRB: 1uf*1

+1.5V_CPU — VCCDQ[1] VCCDQ[2] — AM28 AN26 — C7327 1U/6.3V_4

+1.5V_CPU +1.5VSUS — C7346 C7347 C7345 C7344 — 0.1U/10V_4

VDDQ_SENSE BC43
VSS_SENSE_VDDQ BA43

TP7027 TP7026

SENSE LINES

R7153 *100/F_4 — +VCCSA — VCCSA_SENSE <36>

Zo:55 ohm

VCCSA VID Lines

VCCSA_VID[0] D48 VCCSA_SEL0 — R7426 1K/F_4 — VCCSA_SEL0 <36>
VCCSA_VID[1] D49 VCCSA_SEL — R7406 1K/F_4 — VCCSA_SEL <36>

SMDDR_VREF_DQ0_M3 — R7490 *1K/F_4 — SMDDR_VREF_DQ0_M3 <12>

SMDDR_VREF_DQ1_M3 — R7491 *1K/F_4 — SMDDR_VREF_DQ1_M3 <13>

+1.5V_CPU — R50 *0_8/S — +1.5V

40mile routing

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

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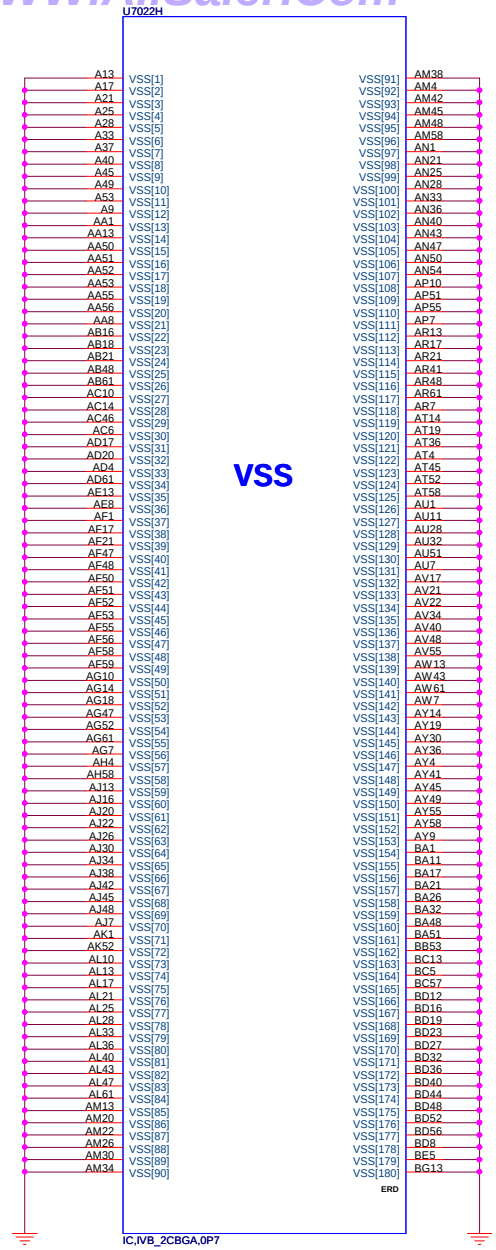
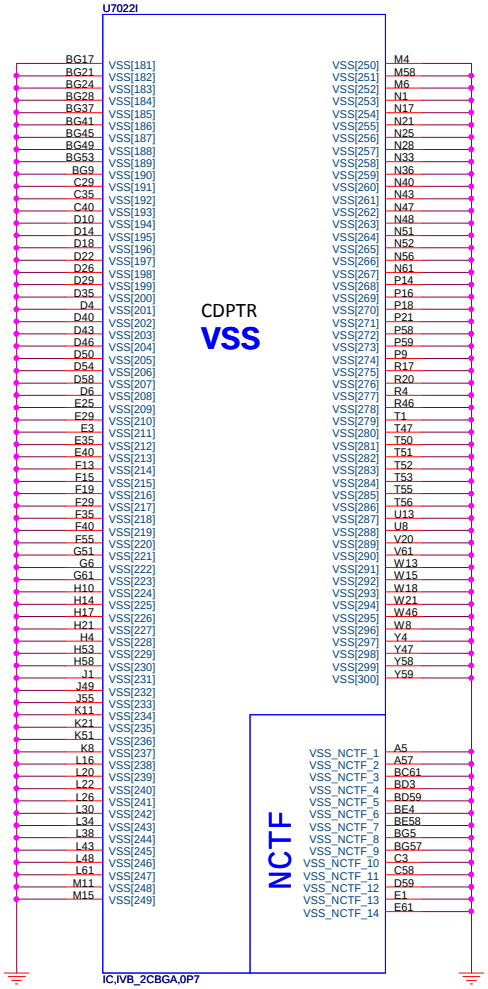
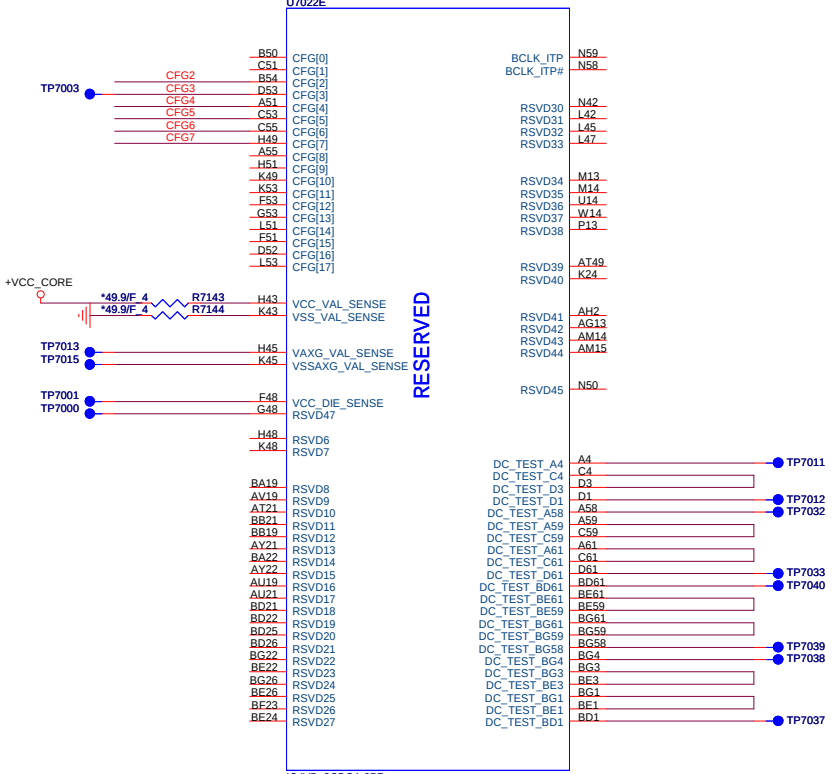
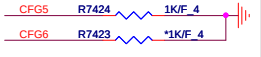






CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

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Cougar Point/Panther Point (DMI,FDI,PM)

U32C

DMI0RXN DMI1RXN DMI2RXN DMI3RXN
DMI0RXP DMI1RXP DMI2RXP DMI3RXP
DMI0TXN DMI1TXN DMI2TXN DMI3TXN
DMI0TXP DMI1TXP DMI2TXP DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
DMI2RBIAS

DMI_RXN0 BC24
DMI_RXN1 BE20
DMI_RXN2 BG18
DMI_RXN3 BG20
DMI_RXP0 BE24
DMI_RXP1 BC20
DMI_RXP2 BJ18
DMI_RXP3 BJ20
DMI_TXN0 AW24
DMI_TXN1 AW20
DMI_TXN2 BB18
DMI_TXN3 AV18
DMI_TXP0 AY24
DMI_TXP1 AY20
DMI_TXP2 AY18
DMI_TXP3 AU18
BJ24
BG25
BH21

+1.05V R567 49.9/F_4 DMI_COMP
R557 750/F_4 DMI_RBIAS

DMI

FDI_RXN0 BJ14
FDI_RXN1 AY14
FDI_RXN2 BE14
FDI_RXN3 BH13
FDI_RXN4 BC12
FDI_RXN5 BJ12
FDI_RXN6 BG10
FDI_RXN7 BG9
FDI_RXP0 BG14
FDI_RXP1 BB14
FDI_RXP2 BF14
FDI_RXP3 BG13
FDI_RXP4 BE12
FDI_RXP5 BG12
FDI_RXP6 BJ10
FDI_RXP7 BH9
FDI_INT AW16
FDI_FSYNC0 AV12
FDI_FSYNC1 BC10
FDI_LSYNC0 AV14
FDI_LSYNC1 BB10

FDI_TXN0 <2>
FDI_TXN1 <2>
FDI_TXN2 <2>
FDI_TXN3 <2>
FDI_TXN4 <2>
FDI_TXN5 <2>
FDI_TXN6 <2>
FDI_TXN7 <2>
FDI_TXP0 <2>
FDI_TXP1 <2>
FDI_TXP2 <2>
FDI_TXP3 <2>
FDI_TXP4 <2>
FDI_TXP5 <2>
FDI_TXP6 <2>
FDI_TXP7 <2>
FDI_INT <2>
FDI_FSYNC0 <2>
FDI_FSYNC1 <2>
FDI_LSYNC0 <2>
FDI_LSYNC1 <2>

FDI

System Power Management

SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
(+3VS5)
SUSWARN#/SUSPWRDNACK/GPIO30
PWRBTN#
(DSW)
ACPRESENT / GPIO31
(+3VS5)
BATLOW# / GPIO72
RI#

SUS_PWR_ACK_R R540 *0_4/S SUSACK#_R C12
XDP_DBRST# <2> K3
SYS_PWROK R485 *0_4/S SYS_PWROK_R P12
EC_PWROK <18,30> R478 *0_4/S EC_PWROK_R L22
EC_PWROK_R R265 *0_4/S APWROK_R L10
PM_DRAM_PWRGD <2> B13
RSMRST# <30> C21
SUS_PWR_ACK <30> R514 *0_4/S SUS_PWR_ACK_R K16
DNBSWON# <30> R560 *0_4/S DNBSWON#_R E20
AC_PRESENT <30> R566 *0_4 AC_PRESENT_R H20
PM_BATLOW# E10
PM_RI# A10

DSWVRMEN A18 DSWVREN
DPWROK E22 R562 *0_4/S RSMRST#
WAKE# B9 PCIE_WAKE# PCIE_WAKE# <29,33>
(+3V)
CLKRUN# / GPIO32 N3 CLKRUN# CLKRUN# <30>
(+3VS5)
SUS_STAT# / GPIO61 G8 TP57
(+3VS5)
SUSCLK / GPIO62 N14 PCH_SUSCLK_L R304 *0_4/S PCH_SUSCLK <30>
(+3VS5)
SLP_S5# / GPIO63 D10 SLP_S5 <30>
SLP_S4# H4 R253 *0_4/S SUSC# <30>
SLP_S3# F4 R538 *0_4/S SUSB# <30>
SLP_A# G10 TP56
SLP_SUS# G16 TP61
PMSYNCH AP14 PM_SYNC <2>
(+3VS5)
SLP_LAN# / GPIO29 K14 SLP_LAN#

TP95
TP99
TP62

CPT_PPT_Rev_0p5

SYS_PWROK_R
C488 *0.1U/10V_4
Reserve for power on sequence

Cougar Point/Panther Point (LVDS,DDI)

U32D

LVDS

<23> LVDS_BLON J47 L_BKLTEN
<23> DISP_ON M45 L_VDD_EN
<23> DPST_PWM P45 L_BKLTCTL
<23> EDIDCLK T40 L_DDC_CLK
<23> EDIDDATA K47 L_DDC_DATA
+3V R331 2.2K_4 L_CTRL_CLK T45 L_CTRL_CLK
R330 2.2K_4 L_CTRL_DATA P39 L_CTRL_DATA
R329 2.37K/F_4 LVDS_IBG AF37 LVD_IBG
TP65 LVDS_VBG AF36 LVD_VBG
AE48 LVD_VREFH
AE47 LVD_VREFL

<23> TXLCLKOUT- AK39 LVDSA_CLK#
<23> TXLCLKOUT+ AK40 LVDSA_CLK
<23> TXLOUT0- AN48 LVDSA_DATA#0
<23> TXLOUT1- AM47 LVDSA_DATA#1
<23> TXLOUT2- AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
<23> TXLOUT0+ AN47 LVDSA_DATA0
<23> TXLOUT1+ AM49 LVDSA_DATA1
<23> TXLOUT2+ AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3

<23> TXUCLKOUT- AF40 LVDSB_CLK#
<23> TXUCLKOUT+ AF39 LVDSB_CLK
<23> TXUOUT0- AH45 LVDSB_DATA#0
<23> TXUOUT1- AH47 LVDSB_DATA#1
<23> TXUOUT2- AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
<23> TXUOUT0+ AH43 LVDSB_DATA0
<23> TXUOUT1+ AH49 LVDSB_DATA1
<23> TXUOUT2+ AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

CRT

<24> CRT_B R340 150/F_4 N48 CRT_BLUE
<24> CRT_G R342 150/F_4 P49 CRT_GREEN
<24> CRT_R R341 150/F_4 T49 CRT_RED
<24> DDCCLK T39 CRT_DDC_CLK
<24> DDCDATA M40 CRT_DDC_DATA
<24> HSYNC_COM R354 33_4 PCH_HSYNC_R M47 CRT_HSYNC
<24> VSYNC_COM R352 33_4 PCH_VSYNC_R M49 CRT_VSYNC
R335 1K/F_4 DAC_IREF T43 DAC_IREF
T42 CRT_IRTN

Digital Display Interface

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 SDVO_CLK <25>
SDVO_CTRLDATA M39 SDVO_DATA <25>
DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 DPB_HPD_Q
DDPB_0N AV42 DPB_LANE0_N
DDPB_0P AV40 DPB_LANE0_P
DDPB_1N AV45 DPB_LANE1_N
DDPB_1P AV46 DPB_LANE1_P
DDPB_2N AU48 DPB_LANE2_N
DDPB_2P AU47 DPB_LANE2_P
DDPB_3N AV47 DPB_LANE3_N
DDPB_3P AV49 DPB_LANE3_P
DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49
DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BE44
DDPD_1P BE42
DDPD_2N BE43
DDPD_2P BJ42
DDPD_3N BG42
DDPD_3P

INT. HDMI

CPT_PPT_Rev_0p5

PD Res place close to PCH
PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance.

Reserve from EMI request
CRT_B
CRT_G
CRT_R
C531 *5.6P/16V_4
C533 *5.6P/16V_4
C532 *5.6P/16V_4

+3V_RTC <7,10>
+1.05V <2,4,7,8,10,30,33,36,38,40>
+3VPCU <7,23,30,31,33,34,35>
+3VS5 <7,8,9,10,23,33,35,38,39,42,43>
+3V <7,8,9,10,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,39,40,42,43>
+5V <7,10,18,24,25,27,30,31,32,33,39>

PCH Pull-high/low(CLG)

+3VS5
PM_RI# R496 10K_4
PM_BATLOW# R494 8.2K_4 INTEL DG
PCIE_WAKE# R528 10K_4
SLP_LAN# R314 *10K_4
SUS_PWR_ACK R497 *10K_4
AC_PRESENT_R R561 10K_4

+3V
CLKRUN# R535 8.2K_4
XDP_DBRST# R507 1K_4 INTEL DG
R530 *1K_4
RSMRST# R565 10K_4
SYS_PWROK R486 *10K_4

INT HDMI disable (DIS only remove)

DPB_LANE0_N IN_D2# <25>
DPB_LANE0_P IN_D2 <25>
DPB_LANE1_N IN_D1# <25>
DPB_LANE1_P IN_D1 <25>
DPB_LANE2_N IN_D0# <25>
DPB_LANE2_P IN_D0 <25>
DPB_LANE3_N IN_CLK# <25>
DPB_LANE3_P IN_CLK <25>

INT HDMI Detect Function

DPB_HPD_Q R600 *0_4/S HDMI_HPD_CON <25>

System PWR_OK(CLG)

R483 *0_4/S IMVP_PWRGD
+3VS5
C796 *0.1U/10V_4
SYS_PWROK
U29 *TC7SH08FU
R482 100K_4
EC_PWROK
IMVP_PWRGD <40>
R484 *0_4

DPWROK FOR DSW

Remove DSW power rail

+3V_RTC R559 330K_4 DSWVREN R558 *330K_4

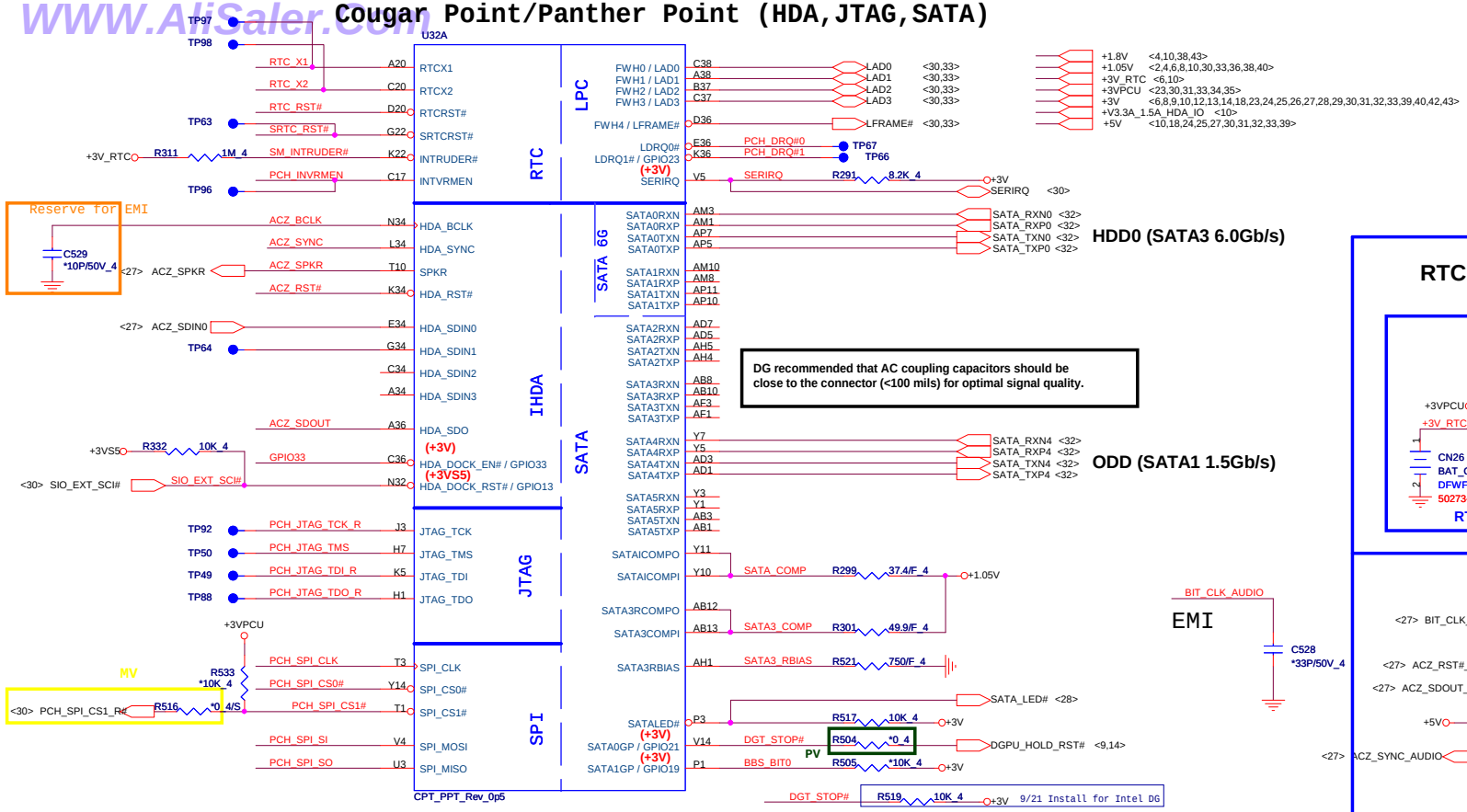
On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PROJECT :R33
Quanta Computer Inc.

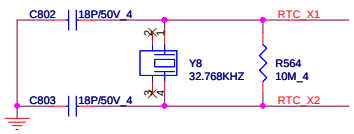
Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

Date: Friday, September 07, 2012 Sheet 6 of 43

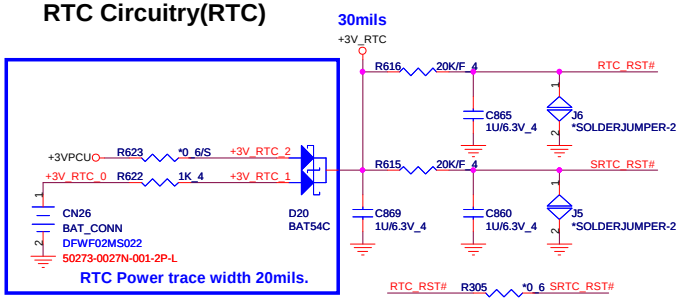
Cougar Point/Panther Point (HDA,JTAG,SATA)



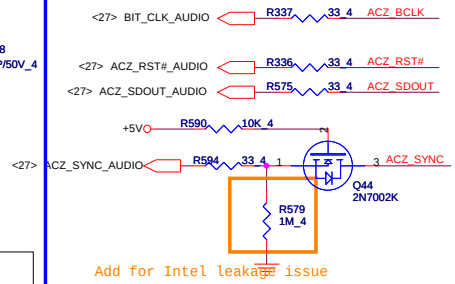
RTC Clock 32.768KHz



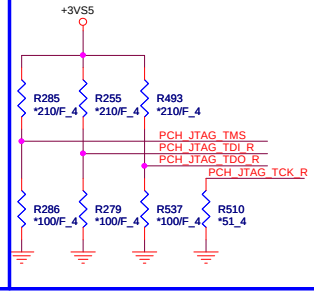
RTC Circuitry(RTC)



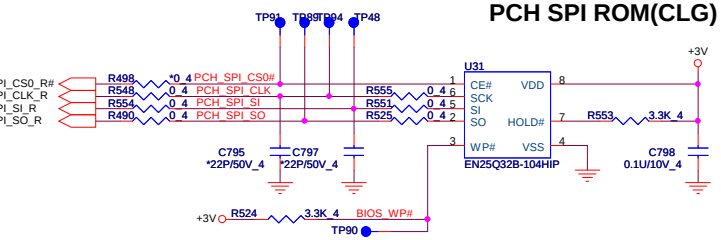
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
Max	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
Socket		DFHS08FS023

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR (Different from Calpella)	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R500 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R584 *1K_4 R595 10K_4 PCI_GNT3# <8>
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R572 0_4 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 (Different from Calpella)	Boot BIOS Selection 0 [bit-0]	PWROK		R534 *1K_4 BBS_BIT0 R585 *1K_4 BBS_BIT1 <8>
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R547 *1K_4 NV_ALE <8>
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R526 2.2K_4 R546 1K_4 NV_CLE <9> H_SNB_IVB# <2> sandy/Ivy bridge
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R334 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overridden	<30> GPIO33_E ACZ_SDOUT R573 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 (Different from Calpella)	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R492 *1K_4 PLL_ODVR_EN <9>
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R292 *1K_4 9/28 HW +3V

PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
Date: Friday, September 07, 2012	Sheet 7 of 43	

Cougar Point/Panther Point (PCI,USB,NVRAM)

Cougar Point/Panther Point(PCI-E,SMBUS,CLK)

PCI/USBOC# Pull-up(CLG)

USB3.0

PCI

USB

RSVD

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

PCI-E*

EMI

RF

PLTRST#(CLG)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PEG Clock detect (SG only)

PCIE Clock

SMBus/Pull-up(CLG)

WLAN

LAN

Cardreader

USB2.0 USB2.0/USB3.0 COMBO 1st

USB2.0 USB2.0/USB3.0 COMBO 2nd

Webcam

Right_USB

WLAN

GPU

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

PV , HP request Image sensor
SMBus reserve to PCH

change 25M to small size

Remove Ra, Rb for UMA &
SG. 27MHz support DIS only.

Remove for UMA only.

CLOCK TERMINATION for FCIM

SG : Rb ; UMA : Ra

PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A

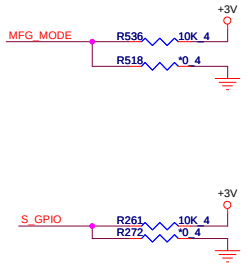
Date: Friday, September 07, 2012 Sheet 8 of 43

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

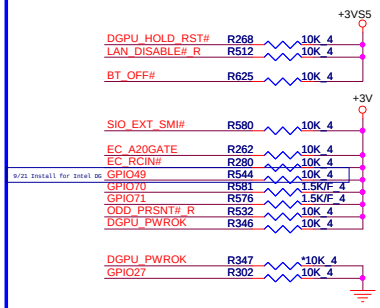
Clock Gen Power OK (CLG)

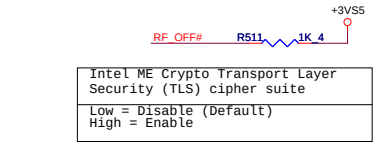
09

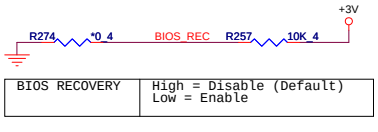
MFG-TEST

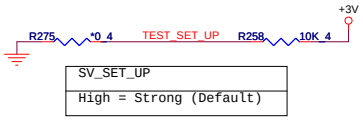


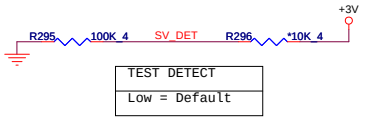
GPIO Pull-up/Pull-down(CLG)

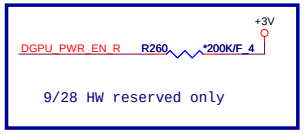


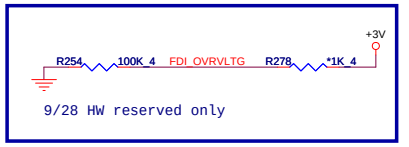






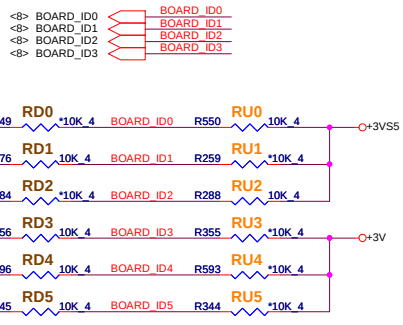






BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R33 UMA	0	0	0	0	0	0
R33 DIS	0	0	0	0	0	1
R33H (BGA) UMA	0	0	0	1	0	0
R33H (BGA) DIS	0	0	0	1	0	1
	0	0	0	0	0	0



GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
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Cougar Point/Panther Point(POWER)

COUGAR POINT/Panther Point (POWER)

POWER

U32J

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA

VCCACLK AD49 +VCCACLK
VCCDSW3_3 T16 +VCCPDSW
DCPSUSBYP V12 PCH_VCCDSW
VCC3_3[5] T38 +3V_SUS_CLKF33
VCCAPLLDMI2 BH23 +VCCPDPLL_CPY_PCH
VCCIO[14] AL29 +VCCPDPLL_CPY
DCPSUS[3] AL24 +VCCSUS1
VCCASW[1] AA19
VCCASW[2] AA21
VCCASW[3] AA24
VCCASW[4] AA26
VCCASW[5] AA27
VCCASW[6] AA29
VCCASW[7] AA31
VCCASW[8] AC26
VCCASW[9] AC27
VCCASW[10] AC29
VCCASW[11] AC31
VCCASW[12] AD29
VCCASW[13] AD31
VCCASW[14] W21
VCCASW[15] W23
VCCASW[16] W24
VCCASW[17] W26
VCCASW[18] W29
VCCASW[19] W31
VCCASW[20] W33
DCPRTC N16 +VCCRTCEXT
VCCVRM[4] Y49 +VCCAFDI_VRM
VCCADPLLA BD47 +1.05V_VCCA_A_DPL
VCCADPLLB BF47 +1.05V_VCCA_B_DPL
VCCIO[7] AF17 +VCCDIFFCLK
VCCDIFFCLKN[1] AF33 +VCCDIFFCLKN
VCCDIFFCLKN[2] AF34
VCCDIFFCLKN[3] AG34
VCCSSC AG33 +V1.05V_SSCVCC
DCPSST V16 +VCCSST
DCPSUS[1] T17 +V1.05M_VCCSUS
DCPSUS[2] V19
V_PROC_IO BJ8 +VTT_VCCPCPU
VCCRTC A22 +3V_RTC
VCCIO[29] N26
VCCIO[30] P26
VCCIO[31] P28
VCCIO[32] T27
VCCIO[33] T29
VCCSUS3_3[7] T23 +3V_VCCPUSB
VCCSUS3_3[8] T24
VCCSUS3_3[9] V23
VCCSUS3_3[10] V24
VCCSUS3_3[6] P24 +3V_VCCAUBG
VCCIO[34] T26 +VCCAUPLL
V5REF_SUS M26 +5V_PCH_VCC5REFSUS
DCPSUS[4] AN23 +VCCA_USBSUS
VCCSUS3_3[1] AN24 +3V_VCCPSUS
V5REF P34 +5V_PCH_VCC5REF
VCCSUS3_3[2] N20
VCCSUS3_3[3] N22
VCCSUS3_3[4] P20 +3V_VCCPSUS
VCCSUS3_3[5] P22
VCC3_3[1] AA16
VCC3_3[8] W16 +3V_VCCPCORE
VCC3_3[4] T34
VCC3_3[2] AJ2
VCCIO[5] AF13
VCCIO[12] AH13
VCCIO[13] AH14
VCCIO[6] AF14
VCCAPLLSATA AK1 +V1.1LAN_VCCAPLL
VCCVRM[1] AF11 +VCCAFDI_VRM
VCCIO[2] AC16
VCCIO[3] AC17 +1.05V_VCCIO1
VCCIO[4] AD17
VCCASW[22] T21
VCCASW[23] V21
VCCASW[21] T19
VCCSUSHDA P32

+1.05V_VCCUSBCORE
R588 *0_8/S
C815 1U/6.3V_4
119mA (20mils)
+3VS5
R319 *0_6/S
C501 0.1U/10V_4
R318 *0_6/S
C504 0.1U/10V_4
R322 *0_6/S +1.05V
C498 *1U/6.3V_4
119mA (15mils)
R320 *0_6/S +3VS5
C499 1U/6.3V_4
266mA (20mils)
R267 *0_6/S +3V
C483 0.1U/10V_4
C790 0.1U/10V_4
C789 0.1U/10V_4
R287 *0_8/S +1.05V
C484 1U/6.3V_4
L53 *10uH/100mA_8 +1.05V
C788 *10U/6.3V_6
R281 *0_6/S +1.05V
C493 1U/6.3V_4
1.01A (60mils) +1.05V_VCCEPW
10mA (10mils) +V3.3A_1.5A_HDA_IO
R569 *0_4 +1.5VSUS
R570 *0_4/S +3VS5
C806 0.1U/10V_4
C808 *1U/6.3V_4

CPT_PPT_Rev_0p5

R589 *0_8 +1.05V
R315 *0_4/S +3VS5
C496 0.1U/10V_4
C487 *0.1U/10V_4
3mA (10mils)
L55 *10uH/100mA_8
C801 *10U/6.3V_6
C502 *1U/6.3V_4
R324 *0_6/S +1.05V
1.01A (60mils)
C505 1U/6.3V_4
C511 1U/6.3V_4
C512 1U/6.3V_4
C482 22U/6.3VS_8
C481 22U/6.3VS_8
R527 *0_6/S +1.05V
C792 1U/6.3V_4
C489 0.1U/10V_4
R592 *0_6/S +1.05V
160mA (20mils)
C817 1U/6.3V_4
65mA (10mils)
8mA (10mils)
R591 *0_6/S +1.05V
C816 1U/6.3V_4
55mA (10mils)
95mA (10mils)
R310 *0_6 +1.05V
C494 *1U/6.3V_4
C490 0.1U/10V_4
9/28 HW
+1.05V_VTT
C784 4.7U/6.3V_6
C785 0.1U/10V_4
C786 0.1U/10V_4
V_PROC_IO=1mA (10mils)
C805 1U/6.3V_4
C809 0.1U/10V_4
C804 0.1U/10V_4
VCCRTC<1mA (10mils)

POWER

U32G

VCC CORE
LVDS
HVCMOS
VCCIO
DMI
DFT / SPI
FDI

VCCCORE[1] AA23
VCCCORE[2] AC23
VCCCORE[3] AD21
VCCCORE[4] AD23
VCCCORE[5] AF21
VCCCORE[6] AF23
VCCCORE[7] AG21
VCCCORE[8] AG23
VCCCORE[9] AG24
VCCCORE[10] AG26
VCCCORE[11] AG27
VCCCORE[12] AG29
VCCCORE[13] AJ23
VCCCORE[14] AJ26
VCCCORE[15] AJ27
VCCCORE[16] AJ29
VCCCORE[17] AJ31
VCCIO[28] AN19
VCCAPLLEXP BJ22
VCCIO[15] AN16
VCCIO[16] AN17
VCCIO[17] AN21
VCCIO[18] AN26
VCCIO[19] AN27
VCCIO[20] AP21
VCCIO[21] AP23
VCCIO[22] AP24
VCCIO[23] AP26
VCCIO[24] AT24
VCCIO[25] AN33
VCCIO[26] AN34
VCC3_3[3] BH29
VCCVRM[2] AP16
VccAFDIPLL BG6
VCCIO[27] AP17
VCCDMI[2] AU20
VCCADAC U48
VSSADAC U47
VCCALVDS AK36
VSSALVDS AK37
VCCTX_LVDS[1] AM37
VCCTX_LVDS[2] AM38
VCCTX_LVDS[3] AP36
VCCTX_LVDS[4] AP37
VCC3_3[6] V33
VCC3_3[7] V34
VCCVRM[3] AT16
VCCDMI[1] AT20
VCCCLKDMI AB36
VCCDFTERM[1] AG16
VCCDFTERM[2] AG17
VCCDFTERM[3] AJ16
VCCDFTERM[4] AJ17
VCCSPI V1 ERD

1.3 A (60mils)
C506 1U/6.3V_4
C500 1U/6.3V_4
C497 10U/6.3VS_6
C510 1U/6.3V_4
+1.05V_PCH_VCCDPLL_EXP
R309 *0_6/S
+1.05V_VCCAPLL_EXP
L54 *1uH/25mA_6
C800 *10U/6.3V_6
2.925 A (140mils)
C520 1U/6.3V_4
C521 1U/6.3V_4
C503 10U/6.3VS_6
C508 1U/6.3V_4
C509 1U/6.3V_4
+3V_VCC_EXP
R568 *0_8/S +3V
C807 0.1U/10V_4
+VCCAFDI_VRM
(Mobile 1.5V) 160mA (15mils)
R598 *0_6/S +1.5V
R599 *0_6 +1.05V
+VCCAFDI_VRM
+1.05V_VCCAPLL_FDI
R545 *0_8 +1.05V
R556 *0_8/S
+1.05V_VCCDPLL_FDI
9/28 HW
+1.05V_VTT

CPT_PPT_Rev_0p5

1mA (10mils) +VCCA_DAC_1_2
L61 *HCB1608KF-181T15/1.5A_6 +3V
+3V_LDO
C827 10U/6.3VS_6
C819 0.1U/10V_4
C823 0.01U/25V_4
R597 *0_6
1mA (10mils)
+VCCALVDS +3V
60mA (10mils)
+VCC_TX_LVDS
L59 0.1uH/250mA_8 +1.8V
C828 22U/6.3VS_8
C527 0.01U/25V_4
C525 0.01U/25V_4
+3V_VCC_GIO
C853 0.1U/10V_4
R608 *0_6/S +3V
42mA (10mils)
+1.1V_VCC_DMI
9/28 HW
+1.05V_VTT
+1.1V_VCC_DMI_CCI
C495 1U/6.3V_4
C833 1U/6.3V_4
C837 *10U/6.3V_6
190 mA (15mils)
+VCCP_NAND +1.8V
R282 *0_8/S
C492 0.1U/10V_4
20mA (10mils)
+3V_VCCME_SPI +3V
R502 *0_6/S
C783 1U/6.3V_4

65mA (10mils)
L57 10uH/100MA_8 +1.05V_VCCA_A_DPL
C818 1U/6.3V_4
C839 *220U/2.5V_3528
8mA (10mils)
L56 10uH/100MA_8 +1.05V_VCCA_B_DPL
C811 1U/6.3V_4
C812 *220U/2.5V_3528
20mA (10mils)
R603 *0_6 +3V_SUS_CLKF33
R606 1/F_4 +3V_SUS_CLKF33_R
L82 10uH/100mA_8
C846 1U/6.3V_4
C841 10U/6.3VS_6
20mA (10mils)
R601 *1/F_4 +VCC_DMI_CCI
R602 *0_4/S
L60 *10uH/100mA_8 +1.1V_VCC_DMI_CCI

+5V_PCH_VCC5REF
V5REF= 1mA
R326 10_4 +5V
D12 RB500V-40 +3V
C514 1U/6.3V_4
VCC5REFSUS=1mA
+5V_PCH_VCC5REFSUS
R328 10_4 +5VS5
D13 RB500V-40 +3VS5
C890 0.1U/10V_4
C515 0.1U/10V_4
9/29 EMI request

If have power noise issue then stuff it.
+5V
U33 G910T21U
+3V_LDO
Vin
GND
Vout
C838 1U/6.3V_4

+1.05V <2,4,6,7,8,30,33,36,38,40>
+3V_RTC <6,7>
+1.5V <4,12,33>
+3VS5 <6,7,8,9,23,33,35,38,39,42,43>
+3V <6,7,8,9,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,39,40,42,43>
+5VS5 <24,28,33,35,36,37,38,39,40,41,42>
+5V <7,18,24,25,27,30,31,32,33,39>
+1.5VSUS <2,4,12,13,37,43>
+1.8V <4,7,38,43>

+1.05V +1.05V_VTT
Reserve for DB only, after DB change to short pad

PV, add
+VCCAFDI_VRM
C907 0.1U/10V_4

PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

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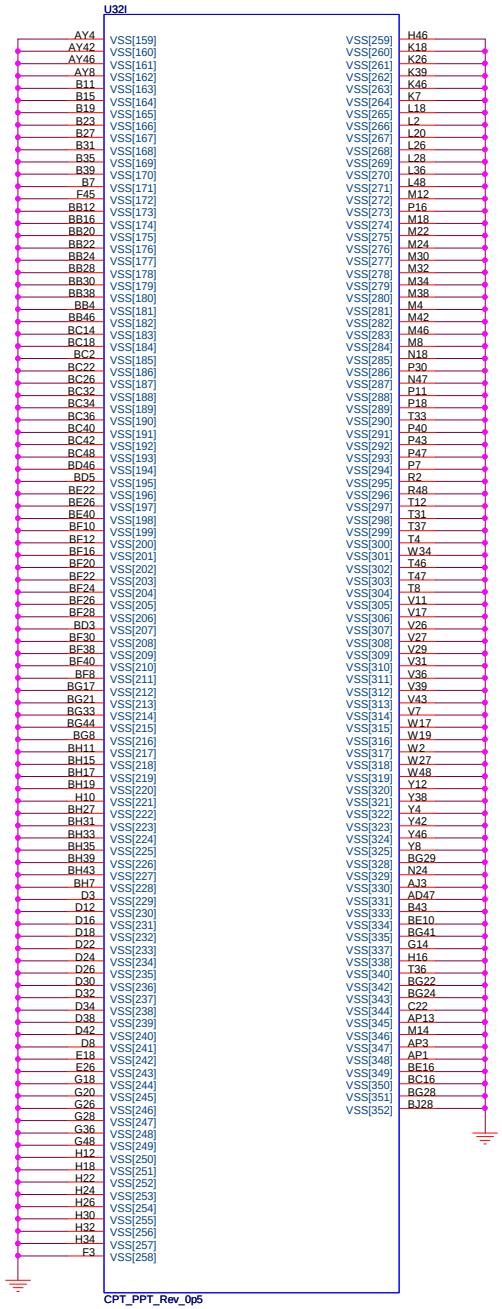
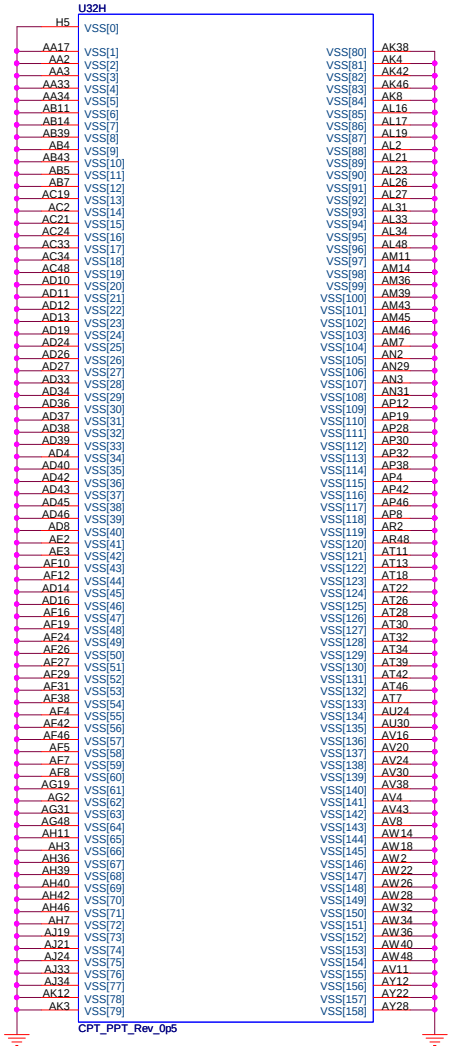
Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)





PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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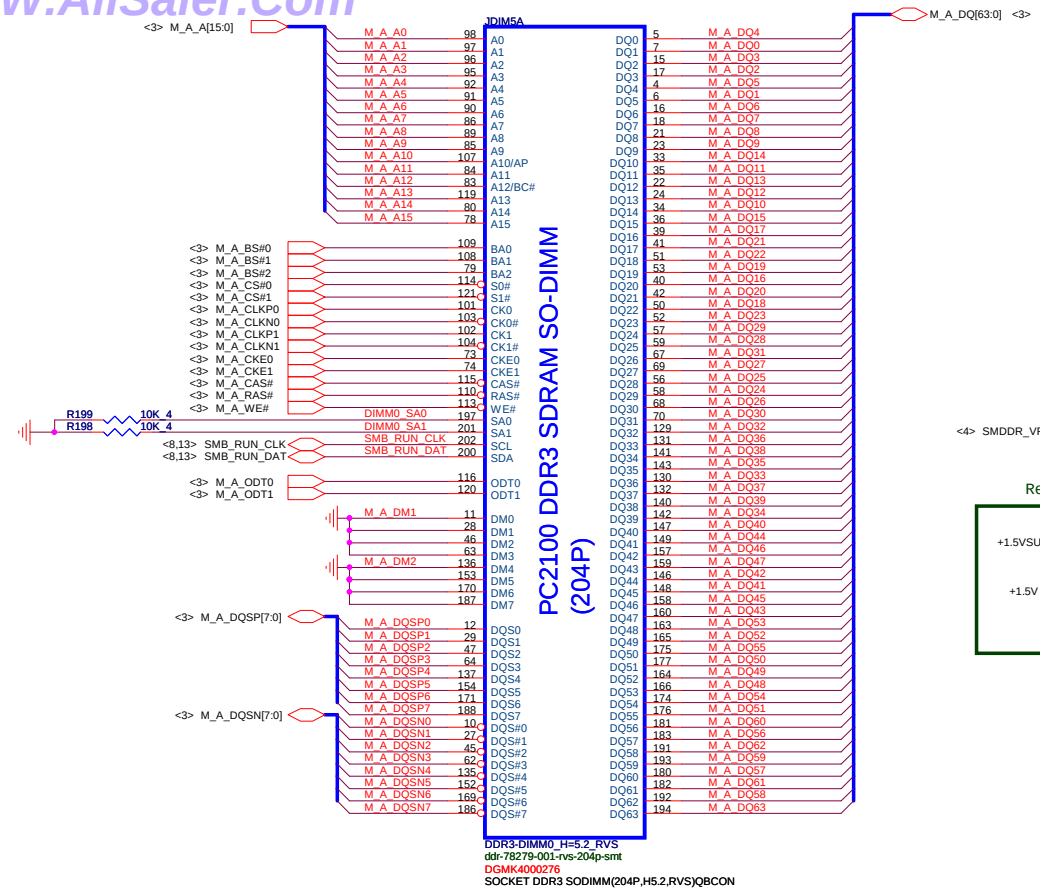
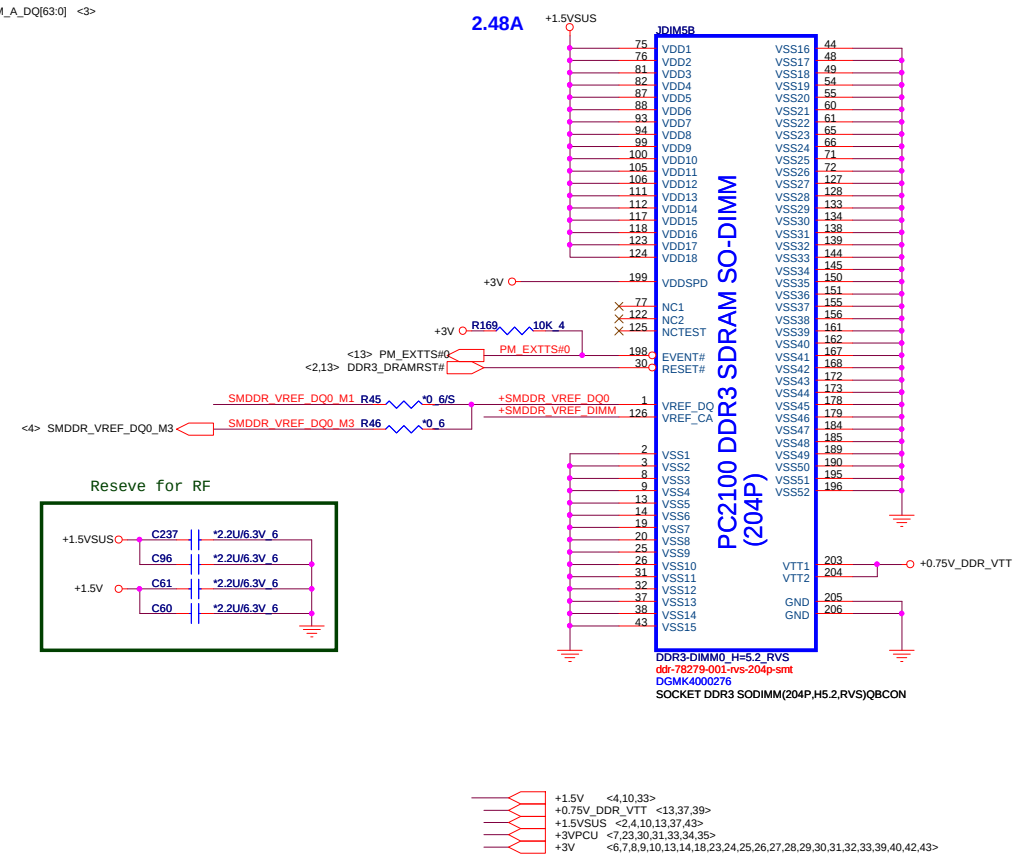
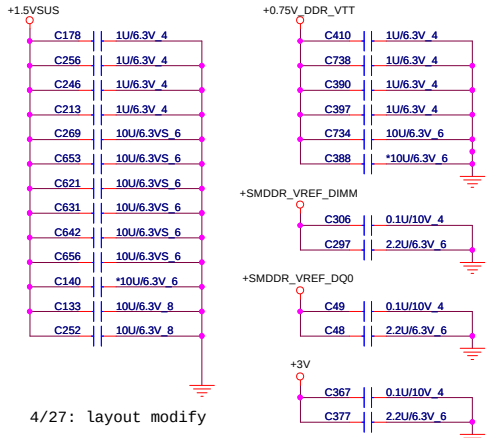




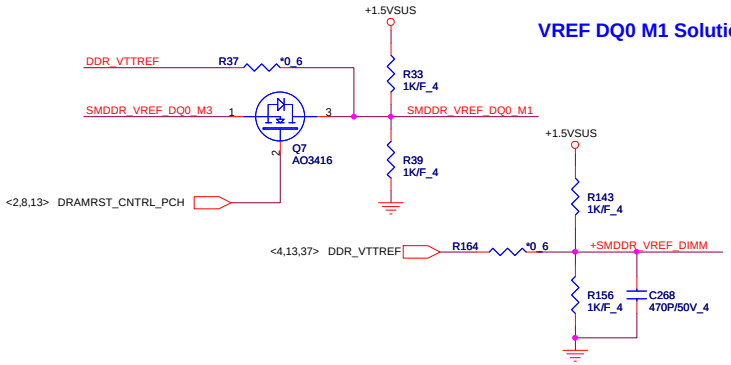
VREF DQ0 M2 Solution

del M2 solution

Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

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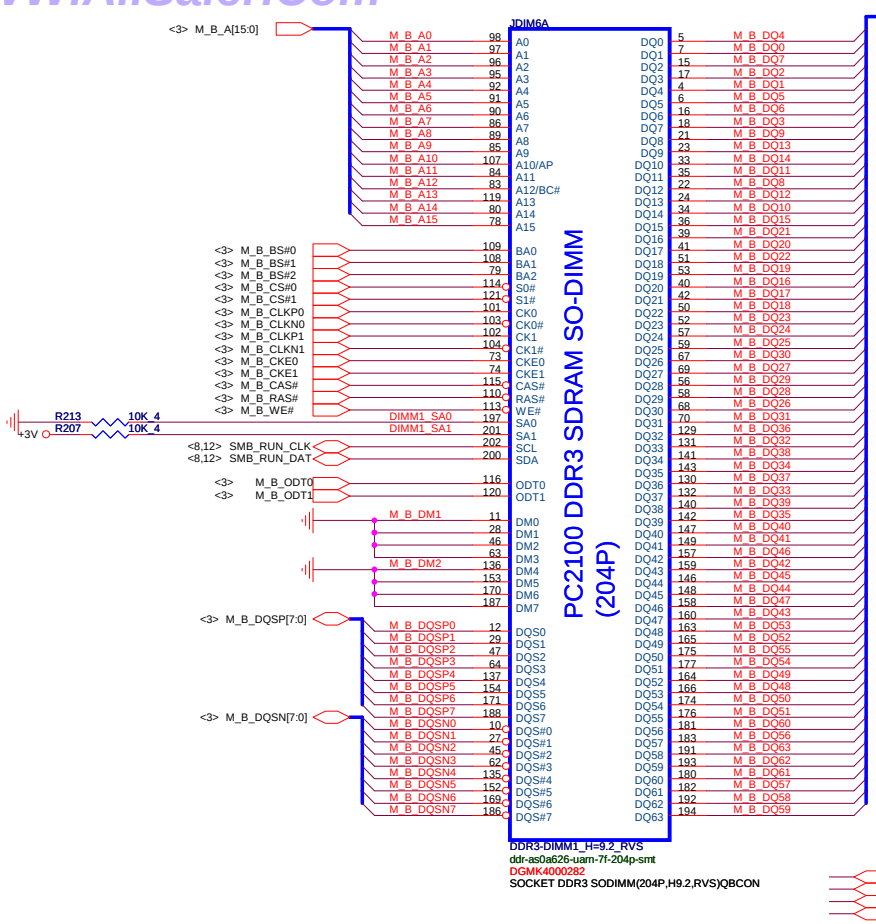
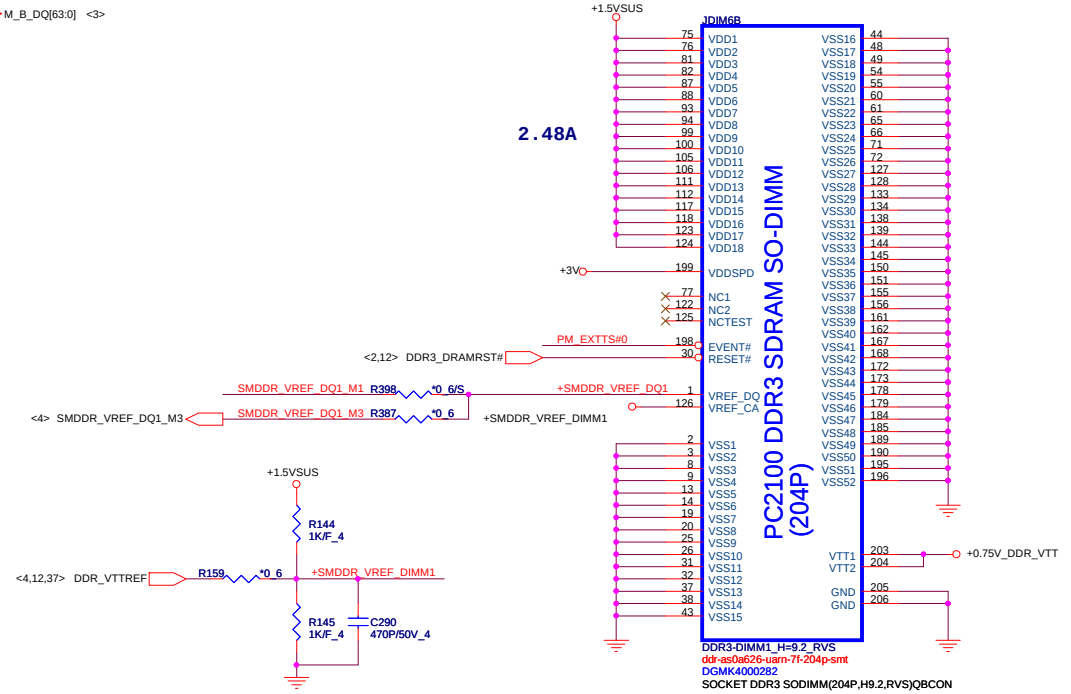
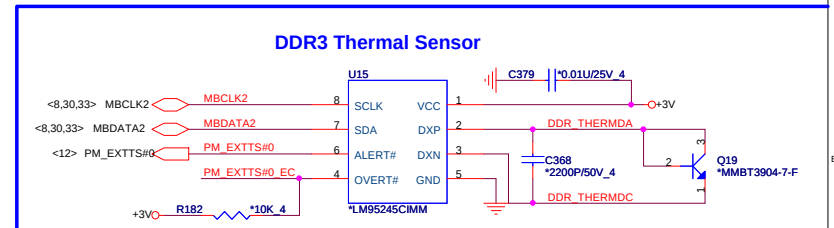
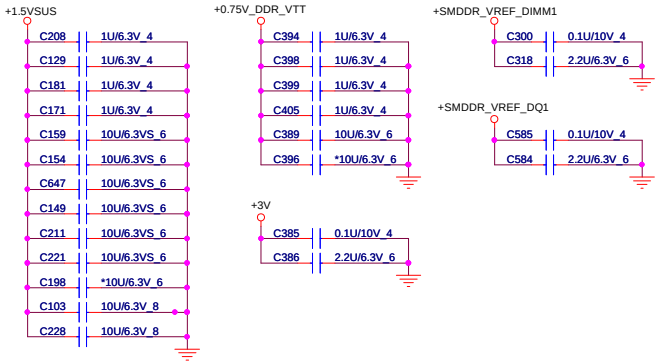
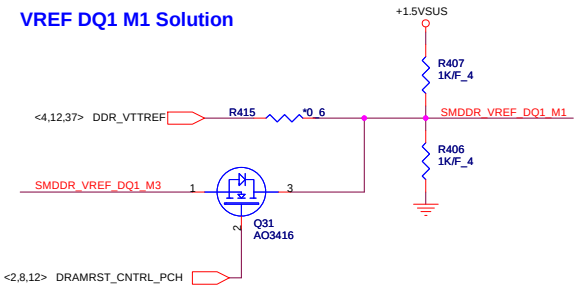






del M2 solution





PROJECT :R33
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Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

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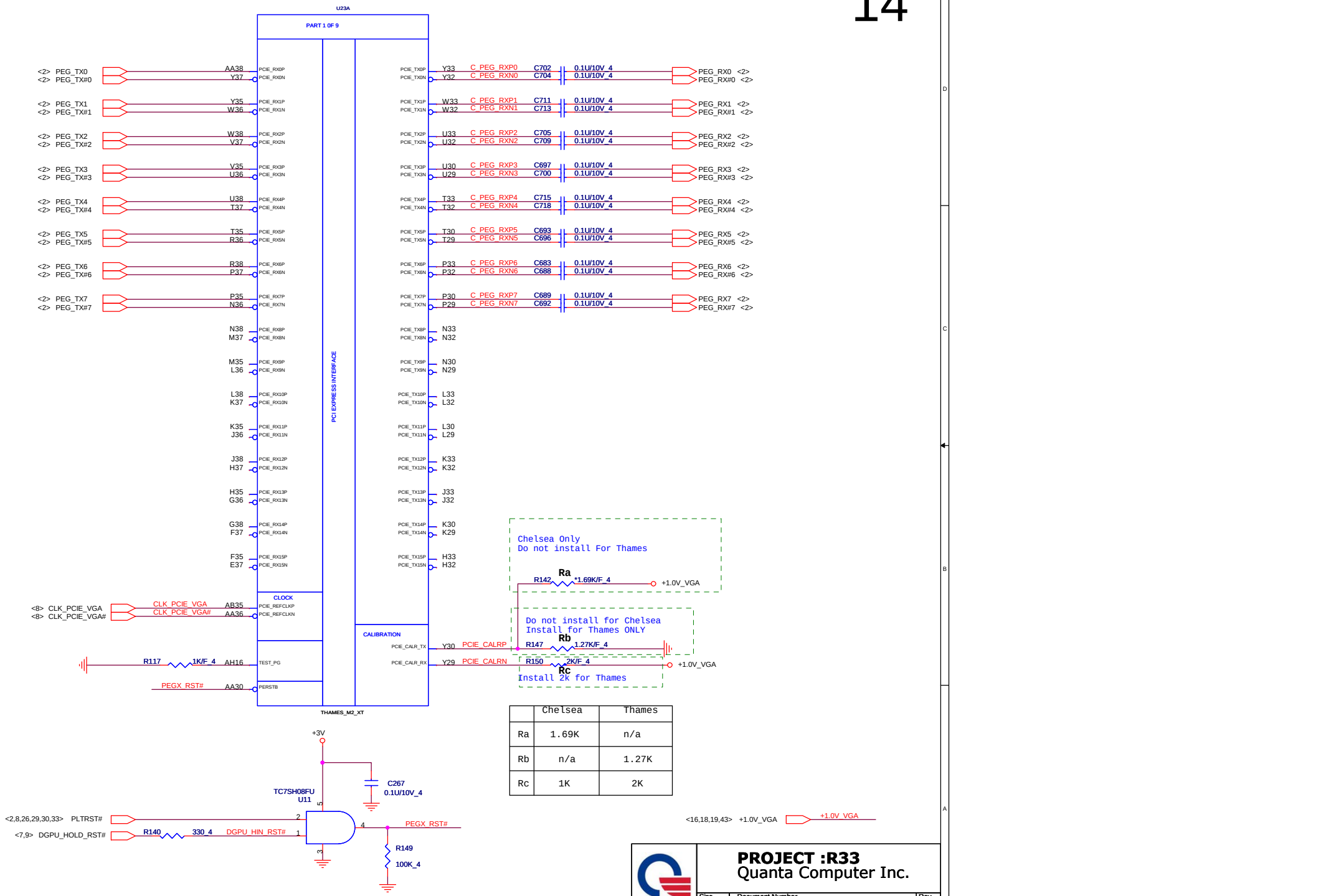

	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_PCIE_Interface	1A

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MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D (VEGA)	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- B (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63BFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110	Micron- K die	128Mx16 *8, 900Mhz	MT41J128M16JT-107G:K
0111	Samsung- E die	128Mx16 *8, 900Mhz	K4W2G1646E-HC11
1000	Reserve		
1001	Hynix- D (VEGA)	128Mx16 *8, 900Mhz	H5TQ2G63DFR-11C
1010			
1011			
1100			
1101			
1110			
1111			

GPIO16 GPIO20 GPIO15

Thames XT	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

Memory ID

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.

Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames

PS_1, PS_2, PS_3 are NC on Thames
Do not install for Thames

PV, change to 0ohm
PV, change to 0ohm
PV, change to DNI

Reserve for Power Play

PROJECT :R33
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Size	Document Number	Rev
Custom	THAMES_Main & GND	1A

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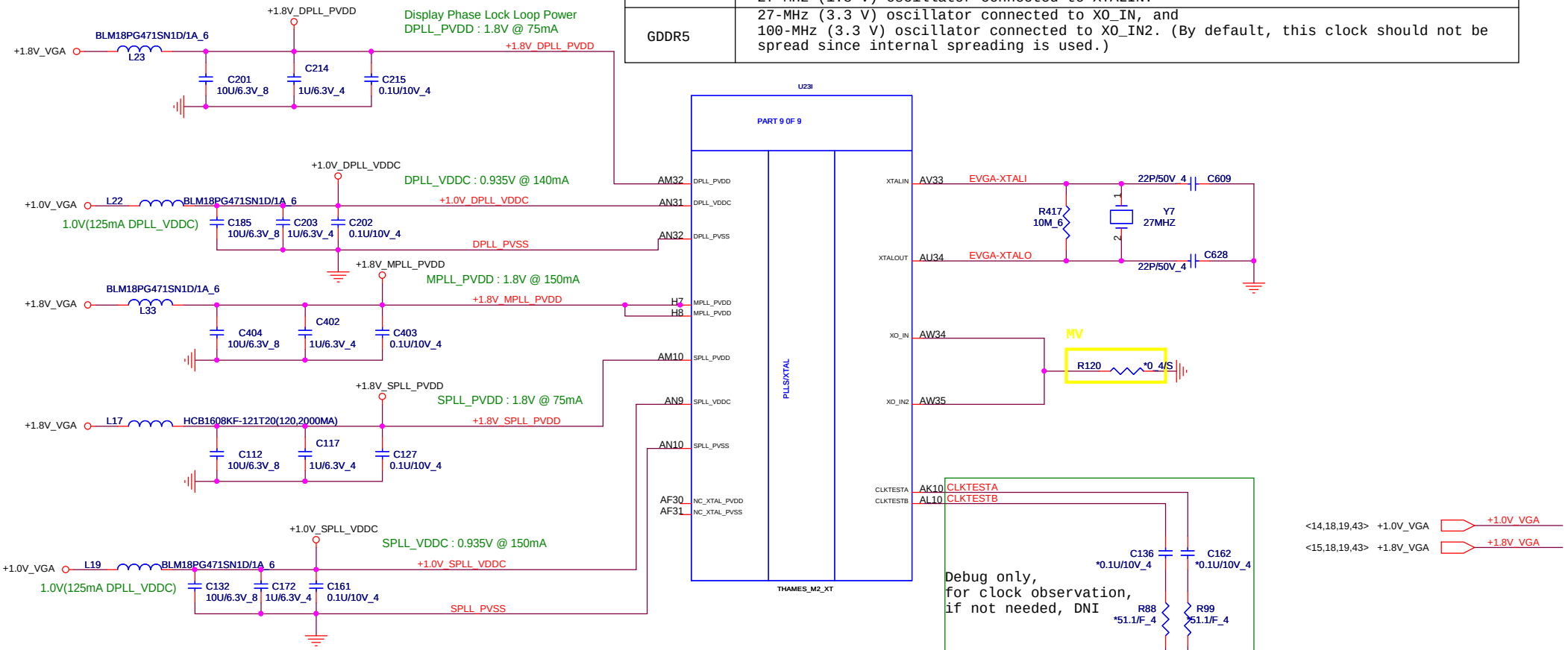
Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_XTAL	1A

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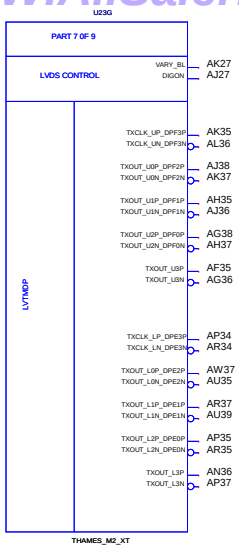
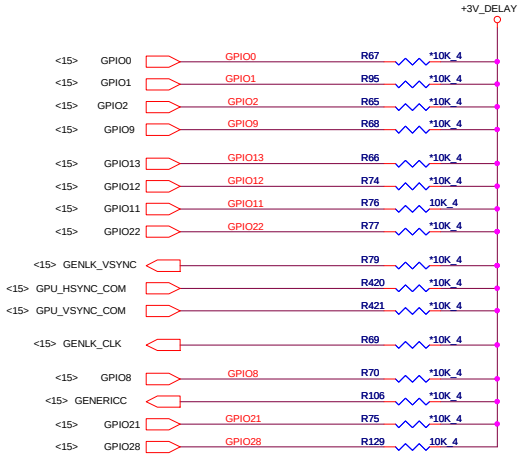




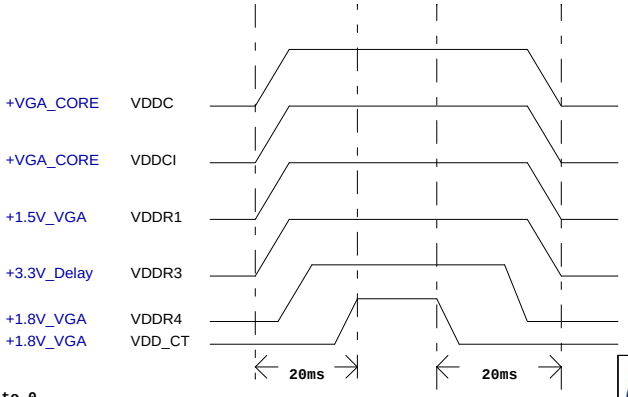
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_LVDS / STRAP	1A
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VDDR1 , 1.5V @ 2A, GDDR5 900MHz

I/O power for the memory interface.

PV, change to 0ohm

VDDC_CT: 1.8V @250mA

VDDR3 : 3.3V @ 60mA

VDDR4 : 1.8V @ 300mA

PV, change to DNI

Reserve for Drop

PCIe I/O power.
PCIE_VDDR : 1.8V @ 200mA

PCIe Digital Power Supply
PCIE_VDDC : 0.935V @ 1.88A (GEN2.0)
PCIE_VDDC : 0.935V @ 2.5A (GEN3.0)

	Ra	Rb	Rc	Rd
Chelsea-non BACO	install	na	na	na
Chelsea-BACO	install	na	na	na
Thames-non BACO	na	install	install	install
Thames-BACO	na	na	install	install

VDDCI 0.8-1.15V @ 6A

Support BACO Mode

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

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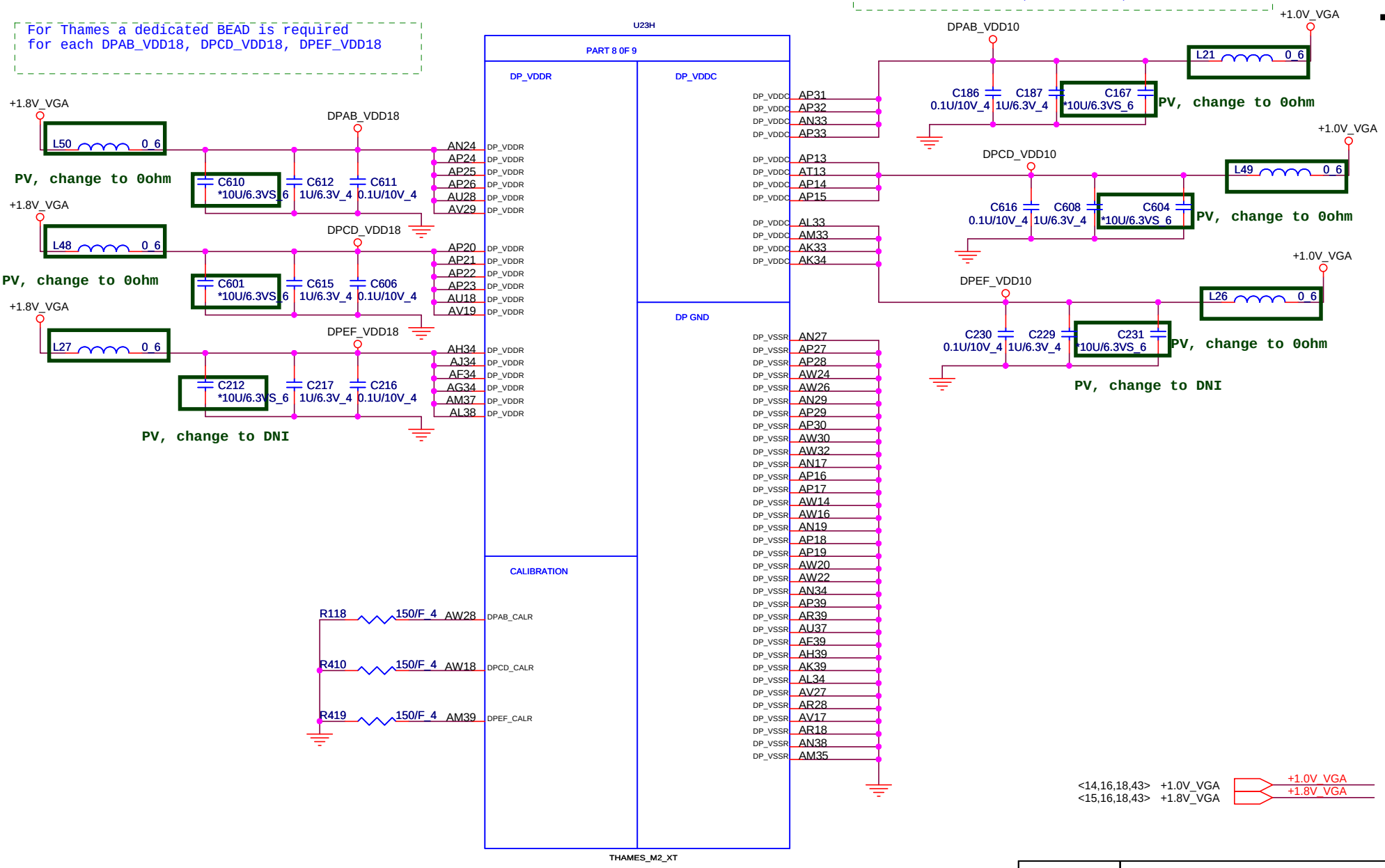
Size: Custom | Document Number: THAMES_Power & BACO | Rev: 1A

Date: Tue, Sep 07, 2012 | Sheet 18 of 43

For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10



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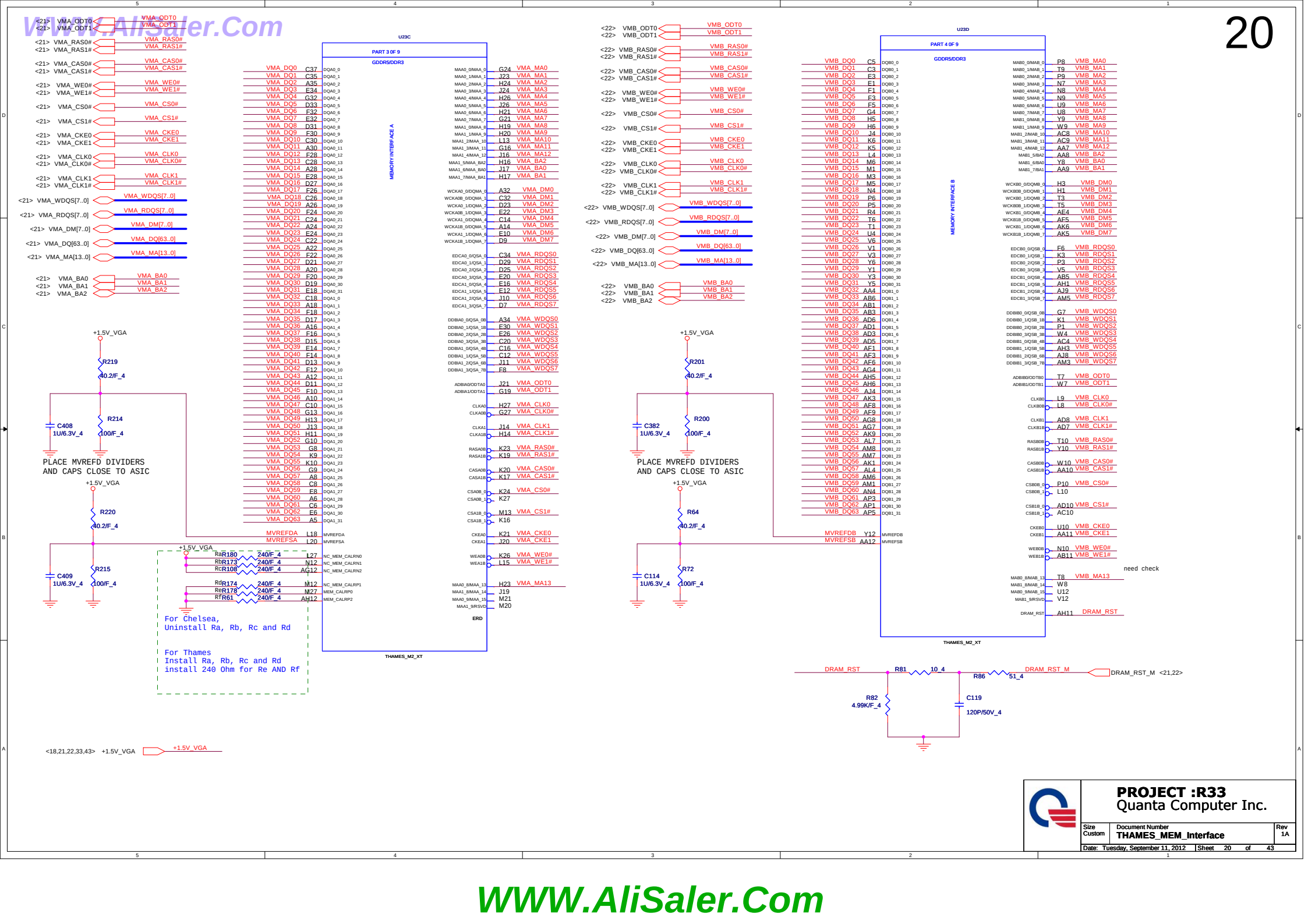
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_DP Powers	1A
Date: Friday, September 07, 2012	Sheet 19 of 43	



PROJECT :R33 Quanta Computer Inc.		
Size: Custom	Document Number: THAMES_MEM_Interface	Rev: 1A
Date: Tuesday, September 11, 2012	Sheet 20 of 43	

CHANNEL A: 256MB/512MB DDR3

Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

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Quanta Computer Inc.
VRAM-A (DDR3 BGA96)
Size: Custom | Document Number | Rev: 3A
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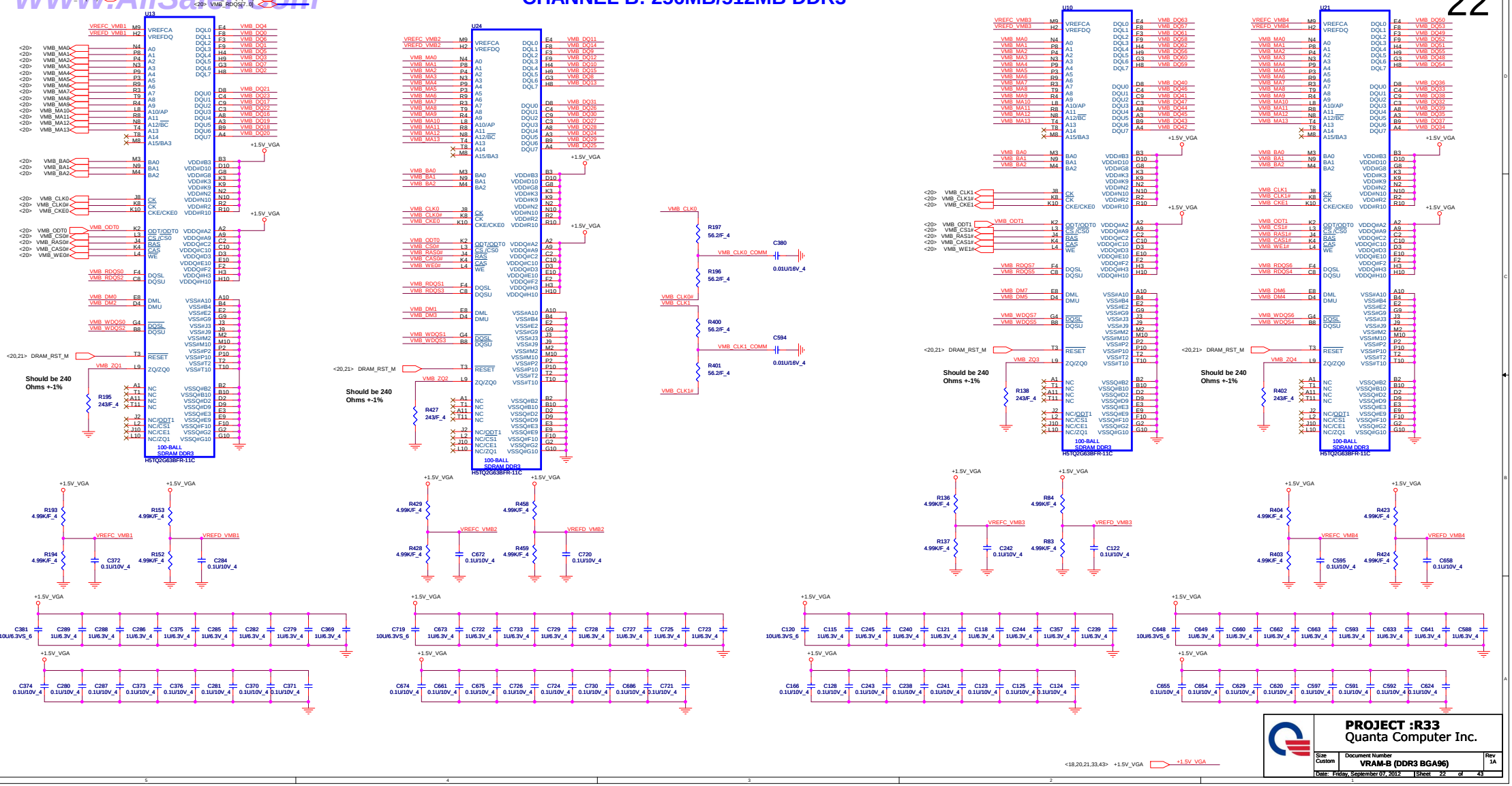
CHANNEL B: 256MB/512MB DDR3



PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-B (DDR3 BGA96)	1A

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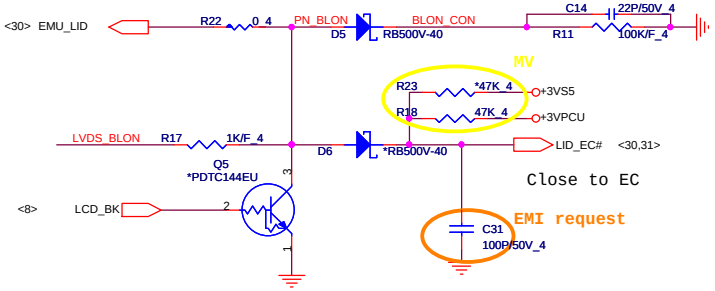
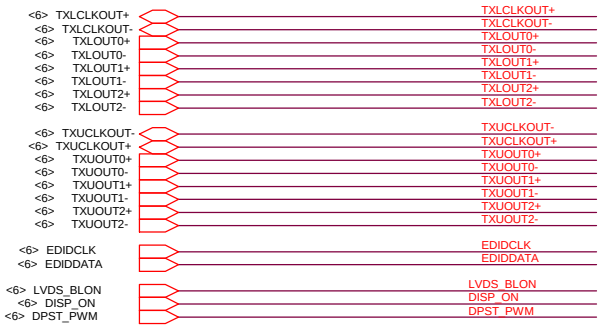
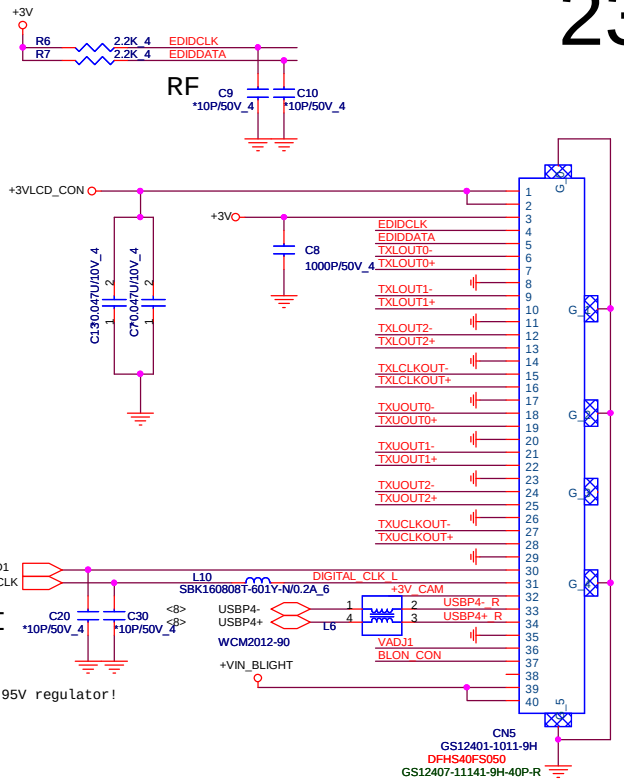
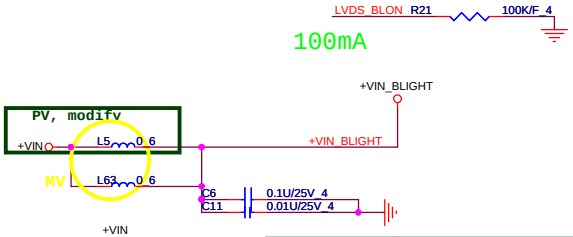
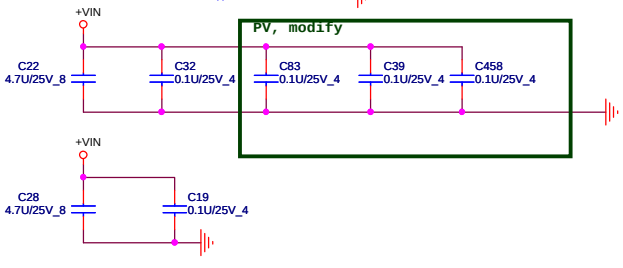
LID Switch

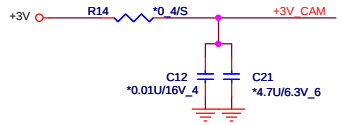




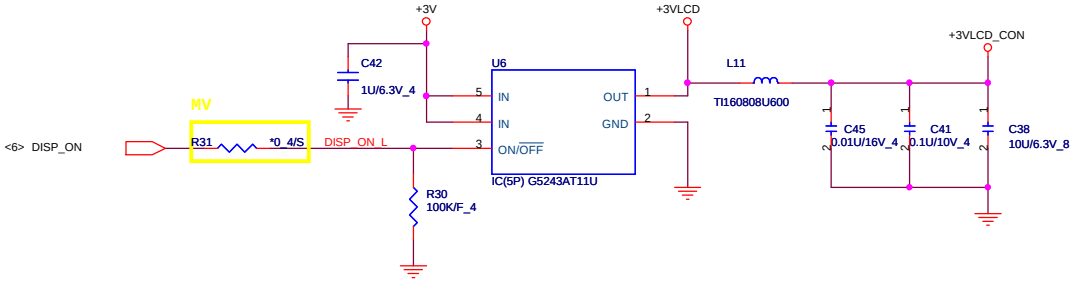








Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!



PROJECT :R33 Quanta Computer Inc.		
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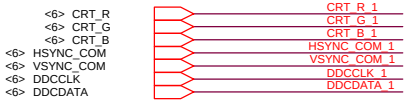
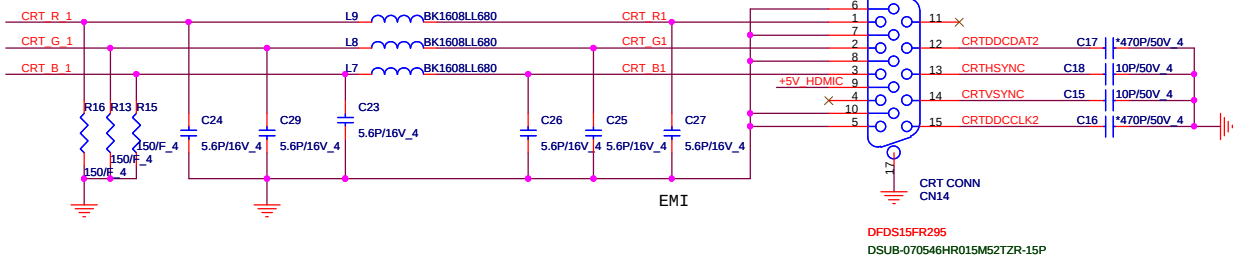
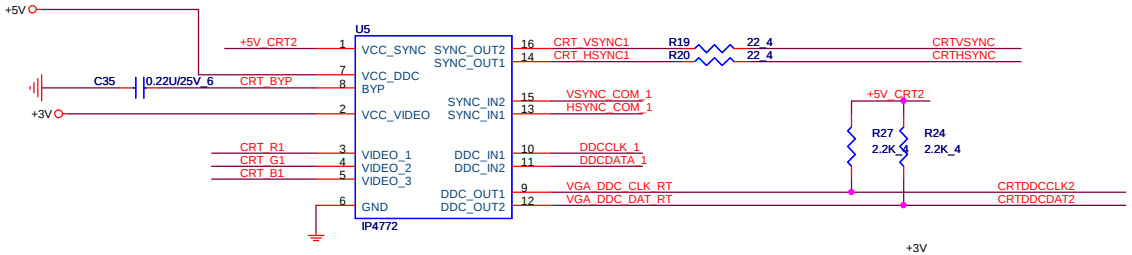
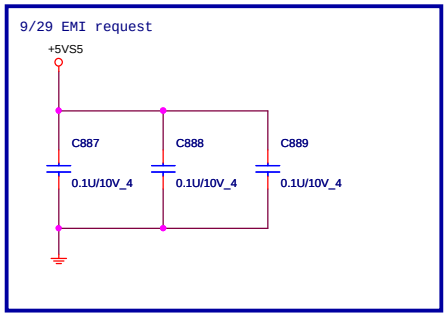
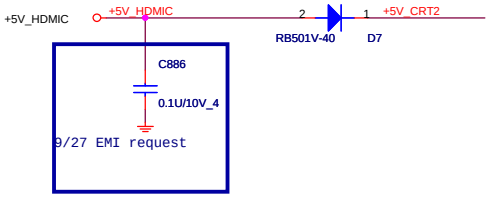
CRT PORT



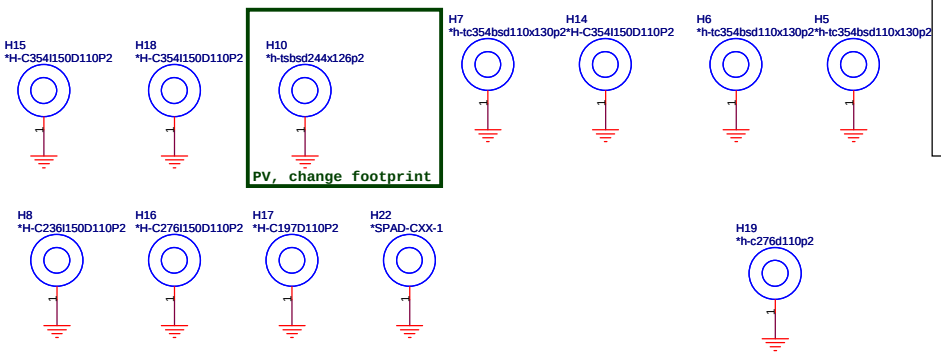


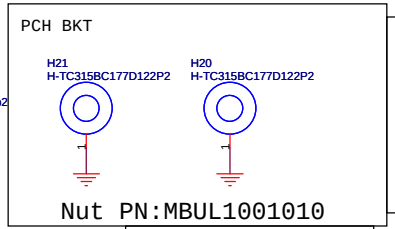


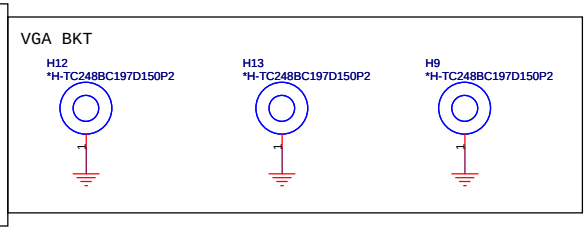


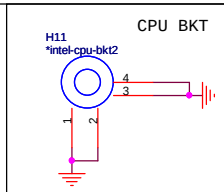


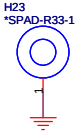
HOLE











PROJECT :R33 Quanta Computer Inc.		
Size: Custom	Document Number: CRT,Hole	Rev: 1A
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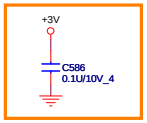
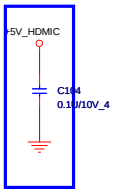
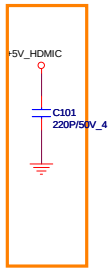
EMI request



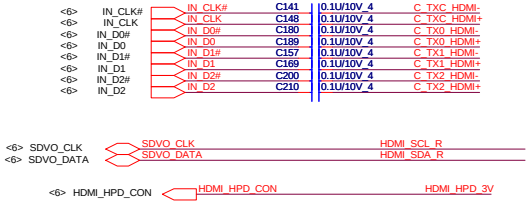
EMI request



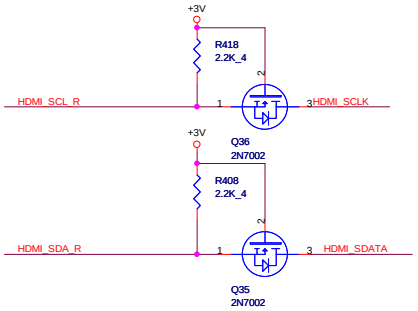
Add for EMI

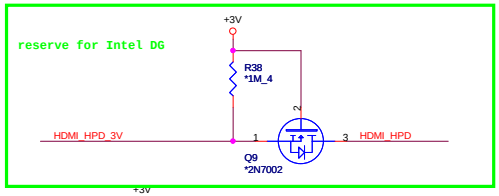


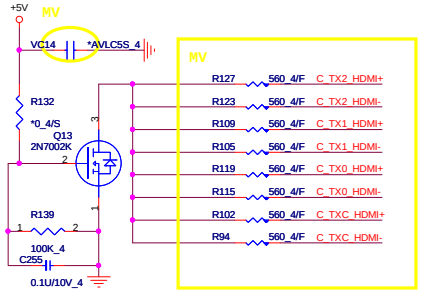
close to HDMI conn

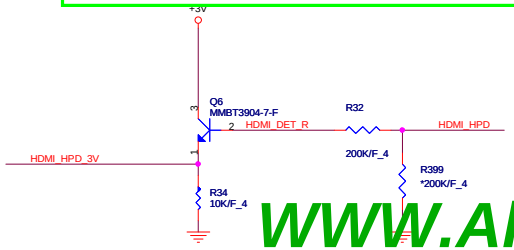


DISCRETE HDMI I2C SELECT
Close to HDMI Connector

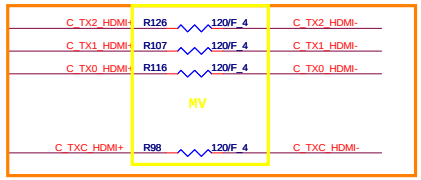


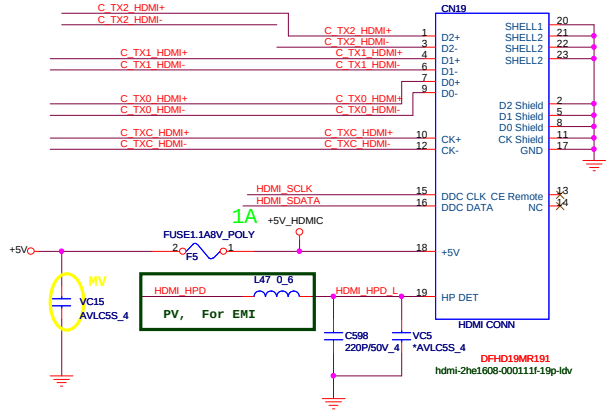


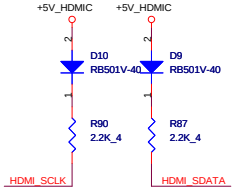




EMI request







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Quanta Computer Inc.

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Custom	HDMI CONN	1A

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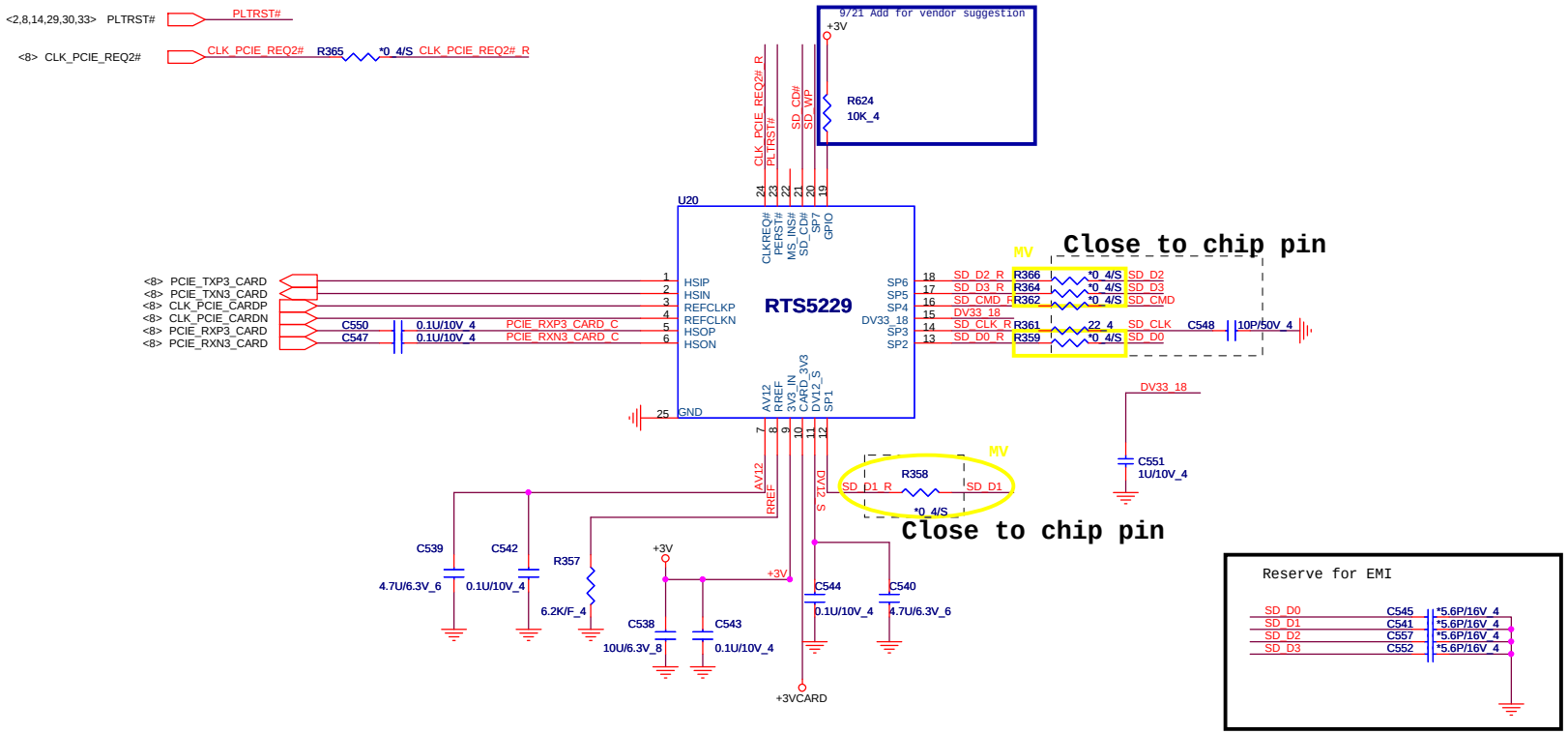
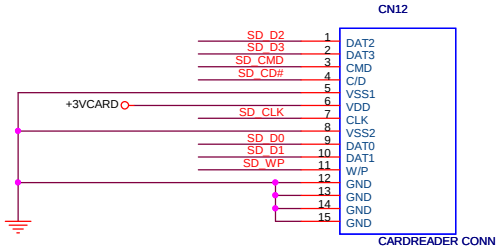
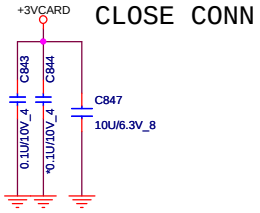


SD / MMC CARD READER





PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5229 & CR SOCKET	1A

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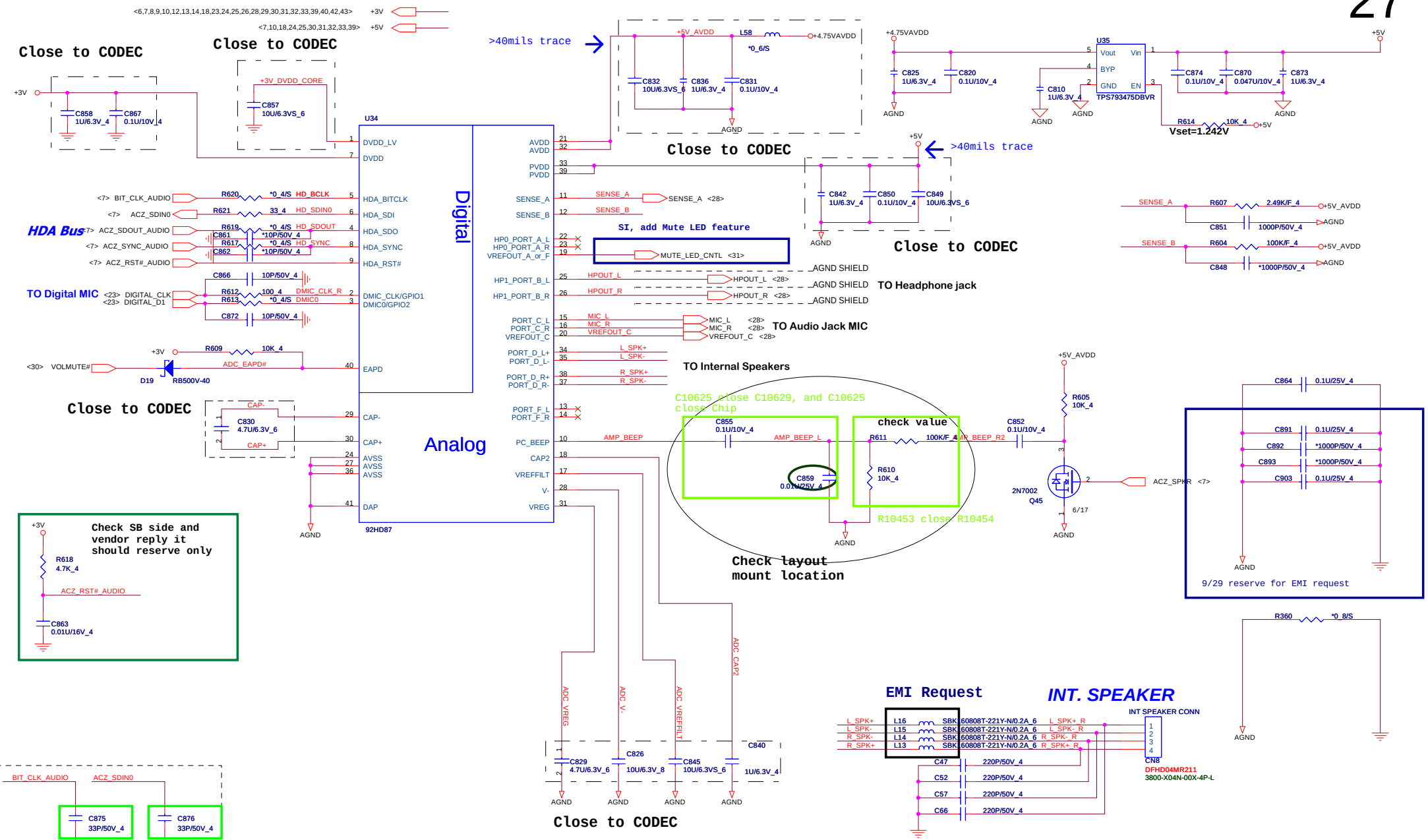

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Quanta Computer Inc.		
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USB3.0 X 2/USB2.0 COMBO

USB 3.0

SI EMI request

EMI request

1A

C739 1000P/50V_4

CN21 USB3.0 CONN

L36 WCM2012-90

USBP0- C C407 *Clamp-Diode

USBP0+ C C412 *Clamp-Diode

USB30_TX1- C C401 *Clamp-Diode

USB30_TX1+ C C383 *Clamp-Diode

USB30_RX1- C C422 *Clamp-Diode

USB30_RX1+ C C419 *Clamp-Diode

R227 *0_4/S

R225 *0_4/S

C395 0.1U/10V_4

C387 0.1U/10V_4

R208 *0_4/S

R203 *0_4/S

USB 3.0

SI EMI request

EMI request

1A

C765 1000P/50V_4

CN22 USB3.0 CONN

L41 WCM2012-90

USBP1- C C465 *Clamp-Diode

USBP1+ C C476 *Clamp-Diode

USB30_TX2- C C457 *Clamp-Diode

USB30_TX2+ C C447 *Clamp-Diode

USB30_RX2- C C479 *Clamp-Diode

USB30_RX2+ C C478 *Clamp-Diode

R249 *0_4/S

R247 *0_4/S

C455 0.1U/10V_4

C451 0.1U/10V_4

R243 *0_4/S

R242 *0_4/S

U30 G547N2P81U 80 mils (Iout=2A)

C793 1U/6.3V_4

C741 470P/50V_4

C740 0.1U/10V_4

C791 470P/50V_4

C782 100U/16V

VC12 AVLC5S_4

VC13 AVLC5S_4

Right SIDE USBX1

C43 0.1U/10V_4

L12 WCM2012-90

EMI request

SATA_LED#

PWRLED_RIGHT

C37 1000P/50V_4

C36 1000P/50V_4

C40 220P/50V_4

C879 0.1U/10V_4

C74 1000P/50V_4

CN6 USB CONN

9/27 EMI request

Line out

AGND SHIELD

HPOUT_L

HPOUT_R

R327 16/F_4

R313 16/F_4

BLM18BD601SN1D L46

BLM18BD601SN1D L45

R317 *20K/F_4

R333 *20K/F_4

C507 1000P/50V_4

C522 1000P/50V_4

VC11 *AVLC5S_4

VC9 *AVLC5S_4

C526 0.1U/10V_4

C518 0.1U/10V_4

CN24 HP-JACK-BLACK Normal Open

SENSE_PHONE

VC10 *AVLC5S_4

R312 20K/F_4

SENSE_A

SENSE_MIC

R283 10K/F_4

VC6 *AVLC5S_4

MIC

VREFOUT_C

C486 1U/6.3V_4

R297 3.9K/F_4

R300 3.9K/F_4

MIC_L

MIC_R

C799 2.2U/6.3V_6

C794 2.2U/6.3V_6

BLM18BD601SN1D L44

BLM18BD601SN1D L43

C485 220P/50V_4

C491 220P/50V_4

VC7 *AVLC5S_4

VC8 *AVLC5S_4

CN23 HP-JACK-BLACK Normal Open

COMPONENT CHOICES:
The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T

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Quanta Computer Inc.

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For EMI 0 ~ 22 ohm

9/27 EMI request

GND VIA x 9 Pcs

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

RJ45

PV EMI request

FOR EMI

Link

PROJECT :R33
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8105E/RJ45	1A

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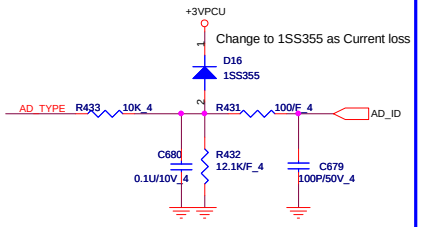
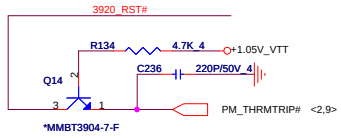
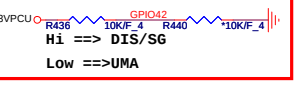
adapter Type check



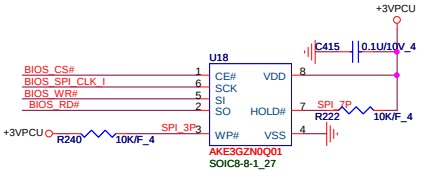


adapter select for EC



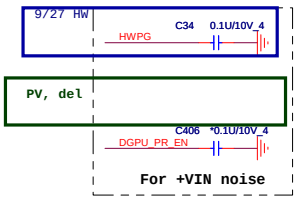
Socket: DFHS08FS023
AMIC AKE3GZP0801
EON AKE3GZN0Q01

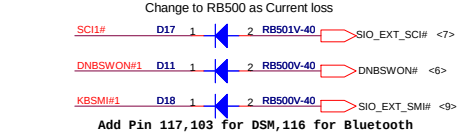
1M byte SPI EC ROM

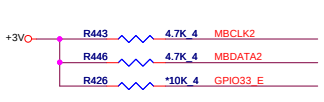


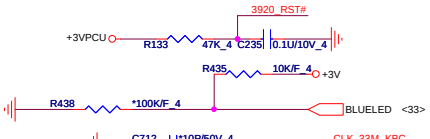
TP SM bus

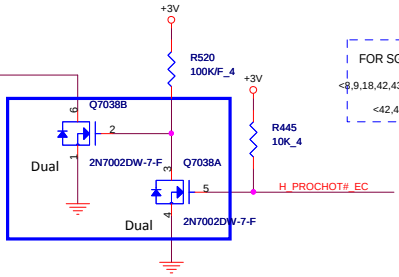
PV, del

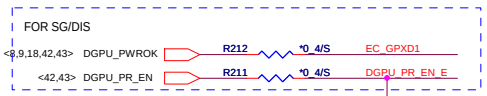


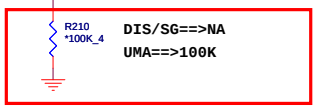












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Quanta Computer Inc.

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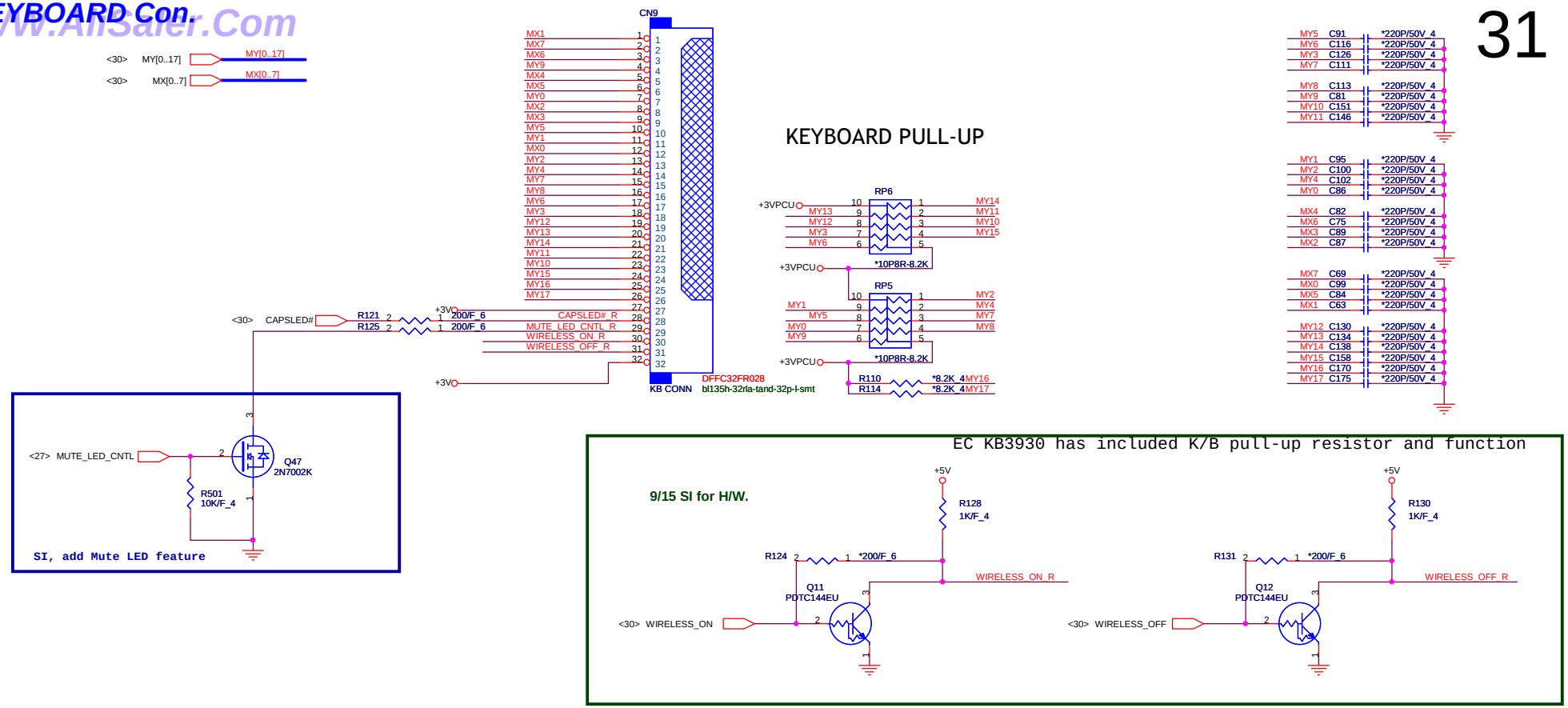
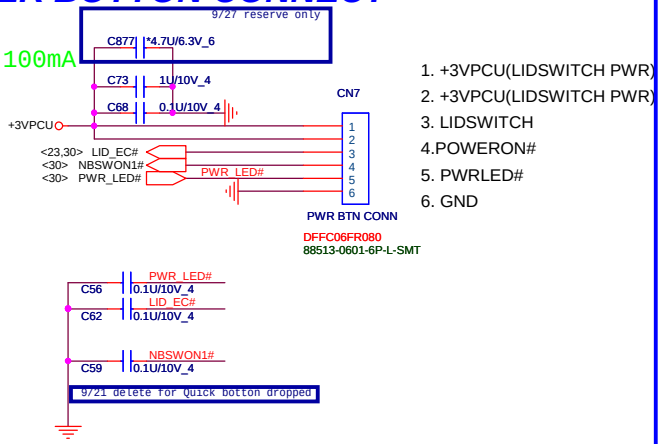
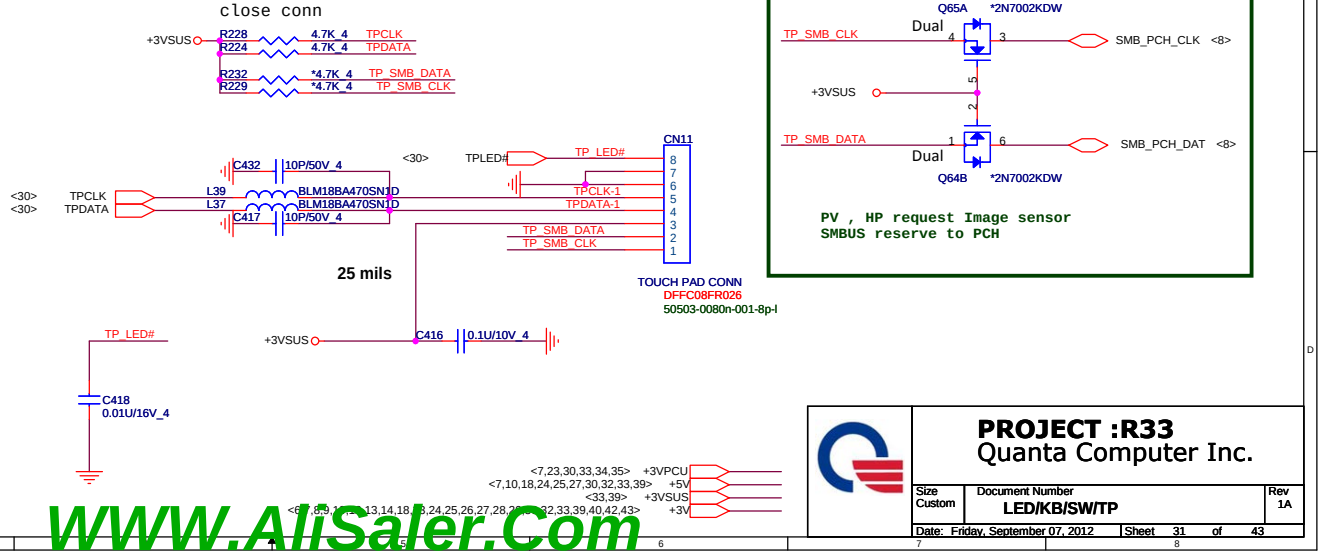
KEYBOARD Con.



POWER BOTTON CONNECT



TOUCH PAD Con.



Quanta Computer Inc.	PROJECT :R33	
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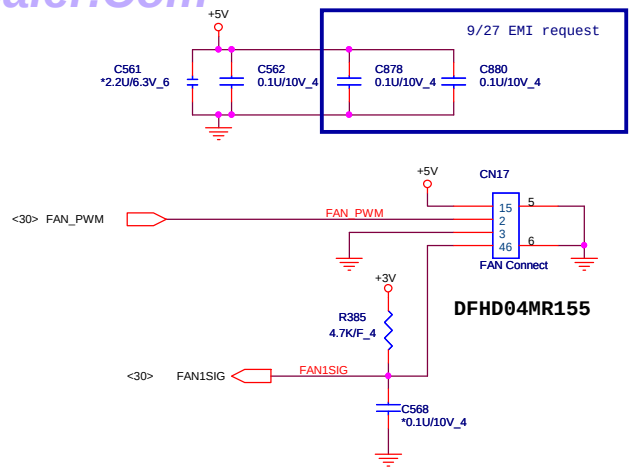
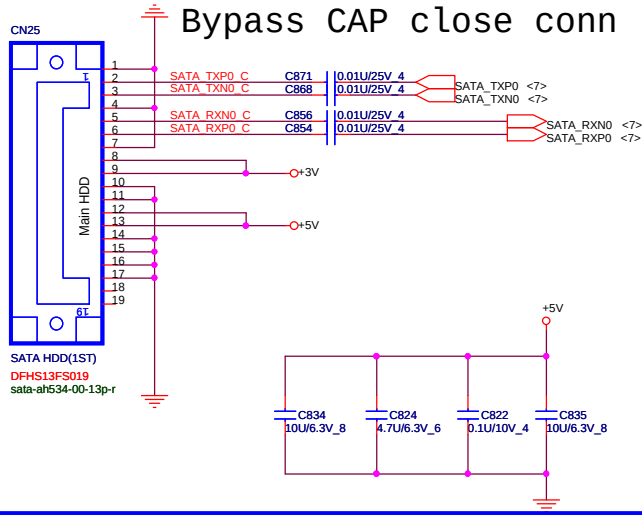
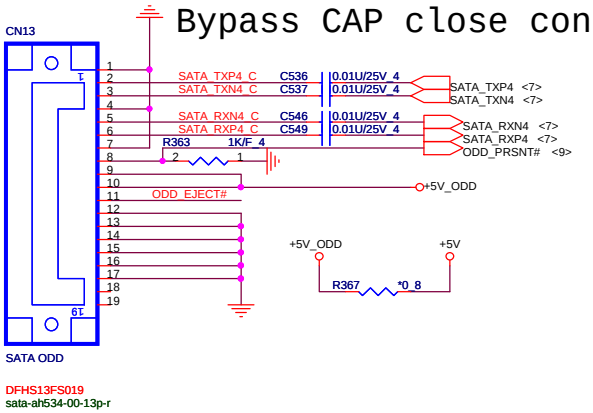
CPU FAN

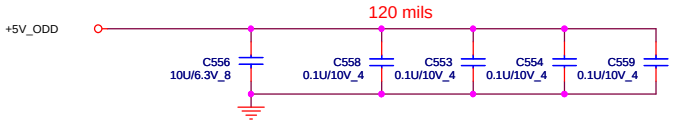


SATA HDD CONNECTOR

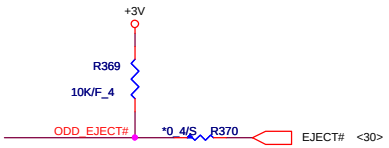


SATA ODD CONNECTOR

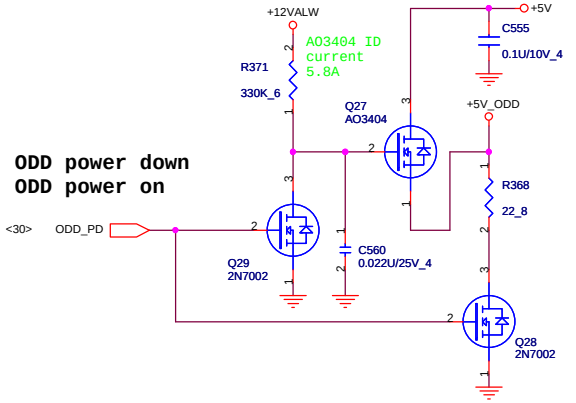




follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



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Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

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Mini PCI-E Card 1
WLAN

33

9/6 SI for HW.

FOR KBC DEBUG

EC debug pin

CN18

MINI PCIE H=11
DFHS52FR097
MIPCI-C-1759513-52P-LDV-SMT

BT_DATA, BT_CHCLK, CLKREQ# internal pull-DOWN 100k ohm

INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

PV, add for AOAC

PV, add for AOAC

Reserve for AOAC function

24mil

for EMI request

Accelerometer Sensor

U12
HP3DC2TR
AL003DC2A00

9/27 EMI request

SI for +VIN noise issue

PV, reserve

MV

MV

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Size	Document Number	Rev
Custom	MINI PCIE CONN & G-sensor	1A
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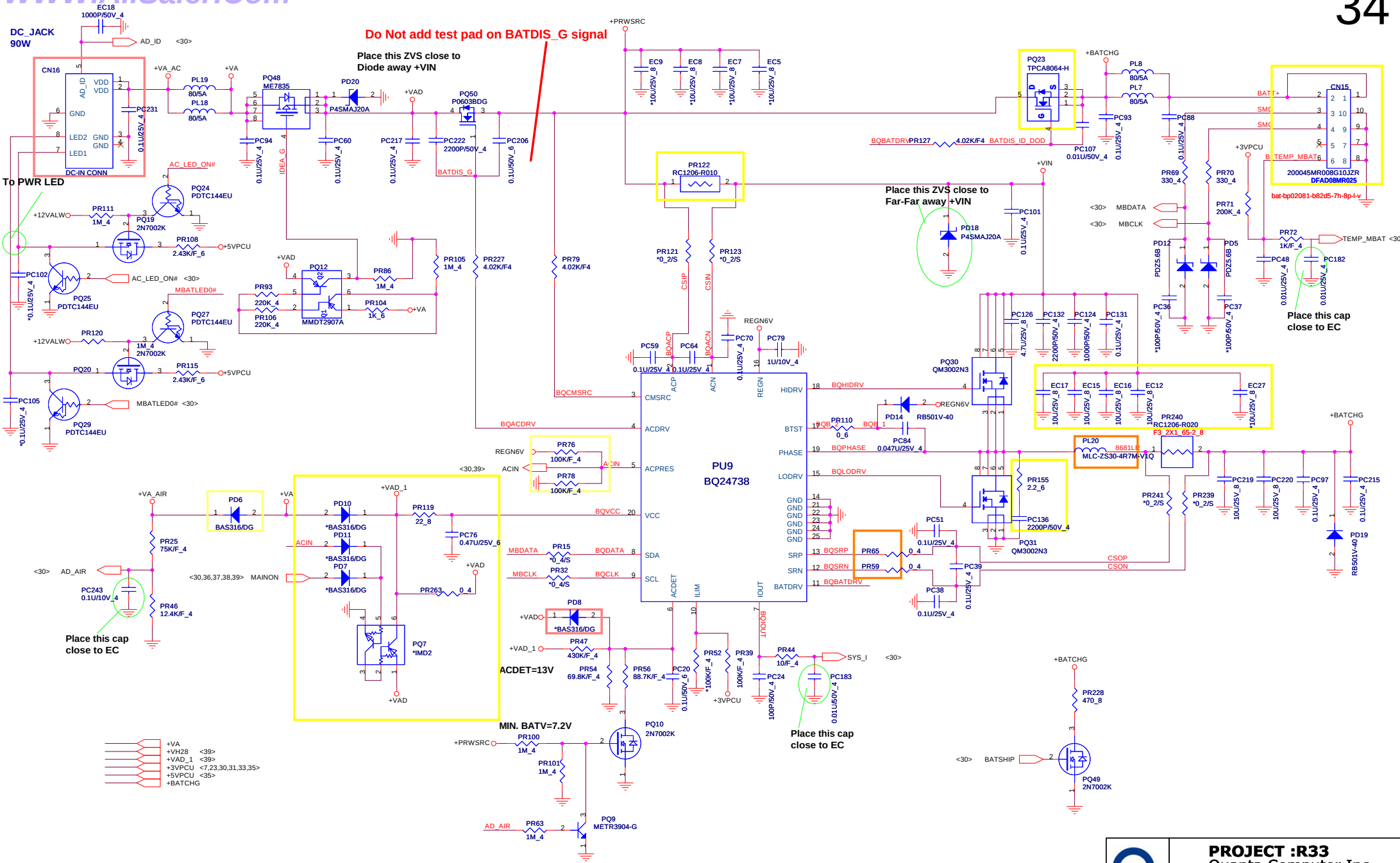

+VA	<39>		
+VH28	<39>		
+VAD_1	<39>		
+3VPCU	<7,23,30,31,33,35>		
+5VPCU	<35>		
+BATCHG			

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Size	Document Number	Rev
Custom	Charger (OZ8681)	1A

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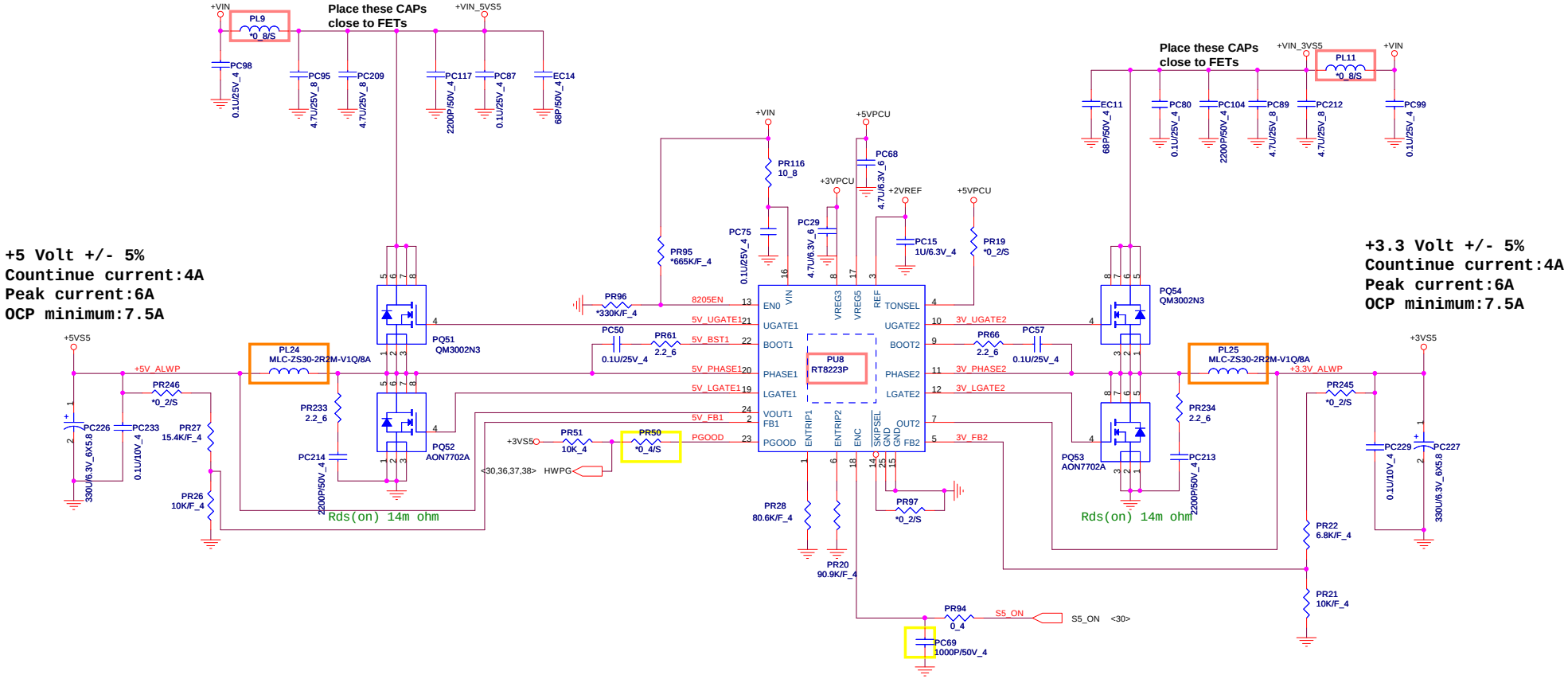

Size: Custom	Document Number: 3/5VPCU(RT8223P)	Rev: 1A
Date: Friday, August 31, 2012	Sheet 35 of 43	

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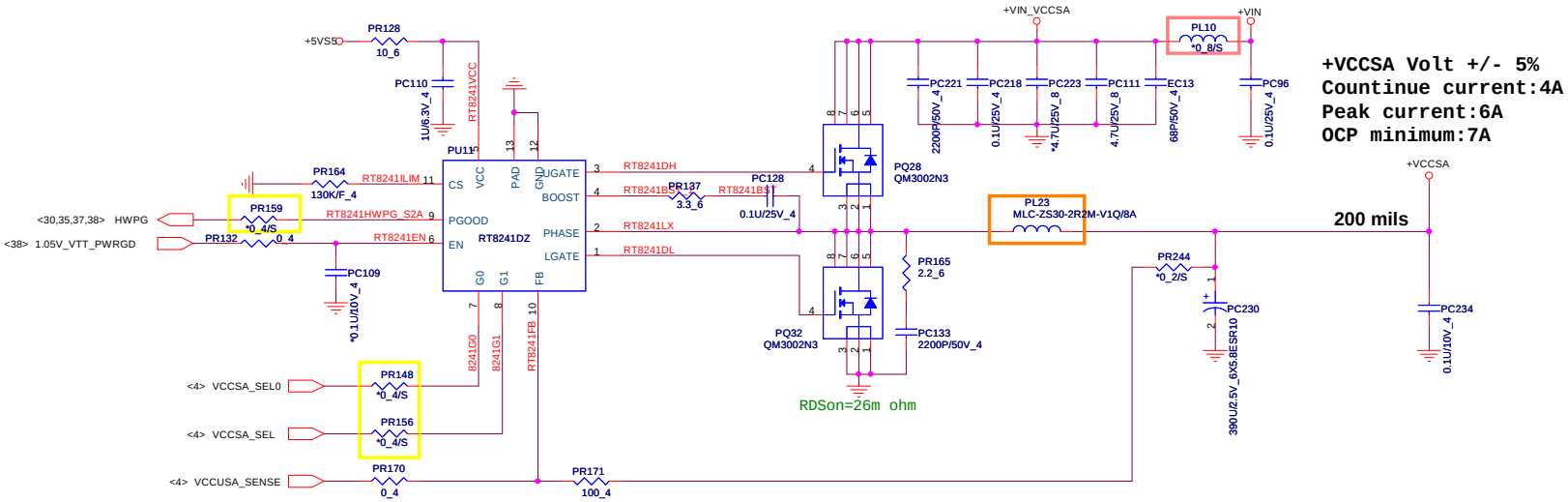
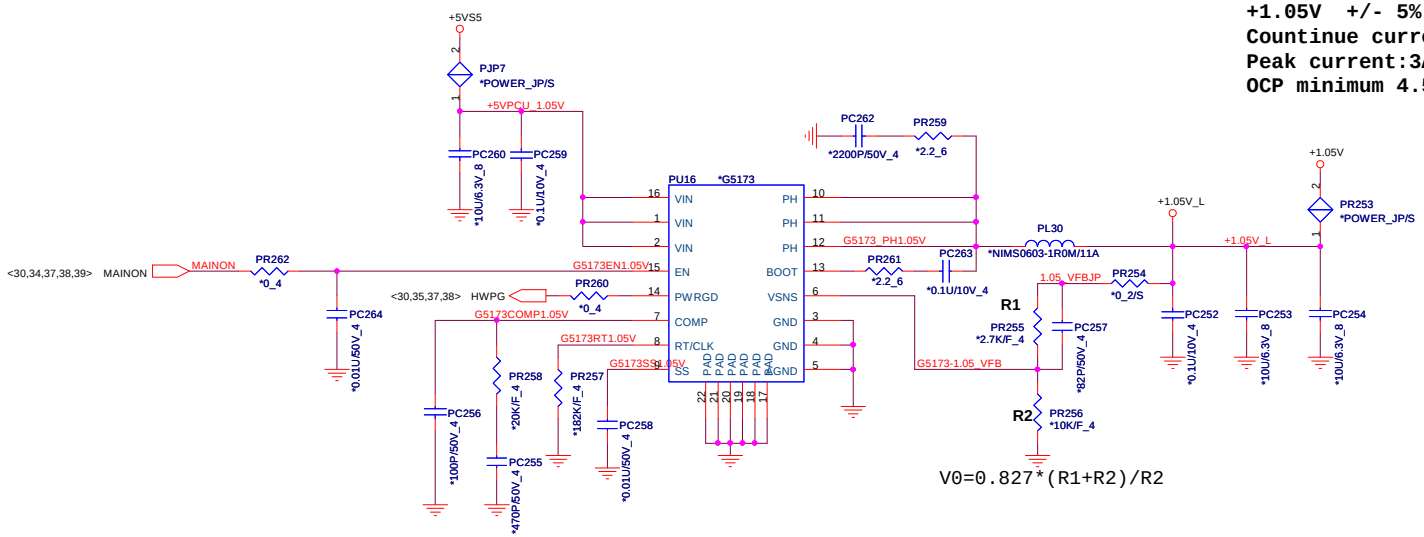
Quanta Computer Inc.



CPU system agent
voltage slew rate of 0.5 -10 mV/µs

H_FC_C22 VID0	VCCSA_SEL VID1	Vout
0	0	0.9V
0	1	0.80V (SV-RT8241DZGQW) 0.85V (LV-RT8241EZGQW)
1	0	0.725V
1	1	0.675V



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Size	Document Number	Rev
Custom	VCCSA (RT8241EZ)	1A
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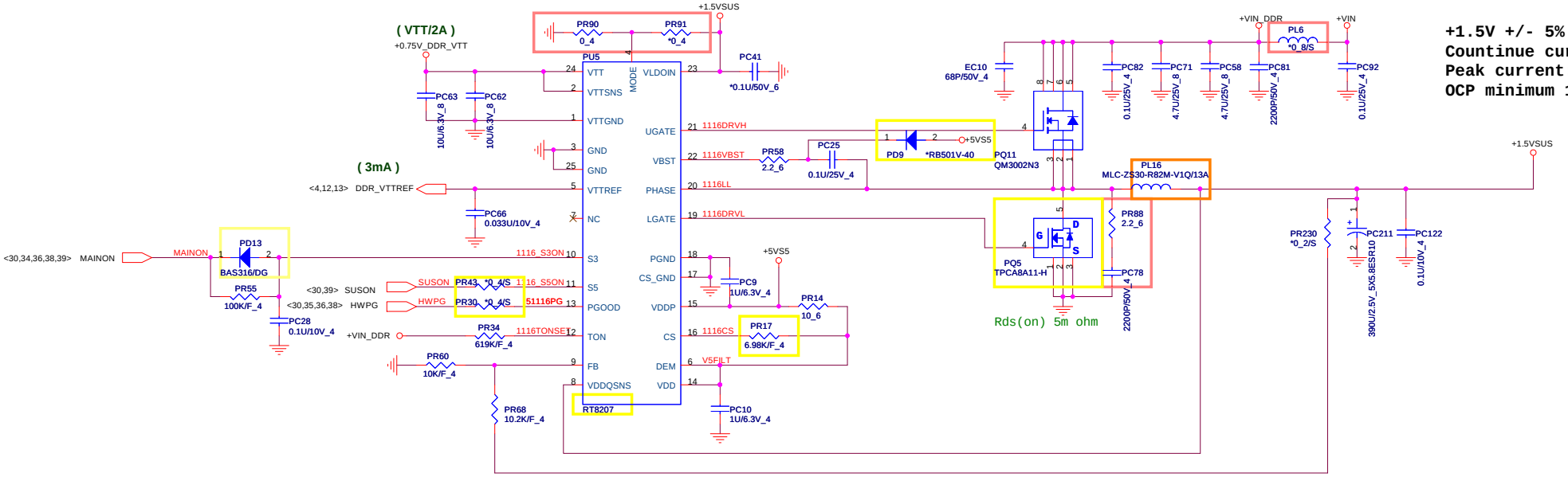

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 15A

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Size	Document Number	Rev
Custom	DDRIII(RT8207LGQW)	1A
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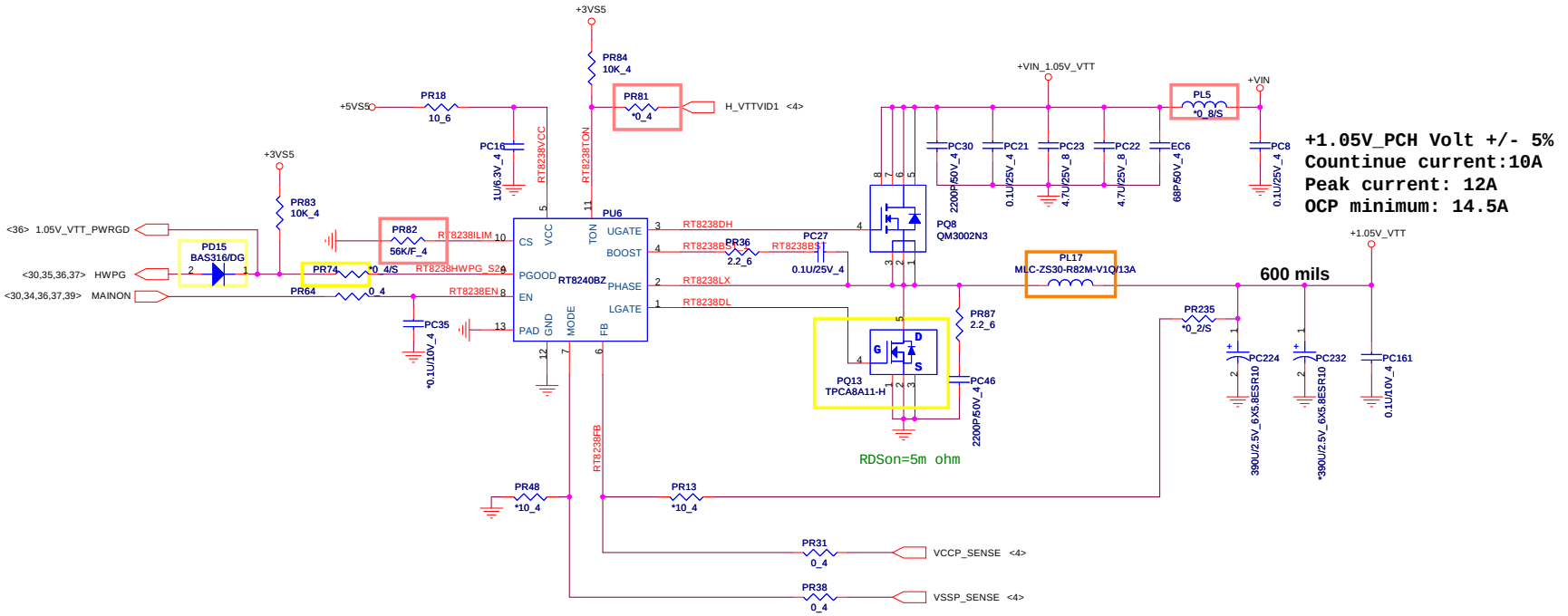
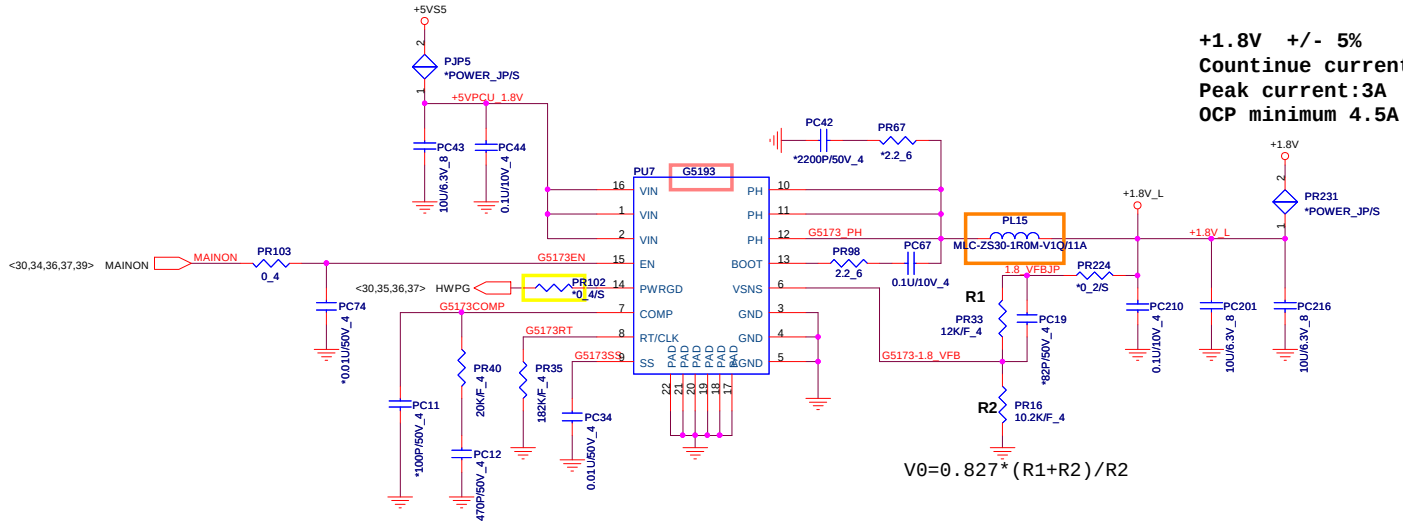
1.05V_VTT





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Size	Document Number	Rev
Custom	1.0V(RT8228BZ)/1.8V(G5173)	1A
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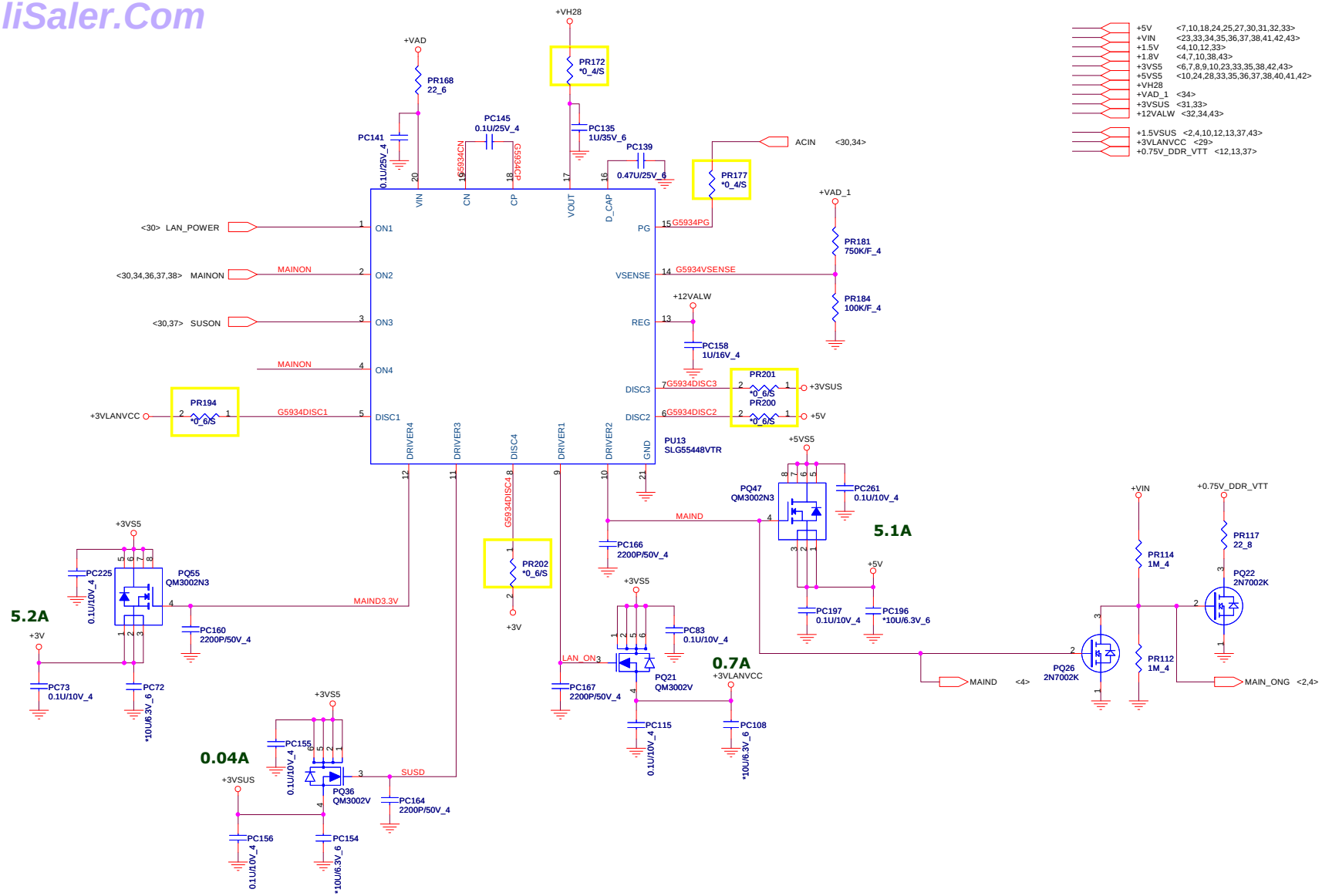

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Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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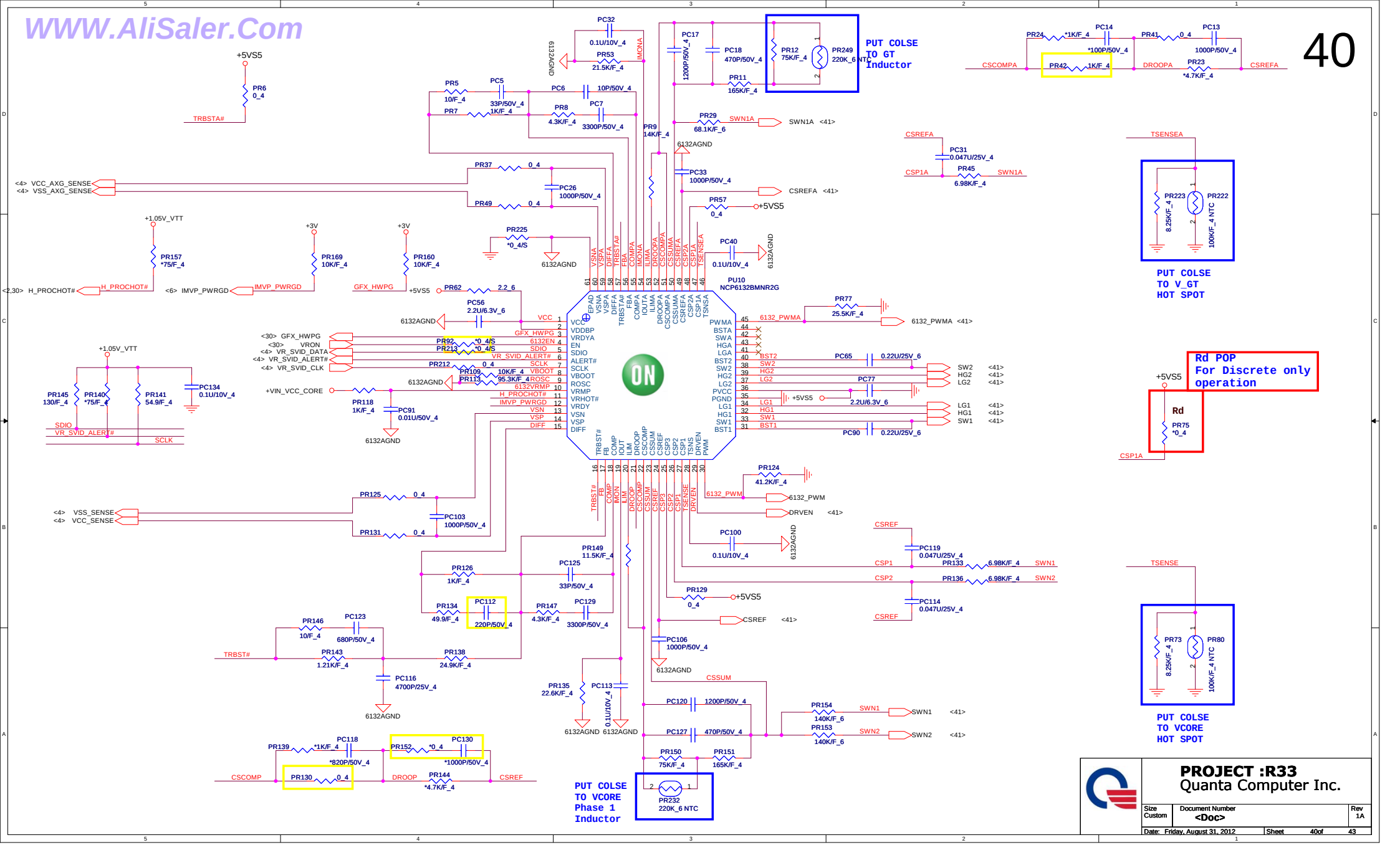
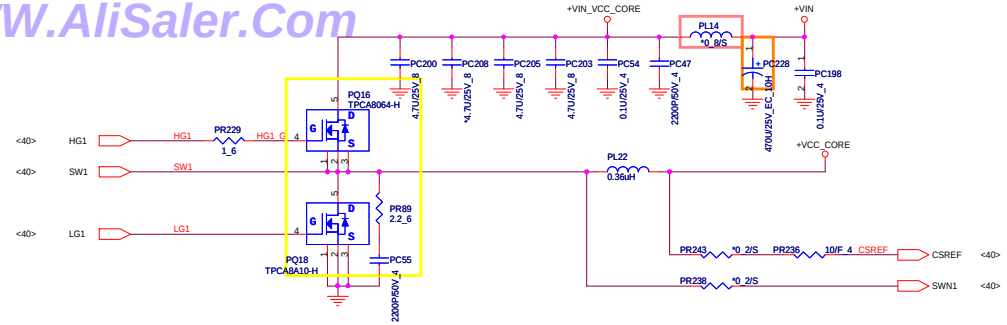
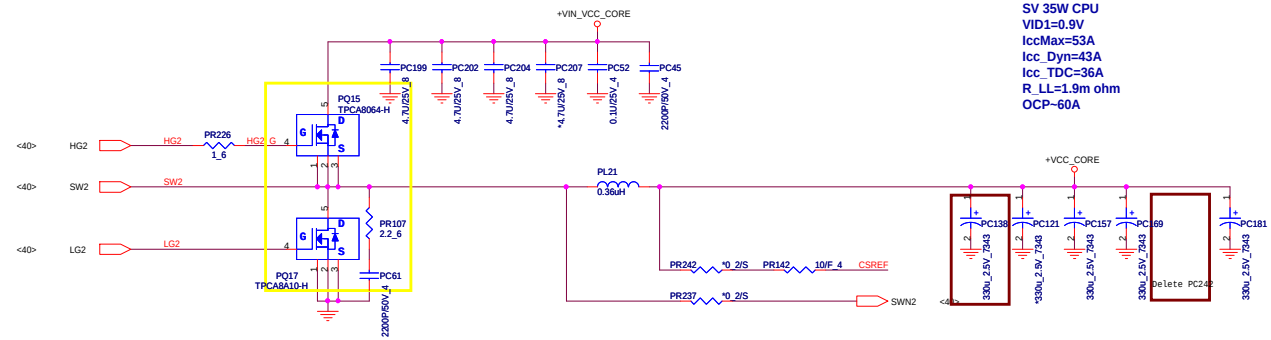
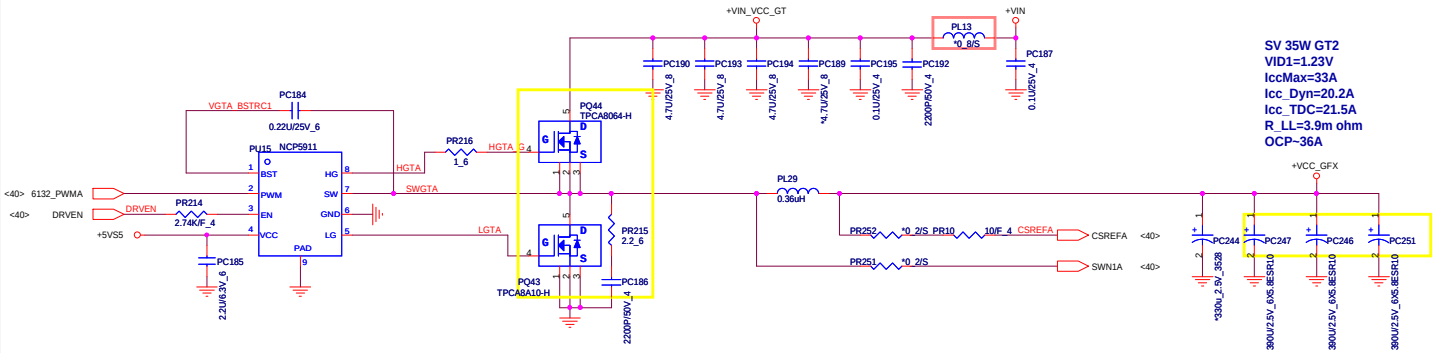






SV 35W CPU
VID1=0.9V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~60A



SV 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~36A

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C	<Doc>	1A

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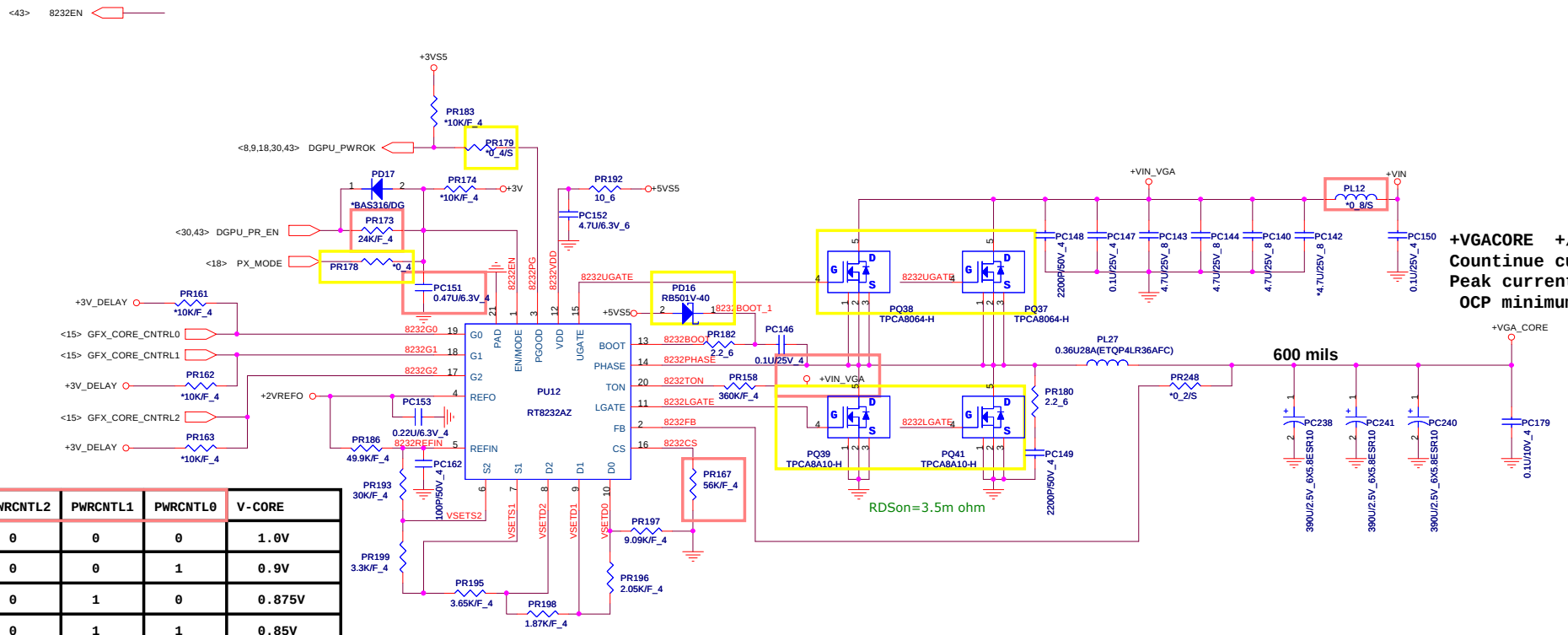
VGA Core



thames xt	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

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Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

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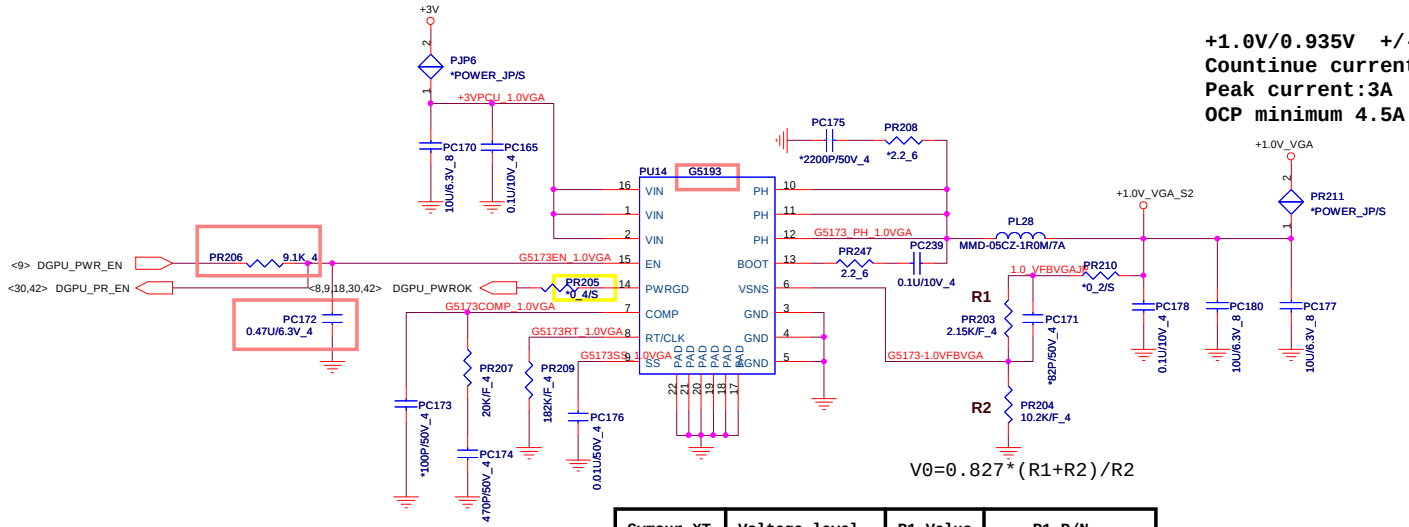
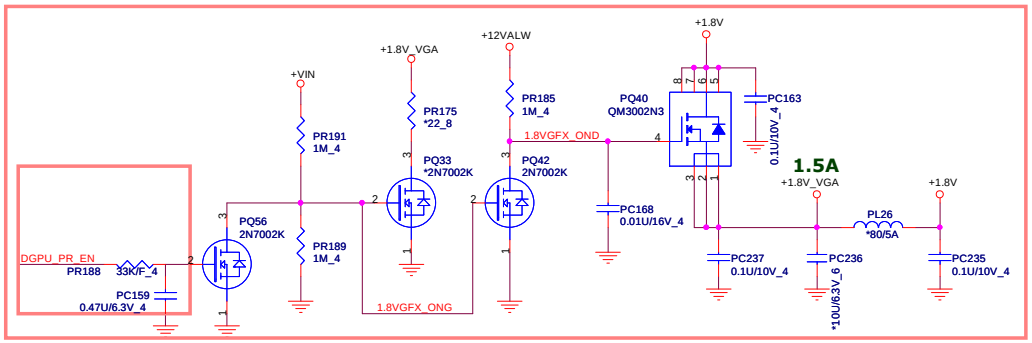
+1.0V/0.935V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

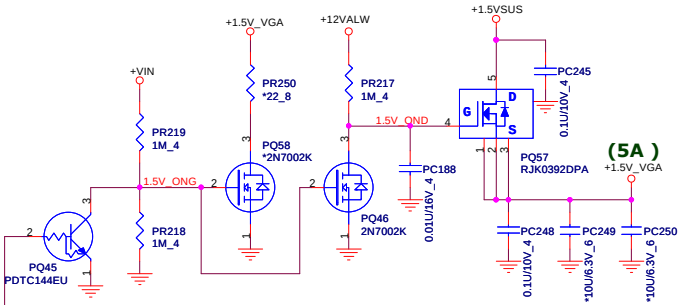
+3V <6,7,8,9,10,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,39,40,42>
+VIN <23,33,34,35,36,37,38,39,41,42>
+1.8V <4,7,10,38>
+3VS5 <6,7,8,9,10,23,33,35,38,39,42>
+5VS5 <10,24,28,33,35,36,37,38,39,40,41,42>
+3V_VGA <18>
+12VALW <32,34,39>
+1.5VSUS <2,4,10,12,13,37>
+1.5V_VGA <18,20,21,22,33>
+1.8V_VGA <15,16,18,19>
+3V_DELAY <15,17,18,42>
+VGA_CORE <18,33,42>

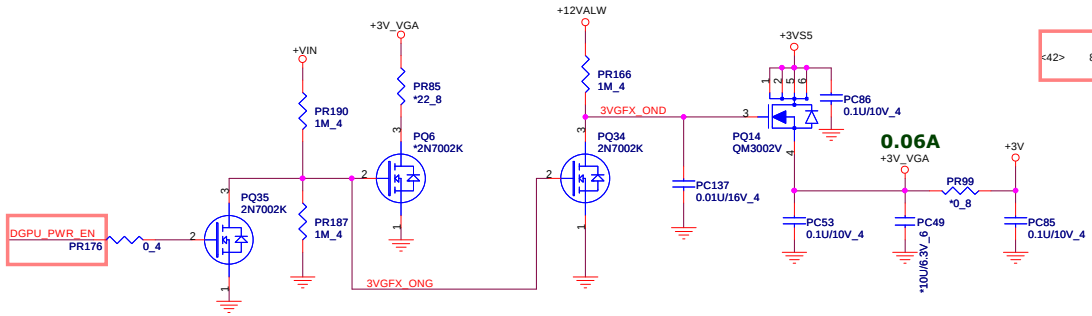


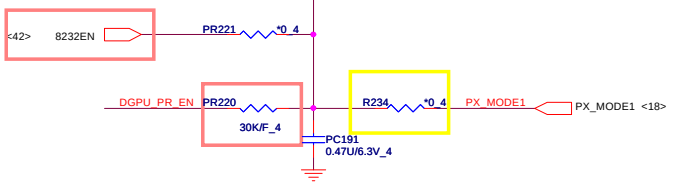
V0=0.827*(R1+R2)/R2

Symour-XT	Voltage level	R1 Value	R1 P/N
17W	1.0V	2.15K	CS22152FB07
25W	0.935V	1.37K	CS21372FB19









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Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

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