Compal Confidential

Pixar AMD M/B LA-9851P Schematics Document

AMD Richland APU / Bolton FCH M3

Date : 2012-11-07

Version T0.1

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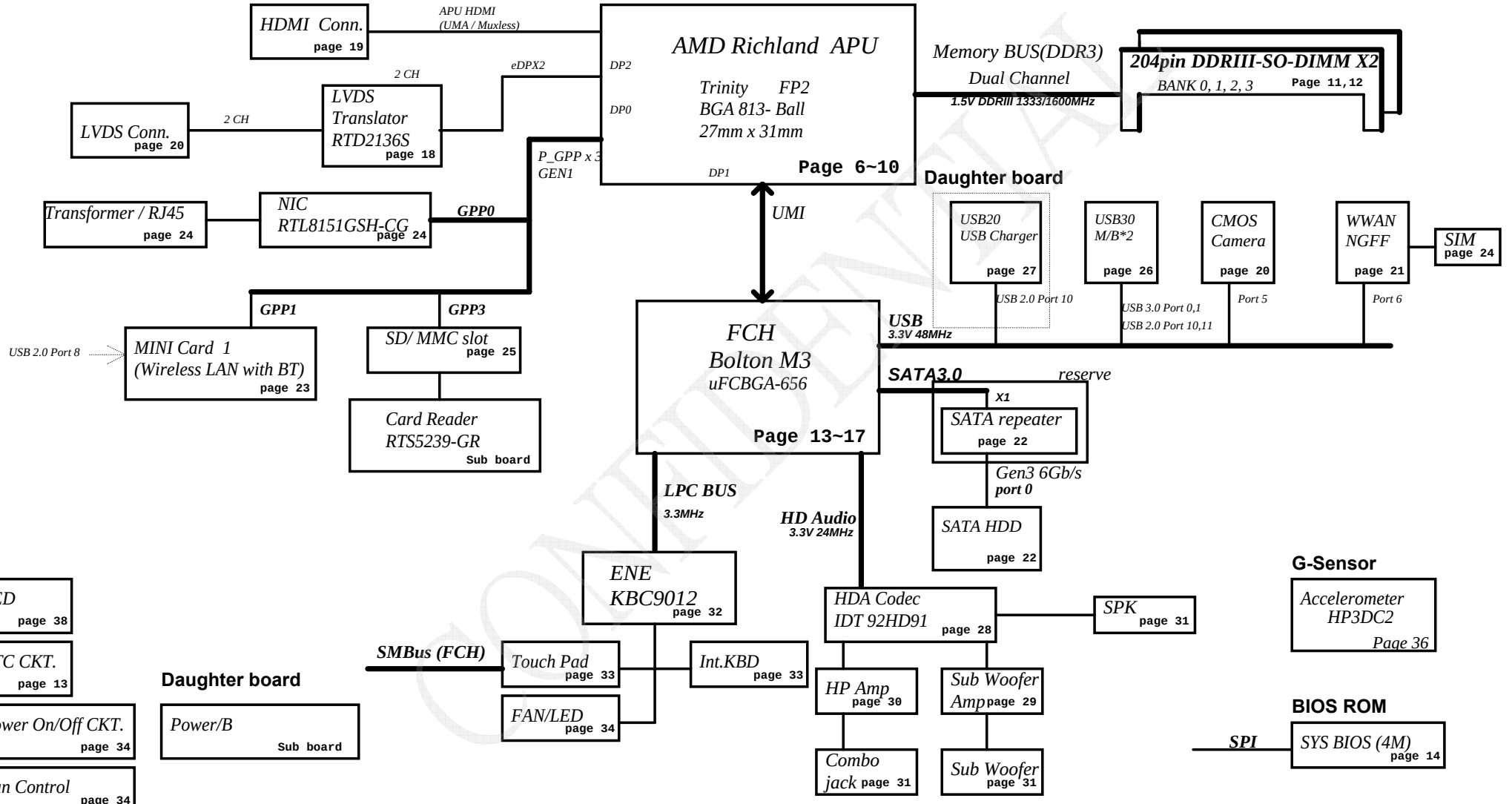
Model Name : VPU00 AMD

AMD Richland



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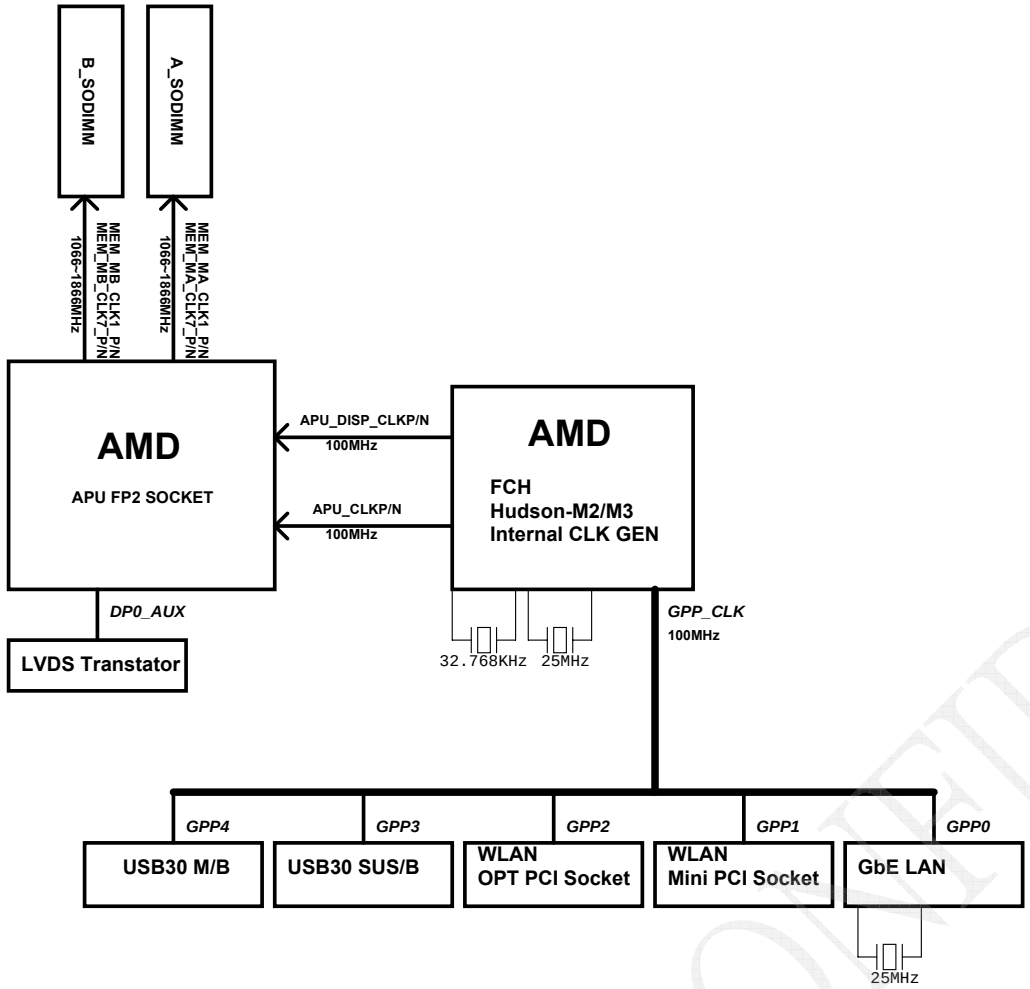
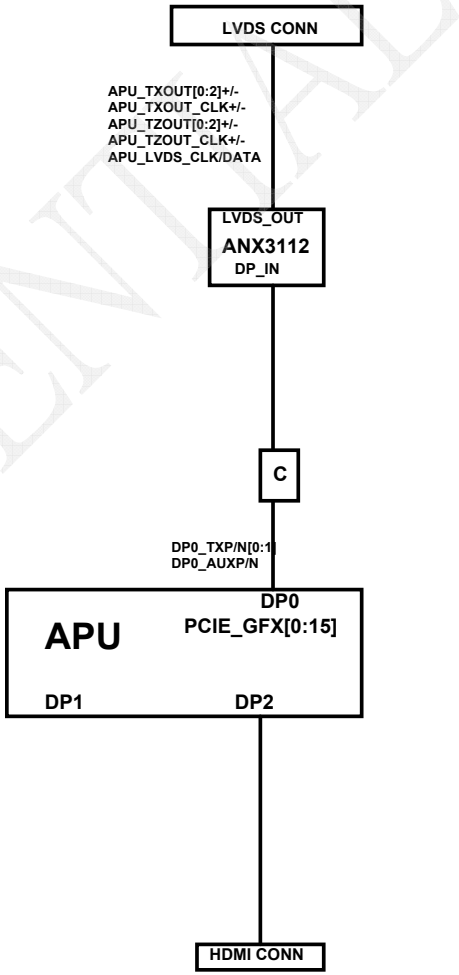
CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Option Table

BOM Structure	Description

BOM Config

UMA
V

USB Port Table

USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	USB2.0 (left side)
		1	
	UHCI1	2	
		3	
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	BT
		9	
	UHCI5	10	USB2.0 (Right side)
		11	USB2.0 (Right side)
	UHCI6	12	
		13	

USB 3.0	Port	1 External USB Port
	0	USB3.0 (Right side)
	1	USB3.0 (Right side)
	2	
	3	

Audio Codec SSID

Platform	Platform ID
Evora 1.0 UMA	0x18DE

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (GPU)	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
LVDS TR(RTD-2132S)	1010 100X b	A8H
VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	90
DDR DIMM2	1101 001X b	94

FCH SM Bus 1 address

Device	Address	HEX

SMBUS Control Table

	SOURCE	BATT	Charger	HP Amp	MINI3	SODIMM	EC_SMB_CK2 EC_SMB_DA2	EC_SMB_CK1 EC_SMB_DA1	G-Sensor	TP
EC_SMB_CK1 EC_SMB_DA1	KB932	V	V						V	
EC_SMB_CK2 EC_SMB_DA2	KB932			V						
FCH_SCLK0 FCH_SDATA0	FCH					V				
FCH_SCLK1 FCH_SDATA1	FCH									V

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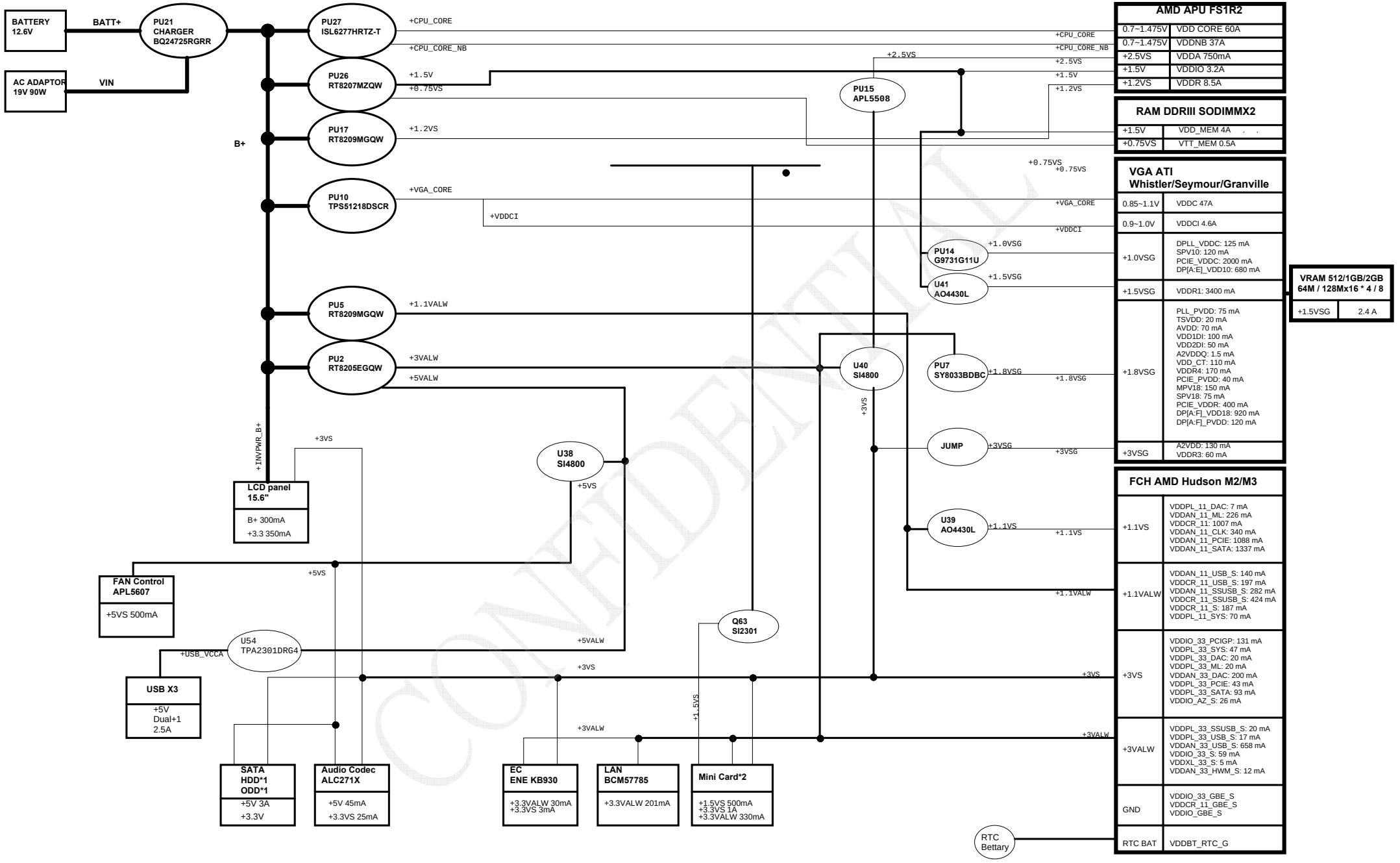

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GPU

Delete GPU
1202 Calvin

UCPU1A

GRAPHICS

AP1	P_GFX_RXP[0]	P_GFX_TXP[0]	AN1
AP2	P_GFX_RXN[0]	P_GFX_TXN[0]	AN2
AM1	P_GFX_RXP[1]	P_GFX_TXP[1]	AM4
AM2	P_GFX_RXN[1]	P_GFX_TXN[1]	AM3
AK3	P_GFX_RXP[2]	P_GFX_TXP[2]	AK2
AK4	P_GFX_RXN[2]	P_GFX_TXN[2]	AK1
AJ1	P_GFX_RXP[3]	P_GFX_TXP[3]	AH1
AJ2	P_GFX_RXN[3]	P_GFX_TXN[3]	AH2
AH4	P_GFX_RXP[4]	P_GFX_TXP[4]	AF3
AH3	P_GFX_RXN[4]	P_GFX_TXN[4]	AF4
AF2	P_GFX_RXP[5]	P_GFX_TXP[5]	AE1
AF1	P_GFX_RXN[5]	P_GFX_TXN[5]	AE2
AD1	P_GFX_RXP[6]	P_GFX_TXP[6]	AD4
AD2	P_GFX_RXN[6]	P_GFX_TXN[6]	AD3
AB3	P_GFX_RXP[7]	P_GFX_TXP[7]	AB2
AB4	P_GFX_RXN[7]	P_GFX_TXN[7]	AB1
AA1	P_GFX_RXP[8]	P_GFX_TXP[8]	Y1
AA2	P_GFX_RXN[8]	P_GFX_TXN[8]	Y2
Y4	P_GFX_RXP[9]	P_GFX_TXP[9]	V3
Y3	P_GFX_RXN[9]	P_GFX_TXN[9]	V4
V2	P_GFX_RXP[10]	P_GFX_TXP[10]	U1
V1	P_GFX_RXN[10]	P_GFX_TXN[10]	U2
T1	P_GFX_RXP[11]	P_GFX_TXP[11]	T4
T2	P_GFX_RXN[11]	P_GFX_TXN[11]	T3
P3	P_GFX_RXP[12]	P_GFX_TXP[12]	P2
P4	P_GFX_RXN[12]	P_GFX_TXN[12]	P1
N1	P_GFX_RXP[13]	P_GFX_TXP[13]	M1
N2	P_GFX_RXN[13]	P_GFX_TXN[13]	M2
M4	P_GFX_RXP[14]	P_GFX_TXP[14]	K3
M3	P_GFX_RXN[14]	P_GFX_TXN[14]	K4
K2	P_GFX_RXP[15]	P_GFX_TXP[15]	J1
K1	P_GFX_RXN[15]	P_GFX_TXN[15]	J2

Delete GPU
1202 Calvin

GPU

GLAN
WLAN
Card reader
UMI

24	PCIE_DTX_C_FRX_P0	AH5	P_GPP_RXP[0]	P_GPP_TXP[0]	AG7	PCIE_FTX_DRX_P0	CC1	1	2 .1U_0402_16V7K	PCIE_FTX_C_DRX_P0	24
24	PCIE_DTX_C_FRX_N0	AG5	P_GPP_RXN[0]	P_GPP_TXN[0]	AG8	PCIE_FTX_DRX_N0	CC2	1	2 .1U_0402_16V7K	PCIE_FTX_C_DRX_N0	24
23	PCIE_DTX_C_FRX_P1	AG6	P_GPP_RXP[1]	P_GPP_TXP[1]	AE7	PCIE_FTX_DRX_P1	CC3	1	2 .1U_0402_16V7K	PCIE_FTX_C_DRX_P1	23
23	PCIE_DTX_C_FRX_N1	AE6	P_GPP_RXN[1]	P_GPP_TXN[1]	AE8	PCIE_FTX_DRX_N1	CC4	1	2 .1U_0402_16V7K	PCIE_FTX_C_DRX_N1	23
		AE5	P_GPP_RXP[2]	P_GPP_TXP[2]	AD7						
25	PCIE_DTX_C_FRX_P3	AD6	P_GPP_RXP[3]	P_GPP_TXP[3]	AD8						
25	PCIE_DTX_C_FRX_N3	AD5	P_GPP_RXN[3]	P_GPP_TXN[3]	AB6	PCIE_FTX_DRX_P3	CC5	1	2 .1U_0402_16V7K	PCIE_FTX_C_DRX_P3	25
					AB5	PCIE_FTX_DRX_N3	CC6	1	2 .1U_0402_16V7K	PCIE_FTX_C_DRX_N3	25
		AM10									
13	UMI_MTX_C_FRX_P0	AN10	P_UMI_RXP[0]	P_UMI_TXP[0]	AN6	UMI_FTX_MRX_P0	CC7	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_P0	13
13	UMI_MTX_C_FRX_N0	AN8	P_UMI_RXN[0]	P_UMI_TXN[0]	AM6	UMI_FTX_MRX_N0	CC8	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_N0	13
13	UMI_MTX_C_FRX_P1	AM8	P_UMI_RXP[1]	P_UMI_TXP[1]	AP6	UMI_FTX_MRX_P1	CC9	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_P1	13
13	UMI_MTX_C_FRX_N1	AP8	P_UMI_RXN[1]	P_UMI_TXN[1]	AR6	UMI_FTX_MRX_N1	CC10	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_N1	13
13	UMI_MTX_C_FRX_P2	AR8	P_UMI_RXP[2]	P_UMI_TXP[2]	AP4	UMI_FTX_MRX_P2	CC11	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_P2	13
13	UMI_MTX_C_FRX_N2	AR7	P_UMI_RXN[2]	P_UMI_TXN[2]	AR4	UMI_FTX_MRX_N2	CC12	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_N2	13
13	UMI_MTX_C_FRX_P3	AP7	P_UMI_RXP[3]	P_UMI_TXP[3]	AP3	UMI_FTX_MRX_P3	CC13	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_P3	13
13	UMI_MTX_C_FRX_N3	AP7	P_UMI_RXN[3]	P_UMI_TXN[3]	AR3	UMI_FTX_MRX_N3	CC14	1	2 .1U_0402_16V7K	UMI_FTX_C_MRX_N3	13

+1.2VS — 1 RC1 2 196_0402_1% — P_ZVDDP AR11 — P_ZVDDP

AP11 P_ZVSS — 1 RC2 2 196_0402_1% — P_ZVSS

RICHLAND-A8-SERIES_BGA813

10/4 Eric chagne back on RC1 & RC2.

P_ZVDDP W/S=8/12 mil, <3000mil

P_ZVSS W/S=8/12 mil, <3000mil

CPU THERMAL SENSOR

+3VS

CC173 0.1U_0402_16V4Z

UC1 SA00003PU00

ADM1032ARMZ-2REEL_MSOP8

1	VDD	SCLK	8 EC_SMB_CK2 — EC_SMB_CK2 18,30,32,8
H_THERMDA 2	D+	SDATA	7 EC_SMB_DA2 — EC_SMB_DA2 18,30,32,8
CC174 2200P_0402_50V7K H_THERMDC 3	D-	ALERT#	6 THERMAL_ALERT# — RC105 10K_0402_5% — +3VS
CPU_THERM# 4	THERM#	GND	5

+3VS — RC106 33K_0402_5% — THERM#

THERMAL_ALERT# 32

Address:0100_1100 EMC1402-1
Address:0100_1101 EMC1402-2

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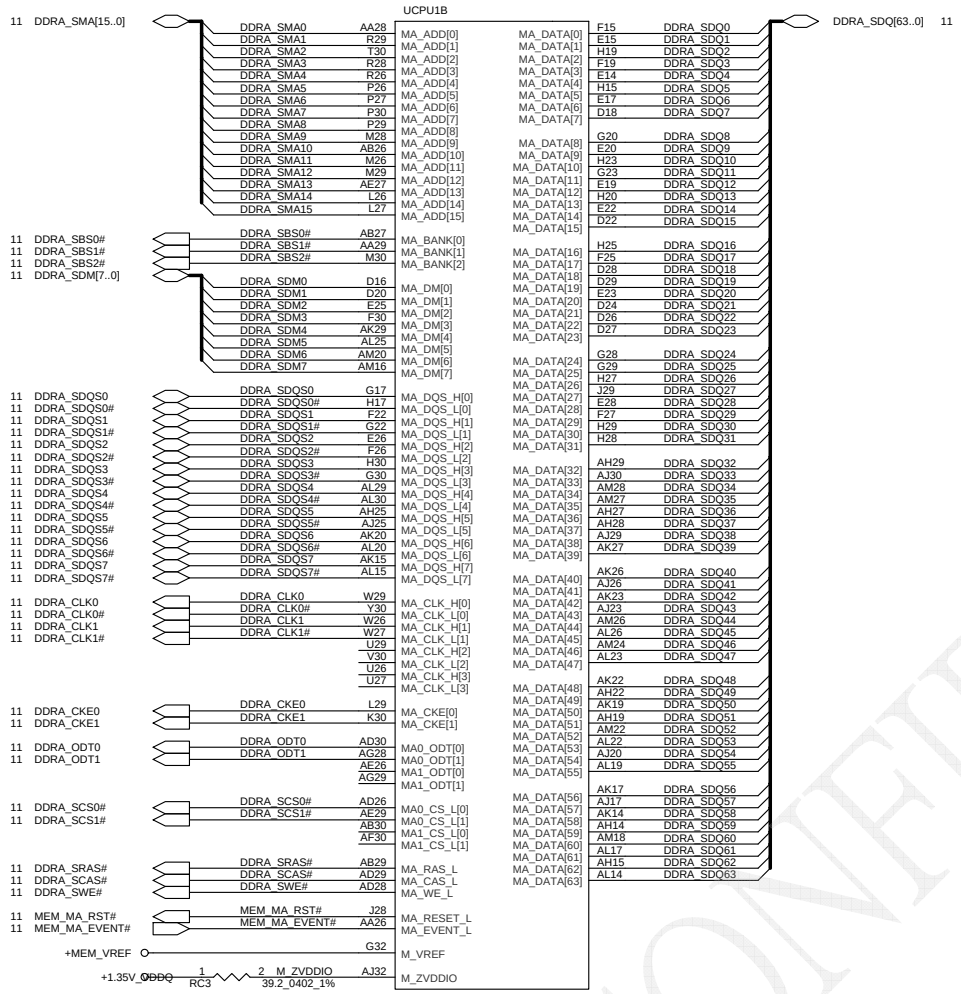
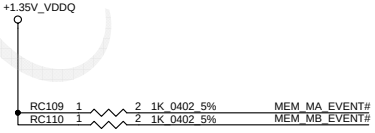
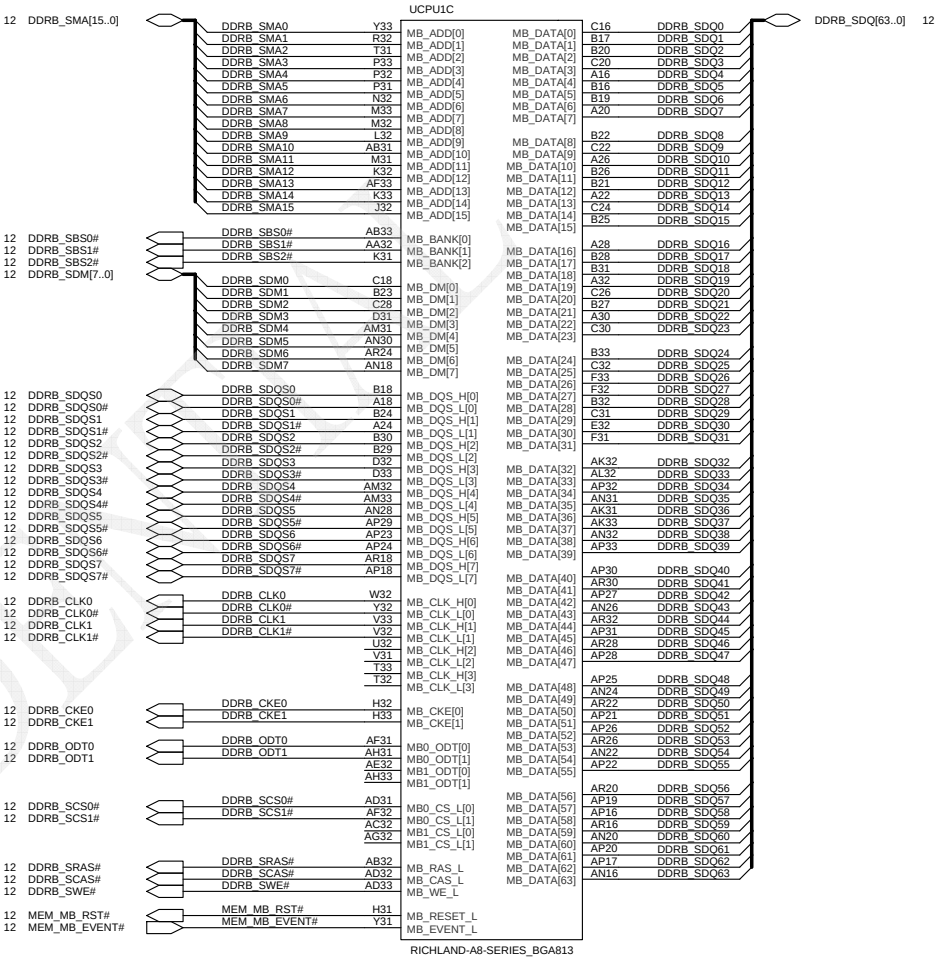
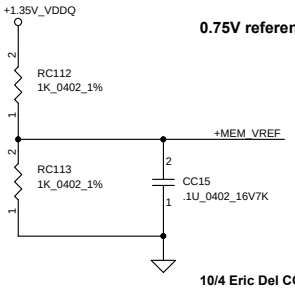


M_ZVDDIO W/S=8/12 mil, <1000mil



11/19 Eric change 4P2R to 8P4R.





10/4 Eric Del CC45.

+MEM_VREF 15mil
Close to JCPU1

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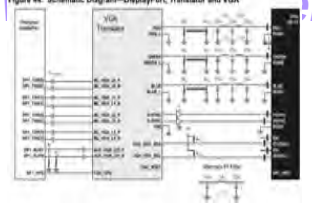

Figure 44 Schematic Diagram—DisplayPort, Translator and VGA

Close to APU (JCPU1)

To LVDS Translator

FHD eDP

UCPU1D

RICHLAND-A8-SERIES_BGA813

Place near APU

12/19 del CC141/CC142, RC10, RC11

To LVDS Translator

To HDMI

LVDS/eDP

HDMI

10/3 Eric Add DP_ENVDD control pin.

DP_AUX_ZVSS W/S=8/12 mil, <3000mil

10/27 add TP.

TEST35 change to PU for HDMI can not output 20110126

+1.35V_VDDQ

RP3 1K_0804_8P4R_5%

APU_SIC

APU_SID

ALLOW_STOP

ALERT_L

Allow_STOP leakage issue

4/17 change to 0ohm new symbol

APU_RST#

APU_PWRGD

APU_SVC

APU_SVD

APU_SVT

To HDMI

100MHz NSS

SVI 2.0 (0 ohm at Power Side)

SB-TSI (S5 Domain)

Check

4/17 change to 0ohm new symbol

10/25 Eric aremovek H_PROCHOT# .

Internal PU when no use HDT

Route as differential with APU_VDD_RUN_FB_L

TC13 near APU.

12/15 change to +1.5V

Close to Header

10/27 300 ohm??

For ESD request close APU side

10/4 Eric Del.

10/4 Eric Del.

12/19 RF request

CPU TSI interface level shift

When APU High -> MOS OFF (Vgs < 0.4V)

APU Low -> MOS ON (Vgs > 1.3V)

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

Vg = 1.607 V

BSH111_SOT23-3

Asserted as an input to force processor into HTC-active state

1/11 Eric mount RC25 for open drain needed.
2/29 remove RC42, add EC_THERM for power leakage issue

2N7002K_SOT23-3

THERMTRIP shutdown temperature: 115 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

MMBT3904_SOT23-3

HDT Debug conn

12/19 remove damping 0ohm.

12/15 change to +1.5V

12/27 Eric Del.

3/9 add QC5 for +5VS power leakage issue

10/18 Eric change Level shift solution with Pagani AMD.

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Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A

Reserve 4 pcs 180pF for EMI DDR noise issue

On power team page

On power team page

+APU_CORE Decoupling

330uF x 4 @ x1
22uF x 10
0.22uF x2
0.01uF x3
180pF x2 @ x1

+APU_CORE_NB Decoupling

330uF x2
22uF x2 @ x2
10uF x1
0.22uF x2
180pF x3

UCPU1E

UCPU1F

RICHLAND-A8-SERIES_BGA813

+1.5V / VDDIO Decoupling

220uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1

Decoupling between CPU and DIMMs across VDDIO and VSS split

VDDR Decoupling
Close JCPU1.AN14,AP14~15,AR14~15

10uF x2
0.22uF x2
180pF x2 @x2
0.01uFx2
4.7uFx2

12/22 for RF request

VDDP Decoupling
Close JCPU1.AH3~7

22uF x4
0.22uF x2
180pF x2 @x2

220uF x1

FBMA-L11-201209-221LMA30T_0805

VDDA Decoupling

47uF x1
0.22uF x1

Northbridge Power Pins for Remote Decoupling

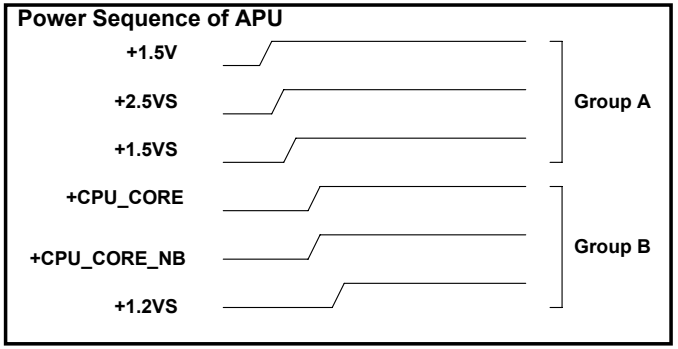
VDDP: 5000mA

VDDR: 3500mA

VDDA: 750mA

Change 180p to 1000p by AMD

Power Sequence of APU



Decoupling Caps.

Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0			0	19/11	7	5	17	3	1	1 / 1	13/3
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

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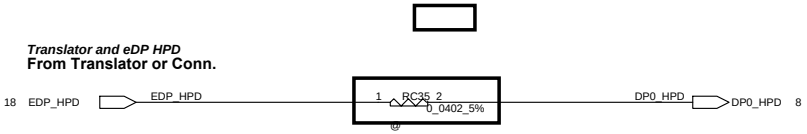
HPD

Del reserved NMOS

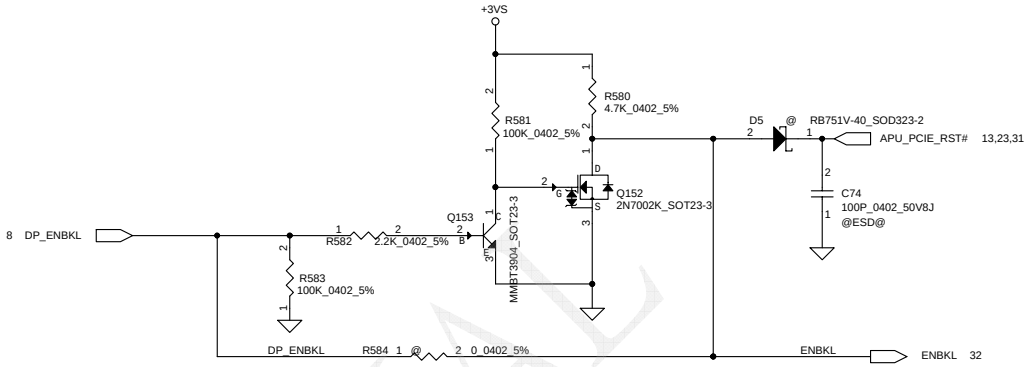


4/17 change to 0ohm new symbol

Del reserved NMOS

12/06 Del FCH_CRT_HPD

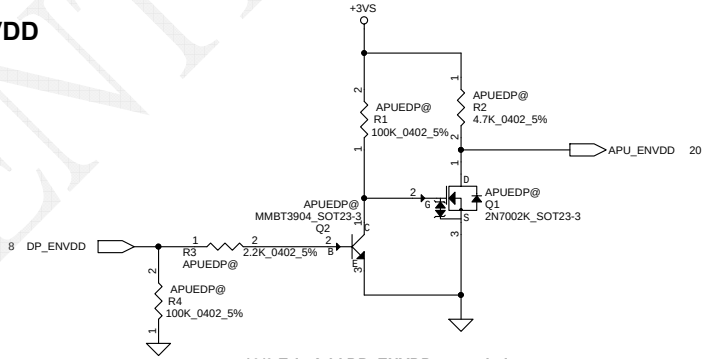
Panel ENBKL



11/13 Eric Add Panel EBBKL circuit.
Verify eDP on DB phase.

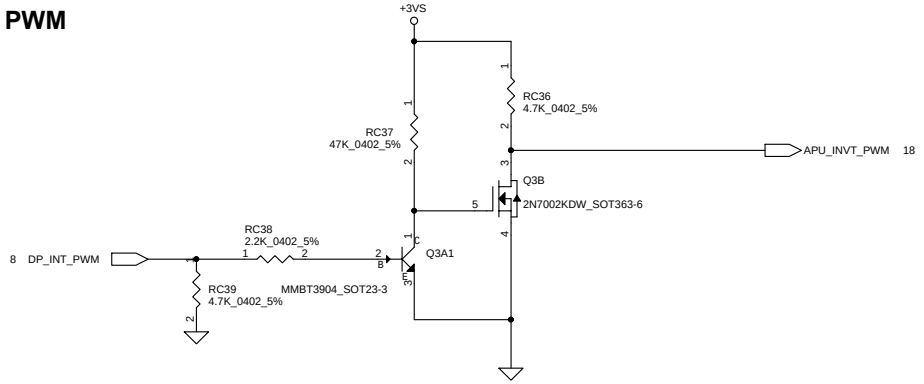
eDP Panel ENVDD

Panel ENVDD



10/3 Eric Add DP_ENVDD control pin.

Panel PWM



Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

Title	SCHEMATIC, MB A9851		
Size: Custom	Document Number: 4019NK		Rev: A
Date: Monday, October 21, 2013	Sheet 10 of 47		

All VREF traces should have 20 mil trace width

7 DDRA_SDQ[0..63] DDRA_SDQ[0..63]
7 DDRA_SDM[0..7] DDRA_SDM[0..7]
7 DDRA_SMA[0..15] DDRA_SMA[0..15]

+1.35V_VDDQ
RD10 1K_0402_1% +V_DDR_REFA
RD11 1K_0402_1%

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.675VS
CD3 1U_0402_6.3V6K
CD4 1U_0402_6.3V6K
CD5 1U_0402_6.3V6K
CD6 1U_0402_6.3V6K
CD7 10U_0603_6.3V6M
CD8 10U_0603_6.3V6M
CD9 10U_0603_6.3V6M

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.35V_VDDQ
CD12 10U_0603_6.3V6M
CD13 10U_0603_6.3V6M
CD14 10U_0603_6.3V6M
CD15 10U_0603_6.3V6M
CD16 10U_0603_6.3V6M
CD17 10U_0603_6.3V6M
CD18 0.1U_0402_16V7K
CD19 0.1U_0402_16V7K
CD20 0.1U_0402_16V7K
CD21 0.1U_0402_16V7K
@ CD22 47U 6.3V M B1 ESR70M

DDR3 SO-DIMM A

3/2 Reserve 4 pcs 180pF for EMI DDR noise issue

+1.35V_VDDQ
CD26 0.1U_0402_16V7K
CD27 0.1U_0402_16V7K
CD28 0.1U_0402_16V7K
CD25 0.1U_0402_16V7K

+1.35V_VDDQ
CD57 180P_0402_50V8J
CD58 180P_0402_50V8J
CD59 180P_0402_50V8J
CD60 180P_0402_50V8J

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

+VREF_DQ 15mil

DDR3 SO-DIMM A

+V_DDR_REFA
+1.35V_VDDQ
+1.35V_VDDQ
CD1 0.1U_0402_16V7K
CD3 1000P_0603_50V7K

JDIMM1

		+V_DDR_REFA	1	VREF_DQ	VSS1	2	
		DDRA_SDQ0	3	VSS2	DQ4	4	DDRA_SDQ4
		DDRA_SDQ1	5	DQ0	DQ5	6	DDRA_SDQ5
			7	DQ1	VSS3	8	
		DDRA_SDM0	9	VSS4	DQS#0	10	DDRA_SDQS0#
			11	DM0	DQS0	12	DDRA_SDQS0
		DDRA_SDQ2	13	VSS5	DQ6	14	
		DDRA_SDQ3	15	DQ2	DQ7	16	DDRA_SDQ6
			17	DQ3	VSS6	18	DDRA_SDQ7
		DDRA_SDQ8	19	VSS7	DQ8	20	
		DDRA_SDQ9	21	DQ8	VSS8	22	DDRA_SDQ12
			23	DQ9	DQ12	24	DDRA_SDQ13
		DDRA_SDQS1#	25	VSS9	DQ13	26	
7	DDRA_SDQS1#	DDRA_SDQS1	27	DQS#1	VSS10	28	DDRA_SDM1
7	DDRA_SDQS1		29	DQS1	DM1	30	MEM_MA_RST#
		DDRA_SDQ10	31	VSS11	RESET#	32	MEM_MA_RST# 7
		DDRA_SDQ11	33	DQ10	VSS12	34	
			35	DQ11	DQ14	36	DDRA_SDQ14
		DDRA_SDQ16	37	VSS13	DQ15	38	DDRA_SDQ15
		DDRA_SDQ17	39	DQ16	VSS14	40	
			41	DQ17	DQ20	42	DDRA_SDQ20
		DDRA_SDQS2#	43	VSS15	DQ21	44	DDRA_SDQ21
7	DDRA_SDQS2#	DDRA_SDQS2	45	DQS#2	VSS16	46	
7	DDRA_SDQS2		47	DQS2	DM2	48	DDRA_SDM2
		DDRA_SDQ18	49	VSS17	DQ22	50	
		DDRA_SDQ19	51	VSS18	DQ23	52	DDRA_SDQ22
			53	DQ18	VSS19	54	DDRA_SDQ23
		DDRA_SDQ24	55	DQ19	DQ28	56	
		DDRA_SDQ25	57	VSS20	DQ29	58	DDRA_SDQ28
			59	DQ24	VSS21	60	DDRA_SDQ29
		DDRA_SDM3	61	DQ25	DQS#3	62	DDRA_SDQS3#
			63	VSS22	DQS3	64	DDRA_SDQS3
		DDRA_SDQ26	65	DM3	VSS24	66	
		DDRA_SDQ27	67	VSS23	DQ30	68	DDRA_SDQ30
			69	DQ26	DQ31	70	DDRA_SDQ31
			71	DQ27	VSS26	72	
				VSS25			
7	DDRA_CKE0	DDRA_CKE0	73	CKE0	CKE1	74	DDRA_CKE1
			75	VDD1	VDD2	76	DDRA_CKE1 7
7	DDRA_SBS2#	DDRA_SBS2#	77	NC1	A15	78	DDRA_SMA15
			79	BA2	A14	80	DDRA_SMA14
		DDRA_SMA12	81	VDD3	VDD4	82	
		DDRA_SMA9	83	A12/BC#	A11	84	DDRA_SMA11
			85	A9	A7	86	DDRA_SMA7
		DDRA_SMA8	87	VDD5	VDD6	88	
		DDRA_SMA5	89	A8	A6	90	DDRA_SMA6
			91	A5	A4	92	DDRA_SMA4
		DDRA_SMA3	93	VDD7	VDD8	94	
		DDRA_SMA1	95	A3	A2	96	DDRA_SMA2
			97	A1	A0	98	DDRA_SMA0
7	DDRA_CLK0	DDRA_CLK0	99	VDD9	VDD10	100	
7	DDRA_CLK0#	DDRA_CLK0#	101	CK0	CK1	102	DDRA_CLK1
			103	CK0#	CK1#	104	DDRA_CLK1#
		DDRA_SMA10	105	VDD11	VDD12	106	
		DDRA_SBS0#	107	A10/AP	BA1	108	DDRA_SBS1#
7	DDRA_SBS0#		109	BA0	RAS#	110	DDRA_SRAS#
		DDRA_SWE#	111	VDD13	VDD14	112	
7	DDRA_SWE#	DDRA_SCAS#	113	WE#	S0#	114	DDRA_SCS0#
7	DDRA_SCAS#		115	CAS#	ODT0	116	DDRA_SCS0#
		DDRA_SMA13	117	VDD15	VDD16	118	DDRA_ODT0
		DDRA_SCS1#	119	A13	ODT1	120	DDRA_ODT1
7	DDRA_SCS1#		121	S1#	NC2	122	DDRA_ODT1 7
			123	VDD17	VDD18	124	
			125	NCTEST	VREF_CA	126	
		DDRA_SDQ32	127	VSS27	VSS28	128	
		DDRA_SDQ33	129	DQ32	DQ36	130	DDRA_SDQ36
			131	DQ33	DQ37	132	DDRA_SDQ37
		DDRA_SDQS4#	133	VSS29	VSS30	134	
7	DDRA_SDQS4#	DDRA_SDQS4	135	DQS#4	DM4	136	DDRA_SDM4
7	DDRA_SDQS4		137	DQS4	VSS31	138	
		DDRA_SDQ34	139	VSS32	DQ38	140	DDRA_SDQ38
		DDRA_SDQ35	141	DQ34	DQ39	142	DDRA_SDQ39
			143	DQ35	VSS33	144	
		DDRA_SDQ40	145	VSS34	DQ44	146	DDRA_SDQ44
		DDRA_SDQ41	147	DQ40	DQ45	148	DDRA_SDQ45
			149	DQ41	VSS35	150	
		DDRA_SDM5	151	VSS36	DQS#5	152	DDRA_SDQS5#
			153	DM5	DQS5	154	DDRA_SDQS5
		DDRA_SDQ42	155	VSS37	VSS38	156	
		DDRA_SDQ43	157	DQ42	DQ46	158	DDRA_SDQ46
			159	DQ43	DQ47	160	DDRA_SDQ47
		DDRA_SDQ48	161	VSS39	VSS40	162	
		DDRA_SDQ49	163	DQ48	DQ52	164	DDRA_SDQ52
			165	DQ49	DQ53	166	DDRA_SDQ53
		DDRA_SDQS6#	167	VSS41	VSS42	168	
7	DDRA_SDQS6#	DDRA_SDQS6	169	DQS#6	DM6	170	DDRA_SDM6
7	DDRA_SDQS6		171	DQS6	VSS43	172	
		DDRA_SDQ50	173	VSS44	DQ54	174	DDRA_SDQ54
		DDRA_SDQ51	175	DQ50	DQ55	176	DDRA_SDQ55
			177	DQ51	VSS45	178	
		DDRA_SDQ56	179	VSS46	DQ60	180	DDRA_SDQ60
		DDRA_SDQ57	181	DQ56	DQ61	182	DDRA_SDQ61
			183	DQ57	VSS47	184	
		DDRA_SDM7	185	VSS48	DQS#7	186	DDRA_SDQS7#
			187	DM7	DQS7	188	DDRA_SDQS7
		DDRA_SDQ58	189	VSS49	VSS50	190	
		DDRA_SDQ59	191	DQ58	DQ62	192	DDRA_SDQ62
			193	DQ59	DQ63	194	DDRA_SDQ63
			195	VSS51	VSS52	196	
+3VS	RD51 2_10K_0402_5%		197	SA0	EVENT#	198	MEM_MA_EVENT#
			199	VDDSPD	SDA	200	MEM_MA_EVENT# 7
			201	SA1	SCL	202	FCH_SDATA0 12,15
			203	VTT1	VTT2	204	FCH_SCLK0 12,15
							+0.675VS
			205	G1	G2	206	

LCN_DAN06-K4406-0102
CONN@

2.2U_0603_6.3V6K CD23 @
0.1U_0402_16V7K CD24 @
RD6 0_0402_5% @

+VREF_CB 15mil
+1.35V_VDDQ
RD12 1K_0402_1%
RD13 1K_0402_1%
+VREF_CA
0.1U_0402_16V7K CD10
1000P_0603_50V7K CD11

DIMM_A REV H:4mm

<Address: 00>

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

Title	SCHEMATIC, MB A9851		
Size C	Document Number LA-8661P		Rev A
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DDR3 SO-DIMM B

All VREF traces should have 20 mil trace width

7 DDRB_SDQ[0..63] — DDRB_SDQ[0..63]
7 DDRB_SDM[0..7] — DDRB_SDM[0..7]
7 DDRB_SMA[0..15] — DDRB_SMA[0..15]

10/03 change to +V_DDR_REFB

+1.35V_VDDQ
RD14 1K_0402_1%
+V_DDR_REFB
RD15 1K_0402_1%

Layout Note: Place near JDIMM1.203 & JDIMM1.204

+0.675VS
CD34 1U_0402_6.3V6K
CD35 1U_0402_6.3V6K
CD36 1U_0402_6.3V6K
CD48 1U_0402_6.3V6K
CD53 10U_0603_6.3V6M
CD52 10U_0603_6.3V6M
CD49 10U_0603_6.3V6M

Layout Note: Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.35V_VDDQ
CD37 10U_0603_6.3V6M
CD38 10U_0603_6.3V6M
CD45 10U_0603_6.3V6M
CD40 10U_0603_6.3V6M
CD42 10U_0603_6.3V6M
CD50 10U_0603_6.3V6M
CD44 0.1U_0402_16V7K
CD43 0.1U_0402_16V7K
CD47 0.1U_0402_16V7K
CD39 0.1U_0402_16V7K
CD36 47U 6.3V M B1 ESR70M

DDR3 SO-DIMM B

+1.35V_VDDQ
CD33 0.1U_0402_16V7K
CD34 0.1U_0402_16V7K
CD35 0.1U_0402_16V7K
CD32 0.1U_0402_16V7K

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

+1.35V_VDDQ
CD61 180P_0402_50V8J
CD62 180P_0402_50V8J
CD63 180P_0402_50V8J
CD64 180P_0402_50V8J

3/2 Reserve 4 pcs 180pF for EMI DDR noise issue

10/05 change to PH.

+VREF_DQ 15mil
+V_DDR_REFB
CD50 0.1U_0402_16V7K
CD29 1000P_0603_50V7K
+1.35V_VDDQ

JDIMM2

1	VREF_DQ	VSS1	2		
3	VSS2	DQ4	4	DDRB_SDQ4	
5	DQ0	DQ5	6	DDRB_SDQ5	
7	DQ1	VSS3	8		
9	VSS4	DQS#0	10	DDRB_SDQS0#	7 DDRB_SDQS0#
11	DM0	DQS0	12	DDRB_SDQS0	7 DDRB_SDQS0
13	VSS5	VSS6	14		
15	DQ2	DQ6	16	DDRB_SDQ6	
17	DQ3	DQ7	18	DDRB_SDQ7	
19	VSS7	VSS8	20		
21	DQ8	DQ12	22	DDRB_SDQ12	
23	DQ9	DQ13	24	DDRB_SDQ13	
25	VSS9	VSS10	26		
27	DQS#1	DM1	28	DDRB_SDM1	
29	DQS1	RESET#	30	MEM_MB_RST#	MEM_MB_RST# 7
31	VSS11	VSS12	32		
33	DQ10	DQ14	34	DDRB_SDQ14	
35	DQ11	DQ15	36	DDRB_SDQ15	
37	VSS13	VSS14	38		
39	DQ16	DQ20	40	DDRB_SDQ20	
41	DQ17	DQ21	42	DDRB_SDQ21	
43	VSS15	VSS16	44		
45	DQS#2	DM2	46	DDRB_SDM2	
47	DQS2	VSS17	48		
49	VSS18	DQ22	50	DDRB_SDQ22	
51	DQ18	DQ23	52	DDRB_SDQ23	
53	DQ19	VSS19	54		
55	VSS20	DQ28	56	DDRB_SDQ28	
57	DQ24	DQ29	58	DDRB_SDQ29	
59	DQ25	VSS21	60		
61	VSS22	DQS#3	62	DDRB_SDQS3#	DDRB_SDQS3# 7
63	DM3	DQS3	64	DDRB_SDQS3	DDRB_SDQS3 7
65	VSS23	VSS24	66		
67	DQ26	DQ30	68	DDRB_SDQ30	
69	DQ27	DQ31	70	DDRB_SDQ31	
71	VSS25	VSS26	72		
73	CKE0	CKE1	74	DDRB_CKE1	DDRB_CKE1 7
75	VDD1	VDD2	76		
77	NC1	A15	78	DDRB_SMA15	
79	BA2	A14	80	DDRB_SMA14	
81	VDD3	VDD4	82		
83	A12/BC#	A11	84	DDRB_SMA11	
85	A9	A7	86	DDRB_SMA7	
87	VDD5	VDD6	88		
89	A8	A6	90	DDRB_SMA6	
91	A5	A4	92	DDRB_SMA4	
93	VDD7	VDD8	94		
95	A3	A2	96	DDRB_SMA2	
97	A1	A0	98	DDRB_SMA0	
99	VDD9	VDD10	100		
101	CK0	CK1	102	DDRB_CLK1	7
103	CK0#	CK1#	104	DDRB_CLK1#	7
105	VDD11	VDD12	106		
107	A10/AP	BA1	108	DDRB_SBS1#	7
109	BA0	RAS#	110	DDRB_SRAS#	7
111	VDD13	VDD14	112		
113	WE#	S0#	114	DDRB_SCS0#	7
115	CAS#	ODT0	116	DDRB_ODT0	7
117	VDD15	VDD16	118		
119	A13	ODT1	120	DDRB_ODT1	7
121	S1#	NC2	122		
123	VDD17	VDD18	124		
125	NCTEST	VREF_CA	126		
127	VSS27	VSS28	128		
129	DQ32	DQ36	130	DDRB_SDQ36	
131	DQ33	DQ37	132	DDRB_SDQ37	
133	VSS29	VSS30	134		
135	DQS#4	DM4	136	DDRB_SDM4	
137	DQS4	VSS31	138		
139	VSS32	DQ38	140	DDRB_SDQ38	
141	DQ34	DQ39	142	DDRB_SDQ39	
143	DQ35	VSS33	144		
145	VSS34	DQ44	146	DDRB_SDQ44	
147	DQ40	DQ45	148	DDRB_SDQ45	
149	DQ41	VSS35	150		
151	VSS36	DQS#5	152	DDRB_SDQS5#	DDRB_SDQS5# 7
153	DM5	DQS5	154	DDRB_SDQS5	DDRB_SDQS5 7
155	VSS37	VSS38	156		
157	DQ42	DQ46	158	DDRB_SDQ46	
159	DQ43	DQ47	160	DDRB_SDQ47	
161	VSS39	VSS40	162		
163	DQ48	DQ52	164	DDRB_SDQ52	
165	DQ49	DQ53	166	DDRB_SDQ53	
167	VSS41	VSS42	168		
169	DQS#6	DM6	170	DDRB_SDM6	
171	DQS6	VSS43	172		
173	VSS44	DQ54	174	DDRB_SDQ54	
175	DQ50	DQ55	176	DDRB_SDQ55	
177	DQ51	VSS45	178		
179	VSS46	DQ60	180	DDRB_SDQ60	
181	DQ56	DQ61	182	DDRB_SDQ61	
183	DQ57	VSS47	184		
185	VSS48	DQS#7	186	DDRB_SDQS7#	DDRB_SDQS7# 7
187	DM7	DQS7	188	DDRB_SDQS7	DDRB_SDQS7 7
189	VSS49	VSS50	190		
191	DQ58	DQ62	192	DDRB_SDQ62	
193	DQ59	DQ63	194	DDRB_SDQ63	
195	VSS51	VSS52	196		
197	SA0	EVENT#	198	MEM_MB_EVENT#	MEM_MB_EVENT# 7
199	VDDSPD	SDA	200		FCH_SDATA0 11,15
201	SA1	SCL	202		FCH_SCLK0 11,15
203	VTT1	VTT2	204		+0.675VS
205	G1	G2	206		

LCN_DAN06-K4406-0102
CONN@

+3VS
RD71 2_10K_0402_5%
CD31 2.2U_0603_6.3V6K
CD38 0.1U_0402_16V7K
RD9 0_0402_5%

+VREF_CB 15mil
+1.35V_VDDQ
RD16 1K_0402_1%
+VREF_CB
RD17 1K_0402_1%
CD55 0.1U_0402_16V7K
CD30 1000P_0603_50V7K

DDR3 SO-DIMM B REV H:8mm
Standard
<Address: 01>

01/15 update DDR address 10 to 01 for common design

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

Compal Electronics, Inc.

Title: SCHEMATIC, MB A9851

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UH1A

HUDSON-2

PCI Host Bus Reset (To EC)

PCIE_CALRP R=50ohm, 4mil,<1000mil
PCIE_CALRN R=50ohm, 4mil,<1000mil

Del GPP PCI-E

ABO connect to USB3.0 PHY.

20mil

SS

For "EXT" CLK mode, input to PCIE,

NSS

APU DISP

APU

VGA

SS

card Reader

Wireless LAN

Ethernet LAN

Del MIN2,Card reader, USB 3.0 IC

25M_X1 and 25M_X1_R=50ohm, 4mil
25M_X2=50ohm, 4mil

25MHZ_10PF_X1E000311000900

RH16 1M_0402_5%

RH130 20M_0402_5%

YC1 32.768KHZ Q13FC13500005

CH15 22P_0402_50V8J

CH16 22P_0402_50V8J

10/22 Eric modify 32.768 footprint.
Close to BOLTON-M2

C1205,C1206
Change for G3
RTC timing issue
<improve amplitude>

32K_X1=50ohm, 4mil,<1500mil
32K_X2=50ohm, 4mil,<1500mil

BOLTON-M2_FCBGA656

PCI CLKS

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

APU

S5 PLUIS

Delete GPU
1202 Calvin

Board ID

VGA_PWRGD_R Change to GPIO51

Del USB3.0_CLKREQ# PH.

ESD@ CH101 0.1U_0402_16V4Z

For EMI Requirement Close to U25

11/08 Reserved BIOS setting

12/25 Eric Del TP_INT#

APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : INOD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

Del USB3.0_CLKREQ#

10/4 Eric Del.

for ESD Close FCH Side

RTC_CLK_R=50ohm, 4mil
RTC_CLK=50ohm, 4mil

W>=15mils

W>=15mils

12/27 Eric Del J1 jumper

01/15 change R860 to Jump for Clear CMOS

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

10/4 Eric Del.

02/02 change +3VALW to +3VS for power rail leakage

Board ID

	FCH_GPIO30	FCH_GPIO31
PX4	0	0
Reserve	0	1
DIS	1	0
UMA	1	1

20mils

W>=15mils

Update to +3VLP

D23 close to U25 (FCH)

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

Compal Electronics, Inc.

Title: SCHEMATIC, MB A9851

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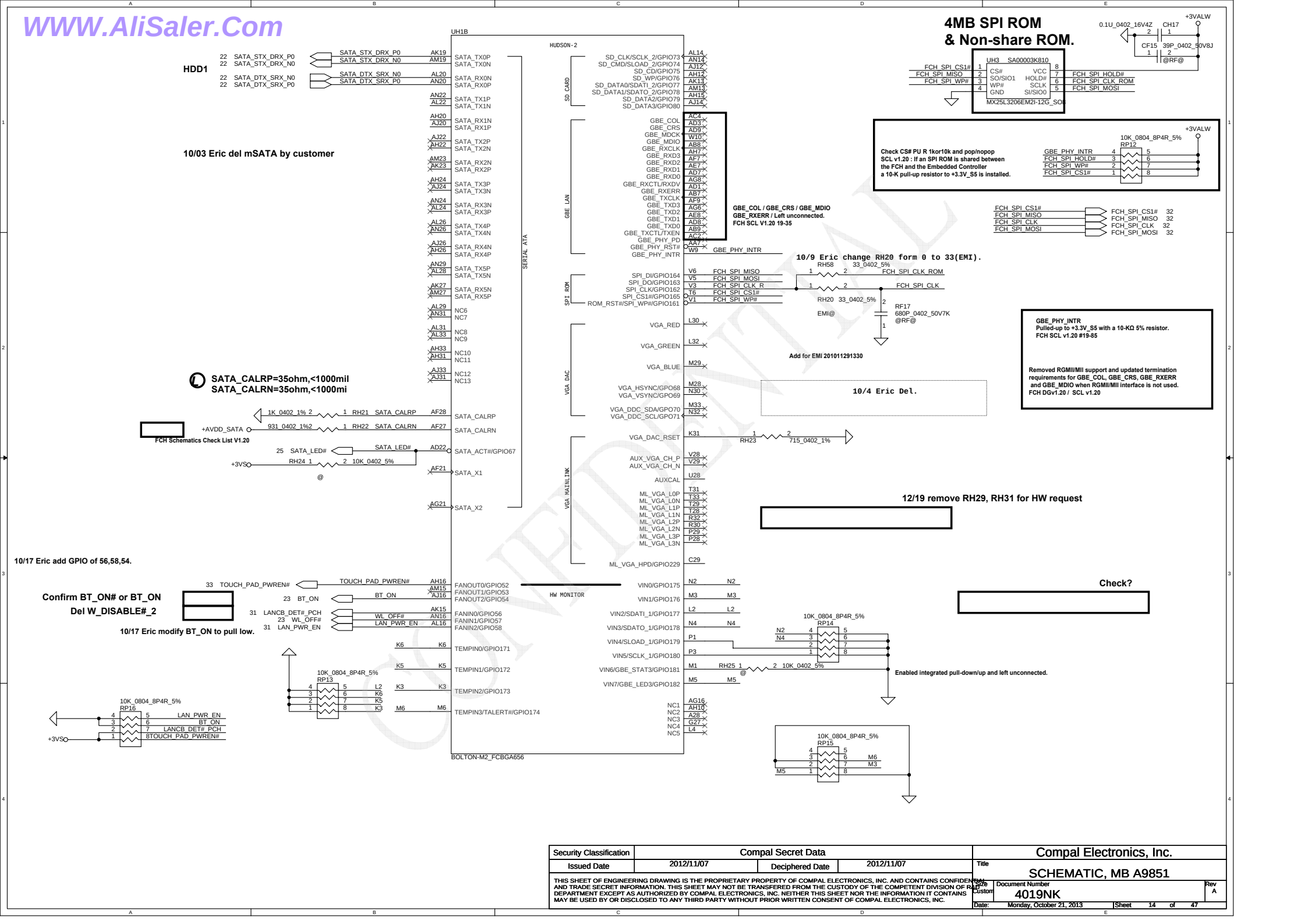

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FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

02/22 Add SUS_STAT#

Check with BIOS

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage

Del ODD_DA#

Del MINI2_CLKREQ#

PC_BEEP use.

10/18 Eric Add SATA_ODD/PCH_AUDIO control pin.

Del SIMB output

Confirm CR det or not.

33ohm termination resistor at CODEC side

Change GPIO fellow Pumori

Del FCH_GPIO187

10/5 Eric modify for EMI requirement

RH65 close to PCH

12/20 Del DDR3L_EN

For FCH internal debug use

Del MINI2_CLKREQ# PH.

10/4 Eric Del.

11/20 Eric add test point from TH8 ~ TH26.

Del FCH_GPIO187 R57 R55

12/06 Del VGA_PWRGD

UH1D

HUDSON-2

BOLTON-M2_FCBGA656

USB 2.0 port(Left-2)

USB 2.0 port(Left-1)/ Charger

Del USB port 9

Mini1-WLAN

Del USB port 7

01/30 Eric del WWAM for USB 6.

Camera

Touch

USB 2.0 / To IO Board. 10/29 change from 2 to 1.

USBSS_CALRP=35ohm,<1000mil
USBSS_CALRN=35ohm,<1000mi

USB 3.0 port(Left-2)

USB 3.0 port(Left-1)

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

Hudson-M2/M3 OHCI CTL DEV 20, Fn 5 <Disable CTL>

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>

Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

Hudson-M2/M3 EHCI CTL DEV 19, Fn 2

Hudson-M2/M3 EHCI CTL DEV 18, Fn 2 <Support Wakeup>

Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

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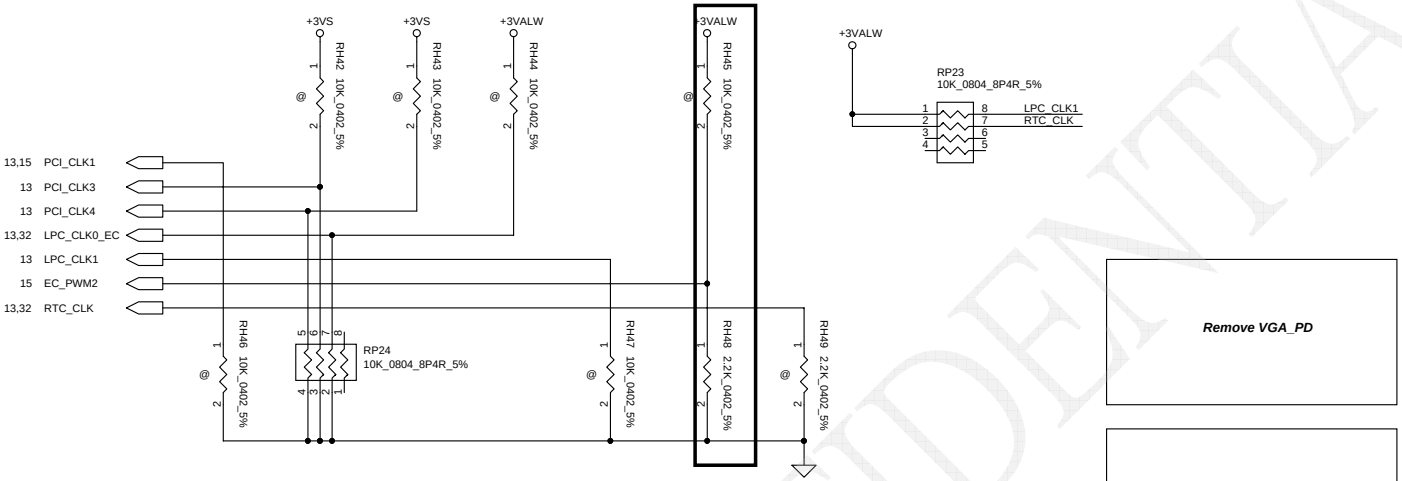
STRAP PINS

Change to SPI

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



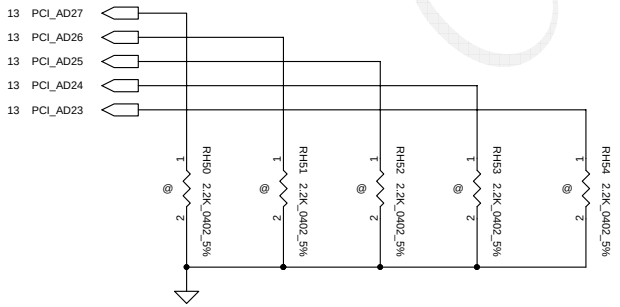
Remove VGA_PD

Remove VGA_PD

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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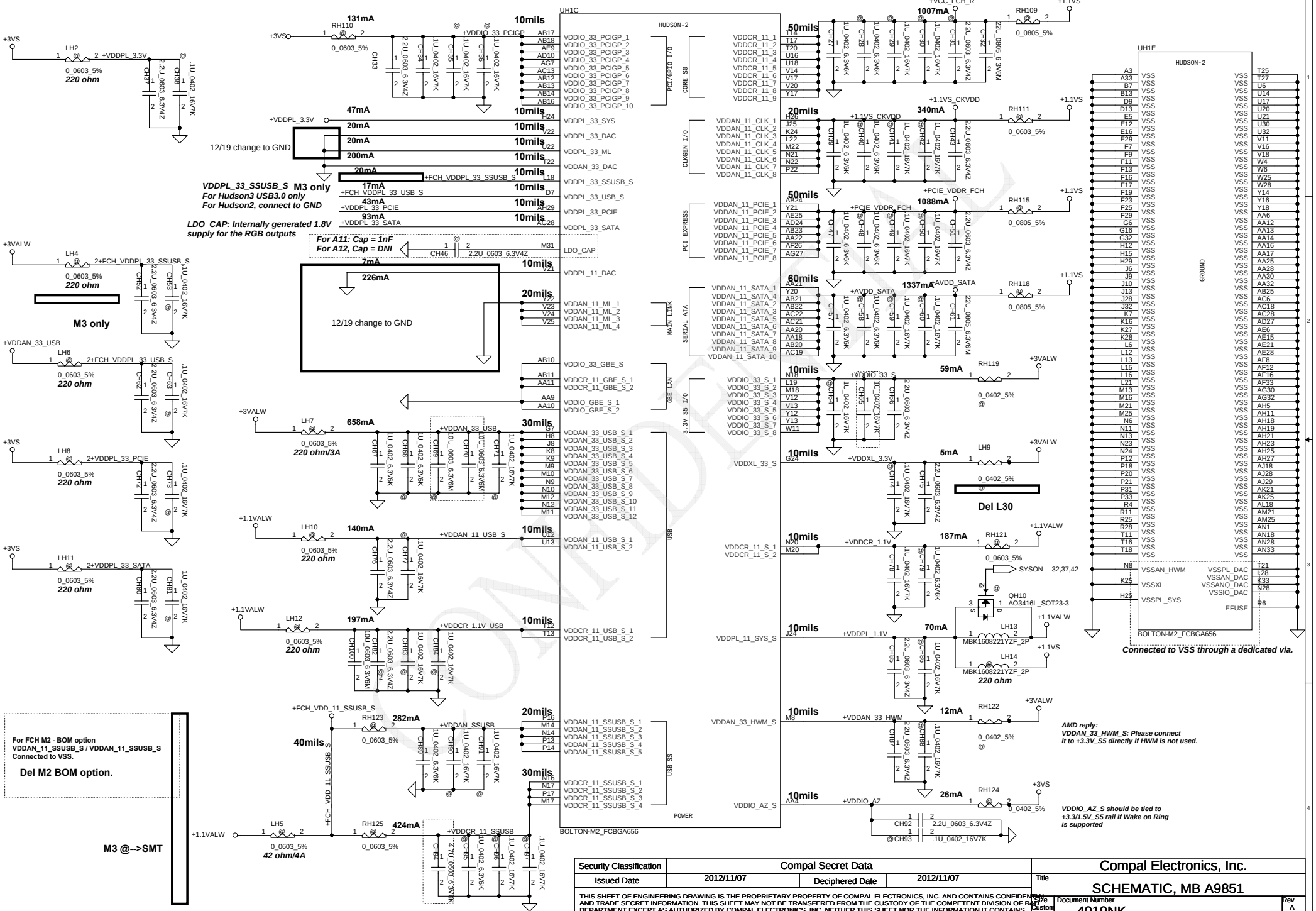

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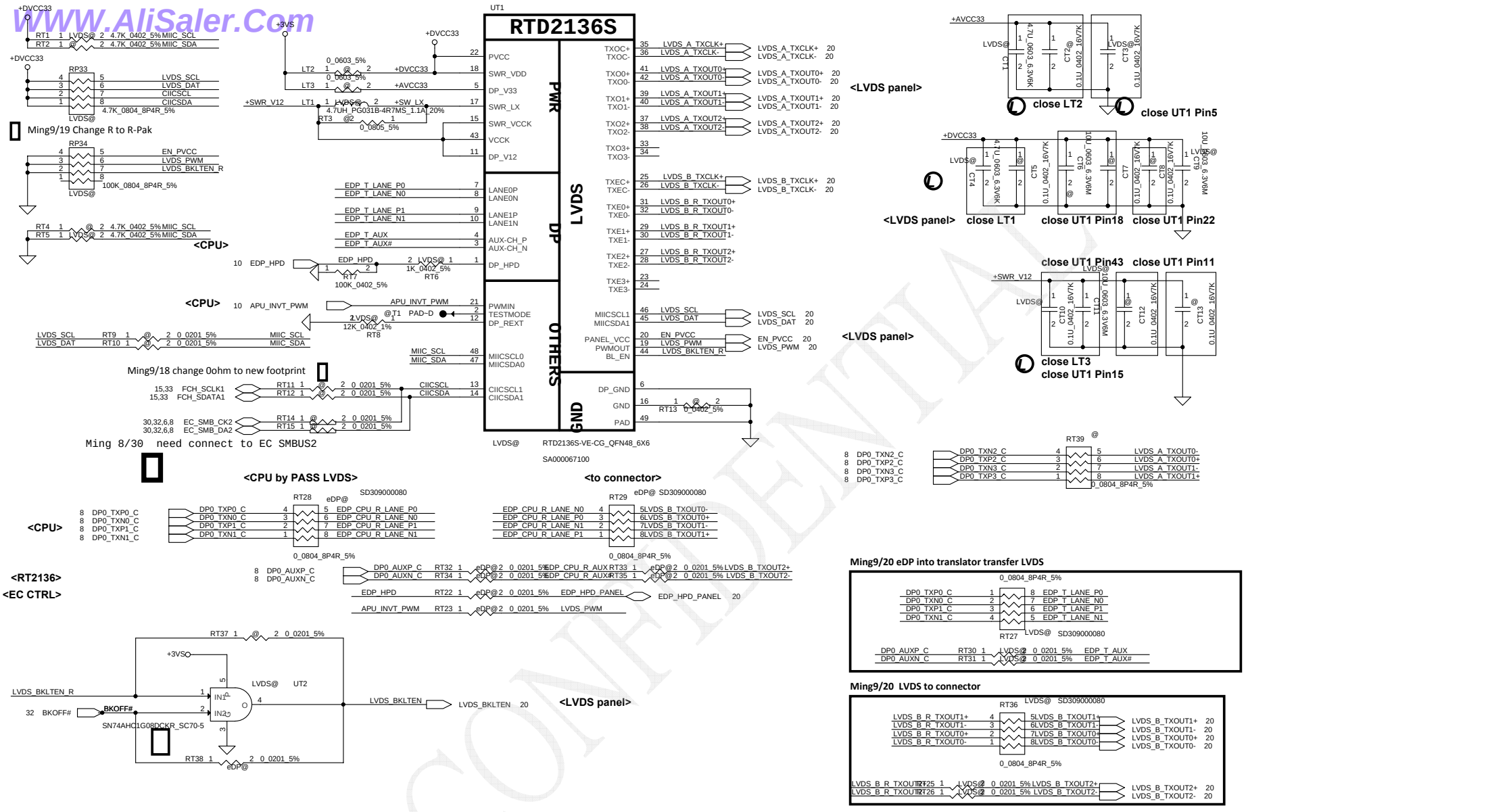

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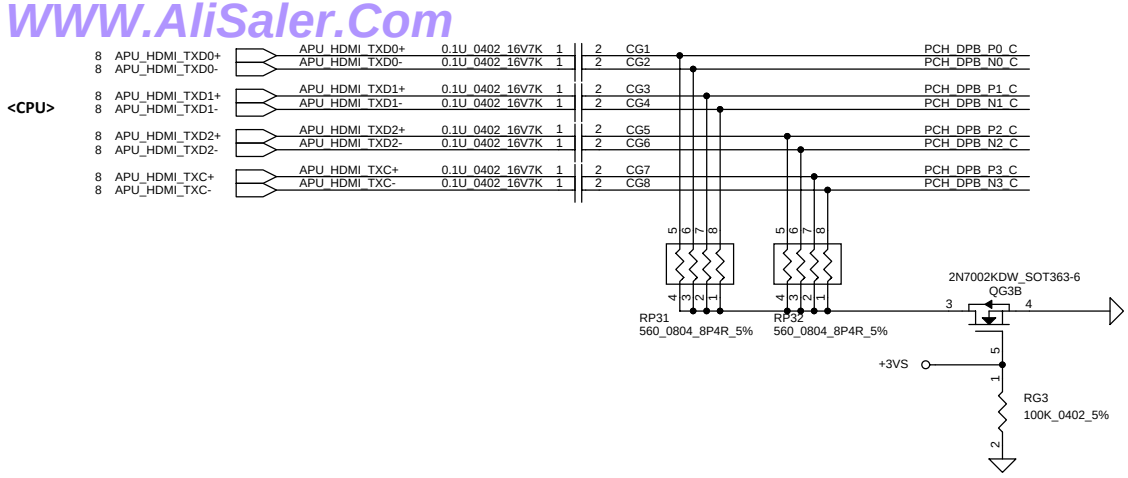
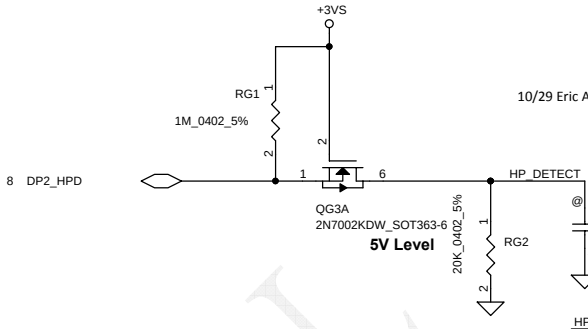
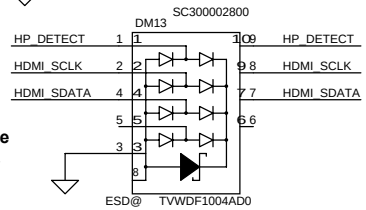
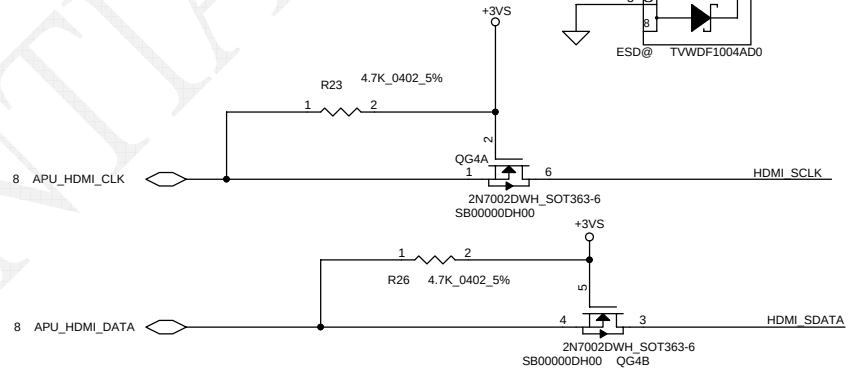




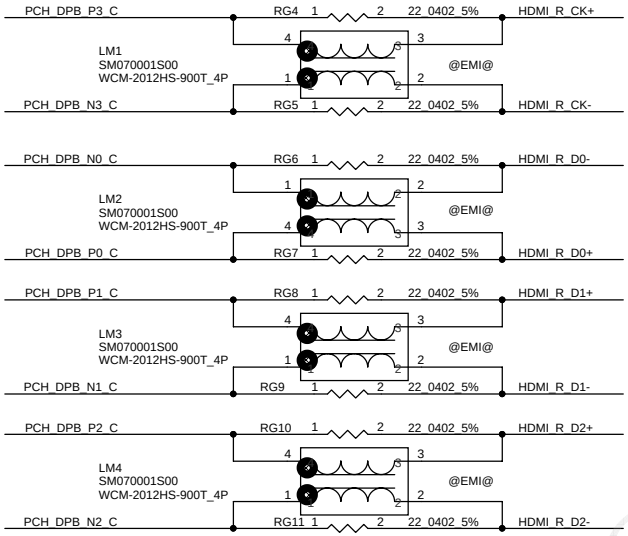
10/29 Eric Add ESD solution on HDMI_HPT

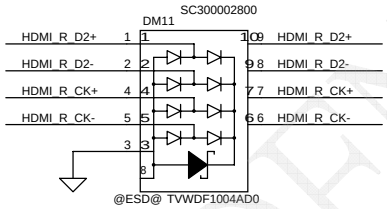


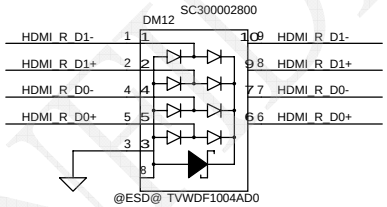
9/11 remove RG58/RG62 for doublle PU to CPU side



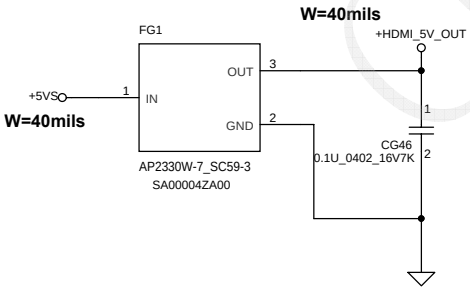
5V PULL UP IN CONNECTER SIDE



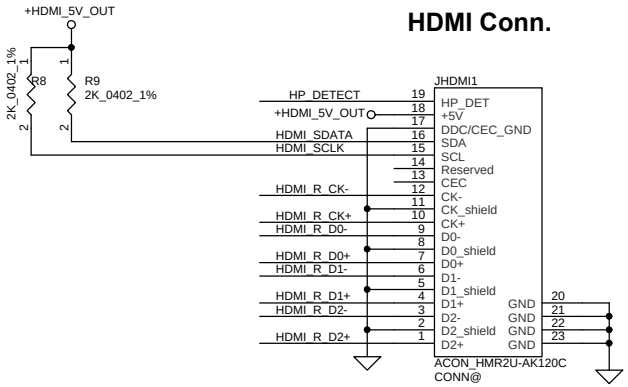




10/9 Eric Remvoe CM2 ~ CM9 for EMI requirement.



HDMI Conn.



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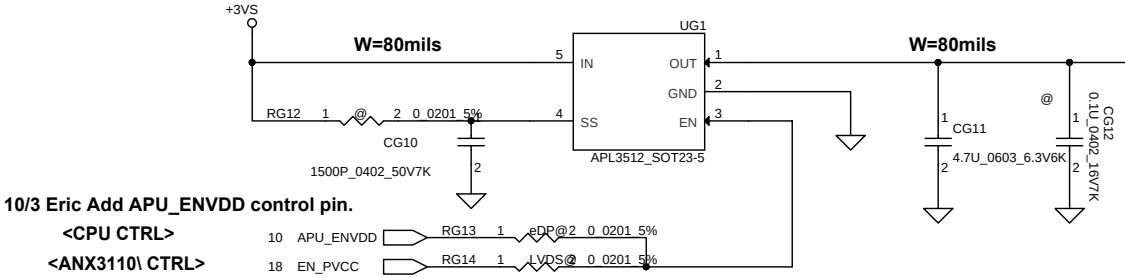
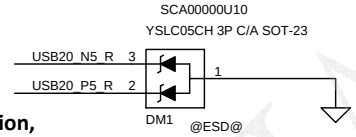


W=60mils W=60mils

10/20 Del LG1.

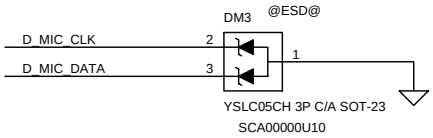
10/4 Eric Del.

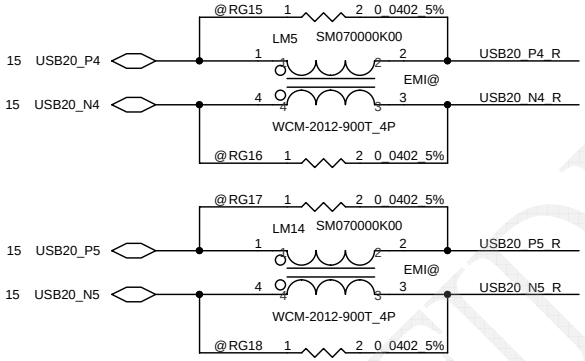
SM010014520 3000ma
220ohm@100mhz
DCR 0.04

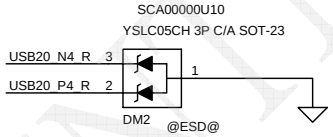


9/26 Eric remove common chock for touch screen portion, ask key part to add in touch IC side.

Put CF11 near webcam connector.







<LVDS>

<DB>eDP-->Dual LVDS

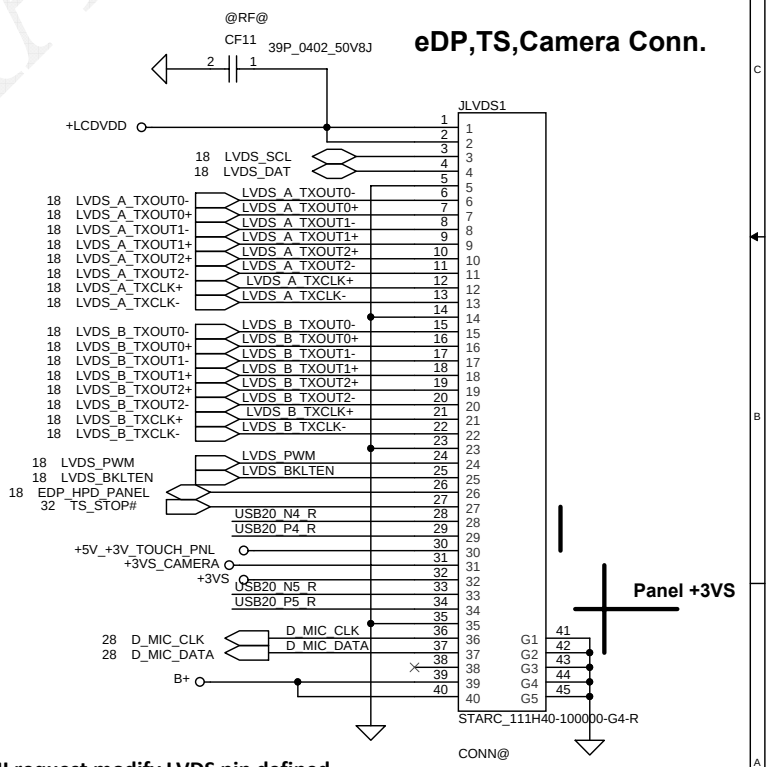
8/30 colay eDP use

<USB Touch panel>

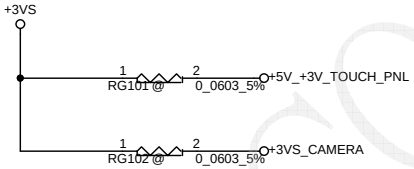
<Touch panel>

<Camara and DMIC>

<Camera>



10/3 Eric Del power switch of +3VS_CAMERA & +5V_+3V_TOUCH_PNL.



9/6 by EMI request modify LVDS pin defined

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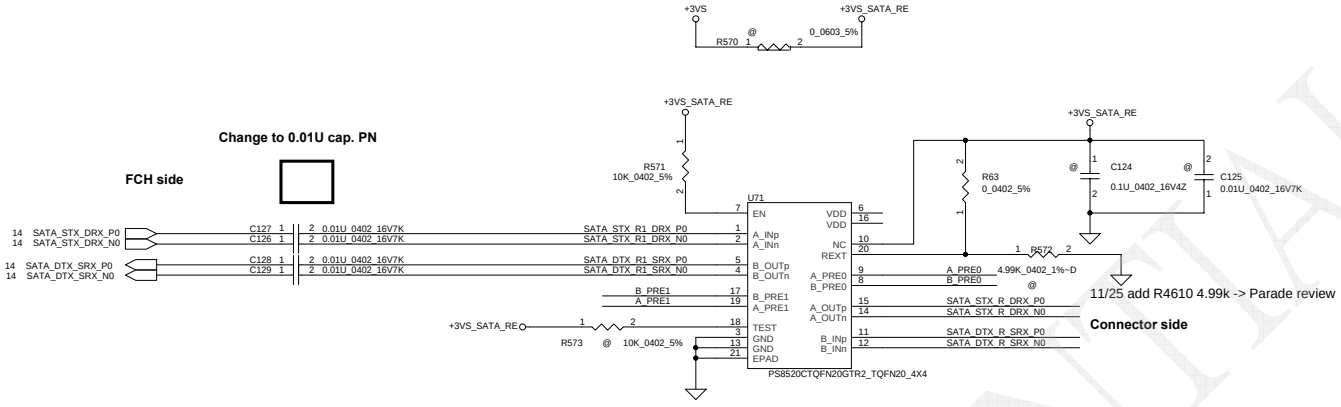
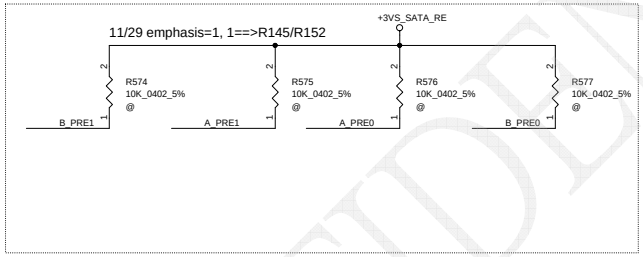
mSATA Conn.

10/03 Eric Del mSATA by customer

Reserve SATA Redriver

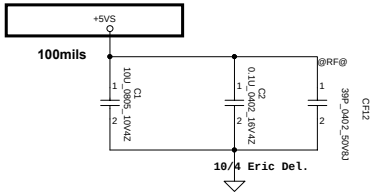




Need Vendor check value

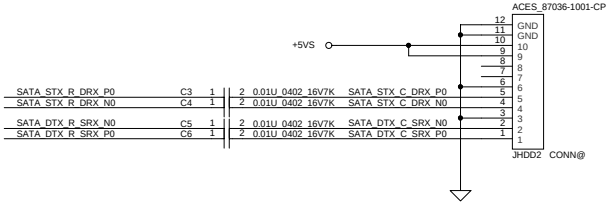
SATA0 (HDD)

02/22 Eric remvoe SATA power 0 ohm to +5VS.



02/22 Eric remvoe SATA 0 ohm co-lay.

<DB>Change to 10 Pin **2.5" HDD Conn.**



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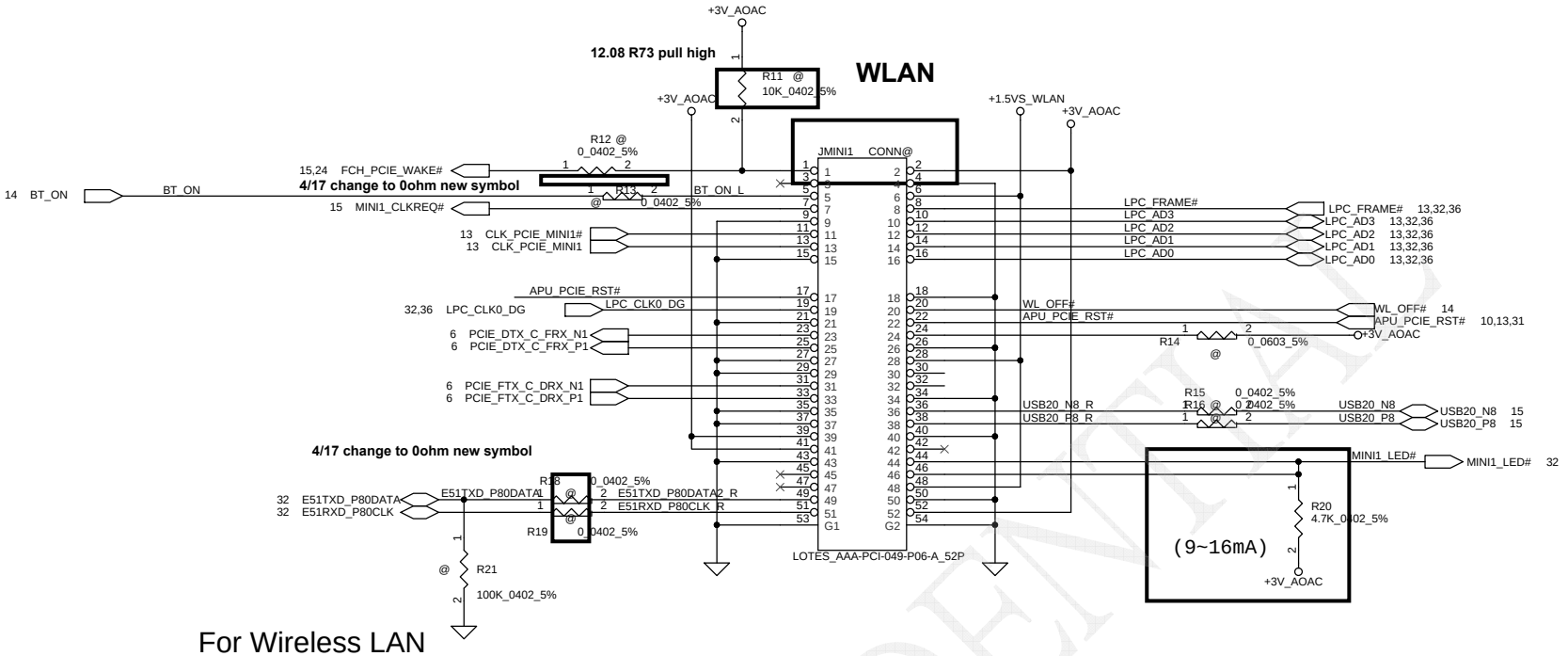
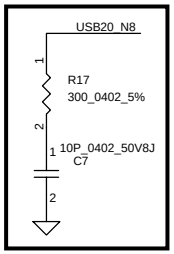
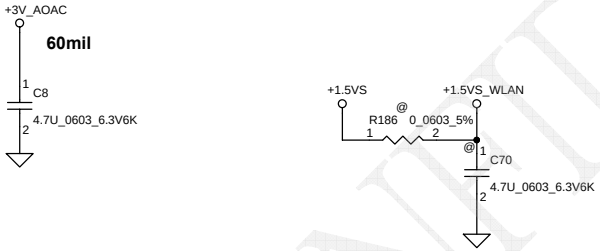


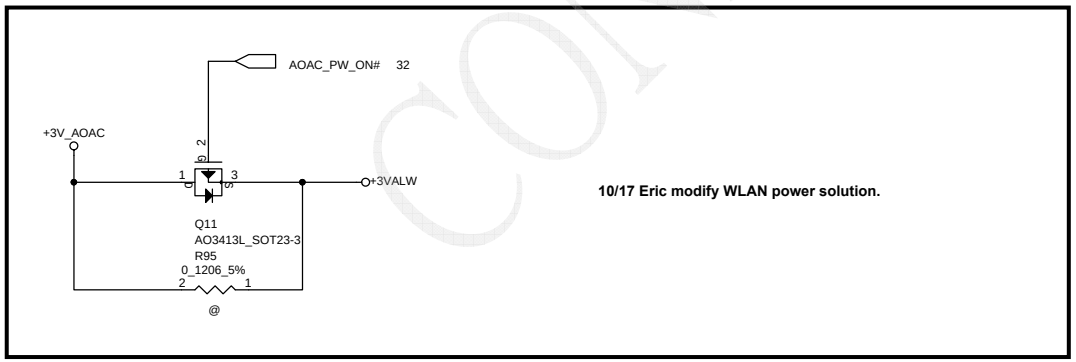
12/21 for AMD issue workaround



For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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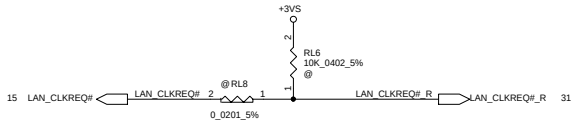
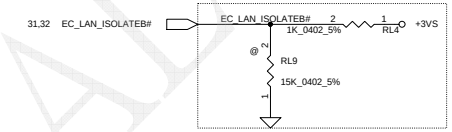
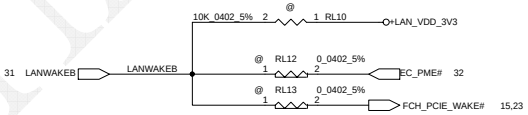




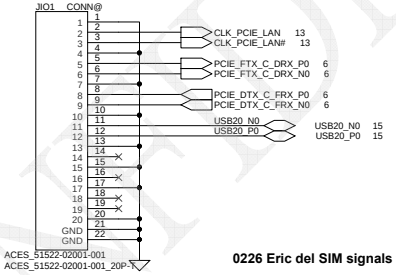
10/19 Eric del @ of RL10 for pull high, Del FCH_PCIE_WAKE# net, short RL12.



LED

<DB>Change to subboard.

20 Pin FFC



0226 Eric del SIM signals for remove WWAN.

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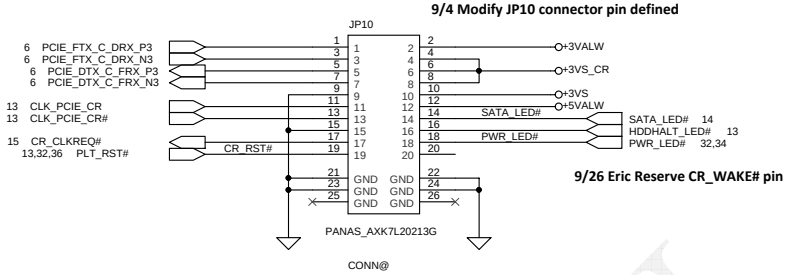
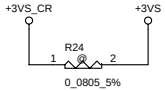
Card reader conn

9/4 Modify JP10 connector pin defined



9/26 Eric Reserve CR_WAKE# pin



10/4 Eric Reserve R212 for card reader power rail.

<CPU>

10/4 Eric Del +3VS_CR power rail from power switch

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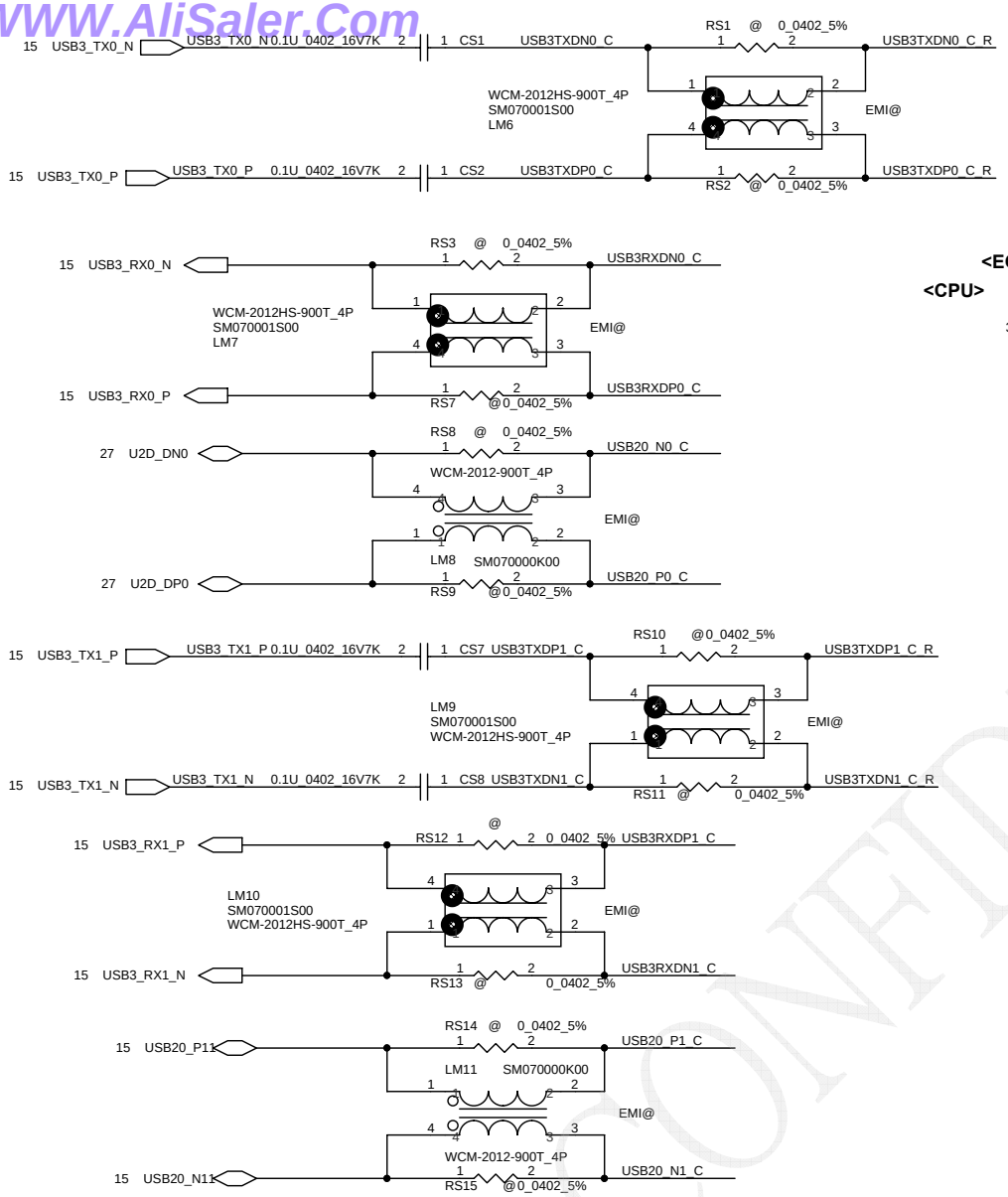
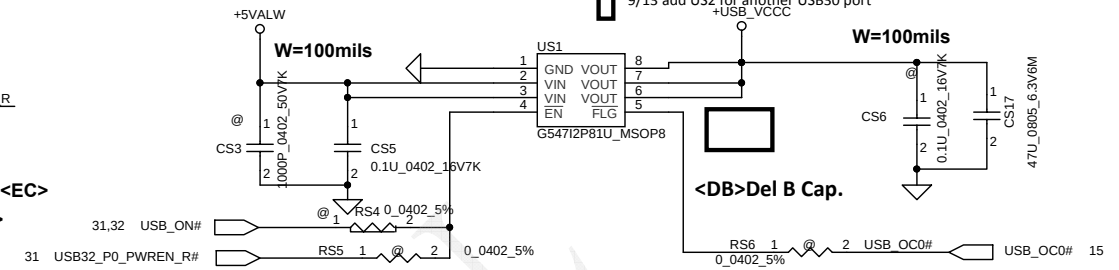


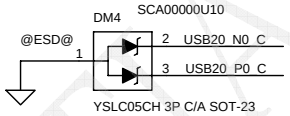
<EC>
<CPU>

USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

9/13 add US2 for another USB30 port



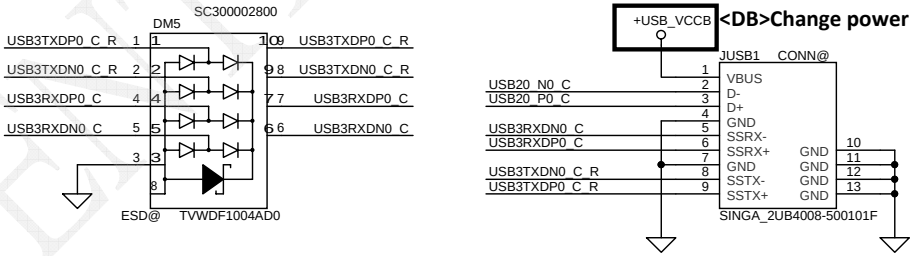
9/26 Eric change CS14 form 150uF to 47uF.

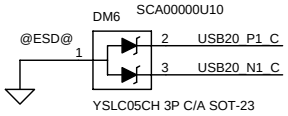


<DB>Update footprint to DC233008M10.

USB2.0/USB3.0 port 1

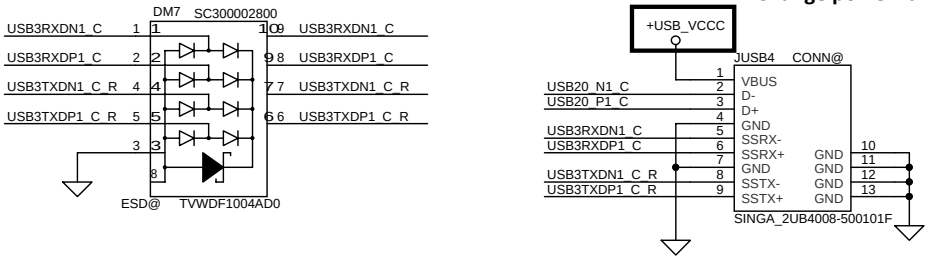
<DB>Change power rail to U18.





USB2.0/USB3.0 port 2

<DB>Change power rail to U18.



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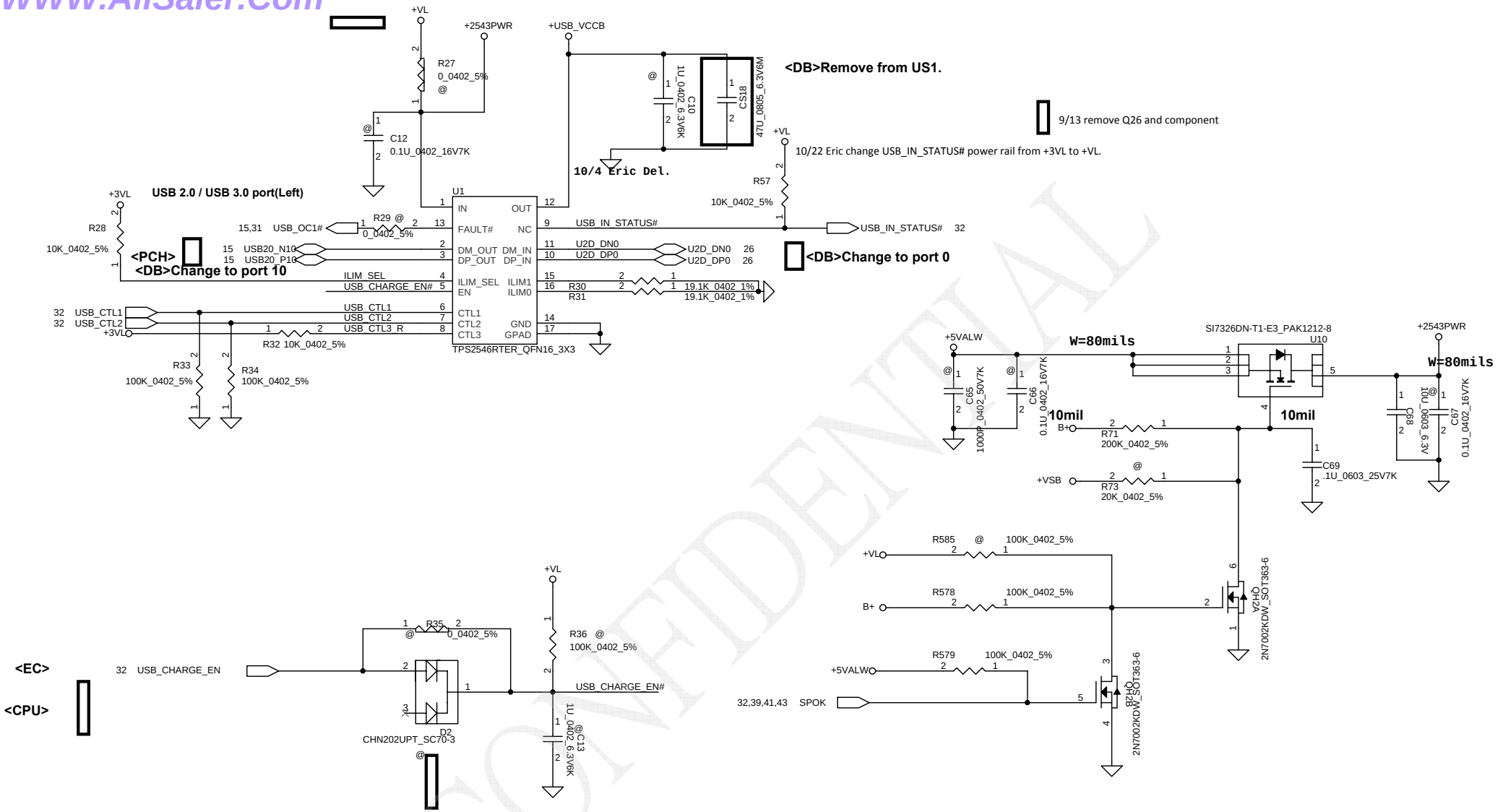

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DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place AVDD ,PVDD,and DVDD capacitor close to Codec

RB3 Bead Max I=200mA

RB1 Bead Max I=3000mA

11/06 Beads close to UB1.

Ext MIC

HP Jack

Internal SPKR

Place C208 close to Codec

Place C209,C210,CA87,CA89 close to Codec

9/17 add RF solution

change PN(SA000059J10) for 92HD91B2X5NLGXWCX8

9/18 add reserve CB28, CB29 and stuff CB25,CB22,CB21 0.1uF

10/9 Eric Add EMI@ solution for CB31, CB35 & CB36 form EMI requirement.

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

PLACE CLOSE TO U1 PIN 14

Place need close UB3

10/17 Eric Del +5VALW to +5VS_AUDIO.

Audio power

Audio power

SB Beep

Check HP LDO PN

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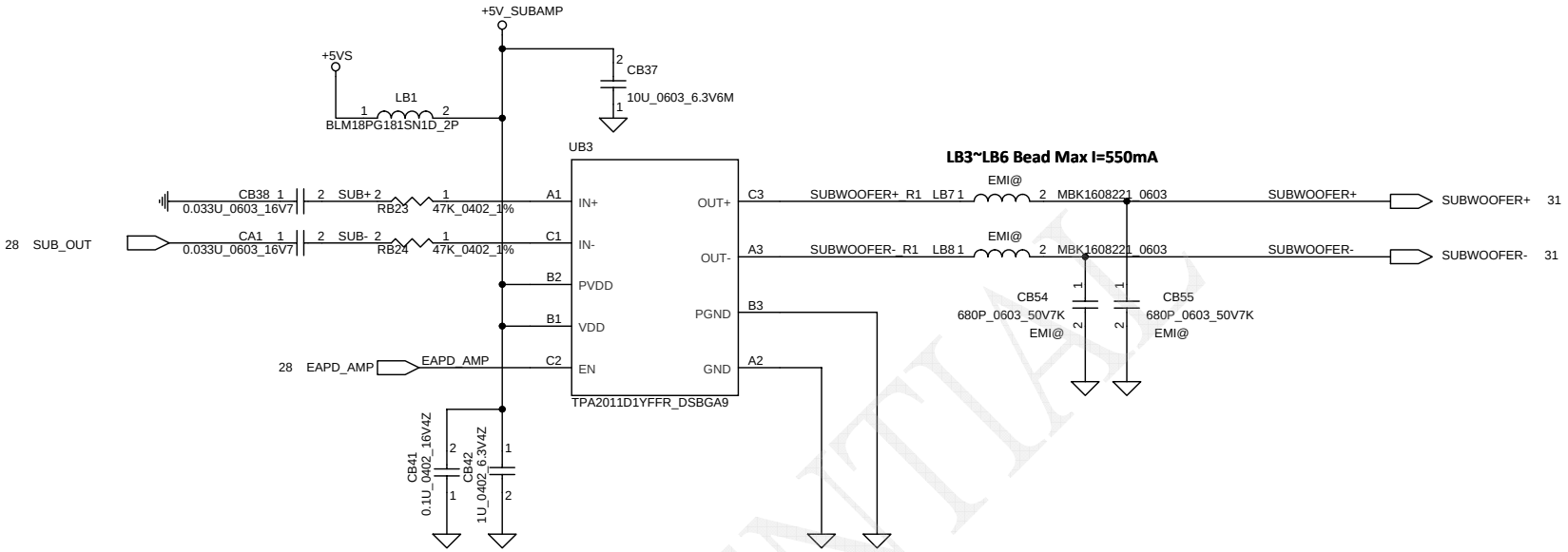
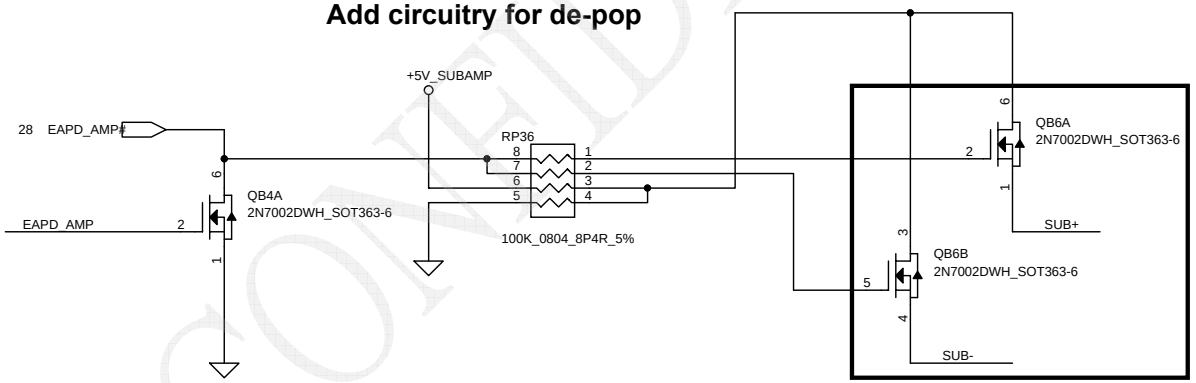
Subwoofer AMP TPA2011 = HPA01086YFFR

DB> TPA2012 Change to TPA2011



Add circuitry for de-pop



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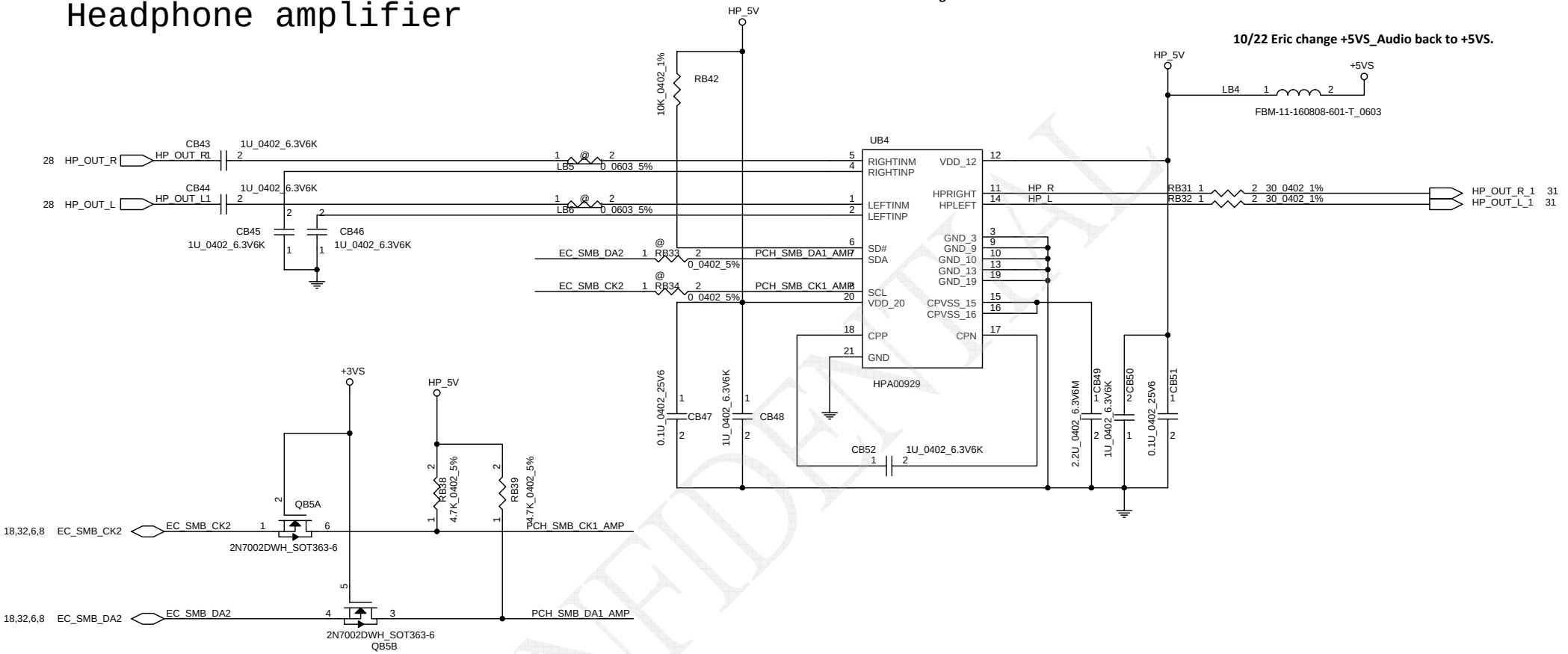
Headphone AMP TPA6130A2 = HPA00929

DB> HPA01196 Change to HPA00929

Headphone amplifier

10/22 Eric change +5VS_Audio back to +5VS.



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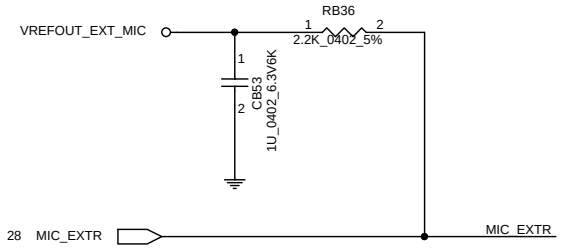
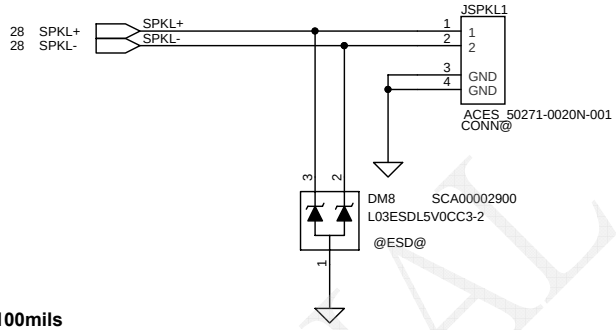
Ext. Mic

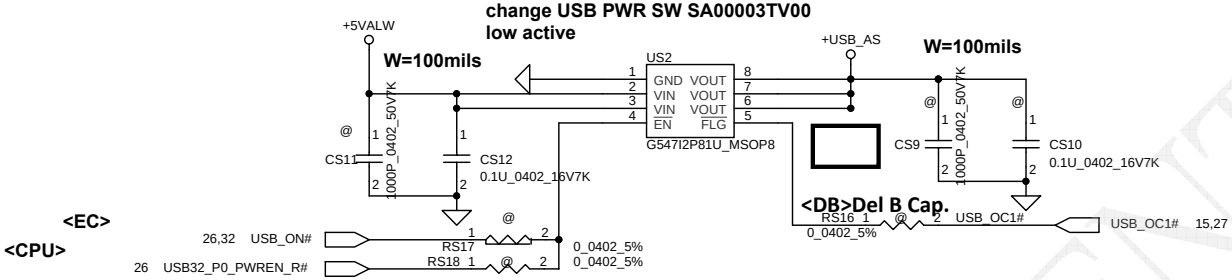


Front Speaker Connector 1

SPK conn

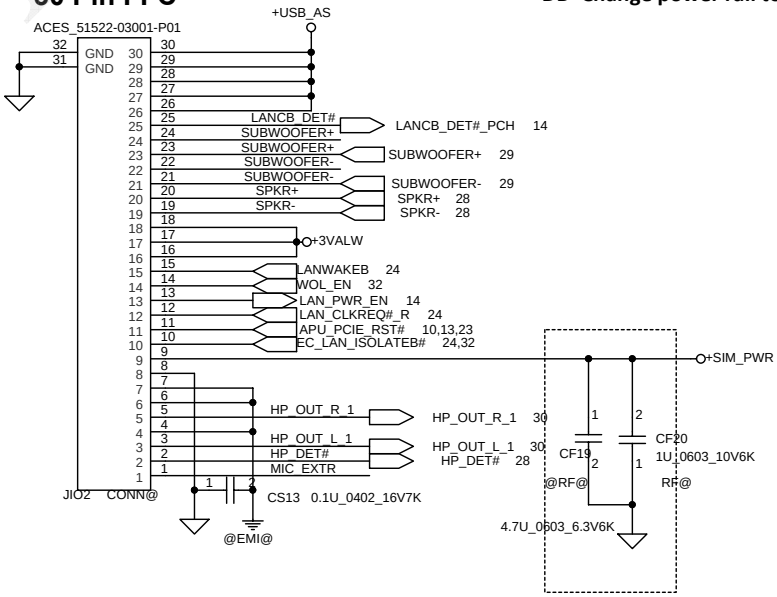


USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active



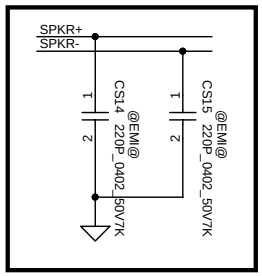
Headphone and Mic conn

30 Pin FFC



<DB>Change power rail to US1.

11/06 EMI Cap close to JIO2.



10/30 RF add, near JIO1 connector.

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Ming9/3 change to 8.2KK for DB phase board ID

	DB	SI	PV	MV
Board ID Rk13	0 K ohm	12K ohm	15K ohm	20K ohm
Project ID RK11	56k ohm	56k ohm	56k ohm	56k ohm

<DB>Add RK57

<DB>KBC 9012

Board ID control

Ming9/3 change Board ID to 8.2K for CS DB phase

<DB>Del HDMI_PWR_PD

<DB> add DGPU_GC6_EN on Pin M2

Ming8/28 remove DGPU_GC6_EN for UMA only

Ming 8/30 remove MINI1_LED#

MINI1_LED# NonCS only

Ming 9/3 add ADP_ID for power

Ming9/18 change 0ohm to new footprint

<DB>Add PM_CLKRUN# and RK59

10/24 Eric modify SMBUS1 power rail to +3VALW_EC.

<PWR>

<HW>

Ming 9/4 add WWAN_OFF# to GPIO3D

Ming 9/3 remove LANCB_DET# EC and RK55

Ming 9/3 remove TP_ON_OFF_LED#

Eric 9/25 Add WWAN_OFF# to GPIO3D

Add LANCB_DET#_EC

EAPD:NonCS only

Ming 8/30 remove EAPD

Ming9/13 remove EC_SMI# for EC request

10/15 Eric remove SUSACK#.

<DB>Del EC SPI signal

EC suggest does not use as GPIO

<DB>Del EC SPI ROM

<DB> add VGA_THRMTRIP# on Pin J2

<DB> add FB_CLAMP_TGL_REQ# on Pin K2

<DB> add DGPU_HOLD_RST# on Pin M1

<DB> add GPU_THERMAL_DET# on Pin N2

Ming8/28 remove GPU GPIO for UMA only

Ming 9/13 remove PM_BATLOW#

Ming9/13 add KSO16/ KSO17 for KB request

10/16 Eric change vgate from pin97 to pin 74.

10/18 Eric Add AOAC_PW_ON.

Add EC_LAN_ISOLATEB#

Ming9/18 change 0ohm to new footprint

2/22 Eric Add SPOK to EC N7.

Add PROC_DETECT#

Ming9/3 remove PROC_DETECT#

change PM_SLP_SUS# to GPIO15

10/3 Eric Del ENBKL control pin.

10/16 Eric Change VR_ON to 108.

<DB>Remove @ 32.768KHz 'XTAL

<DB>Pin117 NC-->NMI_DBG#

<DB>RK56 10K-->100K

10/4 Eric Del.

<DB>Remove JFW1

<DB>RK50 10K-->100K

10/4 Eric Del.

20mil

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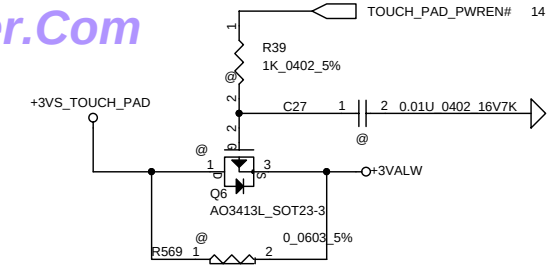
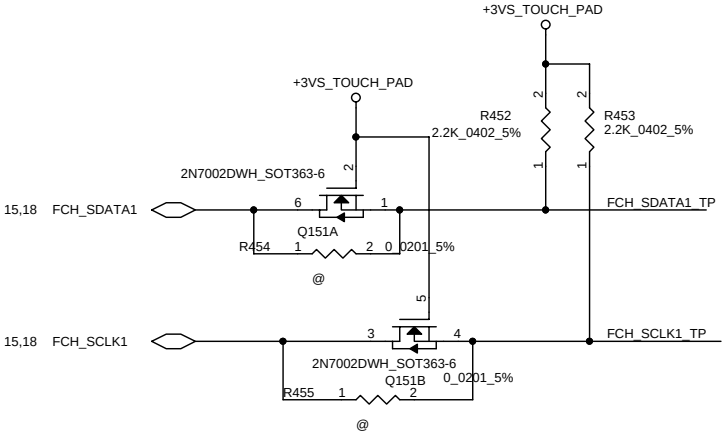
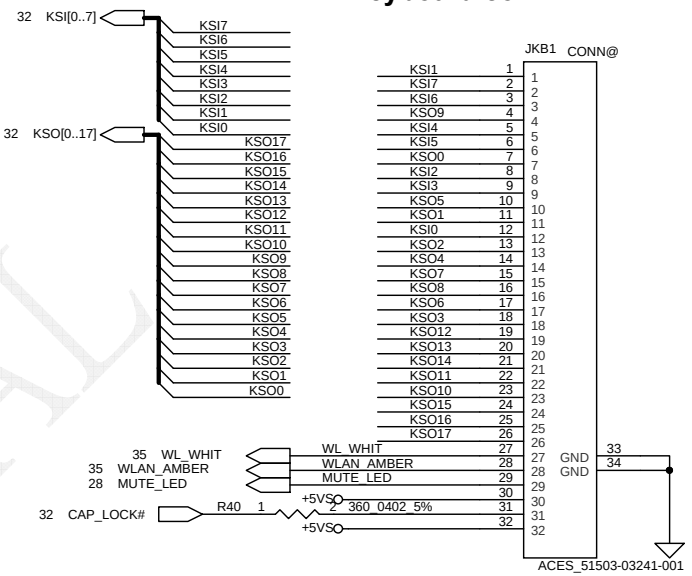




10/29 Del all KB caps.

EMI reserve

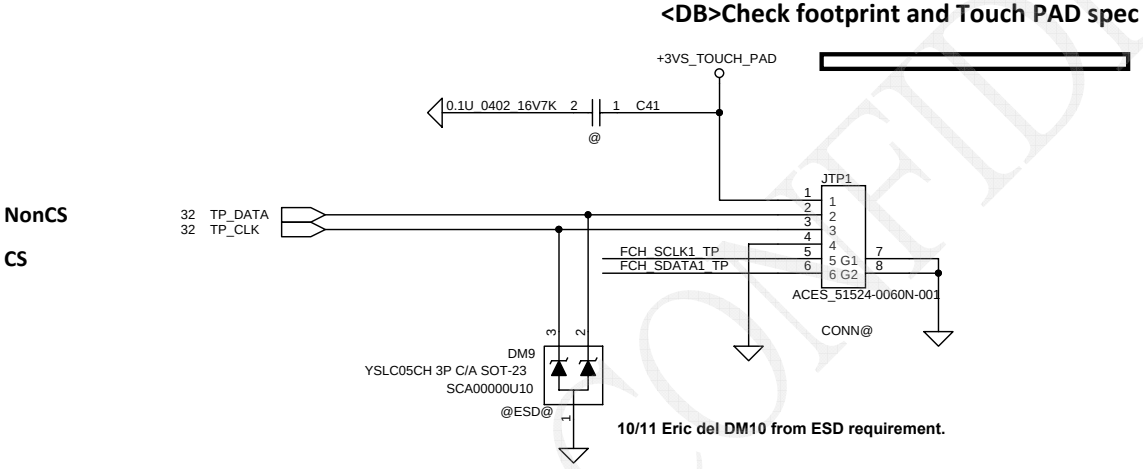
Keyboard conn



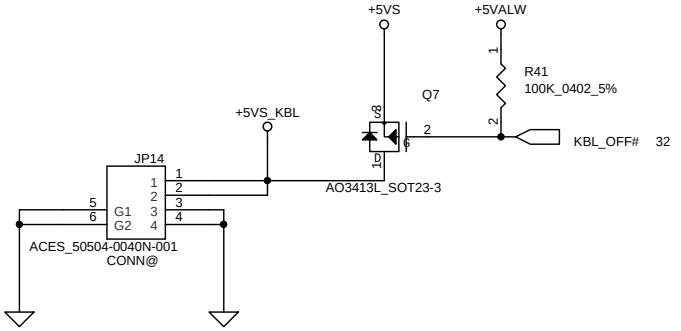
Touch pad conn

Keyboard backlight Conn

<DB>Check footprint and Touch PAD spec



10/11 Eric del DM10 from ESD requirement.



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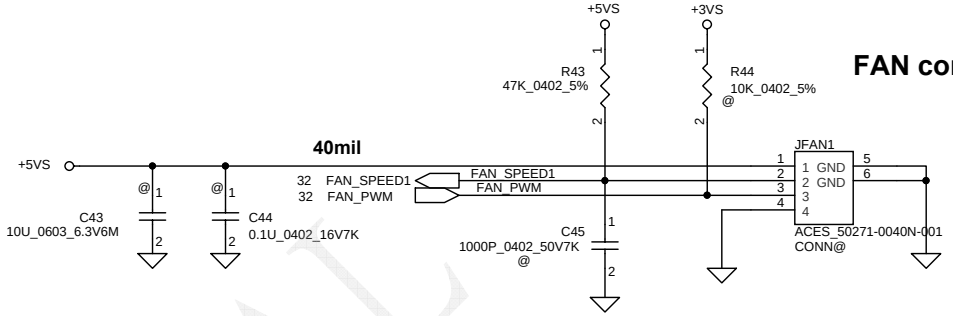
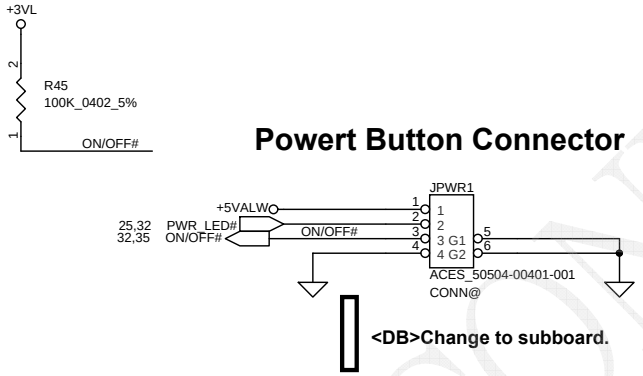
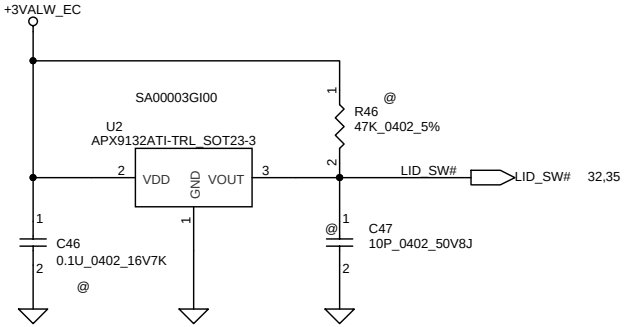
FAN conn



Powert Button Connector



Lid Switch (Hall Effect Sensor)



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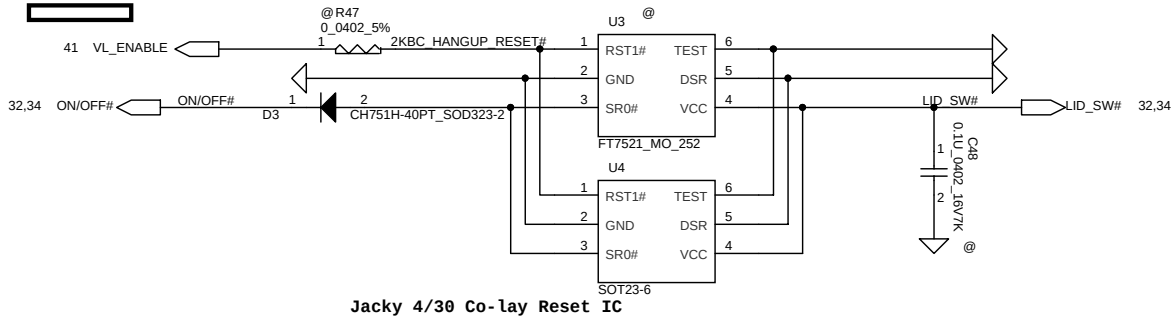
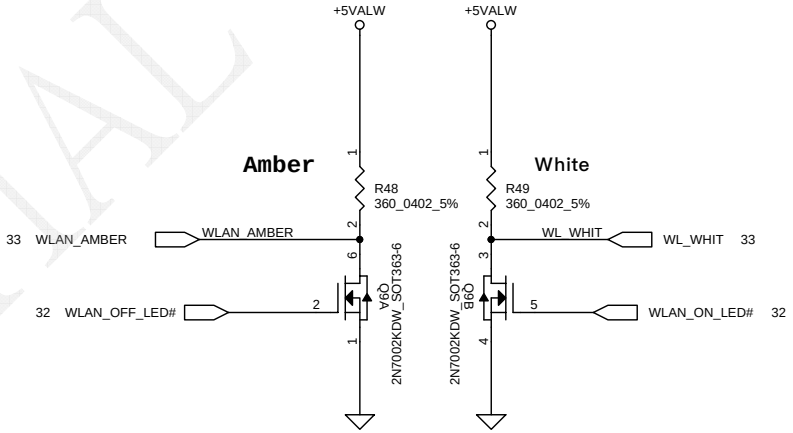
Reset IC

<DB> RST1# connect to ENM



Jacky 4/30 Co-lay Reset IC



CPU

H1 H_3P3 HOLEA
H2 H_3P3 HOLEA
H3 H_3P3 HOLEA
H4 H_3P3 HOLEA

PAD1
MB_SUP_BRK_25X5
HOLEA

Card reader

H7 H_3P3 HOLEA
H8 H_3P3 HOLEA

PCB
ZZZ1
LA-9851P
DA6000Y8000

H13 H_2P8 HOLEA
H5 H_2P8 HOLEA
H6 H_2P8 HOLEA
H16 H_2P8 HOLEA
H10 H_2P8 HOLEA

FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

H15 H_3P0X2P5 HOLEA
WWAN
H9 H_2P8 HOLEA
H11 H_3P3 HOLEA
H12 H_3P3 HOLEA
WLAN

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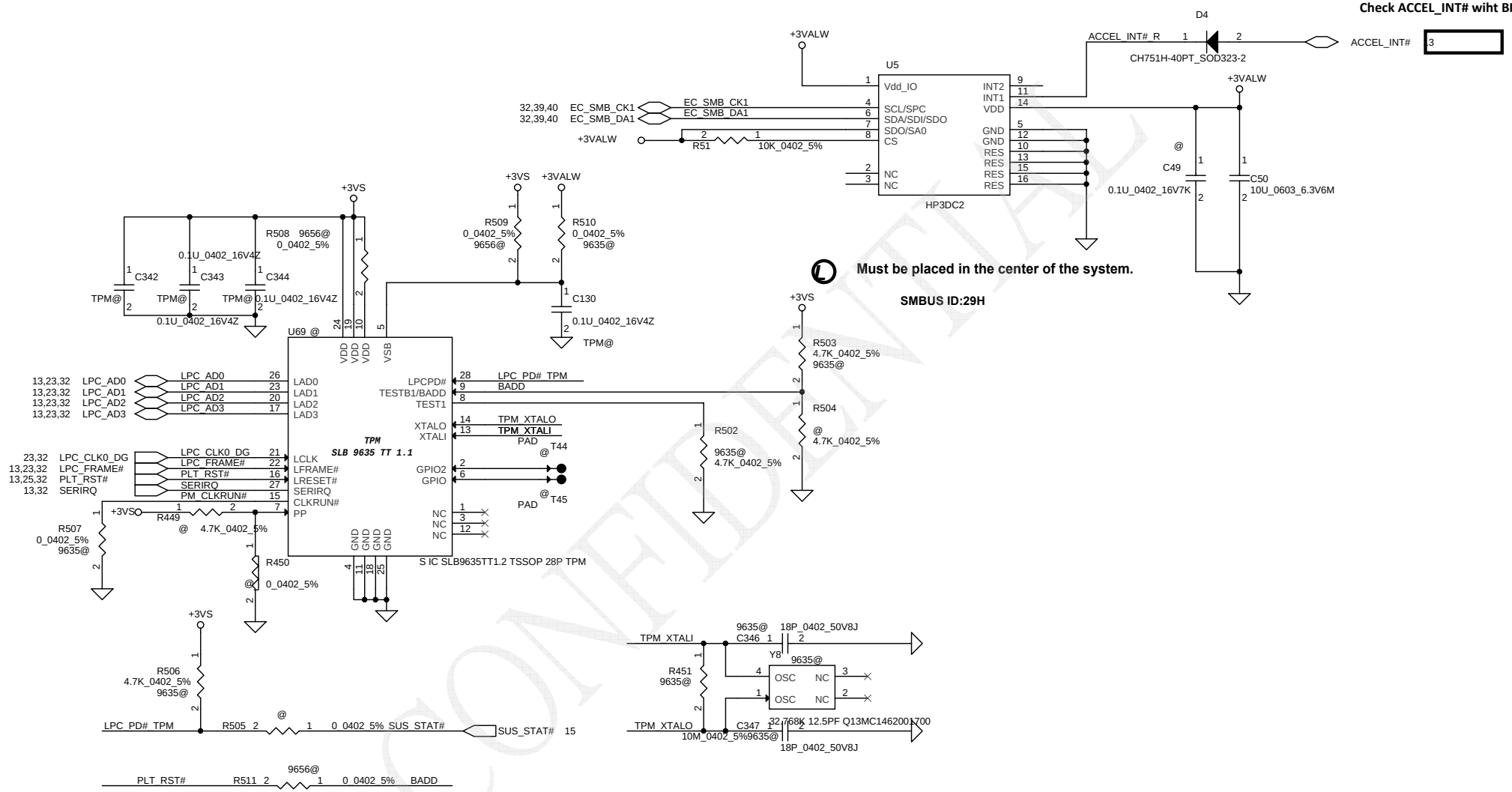
ACCELEROMETER

Sensor hub -->G-sensor

Check ACCEL_INT# wiht BIOS



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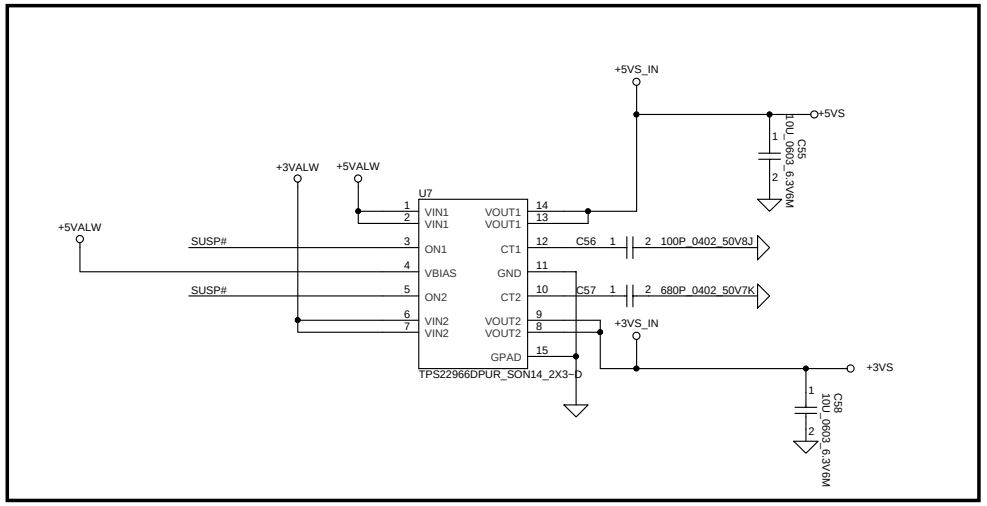
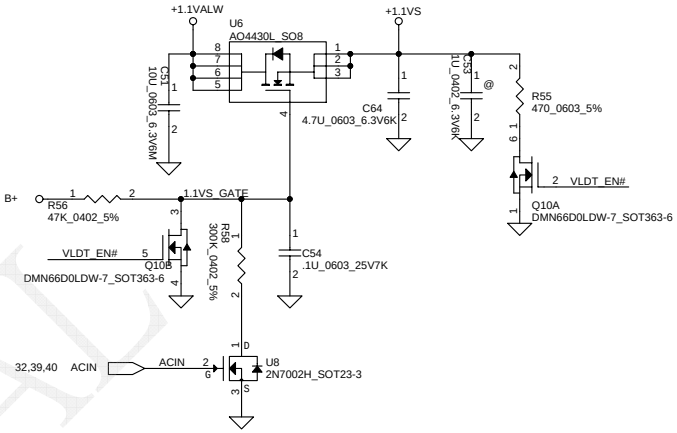
3/6 Co-lay 3VS/5VS low switch circuit

Each 250pF on CAP_MOS1 (2) will make
Slew Rate(uS/V) increase of 100uS/V

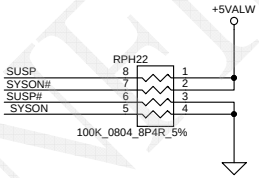


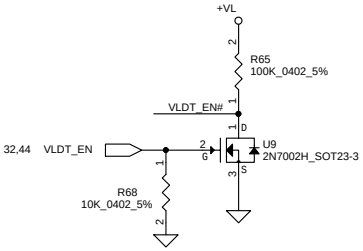
+1.1VALW TO +1.1VS (1.1A)

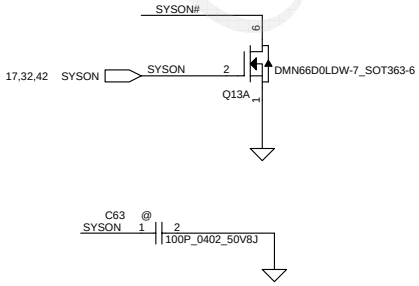


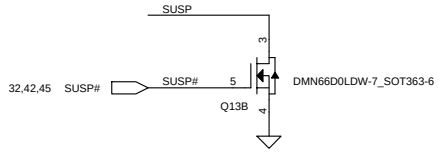
+1.5VTO +1.5V_PCIE

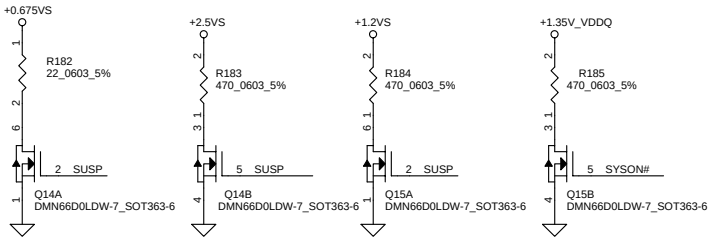
10/17 Eric Del +1.5V to +1.5V_PCIE.











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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Version
1	23	Del short pad of R22	1/7		For Port80 issue	0.2
2	32	Change RK33 from 0 ohm to 12k ohm.	1/7		For SI phase board ID requirement	0.2
3	27	Add R578	1/7		For USB charger port requirement	0.2
4	13	Add CH101	1/7		For ESD requirement	0.2
5	23	Del R76, Q150, R370 and C73	1/7		For EC control directly	0.2
6	15	Change RF9 from 680pF to 15pF	1/7		For FIX EA issue	0.2
7	13	Add CH18	1/7		For FIX PLT_RST# noise	0.2
8	32	Del RK35	1/7		For EM1 no requirement	0.2
9	26	Add RK37	1/7		For support WOL in DC S5 mode	0.2
10	41	Change jump net name +3VLP to +3VL	1/7		For connection between PWR and HW	0.2
11	41	Change net name VL to +VL	1/7		For connection between PWR and HW	0.2
12	44	Change net name SUSP# to VLDT_EN for 1.2V EN	1/7		For connection between PWR and HW	0.2
13	39	Reserve PC9, PC10, PC13, PR13, PR14, PR16, PR18, PQ2, PQ4	1/7		For charger IC +VSB circuit	0.2
14	40	Change net name +3VALW to +3VL	1/7		For correct cell selection in S5	0.2
15	40	Change PR111 from 0 ohm to 2.2 ohm.	1/7		For EM1 request	0.2
16	40	Mount PC110, PC108, PR113, PC120	1/7		For EM1 request	0.2
17	40	Add PC136 0805 10uF	1/7		For EM1 request	0.2
18	39	Reserve PR29, PR31, PR32, PR33	1/7		For AC LED circuit	0.2
19	39	Reserve PQ6, PU4A, PU4B, PD8, PR19, PR20, PR21, PR22, PC22, PC23	1/7		For One Shot circuit	0.2
20	39	Reserve PR23	1/7		For Hysteresis resistor	0.2
21	39	Change net name H_PROCHOT#_EC to EC_THERM	1/7		For correction	0.2
22	41	Change PR302 from 30k ohm to 30.9k ohm	1/7		For USB port load issue	0.2
SI2		SI2	SI2		SI2	
1	21	Remove WWAN portion.	1/30		For HP requirement.	0.4
2	32	Change RK33 to 20K ohm from 15kohm.	1/30		For EC requirement.	0.4
3	45	Change PWM IC from ISL62771 to ISL6277A	1/30		For Power +APU_CORE_NB two pahse requirement.	0.4
4	45	Add one more phase for CORE NB and Use Dual-N MOSFET for each phase.	1/30		For Power requirement.	0.4
PV		PV				
1	32	Change RK33 from 20k ohm to 27k ohm.	3/03		For PV phase board ID requirement	0.5
2	36	Reserve TPM circuit	3/03		For HP requirement.	0.5
3	22	Remove R60, R61, R62 and R63.	3/03		Remove SATA co-lay.	0.5
4	43	Add PR1106.	3/03		For EC Fix code requirement.	0.5
5	22	Remove R69.	3/03		Remove +5V_HDD 0hm.	0.5
6	46	Modify +CPU_CORE_NB to two phase soluiton.	3/03		For PWR requirement.	0.5
7	32	Add C71, C73.	3/03		For ESD requirement.	0.5
8	15	Add C72.	3/03		For ESD requirement.	0.5
9	15	Reserve C74.	3/03		For ESD requirement.	0.5
10	13	Add C75.	3/03		For ESD requirement.	0.5
11	24	Move Lan chip to sub board.	3/03		For HW requirement.	0.5
12	41	Reserve PR318	3/03		For EM1 requirement.	0.5
MV		MV				
1	40	Add PC137	4/09		For PWR requirement.	1.0
2		change PR151, PR318, PR412, PR1106, PR1203, PRG4, PRG8, PRG10. PRG22, PRG23, PRG28, PRZ9, PRZ12, PRZ20, PRZ33, PRZ44 from 0 ohm to short pad	4/11		For PWR requirement.	1.0

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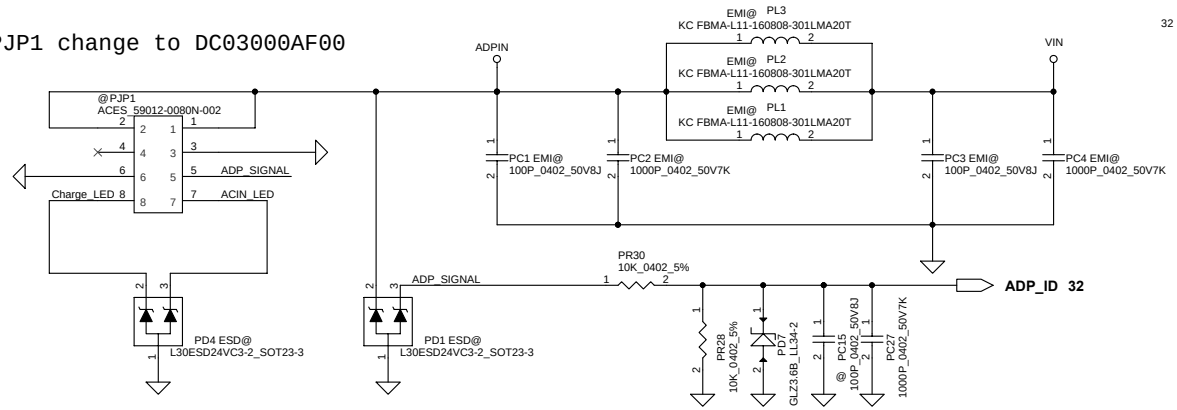
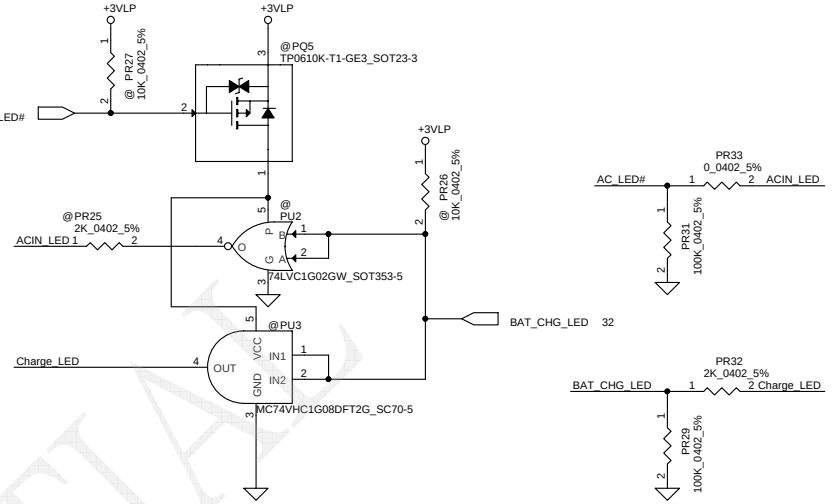
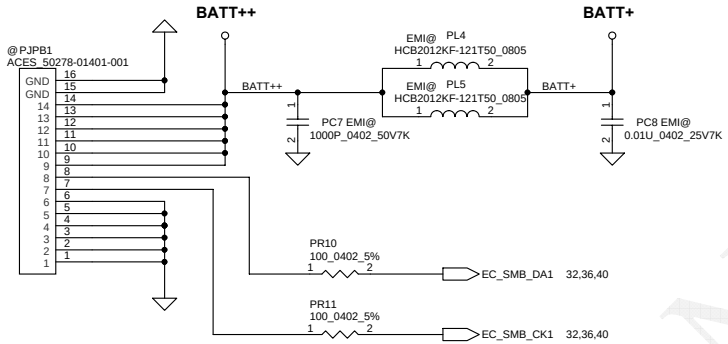
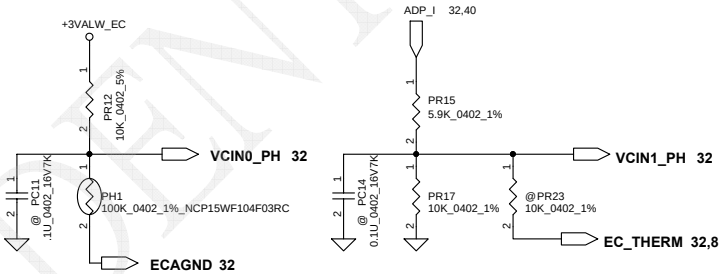
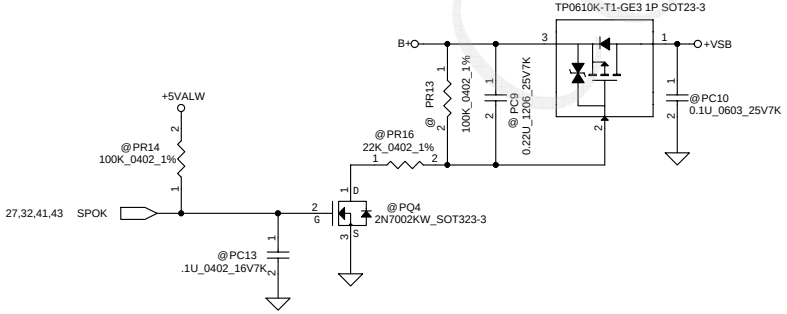
PJP1 change to DC03000AF00

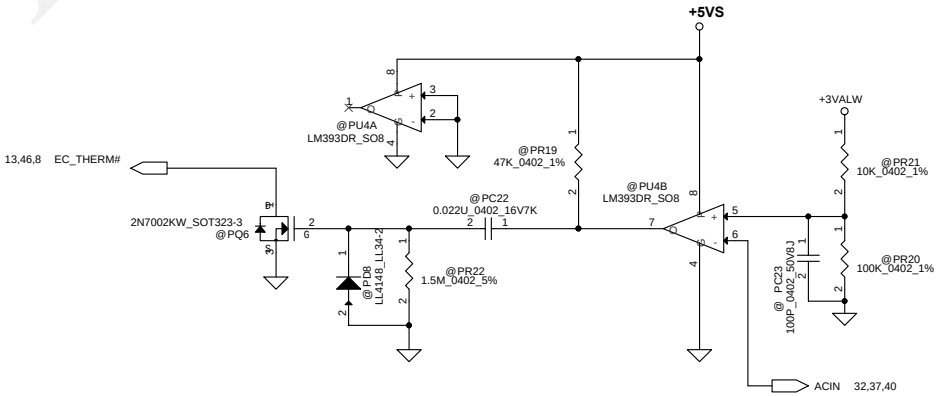












Security Classification	Compal Secret Data		
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Title: **SCHEMATIC, MB A9851**

Size	Document Number	Rev
Custom	4019NK	A

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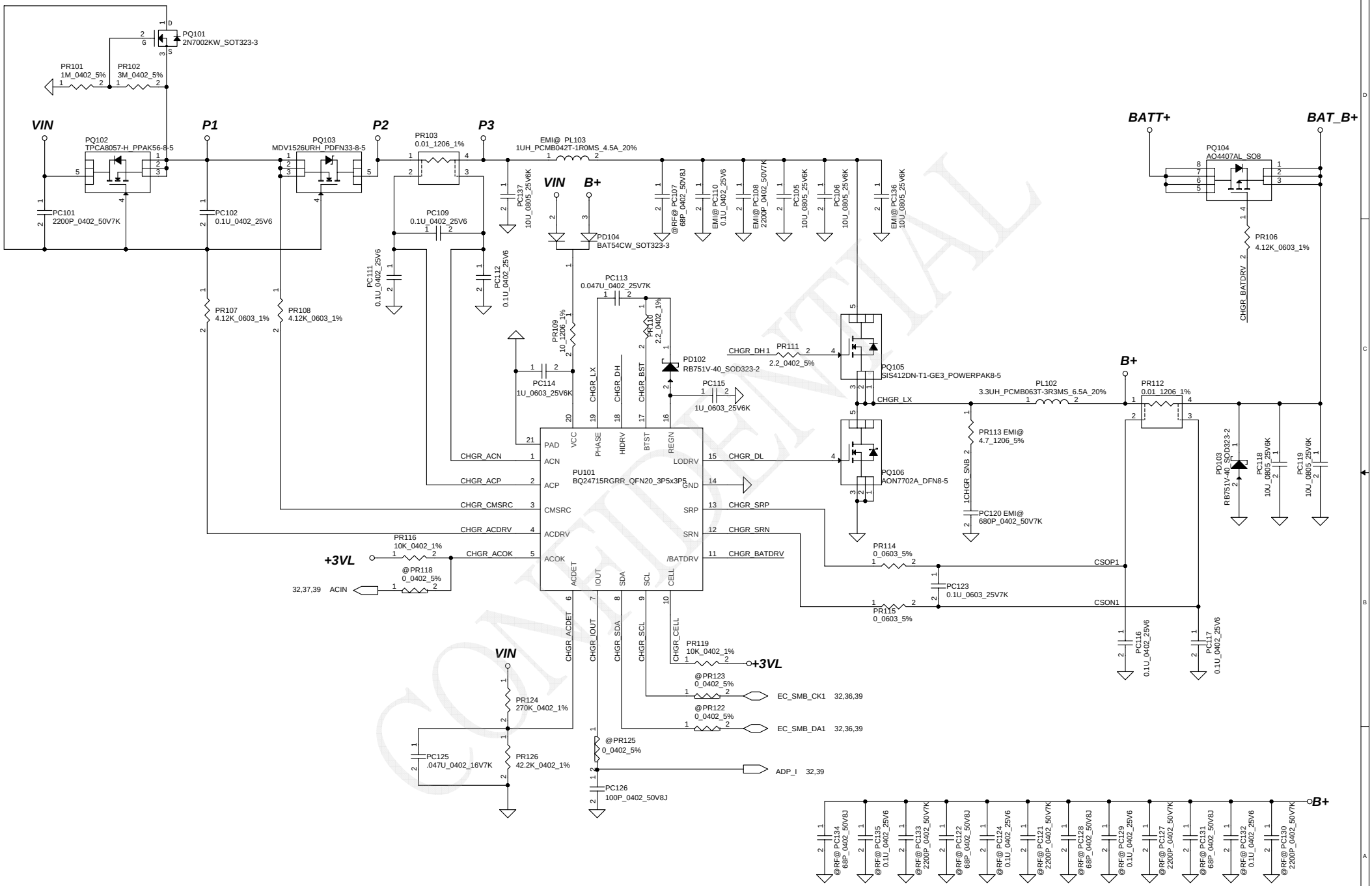

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

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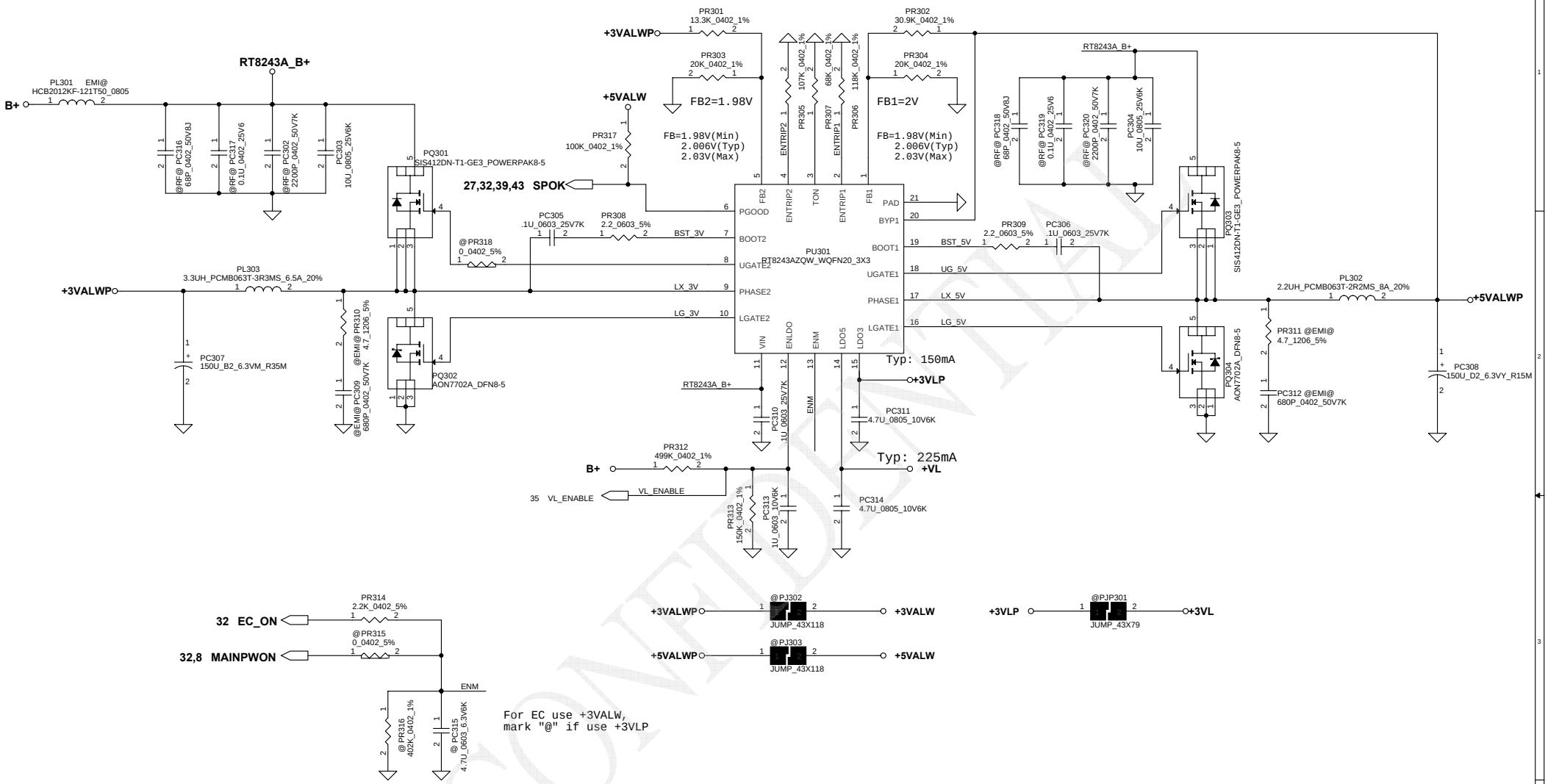

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

Compal Electronics, Inc.			
Title: SCHEMATIC, MB A9851			
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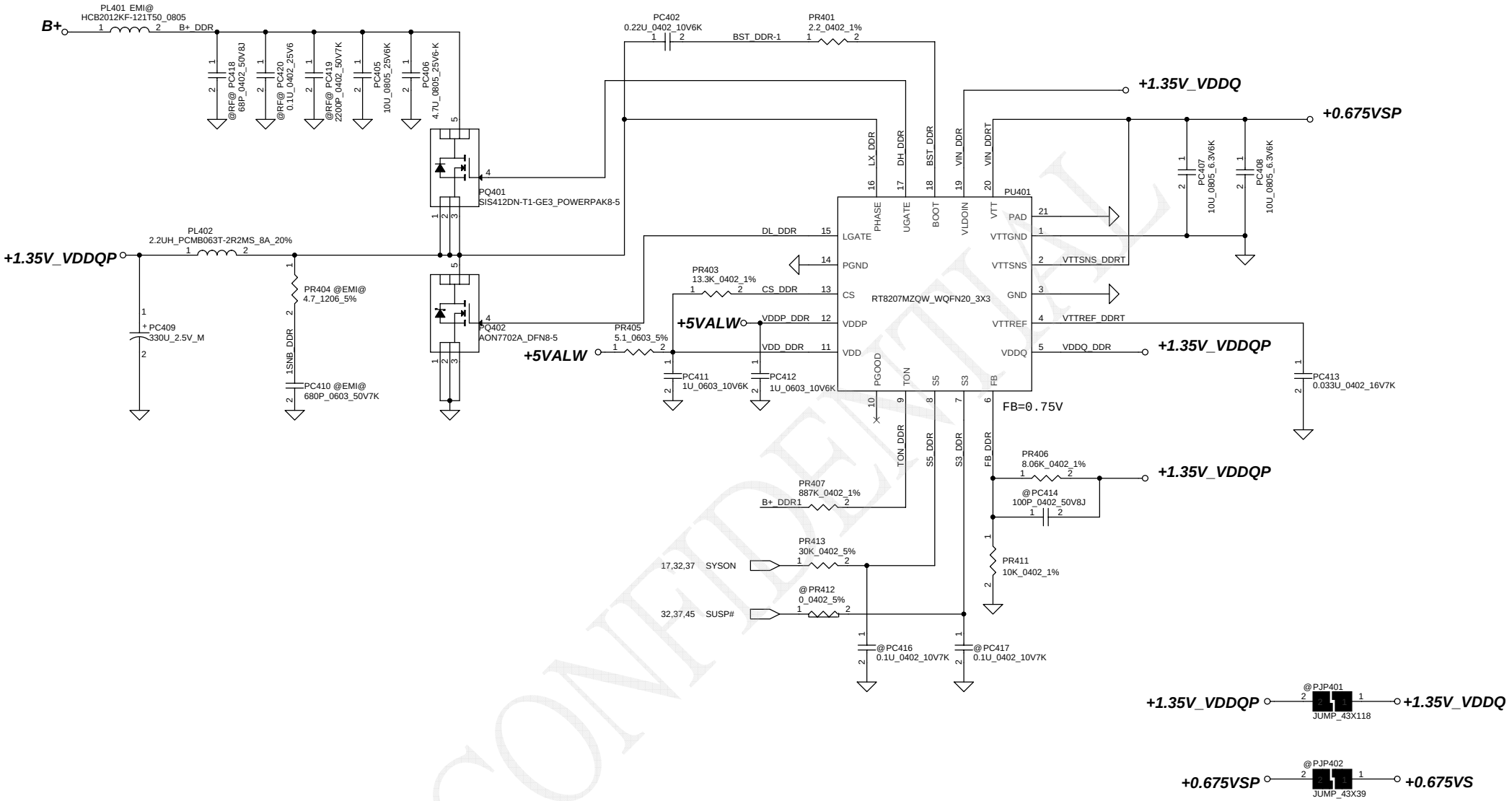

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

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Title: **SCHEMATIC, MB A9851**

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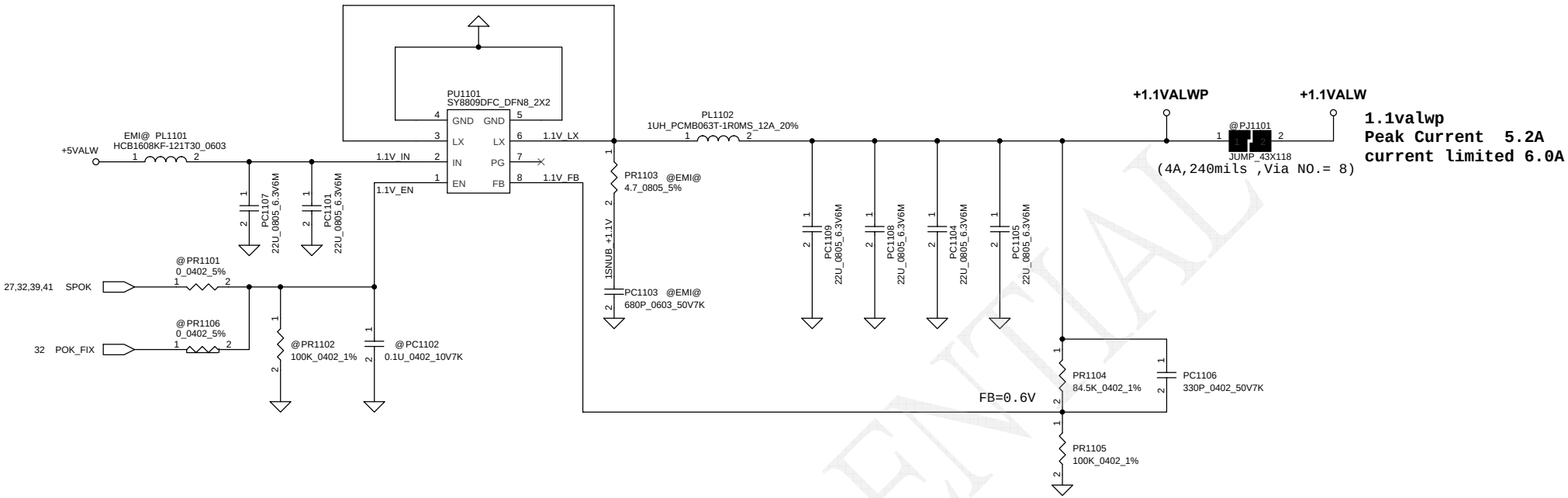

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Issued Date	2012/11/07	Deciphered Date	

Compal Electronics, Inc.

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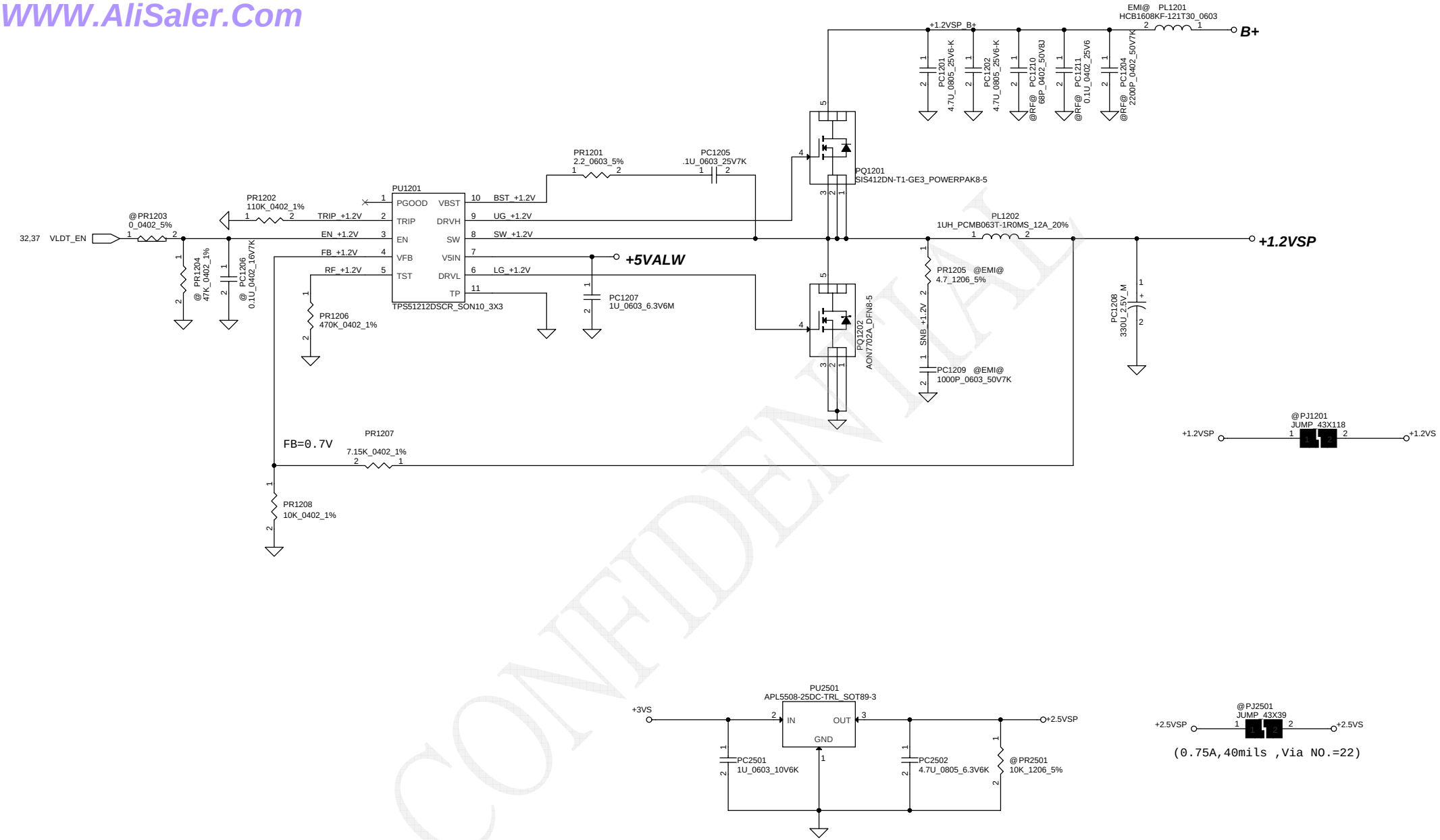

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	

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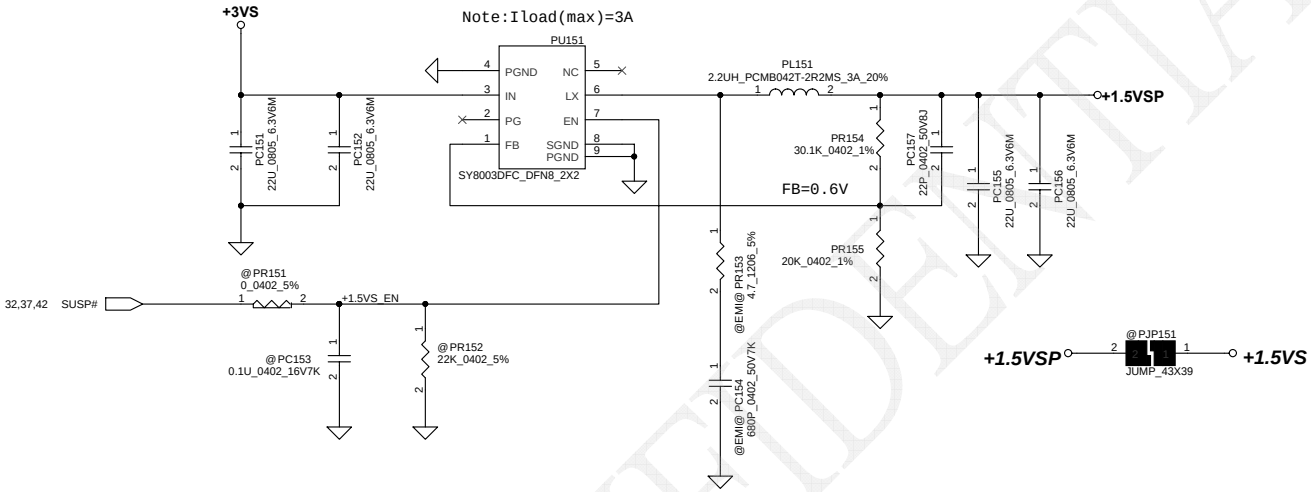

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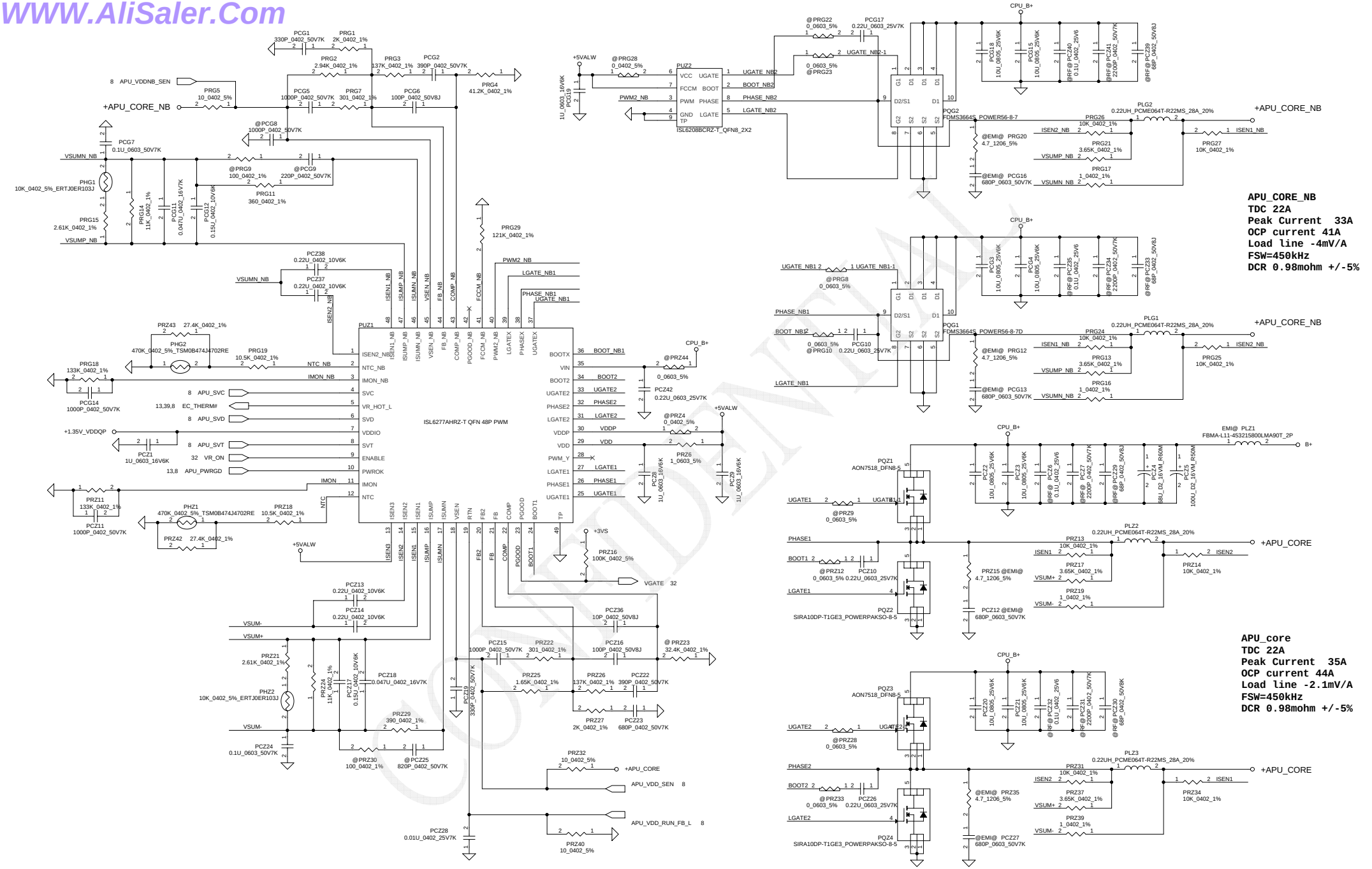

APU_CORE_NB
TDC 22A
Peak Current 33A
OCP current 41A
Load line -4mV/A
FSW=450kHz
DCR 0.98mohm +/-5%

APU_core
TDC 22A
Peak Current 35A
OCP current 44A
Load line -2.1mV/A
FSW=450kHz
DCR 0.98mohm +/-5%

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Title: SCHEMATIC, MB A9851			
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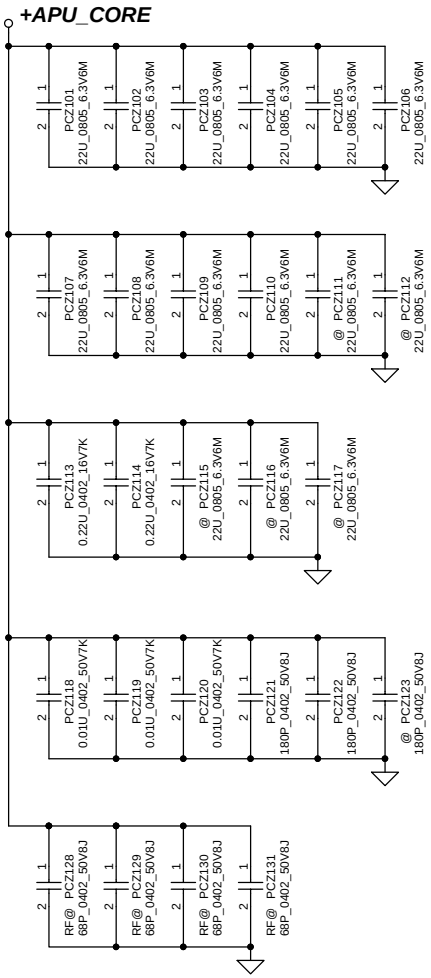
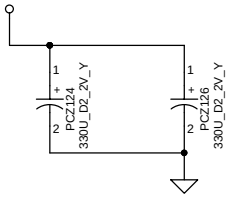
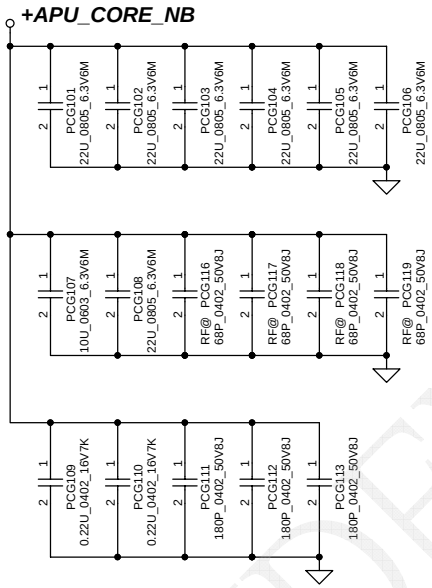
+APU_CORE



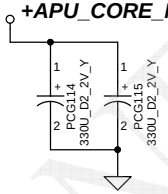
+APU_CORE Local



+APU_CORE_NB



+APU_CORE_NB Local



	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
APU_CORE	2	10	2		3	2
APU_CORE_NB	2	7	2	1		3

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