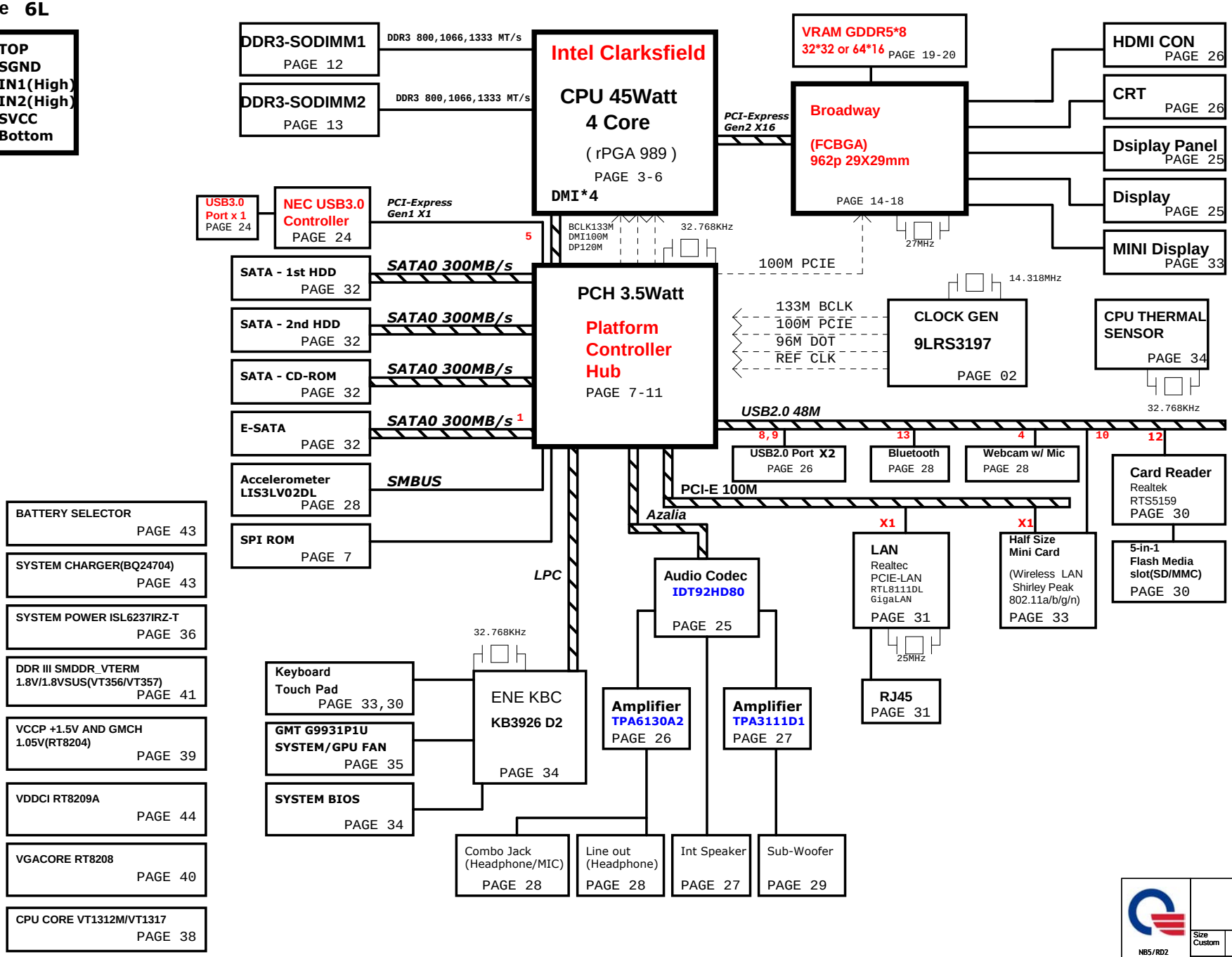
SP8 BLOCK DIAGRAM

01

PCB STACK UP

Discrete 6L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SVCC
LAYER 6 : Bottom



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3A

Date: Thursday, August 05, 2010 Sheet 1 of 47

NB5/RD2

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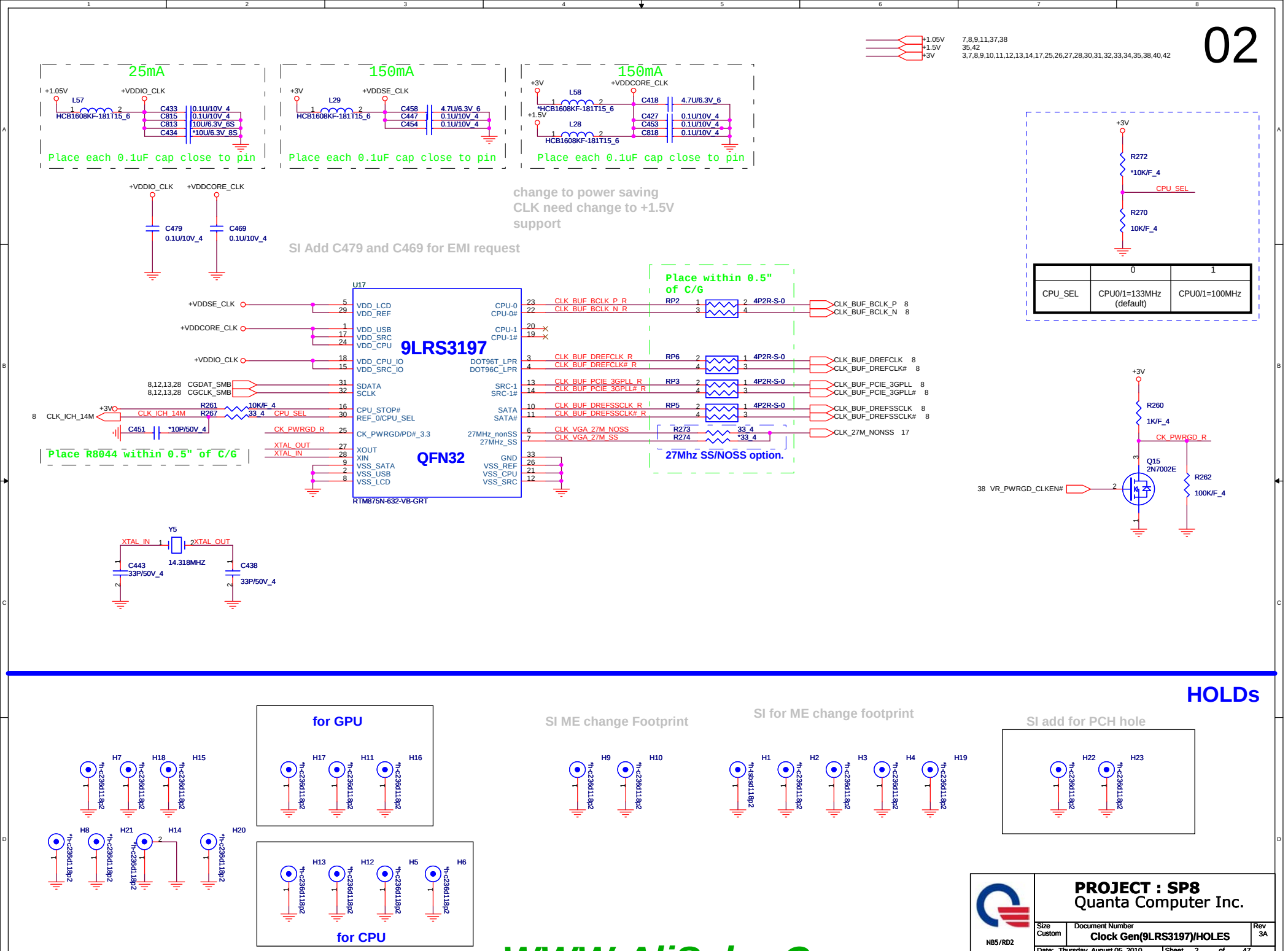

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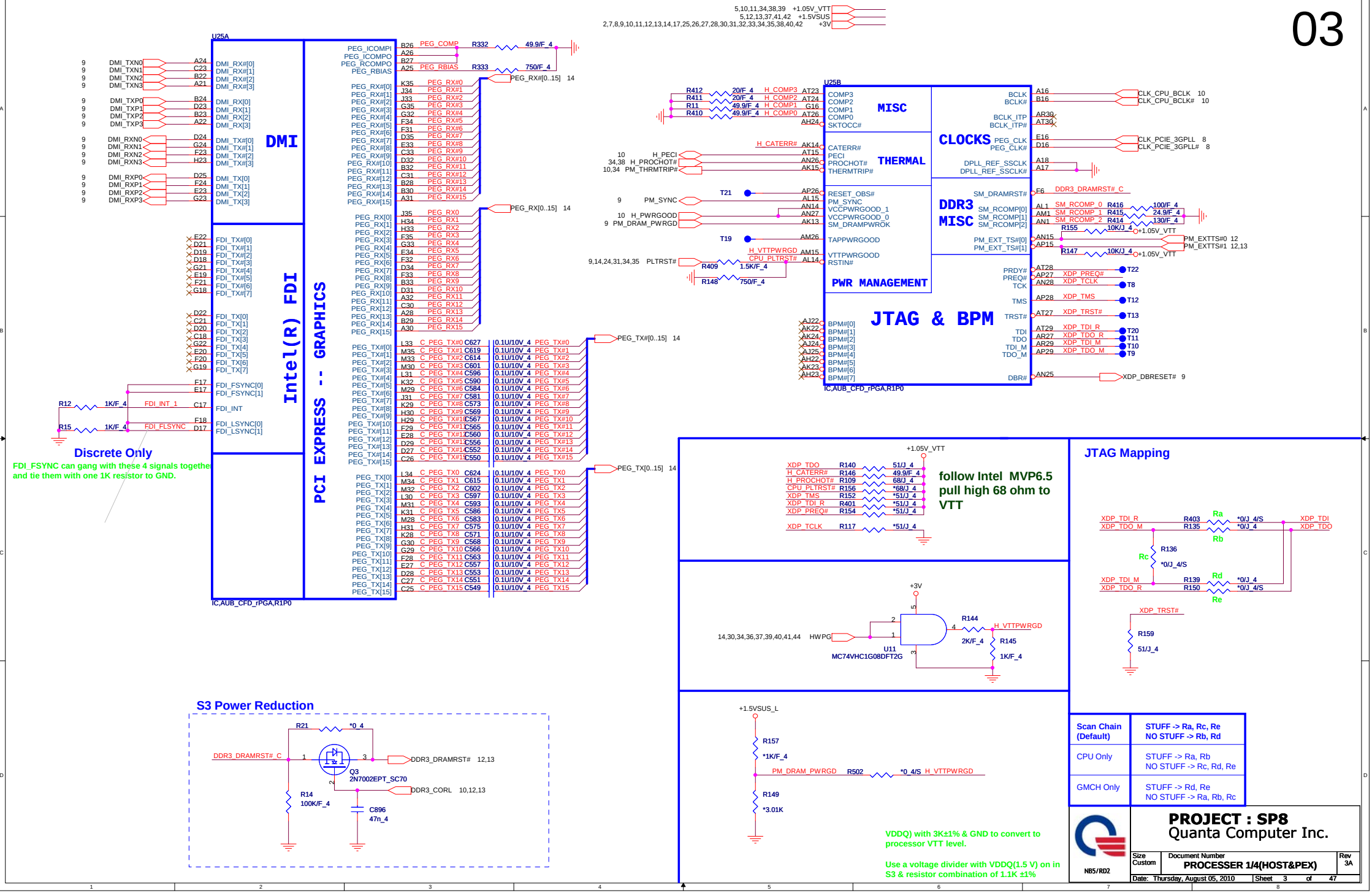

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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	3A

NB5/RD2

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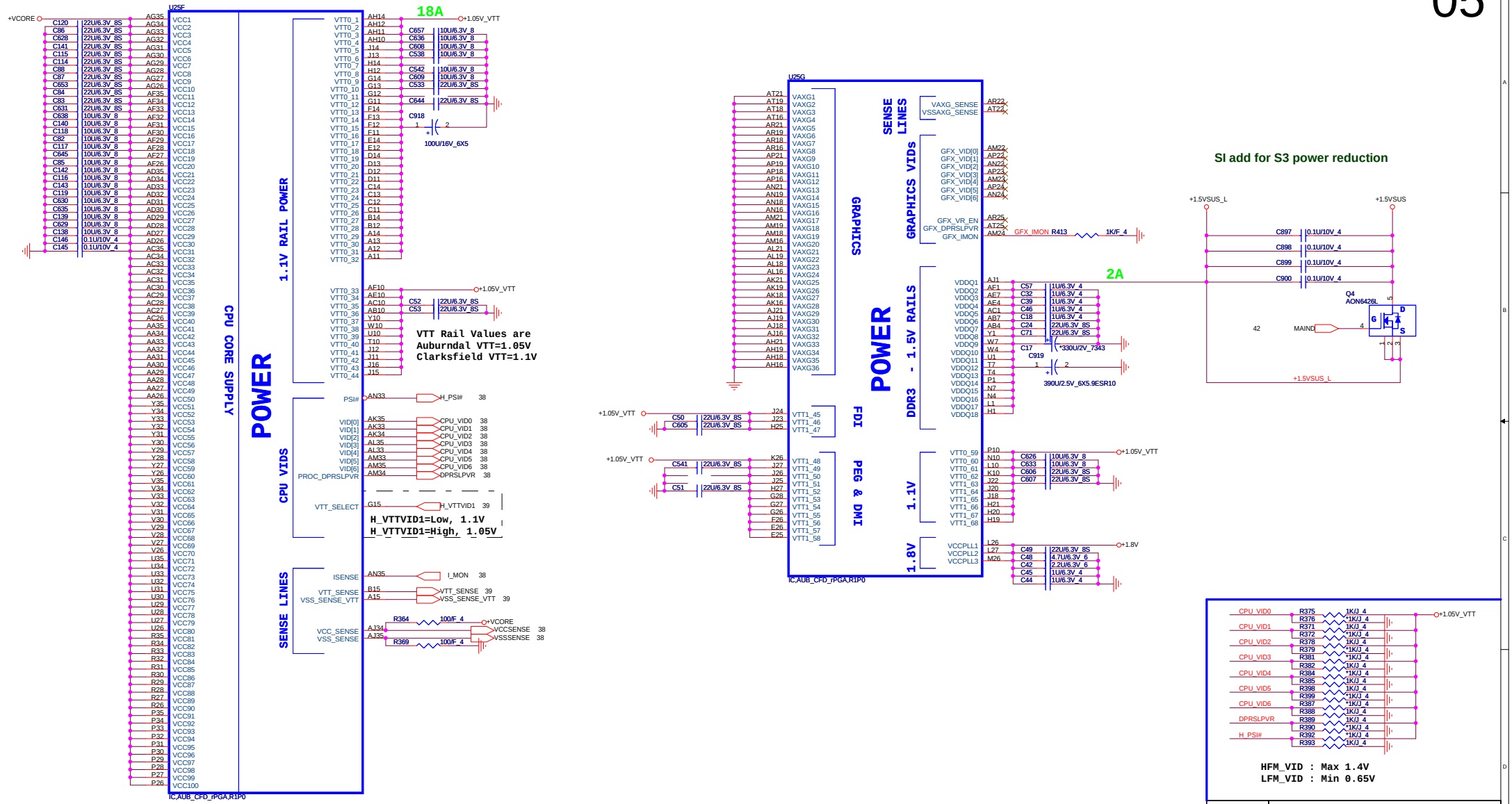

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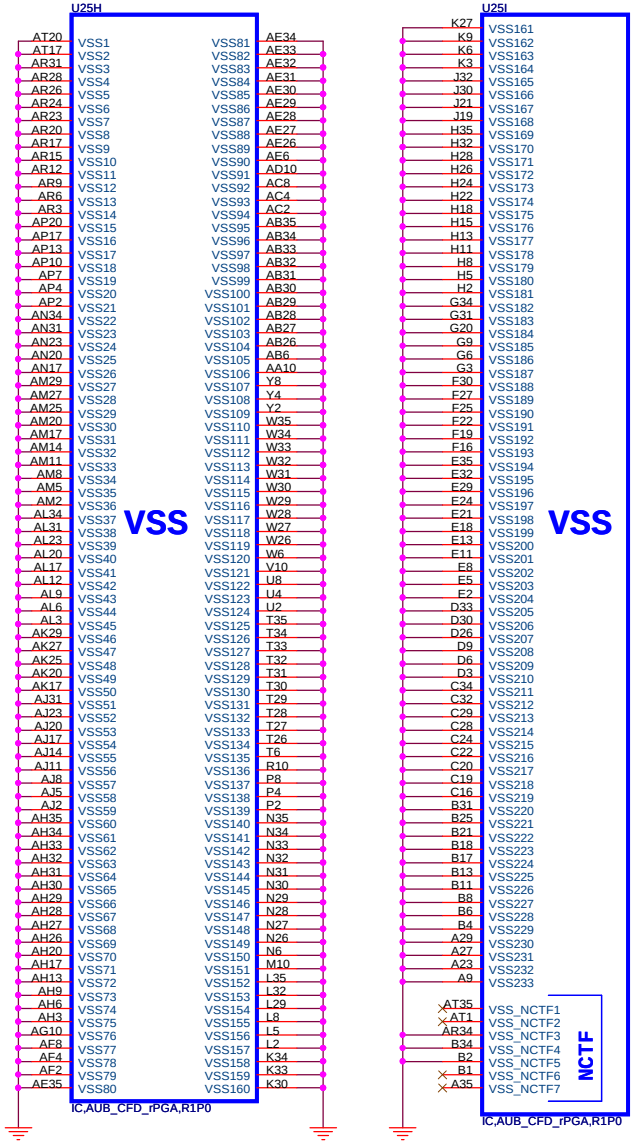
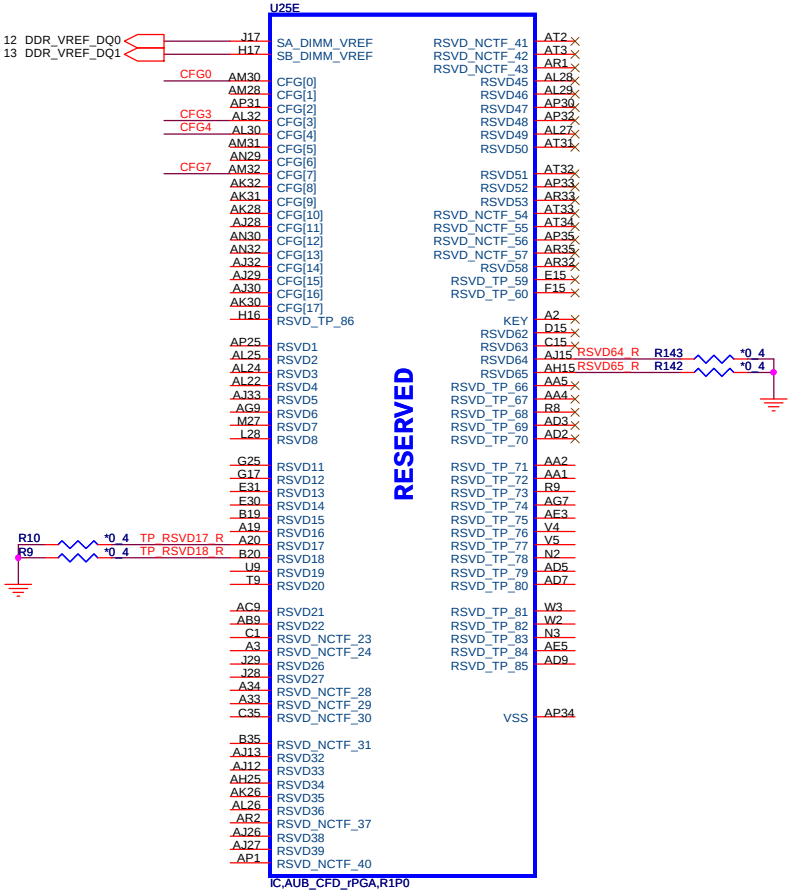
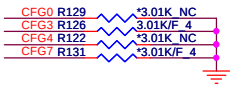
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For Discrete only



CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4 (GND)	3A

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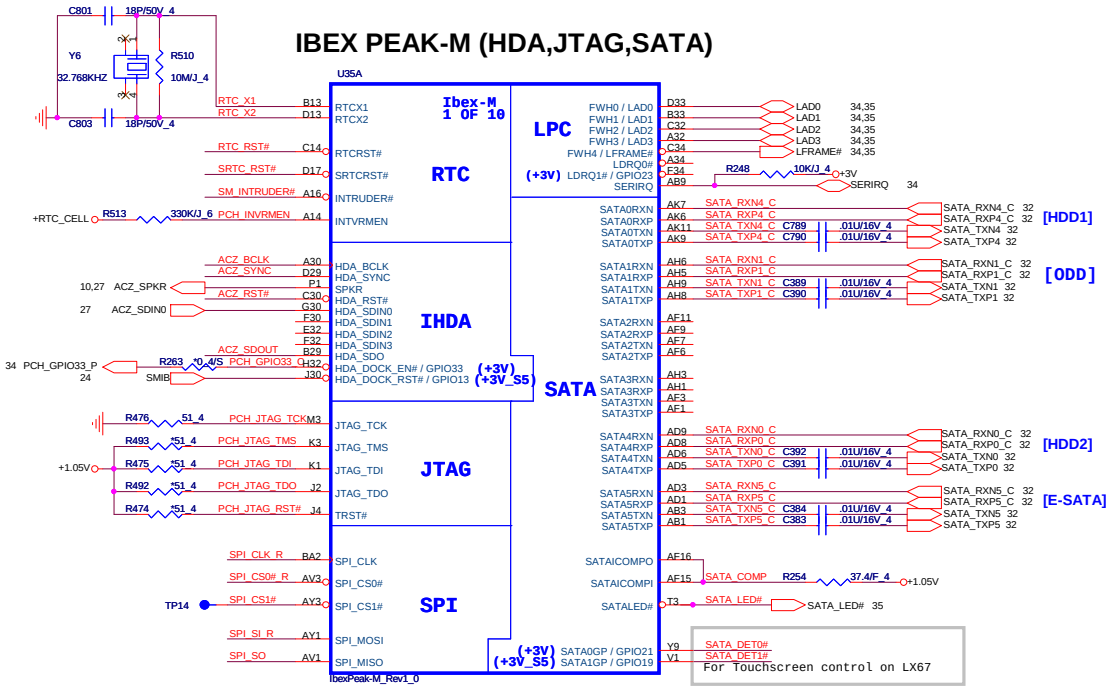
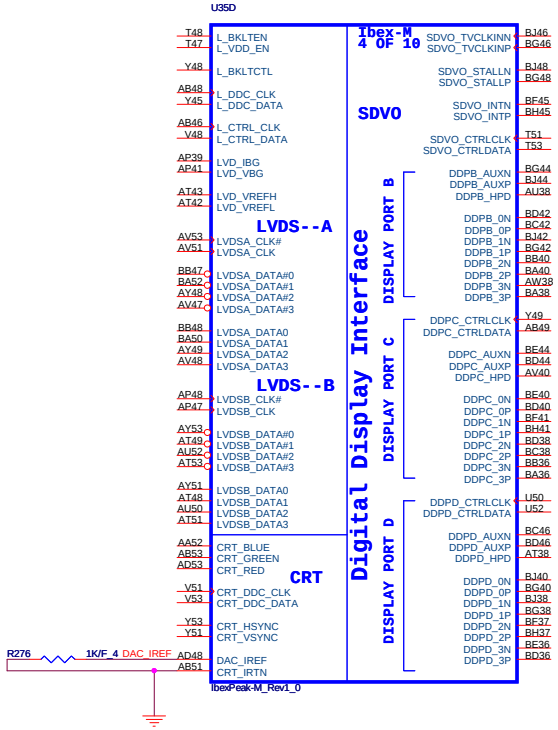
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

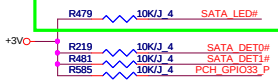
IBEX PEAK-M (HDA,JTAG,SATA)



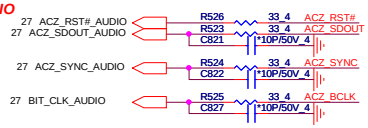
IBEX PEAK-M (LVDS,DDI)



The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3

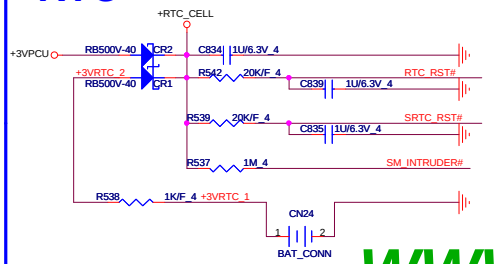


For AUDIO

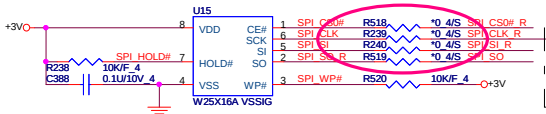


RTC

1mA



4M byte SPI ROM



Socket DG008000031
MXIC AKE39FP0Z00
WINBOND AKE391P0N00

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PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	3A

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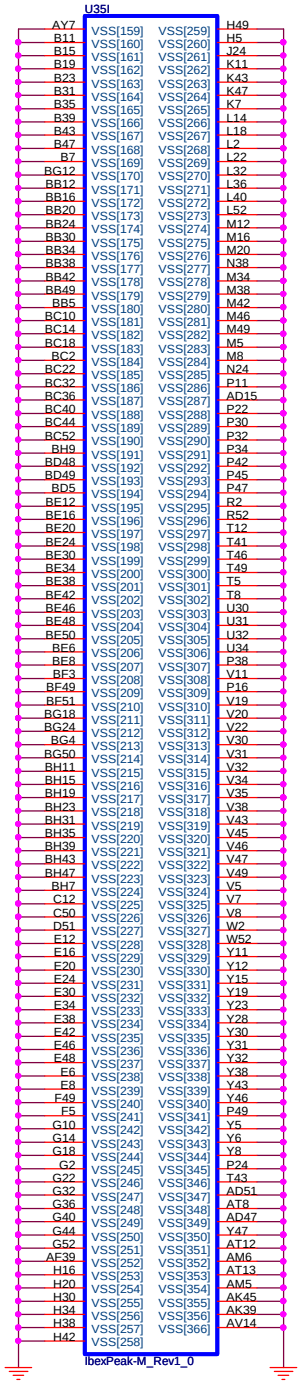
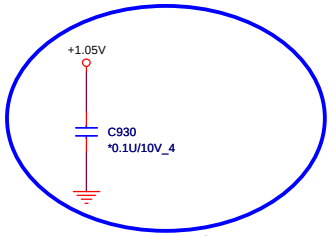
NB5/RD2

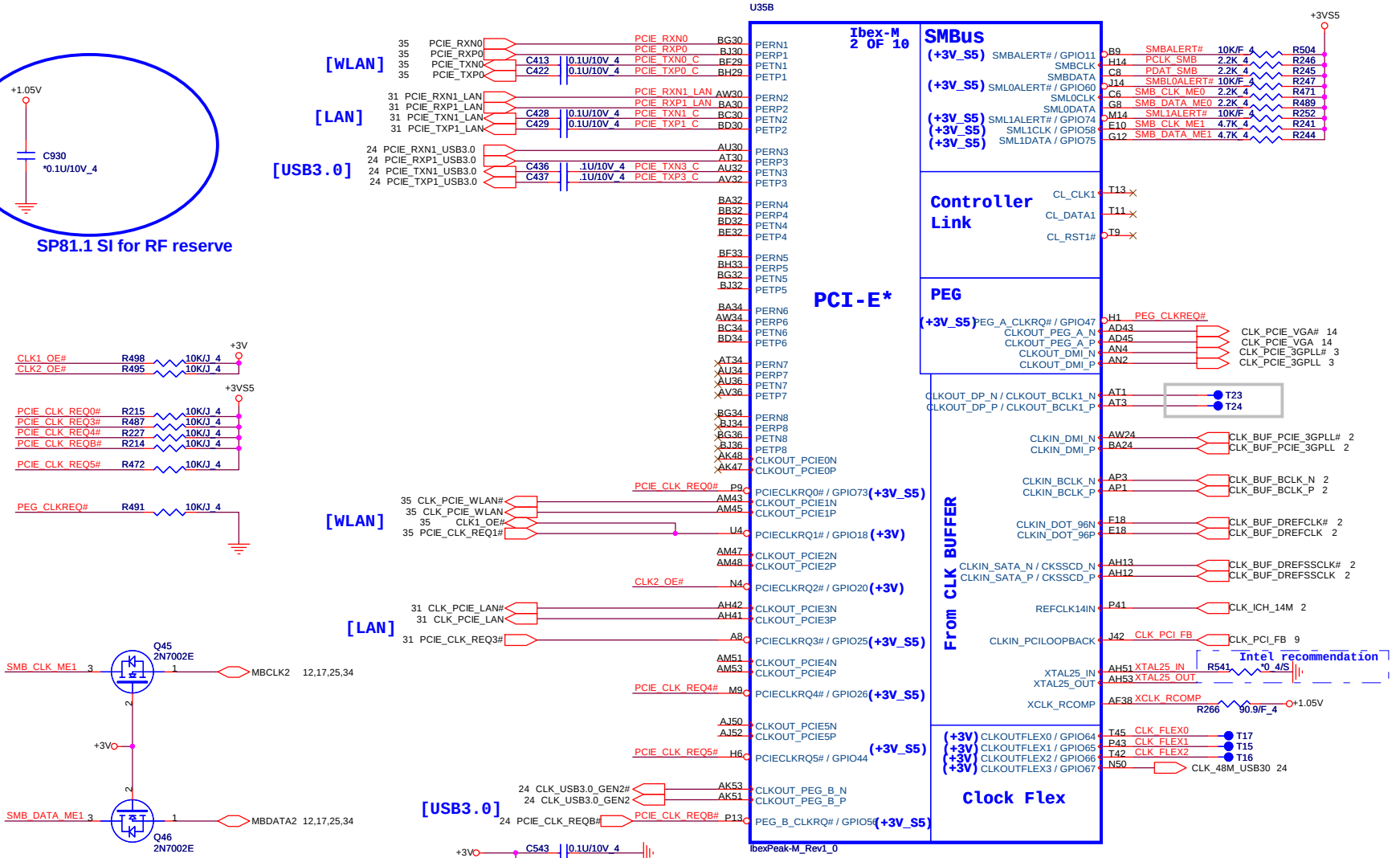
IBEX PEAK-M (GND)





SP81.1 SI for RF reserve

IBEX PEAK-M (PCI-E,SMBUS,CLK)



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS, CK)	3A

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NB5/RD2

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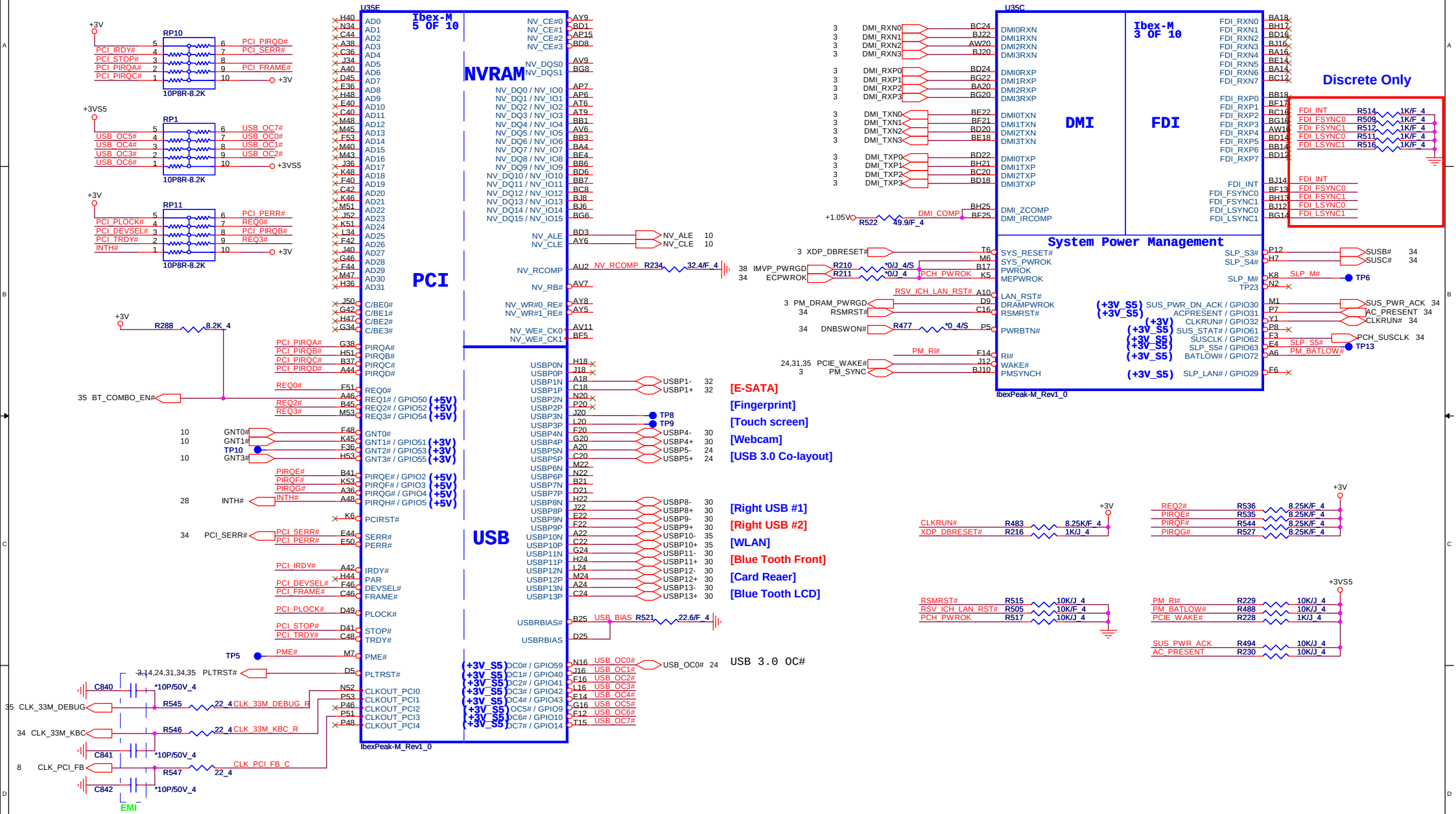
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/5 (PCI,ONFI,USB,DMI)	3A

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NB5/RD2

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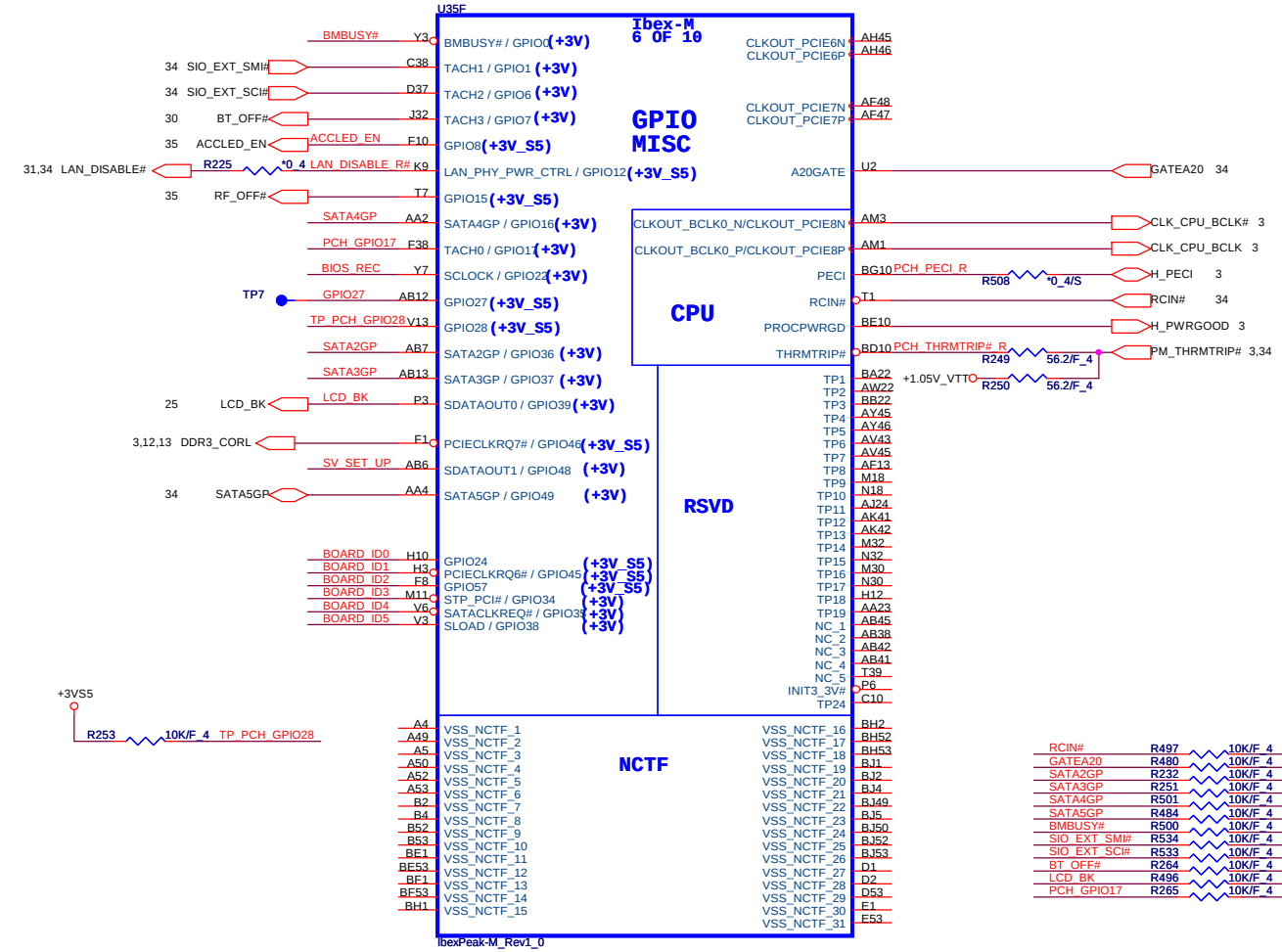
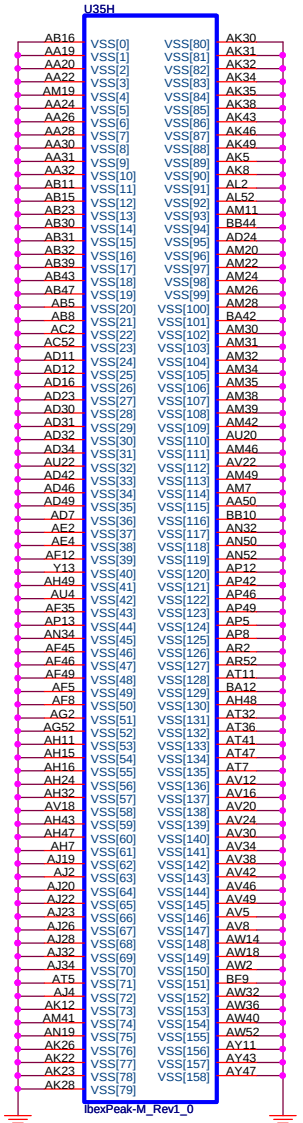
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



9 GNT3# R543 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R218 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

9 GNT0# R269 *1K/F_4
9 GNT1# R268 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

9 NV_ALE R506 *1K/F_4 +1.8V
9 NV_CLE R507 *1K/F_4

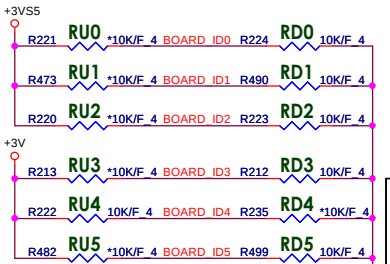
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

BOARD ID SETTING

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0 GPIO 24	ID1 GPIO 45	ID2 GPIO 57	ID3 GPIO 34	ID4 GPIO 35	ID5 GPIO 38
SP8	0	0			0	0
SP8 1.1	0	0			1	0
Discrete			0	0		
Reserve			0	0		
ROM Size				0= 4M 1= 2M		



No Reboot Strap

7,27 ACZ_SPKR R478 *1K/F_4 +3V

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	3A

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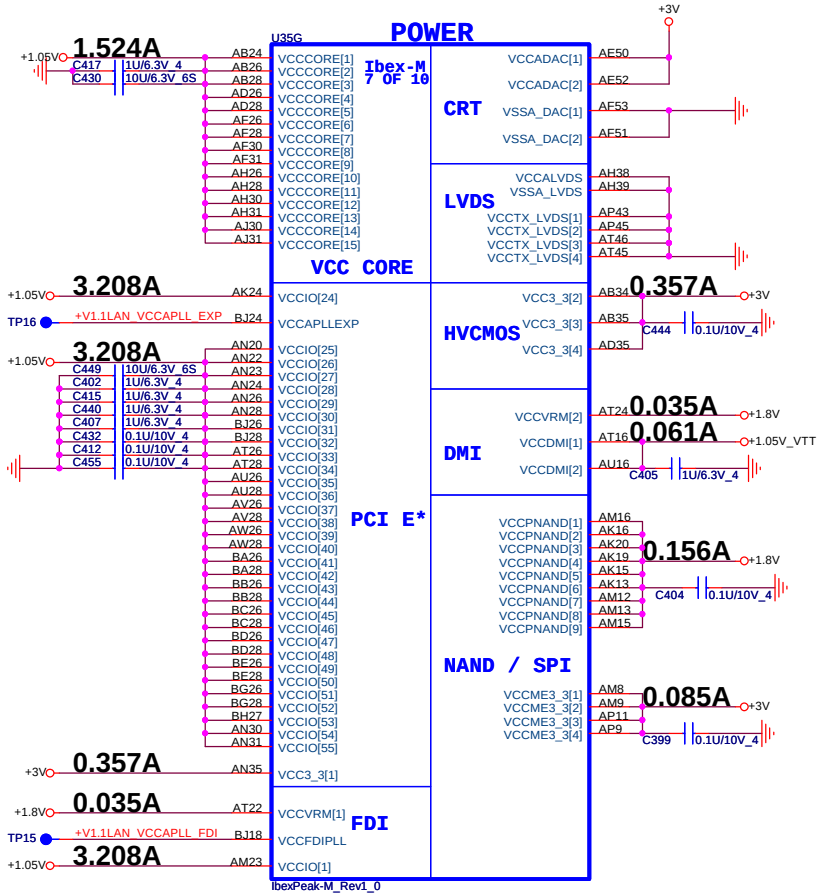

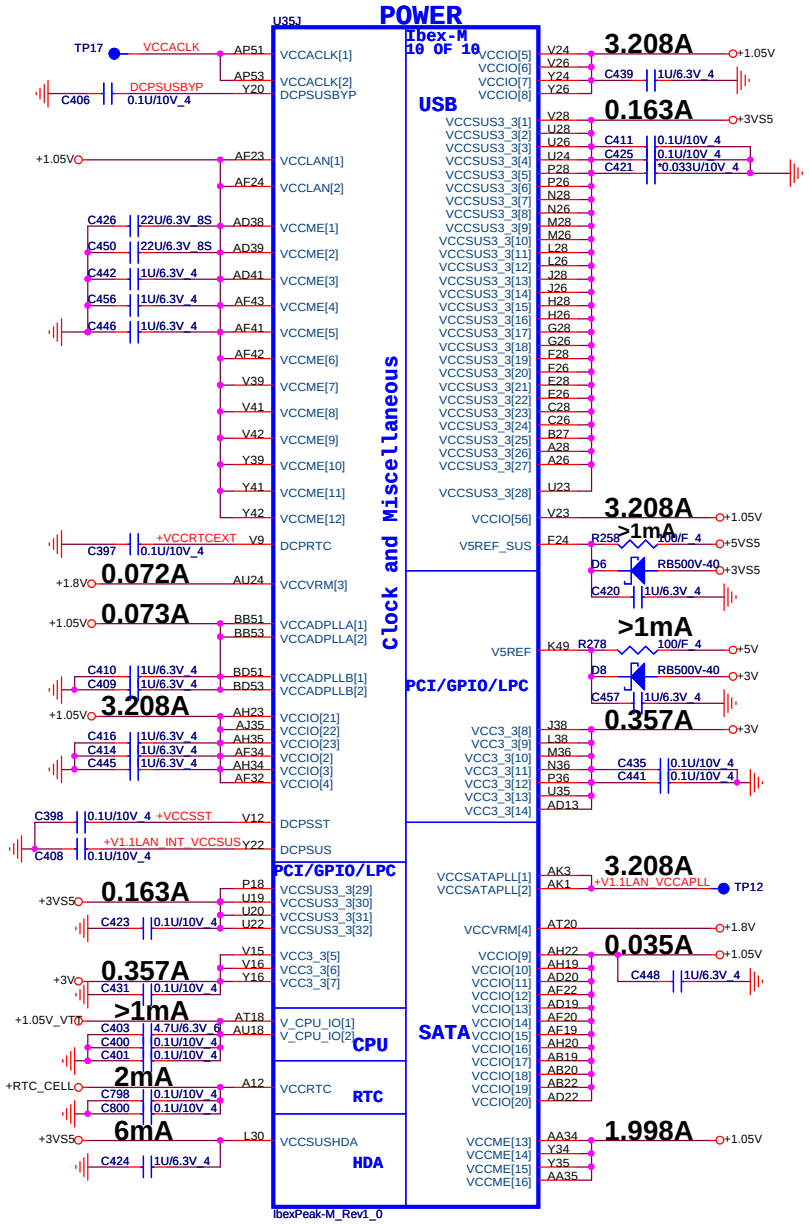

2,7,8,9,37,38 +1.05V
3,5,10,34,38,39 +1.05V_VTT
5,10,37,42 +1.8V
2,3,7,8,9,10,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
8,9,10,42 +3VS5
25,26,27,29,30,31,32,33,35,42 +5V
42 +5VS5

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	3A

Date: Thursday, August 05, 2010 Sheet 11 of 47

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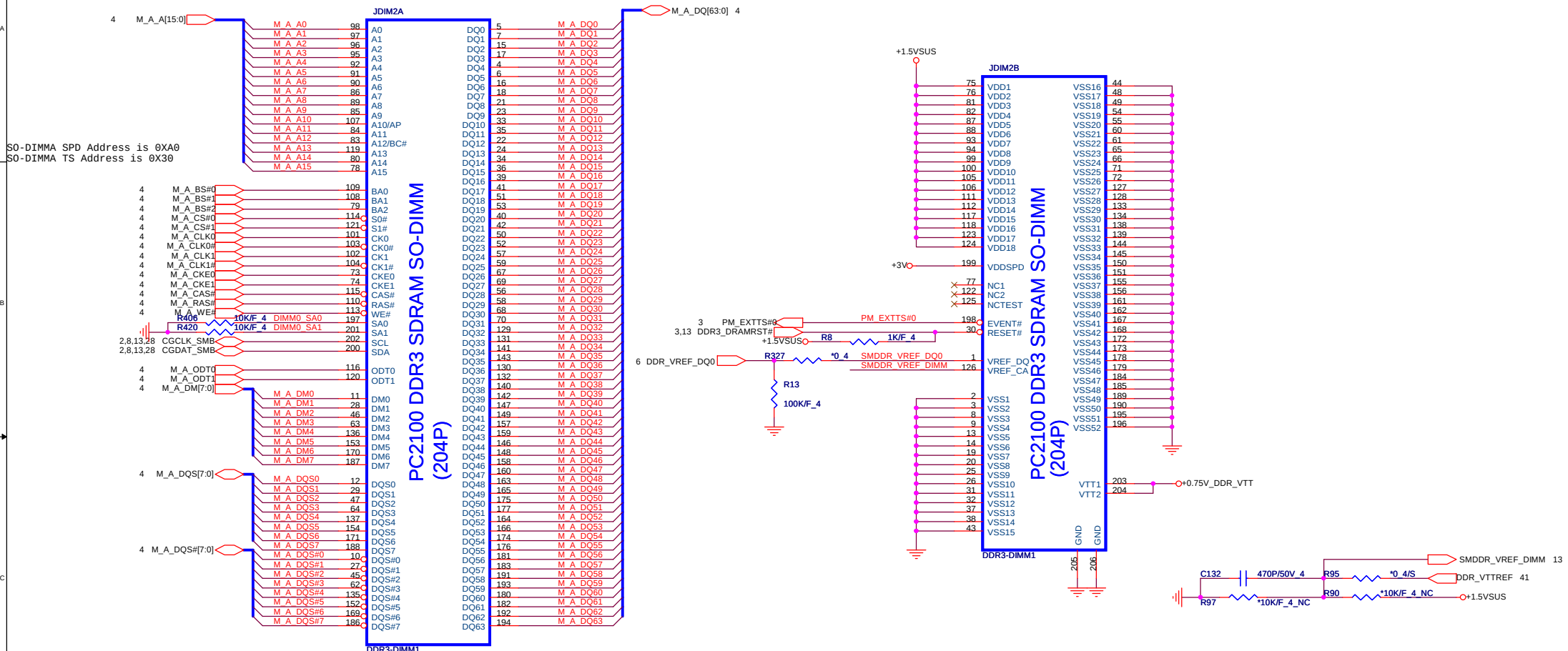
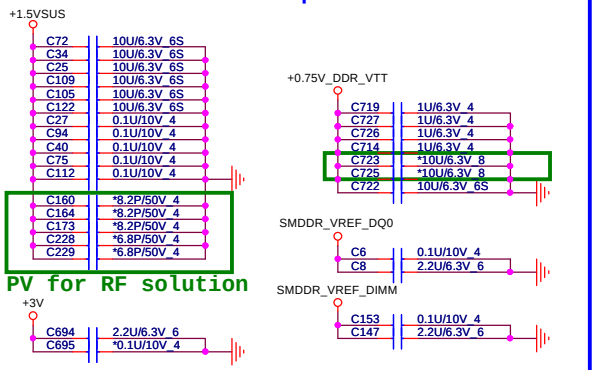
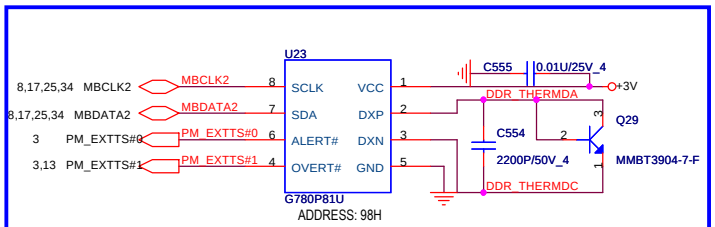
13,41 +0.75V_DDR_VTT
5,13,37,41,42 +1.5VSUS
2,3,7,8,9,10,11,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
7,25,30,33,34,35,36,37,39,40,42,43 +3VPCU
24,30,32,34,36,37,38,39,40,41,42,43,44 +5VPCU

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30



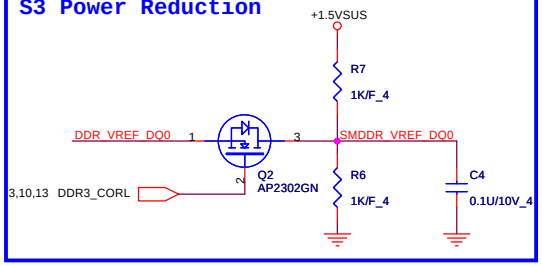
Place these Caps near So-Dimm0.





Place these U8008 near So-Dimm0(JDIM8000)

S3 Power Reduction



NB5/RD2	**PROJECT : SP8** Quanta Computer Inc.	
Size Custom	Document Number DDR3 DIMM-0	Rev 3A
Date: Thursday, August 05, 2010	Sheet 12 of 47	

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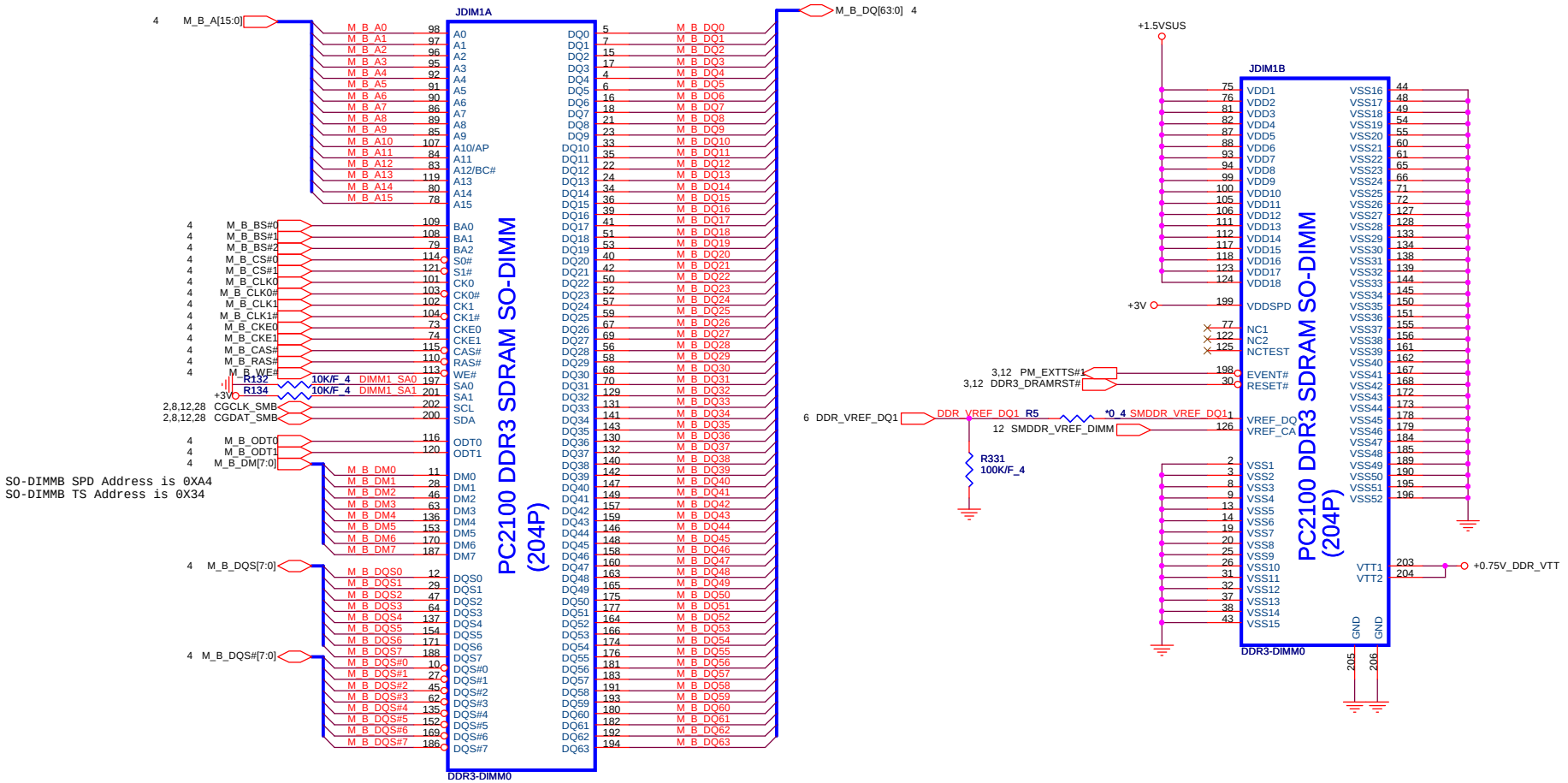
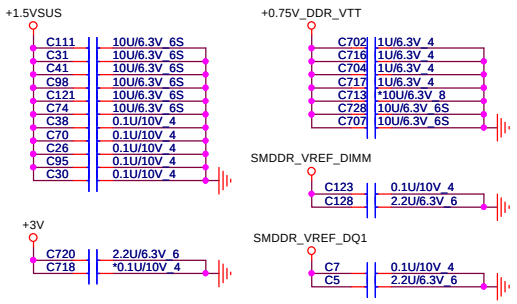
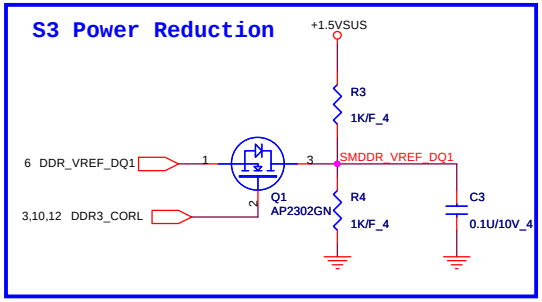
12,41 +0.75V_DDR_VTT
5,12,37,41,42 +1.5VSUS
2,3,7,8,9,10,11,12,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
7,25,30,33,34,35,36,37,39,40,42,43 +3VPCU
24,30,32,34,36,37,38,39,40,41,42,43,44 +5VPCU



Place these Caps near So-Dimm1



S3 Power Reduction



NB5/RD2	**PROJECT : SP8** Quanta Computer Inc.	
Size Custom	Document Number DDR3 DIMM-1	Rev 3A
Date: Thursday, August 05, 2010	Sheet 13 of 47	

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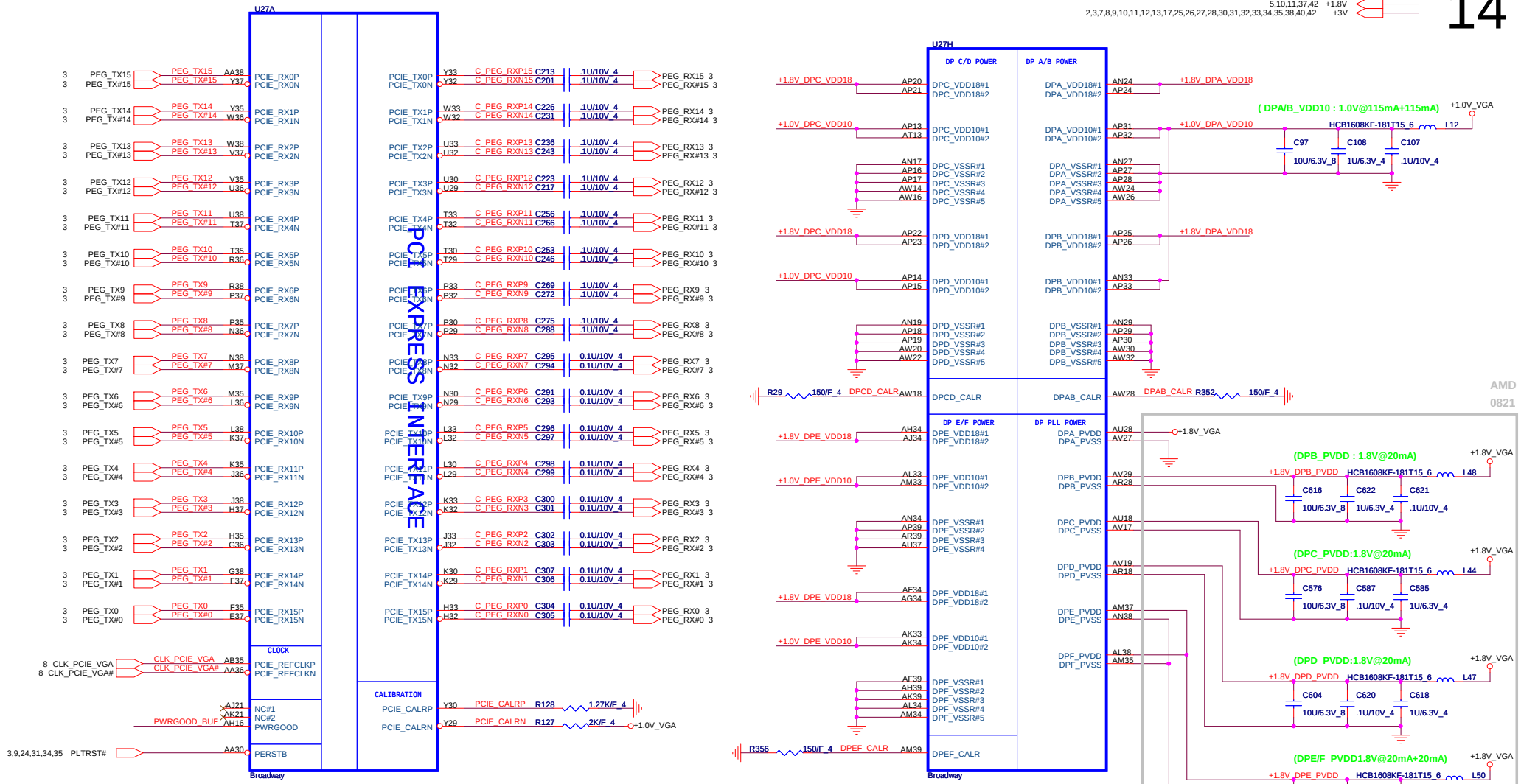
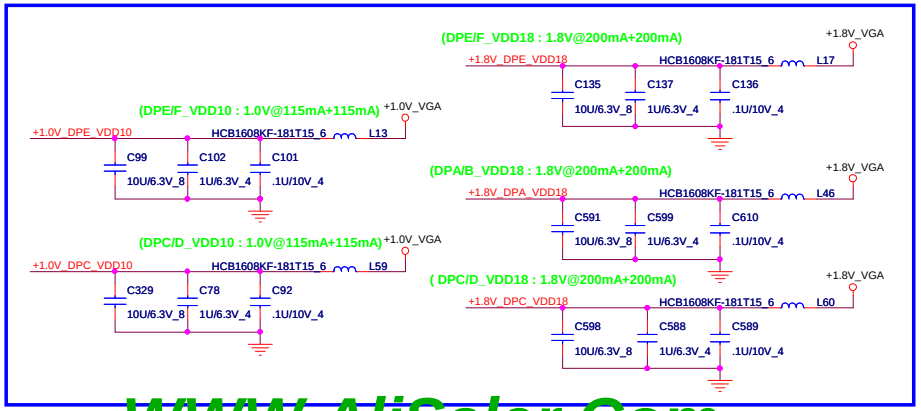
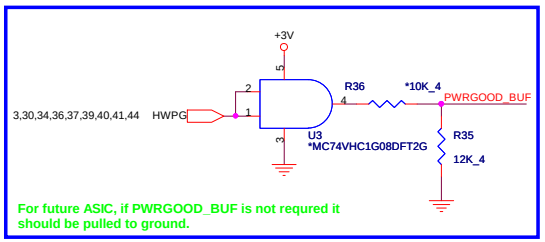
16,18,41 +1.0V_VGA
5,10,11,37,42 +1.8V
2,3,7,8,9,10,11,12,13,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V







PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97-M2 (PCIE I/F) 1/5	3A

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N85/RD2

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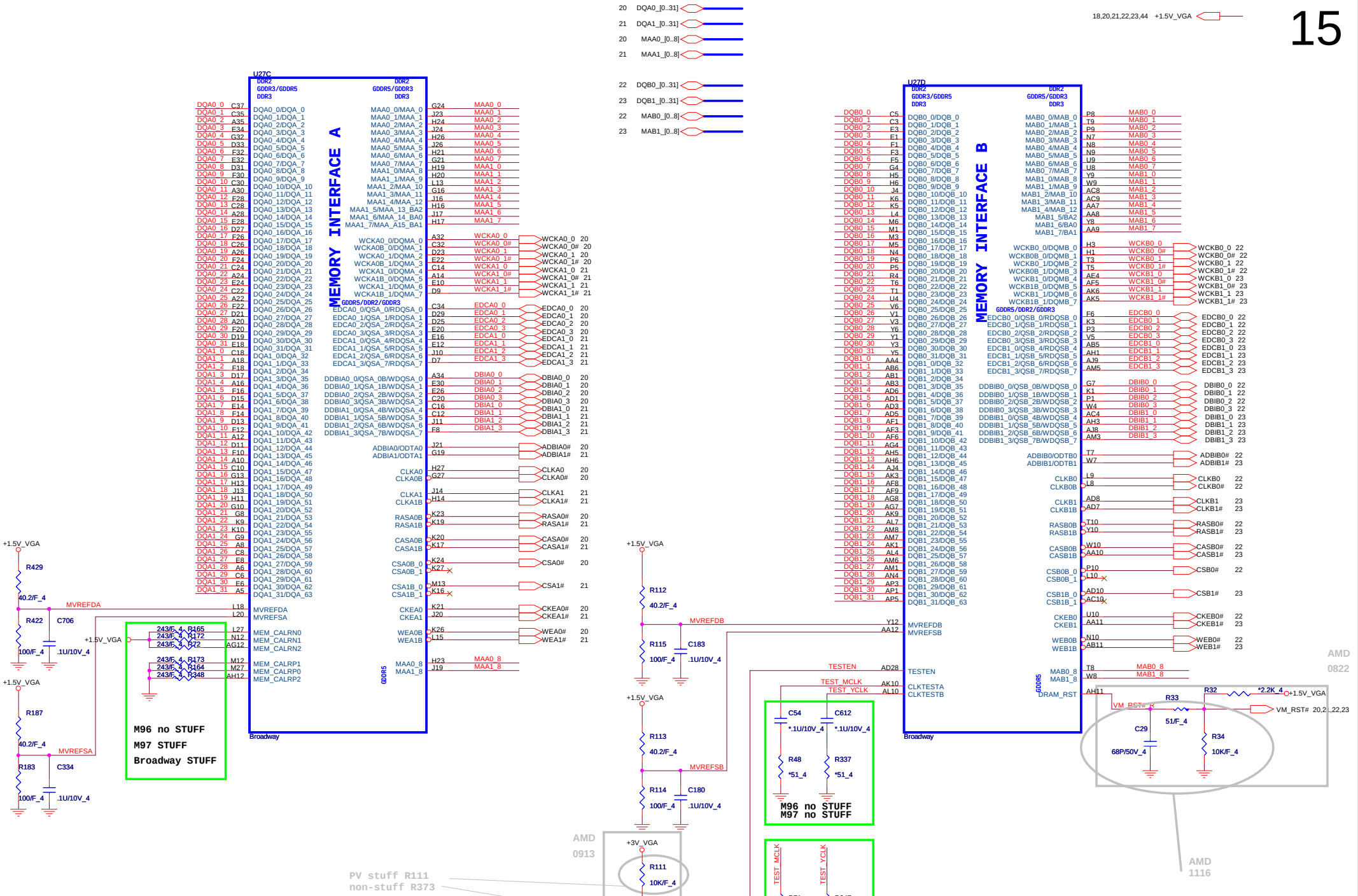

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97-M2 (MEM I/F) 2/5	3A

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N85/RD2

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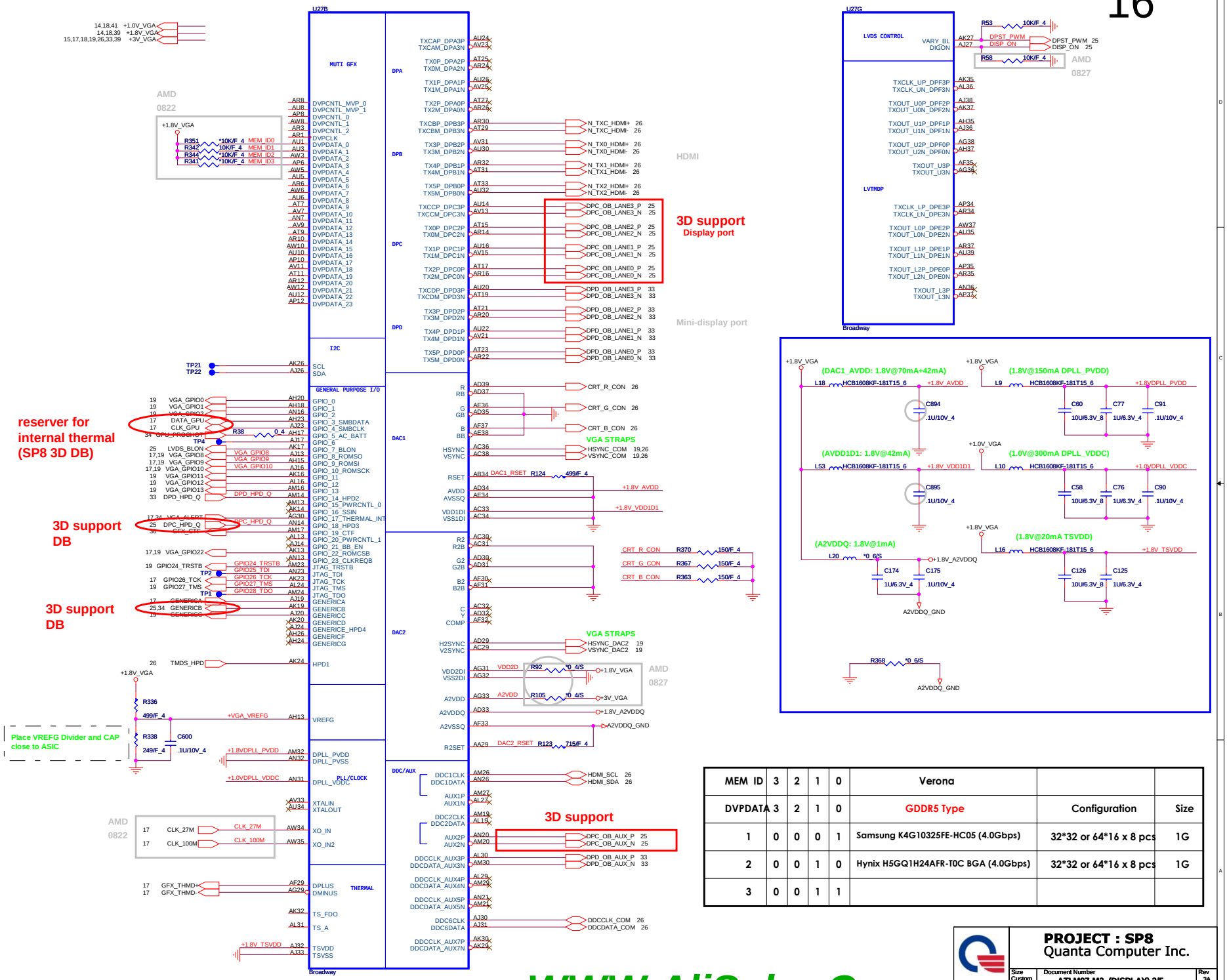

MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	GDDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1			

PROJECT : SP8
Quanta Computer Inc.

Size: Custom | Document Number: ATI M97-M2 (DISPLAY) 3/5 | Rev: 3A

Date: Thursday, August 05, 2010 | Sheet 16 of 47

N85/RD2

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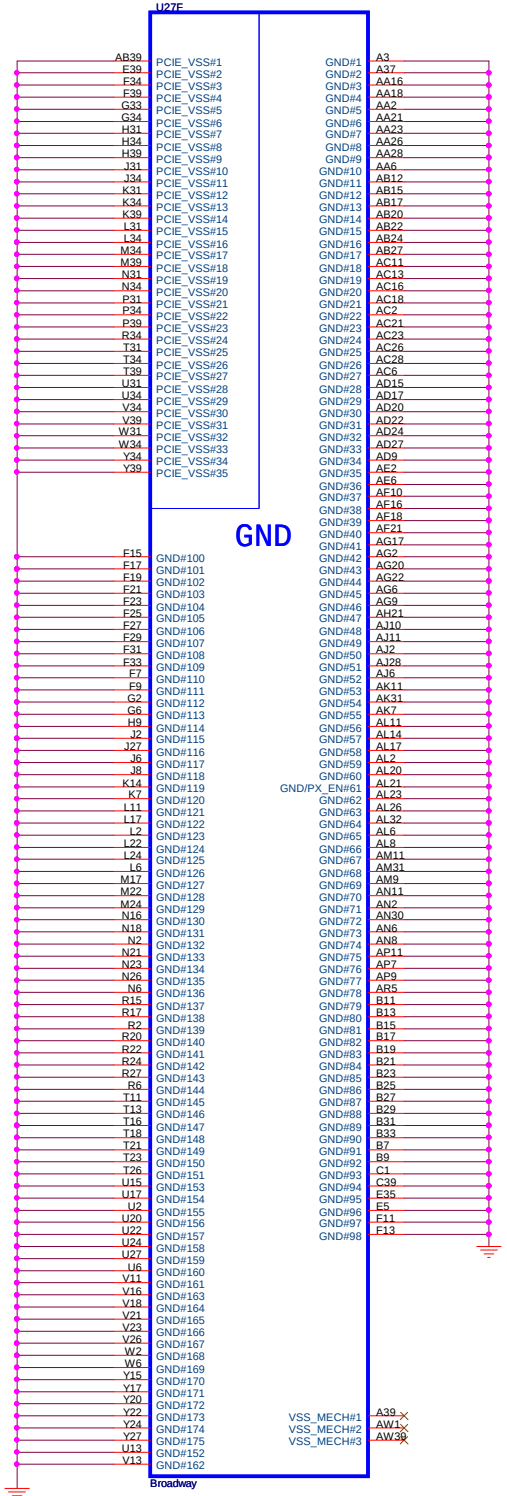
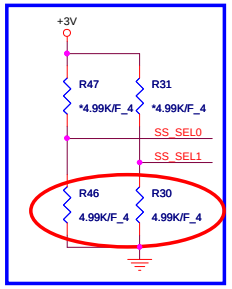
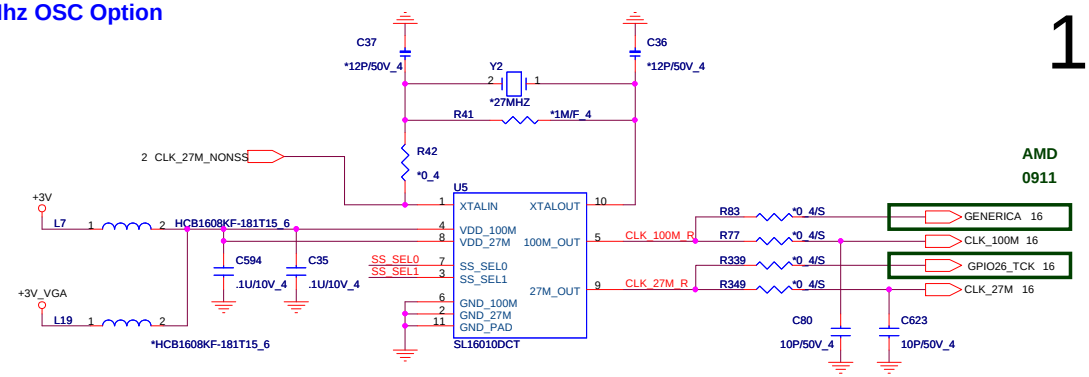


27MHz + 100Mhz OSC Option



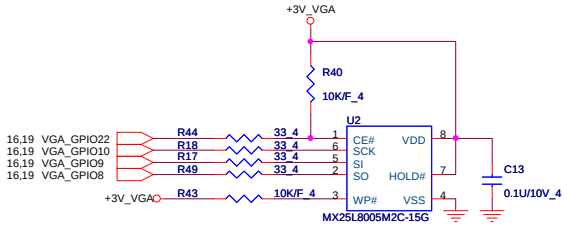
SP8 1.1 DB



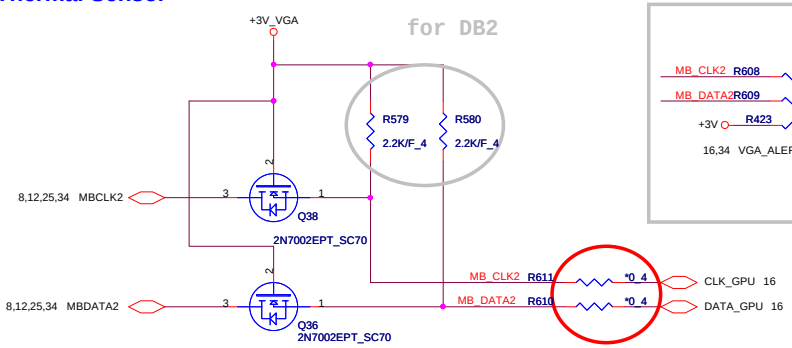
AMD
0911

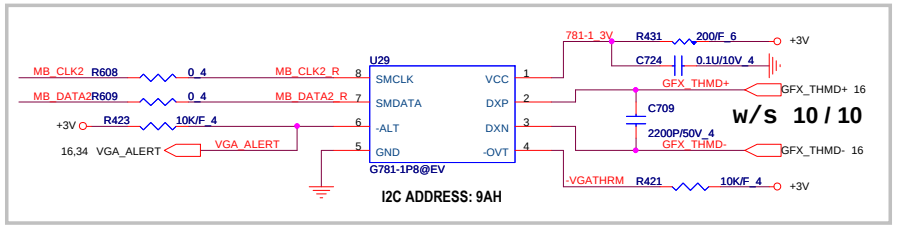
SS_SEL1	SS_SEL0	Spread Percent(%) SS_CLK (PIN 5)
LOW	LOW	Spread Off
LOW	Middle	-0.5%
LOW	High	-2.5%
Middle	LOW	-0.25%
Middle	Middle	-0.75%
Middle	High	-1.0%
High	LOW	-1.5%
High	Middle	-2.0%
High	High	-3.0%

Ext EEPROM



Thermal Sensor





reserver for
internal thermal
SP8 1.1 DB

2,3,7,8,9,10,11,12,13,14,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V

15,16,18,19,26,33,39 +3V_VGA

N85/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97(GND&Str&Ther)4/5	3A

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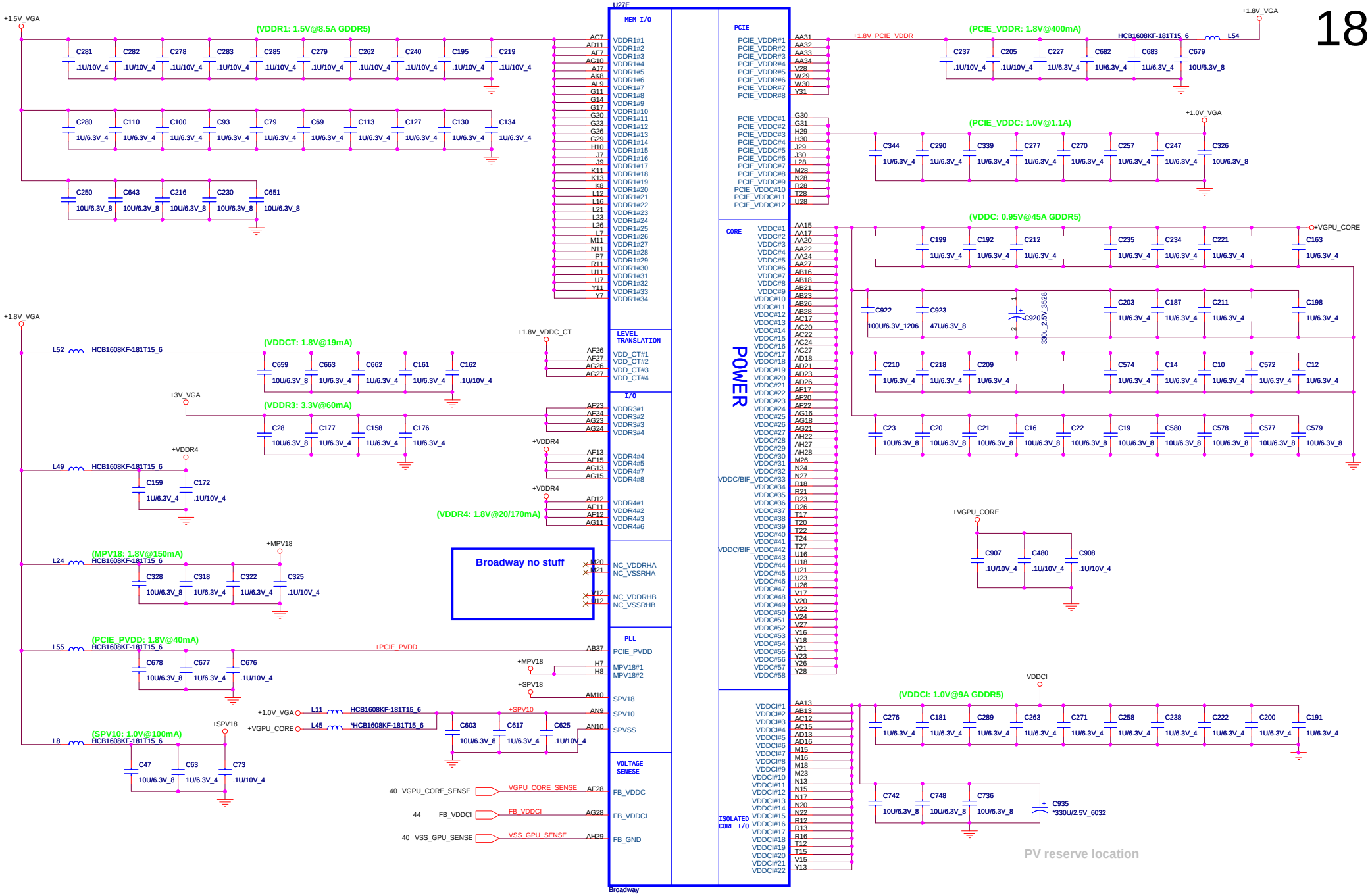

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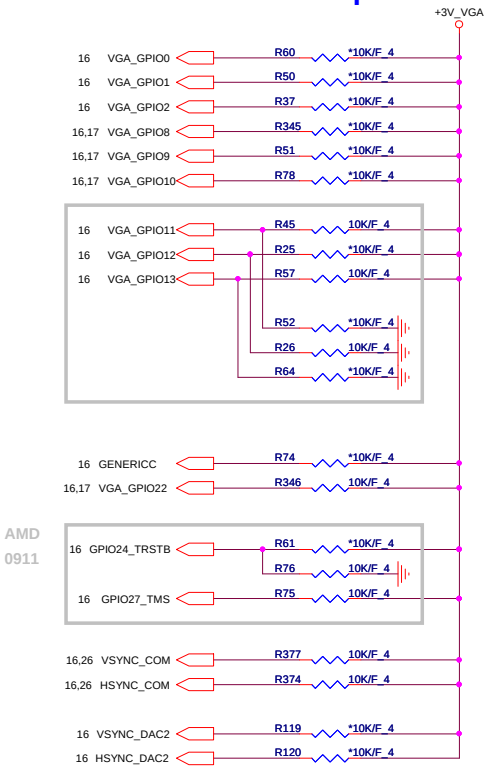
Straps



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground ↓ High logic voltage

Signal

Strap Name	Pin Straps Description		Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSYNC		
AUD(1)	HSYNC		
VSYNC_DAC2	V2SYNC		
HSYNC_DAC2	H2SYNC		
	GENERICC		

Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	3A

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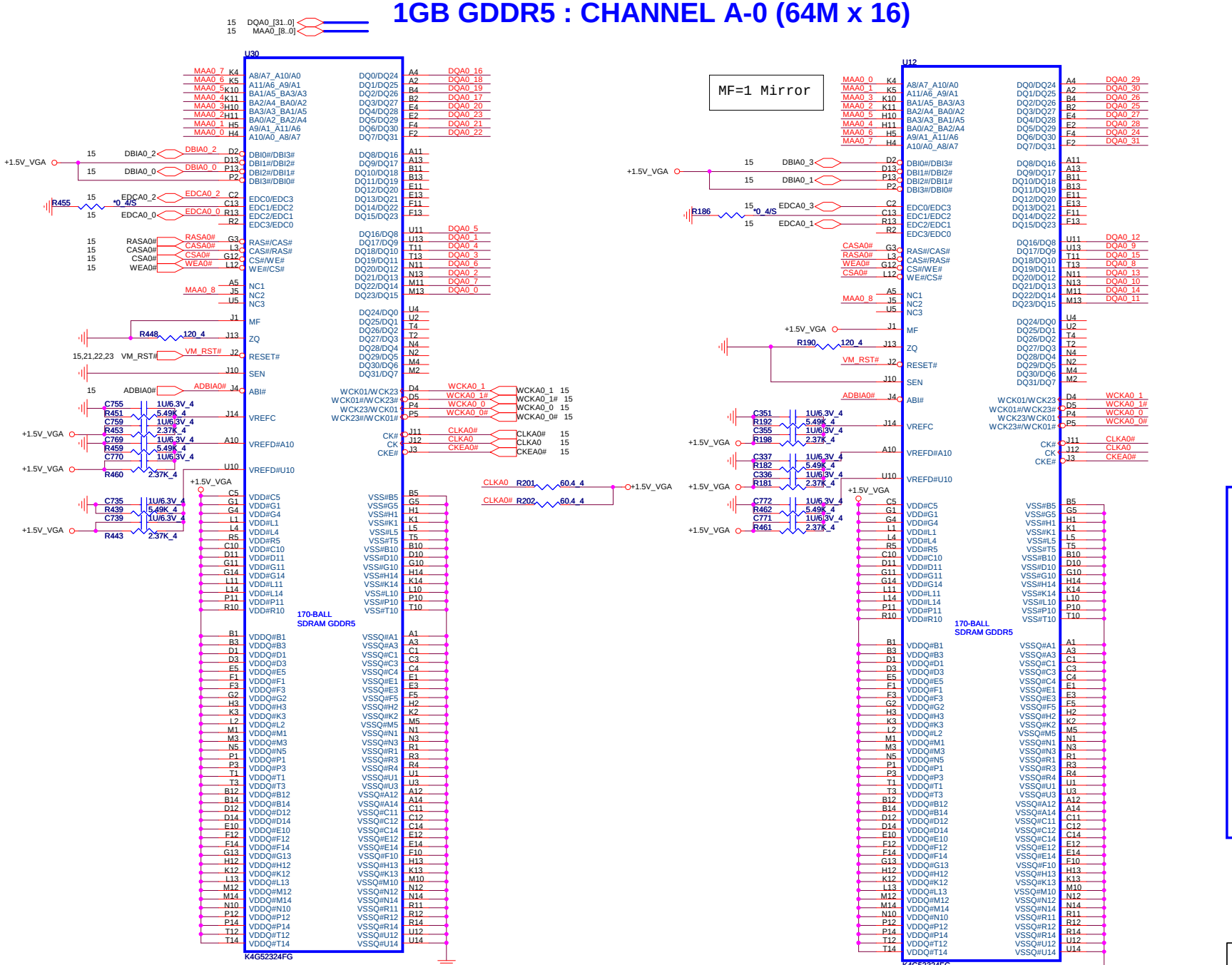
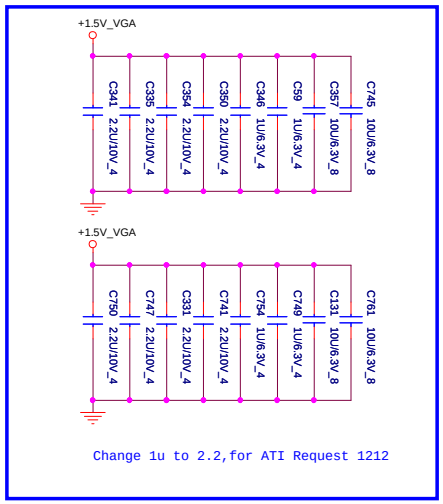
1GB GDDR5 : CHANNEL A-0 (64M x 16)





Change 1u to 2.2,for ATI Request 1212

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	3A

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N85/RD2

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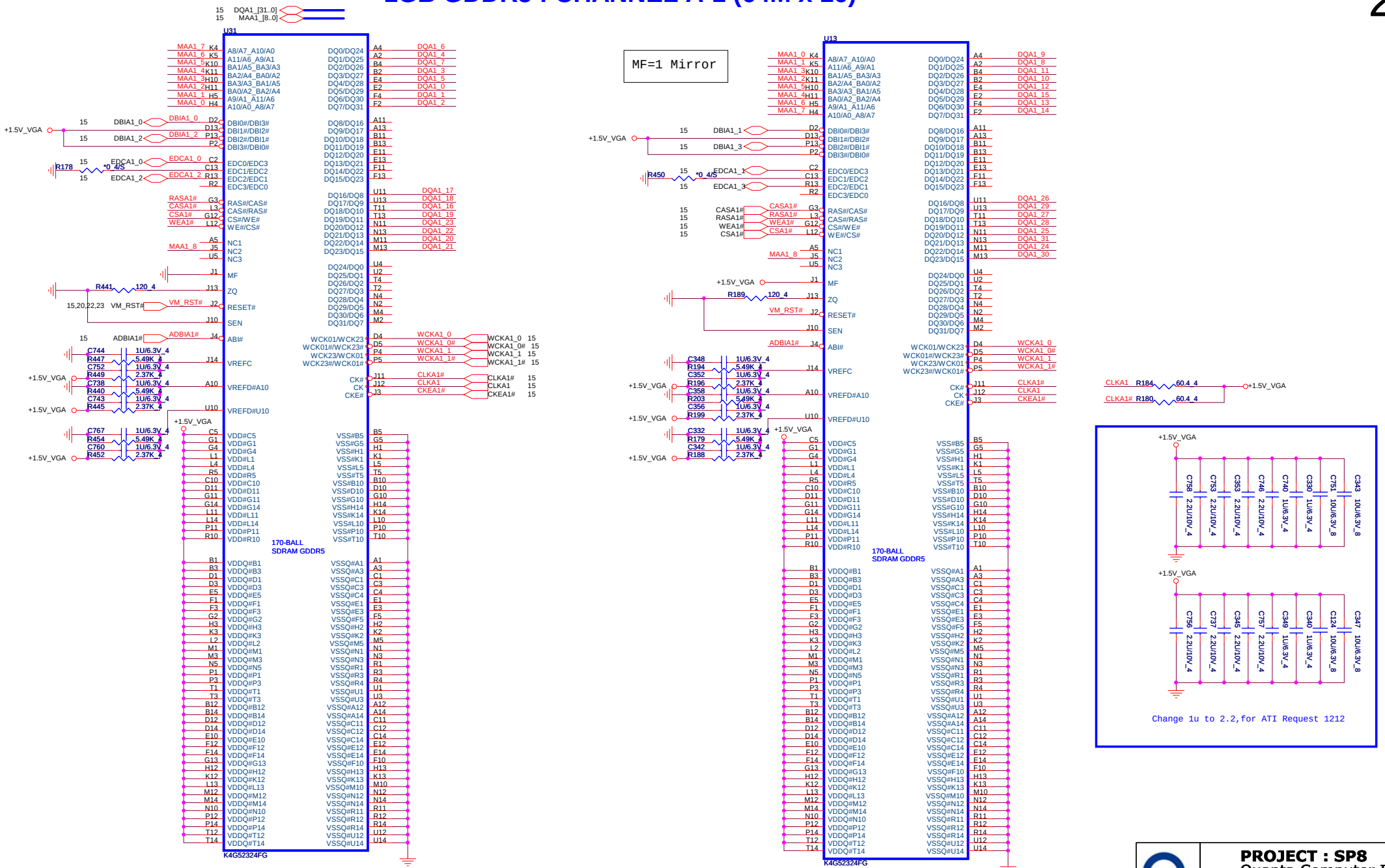
1GB GDDR5 : CHANNEL A-1 (64M x 16)



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	3A

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N85/RD2

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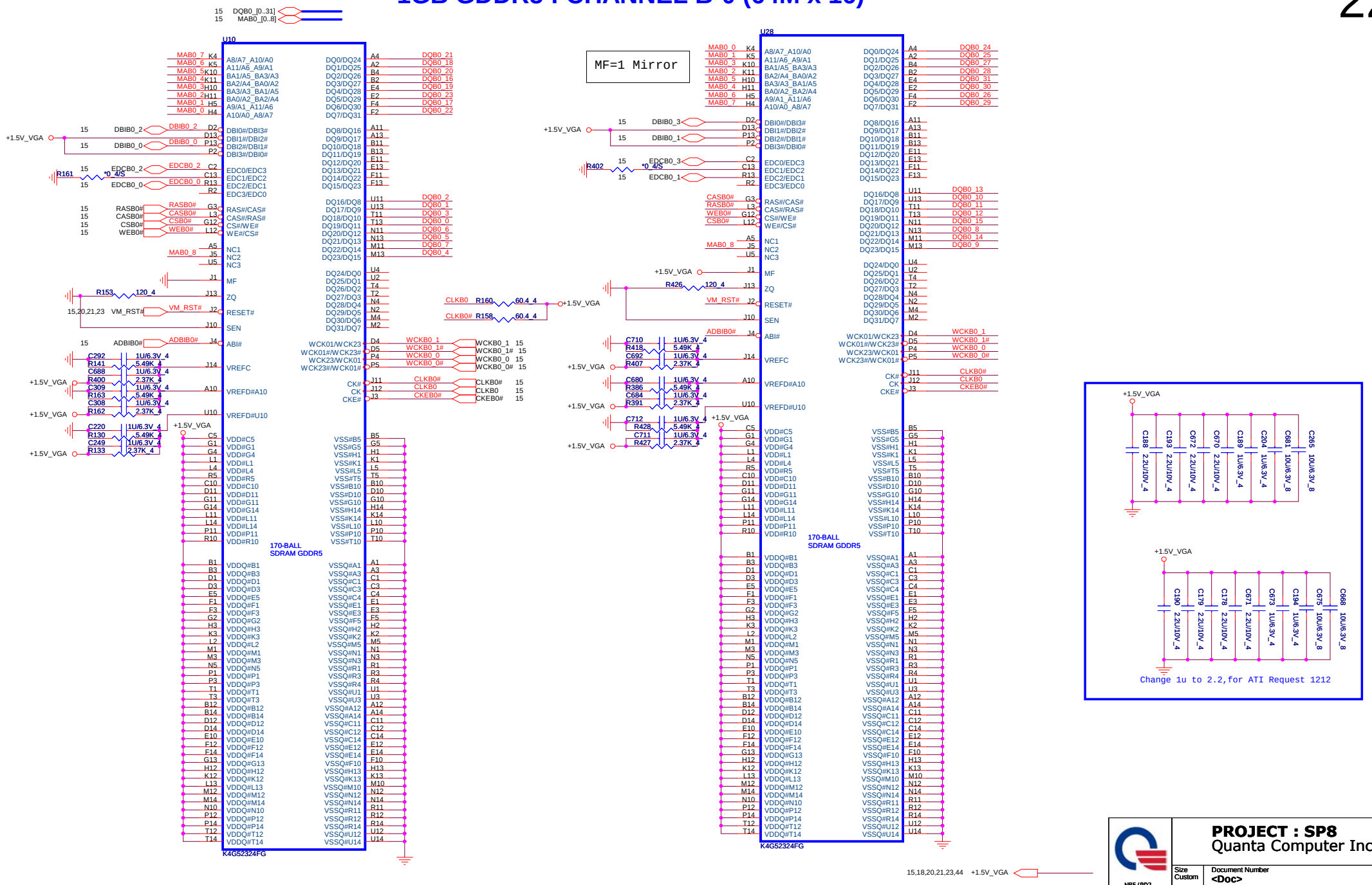
1GB GDDR5 : CHANNEL B-0 (64M x 16)



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	3A

NB5/RD2

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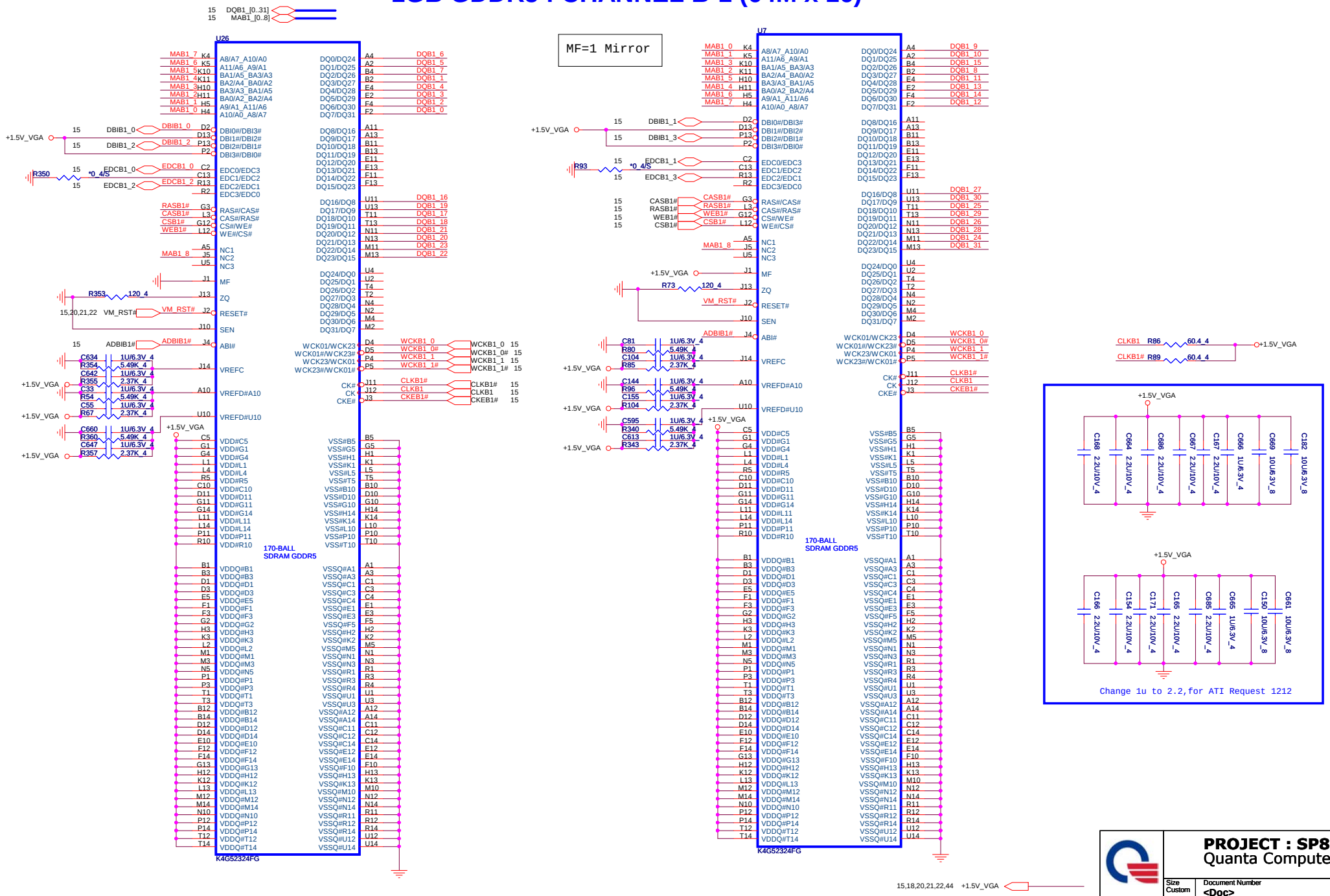
1GB GDDR5 : CHANNEL B-1 (64M x 16)



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	3A

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NB5/RD2

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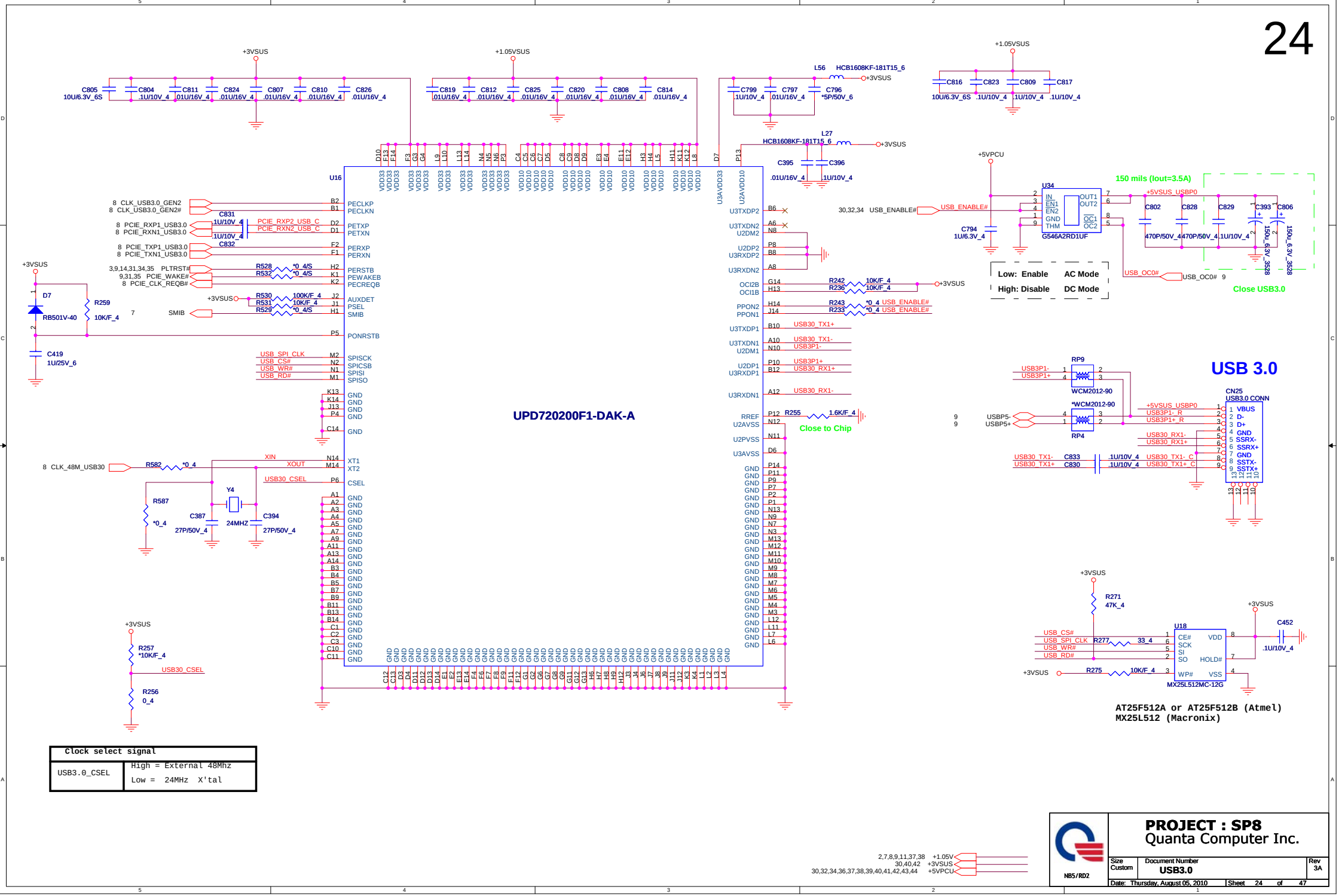

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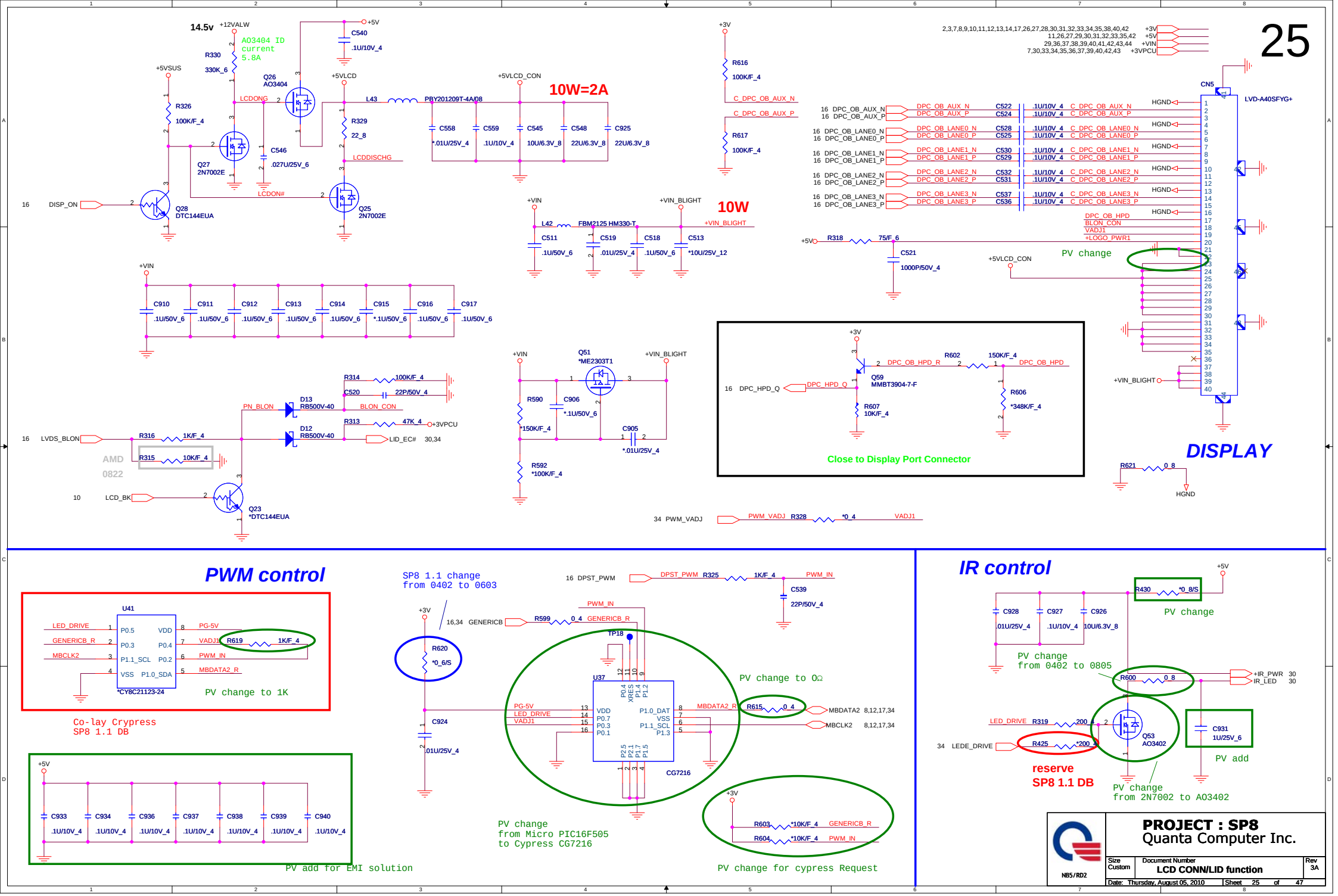

PWM control

Co-lay Crypress
SP8 1.1 DB

PV add for EMI solution

PV change for cypress Request

IR control

N85/RD2	**PROJECT : SP8** Quanta Computer Inc.	
Size Custom	Document Number **LCD CONN/LID function**	Rev 3A
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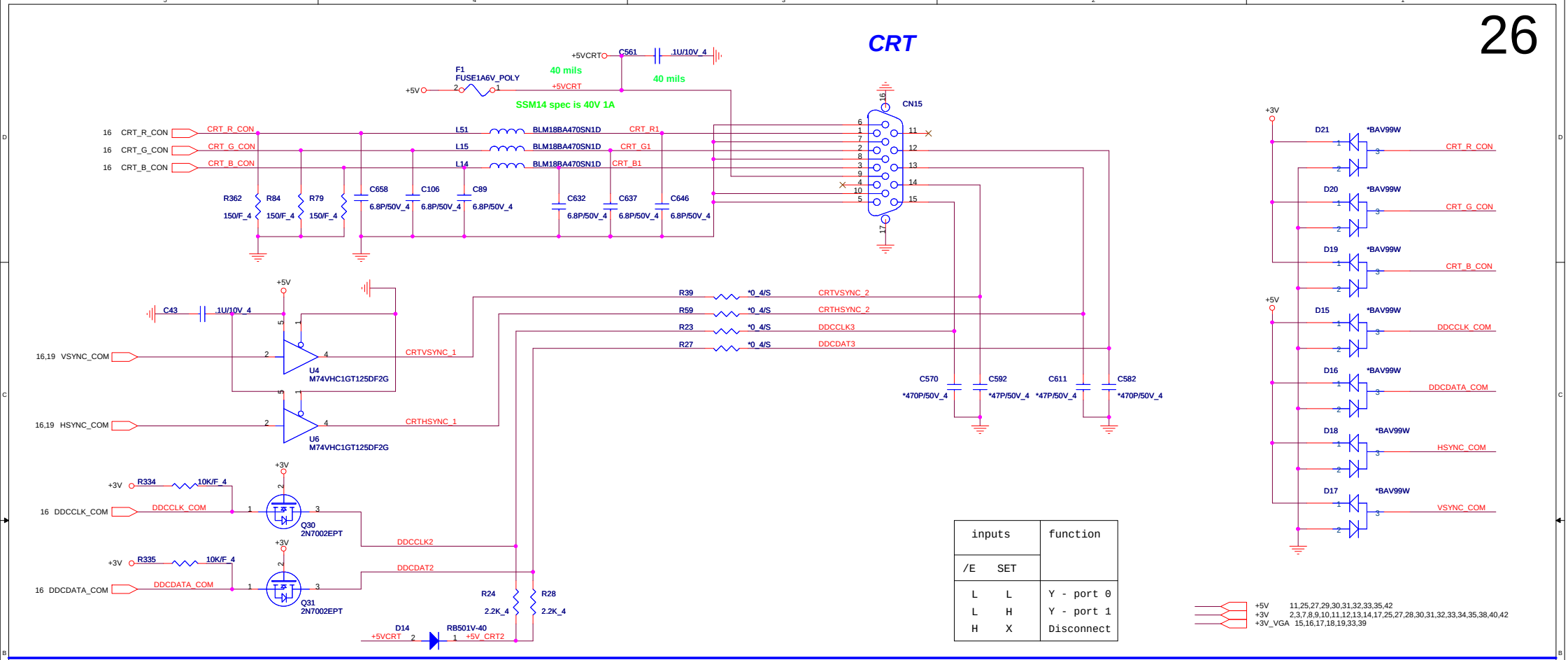
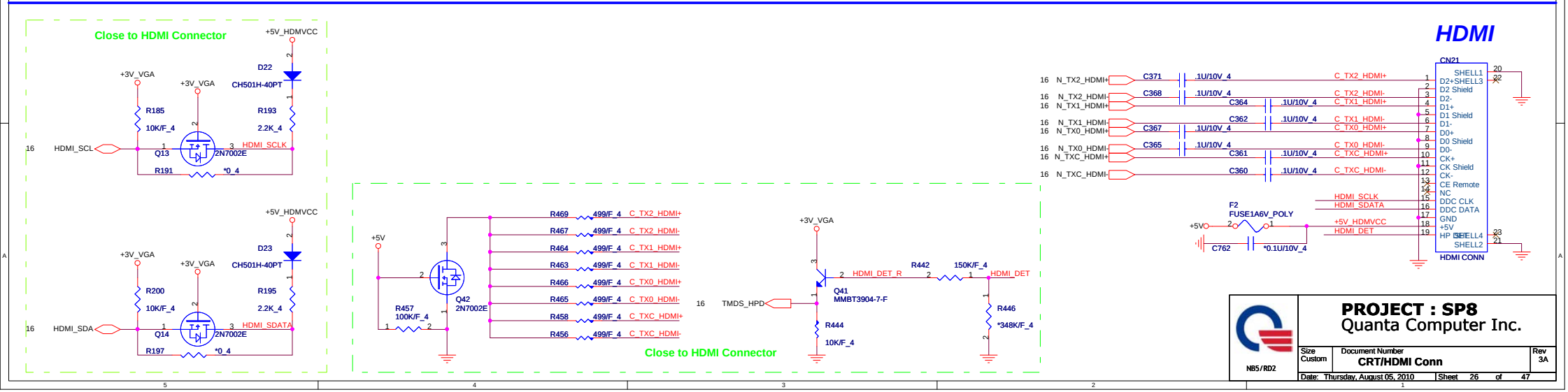
CRT



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

HDMI



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	3A

NB5/RD2

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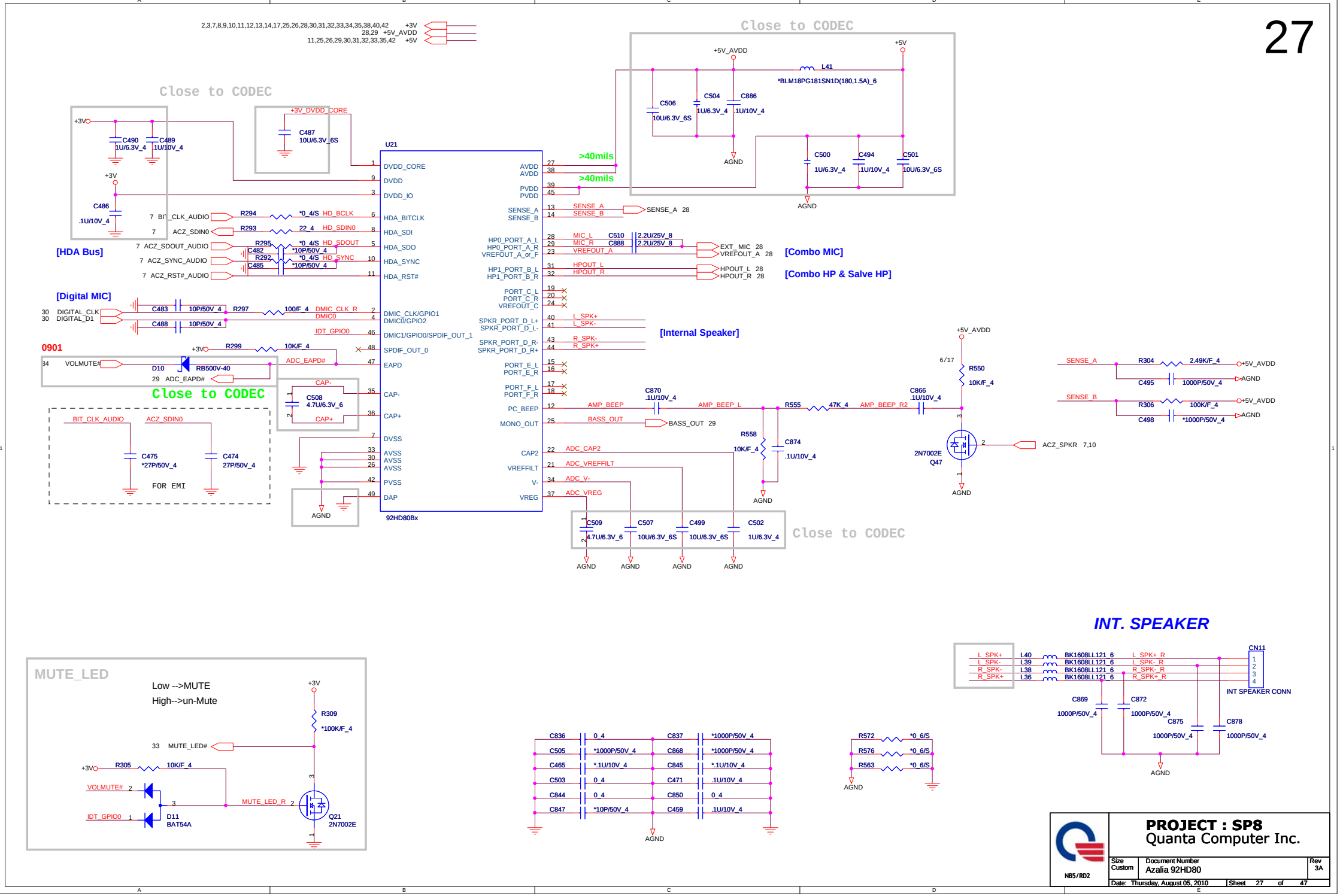

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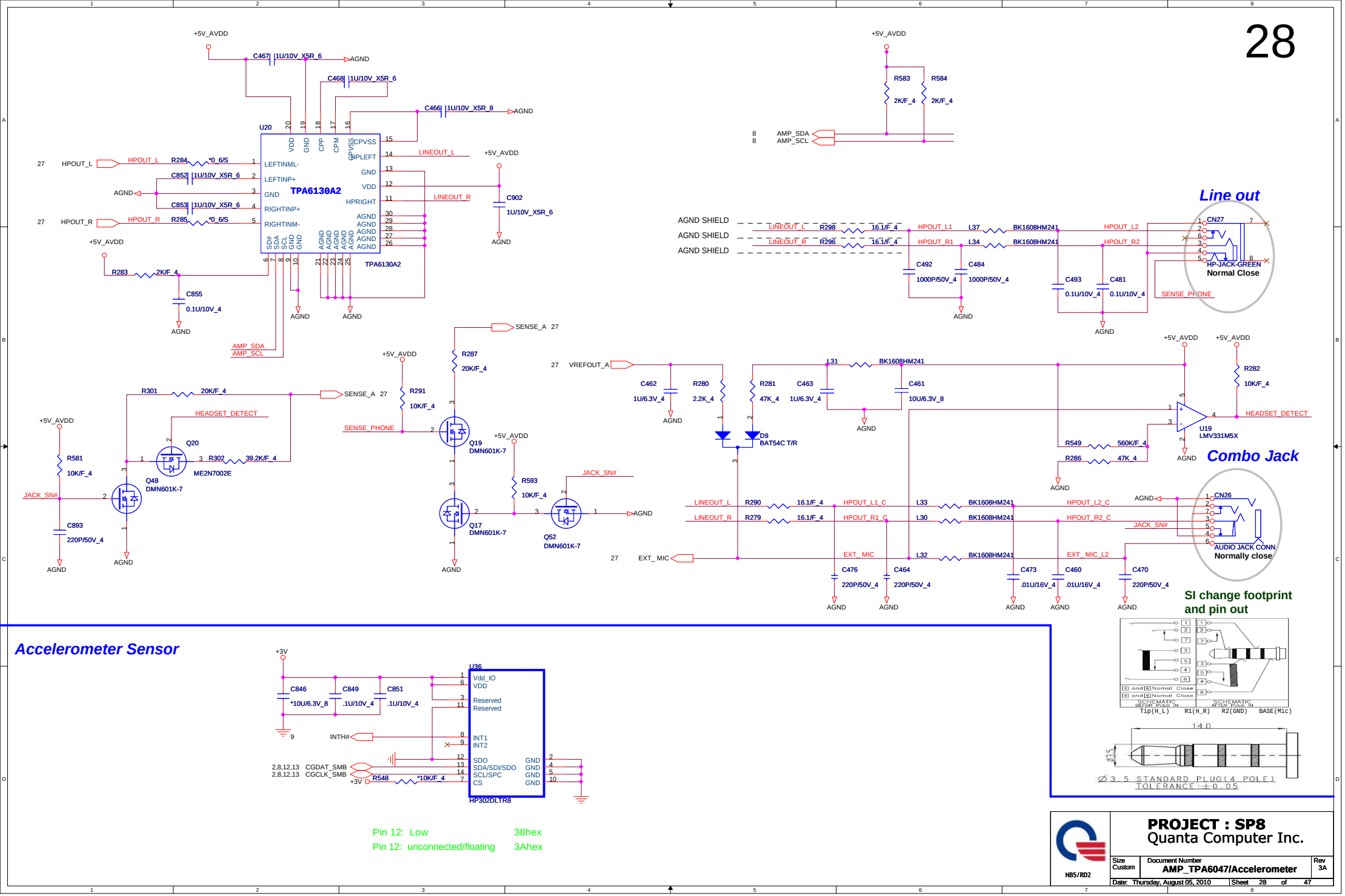

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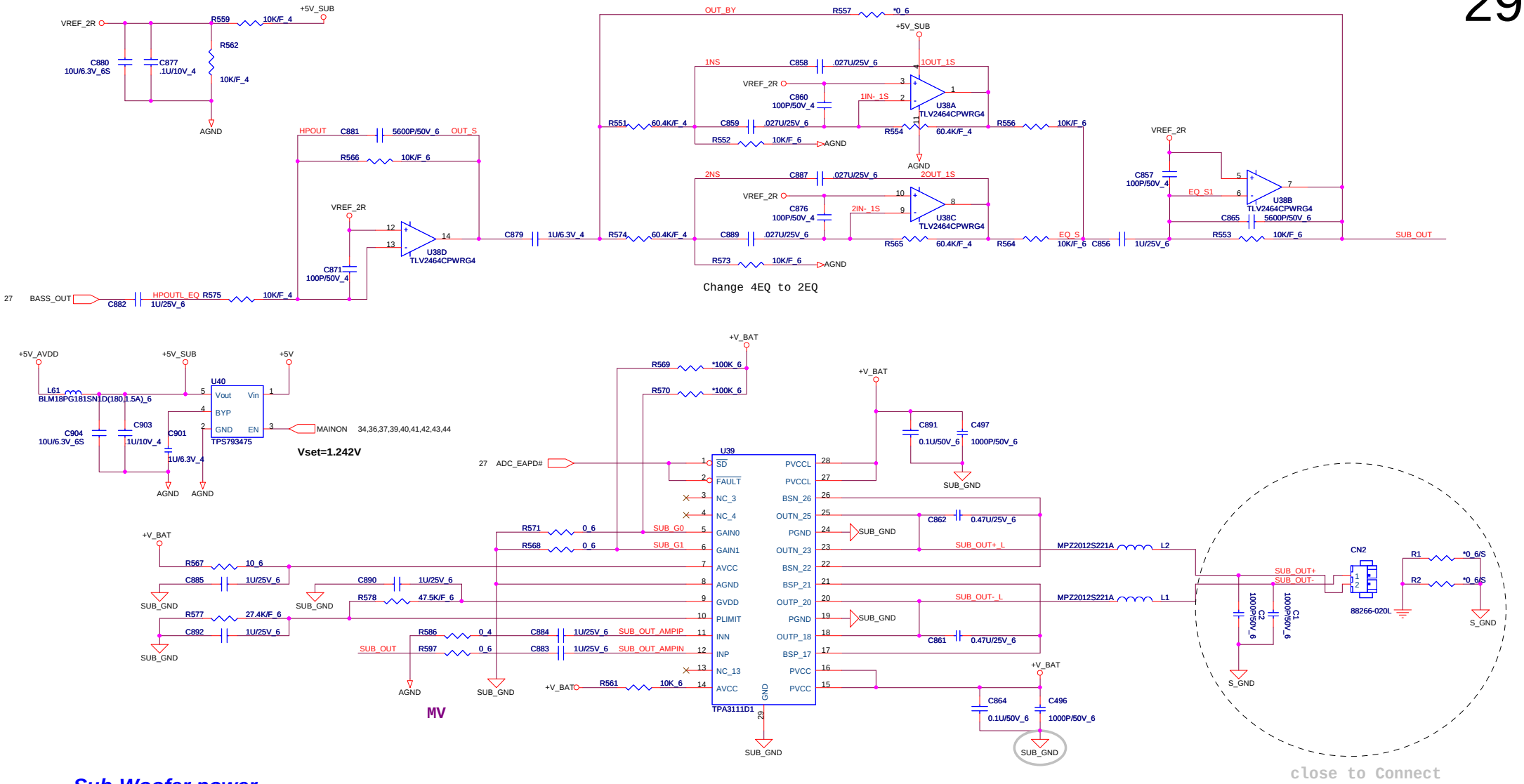
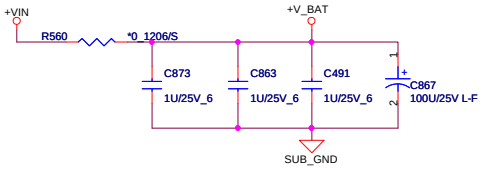
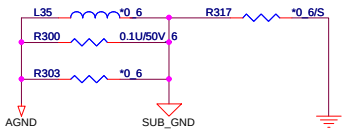
SUBWOOFER

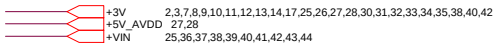


Sub-Woofer power



GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36





PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER (EQ & AMP.)	3A

NB5/RD2

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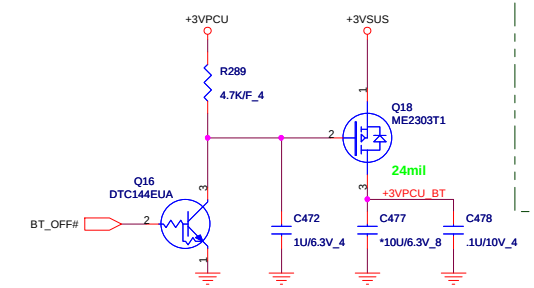
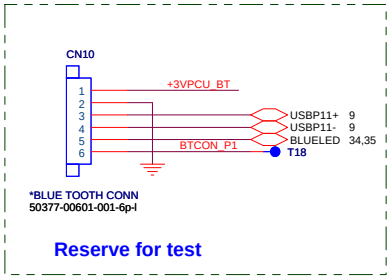
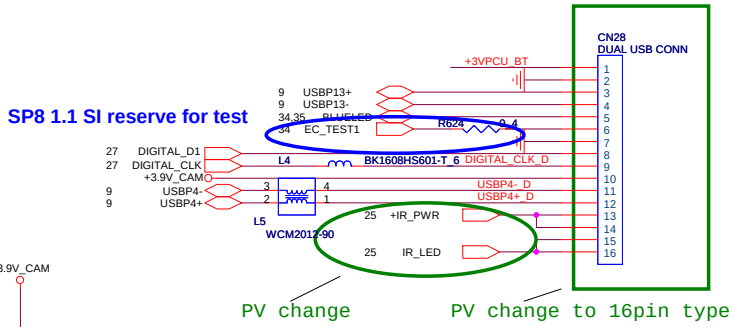
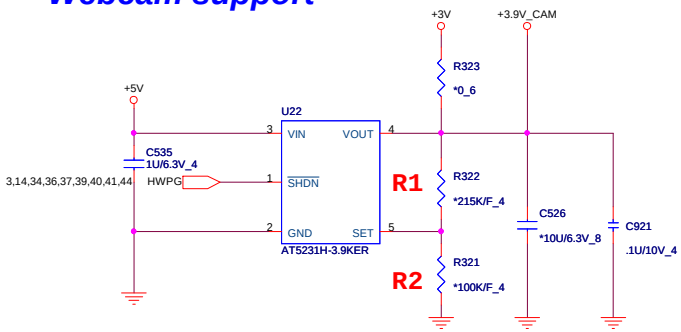
Bluetooth





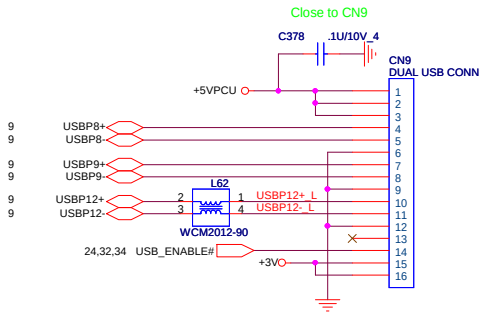


Webcam support

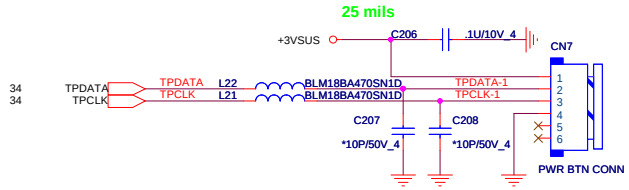


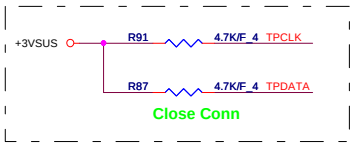
Vout=1.25(1+R1/R2)

Ext USB & Card Reader

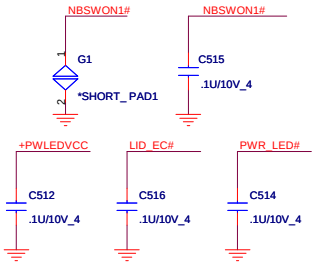


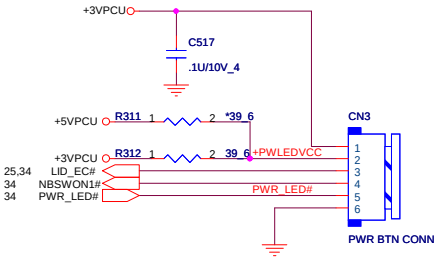
Touch Pad Botton





Power Botton





1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/Touchscreen	3A

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T : Stuffed for RTL8111DL(10/100/1000)

for RTL8111DL use close Pin 44,45

for RTL8111DL use

+CTRL12DVDD — +CTRL12DVDD — C366 22U/6.3V_8 — C775 0.1U/10V_4 — R468 *0_6/S short0603 — +3V_LAN

Remove R3571,R3573

R3571 and R3573 are used in RTL8111DL , remove R3573 if switching regulator is enable , Remove R3571 external power is used.

+3VLANVCC — R470 *0_8/S short0805 — +3V_LAN

C777 0.1U/10V_4, C776 0.1U/10V_4, C778 0.1U/10V_4, C768 0.1U/10V_4

Close to PIN 1

Y3 25MHZ — C376 33P/50V_4 — C370 33P/50V_4 — XTAL1 — XTAL2

+CTRL12DVDD — R204 2.49K/F_4 — LANRSET

+3V_LAN — +DVDD12_LAN — ENSWREG — +CTRL12A — LAN_TX# — +3V_LAN

AL08111DB00 RTL8111DL-GR

U32 NS892405

C766 .01U/16V_4	V_DAC0	TCT1 / TD1+	MCT1 / MX1+	LAN_MCT0 / LAN_MX0+	C734 0.01U/100V_0603, R433 75/F_4
	MDI0+ / MDI0-	TD1-	MX1-	LAN_MX0-	
C765 .01U/16V_4	V_DAC1	TCT2 / TD2+	MCT2 / MX2+	LAN_MCT1 / LAN_MX1+	C733 0.01U/100V_0603, R432 75/F_4
	MDI1+ / MDI1-	TD2-	MX2-	LAN_MX1-	
C764 .01U/16V_4	V_DAC2	TCT3 / TD3+	MCT3 / MX3+	LAN_MCT2 / LAN_MX2+	C732 0.01U/100V_0603, R436 75/F_4
	MDI2+ / MDI2-	TD3-	MX3-	LAN_MX2-	
C763 .01U/16V_4	V_DAC3	TCT4 / TD4+	MCT4 / MX4+	LAN_MCT3 / LAN_MX3+	C731 0.01U/100V_0603, R435 75/F_4
	MDI3+ / MDI3-	TD4-	MX4-	LAN_MX3-	

C323 1000P/3KV_1808

U14 RTL8103EL/8111DL

AVDD33, MDIP0, MDIN0, NC/FB12, MDIP1, MDIN1, GND1, NC/MDIP2, NC/MDIN2, DVDD12/AVDD12, NC/MDIP3, NC/MDIN3

DVDD12B, LED1/EESK, LED2/EEDI, LED3/EEDO, EECS, GND3, DVDD12A, VDD33A, ISOLATEB, PERSTB, LANWAKEB, CLKREQB

LAN_GLINK100# — +DVDD12_LAN; LAN_GLINK10# — R207 3.6K_6 — +3V_LAN; EECS — T14; +DVDD12_LAN; +3V_LAN; ISOLATEB; PLTRST#_R# — R205 *0_4/S — PLTRST# 3,9,14,24,34,35; PCIE_WAKE# — PCIE_WAKE# 9,24,35; PCIE_CLK_REQ3# — PCIE_CLK_REQ3# 8

+3V_LAN, +DVDD12_LAN, MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-, +DVDD12_LAN

VCTRL12A/SROUT12, GND4, RSET, VCTR12DVDDSR, NC/VDDSR, NC/ENSWREG, CKTAL2, CKTAL1, NC/AVDD33, NC/LV_PLL, LED0, VDD33B

DVDD12, GND2, HSIP, HSIN, REFCLK_P, REFCLK_N, EVDD12, HSOP, HSON, EGND, NC/GPO, NC/NC

+DVDD12_LAN

8 PCIE_TXP1_LAN — PCIE_TXP6_LAN
8 PCIE_TXN1_LAN — PCIE_TXN6_LAN
8 CLK_PCIE_LAN — CLK_PCIE_LAN
8 CLK_PCIE_LAN# — CLK_PCIE_LAN#

PCIE_RXN1_LAN_L — C374 0.1U/10V_4 — PCIE_RXN1_LAN 8
PCIE_RXP1_LAN_L — C372 0.1U/10V_4 — PCIE_RXP1_LAN 8

EVDD12

+3V — R208 *1K/F_4 — ISOLATEB — R209 100_4 — LAN_DISABLE# 10,34

R206 15K/F_4 — *RB501V-40 D5

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

LAN_GLINK100# — LAN_White#
LAN_TX# — LAN_Amber#
C381 *.01U/16V_4 — C375 *.01U/16V_4

Link

NS892402:GIGABIT DB0AT9LAN05

>60mil — +CTRL12A — L25 4.7UH_8 — >60mil — +CTRL12A_L

Power trace Layout 寬度> 60mil

L23
RTL8111DL (Gaga lan) use 4.7uH power choke A>600mA tolerance ±15%

C359 22U/6.3V_8 — C373 0.1U/10V_4

EVDD12 — C363 1U/10V_4 — C380 1U/10V_4

Close to 8111DL DVDD12 pins-- 19

+DVDD12_LAN

C773 0.1U/10V_4, C369 0.1U/10V_4, C379 0.1U/10V_4, C779 0.1U/10V_4, C774 0.1U/10V_4

Close to 8111DL DVDD12 pins-- 10, 13, 30, 36, 39.

PV Stuff for EMI solution

RJ45

+3V_LAN — R380 *30_4 — C674 .1U/10V_4

+5V — R596 100_4

CN17 RJ45_CONN

LAN_White# 12, LAN_White 11 — LED_White_N, LED_White_P

LAN_MX3- 8, LAN_MX3+ 7, LAN_MX1- 6, LAN_MX2- 5, LAN_MX2+ 4, LAN_MX1+ 3, LAN_MX0- 2, LAN_MX0+ 1 — RX1-, RX1+, RX0-, TX1-, TX1+, RX0+, TX0-, TX0+ — FOR EMI

GND 13, GND 14, GND 15, GND 16

LAN_Amber# 10, LAN_Amber 9 — LED_Amber_N, LED_Amber_P

+3V_LAN — R419 56_4 — C693 .1U/10V_4

White is Link,Amber is active

PV Stuff for EMI solution

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Size	Document Number	Rev
Custom	8103E/RJ45	3A

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NB5/RD2

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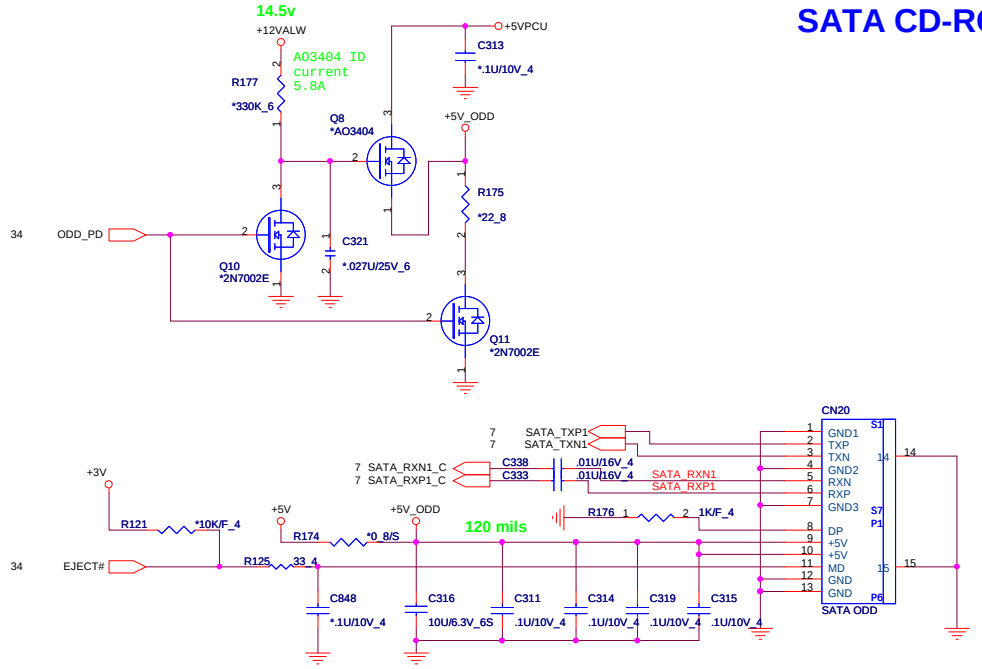
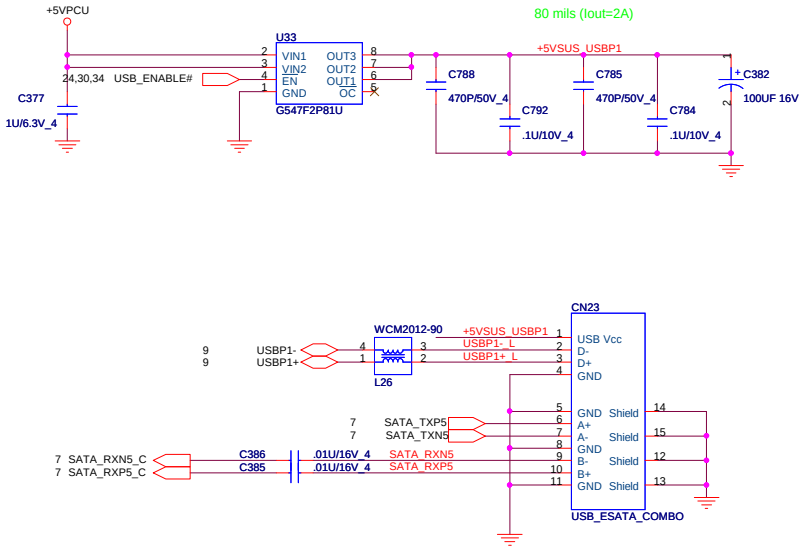
SATA CD-ROM

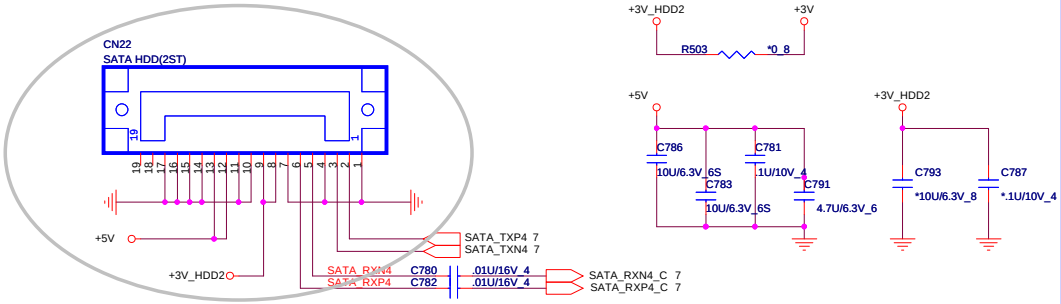


E-SATA



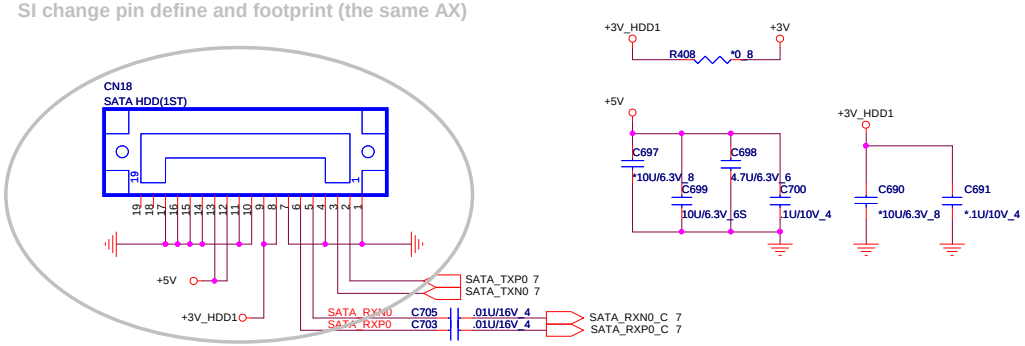
SATA HDD #1

SI change pin define and footprint (the same AX)



SATA HDD #2

SI change pin define and footprint (the same AX)



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/ONFI	3A

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NB5/RD2

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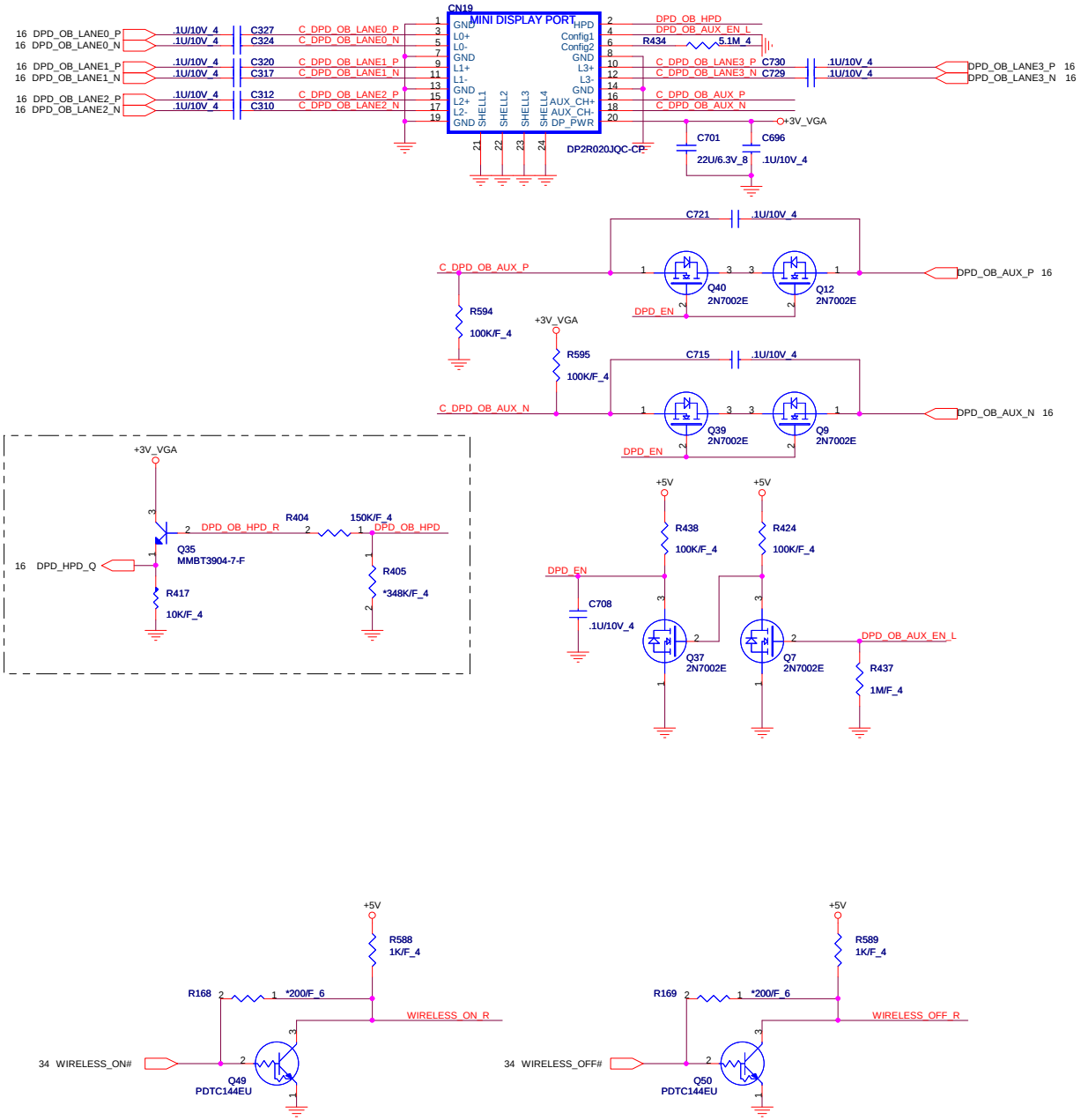
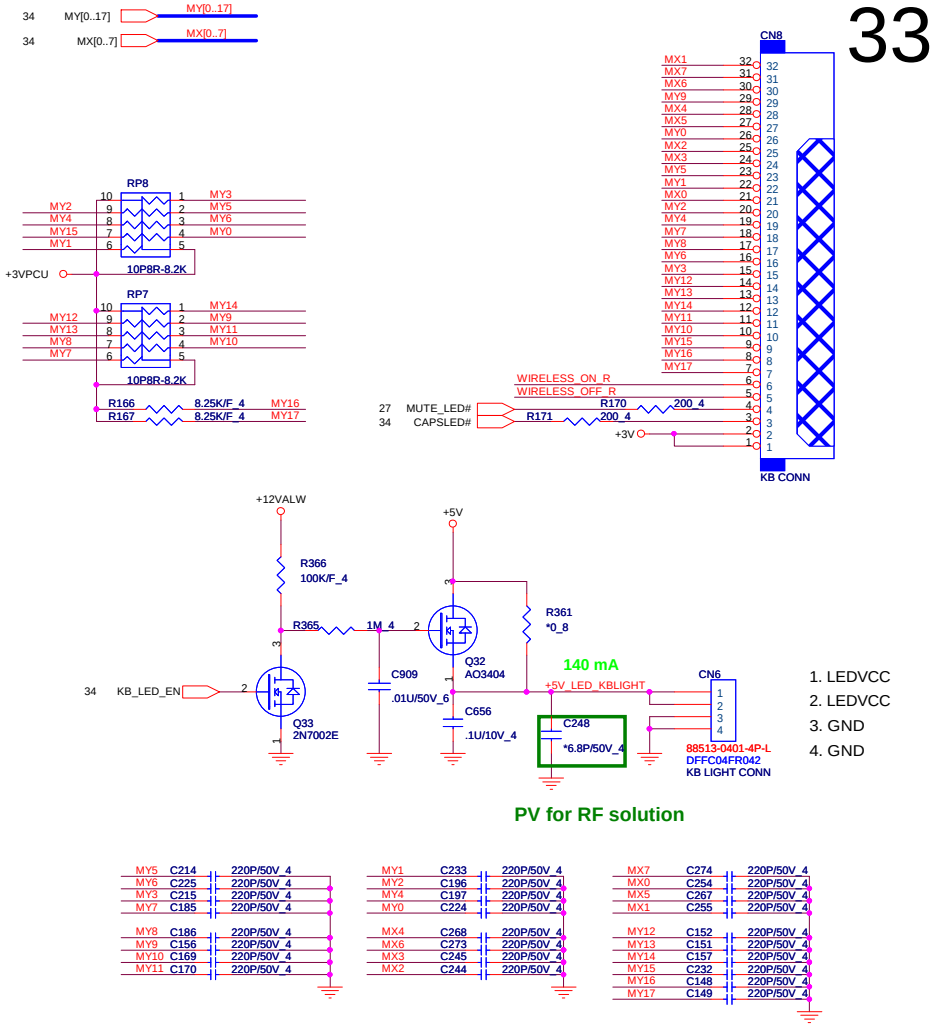
Mini Display





PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/LED/POWER CONN	3A

N85/RD2

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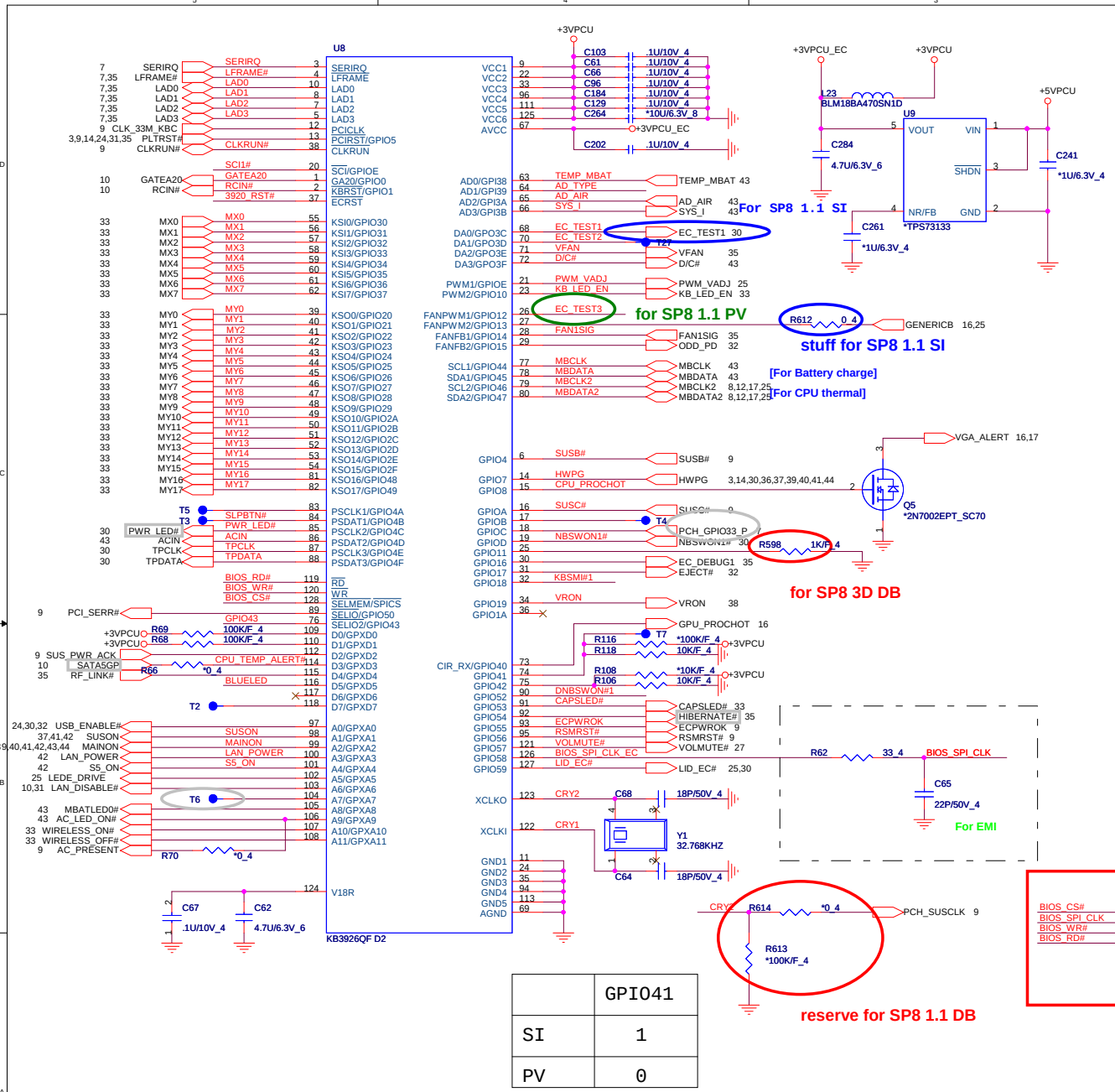
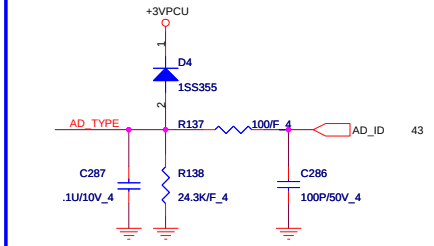


Adapter Type



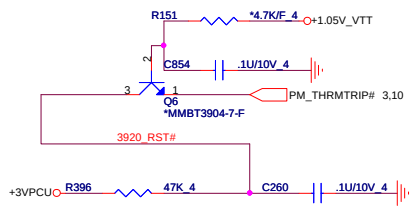
R273

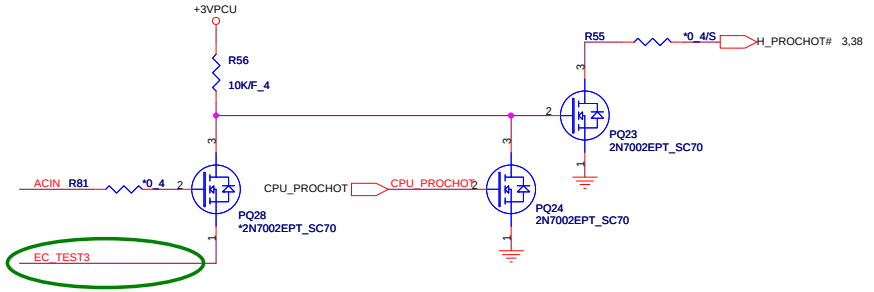
64.9K -->65W CS36492FB17

33.2K -->90W CS33322FB13

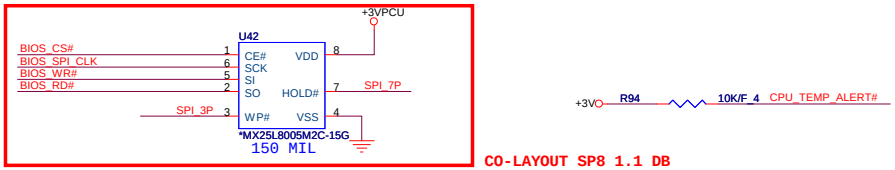
Change to 1SS355 as Current loss

Thermal Shutdown





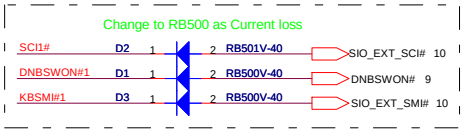
for SP8 1.1 PV EC request

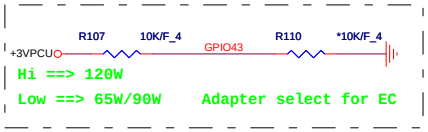


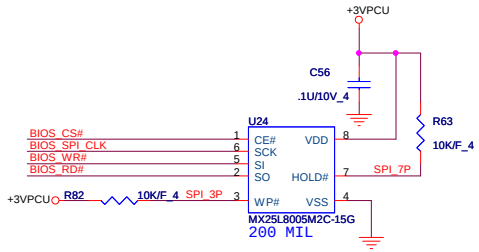
CO-LAYOUT SP8 1.1 DB

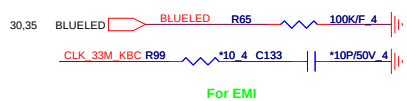
+3V R94 10K/F_4 CPU_TEMP_ALERT#

	GPIO41
SI	1
PV	0









PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	3A

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NB5/RD2

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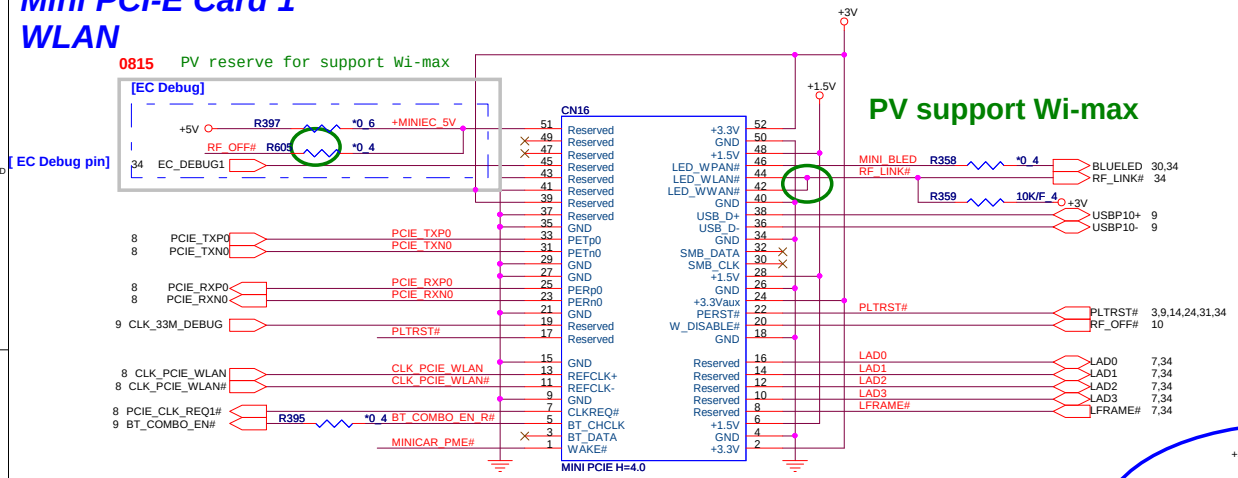
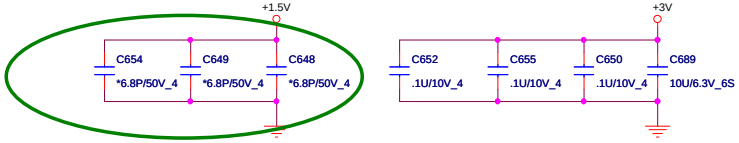
Mini PCI-E Card 1
WLAN

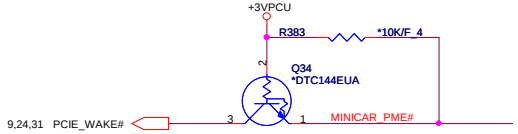
0815 PV reserve for support Wi-max

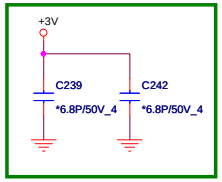


PV support Wi-max

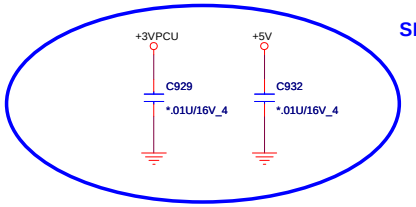


PV for RF solution

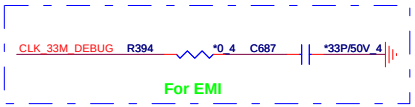




PV for RF solution

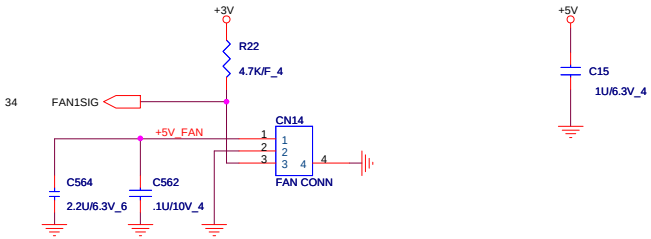


SP8 1.1 SI for RF reserve

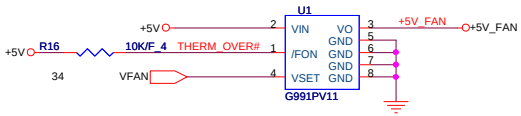


BT_DATA,BT_CHCLK,CLKREQ#,W_DISABLE# pin has internal pull-Down 100k resister.

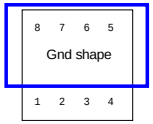
CPU FAN



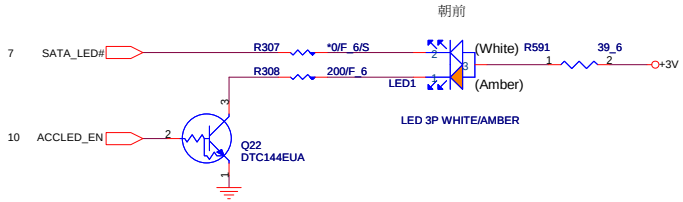
FANPWR = 1.6*VSET 30 MIL

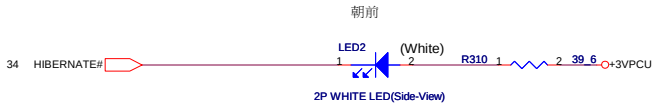


G995 layout notice



LED





PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2	3A

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NB5/RD2

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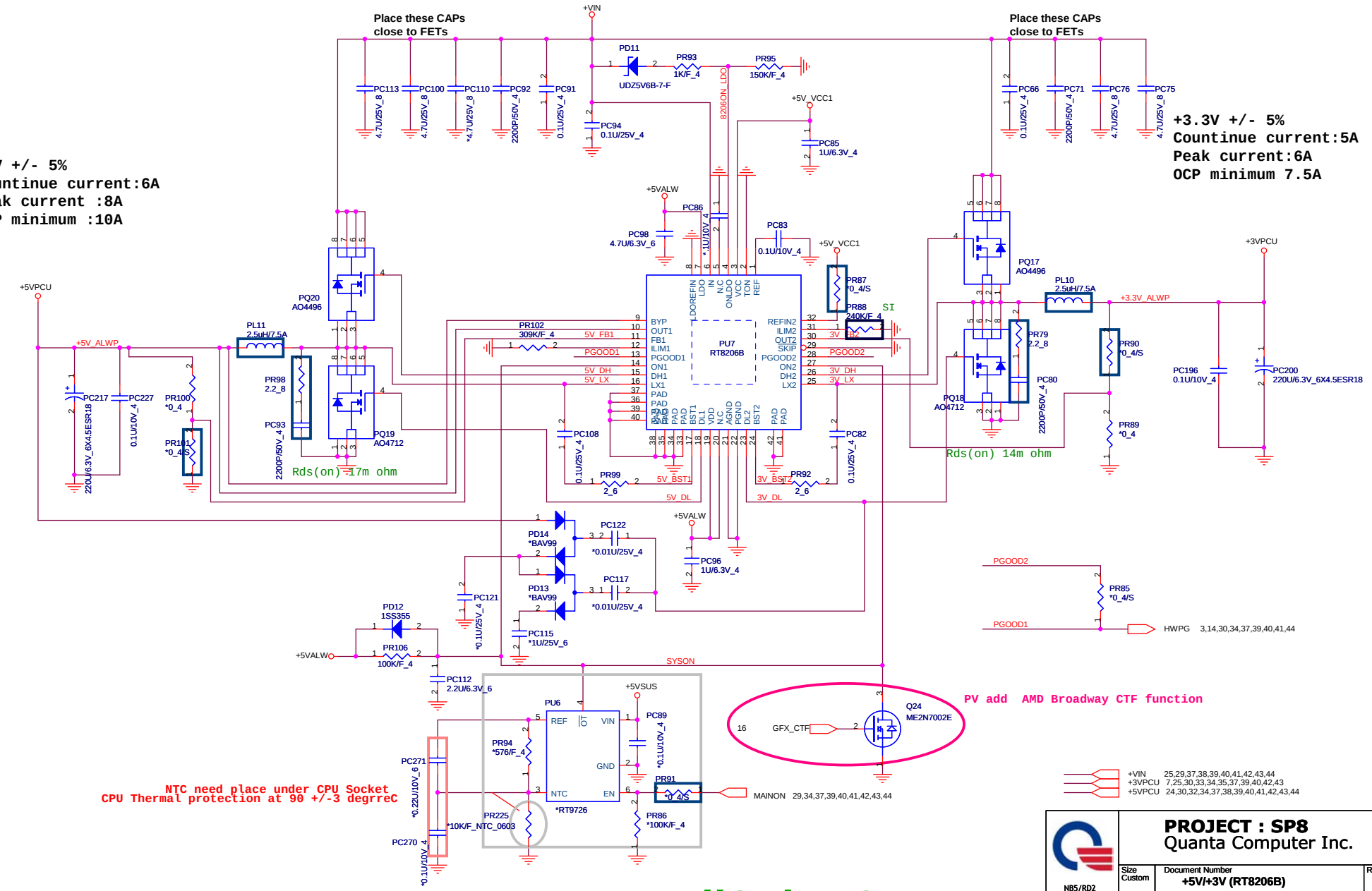
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	3A

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NB5/RD2

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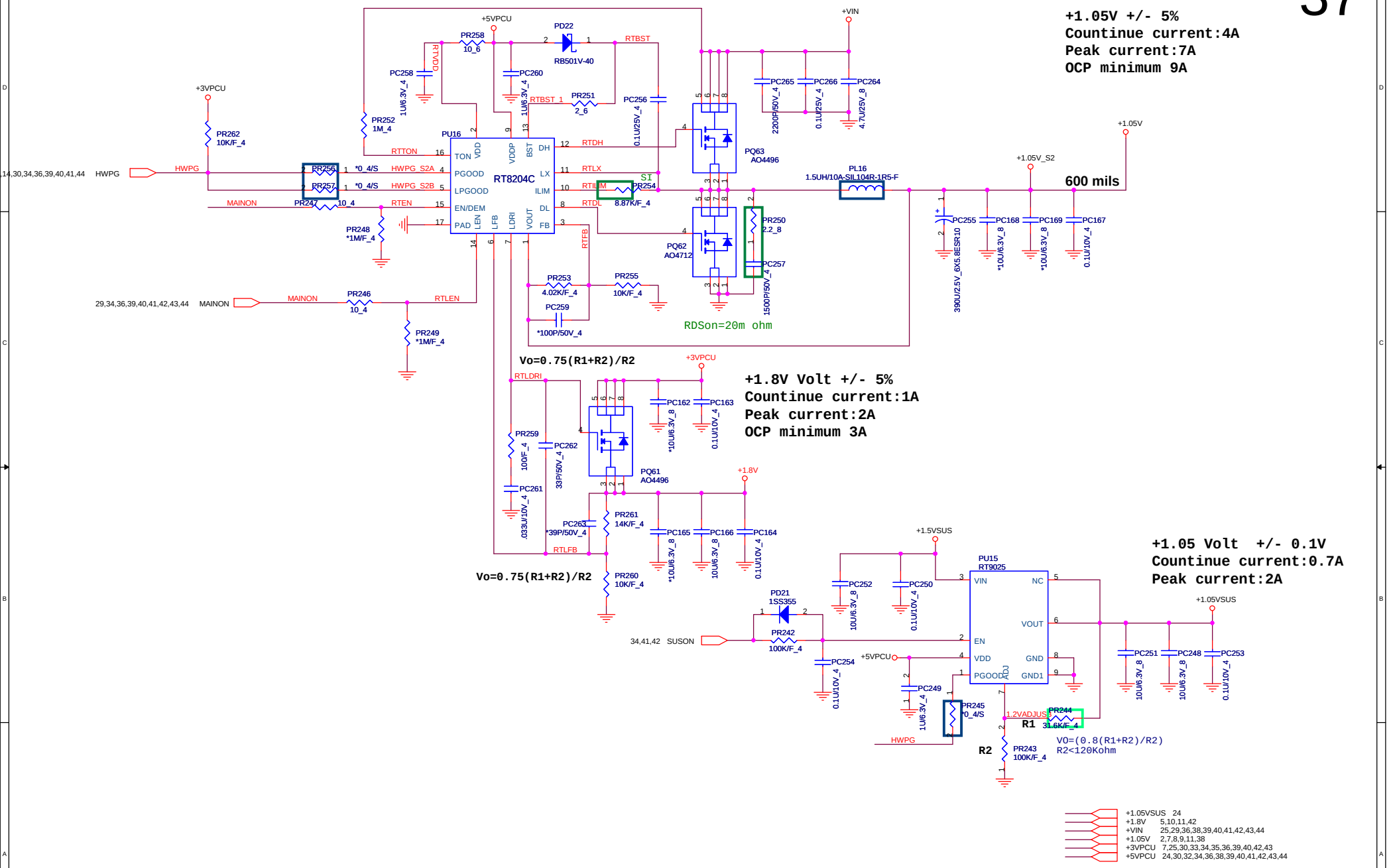

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V/+1.8V (RT8204C)	3A

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NB5/RD2

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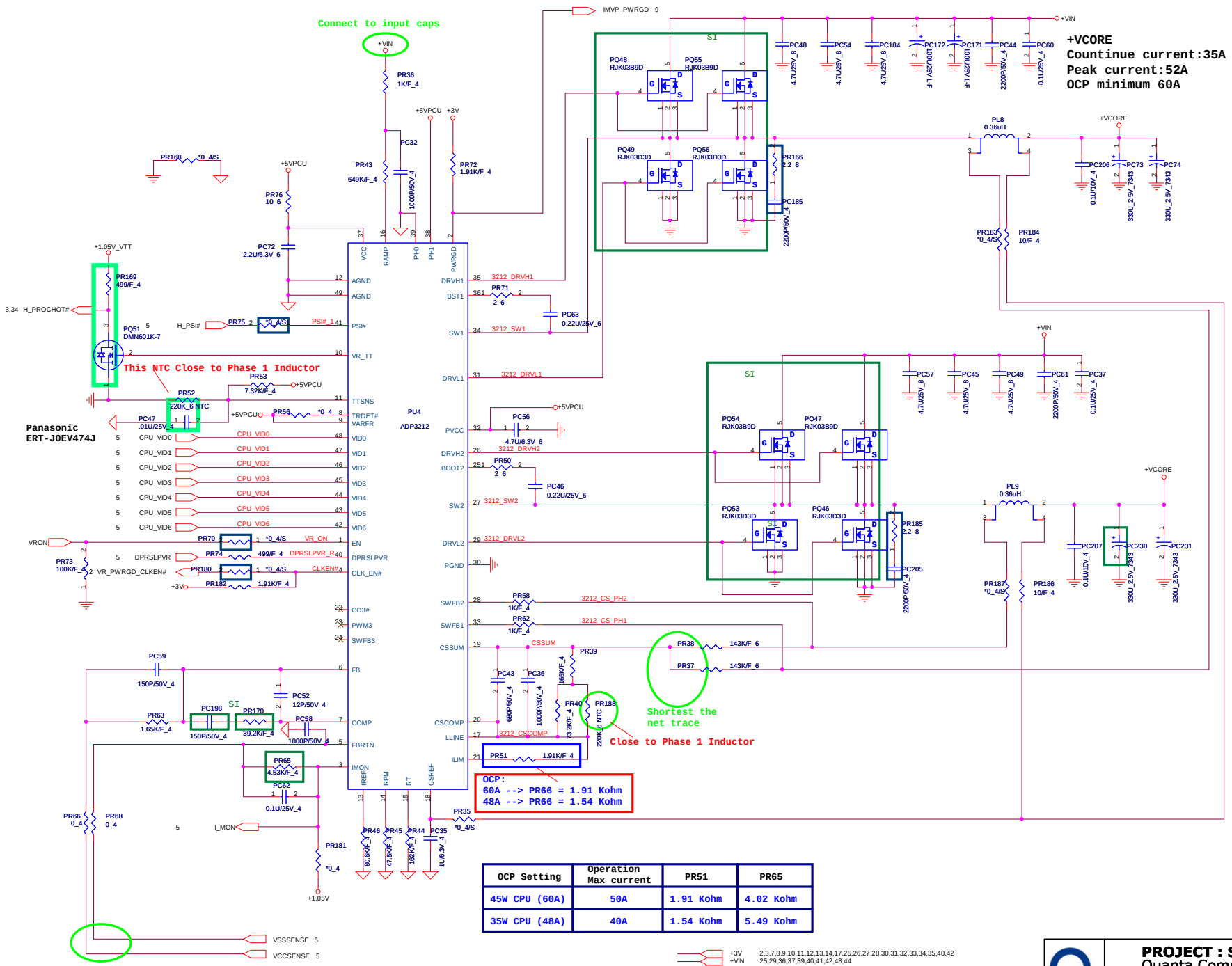

OCP Setting	Operation Max current	PR51	PR65
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	5.49 Kohm

+3V 2,3,7,8,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,40,42
+VIN 25,29,36,37,39,40,41,42,43,44
+1.05V 2,7,8,9,11,37
+5VPCU 24,30,32,34,36,37,39,40,41,42,43,44
+VCORE 5
+1.05V_VTT 3,5,10,11,34,39

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (ADP3212)	3A

N85/RD2

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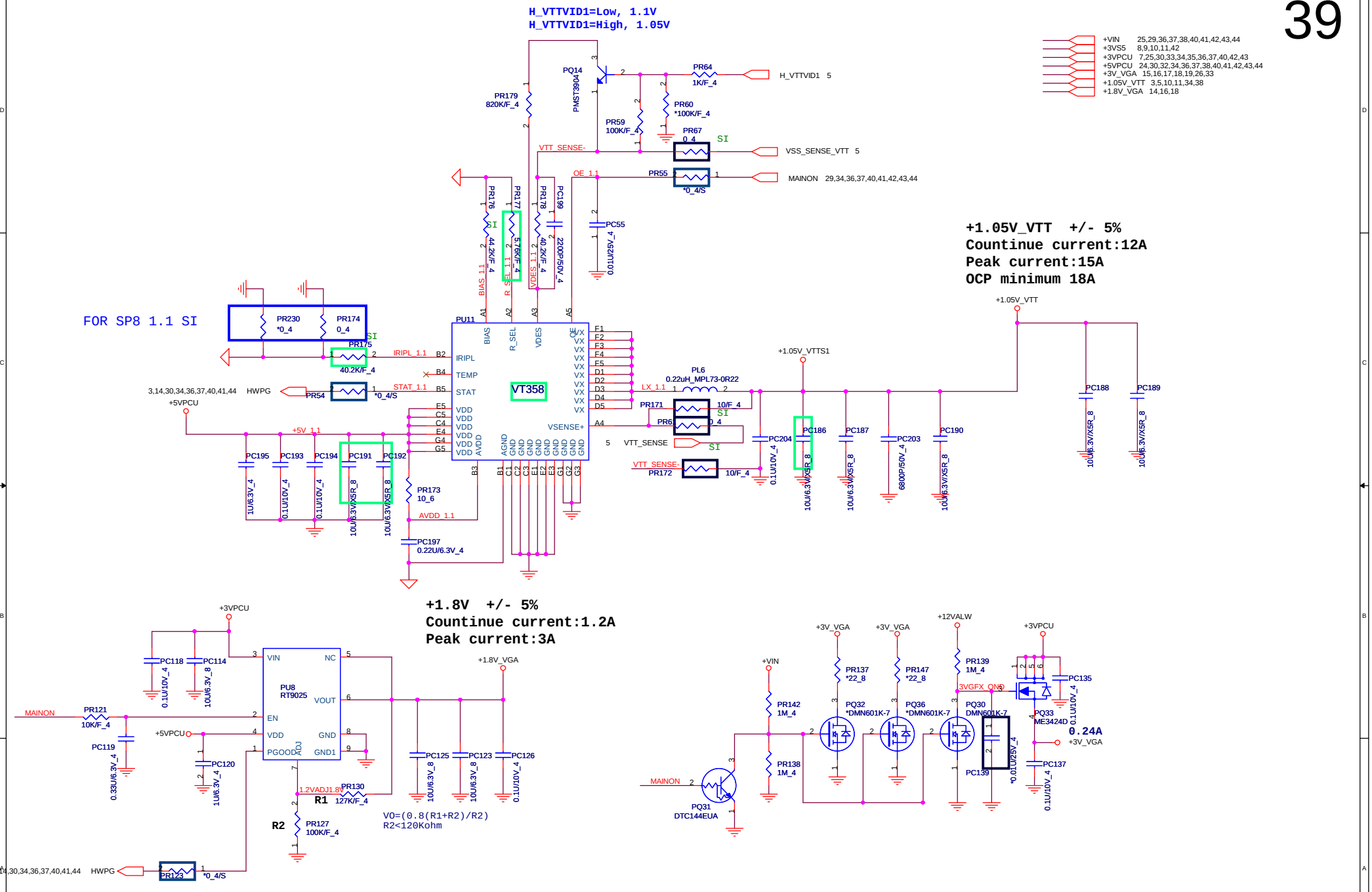

PROJECT : SP8
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	+1.05V_VTT (VT358)	3A

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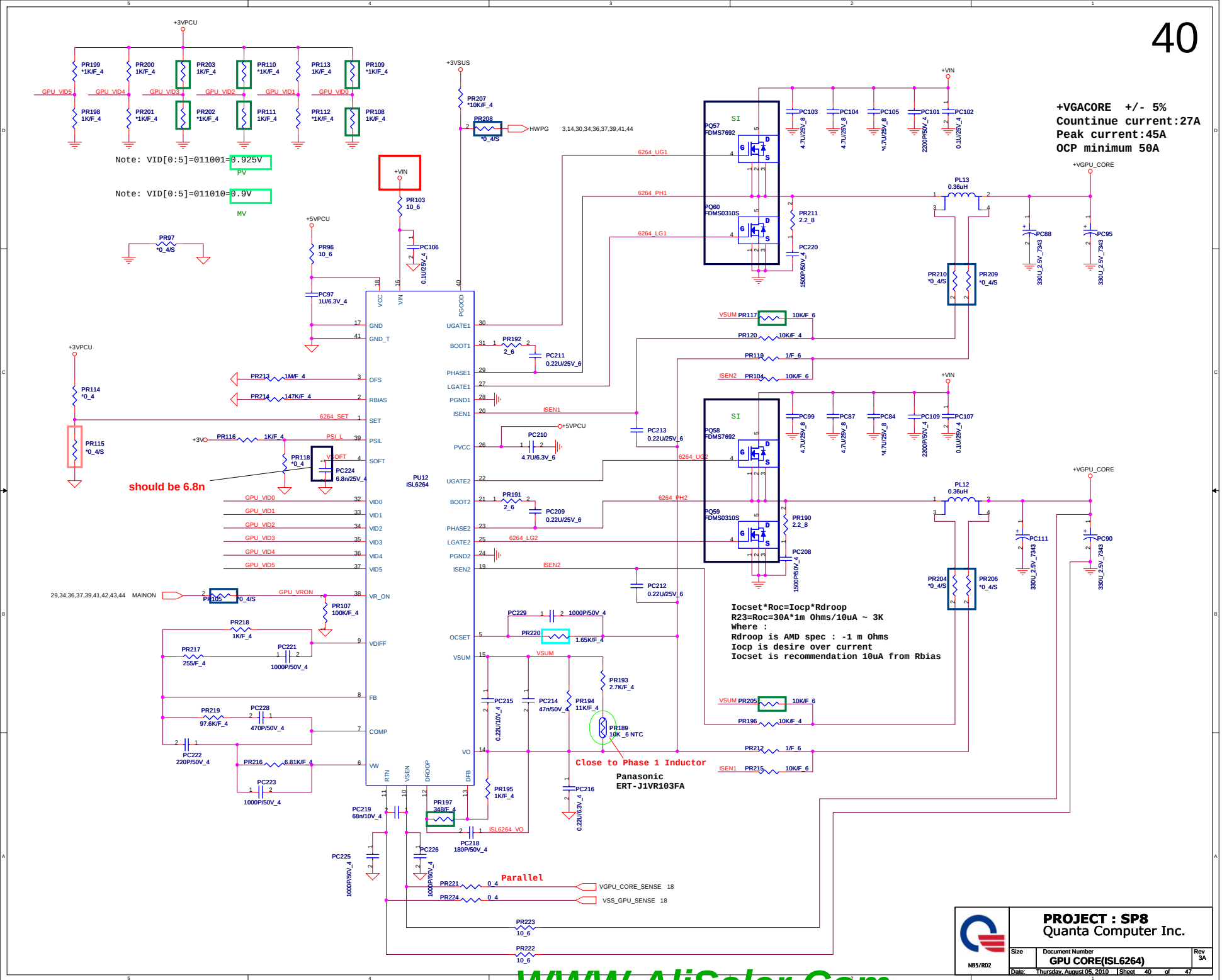

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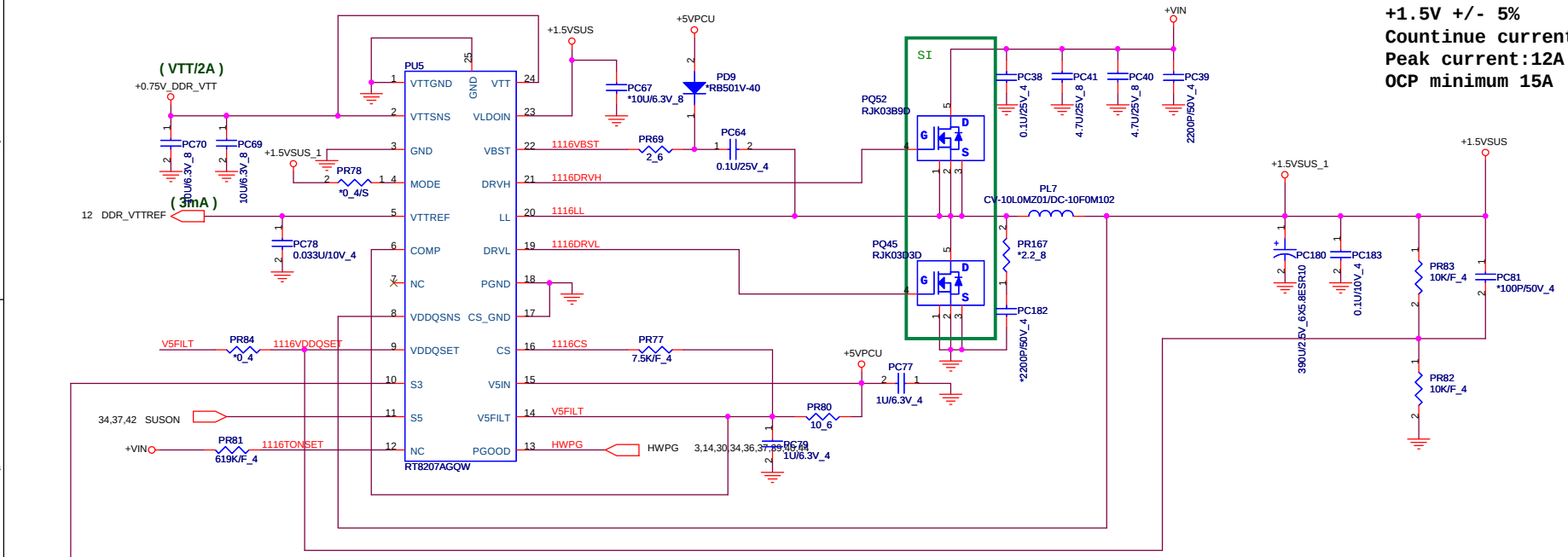
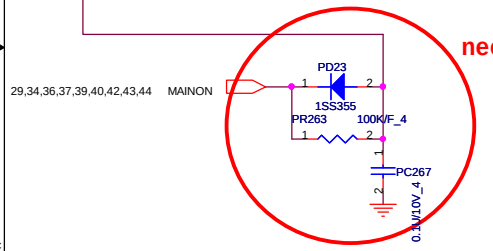
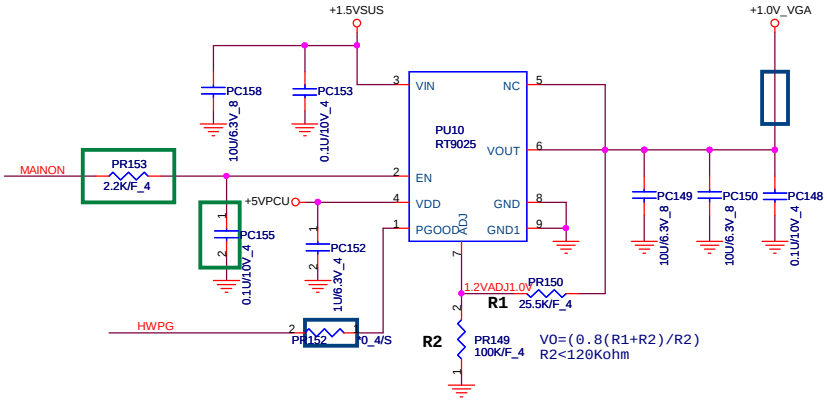
+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A



need to stuff for S3 and PR263 change to 100K



+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A



PROJECT : SP8
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	DDR3 (RT8207)	3A

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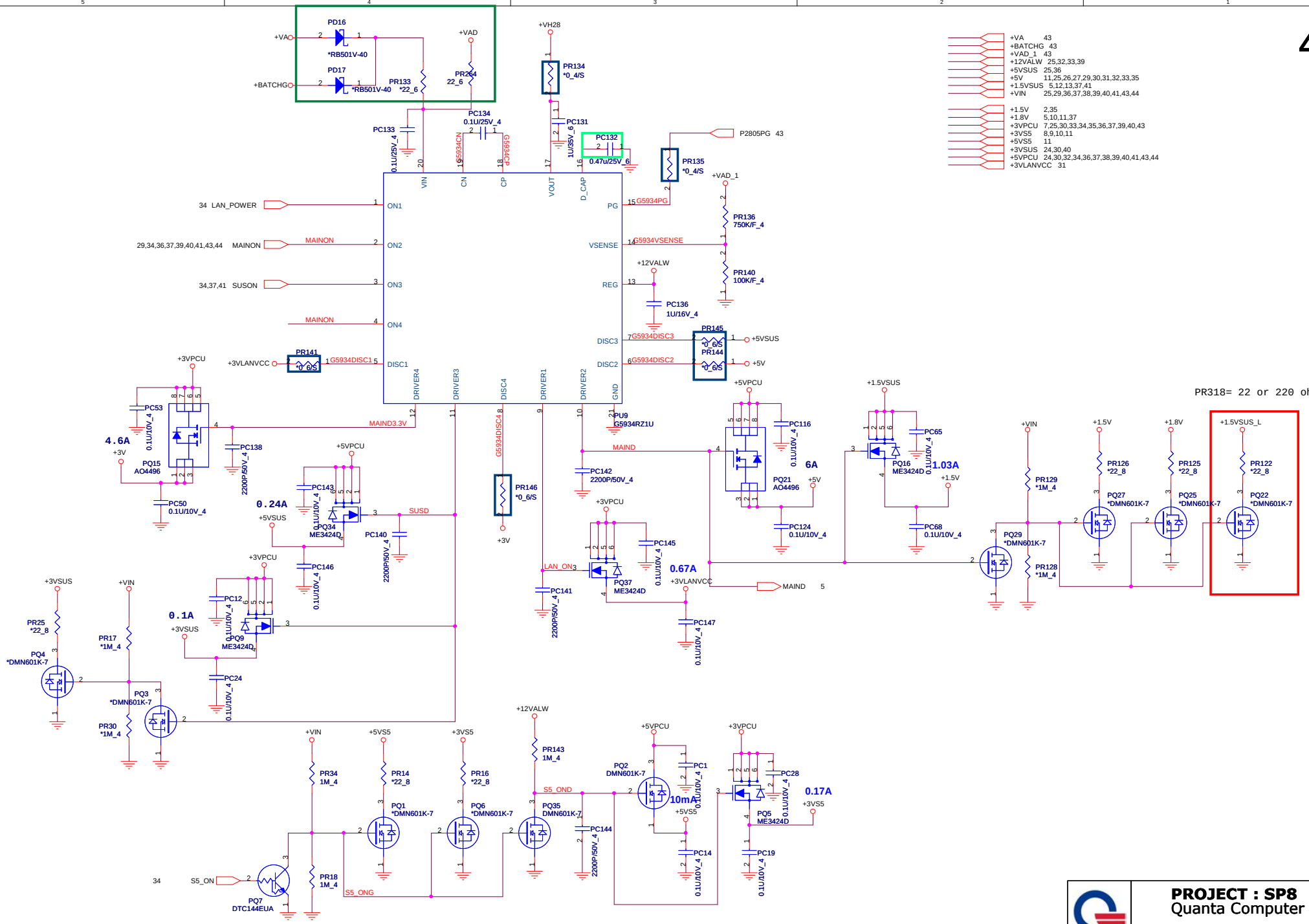

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (P2806)	3A

NB5/RD2

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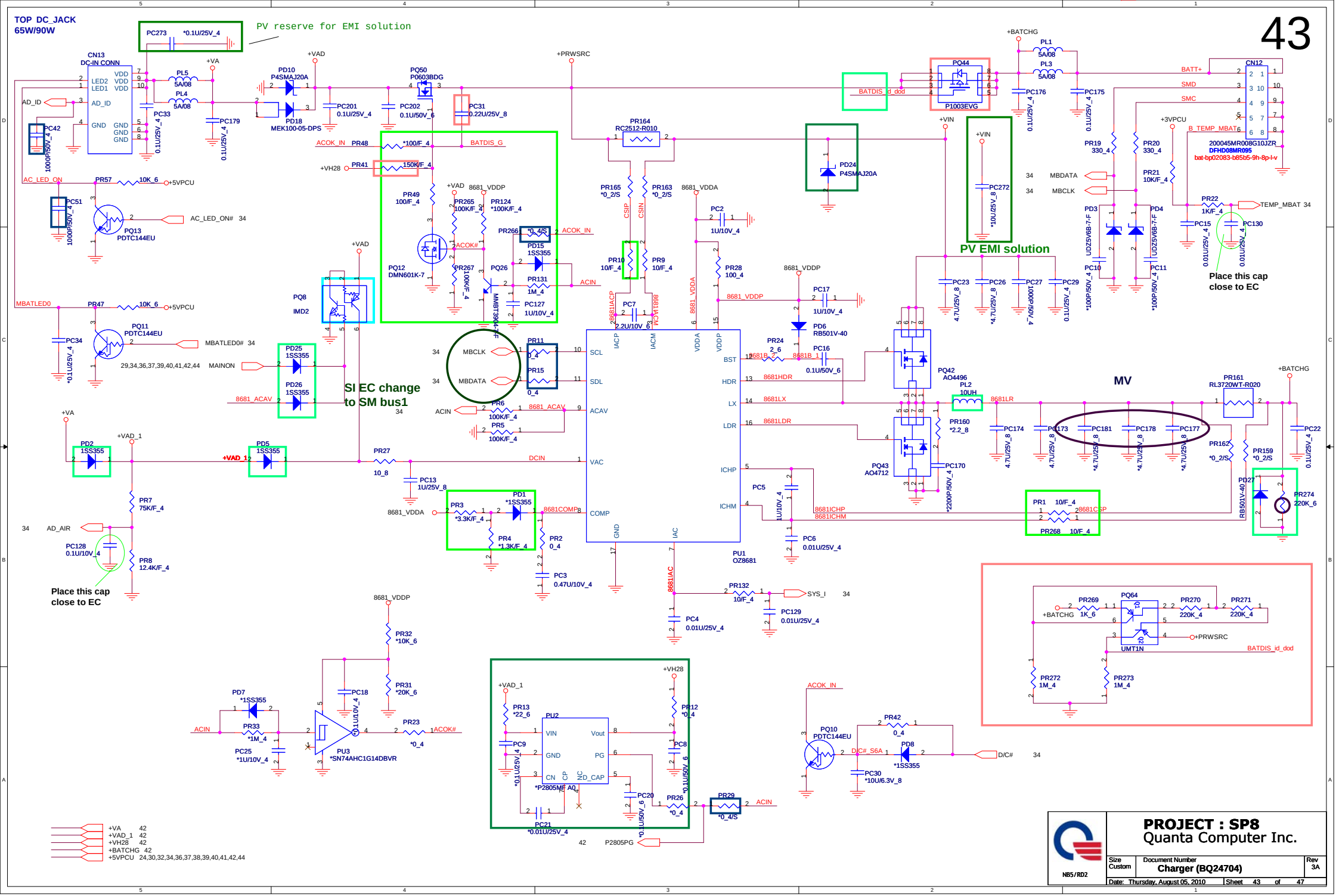

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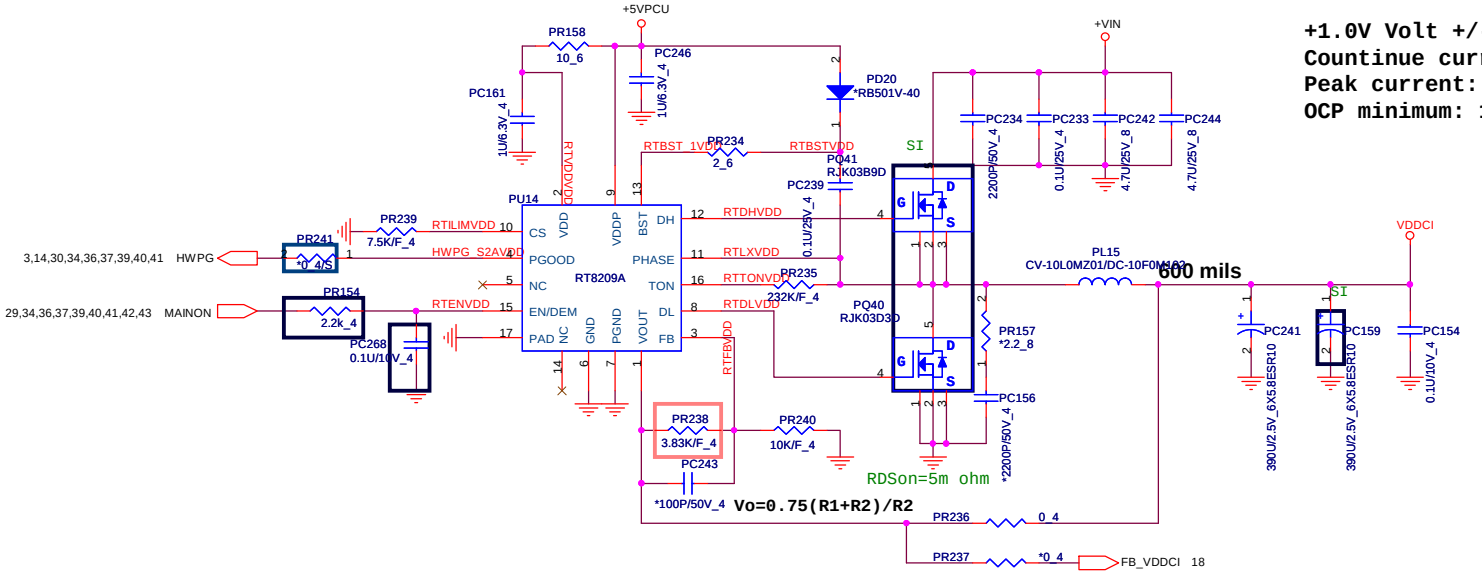
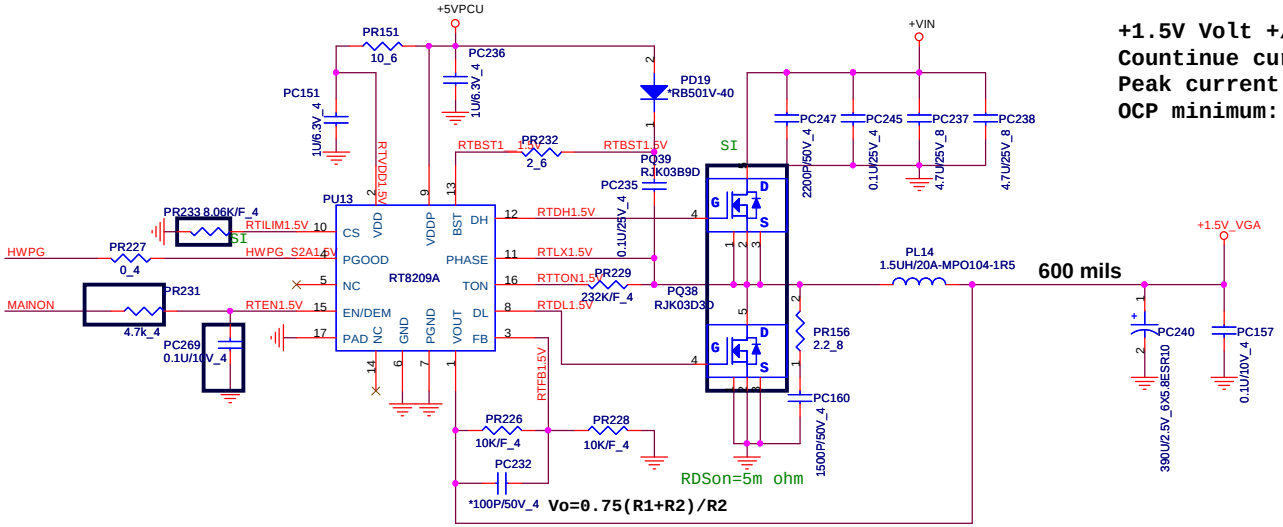


+1.0V Volt +/- 5%
Countinue current:9A
Peak current: 12A
OCP minimum: 15A



+1.5V Volt +/- 5%
Countinue current:9A
Peak current:12A
OCP minimum: 15A

NB5/RD2	**PROJECT : SP8** Quanta Computer Inc.	
Size Custom	Document Number **VGA Core/+1.8VGFX/1.0VGFX**	Rev 3A
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