SP7(Nikita) BLOCK DIAGRAM PV

01

PCB STACK UP

12L Dis.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : IN3(High)
LAYER 7 : SVCC1
LAYER 8 : SVCC2
LAYER 9 : IN4
LAYER10 : IN5(High)
LAYER11 : GND
LAYER12 : BOT

A Channel
DDR3-SODIMM1
DDR3-SODIMM2
PAGE 13,14

DDR3 800,1066,1333 MT/s

B Channel
DDR3-SODIMM3
DDR3-SODIMM4
PAGE 15,16

DDR3 800,1066,1333 MT/s

Intel Clarksfield
CPU 45Watt
4 Core
(rPGA 989)
PAGE 3-6

PCI-Express Gen2 X8

VRAM DDR3*8 (1Gb) PAGE 23-24

ATI M97/Broadway/Madison (128bit)
(FCBGA)
962p 29X29mm
PAGE 18-22

Dual Channel LVDS

HDMI CON (1920*1200) PAGE 25

LCD CONN for dual channel (15.6") PAGE 25

PCI-Express Gen2 X1

USB3.0 Port x2 PAGE 26

NEC USB3.0 Controller PAGE 26

DMI*4

BCLK133M
DMI100M
DP120M

32.768KHz

27MHz

14.318MHz

PCH 3.5Watt
Platform Controller Hub
PAGE 7-12

100M PCIE
133M BCLK
100M PCIE
96M DOT
REF CLK

CLOCK GEN 9LRS3197 PAGE 02

Braiwood (NAND Flash Memory) PAGE 34

ONFI

CPU THERMAL SENSOR PAGE 27

32.768KHz

SATA 2.5" HDD
SATA 1.8" SSD1
PAGE 30

SATA0 150MB

SATA 1.8" SSD2 PAGE 30

SATA1 150MB

E-SATA(USB2.0) PAGE 26

SATA2 150MB

USB2.0 48M

6,7 USB2.0 Port X2 PAGE 26

5 BlueTooth PAGE 31

4 Webcam w/ Mic PAGE 31

3

2 Card Reader
Realtek
RTS5159
PAGE 30

SMBUS

Accelerometer
LIS3LV02DL PAGE 31

32.768KHz

LPC

PCI-E 100M

Azalia

Keyboard Touch Pad
Light Sensor
PAGE 31

GMT G9931P1U
SYSTEM/VGA FAN
PAGE 27

SPI
(SYSTEM BIOS)
PAGE 33

ENE KBC
KB3926 C2
PAGE 33

Audio
IDT92HD75B2
PAGE 28

X1 **LAN**
Atheros
PCIE-LAN
AR8131(M)
GigaLAN
PAGE 32

25MHz

RJ45
PAGE 32

X1 half size mini-card
(Wireless LAN
Shirley Peak
802.11a/b/g/n)
PAGE 34

2-in-1 flash media slot(SD/MMC)
PAGE 30

AUDIO Amplifier TPA6047A4
PAGE 29

Internal Micophones (MEMs)
PAGE 31

Combo Jack (Headphone/MIC)
PAGE 28

Jack to Speaker
PAGE 29

BATTERY SELECTOR PAGE 42
SYSTEM CHARGER(BQ24704) PAGE 41
SYSTEM POWER ISL6237IRZ-T PAGE 35
DDR III SMDDR_VTERM 1.8V/1.8VSUS(VT356/VT357) PAGE 39
VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 36
VGACORE RT8208 PAGE 38
CPU CORE VT1312M/VT1317 PAGE 37

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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02

U31

9LRS3197

QFN32

ICS9LRS3197AKLFT

IDT/ICS

Place the 33 ohm resistors close to the CK 505

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

M/B Screw Hole

Close hole

Close hole

SI2 0413 chage hole pad for HP request

MINI CARD

MINI CARD

SI 0223 change footprint

SI2 0413 change BOM

CPU Thermal hole

CPU Thermal hole

PV 0605 MODIFY PV 0605 MODIFY

SPAD

PV-2 0702 MODIFY

2nd Battery Hole

PV 0605 MODIFY

2nd Battery Hole

VGA Thermal hole

VGA Thermal hole

HDD Board Hole

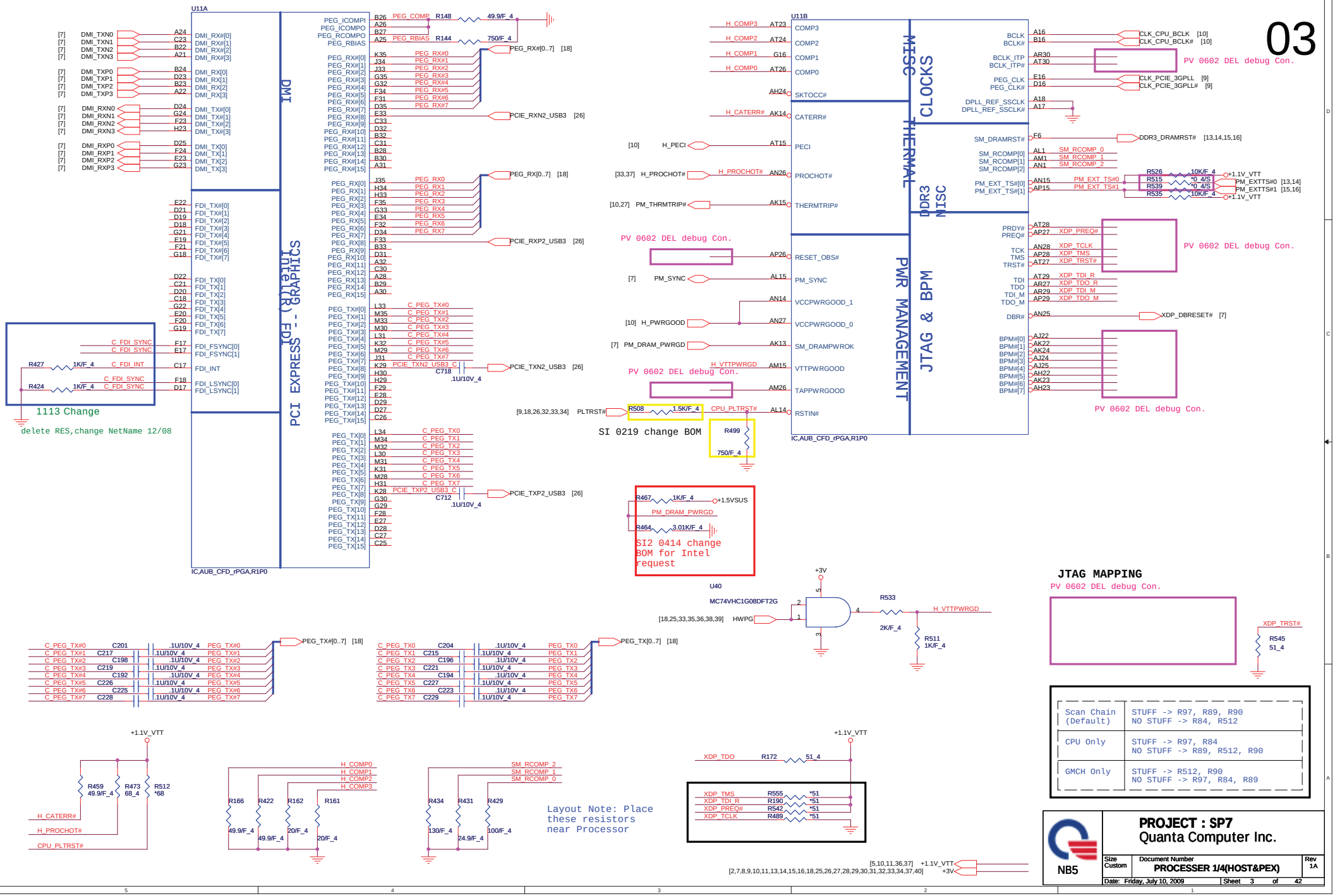
HDD hole

PROJECT : SP7
Quanta Computer Inc.

NB5

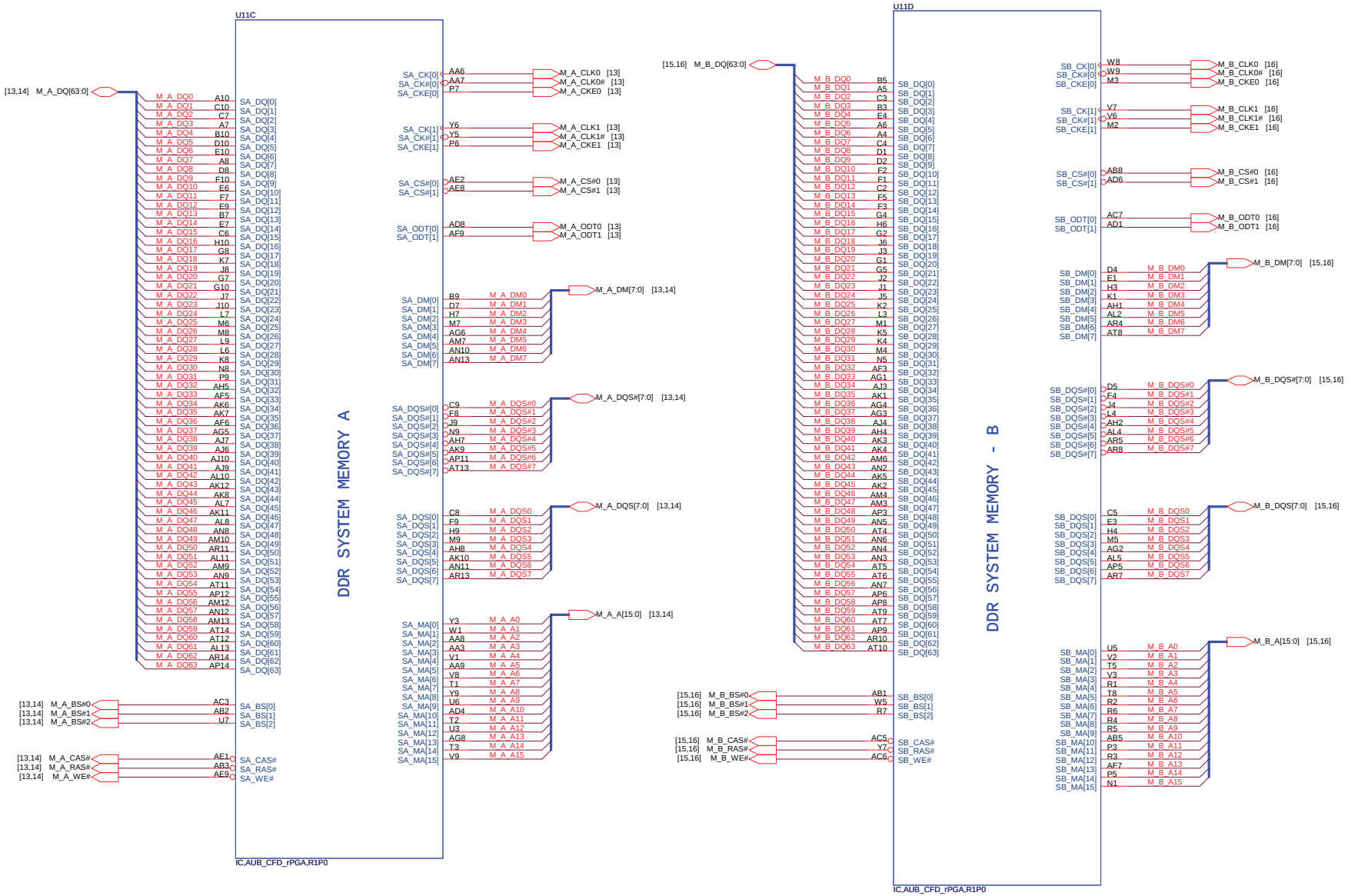
Size: Custom | Document Number: CLOCK & Screw Holes | Rev: 1A

Date: Friday, July 10, 2009 | Sheet 2 of 42

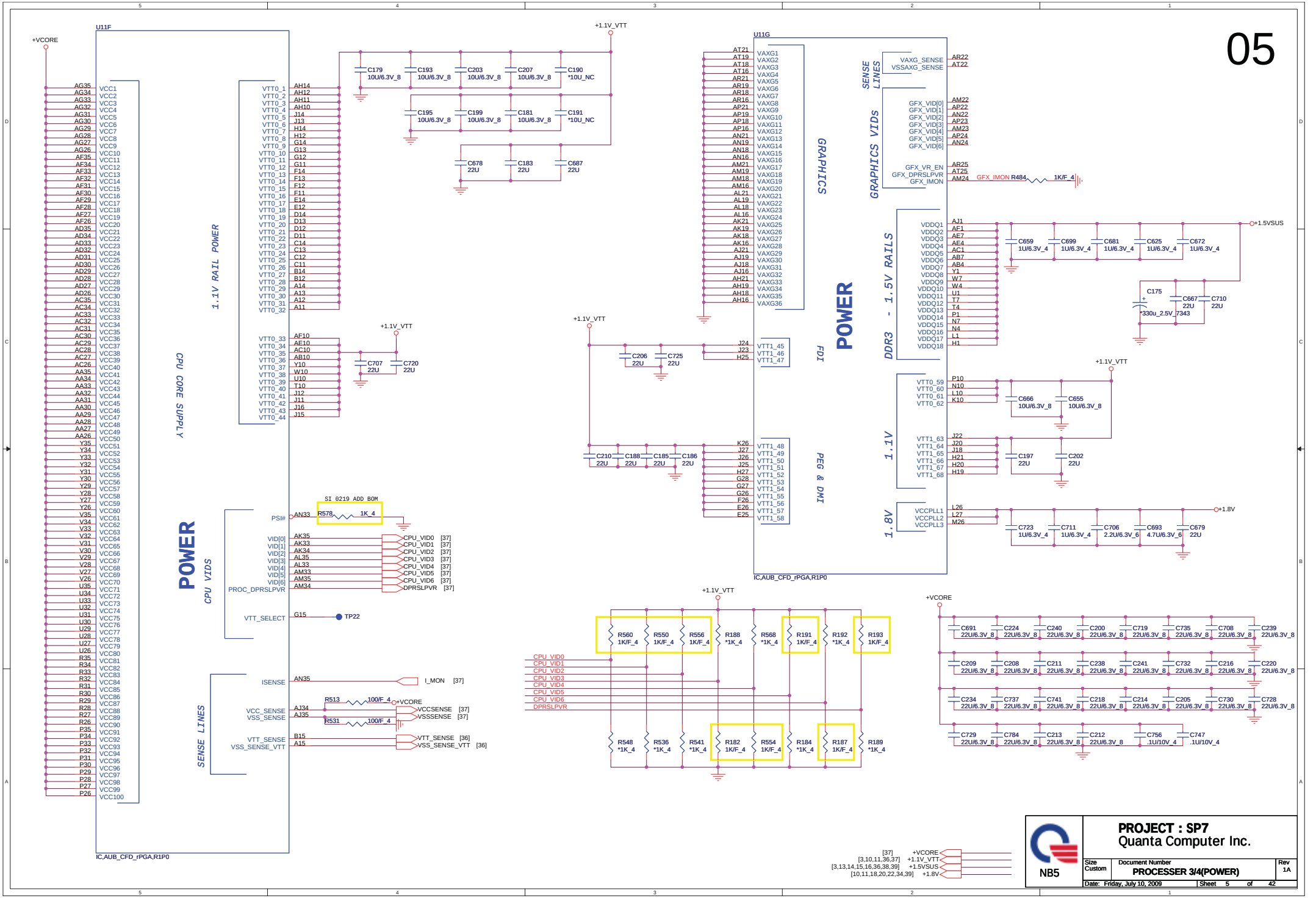


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

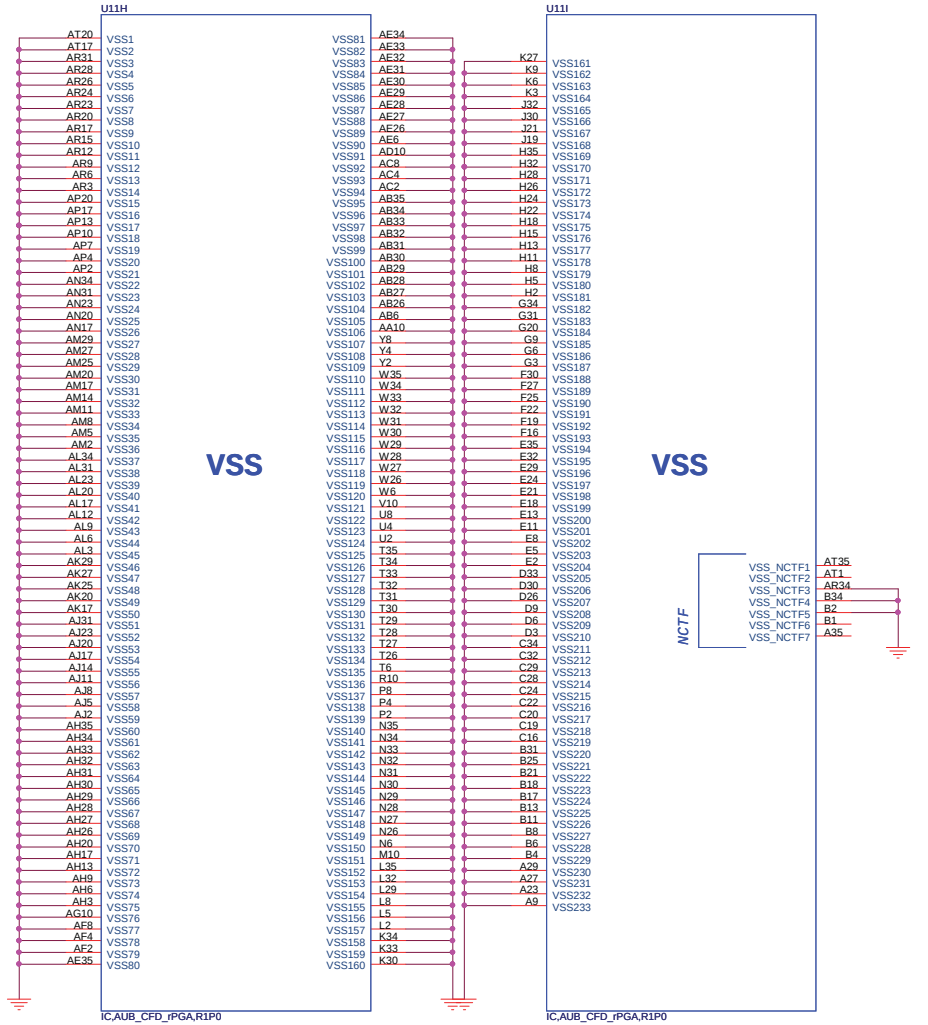
04



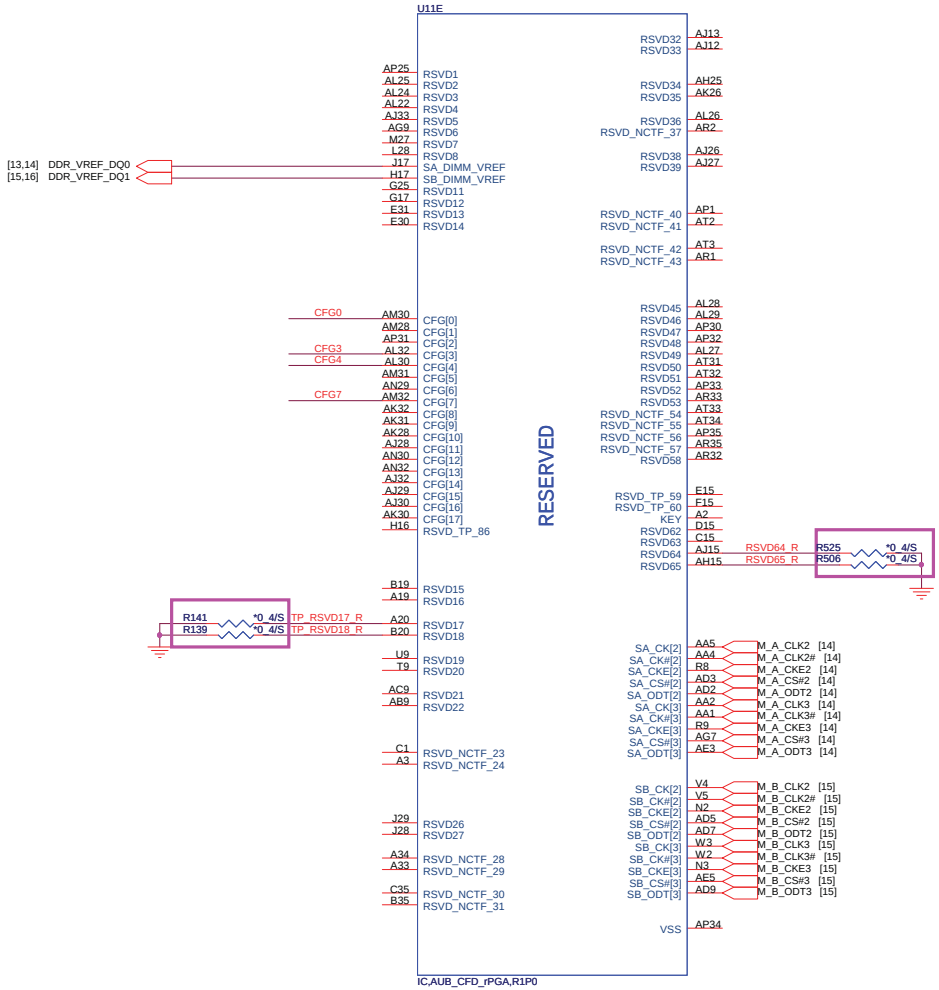
PROJECT : SP7	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: PROCESSER 2/4(DDR); Rev: 1A
Date: Friday, July 10, 2009	Sheet 4 of 42


05
U11F
U11G
+VCORE
+1.1V_VTT
+1.5VSUS
+1.8V
1.1V RAIL POWER
CPU CORE SUPPLY
CPU VIDS
SENSE LINES
GRAPHICS
GRAPHICS VIDS
DDR3 - 1.5V RAILS
FDI
PEG & DMI
1.1V
1.8V
POWER
SI 0219 ADD BOM
IC,AUB_CFD_rPGA,R1P0
PROJECT : SP7
Quanta Computer Inc.
PROCESSER 3/4(POWER)
NB5
Date: Friday, July 10, 2009
Sheet 5 of 42
WWW.AliSaler.Com

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



06

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

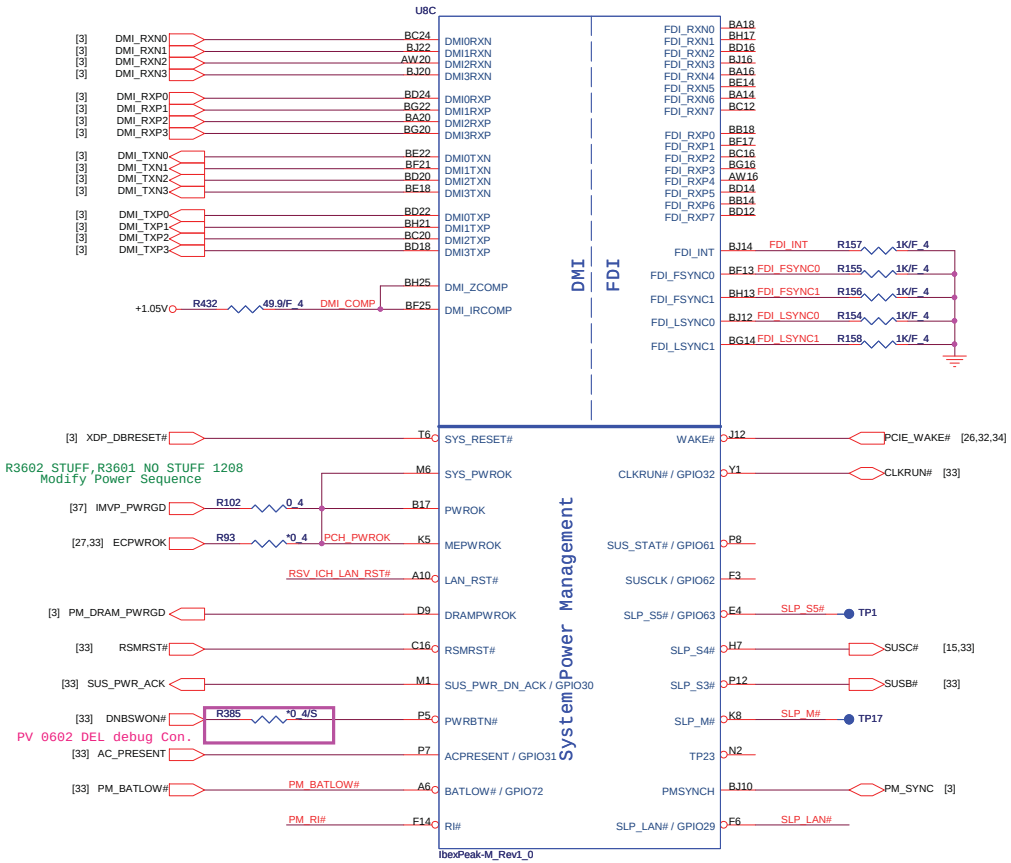
NB5

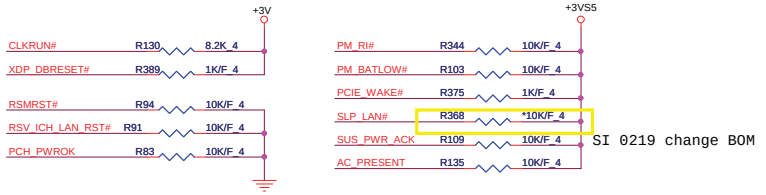
PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

Date: Friday, July 10, 2009 Sheet 6 of 42

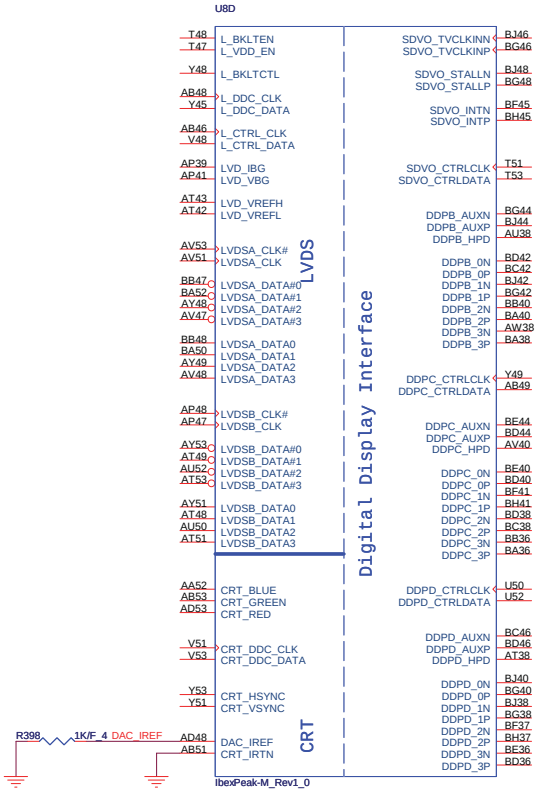
IBEX PEAK-M (DMI,FDI,GPIO)





SI 0219 change BOM

IBEX PEAK-M (LVDS,DDI)



[2,8,9,11,26,27,36,37] +1.05V
[2,3,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[9,10,11,25,40] +3VS5

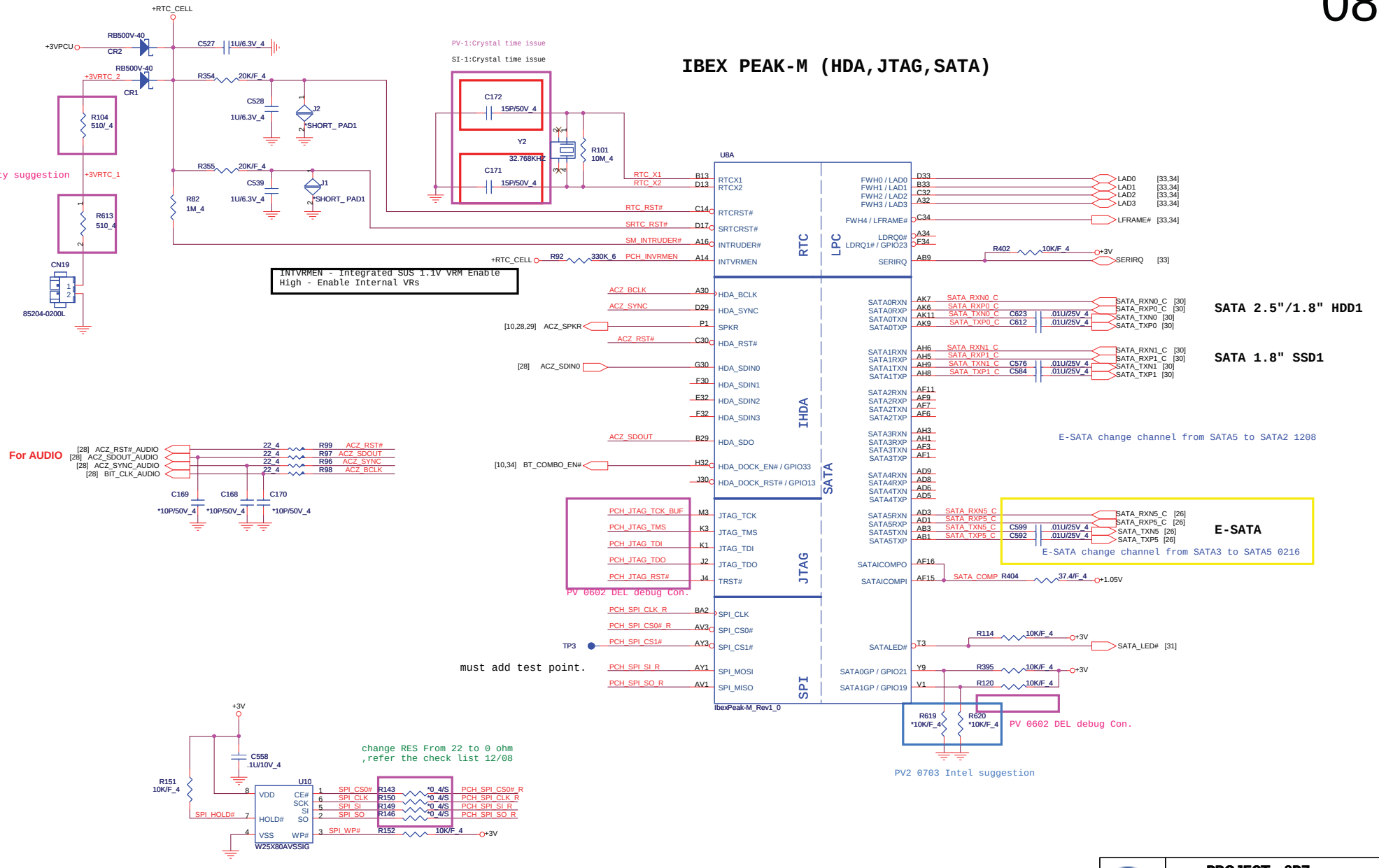
NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI,PM,VIDEO)	1A

Date: Friday, July 10, 2009 | Sheet 7 of 42

IBEX PEAK-M (HDA,JTAG,SATA)

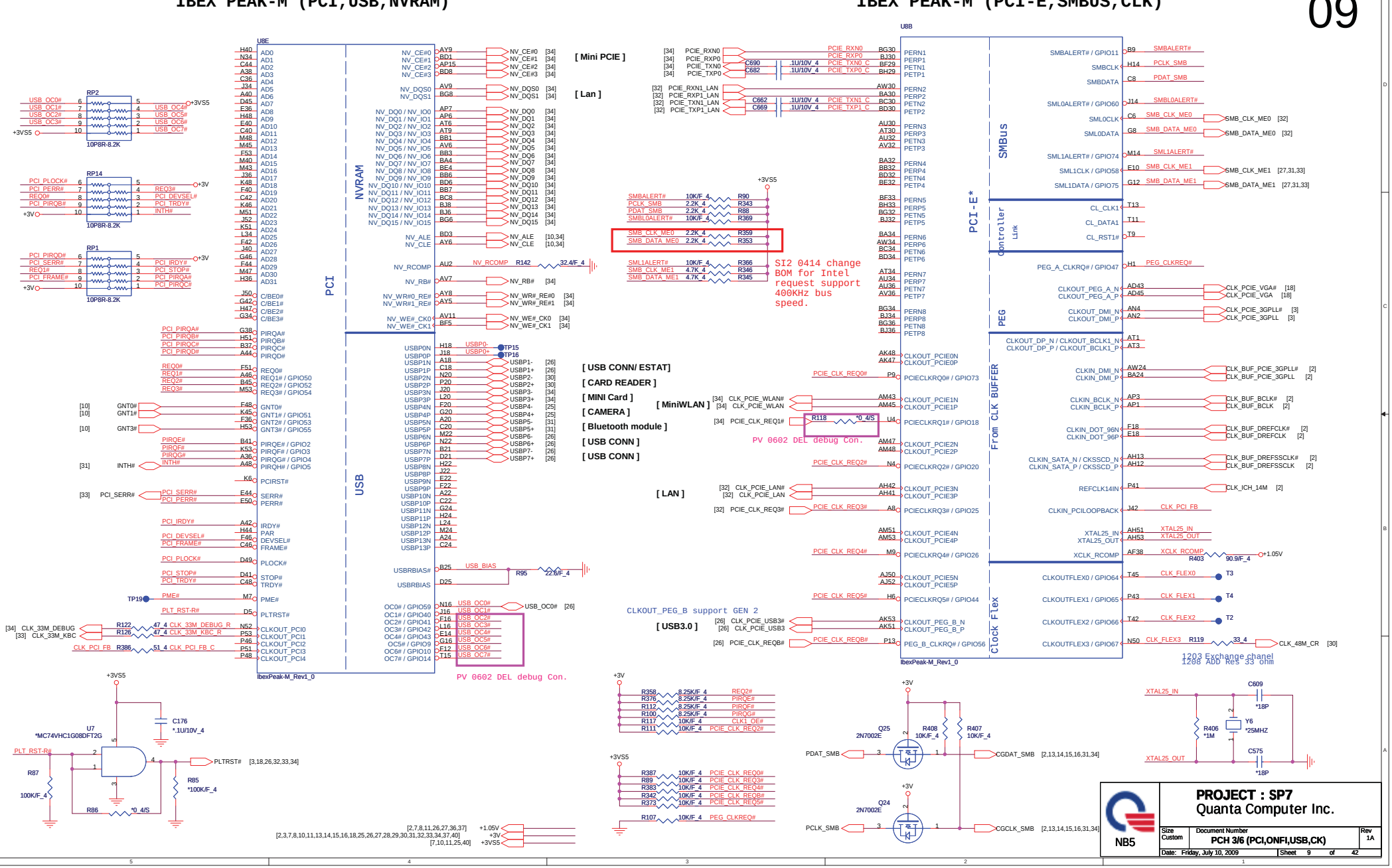


NB5	PROJECT : SP7 Quanta Computer Inc.	
	Size: Custom Document Number: PCH 2/6 (SATA,HDA,LPC)	Rev: 1A
	Date: Friday, July 10, 2009	Sheet 8 of 42

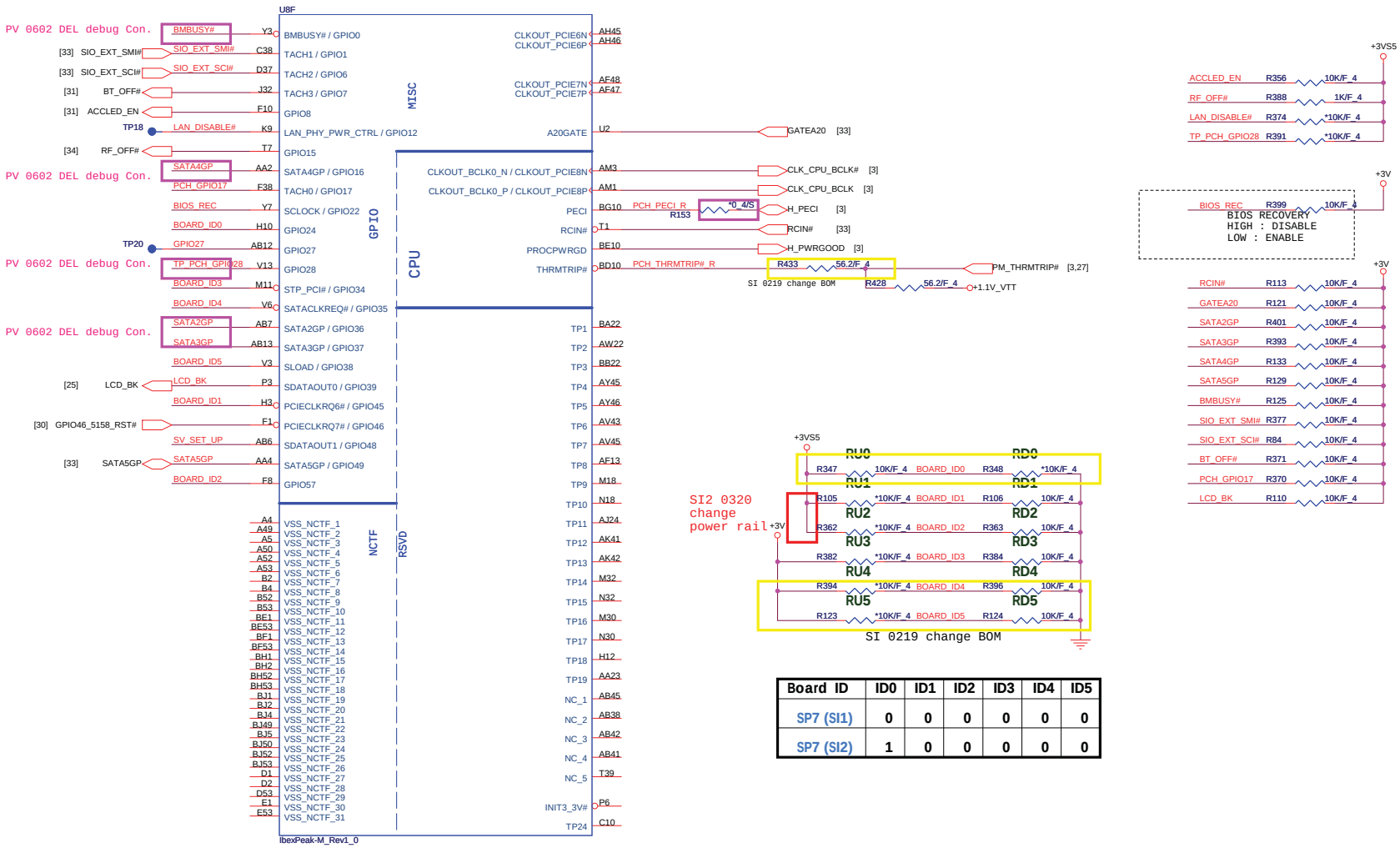
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

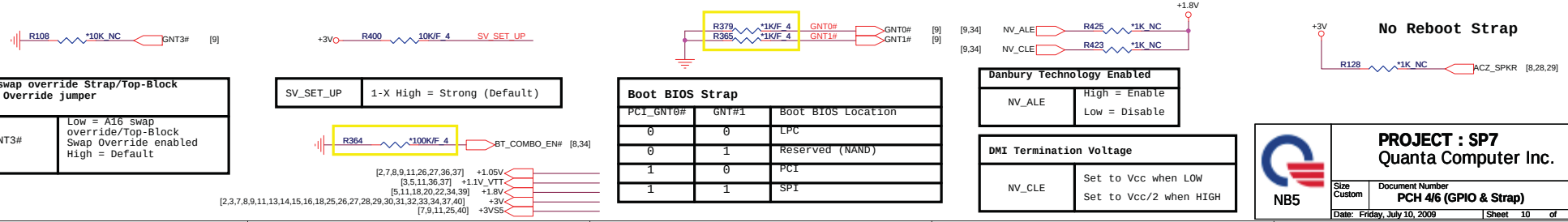
09



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



Board ID	ID0	ID1	ID2	ID3	ID4	ID5
SP7 (SI1)	0	0	0	0	0	0
SP7 (SI2)	1	0	0	0	0	0



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP	1-X High = Strong (Default)

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

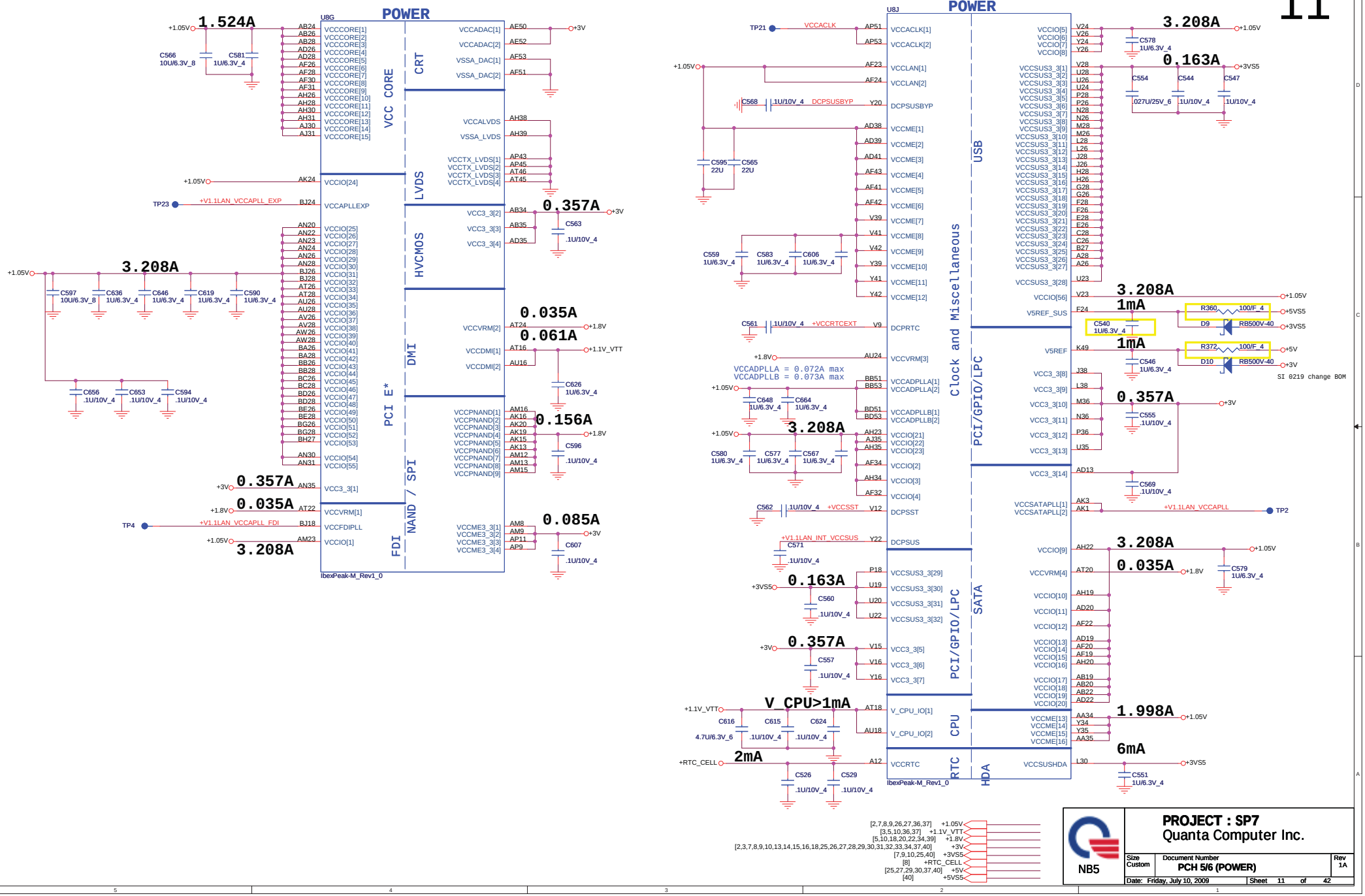
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

NB5

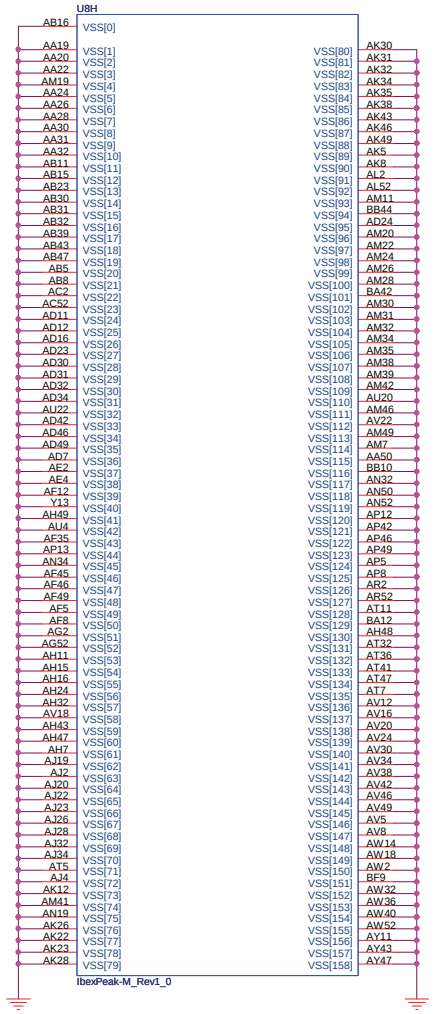
PROJECT : SP7
Quanta Computer Inc.

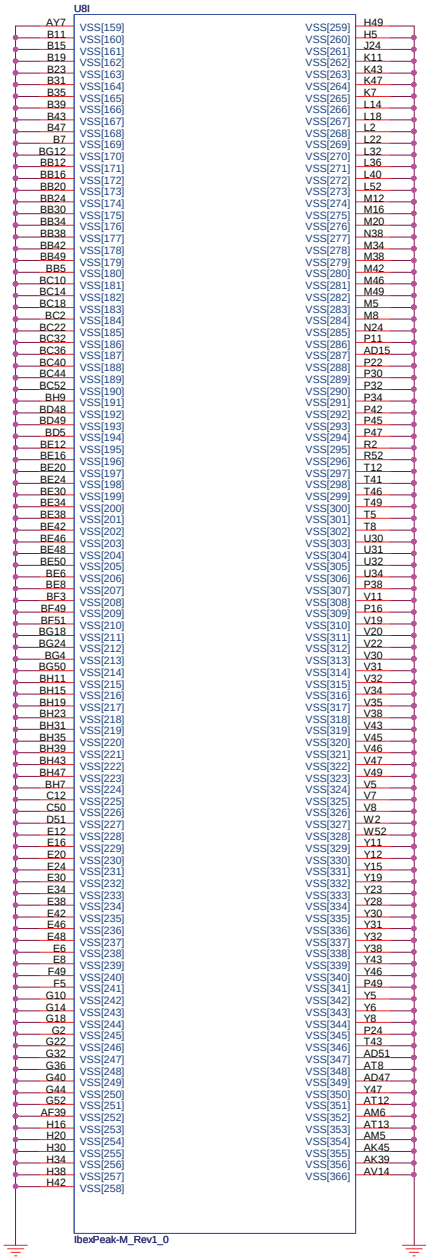
Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	1A

Date: Friday, July 10, 2009 Sheet 10 of 42



IBEX PEAK-M (GND)





Move to Page 37

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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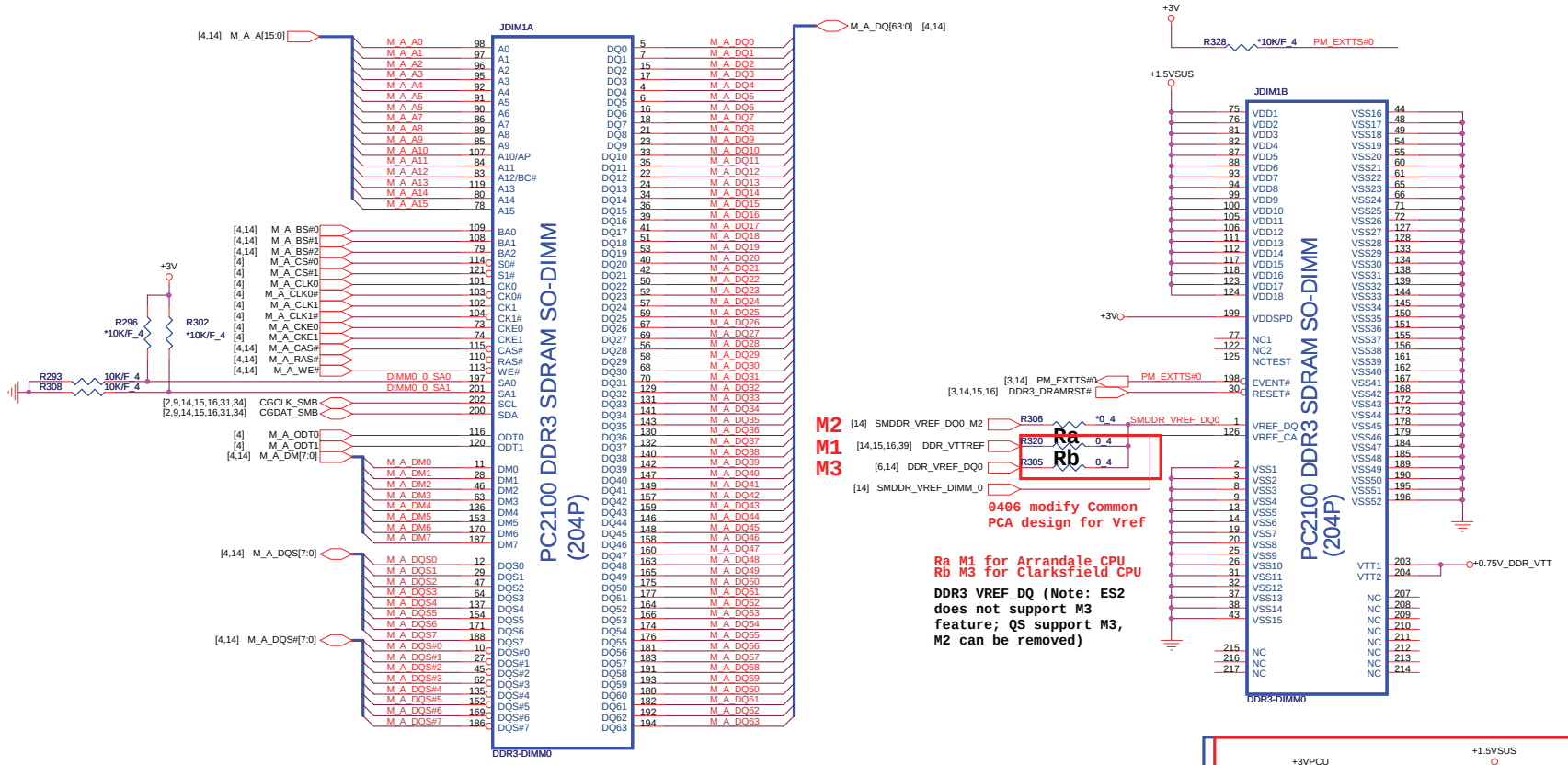
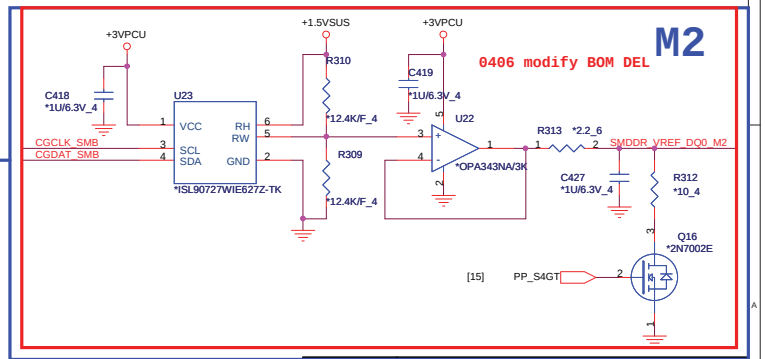
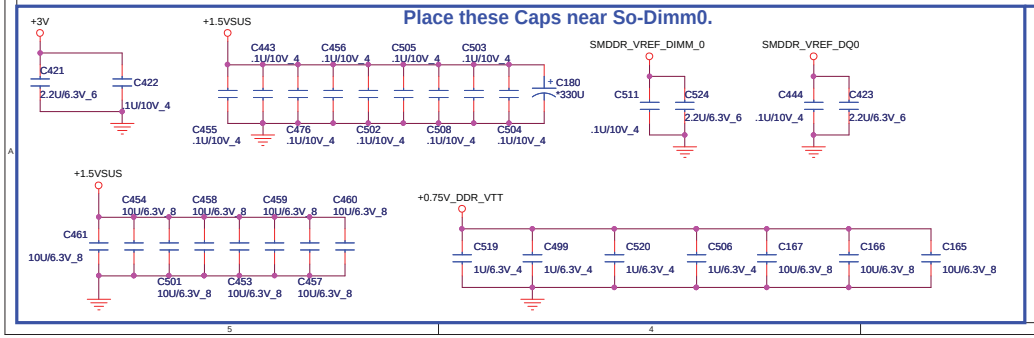
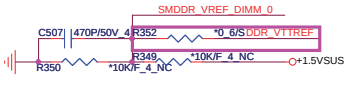
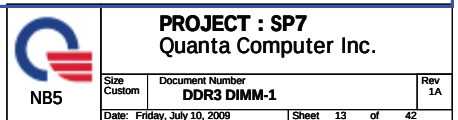
DDR3 -SODIMM 1 A0



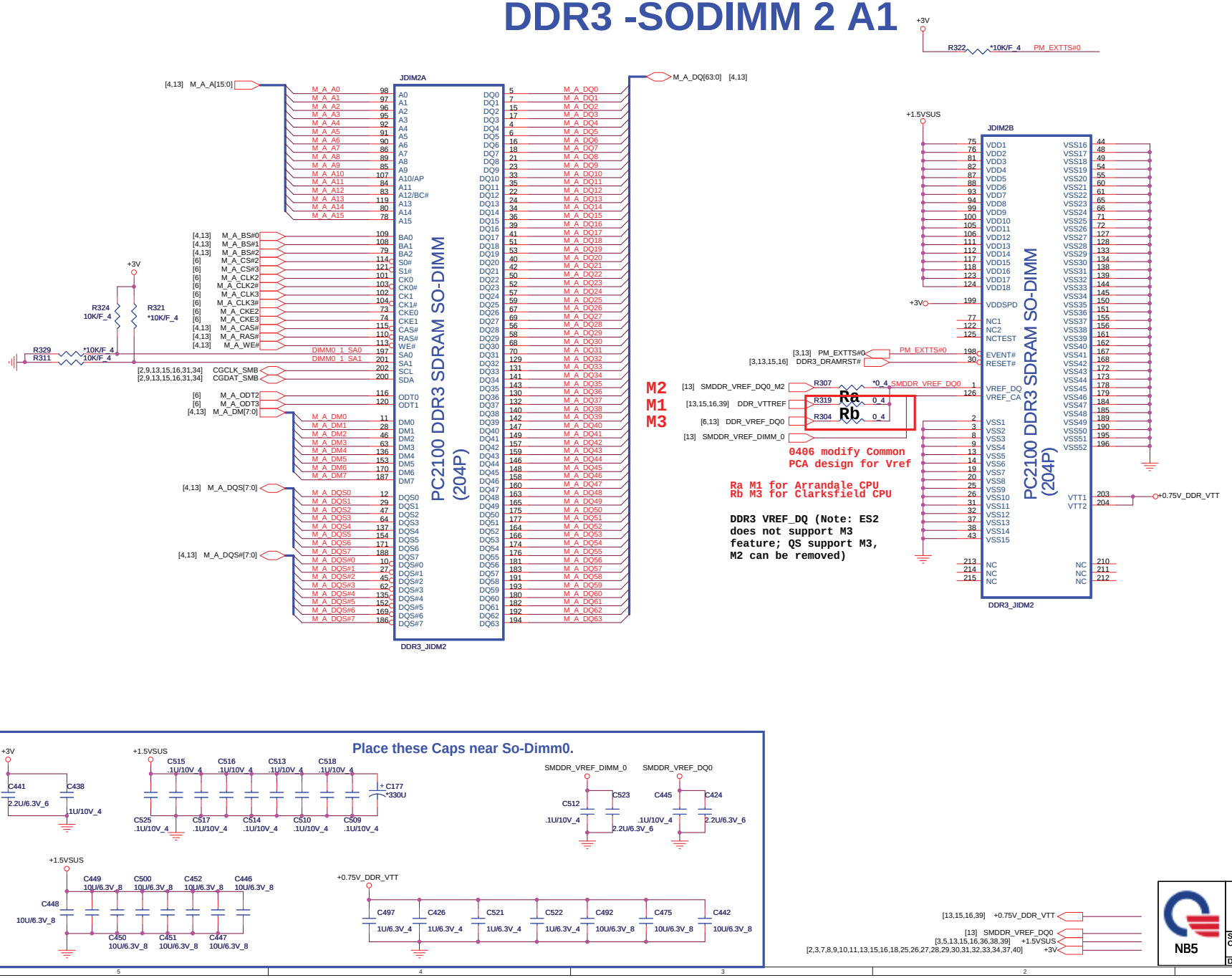






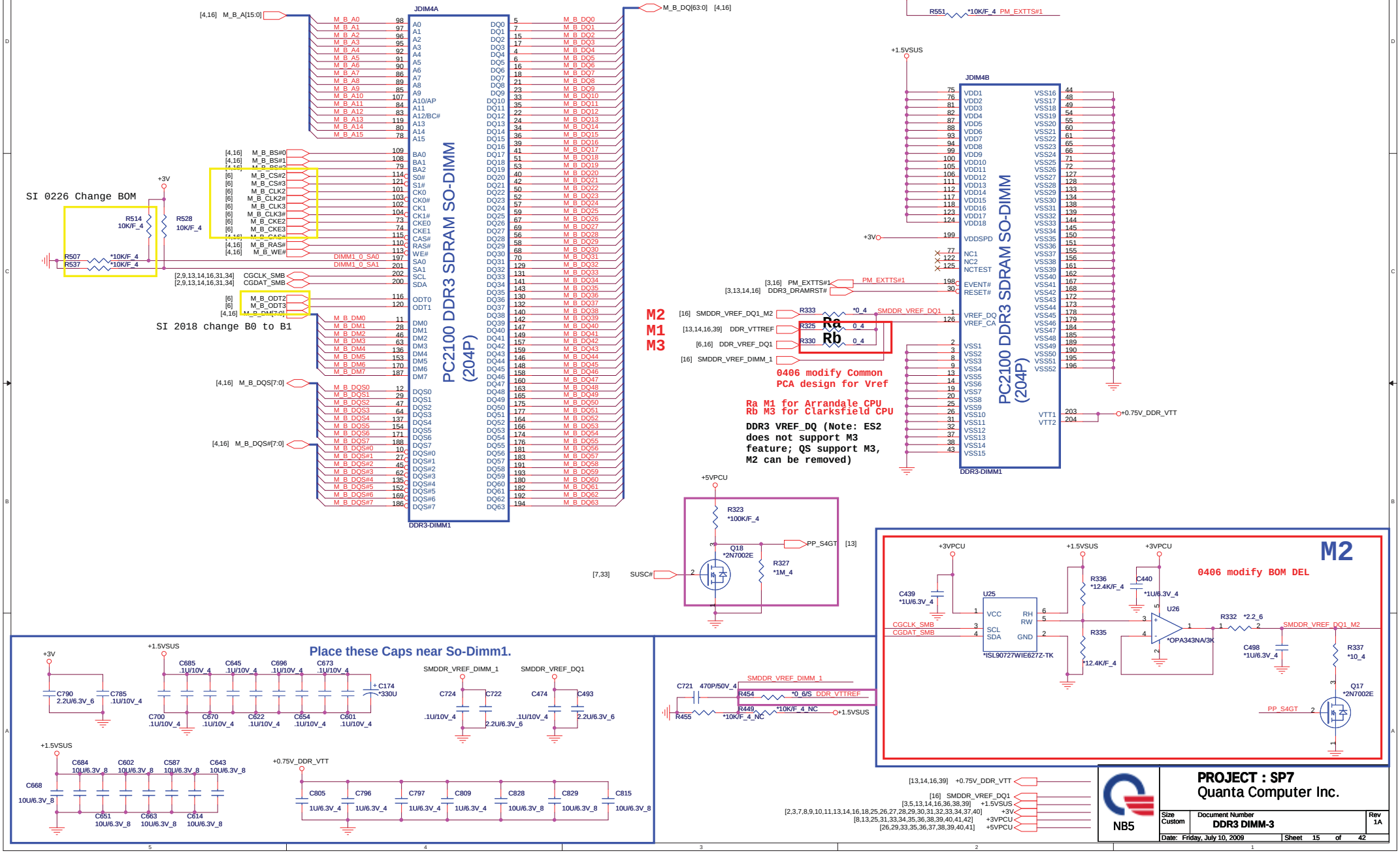


DDR3 -SODIMM 2 A1

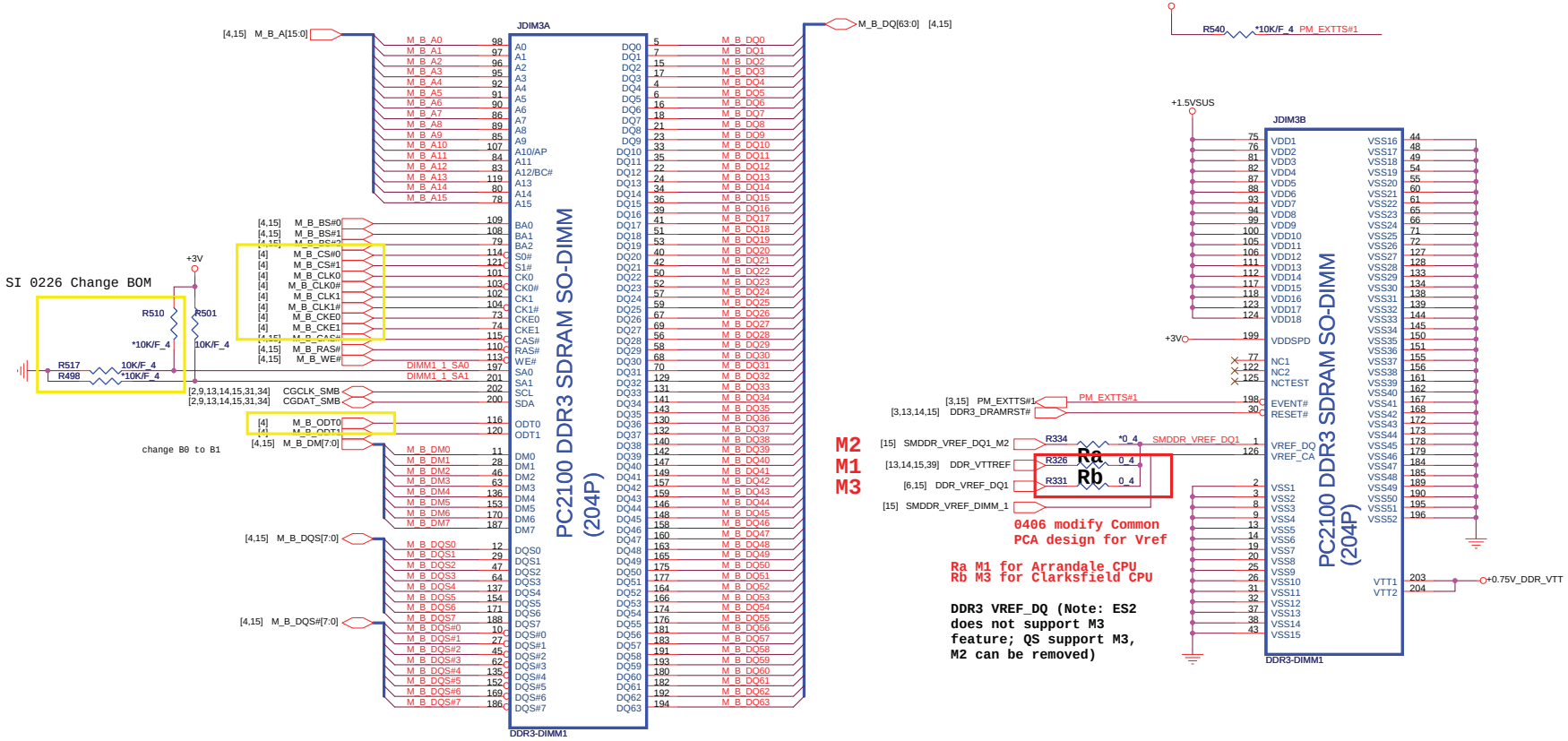


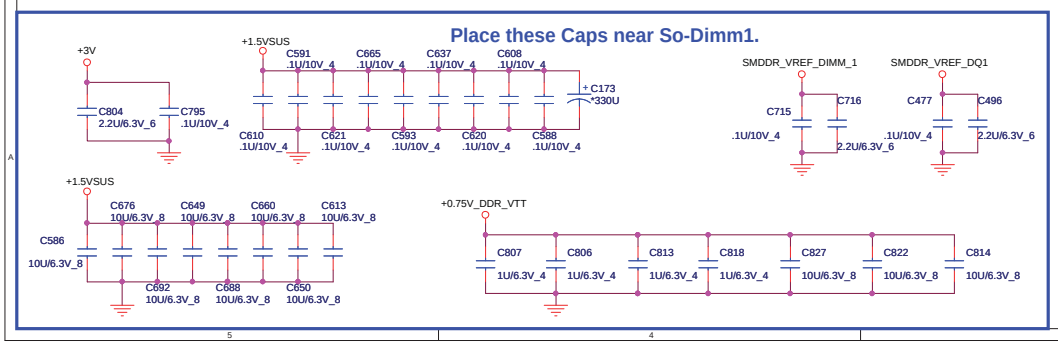
NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM-2	Rev: 1A
Date: Friday, July 10, 2009	Sheet 14 of 42	

DDR3 -SODIMM 3 B1



DDR3 -SODIMM 4 B0





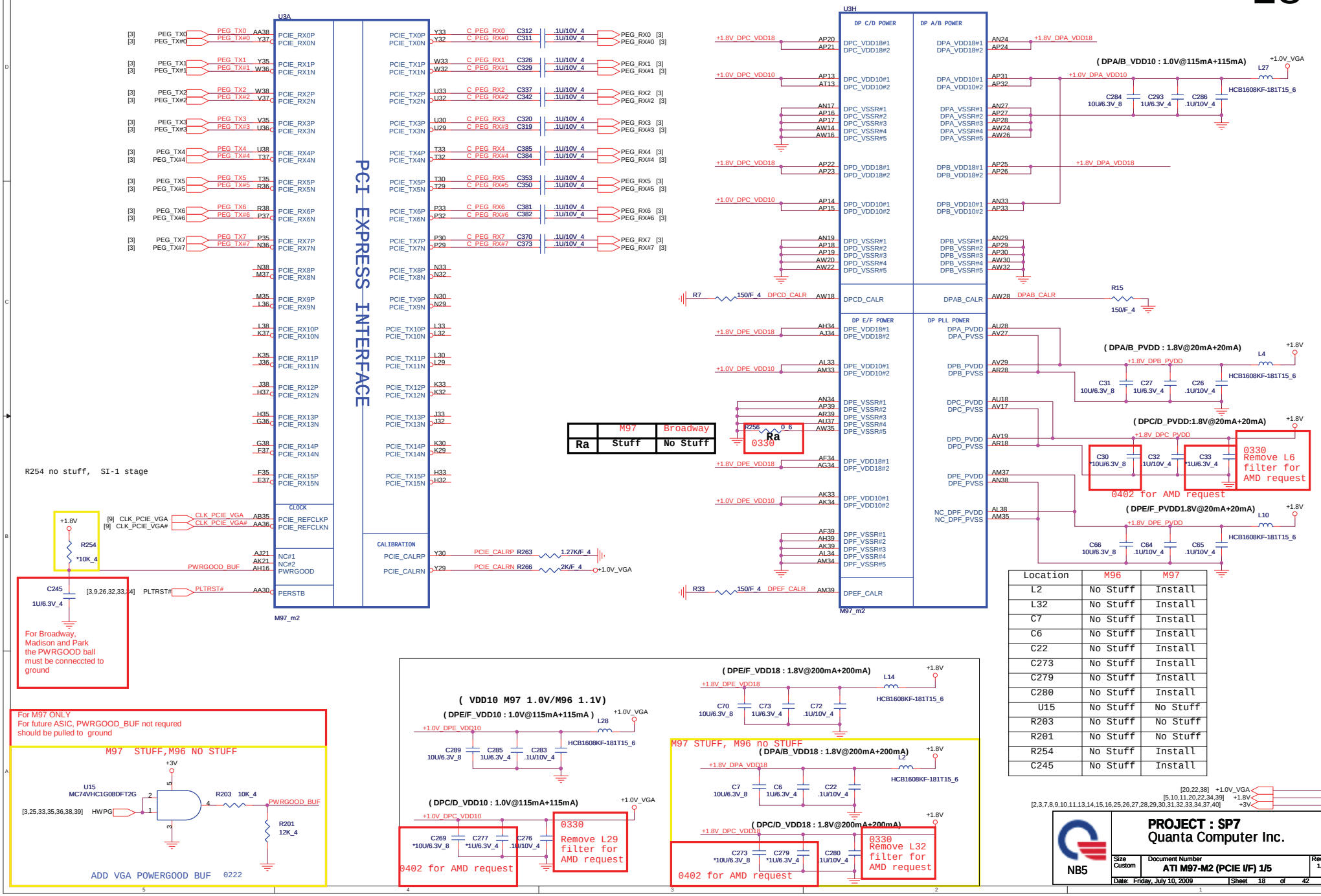
NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM-4	Rev: 1A
Date: Friday, July 10, 2009	Sheet 16 of 42	

[2,7,8,9,11,26,27,36,37] +1.05V
[3,5,10,11,36,37] +1.1V_VTT
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,9,10,11,25,40] +3VS5

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	XDP	1A
Date: Friday, July 10, 2009	Sheet 17 of 42	



	M97	Broadway
Ra	Stuff	No Stuff

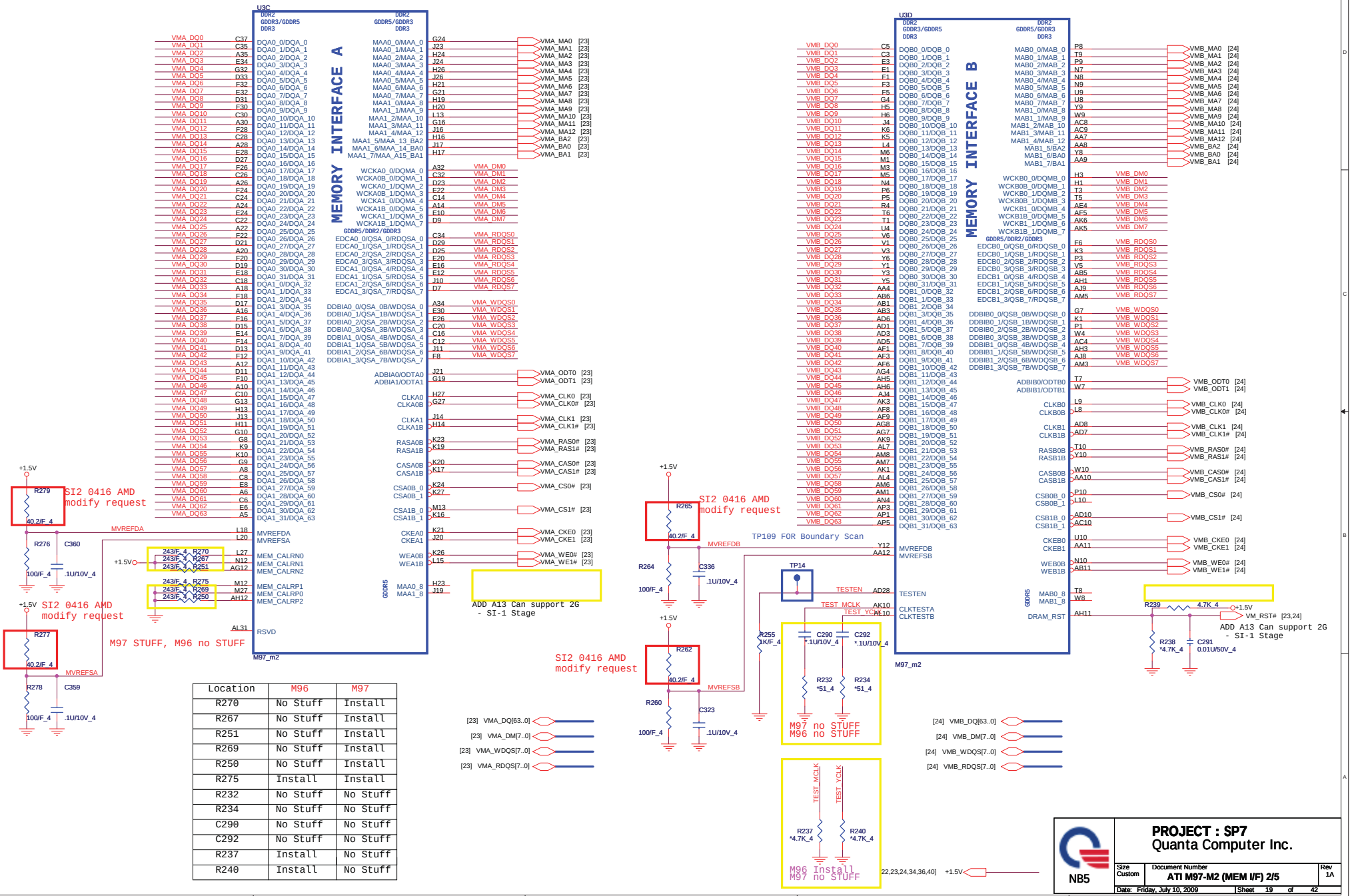
Location	M96	M97
L2	No Stuff	Install
L32	No Stuff	Install
C7	No Stuff	Install
C6	No Stuff	Install
C22	No Stuff	Install
C273	No Stuff	Install
C279	No Stuff	Install
C280	No Stuff	Install
U15	No Stuff	No Stuff
R203	No Stuff	No Stuff
R201	No Stuff	No Stuff
R254	No Stuff	Install
C245	No Stuff	Install

PROJECT : SP7
Quanta Computer Inc.

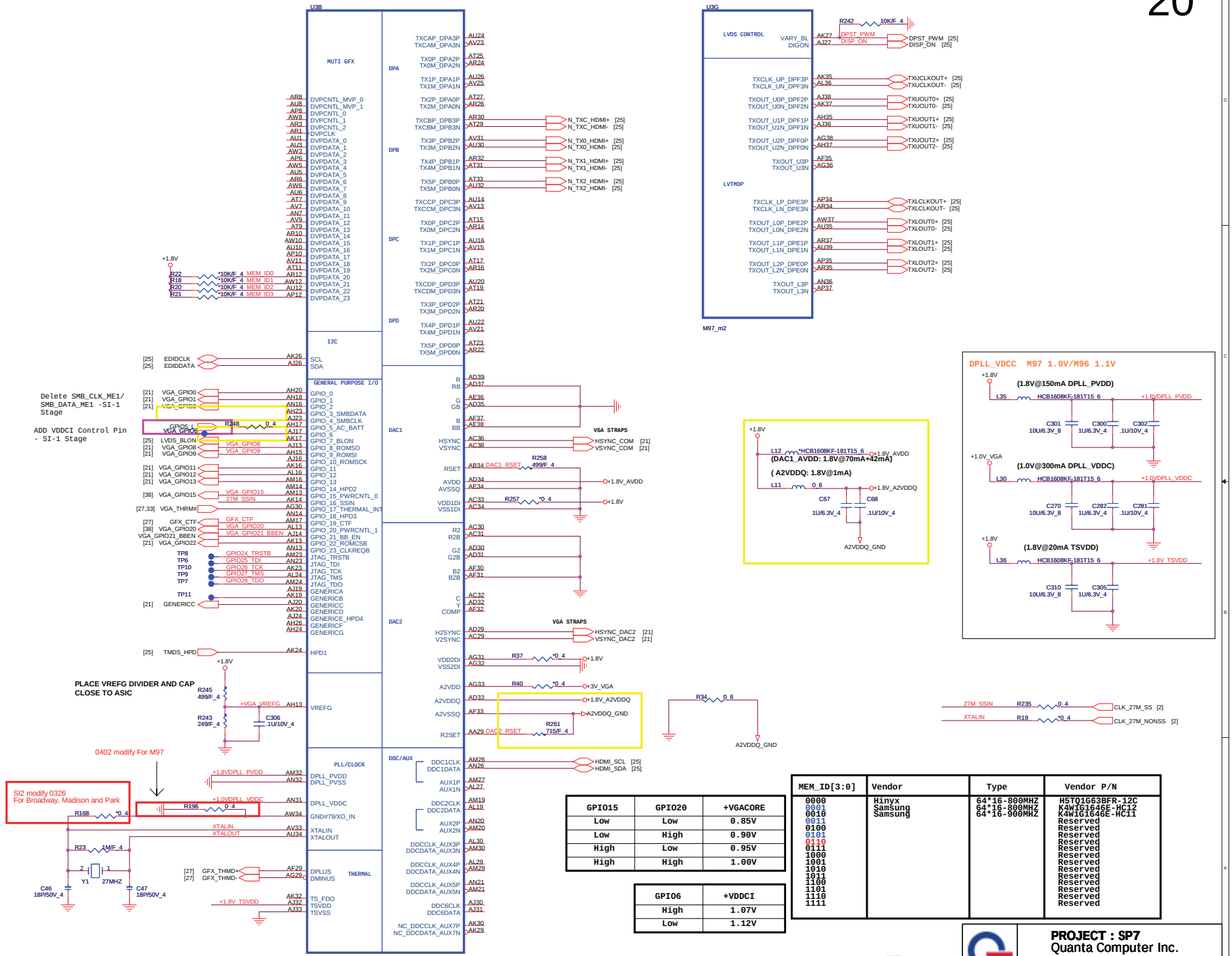
NB5

Size	Document Number	Rev
Custom	ATI M97-M2 (PCIE I/F) 1/5	1A

Date: Friday, July 10, 2009 | Sheet 18 of 42



Location	M96	M97
R270	No Stuff	Install
R267	No Stuff	Install
R251	No Stuff	Install
R269	No Stuff	Install
R250	No Stuff	Install
R275	Install	Install
R232	No Stuff	No Stuff
R234	No Stuff	No Stuff
C290	No Stuff	No Stuff
C292	No Stuff	No Stuff
R237	Install	No Stuff
R240	Install	No Stuff



GPIO15	GPIO20	+VGACORE
Low	Low	0.85V
Low	High	0.90V
High	Low	0.95V
High	High	1.00V

GPIO6	+VDDCI
High	1.07V
Low	1.12V

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hinyx	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0010	Samsung	64*16-900MHZ	K4W1G1646E-HC11
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

PROJECT : SP7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: ATI M97-M2 (DISPLAY) 3/5
Rev: 1A
Date: Friday, July 10, 2009
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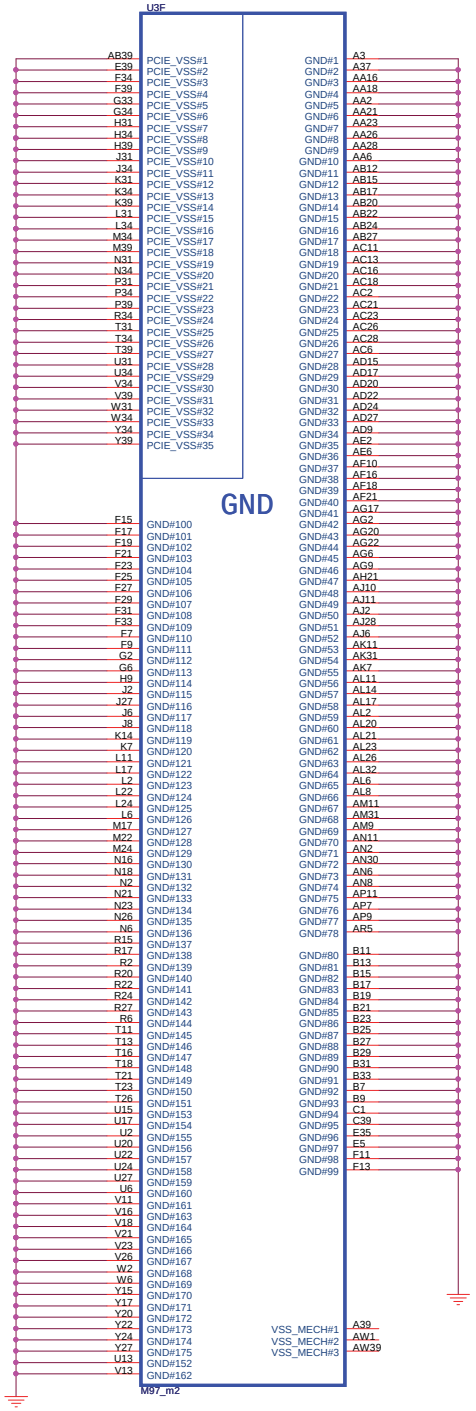
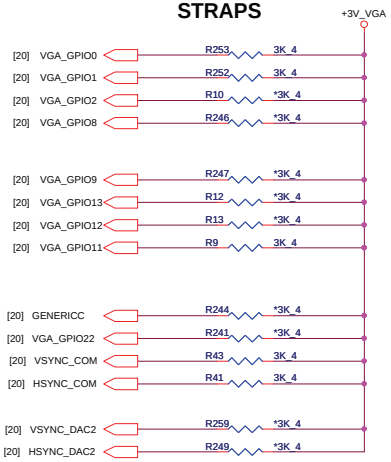
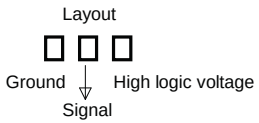


STRAPS



Location	M96	M97
pull-up for straps	10K (CS31002FB26)	3K (CS23002FB11)

Overlap pads to save space and to prevent assembly of both resistors.



Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		0
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VSYNC_DAC2	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
HSYNC_DAC2	H2SYNC		0
	GENERICC		0

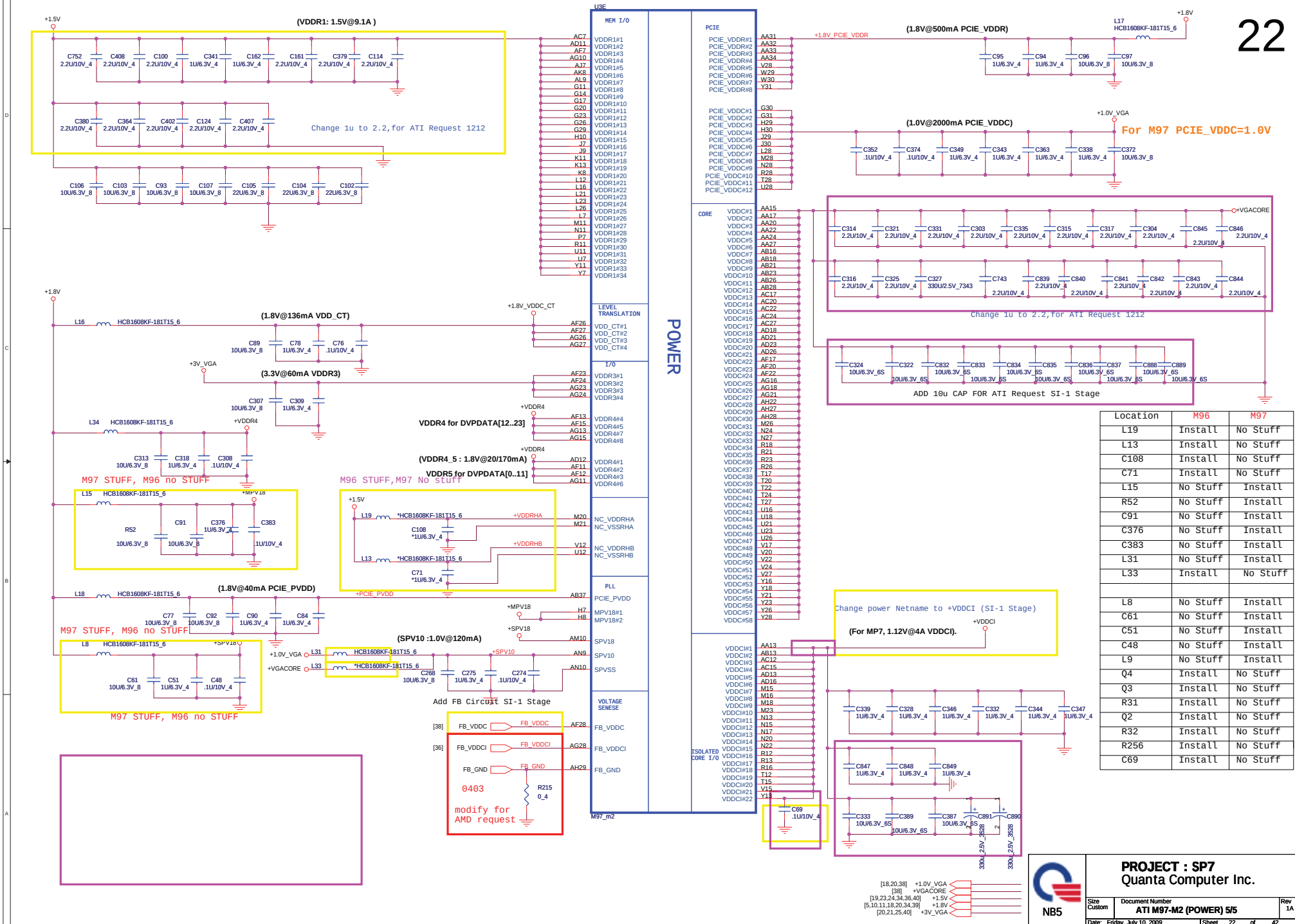
[20,22,25,40] +3V_VGA

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97(GND&Str&Ther)4/5	1A

Date: Friday, July 10, 2009 Sheet 21 of 42



Location	M96	M97
L19	Install	No Stuff
L13	Install	No Stuff
C108	Install	No Stuff
C71	Install	No Stuff
L15	No Stuff	Install
R52	No Stuff	Install
C91	No Stuff	Install
C376	No Stuff	Install
C383	No Stuff	Install
L31	No Stuff	Install
L33	Install	No Stuff
L8	No Stuff	Install
C61	No Stuff	Install
C51	No Stuff	Install
C48	No Stuff	Install
L9	No Stuff	Install
Q4	Install	No Stuff
Q3	Install	No Stuff
R31	Install	No Stuff
Q2	Install	No Stuff
R32	Install	No Stuff
R256	Install	No Stuff
C69	Install	No Stuff

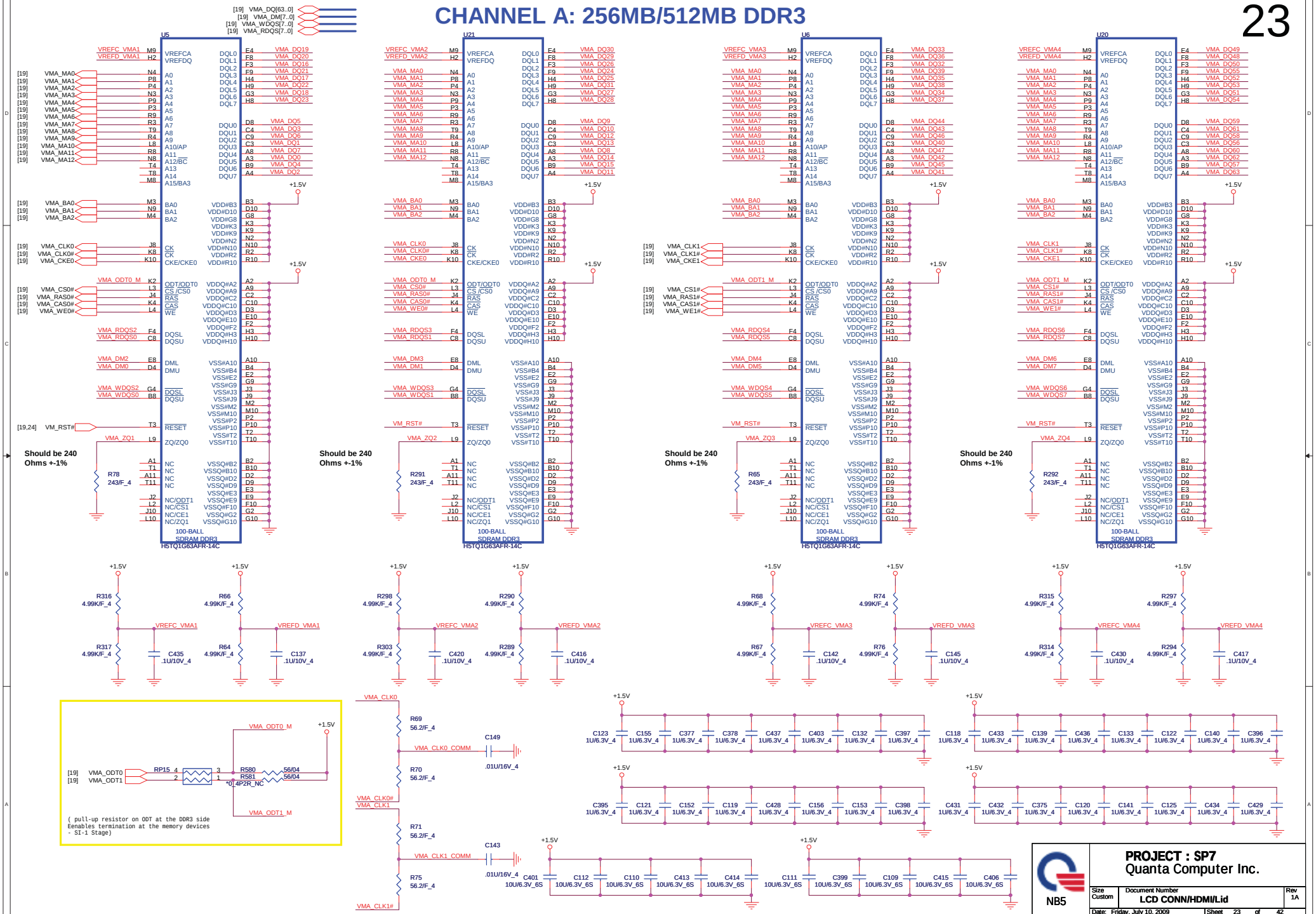
PROJECT : SP7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	ATI M97-M2 (POWER) 5/5	1A

Date: Friday, July 10, 2009 Sheet 22 of 42

CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3

[19] VMB_DQ[63..0]
[19] VMB_DM[7..0]
[19] VMB_WDQS[7..0]
[19] VMB_RDQS[7..0]

U4 / U19 / U2 / U18 — H5TQ1G63AFR-14C — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

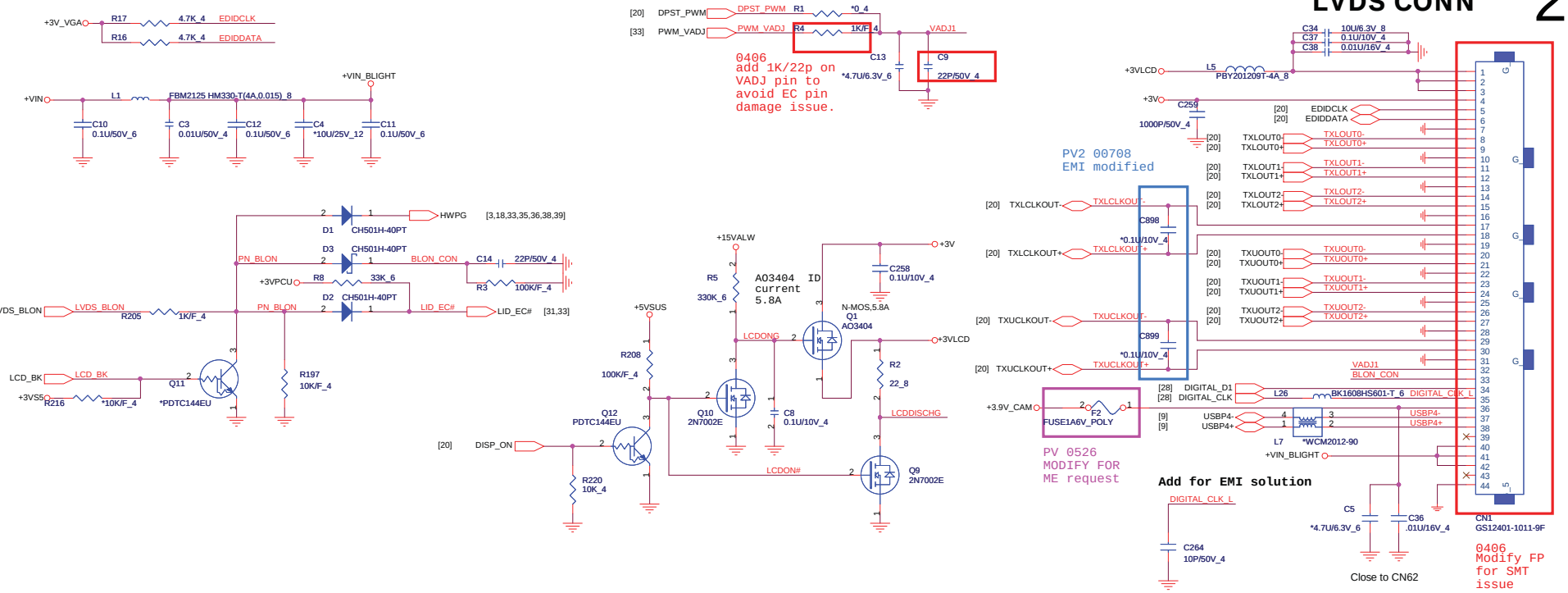
R50 243/F_4 (U4) | R61 243/F_4 (U19) | R29 243/F_4 (U2) | R51 243/F_4 (U18)

(pull-up resistor on ODT at the DDR3 side
Eenables termination at the memory devices
- SI-1 Stage)

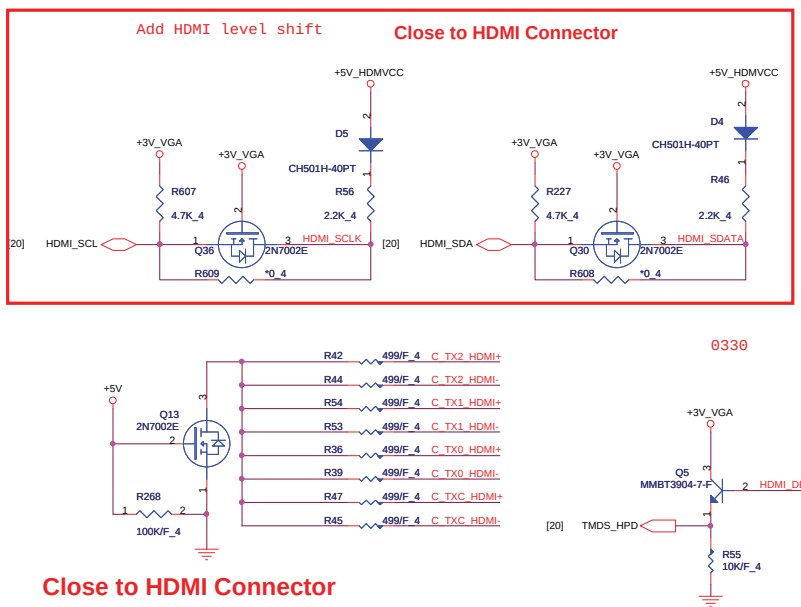
PROJECT : SP7	Quanta Computer Inc.
NB5	Size: Custom; Document Number: LCD CONN/HDMI/Lid; Rev: 1A
Date: Friday, July 10, 2009	Sheet 24 of 42

LVDS CONN

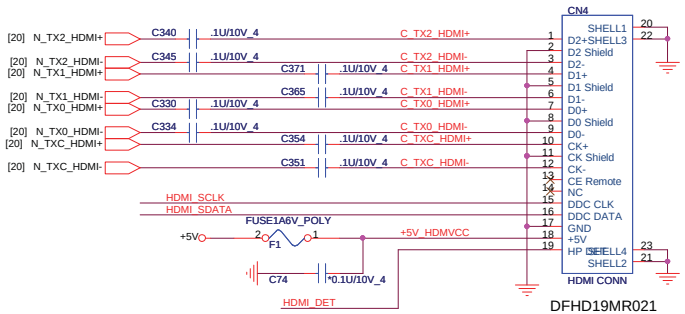
25



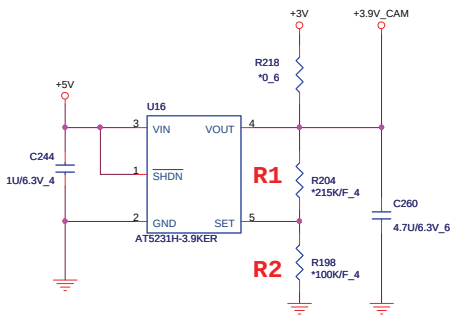
HDMI PORT



HDMI HPD SENSE



USB CAMERA /DIGITAL MIC CONNECT



Vout=1.25(1+R1/R2)

[2,3,7,8,9,10,11,13,14,15,16,18,26,27,28,29,30,31,32,33,34,37,40] +3V
[20,21,22,40] +3V_VGA
[7,9,10,11,40] +3VS5
[8,13,15,31,33,34,35,36,38,39,40,41,42] +3VPCU
[11,27,29,30,37,40] +5V
[40] +5VSUS
[35,38,40,41] +VIN
[35,40] +15VALW

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN/HDMI/Lid	Rev: 1A
Date: Friday, July 10, 2009	Sheet 25 of 42	

USB3.0 X 2 and E-SATA/USB2.0 COMBO

26

SI U29.P13 Change to +3V

SI2 0414 NEC request

SI 0219 change BOM

SI2 0320 change Footprint

close USB3

150 mils (Iout=3.5A)

Low: Enable AC Mode

High: Disable DC Mode

PV2 stage modify

1125 Modify

1119 Modify

6.3V to 25V from NEC

*nPD720200

Close to chip
Use 1% RES

USB CON. co-lay

SI2 0325 change Footprint

AT25F512A or AT25F512B (Atmel)
MX25L512 (Macronix)

*MX25L8005M2C-15G

PV-2 0702 Change Footprint

PV-2 0702 EMI add

PV-2 0702 EMI add

E_SATA change channel from SATA2 to SATA5 0216

USB3.0 PORT1

USB3.0 PORT2

USB2.0 PORT6

USB2.0 PORT7

*USB3.0 CONN

USB_ESATA_COMBO

Clock select signal	
USB3.0_CSEL	High = External 48Mhz Low = 24MHz X'tal

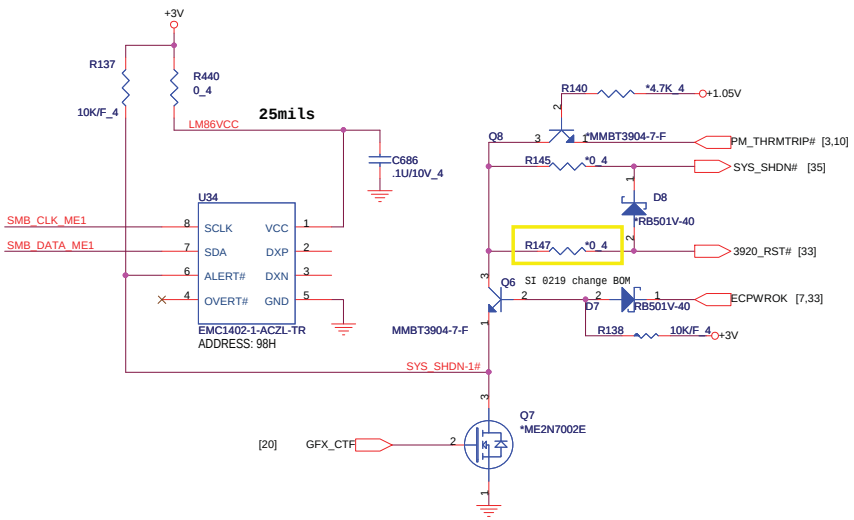
PROJECT : SP7
Quanta Computer Inc.

NB5

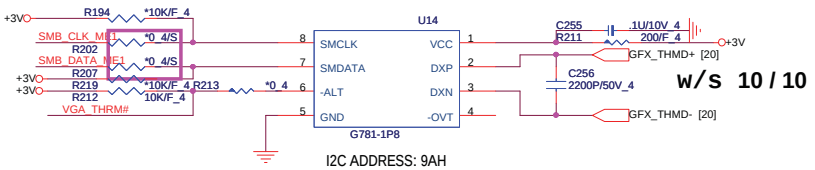
Size	Document Number	Rev
Custom	NEC USB 3.0	1A

Date: Friday, July 10, 2009 Sheet 26 of 42

CPU THERMAL MONITOR

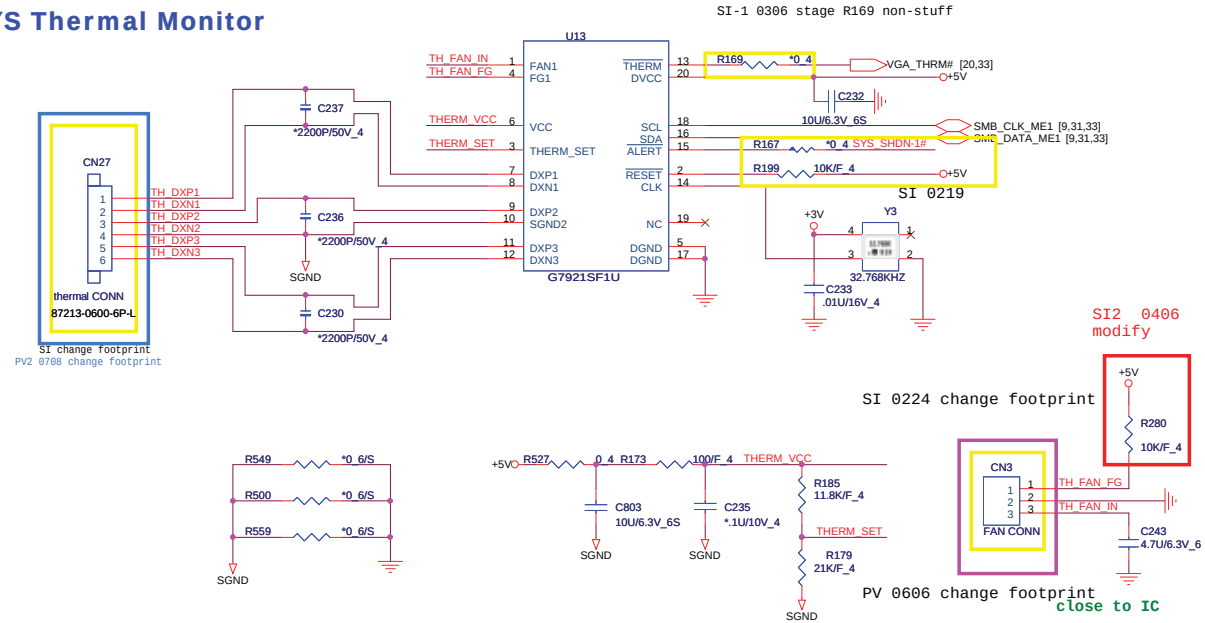


GPU Thermal Sensor



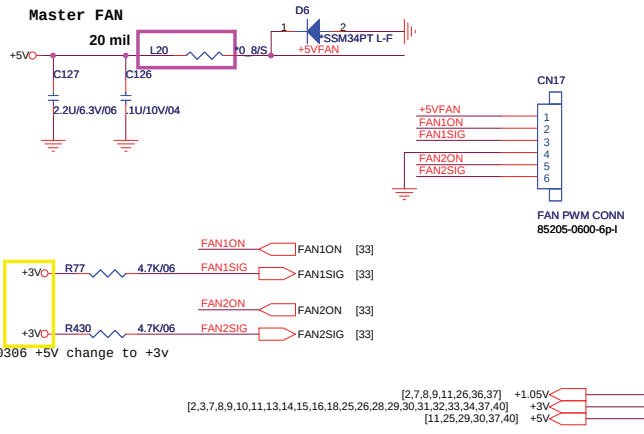
w/s 10 / 10

SYS Thermal Monitor



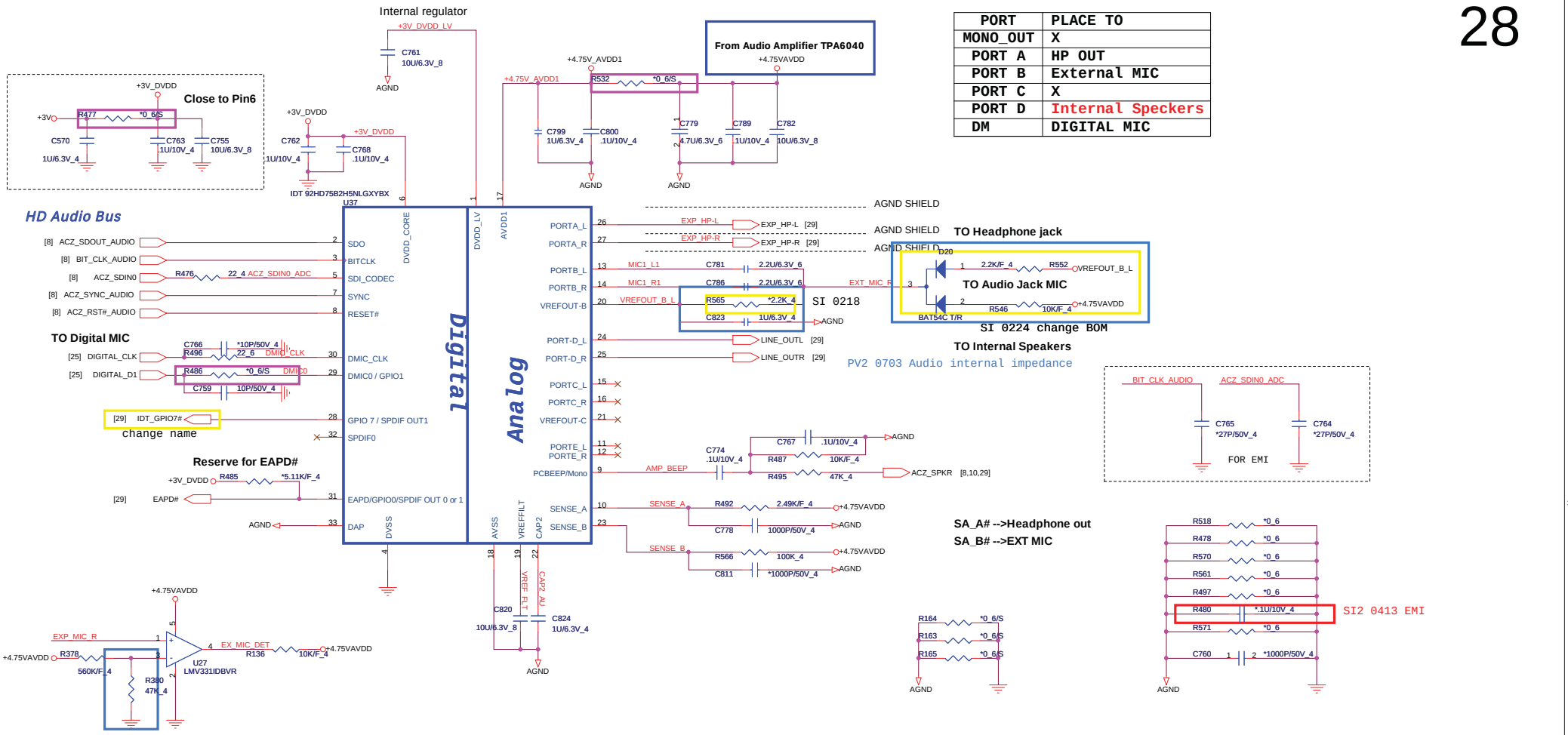
CPU FAN1/2 CONN

RPM Control



NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: CPU/VGA/SYSTEM THERMAL	Rev: 1A
Date: Friday, July 10, 2009	Sheet 27 of 42	

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	External MIC
PORT C	X
PORT D	Internal Speckers
DM	DIGITAL MIC



Combo Jack (Headphone/MIC)

Normal Close

SI 0227Change footprint

SI 2/10
CN22.8,CN22.9 connect to AGND

SIE 2SJ-B960-001

SI 0218 For EMI

SI2 0413 EMI

TIP	Headphone Left
R1	Headphone Right
R2	GND
BASE	MIC

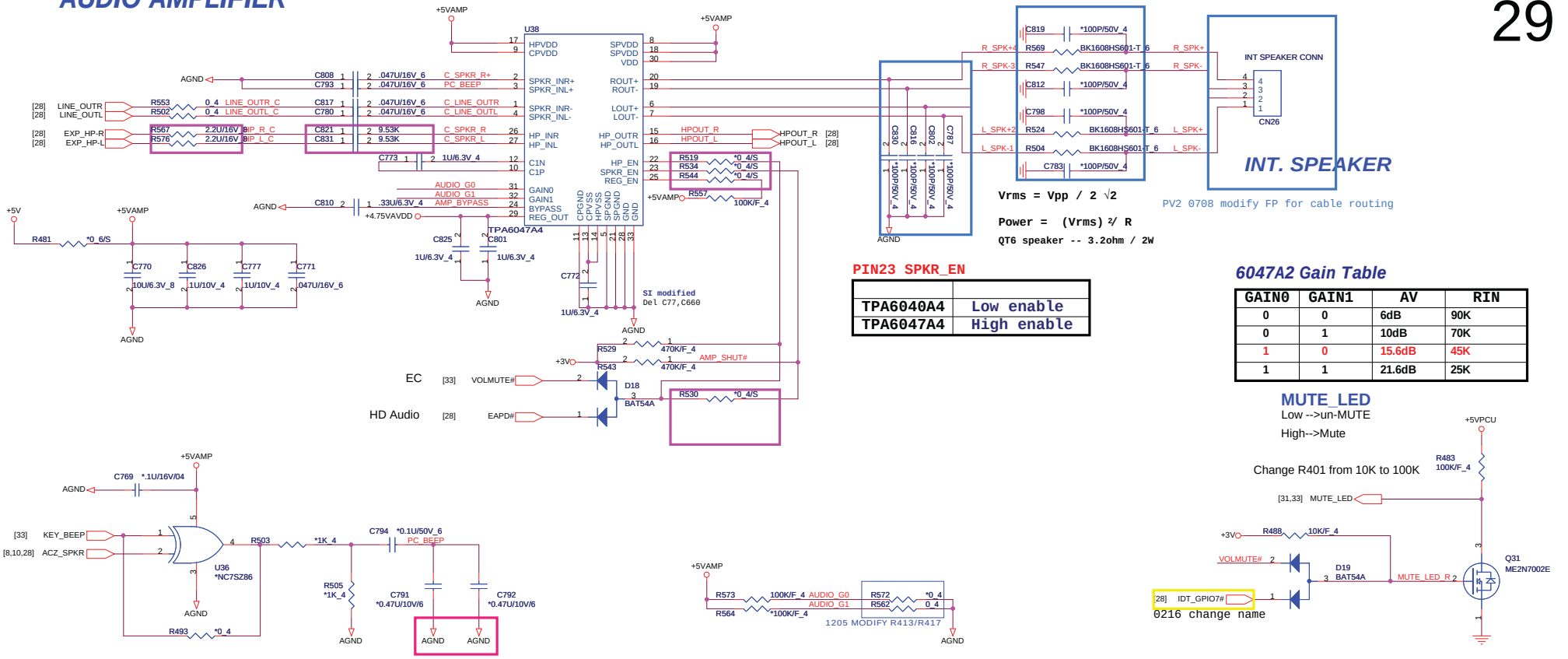
PROJECT : SP7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Azalia 92HD75	1A

Date: Friday, July 10, 2009 | Sheet 28 of 42

AUDIO AMPLIFIER



PIN23 SPKR_EN

TPA6040A4	Low enable
TPA6047A4	High enable

6047A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

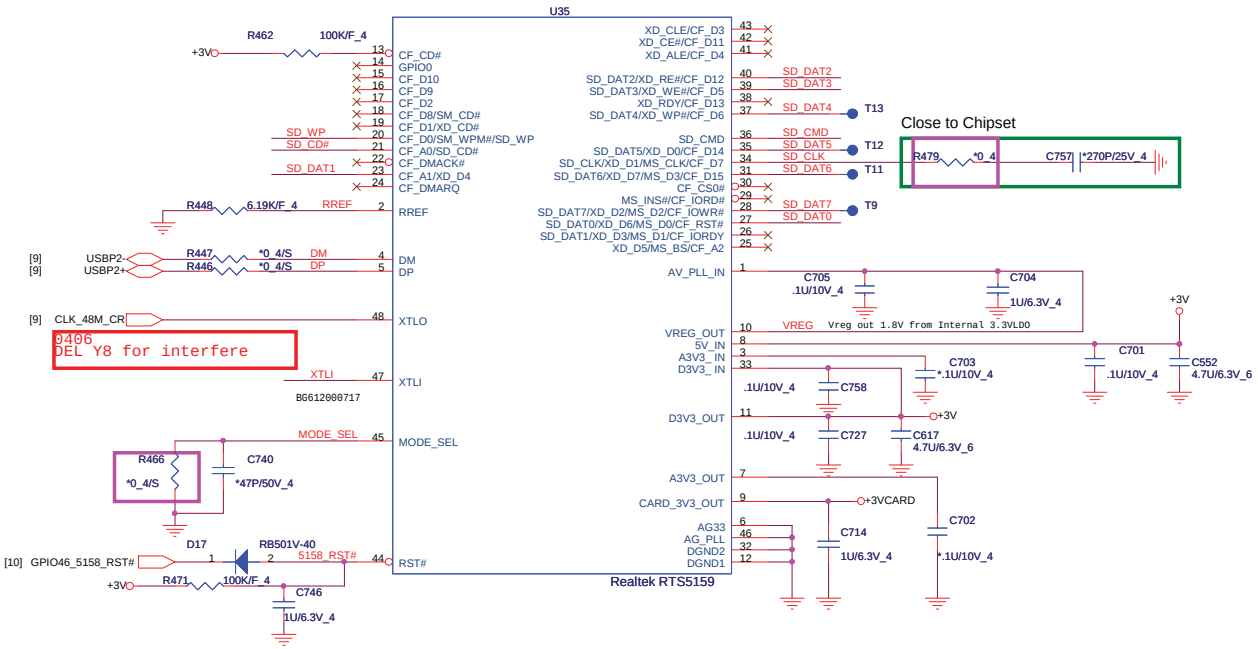
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,30,31,32,33,34,37,40] +3V
[28] +4.75VAVDD
[11,25,27,30,37,40] +5V
[15,26,33,35,36,37,38,39,40,41] +5VPCU

NB5

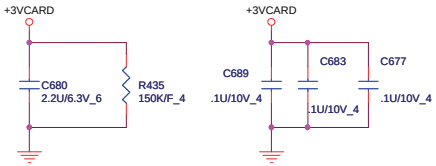
PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6047	1A

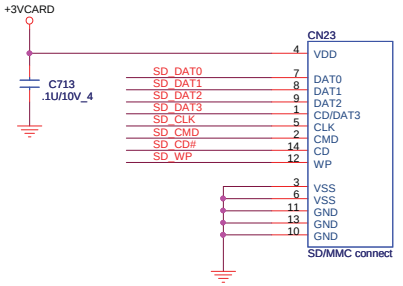
Date: Friday, July 10, 2009 Sheet 29 of 42



CLOSE CONN



2 IN1 CARD READER SD/MMC

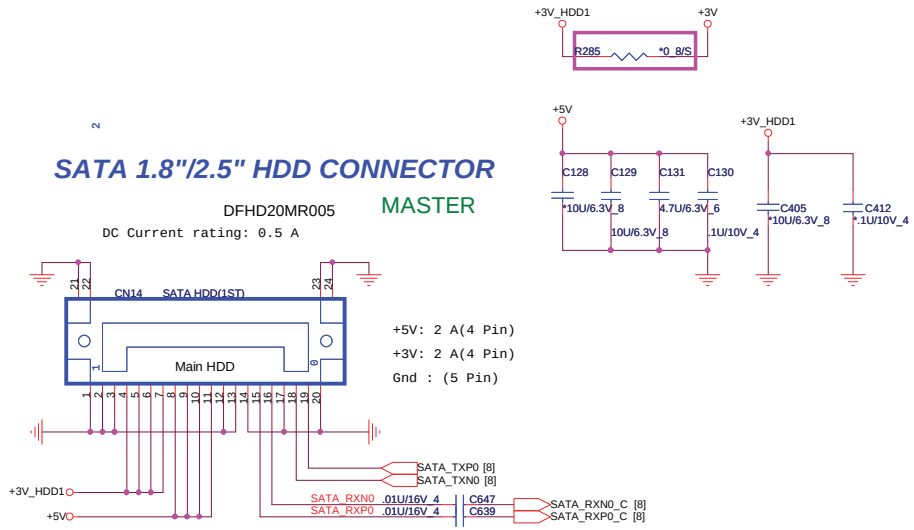


SATA 1.8"/2.5" HDD CONNECTOR

MASTER

DFHD20MR005

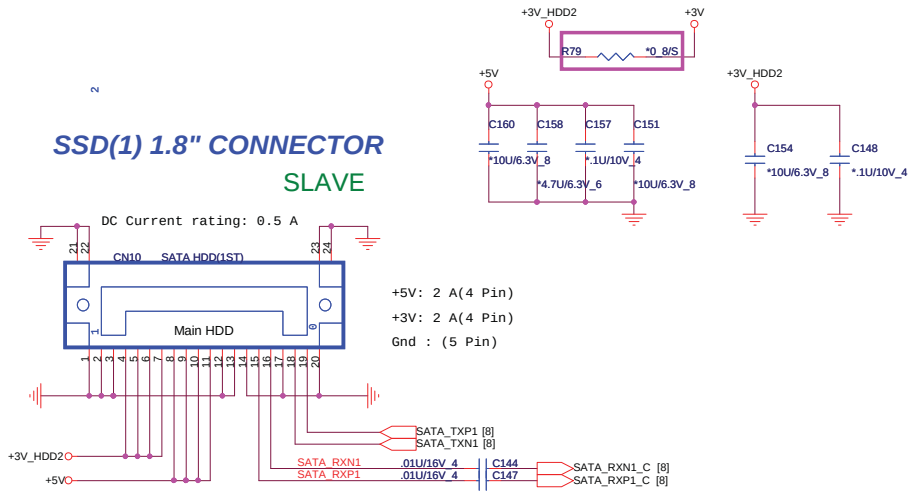
DC Current rating: 0.5 A



SSD(1) 1.8" CONNECTOR

SLAVE

DC Current rating: 0.5 A



[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,31,32,33,34,37,40] +3V

[11,25,27,29,37,40] +5V

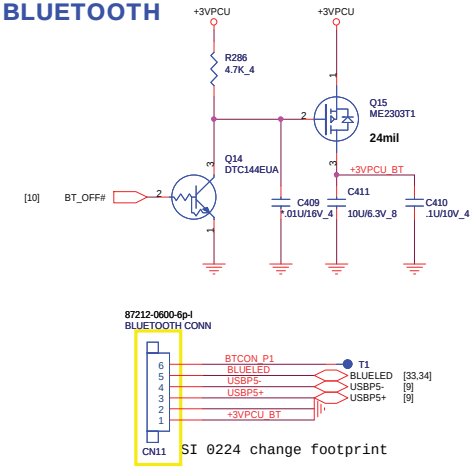
NB5

PROJECT : SP7
Quanta Computer Inc.

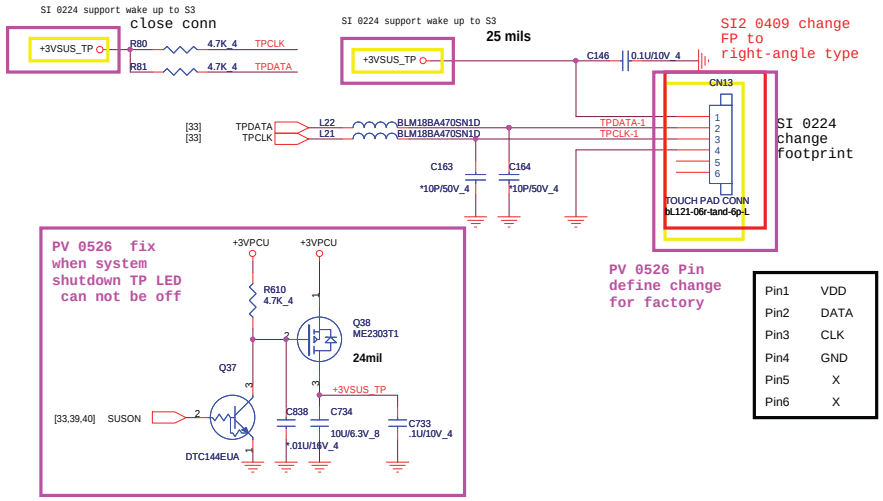
Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET	1A

Date: Friday, July 10, 2009 | Sheet 30 of 42

BLUETOOTH

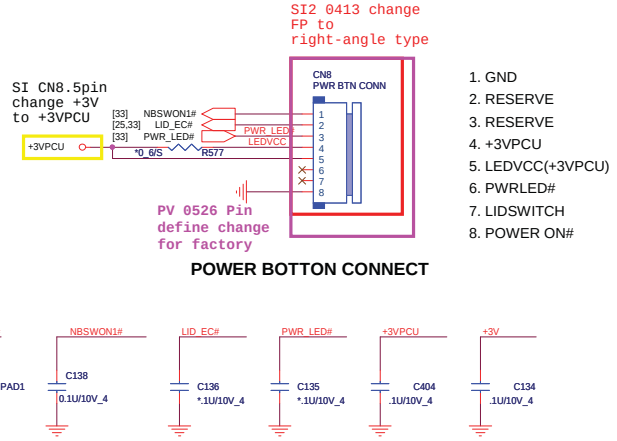


TOUCH PAD CONNECTOR

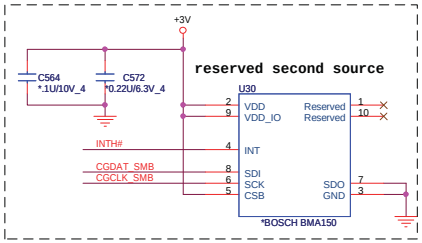


Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	X
Pin6	X

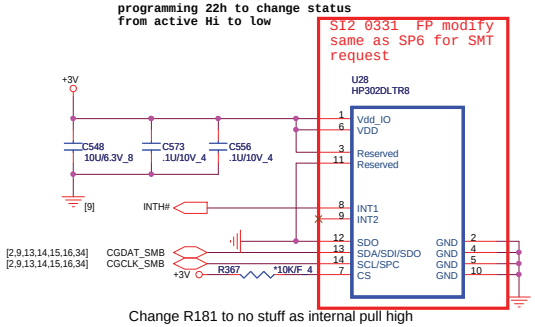
Power Botton



Accelerometer Sensor



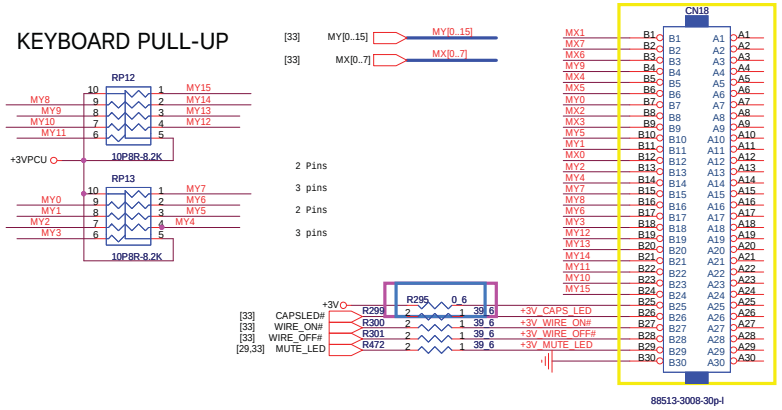
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



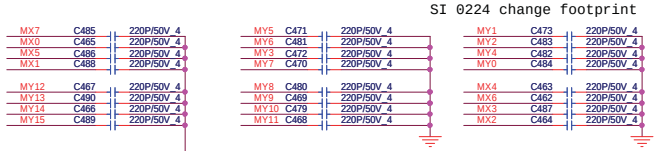
Change R181 to no stuff as internal pull high

Pin 12: Low	38hex
Pin 12: unconnected/floating	3Ahex

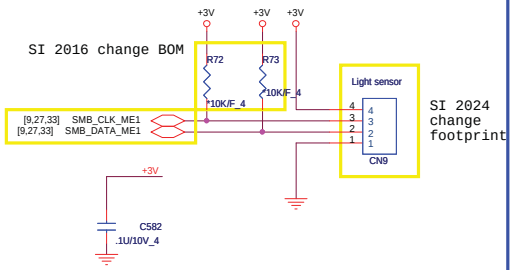
Key Board CONN



SI 0224 change footprint

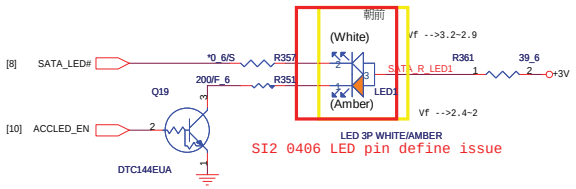


Ambient Light Sensor



LED

SI0210 white for HDD active
Amber for HDD locked

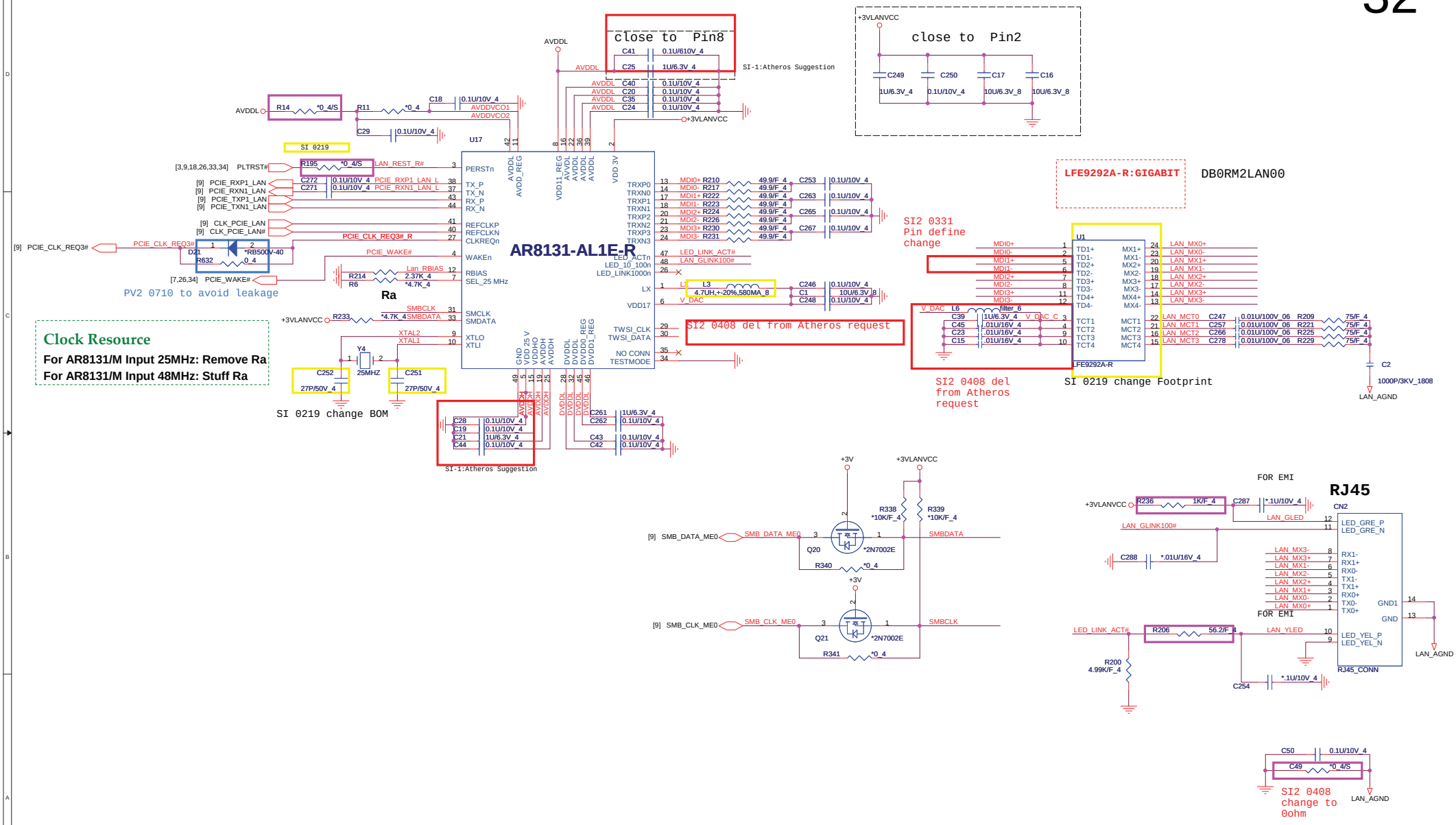


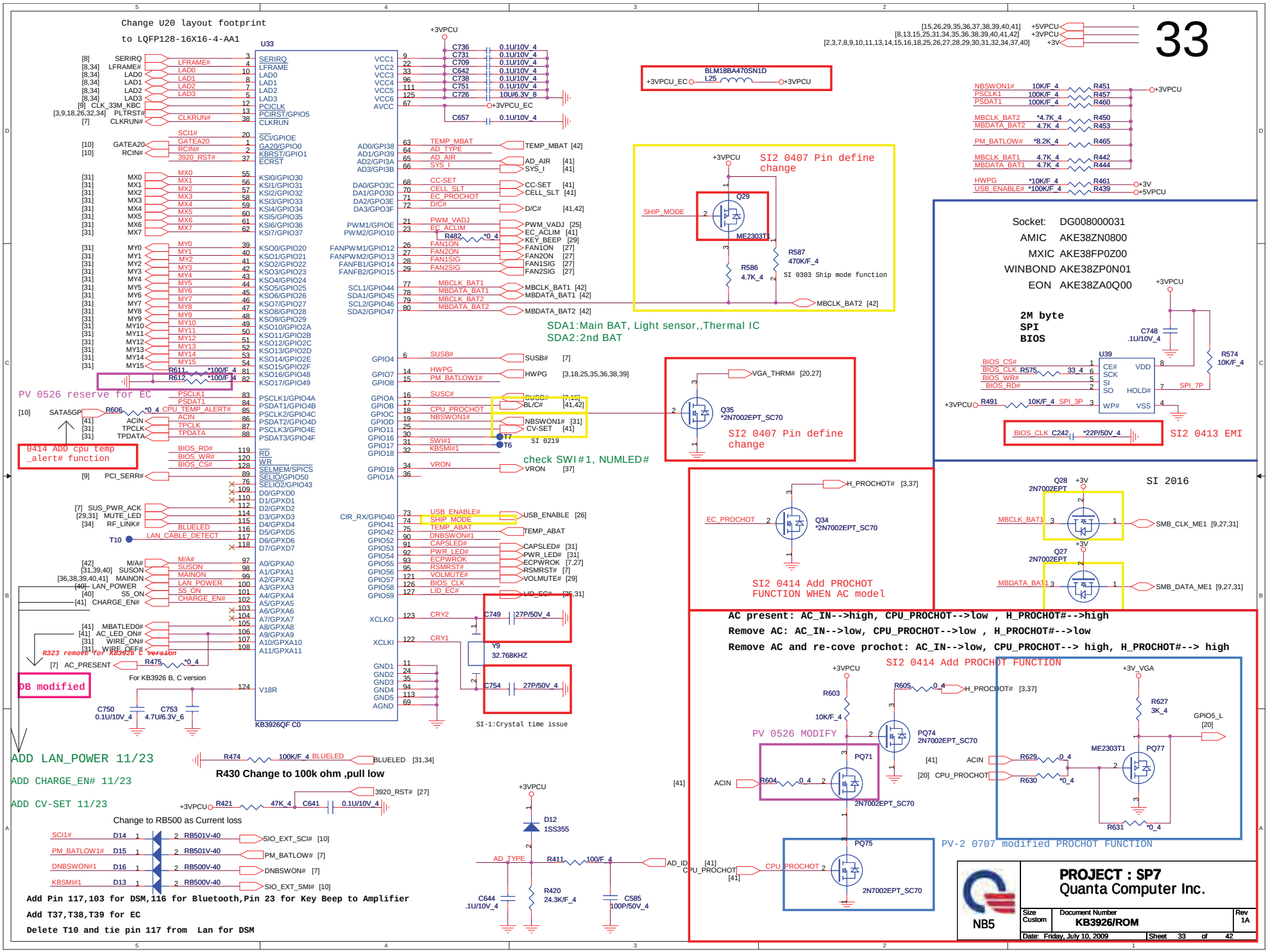
SI2 0406 LED pin define issue

[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,32,33,34,37,40]
[8,13,15,25,33,34,35,36,38,39,40,41,42]
+3V
+3VPCU

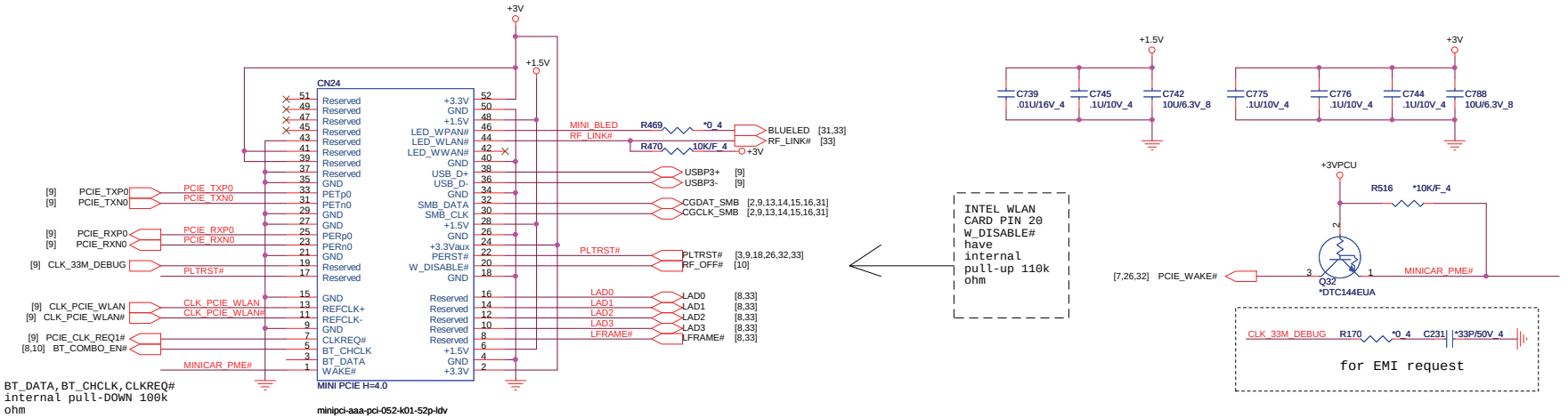
PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/TP/PW BN/Key CON/Acc/LED/ALS	1A
NB5	Date: Friday, July 10, 2009	Sheet 31 of 42

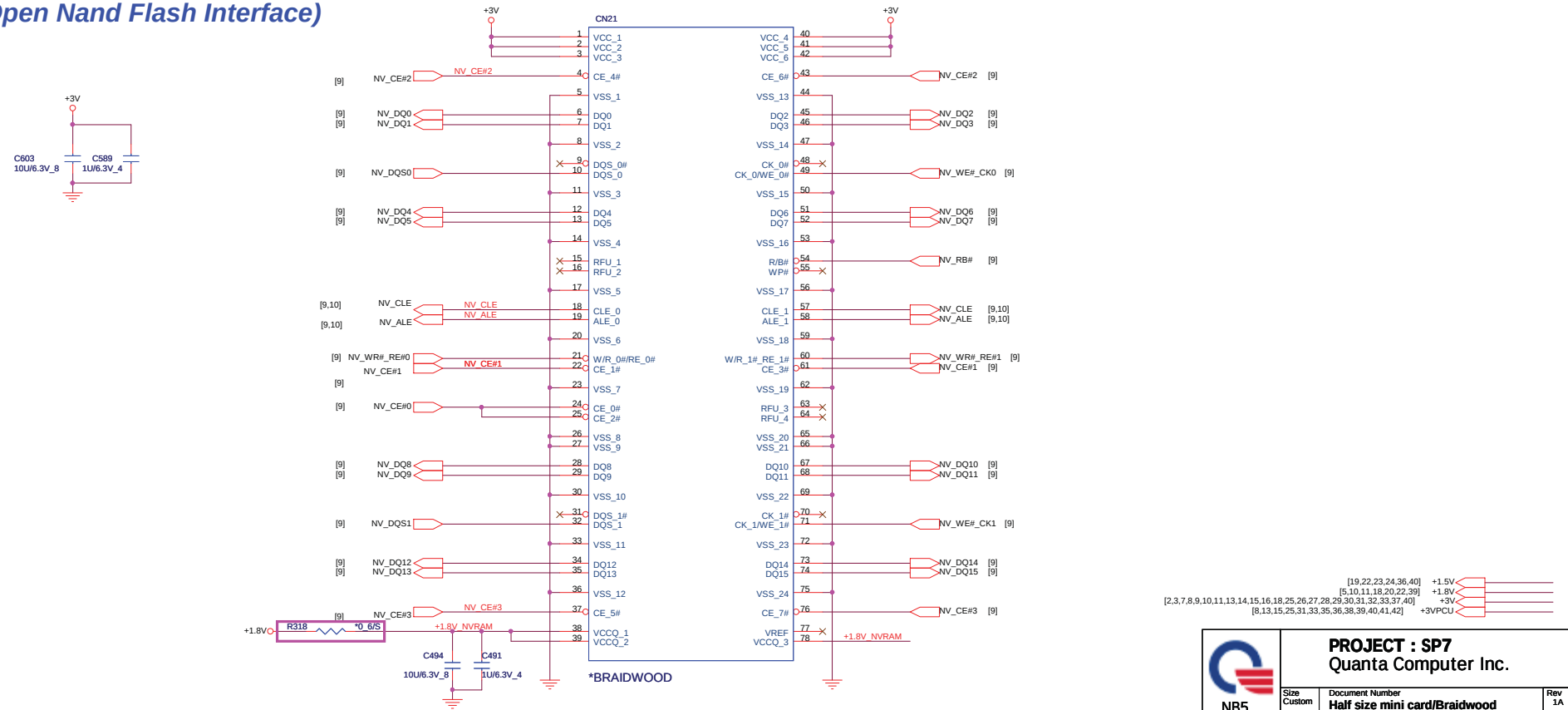




Half size mini card(802.11a/b/g/n)



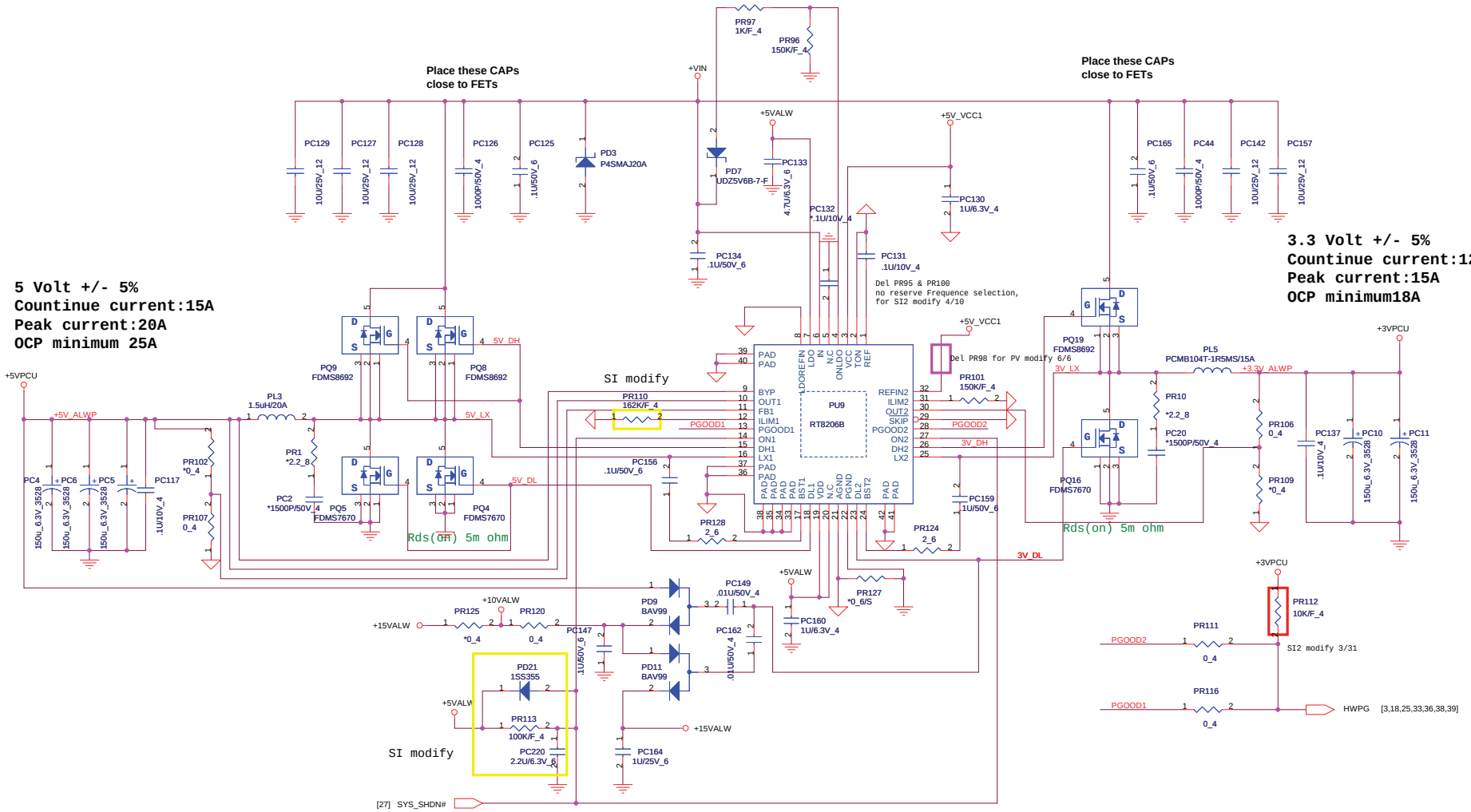
Braidwood(Open Nand Flash Interface)



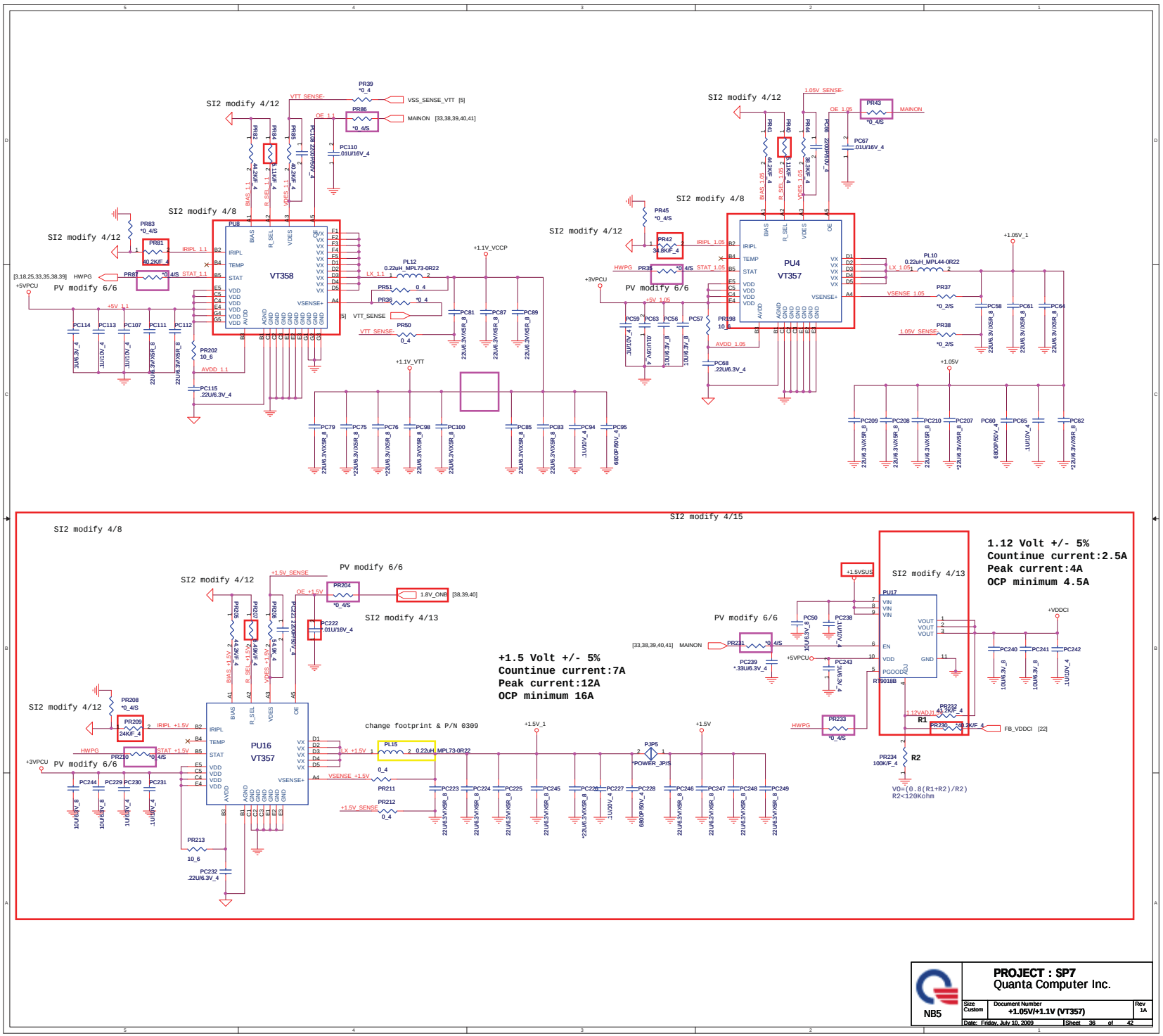
Size: Custom	Document Number: Half size mini card/Braidwood
NB5	Rev: 1A
Date: Friday, July 10, 2009	Sheet 34 of 42

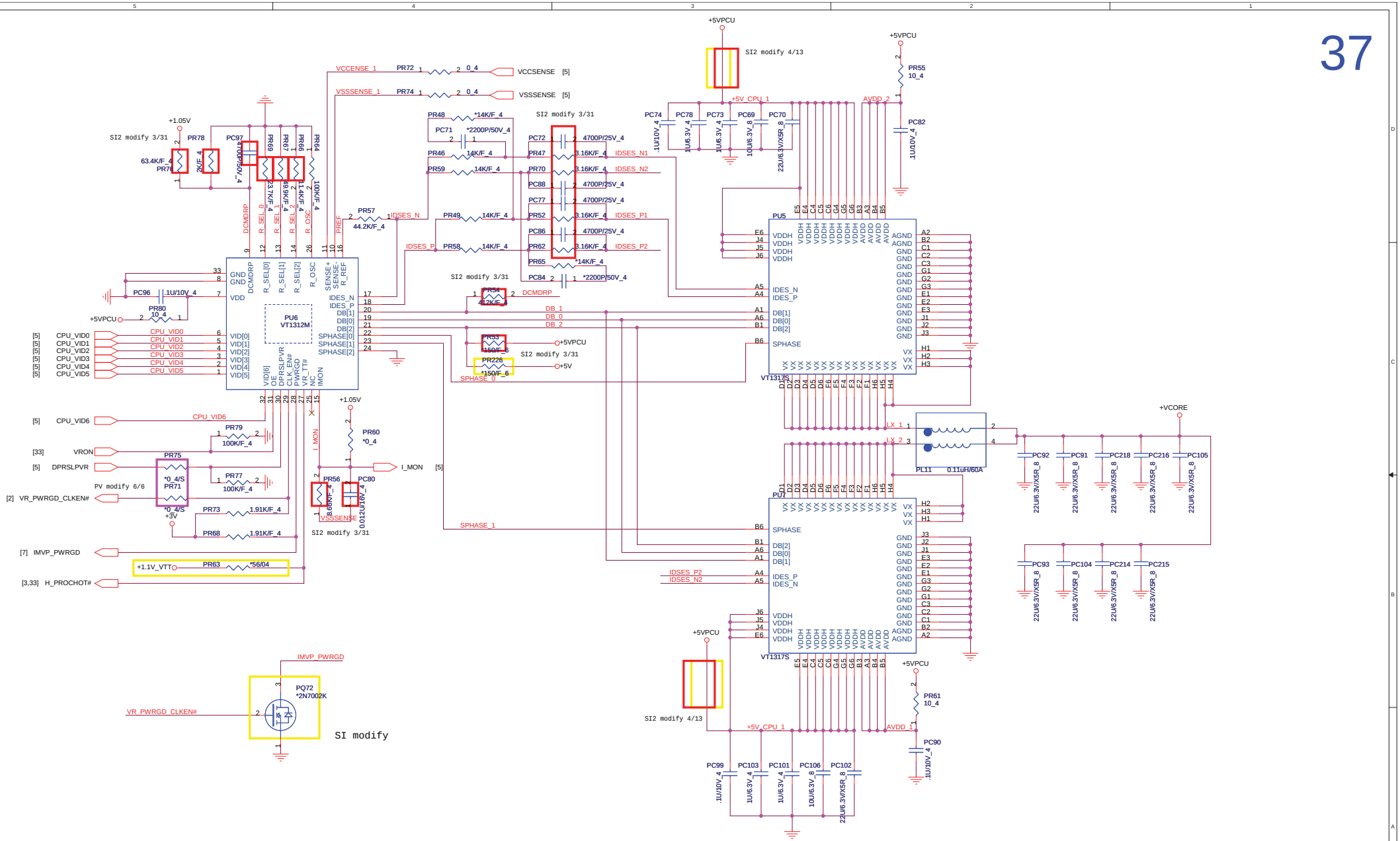
PROJECT : SP7
Quanta Computer Inc.

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW



NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 35 of 42	

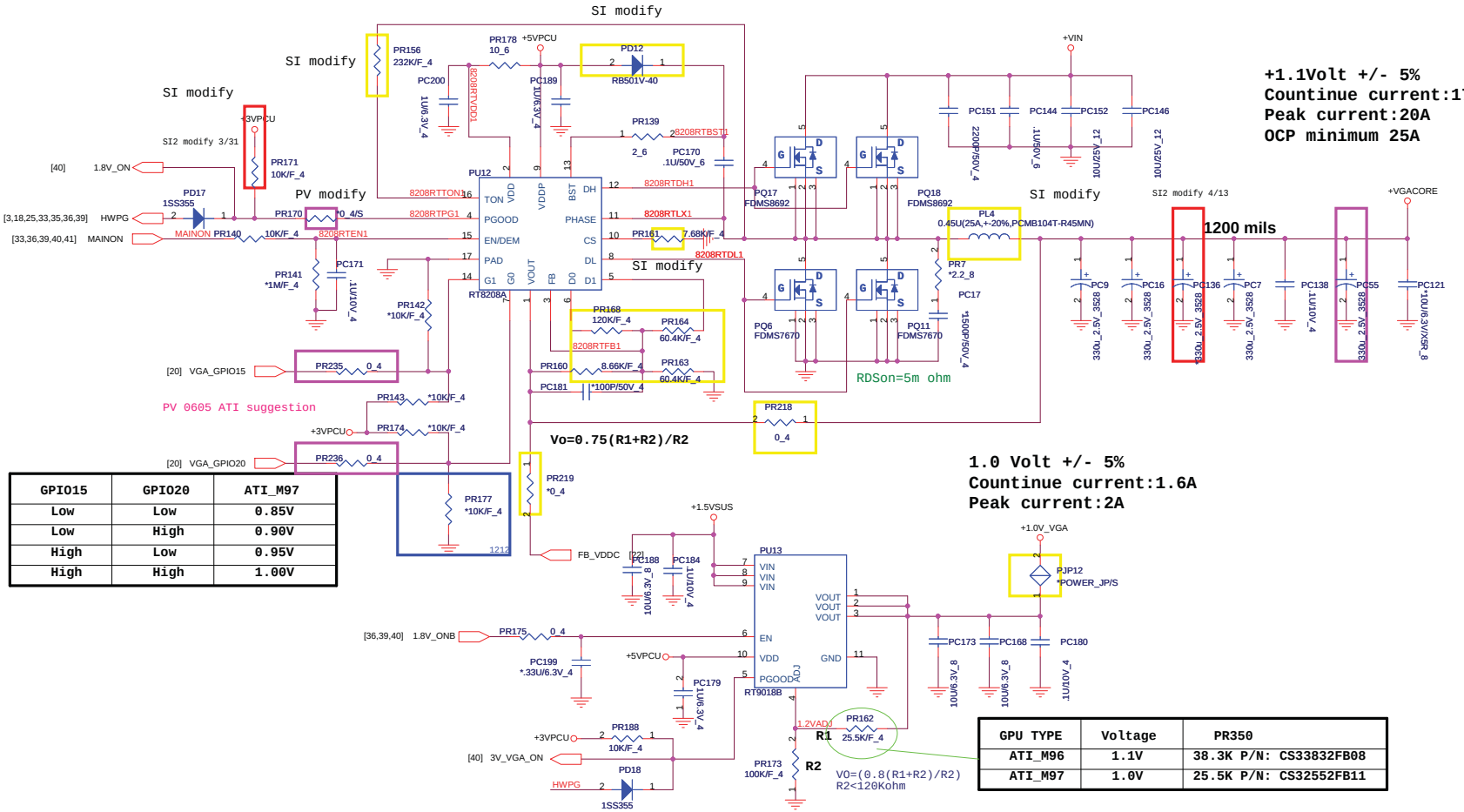




PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (VT1312M/VT1317)	1A
NB5	Date: Friday, July 10, 2009	Sheet 37 of 42

VGA Core & VCC1.1



GPIO15	GPIO20	ATI_M97
Low	Low	0.85V
Low	High	0.90V
High	Low	0.95V
High	High	1.00V

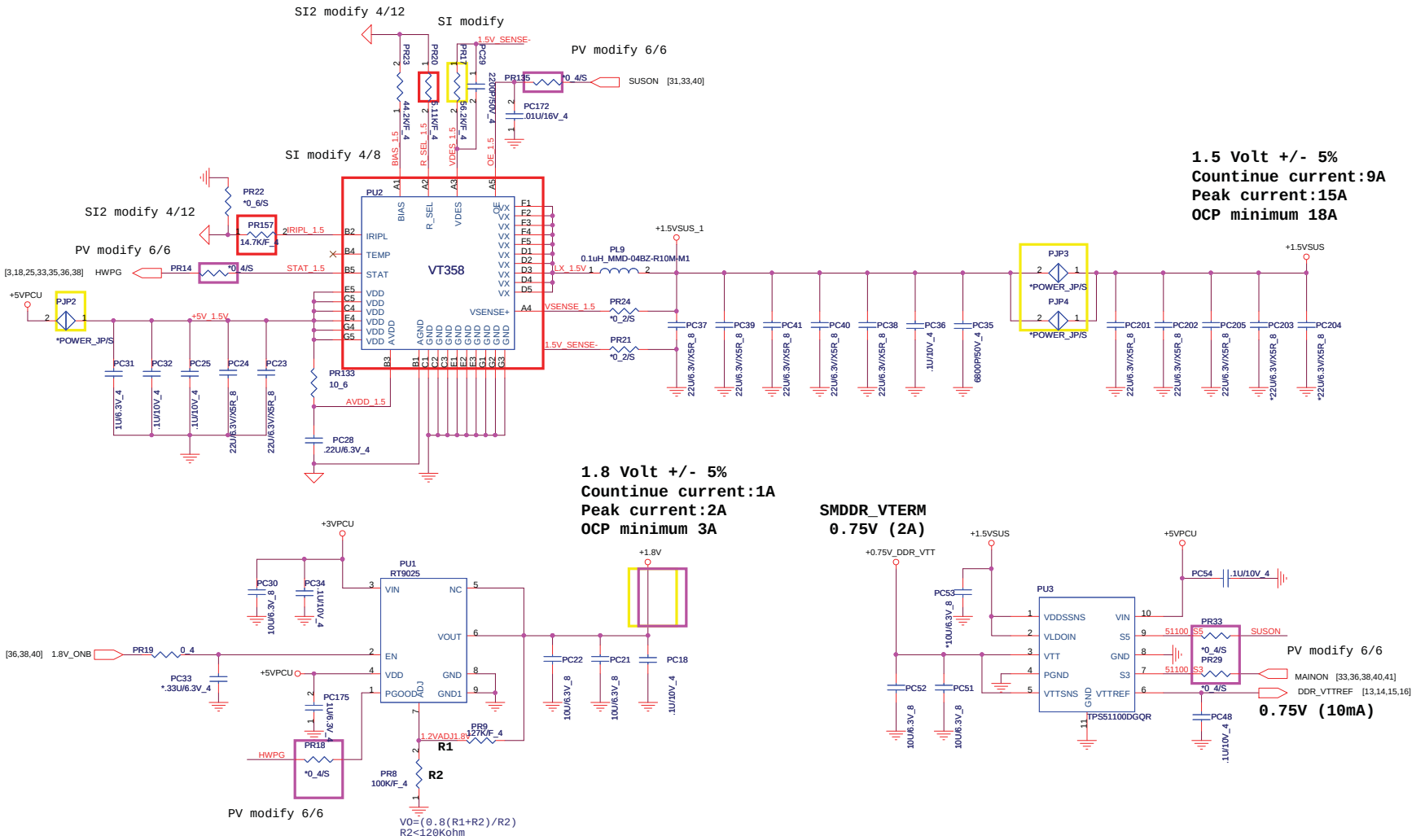
GPU TYPE	Voltage	PR350
ATI_M96	1.1V	38.3K P/N: CS33832FB08
ATI_M97	1.0V	25.5K P/N: CS32552FB11

PROJECT : SP7
Quanta Computer Inc.

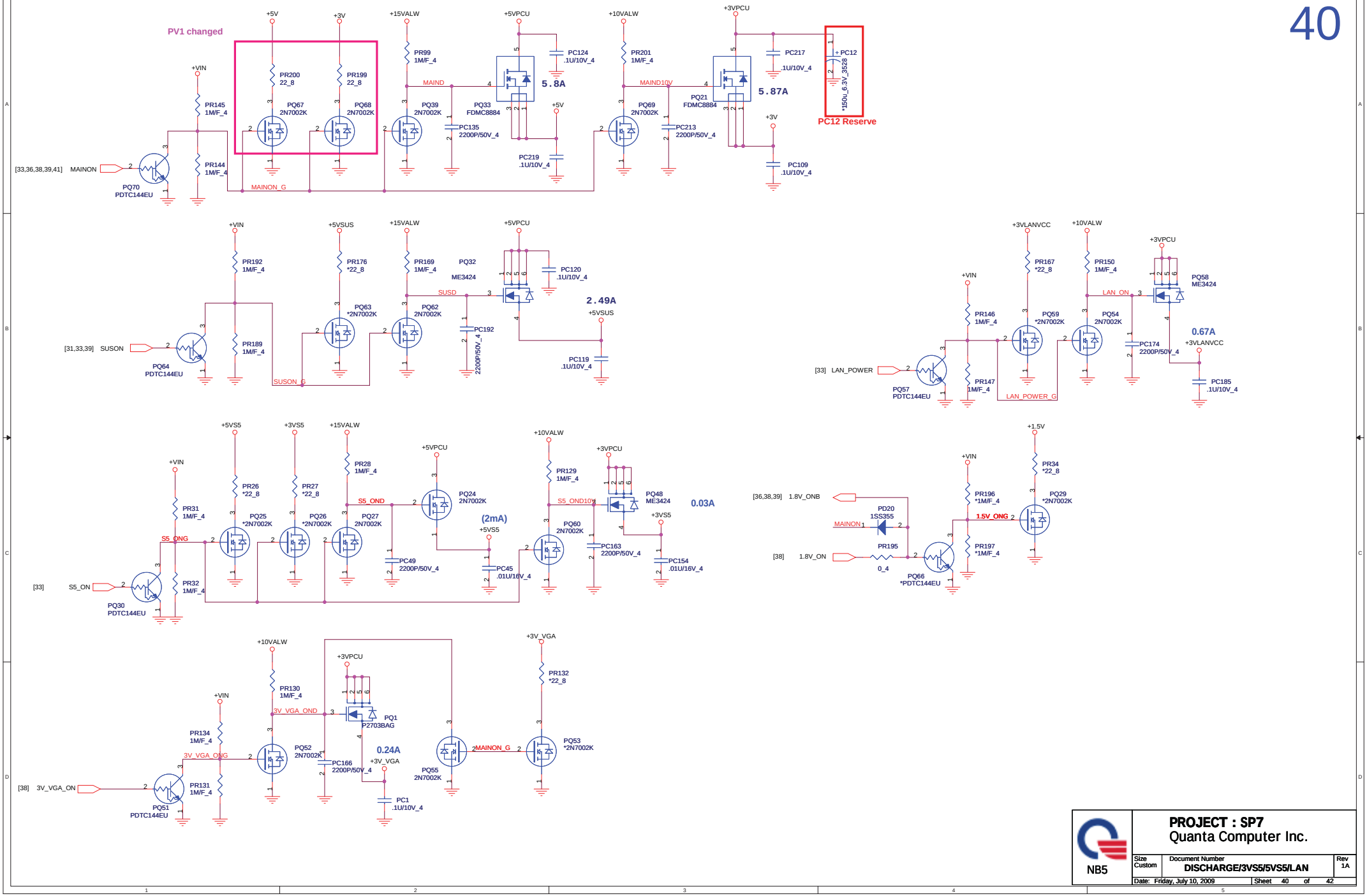
NB5

Size: Custom | Document Number: VGA Core (RT8208) | Rev: 1A

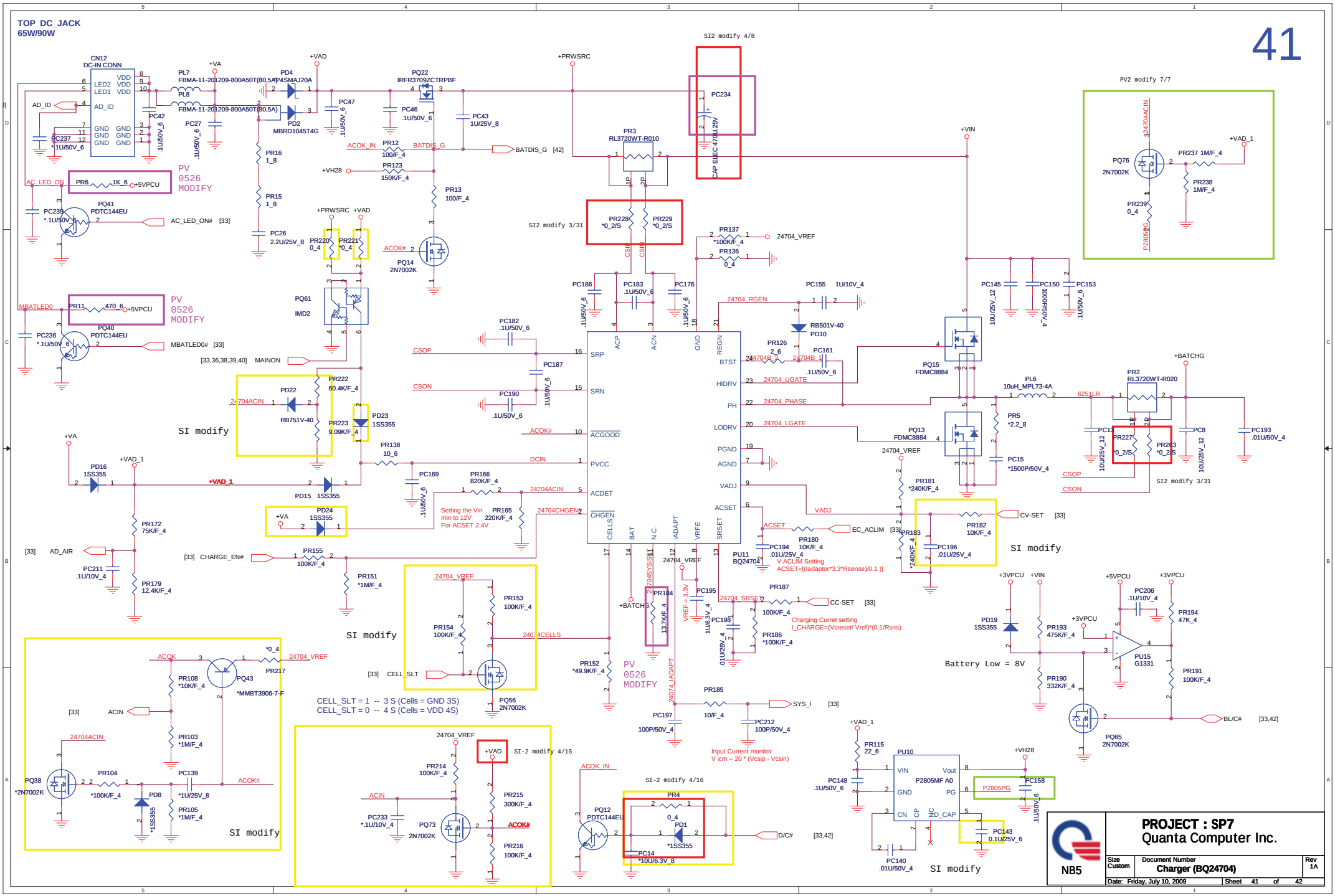
Date: Friday, July 10, 2009 | Sheet 38 of 42

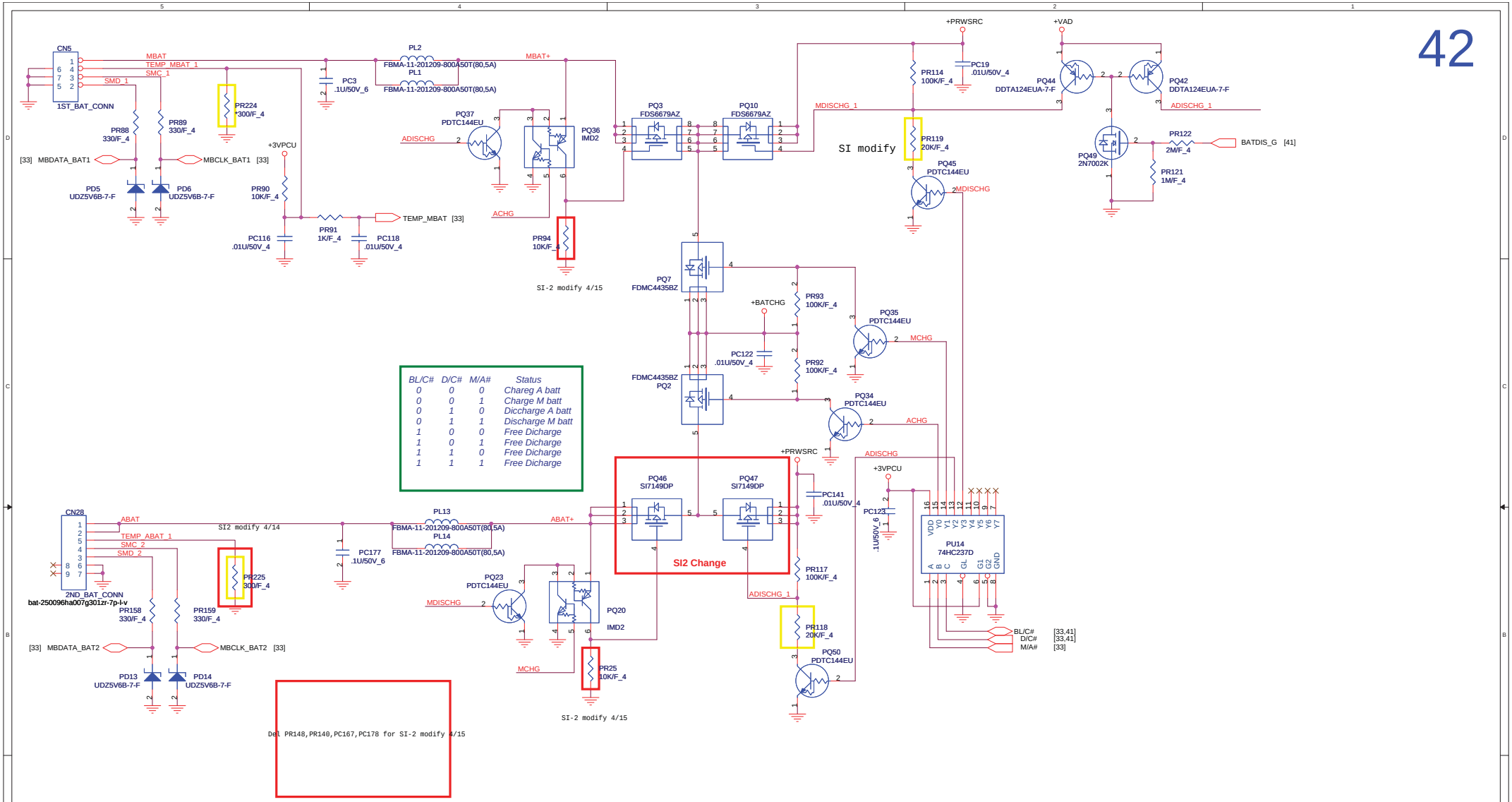


NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3/1.8V (VT356/VT357)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 39 of 42	



NB5	PROJECT : SP7 Quanta Computer Inc.	
	Size: Custom Document Number: DISCHARGE/3VS5/5VS5/LAN	Rev: 1A
	Date: Friday, July 10, 2009 Sheet 40 of 42	





BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

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