Wistron Confidential

MV

2008/07/16 REV :MV-01

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NORN 2.0

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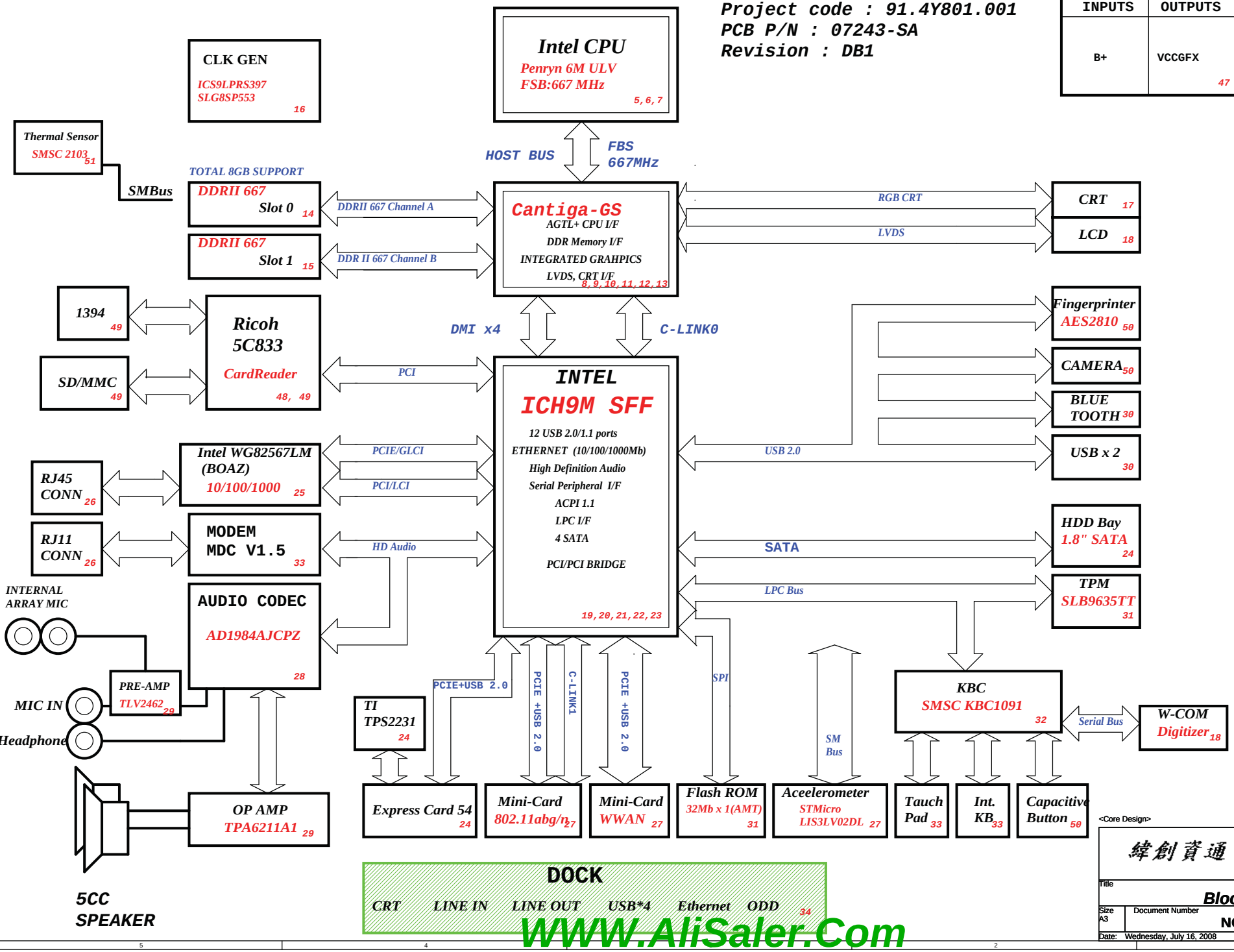
NORN 2.0 Block Diagram

Project code : 91.4Y801.001
PCB P/N : 07243-SA
Revision : DB1



VGA
ISL6263A

INPUTS	OUTPUTS
B+	VCCGFX 47

SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
B+	+5VALW 5A +3VALW 4A 41

SYSTEM DC/DC
TPS51124

INPUTS	OUTPUTS
B+	+1.5VS 4A +VCCP 6A 42

CHARGER
BQ24740

INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA 39

CPU DC/DC
ISL6261ACRZ

INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 44, 45

PCB LAYER

L1:	TOP
L2:	Signal
L3:	GND
L4:	Signal
L5:	VCC
L6:	GND
L7:	Signal
L8:	Bottom

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Title: Block Diagram

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Title: Change Notes List

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Voltage Rails

o MEANS ON x MEANS OFF

State \ power plane	+BB LDO3 LDO5	+3VALW +5VALW	+1.8V +0.9V	+5VS +3VS +1.5VS +1.05VM +VGA_CORE +CPU_CORE +VCCP	+3VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	X	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EETERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G,E

DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	~~Floppy Disk~~
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up1 (Right Side)
1	Free
2	EXPRESS SLOT
3	WLAN
4	Walk-up2 (Left Side)
5	Walk-up3
6	Bluetooth
7	WWAN
8	Fingerprint
9	Dock1 (HUB)
10	Camera
11	Dock2 (IDE)

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Control
18	Intel 82801H (ICH8 Family) USB Universal Host Control Richo R5C853 Integrates FlashMedia Control Richo R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port -27D6 Intel 82801H (ICH8 Family) USB Universal Host Control
20	Intel 82801H (ICH8 Family) USB Universal Host Control Intel 82801H (ICH8 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH8 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

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Title: **Notes List**

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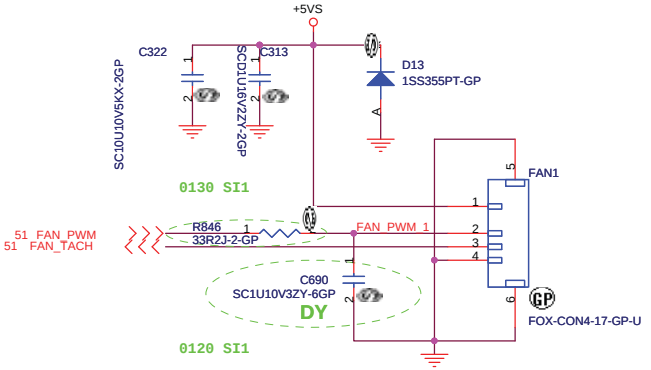
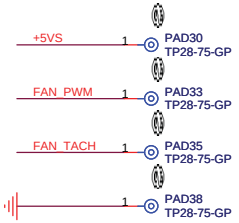
4 WIRE PWM Fan Control circuit

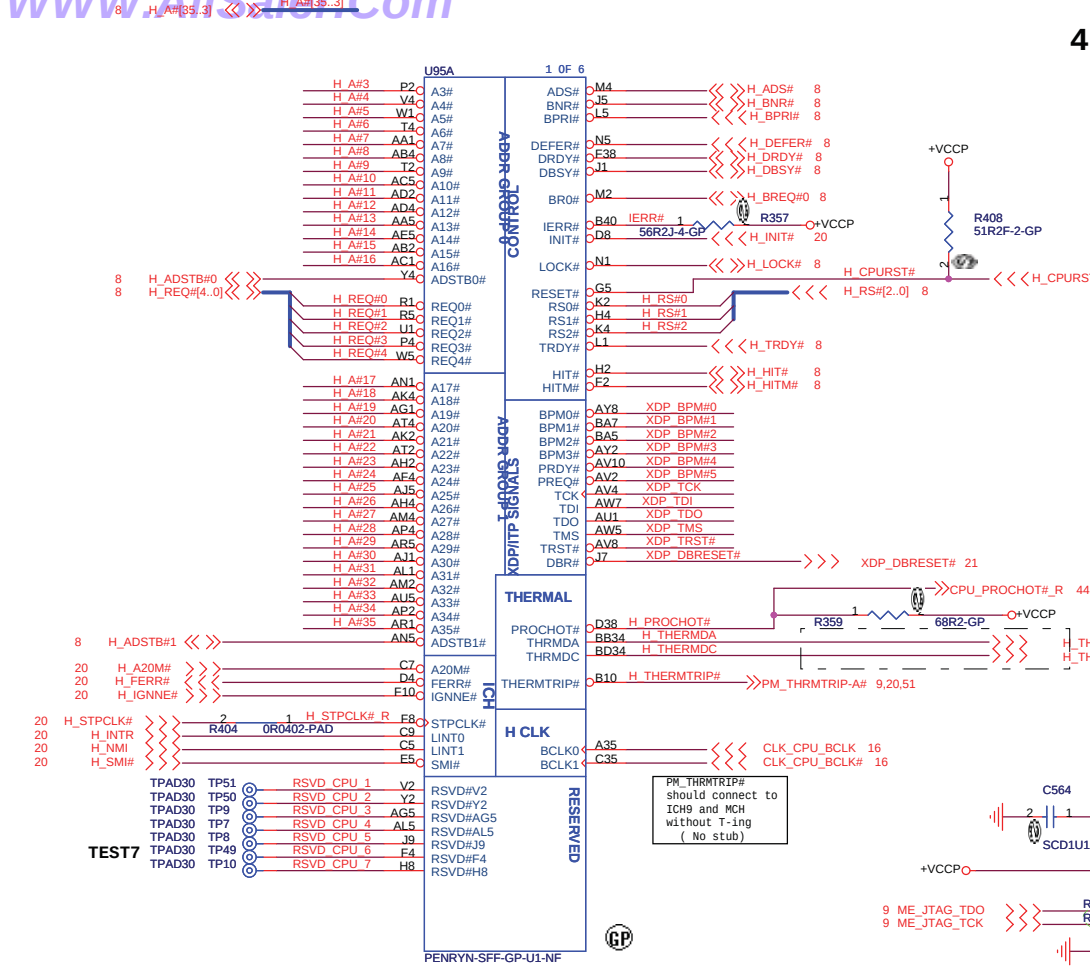


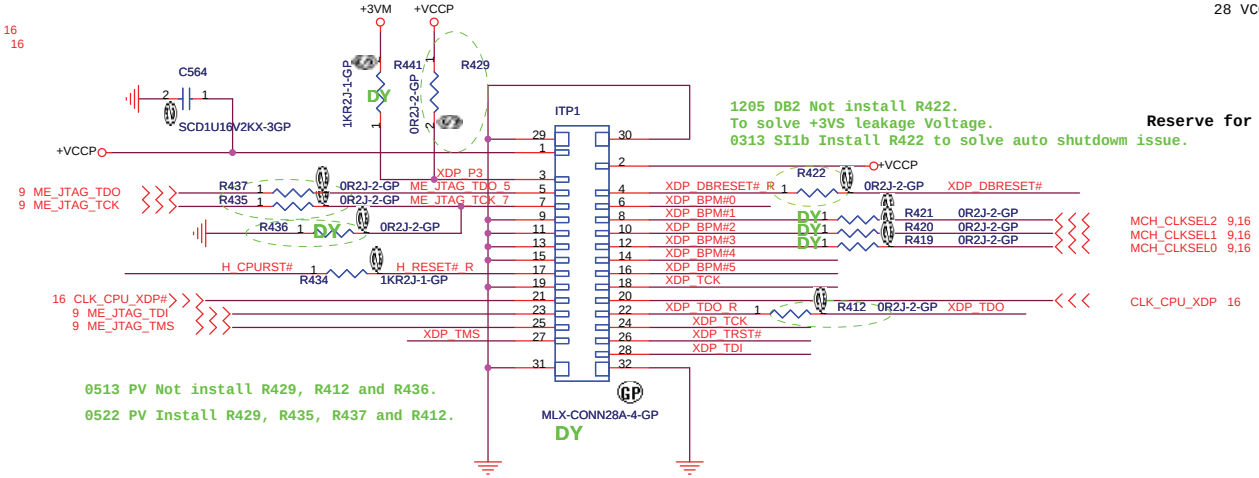


1 TDI
2 TMS
3 TRST#
4 NC
5 TCK
6 NC
7 TDO
8 BCLK#
9 BCLK
10 GND
11 FBO
12 RESET#
13 BPM5#
14 GND
15 BPM4#
16 GND
17 BPM3#
18 GND
19 BPM2#
20 GND
21 BPM1#
22 GND
23 BPM0#
24 DBA#
25 DBR#
26 VCC
27 VCC
28 VCC

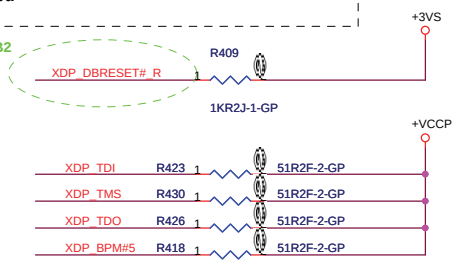
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

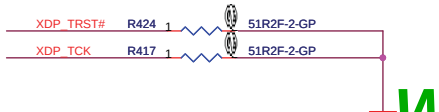
ITP Connector





layout note : R7,R10 Pull near cpu





<Core Design> (Trace R310 with in 200ps (~1") to CPU

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Title	Penryn(1/3)-AGTL+/XDP	
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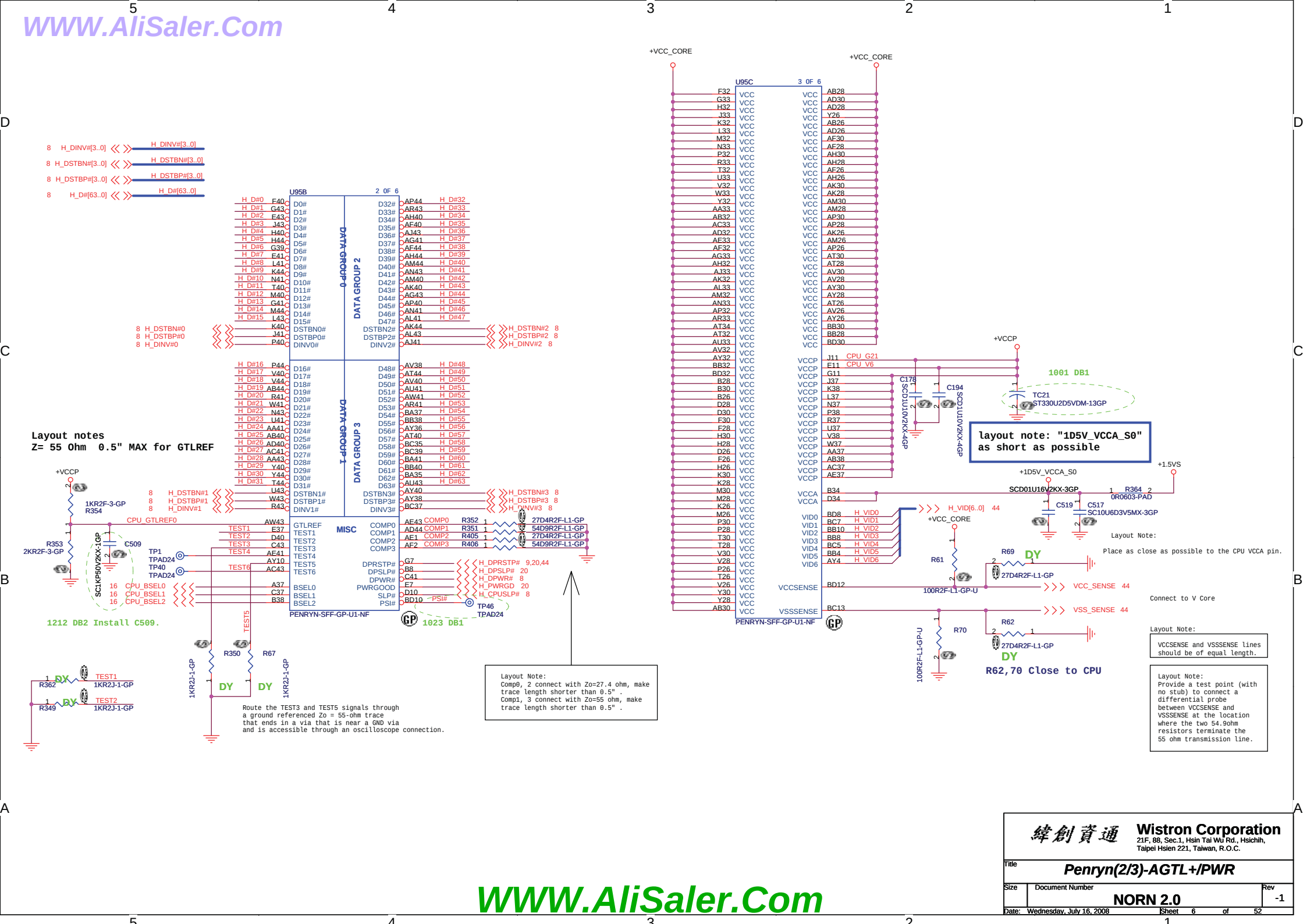

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Title	Penryn(2/3)-AGTL+/PWR	
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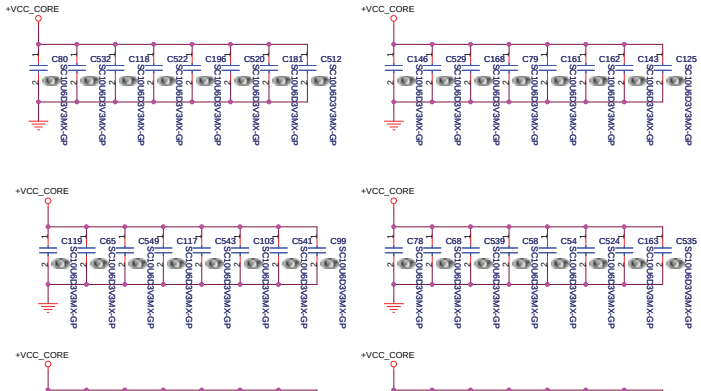
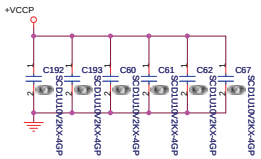
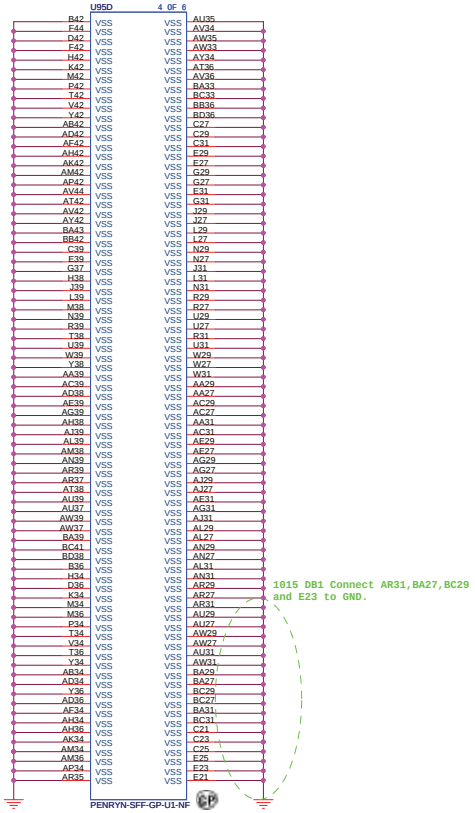
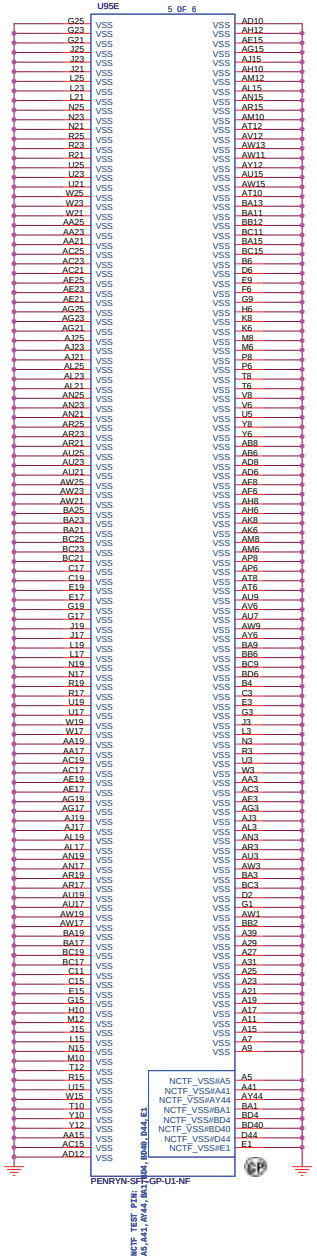
Place these inside socket cavity on L8(North side Secondary)

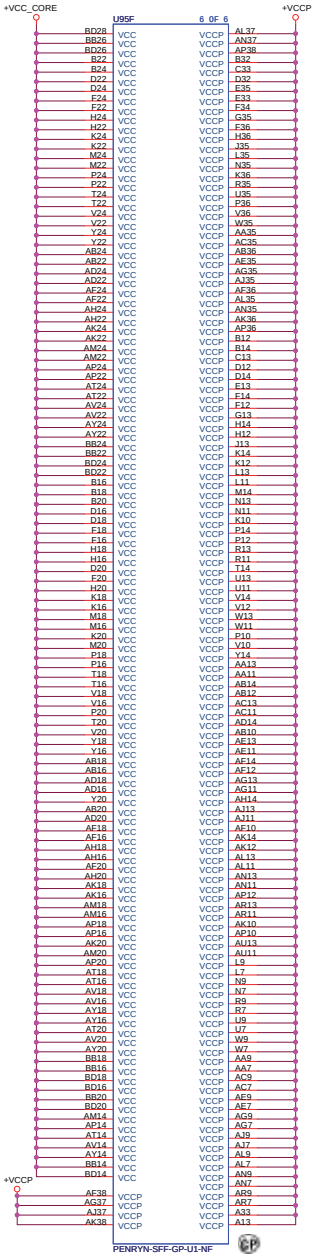


Place these inside socket cavity on L8(North side Secondary)









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Title: Penryn(3/3)-GND&Bypass		
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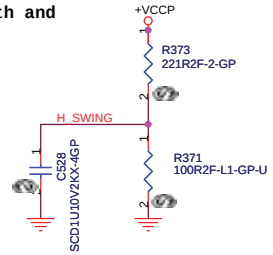
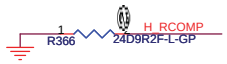
H_SWING routing Trace width and Spacing use 10 / 20 mil

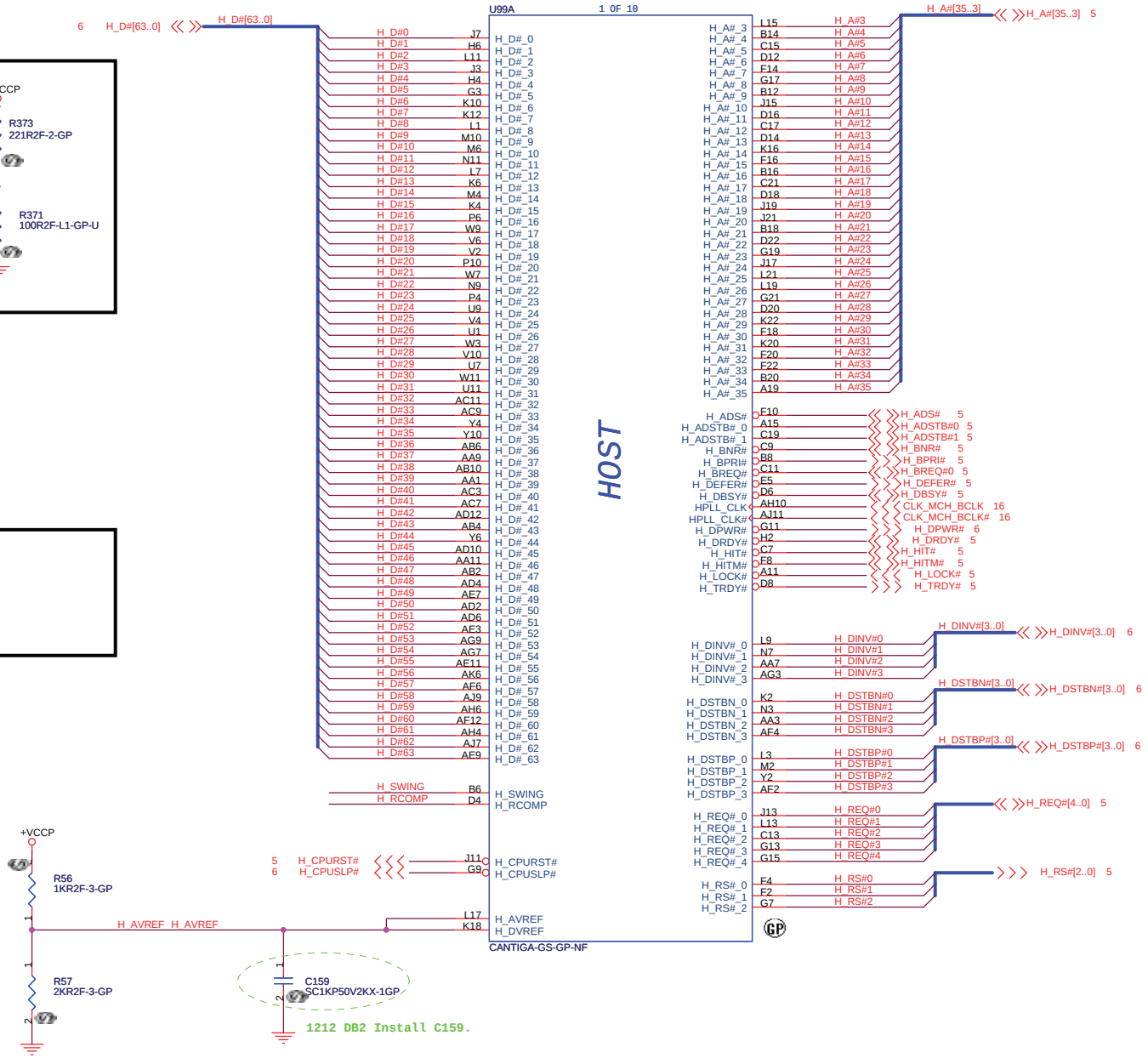
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title	*Cantiga(1/6)-Host*	
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1206 DB2 Not install R509, R510 and R511.

Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

FSB setting

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Teenah = 4.02K
Cantiga = 2.2K

PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Teenah = 4.02K
Cantiga = 2.2K

1015 DB1 Remove TV-OUT

Teenah 1.25V Rail
Cantiga 1.05V Rail

FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil

Cantiga : 511Ohm
Teenah :392 Ohm

Place Close GMCH

1015 DB1 Remove R966,R967 and R968.

0120 SI1

CRT Termination/EMI Filter
T-Filter network should be placed near CANTIGA.

0418 SI2b Change L15, L17 and L18 from 120nH to 39nH for solving RGB rising/falling time failed issue.

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Title: Cantiga(2/6)-LVDS/VGA
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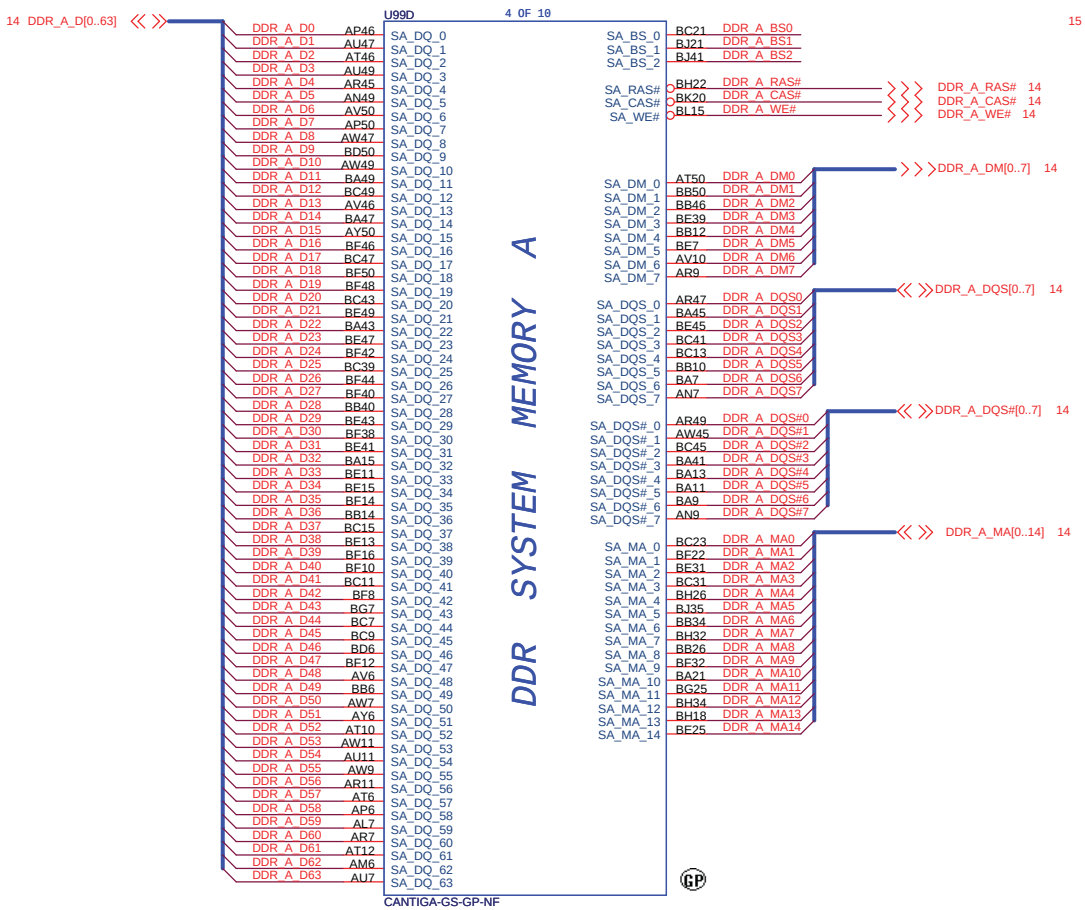

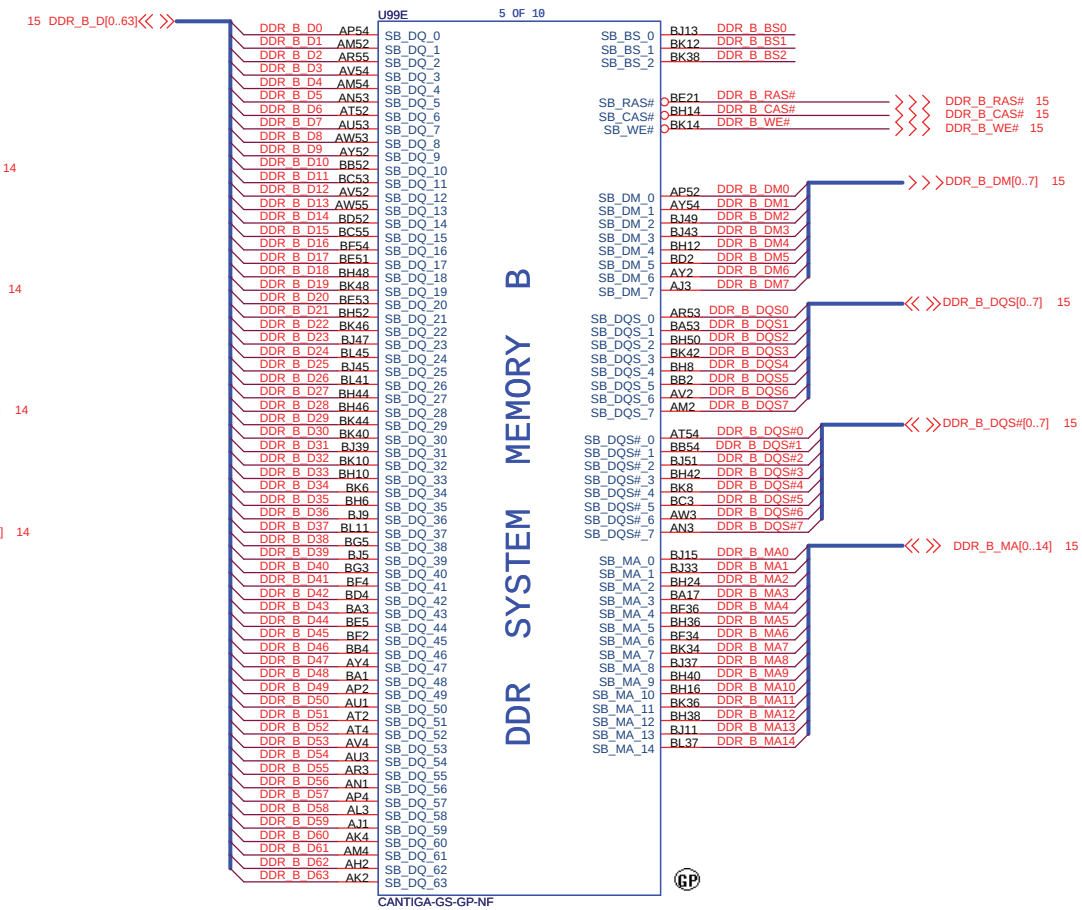

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Title: ***Cantiga(3/6)-DDR2***

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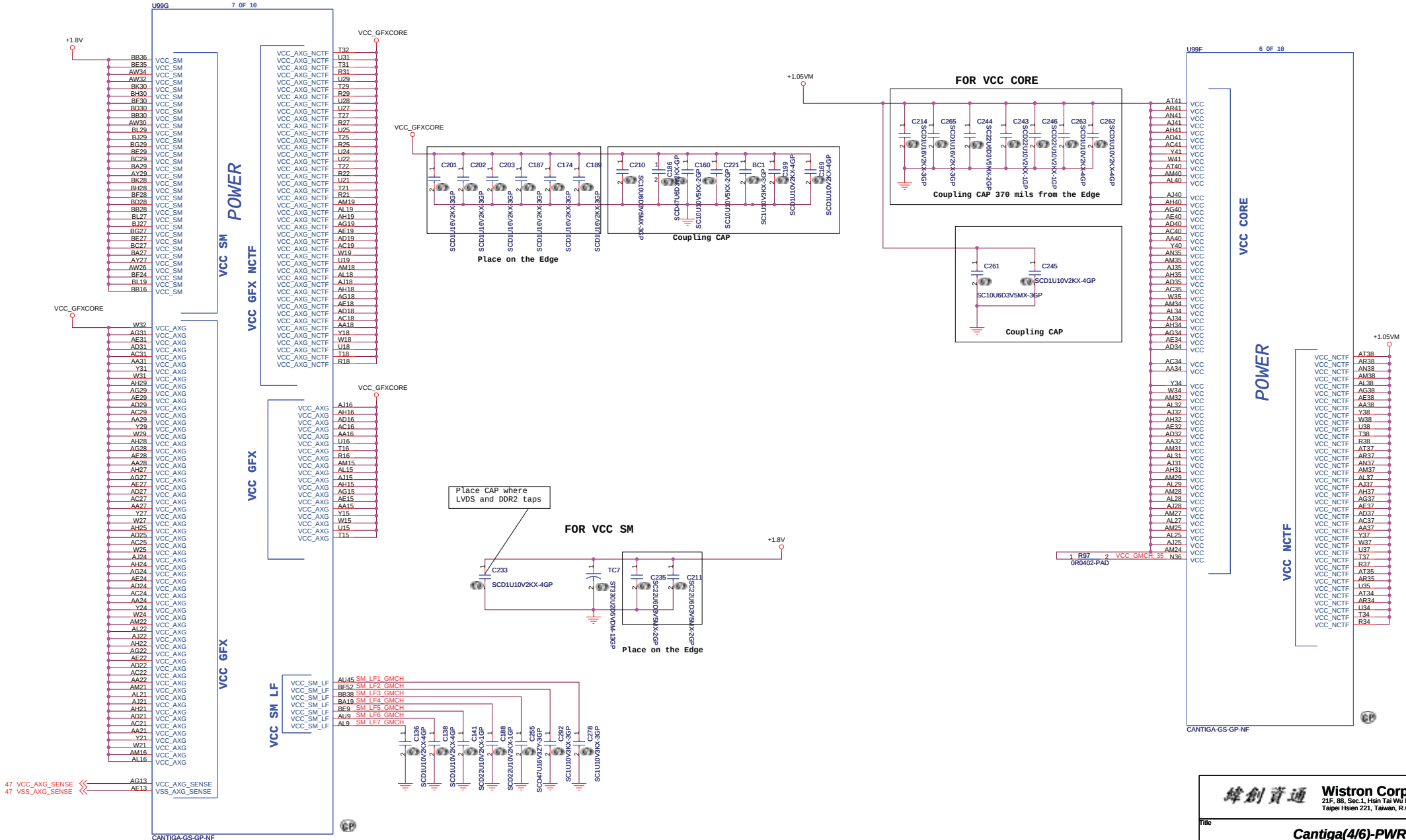

Title	Cantiga(4/6)-PWR
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VCC_GFXCORE setting to 1.25V for teenah

80mA

1001 DB1 Change R75 to 0805 size.

10mA

180ohm 100MHz

852mA

350mA

120ohm 100MHz

220ohm 100MHz

200mA

100mA

106mA

1782mA

456mA

1001 DB1_Change R535 to 0805 size.

0124 SI1

For Teenah, please tie the above to 1.25V rail
For Cantiga, please tie the above to 1.05V rail.

VCCD_HPLL(AF1) & CL_VREF(AH34)
are connected to 1.25V on Teenah as indicated on ERB

1D8V=1.8V_S4

For Discrete change
C166 to 0 ohm

POWER

CANTIGA-GS-GP-NF

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Title: Cantiga(5/6)-PWR&Bypass	
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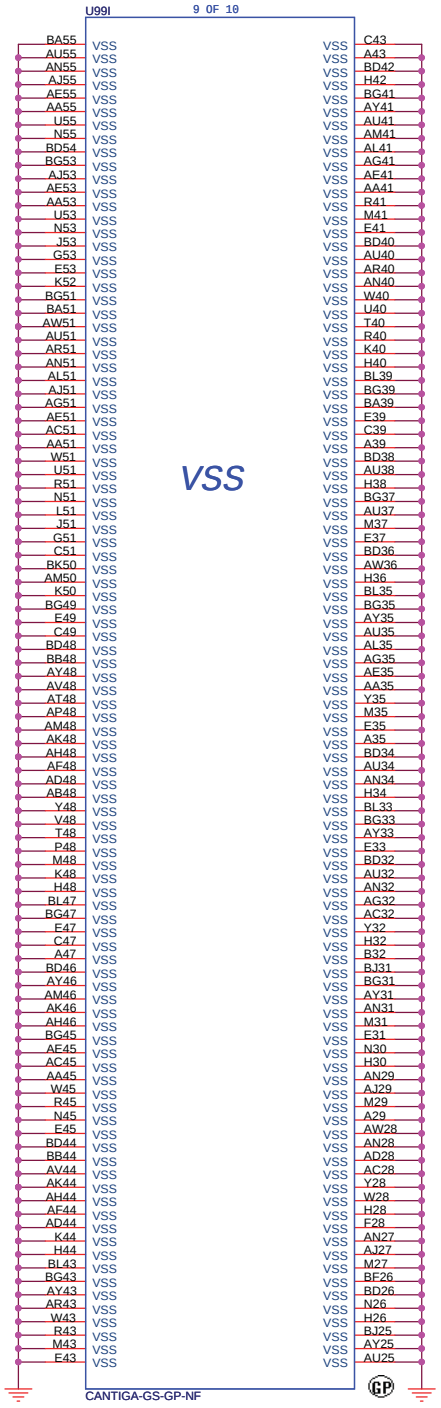
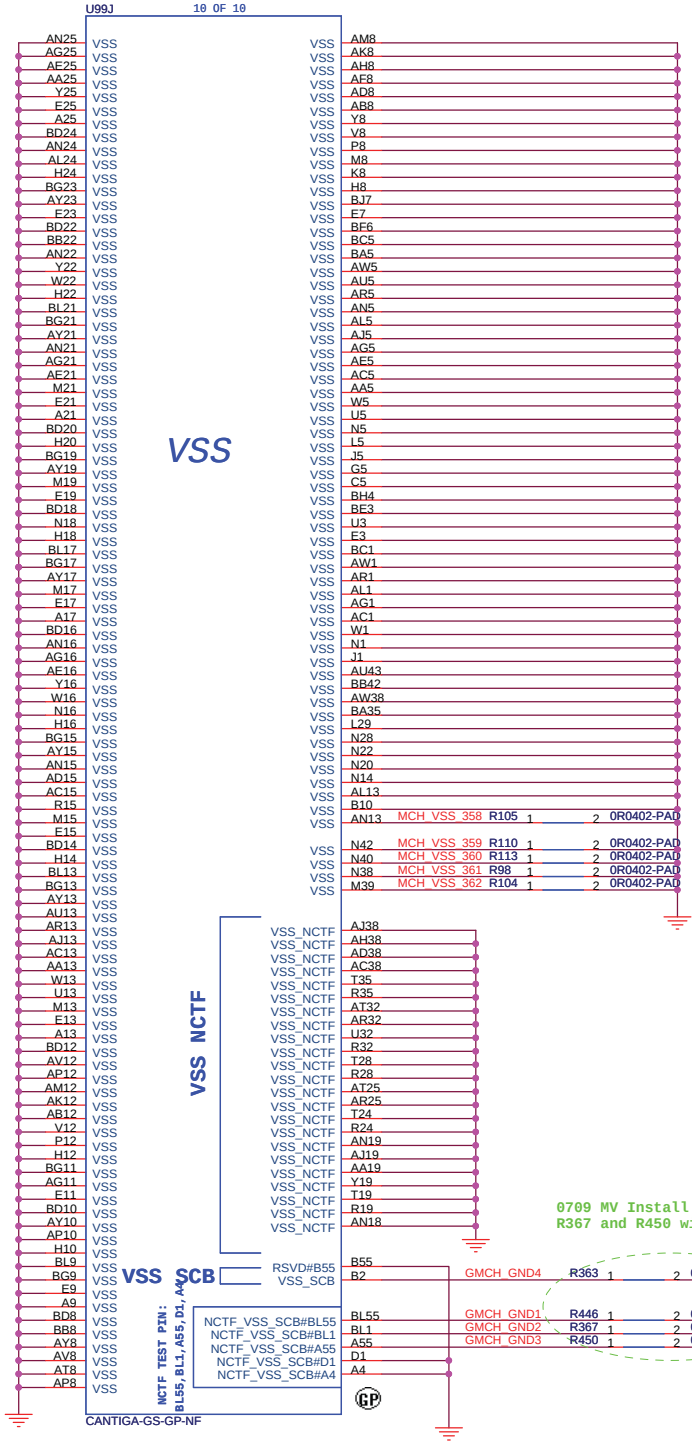
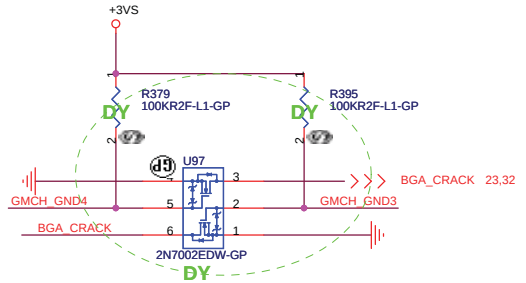
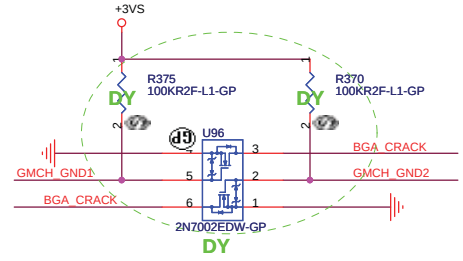






0709 MV Not install U97, U96, R379, R395, R375 and R370.



0709 MV Install R363, R446, R367 and R450 with 0402_0 ohm pads.

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Title	Cantiga(6/6)-GND	
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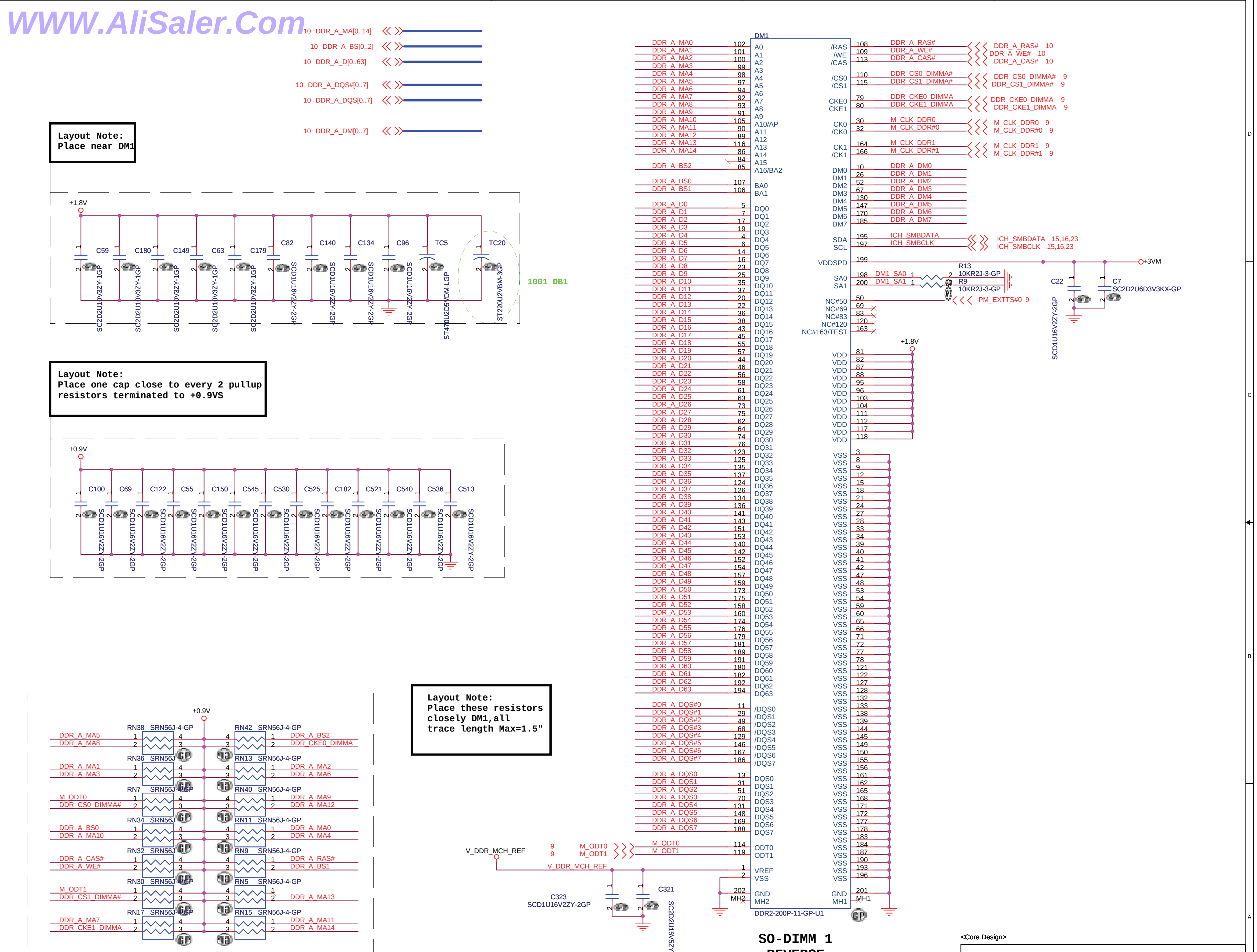
10 DDR_A_MA[0..14]
10 DDR_A_BS[0..2]
10 DDR_A_D[0..63]
10 DDR_A_DQS#[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_DM[0..7]
Layout Note:
Place near DM1
+1.8V
C59 C180 C149 C63 C179 C82 C140 C134 C96 TC5 TC20
SC2D2U10V3ZY-1GP
SCD1U16V2ZY-2GP
ST470U2D5VDM-LGP
ST220U2VBM-3GP
1001 DB1
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9V
C100 C69 C122 C55 C150 C545 C530 C525 C182 C521 C540 C536 C513
SCD1U16V2ZY-2GP
DM1
DDR_A_MA0 ... DDR_A_MA14 — A0 ... A15, A10/AP
DDR_A_BS2 — A16/BA2
DDR_A_BS0 — BA0
DDR_A_BS1 — BA1
DDR_A_D0 ... DDR_A_D63 — DQ0 ... DQ63
DDR_A_DQS#0 ... DDR_A_DQS#7 — /DQS0 ... /DQS7
DDR_A_DQS0 ... DDR_A_DQS7 — DQS0 ... DQS7
M_ODT0 — ODT0
M_ODT1 — ODT1
9 M_ODT0
9 M_ODT1
V_DDR_MCH_REF — VREF
VSS
GND MH2
GND MH1
DDR2-200P-11-GP-U1
C323 SCD1U16V2ZY-2GP
C321 SC2D2U16V5ZY-2GP
/RAS — DDR_A_RAS# — DDR_A_RAS# 10
/WE — DDR_A_WE# — DDR_A_WE# 10
/CAS — DDR_A_CAS# — DDR_A_CAS# 10
/CS0 — DDR_CS0_DIMMA# — DDR_CS0_DIMMA# 9
/CS1 — DDR_CS1_DIMMA# — DDR_CS1_DIMMA# 9
CKE0 — DDR_CKE0_DIMMA — DDR_CKE0_DIMMA 9
CKE1 — DDR_CKE1_DIMMA — DDR_CKE1_DIMMA 9
CK0 — M_CLK_DDR0 — M_CLK_DDR0 9
/CK0 — M_CLK_DDR#0 — M_CLK_DDR#0 9
CK1 — M_CLK_DDR1 — M_CLK_DDR1 9
/CK1 — M_CLK_DDR#1 — M_CLK_DDR#1 9
DM0 ... DM7 — DDR_A_DM0 ... DDR_A_DM7
SDA — ICH_SMBDATA — ICH_SMBDATA 15,16,23
SCL — ICH_SMBCLK — ICH_SMBCLK 15,16,23
VDDSPD — +3VM
SA0 — DM1_SA0 — R13 10KR2J-3-GP
SA1 — DM1_SA1 — R9 10KR2J-3-GP
NC#50 — PM_EXTTS#0 9
NC#69 NC#83 NC#120 NC#163/TEST
C22 SCD1U16V2ZY-2GP
C7 SC2D2U6D3V3KX-GP
+1.8V VDD
VSS
+0.9V
RN38 SRN56J-4-GP DDR_A_MA5 DDR_A_MA8
RN42 SRN56J-4-GP DDR_A_BS2 DDR_CKE0_DIMMA
RN36 SRN56J DDR_A_MA1 DDR_A_MA3
RN13 SRN56J-4-GP DDR_A_MA2 DDR_A_MA6
RN7 SRN56J-4-GP M_ODT0 DDR_CS0_DIMMA#
RN40 SRN56J-4-GP DDR_A_MA9 DDR_A_MA12
RN34 SRN56J DDR_A_BS0 DDR_A_MA10
RN11 SRN56J-4-GP DDR_A_MA0 DDR_A_MA4
RN32 SRN56J DDR_A_CAS# DDR_A_WE#
RN9 SRN56J-4-GP DDR_A_RAS# DDR_A_BS1
RN30 SRN56J-4-GP M_ODT1 DDR_CS1_DIMMA#
RN5 SRN56J-4-GP DDR_A_MA13
RN17 SRN56J-4-GP DDR_A_MA7 DDR_CKE1_DIMMA
RN15 SRN56J-4-GP DDR_A_MA11 DDR_A_MA14
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
SO-DIMM 1
REVERSE
Foxcon Black
62.10017.E11

<Core Design>

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Title	DDRII-SODIMM SLOT1
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10 DDR_B_MA[0..14]
10 DDR_B_BS[0..2]
10 DDR_B_D[0..63]
10 DDR_B_DQS#[0..7]
10 DDR_B_DQS[0..7]
10 DDR_B_DM[0..7]

Layout Note:
Place near DM2

+1.8V
C77 C171 C70 C175 C66 C135 C137 C106 C116
SC2D2U10V2ZY-1GP
SCD1U16V2ZY-2GP

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9V
C523 C185 C165 C142 C121 C101 C81 C516 C548 C542 C538 C533 C527
SCD1U16V2ZY-2GP

Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"

+0.9V
RN35 SRN56J-4-GP DDR_B_MA0 DDR_B_BS1 DDR_B_MA8 DDR_B_MA9
RN4 SRN56J-4-GP DDR_B_CAS# DDR_B_WE# DDR_B_MA10 DDR_B_MA1
RN41 SRN56J-4-GP DDR_B_MA14 DDR_B_MA11 DDR_B_MA7 DDR_B_MA6
RN6 SRN56J-4-GP DDR_B_BS0 M_ODT3 DDR_B_MA4 DDR_B_MA2
RN43 SRN56J-4-GP DDR_CKE3_DIMMB DDR_B_MA3 DDR_CS3_DIMMB#
RN31 SRN56J-4-GP M_ODT2 DDR_B_MA13 DDR_B_MA5 DDR_CKE2_DIMMB
RN33 SRN56J-4-GP DDR_B_RAS# DDR_CS2_DIMMB# DDR_B_MA12 DDR_B_BS2
RN14 RN10 RN39 RN37 RN8 RN12 RN16

V_DDR_MCH_REF
C327 C324
SCD1U16V2ZY-2GP
SC2D2U16V5ZY-2GP

DM2

DDR_B_MA0	102	A0	RAS#	108	DDR_B_RAS# 10
DDR_B_MA1	101	A1	WE#	109	DDR_B_WE# 10
DDR_B_MA2	100	A2	CAS#	113	DDR_B_CAS# 10
DDR_B_MA3	99	A3			
DDR_B_MA4	98	A4	CS0#	110	DDR_CS2_DIMMB# 9
DDR_B_MA5	97	A5	CS1#	115	DDR_CS3_DIMMB# 9
DDR_B_MA6	94	A6			
DDR_B_MA7	92	A7	CKE0	79	DDR_CKE2_DIMMB 9
DDR_B_MA8	93	A8	CKE1	80	DDR_CKE3_DIMMB 9
DDR_B_MA9	91	A9			
DDR_B_MA10	105	A10/AP	CK0	30	M_CLK_DDR2 9
DDR_B_MA11	90	A11	CK0#	32	M_CLK_DDR#2 9
DDR_B_MA12	89	A12			
DDR_B_MA13	116	A13	CK1	164	M_CLK_DDR3 9
DDR_B_MA14	86	A14	CK1#	166	M_CLK_DDR#3 9
	84	A15			
DDR_B_BS2	85	A16/BA2	DM0	10	DDR_B_DM0
			DM1	26	DDR_B_DM1
DDR_B_BS0	107	BA0	DM2	52	DDR_B_DM2
DDR_B_BS1	106	BA1	DM3	67	DDR_B_DM3
			DM4	130	DDR_B_DM4
DDR_B_D0	5	DQ0	DM5	147	DDR_B_DM5
DDR_B_D1	7	DQ1	DM6	170	DDR_B_DM6
DDR_B_D2	17	DQ2	DM7	185	DDR_B_DM7
DDR_B_D3	19	DQ3			
DDR_B_D4	4	DQ4	SDA	195	ICH_SMBDATA 14,16,23
DDR_B_D5	6	DQ5	SCL	197	ICH_SMBCLK 14,16,23
DDR_B_D6	14	DQ6			
DDR_B_D7	16	DQ7	VDDSPD	199	+3VM
DDR_B_D8	23	DQ8			
DDR_B_D9	25	DQ9	SA0	198	DM2_SA0 R329 10KR2J-3-GP
DDR_B_D10	35	DQ10	SA1	200	DM2_SA1 R328 10KR2J-3-GP +3VM
DDR_B_D11	37	DQ11			
DDR_B_D12	20	DQ12	NC#50	50	PM_EXTTS#1 9
DDR_B_D13	22	DQ13	NC#69	69	
DDR_B_D14	36	DQ14	NC#83	83	
DDR_B_D15	38	DQ15	NC#120	120	
DDR_B_D16	43	DQ16	NC#163/TEST	163	
DDR_B_D17	45	DQ17			
DDR_B_D18	55	DQ18	VDD	81	+1.8V
DDR_B_D19	57	DQ19	VDD	82	
DDR_B_D20	44	DQ20	VDD	87	
DDR_B_D21	46	DQ21	VDD	88	
DDR_B_D22	56	DQ22	VDD	95	
DDR_B_D23	58	DQ23	VDD	96	
DDR_B_D24	61	DQ24	VDD	103	
DDR_B_D25	63	DQ25	VDD	104	
DDR_B_D26	73	DQ26	VDD	111	
DDR_B_D27	75	DQ27	VDD	112	
DDR_B_D28	62	DQ28	VDD	117	
DDR_B_D29	64	DQ29	VDD	118	
DDR_B_D30	74	DQ30	VDD		
DDR_B_D31	76	DQ31			
DDR_B_D32	123	DQ32	VSS	3	
DDR_B_D33	125	DQ33	VSS	8	
DDR_B_D34	135	DQ34	VSS	9	
DDR_B_D35	137	DQ35	VSS	12	
DDR_B_D36	124	DQ36	VSS	15	
DDR_B_D37	126	DQ37	VSS	18	
DDR_B_D38	134	DQ38	VSS	21	
DDR_B_D39	136	DQ39	VSS	24	
DDR_B_D40	141	DQ40	VSS	27	
DDR_B_D41	143	DQ41	VSS	28	
DDR_B_D42	151	DQ42	VSS	33	
DDR_B_D43	153	DQ43	VSS	34	
DDR_B_D44	140	DQ44	VSS	39	
DDR_B_D45	142	DQ45	VSS	40	
DDR_B_D46	152	DQ46	VSS	41	
DDR_B_D47	154	DQ47	VSS	42	
DDR_B_D48	157	DQ48	VSS	47	
DDR_B_D49	159	DQ49	VSS	48	
DDR_B_D50	173	DQ50	VSS	53	
DDR_B_D51	175	DQ51	VSS	54	
DDR_B_D52	158	DQ52	VSS	59	
DDR_B_D53	160	DQ53	VSS	60	
DDR_B_D54	174	DQ54	VSS	65	
DDR_B_D55	176	DQ55	VSS	66	
DDR_B_D56	179	DQ56	VSS	71	
DDR_B_D57	181	DQ57	VSS	72	
DDR_B_D58	189	DQ58	VSS	77	
DDR_B_D59	191	DQ59	VSS	78	
DDR_B_D60	180	DQ60	VSS	121	
DDR_B_D61	182	DQ61	VSS	122	
DDR_B_D62	192	DQ62	VSS	127	
DDR_B_D63	194	DQ63	VSS	128	
			VSS	132	
DDR_B_DQS#0	11	DQS0#	VSS	133	
DDR_B_DQS#1	29	DQS1#	VSS	138	
DDR_B_DQS#2	49	DQS2#	VSS	139	
DDR_B_DQS#3	68	DQS3#	VSS	144	
DDR_B_DQS#4	129	DQS4#	VSS	145	
DDR_B_DQS#5	146	DQS5#	VSS	149	
DDR_B_DQS#6	167	DQS6#	VSS	150	
DDR_B_DQS#7	186	DQS7#	VSS	155	
			VSS	156	
DDR_B_DQS0	13	DQS0	VSS	161	
DDR_B_DQS1	31	DQS1	VSS	162	
DDR_B_DQS2	51	DQS2	VSS	165	
DDR_B_DQS3	70	DQS3	VSS	168	
DDR_B_DQS4	131	DQS4	VSS	171	
DDR_B_DQS5	148	DQS5	VSS	172	
DDR_B_DQS6	169	DQS6	VSS	177	
DDR_B_DQS7	188	DQS7	VSS	178	
			VSS	183	
M_ODT2	114	OTD0	VSS	184	
M_ODT3	119	OTD1	VSS	187	
			VSS	190	
	1	VREF	VSS	193	
	2	VSS	VSS	196	
	202	GND	GND	201	
	MH1		MH2	MH2	

DDR2-200P-20-GP-U1

SO-DIMM 2
STANDARD

<Core Design>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDRII-SODIMM SLOT2***

Size: Custom | Document Number: **NORN 2.0** | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 15 of 52

CL=20pF±0.2pF

1011 DB1

1017 DB1 Reserve pads.
Place close to U34.

1008 DB1

0513 PV Change C351 and C346 from 27pF to 33pF.

1207 DB2 Change R119 from 22R to 10R.

PCI1/REQ_B#USE for Discrete

1001 DB1 Delete R1016

1129 DB2

Reference 14.318 CLK

Follow Intel CK505

FSA

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

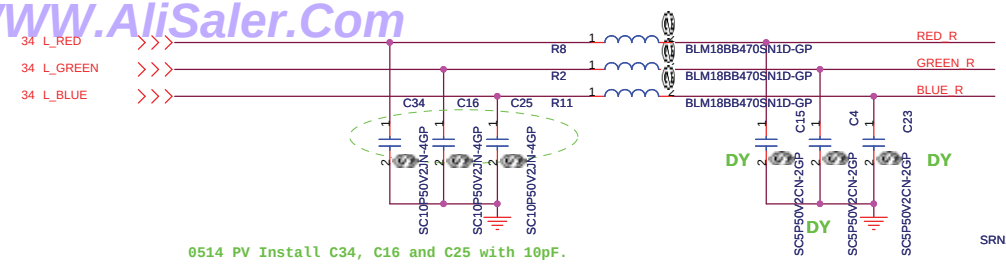
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

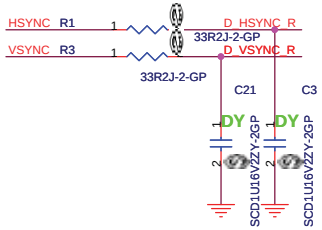
Title: Clock Generator SLG8SP553

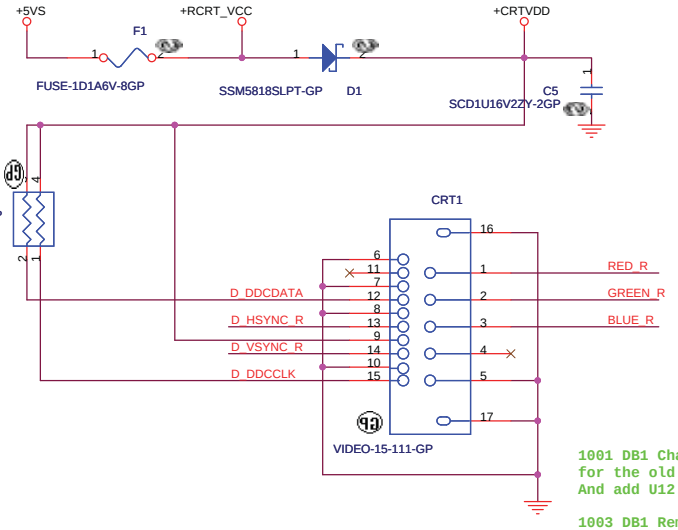
Size | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 16 of 52



0514 PV Install C34, C16 and C25 with 10pF.



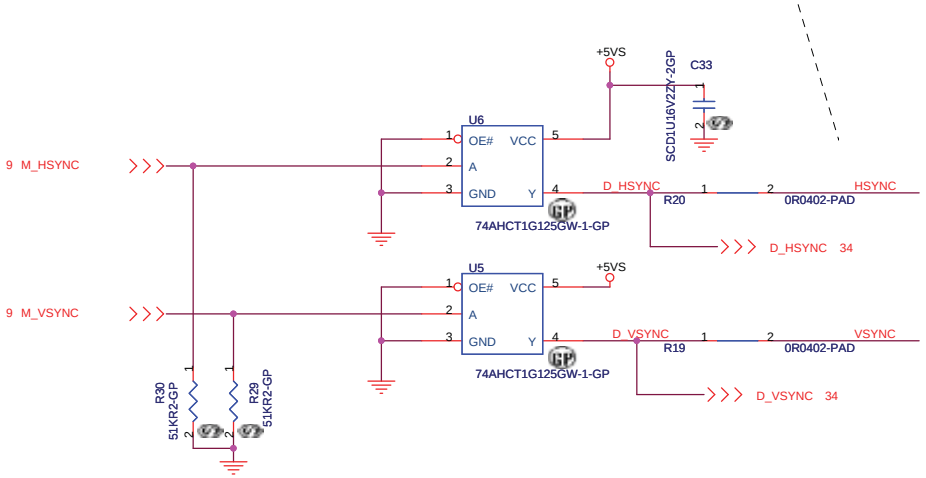


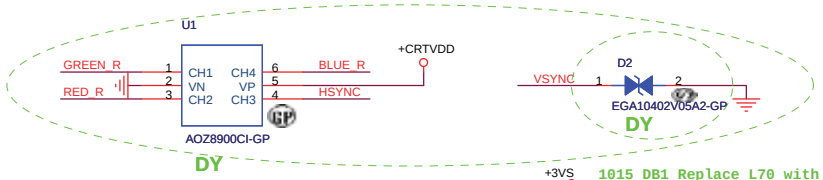
1001 DB1 Change U1 to 83.08900.0AE
for the old part is obsoleted.
And add U12.

1003 DB1 Remove U12 and add L70
for free space and cost down.

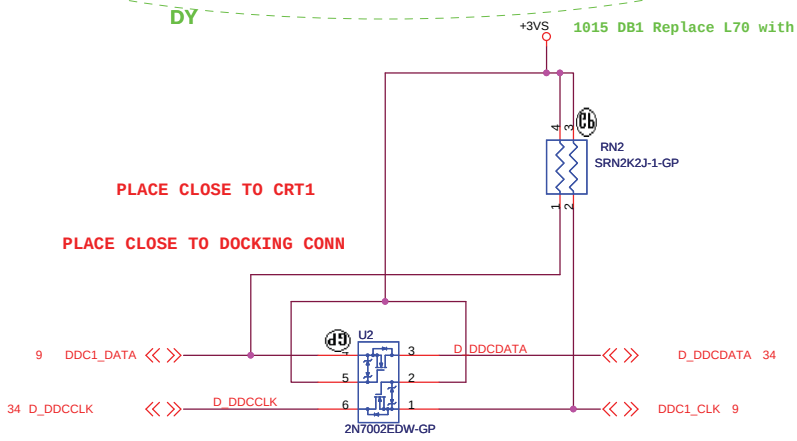
CRT

Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. ,THEN TO SYSTEM CRT CONN.





1015 DB1 Replace L70 with D84.



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV CONNECTOR

Size	Document Number	Rev
A3	NORN 2.0	-1

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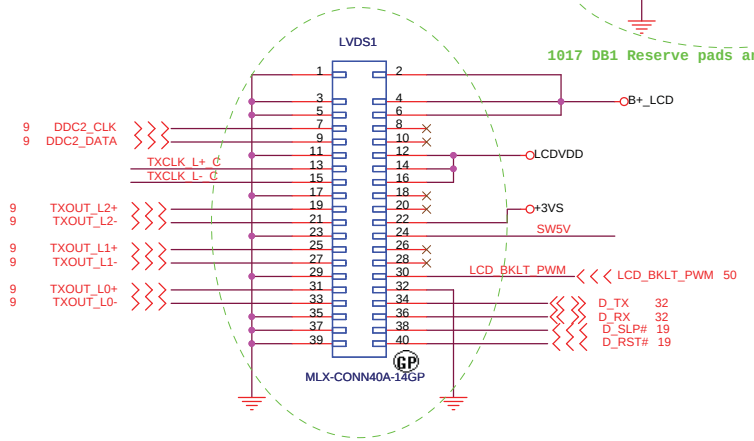
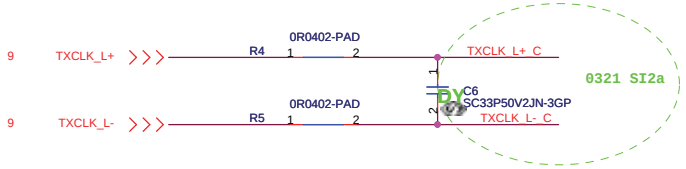
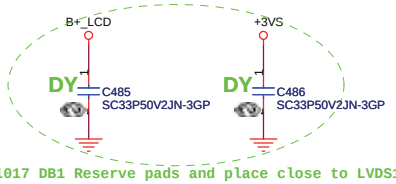
LVDS CONN

1016 DB1 Change the P/N of LVDS.



Near the LVDS1 connector

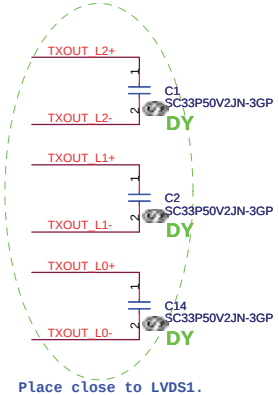




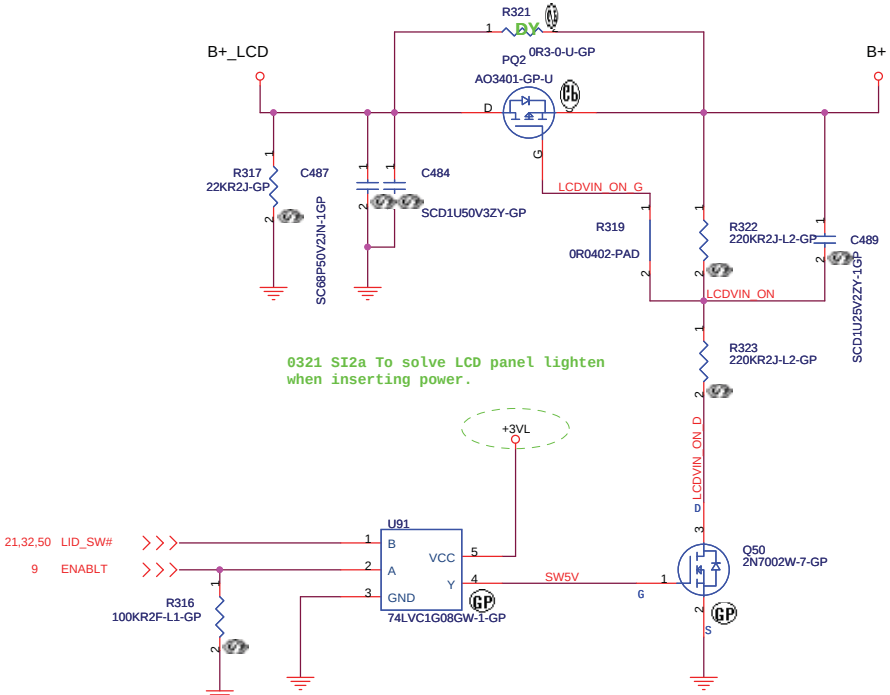
1017 DB1 Reserve pads and place close to LVDS1.

SUPPORT LED INVETER

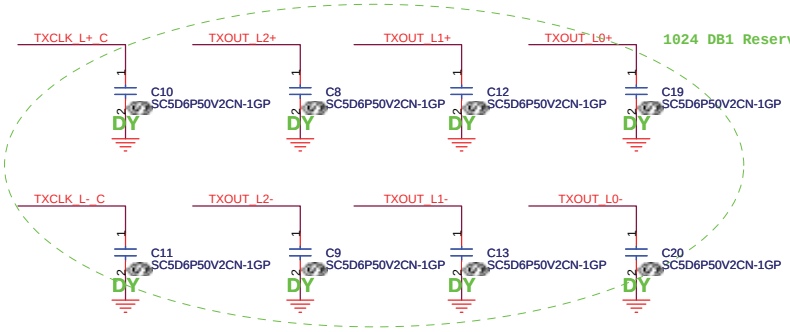
1019 DB1 Reserve C700, C710 and C711 and place near to LVDS1.



Place close to LVDS1.



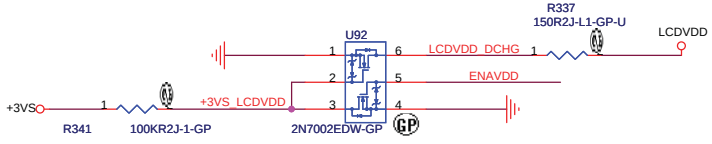
0321 SI2a To solve LCD panel lighten when inserting power.

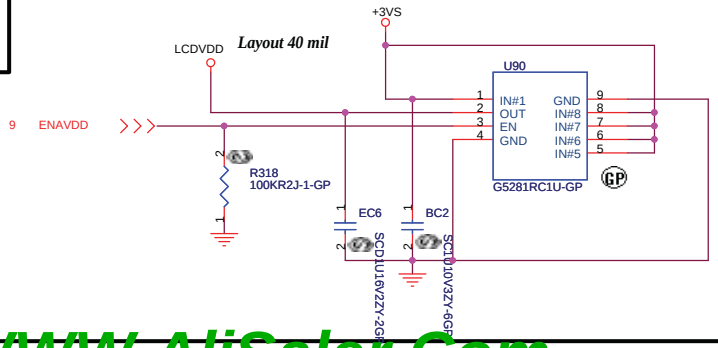


Place close to LVDS1.

1024 DB1 Reserve Pads for RF solution.

LCD POWER CIRCUIT





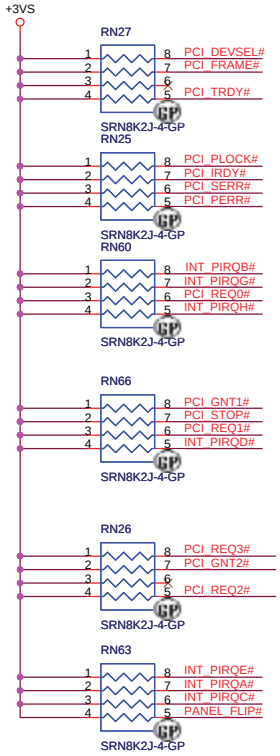
<Core Design>

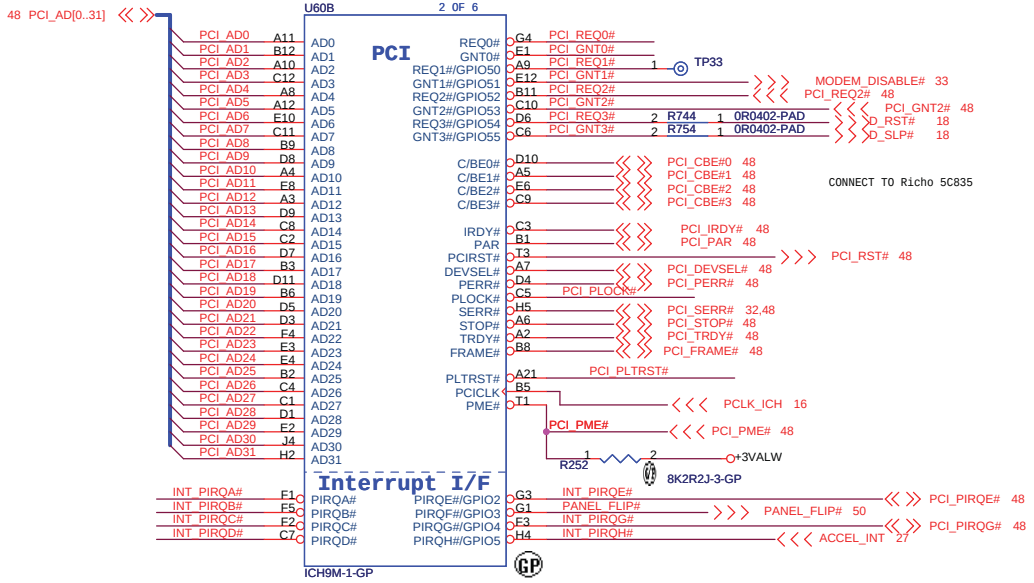
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

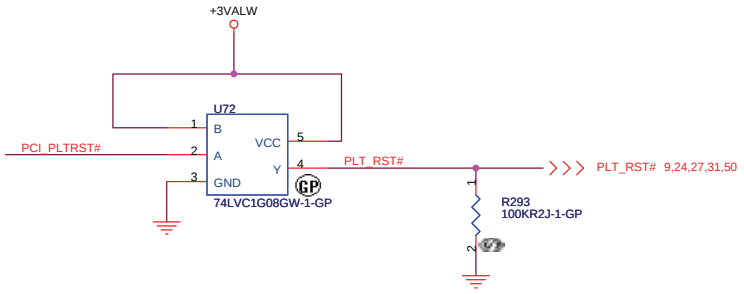
Title: LCD CONN.

Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 18 of 52







BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

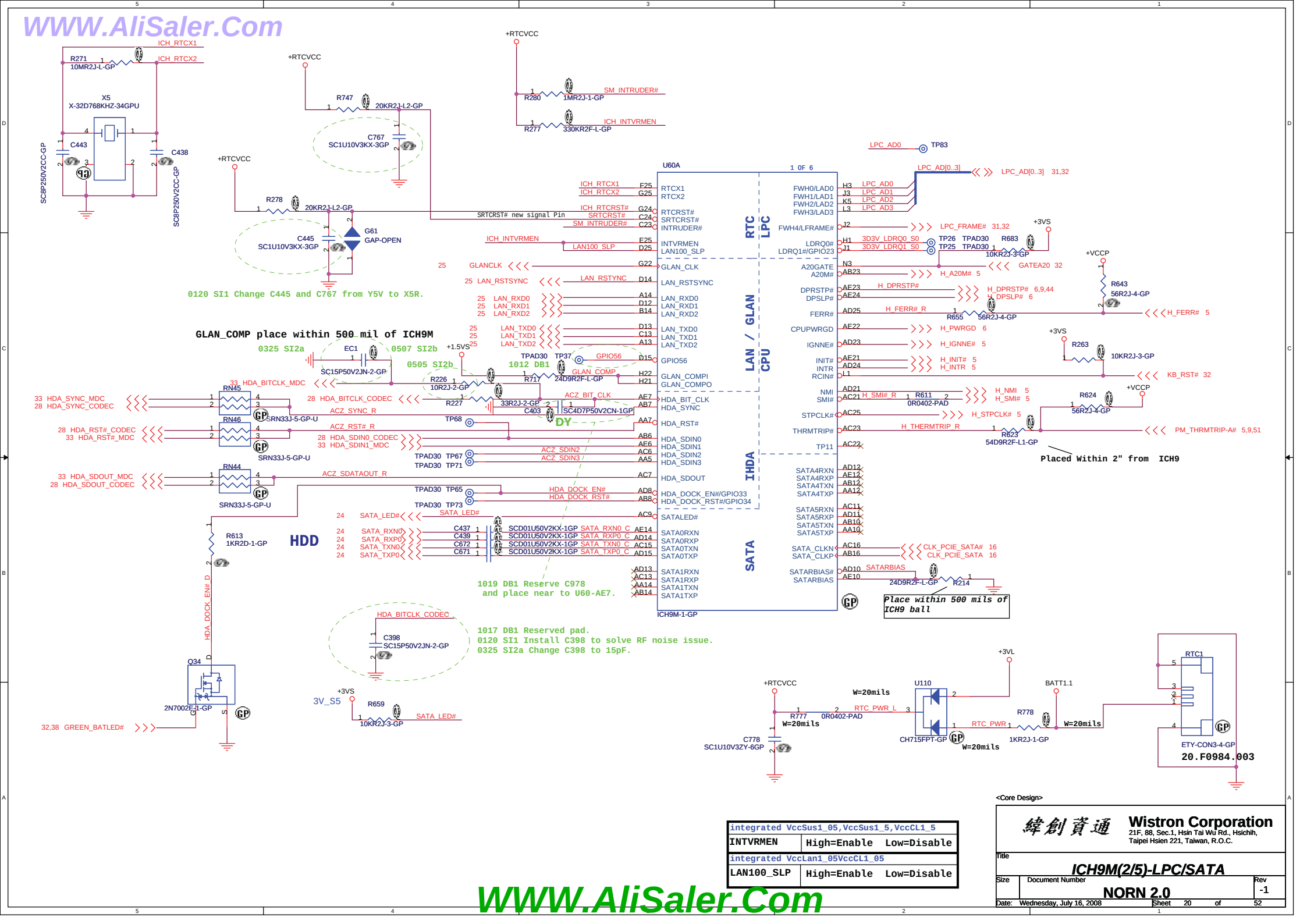
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9M(1/5)-PCI

Size | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 19 of 52



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9M(2/5)-LPC/SATA

Size | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 20 of 52

1129 DB2 Delete pull-high net of GPIO19.

1022 DB1

1129 DB2

1001 DB1

1016 DB1

USB

Pair	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
9	DOCK1
10	WEBCAM
11	DOCK2

U60C — ICH9M-1-GP

SMB: SMBCLK, SMBDATA, LINKALERT#/GPIO60/CLGPIO4, SMLINK0, SMLINK1

SYS GPIO / Power MGT: RI#, SUS_STAT#/LPCPD#, SYS_RESET#, PMSYNC#/GPIO0, SMBALERT#/GPIO11, STP_PCI#/GPIO15, STP_CPU#/GPIO25, CLKRUN#/GPIO32, WAKE#, SERIRQ, THRM#, VRMPWRGD, TP12

GPIO / Controller Link: GPIO1, GPIO6, GPIO7, GPIO8, GPIO12, GPIO13, GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, GPIO27, GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, GPIO49, GPIO57/CLGPIO5

MISC: SPKR, MCH_SYNC#, TP3, TP8, TP9, TP10

SATA GPIO: SATA0GP/GPIO21, SATA1GP/GPIO19, SATA4GP/GPIO36, SATA5GP/GPIO37

iClocks: CLK14, CLK48, SUSCLK

U60D — ICH9M-1-GP

PCI-Express: PERN1–5, PERP1–5, PETN1–5, PETP1–5

Direct Media Interface: DMI0RXN, DMI0RXP, DMI0TXN, DMI0TXP, DMI1RXN, DMI1RXP, DMI1TXN, DMI1TXP, DMI2RXN, DMI2RXP, DMI2TXN, DMI2TXP, DMI3RXN, DMI3RXP, DMI3TXN, DMI3TXP, DMI_CLKN, DMI_CLKP, DMI_ZCOMP, DMI_IRCOMP

SPI: SPI_CLK, SPI_CS0#, SPI_CS1#/GPIO58/CLGPIO6, SPI_MOSI, SPI_MISO

USB: OC0#/GPIO59, OC1#/GPIO40, OC2#/GPIO41, OC3#/GPIO42, OC4#/GPIO43, OC5#/GPIO29, OC6#/GPIO30, OC7#/GPIO31, OC8#/GPIO44, OC9#/GPIO45, OC10#/GPIO46, OC11#/GPIO47, USBRBIAS, USBRBIAS#, USBP0N–USBP11N, USBP0P–USBP11P

WLAN — PCIE_RXN2 / PCIE_RXP2 / PCIE_TXN2 / PCIE_TXP2 — C705 SCD1U10V2KX-5GP, C715 SCD1U10V2KX-5GP

NEW CARD — PCIE_RXN3 / PCIE_RXP3 / PCIE_TXN3 / PCIE_TXP3 — C745 SCD1U10V2KX-5GP, C737 SCD1U10V2KX-5GP

WWAN — PCIE_RXN4 / PCIE_RXP4 / PCIE_TXN4 / PCIE_TXP4 — C733 SCD1U10V2KX-5GP, C724 SCD1U10V2KX-5GP

GLAN — GLAN_RXN / GLAN_RXP / GLAN_TXN / GLAN_TXP — SCD1U16V2KX-3GP, C749 GLAN_TXN_C, C756 GLAN_TXP_C

USB1

NEW/EX-P

WLAN

USB2

BT

WWAN

FP

DK(HUB)

CAM

DK(ODD)

0120 SI1

1205 DB2

1206 DB2

0507 SI2b

1129 DB2

1011 DB1

1005 DB1

0120 SI1 Remove R275.

1206 DB2 — Note: For iTPM option.

1001 DB1 — 1129 DB2 To dupicate with RN56-7 net.

1129 DB2 To dupicate with RP2-1 net.

1129 DB2 Pull OCP# to +3VS for system working slowly issuee.

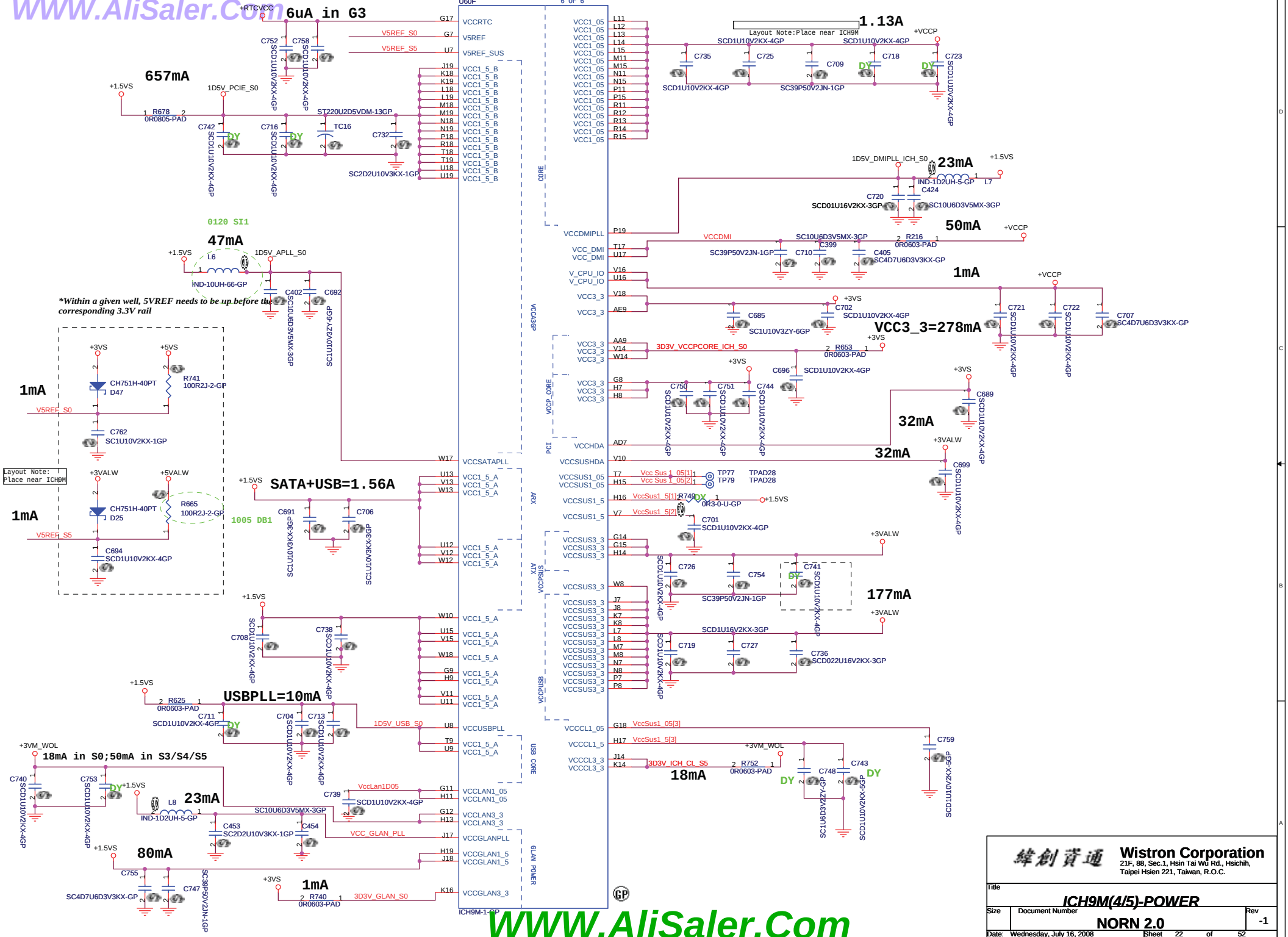
<Core Design>

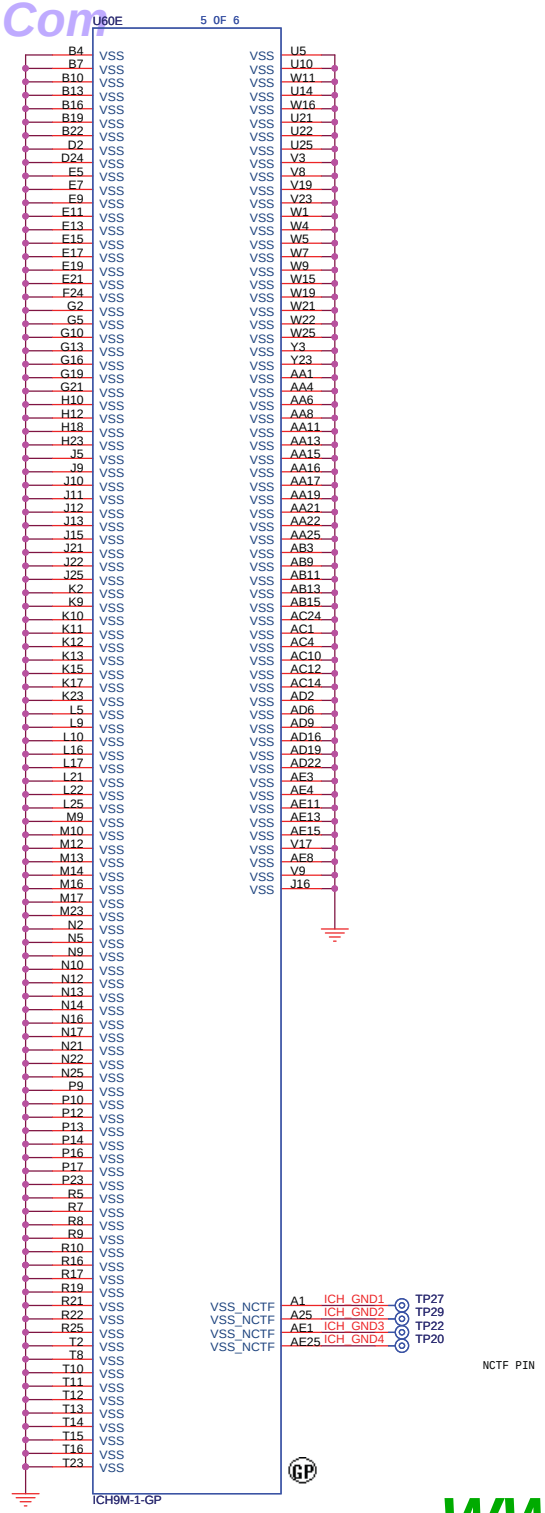
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

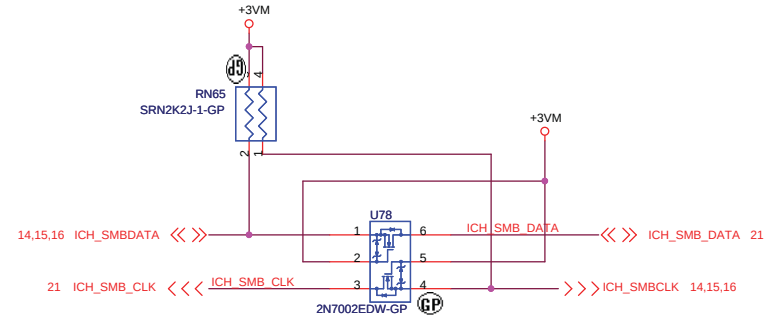
Title: ICH9M(3/5)-GPIO/USB

Size: | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 21 of 52

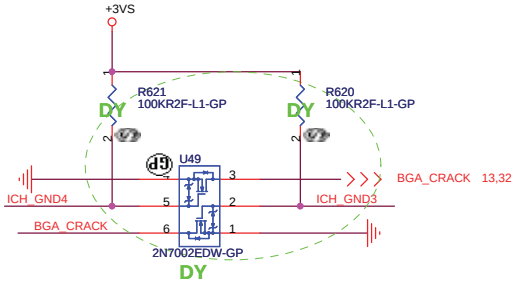




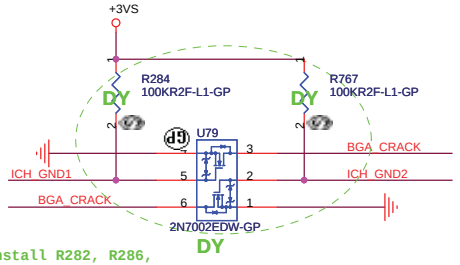


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

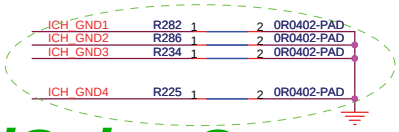
SMBUS



0709 MV Not install U49, U79, R621, R620, R284 and R767.



0709 MV Install R282, R286, R234 and R225 with 0402_0 ohm pads.



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ICH9M(5/5)-GND	
Size	Document Number: NORN 2.0	Rev: -1
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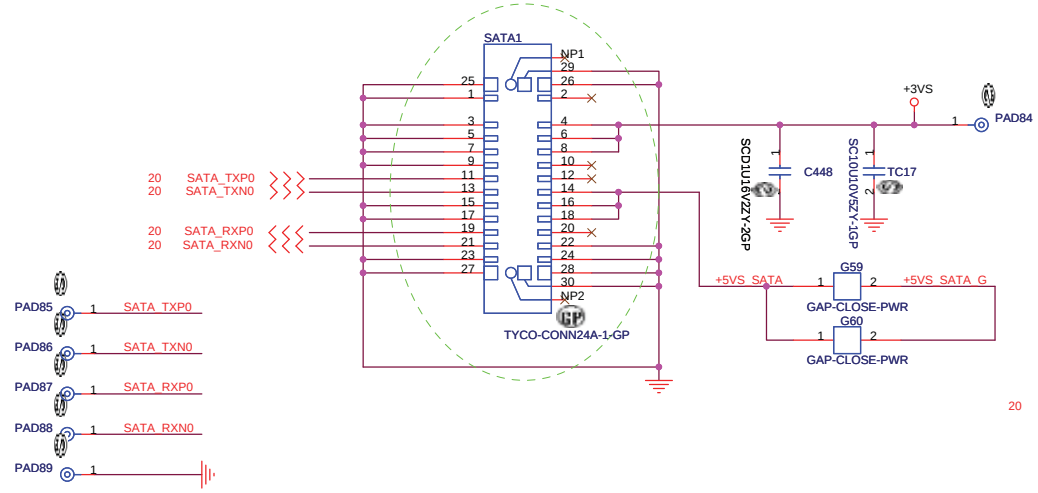
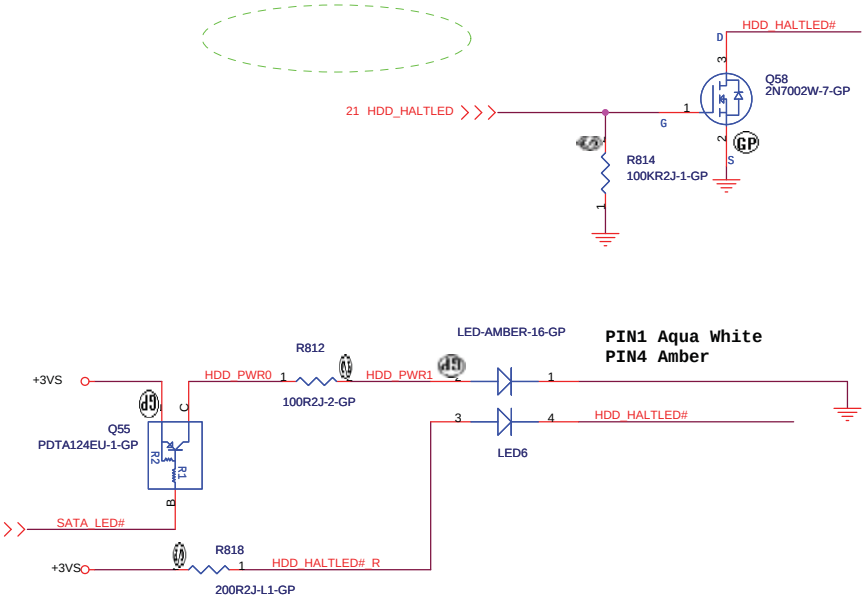
SATA HDD

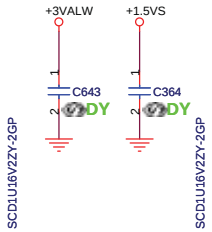
1016 DB1 Change SATA1 connector to 14 pins.
1018 DB1 Change SATA1 connector to 30 pins.
1018 DB1 Change SATA1 connector to 24 pins.



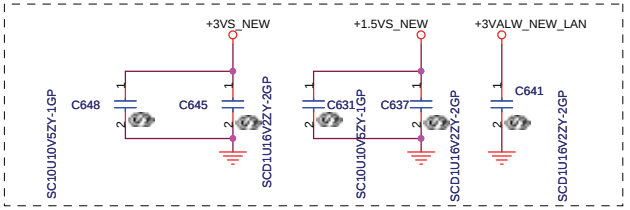
1023 DB1 Remove R384.

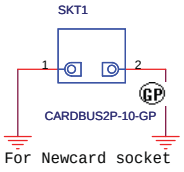


Place them Near to Chip

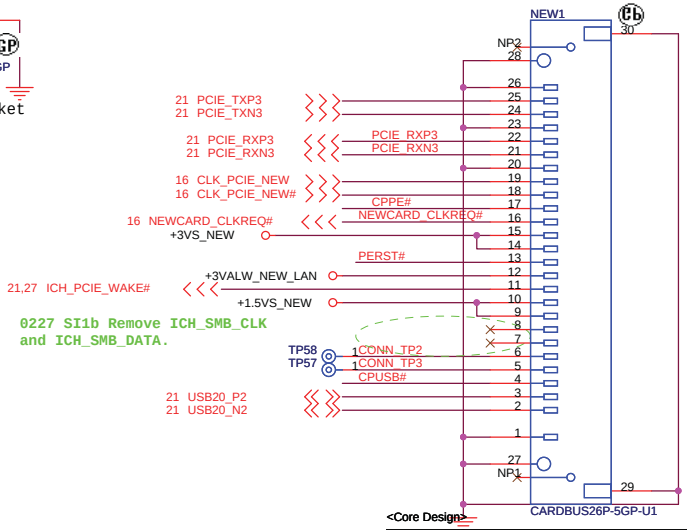


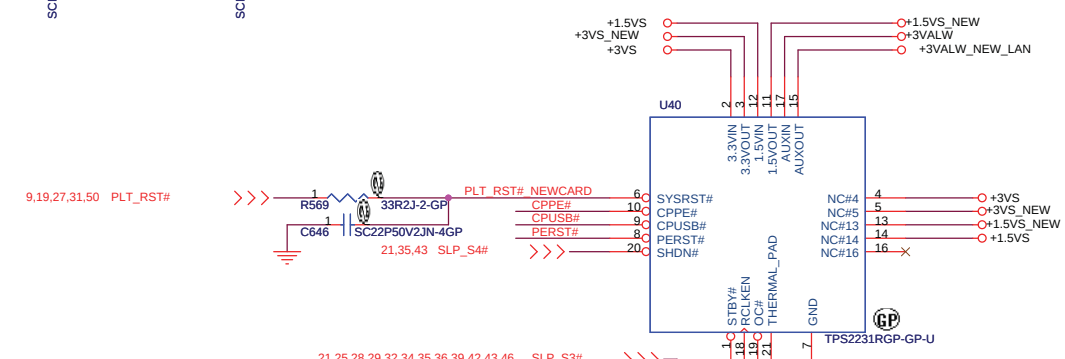
Place them Near to Connector

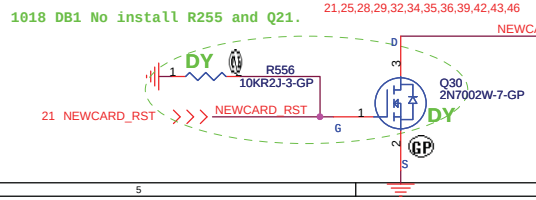




NEWCARD Connector







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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD /NEW CARD CONN.

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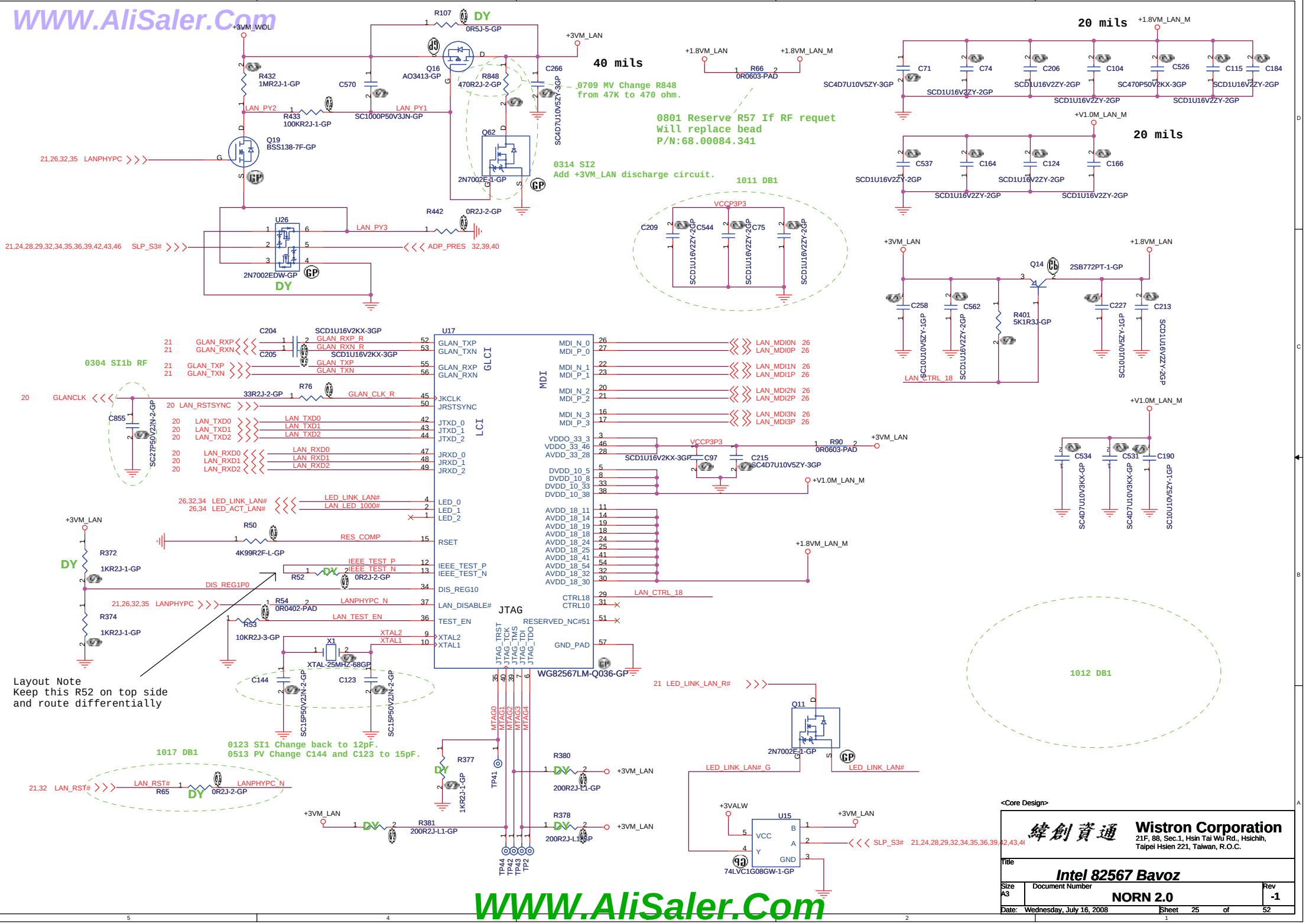

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Intel 82567 Bavoz

Size: A3 | Document Number: NORN 2.0 | Rev: -1

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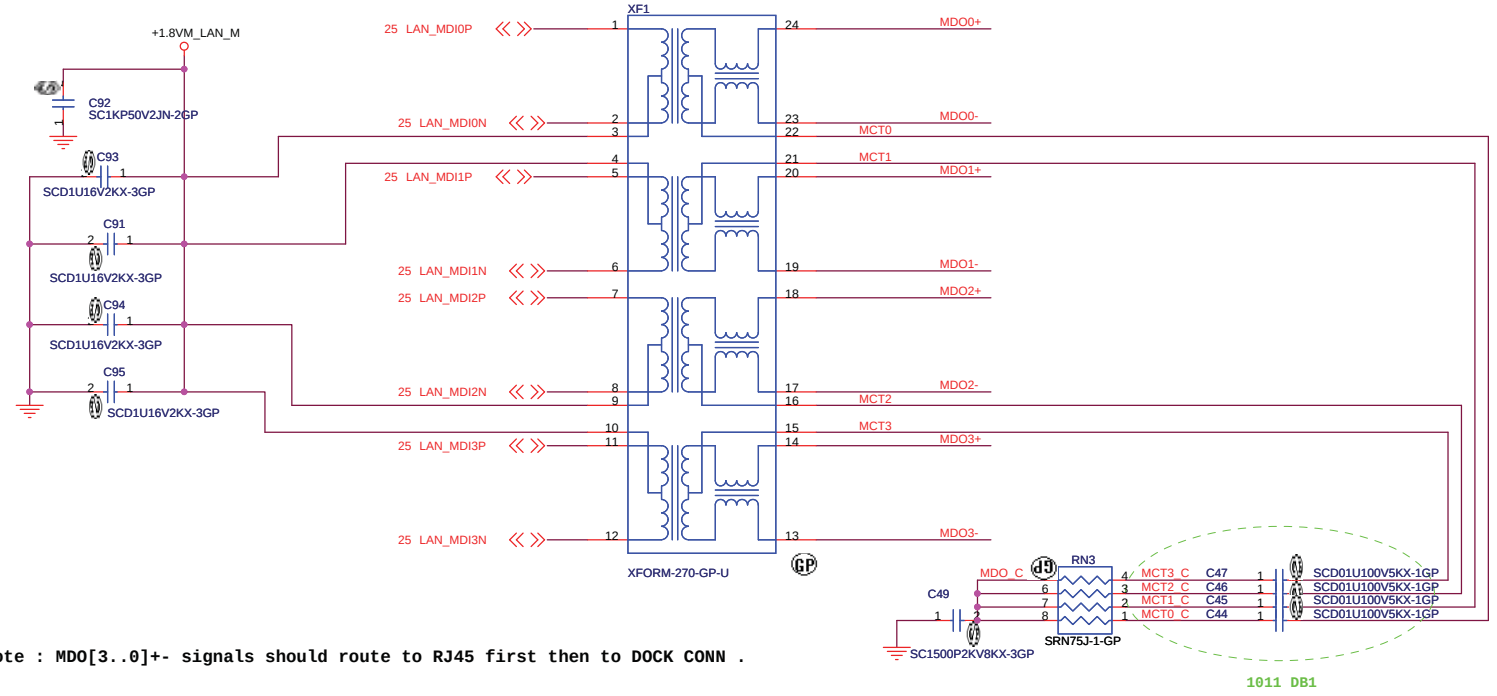
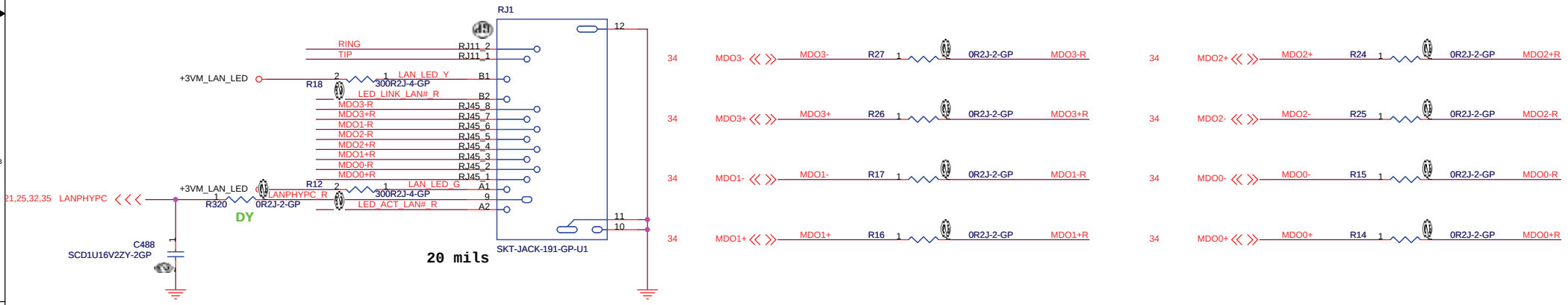
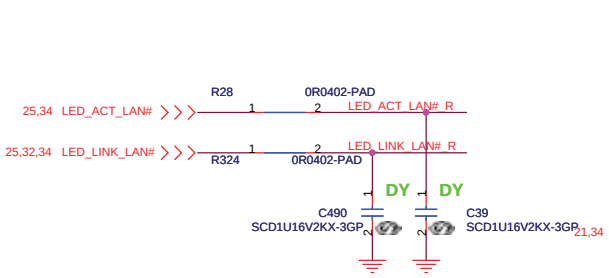
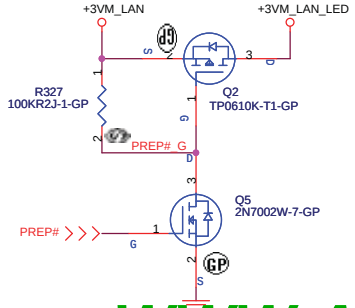


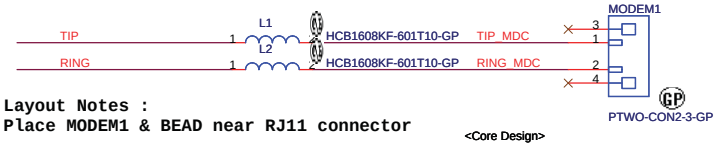
Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .

1011 DB1









Layout Notes :
Place MODEM1 & BEAD near RJ11 connector

3.2 mm keep out on all layers from TIP/RING to all other traces, vias and pads

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Magnetic & RJ45/RJ11***

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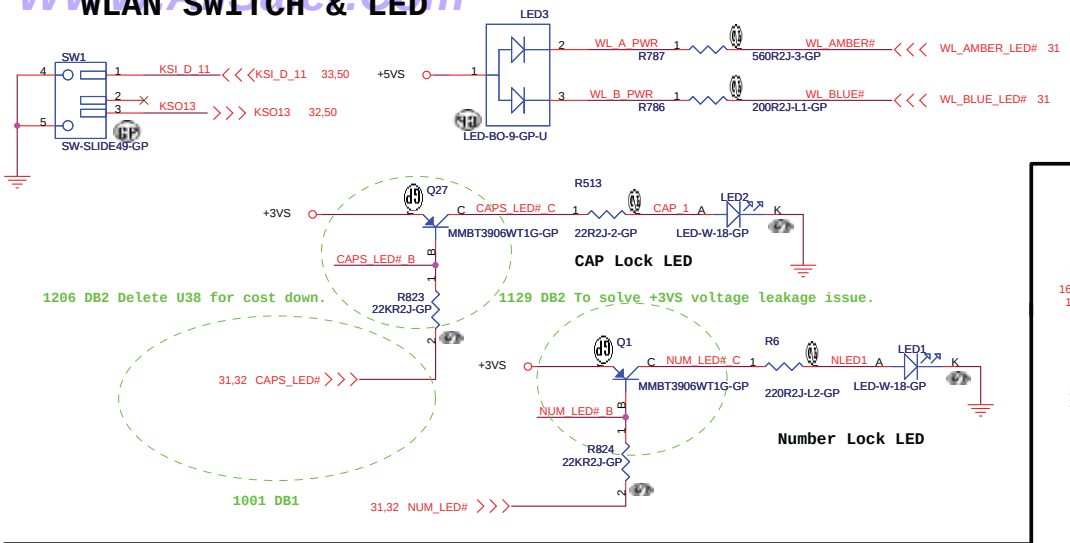
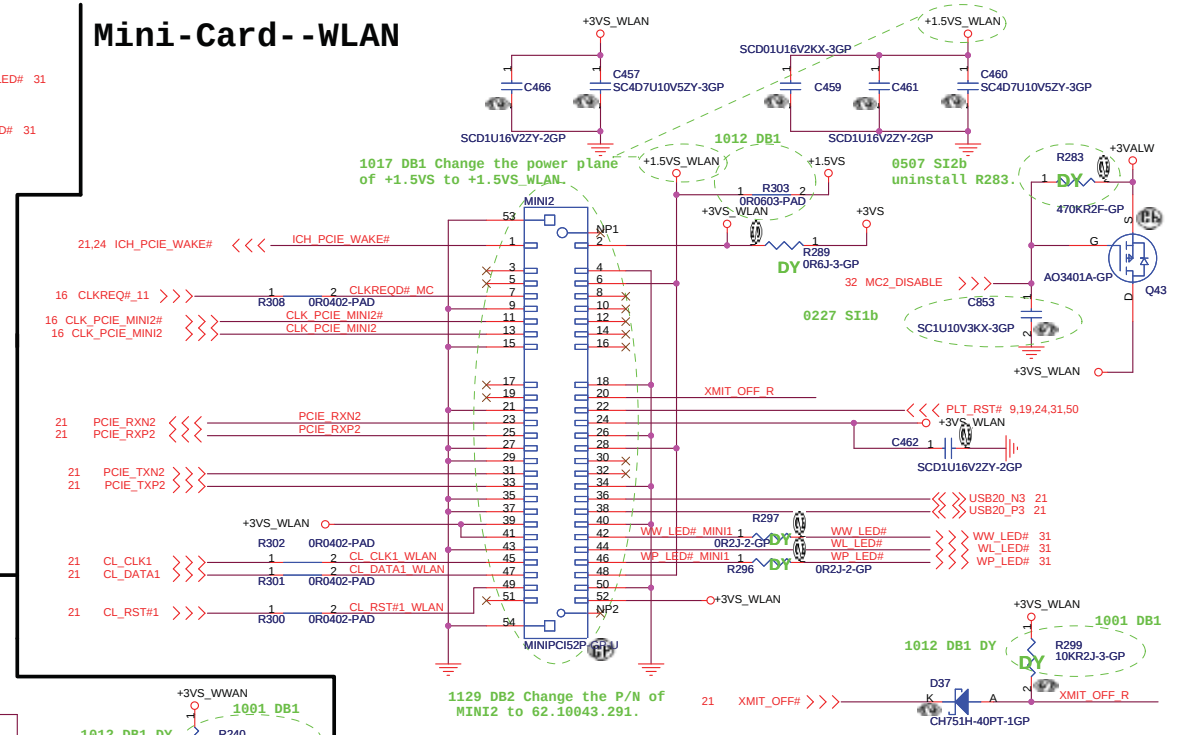
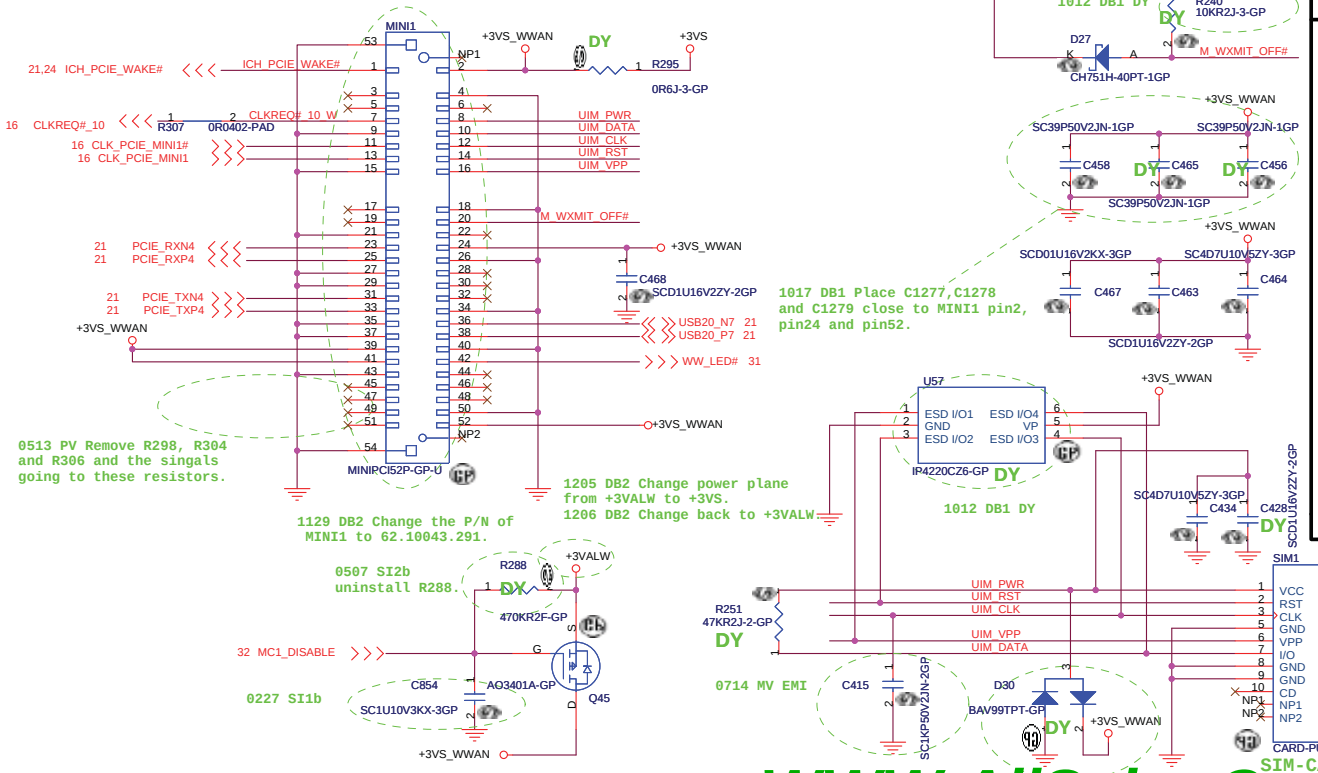
WLAN SWITCH & LED

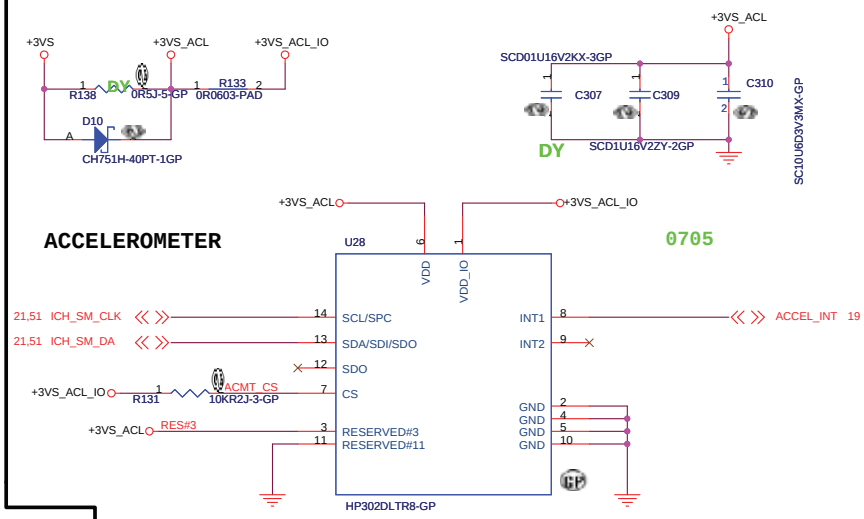


Mini-Card--WLAN



Mini-Card--WWAN





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini-Card/Accelerometer

Size: Custom | Document Number: NORN 2.0 | Rev: -1

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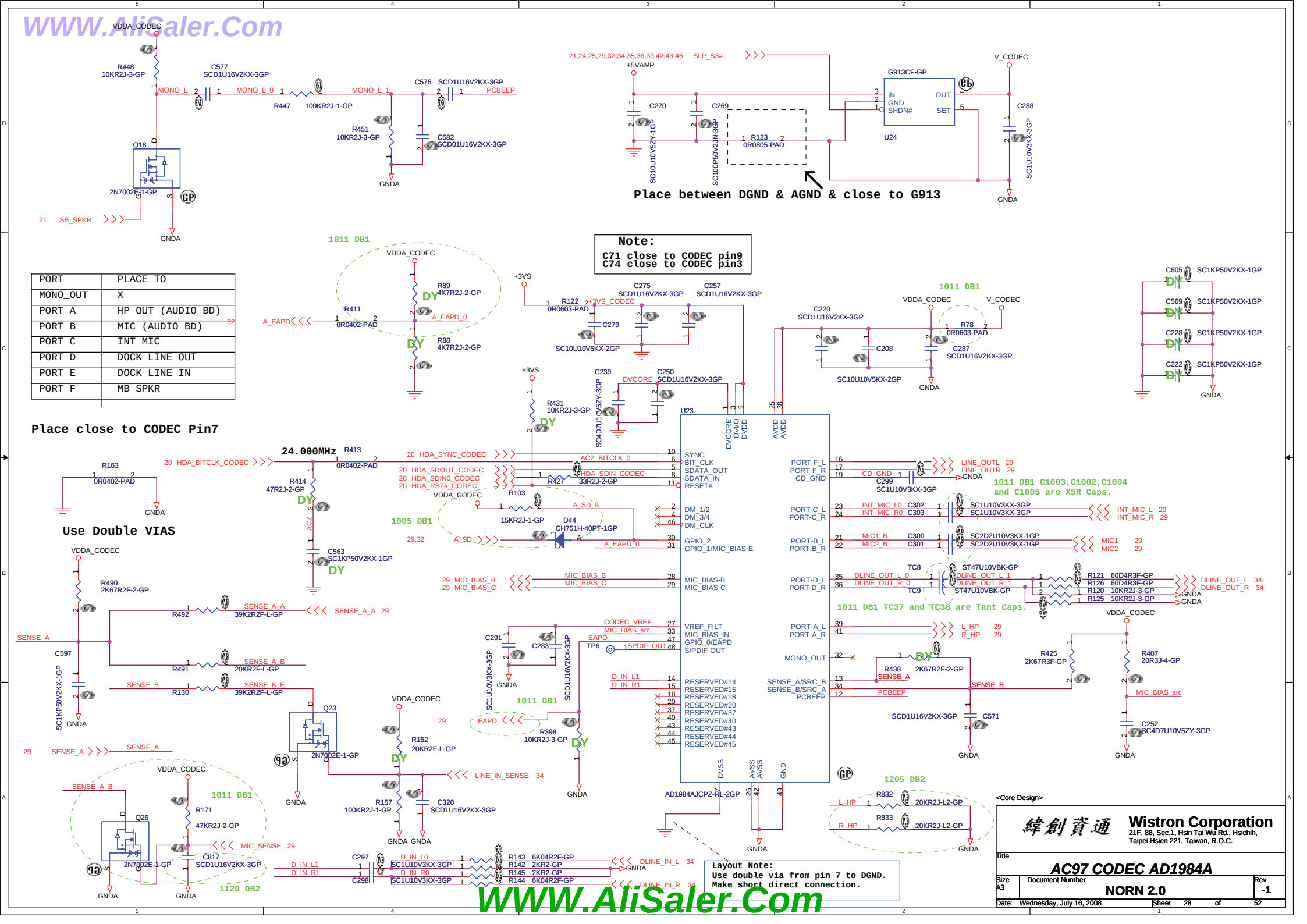
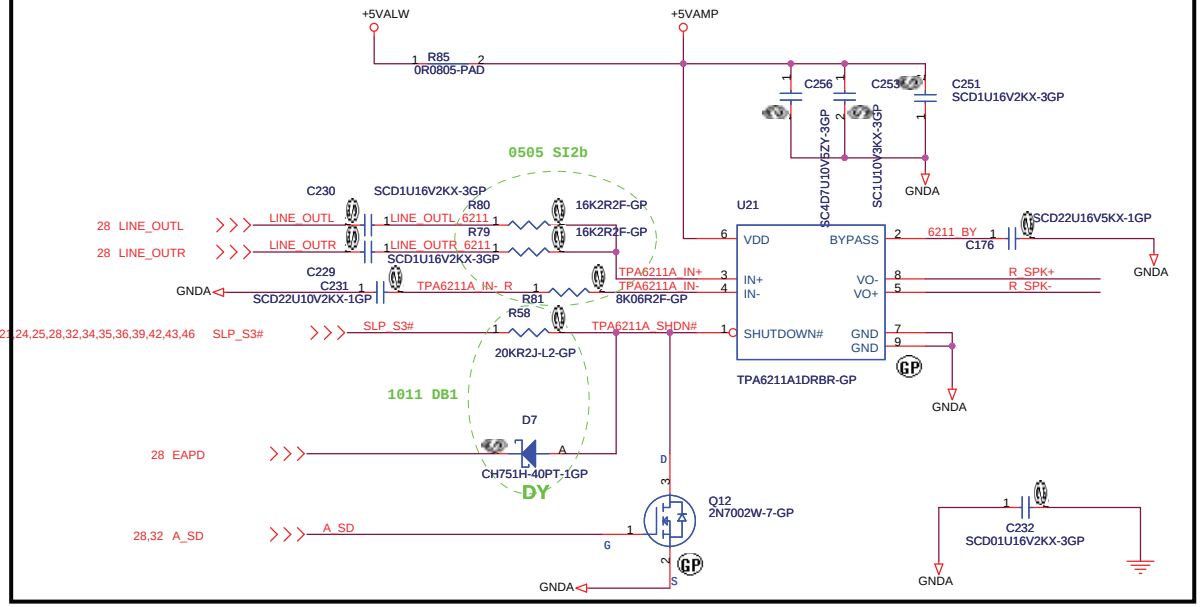
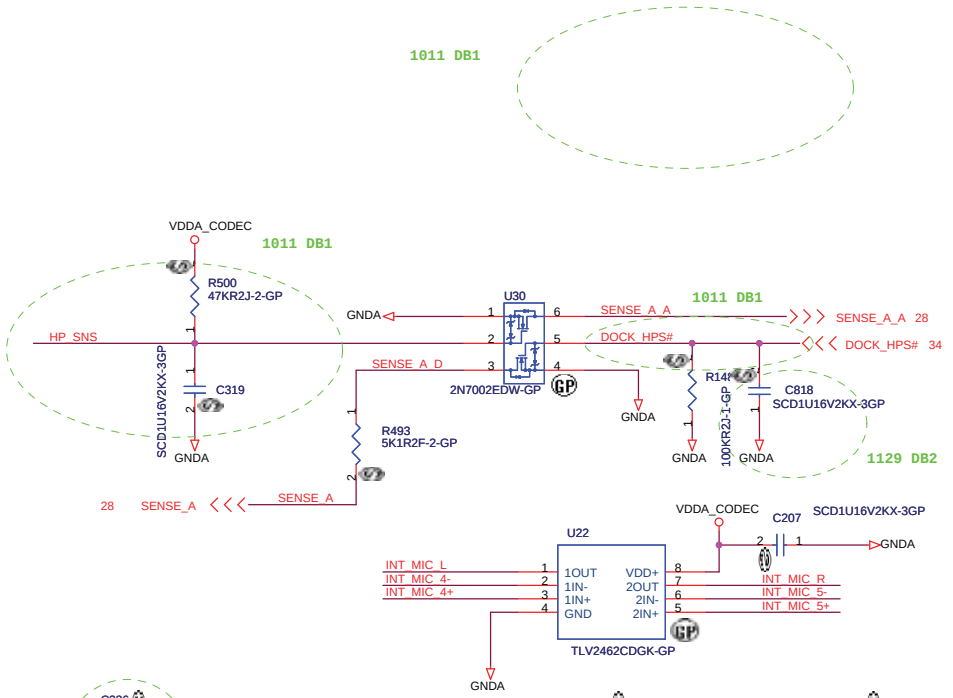
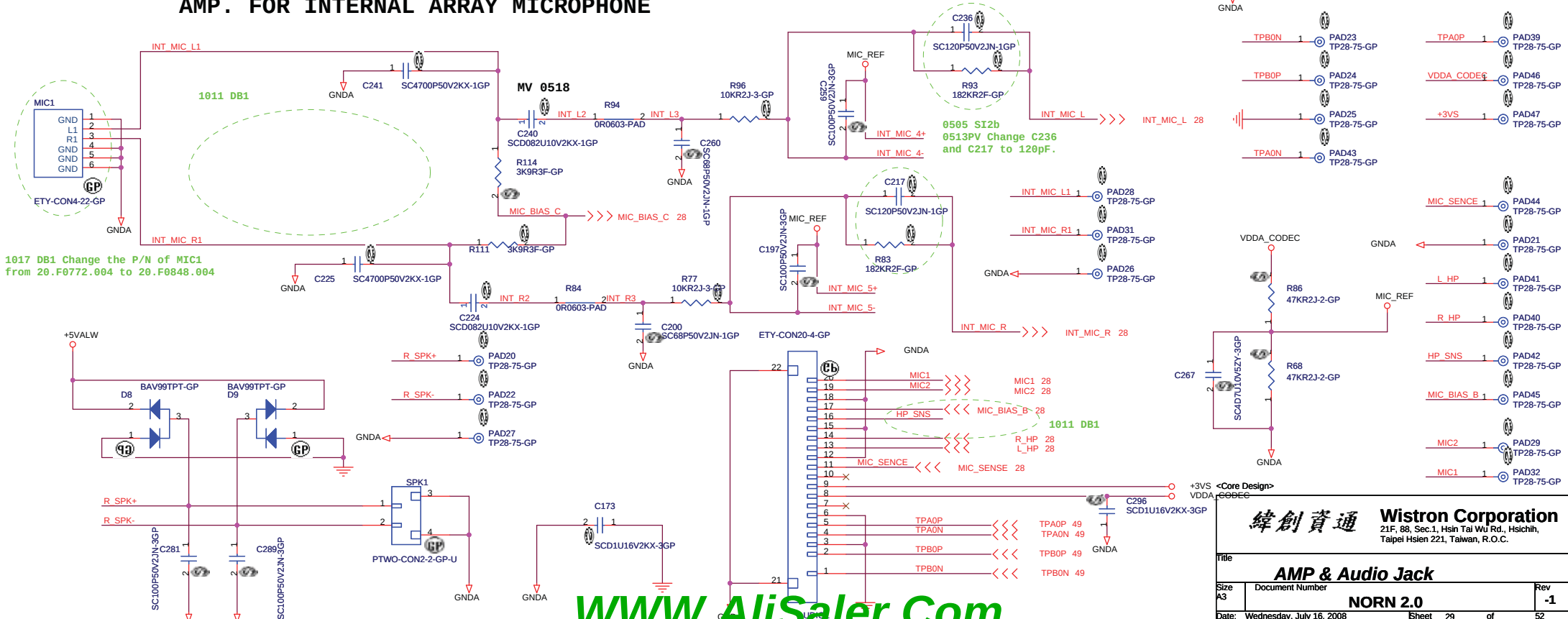


AMP. FOR INTERNAL SPEAKER





AMP. FOR INTERNAL ARRAY MICROPHONE



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AMP & Audio Jack**

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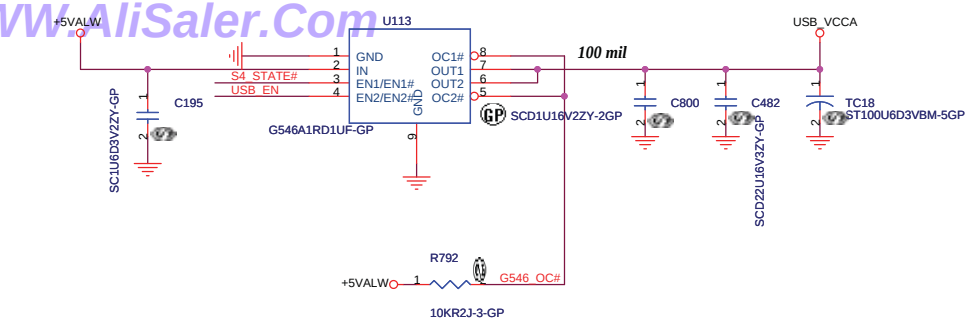

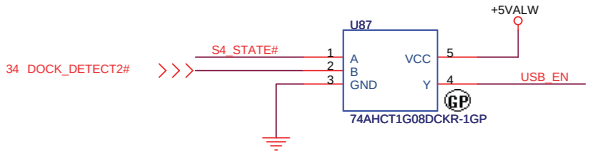

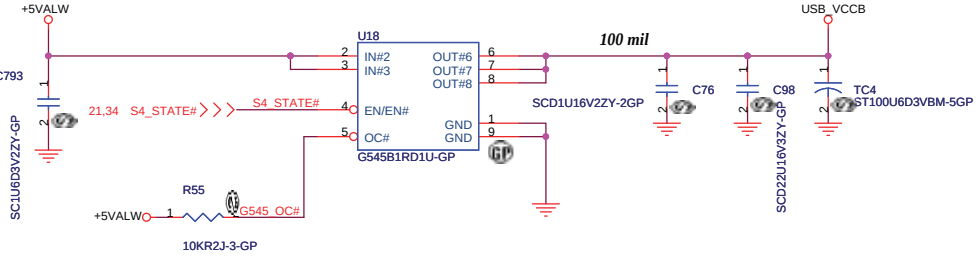

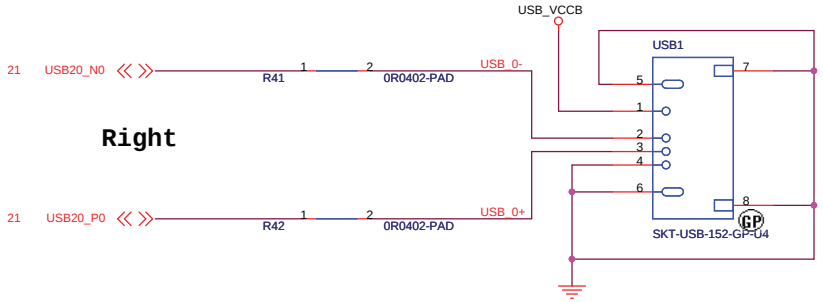

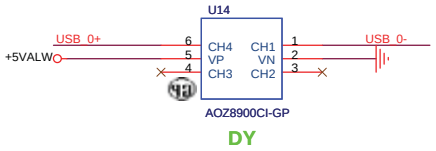

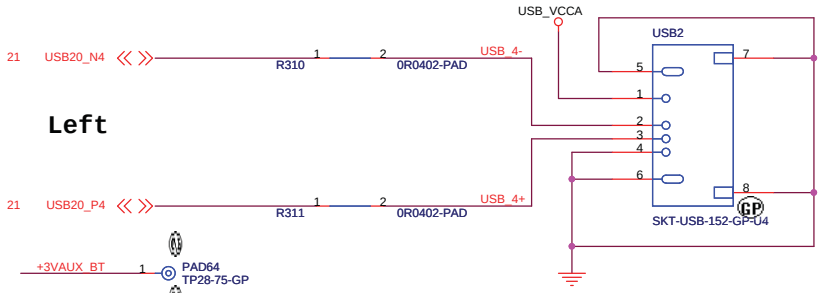

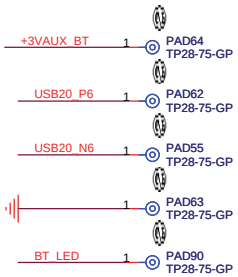

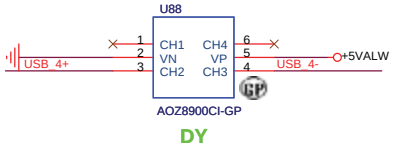

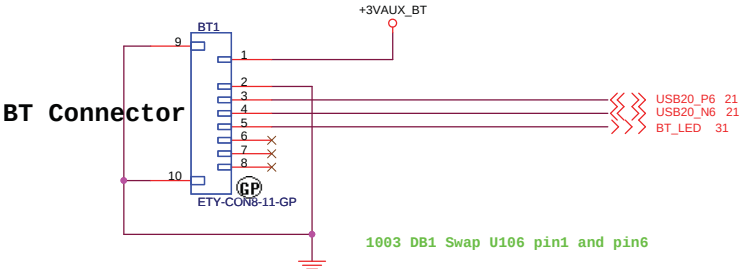

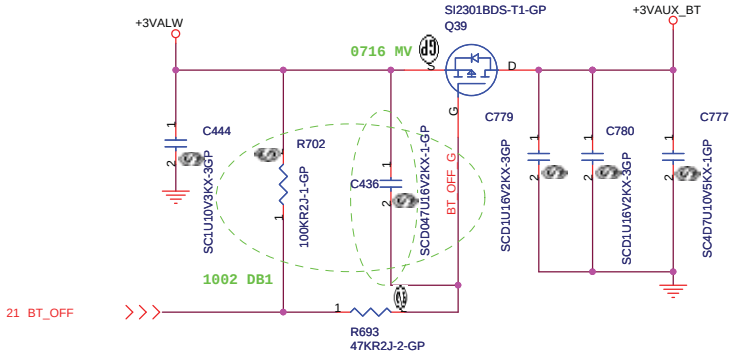

<Core Design>

緯創資通 Wistron Corporation
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Title: USB&1394 & BT Connector

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32Mb x 1

0120 SI1 Change R249 from 56R to 15R.

0120 SI1 Remove R250, R248, R273 and R274.

0128 SI1 Change R266 and R267 from 15Rto 47R.

62.10089.001 is SPI Socket part number

32M SPI
> 72.25325.A01 MX25L3205DM2I-12G, by MXIC
32M SPI
> 72.26321.A01 IC FEROM AT26DF321-SU, by Atmel

Debug port

1001 DB1

0128 SI1

1. Keep traces of SPI as short as possible and keep trace spacing close to 7mils to any other signal (basically follow specs).

2. AMT designs need 2x2MB SPI parts in addition to connecting to a debug connector. Keep stuffing options from 2nd SPI part to debug connector very close to 2nd part so stub effect can be eliminated during testing as needed.

TPM 1.2

0522 PV Change C412 from 22pF to 18pF and C420 from 18pF to 15pF.

Mini-PCIE Card LED control circuit

<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TPM/BIOS/24 DEBUG PORT		
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1001 DB1

0128 SI1 Remove RN52, RN53 and RN55.

1019 DB1Add a 0805 resistor in series with +3VL to U48.
Change +3VL power plane to +3VL_KBC.

0227 SI1b Change R630 and R618 to 1K ohm.

1206 DB2

0513 PV
0520 PV Install D63.

1011 DB1

0120 SI1 Not install R707.
0314 SI2 Not install R669.

1019 DB1 Change power rail to +3VL_KBC.

1129 DB2

0120 SI1

1001 DB1

0417 SI2b Swap THP and TP port of U58.

0124 SI1

0120 SI1 Remove D32.

1129 DB2

0709 MV Change R605 from 10K to 2.2K.

0522 PV Change C440 from 27pF to 18pF.

1016 DB1

Num _LED change to Cap Bottom

U58

KBC1091-NU-GP-U1

Keyboard/Mouse Interface

General Purpose I/O Interface

LPC Bus

Layout Note:
Place D51, D49, D50,
D55, D57 and D58 close to U58.

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_SMSC 1091

Size: Custom | Document Number: NORN 2.0 | Rev: -1

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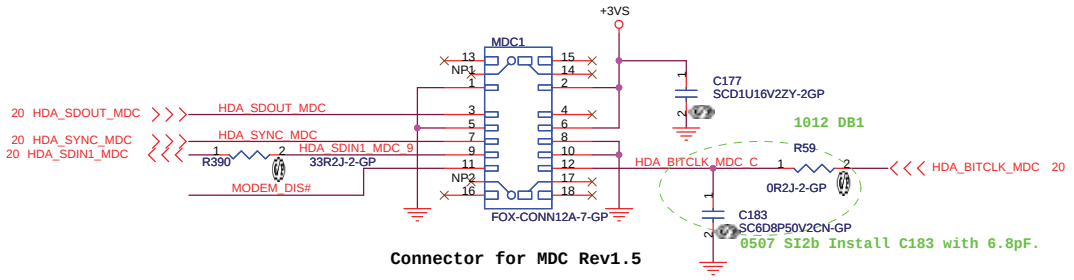
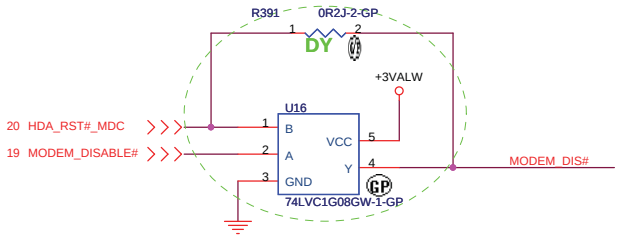
MDC 1.5 Conn.

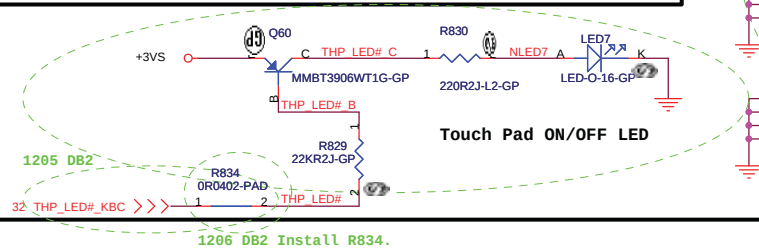


Connector for MDC Rev1.5

1129 DB2



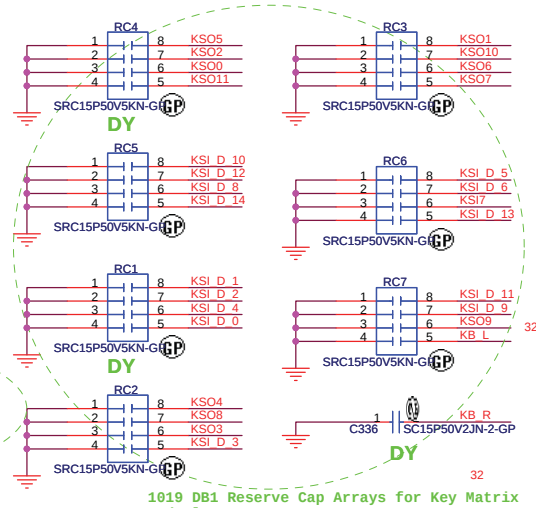
1203 DB2 Add Touch Pad ON/OFF LED circuit.



Touch Pad ON/OFF LED

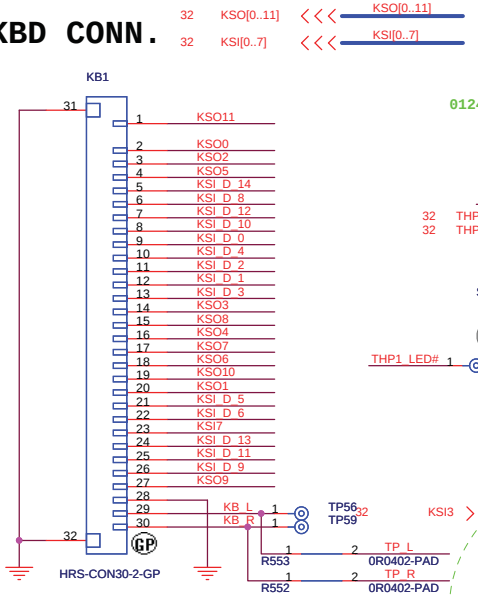
1205 DB2

1206 DB2 Install R834.



1019 DB1 Reserve Cap Arrays for Key Matrix and place near to KB1.

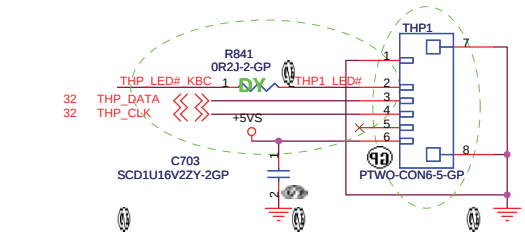
INT_KBD CONN.

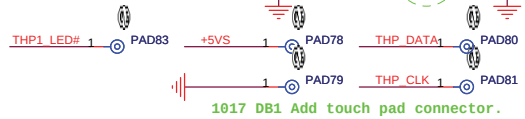


Touch_Pad CONN.

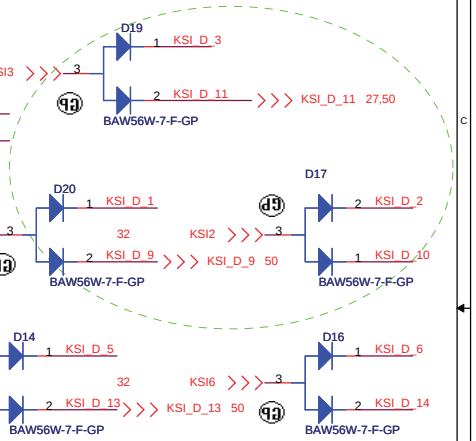
1203 DB2 Change THP1 from 8pin to 6pin.
0227 SI1b Reverse the pin define of THP1.

0124 SI1

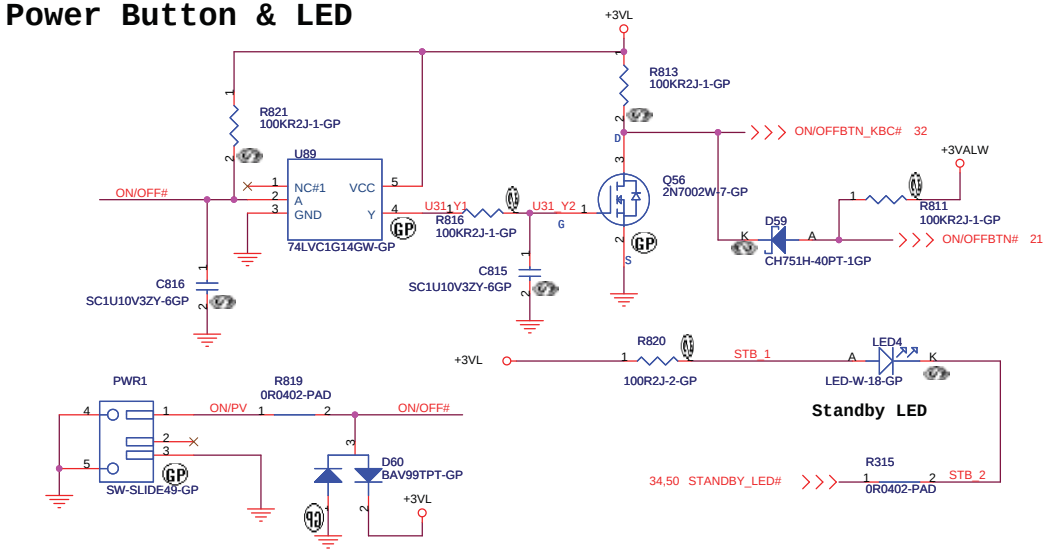




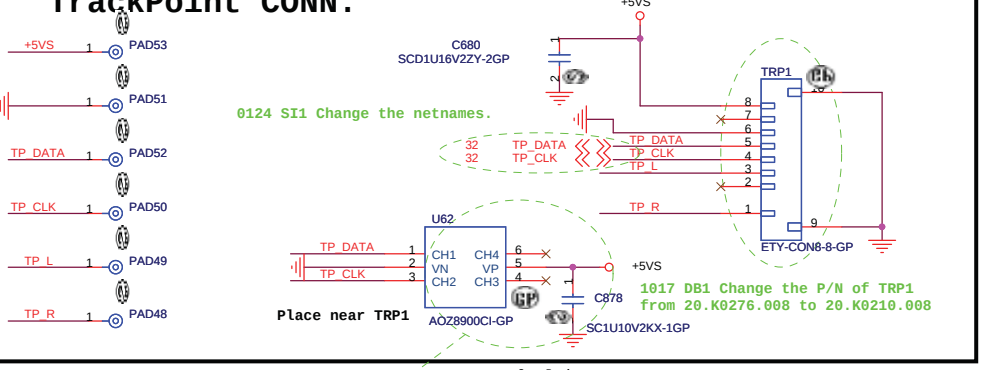
1017 DB1 Add touch pad connector.



Power Button & LED

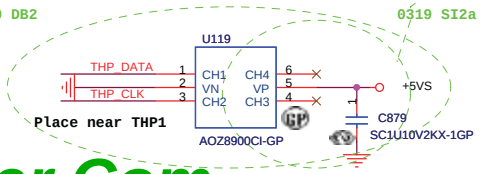


TrackPoint CONN.



1130 DB2

0319 SI2a



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC/KBD/ON OFF/T.P.

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current rating 6A

L11 BLM21PG220SN1DGP
VIN — DOCKVIN
C503 SC1KP50V2KX-1GP
C504 SC1KP50V2KX-1GP

1002 DB1
C37 DY SC1KP50V2KX-1GP
C38 DY SC1KP50V2KX-1GP
GNDA

1001 DB1 Add RC for EMI resuest.

28 DLINE_OUT_R — DLINE_OUT_R — R39 0R3-0-U-GP — DLINE_OUT_R_D
28 DLINE_OUT_L — DLINE_OUT_L — R38 0R3-0-U-GP — DLINE_OUT_L_D
28 DLINE_IN_R — DLINE_IN_R — R37 0R3-0-U-GP — DLINE_IN_R_D
28 DLINE_IN_L — DLINE_IN_L — R36 0R3-0-U-GP — DLINE_IN_L_D

C43 DY SC5P50V2CN-2GP
C42 DY SC5P50V2CN-2GP
C41 DY SC5P50V2CN-2GP
C40 DY SC5P50V2CN-2GP
GNDA

MAX4596

IN	NO TO COM COM TO NO
L	OFF
H	ON

CLOSE DOCKING CONN.

+5VS
R34 10KR2J-3-GP

U8 MAX4596DCKR-GP
30 DOCK_DETECT2# — DOCK_DETECT2# — 9 RED — L_RED 17
U9 MAX4596DCKR-GP
9 GREEN — L_GREEN 17
U7 MAX4596DCKR-GP
9 BLUE — L_BLUE 17

DOCK1
DOCKVIN — DOCKVIN
DOCK_DETECT2#
GNDA
DLINE_OUT_R_D
DLINE_OUT_L_D
DLINE_IN_R_D
DLINE_IN_L_D
28 LINE_IN_SENSE — LINE_IN_SENSE
29 DOCK_HPS# — DOCK_HPS#
LIMIT_SIGNAL — LIMIT_SIGNAL

0513 PV Change the power source of +3VM_LAN_LED to +3VM_LAN.
+3VM_LAN

26 MDO3- / 26 MDO3+ — MDO3- / MDO3+
26 MDO1- / 26 MDO1+ — MDO1- / MDO1+
26 MDO2- / 26 MDO2+ — MDO2- / MDO2+
26 MDO0+ / 26 MDO0- — MDO0+ / MDO0-

1015 DB1 Remove TV-OUT connection.

17 D_VSYNC / 17 D_HSYNC
GREEN_C
RED_C
BLUE_C
B+
C508 SC1KP50V2KX-1GP

USB20_N11 — USB20_N11 21
USB20_P11 — USB20_P11 21
USB20_N9 — USB20_N9 21
USB20_P9 — USB20_P9 21
STANDBY_LED# — STANDBY_LED# 33,50
SLP_S3# — SLP_S3# 21,24,25,28,29,32,35,36,39,42,43,46
LED_ACT_LAN#_DOCK
LED_LINK_LAN#_DOCK
D_DDCDATA — D_DDCDATA 17
D_DDCCLK — D_DDCCLK 17
S4_STATE# — S4_STATE# 21,30
DOCK_DETECT1#
R7 0R0402-PAD

JAE-CONN100-1-GP-U4

DK(ODD)
DK(HUB)

DOCK CONN. 100 PIN

Power Pins
2 sets
Set 1 = 18.5V @ 4A per contact
Set 2 = VBATR @ 3A per contact

0514 PV Change R344, R345 and R346 from 0 ohm to 22 ohm@100MHz beads.

GREEN — R346 BLM18BB220SN-GP — GREEN_C
RED — R345 BLM18BB220SN-GP — RED_C
BLUE — R344 BLM18BB220SN-GP — BLUE_C
C507 DY SC5P50V2CN-2GP
C505 DY SC5P50V2CN-2GP
C506 DY SC5P50V2CN-2GP

U4 AOZ8900CI-GP
USB20_N9 — CH1 CH4 — USB20_N11
USB20_P9 — VN VP — USB20_P11
CH2 CH3 — +5VALW
DY

1018 DB1

+5VS
R40 10KR2J-3-GP
U12 2N7002EDW-GP
DOCK_DETECT2#
21,26 PREP# — PREP#
PREP#_DOCK

+3VM_LAN
R21 10KR2J-3-GP
LAN_LINK_EN
U3 2N7002EDW-GP
25,26 LED_ACT_LAN# — LED_ACT_LAN#_DOCK
LED_LINK_LAN#_DOCK — LED_LINK_LAN# — LED_LINK_LAN# 25,26,32

0227 SI1b Swap the connections of U3-1 and U3-6

<Core Design>

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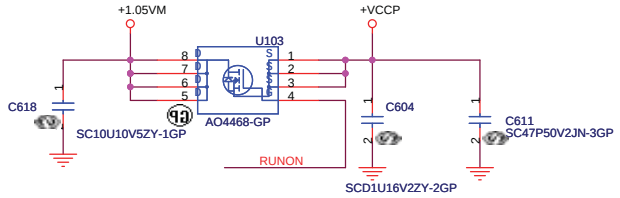
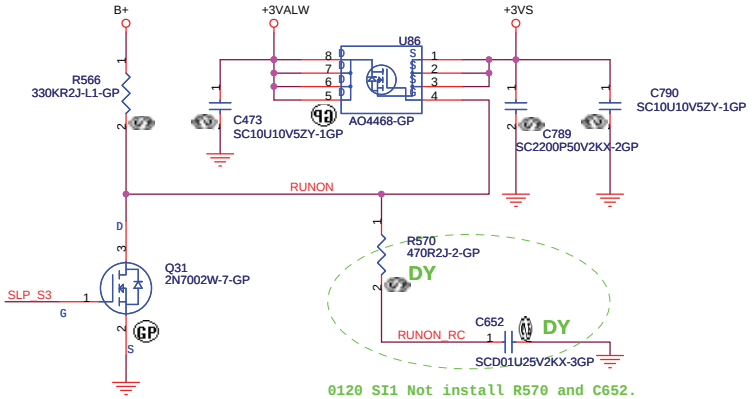
Title: Docking CONN
Size: A3
Document Number: NORN 2.0
Rev: -1
Date: Wednesday, July 16, 2008
Sheet 34 of 52

+1.05VM to +VCCP Transfer



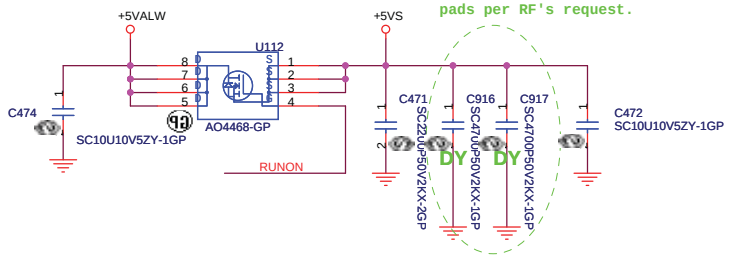
+3VALW to +3VS Transfer



0120 SI1 Not install R570 and C652.

+5VALW to +5VS Transfer

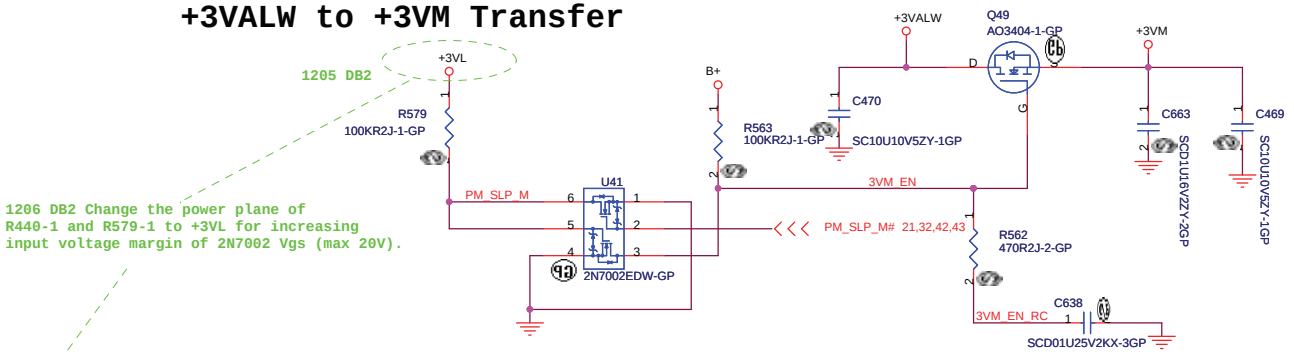
0421 SI2b Reserve two cap pads per RF's request.



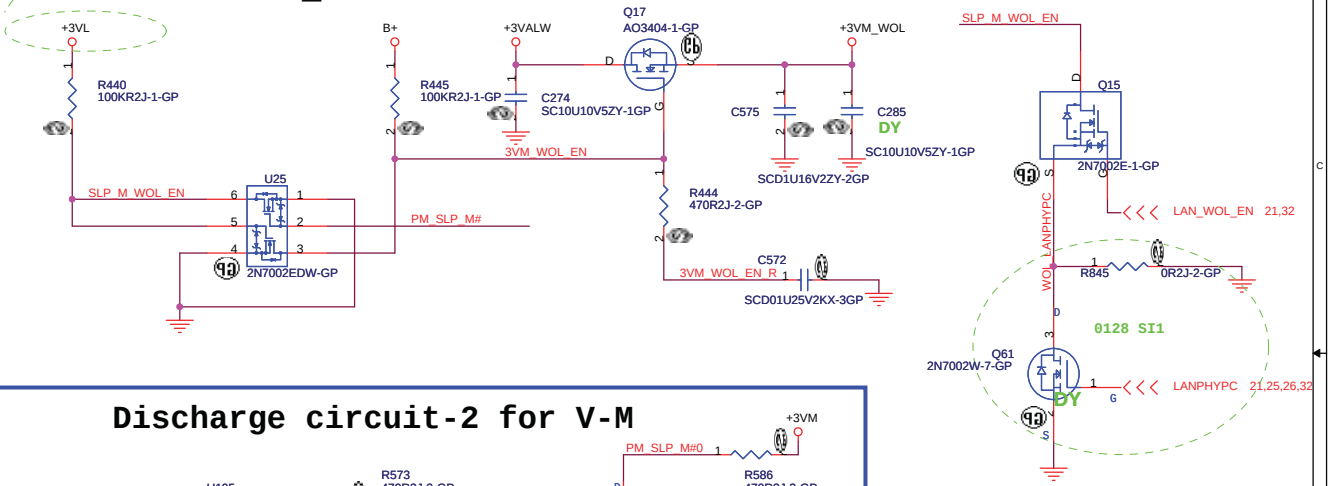
+3VALW to +3VM Transfer

1205 DB2

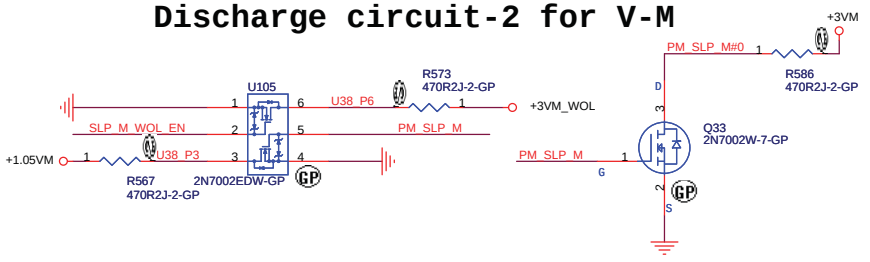
1206 DB2 Change the power plane of R440-1 and R579-1 to +3VL for increasing input voltage margin of 2N7002 Vgs (max 20V).



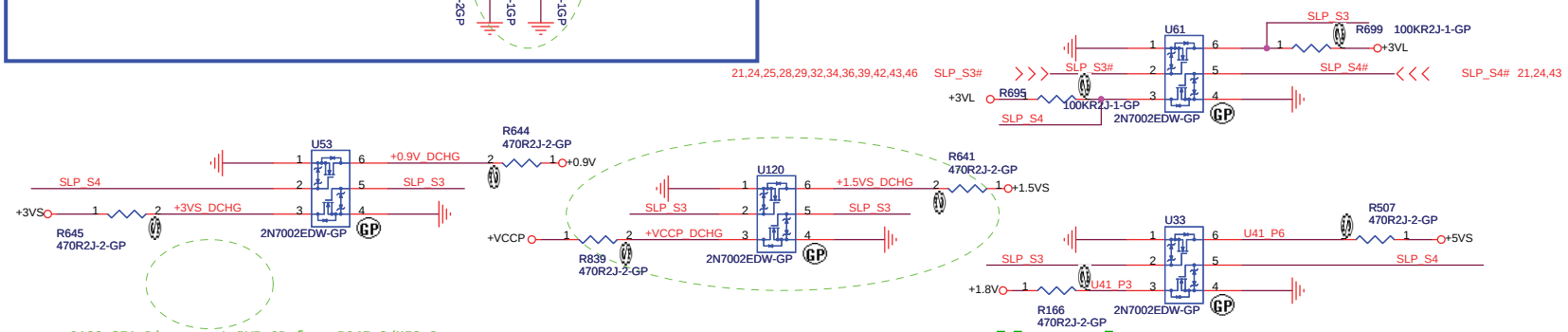
+3VALW to +3VM_WOL



Discharge circuit-2 for V-M



Discharge circuit-1



0120 SI1 Disconnect PWR_GD from R645-2/U53-3.

<Core Design>

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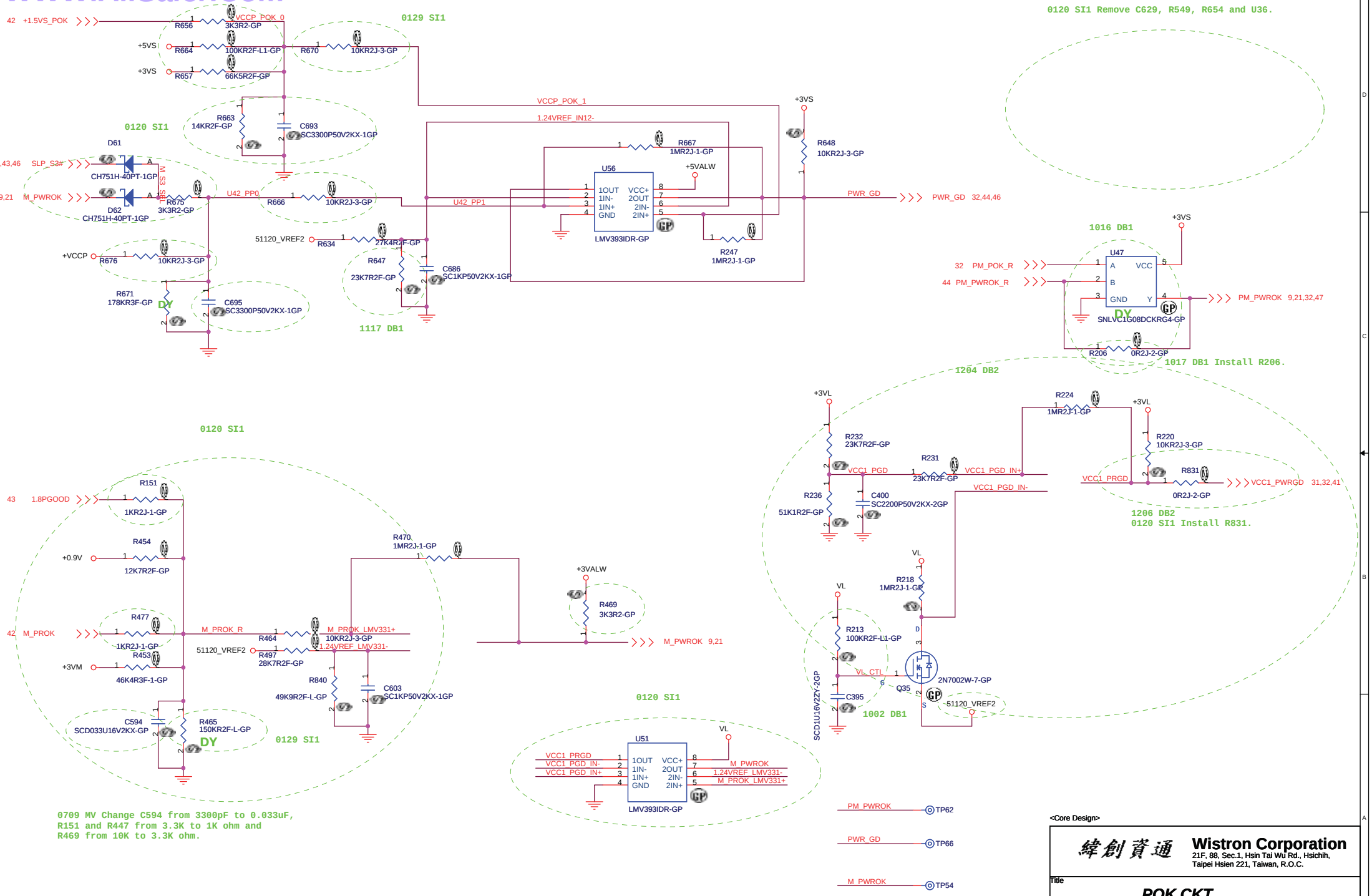
Title: DC/DC Circuit

Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 35 of 52



<Core Design>

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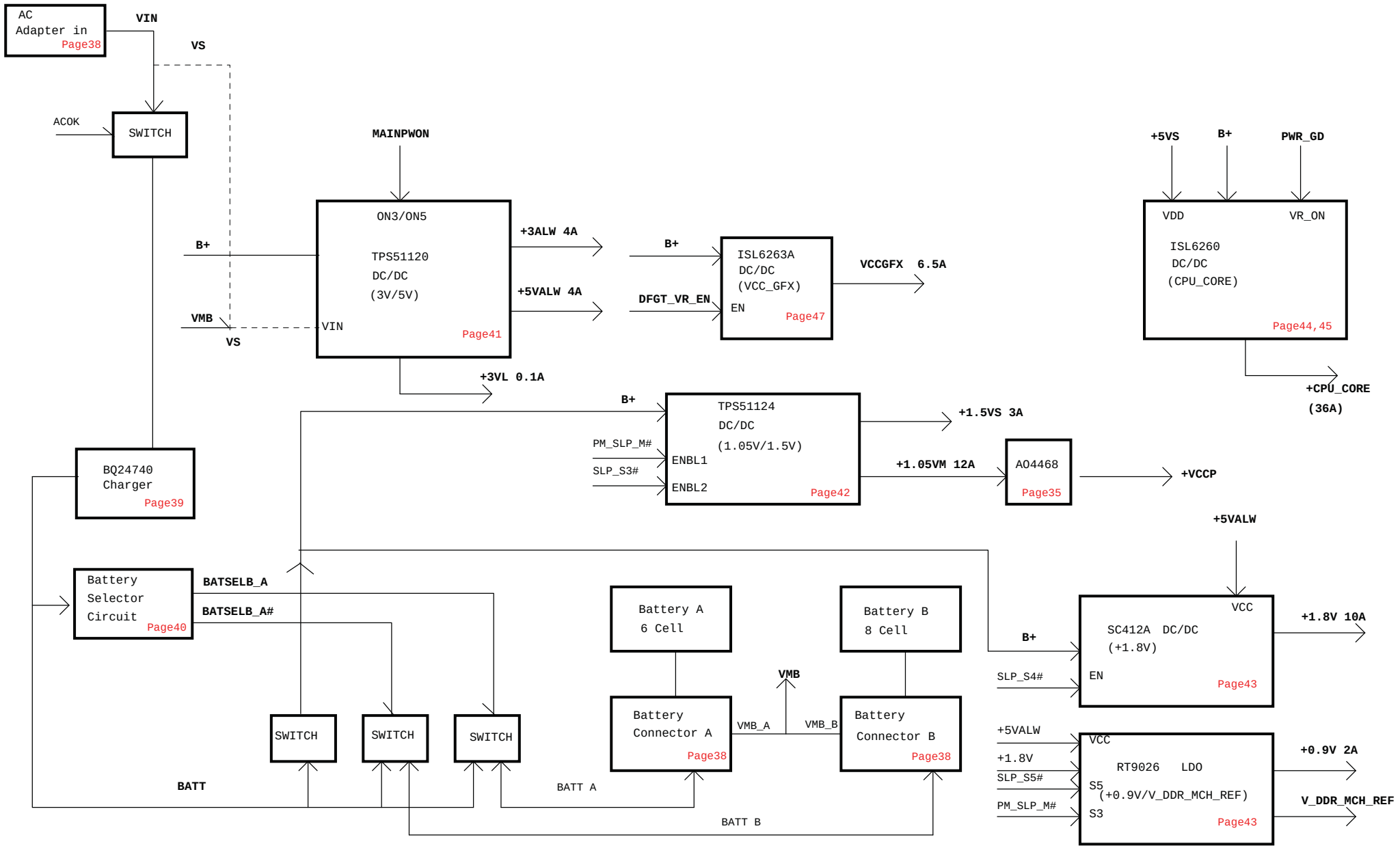
Taipei Hsien 221, Taiwan, R.O.C.

Title: POK CKT

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 36 of 52



<Core Design>

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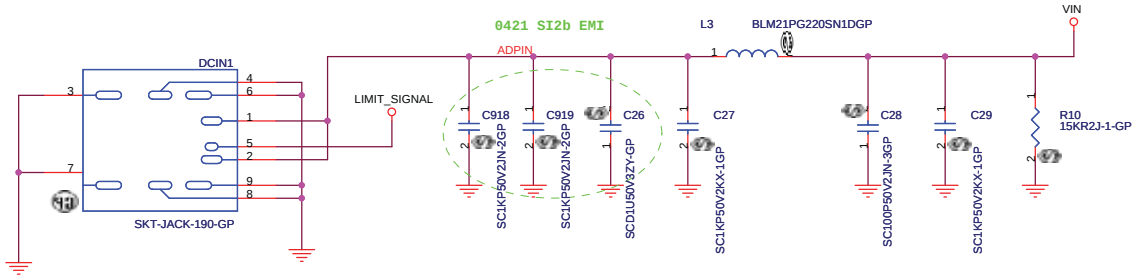
Title: Power Block Diagram

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 37 of 52

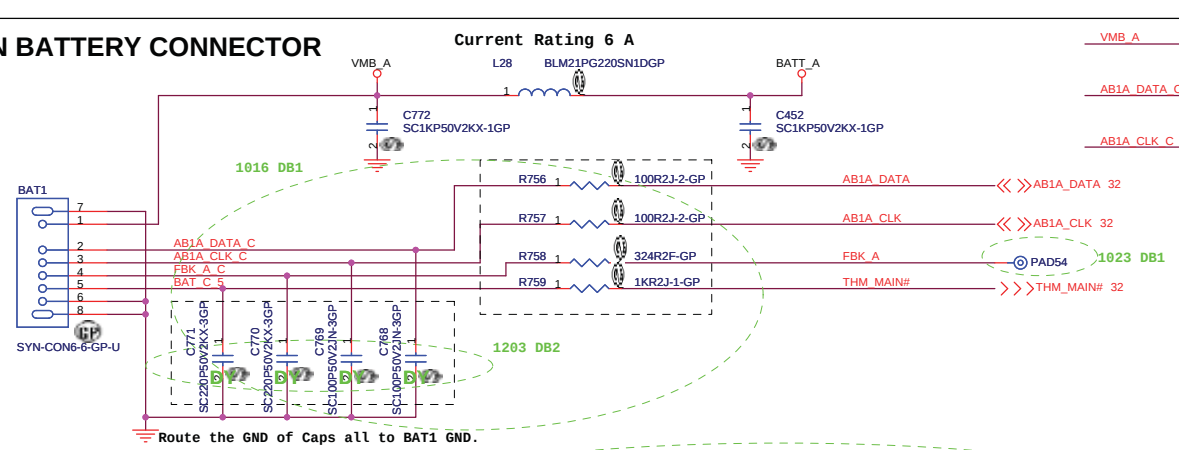
Adaptor in to generate DCBATOUT

Current Rating 6 A



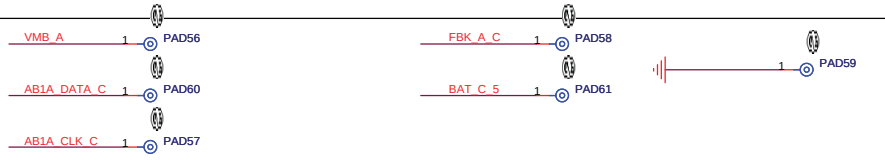
MAIN BATTERY CONNECTOR

Current Rating 6 A

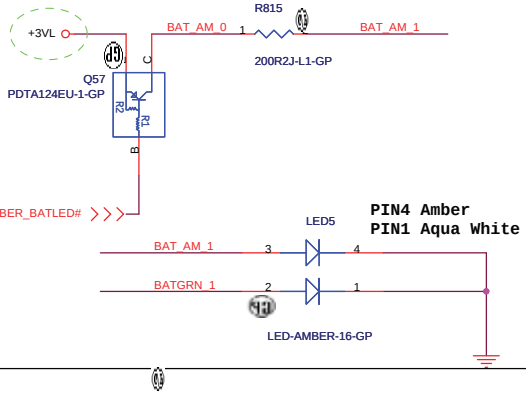


Layout Note:
Place R677, R678, R423, R818,
C618, C617, C613 and C609 close to BAT1.

1008 DB1 Remove D74 and
move D68, D73 and D75 to Page32.



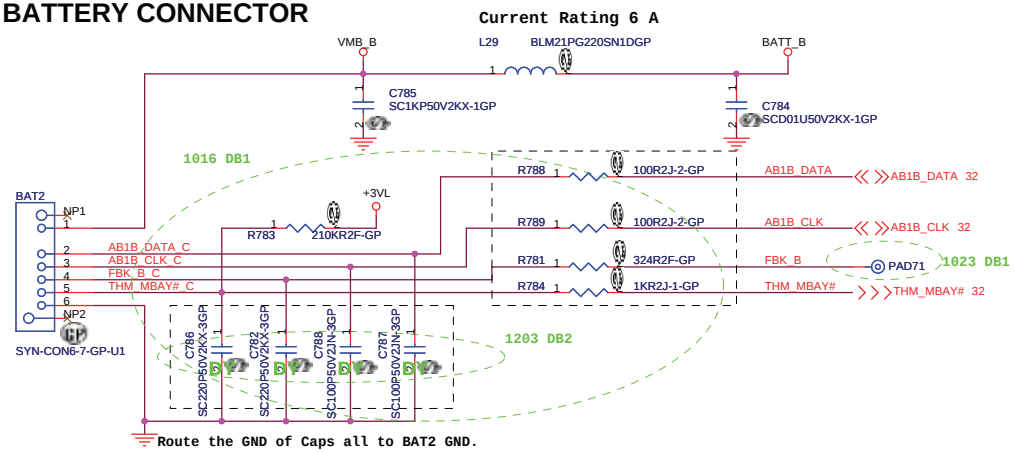
1017 DB1 Change +3VALW to +3VL.



PIN4 Amber
PIN1 Aqua White

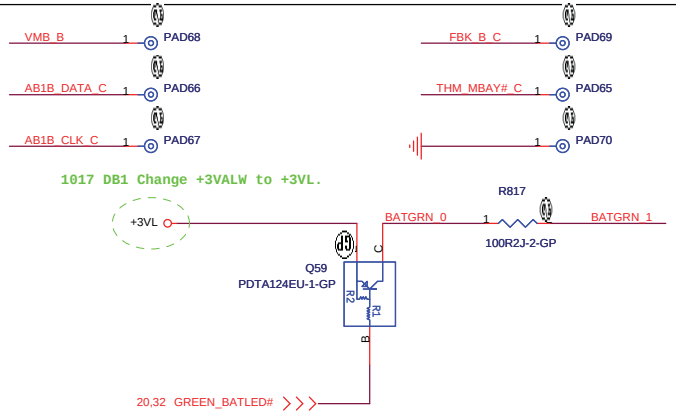
BAY BATTERY CONNECTOR

Current Rating 6 A



Layout Note:
Place R704, R705, R709, R707,
C639, C640, C635 and C636 close to BAT2.

1008 DB1 Remove D77 and
move D76, D78 and D79 to Page32.



1017 DB1 Change +3VALW to +3VL.

<Core Design>

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Title: DC & BATTERT CONN.

Size	Document Number	Rev
Custom	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 38 of 52

1012 DB1 Change
C1236 voltage tolerance
from 16V to 25V.

1008 Connect DCBAT to B+

0716 MV PW team

1002 DB1 Remove R1396

1011 Correct circuits for the sense issue.

1008 Remove G109, G110.

Add close GAP reduce
Caps Effect

1002 DB1 Disconnect PQ1-5,6,7,8
from BT+ and connect to BTT_1.

1002 DB1 Connect ACP_L to 24740_SRN
and ACN_L to 24740_SRP.

0515 PV

0304 SI1b
Setting current limit=3.38A.
0314 SI2 Not install R847.

1001 DB1

1204 DB2

1011 DB1 Replace resistors
with closed pads.

FDS8878 SO-8
Id=9.3A, Qg=9~14nC
Rdson=14~17mohm

0313 SI1b

1011 DB1 Add one 0.1uFvCap.

0120 SI1 Change U44 and U64
from LM393 to LMV393.

0120 SI1
Change R269 from 10K to 100K_5%,
R585 from 10K to 22K_5%,
R688 from 22K to 47K_5%,
and R689 from 140K to 300K_5%.

BQ24740RHDR-GP

<Core Design>

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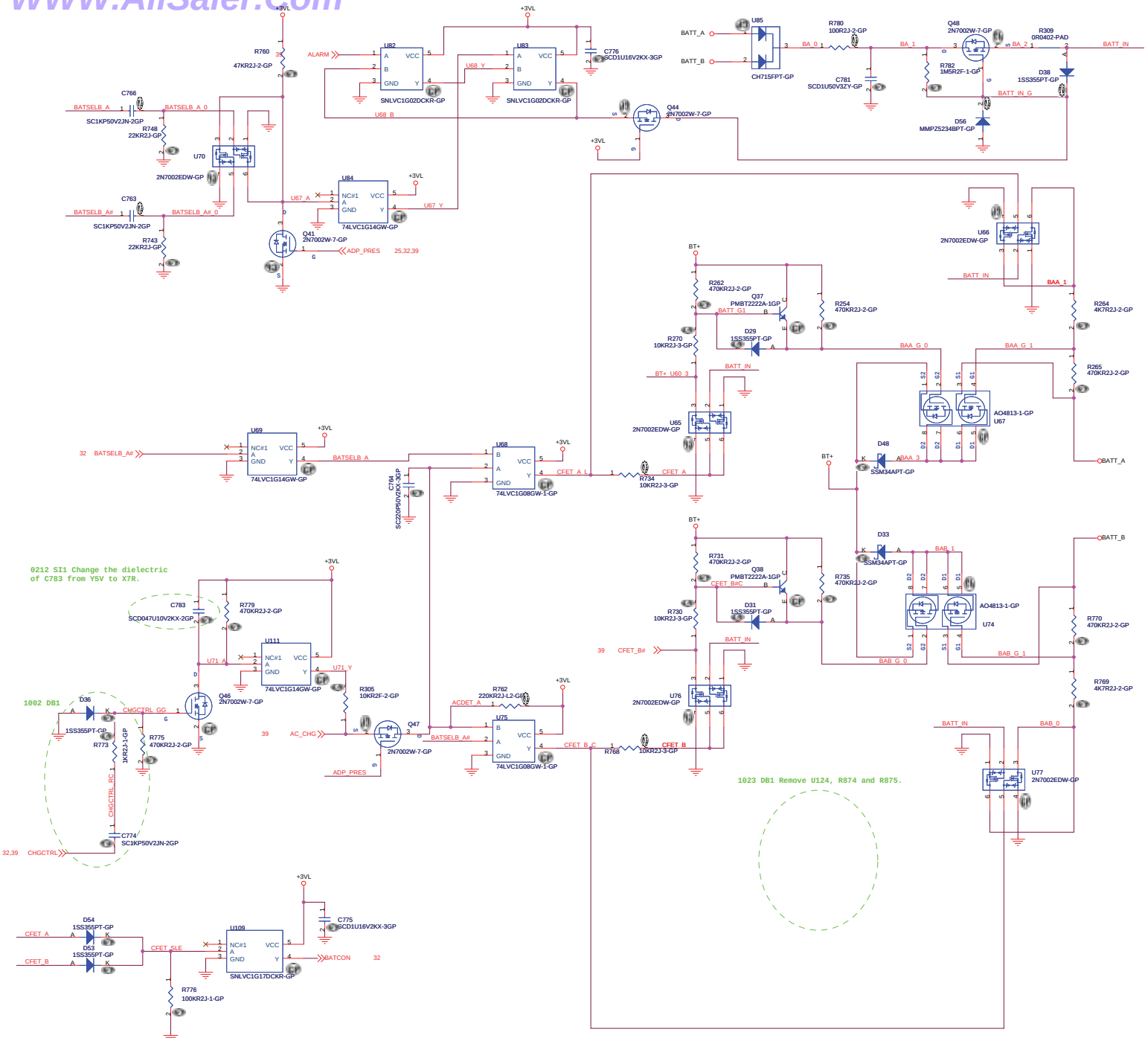
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24740

Size: C | Document Number | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 39 of 52



<Core Design>

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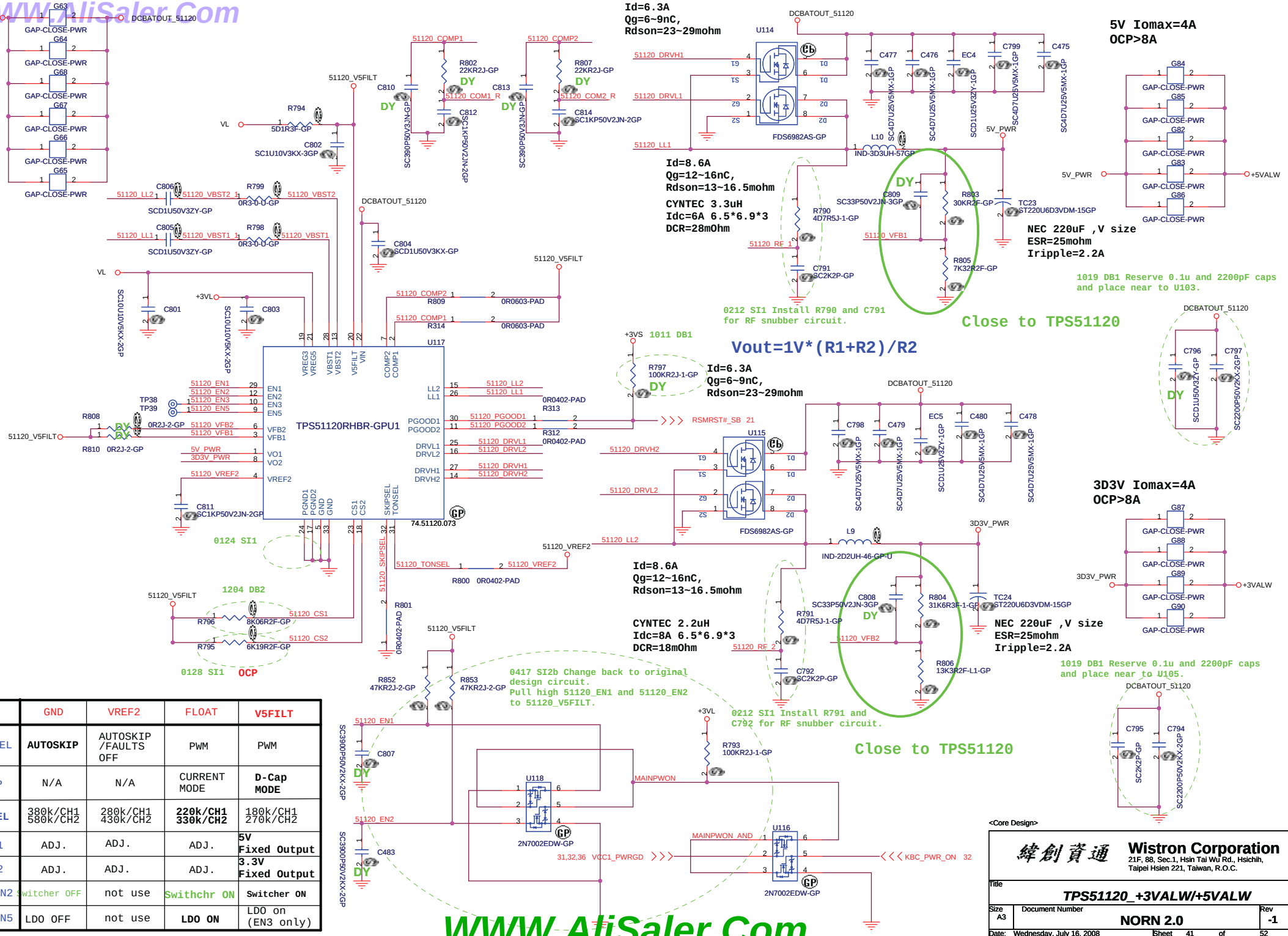
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Battery Selector

Size: A2 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 40 of 52



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	**220k/CH1 330k/CH2**	180k/CH1 270k/CH2
VFB1	ADJ.	ADJ.	ADJ.	**5V Fixed Output**
VFB2	ADJ.	ADJ.	ADJ.	**3.3V Fixed Output**
EN1, EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3, EN5	LDO OFF	not use	**LDO ON**	LDO on (EN3 only)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51120_+3VALW/+5VALW***

Size	Document Number	Rev
A3	**NORN 2.0**	**-1**

Date: Wednesday, July 16, 2008 Sheet 41 of 52

1D05V
Iomax=12A
OCP>18A

1204 DB2

1019 DB1 Reserve 0.1u and 2200pF caps and place near to U119.

1011 DB1 Add one more GAP.

84.08880.037
FDS8880, Id=10.7A
Qg=12~16nC,
Rdson=9.6~12mohm

68.1R01A.20A
CYNTEC 1uH
Idc=15A 10*11.5*4
DCR=3.5mOhm

84.08672.A37
FDS6676AS, Id=15A
Qg=15~21nC,
Rdson=5.3~7mohm

0128 SI1

1017 DB1 Reserve pads.
Place R1410 and C1284 close to U123.

Close to TPS51124

79.33719.L01
Panasonic 330uF 2V
ESR=9mohm
Iripple=3A

1129 DB2 Install C667 to filter high-frequenct noise.

Id=6.3A
Qg=6~9nC,
Rdson=23~29mohm

1019 DB1 Reserve 0.1u and 2200pF caps and place near to U101.

1D5V Iomax=3A
OCP>6A

Id=8.6A
Qg=12~16nC,
Rdson=13~16.5mohm

KEMET 220uF
ESR=35mohm
B2 size

1017 DB1 Reserve pads.
Place R1455 and C1285 close to U101.

Close to TPS51124

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.764V*(R1+R2)/R2

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

<Core Design>

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Title: TPS51124_+1.05VM / +1.5VS

Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 42 of 52

SC412A for 1D8V / RT9026_0D9V

1019 DB1 Reserve 0.1u and 2200pF caps and place near to U147.

1D8V_PWR
10A , OCP >16A

0120 SI1 Not install R246 and C714.

84.08880.037
FDS8880, Id=10.7A
Qg=12~16nC,
Rdson=9.6~12mohm

0522 PV
Change R238 to 15K ohm.

1204 DB2

1212 DB2

0128 SI1

84.08672.A37
FDS6676AS, Id=15A
Qg=15~21nC,
Rdson=5.3~7mohm

0212 SI1 Install R581 and C659 for RF snubber circuit.

68.1R01A.20B
CYNTEC 1uH
Idc=11A 6.5*6.9*3
DCR=10mOhm

77.C3371.051
NEC 330uF 2.5V
ESR=9mOhm
Iripple=3.725A

Close to SC412A

0D9V
Iomax=2A

<Core Design>

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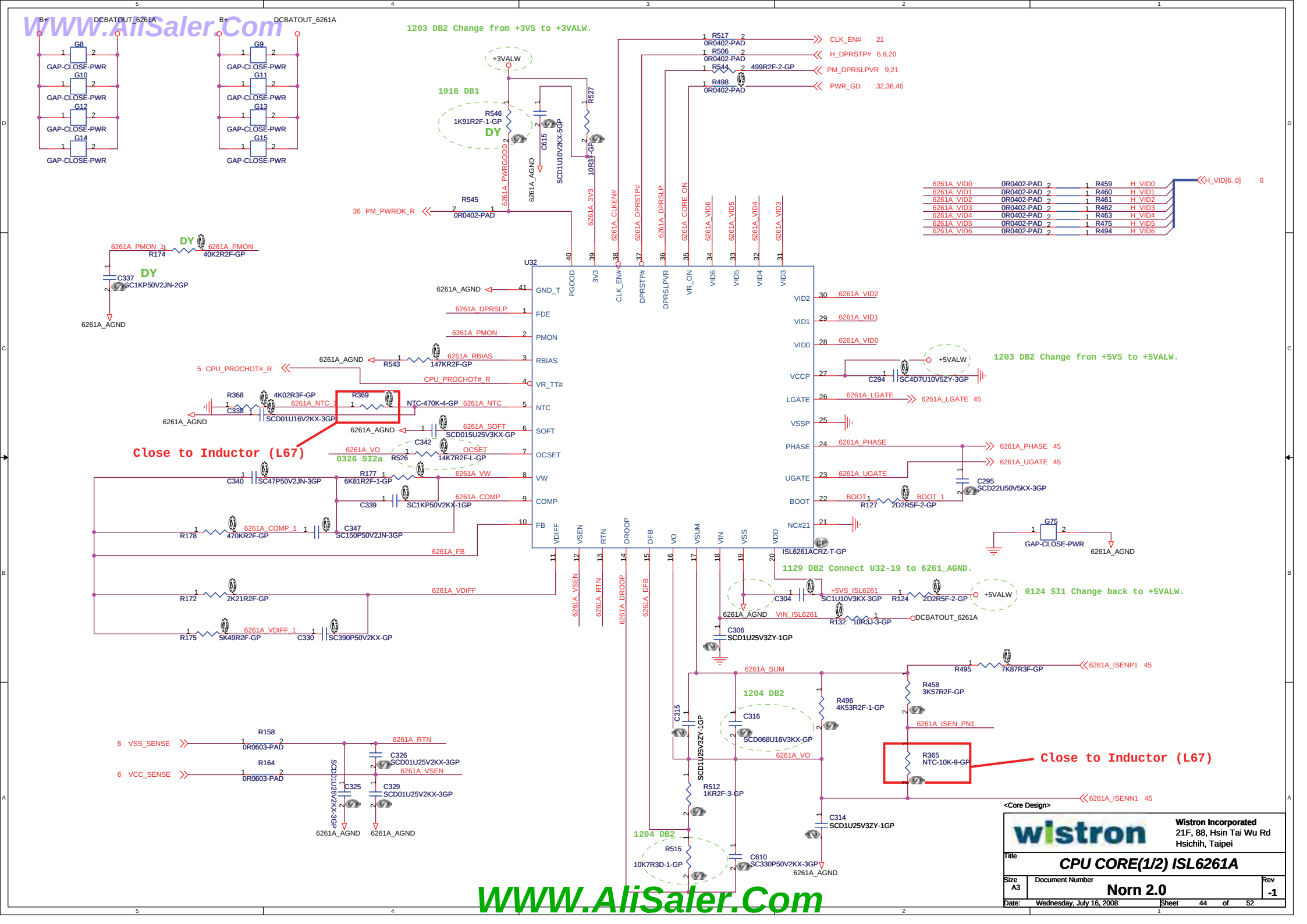
Title: SC 412A 1D8V/0.9VP RT9026

Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 43 of 52



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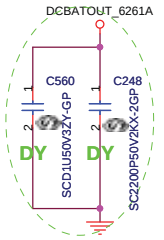
Hsichih, Taipei

Title: CPU CORE(1/2) ISL6261A

Size: A3 | Document Number: Norn 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 44 of 52

1019 DB1 Reserve 0.1u and 2200pF caps
and place near to U152.



When test without cpu,
R581 & R582 change to 0 ohms

<Core Design>

wistron

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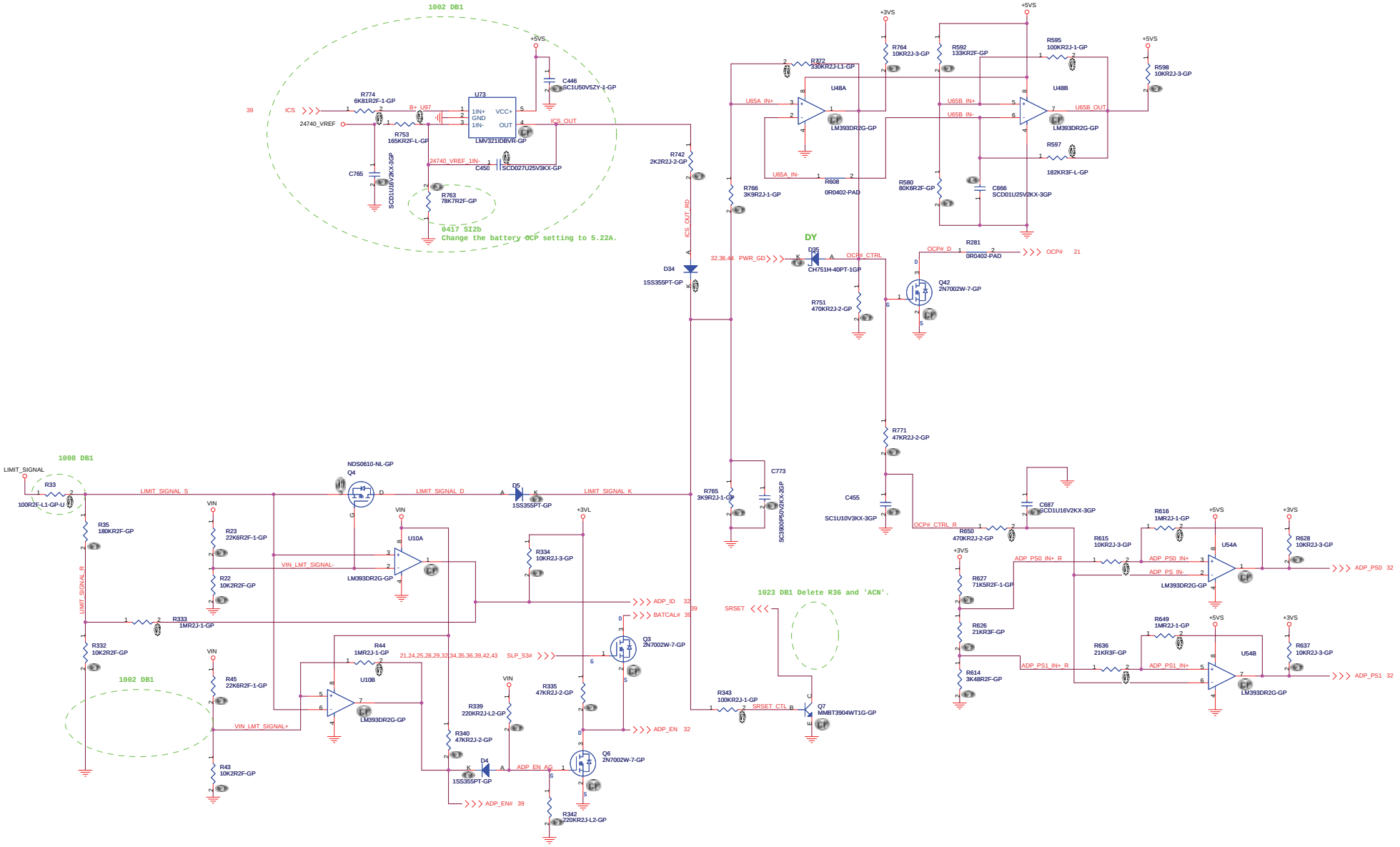
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU CORE(2/2) ISL6261A

Size: A3 | Document Number: Norn 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 45 of 52



<Core Design>

Wistron Corporation
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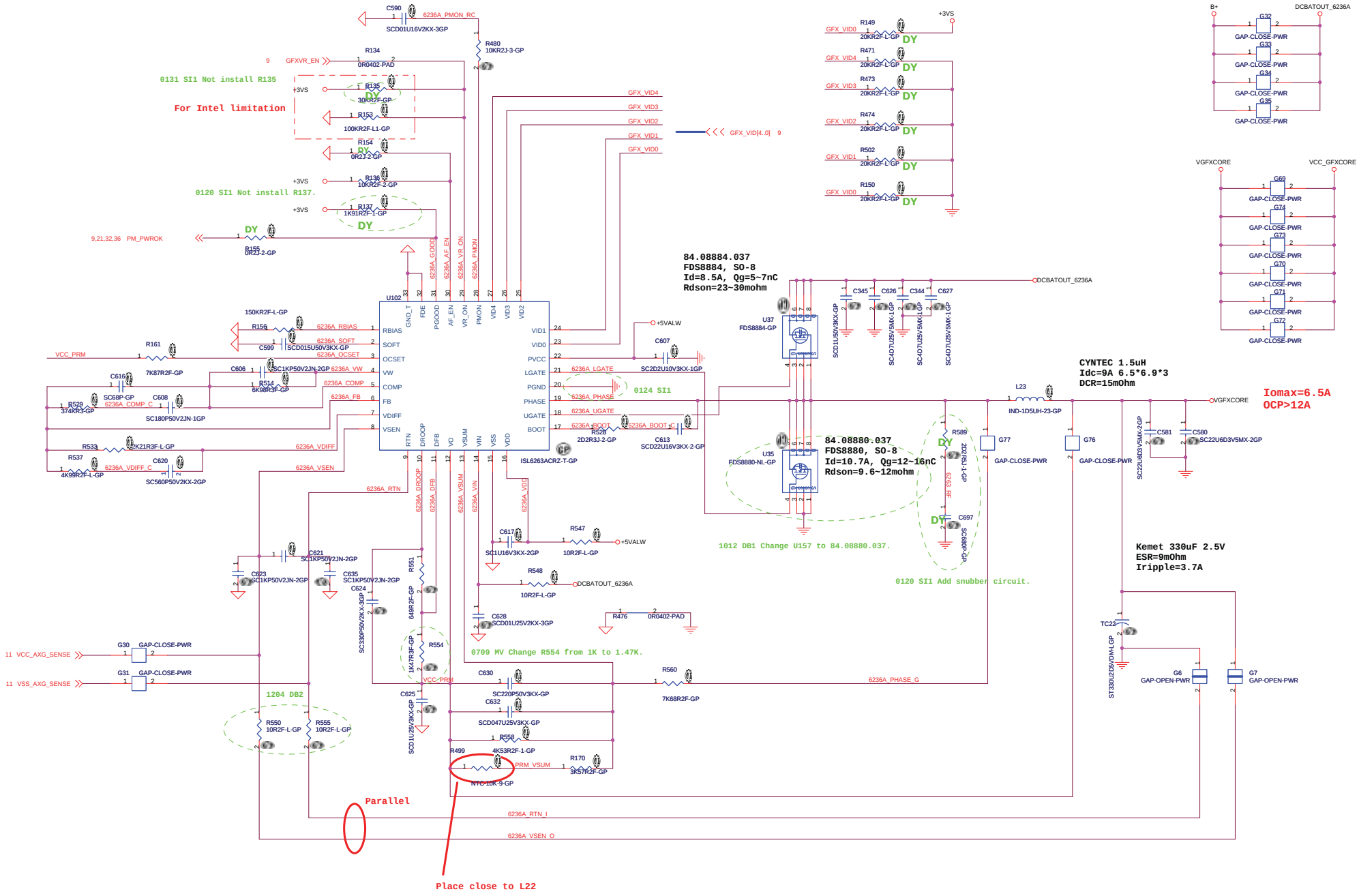
Title: ADP OCP

Size: A2 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 46 of 52



<Core Design>

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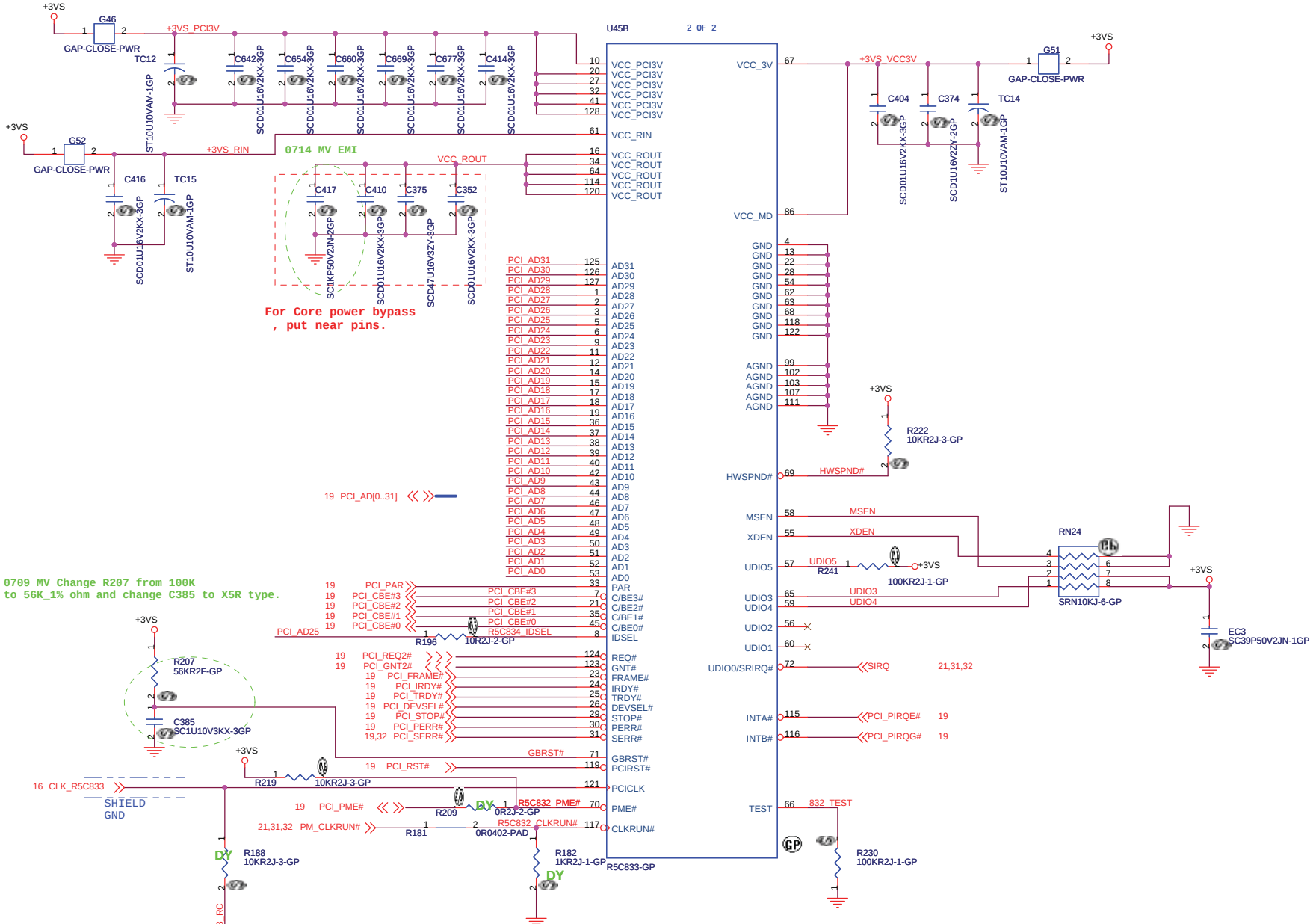
Title: ISL6263A_GFX CORE

Size: C | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 47 of 52



<Core Design>

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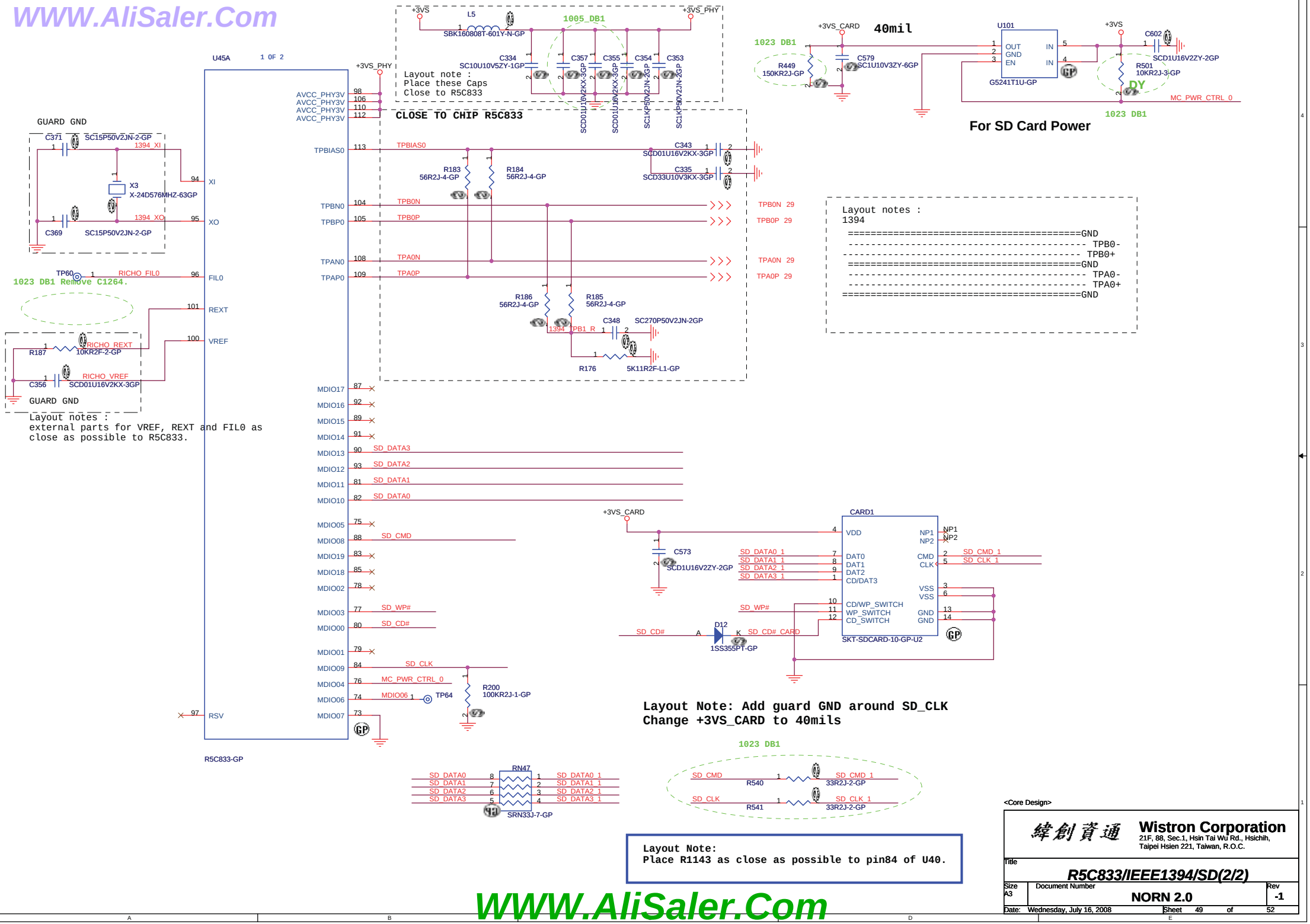
Title: R5C833/PCI(1/2)

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 48 of 52



<Core Design>

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Title: R5C833/IEEE1394/SD(2/2)

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 49 of 52

CAMERA

1203 DB2 Remove R167, R168, R139 and R140 pads.

1019 DB1 Reserve 4 Caps pads.

Place these 4 Caps close to CAP1.

1011 DB1 Correct netnames.

1002 DB1

0319 SI2a

1130 DB2 For layout smoothly.

1130 DB2 Define the pin assignments

1022 DB1

Backlight PWM

Sleep & Rotation

Crtl+Alt+Delect/Rotate

CAMERA Conn.

1003 DB1 Per EMI request.

FingerPrint

1203 DB2 Remove ESD diodes U27 and U31.

0325 SI2a

HOTSTART

FingerPrint Conn.

1011 DB1 Correct netnames.

1001 DB1

SYSTEM CAPACITY BOARD.

1017 DB1 Change the P/N of CAP1 from 20.K0276.008 to 20.K0210.008

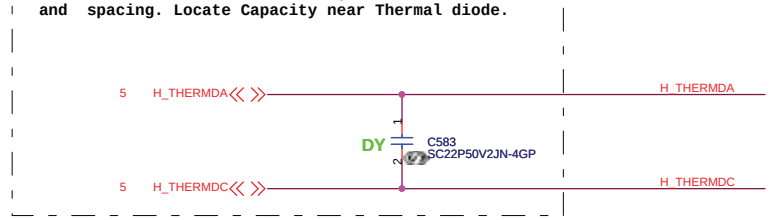
1011 DB1 Not install R326.
1129 DB2 Install R326.
1205 DB2 Not install R326.

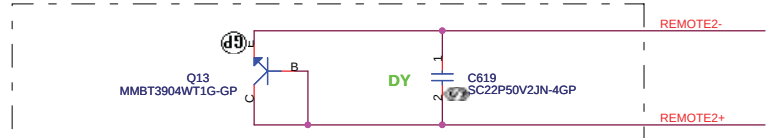
Vol up , Vol down , Mute ,Presentation

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Camera/W-COM/Light Sensor	
Size: A3	Document Number: NORN 2.0
Rev: -1	
Date: Wednesday, July 16, 2008	Sheet 50 of 52

CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.





AMBIENT TEMP: Q24 used for GPU

REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing. Lacate Cap near thermal diode .

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMSC2103 Thermal Sensor

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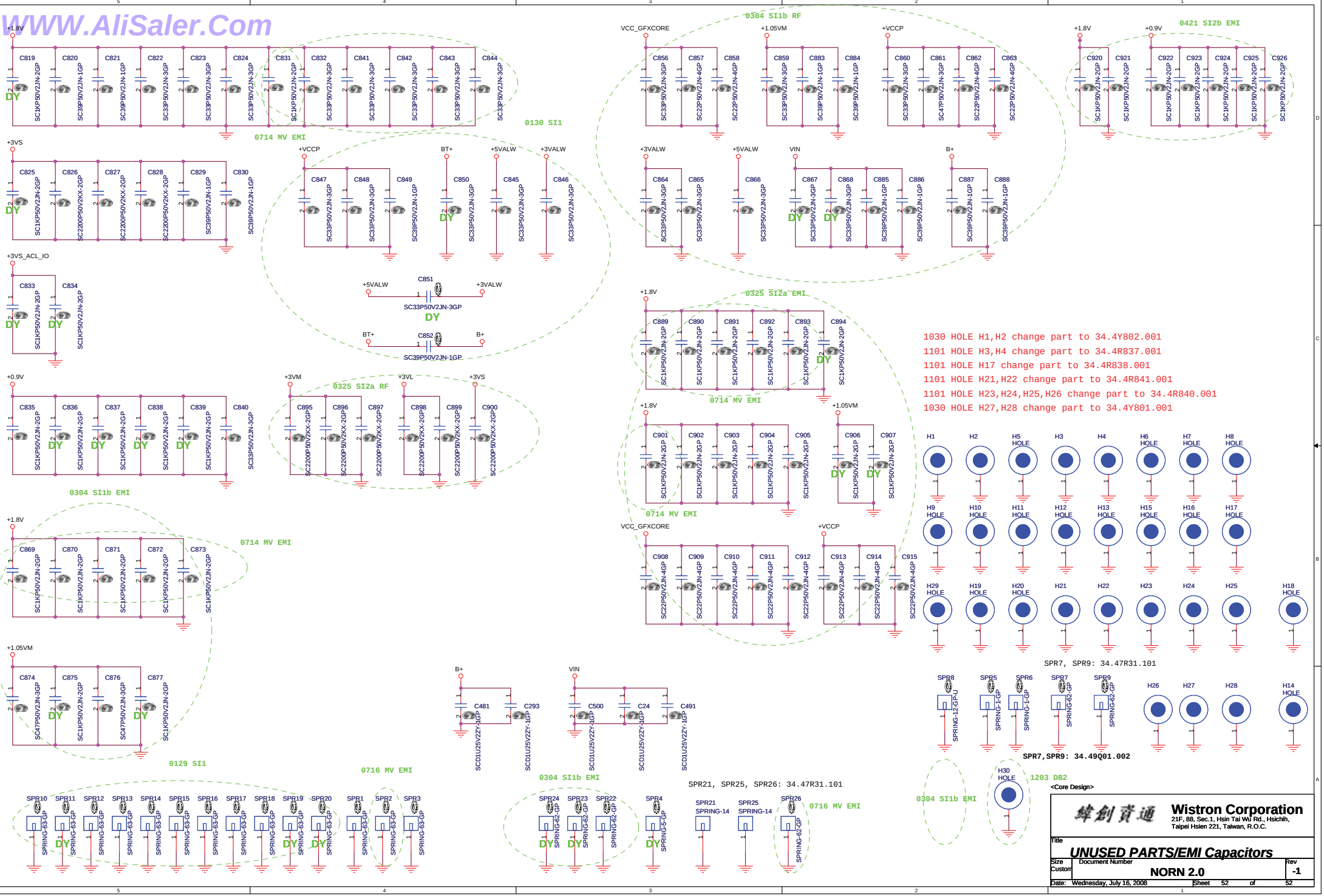

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
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