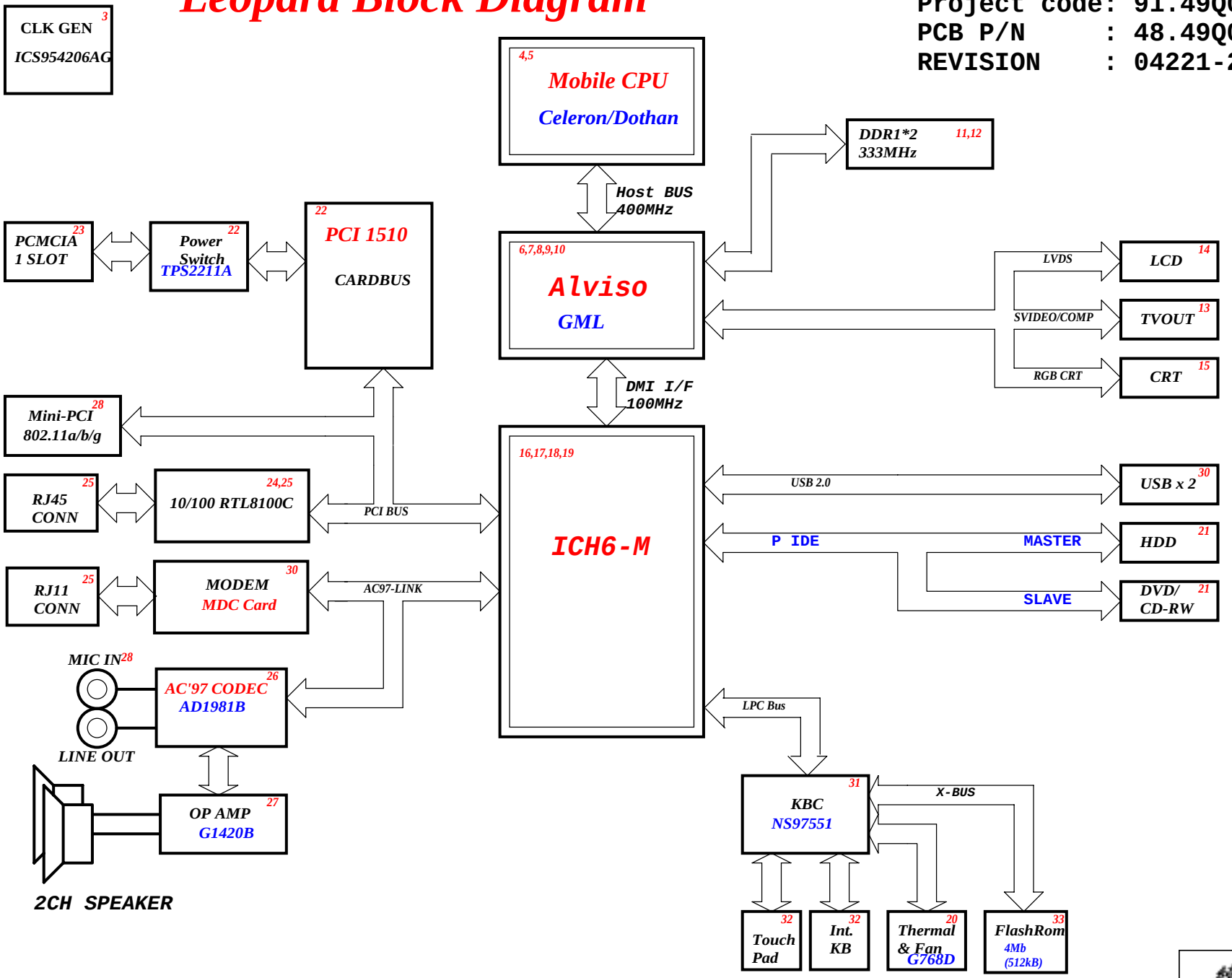
Leopard Block Diagram

Project code: 91.49Q01.001
PCB P/N : 48.49Q01.001
REVISION : 04221-2 DF



SYSTEM DC/DC 37 MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC 38,39 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER 35 MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 36 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

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Title		
Block Diagram		
Size A3	Document Number Leopard	Rev -2
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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
1D25V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

38,39,40,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,40,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,40,41 CORE_GMCH_S0 — CORE_GMCH_S0
12,39 1D25V_S0 — 1D25V_S0
7,11,40 DDR_VREF_S3 — DDR_VREF_S3
5,7,9,17,18,38,39,41 1D5V_S0 — 1D5V_S0
18,39 1D5V_S5 — 1D5V_S5
5 1D5V_VCCA_S0 — 1D5V_VCCA_S0
4,5,36 VCC_CORE_S0 — VCC_CORE_S0
7,9,15,18,40 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,40,41 2D5V_S3 — 2D5V_S3
3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 — 3D3V_S0
28,30,40 3D3V_S3 — 3D3V_S3
17,18,19,24,29,31,35,37,39,40 3D3V_S5 — 3D3V_S5
24,41 3D3V_LAN_S5 — 3D3V_LAN_S5
16,20,31,32,34,35,36,37 3D3V_AUX — 3D3V_AUX
27 5VA_OP_S0 — 5VA_OP_S0
14,15,18,19,20,21,22,26,27,29,32,36,39,40,41 5V_S0 — 5V_S0
14,25,30,32,37,38,40,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
14,35,37,38,39 5V_AUX — 5V_AUX
14,35,37,38,39,40,41 DCBATOUT — DCBATOUT
34,35,41 AD+ — AD+
31,34,35,41 BT+ — BT+

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI PCI1510	AD22	(CARBUS)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#

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Title: ITP
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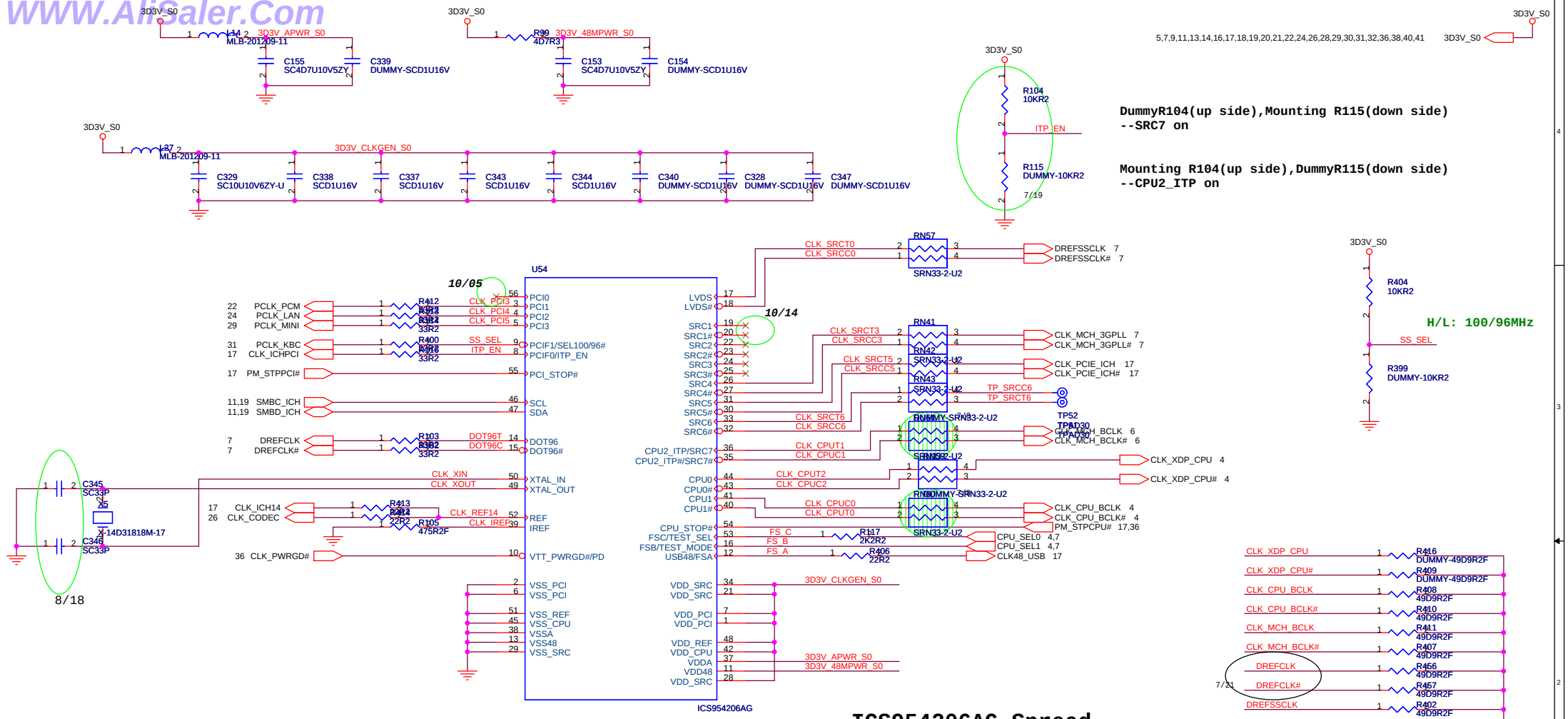
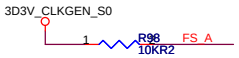


NEAR CLKGEN



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

ICS954206AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5

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Title: Clock Generator (ICS954206AG)

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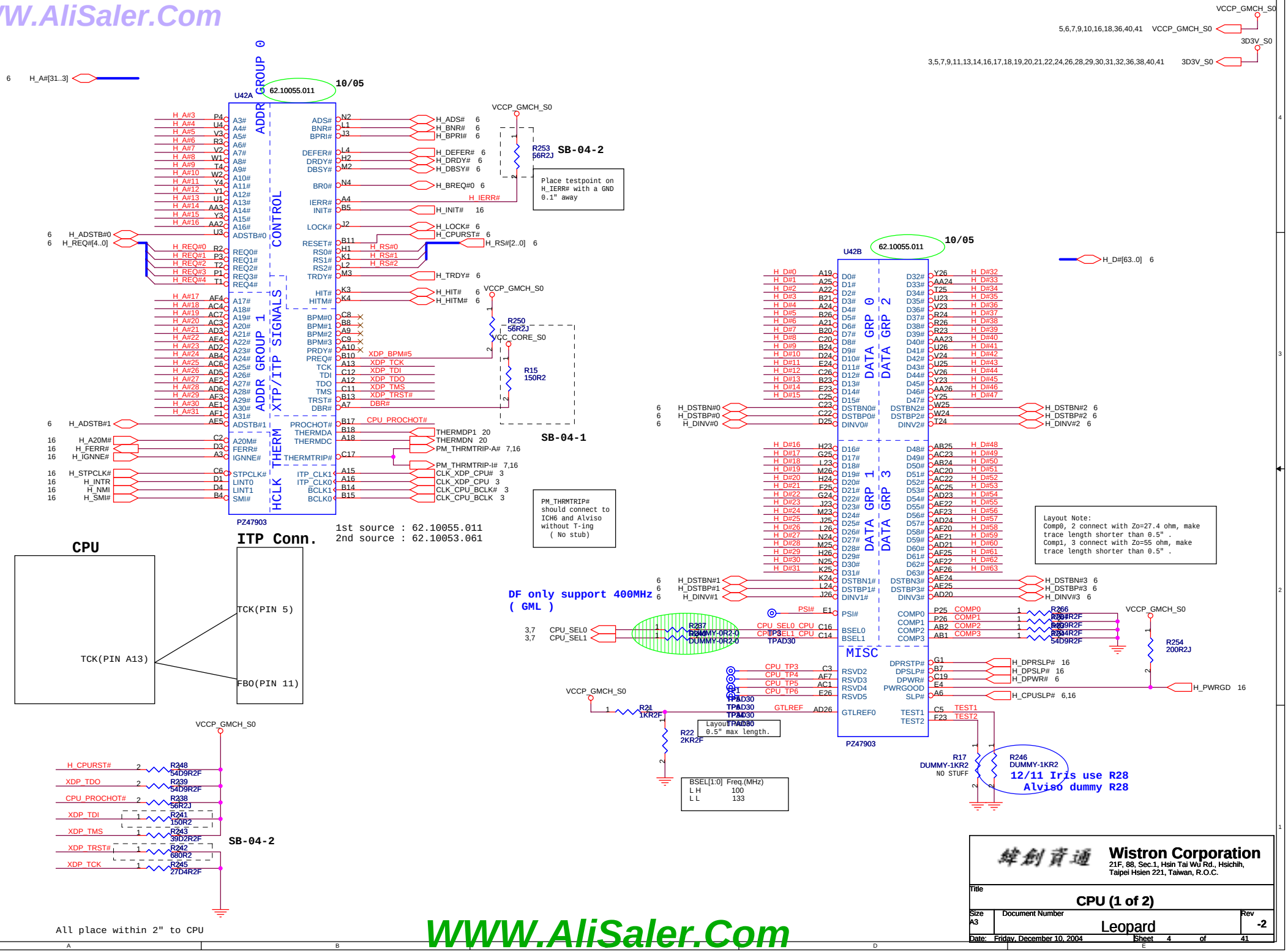

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Title	CPU (1 of 2)
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10/05

1.8V is for Dothan A2 before.

1D5V OR 1D8V
Intel suggest Dothan A2 or later only use 1.5V

U42C — PZ47903 — 62.10055.011

U42D — PZ47903 — 62.10055.011

SB-05-01

PUMA SC

I max = 120 mA

U41 DY-G913C-U

10/14

8/18

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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Title	CPU (2 of 2)
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12/12 Trace 10 mil wide with 20 mil spacing

H_XRCOMP — R61 24D9R2F — H_YRCOMP — R80 24D9R2F

VCCP_GMCH_S0 — R63 54D9R2F — H_XSCOMP — VCCP_GMCH_S0 — R81 54D9R2F — H_YSCOMP

VCCP_GMCH_S0 — R60 221R3F — H_XSWING — R62 100R2F — C76 SCD1U16V

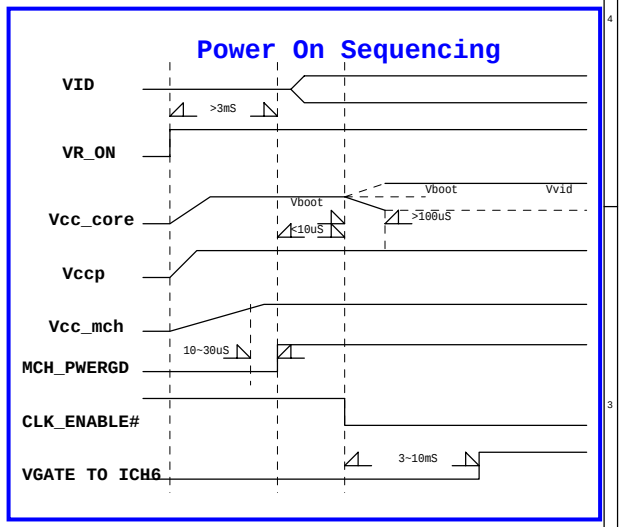
VCCP_GMCH_S0 — R78 221R3F — H_YSWING — R79 100R2F — C94 SCD1U16V

12/12 Trace 10 mil wide with 20 mil spacing

CORE_GMCH_S0
9,10,40,41 CORE_GMCH_S0

VCCP_GMCH_S0
4,5,7,9,10,16,18,36,40,41 VCCP_GMCH_S0

Power On Sequencing



Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

4 H_D#[63..0] — U17A — HOST — 71.0GMCH.AJU

H_A#[31..3] 4

VCCP_GMCH_S0 — R297 100R2F — H_VREF — C281 SCD1U16V — R298 200R2F

2/10 HM1-SC Intel Sightings issue 54489

H_ADS# 4
H_ADSTB#0 4
H_ADSTB#1 4
H_BNR# 4
H_BPRI# 4
H_BREQ#0 4
H_CPURST# 4
CLK_MCH_BCLK# 3
CLK_MCH_BCLK 3
H_DBSY# 4
H_DEFER# 4
H_DINV#[3..0] 4
H_DPWR# 4
H_DRDY# 4
H_DSTBN#[3..0] 4
H_DSTBP#[3..0] 4
H_HIT# 4
H_HITM# 4
H_LOCK# 4
H_REQ#[4..0] 4
H_RS#[2..0] 4
H_TRDY# 4
H_CPUSLP# 4,16

CORE_GMCH_S0 — R347 DUMMY-0R2-0 — H_DPWR#

TP37 TPAD30 — TP_H_EDRDY#
TP9 TPAD30 — TP_H_PCREQ#

R296 0R2-0

PUMA SC

For Banias/Celeron-M:R1079=DUMMY
For Dothan A:R1079=DUMMY
For Dothan B:R1079=0R

ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

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Title: GMCH (1 of 5)
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Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die

9,15,18,40 2D5V_S0 → 2D5V_S0
9,10,11,12,38,39,40,41 2D5V_S3 → 2D5V_S3
5,9,17,18,38,39,41 1D5V_S0 → 1D5V_S0
6,9,10,40,41 CORE_GMCH_S0 → CORE_GMCH_S0
11,40 DDR_VREF_S3 → DDR_VREF_S3

U17B

DMI: DMI_TXN0 AA31, DMI_TXN1 AB35, DMI_TXN2 AC31, DMI_TXN3 AD35 (17 DMI_TXN[3..0]) → DMIRXN0..3
DMI_TXP0 Y31, DMI_TXP1 AA35, DMI_TXP2 AB31, DMI_TXP3 AC35 (17 DMI_TXP[3..0]) → DMIRXP0..3
DMI_RXN0 AA33, DMI_RXN1 AB37, DMI_RXN2 AC33, DMI_RXN3 AD37 (17 DMI_RXN[3..0]) → DMITXN0..3
DMI_RXP0 Y33, DMI_RXP1 AA37, DMI_RXP2 AB33, DMI_RXP3 AC37 (17 DMI_RXP[3..0]) → DMITXP0..3

CFG/RSVD: CFG0 G16 … CFG20 G23; RSVD21 G25 … RSVD27 D25

DDR MUXING:
11 CLK_DDR0 AM33, CLK_DDR1 AL1; CLK_DDR3 AE11, CLK_DDR4 AJ34; CLK_DDR5 AF6, CLK_DDR6 AC10
11 CLK_DDR0# AN33, CLK_DDR1# AK1; CLK_DDR3# AE10, CLK_DDR4# AJ33; CLK_DDR5# AF5, CLK_DDR6# AD10
11,12 M_CKE0_R# AP21, M_CKE1_R# AM21, M_CKE2_R# AH21, M_CKE3_R# AK21
11,12 M_CS0_R# AN16, M_CS1_R# AM14, M_CS2_R# AH15, M_CS3_R# AG16
M_OCDCOMP0 AF22, M_OCDCOMP1 AF16
SM_ODT0 AP14, SM_ODT1 AL15, SM_ODT2 AM11, SM_ODT3 AN10
M_RCOMPN AK10, M_RCOMPP AK11; SMVREF0 AF37, SMVREF1 AD1; SMXSLEW AE27, SMYSLEW AE28; SMXSLEWIN AF9, SMYSLEWIN AF10; SMXSLEWOUT AE29, SMYSLEWOUT AF10

Layout Note: Route as short as possible
R364 40D2R2F, R363 40D2R2F
DDR_VREF_S3
C107 SCD1U10V2MX-1

PM: BM_BUSY# J23, EXT_TS0# J21, EXT_TS1# H22, THRMTRIP# E5, PWROK AD30, RSTIN# AE29
PM_EXTTS#0 → PM_EXTTS#0 J21; PM_EXTTS#1 → PM_EXTTS#1 H22
PM_BMBUSY# 17
PM_THRMTRIP-A# 4,16 → GMCH_PWROK 36 → R365 100R2 → PLT_RST1# 19
RST1# AE29

CLK: DREF_CLKN A24, DREF_CLKP A23, DREF_SSCLKN C37, DREF_SSCLKP D37
DREFCLK# 3, DREFCLK 3, DREFSSCLK# 3, DREFSSCLK 3

NC: NC#AP37 AP37 … NC#A37 A37
GMCH_TP3 AP37, GMCH_TP4 AN37, GMCH_TP5 AP36, GMCH_TP6 AP2, GMCH_TP7 AP1, GMCH_TP8 AN1, GMCH_TP9 B1, GMCH_TP10 A2, GMCH_TP11 B37, GMCH_TP12 A36, GMCH_TP13 A37

71.0GMCH.AJU

Intel suggest NC Due to votusly DVO

U17G

MISC: SDVO_DAT H24, SDVO_CLK H25, GCLKN AB29, GCLKP AC29
3 CLK_MCH_3GPLL#, 3 CLK_MCH_3GPLL → TP41 TPAD30
TV: TVDAC_A A15, TVDAC_B A17, TVDAC_C B15, TV_REFSET J18, TV_IRTNA B16, TV_IRTNB B17, TV_IRTNC
COMP_VGA → R51 75R2F, R52 150R2F, R53 150R2F → TV_REFSET → R331 4K99R2F
8/23
SB-07-01

VGA: 13 LUMA_VGA, 13 CRMA_VGA
15 GMCH_DDCCLK, 15 GMCH_DDCDATA
Trace impendance 50ohm Less than 0.5", trace impendance 37.5ohm
DDCCLK E24, DDCDATA E23, BLUE E21, BLUE# D21, GREEN C20, GREEN# B20, RED A19, RED# B19, VSYNC H21, HSYNC G21, CRTIREF J20, REFSET
15 VGA_BLUE, 15 VGA_GREEN, 15 VGA_RED → R57 150R2F, R58 255R2F
15 VGA_VSYNC, 15 VGA_HSYNC
SB-07-01

LVDS: LBKLT_CRTL E25, LBKLT_EN F25, LCTLA_CLK C23, LCTLB_DATA C22, LDDC_CLK F23, LDDC_DATA F22, LVDD_EN F26, LIBG C33, LVBG C31, LVREFH F28, LVREFL F27
31 BL_ON
14 LCDVDD_ON → PJ30 STUFF
LCTLA_CLK 1, LCTLB_DATA 2, LDDC_CLK 3, LDDC_DATA 4 → RN40 SRN2K2
TXACLK- B30, TXACLK+ B29, TXBCLK- C25, TXBCLK+ C24 → LACLKN, LACLKP, LBCLKN, LBCLKP
TXAOUT0- B34, TXAOUT1- B33, TXAOUT2- B32 → LADATAN0, LADATAN1, LADATAN2
TXAOUT0+ A34, TXAOUT1+ A33, TXAOUT2+ B31 → LADATAP0, LADATAP1, LADATAP2
TXBOUT0- C29, TXBOUT1- D28, TXBOUT2- C27 → LBDATAN0, LBDATAN1, LBDATAN2
TXBOUT0+ C28, TXBOUT1+ D27, TXBOUT2+ C26 → LBDATAP0, LBDATAP1, LBDATAP2
BL_ON → R337 100KR2; LBKLT_CRTL → R339 100KR2; LIBG → R335 1K5R2F
3D3V_S0
RN39 SRN4D7KJ
LDDC_CLK, LDDC_DATA → U13 2N7002DW
14 EDID_CLK, 14 EDID_DAT
71.0GMCH.AJU

PCI-EXPRESS GRAPHICS:
EXP_COMPI D36, EXP_ICOMPO D34 → PEG_COMP → R64 24D9R2F
EXP_RXN0 E30 … EXP_RXN15 Y34
EXP_RXP0 D30 … EXP_RXP15 W34
EXP_TXN0 E32 … EXP_TXN15 Y36
EXP_TXP0 D32 … EXP_TXP15 W36

1D5V_S0
2D5V_S0
When High 1K Ohm
R336 DUMMY-R2 → CFG18
R332 DUMMY-R2 → CFG19
R333 DUMMY-R2 → CFG20

2D5V_S0
R334 10KR2 PM_EXTTS#0
R338 10KR2 PM_EXTTS#1

FOR DDR1
2D5V_S3
R362 80D6R2F
M_RCOMPN
M_RCOMPP
R384 80D6R2F
7/14

VCCP_GMCH_S0
Ref ALVISO EDS-1 Page 115
For Dothan-B
R305 10KR2, R47 DUMMY-1KR2, R48 1KR2
8/18
CFG2 → CPU_SEL0 3,4
CFG1 → CPU_SEL1 3,4
CFG0
R45 4K7R2, R49 DUMMY-4K7R2
CFG(2..1) FREQ.(MHz)
10 400
00 533
11 Reserved
CFG2=0(R97):133MHZ
CFG2=1(R98):100MHZ

When Low 2.2K Ohm
R11 DUMMY-R2 → CFG3
R09 DUMMY-R2 → CFG4
R04 DUMMY-R2 → CFG5
R12 DUMMY-R2 → CFG6
R13 DUMMY-R2 → CFG7
R01 DUMMY-R2 → CFG8
R08 DUMMY-R2 → CFG9
R10 DUMMY-R2 → CFG10
R02 DUMMY-R2 → CFG11
R07 DUMMY-R2 → CFG12
R99 DUMMY-R2 → CFG13
R06 DUMMY-R2 → CFG14
R03 DUMMY-R2 → CFG15
R00 DUMMY-R2 → CFG16
R02 DUMMY-R2 → CFG17

Strapping

CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

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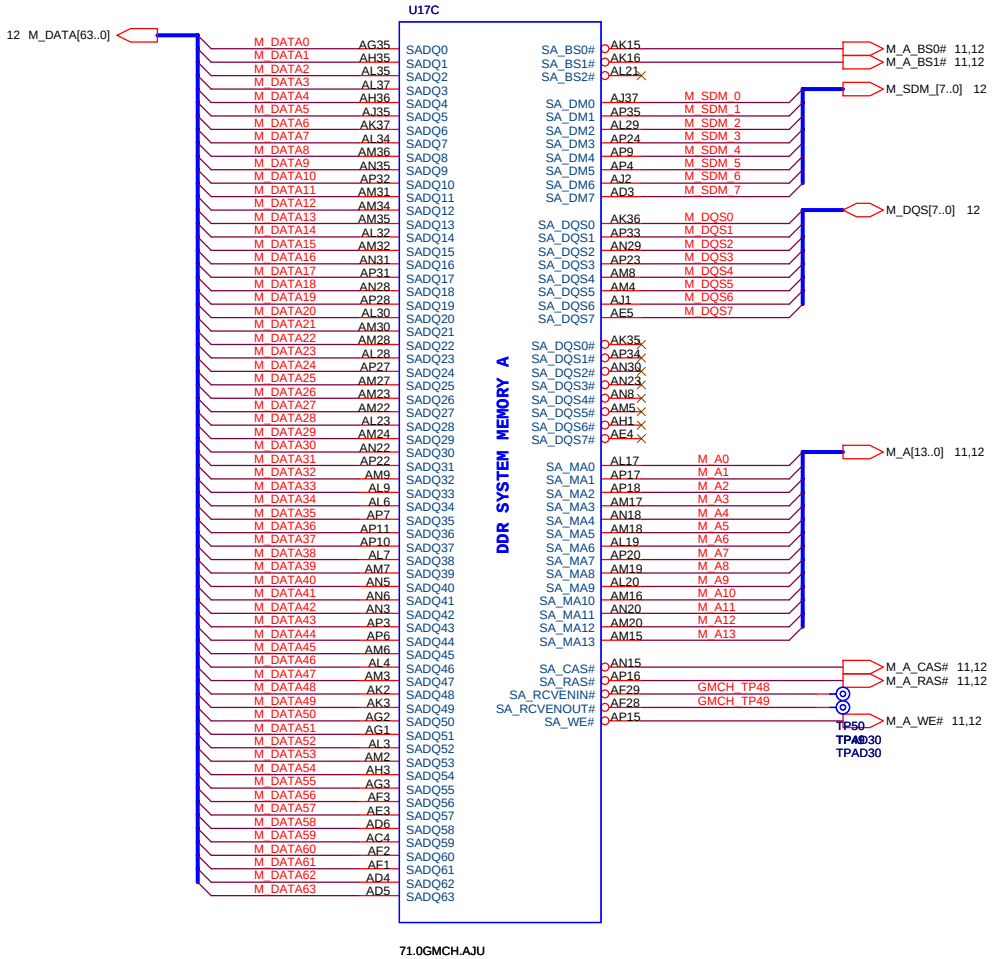
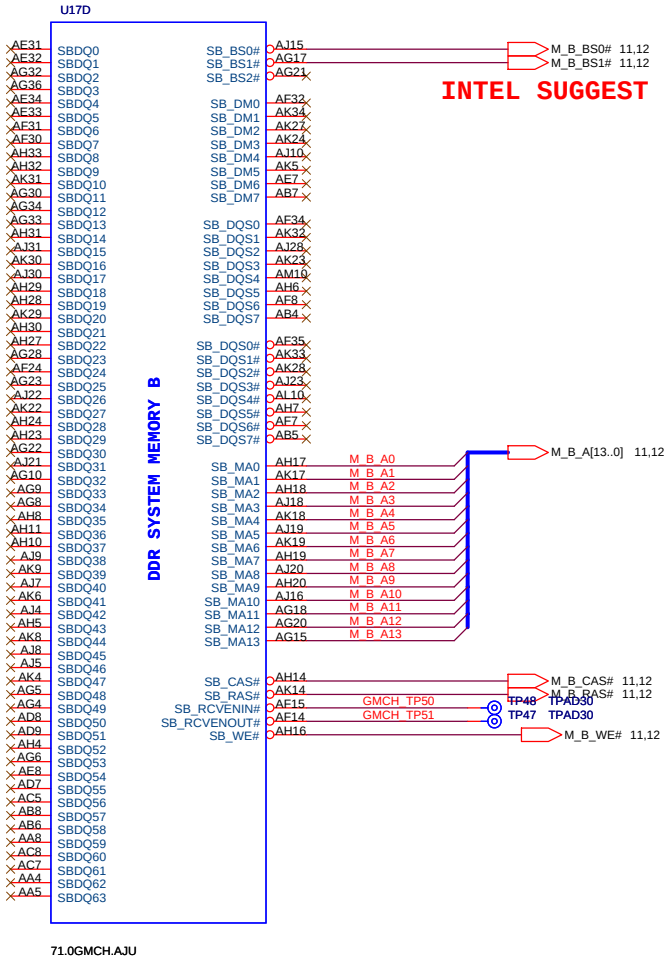
SUPPORT DDR333 ONLY





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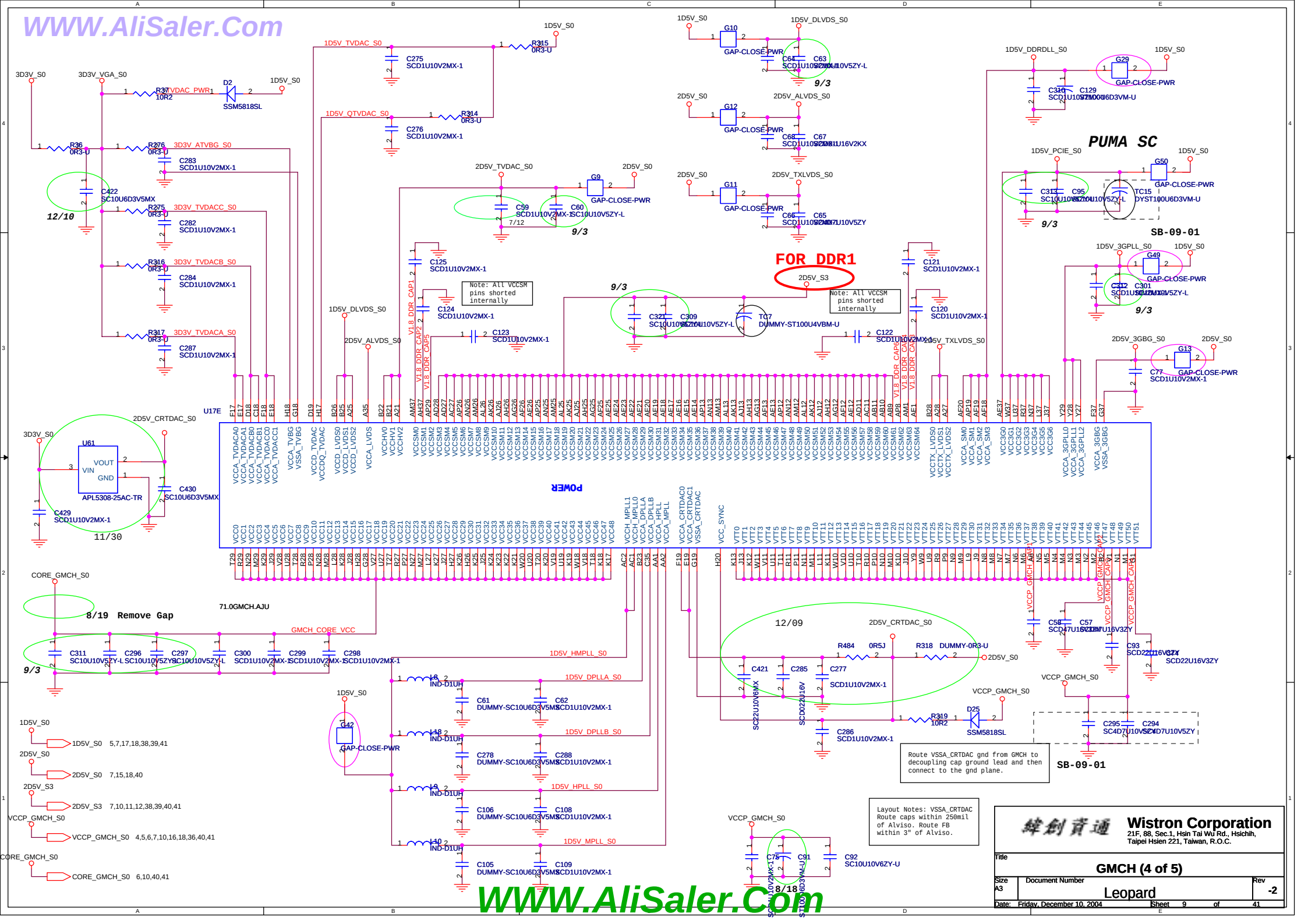
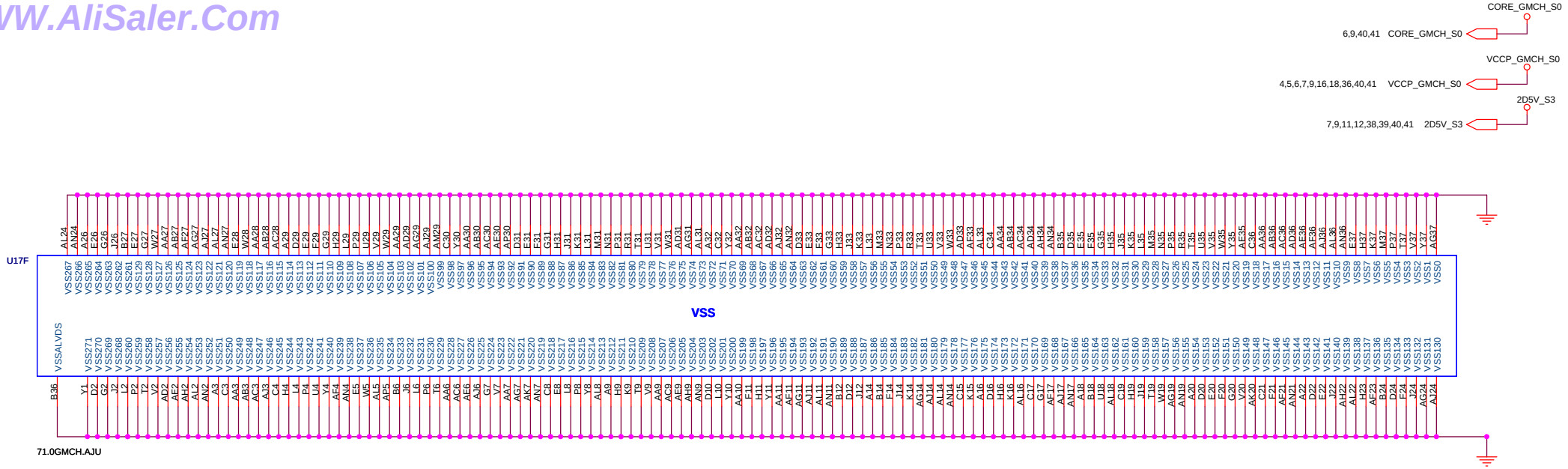
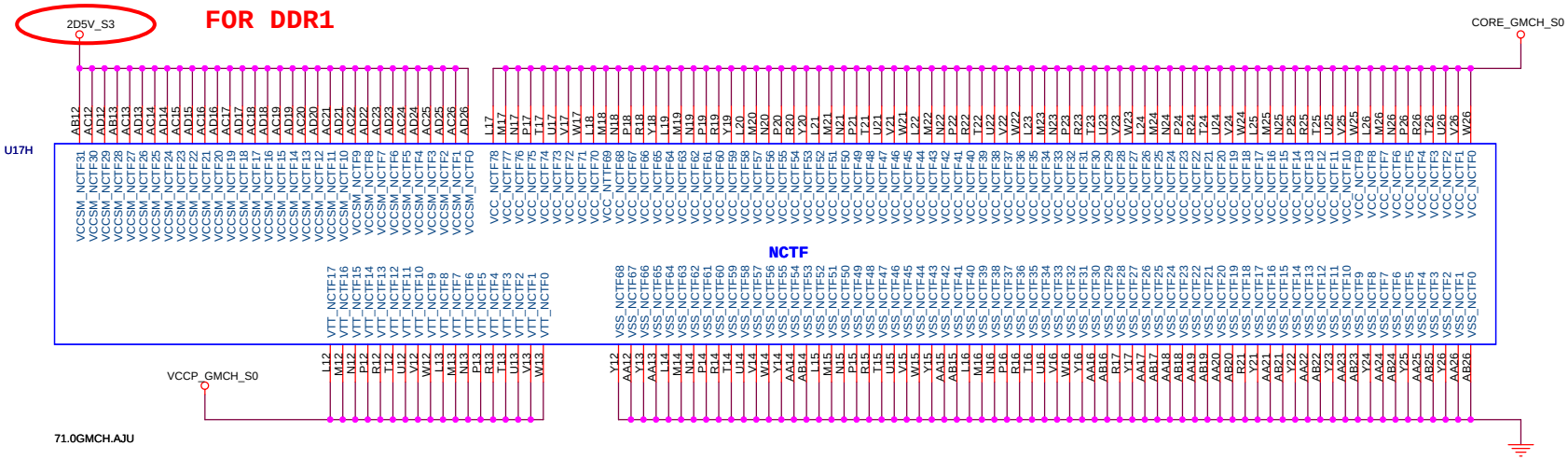






緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GMCH (5 of 5)		
Size: A3	Document Number: Leopard	Rev: -2
Date: Thursday, December 09, 2004	Sheet 10 of 41	

SUPPORT DDR333 ONLY

DDR_VREF_S3

8,12 M_A[13..0]

DM2

MH1

C333 SCD1U16V

2D5V_S3

M_DATA_R_0 M_DATA_R_1 M_DQS_R0 M_DATA_R_2 M_DATA_R_3 M_DATA_R_8 M_DATA_R_9 M_DQS_R1 M_DATA_R_10 M_DATA_R_11

M_DATA_R_4 M_DATA_R_5 M_SDM_R0 M_DATA_R_6 M_DATA_R_7 M_DATA_R_12 M_DATA_R_13 M_SDM_R1 M_DATA_R_14 M_DATA_R_15

CLK_DDR0 CLK_DDR0#

M_DATA_R_16 M_DATA_R_17 M_DQS_R2 M_DATA_R_18 M_DATA_R_19 M_DATA_R_24 M_DATA_R_25 M_DQS_R3 M_DATA_R_26 M_DATA_R_27

M_DATA_R_20 M_DATA_R_21 M_SDM_R2 M_DATA_R_22 M_DATA_R_23 M_DATA_R_28 M_DATA_R_29 M_SDM_R3 M_DATA_R_30 M_DATA_R_31

CLK_DDR2 CLK_DDR2#

7,12 M_CKE1_R# — M_CKE0_R# 7,12

TP24 TP-2

M_A12 M_A9 M_A7 M_A5 M_A3 M_A1 M_A10 M_A13

M_A11 M_A8 M_A6 M_A4 M_A2 M_A0

8,12 M_A_BS0# 8,12 M_A_WE# 7,12 M_CS0_R#

M_A_BS1# 8,12 M_A_RAS# 8,12 M_A_CAS# 8,12 M_CS1_R# 7,12

M_DATA_R_32 M_DATA_R_33 M_DQS_R4 M_DATA_R_34 M_DATA_R_35 M_DATA_R_40 M_DATA_R_41 M_DQS_R5 M_DATA_R_42 M_DATA_R_43

M_DATA_R_36 M_DATA_R_37 M_SDM_R4 M_DATA_R_38 M_DATA_R_39 M_DATA_R_44 M_DATA_R_45 M_SDM_R5 M_DATA_R_46 M_DATA_R_47

CLK_DDR1# 7 CLK_DDR1 7

M_DATA_R_48 M_DATA_R_49 M_DQS_R6 M_DATA_R_50 M_DATA_R_51 M_DATA_R_56 M_DATA_R_57 M_DQS_R7 M_DATA_R_58 M_DATA_R_59

M_DATA_R_52 M_DATA_R_53 M_SDM_R6 M_DATA_R_54 M_DATA_R_55 M_DATA_R_60 M_DATA_R_61 M_SDM_R7 M_DATA_R_62 M_DATA_R_63

SMBD_ICH SMBC_ICH 3D3V_S0

MH2

SX_SODIMM200-7U 62.10024.481

1st source : 62.10024.481
2nd source : 62.10017.421

10/05

High 9.2mm NORMAL TYPE

12 M_DATA_R_[63..0]
8,12 M_B_A[13..0]

2D5V_S3

CLK_DDR2 — R141 200R2J
CLK_DDR5 — R109 200R2J
CLK_DDR2# — R140 200R2J
CLK_DDR5# — R107 200R2J

12/15 INTEL Ref. schematic

DM1

M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12

8,12 M_B_BS0# 8,12 M_B_BS1#

M_DATA_R_0 M_DATA_R_1 M_DATA_R_2 M_DATA_R_3 M_DATA_R_4 M_DATA_R_5 M_DATA_R_6 M_DATA_R_7 M_DATA_R_8 M_DATA_R_9 M_DATA_R_10 M_DATA_R_11 M_DATA_R_12 M_DATA_R_13 M_DATA_R_14 M_DATA_R_15 M_DATA_R_16 M_DATA_R_17 M_DATA_R_18 M_DATA_R_19 M_DATA_R_20 M_DATA_R_21 M_DATA_R_22 M_DATA_R_23 M_DATA_R_24 M_DATA_R_25 M_DATA_R_26 M_DATA_R_27 M_DATA_R_28 M_DATA_R_29 M_DATA_R_30 M_DATA_R_31 M_DATA_R_32 M_DATA_R_33 M_DATA_R_34 M_DATA_R_35 M_DATA_R_36 M_DATA_R_37 M_DATA_R_38 M_DATA_R_39 M_DATA_R_40 M_DATA_R_41 M_DATA_R_42 M_DATA_R_43 M_DATA_R_44 M_DATA_R_45 M_DATA_R_46 M_DATA_R_47 M_DATA_R_48 M_DATA_R_49 M_DATA_R_50 M_DATA_R_51 M_DATA_R_52 M_DATA_R_53 M_DATA_R_54 M_DATA_R_55 M_DATA_R_56 M_DATA_R_57 M_DATA_R_58 M_DATA_R_59 M_DATA_R_60 M_DATA_R_61 M_DATA_R_62 M_DATA_R_63

CB0 CB1 CB2 CB3 CB4 CB5 CB6 CB7

NC NC/(RESET#) NC/A13 NC/BA2 NC NC NC

TP53 TP-2 M_B_A12

8,12 M_B_RAS# 8,12 M_B_CAS# 8,12 M_B_WE#

/RAS /CAS /WE

DDR_VREF_S3

3D3V_S0

C180 SCD1U10V2MX-1

VREF VREF VDDSPD VDDID GND

DDR-SODIMM200-U1

10/05

Low 5.2mm NORMAL TYPE

3,5,7,9,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41

/CS0 /CS1 — M_CS2_R# 7,12 M_CS3_R# 7,12

CKE0 CKE1 — M_CKE2_R# 7,12 M_CKE3_R# 7,12

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS8

M_DQS_R0 M_DQS_R1 M_DQS_R2 M_DQS_R3 M_DQS_R4 M_DQS_R5 M_DQS_R6 M_DQS_R7

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 DM8

M_SDM_R0 M_SDM_R1 M_SDM_R2 M_SDM_R3 M_SDM_R4 M_SDM_R5 M_SDM_R6 M_SDM_R7

CK0 /CK0 CK1 /CK1 CK2 /CK2

CLK_DDR3 7 CLK_DDR3# 7 CLK_DDR4 7 CLK_DDR4# 7 CLK_DDR5 CLK_DDR5#

SCL SDA — SMBC_ICH 3,19 SMBD_ICH 3,19

SA0 SA1 SA2 — 3D3V_S0

VDD — 2D5V_S3

VSS

3D3V_S0 2D5V_S3 DDR_VREF_S3

7,9,10,12,38,39,40,41 2D5V_S3

7,40 DDR_VREF_S3

M_DQS_R[7..0] 12
M_SDM_R[7..0] 12

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR Socket

Size: Custom | Document Number: Leopard | Rev: -2

Date: Thursday, December 09, 2004 | Sheet 11 of 41

SERIES DAMPING

SC

Change RN to small size

RN45 SRN10-1: M_DATA60, M_DATA55, M_DATA53, M_SDM_6, M_DATA63, M_DATA62, M_SDM_7, M_DATA61 → M_DATA_R_60, M_DATA_R_55, M_DATA_R_54, M_SDM_R6, M_DATA_R_63, M_DATA_R_62, M_SDM_R7, M_DATA_R_61

RN6 SRN10-1: M_DATA421, M_DATA432, M_DATA483, M_DATA494 → M_DATA_R_42, M_DATA_R_43, M_DATA_R_48, M_DATA_R_49

RN56 SRN10-1: M_DATA6, M_SDM_0, M_DATA5, M_DATA4 → M_DATA_R_6, M_SDM_R0, M_DATA_R_5, M_DATA_R_4

RN54 SRN10-1: M_DATA211, M_DATA202, M_DATA153, M_DATA144 → M_DATA_R_21, M_DATA_R_20, M_DATA_R_15, M_DATA_R_14

RN55 SRN10-1: M_SDM_1, M_DATA13, M_DATA12, M_DATA7 → M_SDM_R1, M_DATA_R_13, M_DATA_R_12, M_DATA_R_7

RN14 SRN10-1: M_DATA101, M_DATA112, M_DATA173, M_DATA164 → M_DATA_R_10, M_DATA_R_11, M_DATA_R_17, M_DATA_R_16

RN13 SRN10-1: M_DQS2, M_DATA19, M_DATA18, M_DATA24 → M_DQS_R2, M_DATA_R_19, M_DATA_R_18, M_DATA_R_24

RN46 SRN10-1: M_DATA531, M_DATA522, M_DATA473, M_DATA464 → M_DATA_R_53, M_DATA_R_52, M_DATA_R_47, M_DATA_R_46

RN12 SRN10-1: M_DATA251, M_DQS3, M_DATA263, M_DATA274 → M_DATA_R_25, M_DQS_R3, M_DATA_R_26, M_DATA_R_27

RN5 SRN10-1: M_DQS6, M_DATA502, M_DATA513, M_DATA564 → M_DQS_R6, M_DATA_R_50, M_DATA_R_51, M_DATA_R_56

RN8 SRN10-1: M_DATA321, M_DATA332, M_DQS4, M_DATA344 → M_DATA_R_32, M_DATA_R_33, M_DQS_R4, M_DATA_R_34

RN1 SRN10-1: M_DATA351, M_DATA402, M_DATA413, M_DQS5 → M_DATA_R_35, M_DATA_R_40, M_DATA_R_41, M_DQS_R5

RN4 SRN10-1: M_DQS7, M_DATA572, M_DATA593, M_DATA584 → M_DQS_R7, M_DATA_R_57, M_DATA_R_59, M_DATA_R_58

RN16 SRN10-1: M_DATA0, M_DATA1, M_DQS0, M_DATA2 → M_DATA_R_0, M_DATA_R_1, M_DQS_R0, M_DATA_R_2

RN15 SRN10-1: M_DATA3, M_DATA8, M_DATA9, M_DQS1 → M_DATA_R_3, M_DATA_R_8, M_DATA_R_9, M_DQS_R1

RN53 SRN10-1: M_DATA281, M_DATA232, M_DATA223, M_SDM_2 → M_DATA_R_28, M_DATA_R_23, M_DATA_R_22, M_SDM_R2

RN48 SRN10-1: M_DATA381, M_SDM_4, M_DATA373, M_DATA364 → M_DATA_R_38, M_SDM_R4, M_DATA_R_37, M_DATA_R_36

RN52 SRN10-1: M_DATA311, M_DATA302, M_SDM_3, M_DATA294 → M_DATA_R_31, M_DATA_R_30, M_SDM_R3, M_DATA_R_29

RN47 SRN10-1: M_SDM_5, M_DATA452, M_DATA443, M_DATA394 → M_SDM_R5, M_DATA_R_45, M_DATA_R_44, M_DATA_R_39

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

2D5V_S3

C197 SCD1U16V, C173 SCD1U16V, C163 SCD1U16V, C156 SCD1U16V, C164 SCD1U16V, C165 SCD1U16V, C331 SCD1U16V, C330 SCD1U16V

C145 SCD1U16V, C332 SCD1U16V, C146 SCD1U16V, C168 SCD1U16V, C172 SCD1U16V, C195 SCD1U16V, C189 SCD1U16V, C183 SCD1U16V

C200 SCD1U16V, C341 SC10U10V5ZY-L, C348 SC10U10V5ZY-L, EC34 SCD1U16V, EC30 SCD1U16V, EC39 SCD1U16V, EC42 SCD1U16V

9/3

1D25V_S0

RN29 SRN56-1: M_DATA_R_4, M_DATA_R_5, M_SDM_R0, M_DATA_R_6 → C196 SCD1U16V

RN28 SRN56-1: M_DATA_R_7, M_DATA_R_13, M_DATA_R_12, M_SDM_R1 → C365 DUMMY-SCD01U16V2KX

RN66 SRN56-1: M_DATA_R_2, M_DQS_R0, M_DATA_R_1, M_DATA_R_0 → C198 SCD1U16V

RN72 SRN56-1: M_DQS_R1, M_DATA_R_9, M_DATA_R_8, M_DATA_R_3 → C349 SCD1U16V

RN75 SRN56-1: M_DATA_R_24, M_DATA_R_19, M_DATA_R_18, M_DQS_R2 → C358 DUMMY-SCD01U16V2KX

RN69 SRN56-1: M_DATA_R_27, M_DATA_R_26, M_DQS_R3, M_DATA_R_25 → C359 SCD1U16V

RN67 SRN56-1: M_DATA_R_14, M_DATA_R_15, M_DATA_R_21, M_DATA_R_20 → C355 SCD1U16V

RN71 SRN56-1: M_DATA_R_17, M_DATA_R_16, M_DATA_R_11, M_DATA_R_10 → C177 DUMMY-SCD01U16V2KX

RN65 SRN56-1: M_SDM_R2, M_DATA_R_23, M_DATA_R_22, M_DATA_R_28 → C174 SCD1U16V

RN25 SRN56-1: M_SDM_R3, M_DATA_R_29, M_DATA_R_30, M_DATA_R_31 → C185 SCD1U16V

RN64 SRN56-1: M_DATA_R_47, M_DATA_R_46, M_DATA_R_52, M_DATA_R_53 → C187 DUMMY-SCD01U16V2KX

RN63 SRN56-1: M_DATA_R_49, M_DATA_R_48, M_DATA_R_43, M_DATA_R_42 → C362 SCD1U16V

RN26 SRN56-1: M_DATA_R_37, M_DATA_R_36, M_SDM_R4, M_DATA_R_38 → C188 SCD1U16V

RN21 SRN56-1: M_DATA_R_39, M_DATA_R_44, M_DATA_R_45, M_SDM_R5 → C357 DUMMY-SCD01U16V2KX

RN60 SRN56-1: M_DATA_R_34, M_DQS_R4, M_DATA_R_33, M_DATA_R_32 → C157 SCD1U16V

RN61 SRN56-1: M_DQS_R5, M_DATA_R_41, M_DATA_R_40, M_DATA_R_35 → C158 SCD1U16V

RN59 SRN56-1: M_SDM_R6, M_DATA_R_54, M_DATA_R_55, M_DATA_R_60 → C176 DUMMY-SCD01U16V2KX

RN58 SRN56-1: M_DATA_R_61, M_SDM_R7, M_DATA_R_62, M_DATA_R_63 → C354 SCD1U16V

RN57 SRN56-1: M_DATA_R_56, M_DATA_R_51, M_DATA_R_50, M_DQS_R6 → C159 SCD1U16V

RN62 SRN56-1: M_DATA_R_59, M_DATA_R_58, M_DQS_R7, M_DATA_R_57 → C186 DUMMY-SCD01U16V2KX

RN27 SRN56-1: M_DATA_R_4, M_DATA_R_5, M_SDM_R0, M_DATA_R_6 → C367 SCD1U16V

RN28 SRN56-1: M_DATA_R_7, M_DATA_R_13, M_DATA_R_12, M_SDM_R1 → C161 SCD1U16V

RN66 SRN56-1: M_DATA_R_2, M_DQS_R0, M_DATA_R_1, M_DATA_R_0 → C171 DUMMY-SCD01U16V2KX

RN72 SRN56-1: M_DQS_R1, M_DATA_R_9, M_DATA_R_8, M_DATA_R_3 → C192 SCD1U16V

RN75 SRN56-1: M_DATA_R_24, M_DATA_R_19, M_DATA_R_18, M_DQS_R2 → C202 SCD1U16V

RN69 SRN56-1: M_DATA_R_27, M_DATA_R_26, M_DQS_R3, M_DATA_R_25 → C324 DUMMY-SCD01U16V2KX

RN67 SRN56-1: M_DATA_R_14, M_DATA_R_15, M_DATA_R_21, M_DATA_R_20 → C351 SCD1U16V

RN71 SRN56-1: M_DATA_R_17, M_DATA_R_16, M_DATA_R_11, M_DATA_R_10 → C170 SCD1U16V

RN65 SRN56-1: M_SDM_R2, M_DATA_R_23, M_DATA_R_22, M_DATA_R_28 → C162 DUMMY-SCD01U16V2KX

RN25 SRN56-1: M_SDM_R3, M_DATA_R_29, M_DATA_R_30, M_DATA_R_31 → C363 SCD1U16V

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION

M_DATA[63..0] 8, M_DATA_R_[63..0] 11, M_DQS[7..0] 8, M_DQS_R[7..0] 11, M_SDM_[7..0] 8, M_SDM_R[7..0] 11

39 1D25V_S0 → 1D25V_S0

7,9,10,11,38,39,40,41 2D5V_S3 → 2D5V_S3

1D25V_S0

RN68 SRN56-1: M_A7, M_A5, M_A3, M_A1 → C178 DUMMY-SCD01U16V2KX; C369 SCD1U16V

10/11

RN18 SRN56-1: M_A9, M_A10, M_A11, M_A12 → C327 DUMMY-SCD01U16V2KX; C193 SCD1U16V

RN24 SRN56-1: M_A6, M_A8, M_A2, M_A4 → C325 DUMMY-SCD01U16V2KX; C364 SCD1U16V

RN9 SRN56-1: M_B_A10, M_B_BS0#, M_B_WE#, M_CS2_R# → C194 DUMMY-SCD01U16V2KX; C199 SCD1U16V

RN50 SRN56-1: M_B_A6, M_B_A4, M_B_A2, M_B_A0 → C361 SCD1U16V; C368 DUMMY-SCD01U16V2KX

1D25V_S0

Address / Command

RN23 SRN56-1: M_A_BS1#, M_A_RAS#, M_A_CAS#, M_CS1_R# → C191 SCD1U16V; C326 DUMMY-SCD01U16V2KX

RN51 SRN56-1: M_B_A11, M_B_A8 → C160 SCD1U16V; C353 DUMMY-SCD01U16V2KX

RN22 SRN56-1: M_B_BS1#, M_B_RAS#, M_B_CAS#, M_CS3_R# → C179 SCD1U16V; C350 DUMMY-SCD01U16V2KX

RN67 SRN56-1: M_A13, M_CS0_R#, M_A_WE#, M_A_BS0# → C370 SCD1U16V; C175 DUMMY-SCD01U16V2KX

RN10 SRN56-1: M_B_A12, M_B_A5, M_B_A3, M_B_A1 → C366 SCD1U16V; C184 DUMMY-SCD01U16V2KX

1D25V_S0

Control

M_CKE2_R#, M_CKE3_R# → R395 56R2J → C190 SCD1U16V

M_CKE1_R#, M_CKE0_R# → R420 56R2J → C352 SCD1U16V

RN19 SRN56-2-U2: M_B_A9, M_B_A7 → C360 SCD1U16V

M_B_A13 → R106 56R2J → C169 DUMMY-SCD01U16V2

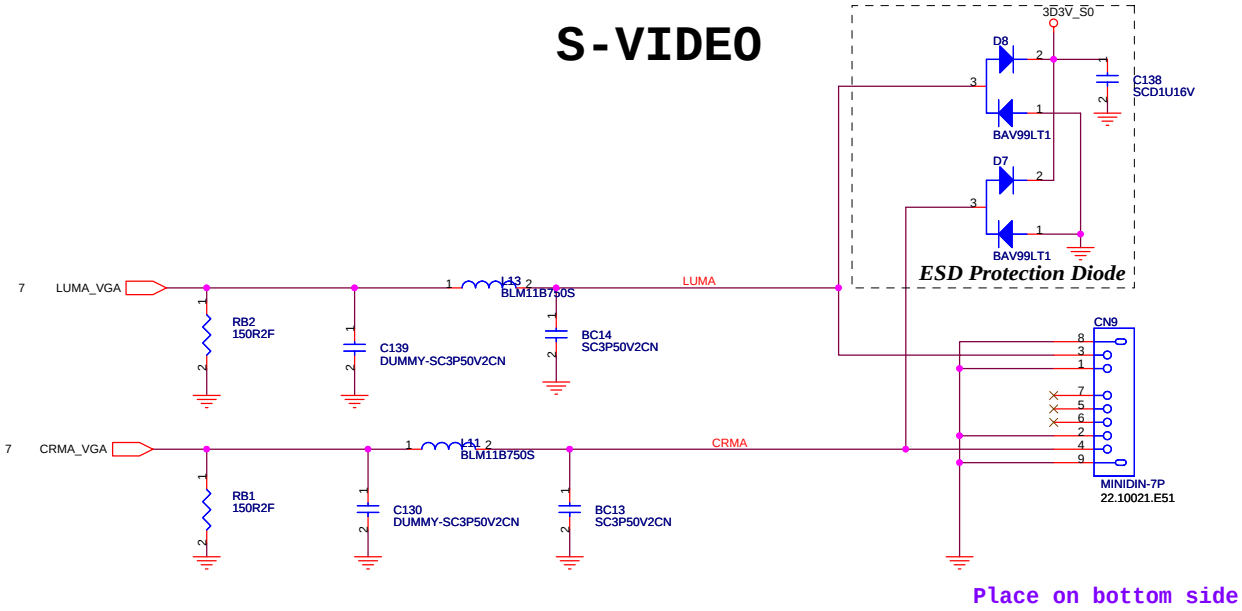
M_A0 → R119 56R2J → C201 SCD1U16V

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR Serial/Terminator Resistor***	
Size A3	Document Number: Leopard	Rev: -2
Date: Thursday, December 09, 2004	Sheet 12 of 41	

3D3V_S0

3,5,7,9,11,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0

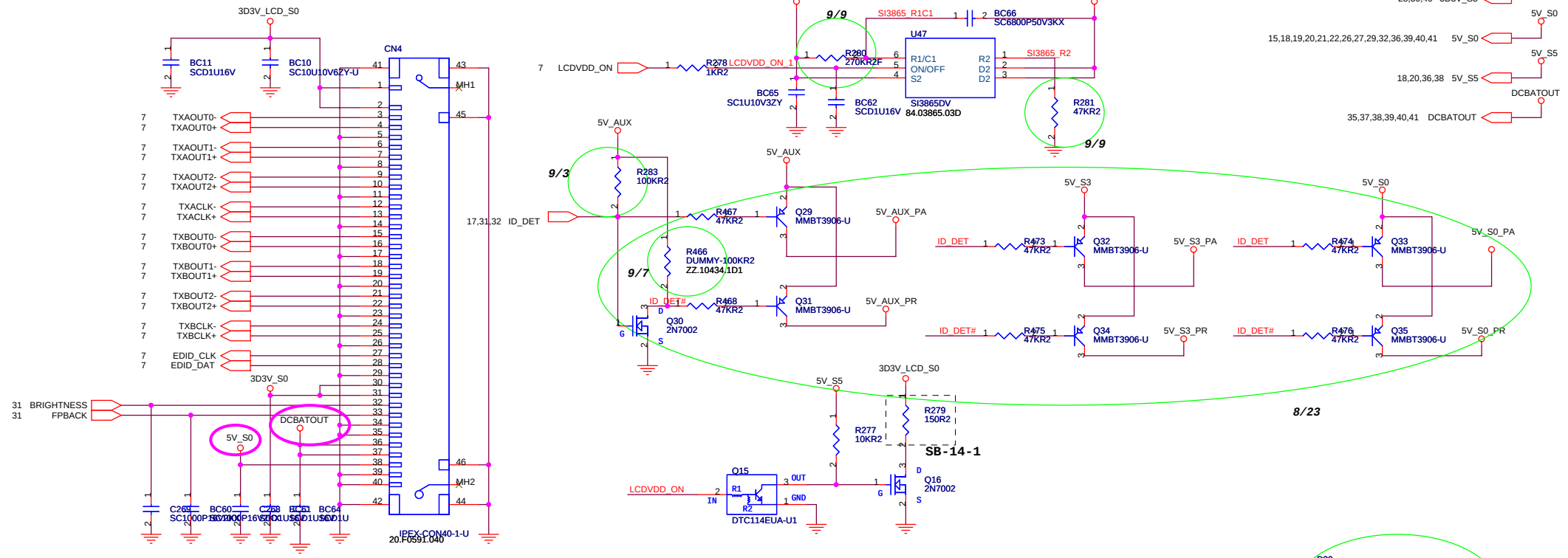
S-VIDEO

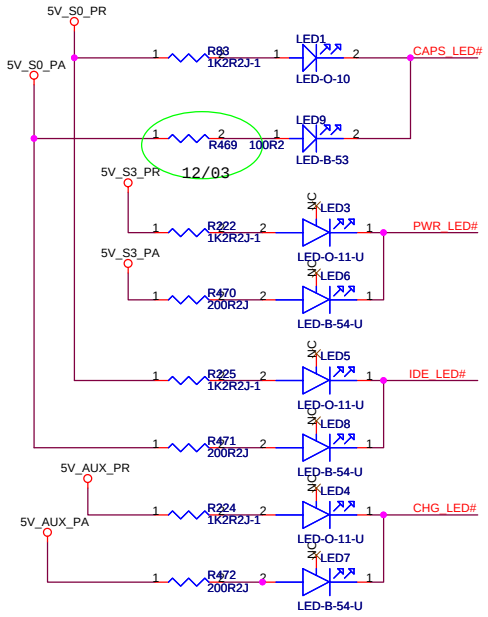


Place on bottom side

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***S-VIDEO***	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 13 of 41	

INVERTER/LCD

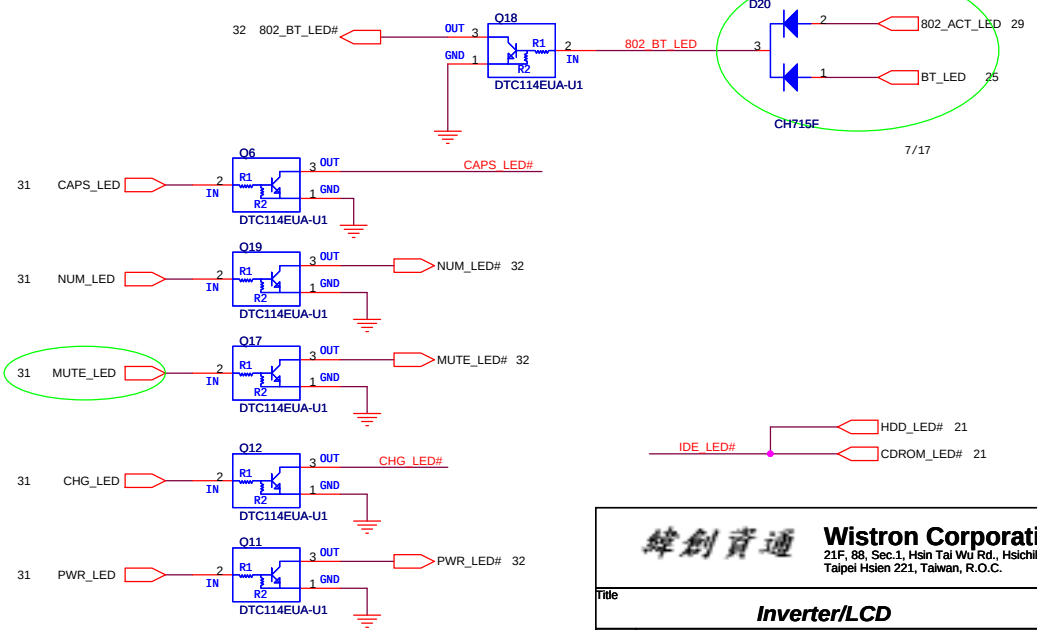




	PWR	CHR	HDD	IR	CAPS
PR Botton	Amber LED3	Amber LED4	Amber LED5	X	Amber LED1
PA Top	Blue LED6	Blue LED7	Blue LED8	X	Blue LED1

PA & PR diffent parts

	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED3	Dummy	83.00110.D70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	83.00110.E70	Dummy
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
R83	63.20134.1D1	63.10234.1D1
R222	63.20134.1D1	63.10234.1D1
R225	63.20134.1D1	63.10234.1D1
R224	63.20134.1D1	63.10234.1D1



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Taipei Hsien 221, Taiwan, R.O.C.

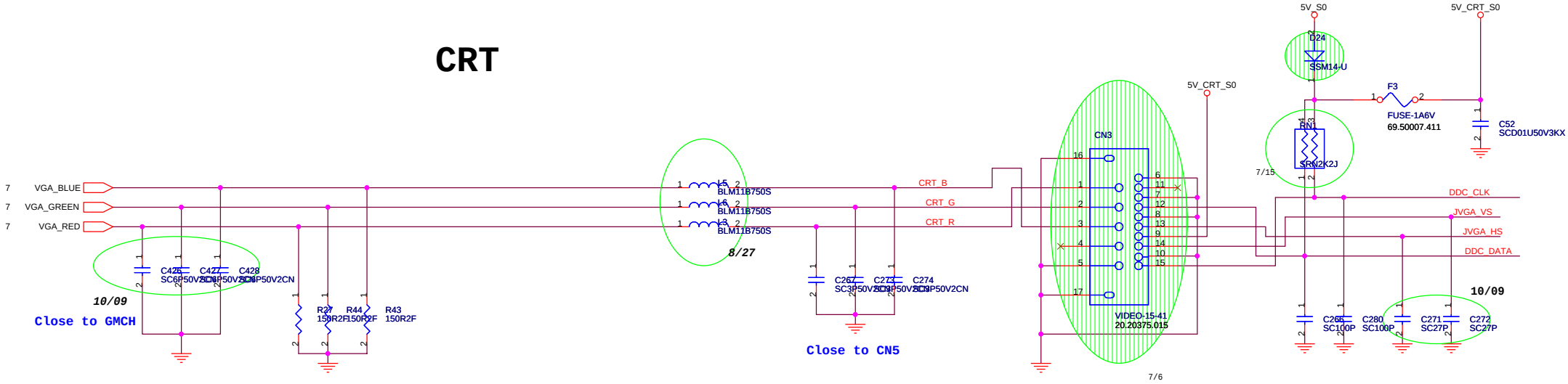
Title: *Inverter/LCD*

Size: A3 | Document Number: *Leopard* | Rev: -2

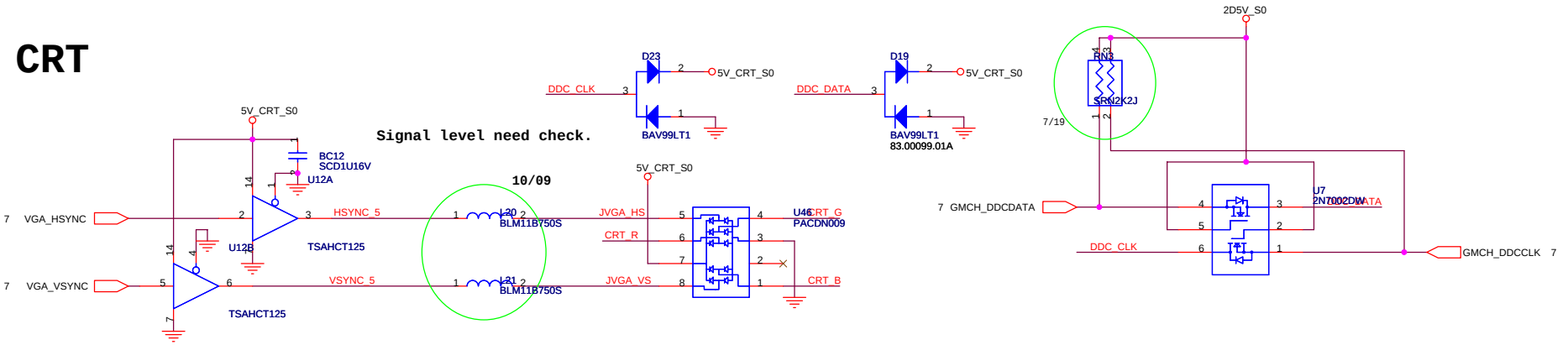
Date: Thursday, December 09, 2004 | Sheet 14 of 41

CRT CONN

CRT



CRT



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Title: CRT/ CIR		
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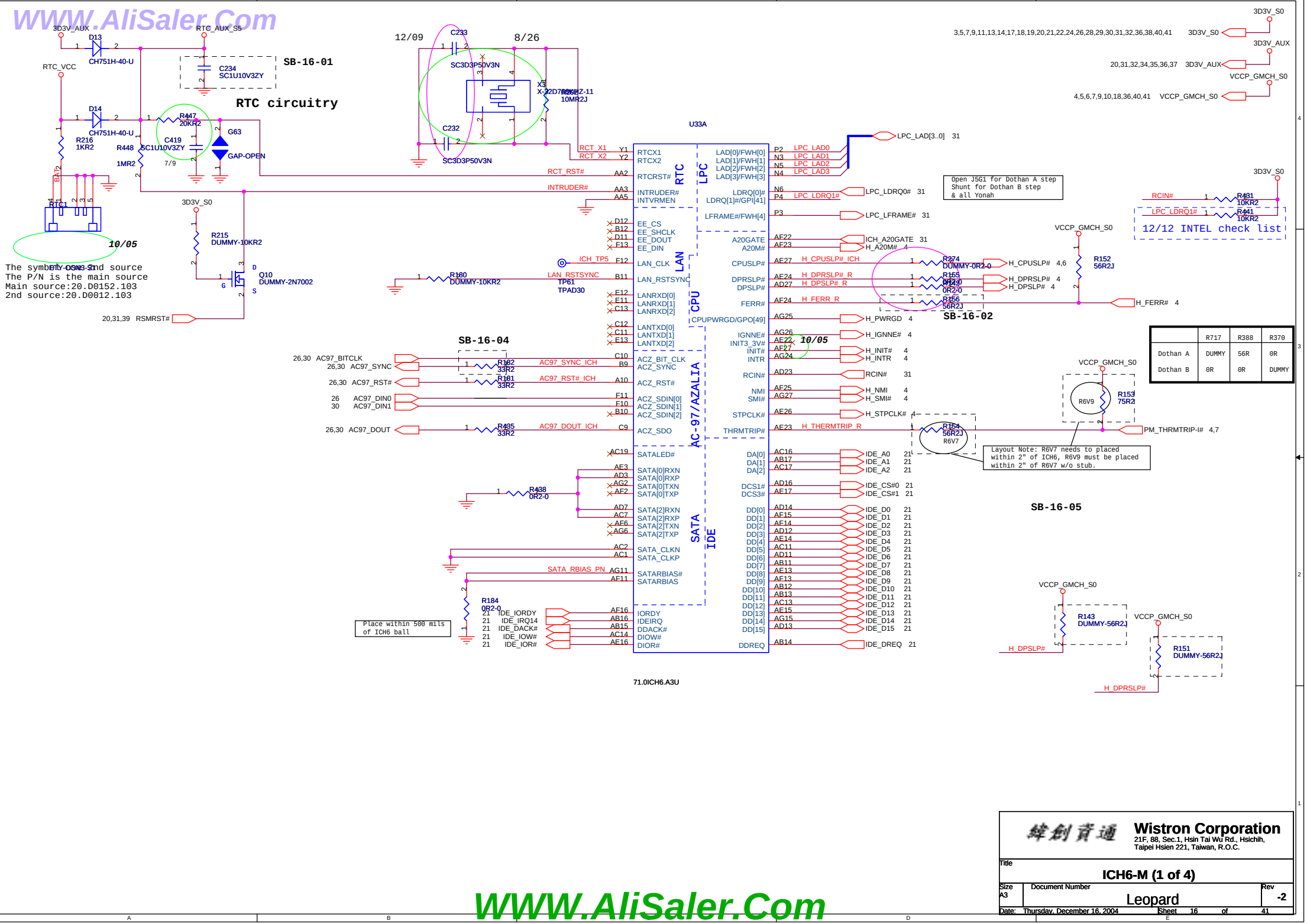

	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY

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ICH6 Pullups

Leopard Board Version Setting

Ver.	PCB_VER0	PCB_VER1
DB	0	0
SI	0	1
PV	1	0
MV	1	1

ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.

Place within 500 mils of ICH

Intel 22.6 ohm 1%

To avoide leakage current

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Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

U33E

1D5V_S0

TC9 DUMMY-ST220U10V2MX-1
C374 SCD1U10V2MX-1
C390 SCD1U10V2MX-1
C204 SCD1U10V2MX-1

PCIE

Layout Note:
IDE decoupling

3D3V_S0

C229 SC10U10V5ZY-L

9/3

Layout Note:
PCI decoupling

3D3V_S0

C213 SC10U10V5ZY-L

9/3

SATA

Place within 100 mils of ICH near pin AG5

Place within 100 mils of ICH near pin AG9

C408 DUMMY-SCD1U10V2MX-1
C411 DUMMY-SCD1U10V2MX-1
C222 DUMMY-SCD1U10V2MX-1
C410 DUMMY-SCD1U10V2MX-1
C223 DUMMY-SCD1U10V2MX-1
C409 DUMMY-SCD1U10V2MX-1

NO_STUFF

1D5V_S0
1D5V_GPLL_ICH_S0

G33 GAP-CLOSE-PWR

Place within 100 mils of ICH

C205 SC10U10V5ZY-L
C206 SCD01U16V2KX

9/3

3D3V_S0

C392 SCD1U10V2MX-1

1D5V_S0
1D5V_ICH_S0

G37 GAP-CLOSE-PWR

C420 DUMMY-SCD1U10V2MX-1

7/14

Place within 100 mils of ICH near E26, E27

Place within 100 mils of ICH pin AE1

Place within 100 mils of ICH pin AG10

3D3V_S0

C224 SCD1U10V2MX-1

10/13

ICH6_VCCLAN3D3

3D3V_S0

Intel dummy

Place within 100 mils of ICH pin A13

3D3V_S5

Place within 100 mils of ICH

C407 SCD1U10V2MX-1

71.0ICH6.A3U

CORE

1D5V_S0

C383 SCD1U10V2MX-1
C386 SCD1U10V2MX-1
C389 SCD1U10V2MX-1
C394 SCD1U10V2MX-1
C391 SCD1U10V2MX-1

Layout Note:
Place near AA19

C404 NO_STUFF
C405 NO_STUFF
C388 NO_STUFF
C387 NO_STUFF
C402 NO_STUFF
C225 NO_STUFF

SCD1U10V6ZY-U

IDE

Place within 100 mils of ICH pin AG13, AG16

3D3V_S0

C217 SCD1U10V2MX-1
C214 SCD1U10V2MX-1

Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1

PCI

3D3V_S0

C401 SCD1U10V2MX-1
C230 SCD1U10V2MX-1
C231 SCD1U10V2MX-1

1D5V_ICH_S5

1D5V_ICH_S5
1D5V_S5

C403 SCD1U10V2MX-1
C406 SCD1U10V2MX-1

Layout Note:
Place near U7

USB CORE

1D5V_ICH_S5

1D5V_S0

C384 SCD1U10V2MX-1

ICH_VCC1_5

C372 SCD1U10V2MX-1
C371 SCD1U10V2MX-1

Place both within 100 mils of ICH near D27

USB

PCI/IDE REF

V2D5S_PCI_IDE

2D5V_S0

G62 GAP-CLOSE-PWR

C393 SCD1U10V2MX-1

Place near AB18

V5REF_S0
V5REF_S5

1D5V_ICH_S0

Place within 100 mils of ICH

C209 SCD01U16V2KX

3D3V_S5

Place within 100 mils of ICH

C208 SCD1U10V2MX-1

10/13

ICH6_VCCLAN1D5V

1D5V_S0

Place within 100 mils of ICH pin G10

VCCP_GMCH_S0

C375 SCD1U10V2MX-1

Layout Note:
Place near AG23

RTC_AUX_S5

Layout Note:
Place near AB3

C417 DUMMY-SCD1U10V2MX-1
C418 DUMMY-SCD1U10V2MX-1

3D3V_S5

C382 SCD1U10V2MX-1
C385 SCD1U10V2MX-1
C381 SCD1U10V2MX-1
C211 SCD1U10V2MX-1

NO_STUFF

Place within 100 mils of ICH pin A17

3,5,7,9,11,13,14,16,17,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 → 3D3V_S0
17,19,24,29,31,35,37,39,40 3D3V_S5 → 3D3V_S5
14,15,19,20,21,22,26,27,29,32,36,39,40,41 5V_S0 → 5V_S0
5,7,9,17,38,39,41 1D5V_S0 → 1D5V_S0
39 1D5V_S5 → 1D5V_S5
7,9,15,40 2D5V_S0 → 2D5V_S0
4,5,6,7,9,10,16,36,40,41 VCCP_GMCH_S0 → VCCP_GMCH_S0

ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

5V_S0

D11 CH751H-40-U

3D3V_S0

D10 CH751H-40-U
R178 100R2 Intel 10 ohm 7/12

V5REF_S0

C221 SCD1U16V
C220 SC1U10V3ZY

SB-17-01

3D3V_S5
5V_S5

D31 CH751H-40-U
R423 10R2 Intel 10 ohm

V5REF_S5

C356 SCD1U16V
C373 SC1U10V3ZY

SB-17-01

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3D3V_S0
3,5,7,9,11,13,14,16,17,18,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0
3D3V_S5
17,18,24,29,31,35,37,39,40 3D3V_S5
5V_S0
14,15,18,20,21,22,26,27,29,32,36,39,40,41 5V_S0

U33D

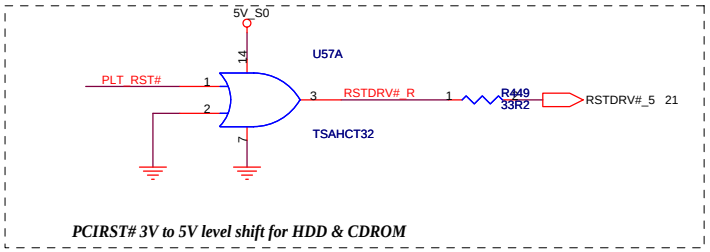
VSS

E27 Y6 Y27 Y26 Y23 W7 W25 W24 W23 W1 V4 V27 V26 V23 U25 U24 U23 U15 U13 T7 T27 T26 T23 T16 T15 T14 T13 T12 T1 R4 R25 R24 R23 R17 R16 R15 R14 R13 R12 R11 P22 P16 P15 P14 P13 P12 N7 N17 N16 N15 N14 N13 N12 N11 N1 M4 M27 M26 M23 M16 M15 M14 M13 M12 L25 L24 L23 L15 L13 K7 K27 K26 K23 K1 J4 J25 J24 J23 H27 H26 H23 G9 G7 G21 G12 G1

F4 F22 F19 F17 F25 E19 E18 E15 E14 D7 D22 D20 D18 D14 D13 D10 D1 C4 C22 C20 C18 C14 B25 B24 B23 B21 B19 B15 B13 AG7 AG3 AG22 AG20 AG17 AG14 AG12 AG1 AE7 AE3 AE26 AE12 AE10 AE1 AE7 AE6 AE25 AE21 AE2 AE12 AE11 AE10 AD6 AD24 AD2 AD18 AD15 AD10 AD1 AC6 AC3 AC26 AC24 AC23 AC22 AC12 AC10 AB9 AB7 AB2 AB19 AB10 AB1 AA4 AA16 AA13 AA11 A9 A7 A4 A26 A23 A21 A19 A15 A12 A1

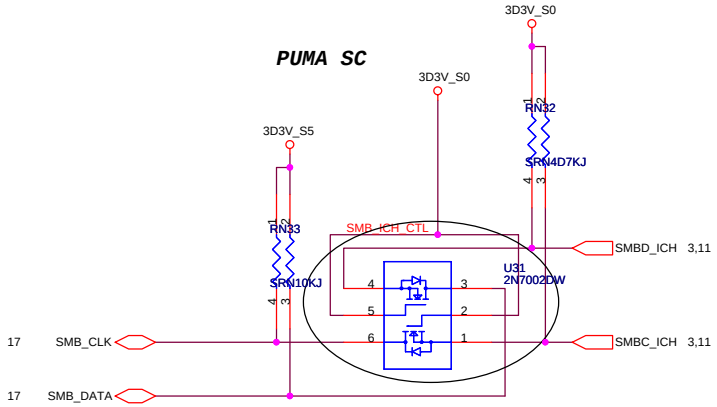
71.0ICH6.A3U

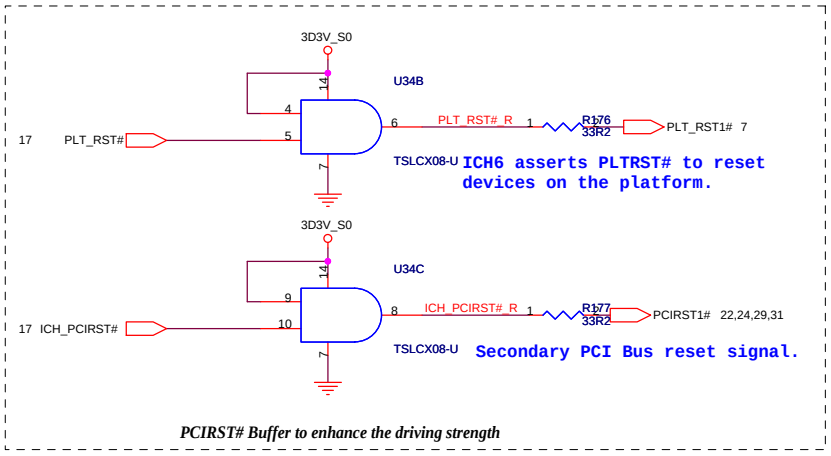
Cougar
SC



PCIRST# 3V to 5V level shift for HDD & CDROM

SMBUS(ICH6 ---> SODIMM,CLKGEN)





PCIRST# Buffer to enhance the driving strength

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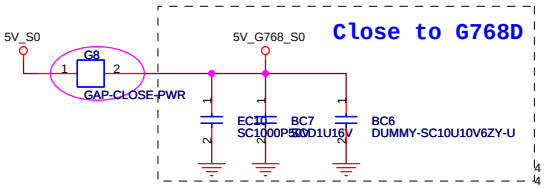
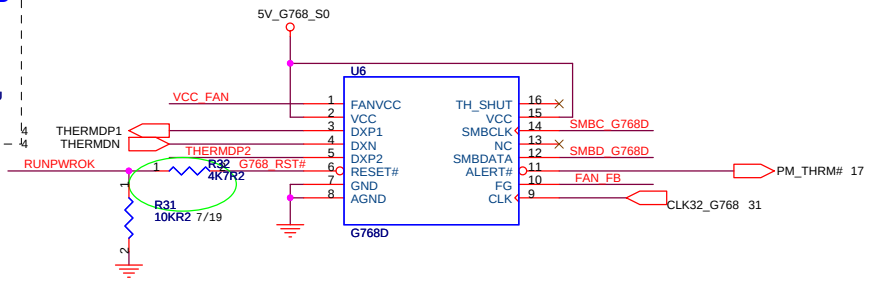
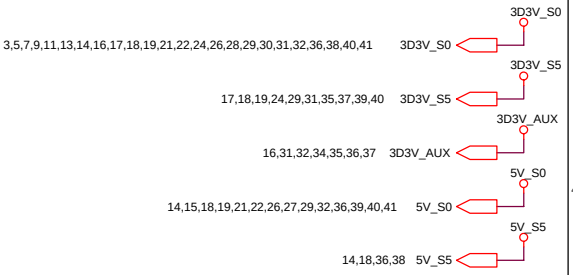
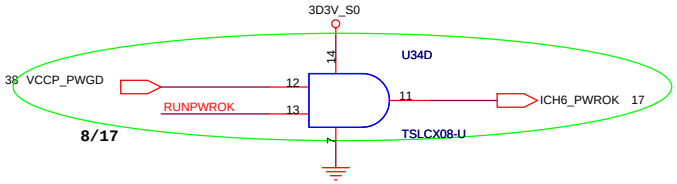


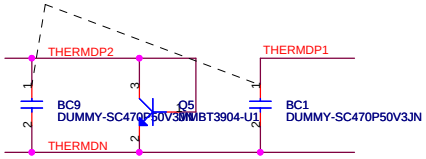
Reserve for G768B
works at High
Speed

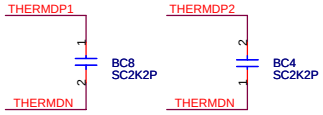






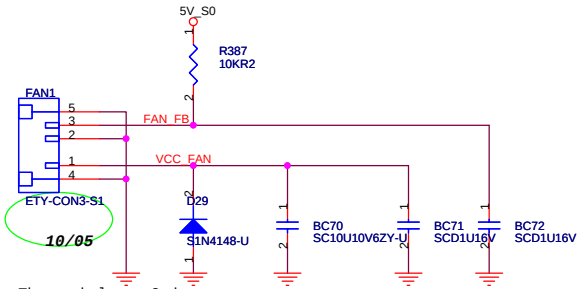
Put these two Caps near the thermal diode.





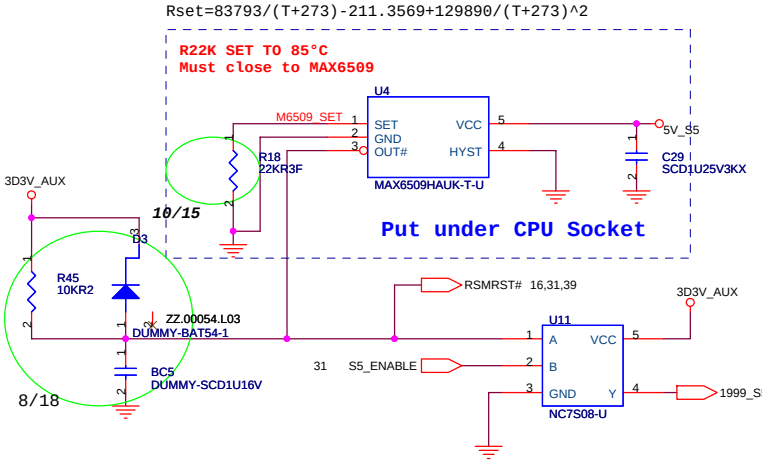
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

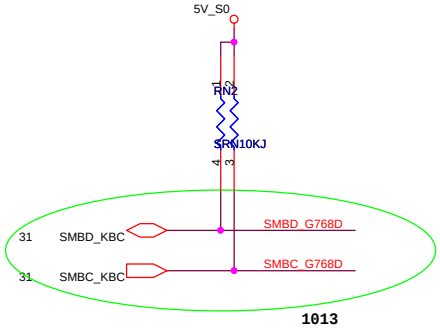
180 ms after VCC_G768 > 4.38v, p2, 7



The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103

Rset=83793/(T+273)-211.3569+129890/(T+273)^2





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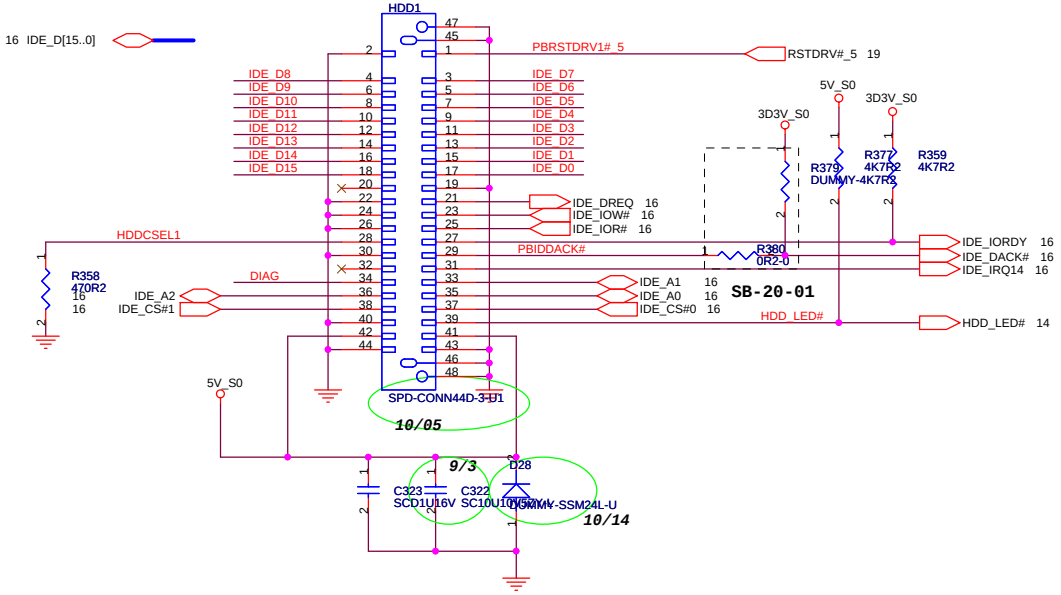
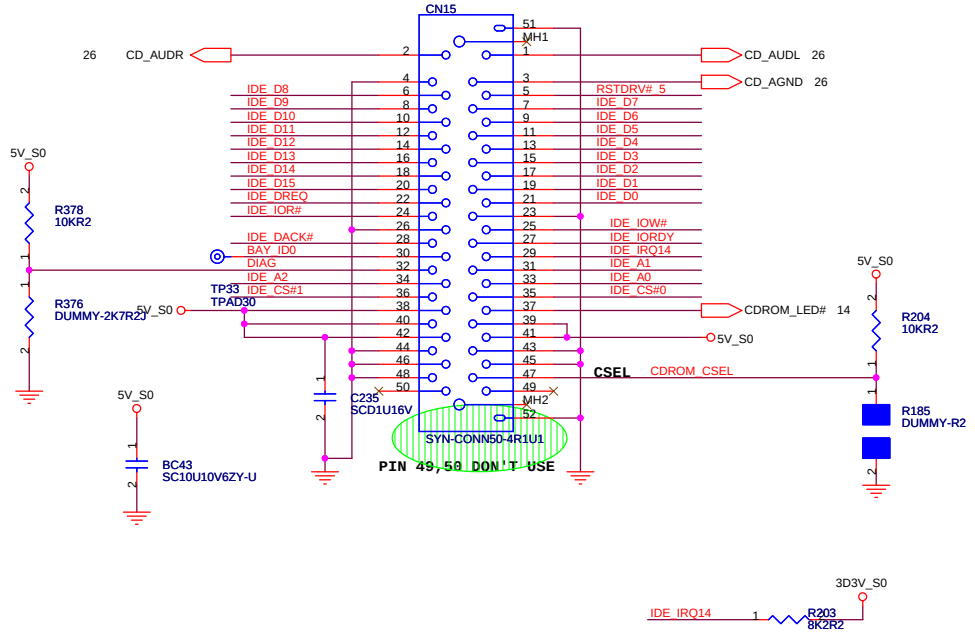
HDD Connector



3,5,7,9,11,13,14,16,17,18,19,20,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 — 3D3V_S0
24,41 3D3V_LAN_S5 — 3D3V_LAN_S5
14,15,18,19,20,22,26,27,29,32,36,39,40,41 5V_S0 — 5V_S0
5,7,9,17,18,38,39,41 1D5V_S0 — 1D5V_S0

CDROM



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Title	HDD / CDROM
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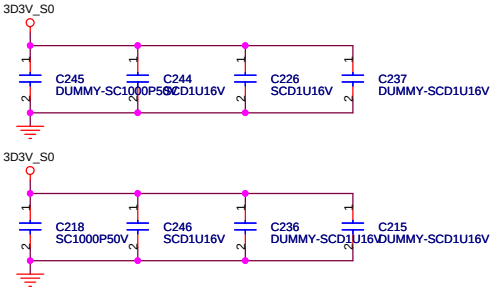
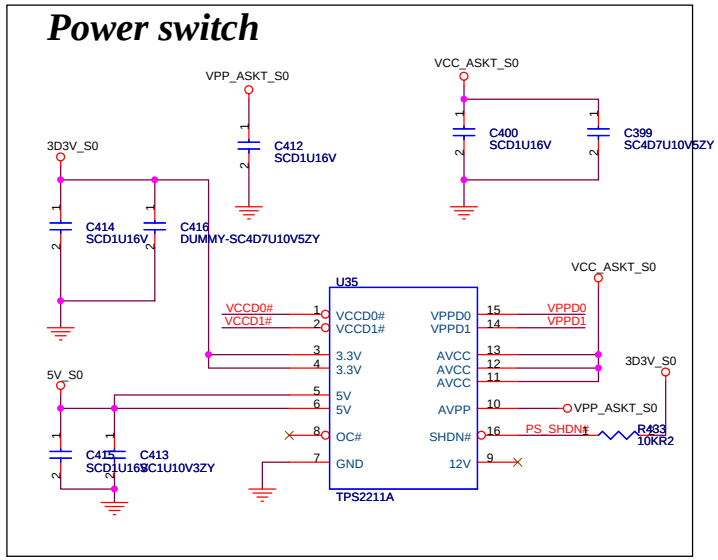
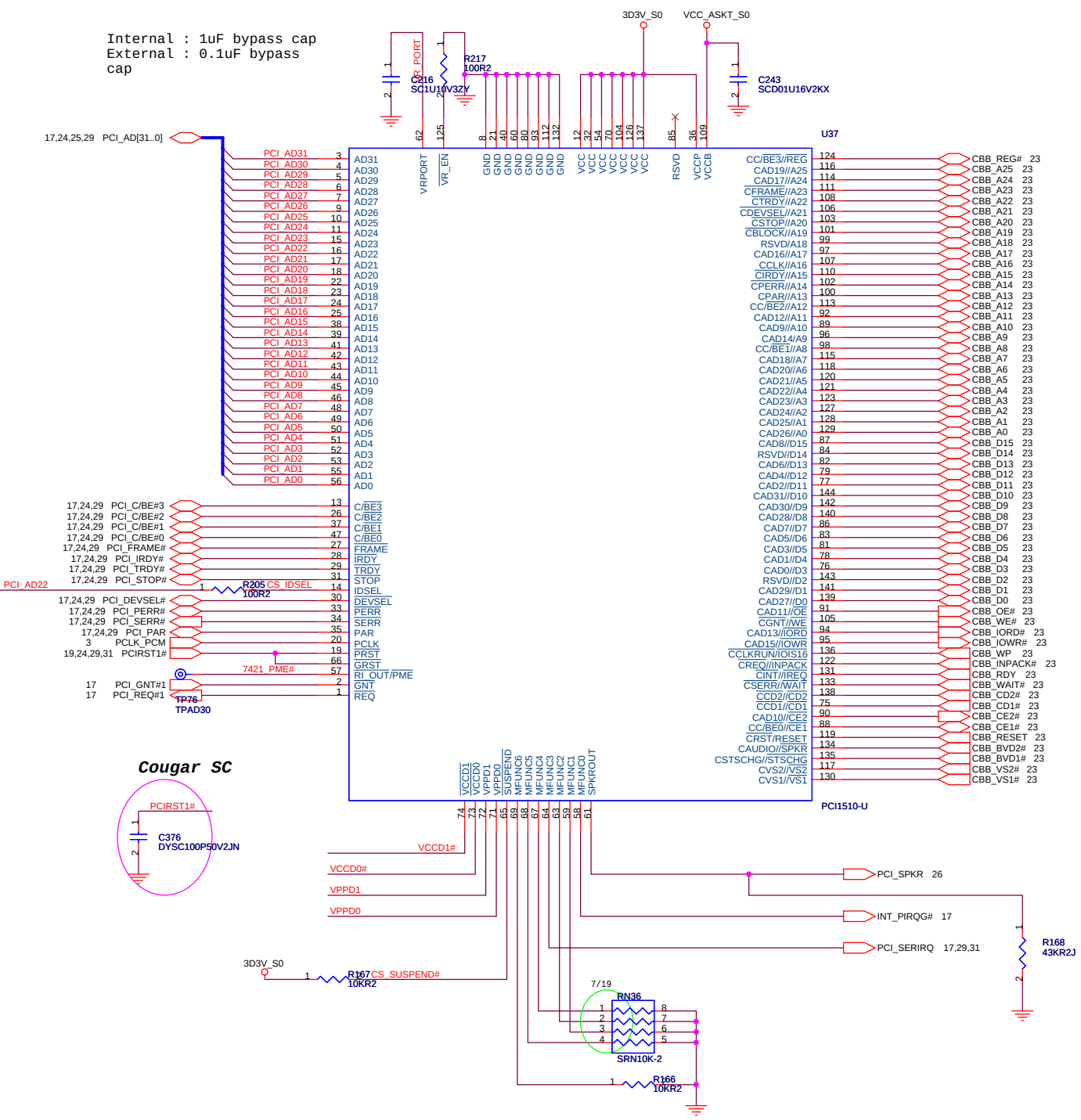
Internal : 1uF bypass cap
External : 0.1uF bypass cap

3,5,7,9,11,13,14,16,17,18,19,20,21,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0

Bypass/Decupoling Capacitors
Should be places as close to
PCI1510 as possible







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Size: A3
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PCMCIA Socket

3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0

3D3V_S0

DCBATOUT

14,35,37,38,39,40,41 DCBATOUT

CBUS1

CARDBUS68P-9
62.10024.491

Cardbus I/F

CBB_D[0..15] 22
CBB_A[0..25] 22

CBB_IORD# 22
CBB_IOWR# 22
CBB_OE# 22
CBB_WE# 22
CBB_REG# 22
CBB_RDY 22
CBB_WP 22
CBB_RESET 22
CBB_WAIT# 22
CBB_INPACK# 22

CBB_CE1# 22
CBB_CE2# 22
CBB_BVD1# 22
CBB_BVD2# 22
CBB_CD1# 22
CBB_CD2# 22
CBB_VS1# 22
CBB_VS2# 22

VCC_ASKT_S0

10/06

C398 SC22U10V6ZY-U
C396 SC1000P50V
C395 SCD1U16V

VPP_ASKT_S0

C397 SCD1U16V

CBB_A16

R175 DUMMY-R2

Place close to pin 19.

C219 DUMMY-C2

Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

VCC_ASKT_S0

R187 DUMMY-R2
47K

CBB_RESET

C227 SCD01U16V3KX

SKT1

CARDBUS-SKT45-U1

9/8

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Title: PCMCIA SLOT

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Close to RTL8100C
Pin121,Pin122

LAN_X1
LAN_X2
RS2 DUMMY-R2
X4 XTAL-25MHZ-43
C144 SC12P50V2JN
C143 SC12P50V2JN
8/26

3D3V_LAN_S5
R96 3K6R3
U29
EECS_3
EESK
EEDI
EEDO
CS SK DI DO VCC DC ORG GND
M93C46-W-3
C167 SCD1U16V

PCI_C/BE#[0..3] 17,22,29
PCI_AD[0..31] 17,22,25,29

AVDD25
VDD25
R85 0R3-U
C134 SCD1U16V

R93 5K6R3F
HM1-SB
Remove LED function
3D3V_LAN_S5
TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30
LAN_X2 LAN_X1 LAN_LED0 LAN_LED1 LAN_LED2 EESK EEDI EEDO EECS_3 PCI_AD0 PCI_AD1

C142 C147 C149 C140 C150 C152 C132 SCD1U16V

TX+ TX- RX+ RX-
R92 49D9R2F R91 49D9R2F R90 49D9R2F R89 49D9R2F
C137 SCD1U16V C136 SCD1U16V
7/8

U28
RTL8100CL-U
RSET XTAL2 XTAL1 LED0 LED1 LED2 EESK EEDI EEDO VDD33 EECS LANWAKE PCIAD0 PCIAD1

25 TX+
25 TX-
AVDD33
25 RX+
25 RX-
AVDD33
CTRL25
AVDD25
AVDD33
ISOLATE
17,29 INT_PIRQE#
3D3V_LAN_S5
19,22,29,31 PCIRST1#
3 PCLK_LAN
17 PCI_GNT#2
17 PCI_REQ#2
17,25,29 ICH_PME#
VDD25
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28

1 GND
2 TX+
3 TX-
4 AVDD33
5 GND
6 RX+
7 RX-
8 AVDD33
9 CTRL25
10 NC
11 NC
12 NC
13 AVDD25
14 NC
15 NC
16 NC
17 NC
18 GND
19 NC
20 NC
21 AVDD33
22 GND
23 NC
24 ISOLATEB
25 NC
26 INTAB
27 VDD33
28 PCIRSTB
29 PCICLK
30 GNTB
31 REQB
32 PMEB
33 VDD25
34 PCIAD31
35 PCIAD30
36 GND
37 PCIAD29
38 PCIAD28
39 GND

40 PCIAD27
41 PCIAD26
42 PCIAD25
43 PCIAD24
44 CBEB3
45 NC
46 IDSEL
47 PCIAD23
48 NC
49 PCIAD22
50 PCIAD21
51 GND
52 GND
53 PCIAD20
54 VDD25
55 PCIAD19
56 VDD33
57 PCIAD18
58 PCIAD17
59 PCIAD16
60 CBEB2
61 FRAMEB
62 NC
63 IRDYB
64 NC

65 CLKRUNB
66 GND
67 TRDYB
68 DEVSELB
69 STOPB
70 PERRB
71 VDD33
72 NC
73 NC
74 SERRB
75 PAR
76 CBEB1
77 VDD25
78 PCIAD15
79 GND
80 GND
81 GND
82 PCIAD14
83 PCIAD13
84 VDD33
85 PCIAD12
86 PCIAD11
87 PCIAD10
88 NC
89 PCIAD9
90 PCIAD8
91 GND
92 PCI_C/BE#0
93 PCIAD7
94 VDD33
95 PCIAD6
96 PCIAD5
97 PCIAD4
98 PCIAD3
99 VDD25
100 GND
101 PCIAD2
102 GND

PCI_AD2
VDD25
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_C/BE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
VDD25
PCI_C/BE#1
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PM_CLKRUN#

PCI_PAR 17,22,29
PCI_SERR# 17,22,29
PCI_PERR# 17,22,29
PCI_STOP# 17,22,29
PCI_DEVSEL# 17,22,29
PCI_TRDY# 17,22,29
PM_CLKRUN# 17,29,31

PCI_IRDY# 17,22,29
PCI_FRAME# 17,22,29

SB-24-01

3D3V_S0
R87 1KR2
ISOLATE
Cougar SC
R86 DUMMY-15KR2 ZZ.15334.1D1

3D3V_LAN_S5
R94 100R2
PCI_AD23

CTRL25
R88 0R2-0
LAN_PWR_CTL
Q8 BCP69T1-U
G30 GAP-CLOSE-PWR
C128 SC22U10V6ZY-U
10/06
VDD25
C131 C141 C148 C151 SCD1U16V

3D3V_LAN_S5
L12 BLM11A601S
AVDD33
C135 C133 SCD1U16V
7/16

3D3V_S5
3D3V_LAN_S5
G31 GAP-CLOSE-PWR

3,5,7,9,11,13,14,16,17,18,19,20,21,22,26,28,29,30,31,32,36,38,40,41 3D3V_S0
17,18,19,29,31,35,37,39,40 3D3V_S5
41 3D3V_LAN_S5

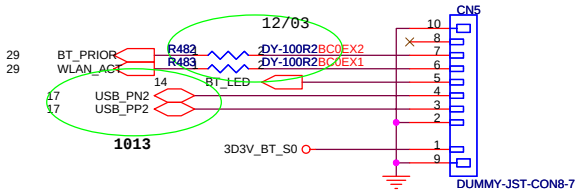
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8100C
Size: A3
Document Number: Leopard
Rev: -2
Date: Thursday, December 09, 2004
Sheet 24 of 41

Cougar SC

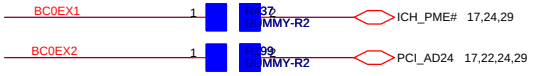
Blue thumb

Place on bottom side
From NEW!



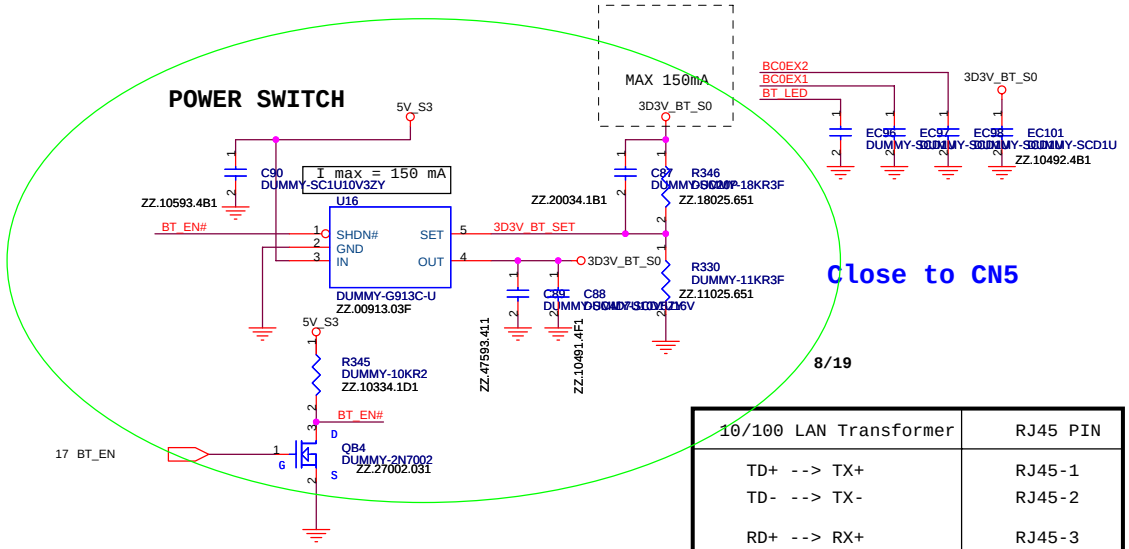
BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.

3D3V_LAN_S5
24,41 3D3V_LAN_S5



Please close to ICH6

POWER SWITCH

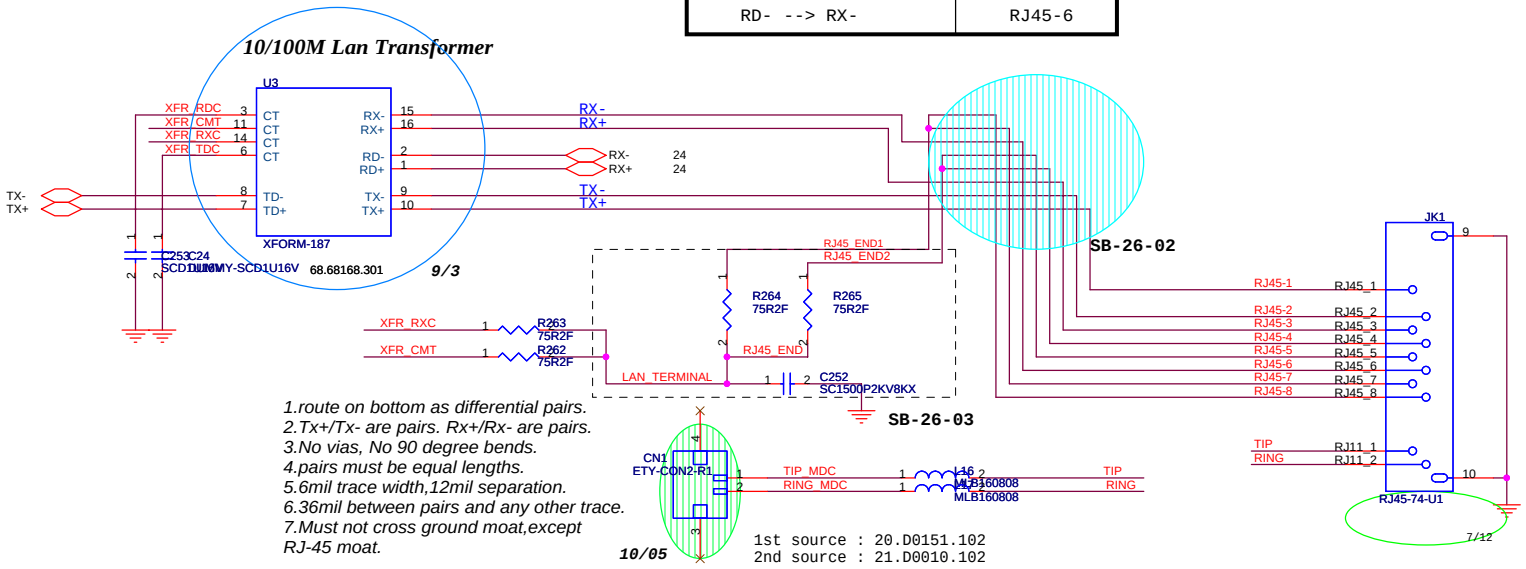


Close to CN5

8/19

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

10/05

1st source : 20.D0151.102
2nd source : 21.D0010.102

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN / 1394 Connector

Size: A3 | Document Number: Leopard | Rev: -2

Date: Thursday, December 09, 2004 | Sheet 25 of 41

3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,28,29,30,31,32,36,38,40,41 3D3V_S0

14,15,18,19,20,21,22,27,29,32,36,39,40,41 5V_S0

3D3V_S0

BC84 SCD1U16V BC83 SCD1U16V

BC82 SC1U10V3ZY BC81 SCD1U16V

AUD_AGND

5V_AUDIO_S0

BC78 SCD1U16V BC46 SCD1U16V BC49 SCD1U16V BC48 SCD1U16V

AUD_AGND

C242 SC270P50V3JN

C240 SC270P50V3JN

C239 SC270P50V3JN

C241 SC270P50V3JN

AUD_AGND

U39

CODECVREF VREFOUT ADAF1 ADAF2 ADAF3 ADAF4

AVDD1 AVDD2 AVDD3 AVDD4 DVDD1 DVDD2 VREF VREFOUT AFILT1 AFILT2 AFILT3 AFILT4

EXT_MIC_1 BC36 AUD_MICIN1

EXT_MIC_2 BC37 AUD_MICIN2 SC1U10V3ZY

MIC1 MIC2 LINE_IN_L LINE_OUT_L LINE_IN_R LINE_OUT_R MONO_OUT PHONE_IN CD_L CD_R CD_GND_REF HP_OUT_L HP_OUT_R AUX_L AUX_R

JS0 JS1 EAPD XTL_IN XTL_OUT SDATA_IN SDATA_OUT BIT_CLK SYNC RESET# SPDIF

AVSS1 AVSS2 AVSS3 AVSS4 DVSS1 DVSS2 ID1# ID0# NC NC

AD1981B-AS

AD1981_JS0 R439 2K2R2 83.22234.1D1

EARPHONE 27,28

EAPD 27,31

CLK_CODEC 3 R209 0R2-0

XTALOUT_CODEC

AC97_DIN0_CODEC R197 22R2 BC42 DUMMY-C2 AC97_DIN0 16 AC97_DOUT 16,30

AC97_CBITCLK R198 33R2 AC97_BITCLK 16,30 AC97_SYNC 16,30 AC97_RST# 16,30

X2 DY-X-24D576MHZ-3-U1

BC50 DUMMY-SC22P BC51 DUMMY-SC22P

R210 DUMMY-R2 XTALOUT_CODEC BC52 DUMMY-C2

SB-27-01

27 AUD_LOL 27 AUD_LOR

30 AUD_MDC_OUT 30 AUD_PHONE

BC47 SCD1U16V AUD_MDC_CODEC BC41 SCD1U16V AUD_PHONE_CODEC

21 CD_AUDL R195 22R2 CDAUDL BC40 SC1U25V5ZY CDAUD_L

21 CD_AUDR R192 22R2 CDAUDR BC38 SC1U25V5ZY CDAUD_R

21 CD_AGND R193 22R2 CDAGND BC39 SC1U25V5ZY CDAUD_GND

R194 DUMMY-150R2J R191 DUMMY-150R2J R196 DUMMY-150R2J

SB-27-03

AUD_AGND

28 HP_OUT_L 28 HP_OUT_R

SB-27-02

5V_AUDIO_S0 U59 SHDN# SET GND IN OUT MAX8863-S

5V_S0 BC87 SC1U10V3ZY

R451 28K7R3F EC145 SCD1U16V

BC86 SC22P 5VA_SET

R452 10KR3F

BC85 SC10U10V6ZY-U

For High limit --> R45

AUD_AGND

UNDER CODEC CUT MOAT

2/2 HM1-SB
ADI suggest

VREFOUT

BC34 DUMMY-SC1U10V3ZY R190 3KR2F

28 EXT_MIC_2

7/15

BC32 SC1000P16V2KX

AUD_AGND

CLOSE TO CODEC

MIC2 PREAMP

VREFOUT

BC35 DUMMY-SC1U10V3ZY R189 3KR2F

28 EXT_MIC_1

7/15

BC33 SC1000P16V2KX

AUD_AGND

CLOSE TO CODEC

MIC1 PREAMP

G32 G67 G65 G36 G66 G35 G39 G38 GAP-CLOSE

AUD_AGND

SB-27-02

SB-27-04

5V_AUDIO_S0 U38A TSAHCT86

22 PCI_SPKR 17 ICH_SPKR

AUD_BEEP1

AUD_AGND

5V_AUDIO_S0 U38C TSAHCT86

31 KBC_BEEP U39_PL

AUD_BEEP2

R219 10KR2

AUD_AGND

5V_AUDIO_S0 U38B TSAHCT86

AUD_SYS_BEEP R206 10KR2 AUD_BEEP C238 SCD1U16V AUD_PC_BEEP

C247 SCD1U16V R218 10KR2

AUD_AGND

PUMA SC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

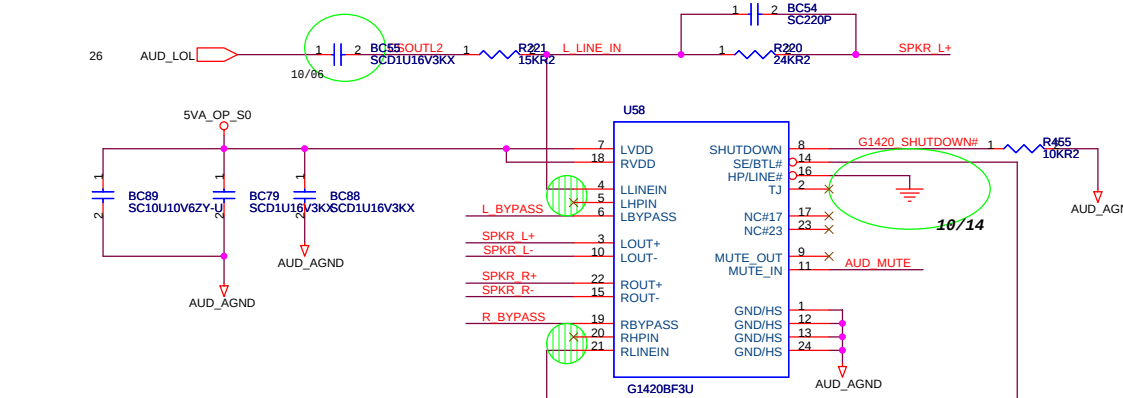
Title: AUDIO CODEC AD1981B

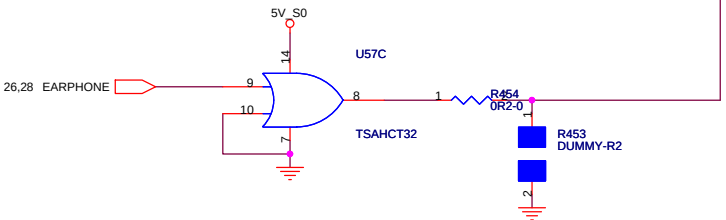
Size: A3 | Document Number: Leopard | Rev: -2

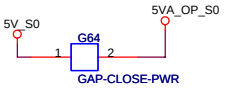
Date: Thursday, December 09, 2004 | Sheet 26 of 41

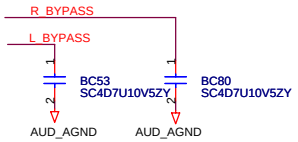
5V_S0

14,15,18,19,20,21,22,26,29,32,36,39,40,41 5V_S0

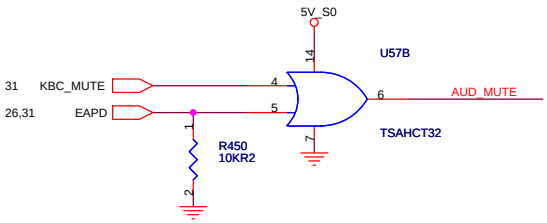


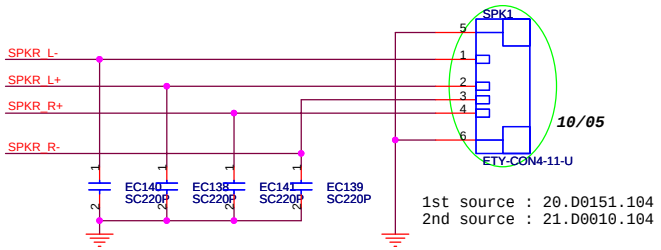






Speaker





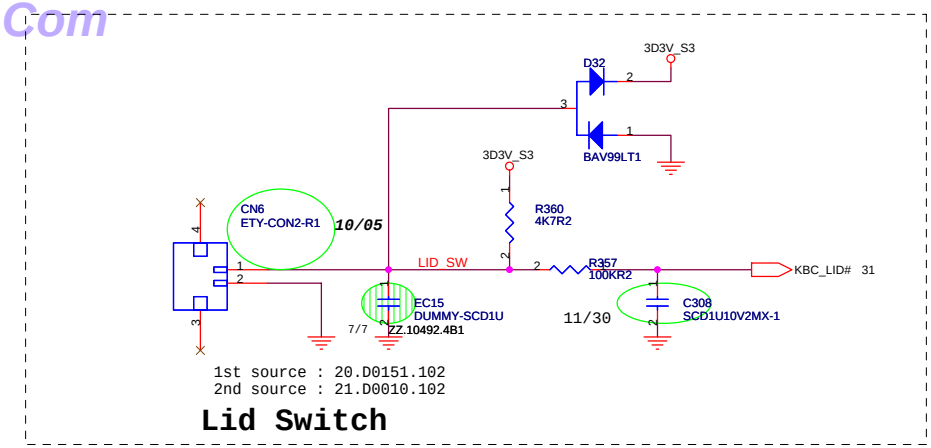
1st source : 20.D0151.104
2nd source : 21.D0010.104

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO

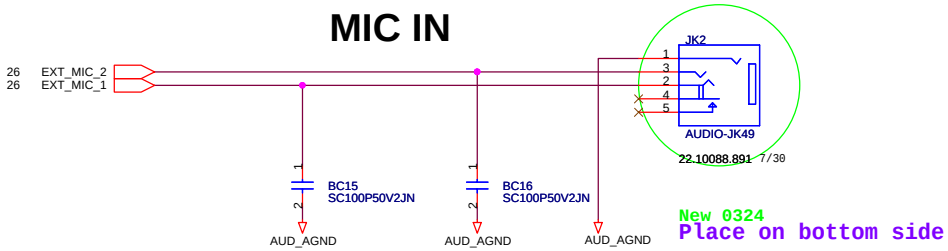
Size: A3 | Document Number: Leopard | Rev: -2

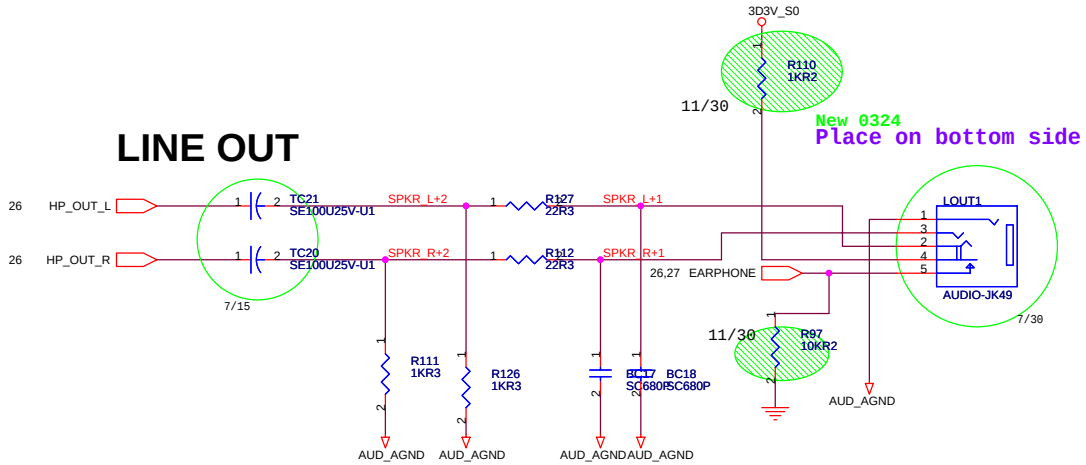
Date: Thursday, December 09, 2004 | Sheet 27 of 41



3D3V_S0

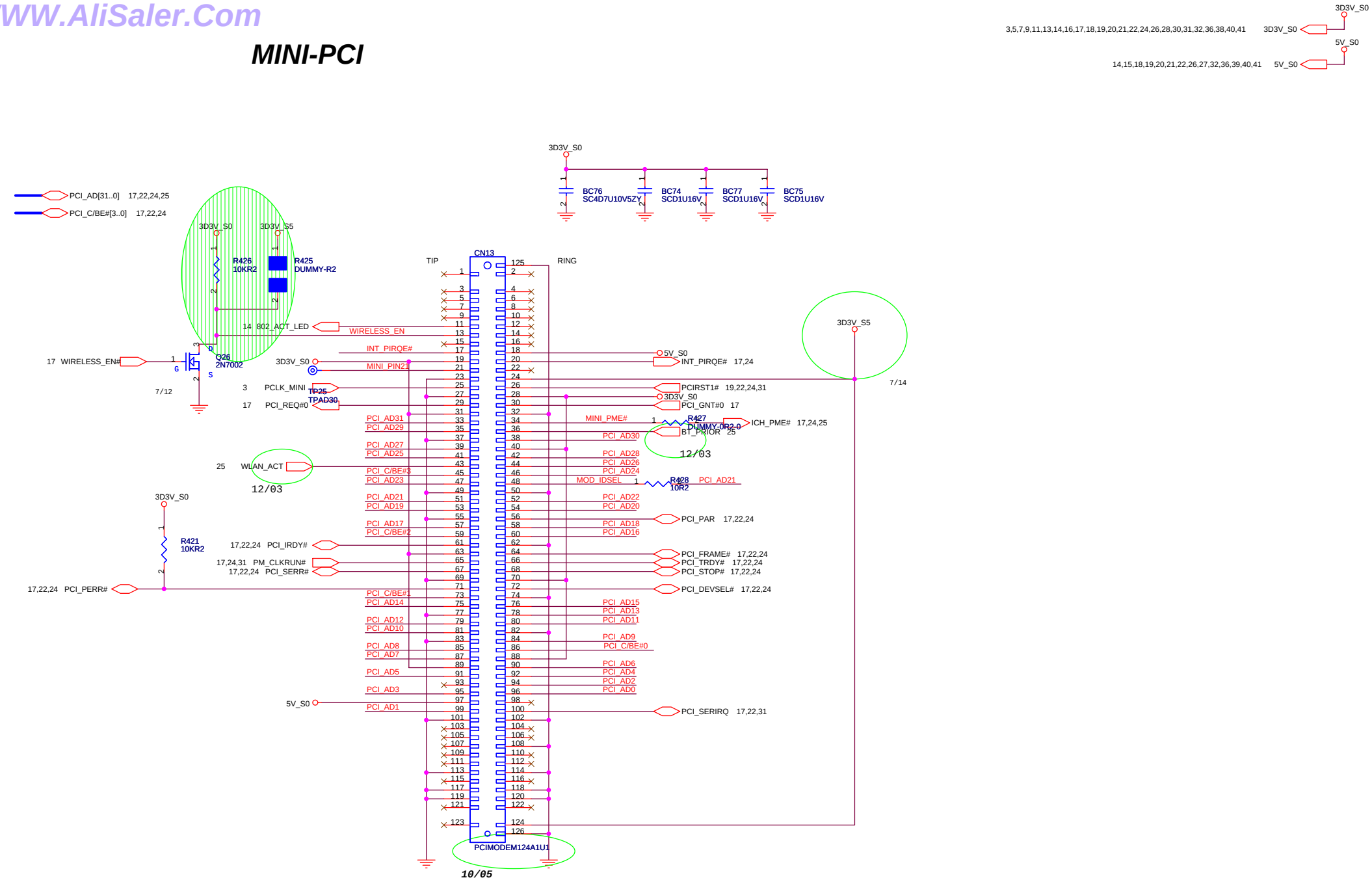
3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,29,30,31,32,36,38,40,41 3D3V_S0





緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO CONN/LID switch	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 28 of 41	

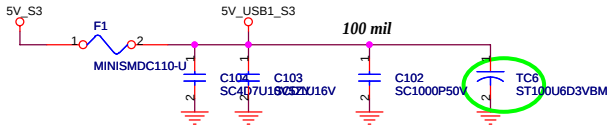
MINI-PCI

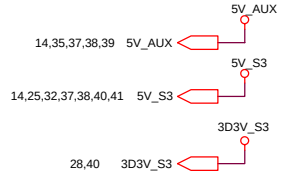


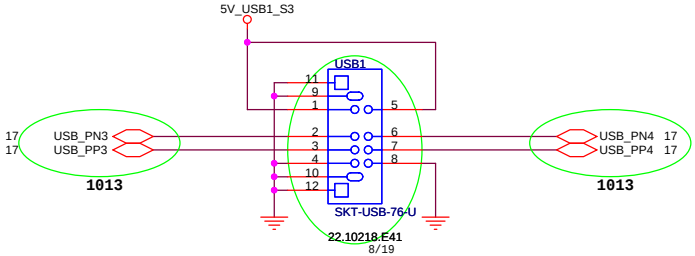
The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **MINI-PCI**		
Size: A3	Document Number: Leopard	Rev: -2
Date: Thursday, December 09, 2004	Sheet 29 of 41	

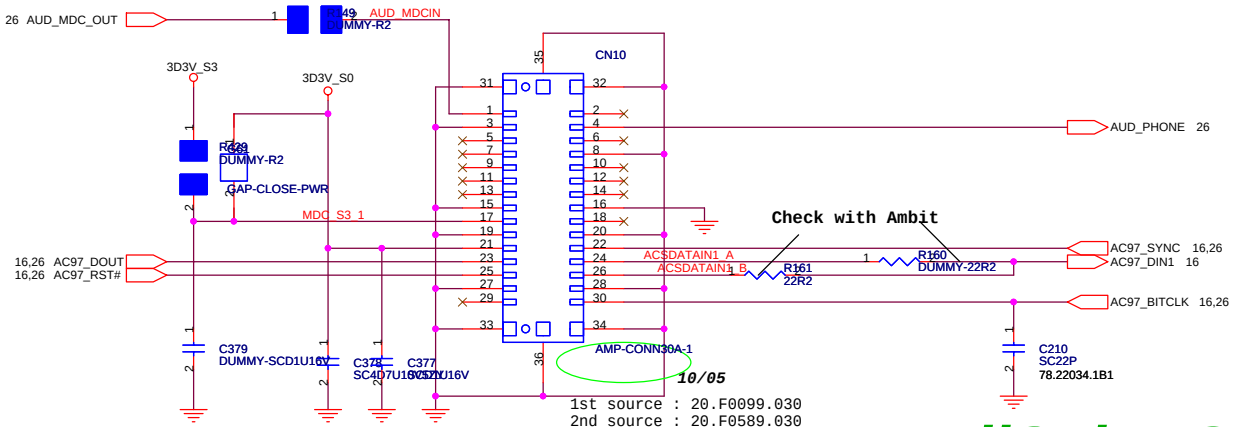
USB POWER



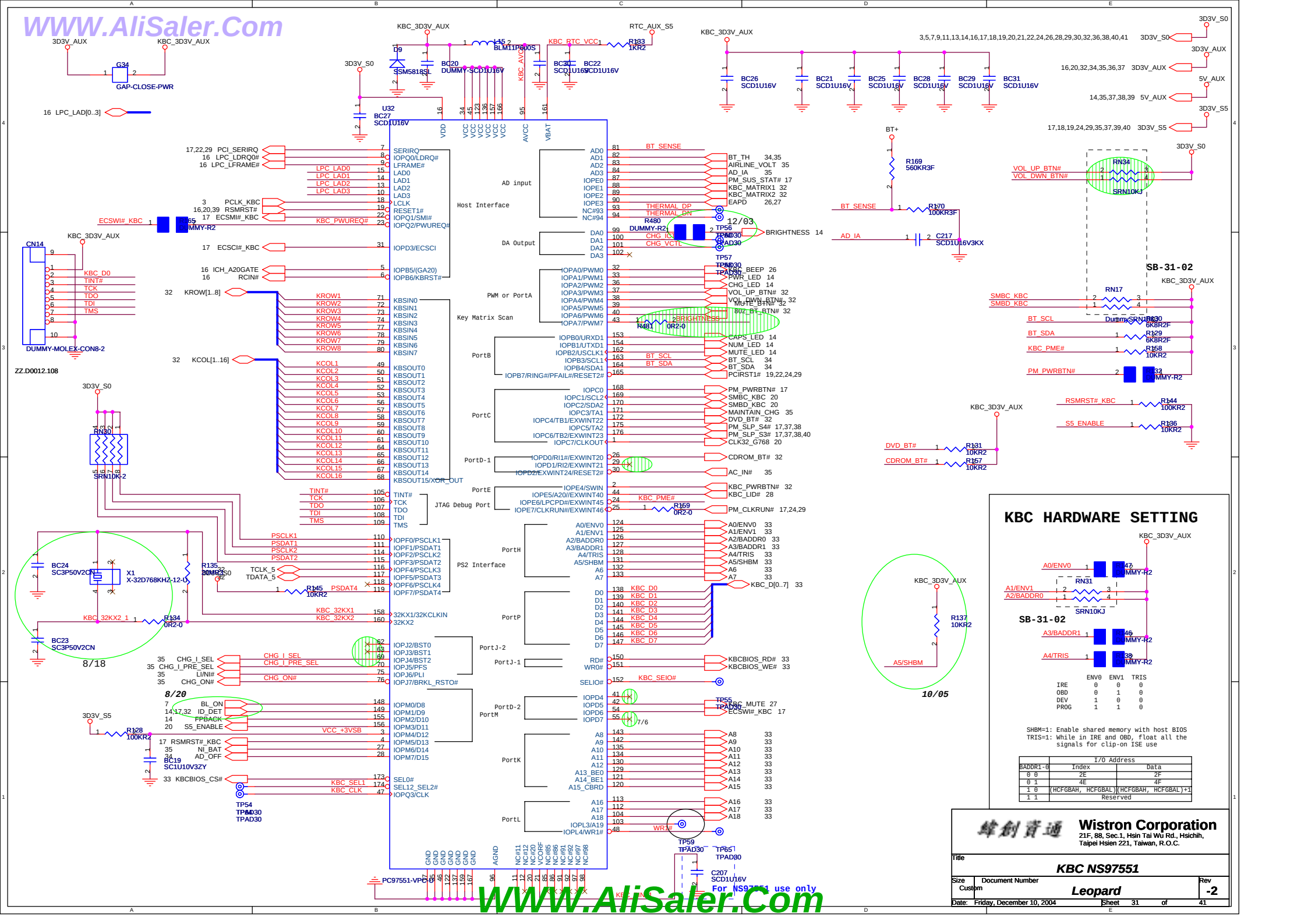




MDC Connector



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB / MDC CONN.		
Size: A3	Document Number: Leopard	Rev: -2
Date: Thursday, December 09, 2004	Sheet 30 of 41	



INTERNAL KEYBOARD CONNECTOR

KROW[1..8] 31 KCOL[1..16] 31

CN7

ETY-CON24-1
20.K0170.001

25	
1	KROW2
2	KROW8
3	KROW7
4	KCOL10
5	KROW5
6	KROW6
7	KCOL1
8	KROW3
9	KROW4
10	KCOL6
11	KCOL2
12	KROW1
13	KCOL3
14	KCOL5
15	KCOL8
16	KCOL9
17	KCOL7
18	KCOL4
19	KCOL13
20	KCOL14
21	KCOL15
22	KCOL12
23	KCOL11
24	KCOL16
26	

KBC_3D3V_AUX

R174 Dummy10KR2

R171 DUMMY-10KR2

KBC_MATRIX2 31
KBC_MATRIX1 31

the matrix table for PCB

KBC_MATRIX2,KBC_MATRIX1

	PA	PR
FF	00	01
DF	10	11

	NONE Quick Play	Quick Play
MATRIXID1#	0	1

KCOL9 KCOL8 KCOL5 KCOL3 — RC4 — SRC150P

KROW1 KCOL2 KCOL6 KROW4 — RC3 — SRC150P

KCOL14 KCOL13 KCOL4 KCOL7 — RC2 — SRC150P

KCOL16 KCOL11 KCOL12 KCOL15 — RC1 — SRC150P

for EMI

KROW3 KCOL1 KROW6 KROW5 — RC6 — SRC150P

KCOL10 KROW7 KROW8 KROW2 — RC5 — SRC150P

for EMI

SB-32-01

LAUNCH Board

POWER BUTTON

3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,36,38,40,41 3D3V_S0

16,20,31,34,35,36,37 3D3V_AUX

14,15,18,19,20,21,22,26,27,29,36,39,40,41 5V_S0

3D3V_S0 R284 10KR2 R282 10KR2

3D3V_AUX R268 10KR2

31 KBC_PWRBTN# R285 470R2 PWRBTN#

BC63 SCD1U16V

31 DVD_BT#
31 CDROM_BT#

5V_S3 CN2

C264 SCD1U10V2MX-1

14 PWR_LED#
14 MUTE_LED#
14 802_BT_LED#
31 VOL_UP_BTN#
31 VOL_DWN_BTN#
31 802_BT_BTN#
14,17,31 ID_DET
14 NUM_LED#
31 MUTE_BTN#

5V_S0

C265 SCD1U10V2MX-1

EC87 SC1000P16V2KX EC86 SC1000P16V2KX

JST-CON20
20.F0622.020

10/05

3D3V_S0 D33 DY-BAV99LT1 VOL_DWN_BTN#

3D3V_S0 D34 DY-BAV99LT1 VOL_UP_BTN#

11/30

VOL_DWN_BTN#
VOL_UP_BTN#
802_BT_LED#
MUTE_LED#
PWR_LED#
NUM_LED#

EC85 EC80 EC81 EC82 EC83 EC84
SC1000P16V2KX

TouchPad Connector

5V_S3

R385 10KR2 R386 10KR2

31 TDATA_5
31 TCLK_5

CN8

BC68 BC69 BC72 BC67
DUMMY-SCD1U16V

10/05

ETY-CON8-5

The symbol use 2nd source
The P/N is the main source
Main source:20.D0151.108
2nd source:21.D0010.108

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KEYBOARD/TOUCH PAD/Launch key
Size A3	Document Number Leopard
Rev	-2
Date: Friday, December 10, 2004	Sheet 32 of 41

3D3V_S0

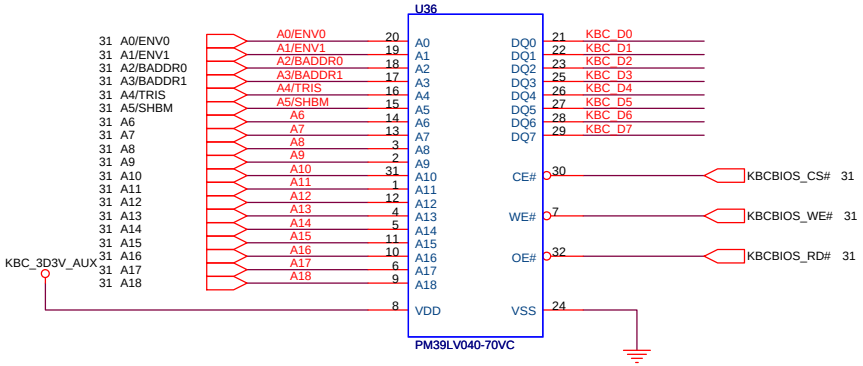
3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0

5V_S0

14,15,18,19,20,21,22,26,27,29,32,36,39,40,41 5V_S0

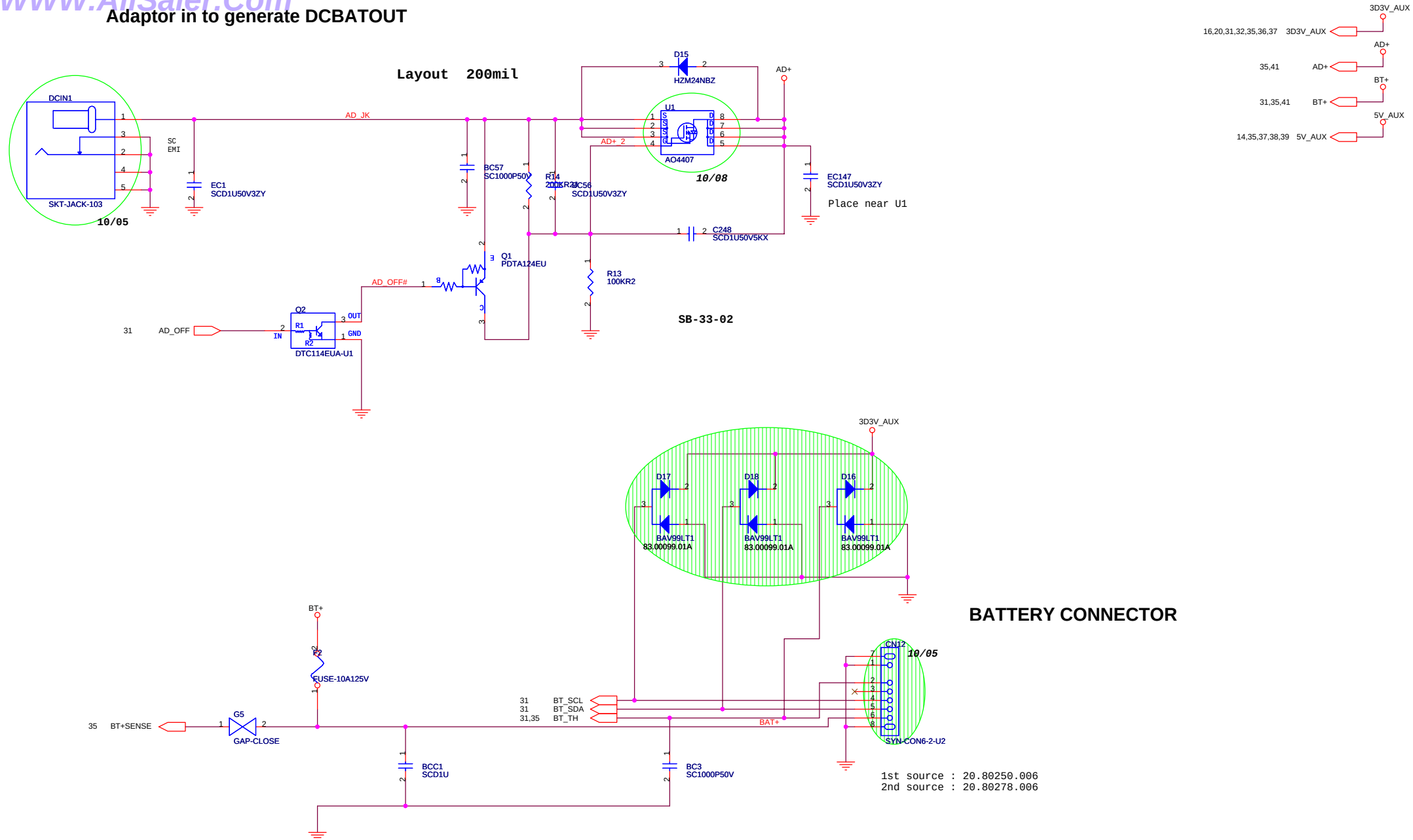
KBC_D[0..7] 31

512KB Flash



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS/GF***	
Size A3	Document Number ***Leopard***	Rev **-2**
Date: Thursday, December 09, 2004	Sheet 33 of 41	

Adaptor in to generate DCBATOUT

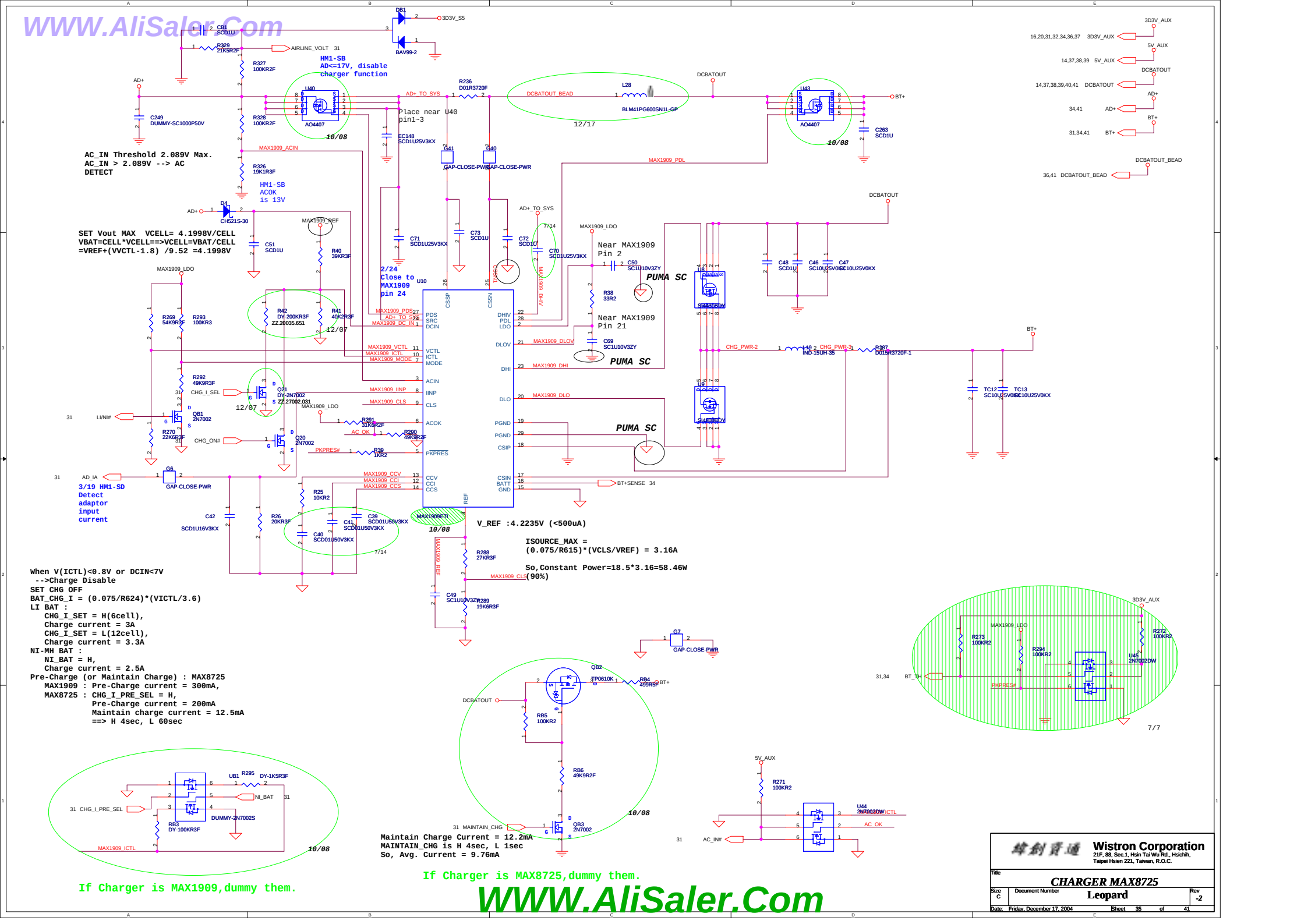


BATTERY CONNECTOR

1st source : 20.80250.006
2nd source : 20.80278.006

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

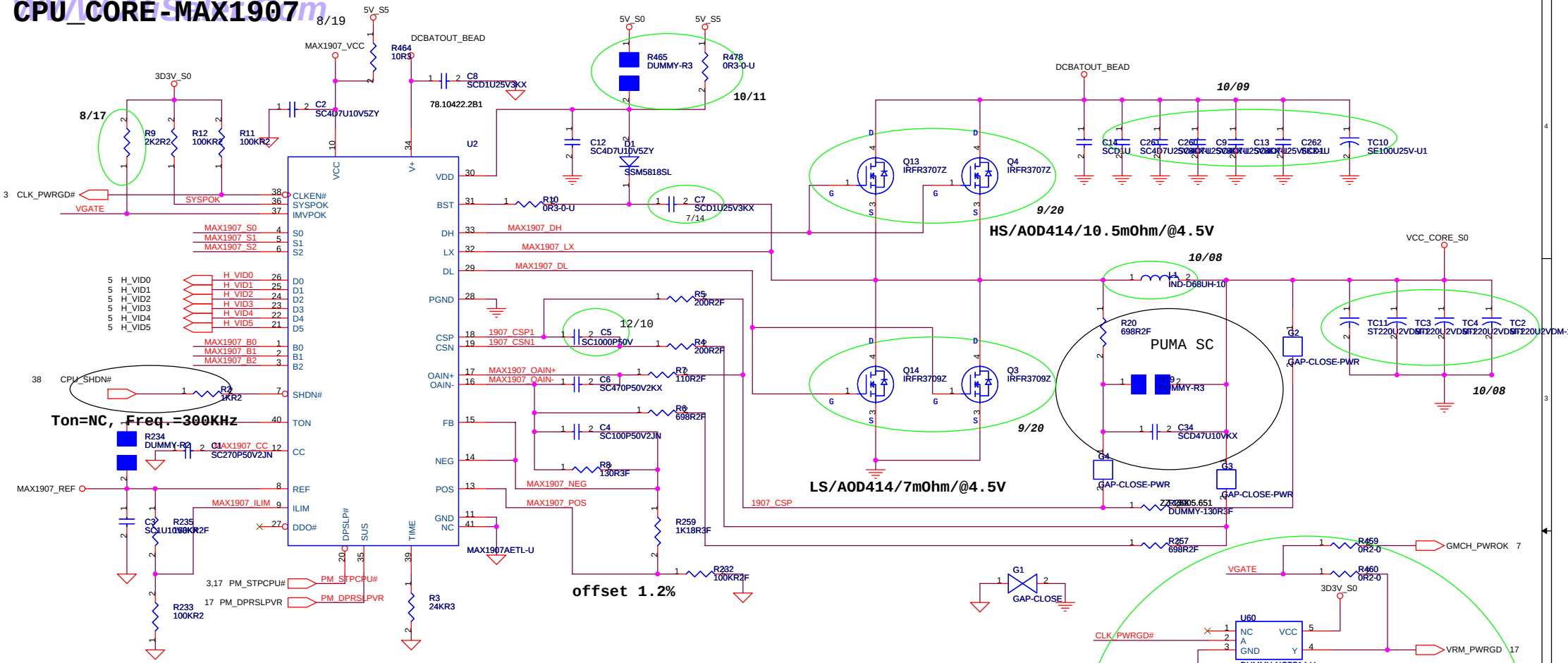
Title	Adaptor/ Bettery conn.	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 34 of 41	



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CHARGER MAX8725
Size C	Document Number Leopard
Rev	-2
Date: Friday, December 17, 2004	Sheet 35 of 41

CPU_CORE-MAX1907

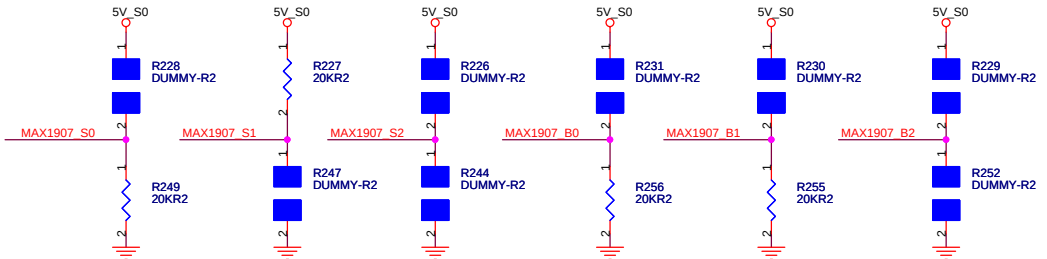
8/19



OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	0	1	1	0	0	0.940

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IMVP IV-CPU POWER-MAX1907
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SYSTEM DC/DC 3D3V_S5 / 5V_S5

3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 → 3D3V_S0
17,18,19,24,29,31,35,39,40 3D3V_S5 → 3D3V_S5
16,20,31,32,34,35,36 3D3V_AUX → 3D3V_AUX
14,18,20,36,38 5V_S5 → 5V_S5
14,35,38,39 5V_AUX → 5V_AUX
14,35,38,39,40,41 DCBATOUT → DCBATOUT

Sanyo / 6*7.7 / CV-AX

3V = 4Arms, OCP>6A

5V = 5Arms, OCP>6.8A

DCBATOUT, 5V_AUX, MAX1999_VCC

R76 4D7R5, C83 SC1U25V5CD1U, C84 SC1U25V5CD1U, R344 47R2, C291 SC1U10V3ZY, D22 BAW56LT1

C119 SCD1U, C118 SC4D7U25V-U

U25 AO4822, U24 AO4822

MAX1999_BST3, MAX1999_BST5, C307 SCD1U50V3KX, R356 0R3-U, R323 0R3-U, C279 SCD1U50V3KX

U52

CLOSE TO CMOS

U15 AO4822, U19 AO4822

C85 SC4D7U25V-U, C86 SC4D7U25V-U, C101 SCD1U

3D3V_DC_S5, 5V_DC_S3

L25 IND-8UH-2, L23 IND-8UH-2

10/08

MAX1999_DH3, MAX1999_LX3, MAX1999_DL3, MAX1999_FB3, MAX1999_ON3, MAX1999_ON5, MAX1999_SHDN#

MAX1999_DH5, MAX1999_LX5, MAX1999_DL5, MAX1999_FB5, MAX1999_PRO#, MAX1999_ILIM

BST3, DH3, LX3, DL3, OUT3, FB3, ON3, ON5, SHDN#, TON, REF, SKIP#, V+, VCC, BST5, DH5, LX5, DL5, OUT5, FB5, PRO#, NC, ILIM5, ILIM3, PGOOD, GND, LDO3, LDO5

TC18 ST220U4VDM-L3, C80 SC100P50V2JN, R73 6K98R3F, C99 SC47P50V2JN, R82 2MR3

TC14 ST150U6D3VDM-, C82 SC47P50V2JN, R71 2MR3, R74 15K4R3, C81 SC100P50V2JN

R75 10KR3F, R72 10KR3F

These components should be located near by MAX1977

R350 1KR2, R341 1KR2

20,38 1999_S5ENABLE

17,31,38 PM_SLP_S4#

D6 DUMMY-1SS400, DUMMY-1SS400

39 BL3#

MAX1999_REF, Vref = 2V, C289 SCD22U10V3KX

3V_LDO=100mA, MAX1999_LDO3, C293 SC1U10V3KX

5V_LDO=100mA, MAX1999_LDO5, C292 SC2D2U6D3V3MX-1, G44 GAP-CLOSE-PWR

MAX1999EEI

MAX1999_VCC, R70 300KR3, R68 200KR3

5V_DC_S3, 5V_S3

MAX1999_V+, R69 300KR3, R67 150KR3

5V_AUX, R342 300KR2J

MAX1999_SKIP#

3D3V_AUX, G43 GAP-CLOSE-PWR, EC149 SCD1U16V

3D3V_S5, Q23 DTC115EE-U (R1, R2, IN, OUT, GND)

17,31,38,40 PM_SLP_S3#

5V_S5 spec. = 10mA

3D3V_DC_S5, 3D3V_S5

PM_SLP_S3# high = PWM
PM_SLP_S3# low = Ultrasonic

SKIP# > 2.4V : PWM mode
SKIP# = GND(,0.8V) : SKIP MODE
SKIP# = REF (1.7V~2.3V)/FloatING
Ultrasonic MODE(25KHz min)

MAX1999_ON3, MAX1999_ON5, C290 DUMMY-C2, C302 DUMMY-C2

G21 GAP-CLOSE

```
ILIM5: 5V * 200K / (200K+300K) = 2.0V
            200mV / 24 = 8.3A
             OCP point = 8.3A +1/2Iripple

ILIM3: 5V * 200K / (200K+300K) = 2.0V
            200mV / 24 = 8.3A
             OCP point = 8.3A +1/2Iripple
            OCP point = 20A +1/2Iripple
```

ILIM=Vcc 100mV*
ILIM=Vref 200mV*
OCP= 0.1Vth/Rds(on) + 0.5Iripple

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*DC/DC 3V_S5/5V_S5*	
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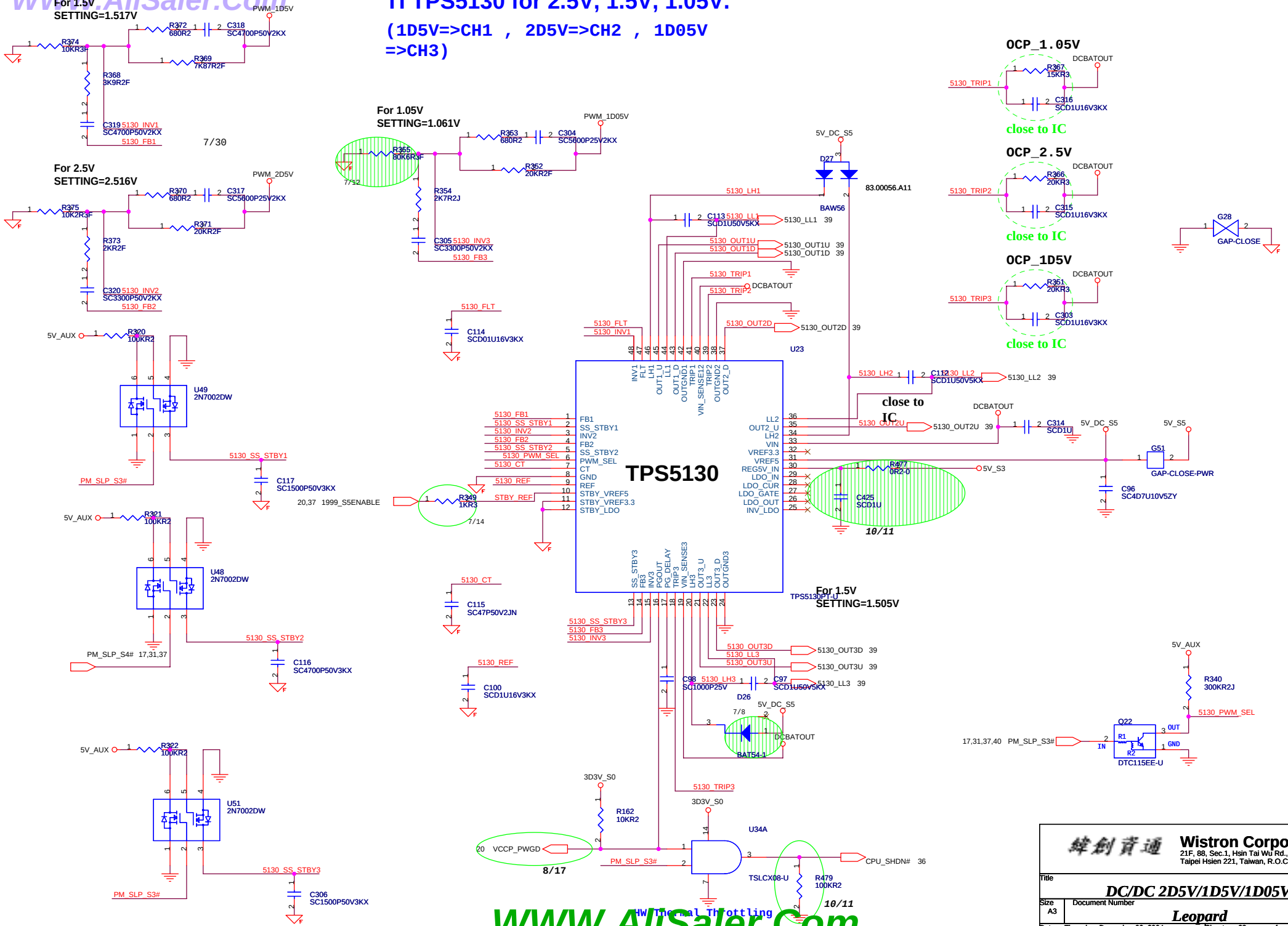
TI TPS5130 for 2.5V, 1.5V, 1.05V.

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



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Title	DC/DC 2D5V/1D5V/1D05V	
Size A3	Document Number: Leopard	Rev -2
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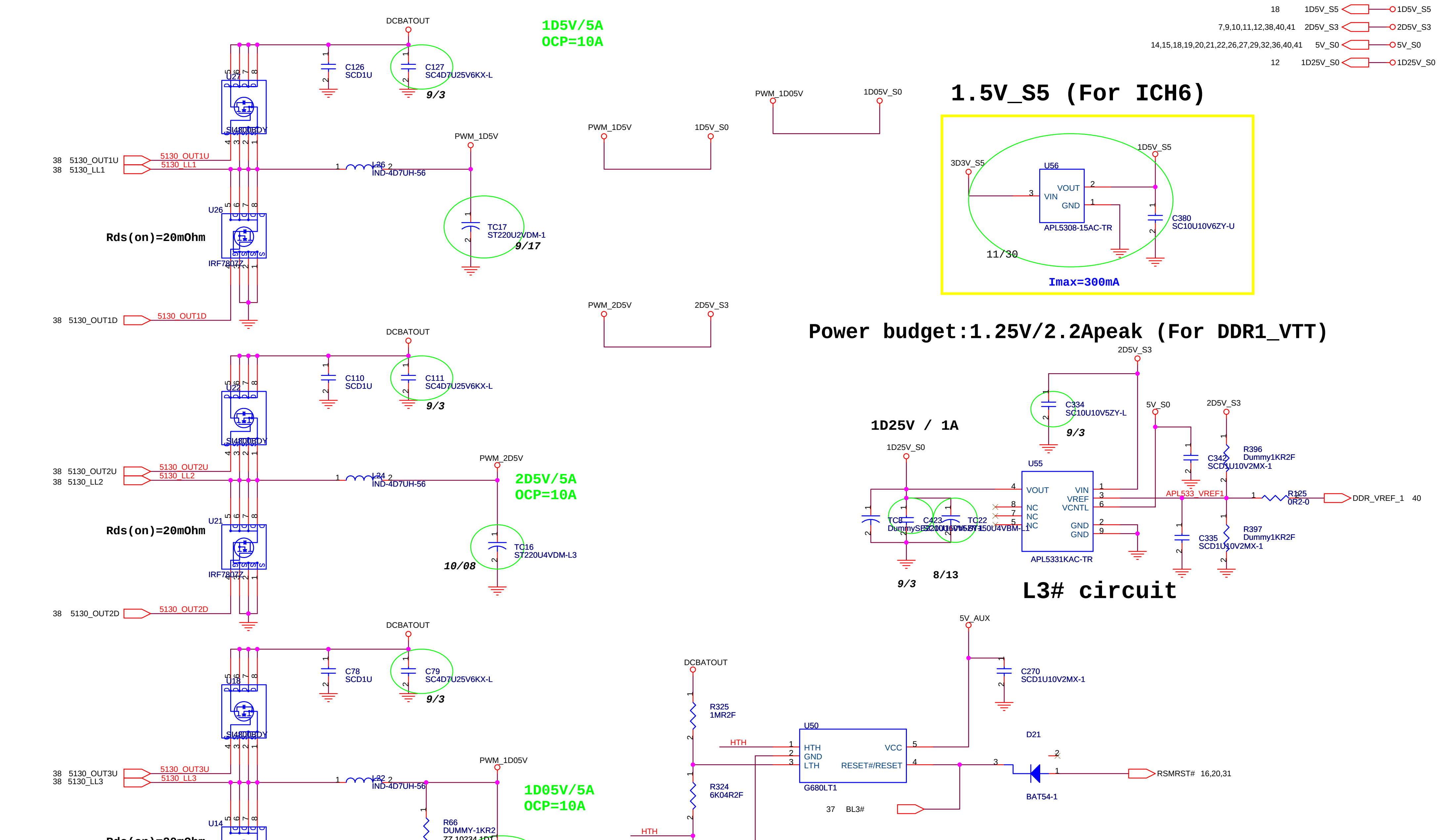
TI TPS5130 for 2.5V, 1.5V, 1.05V

(2D5V=>CH1 , 3D3V=>CH2 , 5V =>CH3)



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Title: 39.DC/DC 2D5V/1D5V/1D05V-2

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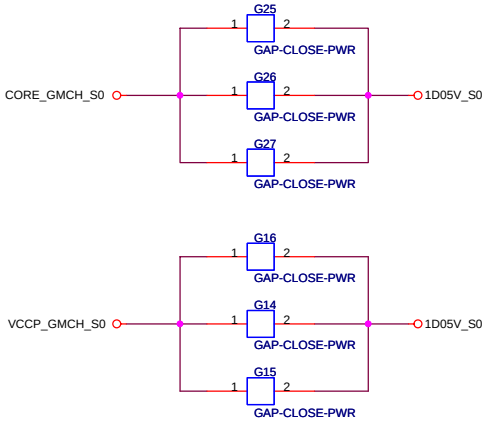
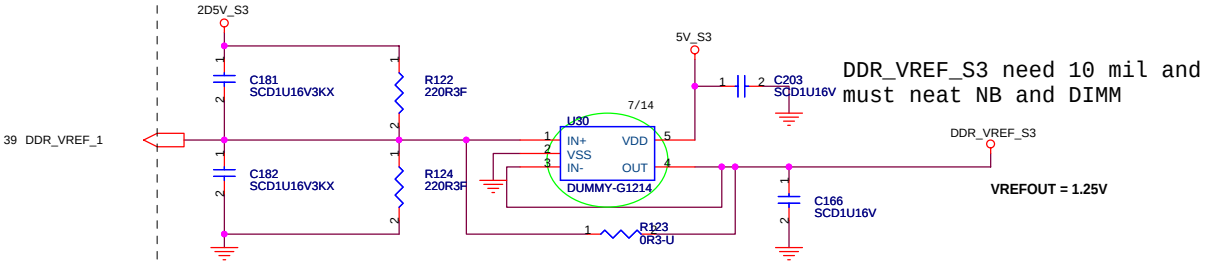
FOR GMCH Power



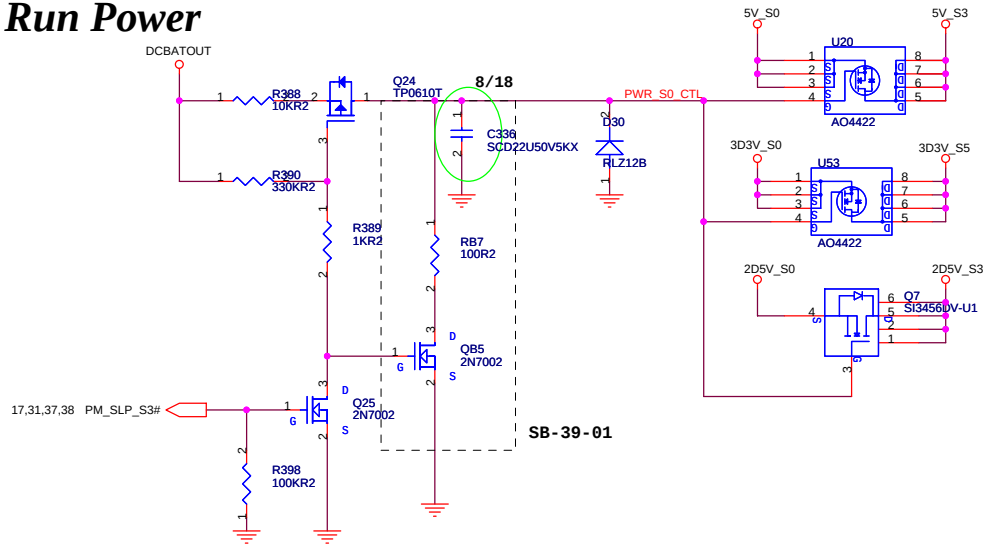
3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,41 3D3V_S0 — 3D3V_S0
28,30 3D3V_S3 — 3D3V_S3
17,18,19,24,29,31,35,37,39 3D3V_S5 — 3D3V_S5
14,15,18,19,20,21,22,26,27,29,32,36,39,41 5V_S0 — 5V_S0
14,25,30,32,37,38,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
7,9,15,18 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,41 2D5V_S3 — 2D5V_S3
7,11 DDR_VREF_S3 — DDR_VREF_S3
14,35,37,38,39,41 DCBATOUT — DCBATOUT
38,39,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,41 CORE_GMCH_S0 — CORE_GMCH_S0



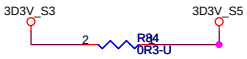
DDR_VREF_S3 need 10 mil and must neat NB and DIMM

FOR DDR Power

Run Power



Suspend Power



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Title	PWRPLANE&RESETLOGIC	
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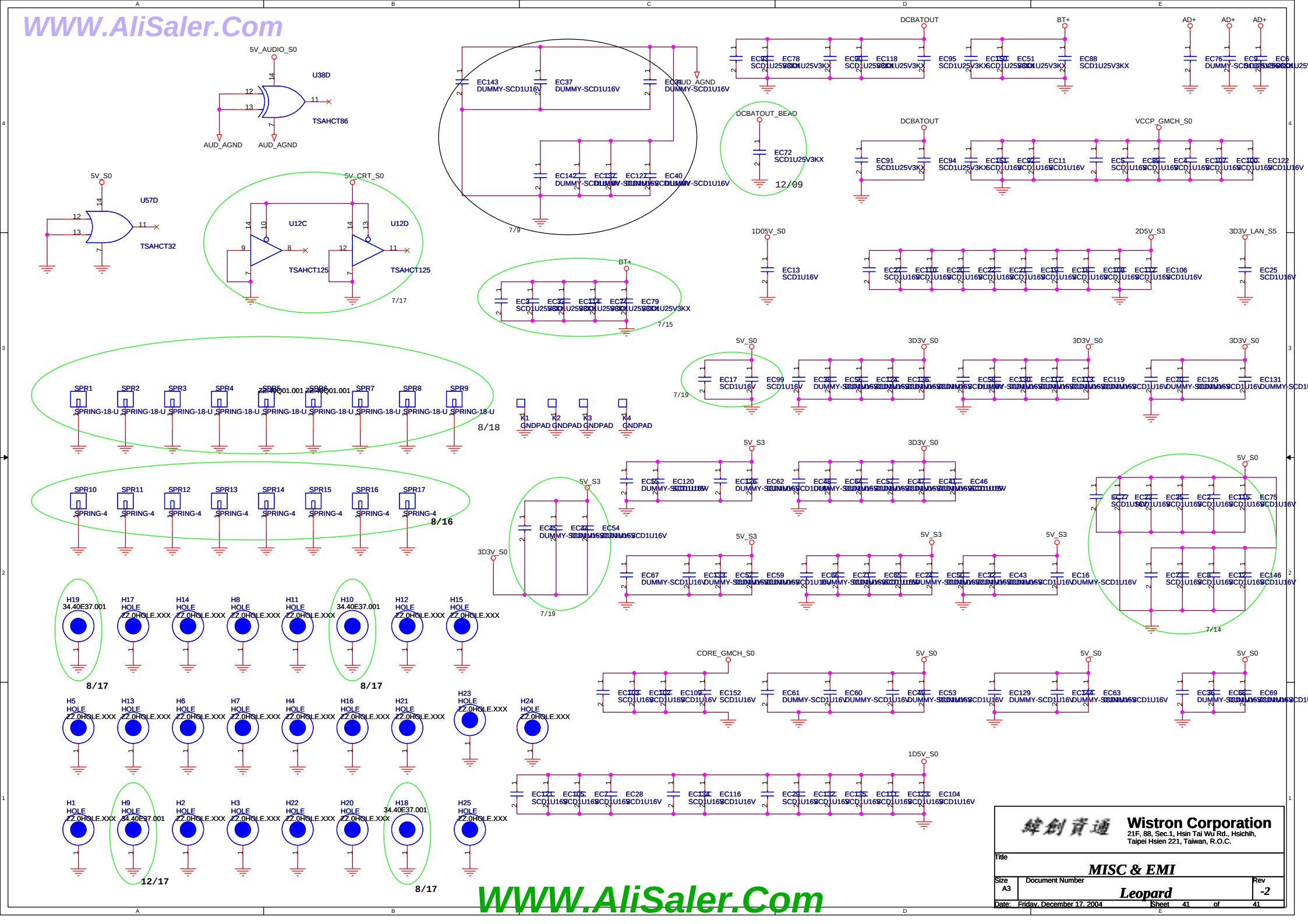

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Title: MISC & EMI

Size: A3 | Document Number: Leopard | Rev: -2

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