Jones/Cujo 2.0 (UP6/7) BLOCK DIAGRAM

01

PCB STACK UP

6L Dis.

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : BOT

CPU
Auburndale 35W
Clarksfield 45W
PAGE 3~6

DDRIII-SODIMM1 PAGE 12 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

DDRIII-SODIMM2 PAGE 13 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

PCI-Express 16X

27MHz

nVIDIA
N10M-GE
N10P-GE
128 Bit
PAGE 14~20
969p

- HDMI CON PAGE 22
- CRT PAGE 22
- Dual Link — LCD CONN PAGE 21

DMI LINK

32.768KHz 25MHz

PCH
Ibex-M
PAGE 7~11

- SATA - HDD PAGE 31 — SATA0 150MB
- SATA - CD-ROM PAGE 31 — SATA1 150MB
- SATA - 2ndHDD PAGE 31 — SATA4 150MB
- E-SATA PAGE 30 — SATA5 150MB
- Accelerometer LIS3LV02DL PAGE 25 — SMBUS

CLOCK GEN
9LRS3197
PAGE 2
14.318MHz

USB2.0

Mini PCI-E Card x2
Express Card x1
Cable Docking x1
4,7,10,11

- USB2.0 Ports X4 PAGE 30 — 0,1,8,9
- BlueTooth PAGE 30 — 5
- Webcam PAGE 30 — 3
- Fingerprint PAGE 30 — 2

Cable Docking PAGE 32
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PCI-E — 24.576MHz

- Mini PCI-E Card WWAN/TV PAGE 34 — X1
- Mini PCI-E Card Wireless LAN PAGE 34 — X1
- LAN Realtek RTL8111DL GigaLAN PAGE 27 — X1
- Express Card PAGE 31 — X1
- JMICRO 380 PAGE 23 — X1
  - IEEE1394 PAGE 23
  - Memory CardReader PAGE 23

25MHz
RJ45 PAGE 27

32.768KHz

ENE KBC
KB3926 D2
PAGE 29

LPC

- Keyboard PAGE 31
- Touch Pad PAGE 29
- Capacitive Sense SW PAGE 32

- GMT G9931P1U FAN PAGE 32
- SPI PAGE 29

ONFI

- Braidwood PAGE 33
- SPI PAGE 7
- MDC CONN PAGE 32

Azalia

Analog
IDT92HD75B3
PAGE 24

- AUDIO Amplifier TPA6047A4 PAGE 25
- AUDIO Amplifier TPA3007D1 PAGE 26

- microphone PAGE 24
- Audio Jacks (Phone/ MIC) PAGE 24
- Jack to Speaker PAGE 25
- Jack to Sub-Woofer PAGE 26

- SYSTEM POWER RT8206B PAGE 35
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 36
- CPU CORE ISL6251A PAGE 41
- VGACORE(1.025V) RT8208A PAGE 38
- DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 39
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 40

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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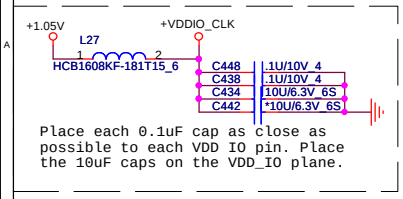
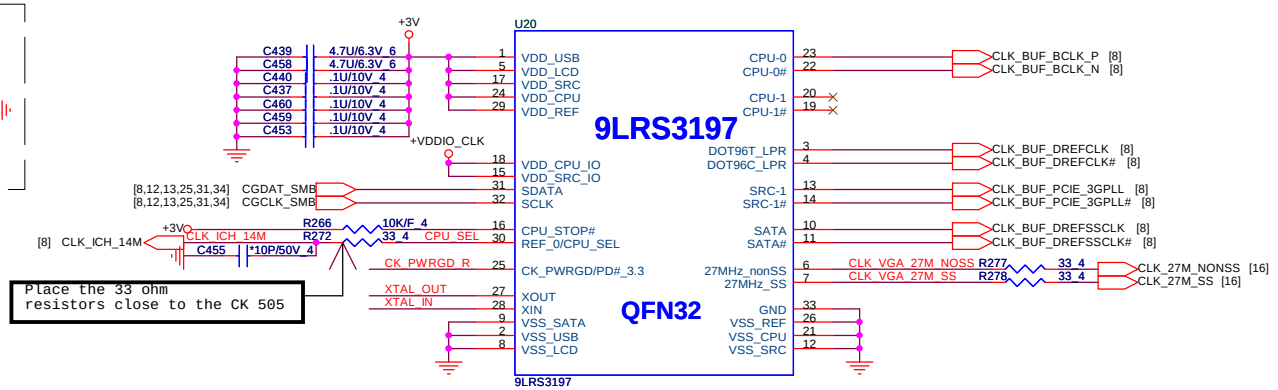
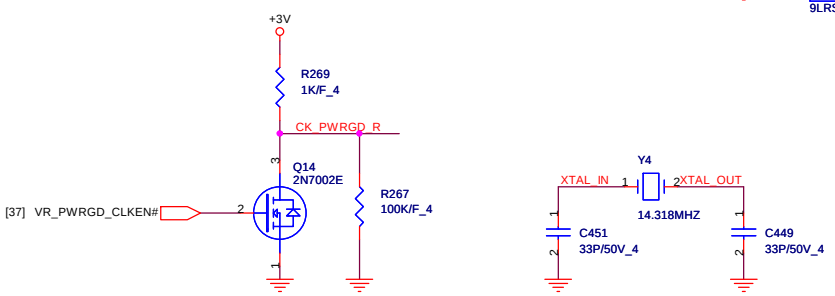
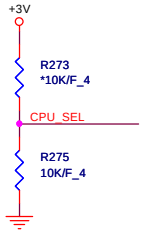


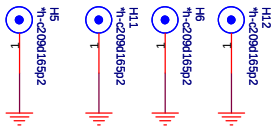




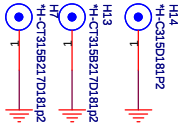


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

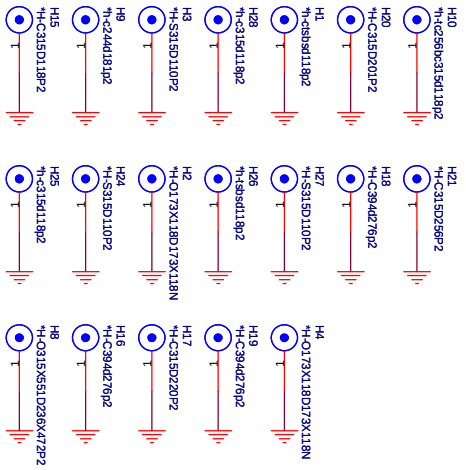
CPU bracket Hole.



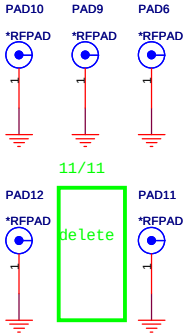
VGA bracket Hole.



M/B Screw Hole

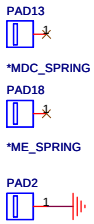


RF PAD

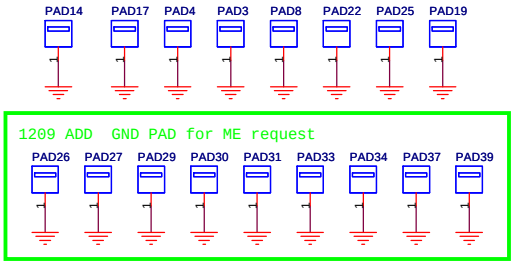


ME PAD

Routed spring



ME-Ground Pad



[3,7,9,10,11,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V

NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: CLOCK & Screw Holes	Rev: 1A
Date: Friday, February 27, 2009	Sheet 2 of 45	

U33A

DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

U33B

MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

SI 2/5 Modified

For ITP CLk

U56 MC74VHC1G08DFT2G

JTAG MAPPING

Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A

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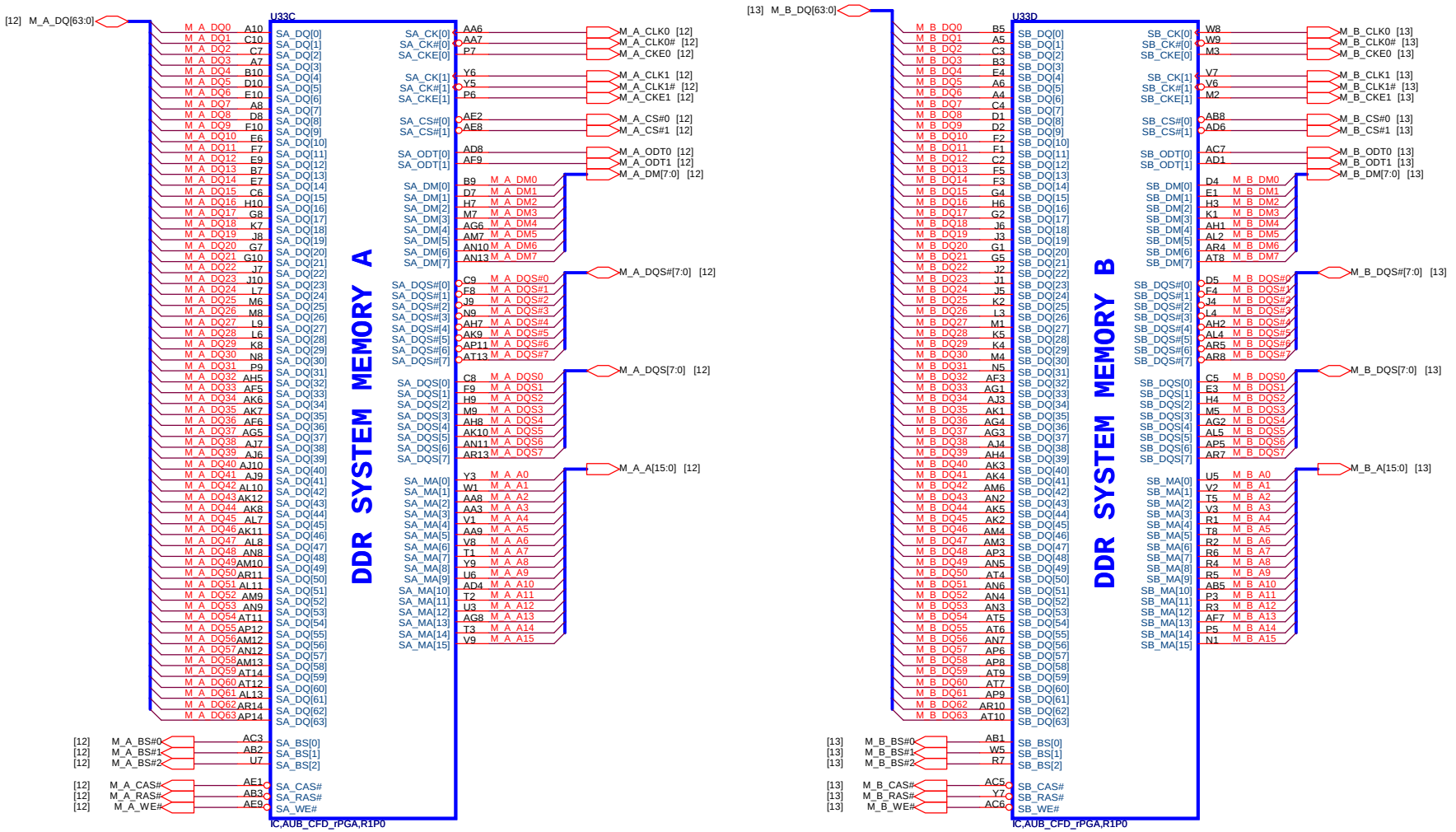
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

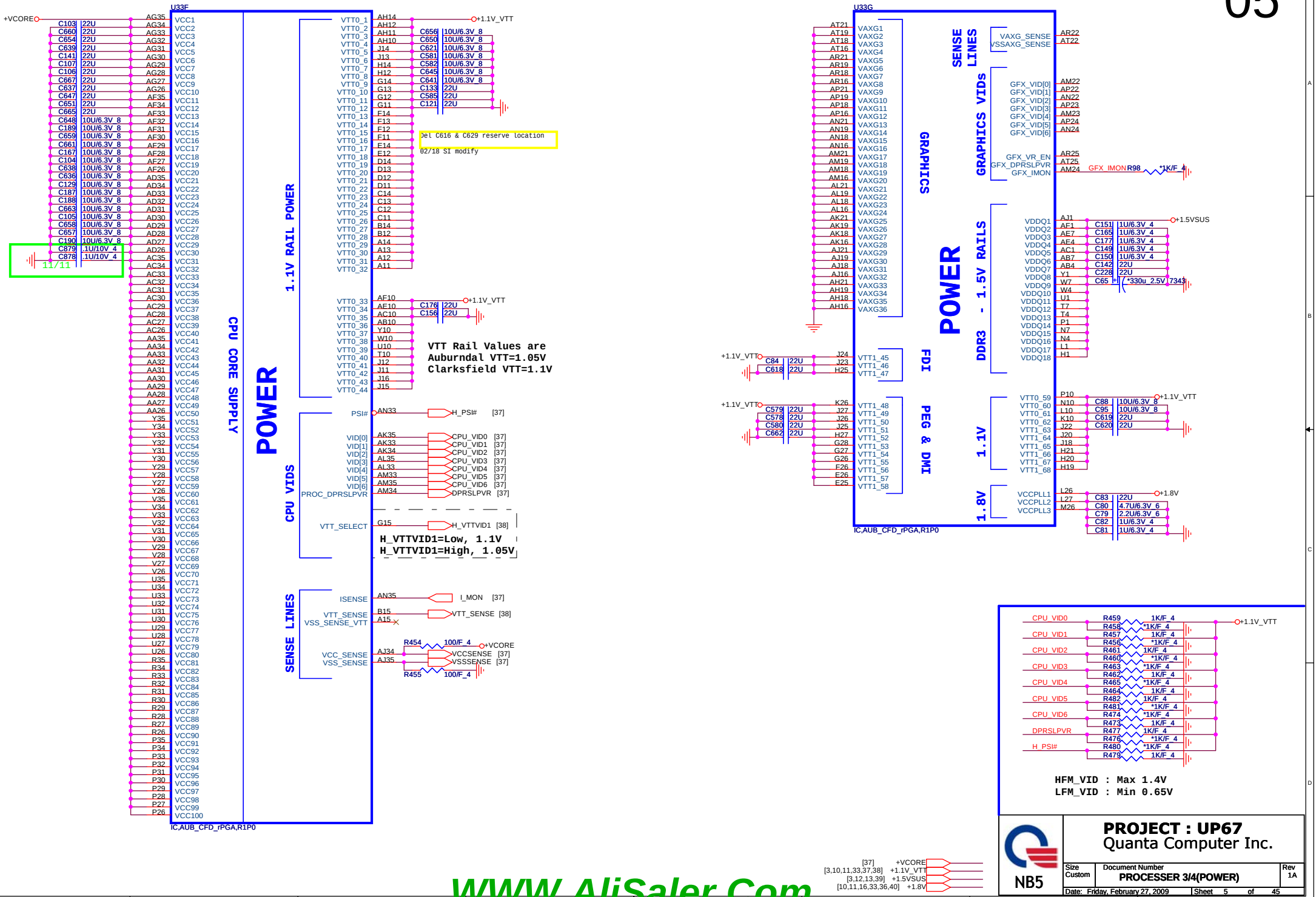


NB5

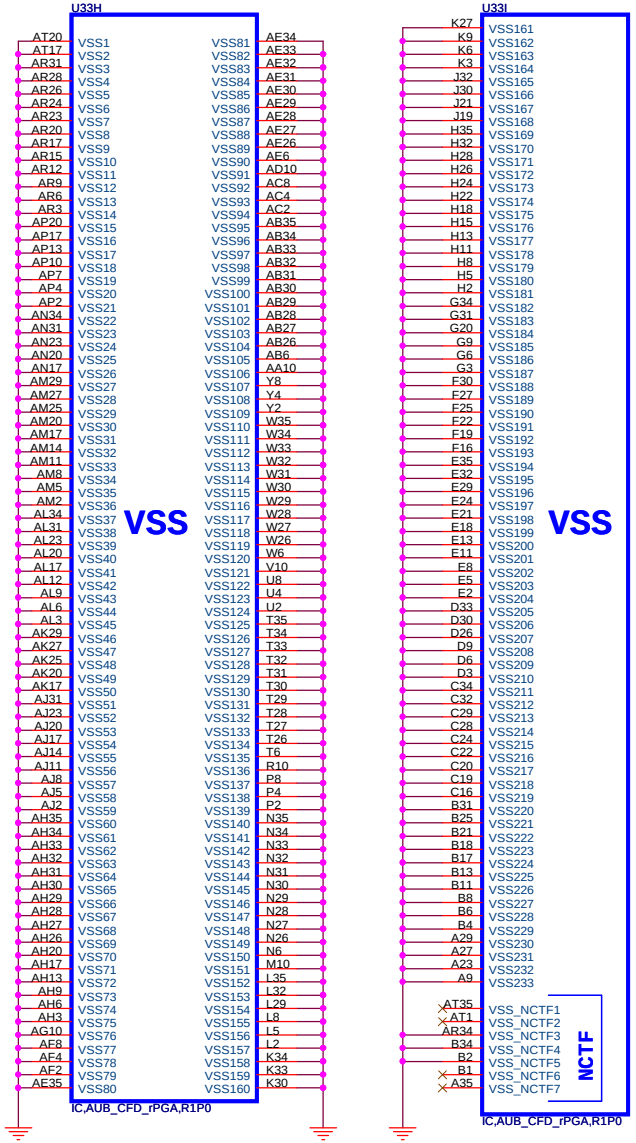
PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

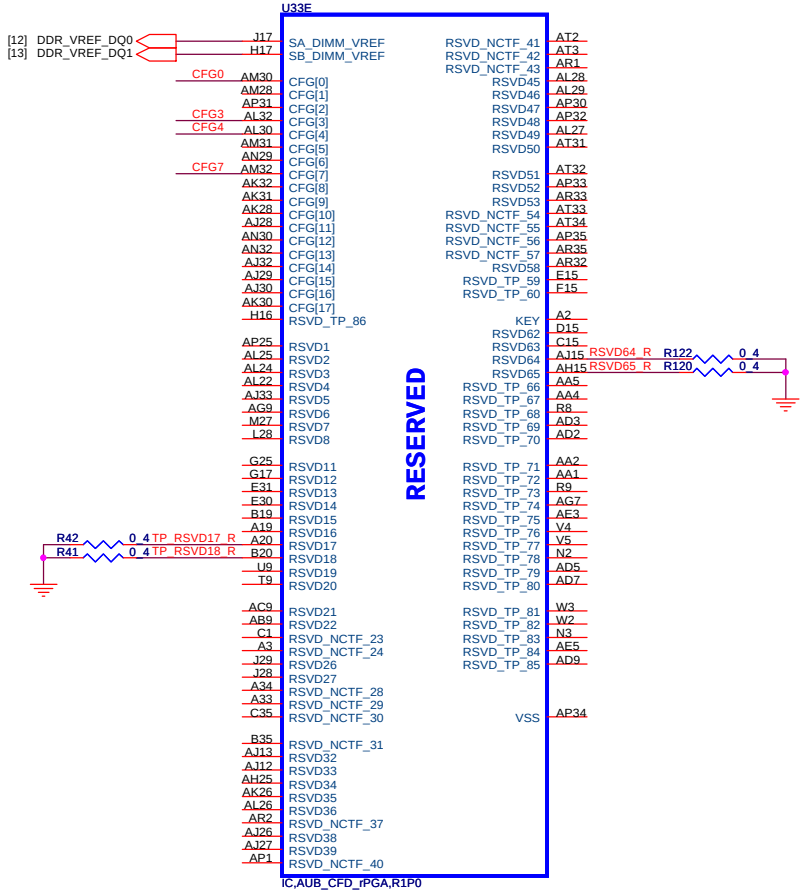
Date: Friday, February 27, 2009 Sheet 4 of 45



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

PROJECT : UP67
Quanta Computer Inc.

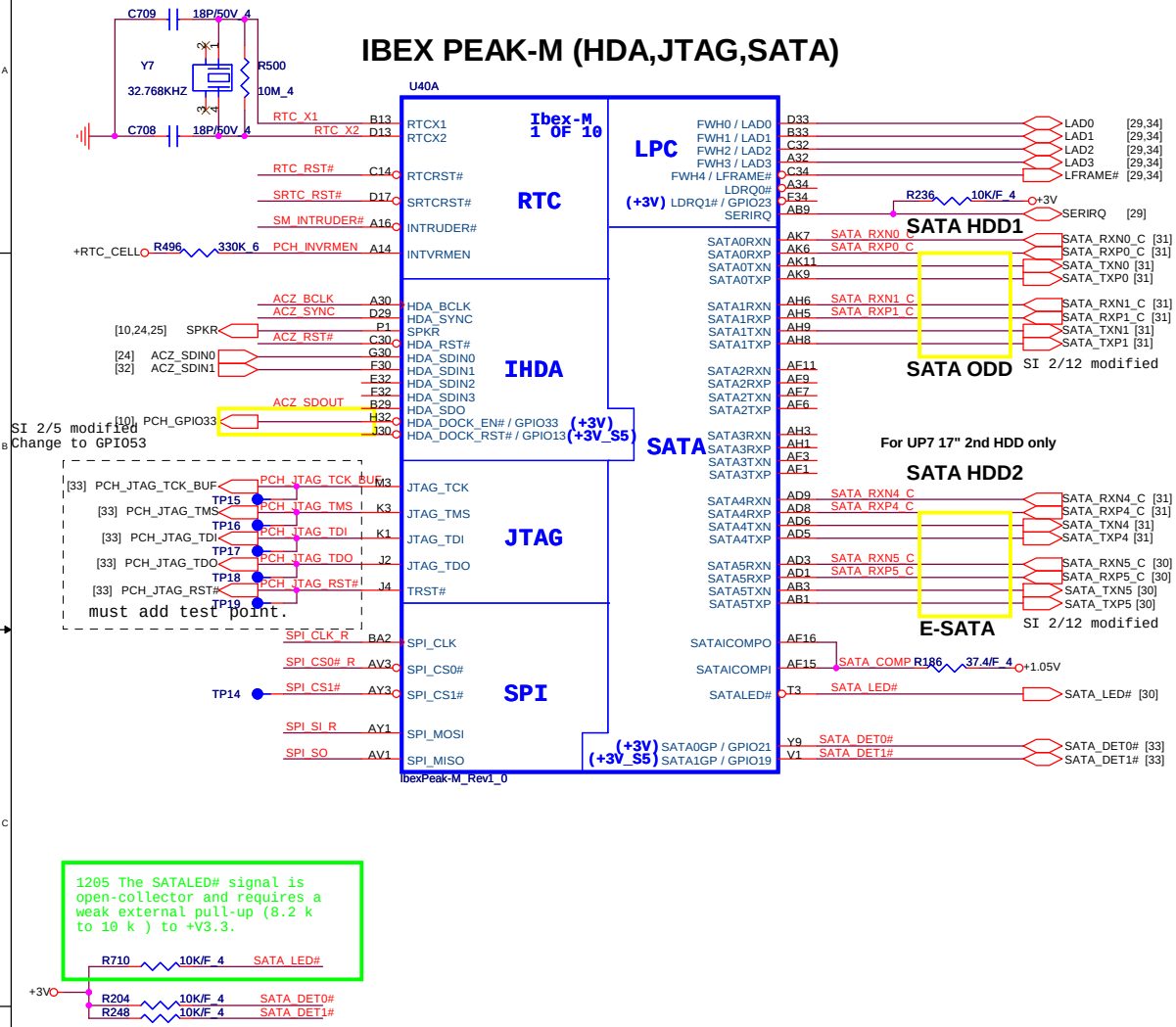
NB5

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

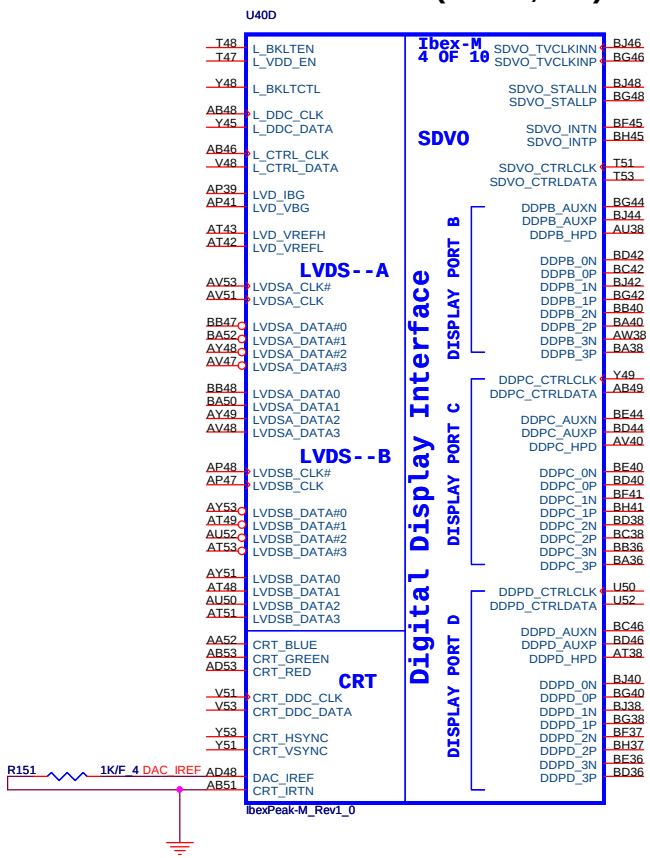
Date: Friday, February 27, 2009 Sheet 6 of 45

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

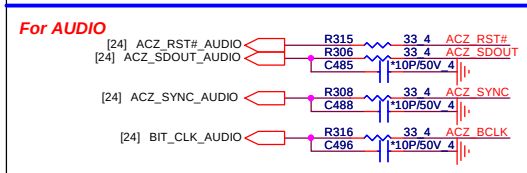


IBEX PEAK-M (LVDS,DDI)

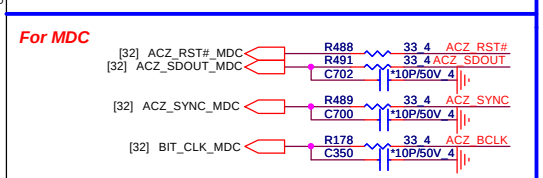


1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

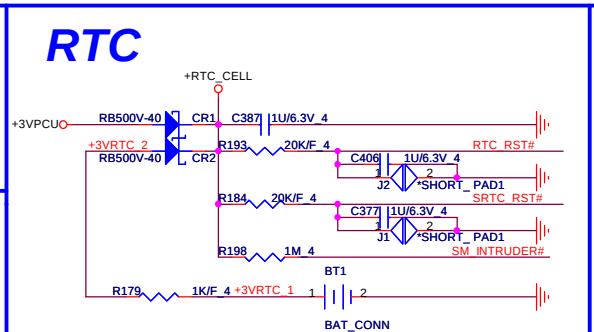
For AUDIO



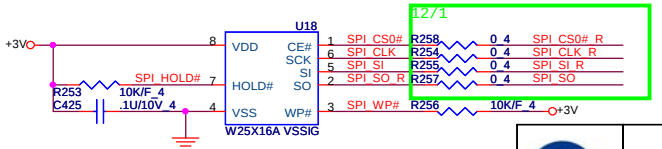
For MDC



RTC



2M byte SPI ROM for ME & Bios



Socket: DG008000031
MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
SI 2/17 modified

NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 2/6 (SATA,HDA,LPC)	Rev: 1A
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IBEX PEAK-M (GND)

U40I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BF6	VSS[206]	VSS[306]	U34
BF8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
F6	VSS[238]	VSS[338]	Y38
F8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

IbexPeak-M_Rev1_0

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U40B

Ibex-M 2 OF 10

PCI-E*

[WLAN] PCIE_RXN0 BG30 / PCIE_RXP0 BJ30 / PCIE_TXN0 BF29 / PCIE_TXP0 BH29 — C697 .1U/10V_4 PCIE_TXN0_C, C698 .1U/10V_4 PCIE_TXP0_C — PERN1 PERP1 PETN1 PETP1

[LAN] PCIE_RXN1_LAN AW30 / PCIE_RXP1_LAN BA30 / PCIE_TXN1_LAN BC30 / PCIE_TXP1_LAN BD30 — C341 .1U/10V_4 PCIE_TXN1_C, C340 .1U/10V_4 PCIE_TXP1_C — PERN2 PERP2 PETN2 PETP2

[USB3.0] PCIE_RXN1_USB3.0 AU30 / PCIE_RXP1_USB3.0 AT30 / PCIE_TXN1_USB3.0 AU32 / PCIE_TXP1_USB3.0 AV32 — C381 .1U/10V_4 PCIE_TXN3_C, C382 .1U/10V_4 PCIE_TXP3_C — PERN3 PERP3 PETN3 PETP3

[TV tuner] PCIE_RXN4 BA32 / PCIE_RXP4 BB32 / PCIE_TXN4 BD32 / PCIE_TXP4 BE32 — C380 .1U/10V_4 PCIE_TXN4_C, C373 .1U/10V_4 PCIE_TXP4_C — PERN4 PERP4 PETN4 PETP4

[Card reader] PCIE_RXN5 BF33 / PCIE_RXP5 BH33 / PCIE_TXN5 BG32 / PCIE_TXP5 BJ32 — C353 .1U/10V_4 PCIE_TXN5_C, C363 .1U/10V_4 PCIE_TXP5_C — PERN5 PERP5 PETN5 PETP5

BA34 PERN6 / AW34 PERP6 / BC34 PETN6 / BD34 PETP6

AT34 PERN7 / AU34 PERP7 / AU36 PETN7 / AV36 PETP7

Swap PCIE port 6 to port 8 for BIOS request

[New Card] PCIE_RXN6 BG34 / PCIE_RXP6 BJ34 / PCIE_TXN6 BG36 / PCIE_TXP6 BJ36 — C345 .1U/10V_4 PCIE_TXN6_C, C331 .1U/10V_4 PCIE_TXP6_C — PERN8 PERP8 PETN8 PETP8

AK48 CLKOUT_PCIE0N / AK47 CLKOUT_PCIE0P

MiniWLAN: PCIE_CLK_REQ0# P9 PCIECLKRQ0# / GPIO73 (+3V_S5); CLK_PCIE_WLAN# AM43 CLKOUT_PCIE1N; CLK_PCIE_WLAN AM45 CLKOUT_PCIE1P; CLK1_OE# [33] — R235 0_4 CLK1_OE# — U4 PCIECLKRQ1# / GPIO18 (+3V); CLK_PCIE_WLAN# [34], CLK_PCIE_WLAN [34]

TVC: CLK_PCIE_TVC# AM47 CLKOUT_PCIE2N; CLK_PCIE_TVC AM48 CLKOUT_PCIE2P; CLK2_OE# [33] — R230 0_4 CLK2_OE# — N4 PCIECLKRQ2# / GPIO20 (+3V); CLK_PCIE_TVC# [34], CLK_PCIE_TVC [34]

LAN: CLK_PCIE_LAN# [27] AH42 CLKOUT_PCIE3N; CLK_PCIE_LAN [27] AH41 CLKOUT_PCIE3P; PCIE_CLK_REQ3# [27] — R191 0_4 PCIE_CLK_REQ3#_R — A8 PCIECLKRQ3# / GPIO25 (+3V_S5)

Express Card: CLK_PCIE_NEW# [31] AM51 CLKOUT_PCIE4N; CLK_PCIE_NEW [31] AM53 CLKOUT_PCIE4P; PCIE_CLK_REQ4# [31] — R220 0_4 PCIE_CLK_REQ4#_R — M9 PCIECLKRQ4# / GPIO26 (+3V_S5)

CARD READER: CLK_PCIE_CARD# [23] AJ50 CLKOUT_PCIE5N; CLK_PCIE_CARD [23] AJ52 CLKOUT_PCIE5P; PCIE_CLK_REQ5# H6 PCIECLKRQ5# / GPIO44 (+3V_S5)

USB3.0 GEN2: CLK_USB3.0_GEN2# [28] AK53 CLKOUT_PEG_B_N; CLK_USB3.0_GEN2 [28] AK51 CLKOUT_PEG_B_P; PCIE_CLK_REQB# [28] — R265 0_4 PCIE_CLK_REQB#_R — P13 PEG_B_CLKRQ# / GPIO56 (+3V_S5)

SMBus (+3V_S5)
SMBALERT# / GPIO11 B9 SMBALERT# 10K/F_4 R217
SMBCLK H14 PCLK_SMB 2.2K_4 R194
SMBDATA C8 PDAT_SMB 2.2K_4 R234
SML0ALERT# / GPIO60 J14 SML0ALERT# 10K/F_4 R187
SML0CLK C6 SMB_CLK_ME0 2.2K_4 R244
SML0DATA G8 SMB_DATA_ME0 2.2K_4 R210
SML1ALERT# / GPIO74 M14 SML1ALERT# 10K/F_4 R185
SML1CLK / GPIO58 E10 SMB_CLK_ME1 4.7K_4 R209
SML1DATA / GPIO75 G12 SMB_DATA_ME1 4.7K_4 R197
+3VS5

Controller Link
CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9

PEG (+3V_S5)
PEG_A_CLKRQ# / GPIO47 H1 PEG_CLKREQ#
CLKOUT_PEG_A_N AD43 CLK_PCIE_VGA# [14]
CLKOUT_PEG_A_P AD45 CLK_PCIE_VGA [14]
CLKOUT_DMI_N AN4 CLK_PCIE_3GPLL# [3]
CLKOUT_DMI_P AN2 CLK_PCIE_3GPLL [3]

From CLK BUFFER
CLKOUT_DP_N / CLKOUT_BCLK1_N AT1
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3
CLKIN_DMI_N AW24 CLK_BUF_PCIE_3GPLL# [2]
CLKIN_DMI_P BA24 CLK_BUF_PCIE_3GPLL [2]
CLKIN_BCLK_N AP3 CLK_BUF_BCLK_N [2]
CLKIN_BCLK_P AP1 CLK_BUF_BCLK_P [2]
CLKIN_DOT_96N F18 CLK_BUF_DREFCLK# [2]
CLKIN_DOT_96P E18 CLK_BUF_DREFCLK [2]
CLKIN_SATA_N / CKSSCD_N AH13 CLK_BUF_DREFSSCLK# [2]
CLKIN_SATA_P / CKSSCD_P AH12 CLK_BUF_DREFSSCLK [2]
REFCLK14IN P41 CLK_ICH_14M [2]
CLKIN_PCILOOPBACK J42 CLK_PCI_FB CLK_PCI_FB [9]
XTAL25_IN AH51 XTAL25_IN
XTAL25_OUT AH53 XTAL25_OUT
XCLK_RCOMP AF38 XCLK_RCOMP — R157 90.9/F_4 — +1.05V

Clock Flex
(+3V) CLKOUTFLEX0 / GPIO64 T45 CLK_LEX0
(+3V) CLKOUTFLEX1 / GPIO65 P43 CLK_LEX1
(+3V) CLKOUTFLEX2 / GPIO66 T42 CLK_LEX2
(+3V) CLKOUTFLEX3 / GPIO67 N50 CLK_FLEX3
T40 T41 T42
R686 22_4 CLK_USB3.0_48M_PCH [28]

1203 Intel EDS1.0 spec change to no support 27and 24MHZ

+3V
CLK1_OE# R228 10K/F_4
CLK2_OE# R229 10K/F_4

+3VS5
PCIE_CLK_REQ0# R196 10K/F_4
PCIE_CLK_REQ3#_R R212 10K/F_4
PCIE_CLK_REQ4#_R R221 10K/F_4
PCIE_CLK_REQB#_R R182 10K/F_4
PCIE_CLK_REQ5# R243 10K/F_4
PEG_CLKREQ# R241 10K/F_4

SMB_CLK_ME1 — Q61 2N7002E — MBCLK2 [17,29]
R246 2.2K_4
+3V — R312 2.2K_4 — 2/5 Modified
SMB_DATA_ME1 — Q62 2N7002E — MBDATA2 [17,29]

[33] PDAT_SMB — Q13 2N7002E — CGDAT_SMB [2,12,13,25,31,34]
R263 10K/F_4
+3V — R250 10K/F_4
[33] PCLK_SMB — Q12 2N7002E — CGCLK_SMB [2,12,13,25,31,34]

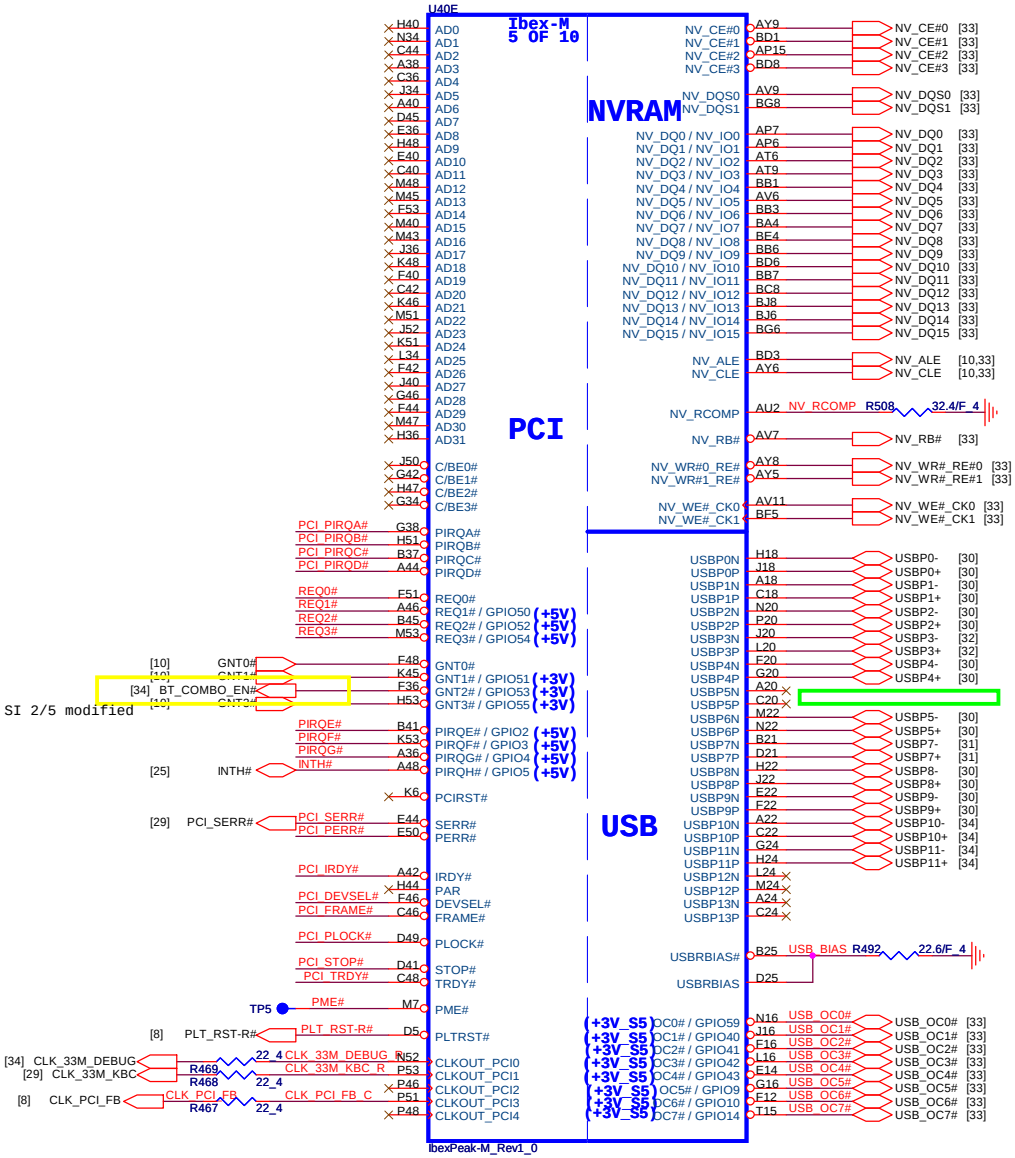
+3VS5
U19 *MC74VHC1G08DFT2G
C432 *.1U/10V_4
[9] PLT_RST-R# — PLT_RST-R# — PLTRST# [3,14,23,27,28,29,31,33,34]
R251 100K/F_4
R264 0_4
R262 *100K/F_4

XTAL25_IN — C671 *18P — Y2 *25MHZ — C670 *18P — XTAL25_OUT
R475 *1M

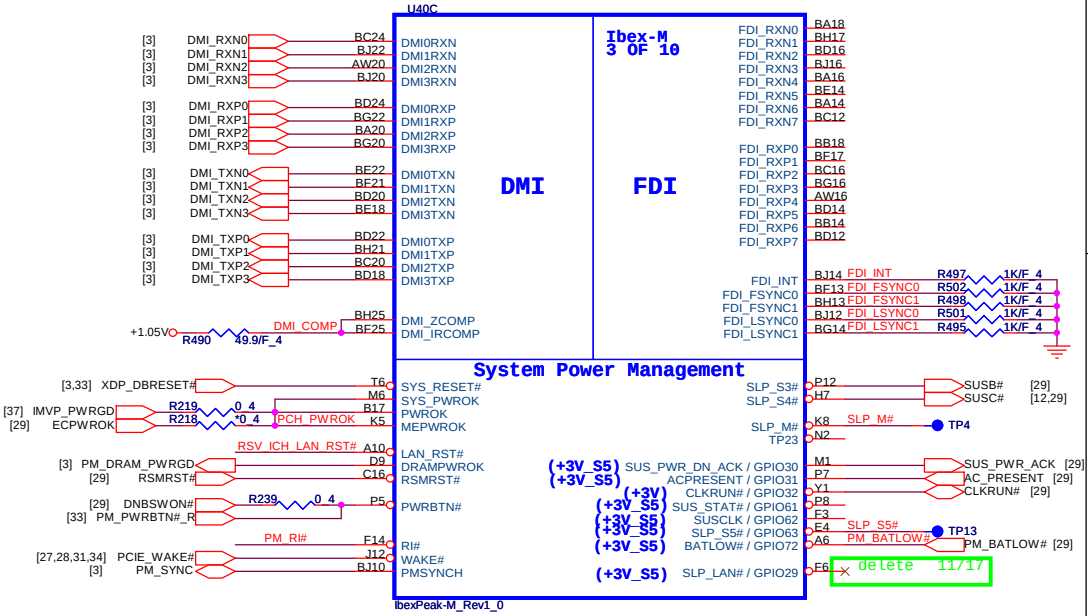
[2,7,9,11,14,15,16,28,29,33,36] +1.05V
[2,3,7,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,10,13,28,29,30,31,32,34,35,36,38,40,41] +3VPCU

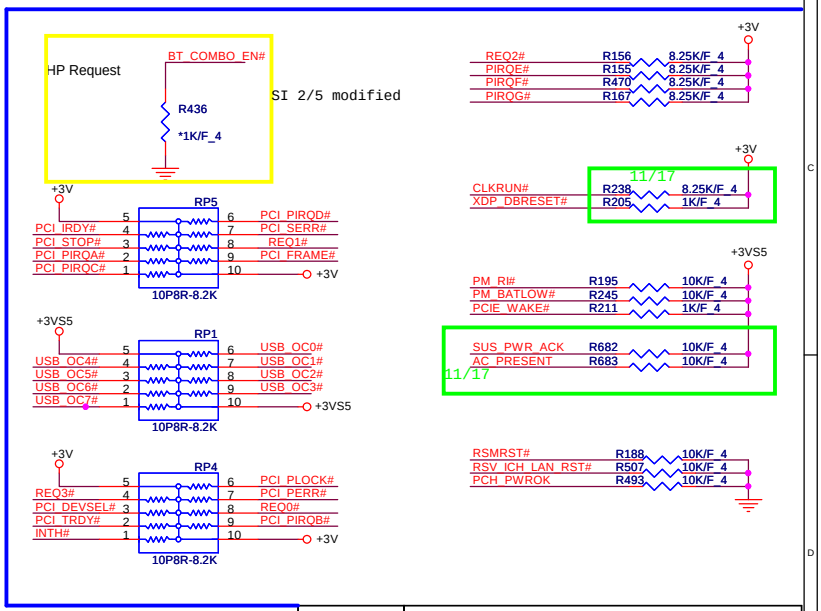
NB5	PROJECT : UP67 Quanta Computer Inc.	
Size Custom	Document Number PCH 3/6 (PCI,ONFI,USB,CK)	Rev 1A
Date: Friday, February 27, 2009	Sheet 8 of 45	

IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)





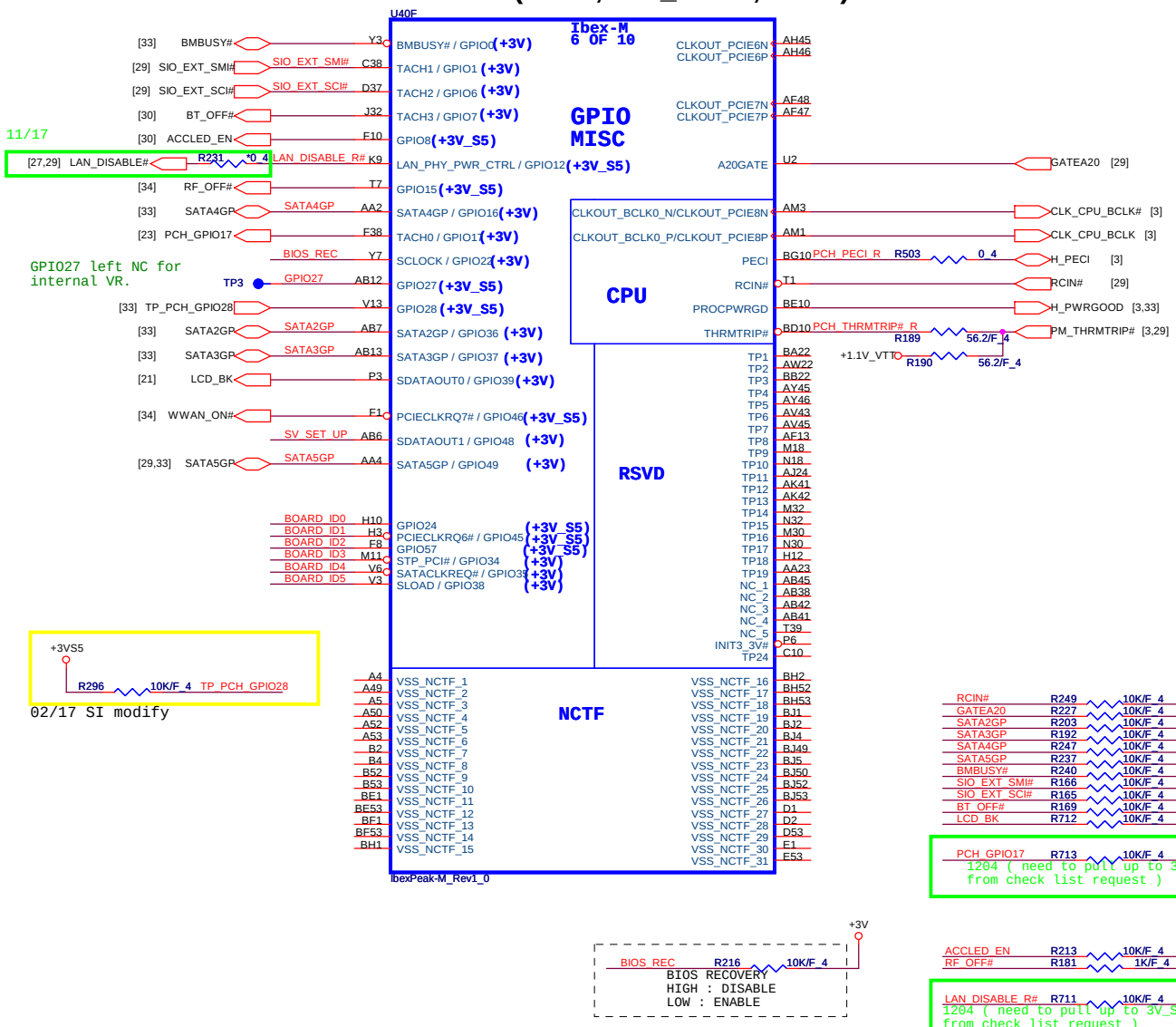
[2,7,8,11,14,15,16,28,29,33,36] +1.05V
[2,3,7,8,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[8,10,11,31,33,40] +3VS5

NB5

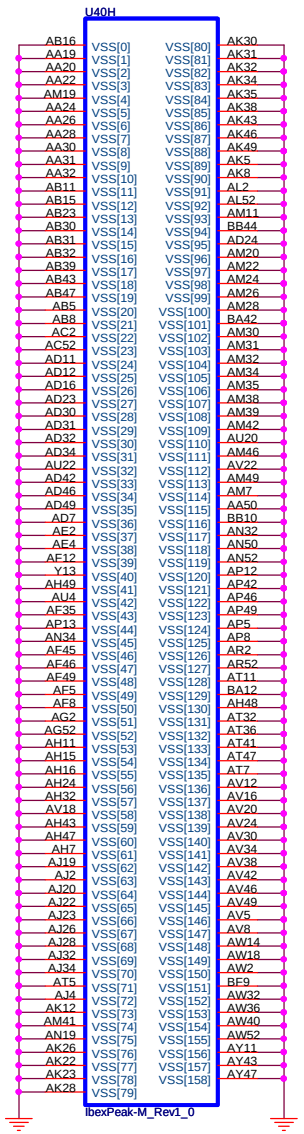
PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)/ Braidwood	1A
Date: Friday, February 27, 2009	Sheet 9 of 45	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



[9] GNT3# R472 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R223 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

[9] GNT0# R150 *1K/F_4
[9] GNT1# R471 *1K/F_4
BIOS boot from SPI
SI 2/5 modified

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

[9,33] NV_ALE R505 *1K/F_4
[9,33] NV_CLE R506 *1K/F_4
11/17
+1.8V

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

[7,24,25] SPKR SPKR *1K/F_4 R313 +3V
[7] PCH_GPIO33 R170 *100K/F_4
SI 2/5 modified

BOARD ID SETTING

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

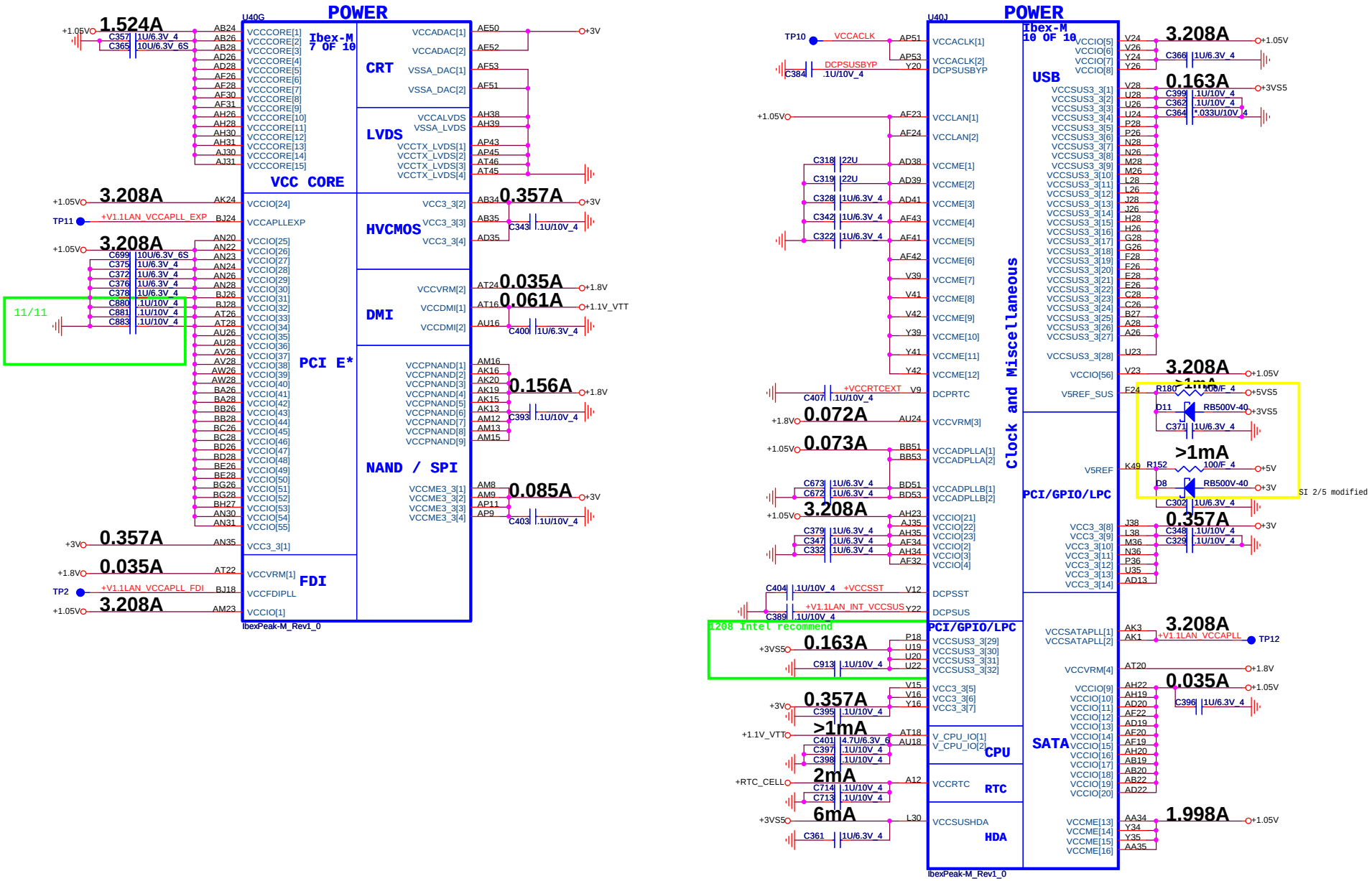
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UP6/7	0=UP6 1=UP7					
UMA/Dis.		0=UMA 1=Dis.				
Project name			00=Jones/Cujo 2.0 (Clarksfield) 10=Jones/Cujo 2.1 (Auburndale UMA)			
ROM Size					0= 2M 1= 4M	

+3VS5 +3V
R233 RU0 *10K/F_4 BOARD_ID0 R232 RD0 10K/F_4
R242 RU1 10K/F_4 BOARD_ID1 R224 RD1 *10K/F_4
R222 RU2 10K/F_4 BOARD_ID2 R208 RD2 10K/F_4
R207 RU3 *10K/F_4 BOARD_ID3 R206 RD3 10K/F_4
R214 RU4 *10K/F_4 BOARD_ID4 R215 RD4 10K/F_4
R226 RU5 *10K/F_4 BOARD_ID5 R225 RD5 10K/F_4

[3,5,11,33,37,38] +1.1V_VTT
[5,11,16,33,36,40] +1.8V
[2,3,7,8,9,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[8,9,11,31,33,40] +3VS5

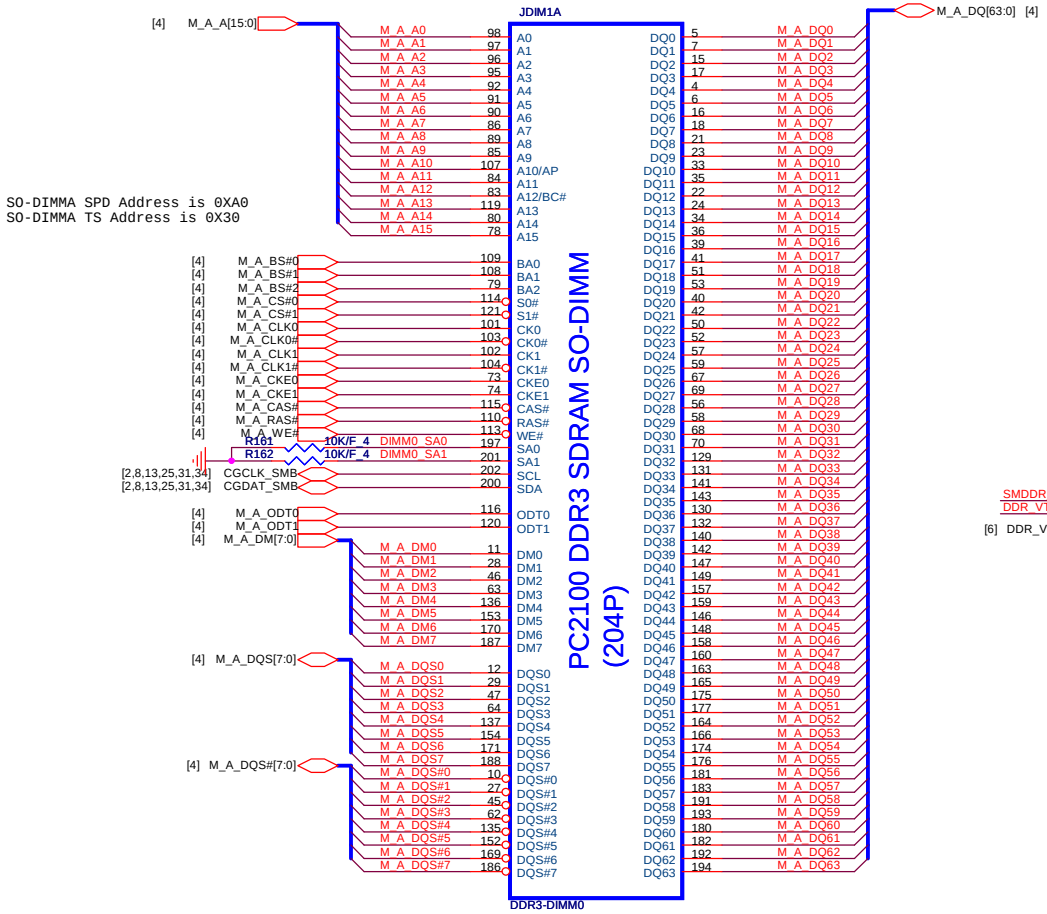
PROJECT : UP67
Quanta Computer Inc.

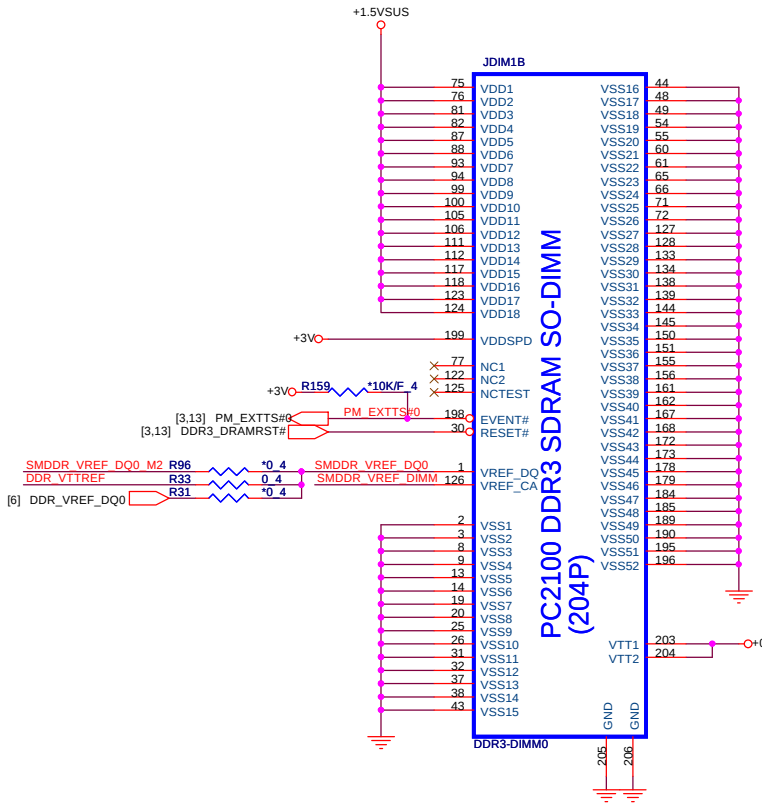
Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	1A
NB5	Date: Friday, February 27, 2009	Sheet 10 of 45

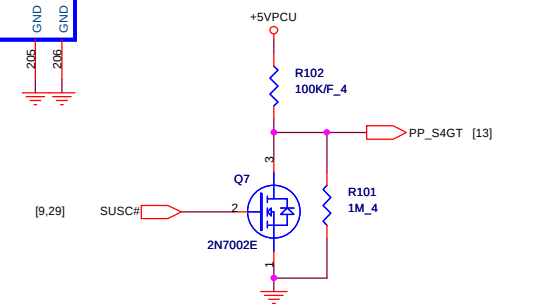


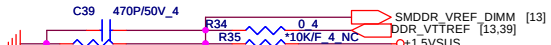
[2,7,8,9,14,15,16,28,29,33,36] +1.05V
[3,5,10,33,37,38] +1.1V_VTT
[5,10,16,33,36,40] +1.8V
[2,3,7,8,9,10,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[8,9,10,31,33,40] +3VS5
[21,22,24,25,30,31,32,34,40] +5V
[40] +5VS5

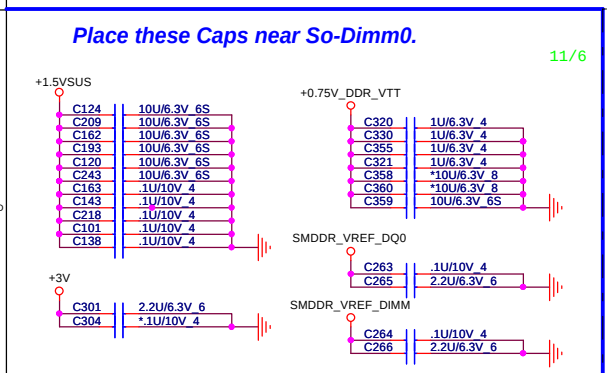
NB5	PROJECT : UP67 Quanta Computer Inc.	
Size Custom	Document Number PCH 5/6 (POWER)	Rev 1A
Date: Friday, February 27, 2009	Sheet 11 of 45	

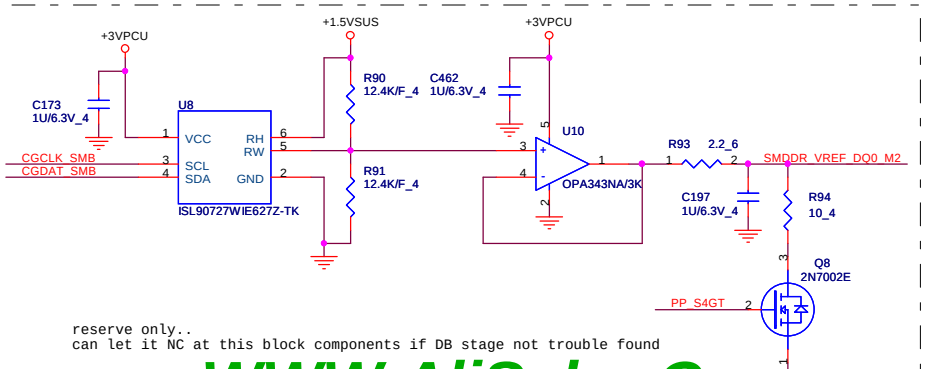










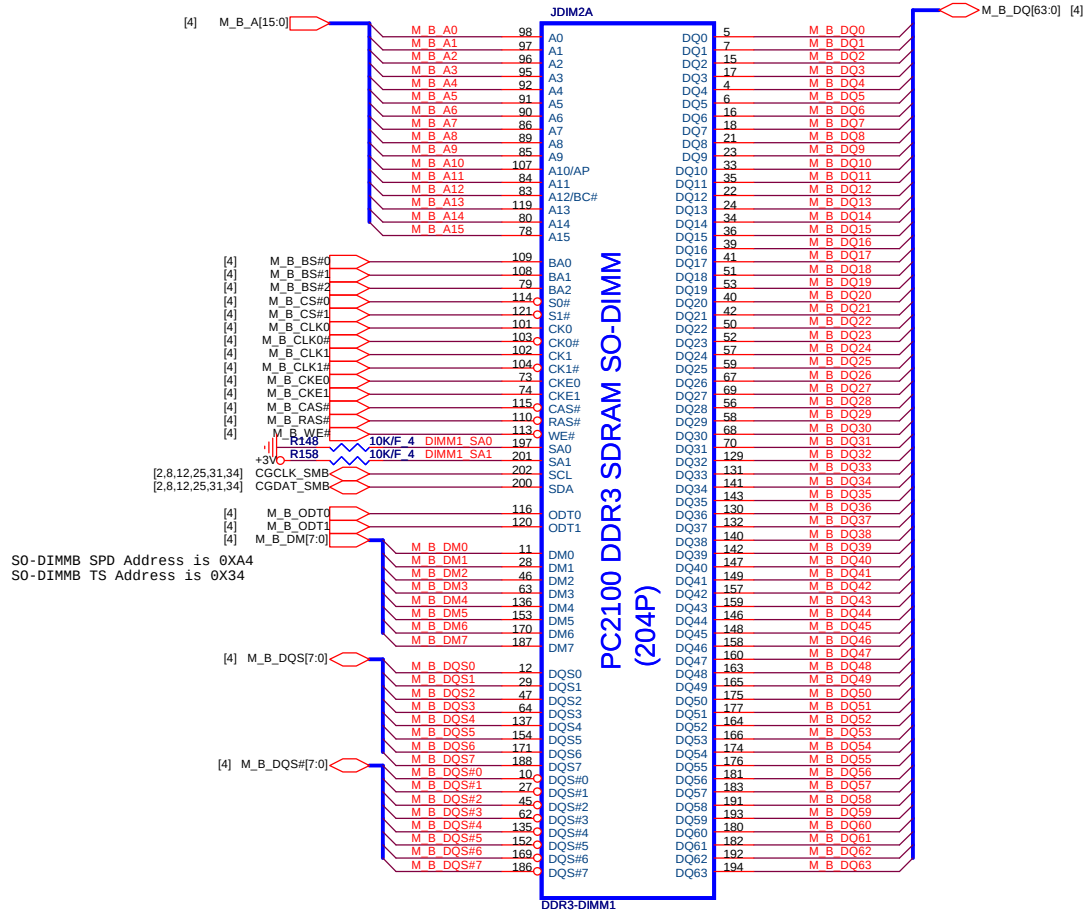


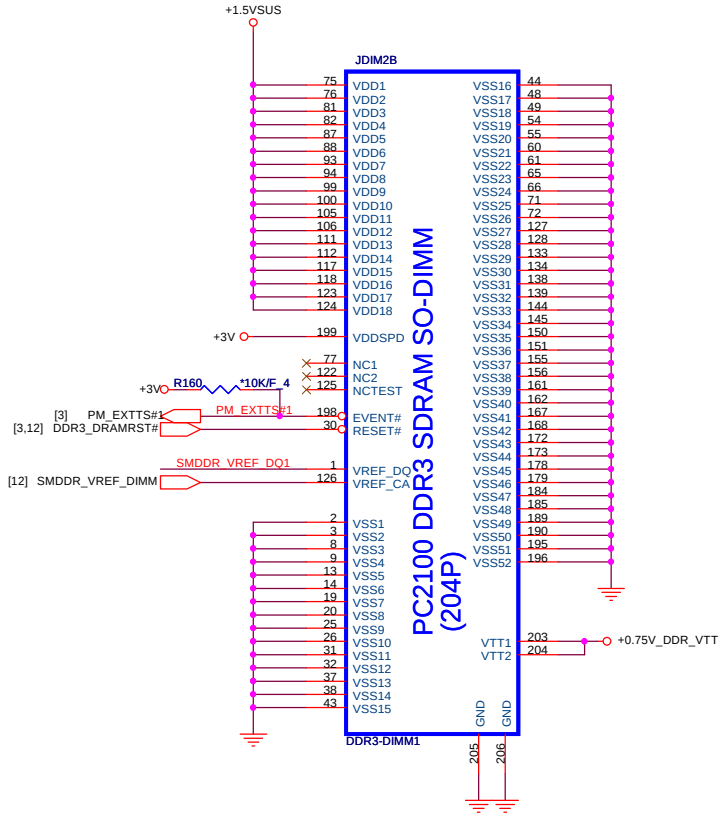
[13,39] +0.75V_DDR_VTT
[3,5,13,39] +1.5VSUS
[2,3,7,8,9,10,11,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,13,21,29,30,31,32,34,35,36,38,40,41] +3VPCU
[24,25,29,31,35,36,37,38,39,40] +5VPCU

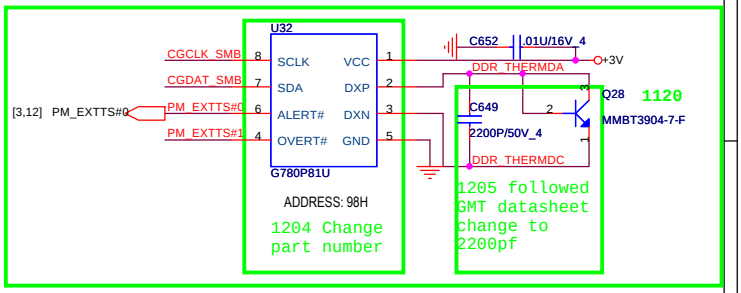
NB5

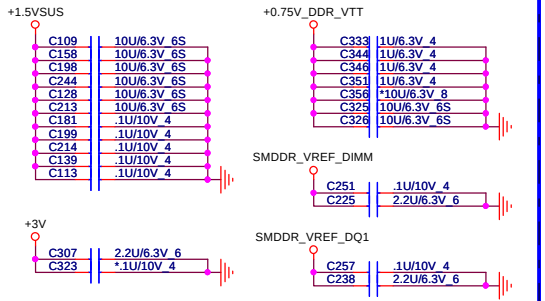
PROJECT : UP67
Quanta Computer Inc.

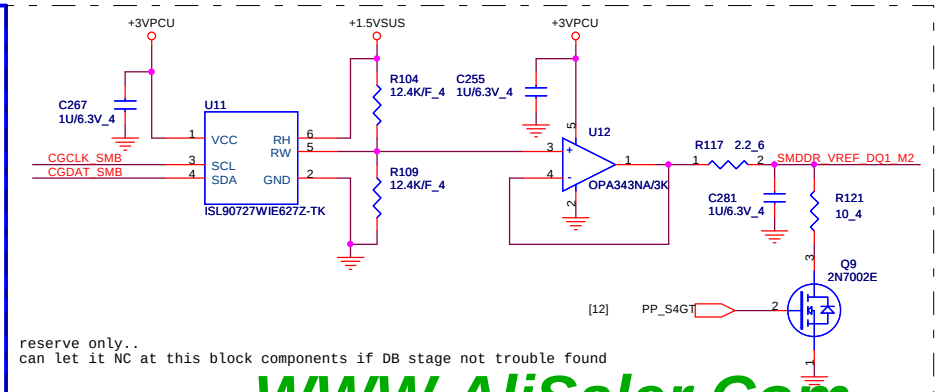
Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A
Date: Friday, February 27, 2009	Sheet 12 of 45	











[12,39] +0.75V_DDR_VTT
[3,5,12,39] +1.5VSUS
[2,3,7,8,9,10,11,12,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,12,21,29,30,31,32,34,35,36,38,40,41] +3VPCU
[12,24,25,29,31,35,36,37,38,39,40] +5VPCU

PROJECT : UP67
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

Date: Friday, February 27, 2009 Sheet 13 of 45

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

Near BGA

11/4

SI 2/13 modified

C116 & C788 close to chip

11/12

12~16 mils width
110mA

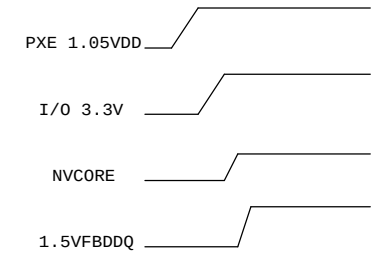
11/10 for placement

SI 2/13 modified

PCI EXPRESS

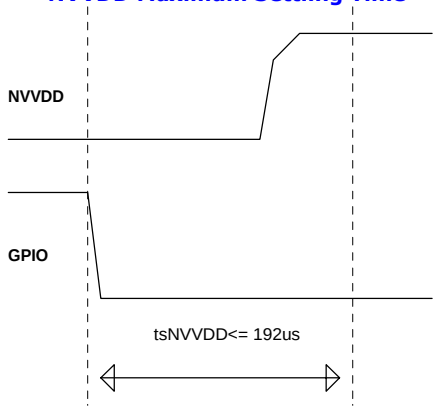
U35A
BGA969-NVIDIA-NB9P-GS
COMMON

power up sequence

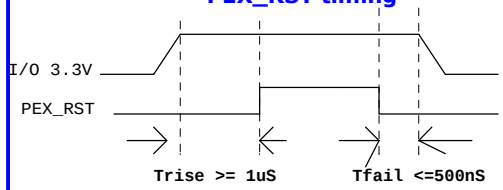


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



VGA Thermal Circuit

I2C ADDRESS: 0x98H

11/19

11/12

*MAX6649

THERMAL TRACE CONSTRAINTS
Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

10/10/10

11/19

1211 for Nvidia request
add transition cap

PROJECT : UP67	
Quanta Computer Inc.	
Size: Custom	Document Number: N10X (PCIE I/F) 1/5
Rev: 1A	
Date: Friday, February 27, 2009	Sheet 14 of 45

NB5

U35B
BGA969-NVIDIA-NB9P-GS
COMMON

12/02 modify
package for N10

MEMORY I/F A

Memory clk spread :
down 1.25% (
30~33KHZ)

use internal Vref, ext
divider no stuff

15mils width

For Debug only

SI 2/13 modified

U35C
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F C

12/16 Modified

11/4

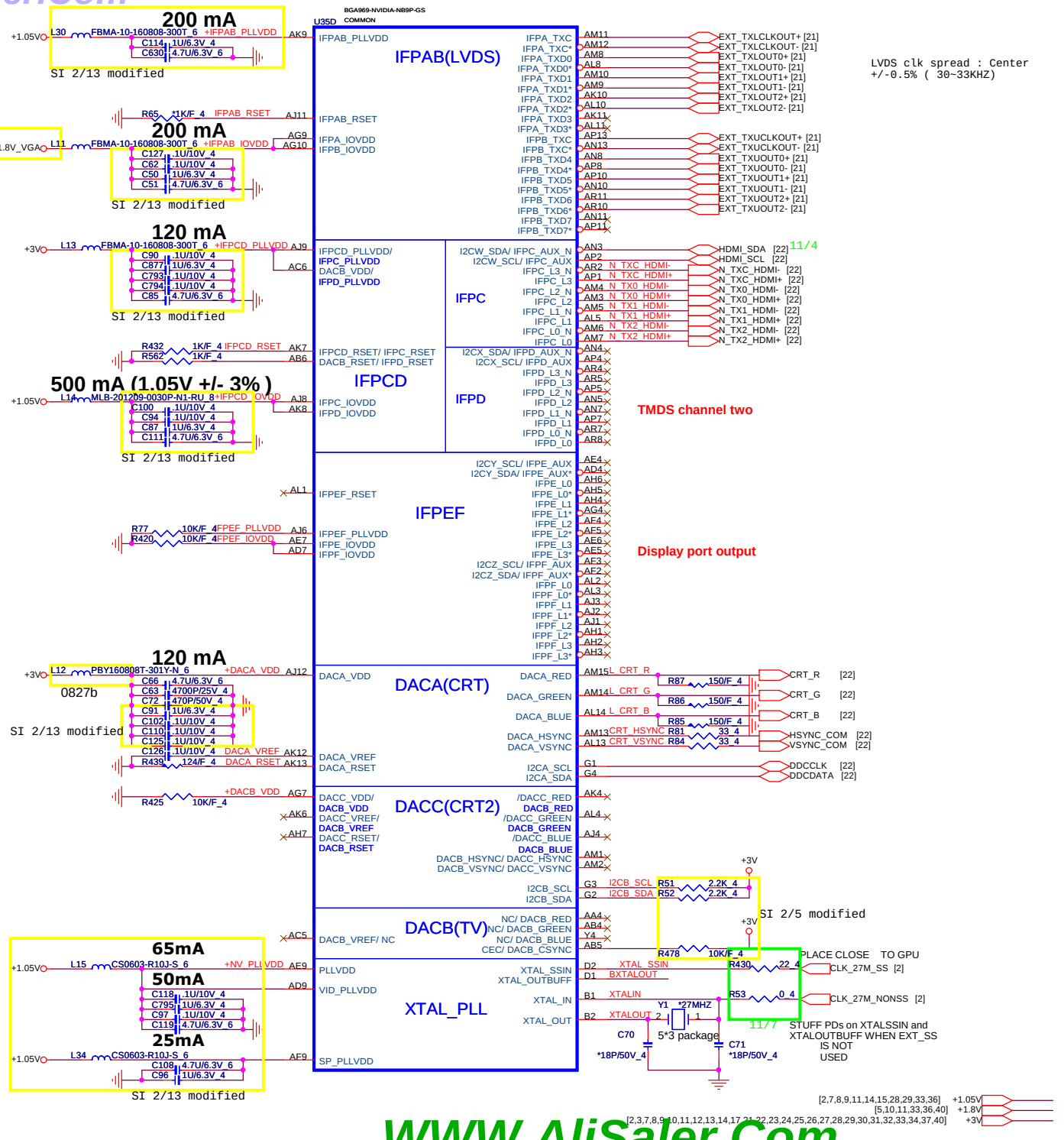
SI 2/5 Modified

R92 no stuff

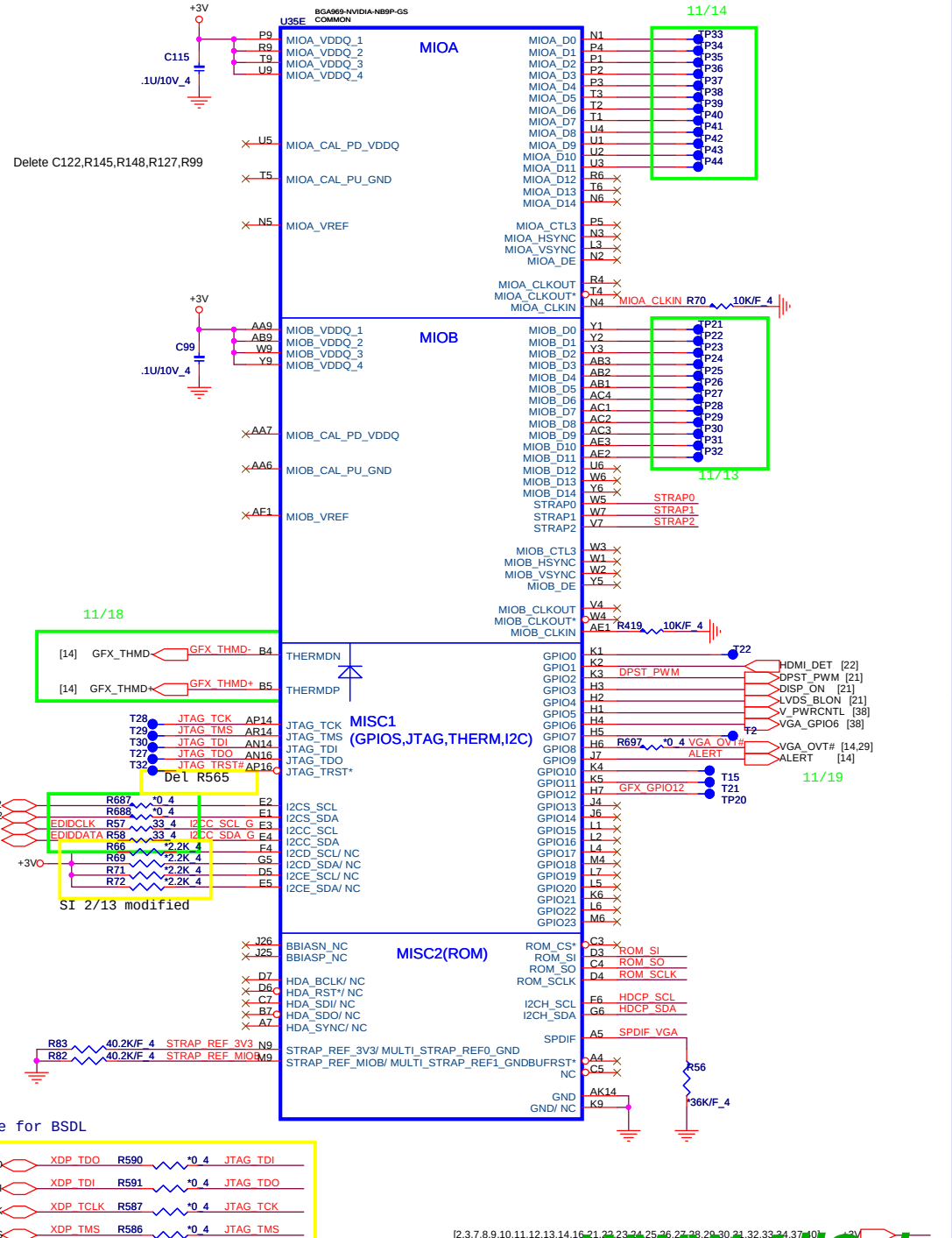
PROJECT : UP67
Quanta Computer Inc.

NB5

Size: Custom
Document Number: N10X (MEMORY I/F) 2/5
Rev: 1A
Date: Friday, February 27, 2009
Sheet 15 of 45



PROJECT : UP67	Quanta Computer Inc.
NB5	Size: Custom; Document Number: N10X (DISPLAY) 3/5; Rev: 2A
	Date: Friday, February 27, 2009; Sheet 16 of 45



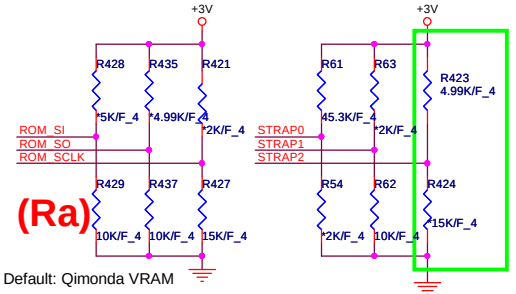
CHIP	PCI_DEVID:	STRAP2
N10P-GE	0x0A28	1000 PU 5K
N10M-GE	0x0A68	1000 PU 5K

SEE Datasheet for details on N10P Straps!

PCI_DEVID[4]/SUBVENDOR

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



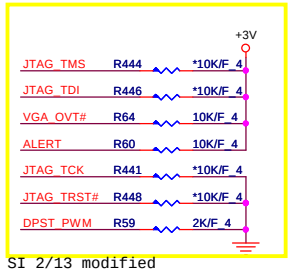
CS31002FB26 (RES CHIP 10K 1/16W +-1% (0402))
CS31502FB08 (RES CHIP 15K 1/16W +-1% (0402))
CS32002FB02 (RES CHIP 20K 1/16W +-1%(0402))

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

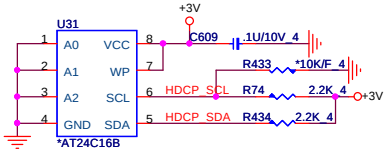
VRAM Configuration Table

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
AKD58GGT^01	0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
AKD5LZGTW00	0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
	0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
	0101		Reserved		
	0110				
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)



HDCP ROM



Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10X (GPIO & STRAPS) 4/5	2A
Date: Monday, March 02, 2009	Sheet 17 of 45	

U35F

BGA969-NVIDIA-NB9P-GS
COMMON

+VGACORE +VGACORE

NVVDD

AB11	VDD_001	VDD_057	P21	AD24	VDD_029
AB13	VDD_002	VDD_058	P23	L11	VDD_030
AB15	VDD_003	VDD_059	P25	L12	VDD_031
AB17	VDD_004	VDD_060	R11	L13	VDD_032
AB19	VDD_005	VDD_061	R12	L14	VDD_033
AB21	VDD_006	VDD_062	R13	L15	VDD_034
AB23	VDD_007	VDD_063	R14	L16	VDD_035
AB25	VDD_008	VDD_064	R15	L17	VDD_036
AC11	VDD_009	VDD_065	R16	L18	VDD_037
AC12	VDD_010	VDD_066	R17	L19	VDD_038
AC13	VDD_011	VDD_067	R18	L20	VDD_039
AC14	VDD_012	VDD_068	R19	L21	VDD_040
AC15	VDD_013	VDD_069	R20	L22	VDD_041
AC16	VDD_014	VDD_070	R21	L23	VDD_042
AC17	VDD_015	VDD_071	R22	L24	VDD_043
AC18	VDD_016	VDD_072	R23	L25	VDD_044
AC19	VDD_017	VDD_073	R24	M12	VDD_045
AC20	VDD_018	VDD_074	R25	M14	VDD_046
AC21	VDD_019	VDD_075	T12	M16	VDD_047
AC22	VDD_020	VDD_076	T14	M18	VDD_048
AC23	VDD_021	VDD_077	T16	M20	VDD_049
AC24	VDD_022	VDD_078	T18	M22	VDD_050
AC25	VDD_023	VDD_079	T20	M24	VDD_051
AD12	VDD_024	VDD_080	T22	P11	VDD_052
AD14	VDD_025	VDD_081	T24	P13	VDD_053
AD16	VDD_026	VDD_082	V11	P15	VDD_054
AD18	VDD_027	VDD_083	V13	P17	VDD_055
AD22	VDD_028	VDD_084	V15	P19	VDD_056

VDD_085	V17	VDD_096	W24
VDD_086	V19	VDD_097	W25
VDD_087	V21	VDD_098	Y12
VDD_088	V23	VDD_099	Y14
VDD_089	V25	VDD_100	Y16
VDD_090	W11	VDD_101	Y18
VDD_091	W12	VDD_102	Y20
VDD_092	W13	VDD_103	Y22
VDD_093	W14	VDD_104	Y24
VDD_094	W15	VDD_105	
VDD_095	W16	VDD_106	
VDD_096	W17	VDD_107	
VDD_097	W18	VDD_108	
VDD_098	W19	VDD_109	
VDD_099	W20	VDD_110	
VDD_100	W21	VDD_111	
VDD_101	W22		
VDD_102	W23		
VDD_103	W24		
VDD_104	W25		
VDD_105	Y12		
VDD_106	Y14		
VDD_107	Y16		
VDD_108	Y18		
VDD_109	Y20		
VDD_110	Y22		
VDD_111	Y24		

02/16 SI modify

NVVDD Decoupling

PLACE NEAR BALLS

+VGACORE

C74	*4.7U/6.3V_6	
C155	1U/6.3V_4	
C73	.22U/25V_6	
C135	.22U/25V_6	
C134	1U/10V_4	
C215	.022U/16V_4	
C201	.022U/16V_4	
C140	.022U/16V_4	
C164	.022U/16V_4	
C200	.047U/16V_4	
C182	.047U/16V_4	
C216	.047U/16V_4	
C169	.01U/16V_4	
C183	.01U/16V_4	
C184	.01U/16V_4	
C217	.01U/16V_4	
C132	.01U/16V_4	
C185	.01U/16V_4	
C203 2	1 4700P/25V_4	
C202 2	1 4700P/25V_4	
C78	330U/2.5V_6032	

U35G

BGA969-NVIDIA-NB9P-GS
COMMON

GROUND

AA11	GND_1	GND_096	E15	AD2	GND_31
AA12	GND_2	GND_097	E18	AD21	GND_32
AA13	GND_3	GND_098	E24	AD23	GND_33
AA14	GND_4	GND_099	E27	AD25	GND_34
AA15	GND_5	GND_100	E30	AD31	GND_35
AA16	GND_6	GND_101	E6	AD34	GND_36
AA17	GND_7	GND_102	E9	AD5	GND_37
AA18	GND_8	GND_103	F2	AE11	GND_38
AA19	GND_9	GND_104	F31	AE12	GND_39
AA2	GND_10	GND_105	F34	AE13	GND_40
AA20	GND_11	GND_106	F5	AE14	GND_41
AA21	GND_12	GND_107	J2	AE15	GND_42
AA22	GND_13	GND_108	J31	AE16	GND_43
AA23	GND_14	GND_109	J34	AE17	GND_44
AA24	GND_15	GND_110	J5	AE18	GND_45
AA25	GND_16	GND_111	L9	AE19	GND_46
AA34	GND_17	GND_112	M11	AE20	GND_47
AA5	GND_18	GND_113	M13	AE21	GND_48
AB12	GND_19	GND_114	M15	AE22	GND_49
AB14	GND_20	GND_115	M17	AE23	GND_50
AB16	GND_21	GND_116	M19	AE24	GND_51
AB18	GND_22	GND_117	M2	AE25	GND_52
AB20	GND_23	GND_118	M21	AG2	GND_53
AB22	GND_24	GND_119	M23	AG31	GND_54
AB24	GND_25	GND_120	M25	AG34	GND_55
AC9	GND_26	GND_121	M31	AG5	GND_56
AD11	GND_27	GND_122	M34	AK2	GND_57
AD13	GND_28	GND_123	M5	AK31	GND_58
AD15	GND_29	GND_124	N11	AK34	GND_59
AD17	GND_30	GND_125	N12	AK5	GND_60

AL12	GND_61	GND_156	T25	AP30	GND_78
AL15	GND_62	GND_157	U11	AP33	GND_79
AL18	GND_63	GND_158	U12	AP6	GND_80
AL21	GND_64	GND_159	U13	AP9	GND_081
AL24	GND_65	GND_160	U14	B12	GND_082
AL27	GND_66	GND_161	U15	B15	GND_083
AL30	GND_67	GND_162	U16	B21	GND_084
AL6	GND_68	GND_163	U17	B24	GND_085
AL9	GND_69	GND_164	U18	B27	GND_086
AN2	GND_70	GND_165	U19	B3	GND_087
AN34	GND_71	GND_166	U20	B30	GND_088
AP12	GND_72	GND_167	U21	B33	GND_089
AP15	GND_73	GND_168	U22	B6	GND_090
AP18	GND_74	GND_169	U23	B9	GND_091
AP21	GND_75	GND_170	U24	C2	GND_092
AP24	GND_76	GND_171	U25	C34	GND_093
AP27	GND_77	GND_172	V12	E12	GND_094
AP3		GND_173	V14		GND_095
		GND_174	V16		
		GND_175	V18		
		GND_176	V2		
		GND_177	V20		
		GND_178	V22		
		GND_179	V24		
		GND_180	V31		
		GND_181	V5		
		GND_182	V9		
		GND_183	Y11		
		GND_184	Y13		
		GND_185	Y15		
		GND_186	Y17		
		GND_187	Y19		
		GND_188	Y21		
		GND_189	Y23		
		GND_190	Y25		
		GND_191			

Del all VRAM termination
(RP16~RP75)

SI 2/5 modified

[38] +VGACORE
[15,19,20,31,34,36,39,40] +1.5V

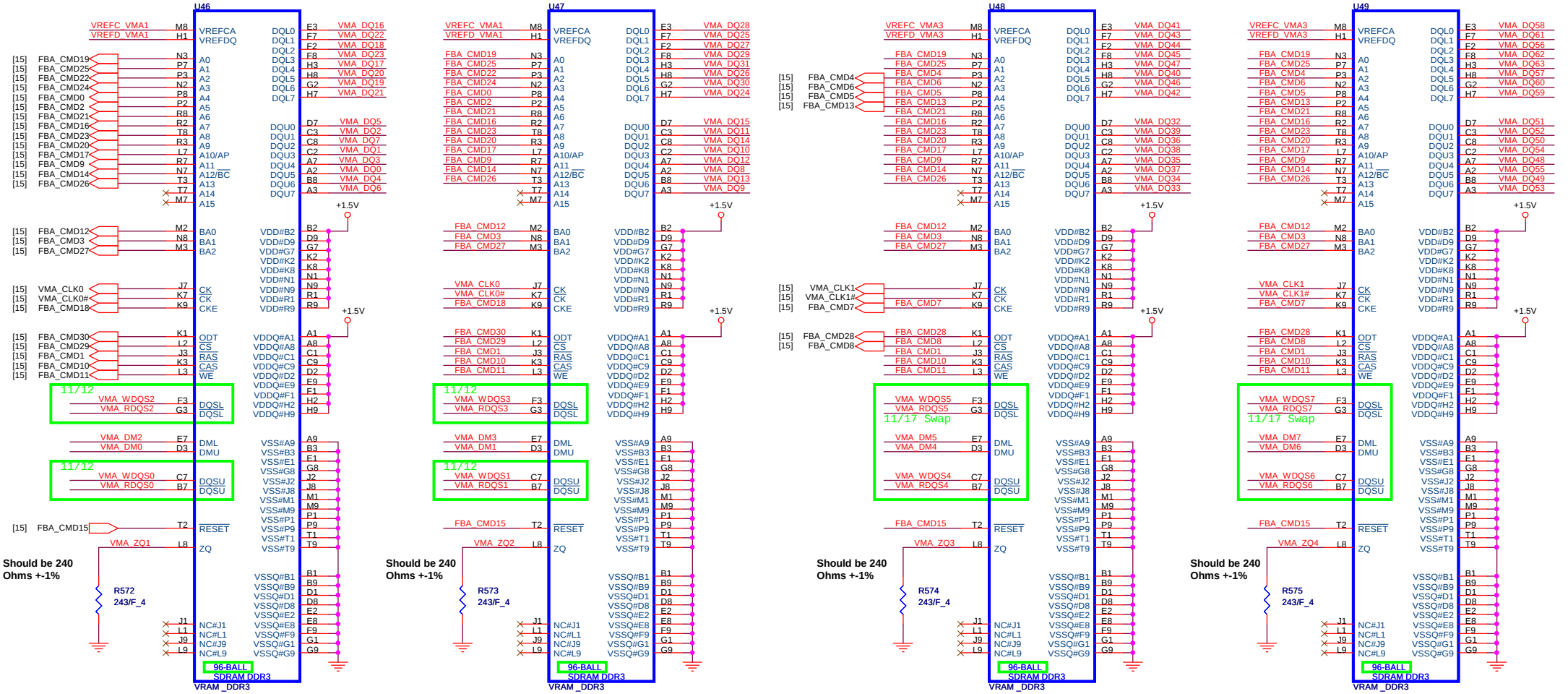
NB5

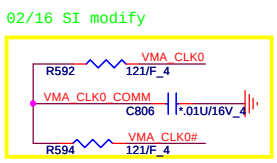
PROJECT : UP67
Quanta Computer Inc.

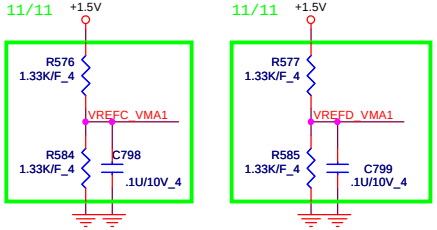
Size	Document Number	Rev
Custom	N10X (POWER & GND) 5/5	2A
Date: Friday, February 27, 2009	Sheet 18 of 45	

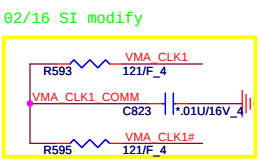
CHANNEL A: 256MB/512MB DDR3

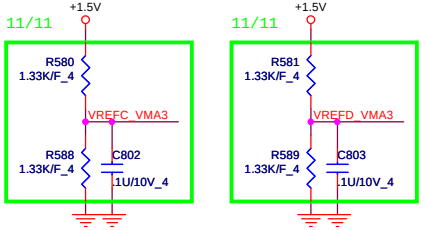
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

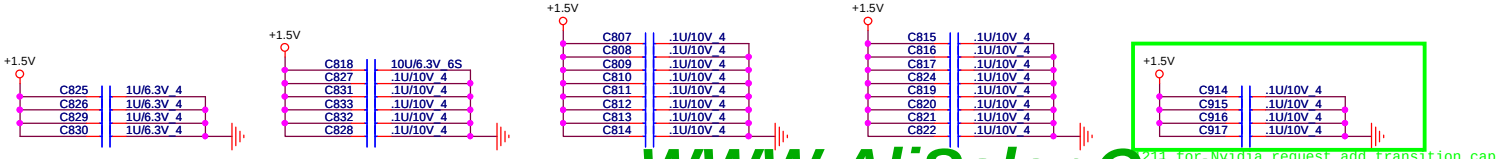












[15,20,31,34,36,39,40] +1.5V

2.1I for Nvidia request add transition cap

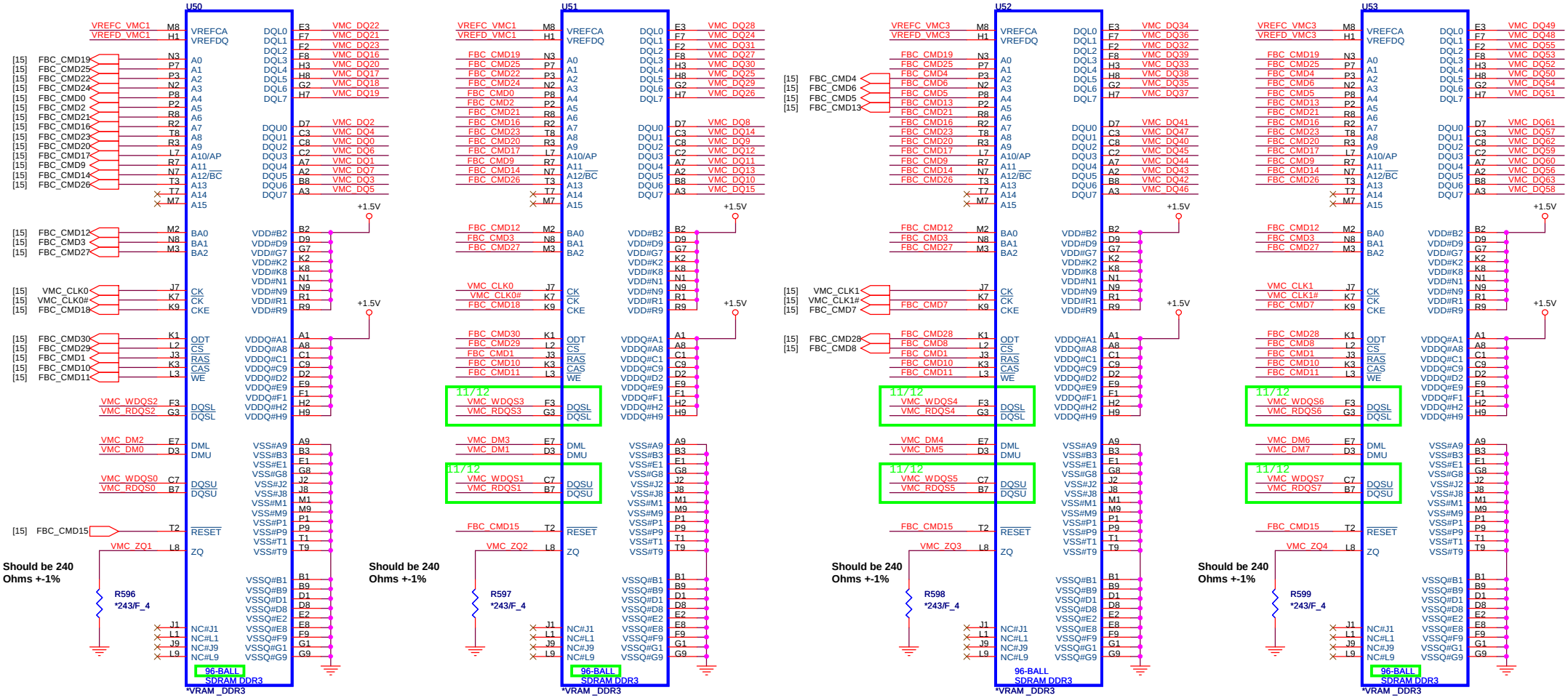
PROJECT : UP67
Quanta Computer Inc.

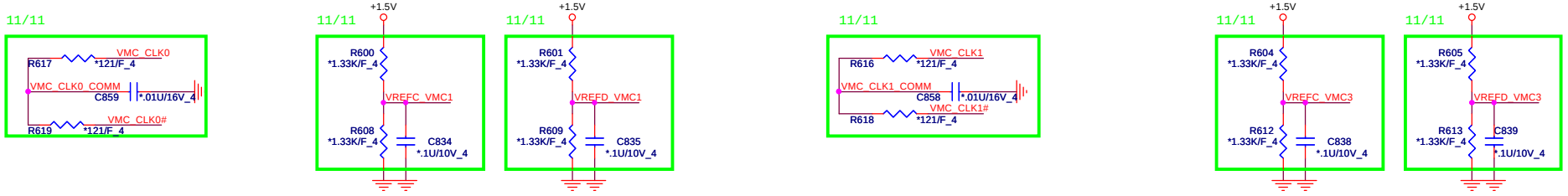
Size	Document Number	Rev
Custom	VRAM channel A	1A
Date: Friday, February 27, 2009	Sheet 19 of 45	

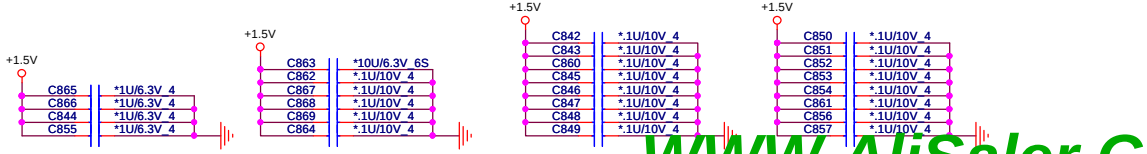
NB5

CHANNEL B: 256MB/512MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]







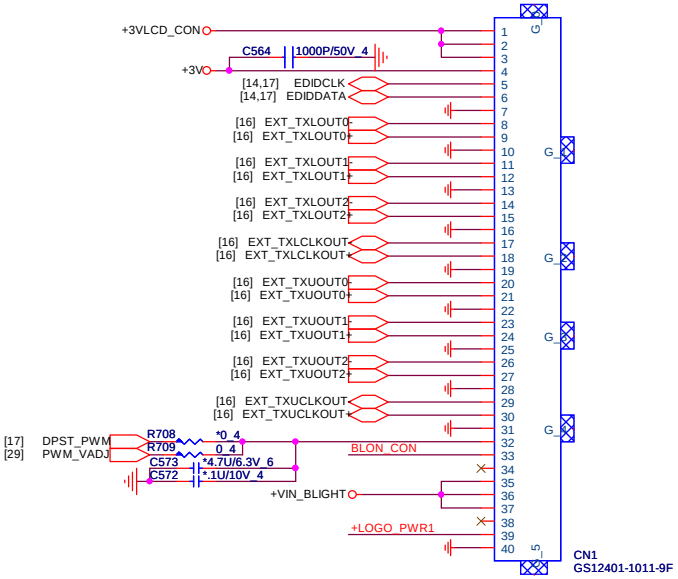
[15,19,31,34,36,39,40] +1.5V

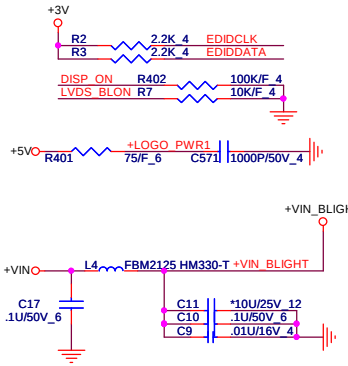
NB5

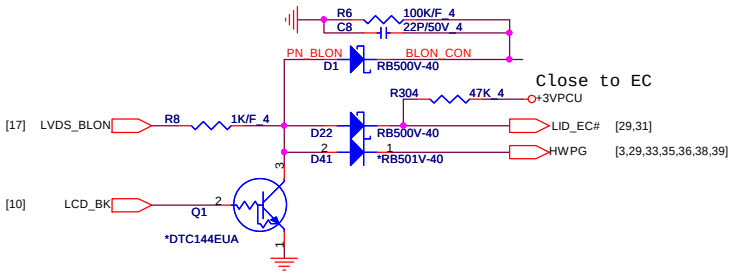
PROJECT : UP67
Quanta Computer Inc.

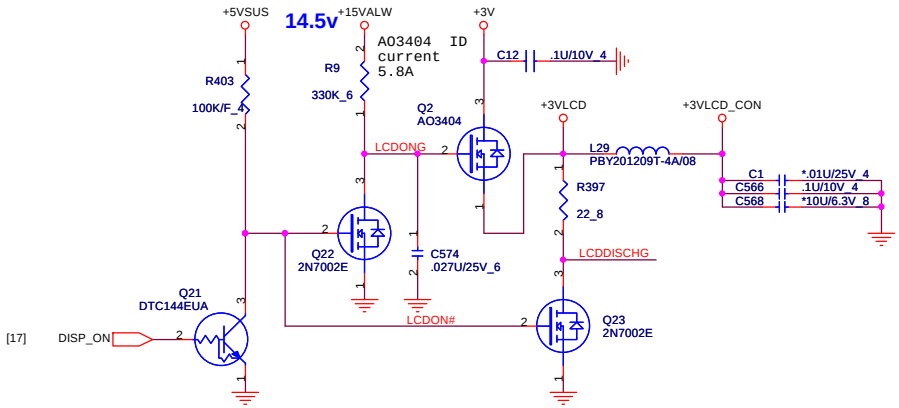
Size	Document Number	Rev
Custom	VRAM channel B	1A

Date: Friday, February 27, 2009 Sheet 20 of 45









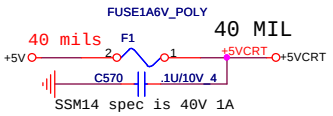
[2,3,7,8,9,10,11,12,13,14,16,17,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,12,13,29,30,31,32,34,35,36,38,40,41] +3VPCU
[11,22,24,25,30,31,32,34,40] +5V
[30,32,40] +5VSUS
[31,35,40] +15VALW
[26,32,35,36,37,38,39,40,41] +VIN

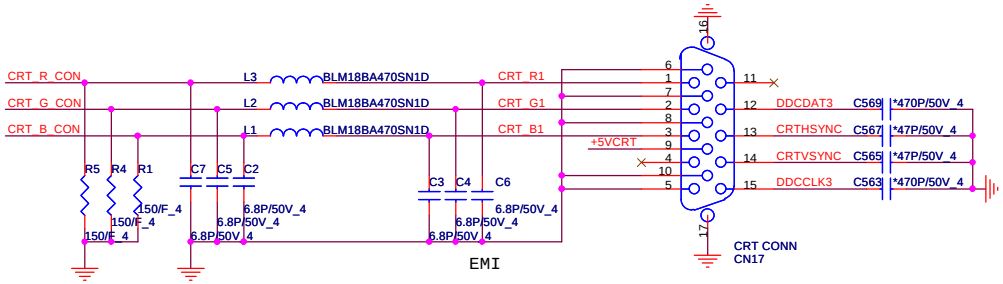
NB5

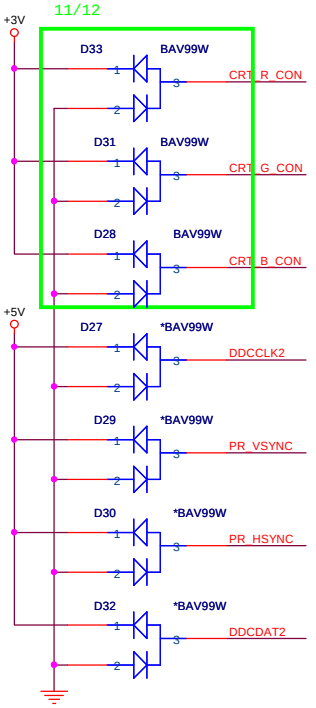
PROJECT : UP67
Quanta Computer Inc.

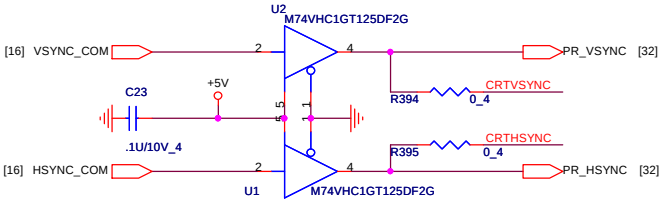
Size	Document Number	Rev
Custom	LCD CONN/LID function	1A
Date: Friday, February 27, 2009	Sheet 21 of 45	

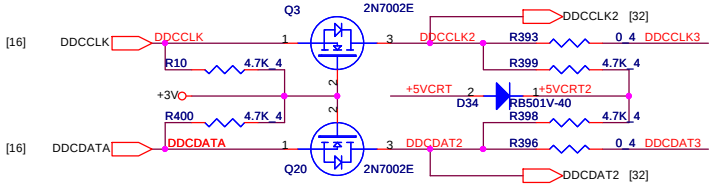
CRT PORT



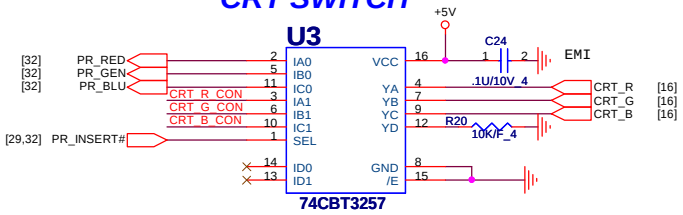






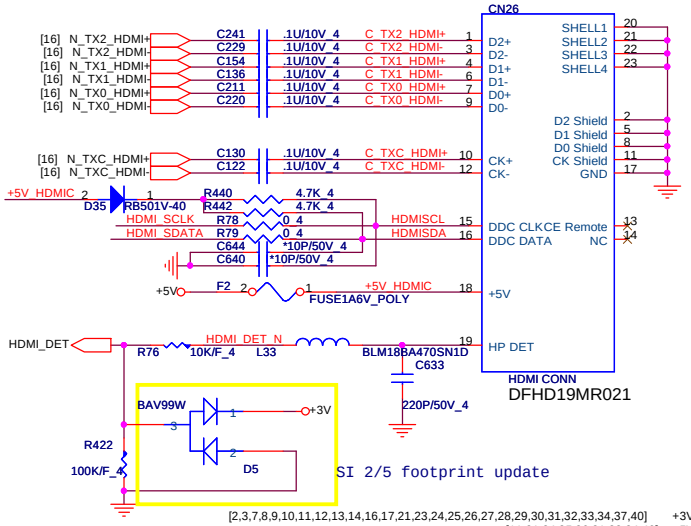


CRT SWITCH

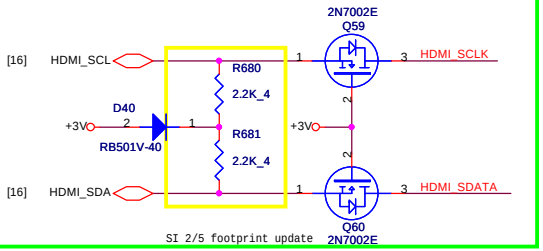


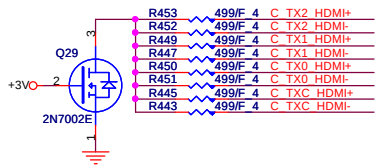
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

HDMI PORT



11/17 add level shift





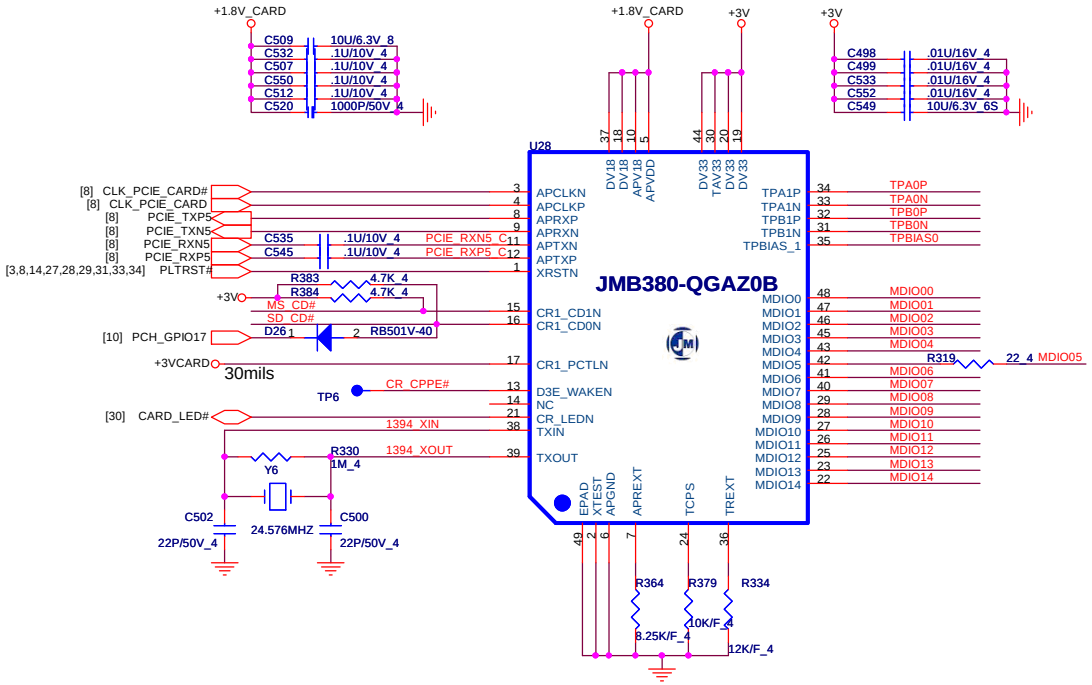
[2,3,7,8,9,10,11,12,13,14,16,17,21,23,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[11,21,24,25,30,31,32,34,40] +5V

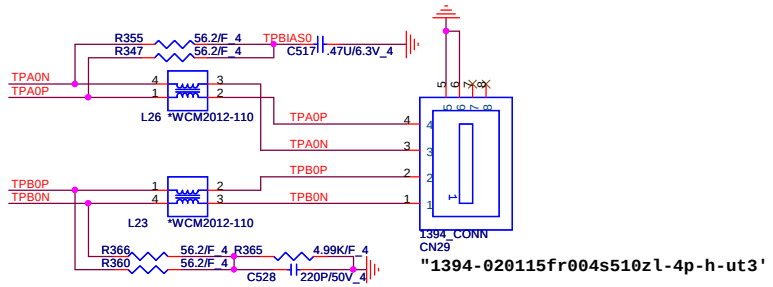
NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A

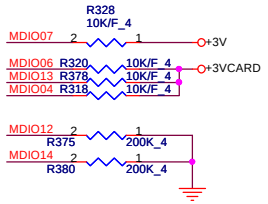
Date: Friday, February 27, 2009 Sheet 22 of 45



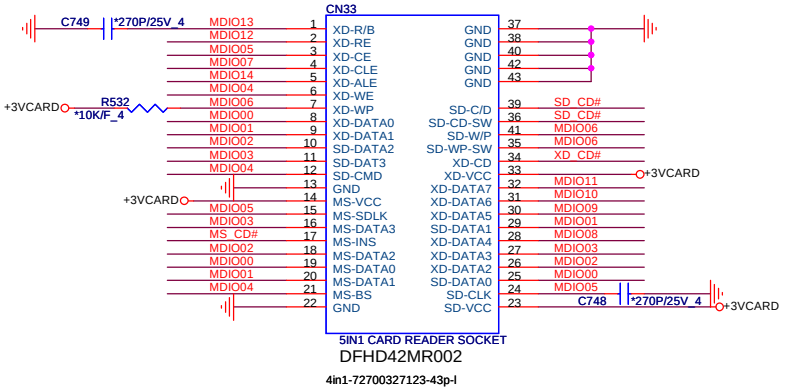


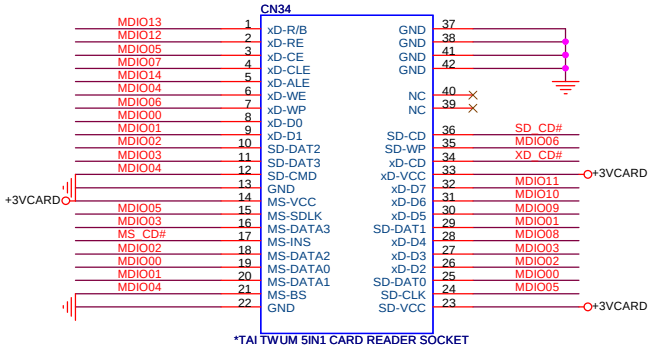
JMB 380 Note:

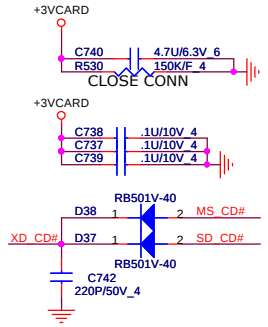
	SD/MMC	MS	XD
MDIO0	SD_DAT0	MS_D0	XD_D0
MDIO1	SD_DAT1	MS_D1	XD_D1
MDIO2	SD_DAT2	MS_D2	XD_D2
MDIO3	SD_DAT3	MS_D3	XD_D3
MDIO4	SD_CMD	MS_BS	XD_WE#
MDIO5	SD_CLK	MS_SCLK	XD_CE#
MDIO6	SD_WP		XD_WP#
MDIO7			XD_CLE
MDIO8	SD_DAT4		XD_D4
MDIO9	SD_DAT5		XD_D5
MDIO10	SD_DAT6		XD_D6
MDIO11	SD_DAT7		XD_D7
MDIO12			XD_RE#
MDIO13			XD_R/B#
MDIO14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#



5 IN1 CARD READER
XD,MMC/SD,MS/MSP



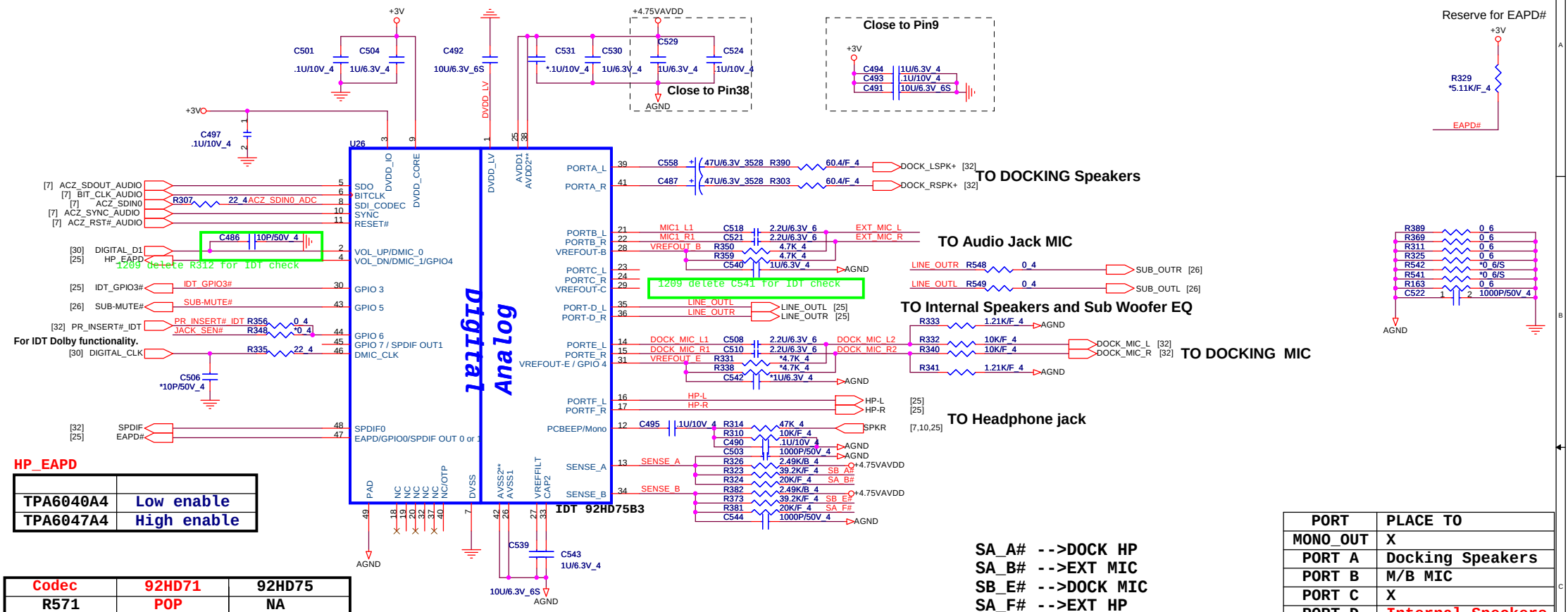




[2,3,7,8,9,10,11,12,13,14,16,17,21,22,24,25,26,27,28,29,30,31,32,33,34,37,40] +3V

NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: JMB380 & CR SOCKET	Rev: 1A
Date: Friday, February 27, 2009	Sheet 23 of 45	

1209 delete R321 for IDT check



HP_EAPD

TPA6040A4	Low enable
TPA6047A4	High enable

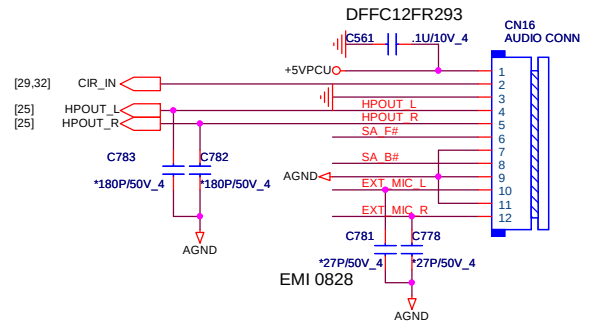
Codec	92HD71	92HD75
R571	POP	NA
C716	NA	POP
R449 R510	5.11K	2.49K

5.11K P/N: CS25112FB15

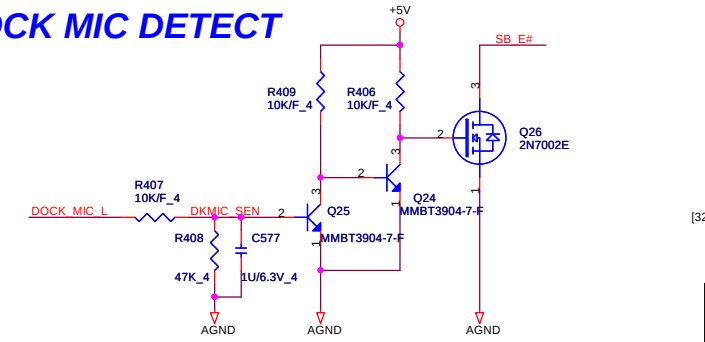
SA_A# -->DOCK HP
SA_B# -->EXT MIC
SB_E# -->DOCK MIC
SA_F# -->EXT HP
Audio JACK: Normal Open

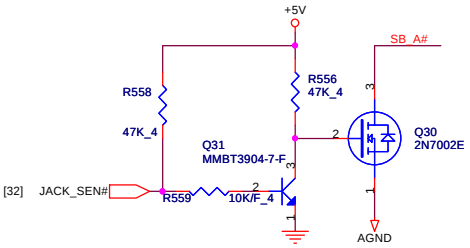
PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

TO AUDIO/B CON.



DOCK MIC DETECT

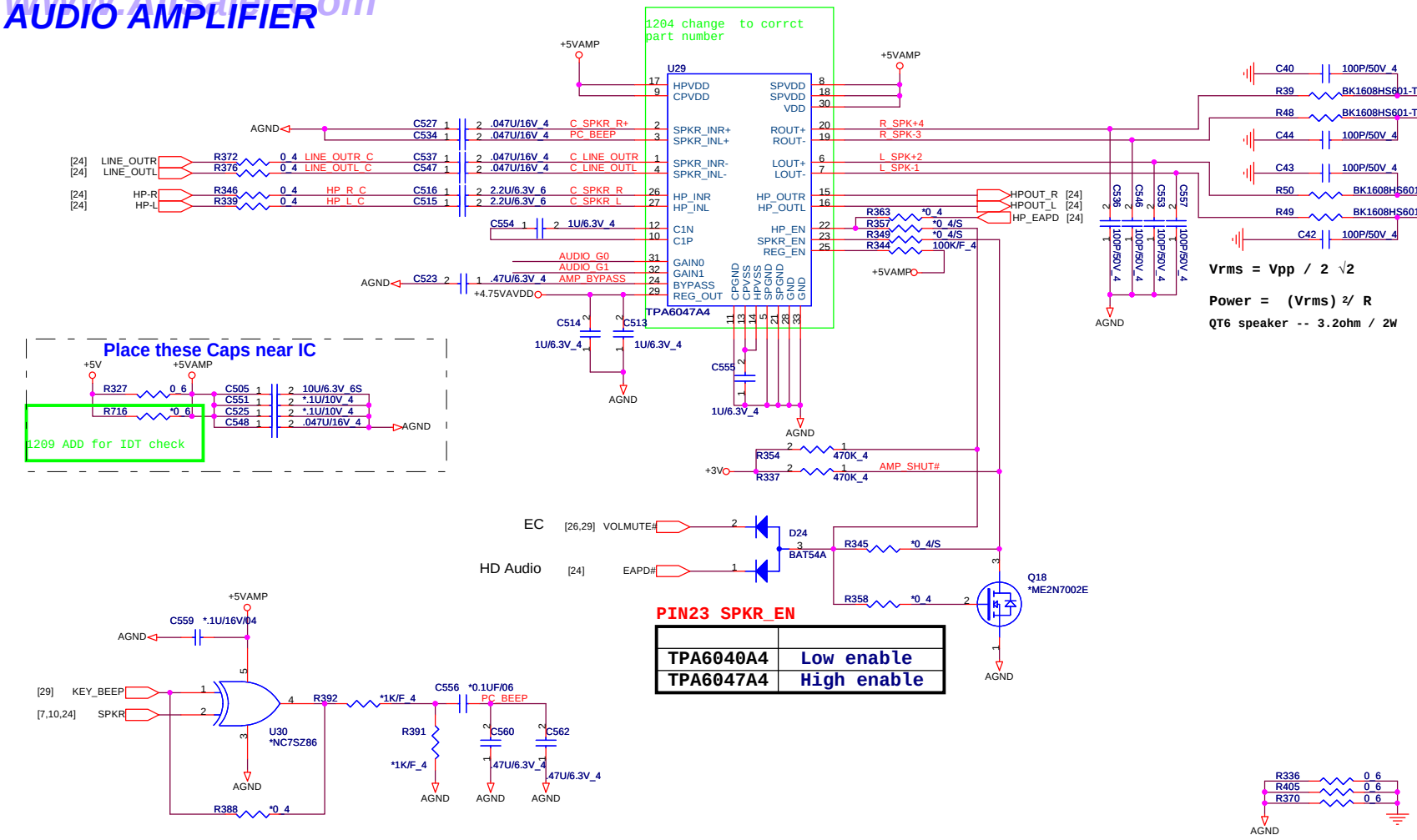




[25,26] +4.75VAVDD
[11,21,22,25,30,31,32,34,40] +5V
[12,25,29,31,35,36,37,38,39,40] +5VPCU
[7,9,11,13,16,17,23,27,28,29,30,31,32,33,34,37,40] +3V

NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: Azalia 92HD75	Rev: 1A
Date: Friday, February 27, 2009	Sheet 24 of 45	

AUDIO AMPLIFIER



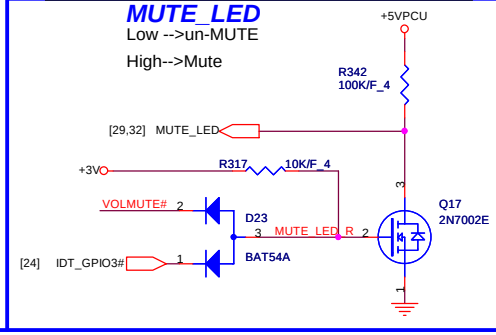
6040A4 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

MUTE_LED

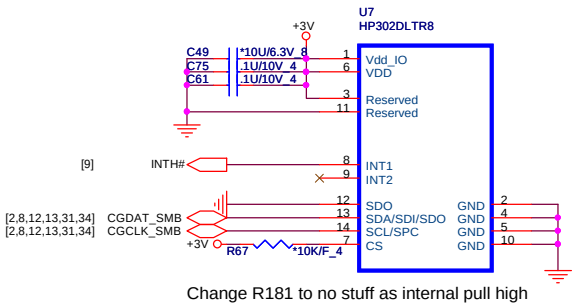
Low -->un-MUTE

High-->Mute



Accelerometer Sensor

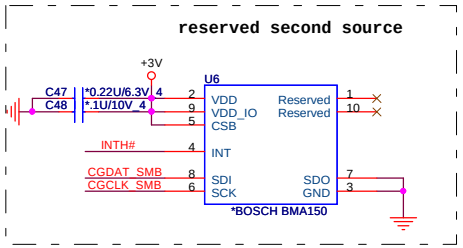
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



Change R181 to no stuff as internal pull high

Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex



[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,26,27,28,29,30,31,32,33,34,37,40] +3V
[11,21,22,24,30,31,32,34,40] +5V
[24,26] +4.75VAVDD
[26] +5VAMP

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6047/Accelerometer	1A

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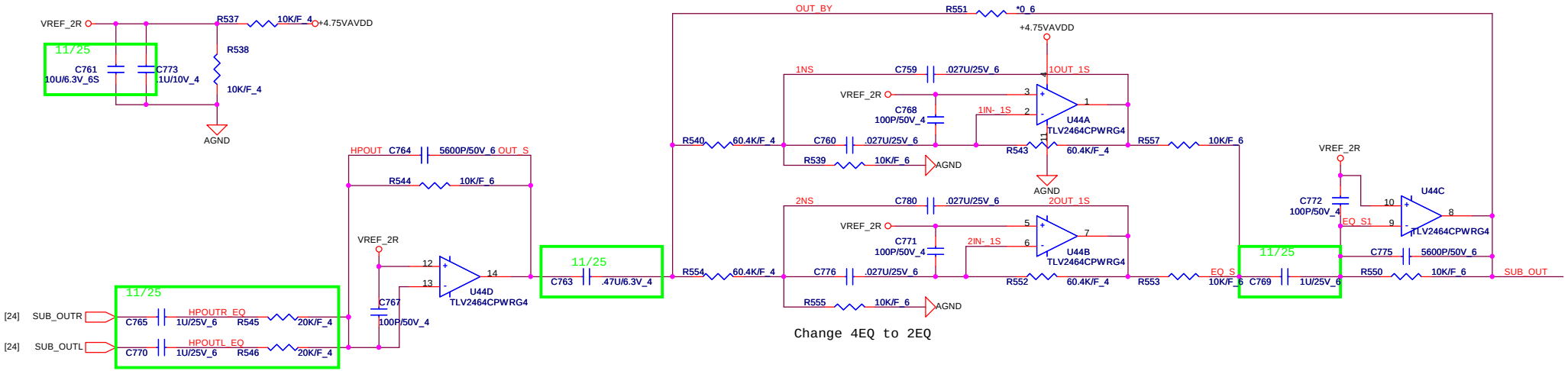
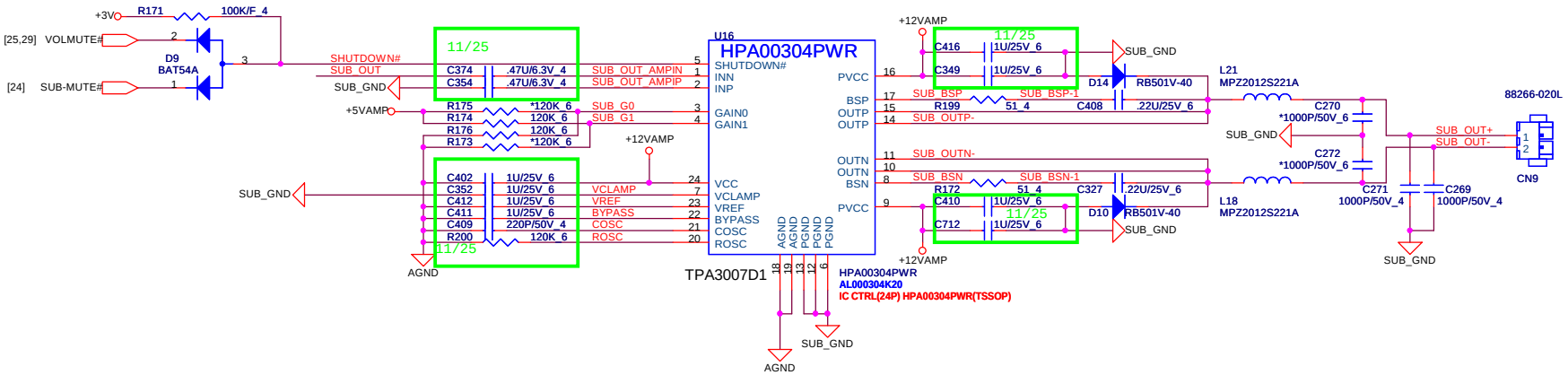
EQ FOR SUBWOOFER

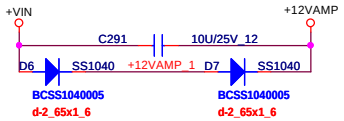


Change 4EQ to 2EQ

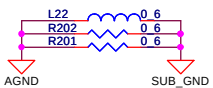
MODEL	UP7
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6



Sub-Woofer power



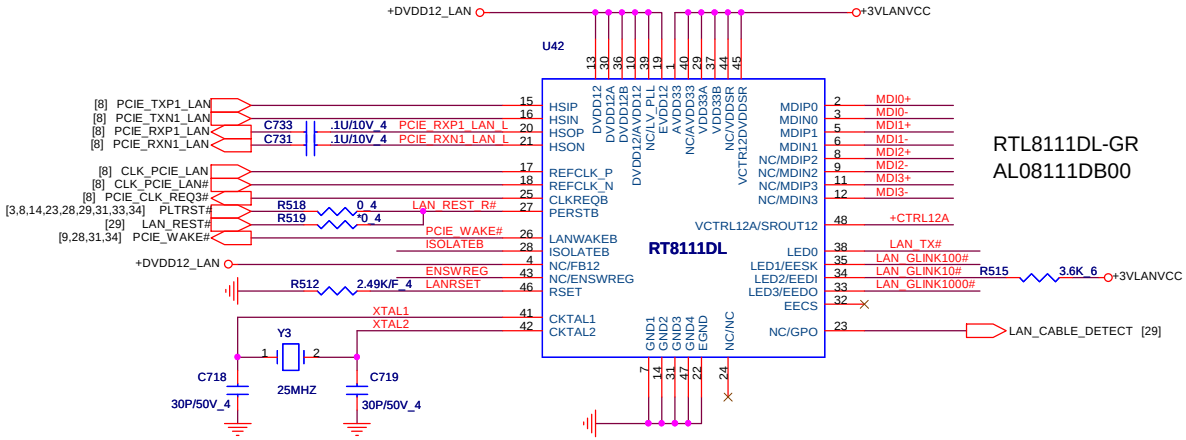
GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

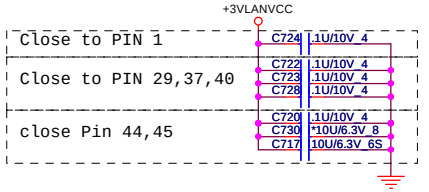


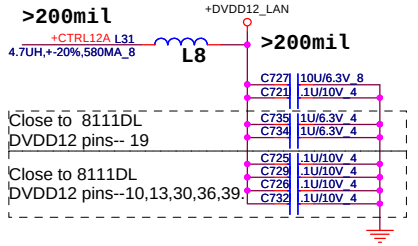
[24,25] +4.75VAVDD
[25] +5VAMP
[21,32,35,36,37,38,39,40,41] +VIN
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,27,28,29,30,31,32,33,34,37,40] +3V

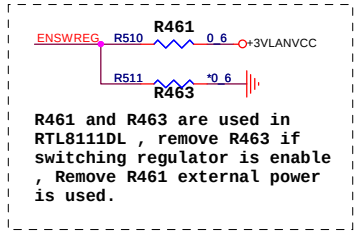
PROJECT : UP67
Quanta Computer Inc.

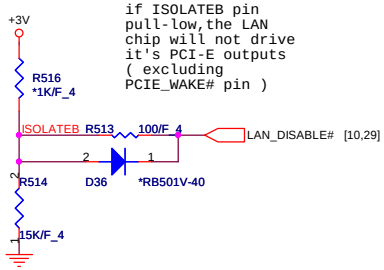
Size	Document Number	Rev
Custom	SUBWOOFER (EQ & AMP.)	1A
NB5	Date: Friday, February 27, 2009	Sheet 26 of 45



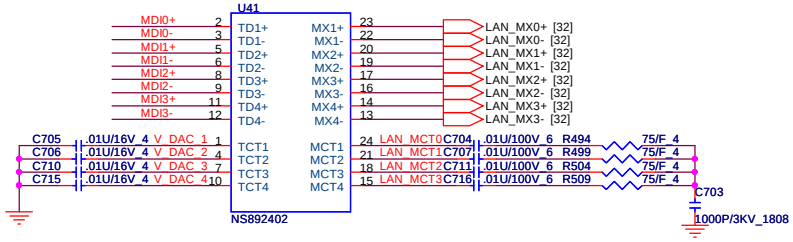




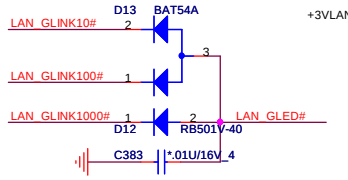


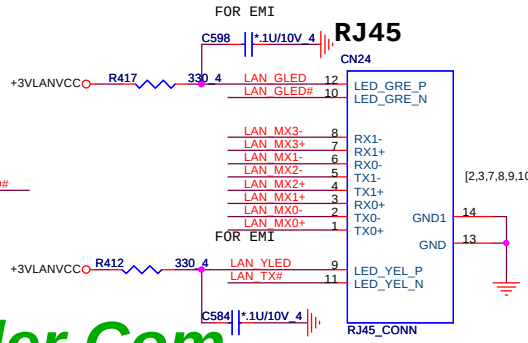


Transformer for 10/100/1000



Lan Con.





NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111DL/8103E/RJ45	1A

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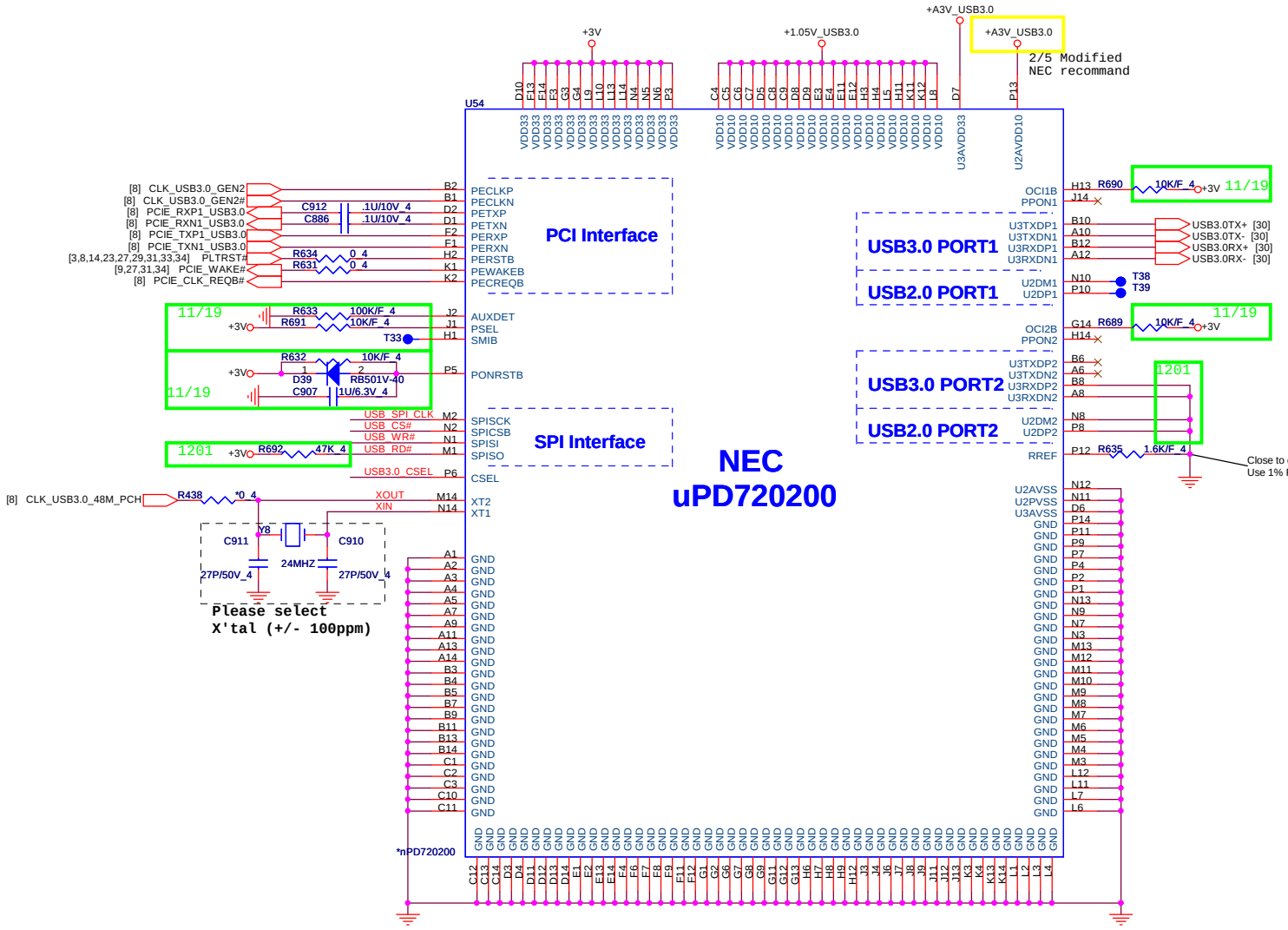
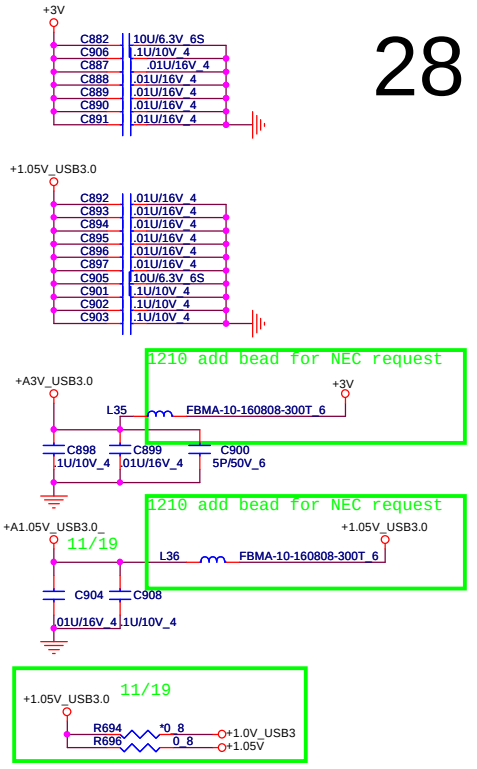
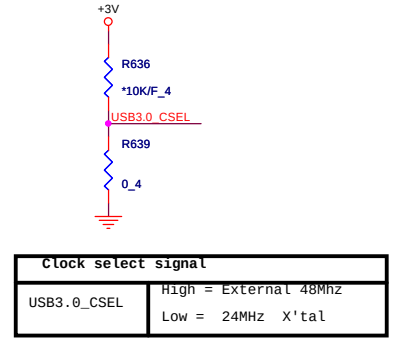
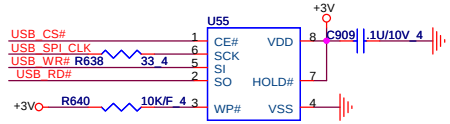






Clock select signal	
USB3.0_CSEL	High = External 48Mhz Low = 24MHz X'tal

Serial ROM IC



NEC recommends to use serial ROM IC "AT25Fxxx Series"

[2,7,8,9,11,14,15,16,29,33,36] +1.05V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,40] +3V

NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: NEC USB3.0 nPD720200	Rev: 1A
Date: Friday, February 27, 2009	Sheet 28 of 45	

1212 Change part number to VERSION D2

U23

KB3926QF D2

for Battery charge/charge and cap board

for VGA/CPU thermal

1206 EC add debug pin

1208 ADD cpu temp _alert# function

1211 EC add for SMT debug pin

SI 2/5 Modified

For KB3926 B, C version

for EMI

Fan table select

ID	Ra	Rb
UP6	10K	N/A
UP7	N/A	10K

adapter Type check

R273

64.9K -->65W CS36492FB17

33.2K -->90W CS33322FB13

Change to 1SS355 as Current loss

thermal shutdown circuit

adapter select for EC

Hi ==> 120W

Low ==> 65W/90W

512K byte SPI EC ROM

Socket: DG008000031

MXIC AKE3KZP0001

WINBOND AKE37ZN0N00

AMIT AKE38ZN0800

1208 ADD cpu temp _alert# function

Change to RB500 as Current loss

Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

Delete T10 and tie pin 117 from Lan for DSM

R430 Change to 100k ohm ,pull low

11/6 for EMI

PROJECT : UP67	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: KB3926/ROM/TP; Rev: 1A
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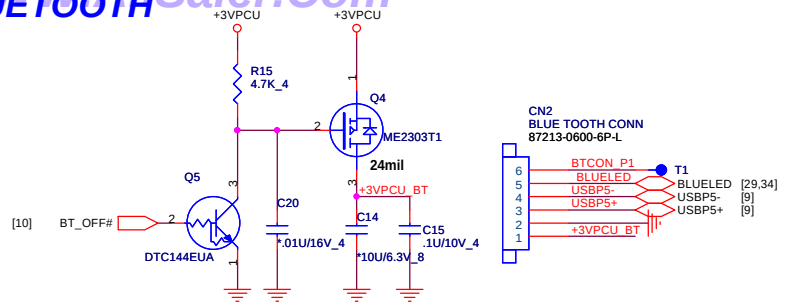
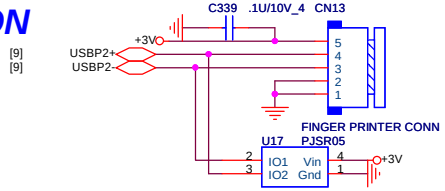
BLUETOOTH

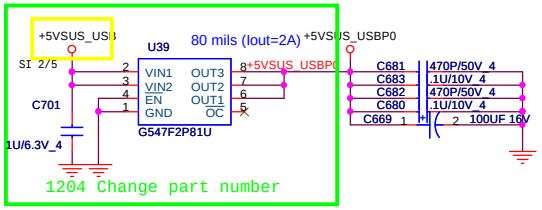


USB fingerprint CON

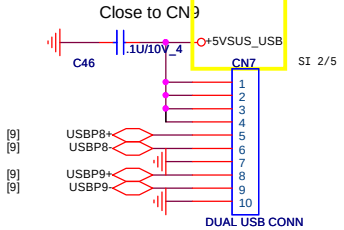
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)



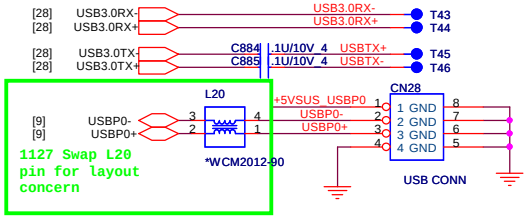
LEFT SIDE USBX1 and E-SATA/USB COMBO



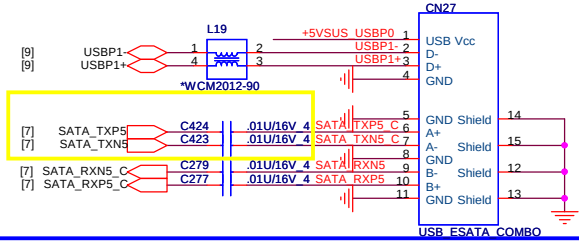
RIGHT SIDE USBX2



Waiting USB3.0 connector

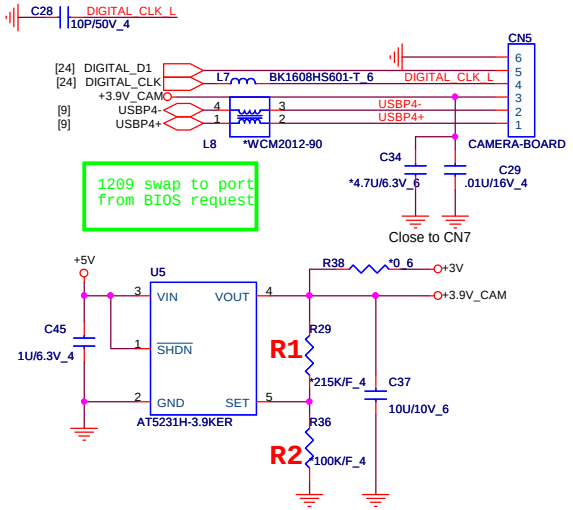


USB & ESATA

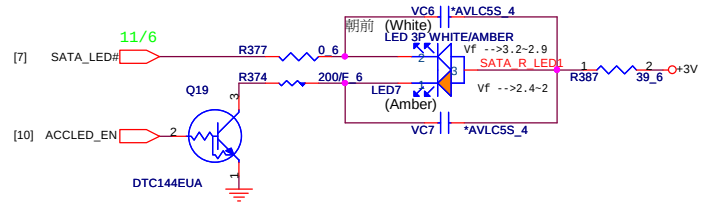


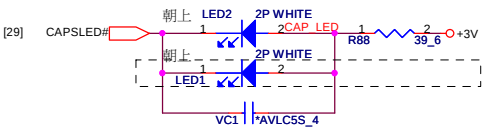
USB CAMERA /DIGITAL MIC CONNECT

Add for EMI solution



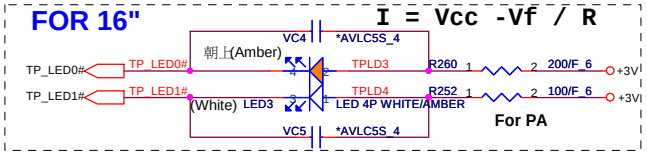
LED

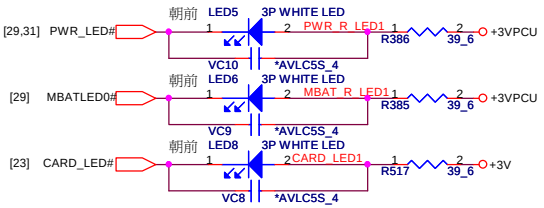


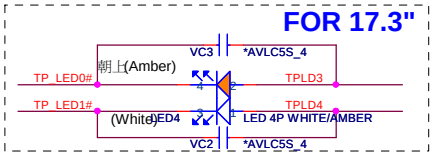


FOR 16"

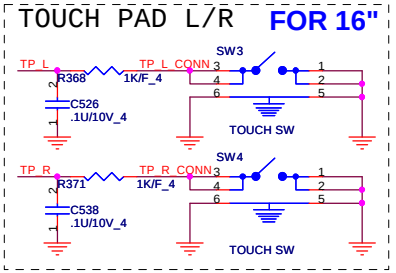
FOR 17.3"

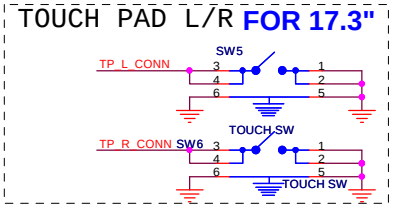


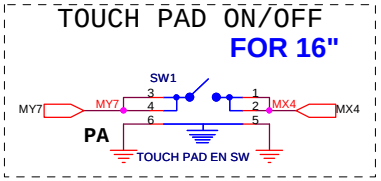


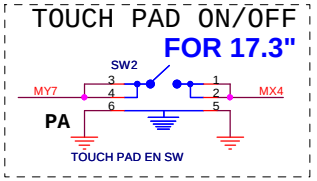


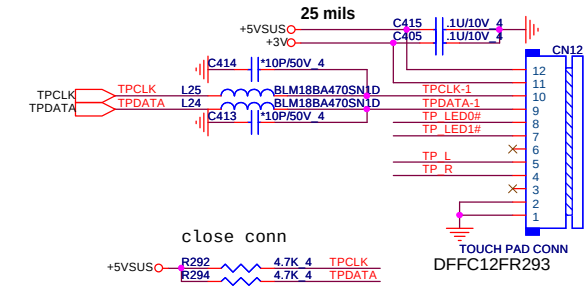
TOUCH PAD CONNECTOR & ON/OFF BOTTOM











[7,12,13,21,29,31,32,34,35,36,38,40,41] +3VPCU
[11,21,22,24,25,31,32,34,40] +5V
[21,32,40] +5VSUS
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,31,32,33,34,37,40] +3V

NB5	**PROJECT : UP67** Quanta Computer Inc.	
Size: Custom	Document Number: BT/WC/FT/ESATA/USB/LED	Rev: 1A
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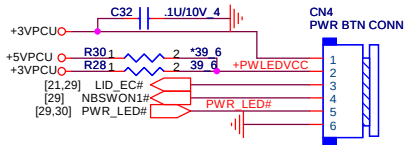
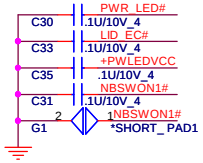
POWER BOTTON CONNECT

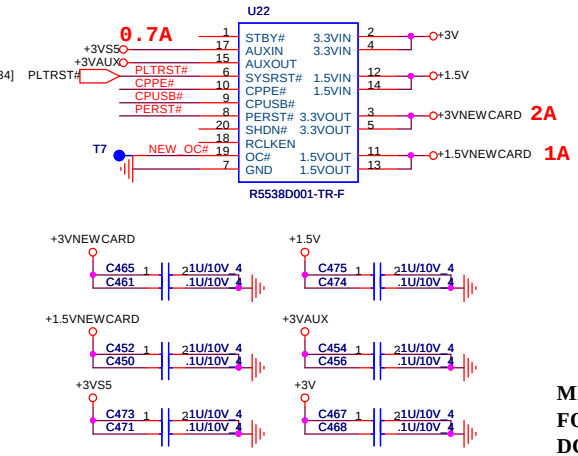


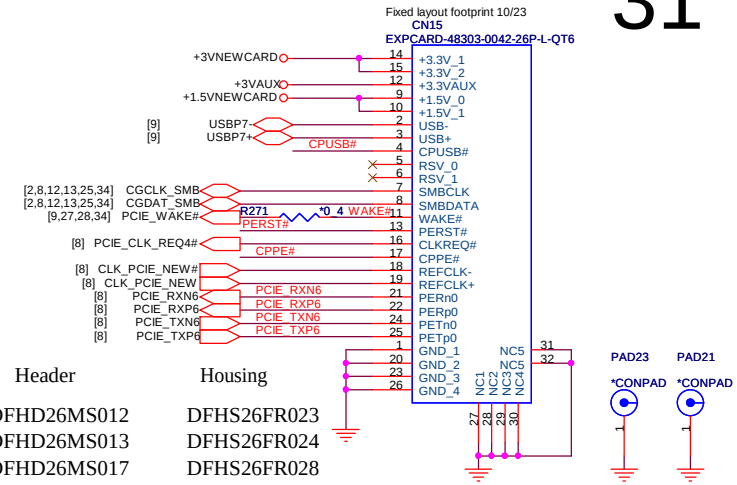
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH [3,8,14,23,27,28,29,33,34] PLTRST#
4. POWERON#
5. PWRLED#
6. GND



NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)



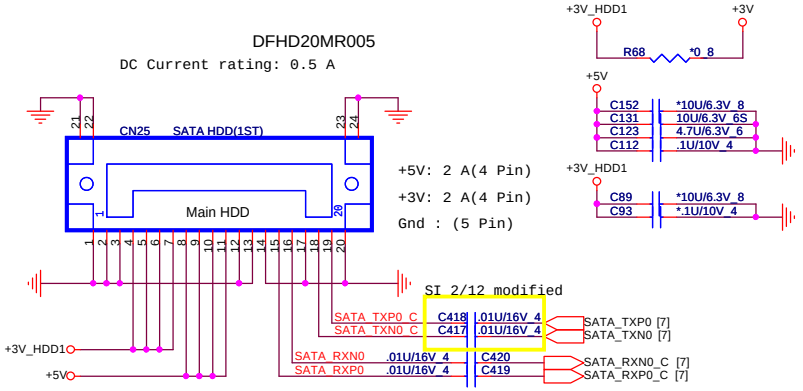


	Header	Housing
MLX	DFHD26MS012	DFHS26FR023
FOX	DFHD26MS013	DFHS26FR024
DGN	DFHD26MS017	DFHS26FR028

SATA HDD CONNECTOR

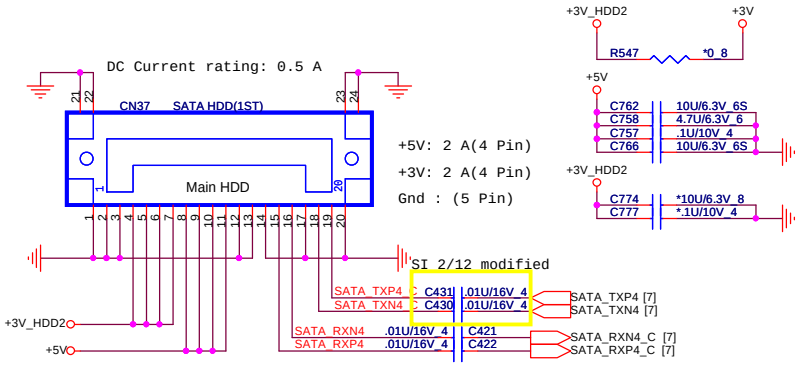
DFHD20MR005

DC Current rating: 0.5 A



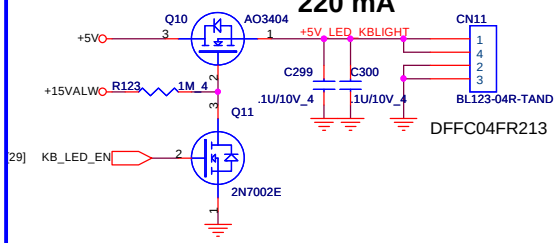
SATA_2 CONNECTOR

DC Current rating: 0.5 A



Backlight Keybaord Con.

220 mA



clear ABS 758 resin for key cap.

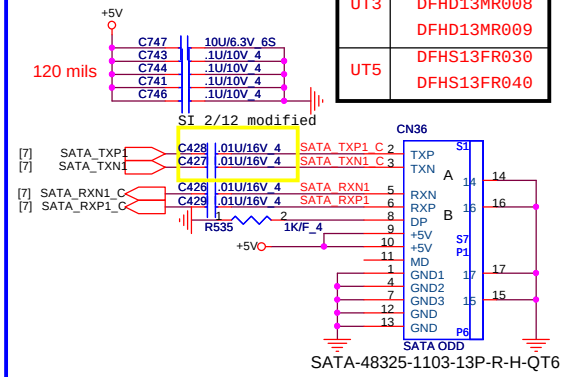
7 LEDs for 15.4" (total LED current 140mA)

11 LEDs for 17" (Total LED current 220mA)

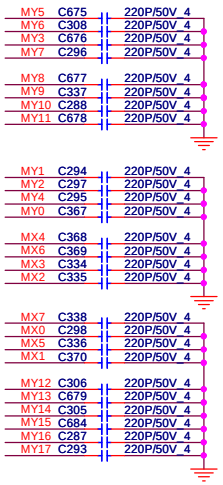
SATA CD-ROM

CN36 part number

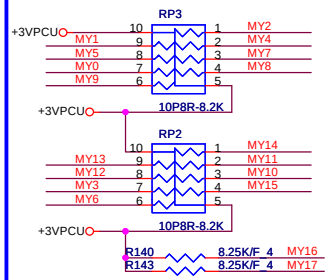
UT3	DFHD13MR006
	DFHD13MR008
	DFHD13MR009
UT5	DFHS13FR030
	DFHS13FR040

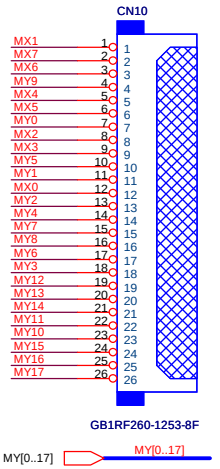


KEYBOARD Con.



KEYBOARD PULL-UP





[15,19,20,34,36,39,40] +1.5V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,32,33,34,37,40] +3V
[7,12,13,21,29,30,32,34,35,36,38,40,41] +3VPCU
[8,9,10,11,33,40] +3VS5
+3VAUX
[11,21,22,24,25,30,32,34,40] +5V
[21,35,40] +15VALW

NB5

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD/PW/KB	1A

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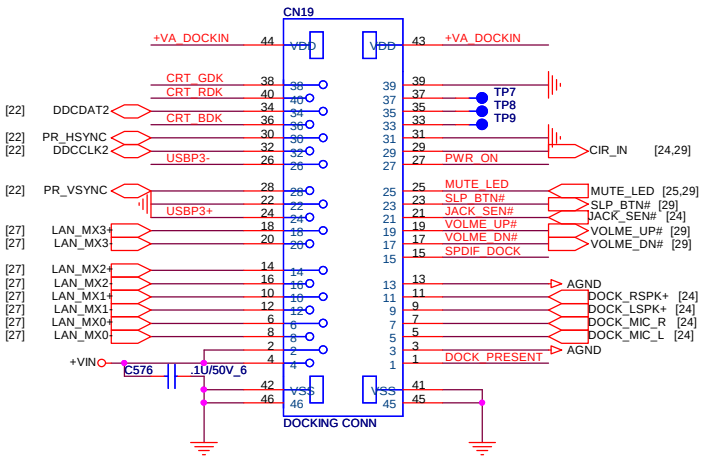
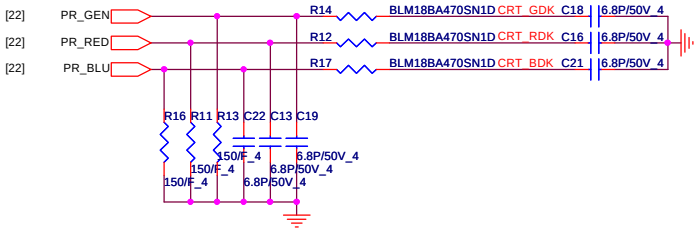
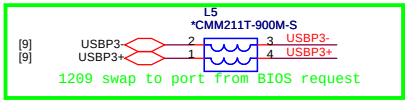
CABLE DOCK

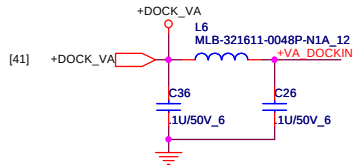
DFHS44FRC04

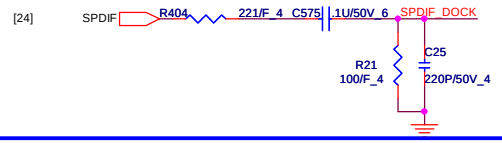


Delete CX08T470000 as CRT rising time and falling time request



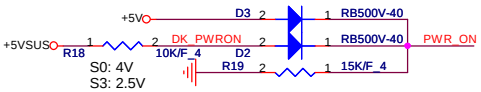


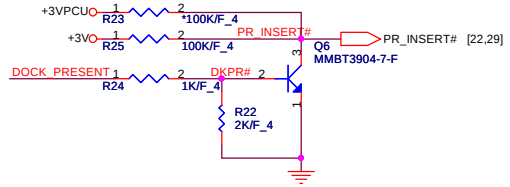




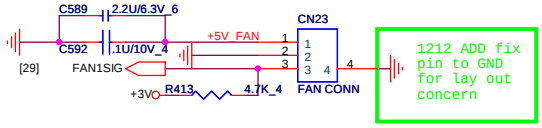
For IDT Dolby functionality.

Change to RB500 as Current loss





CPU FAN



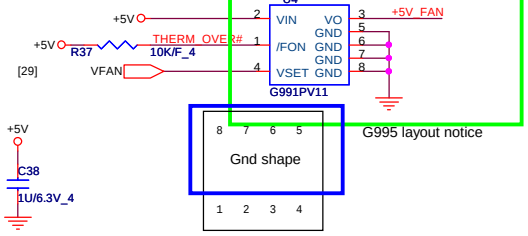
1212 ADD fix pin to GND for lay out concern

DFHD03MR008

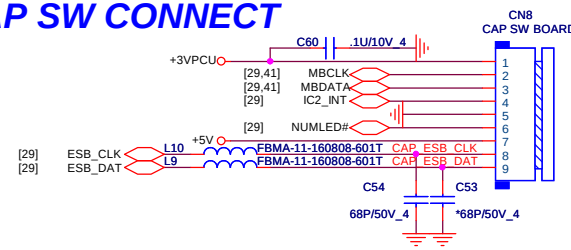
1204 Change part number

FANPWR = 1.6*VSET

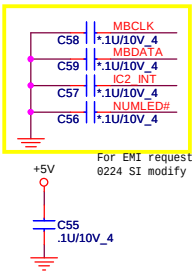
30 MIL



CAP SW CONNECT

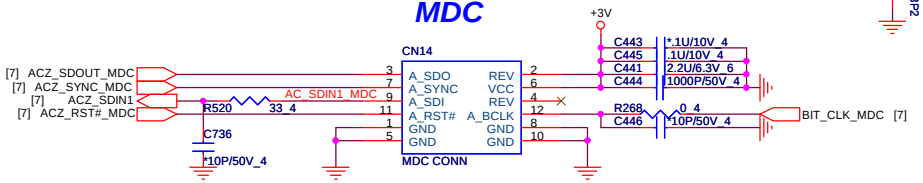


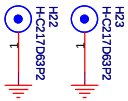
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT



Modem CONN

MDC





[7,12,13,21,29,30,31,34,35,36,38,40,41] +3VPCU
[11,21,22,24,25,30,31,34,40] +5V
[21,30,40] +5VSUS
[41] +DOCK_VA
[21,26,35,36,37,38,39,40,41] +VIN
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,33,34,37,40] +3V

PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DOCKING/FAN/CAP/MDC	1A
NB5		
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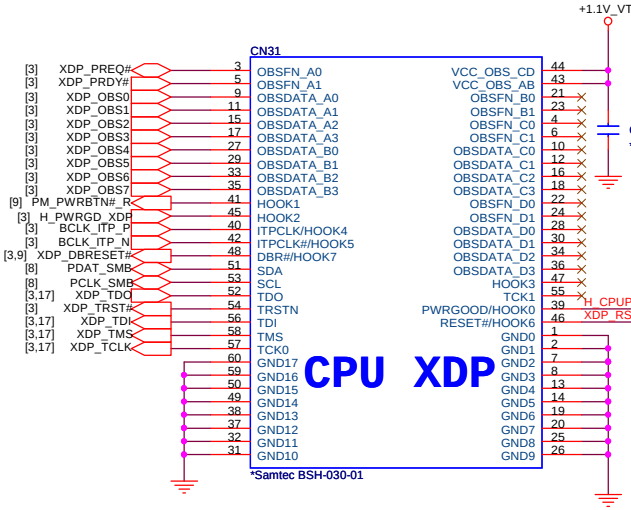
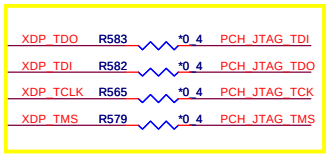
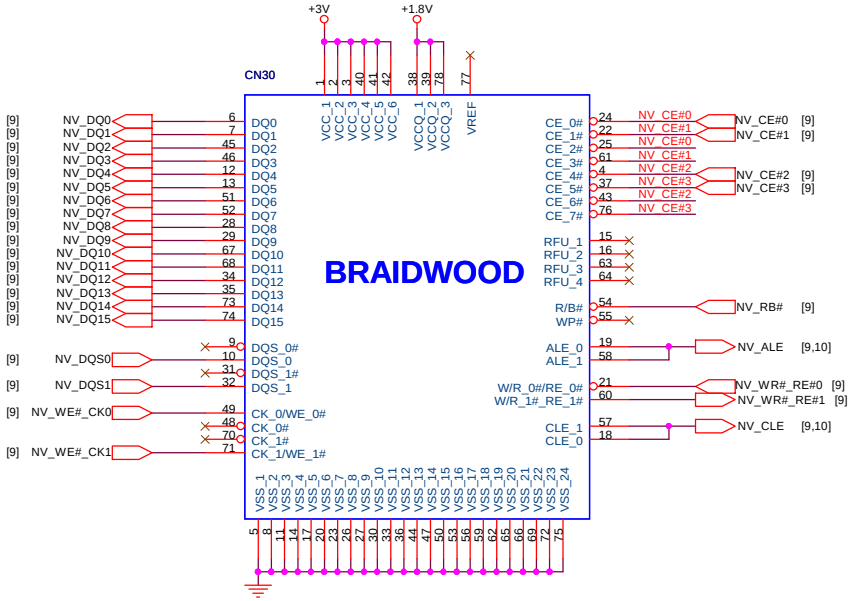
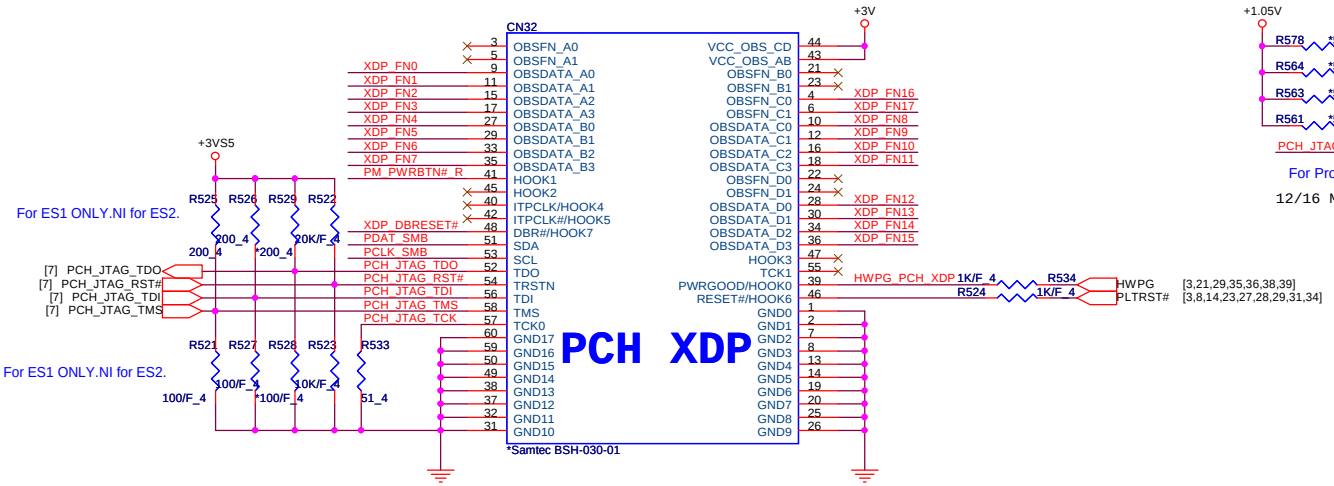
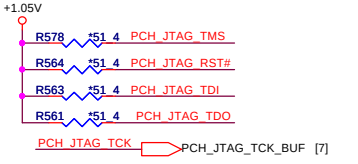


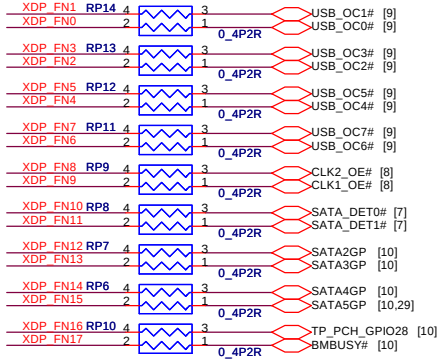
Reserve for BSDL











[3,5,10,11,37,38] +1.1V_VTT
[2,7,8,9,11,14,15,16,28,29,36] +1.05V
[5,10,11,16,36,40] +1.8V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,34,37,40] +3V
[8,9,10,11,31,40] +3VS5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	XDP/BRAIDWOOD	1A
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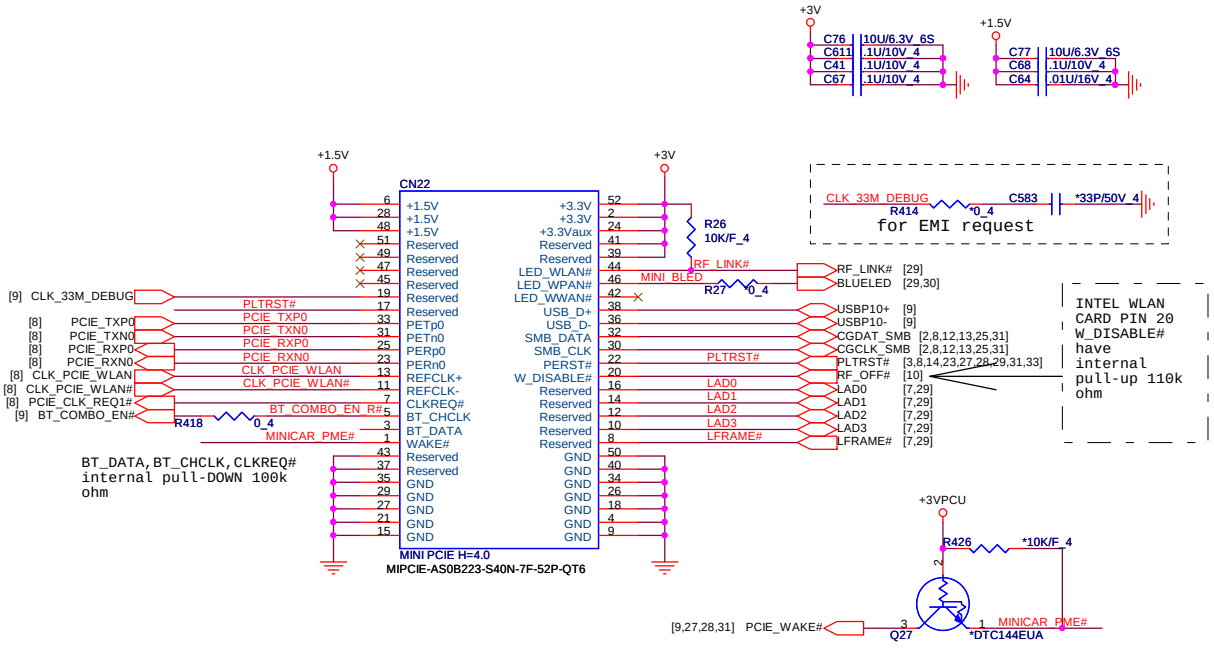
NB5

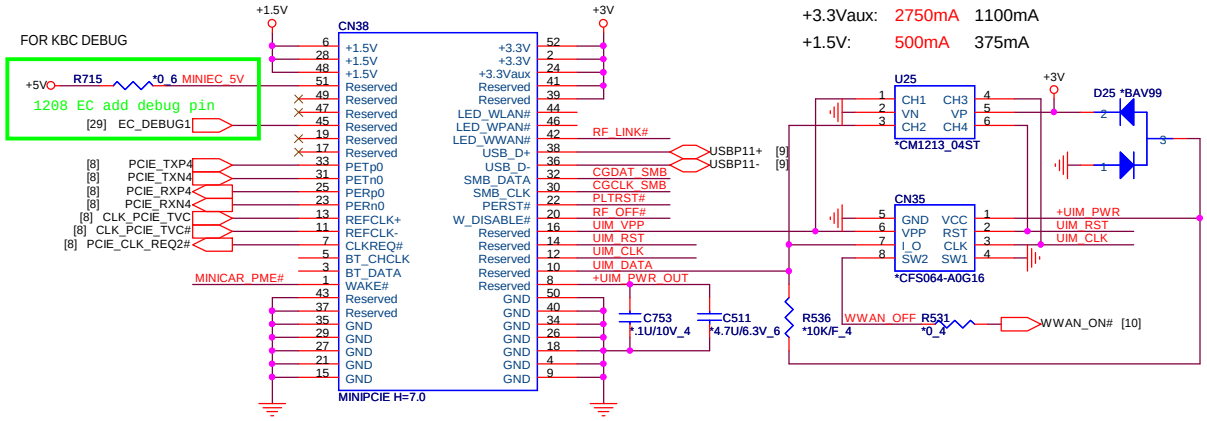
Mini PCI-E Card 1
WLAN

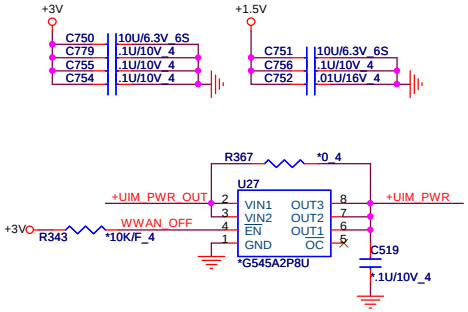


Mini PCI-E Card 2 TV Tuner or WWAN

TV tuner card

	Peak	Normal
+3.3Vaux:	2750mA	1100mA
+1.5V:	500mA	375mA





[15,19,20,31,36,39,40] +1.5V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40] +3V
[7,12,13,21,29,30,31,32,35,36,38,40,41] +3VPCU
[11,21,22,24,25,30,31,32,40] +5V

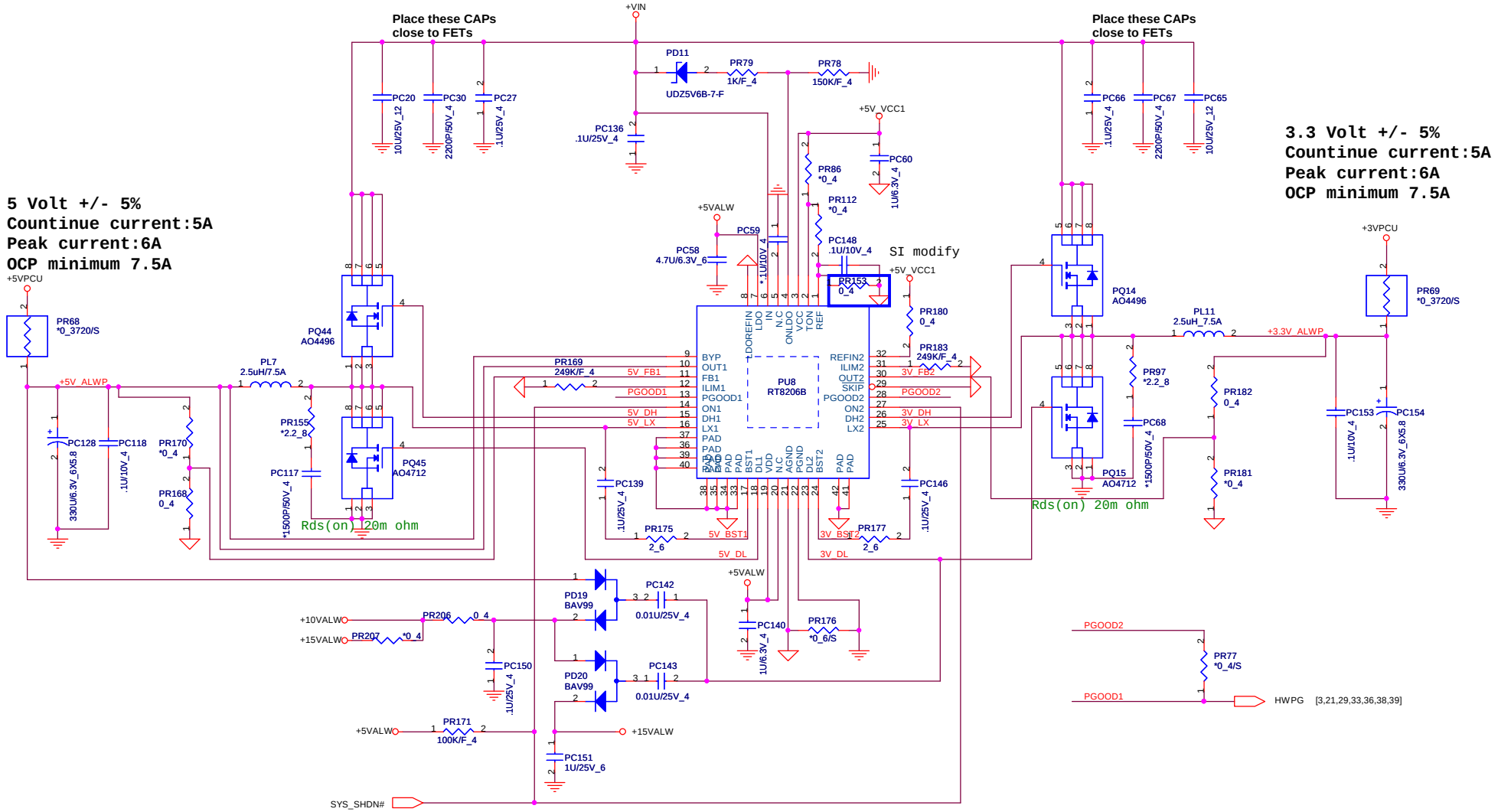
NB5

PROJECT : UP67
Quanta Computer Inc.

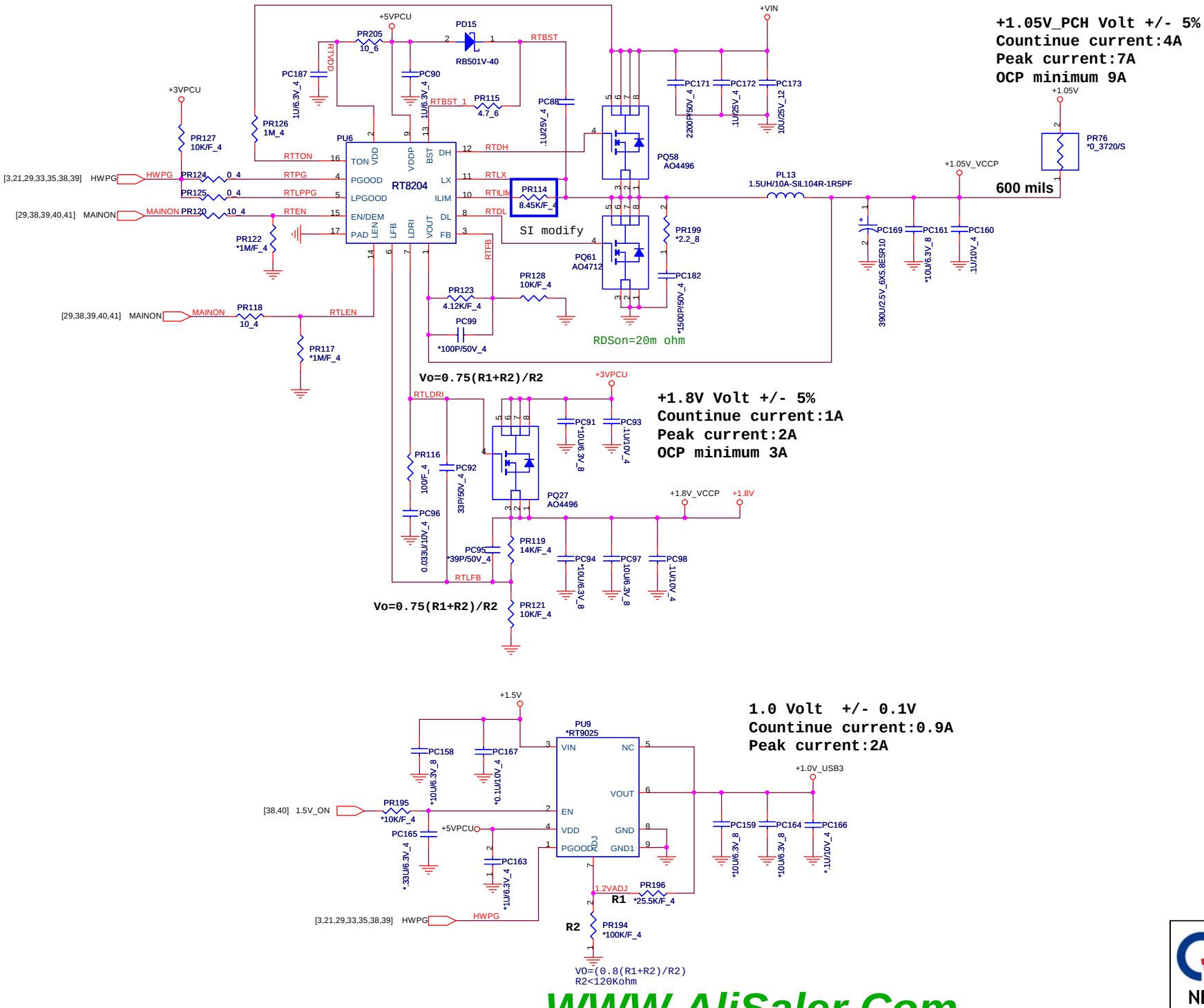
Size	Document Number	Rev
Custom	MINI PCIE CONN X2	1A

Date: Friday, February 27, 2009 Sheet 34 of 45

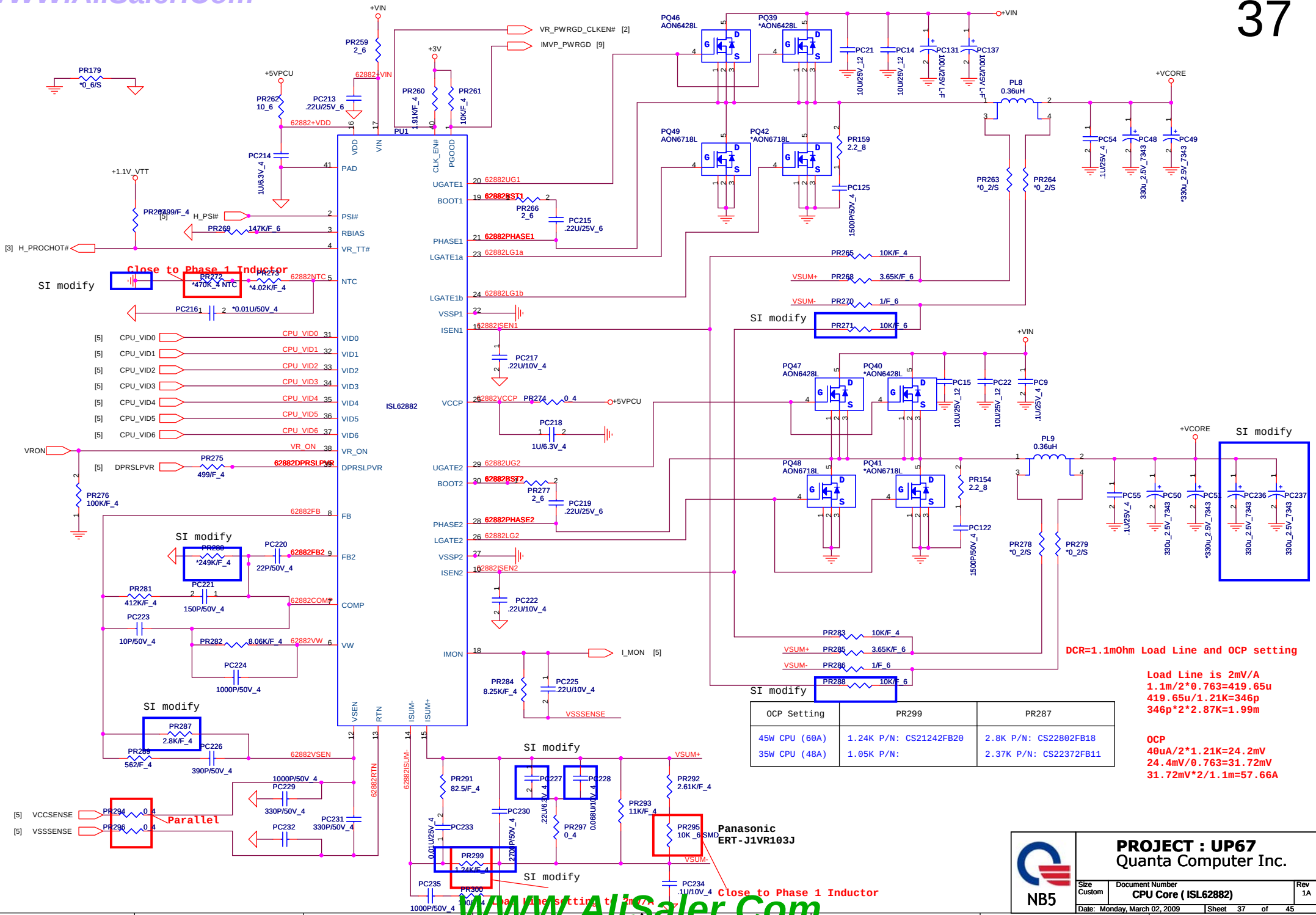
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, February 27, 2009	Sheet 35 of 45	



NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, February 27, 2009	Sheet 36 of 45	



OCP Setting	PR299	PR287
45W CPU (60A)	1.24K P/N: CS21242FB20	2.8K P/N: CS22802FB18
35W CPU (48A)	1.05K P/N:	2.37K P/N: CS22372FB11

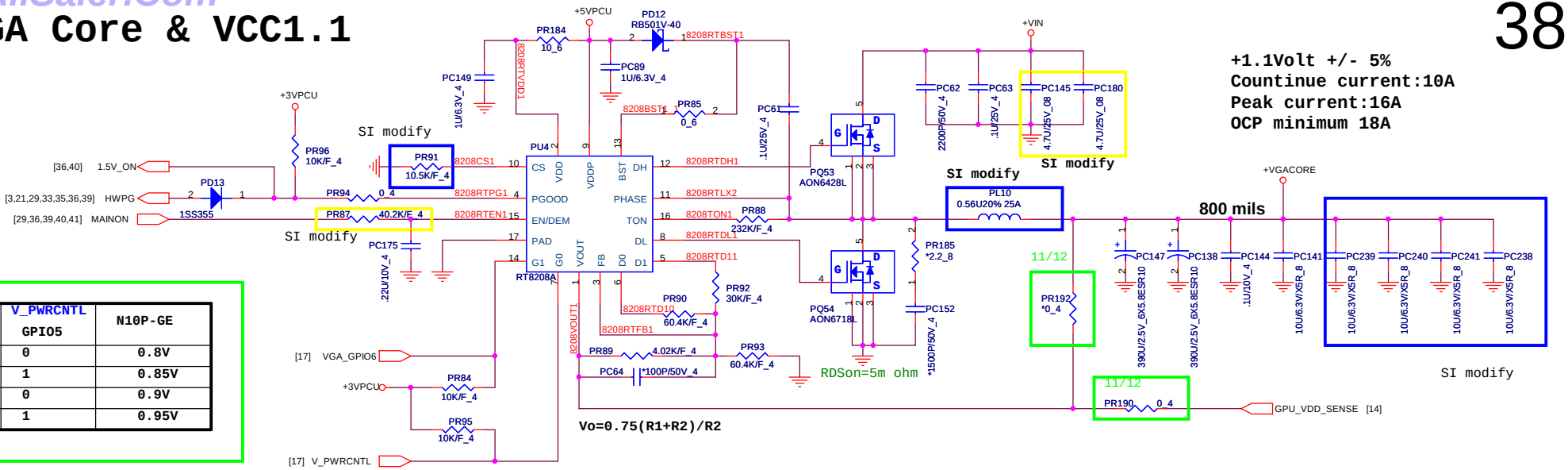
NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core (ISL62882)	Rev: 1A
Date: Monday, March 02, 2009	Sheet 37 of 45	

VGA Core & VCC1.1

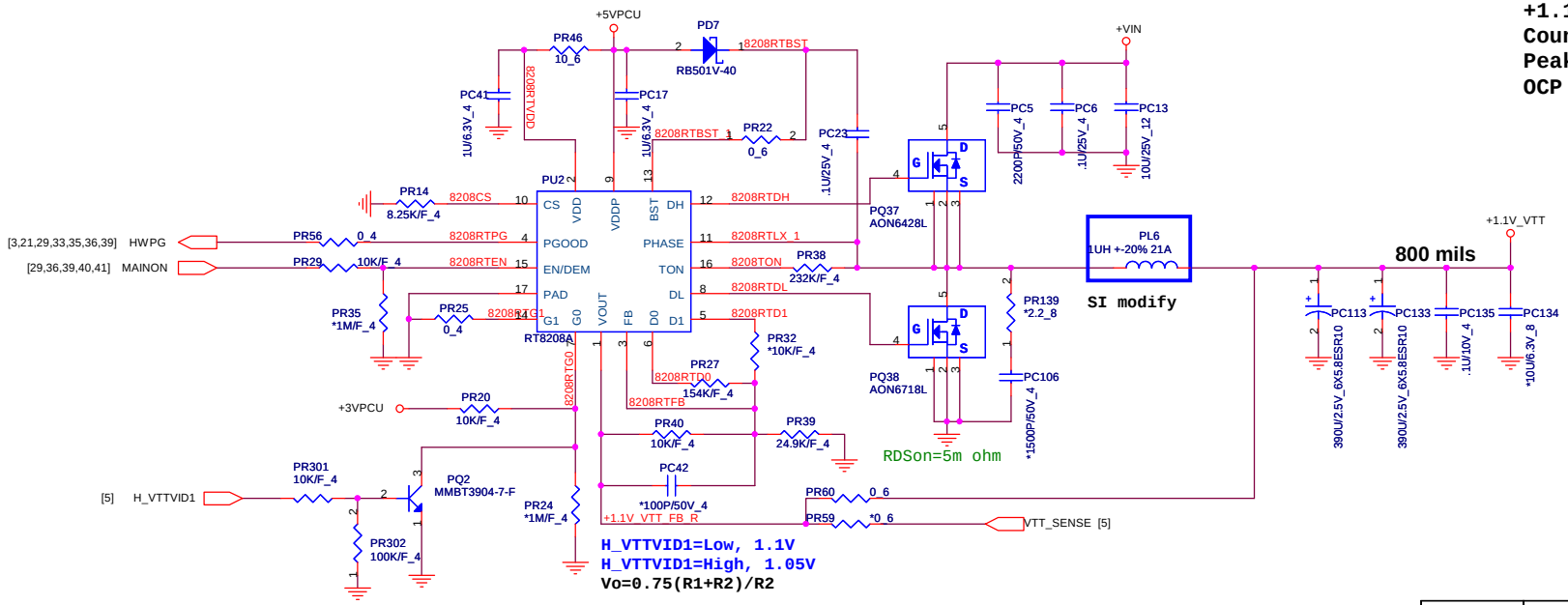
+1.1Volt +/- 5%
Countinue current:10A
Peak current:16A
OCP minimum 18A

11/13

VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5	N10P-GE
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V



+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



PROJECT : UP67
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	+1.1V_VTT/VGA Core (RT8208)	1A

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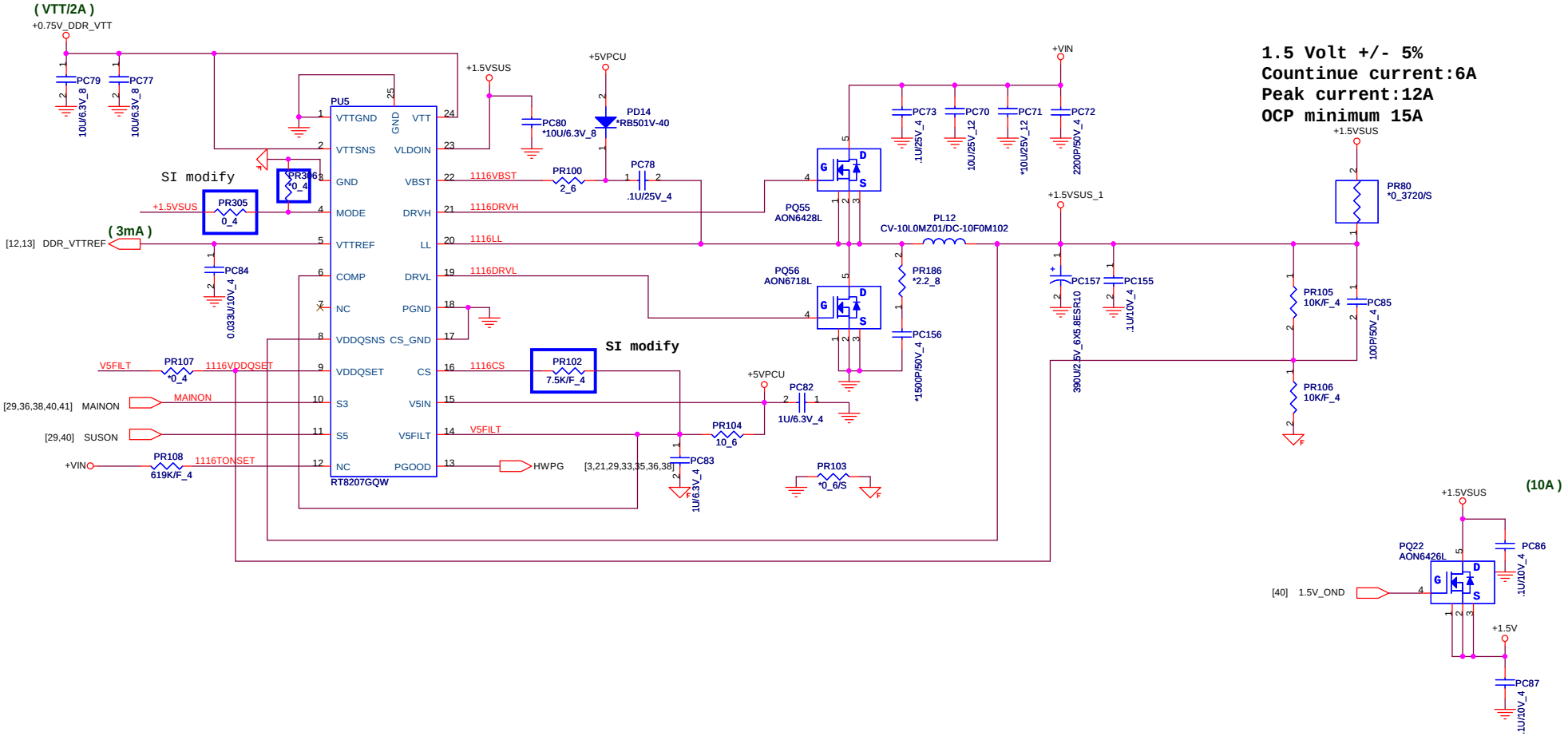
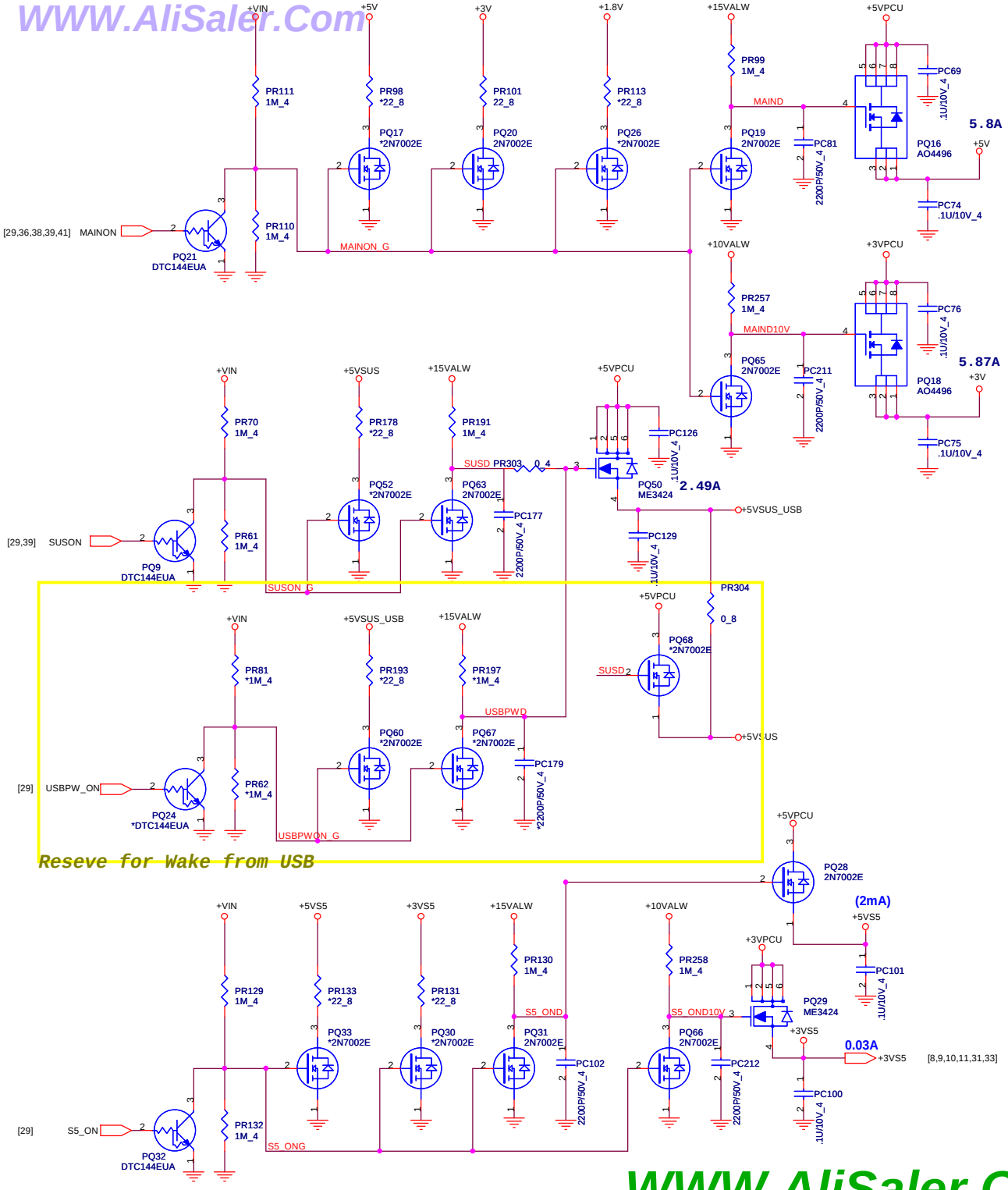
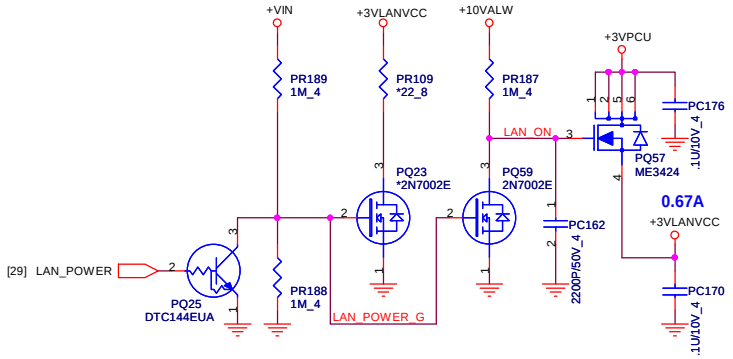
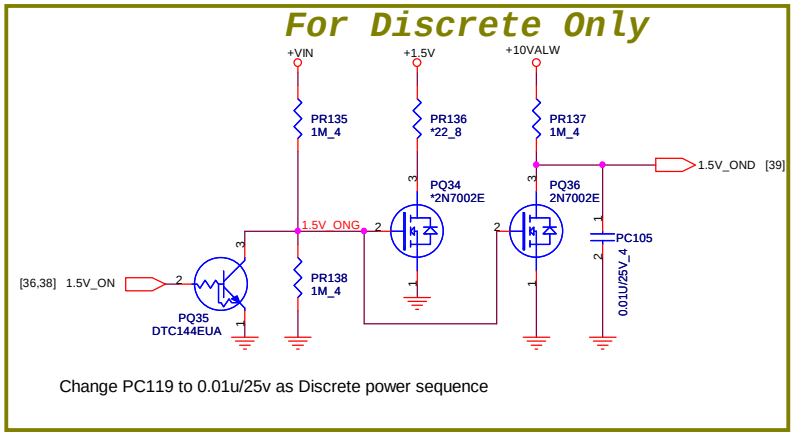
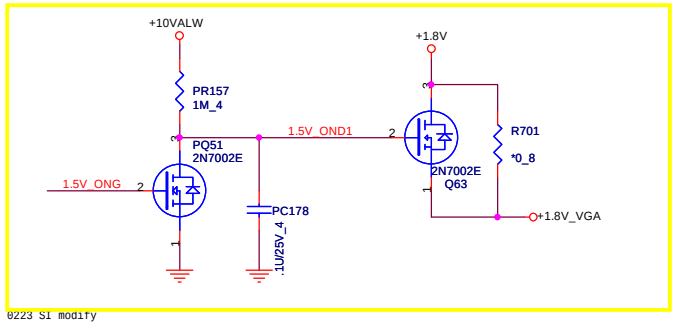


NB5	PROJECT : UP67 Quanta Computer Inc.	
	Size: Custom Document Number: DDR3 (RT8207)	Rev: 1A
	Date: Friday, February 27, 2009	Sheet 39 of 45









NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: DISCHARGE/3VS5/5VS5/LAN	Rev: 1A
Date: Friday, February 27, 2009	Sheet 40 of 45	

BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

SI modify

Change CN21 to BAT-BP02083-B09065-7F-9P-V-QT6

FOR 16"

CN20

BP07061-BA015

SI modify

FOR 17.3"

CN18

200045MR008G10JZR

DB modified *DFHD08MR030 bat-200045mr008g10jzr-8p-l-v

41

DC-IN CONN 120W

DC_JACK 90W/120W

DC-IN CONN

To PWR LED

Place this ZVS close to Diode away +VIN

Place these short pad close to RSENSE

Place this ZVS close to Far-Far away +VIN

Place these CAPs close to FETs

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

Setting the Vin min to 12V For ACSET 1.26V

Setting the Vin min to 17V For EN = 1.06V

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Charging Curret setting = I chg = 165mV / Rsense * (Vchlim / 3.3V)

V ACLIM = VREF * (RI // 152K) / (Rhi // 152K + Rlow// 152K)
Input curretn = 2.9A (71.5K , 10K)
(0.05/Vref * Vaclim + 0.05) / Rsense

Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)

Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

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Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Charger (ISL6251)	1A

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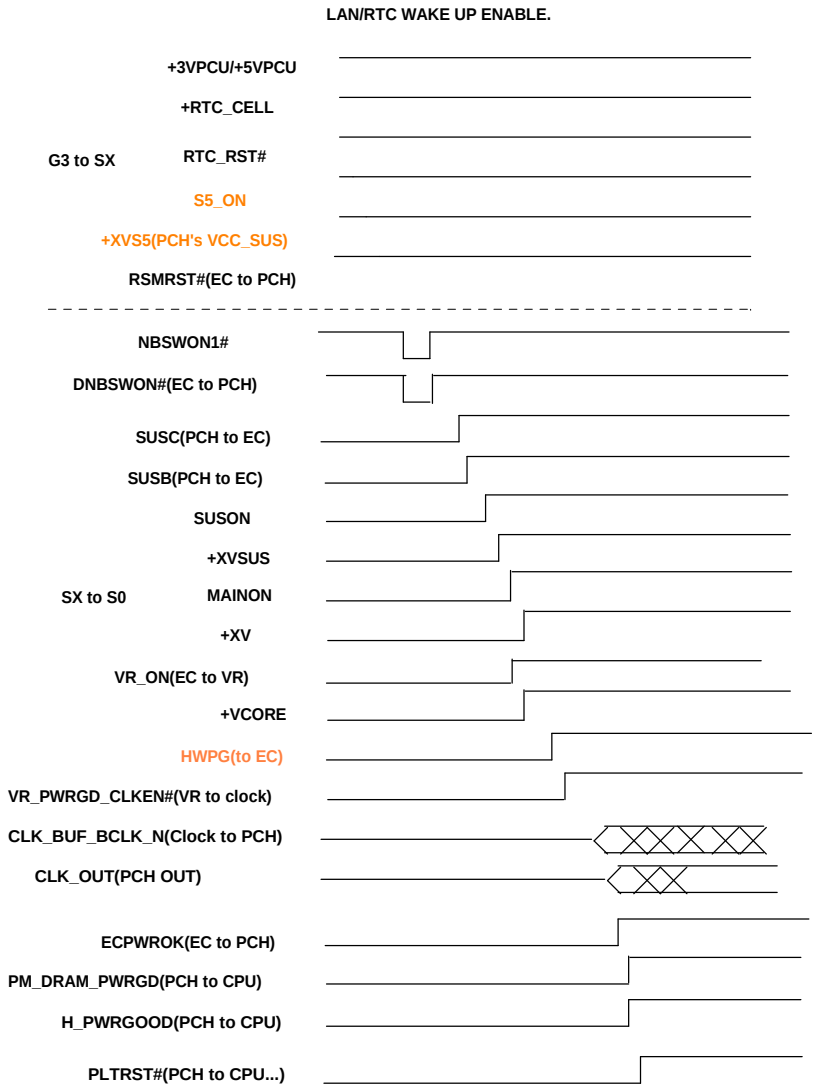
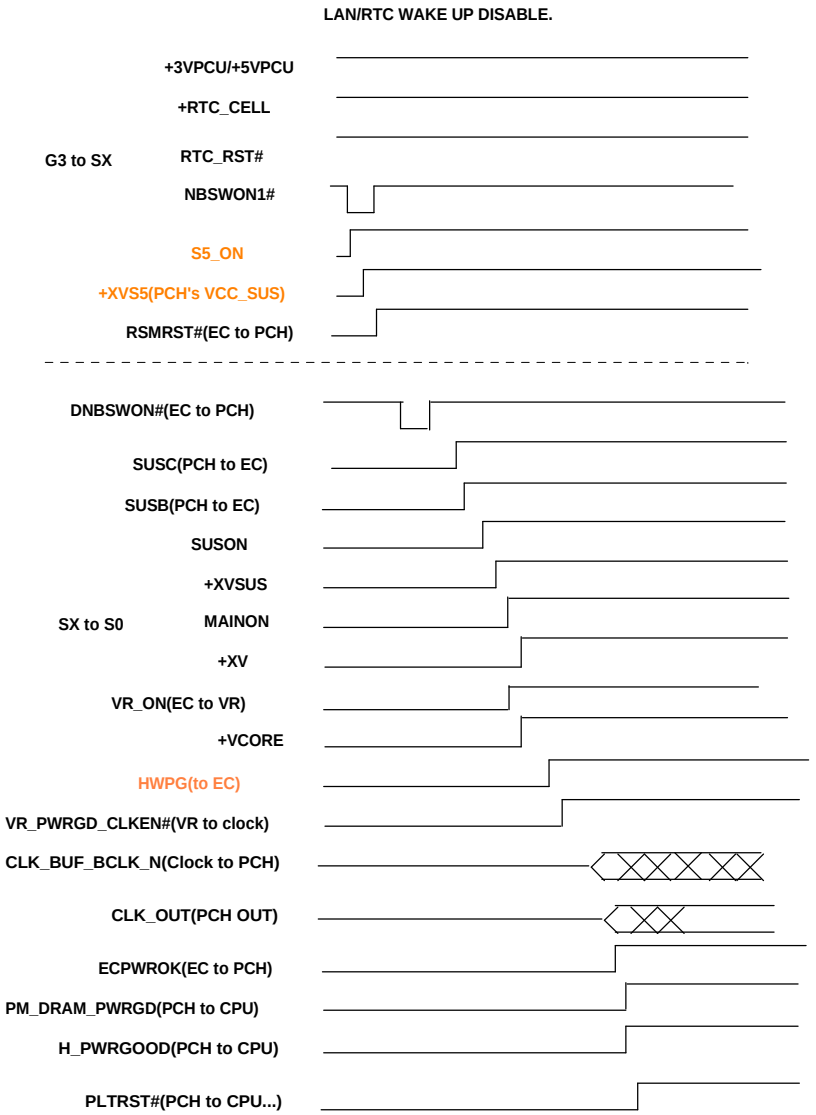
Power up sequence





NB5	PROJECT : UP67 Quanta Computer Inc.	
Size: Custom	Document Number: Power up sequence	Rev: 1A
Date: Friday, February 27, 2009	Sheet 42 of 45	