Colossus 15/17
DIS_OPT Schematic
IVY Bridge (rPGA989)
Intel PCH (Panther Point)

REV:-1
2012-01-05.

DY:No stuff
DIS_OPT:DISCRTE OPTIMUS installed
DY_35W:No stuff on 35W CPU
DY_45W:No stuff on 45W CPU
CR_Balen17:Stuff for 17"
CR_Goya:Stuff for 15"

<Core Design>

緯創資通 Wistron Corporation
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Title: Cover Page		
Size: A4	Document Number: Colossus	Rev: 1
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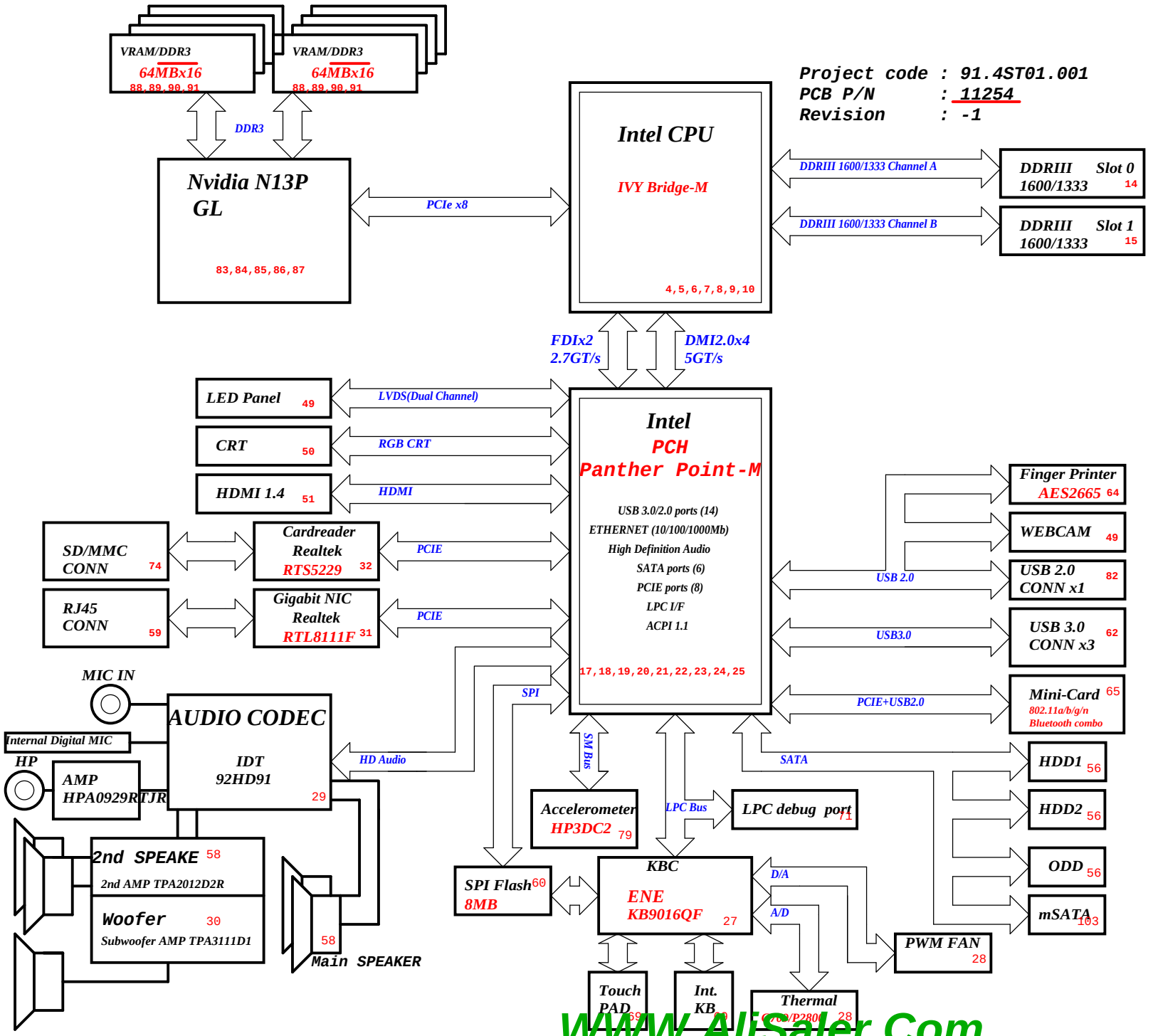
COLOSSUS Block Diagram



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
5V_S5	VCCSA=0D85V_S0

CPU DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_CORE

SYSTEM DC/DC SN1003055RUWR 45	
INPUTS	OUTPUTS
5V_S5/3D3V_S5	1D05V_S0

SYSTEM DC/DC RT8223M_5V/3D3V 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207MZ 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_GFXCORE

VGA NCP3218G 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24738 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC VT385FCX 93	
INPUTS	OUTPUTS
3D3V_S0 1D5V_S0 1D5V_S3	3D3V_VGA_S0 1D5V_VGA_S0 1V05_VGA_S0

Switches 36	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER (DISCRETE)	
L1:Top	L5:Vcc
L2:GND	L6:Signa
L3:Signal	L7:GND
L4:Signal	L8::Bottom

<Core Design>

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Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA_0D85V 0D75V_S0 VCC_CORE VCC_GFXCORE 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 3.3V 1D5V 1D05V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

PCIe Routing

LANE1	N/A
LANE2	17"Card Reader
LANE3	15"Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel GBE LAN / LAN
LANE7	N/A
LANE8	N/A

USB2.0 Table

Pair	Device
0	USB 3.0 I/O CONN. 1
1	N/A
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN.
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1
2	FREE
3	I/O CONN. 2
4	I/O CONN. 3

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	HDD2
3	N/A
4	ODD
5	N/A

<Core Design>

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CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

DP Compensation, within 500mil

1D05V_S0 — R402 24D9R2F-L-GP — 4mil / 12mil — DP_COMP

NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

PEG Compensation

1D05V_S0 — R401 24D9R2F-L-GP — PEG_COMP (J22)

PEG_ICOMPI (J21), PEG_ICOMPO (H22), PEG_RCOMPO

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

CPU1A — IVY-BRIDGE — 1 OF 9

19 DMI_TXN[3:0]	DMI_TXN0 B27, DMI_TXN1 B25, DMI_TXN2 A25, DMI_TXN3 B24	DMI_RX#0, DMI_RX#1, DMI_RX#2, DMI_RX#3
19 DMI_TXP[3:0]	DMI_TXP0 B28, DMI_TXP1 B26, DMI_TXP2 A24, DMI_TXP3 B23	DMI_RX0, DMI_RX1, DMI_RX2, DMI_RX3
19 DMI_RXN[3:0]	DMI_RXN0 G21, DMI_RXN1 E22, DMI_RXN2 F21, DMI_RXN3 D21	DMI_TX#0, DMI_TX#1, DMI_TX#2, DMI_TX#3
19 DMI_RXP[3:0]	DMI_RXP0 G22, DMI_RXP1 D22, DMI_RXP2 F20, DMI_RXP3 C21	DMI_TX0, DMI_TX1, DMI_TX2, DMI_TX3
19 FDI_TX_N[7:0]	FDI_TX_N0 A21, FDI_TX_N1 H19, FDI_TX_N2 E19, FDI_TX_N3 F18, FDI_TX_N4 B21, FDI_TX_N5 C20, FDI_TX_N6 D18, FDI_TX_N7 E17	FDI0_TX#0, FDI0_TX#1, FDI0_TX#2, FDI0_TX#3, FDI1_TX#0, FDI1_TX#1, FDI1_TX#2, FDI1_TX#3
19 FDI_TX_P[7:0]	FDI_TX_P0 A22, FDI_TX_P1 G19, FDI_TX_P2 E20, FDI_TX_P3 G18, FDI_TX_P4 B20, FDI_TX_P5 C19, FDI_TX_P6 D19, FDI_TX_P7 F17	FDI0_TX0, FDI0_TX1, FDI0_TX2, FDI0_TX3, FDI1_TX0, FDI1_TX1, FDI1_TX2, FDI1_TX3
19 FDI_FSYNC0, 19 FDI_FSYNC1	J18, J17	FDI0_FSYNC, FDI1_FSYNC
19 FDI_INT	H20	FDI_INT
19 FDI_LSYNC0, 19 FDI_LSYNC1	J19, H17	FDI0_LSYNC, FDI1_LSYNC
	A18, A17, B16	EDP_COMPIO, EDP_ICOMPO, EDP_HPD
	C15, D15	EDP_AUX, EDP_AUX#
	C17, F16, C16, G15	EDP_TX0, EDP_TX1, EDP_TX2, EDP_TX3
	C18, E16, D16, F15	EDP_TX#0, EDP_TX#1, EDP_TX#2, EDP_TX#3

DMI | Intel(R) FDI | PCI EXPRESS* - GRAPHICS | eDP

PEG_RXN[0..7] 83

PEG_RX#0	K33 PEG_RXN0
PEG_RX#1	M35 PEG_RXN1
PEG_RX#2	L34 PEG_RXN2
PEG_RX#3	J35 PEG_RXN3
PEG_RX#4	J32 PEG_RXN4
PEG_RX#5	H34 PEG_RXN5
PEG_RX#6	H31 PEG_RXN6
PEG_RX#7	G33 PEG_RXN7
PEG_RX#8	G30
PEG_RX#9	F35
PEG_RX#10	E34
PEG_RX#11	E32
PEG_RX#12	D33
PEG_RX#13	D31
PEG_RX#14	B33
PEG_RX#15	C32

PEG_RXP[0..7] 83

PEG_RX0	J33 PEG_RXP0
PEG_RX1	L35 PEG_RXP1
PEG_RX2	K34 PEG_RXP2
PEG_RX3	H35 PEG_RXP3
PEG_RX4	H32 PEG_RXP4
PEG_RX5	G34 PEG_RXP5
PEG_RX6	G31 PEG_RXP6
PEG_RX7	F33 PEG_RXP7
PEG_RX8	F30
PEG_RX9	E35
PEG_RX10	E33
PEG_RX11	F32
PEG_RX12	D34
PEG_RX13	E31
PEG_RX14	C33
PEG_RX15	B32

PEG_TXN[0..7] 83

PEG_TX#0	M29	PEG_C_TXN0	DIS_OPT416 1 — SCD22U10V2KX-1GP — PEG_TXN0
PEG_TX#1	M32	PEG_C_TXN1	DIS_OPT415 1 — SCD22U10V2KX-1GP — PEG_TXN1
PEG_TX#2	M31	PEG_C_TXN2	DIS_OPT414 1 — SCD22U10V2KX-1GP — PEG_TXN2
PEG_TX#3	L32	PEG_C_TXN3	DIS_OPT413 1 — SCD22U10V2KX-1GP — PEG_TXN3
PEG_TX#4	L29	PEG_C_TXN4	DIS_OPT412 1 — SCD22U10V2KX-1GP — PEG_TXN4
PEG_TX#5	K31	PEG_C_TXN5	DIS_OPT411 1 — SCD22U10V2KX-1GP — PEG_TXN5
PEG_TX#6	K28	PEG_C_TXN6	DIS_OPT410 1 — SCD22U10V2KX-1GP — PEG_TXN6
PEG_TX#7	J30	PEG_C_TXN7	DIS_OPT409 1 — SCD22U10V2KX-1GP — PEG_TXN7
PEG_TX#8	J28		
PEG_TX#9	H29		
PEG_TX#10	G27		
PEG_TX#11	F29		
PEG_TX#12	F27		
PEG_TX#13	D28		
PEG_TX#14	F26		
PEG_TX#15	E25		

PEG_TXP[0..7] 83

PEG_TX0	M28	PEG_C_TXP0	DIS_OPT432 1 — SCD22U10V2KX-1GP — PEG_TXP0
PEG_TX1	M33	PEG_C_TXP1	DIS_OPT431 1 — SCD22U10V2KX-1GP — PEG_TXP1
PEG_TX2	M30	PEG_C_TXP2	DIS_OPT430 1 — SCD22U10V2KX-1GP — PEG_TXP2
PEG_TX3	L31	PEG_C_TXP3	DIS_OPT429 1 — SCD22U10V2KX-1GP — PEG_TXP3
PEG_TX4	L28	PEG_C_TXP4	DIS_OPT428 1 — SCD22U10V2KX-1GP — PEG_TXP4
PEG_TX5	K30	PEG_C_TXP5	DIS_OPT427 1 — SCD22U10V2KX-1GP — PEG_TXP5
PEG_TX6	K27	PEG_C_TXP6	DIS_OPT425 1 — SCD22U10V2KX-1GP — PEG_TXP6
PEG_TX7	J29	PEG_C_TXP7	DIS_OPT426 1 — SCD22U10V2KX-1GP — PEG_TXP7
PEG_TX8	J27		
PEG_TX9	H28		
PEG_TX10	G28		
PEG_TX11	E28		
PEG_TX12	F28		
PEG_TX13	D27		
PEG_TX14	E26		
PEG_TX15	D25		

GP

633996-302

Hand control CPU1 P/N

2ND = 62.10055.321
3RD = 62.10055.551

1st 633996-302
2nd 633996-501
3rd 633996-301

<Core Design>

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Title: **CPU(1/7): DMI/PEG/FDI**

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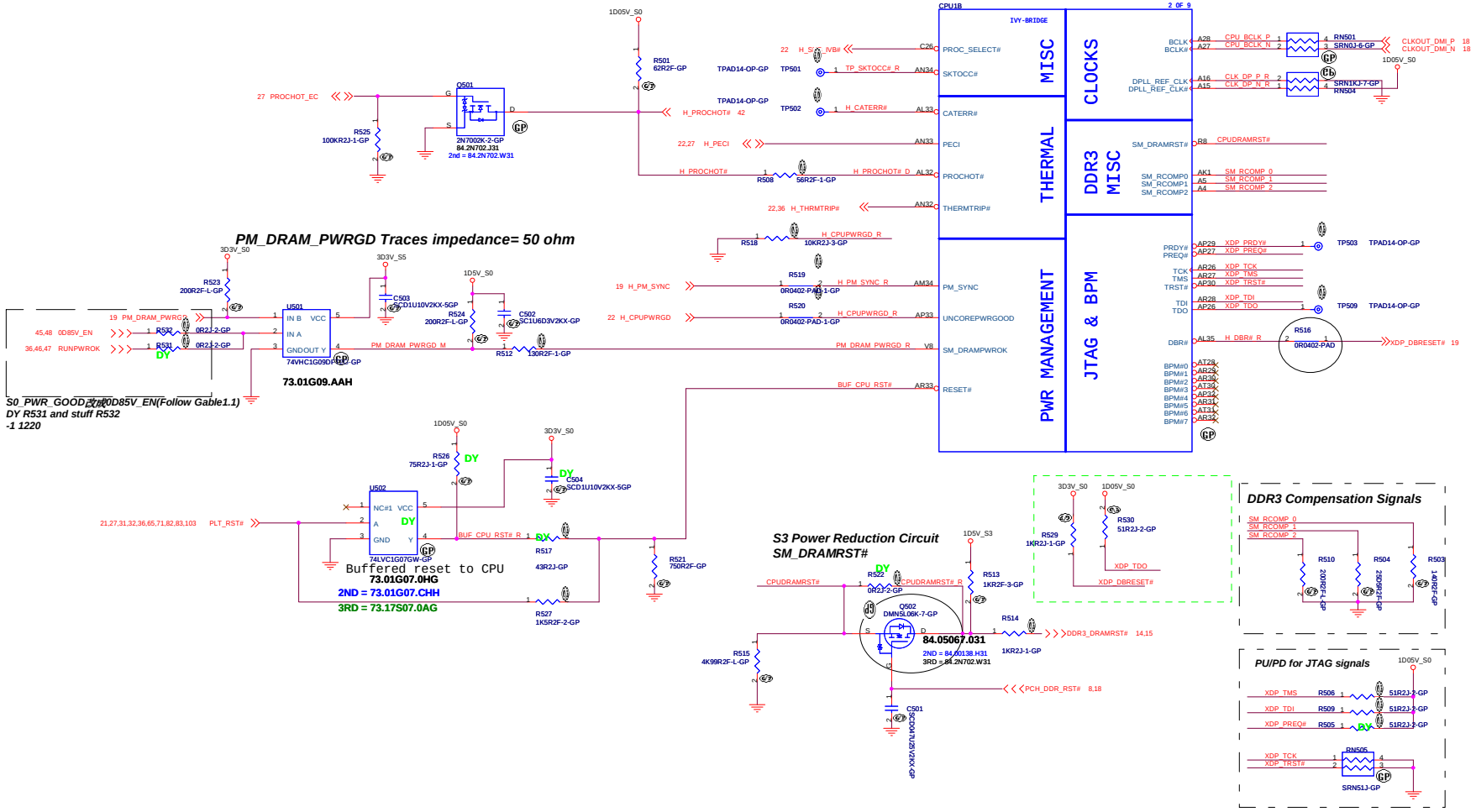
CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



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Title: CPU(2/7): CLK/MISC/JTAG

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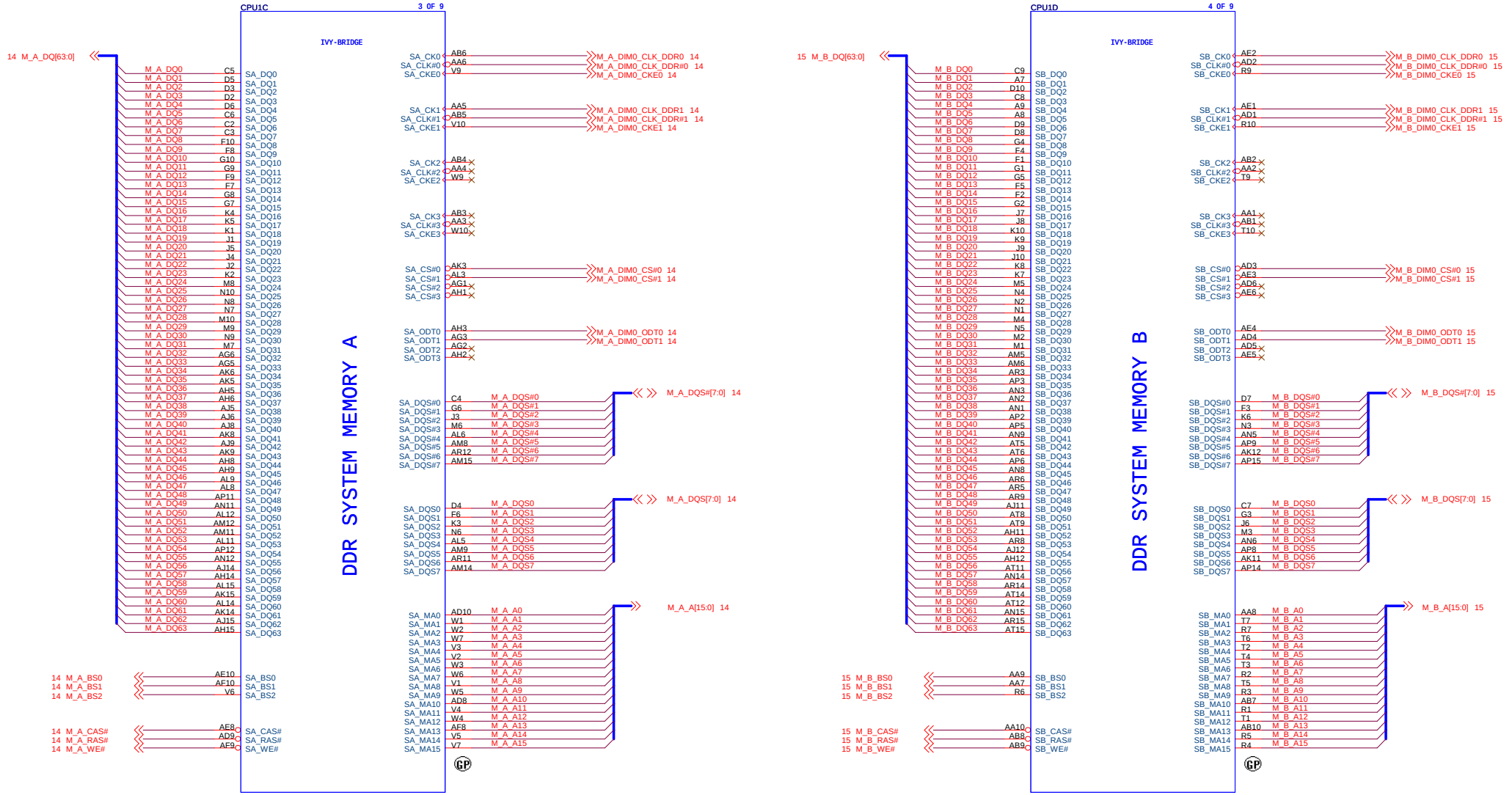
CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



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CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

CPU1F

POWER

6 OF 9

IVY-BRIDGE

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR CORE POWER

53A

VCC_CORE

PROCESSOR UNCORE POWER

8.5A

1D05V_S0

Place Bottom

Place Top

Power 78.22610.51L

Differential Sense feedback

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(4/7): PWR

Size: Custom | Document Number: Colossus | Rev: 1

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CPU(5/7)

IVY BRIDGE PROCESSOR (GRAPHICS POWER)

M3 - Processor Generated SO-DIMM VREF_DQ

33A

VCC_GFXCORE

470U*2 22U*6

Under Socket and Closed to CPU

C820 C821 C822 C823 C824 C825 SC22U6D3V5MX-2GP

VCC_GFXCORE

22U*6

Closed to CPU Socket

C826 C827 C828 C829 C830 C831 SC22U6D3V5MX-2GP

Power 78.22610_51L

C837 C836 C835 C834 C833 SC22U6D3V5MX-2GP

C832 SC10U6D3V5KX-1GP

1.5A

1D8V_S0

C819 C816 SC10U6D3V5KX-1GP

C817 SC1U10V2KX-1GP

C818 SC1U10V2KX-1GP

CPU1G

IVY-BRIDGE

7 OF 9

POWER

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 42

VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

VREF

SM_VREF AL1 ← +V_SM_VREF_CNT

B4:VREF_DQ CHA

D1:VREF_DQ CHB

SA_DIMM_VREFDQ B4 ← DDR_VREF_S3_B4

SB_DIMM_VREFDQ D1 ← DDR_VREF_S3_D1

R815 1KR2F-3-GP DY

R816 1KR2F-3-GP DY

C801 SCD1U16V2ZY-2GP DY

C802 SCD2U10V2ZY-1GP DY

CAD Note: +V_SM_VREF should have 10 mil trace width

DDR_VREF_S3

R808 0R2J-2-GP DY

R809 0R2J-2-GP DY

14 M_VREF_DQ_DIMM0

15 M_VREF_DQ_DIMM1

0R2J-2-GP R812

0R2J-2-GP R813

M_VREF_DQ_DIMM0_R

M_VREF_DQ_DIMM1_R

DDR_VREF_S3_B4

DDR_VREF_S3_D1

84.05067.031

2ND = 84.00138.H31

3RD = 84.2N702.W31

Q802 DMN5L06K-7-GP

R810 0R2J-2-GP DY

PCH_DDR_RST# 5,18

R814 0R2J-2-GP DY

Q803 DMN5L06K-7-GP

-1 1221

DDR3 -1.5V RAILS

12~16A

1D5V_S0

330U*1 10U*6

VDDQ1 AE7

VDDQ2 AE4

VDDQ3 AE1

VDDQ4 AC7

VDDQ5 AC4

VDDQ6 AC1

VDDQ7 Y7

VDDQ8 Y4

VDDQ9 Y1

VDDQ10 U7

VDDQ11 U4

VDDQ12 U1

VDDQ13 P7

VDDQ14 P4

VDDQ15 P1

C803 SC4D7U6D3V3KX-GP

C804 SC4D7U6D3V3KX-GP

C805 SC10U6D3V5KX-1GP

C806 SC10U6D3V5KX-1GP

C807 SC10U6D3V5KX-1GP

C808 SC10U10V5KX-2GP

TC801 ST330U2D5VDM-9GP

77.23371.13L

2nd = 79.33719.L01

SA RAIL

6A

0D85V_S0

VCCSA1 M27

VCCSA2 M26

VCCSA3 L26

VCCSA4 J26

VCCSA5 J25

VCCSA6 J24

VCCSA7 H26

VCCSA8 H25

C813 C814 C815 SC10U6D3V5KX-1GP

0D85V_S0

R801 100R2J-2-GP DY

VCCSA_SENSE H23 → VCCUSA_SENSE

VCCUSA_SENSE 48

MISC

VCCSA_VID0 C22

VCCSA_VID1 C24

H_FC_C22

VCCSA_SEL

H_FC_C22 48

VCCSA_SEL 48

RN801 SRN1KJ-11-GP-U

VCCIO_SEL A19 ← H_VCCP_SEL

SNB: No Connect

IVB: VSS

R817 0R2J-2-GP DY

H_SNB_IVB#_PWRCTRL

TP801 TPAD14-OP-GP

R818 0R2J-2-GP DY

1.8V RAIL

VCCPLL1 B6

VCCPLL2 A6

VCCPLL3 A2

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

S3 Power Reduction Circuit Processor VREF_DQ Implementation

DDR_VREF_S3

R807 0R2J-2-GP

R811 0R2J-2-GP DY

14 M_VREF_DQ_DIMM0

R805 0R2J-2-GP DY

+V_SM_VREF

Q801 DMN5L06K-7-GP

84.05067.031

2ND = 84.00138.H31

3RD = 84.2N702.W31

+V_SM_VREF_CNT

R803 100KR2J-1-GP

R802 0R2J-2-GP DY

5,18 PCH_DDR_RST#

19,27,36,46,47,92 PM_SLP_S3#

<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

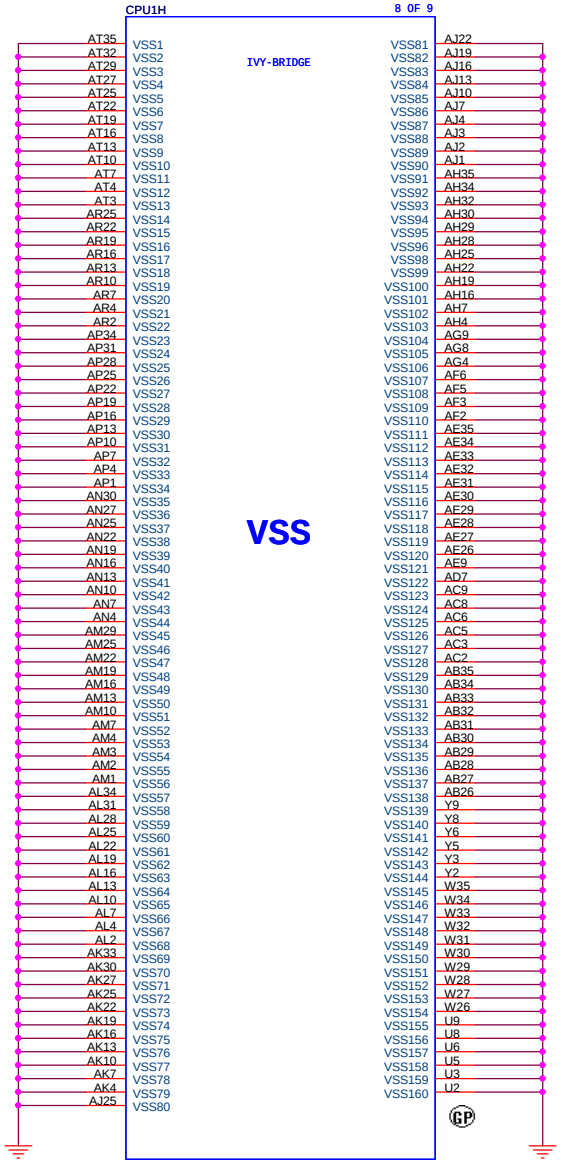
Title: CPU(5/7): GFX/PWR

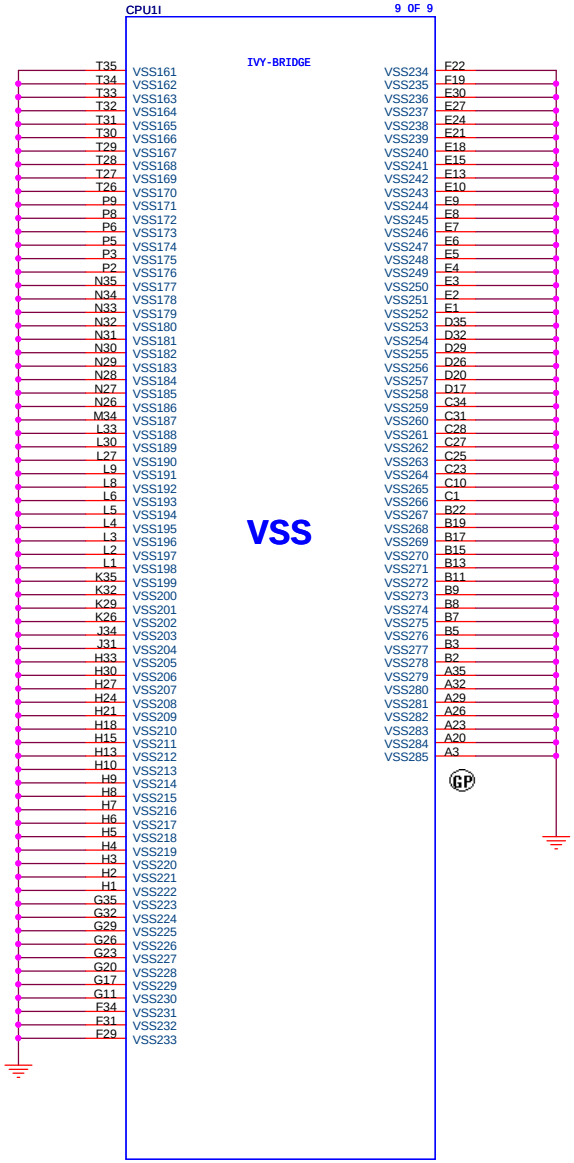
Size: Custom | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 8 of 103

CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





<Core Design>

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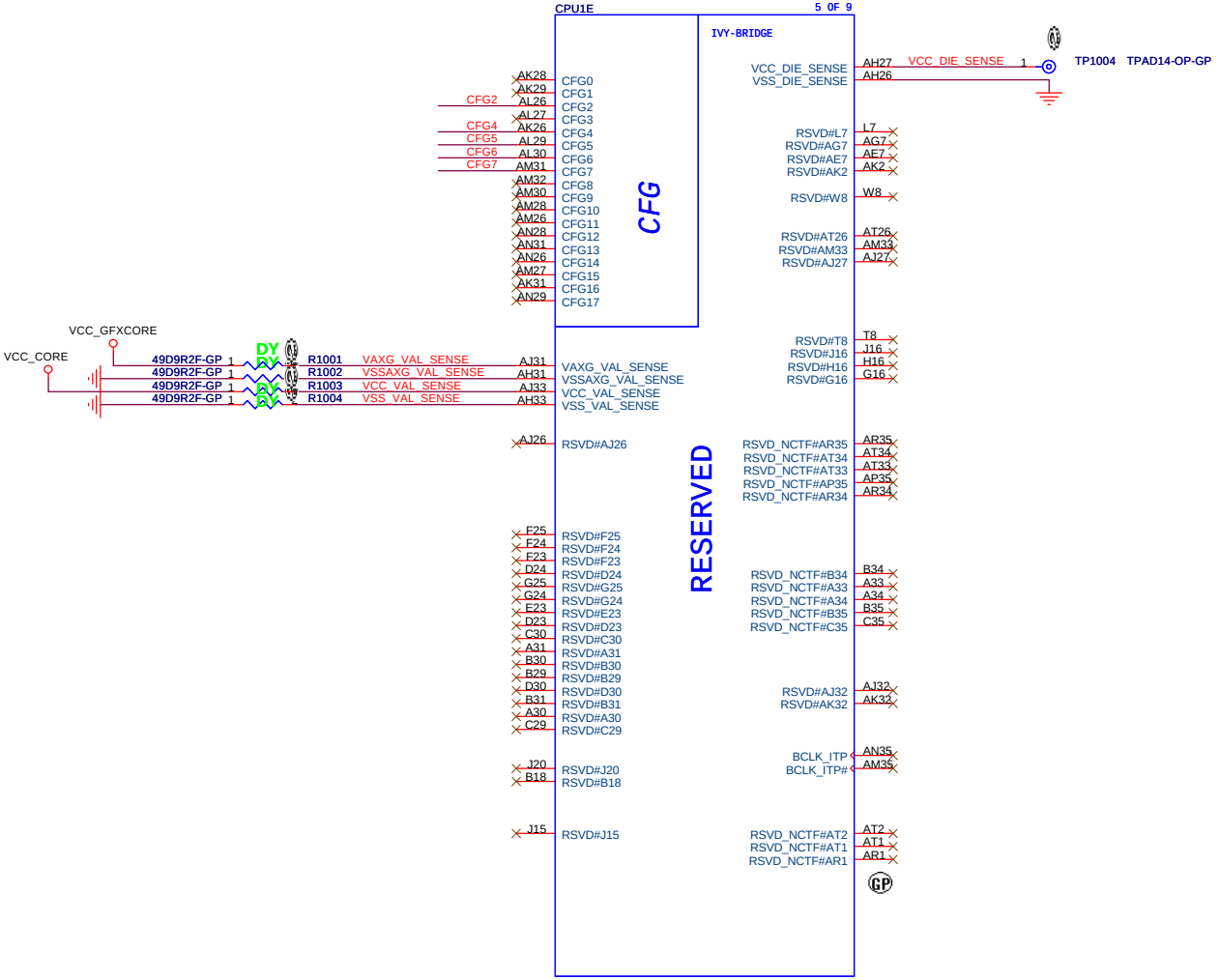
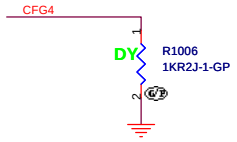
Title: CPU (6/7):GND		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 9 of 103	

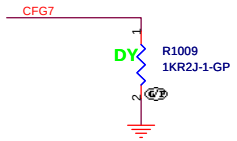
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

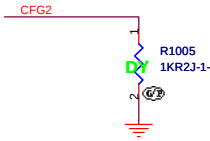




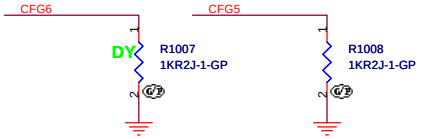
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(7/7): CFG/RSVD/DDR3_VRE

Size	Document Number	Rev
A3	Colossus	1

Date: Tuesday, December 27, 2011 Sheet 10 of 103

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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title		
CPU XDP		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 11 of 103	

(Blanking)

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Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 12 of 103

<Core Design>

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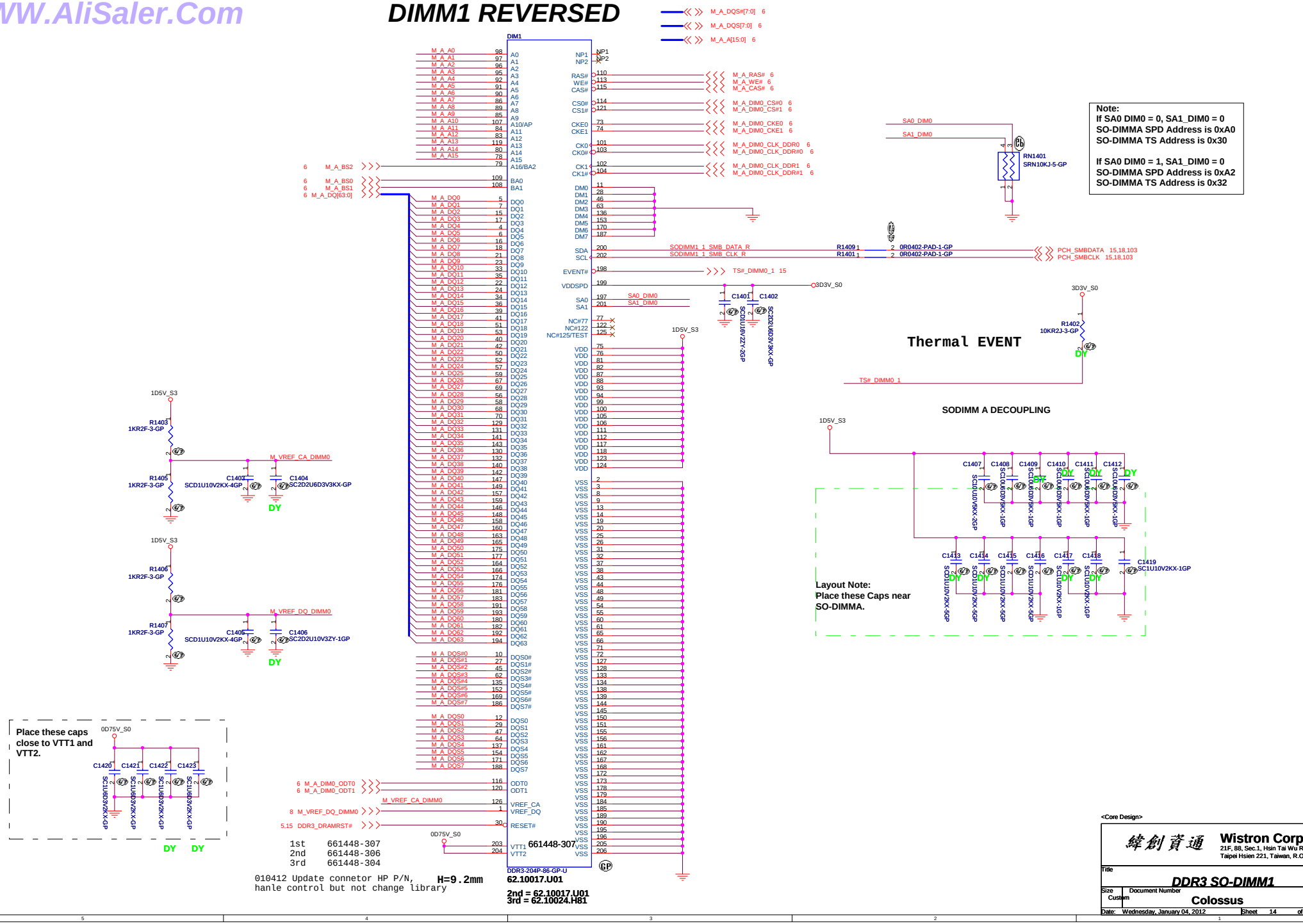
Title: ***AOAC***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 13 of 103

DIMM1 REVERSED



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

DIMM2 REVERSED

DIM2

DDR3-204P-85-GP-U

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

Place these caps close to VTT1 and VTT2.

1st 661447-301
2nd 661447-306
3rd 661447-304

010412 Update connetor HP P/N, hanle control but not change library

62.10017.U21
2ND = 62.10017.T91
3rd = 62.10024.I61
H=5.2mm

661447-301

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Title: DDR3 SO-DIMM2

Size: Custom | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 15 of 103

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
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Date: Monday, December 26, 2011 Sheet 16 of 103

PCH(1/9)

INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — PANTHER-GP-NF

RTC_AUX_S5 R1705 20KR2J-L2-GP C1701 SC1U10V2KX-1GP
RTC_X1 R1706 10MR2J-L-GP RTC_X2
X1701 82.30001.661 C1702 C1703 7pF20PPM SC6B8P50V2CN-GP
X-32D768KHZ-34GP
2ND = 82.30001.B21
R1708 20KR2J-L2-GP C1704 SC1U10V2KX-1GP G1701 GAP-OPEN
R1707 DY 330KR2J-L1-GP PCH_INTVRMEN
27,71 LPC_AD[0..3]

RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

LPC
FWH0/LAD0 C38 LPC_AD0_L
FWH1/LAD1 A38 LPC_AD1_L
FWH2/LAD2 B37 LPC_AD2_L
FWH3/LAD3 C37 LPC_AD3_L
FWH4/LFRAME# D36 LPC_FRAME#_R R1726 33R2J-2-GP LPC_FRAME# 27,71
LDRQ0# E36
LDRQ1#/GPIO23 K36 PCH_GPIO23 TP1701 TPAD14-OP-GP
SERIRQ V5 INT_SERIRQ 27
RN1705 SRN47J-8-GP
LPC_AD3_L LPC_AD2_L LPC_AD0_L LPC_AD1_L → LPC_AD3 LPC_AD2 LPC_AD0 LPC_AD1 27,71

RTC_AUX_S5 R1709 1MR2J-1-GP R1710 330KR2J-L1-GP
RN1701 SRN33J-7-GP R1711 0R0402-PAD-1-GP -1 1220
29 HDA_SDOUT_CODEC
29 HDA_BITCLK_CODEC
29 HDA_RST#_CODEC
29 HDA_SYNC_CODEC
29 HDA_SPKR
EC1701 EC1702 SC2200P50V2KX-1GP DY_PCH DY_PCH

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
PCH_HDA_SPKR T10 SPKR
PCH_HDA_RST# K34 HDA_RST#
HDA_SYNC_C
E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
29 HDA_SDIN0_CODEC
HDA_SDO A36 HDA_SDO
IHDA

SATA 6G
SATA0RXN AM3 SATA_RXN0 56
SATA0RXP AM1 SATA_RXP0 56
SATA0TXN AP7 SATA_TXN0 56
SATA0TXP AP5 SATA_TXP0 56 HDD1
SATA1RXN AM10 SATA_RXN1 103
SATA1RXP AM8 SATA_RXP1 103
SATA1TXN AP11 SATA_TXN1 103
SATA1TXP AP10 SATA_TXP1 103 mSATA
SATA2RXN AD7 SATA_RXN2 56
SATA2RXP AD5 SATA_RXP2 56
SATA2TXN AH5 SATA_TXN2 56
SATA2TXP AH4 SATA_TXP2 56 HDD2
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7 SATA_RXN4 56
SATA4RXP Y5 SATA_RXP4 56
SATA4TXN AD3 SATA_TXN4 56
SATA4TXP AD1 SATA_TXP4 56 ODD
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11 1D05V_S0
SATAICOMPI Y10 SATA_COMP R1713 37D4R2F-GP
SATA3RCOMPO AB12 1D05V_S0
SATA3COMPI AB13 SATA3_COMP R1714 49D9R2F-GP
SATA3RBIAS AH1 RBIAS_SATA3 R1715 750R2F-GP
NEED TO PLACE CLOSE TO PCH
5V_S0 DY R1716 10KR2J-3-GP
SATALED# P3 SATA_LED# SATA_LED# 82
SATA0GP/GPIO21 V14 3D3V_S0 SATA0GP_GPIO21 22
SATA1GP/GPIO19 P1 PCH_GPIO19 R1731 10KR2J-3-GP
SATA

RN1704 SRN1KJ-11-GP-U
27 ME_UNLOCK
82 HDD_HALTLED
HDD_HALTLED_R C36 HDA_DOCK_EN#/GPIO33
ISO_PREP# N32 HDA_DOCK_RST#/GPIO13

27 RTCRST_ON Q1701 2N7002K-2-GP RTC_RST# R1737 100KR2J-1-GP R1736 2K2R2J-2-GP

PCH_JTAG_TCK_BUF J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

60 PCH_SPI_CLK T3 SPI_CLK
60 PCH_SPI_CS0 Y14 SPI_CS0#
TPAD14-OP-GP TP1702 SPI_CS1# T1 SPI_CS1#
60 PCH_SPI_MOSI V4 SPI_MOSI
60 PCH_SPI_MISO U3 SPI_MISO
SPI

3D3V_S5 R1724 1KR2J-1-GP HDA_SYNC
R1729 10KR2J-3-GP ISO_PREP#

RTC Battery

RTC1 ACES-CON2-18-GP 20.F1637.002
2ND = 20.F1864.002
+RTC_VCC R1720 1KR2J-1-GP
3D3V_AUX_S5 U1701 TS715FPT-GP RTC_AUX_S5
C1705 SC1U10V3ZY-6GP
83.R0304.B81
2ND = 83.R2004.C81

NO REBOOT STRAP

No Reboot Strap R1722	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S0 DY R1722 10KR2J-3-GP HDA_SPKR
R1723 10KR2J-3-GP INT_SERIRQ

5V_S0 R1730 10KR2J-3-GP HDA_SDO_G
84.05067.031
2ND = 84.00138.H31
3RD = 84.2N702.W31
HDA_SYNC_C HDA_SYNC
DMN5L06K-7-GP U1703

3D3V_S5
PCHXDP R1717 210R2F-L-GP PCH_JTAG_TMS
PCHXDP R1718 210R2F-L-GP PCH_JTAG_TDO
PCHXDP R1719 210R2F-L-GP PCH_JTAG_TDI
DY_PCHXDP RN1703 SRN100F-7-GP
PCH_JTAG_TMS PCH_JTAG_TDI PCH_JTAG_TDO
PCHXDP R1721 51R2J-2-GP PCH_JTAG_TCK_BUF
R1727 1KR2J-1-GP HDD_HALTLED_R
R1728 DY 20KR2J-L2-GP HDA_SDO

LAYOUT NOTE:
JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

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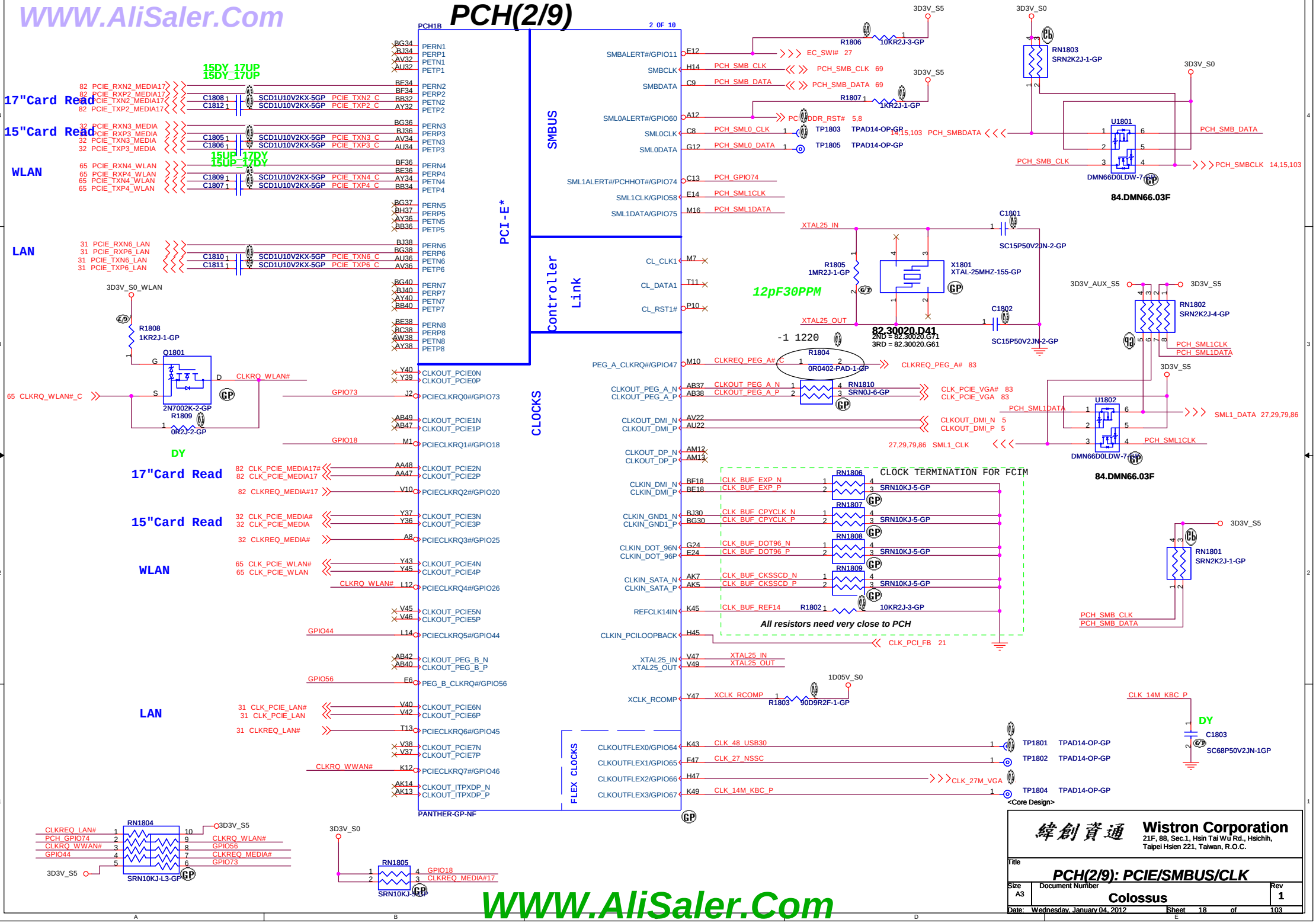
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: PCH(1/9): HDA/JTAG/SATA		
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 17 of 103	

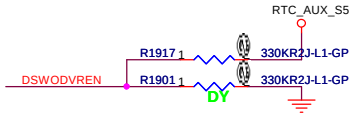
PCH(2/9)

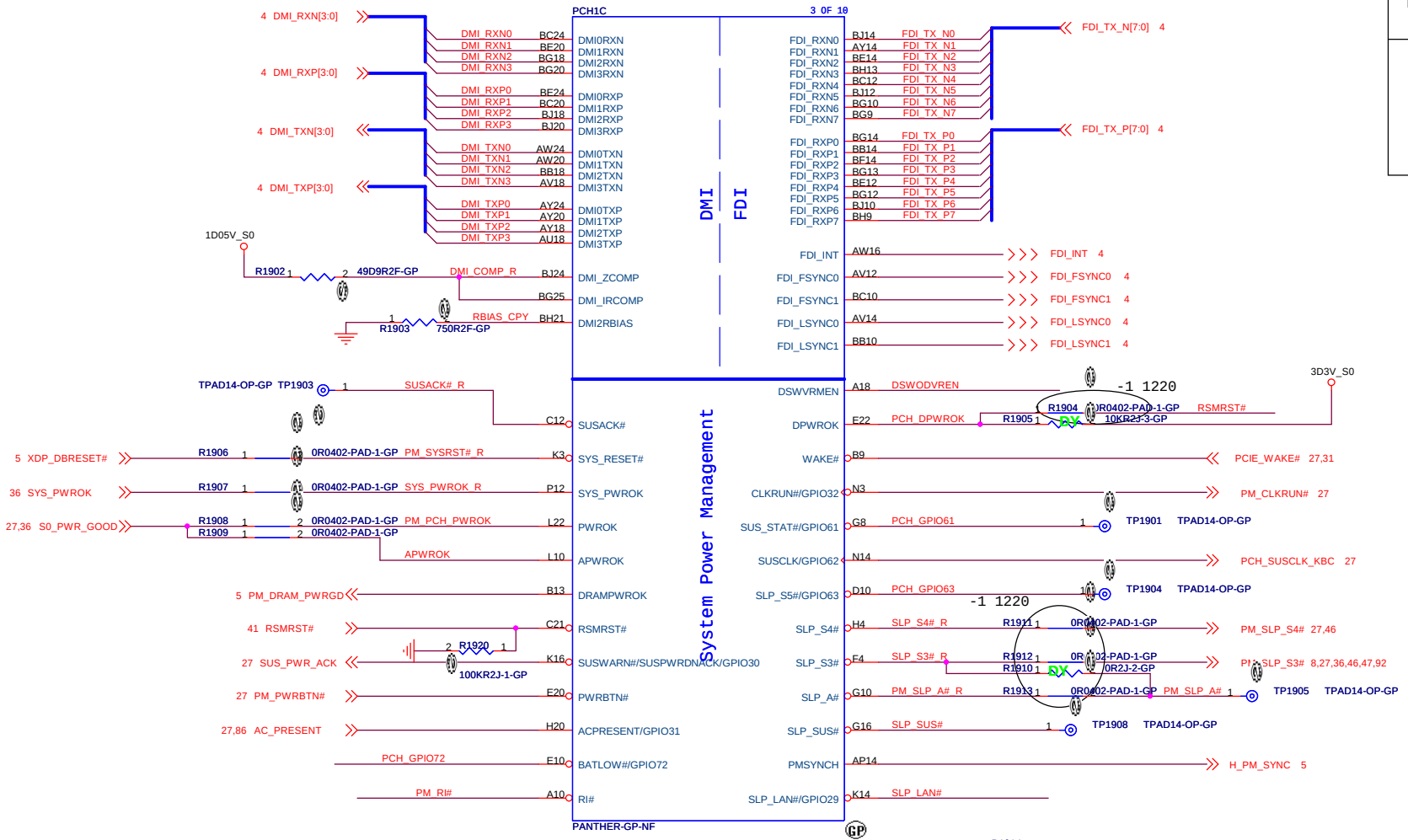


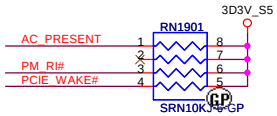
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH(2/9): PCIE/SMBUS/CLK	
Size A3	Document Number: Colossus	Rev 1
Date: Wednesday, January 04, 2012	Sheet 18 of 103	

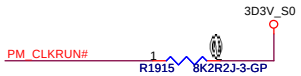
PCH(3/9)

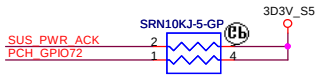
DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1917 UNSTUFFED, R1901 STUFFED	Disabled

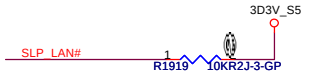












Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

<Core Design>

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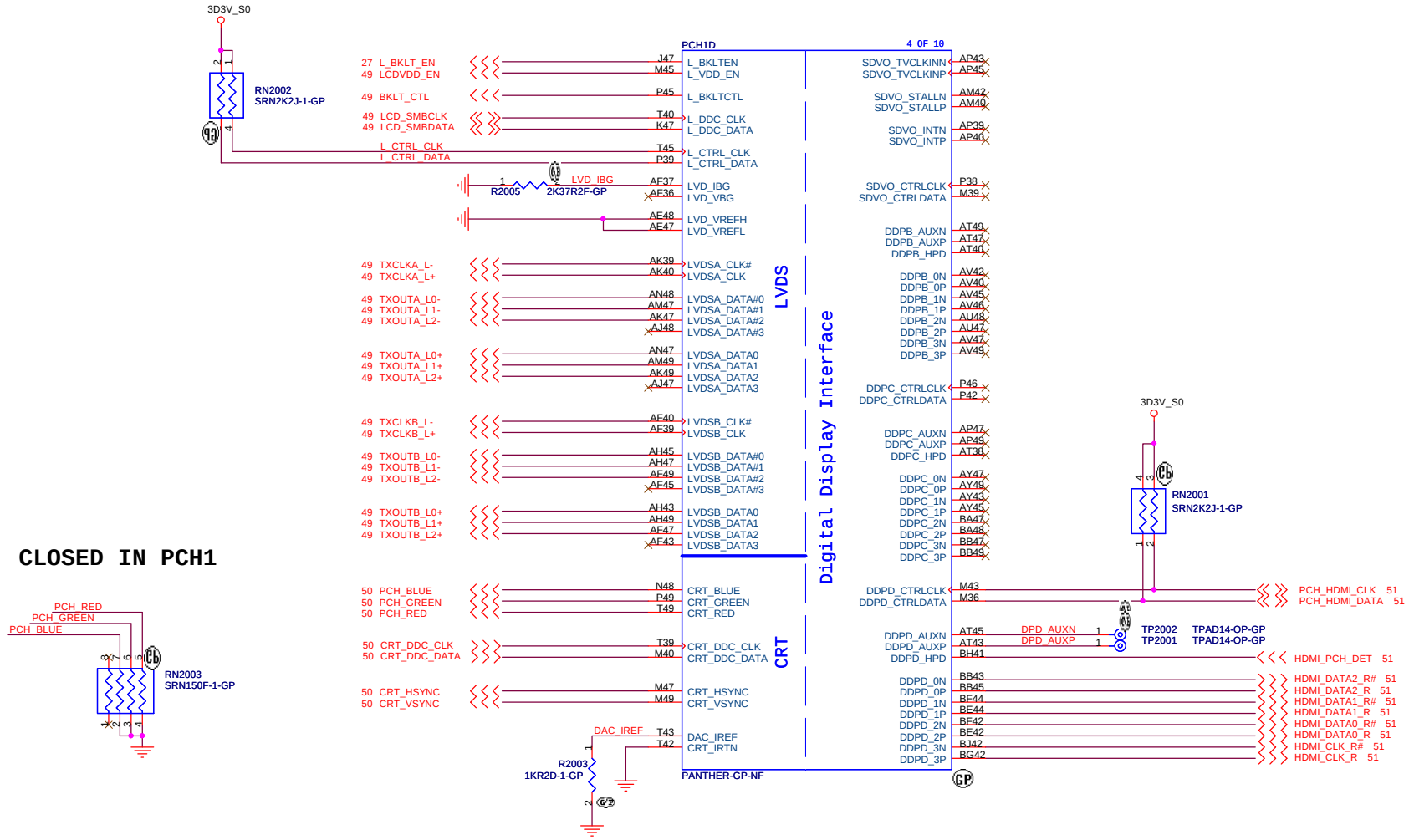
Title: PCH(3/9): DMI/FDI/PM

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 19 of 103

PCH(4/9)



CLOSED IN PCH1

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(4/9): LVDS/CRT/DDI

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 20 of 103

PCH(5/9)

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1 LEFT_DOWN
2	FREE
3	I/O CONN. 2 LEFT_UP
4	I/O CONN. 3 RIGHT_UP

USB2.0 Table

USB	
Pair	Device
0	USB 3.0 I/O CONN.
1	N/A
2	USB 3.0 I/O CONN.
3	USB 3.0 I/O CONN.
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 CONN(Debug)
10	Camera
11	FREE
12	FREE
13	FREE

USB 3.0 Conn. 1
USB 3.0 Conn. 2
USB 3.0 Conn. 3 (UB1)
BT WLAN combo
Fingerprint
USB 2.0 Conn. 1 (UB1)
Camera

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

AND GATE

73.01G08.L04
2ND = 73.7SZ08.EAH
3RD = 73.7SZ08.DAH

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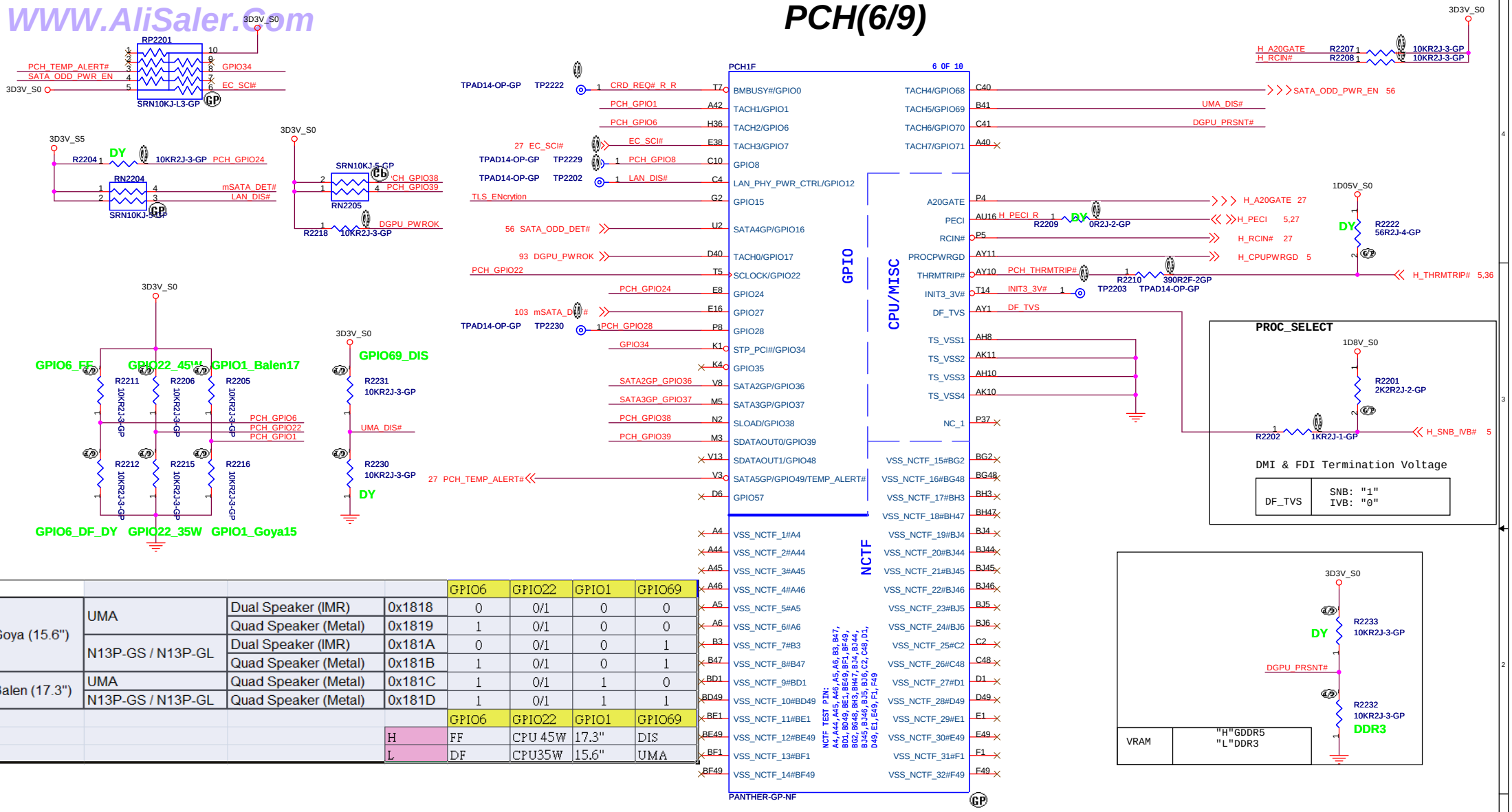
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(5/9): PCI/USB/NVM
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 21 of 103

PCH(6/9)



				GPIO6	GPIO22	GPIO1	GPIO69
Goya (15.6")	UMA	Dual Speaker (IMR)	0x1818	0	0/1	0	0
		Quad Speaker (Metal)	0x1819	1	0/1	0	0
	N13P-GS / N13P-GL	Dual Speaker (IMR)	0x181A	0	0/1	0	1
		Quad Speaker (Metal)	0x181B	1	0/1	0	1
Balen (17.3")	UMA	Quad Speaker (Metal)	0x181C	1	0/1	1	0
	N13P-GS / N13P-GL	Quad Speaker (Metal)	0x181D	1	0/1	1	1
				GPIO6	GPIO22	GPIO1	GPIO69
			H	FF	CPU 45W	17.3"	DIS
			L	DF	CPU35W	15.6"	UMA

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

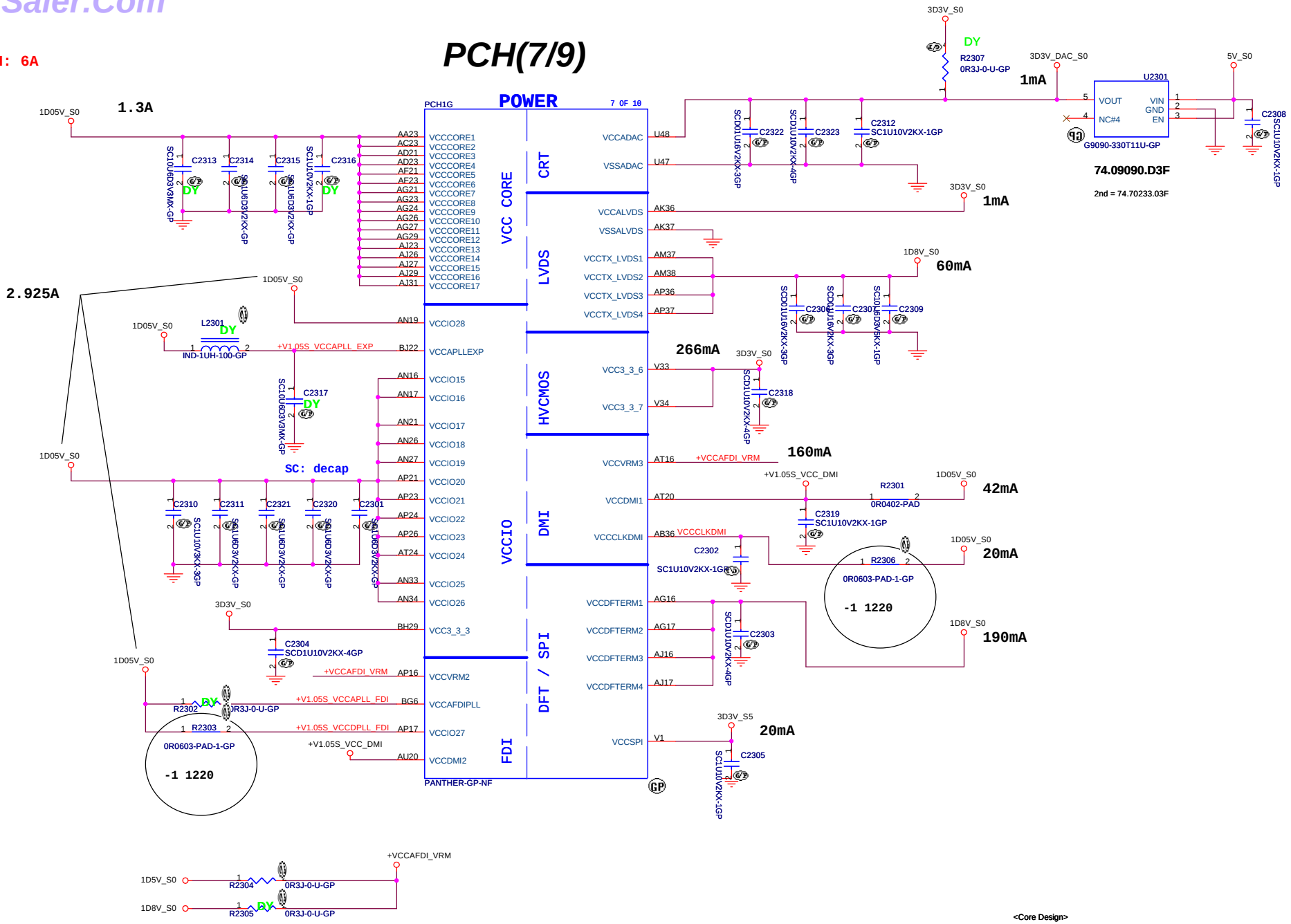
Title: PCH(6/9): GPIO/NTCF/RSVD

Size: A3 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 22 of 103

PCH(7/9)

VCC_PCH: 6A



<Core Design>

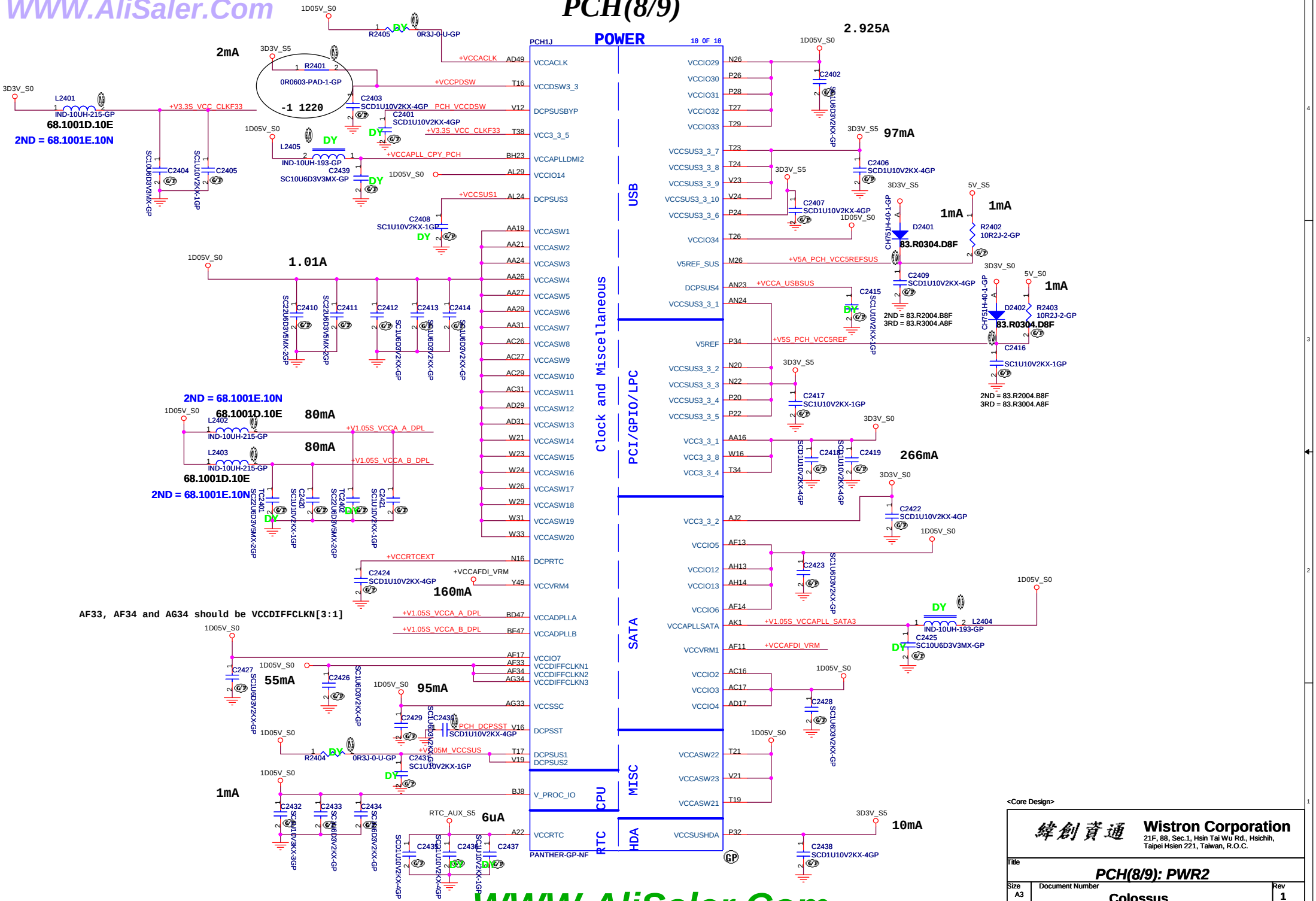
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(7/9): PWR1

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 23 of 103

PCH(8/9)



<Core Design>

Wistron Corporation
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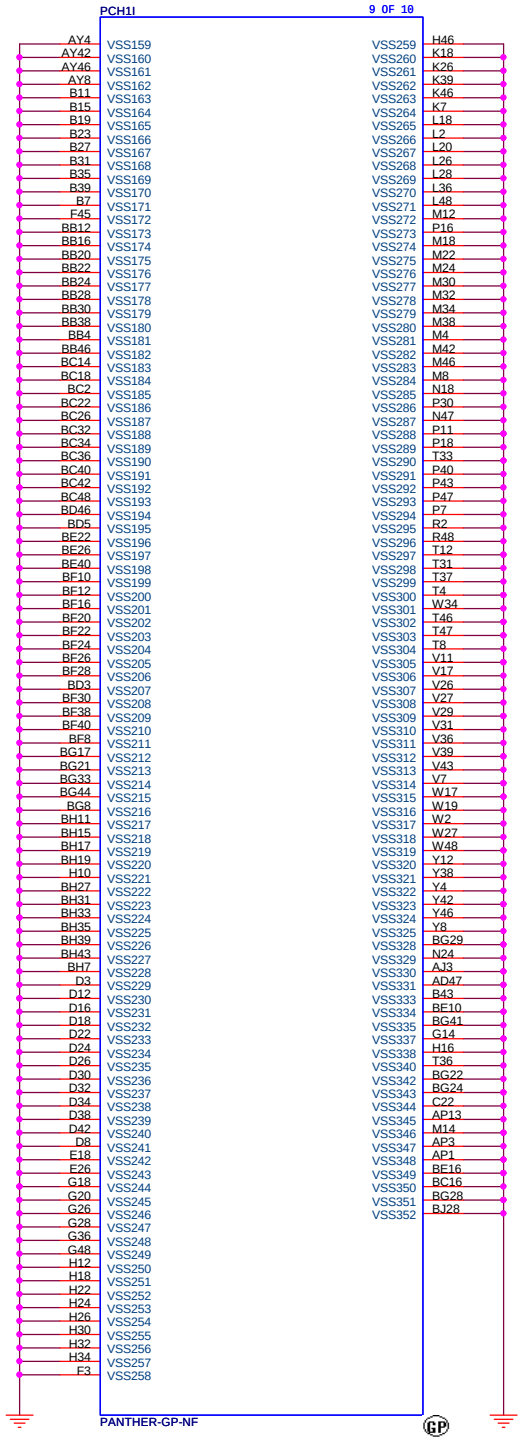
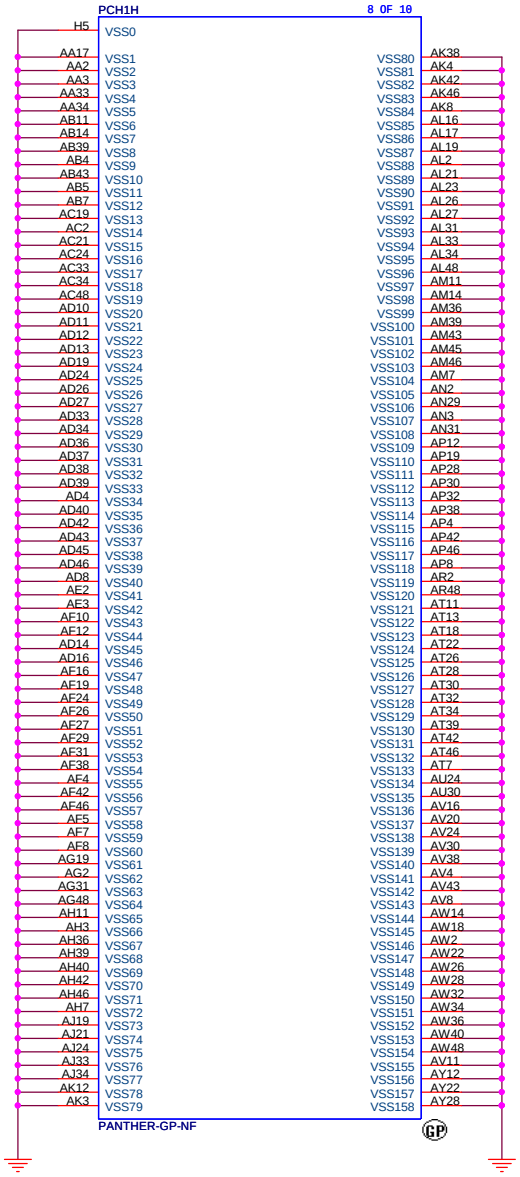
Title: PCH(8/9): PWR2

Size	Document Number	Rev
A3	Colossus	1

Date: Tuesday, December 27, 2011 Sheet 24 of 103

PCH(9/9)





<Core Design>

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Title: **PCH(9/9): GND**

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 25 of 103

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Title: PCH XDP		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 26 of 103	

SSID = KBC

U2701

20110608 for vendor debug

KB9016QF-A3-GP
71.09016.B0G

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
!	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

MODEL ID

83.00355.F1F

Model_ID	Model_ID (SI2)	Pull-Low Register	Pull-High Register	Typical Voltage
Goya(15.6")	UMA	UMA (35W)	100.0 K	10.0 K	3.000 V
	UMA	UMA (45W)	100.0 K	20.0 K	2.750 V
Goya(15.6")	DIS	DIS GL (35W)	100.0 K	33.0 K	2.481 V
	DIS	DIS GL (45W)	100.0 K	47.0 K	2.245 V
Balen(17.3")	UMA	UMA (35W)	100.0 K	64.9 K	2.001 V
Balen(17.3")	DIS	DIS GL (35W)	100.0 K	76.8 K	1.867 V
Balen(17.3")	eserved for project u	DIS GL (45W)	100.0 K	100.0 K	1.650 V
Balen(17.3")	eserved for project u	DIS GT (35W)	100.0 K	143.0 K	1.358 V
Balen(17.3")	eserved for project u	DIS GT (45W)	100.0 K	174.0 K	1.204 V
Balen(17.3")	eserved for project u	UMA (45W)	100.0 K	215.0 K	1.048 V
Goya(15.6")	eserved for project u	DIS GT (35W)	100.0 K	237.0 K	0.979 V
Goya(15.6")	eserved for project u	DIS GT (45W)	100.0 K	261.0 K	0.914 V

Prevent BIOS data loss solution

Q2701 MMBT3906-4-GP
84.T3906.A11
2nd = 84.03906.F11

GPIO06-->PWRBTN

HP Limit Signal Detect

D2701 BAV99PT-GP-U
83.00099.K11
2ND = 83.00099.M11
3RD = 83.00099.T11

HP AIRLINE COMBO

EC GPIO standard PH/PL

RN2701 SRN4K7J-8-GP

RN2713 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

GPIO70-->PWR_CHG_ACOK# OW active

Q2703 2N7002K-2-GP
3RD = 84.2N702.W31
2ND = 84.07002.I31
84.2N702.J31

Wistron Corporation	緯創資通
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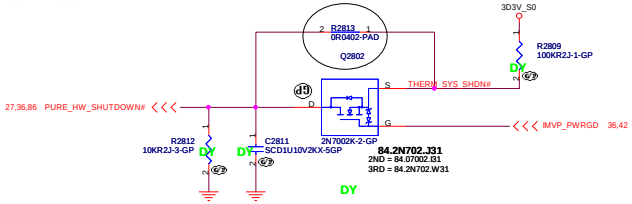
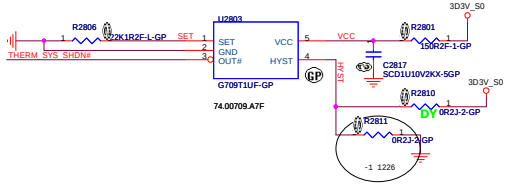
Title: EC CONTROLLER	
Size: A2	Document Number: Colossus	Rev: 1
Date: Thursday, January 05, 2012	Sheet 27 of 103

$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$

where T is the trip temperature in Centigrade. R_{SET} is the set- point resistance.



90 C

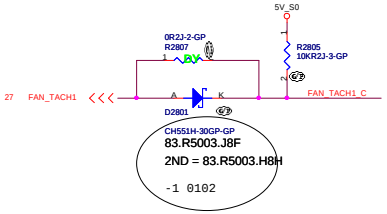


Global Mixed-mode Technology Inc. G709/G710

Pin Description

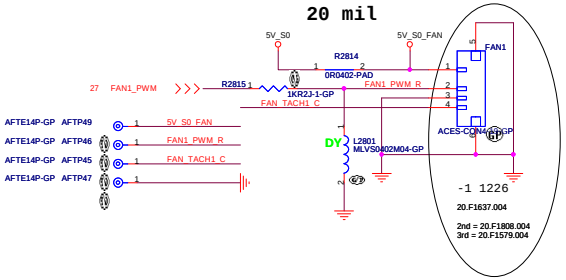
PIN		NAME	FUNCTION
G709	G710		
1	1	SET	Temperature Set Point, Connect an external 1% resistor from SET to GND to set trip point.
2	2	GND	Ground
3	3	$\overline{OT}$	Open-Drain Active Low Output.
4	4	HYST	Hysterisis Selection. Hysterisis is 10°C for HYST = V_{CC}, 2°C for HYST = GND.
	5	N.C.	Not Connected.
5	6	VCC	Power-Supply Input.

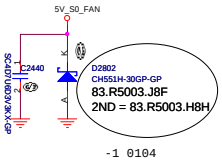
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
HYST Input Threshold	V_{IH}		0.7 x V_{CC}	---	---	V
	V_{IL}		---	---	0.3 x V_{CC}	V



FOR PWM FAN

20 mil





<Core Design>

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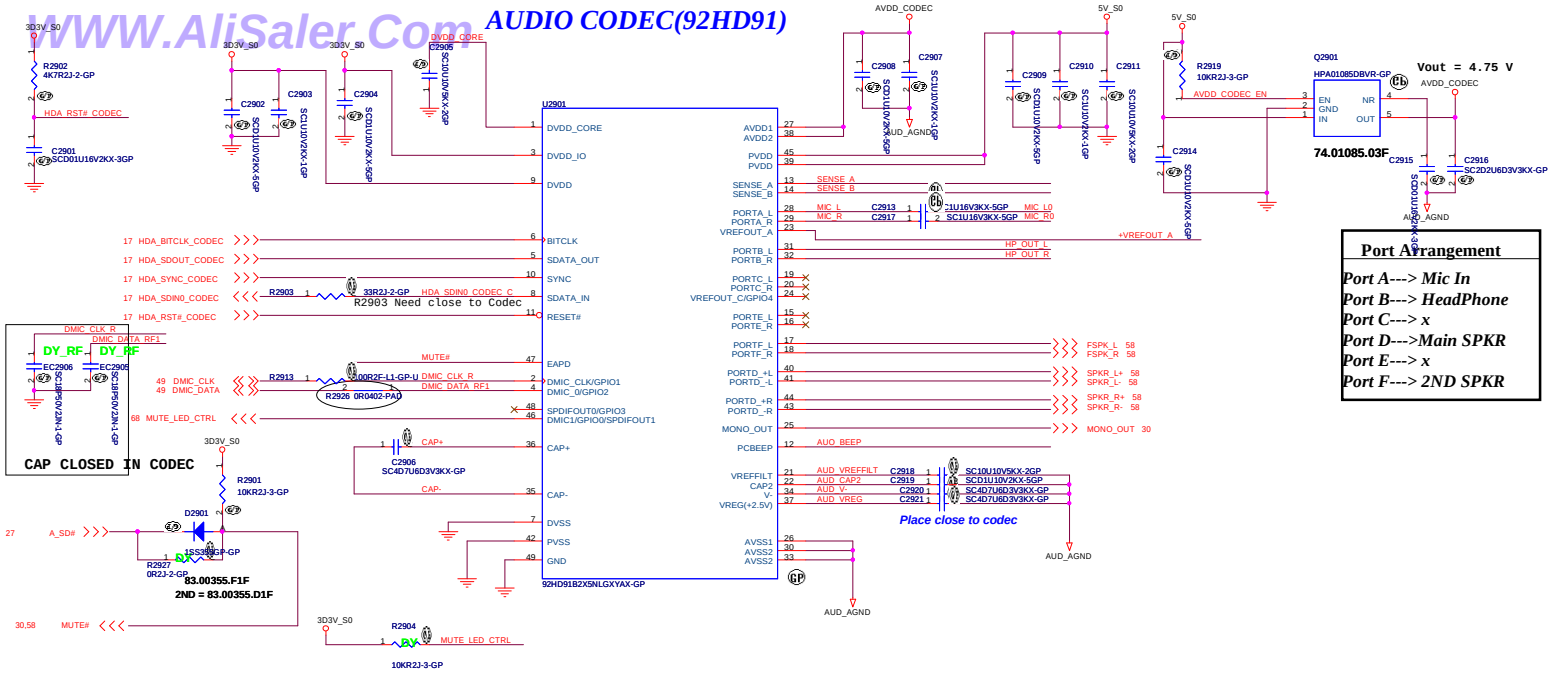
Title: Thermal/FAN

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 28 of 103

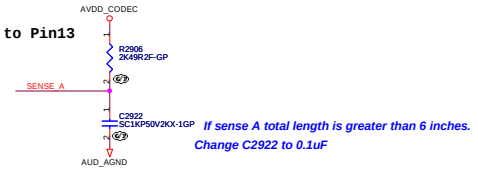
AUDIO CODEC(92HD91)



SENSE Detect

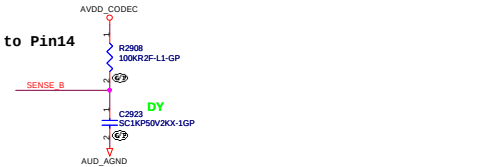
Headphone Trace = 15mil

Close to Pin13



If sense A total length is greater than 6 inches.
Change C2922 to 0.1uF

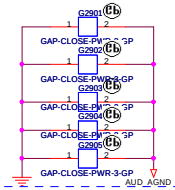
Close to Pin14



Digital GND & AUD_AGND

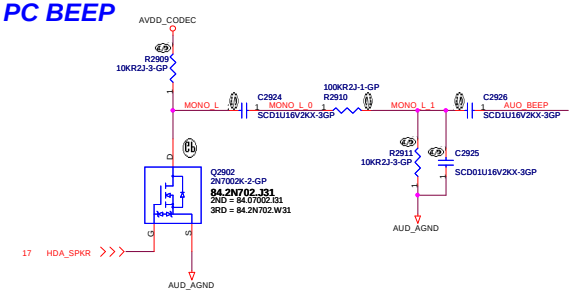
Tie Analog GND and Digital GND under codec by a single point

0818 IDT request
Place under U2901



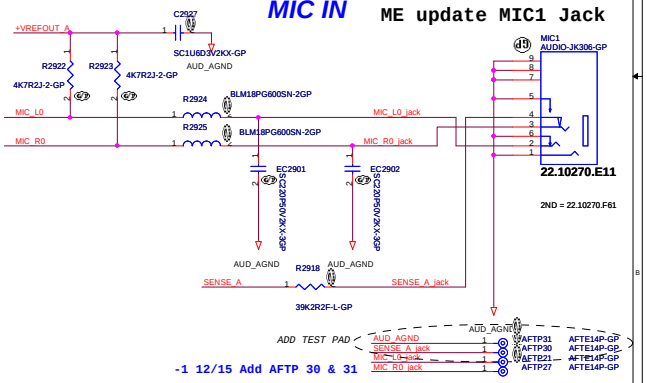
audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



MIC IN

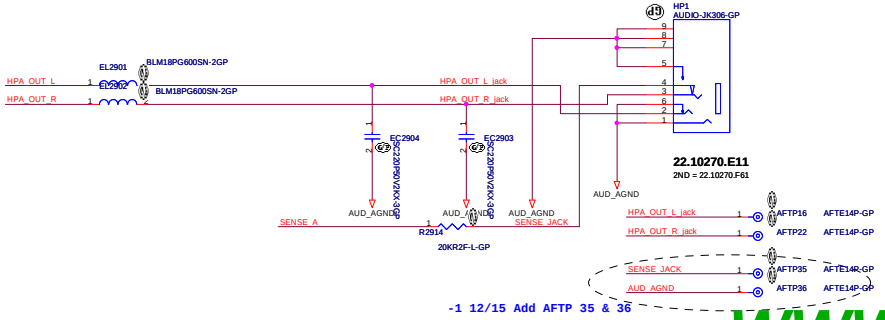
ME update MIC1 Jack



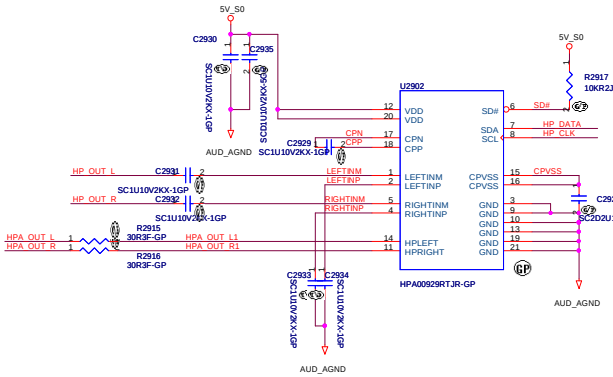
-1 12/15 Add AFTP 30 & 31

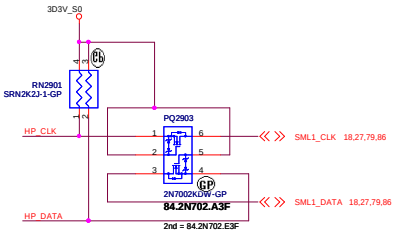
HeadPhone

ME update HP1 Jack



-1 12/15 Add AFTP 35 & 36

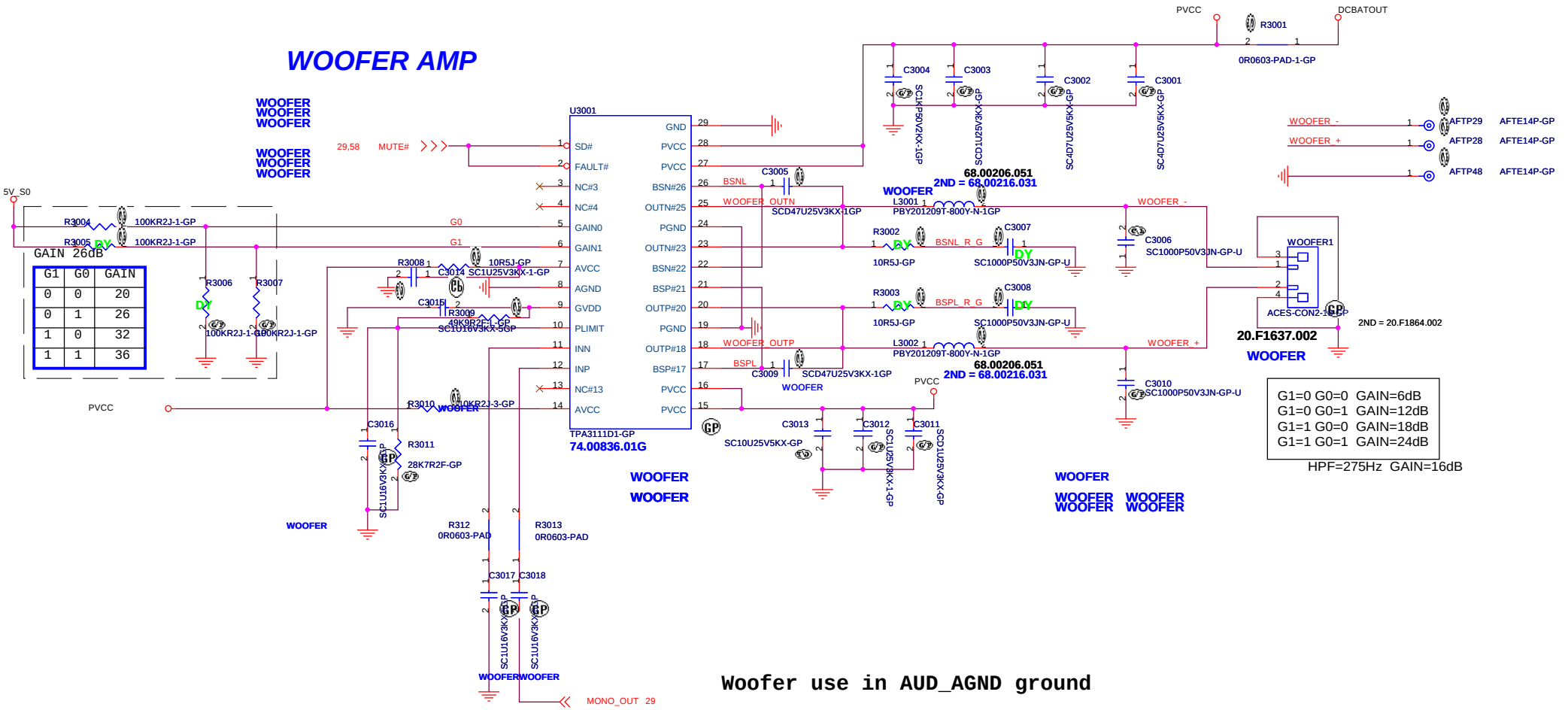




<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD91/HeadphoneAMP
Size: A2 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 29 of 103

WOOFER AMP



Woofer use in AUD_AGND ground

<Core Design>

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Title: ***Audio AMP SPK/WOOFER***

Size	Document Number	Rev
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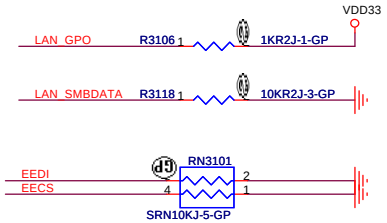
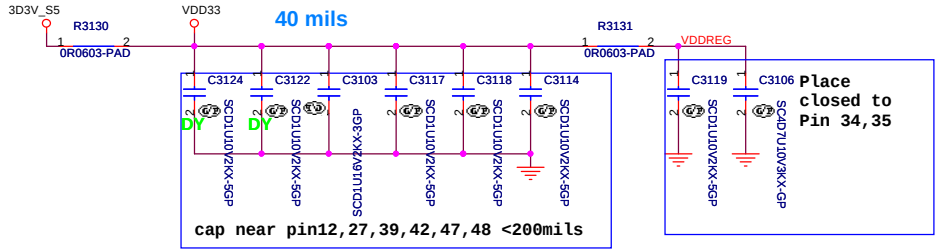
LAN CHIP-RTL8111F

USE EFuse No ASF

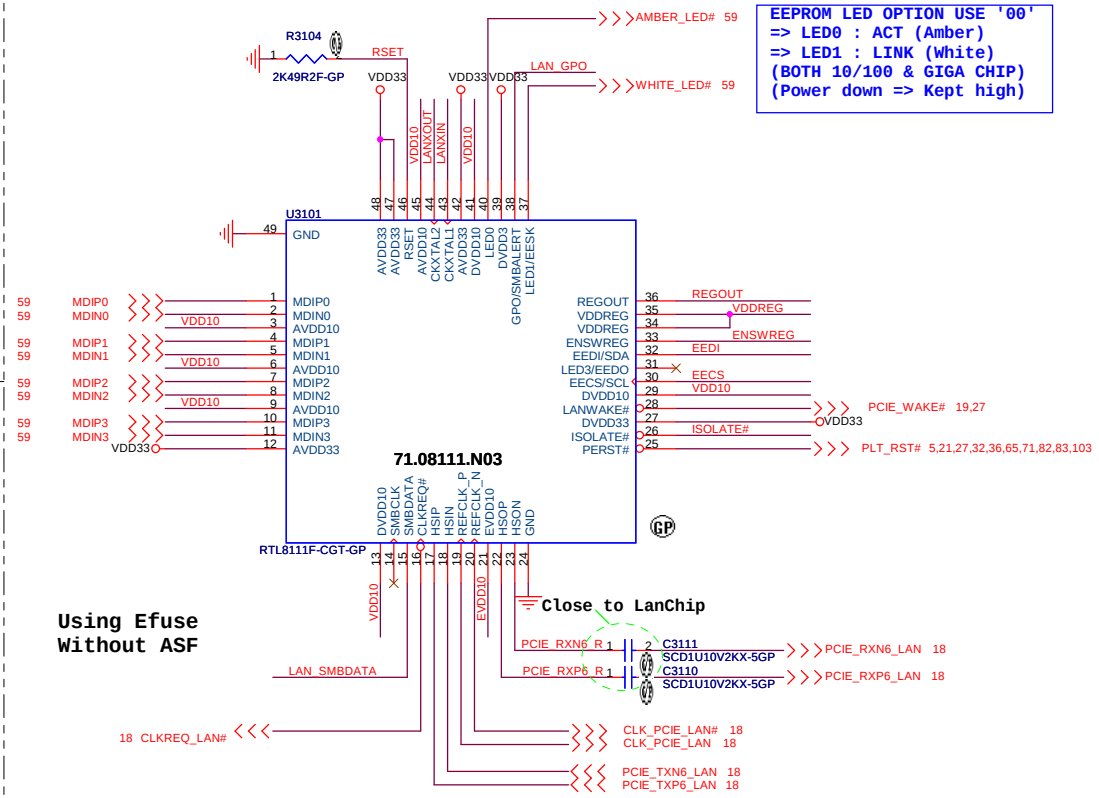




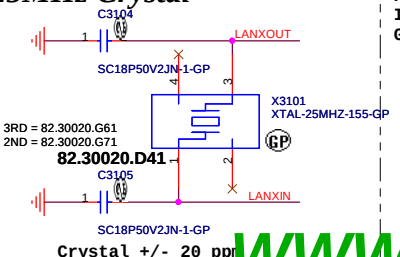
Avoid Leakage

LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS

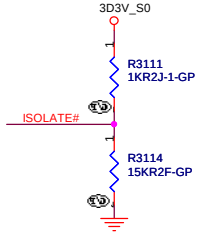


25MHz Crystal

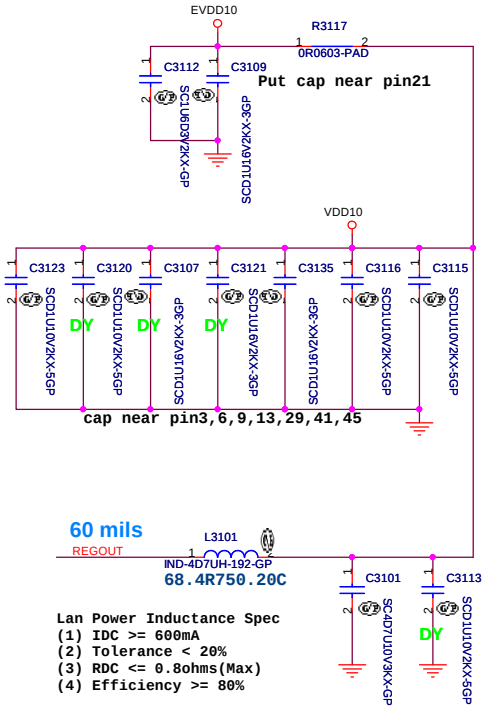


KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO => EFuse Strap Pin

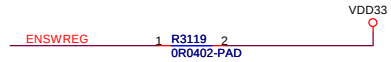
Isolate Strap Pin



Regout power plane(1D05V)



Regout Switch



ENSWREG (REGOUT 1D05V)
PH = Enable
PL = Disable

<Core Design>
緯創資通 Wistron Corporation
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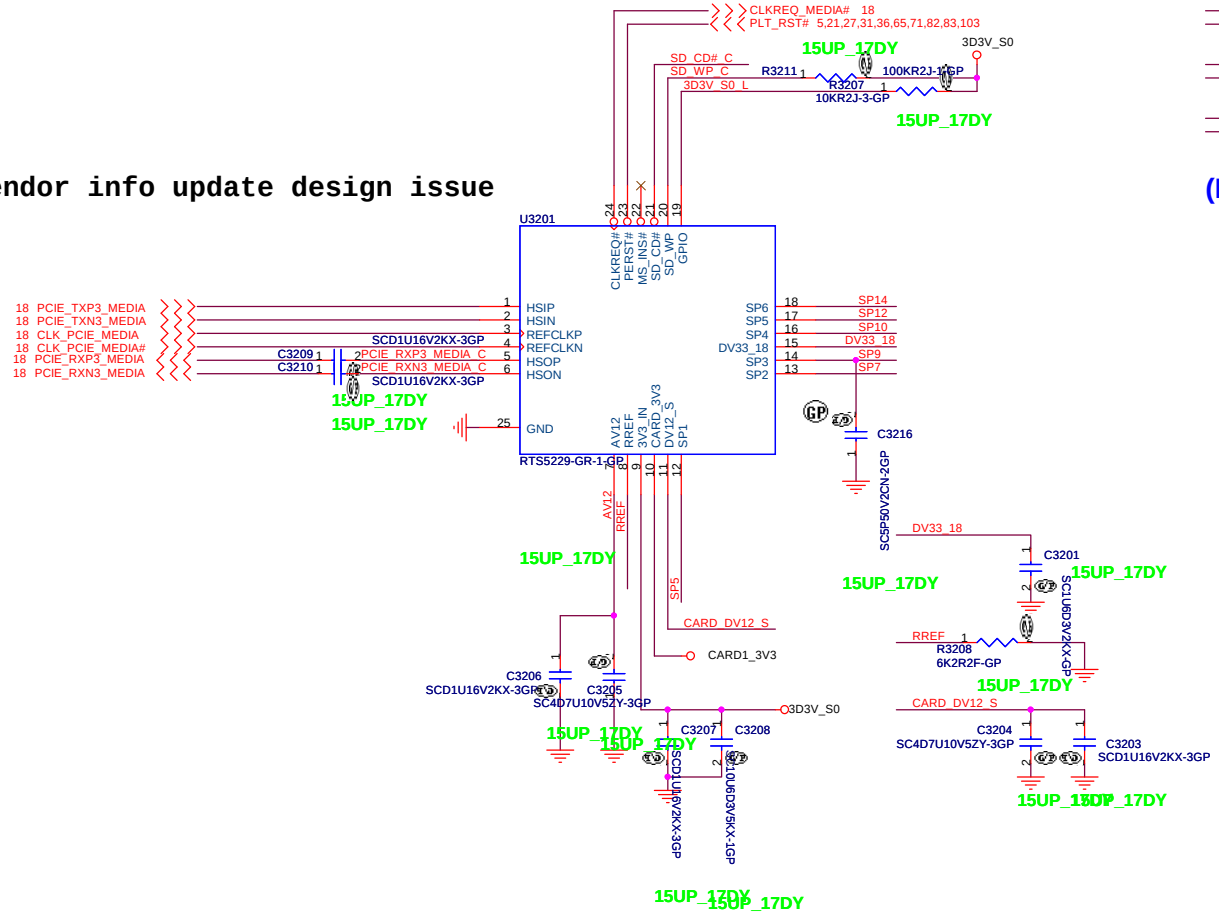
Title: LAN_RTL8111F
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 31 of 103

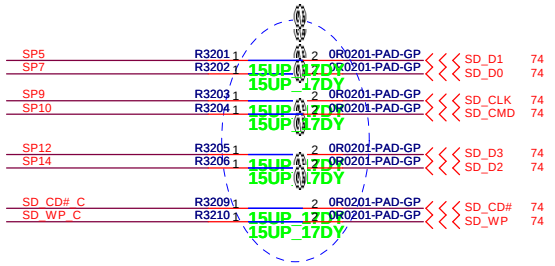
RTS5229

-1 12/15 0201 0 Ohm change to short pad

Vendor info update design issue



(RTS5229)U3201 closed near



<Core Design>

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Title: Card Reader-RTS5229

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 32 of 103

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<Core Design>

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Title: 1394		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 33 of 103	

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 34 of 103

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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Power Sequence

R3614
CRB 1K

28,42 IMVP_PWRGD — R3614 0R0201-PAD-GP — SYS_PWROK
SYS_PWROK 19
19,27 S0_PWR_GOOD — D3603 BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
C3612 SCD01U50V2KX-1GP
DY

R3623 0R0402-PAD
3D3V_S5
5,46,47 RUNPWROK
8,19,27,46,47,92 PM_SLP_S3#
U3608 74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
PWR_1D05V_1V_EN 45
DY

ANNIE Run Power

Run power follow TOP-1

DCBATOUT
R3619 330KR2J-L1-GP
RUN_ENABLE
R3622 0R0402-PAD
R3618 470R2J-2-GP
RUN_PWR_ON_G
C3615 SCD01U50V2KX-1GP
78.10324.2FL
D3602 MMPZ5239BPT-GP
83.9R103.D3F
2ND = 83.9R103.F3F

3D3V_AUX_S5
R3612 100KR2J-1-GP
Q3603 DMN66D0LDW-7-GP
84.DMN66.03F
8,19,27,46,47,92 PM_SLP_S3#
PS_S3CNTRL

PS_S3CNTRL
0D75V_S0
R3621 22R2J-2-GP
Q3604 DMN66D0LDW-7-GP
84.DMN66.03F
R3620 220R2F-GP
1D5V_S0

5V_S0
C3607 SCD1U25V2KX-GP
U3604 QM3004M3-GP
C3608 SCD1U25V2KX-GP
84.30043.037
2nd = 84.02657.037
5V_S5

3D3V_S0
C3616 SCD1U25V2KX-GP
U3607 QM3004M3-GP
C3609 SCD1U25V2KX-GP
84.30043.037
2nd = 84.02657.037
3D3V_S5

1D5V_S0
C3611 SCD1U25V2KX-GP
U3605 TPCA8062-H-GP
C3610 SCD1U25V2KX-GP
84.08062.037
2ND = 84.00460.037
1D5V_S3

-1 0103 check Power list

5V_S0
C3613 SCD1U10V2KX-5GP
5V_S5
C3614 SCD1U10V2KX-5GP

5V_S0
R3624 1KR2J-1-GP
Q3605 2N7002K-2-GP
PS_S3CNTRL

1D5V_S0
MAX Current 3000 mA
Design Current 2100 mA

Total= 11.39A

H_THRMTRIP# 5,22
H_PWRGD_R
MMBT2222ALT1G-GP
Q3601
84.02222.X11
2ND = 84.02222.V11
C3602 SCD1U10V2KX-5GP
5,21,27,31,32,65,71,82,83,103 PLT_RST#
R3616 4K7R2J-2-GP
R3632 2K2R2J-2-GP
83.R0304.D8F
2ND = 83.R2004.B8F
3RD = 83.R3004.A8F
41 3V_5V_EN
D3601 CH751H-40-1-GP
R3603 2KR2F-3-GP
R3602 200KR2J-L1-GP
DY
PURE_HW_SHUTDOWN# 27,28,86
S5_ENABLE 27

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 36 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size: A3 | Document Number: Colossus | Rev: 1

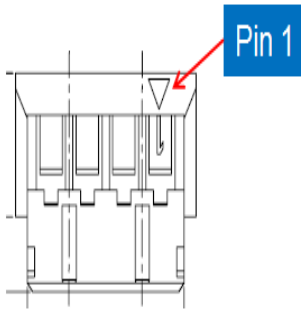
Date: Monday, December 26, 2011 | Sheet 37 of 103

Adaptor in to generate DCBATOUT

LIMIT_SIGNAL
AD_JK
AD+
PC3808 SC1KP50V2KX-1GP
PD3802 SM24DTCT-GP-U
PD3803 P6SMB27A-1-GP
DY
83.P6SMB.KAG
2ND = 83.P6SBM.DAG
PC3807 SCD1U50V3KX-GP
PU3802 SI7121DN-T1-GE3-GP
PWR_AD+_2
84.07121.037
2ND = 84.06675.030
PC3805 SC1KP50V2KX-1GP
EC3801 SCD1U25V2KX-GP
PR3807 200KR2F-L-GP
PC3806 SCD1U50V3KX-GP
PQ3802 PDTA124EU-1-GP
84.00124.K1K
PWR_ADJK_EN
PR3808 100KR2J-1-GP
DCIN1
DC_PIN2
DC_PIN1
LIMIT_SIGNAL
AD_JK
ACES-CON10D-4-GP
20.81633.010
2nd = 20.81772.010
1Pin=3A
83.0SM24.A11
2ND = 83.0024V.0A1
27 AD_OFF
PQ3801 PDTC124EU-1-GP
84.00124.H1K
2ND = 84.05124.011
40 PWR_ADJK_EN
2ND = 84.00024.01K

-1 1222 PR3802 to save 100mW when battery full.

Pin	Description	Wire color
Pin 1	White LED	White
Pin 2	Amber LED	Yellow
Pin 3	ID	Brown
Pin 4	GND	Black
Pin 5	GND	Black
Pin 6	GND	Black
Pin 7	-	
Pin 8	+VA	Red
Pin 9	+VA	Red
Pin 10	+VA	Red



PQ3803_C
PR3802 510R2J-1-GP
PL3801 MLVS0402M04-GP
PU3801
27 DC_BATFULL
CHARGE_LED 27
84.DM601.03F
DMN601DWK-7-GP
5V_AUX_S5
PR3811 510R2J-1-GP
PL3802 MLVS0402M04-GP
2nd = 84.2N702.E3F

ADD TEST PAD
PG3801 GAP-CLOSE-PWR
PG3802 GAP-CLOSE-PWR
PG3803 GAP-CLOSE-PWR
PG3804 GAP-CLOSE-PWR
PG3805 GAP-CLOSE-PWR
PG3806 GAP-CLOSE-PWR
PG3807 GAP-CLOSE-PWR
LIMIT_SIGNAL AFTP32 AFTE14P-GP
DC_PIN2 AFTP33 AFTE14P-GP
DC_PIN1 AFTP34 AFTE14P-GP
AD_JK
AFTP20 AFTE14P-GP
AFTP23 AFTE14P-GP
AFTP24 AFTE14P-GP
AFTP25 AFTE14P-GP
AFTP26 AFTE14P-GP
AFTP50 AFTE14P-GP

AC Present = White
Standby = White pulsing
Charging = Amber
***LED's are off if no AC jack pluged in**

AD_JK
PR3809 200KR2F-L-GP
PC3809 SCD1U50V3KX-GP
PR3810 34K8R2F-1-GP
27 AD_DETECT

-1 1222 PR3802 to save 100mW when battery full.

5V_AUX_S5
CHARGE_LED
PQ3804 2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.W31
PR3803 10KR2J-3-GP
PQ3803 MMBT3906-4-GP
84.T3906.A11
2nd = 84.C3906.A11
3rd = 84.03906.R11
PQ3803_C

<Core Design>

Wistron Corporation
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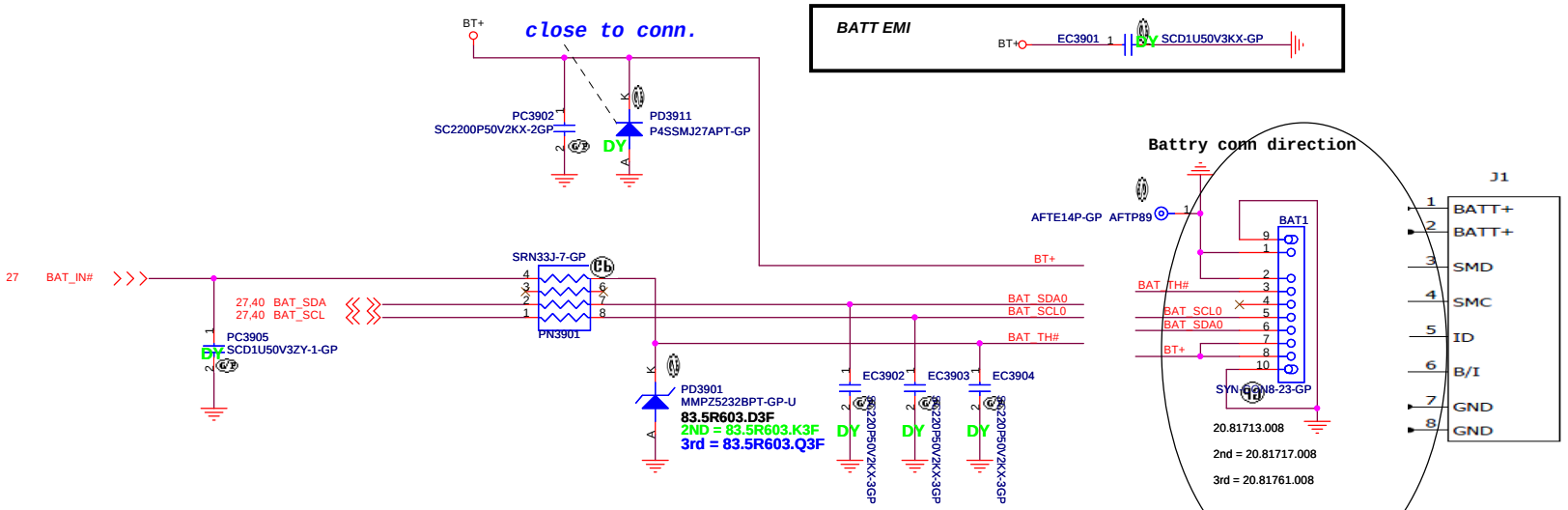
Taipei Hsien 221, Taiwan, R.O.C.

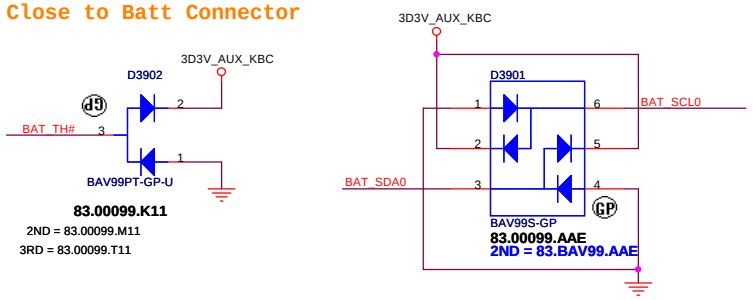
Title: DCIN JACK

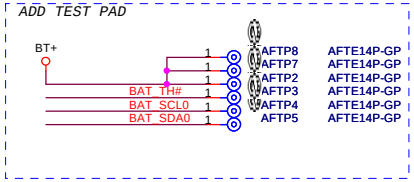
Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 38 of 103

BATT Connector



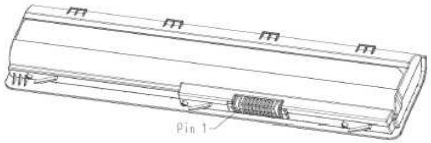




3. Interface

Connector ; 8pin
(Alltop C19029-10803-B, Foxconn BR0208C-B61H5-4H, Octek BTK-08ABEB)

Pin No.	Symbol	Description
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



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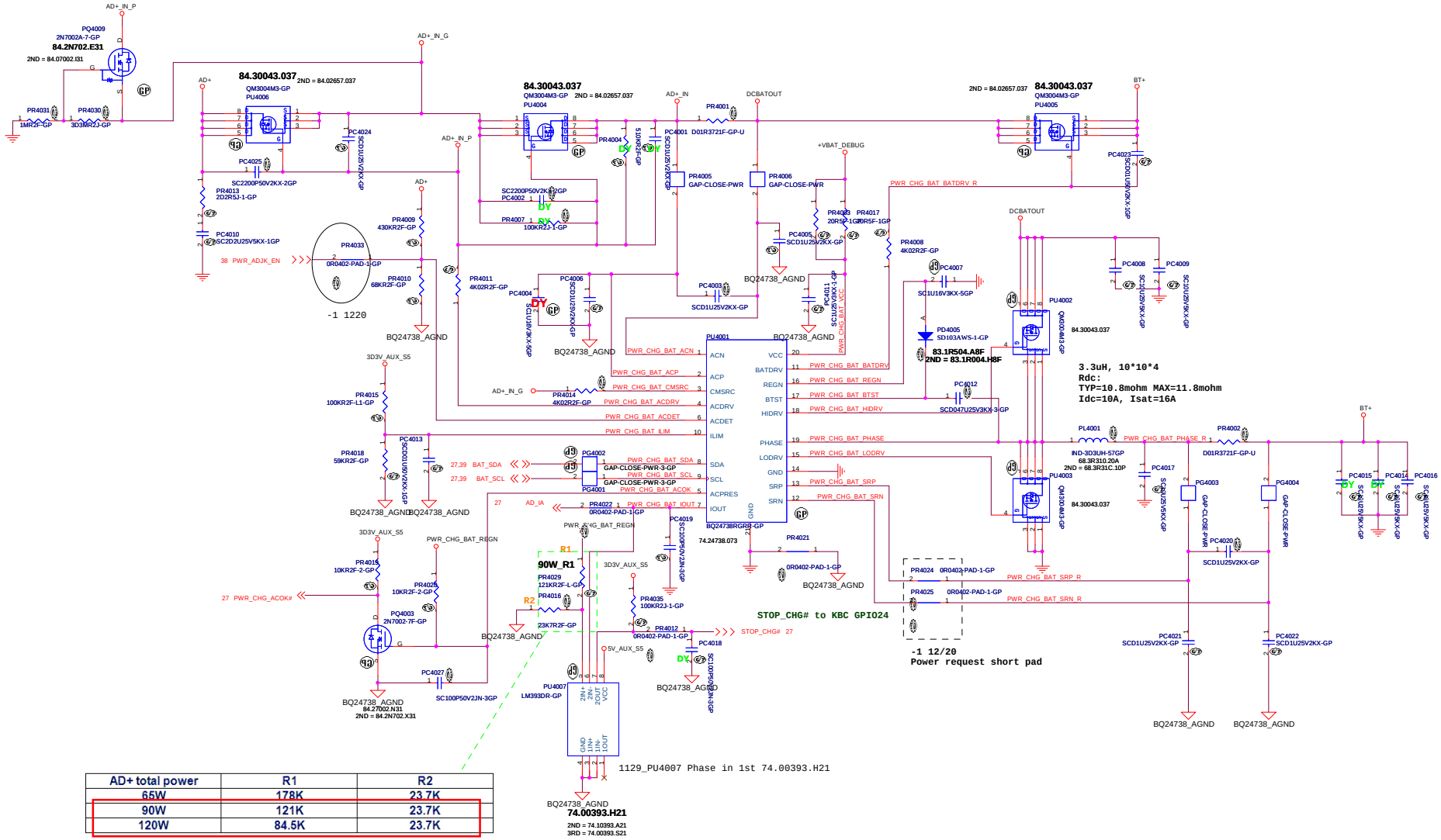
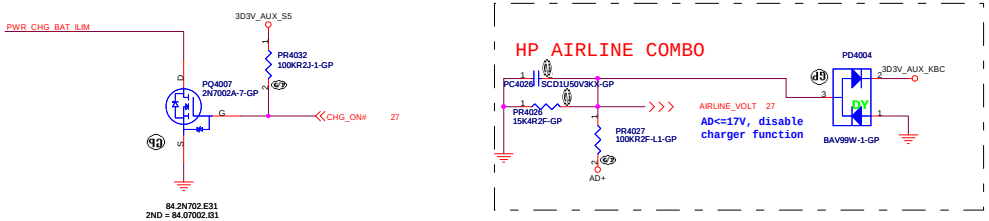
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 39 of 103



AD+ total power	R1	R2
65W	178K	23.7K
90W	121K	23.7K
120W	84.5K	23.7K



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24738

Size: A2 | Document Number: Colossus | Rev: 1

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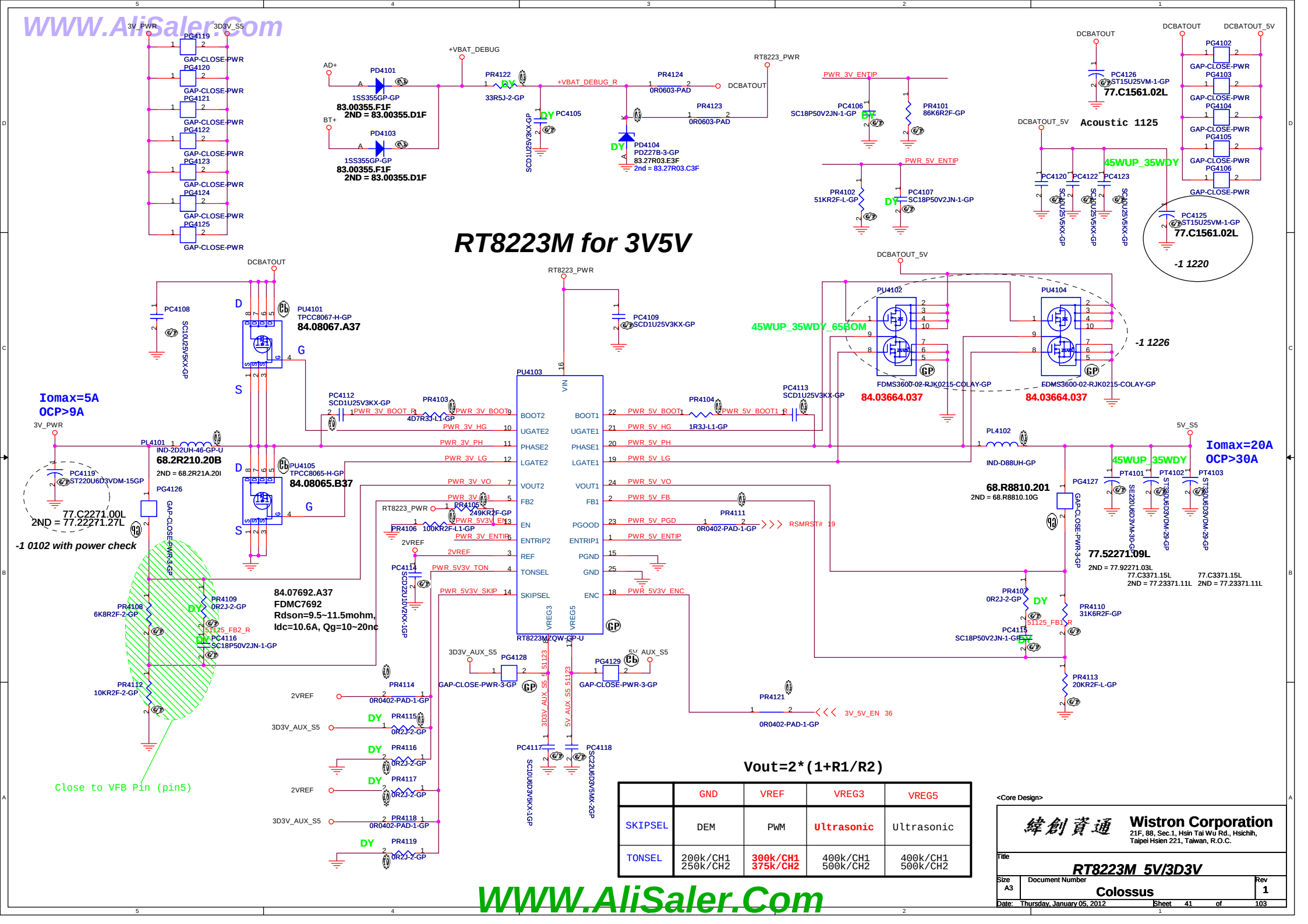
RT8223M for 3V5V



Vout=2*(1+R1/R2)

	GND	VREF	VREG3	VREG5
SKIPSEL	DEM	PWM	Ultrasonic	Ultrasonic
TONSEL	200k/CH1 250k/CH2	300k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223M 5V/3D3V

Size: A3 | Document Number: Colossus | Rev: 1

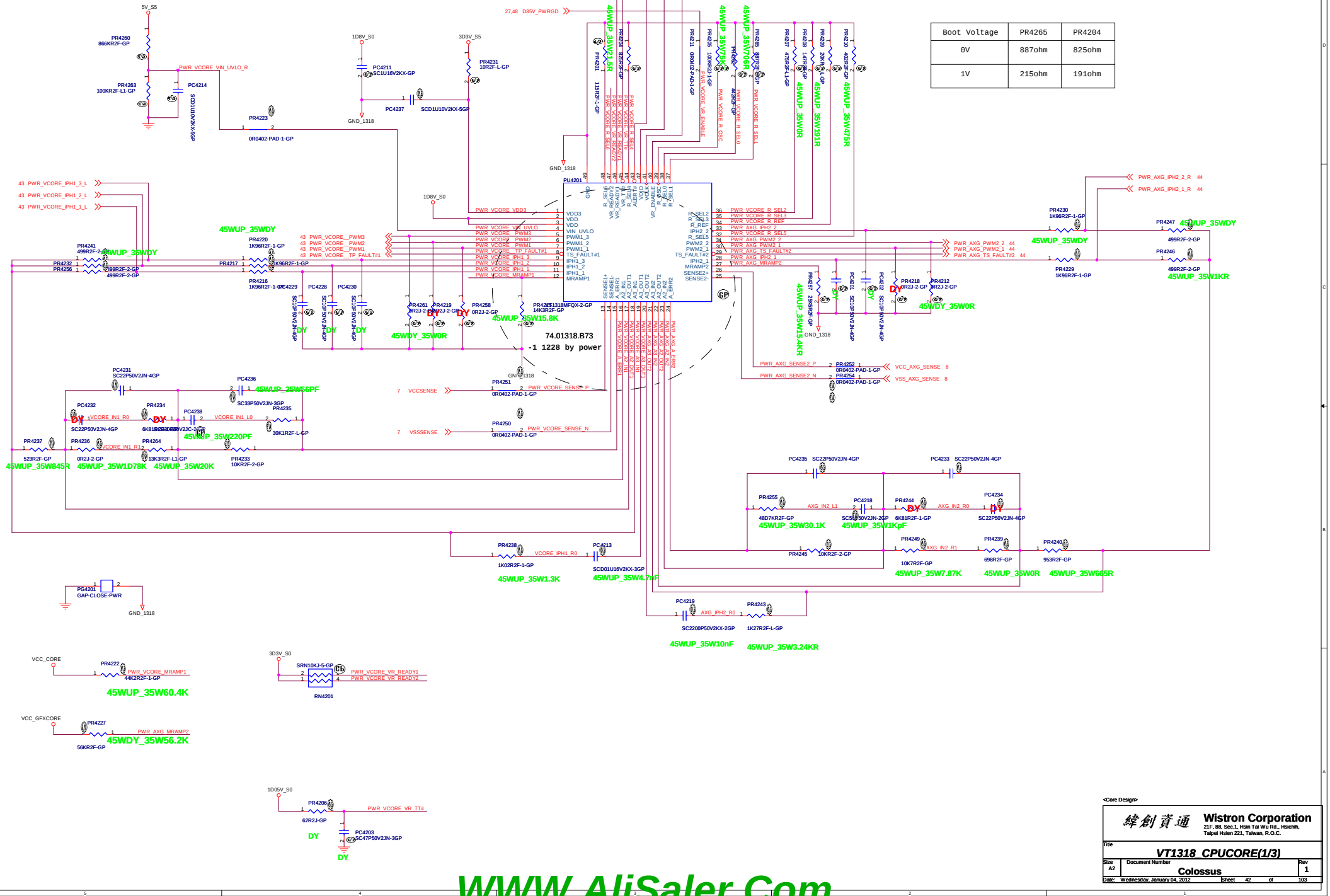
Date: Thursday, January 05, 2012 | Sheet 41 of 103

SSID = CPU.Regulator

Volterra's suggestion:
The total output MLCC is 30x22uF for 3-PHASE VCC
The total output MLCC is 20x22uF+4x10uF for 2-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm

74.01318.B73
-1 1228 by power



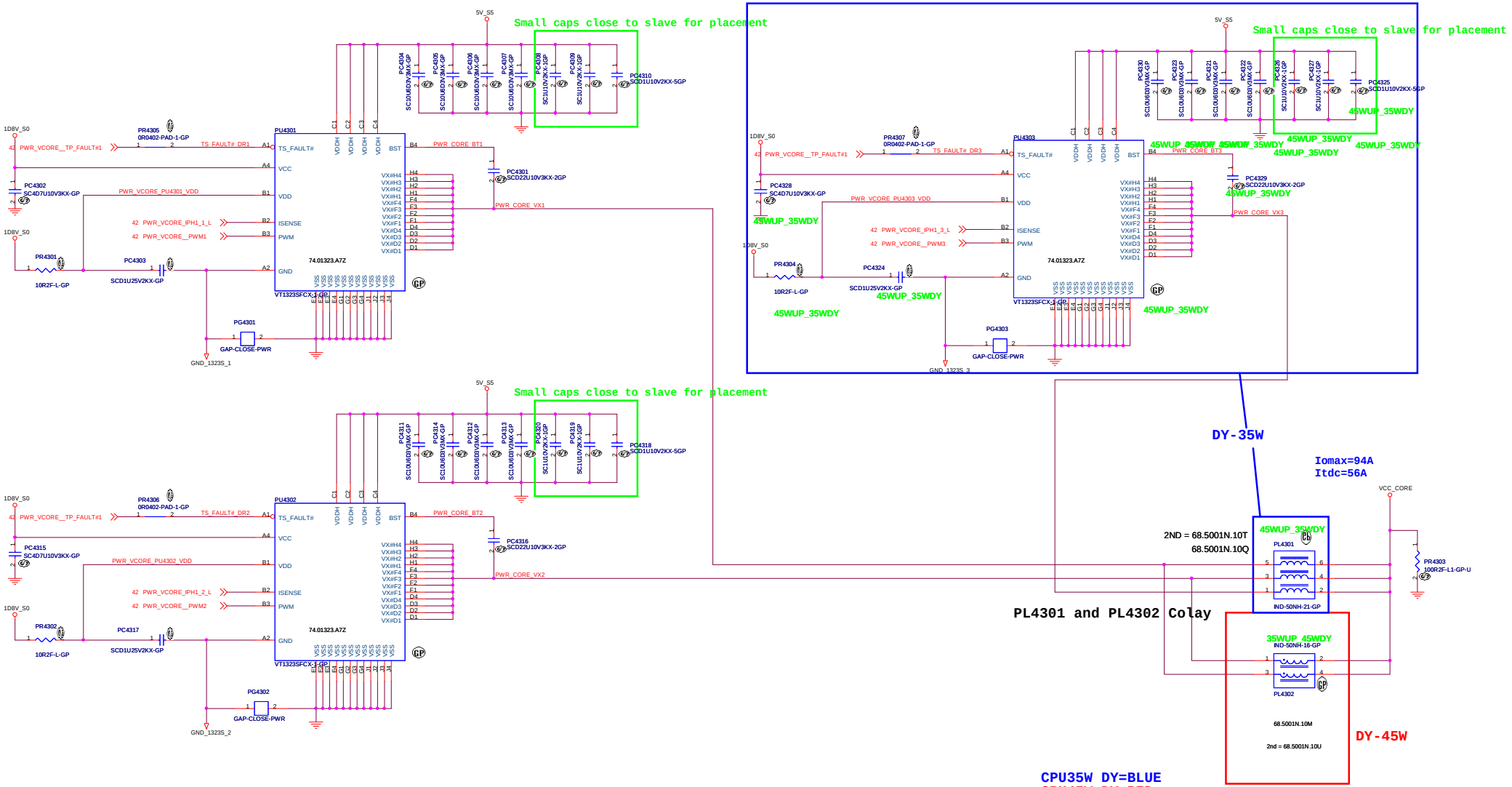
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1318_CPUCORE(1/3)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 42 of 103



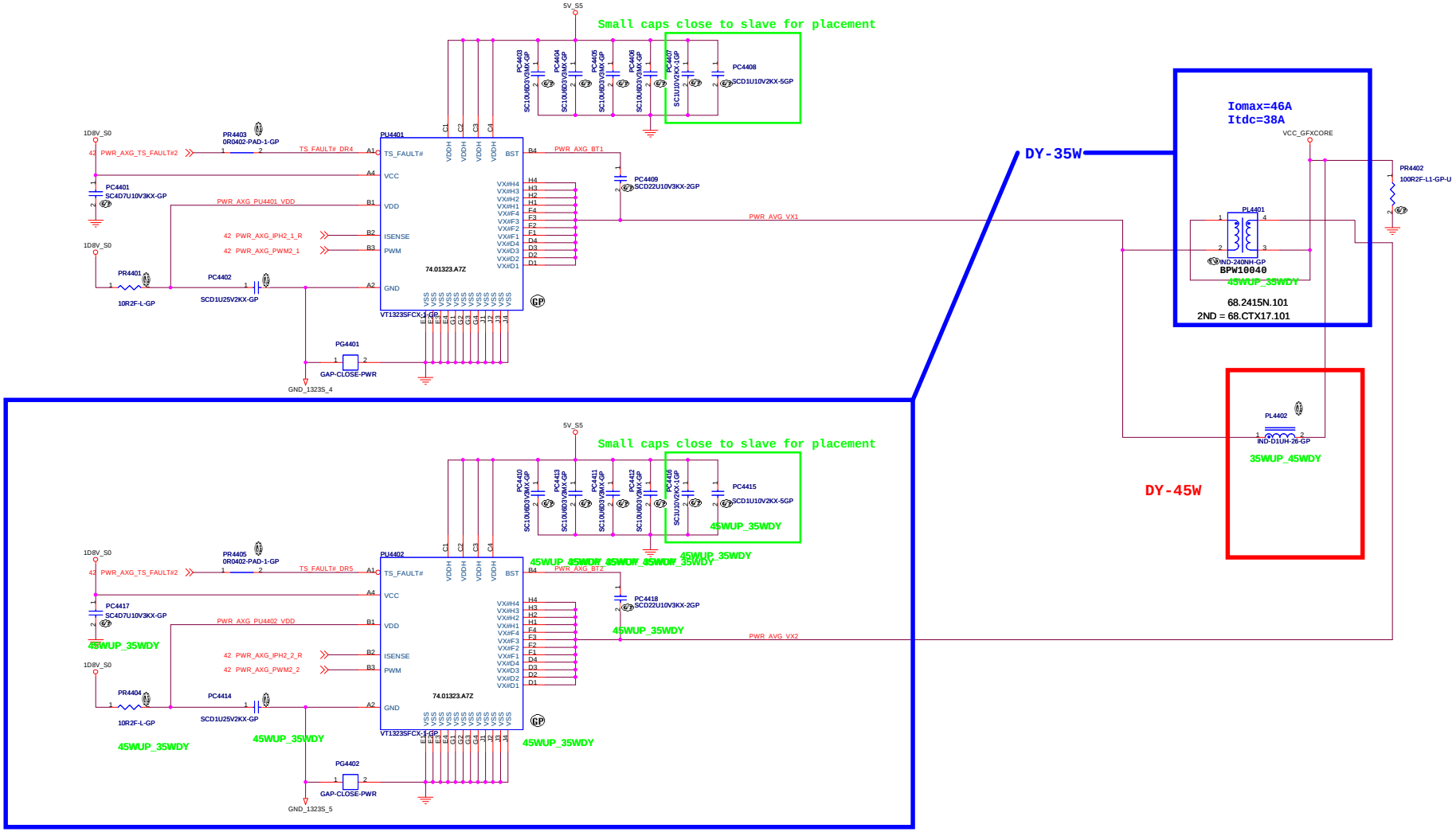
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1323_CPUCORE(2/3)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 43 of 103



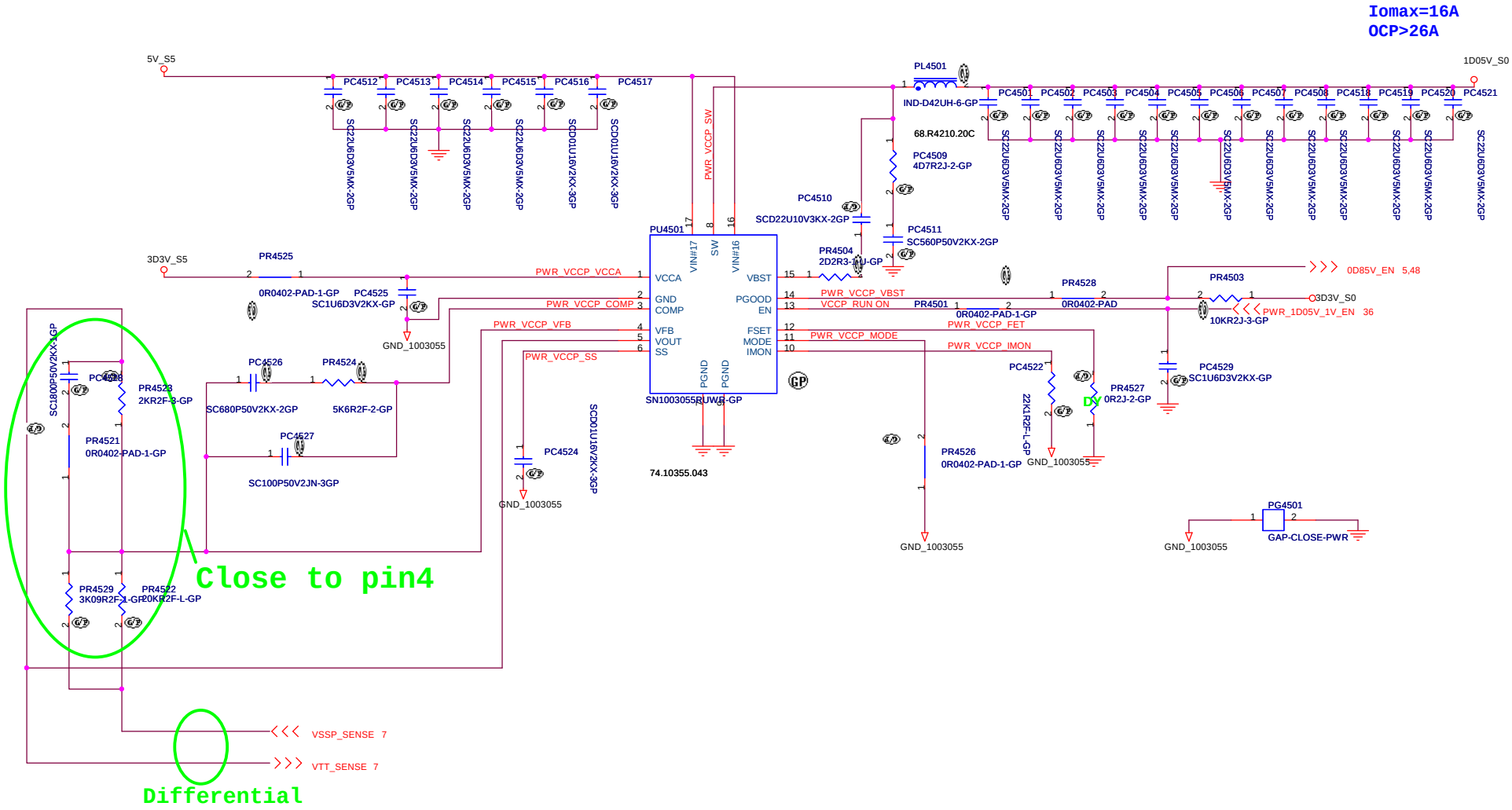
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1323_CPUCORE(3/3)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 44 of 103



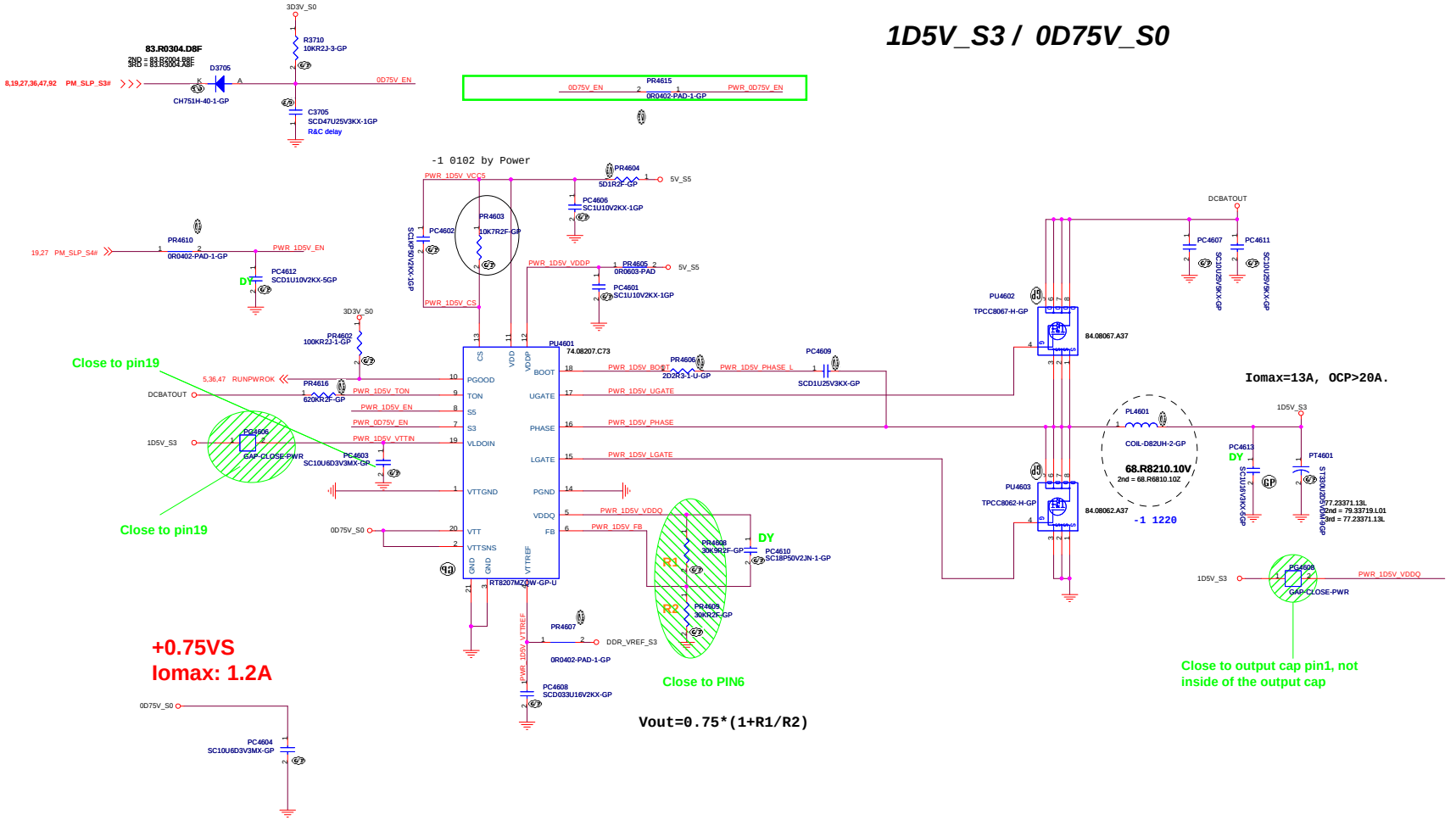
<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SN1003055RUWR		
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 45 of 103	

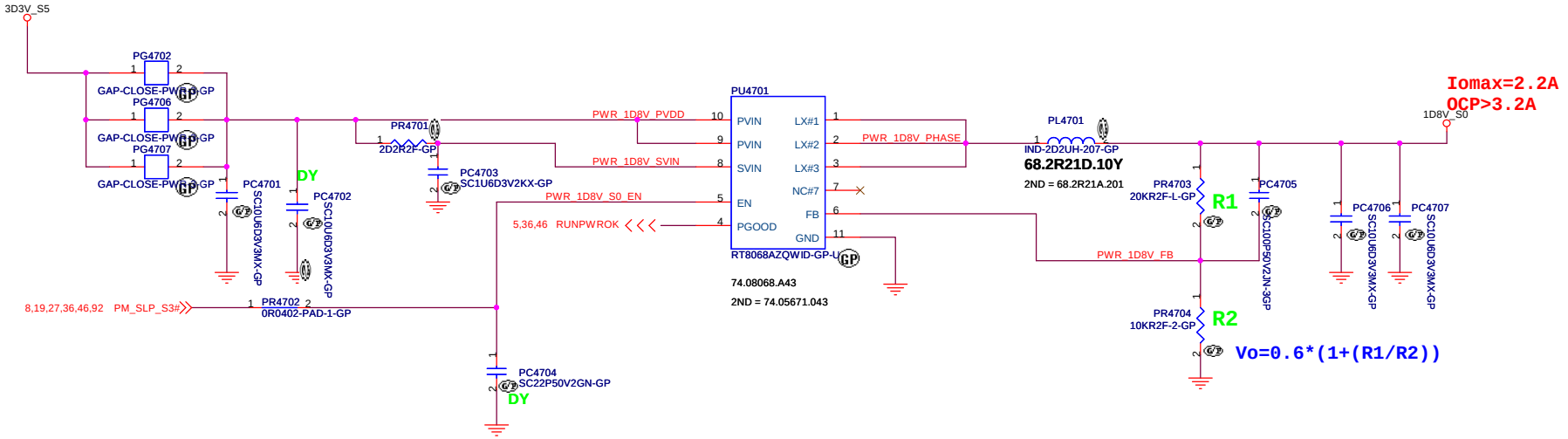
SSID = PWR.Plane.Regulator_1p5v0p75v

⑤

1D5V_S3 / 0D75V_S0



RT8068A for 1D8V_S0



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT8068A_1D8V***	
Size: A3	Document Number: **Colossus**	Rev: 1
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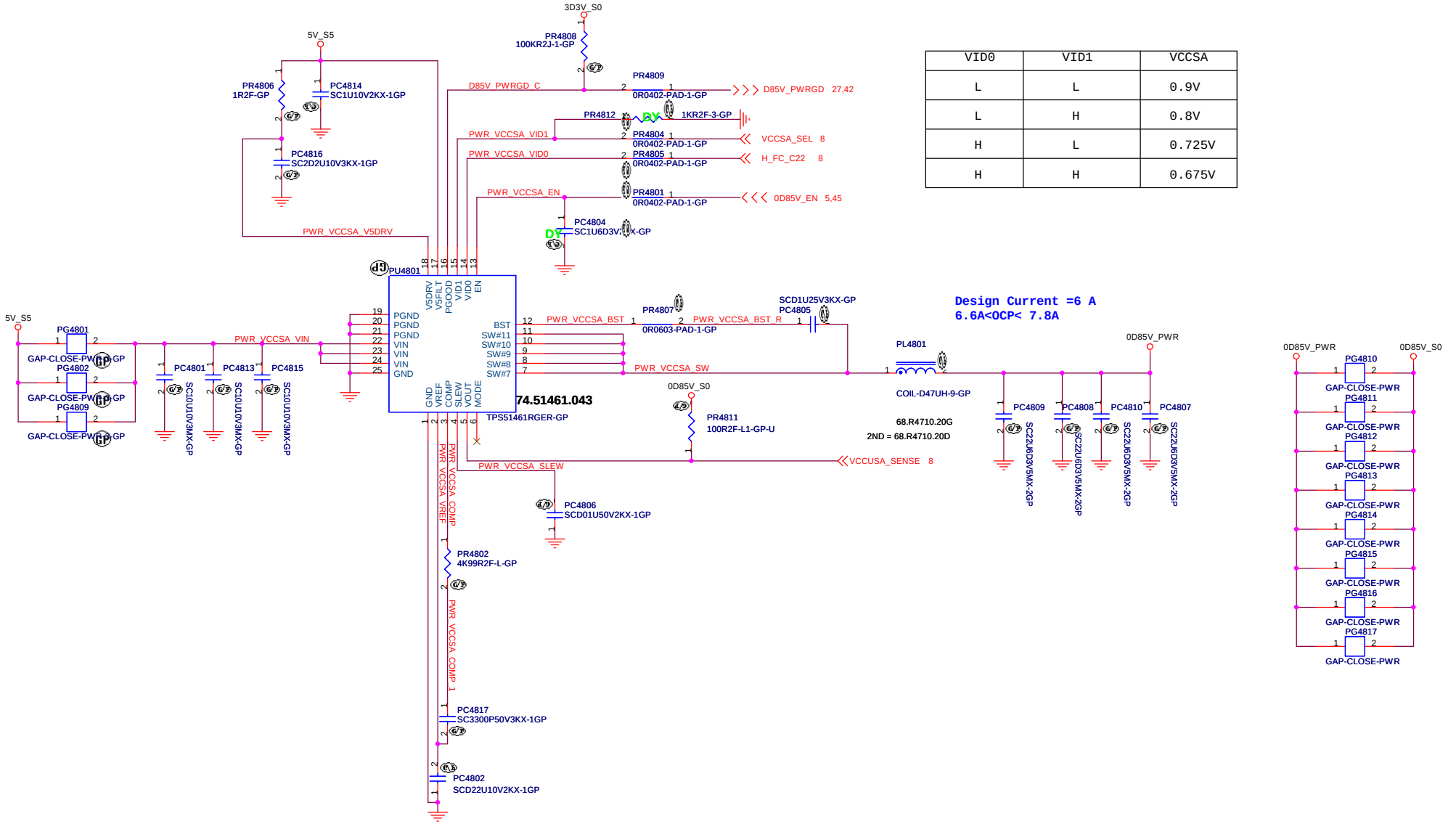
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

Design Current =6 A
6.6A<OCP< 7.8A

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **TPS51461 VCCSA**

Size	Document Number	Rev
A3	Colossus	1

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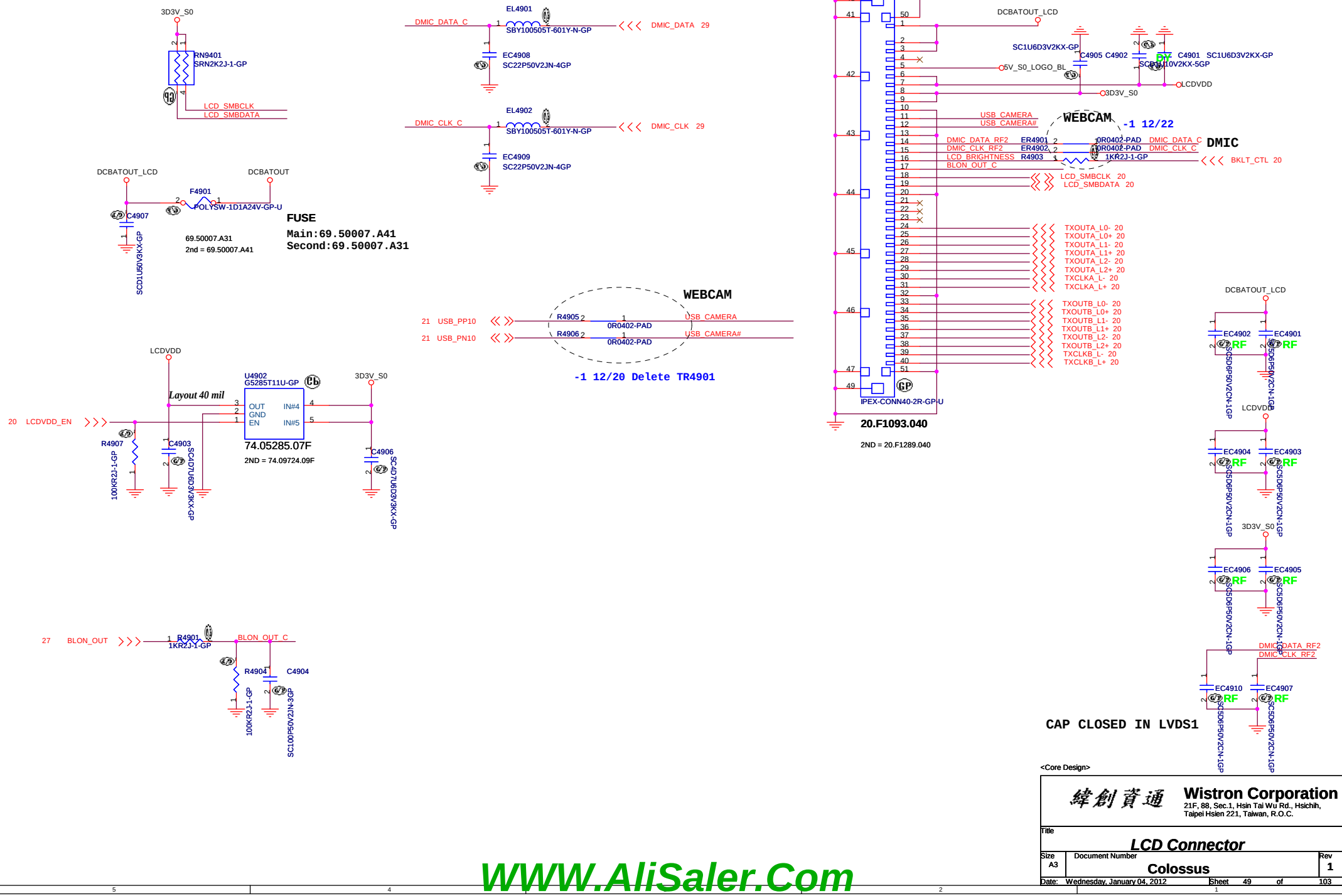
LVDS CONNECTOR
AUO B156HB01 V0

D_MIC by EMI

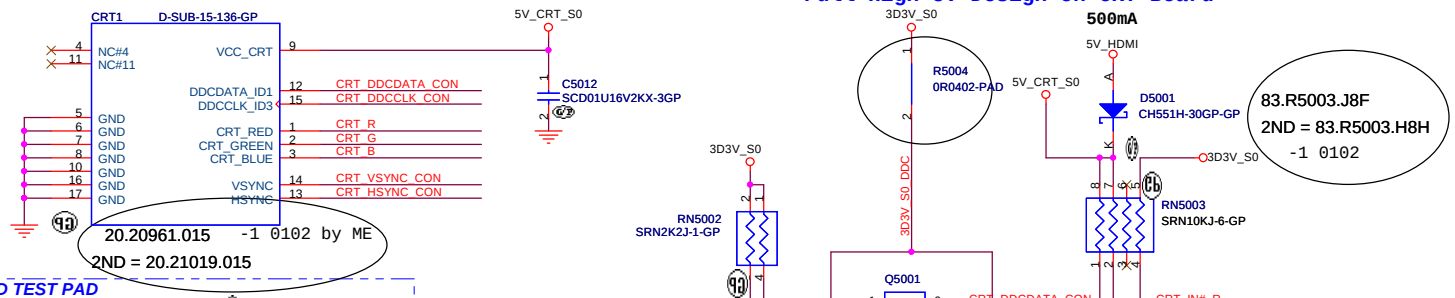
LVDS Impedance:90 ohm

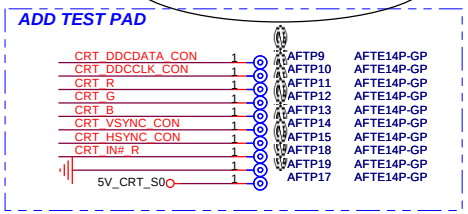


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**LCD Connector**
Size: A3	Document Number: Colossus
Rev: 1	
Date: Wednesday, January 04, 2012	Sheet 49 of 103

CRT Connector

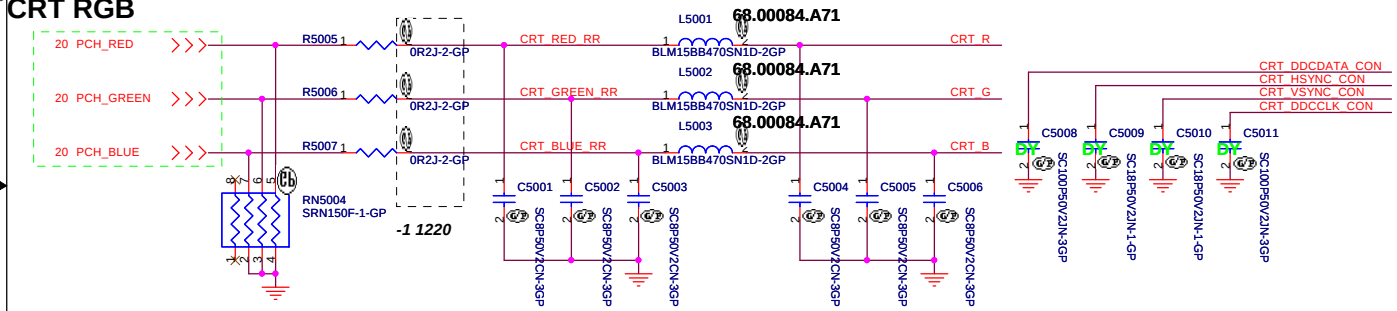


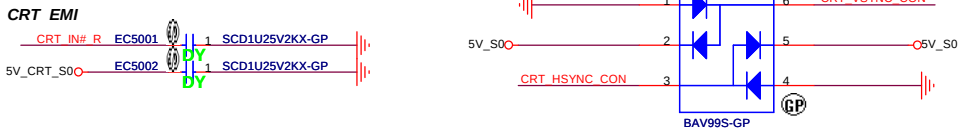


CRT DDCDATA & DDCCLK level shift

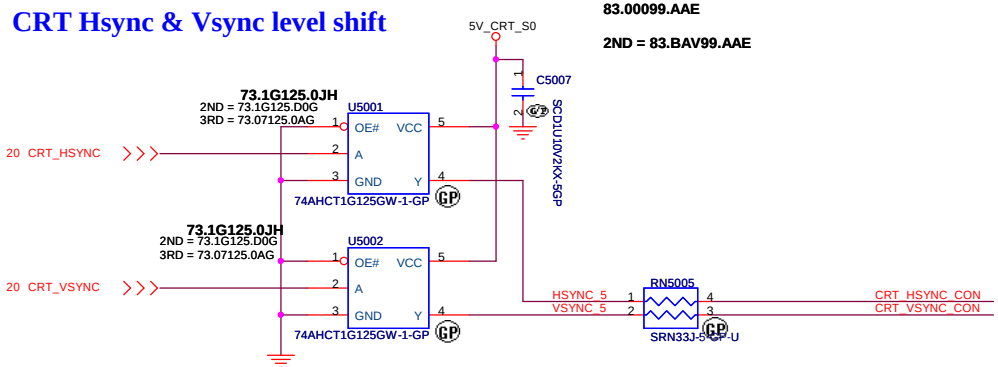
Pull High 5V Design on CRT Board

CRT RGB





CRT Hsync & Vsync level shift



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CRT_CONN		
Size: A3	Document Number: Colossus	Rev: 1
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HDMI Level Shifter & CONNECTOR

HDMI_CLK_R_C → TR5101 FILTER-4P-49-GP → HDMI_CLK_R_C_CON
HDMI_CLK_R_C# → TR5101 FILTER-4P-49-GP → HDMI_CLK_R_C#_CON
69.10118.111

HDMI_DATA1_R_C → TR5103 FILTER-4P-49-GP → HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C# → TR5103 FILTER-4P-49-GP → HDMI_DATA1_R_C#_CON
69.10118.111

HDMI_DATA0_R_C → TR5102 FILTER-4P-49-GP → HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C# → TR5102 FILTER-4P-49-GP → HDMI_DATA0_R_C#_CON
69.10118.111

HDMI_DATA2_R_C → TR5104 FILTER-4P-49-GP → HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C# → TR5104 FILTER-4P-49-GP → HDMI_DATA2_R_C#_CON
69.10118.111

Close to GPU

HDMI DISCRETE/ UMA Co-lay

20 HDMI_CLK_R# / 20 HDMI_CLK_R → C5103 / C5104 SCD1U10V2KX-5GP → HDMI_CLK_R_C# / HDMI_CLK_R_C
20 HDMI_DATA0_R# / 20 HDMI_DATA0_R → C5105 / C5106 SCD1U10V2KX-5GP → HDMI_DATA0_R_C# / HDMI_DATA0_R_C
20 HDMI_DATA1_R# / 20 HDMI_DATA1_R → C5110 / C5107 SCD1U10V2KX-5GP → HDMI_DATA1_R_C# / HDMI_DATA1_R_C
20 HDMI_DATA2_R# / 20 HDMI_DATA2_R → C5108 / C5109 SCD1U10V2KX-5GP → HDMI_DATA2_R_C# / HDMI_DATA2_R_C

66.05136.08L=>680ohm for UMA
66.47136.A8L=>470ohm for GPU

Close to HDMI Connector

RN5106 SRN470J-5-GP
RN5107 SRN470J-5-GP
HDMI_PLL_GND

HDMI CONN

HDMI1 SKT-HDMI21-4-GP
22.10296.711
2ND = 22.10296.751

HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI

5V_HDMI → F5101 FUSE-1D1A6V-4GP-U 69.50007.691 (2nd = 69.50007.771, 3RD = 69.50007.C21) → 5V_S0
C5102 SCD1U10V2KX-5GP
HPD_HDMI_CON

AFTP95 AFTE14P-GP
AFTP94 AFTE14P-GP
AFTP41 AFTE14P-GP
AFTP42 AFTE14P-GP
AFTP37 AFTE14P-GP
AFTP38 AFTE14P-GP
AFTP43 AFTE14P-GP
AFTP44 AFTE14P-GP
AFTP72 AFTE14P-GP
AFTP81 AFTE14P-GP
AFTP80 AFTE14P-GP
AFTP93 AFTE14P-GP
AFTP130 AFTE14P-GP

3D3V_S0 → R5111 150KR2J-L1-GP → HDMI_HPD_B → Q5102 PMBS3904-1-GP
R5110 200KR2J-L1-GP DY
84.03904.L06 (2nd = 84.03904.P11)
HDMI_HPD_E → R5128 0R0402-PAD → HDMI_PCH_DET 20
R5112 20KR2F-L-GP

5V_S0 → D5102 BAW56-5-GP 83.00056.Q11 (2nd = 83.00056.G11, 3RD = 83.00056.K11)
DDC_CLK_PH1
DDC_DATA_PH1
RN5101 SRN2K2J-1-GP

3D3V_S0 → Q5104 ME2N7002DKW-G-GP 84.2N702.F3F (2ND = 84.2N702.E3F)
DDC_CLK_Q
DDC_DATA_Q
DDC_CLK_HDMI
DDC_DATA_HDMI
RN5117 SRN0J-6-GP
20 PCH_HDMI_CLK / 20 PCH_HDMI_DATA

3D3V_S0 → Q5106 2N7002K-2-GP
84.2N702.J31 (2ND = 84.2N702.W31)
HDMI_PLL_GND

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: HDMI Level Shifter/Conn
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 51 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display Port

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 52 of 103

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 53 of 103

(Blanking)

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 54 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

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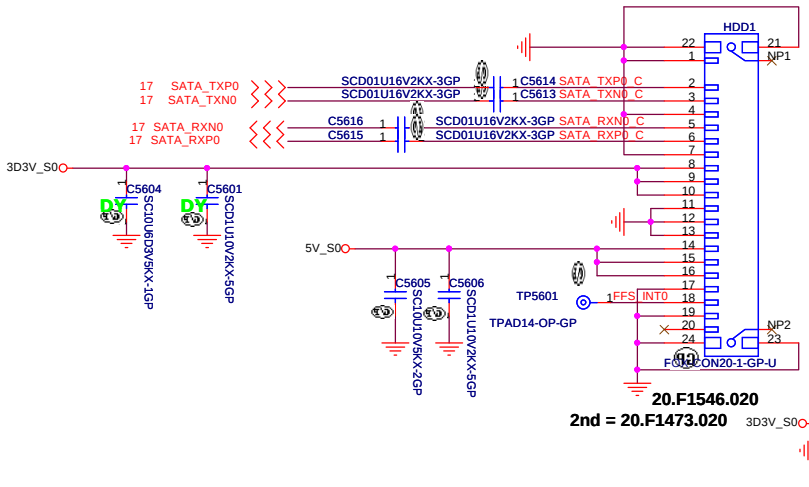
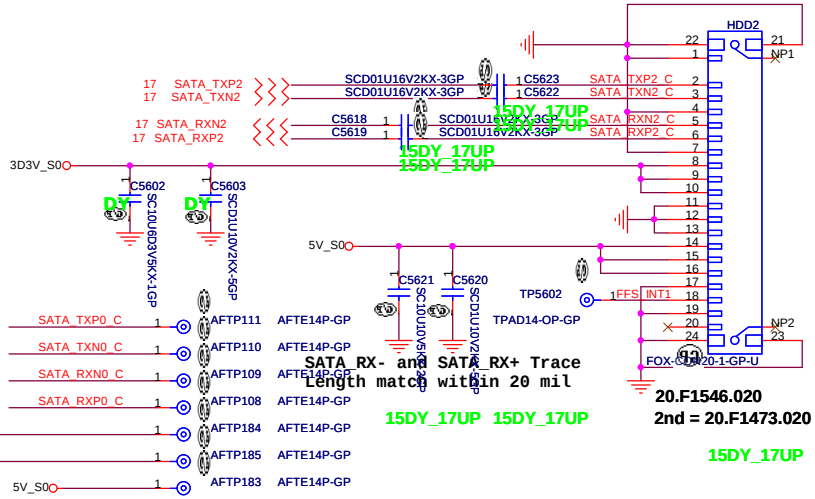
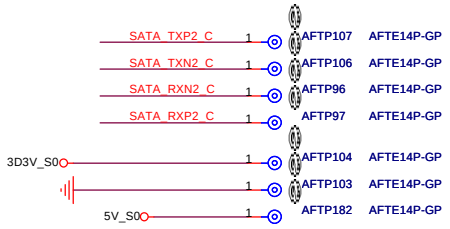
SATA HDD1 Connector

CHECK HDD conn model pin define_ME wire

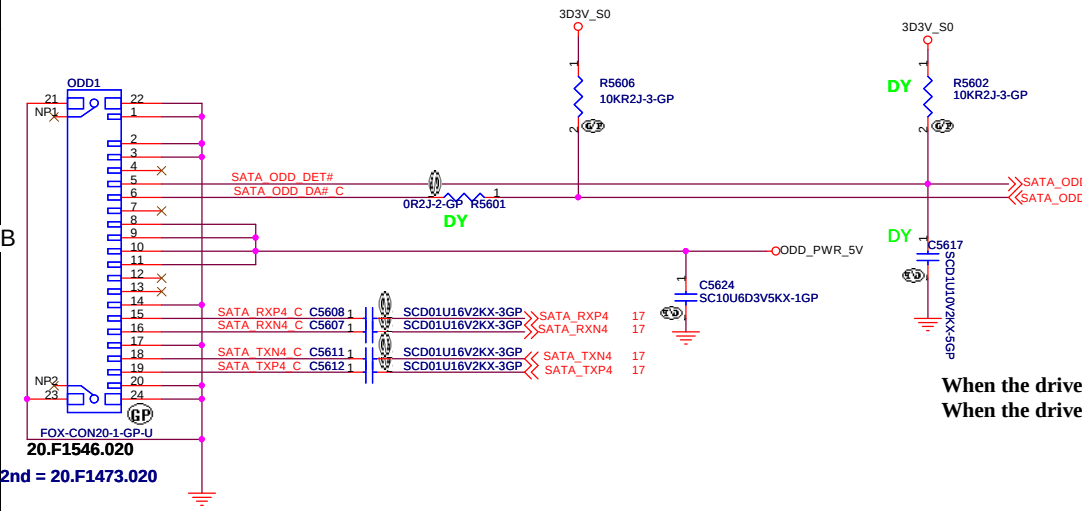


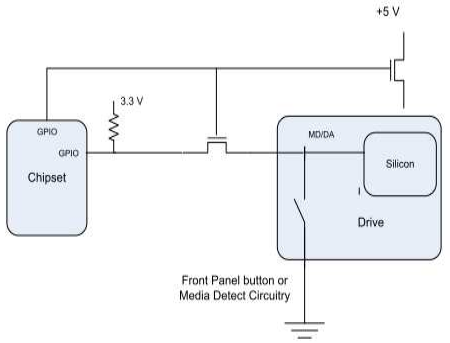
SATA HDD2 Connector





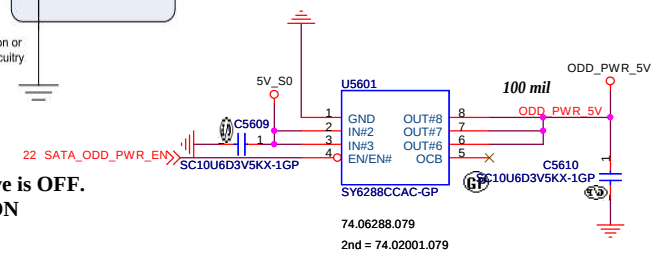
ODD Connector



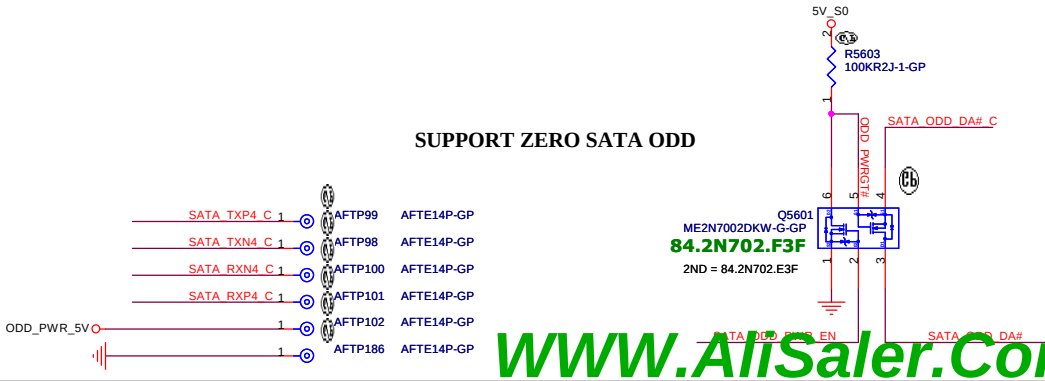


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SATA Zero Power ODD



SUPPORT ZERO SATA ODD



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 56 of 103

(Blanking)

<Core Design>

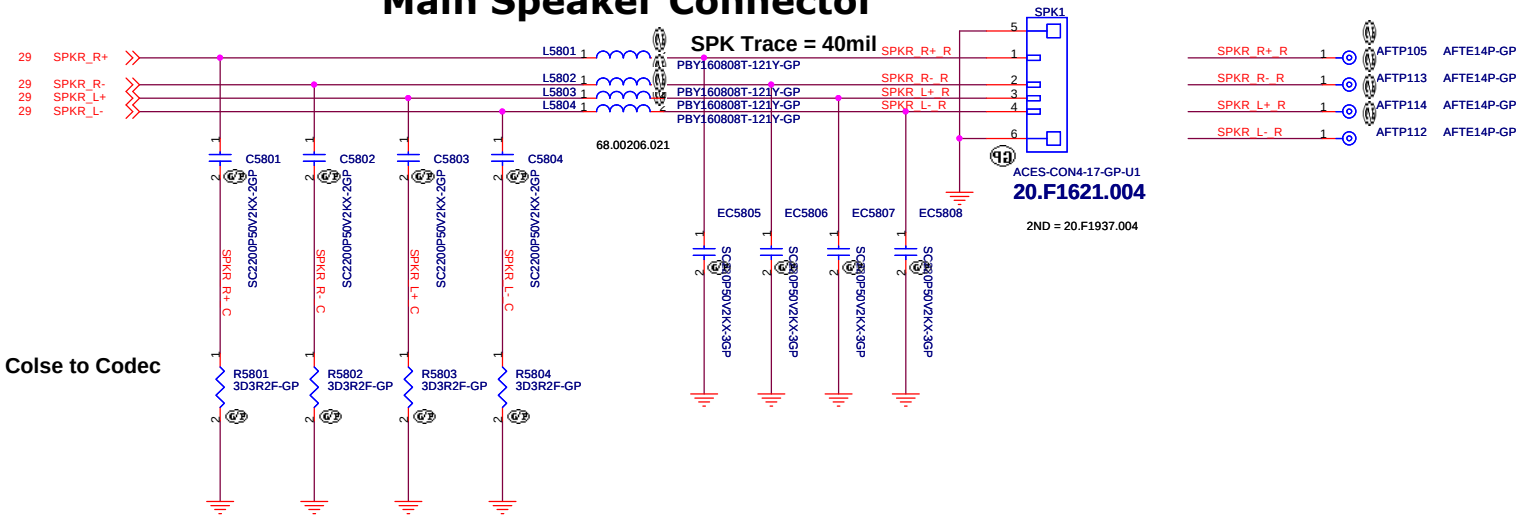
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 57 of 103

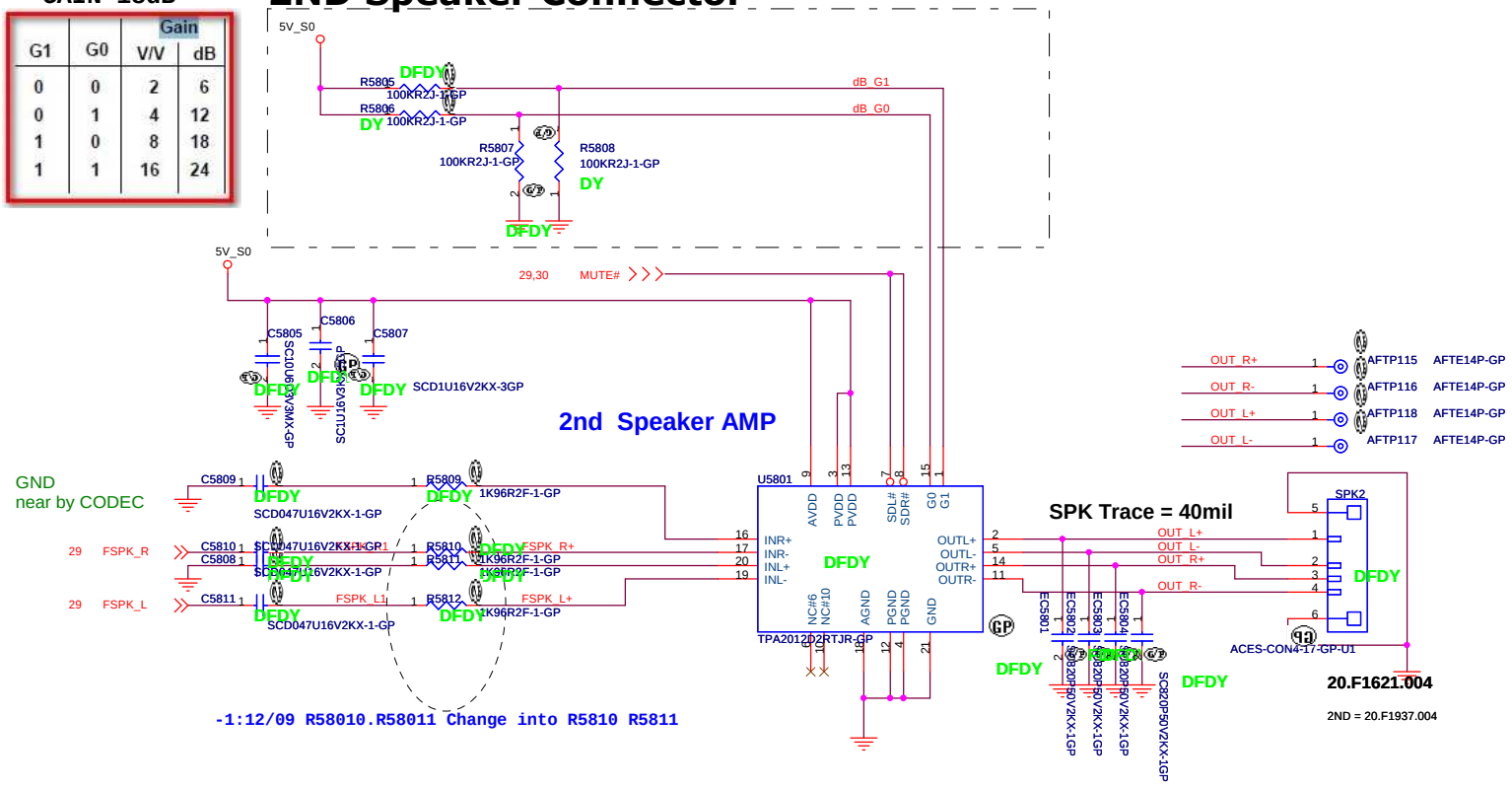
Main Speaker Connector



2ND Speaker Connector

GAIN 18dB

G1	G0	Gain V/V	Gain dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24



-1:12/09 R58010.R58011 Change into R5810 R5811

<Core Design>

緯創資通 **Wistron Corporation**
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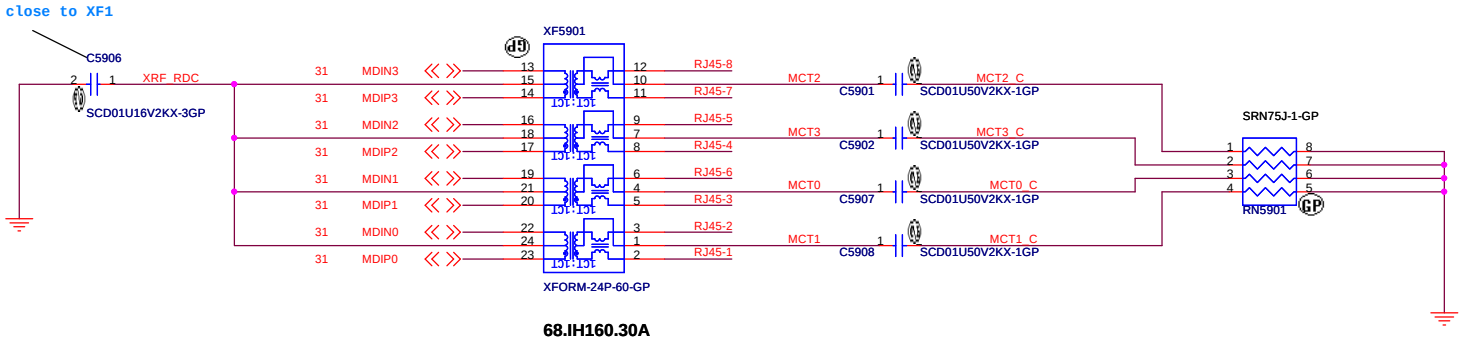
Title: **SPEAKER CONN**

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 58 of 103

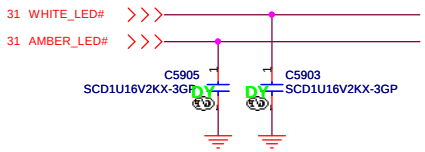
White LED for connectivity and Amber LED for activity located on RJ-45 connector

close to XF1

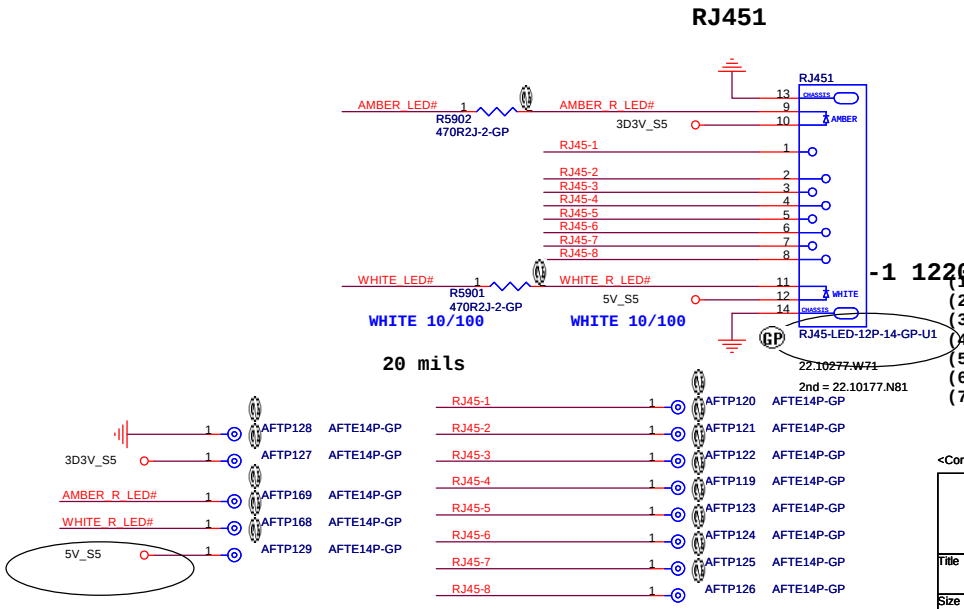


68.IH160.30A

2ND = 68.89246.301



AMBER = LAN ACK



-1 1220

(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

<Core Design>

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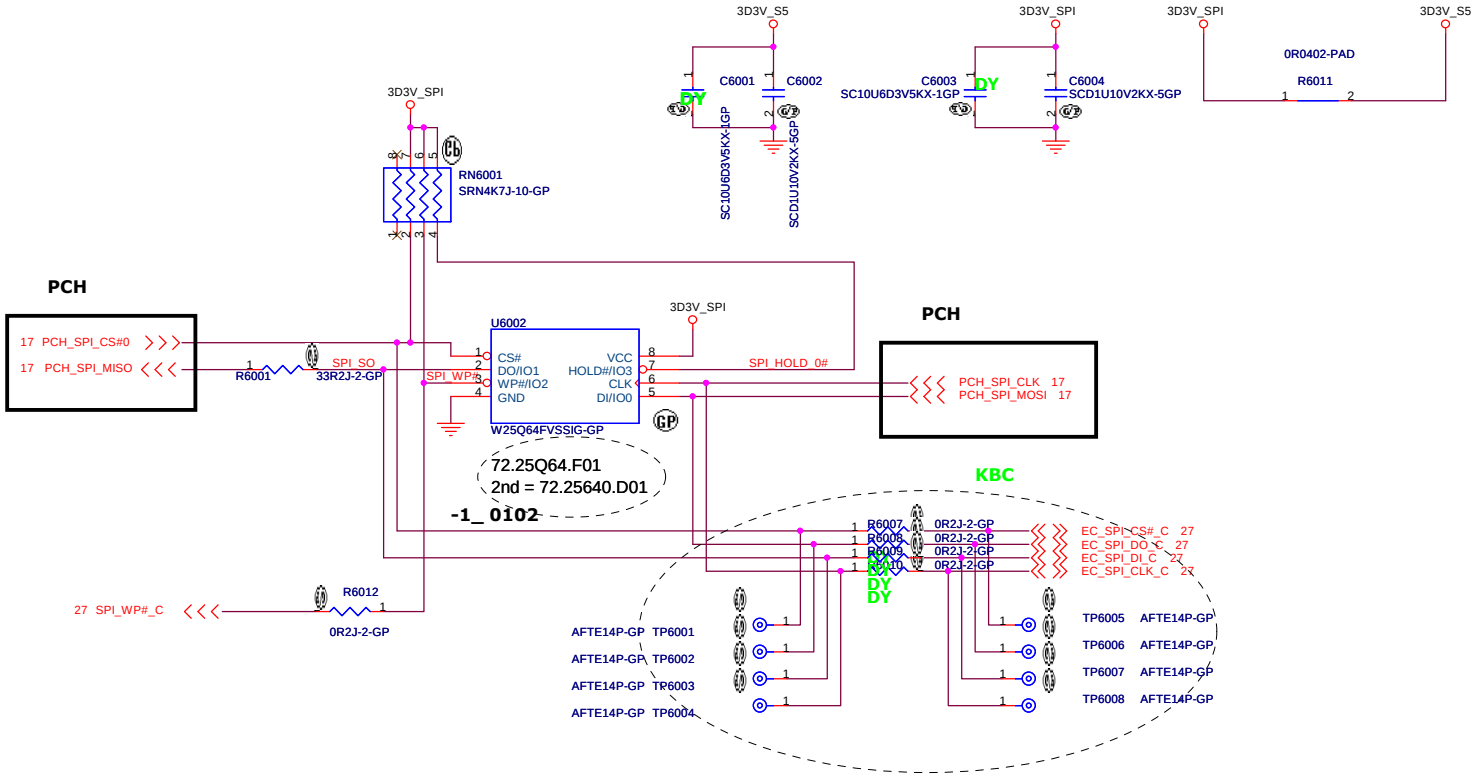
Title: RJ45+Transformer

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 59 of 103

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH & KBC



Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

-1 1223 Reversed TP6001~TP6008 / R6007~R6010 is DY
1, 測試點請使用14mil, 測試之間距離75mil以上。
2，測試點必須在Top層.

<Core Design>

緯創資通 Wistron Corporation
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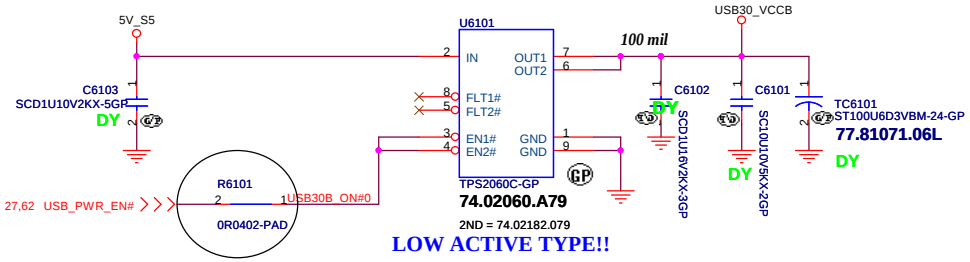
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash		
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 60 of 103	

RESERVED USB 2.0/3.0 BD

SSID = USB

Power switcher Low active

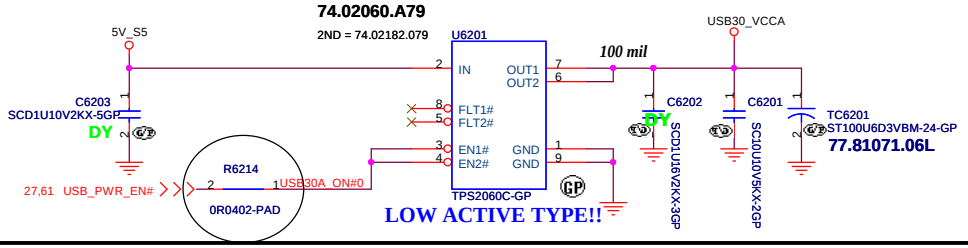


LOW ACTIVE TYPE!!

<Core Design>

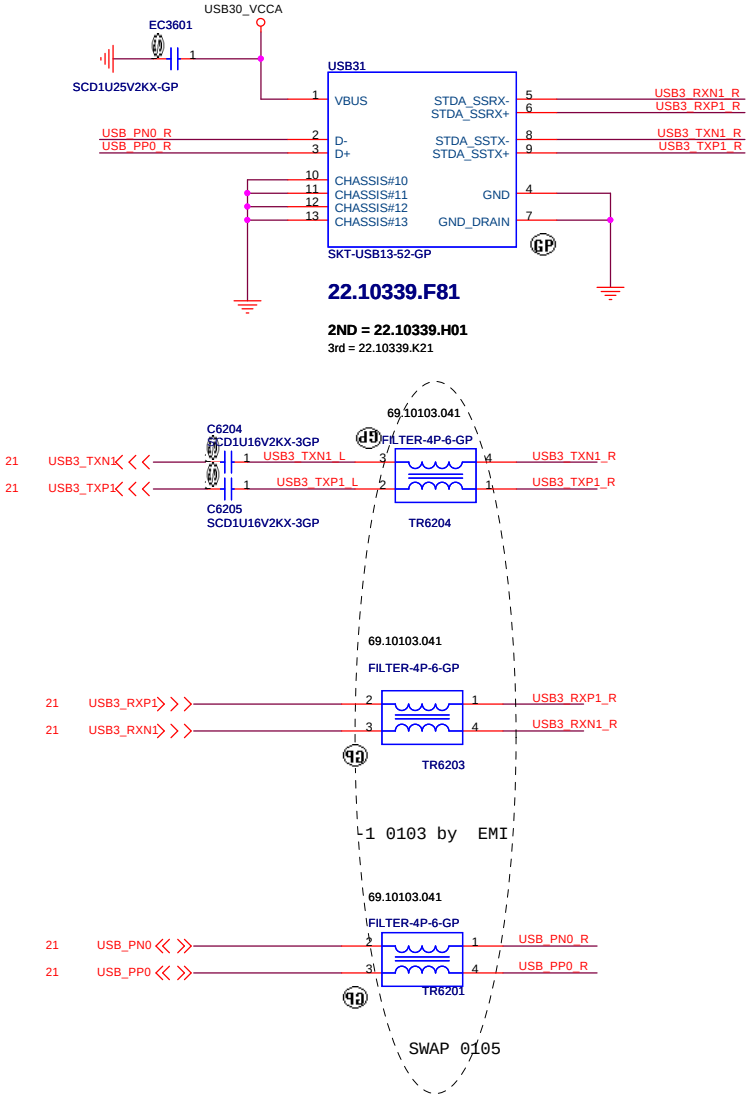
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: *USB Power SW_USB IO*	
Size: A3	Document Number: Colossus — Rev: 1
Date: Wednesday, January 04, 2012	Sheet 61 of 103

Power switcher Low active

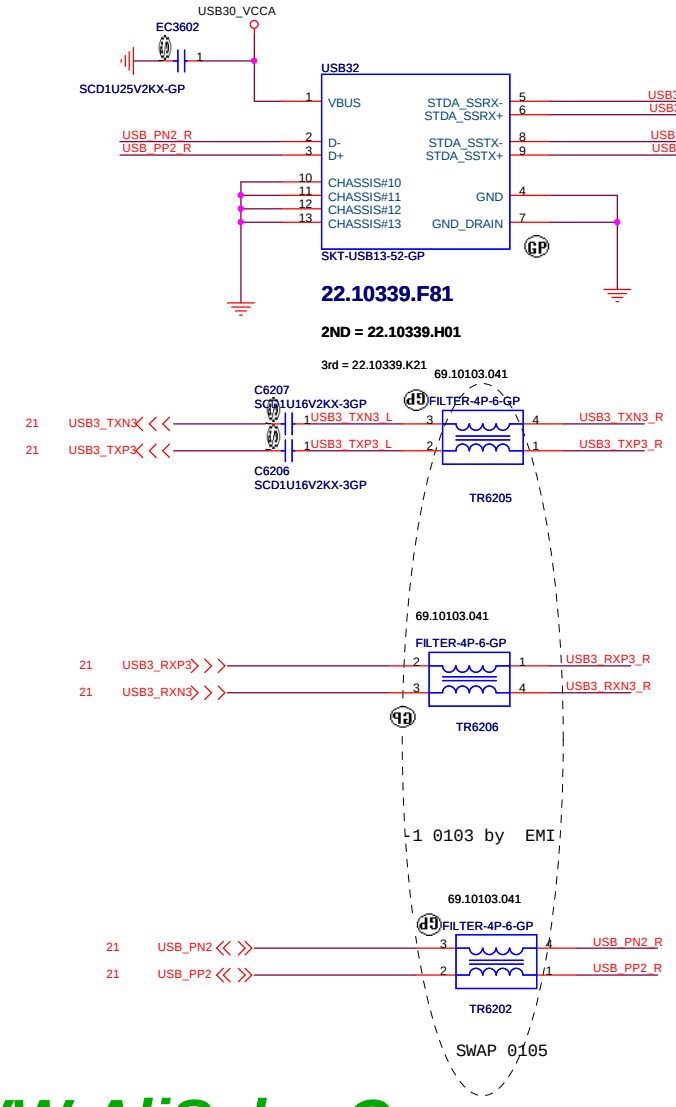


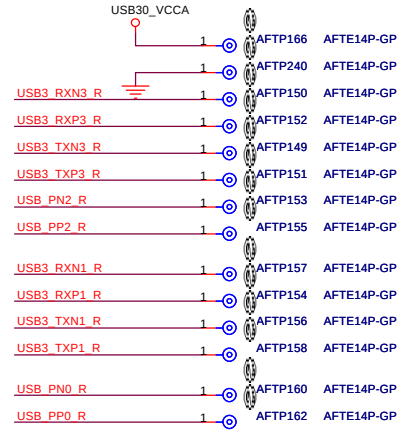
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB3_1

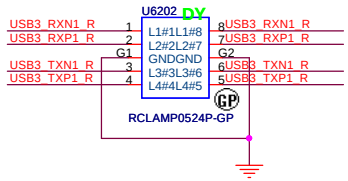


USB3_2

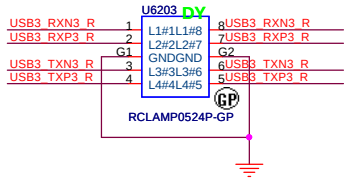




Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



<Core Design>

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Title: **USB3.0**

Size	Document Number	Rev
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<Variant Name>

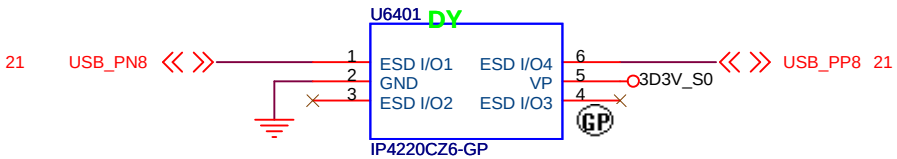
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

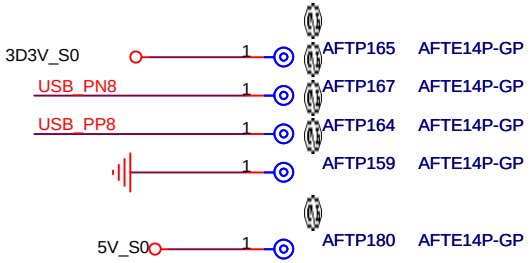
Title: *Resered(Bluetooth)*

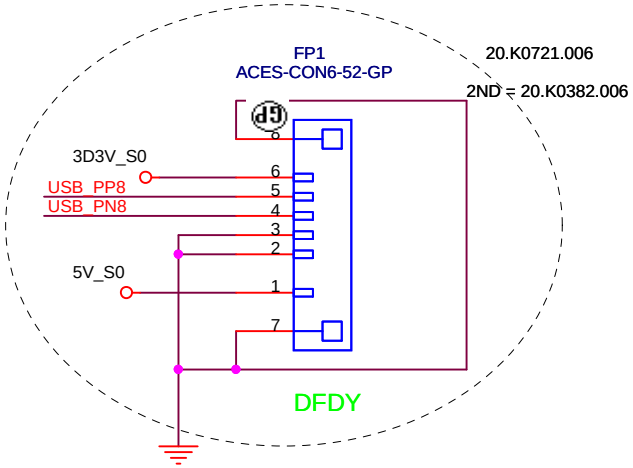
Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 63 of 103

Finger Printer







-1 12/23 FP1 change source

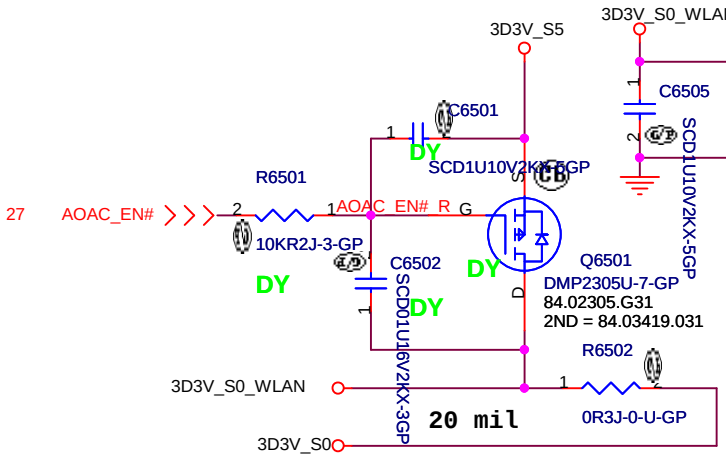
<Core Design>

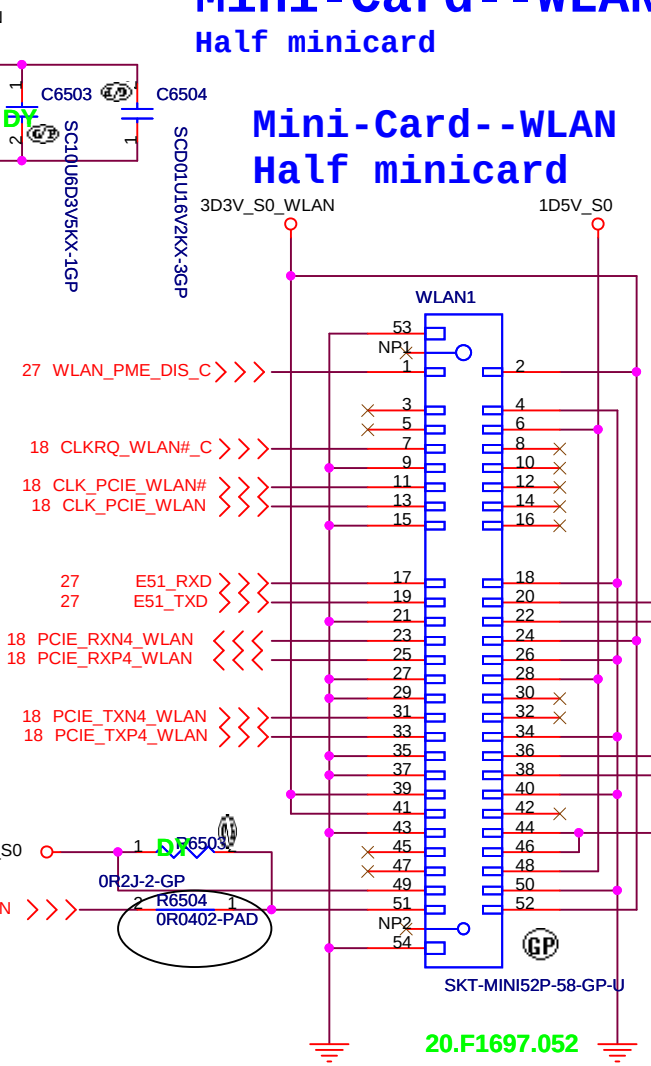
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Finger Print Conn*		
Size: A4	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 64 of 103	

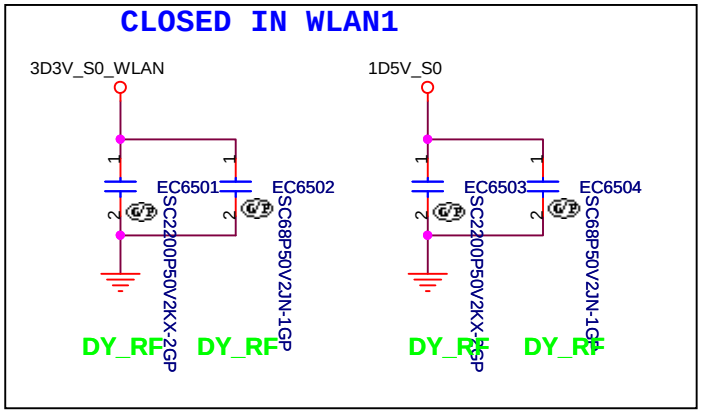
SSID = Wireless

Mini-Card--WLAN

Half minicard







51	BT_ DISABLE_L (low active to disable Bluetooth)

Pin	Active	Function
5	High(3V)	GPIO/BT_WAKE
20	High(3V)	WIFI_Enable
47	Reserved	BT_PRISEL(coexistence)
51	Reserved	BTCX_STAT(coexistence)

1-1 1226 del TR6501

<Core Design>

677869-FM8

1st	677869-FM8
2nd	677869-AM8
3rd	677869-BM8
4th	677869-LM8

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN+Bluetooth)/CONN***

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 65 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 66 of 103

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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: Colossus | Rev: 1

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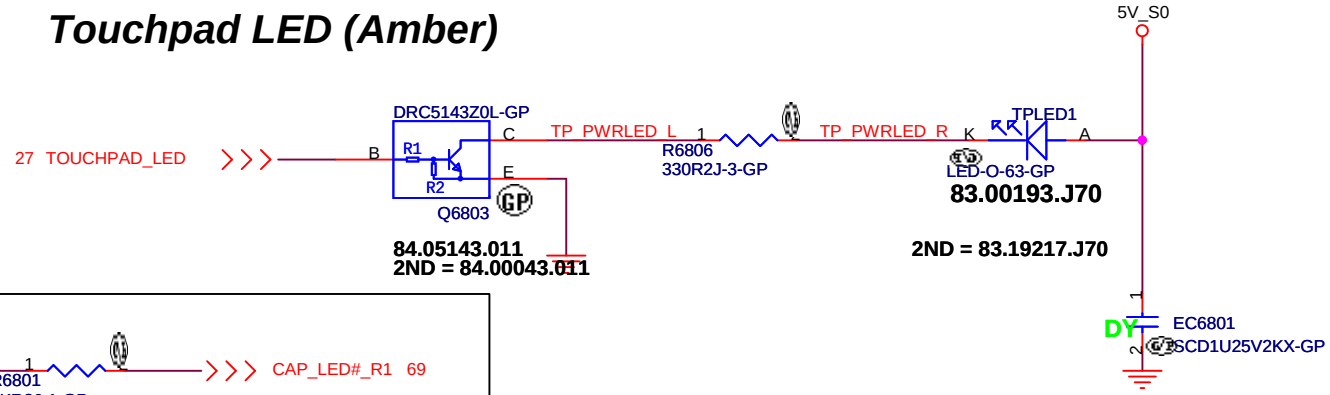
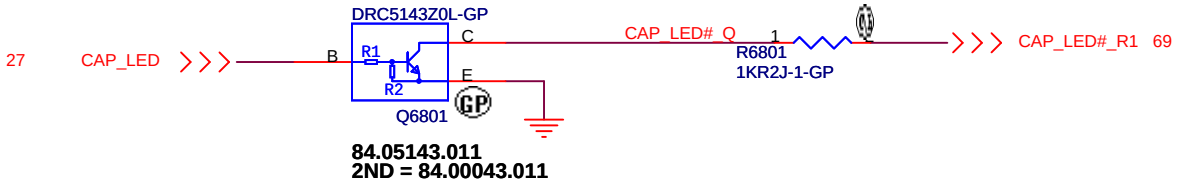
SSID = User.Interface

On Keyboard LEDs

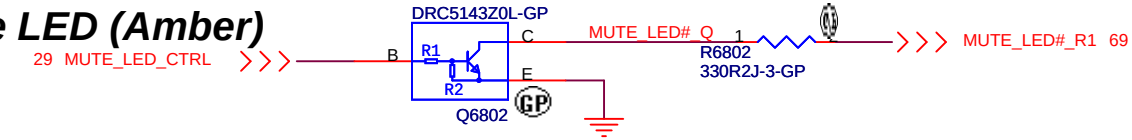
Touchpad LED (Amber)



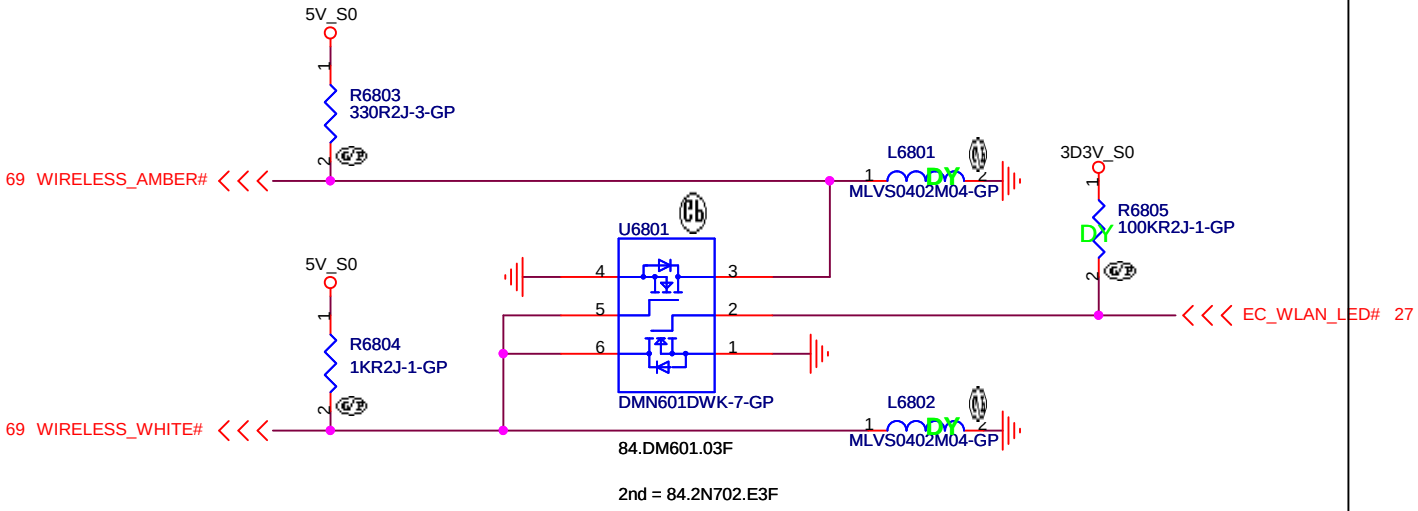
Cap locks LED (White)



Mute LED (Amber)



Wireless LED (White-On, Amber-Off)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	LED Bard/Power Button	
Size A4	Document Number: Colossus	Rev 1
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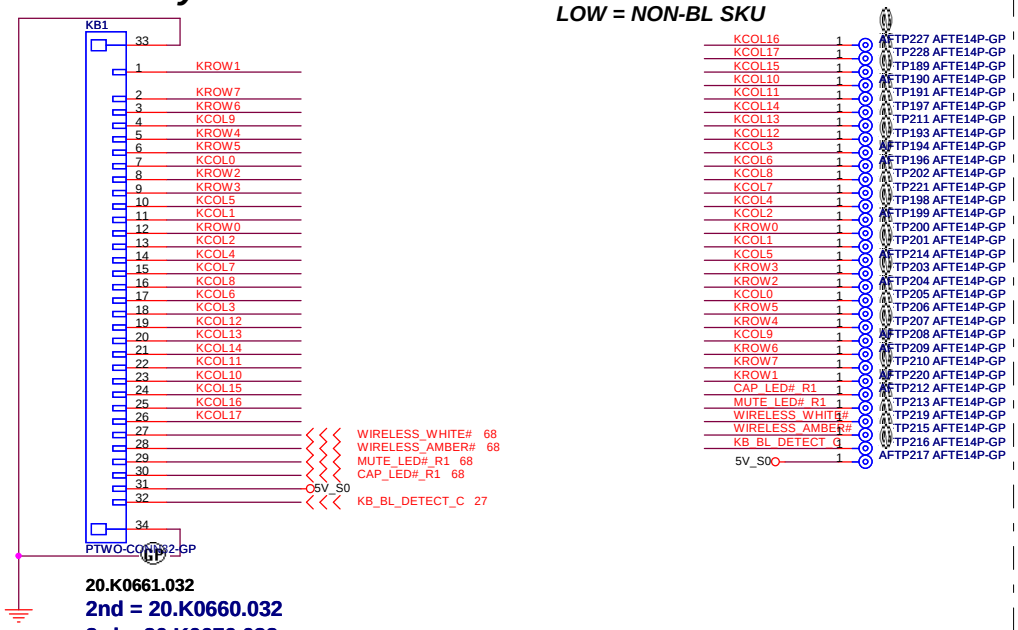
SSID = KBC

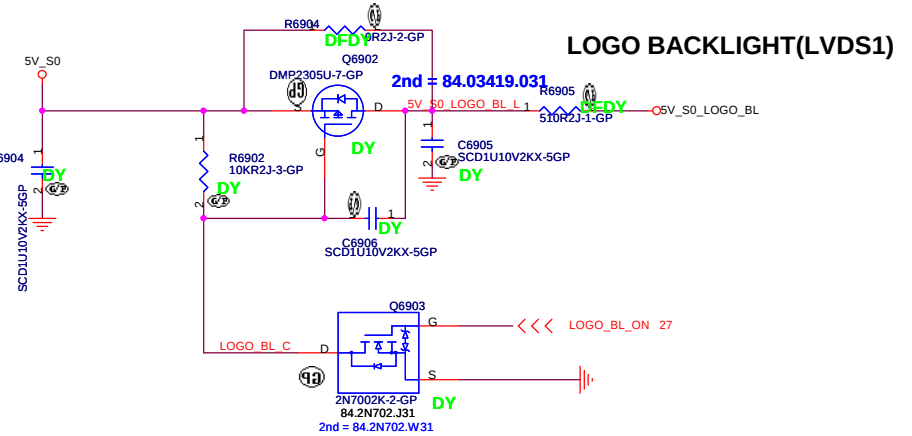
Internal KeyBoard Connector

KB_BL_DETECT
HIGH = BL SKU
LOW = NON-BL SKU

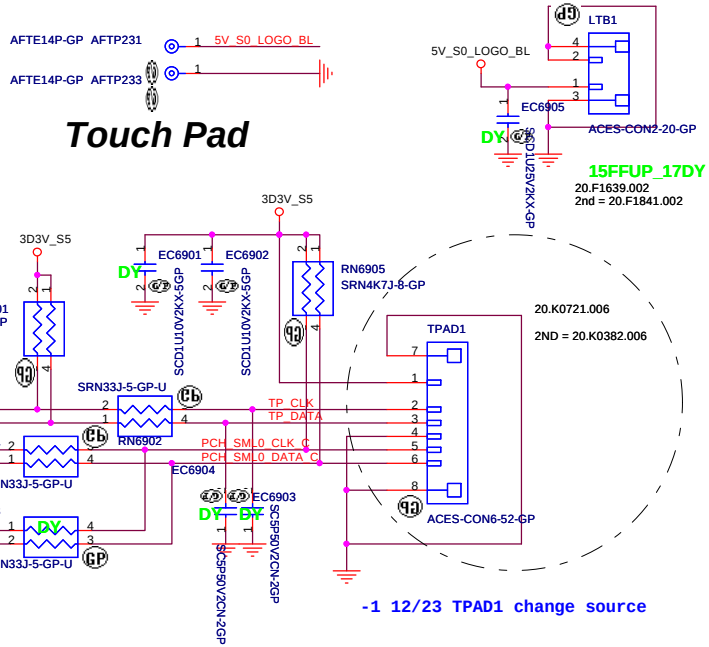


20.K0661.032
2nd = 20.K0660.032
3rd = 20.K0676.032

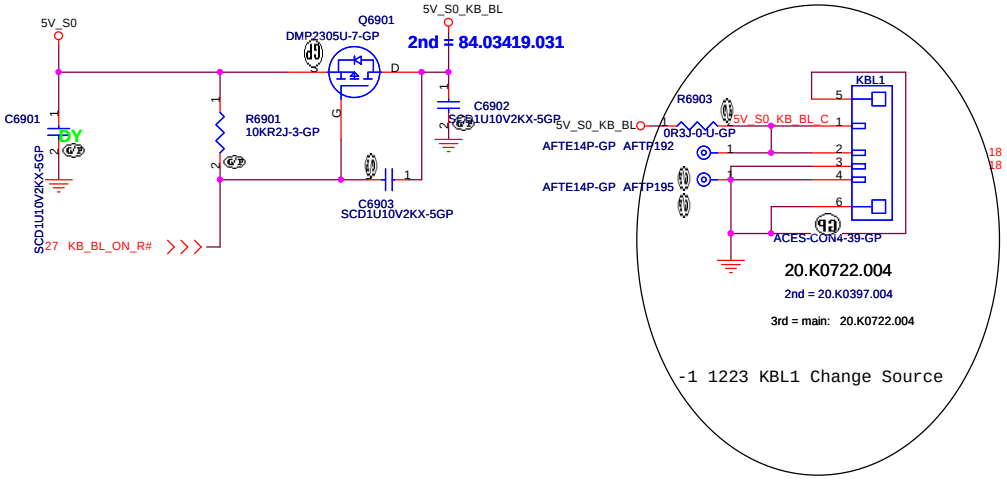
A Cover Logo Backlight

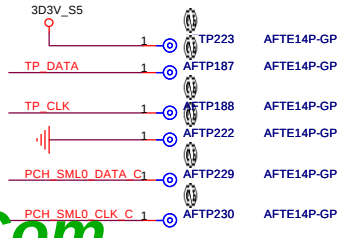


Touch Pad



Internal KeyBoard Backlight Connector





<Core Design>

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Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	Colossus	1

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(Hall sensor at Power BD)

<Core Design>

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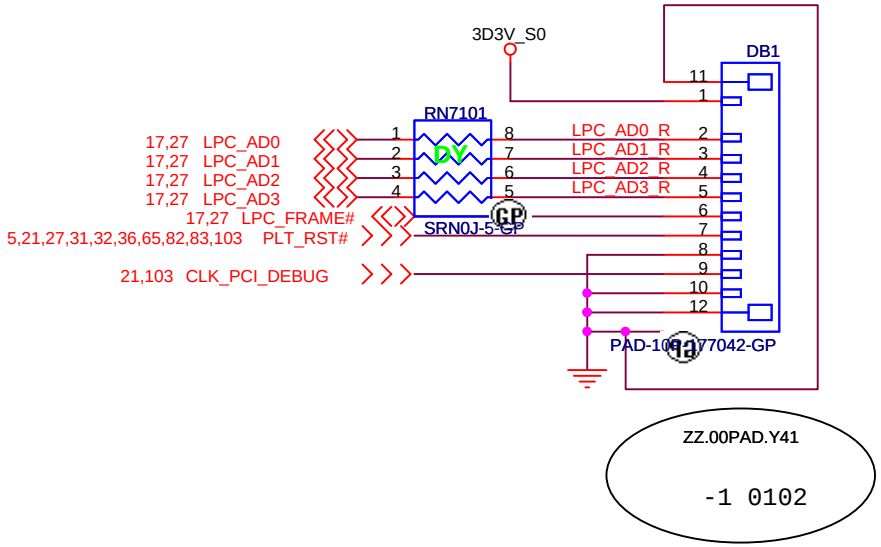
Title: Hall Sensor

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 70 of 103

DEBUG BD for Factory Test



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Dubug connector*		
Size: A4	Document Number: Colossus	Rev: 1
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
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<Core Design>

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Title: *Reserved*

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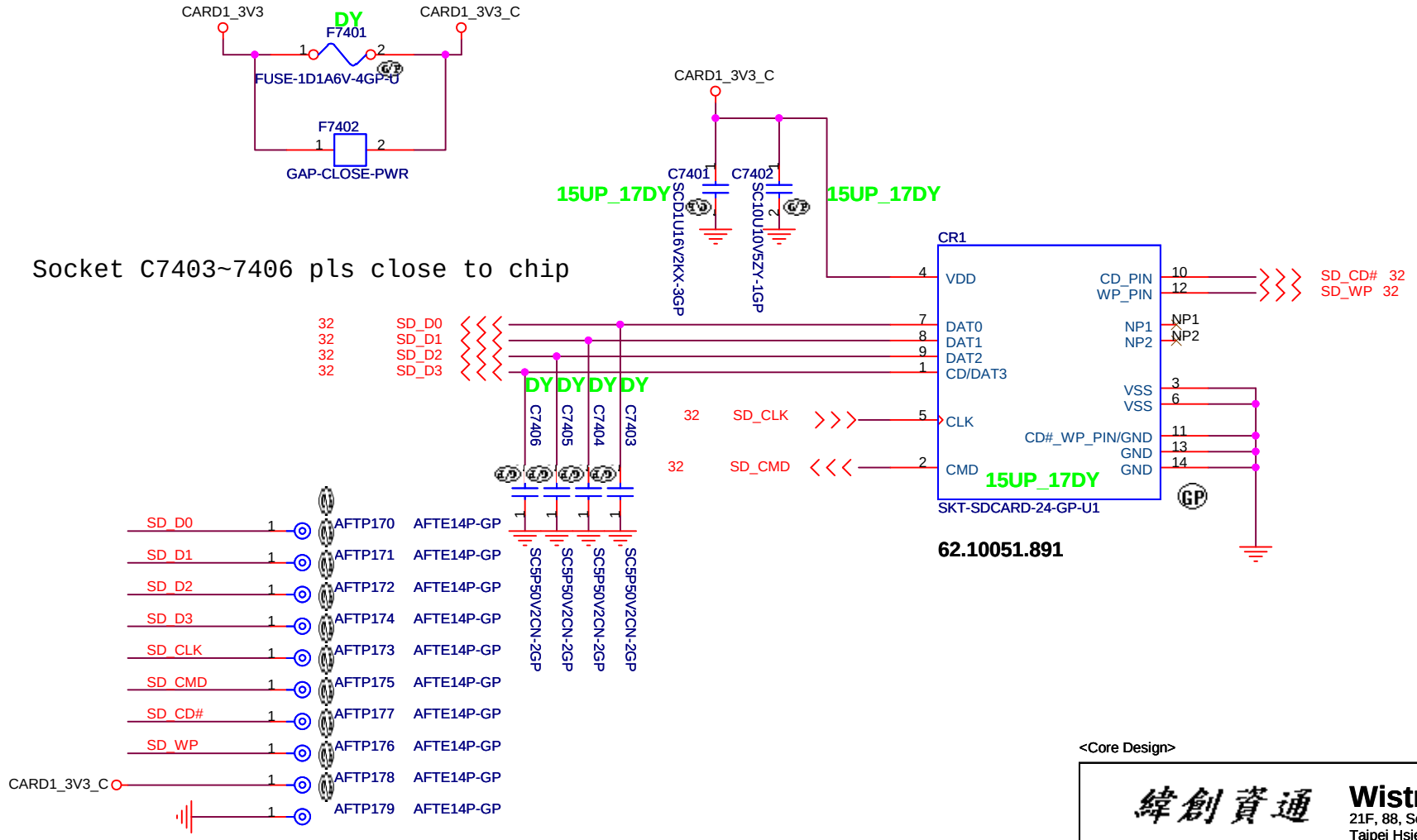
2 IN1 CARD-READER (SD/MMC)



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	Colossus	1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Express Card*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 75 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 76 of 103	

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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM

Size	Document Number	Rev
A3	Colossus	1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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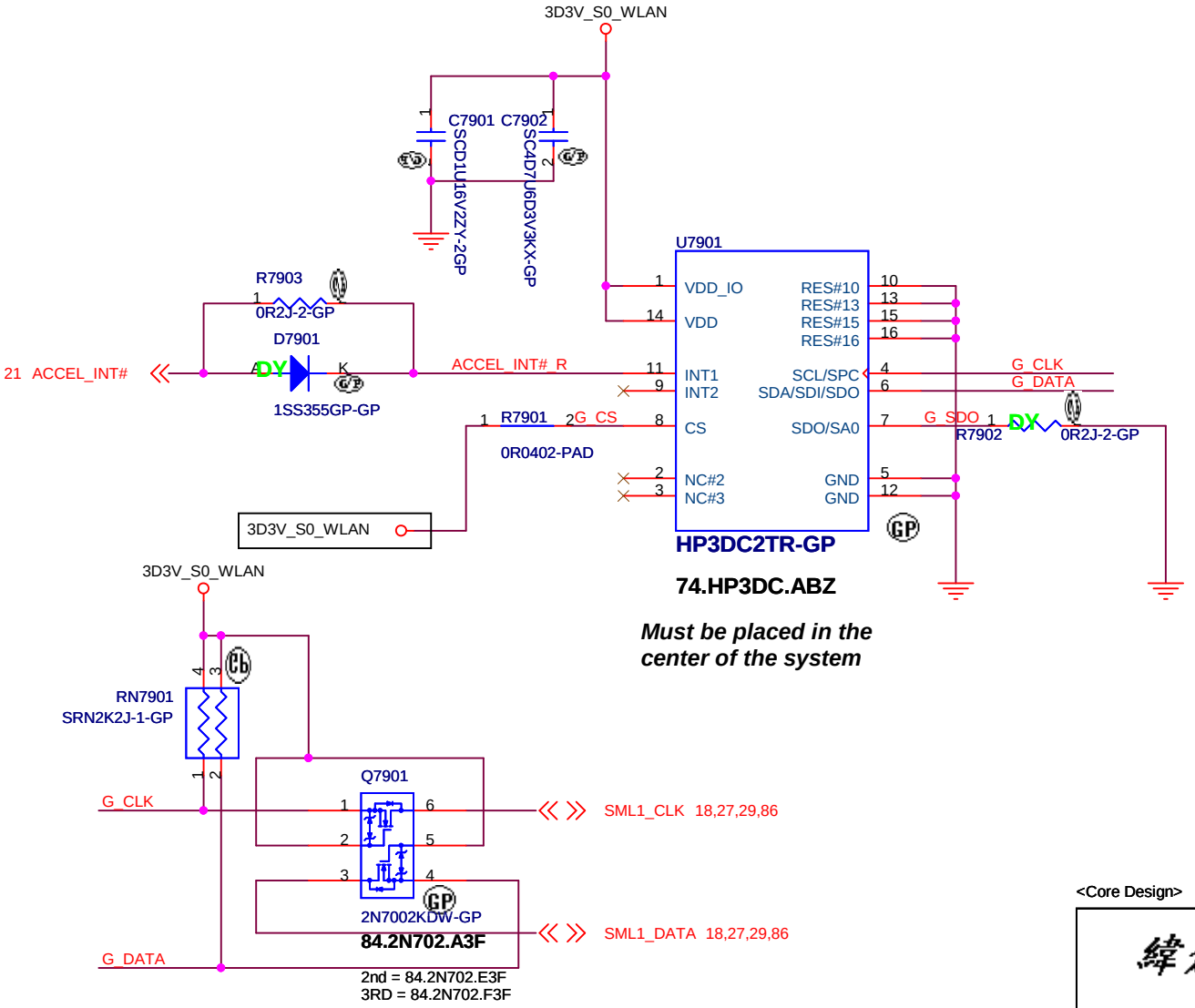
ACCELEROMETER



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ACCELEROMETER		
Size: A4	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 79 of 103	

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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

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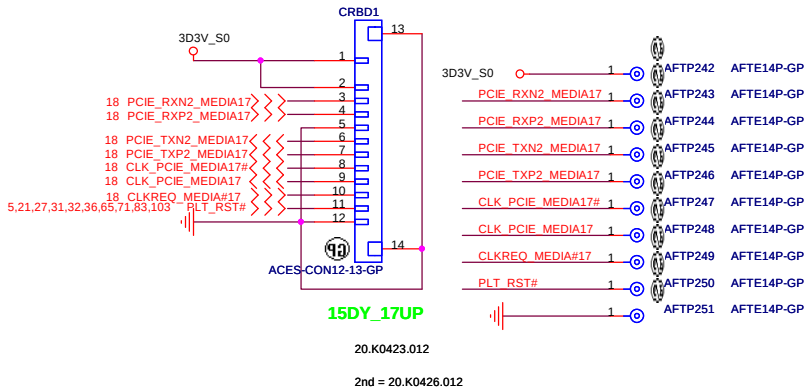
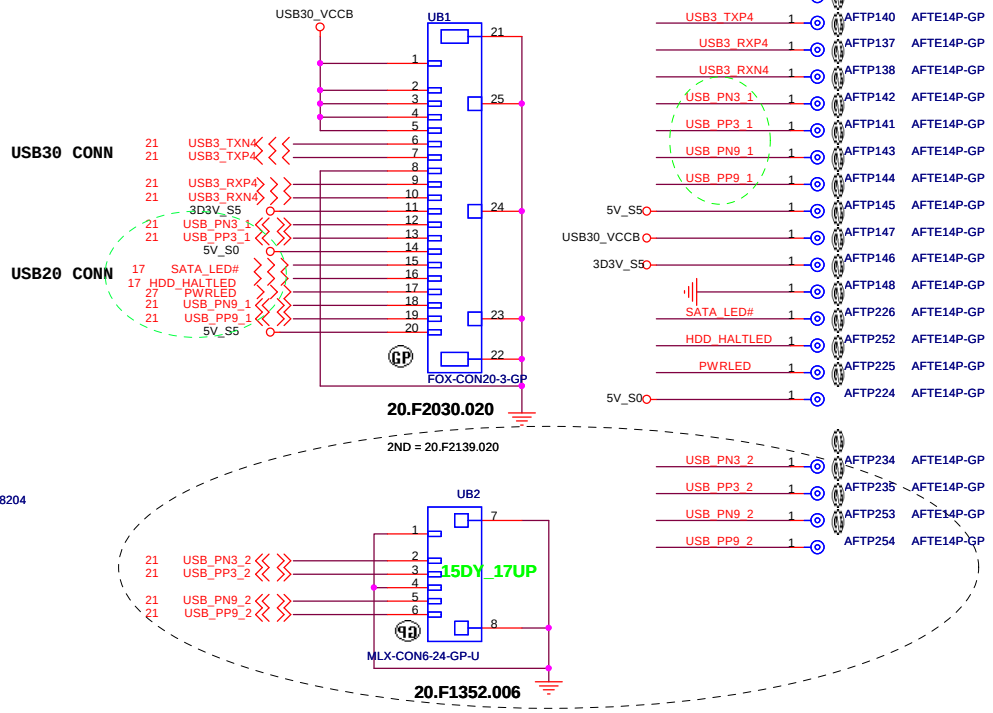
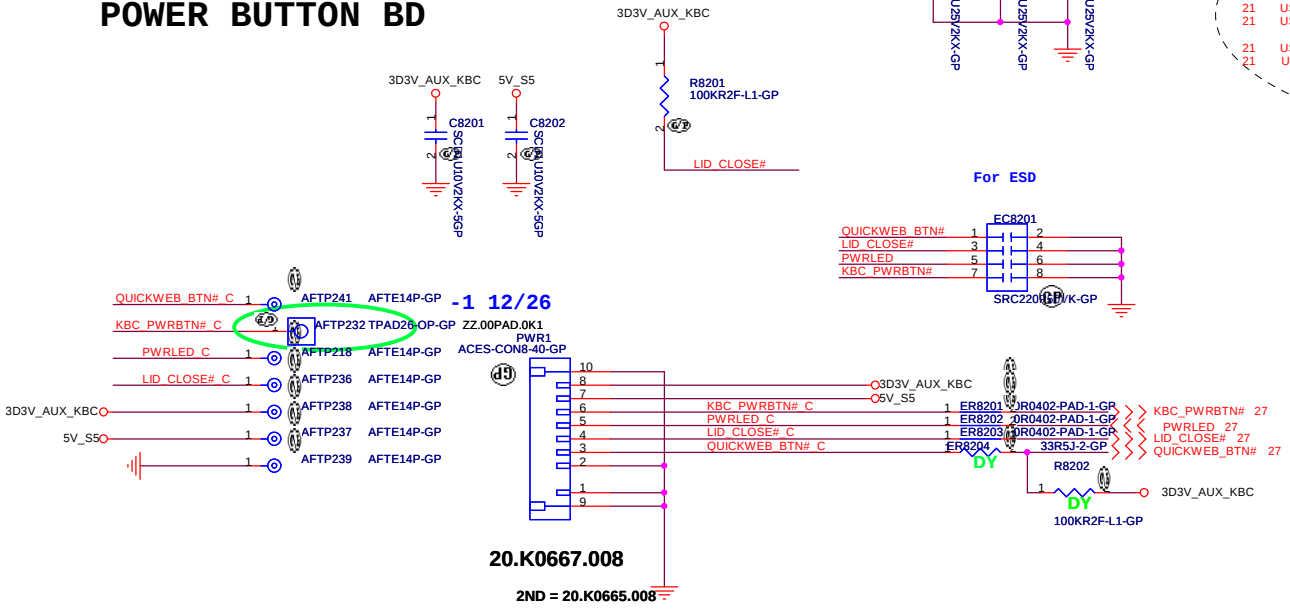
Card Reader BD 15"=DY 17"=PHASE IN



USB BD(USB3.0*1+USB2.0*1)



POWER BUTTON BD

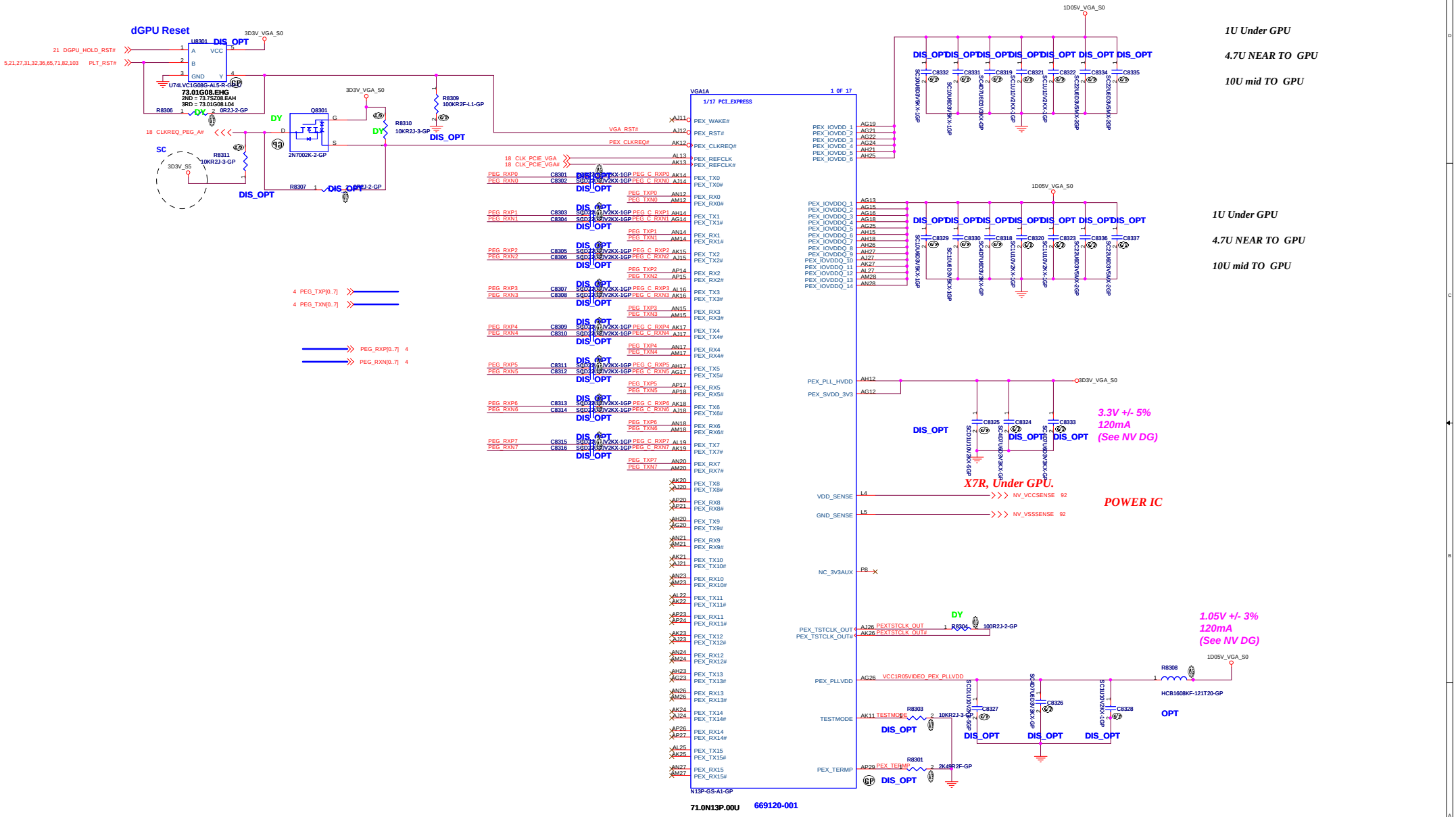


TOUCHPAD BD PAGE 69

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

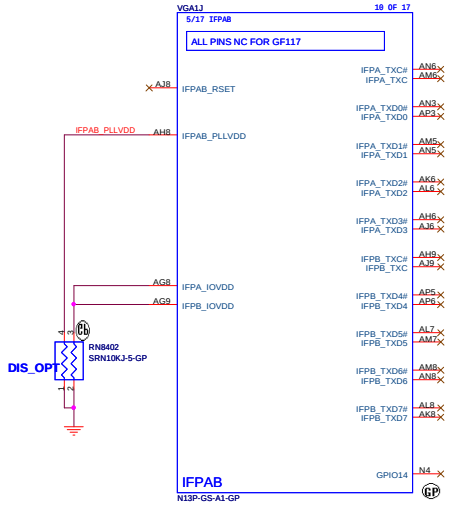
Title: IO Board Connector
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 82 of 103



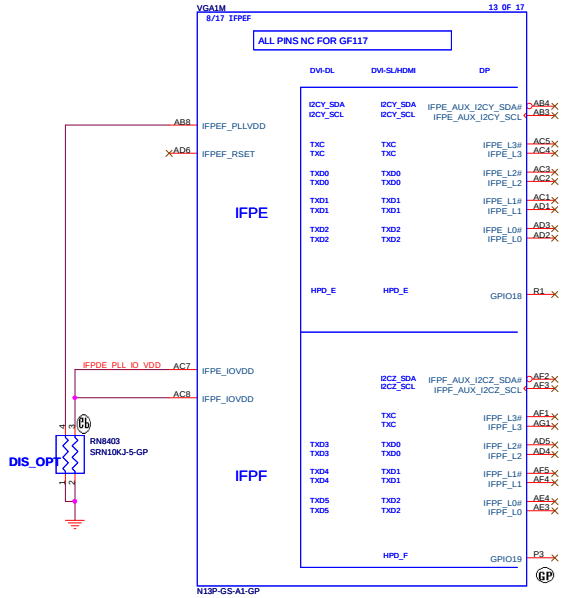
<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU_PCIE/STRAPPING(1/5)		
Size: A2	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 83 of 103	

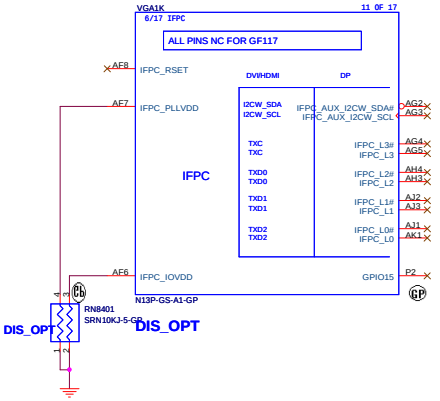
LVDS Interface



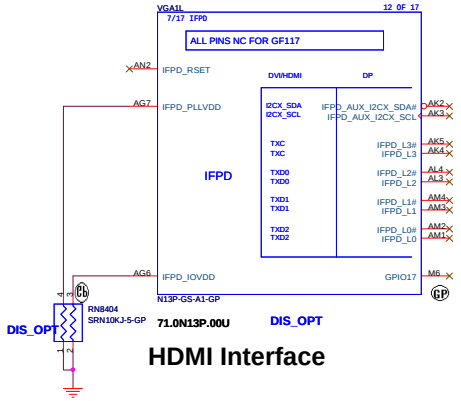
71.0N13P.00U DIS_OPT



71.0N13P.00U DIS_OPT



DIS_OPT



71.0N13P.00U DIS_OPT

HDMI Interface

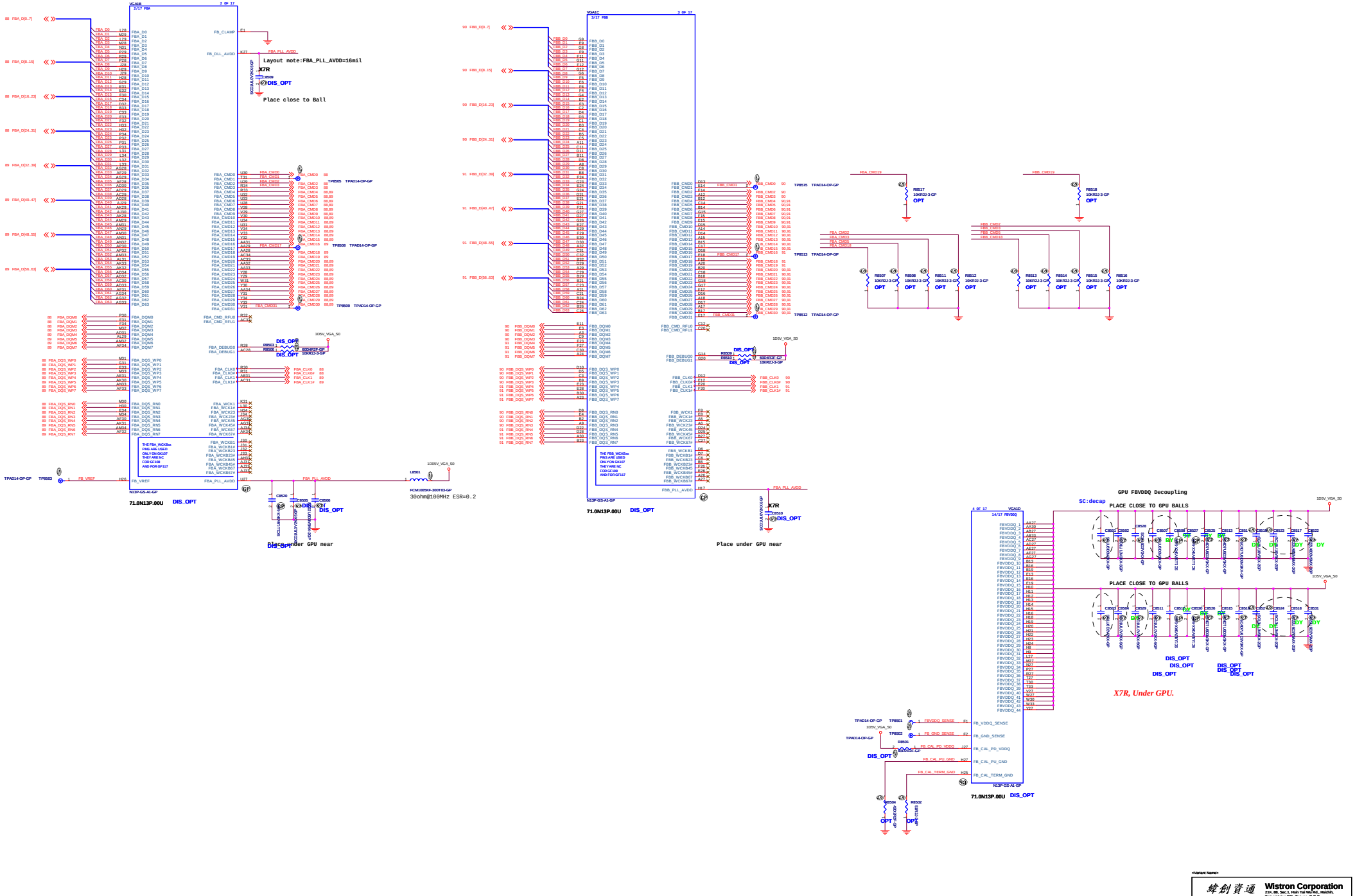
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

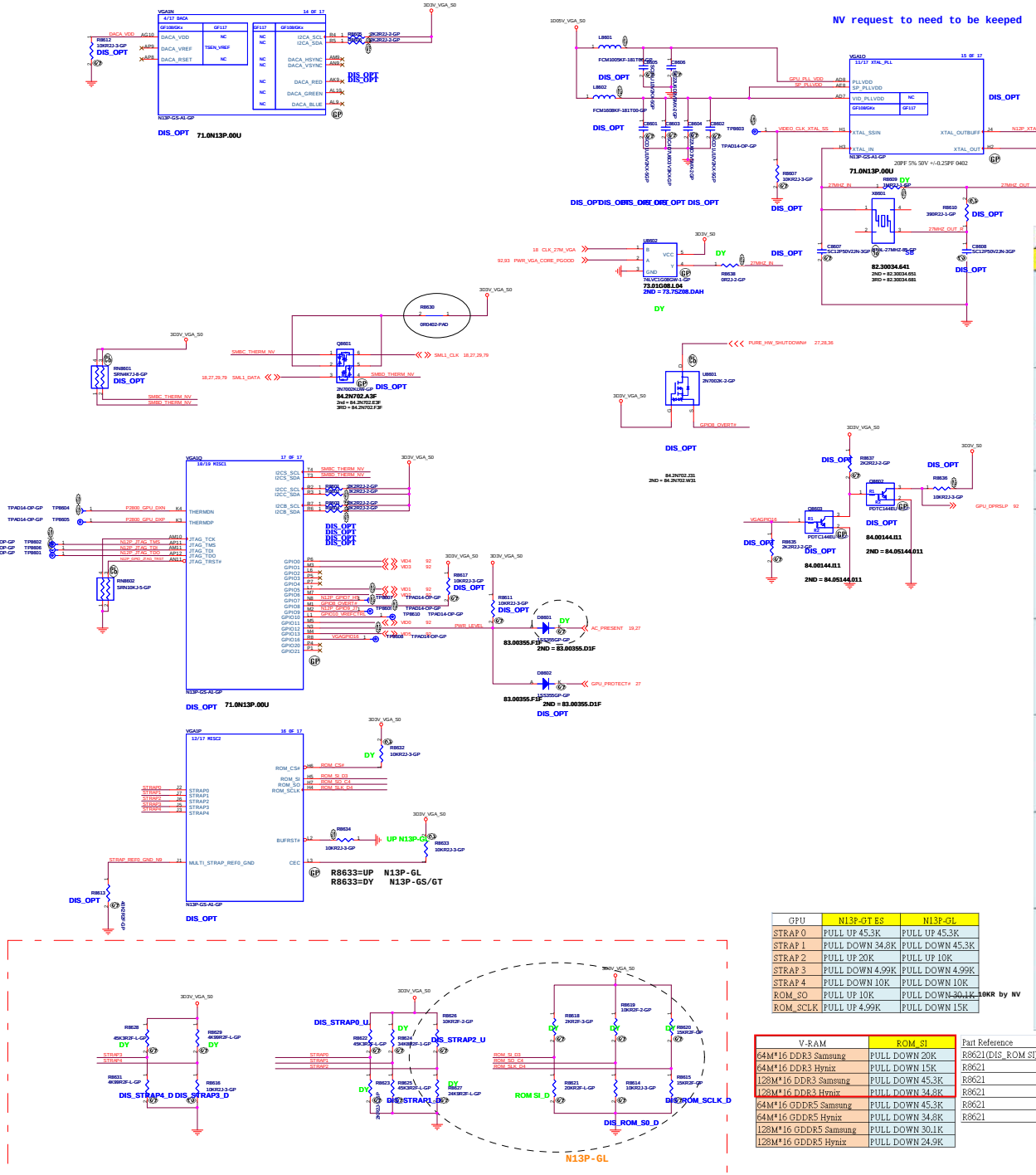
Size: A2 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 84 of 103



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_DP/LVDS/CRT/GPIO(3/5)		
Size A1	Document Number: Colossus		Rev 1
Date: Wednesday, January 04, 2012	Sheet 85 of 103		



01/04/12 N13P-GL

Strap Option for N13P-GL/LP/GS/GT

Strap Name	GPU Sku	Logical strapping name bit[3]	Logical strapping name bit[2]	Logical strapping name bit[1]	Logical strapping name bit[0]	Set your BOM according to this column	Comment from NVIDIA
		XCLK_417/FB[1]	FB_0_BAR_SIZE/FB[0]	SMB_ALT_ADDR	VGA_DEVICE		
ROM_SO	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	1	0	0	1	PULL UP 10K	
	N13P-GS	1	0	0	1	PULL UP 10K	
	N13P-GT	1	0	0	1	PULL UP 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	1	0	1	PULL DOWN 30.1K	
		PCI_DEVID[4]	SUR_VENDOR	PCI_DEVID[3]	PEX_PLL_EN_TERM		
ROM_SCLK	N13P-GL	0	0	1	0	PULL DOWN 15K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13P-LP	1	0	0	0	PULL UP 4.99K	
	N13P-GS	1	0	0	0	PULL UP 4.99K	
	N13P-GT	1	0	0	0	PULL UP 4.99K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13M-GE1	1	0	0	0	PULL UP 4.99K	
		RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]		
ROM_SI	Hynix	X	X	X	X	This is depends on what Vram you will use. Please check latest RVL.	
	Samsung	X	X	X	X		
		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		
STRAP2	N13P-GL	1	0	0	1	PULL UP 10K	N13P-GL DID => 0x0DE9
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13P-LP	0	0	1	1	PULL DOWN 20K	N13P-LP DID => 0x0FD2
	N13P-GS	0	0	1	0	PULL DOWN 15K	N13P-GS QS DID =>0x0FD2
	N13P-GT	0	0	0	1	PULL DOWN 10K	N13P-GT QS DID =>0x0FD1
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13M-GE1	1	0	0	0	PULL UP 4.99K	N13M-GE1 DID => 0x1056
		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		
STRAP1	N13P-GL	0	1	1	1	PULL DOWN 45.3K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13P-LP	0	1	1	0	PULL DOWN 34.8K	
	N13P-GS	0	1	1	0	PULL DOWN 34.8K	
	N13P-GT	0	1	1	0	PULL DOWN 34.8K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13M-GE1	0	1	1	0	PULL DOWN 34.8K	
		USER[3]	USER[2]	USER[1]	USER[0]		
STRAP0	N13P-GL	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13P-LP	1	1	1	1	PULL UP 45.3K	
	N13P-GS	1	1	1	1	PULL UP 45.3K	
	N13P-GT	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13M-GE1	1	1	1	1	PULL UP 45.3K	
		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		
STRAP3	N13P-GL	0	0	0	0	PULL DOWN 4.99K	No display for Optimus sku
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13P-LP	0	0	0	0	PULL DOWN 4.99K	
	N13P-GS	0	0	0	0	PULL DOWN 4.99K	
	N13P-GT	0	0	0	0	PULL DOWN 4.99K	
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13M-GE1	0	0	0	0	PULL DOWN 4.99K	
		RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V		
STRAP4	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GS	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GT	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	0	0	1	PULL DOWN 10K	

GPU	N13P-GT ES	N13P-GL
STRAP 0	PULL UP 45.3K	PULL UP 45.3K
STRAP 1	PULL DOWN 34.8K	PULL DOWN 45.3K
STRAP 2	PULL UP 20K	PULL UP 10K
STRAP 3	PULL DOWN 4.99K	PULL DOWN 4.99K
STRAP 4	PULL DOWN 10K	PULL DOWN 10K
ROM_SO	PULL UP 10K	PULL DOWN ~~30.1K~~ 10KR by NV
ROM_SCLK	PULL UP 4.99K	PULL DOWN 15K

V-RAM	ROM_SI
64M*16 DDR3 Samsung	PULL DOWN 20K
64M*16 DDR3 Hynix	PULL DOWN 15K
128M*16 DDR3 Samsung	PULL DOWN 45.3K
128M*16 DDR3 Hynix	PULL DOWN 34.8K
64M*16 GDDR5 Samsung	PULL DOWN 45.3K
64M*16 GDDR5 Hynix	PULL DOWN 34.8K
128M*16 GDDR5 Samsung	PULL DOWN 30.1K
128M*16 GDDR5 Hynix	PULL DOWN 24.9K

Part Reference	Part Number	Value	PCB Footprint
R8621(DIS_ROM SI)	64.20025.6DL	20KR2F-L-GP	R402H16
R8621	64.15025.6DL	15KR2F-GP	R402H16
R8621	64.34825.6DL	34K8R2F-L-GP	R402H16
R8621	64.45325.6DL	45K3R2F-L-GP	R402H16
R8621	64.30125.6DL	30K1R2F-L-GP	R402H16
R8621	64.24925.6DL	24K9R2F-L-GP	R402H16

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., HsiChih, Taipei Hsien 221, Taiwan, R.O.C.

GPU_POWER(4/5)

Size: A1 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 85 of 103

EDP 60A
(TDP 55W)

VGA_CORE

Under GPU

SC:decap

DIS_OPT DIS_OPT DIS_OPT C8711 DY DY DIS_OPT DIS_OPT

C8714 C8713 C8712 C8704 C8703 C8702 C8701

SC:decap

DIS_OPT DIS_OPT DIS_OPT DIS_OPT DIS_OPT DIS_OPT DIS_OPT DIS_OPT

C8731 C8730 C8729 C8728 C8727 C8726 C8725

SC:decap

C8722 C8721 C8724 C8723 C8720 C8719 C8718 C8717

SC:decap NEAR TO GPU

TC8701 C8707 C8706 C8705 C8708 C8710 C8715 C8716

DY DY DY DY DY DY DY DY

DIS_OPT

VGA1F 6 OF 17
13/17 NVVDD

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14 VDD_15 VDD_16 VDD_17 VDD_18 VDD_19 VDD_20 VDD_21 VDD_22 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31 VDD_32 VDD_33 VDD_34 VDD_35 VDD_36 VDD_37 VDD_38 VDD_39 VDD_40 VDD_41 VDD_42 VDD_43 VDD_44 VDD_45 VDD_46 VDD_47 VDD_48 VDD_49 VDD_50 VDD_51 VDD_52 VDD_53 VDD_54 VDD_55 VDD_56 VDD_57 VDD_58 VDD_59 VDD_60 VDD_61 VDD_62 VDD_63 VDD_64 VDD_65 VDD_66 VDD_67 VDD_68 VDD_69 VDD_70 VDD_71 VDD_72

N13P-GS-A1-GP

71.0N13P.00U DIS_OPT

VGA1I 9 OF 17
15/17 GND_1/2

GND_1 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_2 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_3 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_4 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70

GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114 GND_115 GND_116 GND_117 GND_118 GND_119 GND_120 GND_121 GND_122 GND_123 GND_124 GND_125 GND_126 GND_127 GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140

AM25 AN1 AN10 AN13 AN16 AN19 AN22 AN25 AN30 AN34 AN4 AN7 AP2 AP33 B1 B10 B22 B25 B28 B31 B34 B4 B7 C10 C13 C19 C22 C25 C28 C7 D2 D31 D33 E10 E22 E25 E5 E7 F28 F7 G10 G13 G16 G19 G2 G22 G25 G28 G3 G30 G32 G33 G5 G7 K2 K28 K30 K32 K33 K5 K7 M13 M15 M17 M18 M20 M22 N12 N14 N16

N13P-GS-A1-GP

71.0N13P.00U DIS_OPT

VGA1H 8 OF 17
16/17 GND_2/2

N19 N2 N21 N23 N28 N30 N32 N33 N5 N7 P13 P15 P17 P18 P20 P22 R12 R14 R16 R19 R21 R23 T13 T15 T17 T18 T2 T20 T22

GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169

GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198

T28 T32 T5 T7 U12 U14 U16 U19 U21 U23 V12 V14 V16 V19 V21 V23 W13 W15 W17 W18 W20 W22 W28 Y12 Y14 Y16 Y19 Y21 Y23

AG11 GND_F GND_H AH11

GND_OPT_1 GND_OPT_2 C16 W32

Optional CMD GNDs (2)
NC for 4-Lyr cards

N13P-GS-A1-GP

DIS_OPT 71.0N13P.00U

VGA1G 7 OF 17
17/17 NC/VDD33

AC6 AJ28 AJ4 AJ5 AL11 C15 D19 D20 D23 D26 H31 T8 V32

NC#AC6 NC#AJ28 NC#AJ4 NC#AJ5 NC#AL11 NC#C15 NC#D19 NC#D20 NC#D23 NC#D26 NC#H31 NC#T8 NC#V32

VDD33_1 VDD33_2 VDD33_3 VDD33_4

J8 K8 L8 M8

N13P-GS-A1-GP

DIS_OPT 71.0N13P.00U

3D3V_VGA_S0

DIS_OPT DIS_OPT DIS_OPT DIS_OPT

C8709 SC1U6D3V2KX-GP X7R C8734 X7R C8732 X7R C8733 X7R C8735

DIS_OPT

DIS_OPT

C8736 SC4D7U6D3V3KX-GP

0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU

VGA1E 5 OF 17
9/17 XVDD

CONFIGURABLE POWER CHANNELS

XVDD_1 XVDD_2 XVDD_3 XVDD_4 XVDD_5 XVDD_6 XVDD_7 XVDD_8 XVDD_9 XVDD_10 XVDD_11 XVDD_12 XVDD_13 XVDD_14 XVDD_15 XVDD_16 XVDD_17 XVDD_18 XVDD_19 XVDD_20 XVDD_21 XVDD_22 XVDD_23 XVDD_24 XVDD_25 XVDD_26 XVDD_27 XVDD_28 XVDD_29 XVDD_30 XVDD_31 XVDD_32 XVDD_33 XVDD_34 XVDD_35 XVDD_36 XVDD_37 XVDD_38

U1 U2 U3 U4 U5 U6 U7 U8 V1 V2 V3 V4 V5 V6 V7 V8 W2 W3 W4 W5 W7 W8 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8

DIS_OPT

XVDD_1~38=No Connect

<Variant Name>

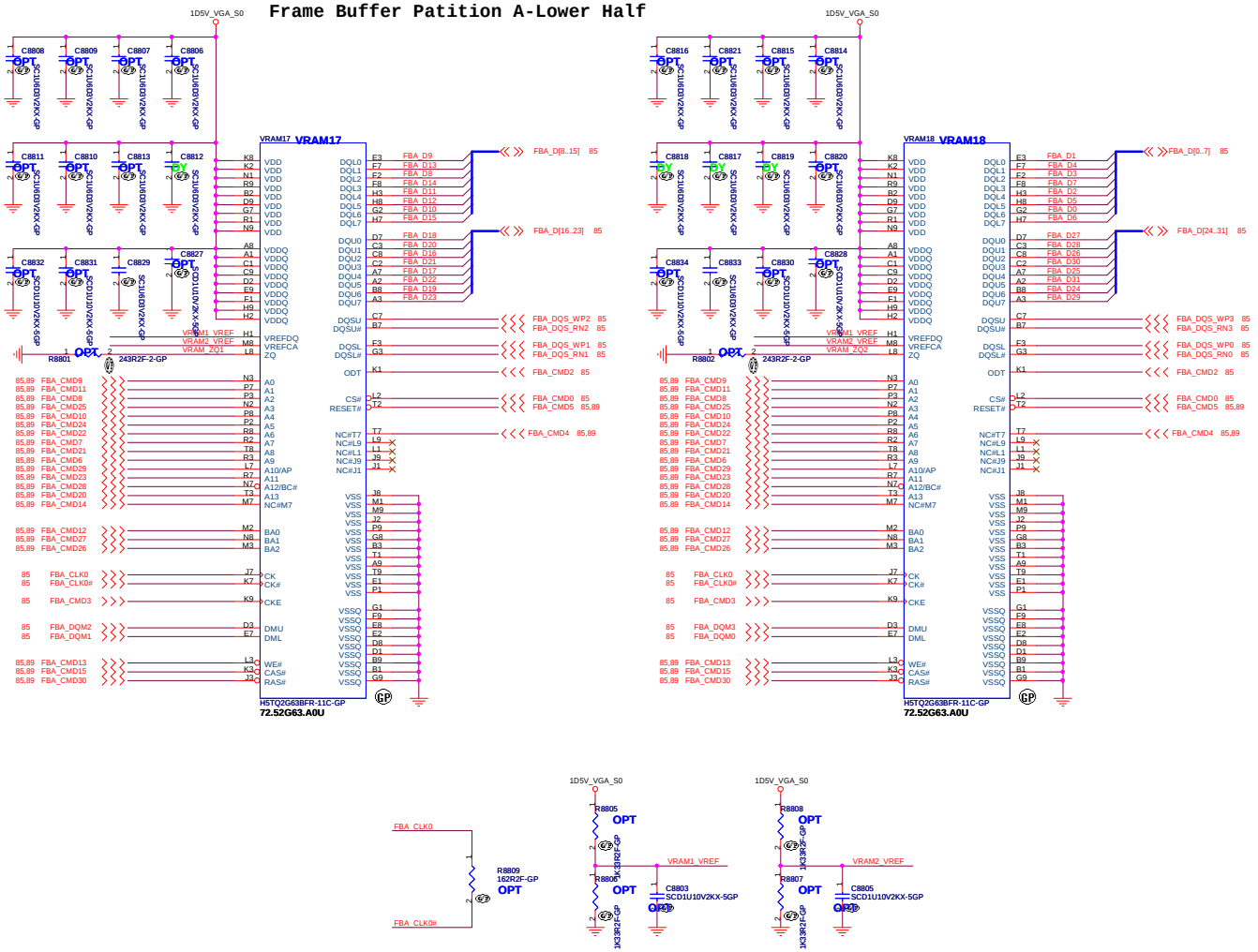
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size: Custom | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 87 of 103

Frame Buffer Patition A-Lower Half



<Variant Name>

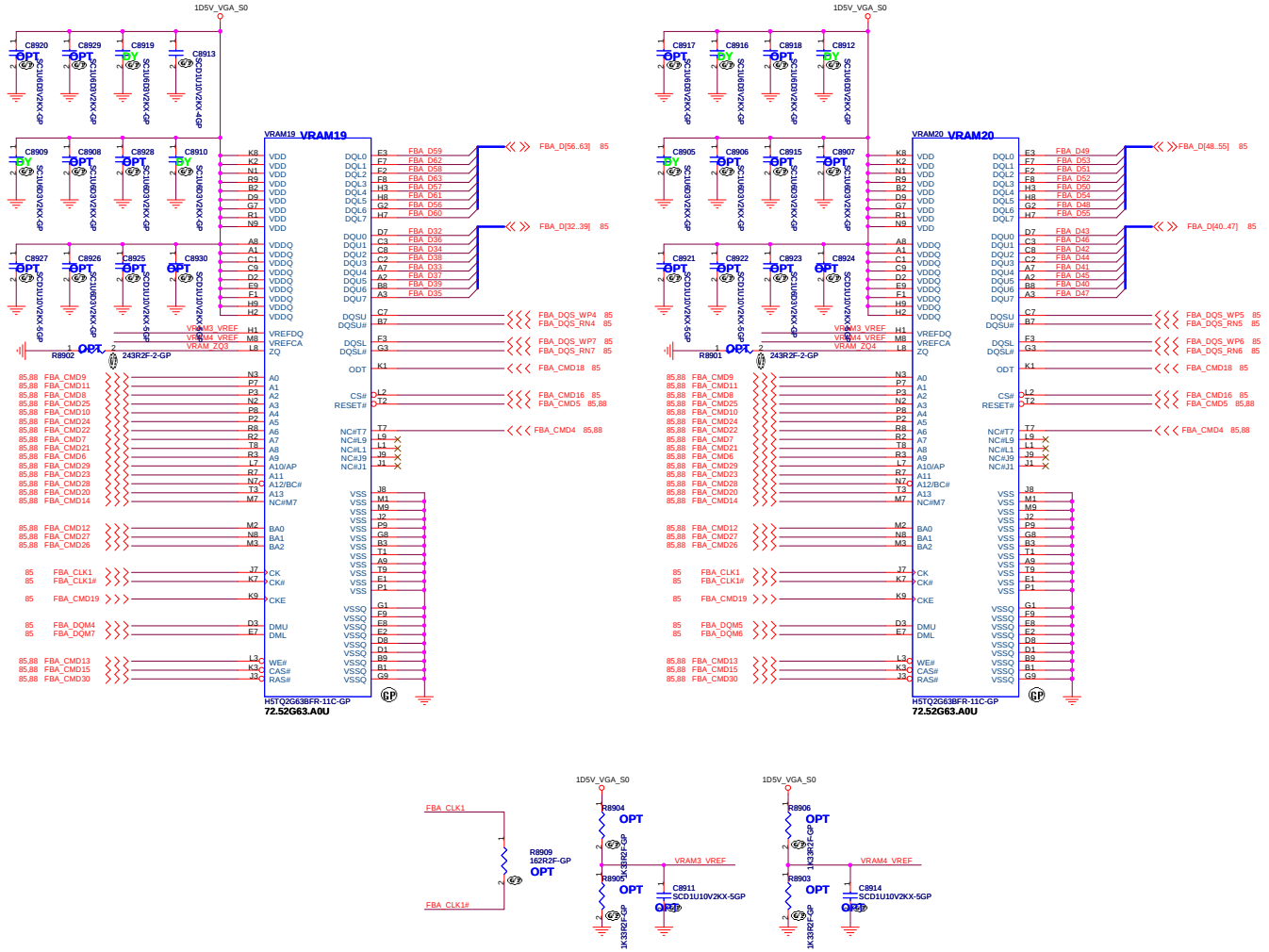
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A2 | Document Number: Colossus | Rev: 1

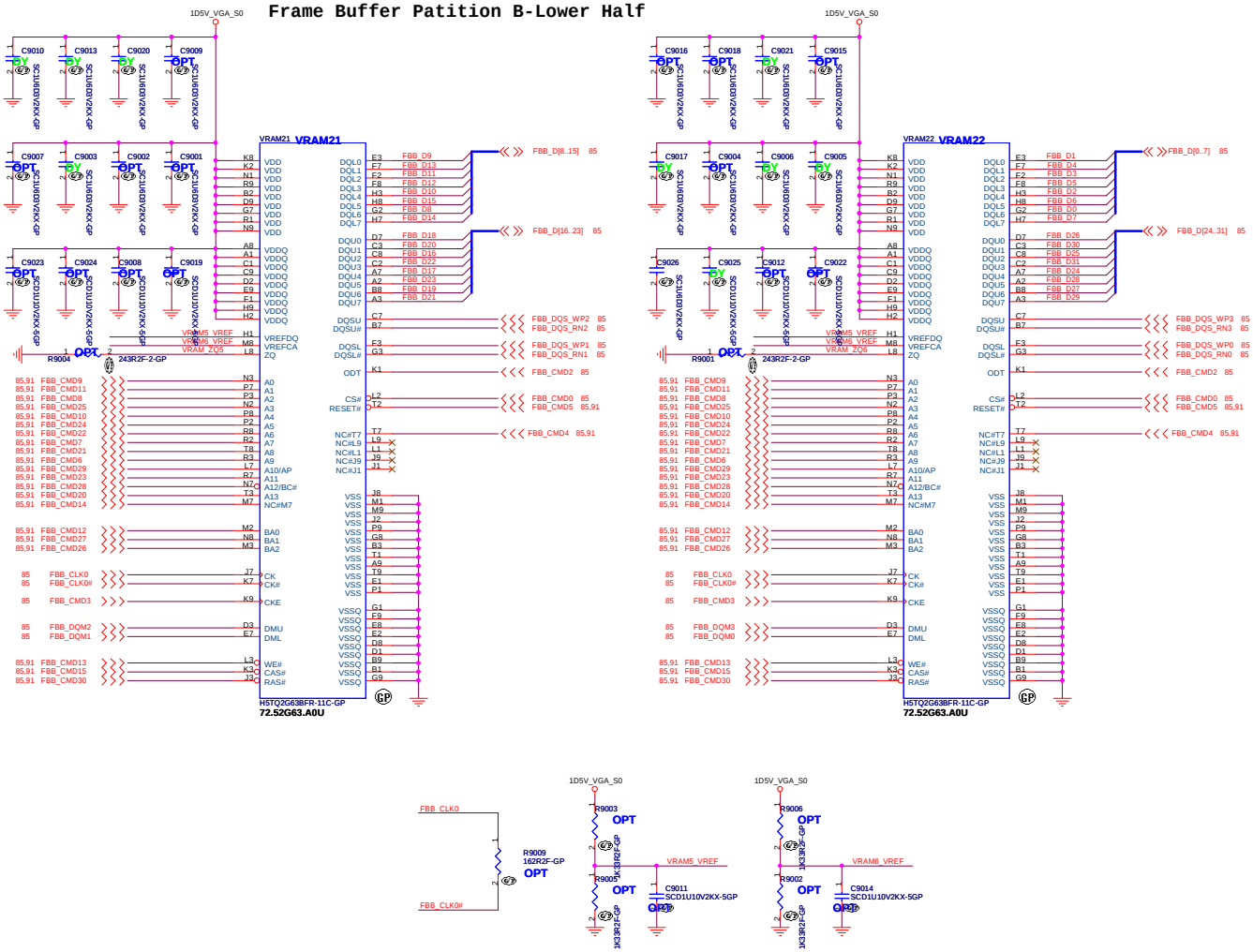
Date: Wednesday, January 04, 2012 | Sheet 88 of 103

Frame Buffer Patition A-Upper Half



<Variant Name>	緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU-VRAM3,4 (2/4)	
Size: A2	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 89 of 103	

Frame Buffer Patition B-Lower Half



<Variant Name>

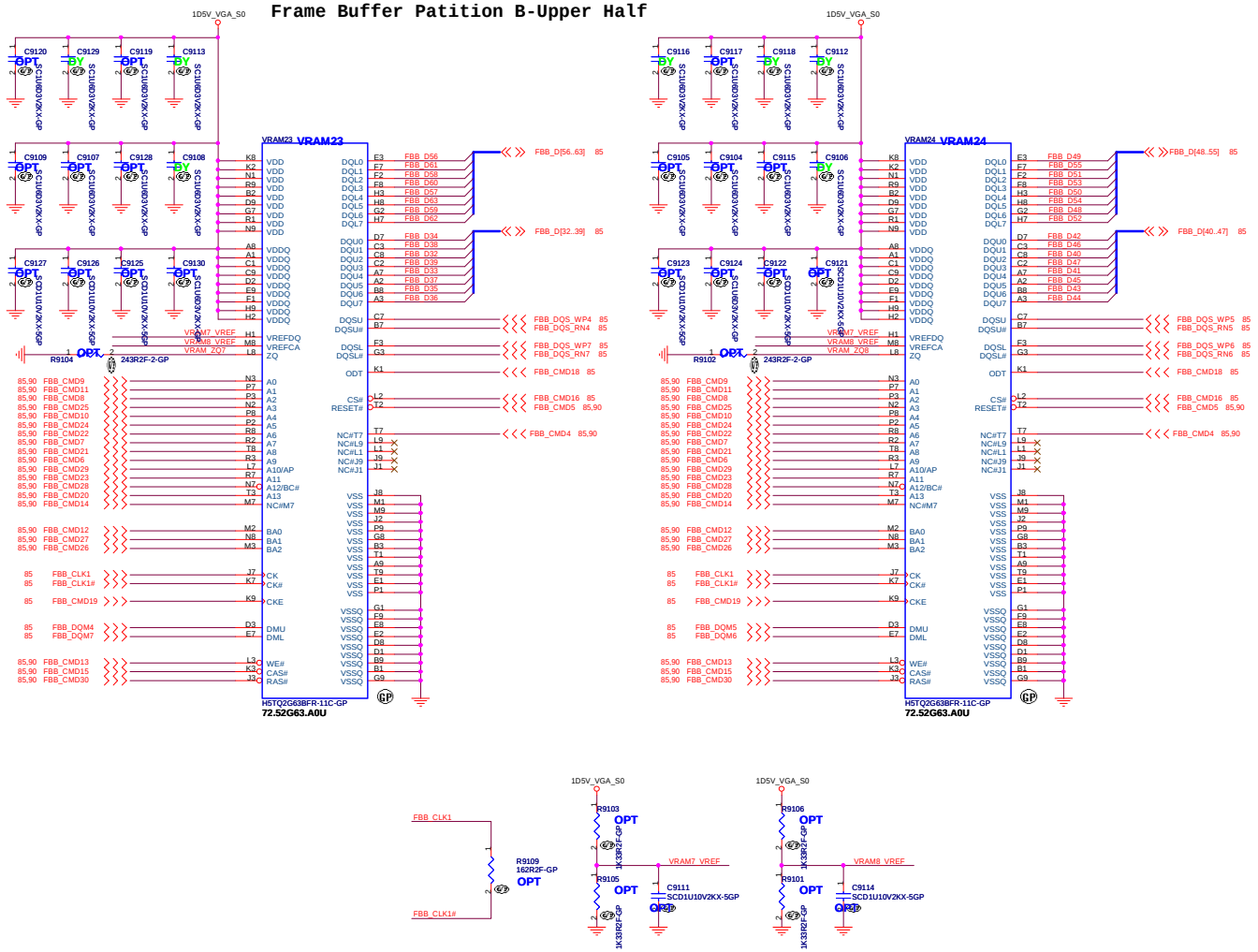
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 90 of 103

Frame Buffer Patition B-Upper Half



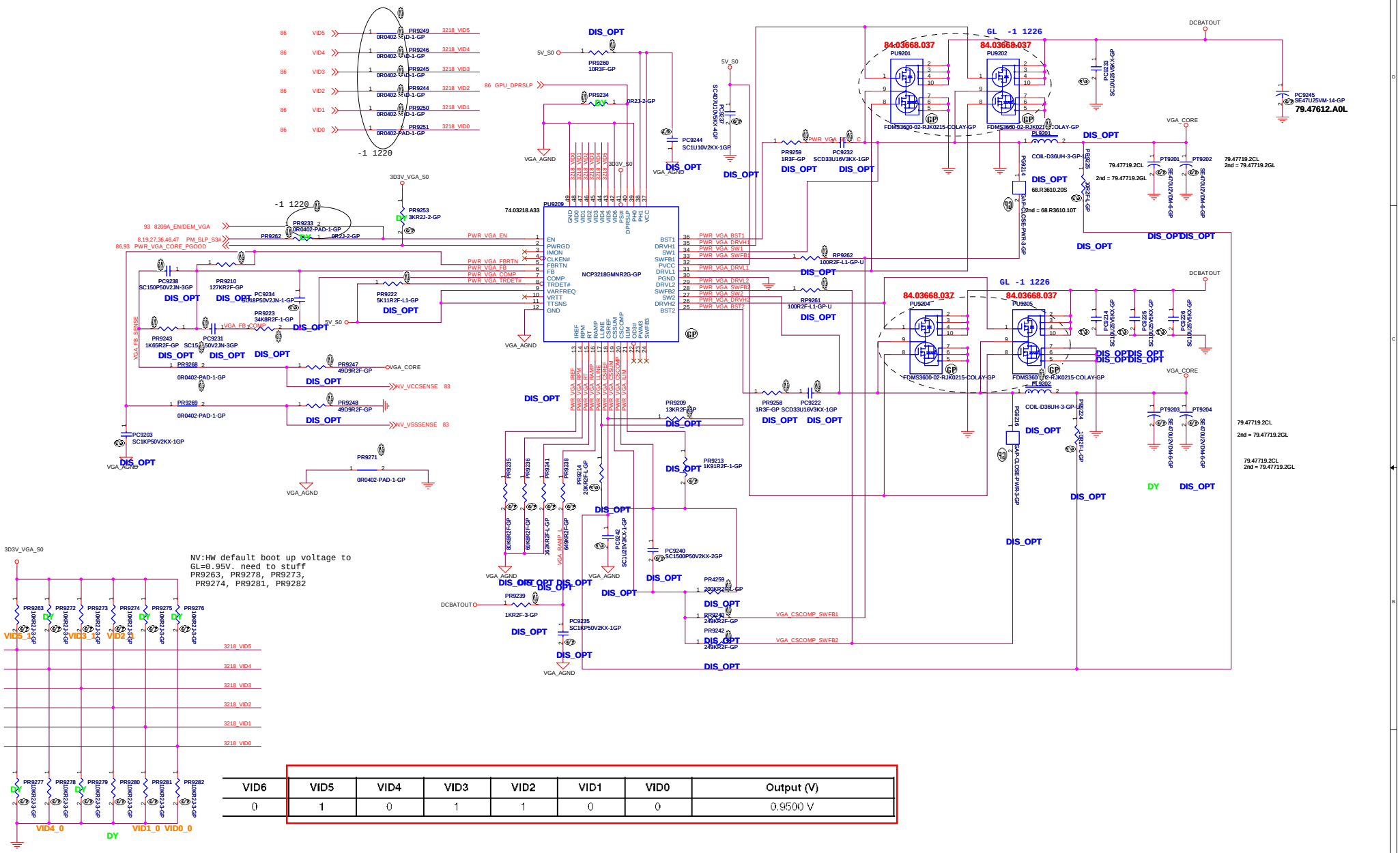
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A2	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 91 of 103



NV:HW default boot up voltage to
GL=0.95V, need to stuff
PR9263, PR9278, PR9273,
PR9274, PR9281, PR9282

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	1	1	0	0	0.9500 V

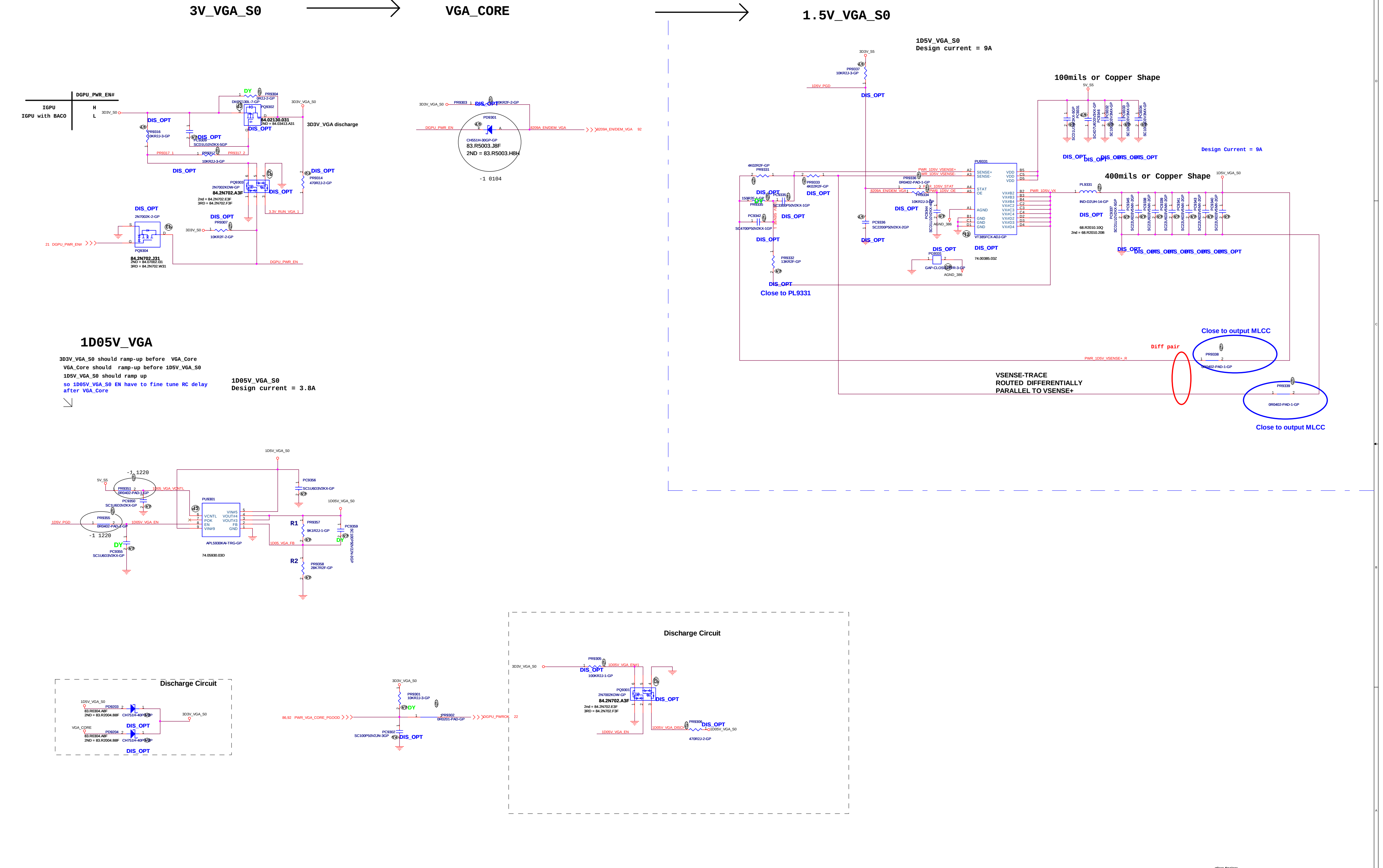
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP3218 VGACORE25W

Size	Document Number	Rev
A2	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 92 of 103



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DISCRETE VGA POWER		
Size A1	Document Number: Colossus		Rev 1
Date: Wednesday, January 04, 2012	Sheet 93	of 103	

(Blanking)

<Core Design>

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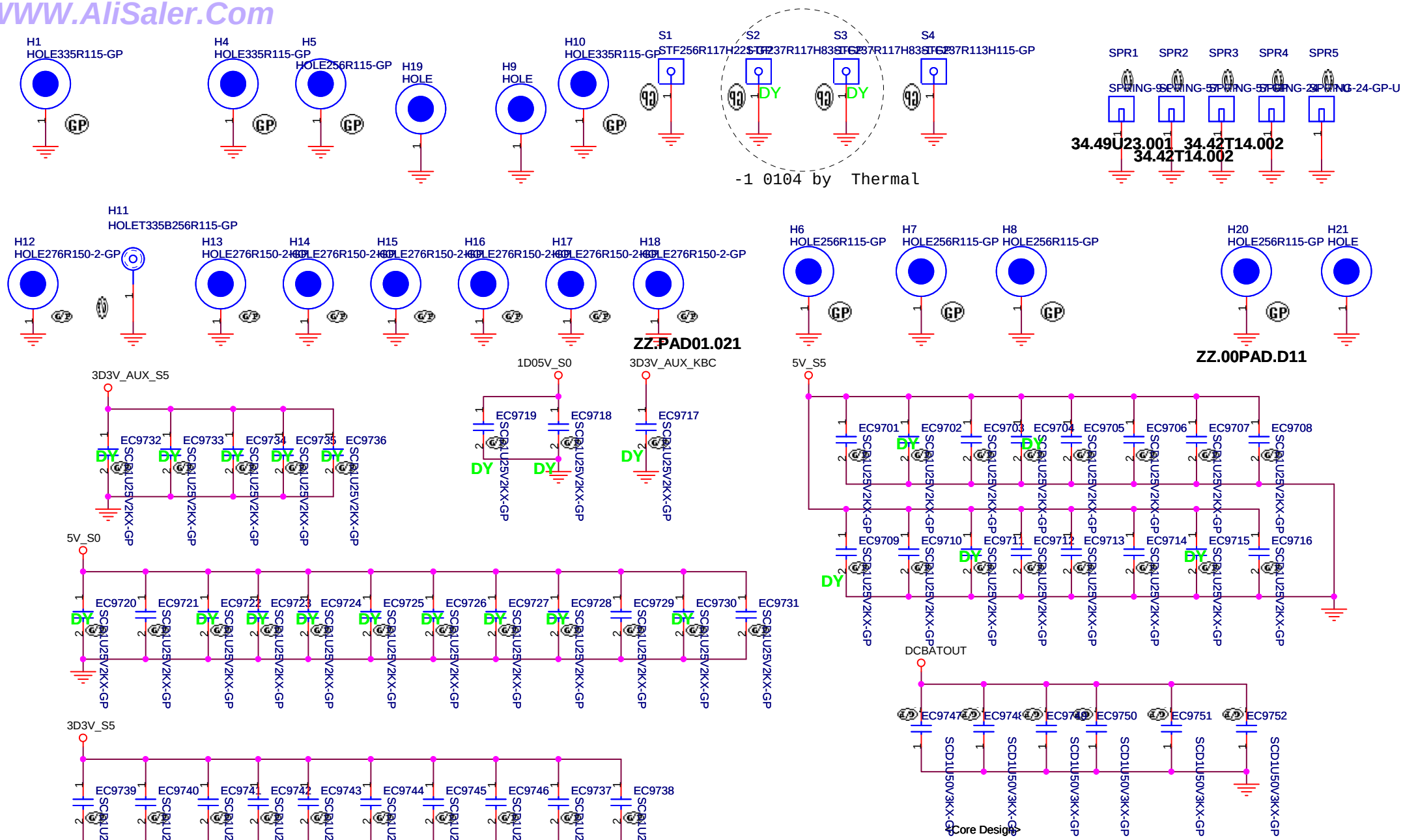

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UNUSED PARTS/EMI Capacitors

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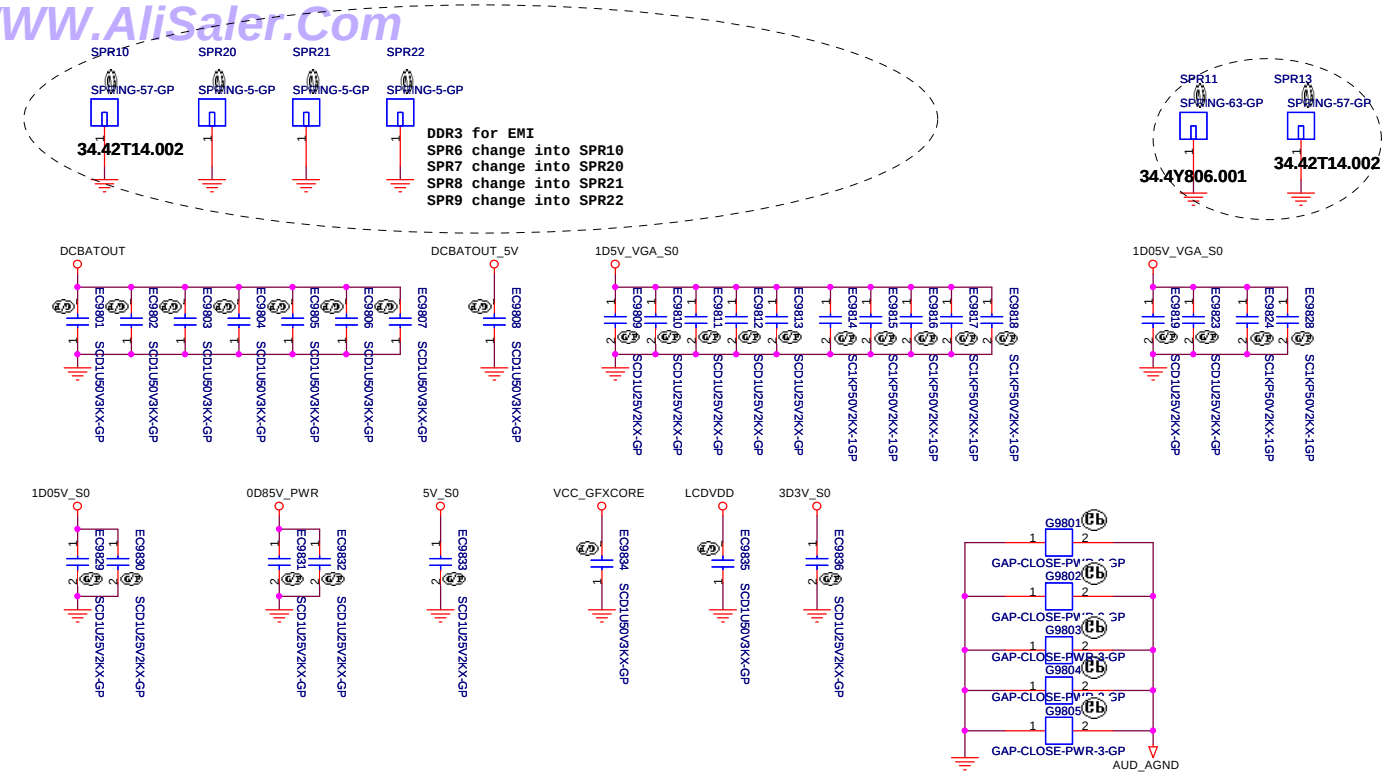

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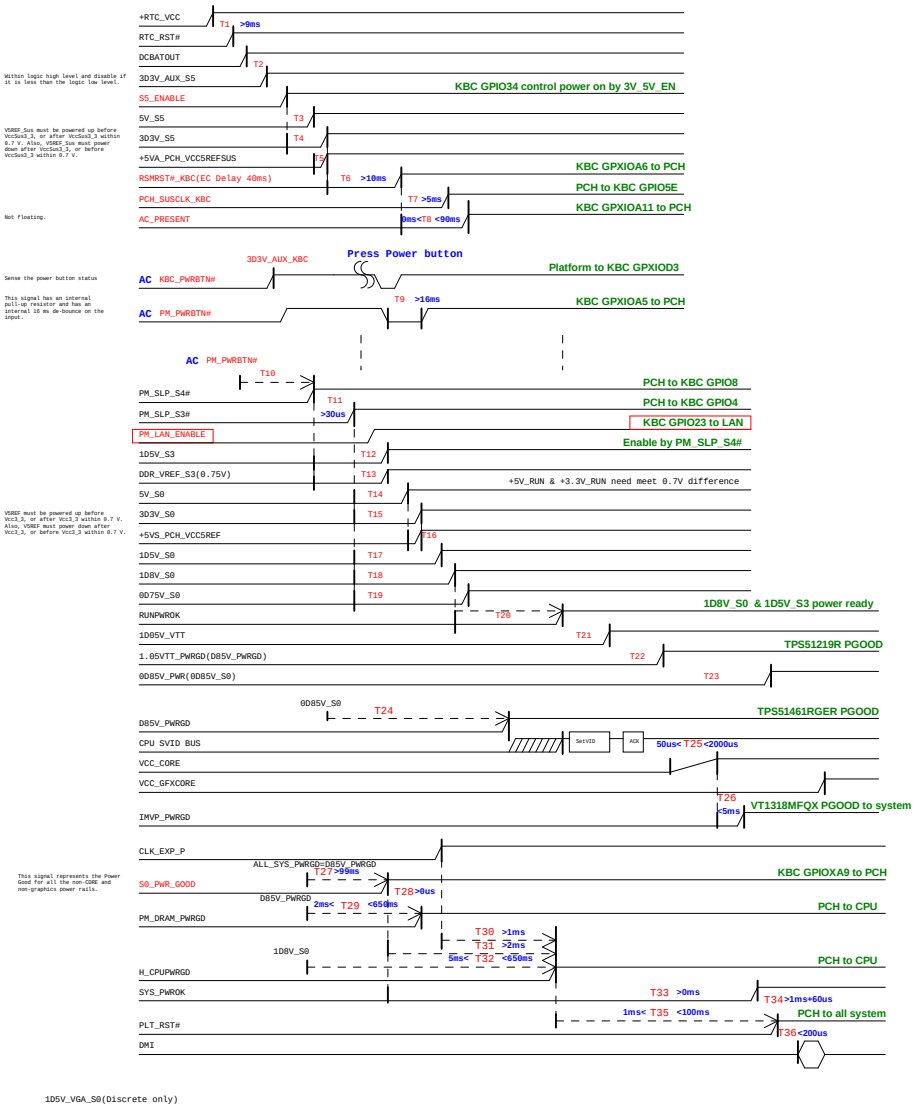
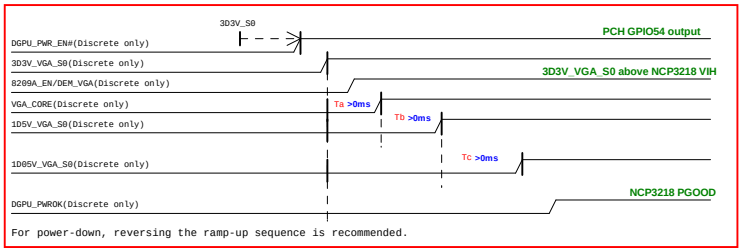
Chief River Platform Power Sequence

(AC mode)

red word: KBC GPIO



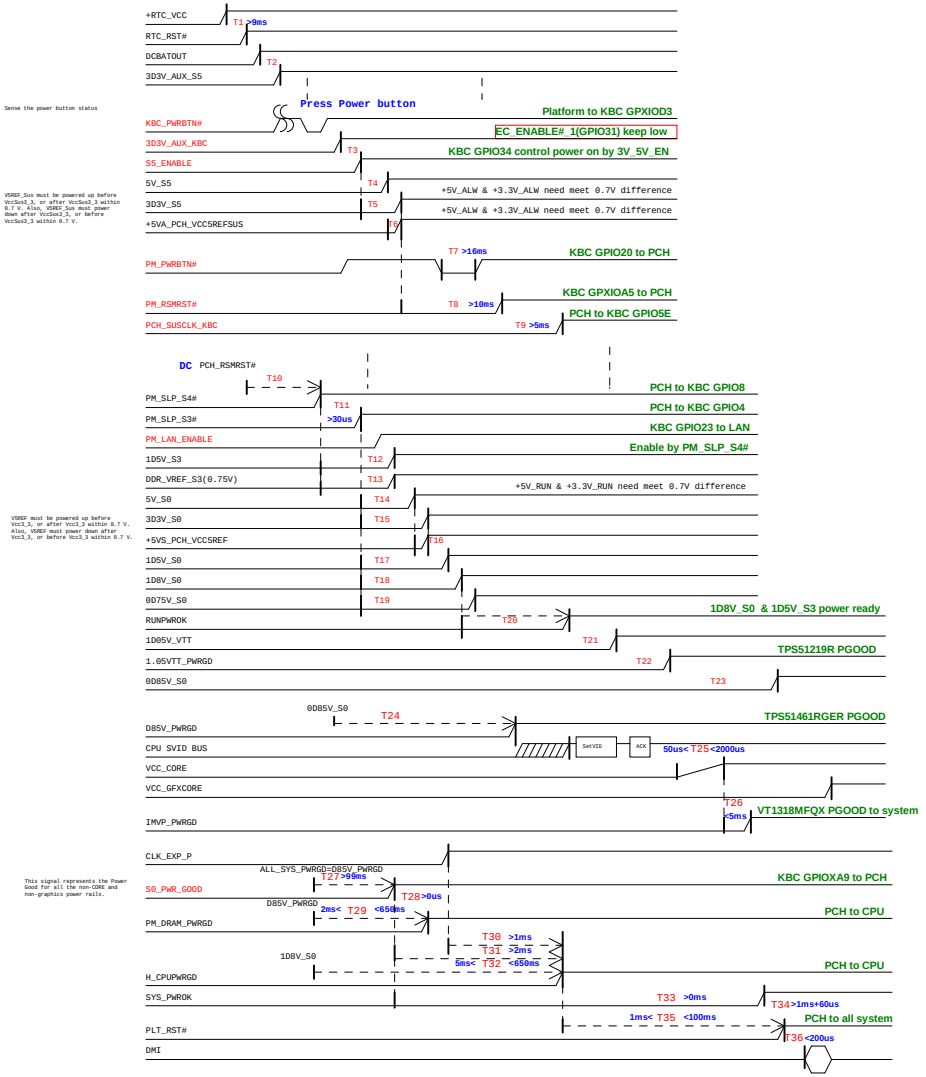
N13P Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

red word: KBC GPIO



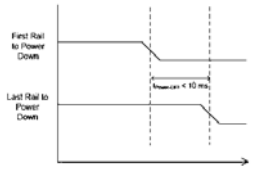


Figure 18. Recommended Power Off Sequencing Order

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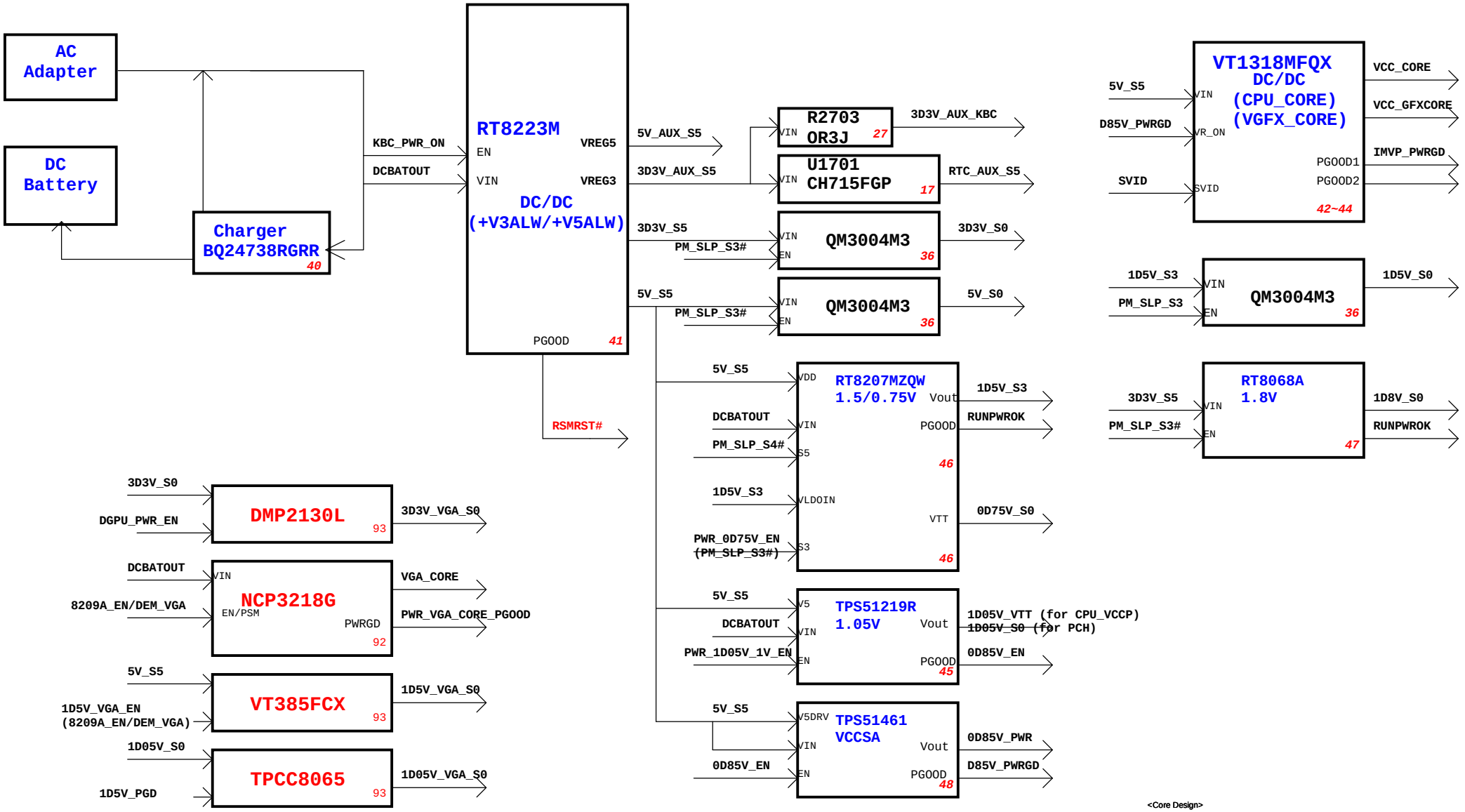
COLOSUSS POWER BLOCK DIAGRAM



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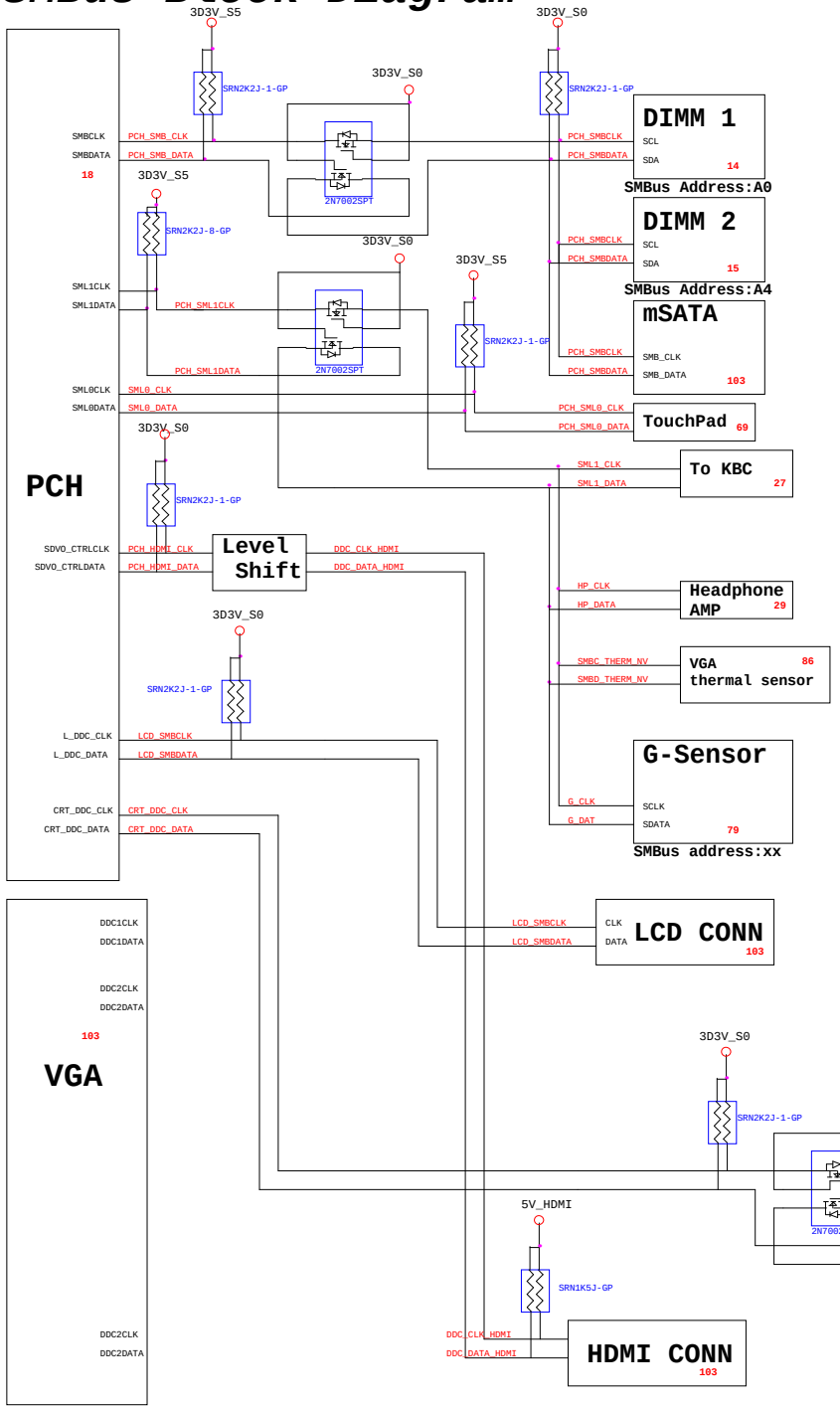
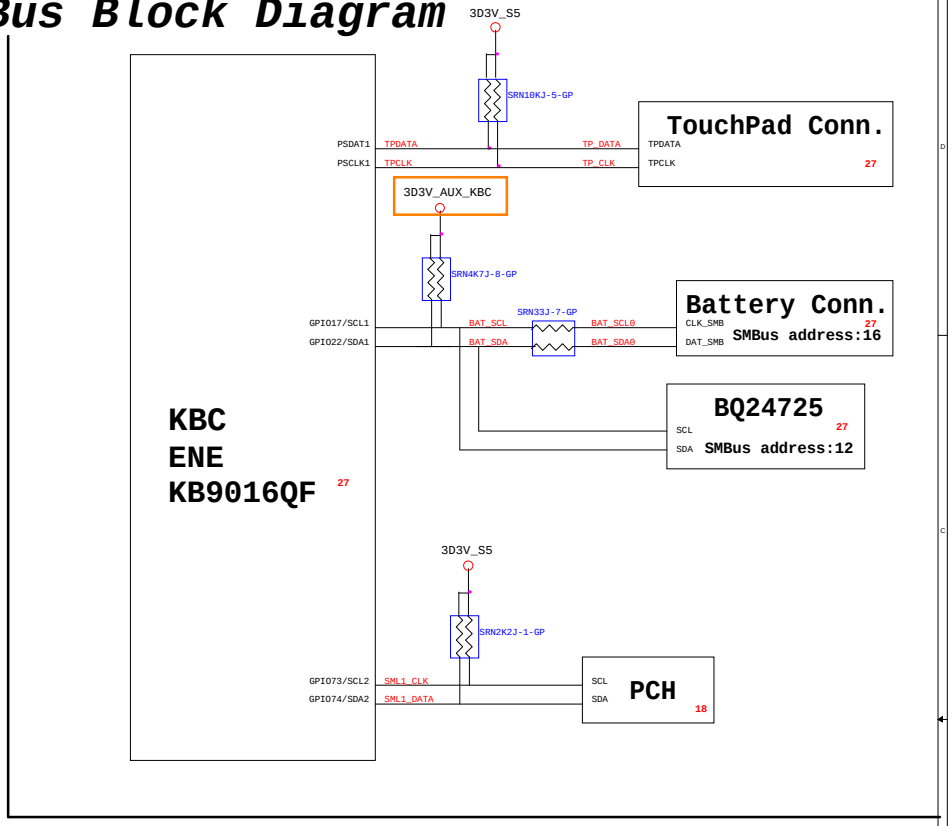
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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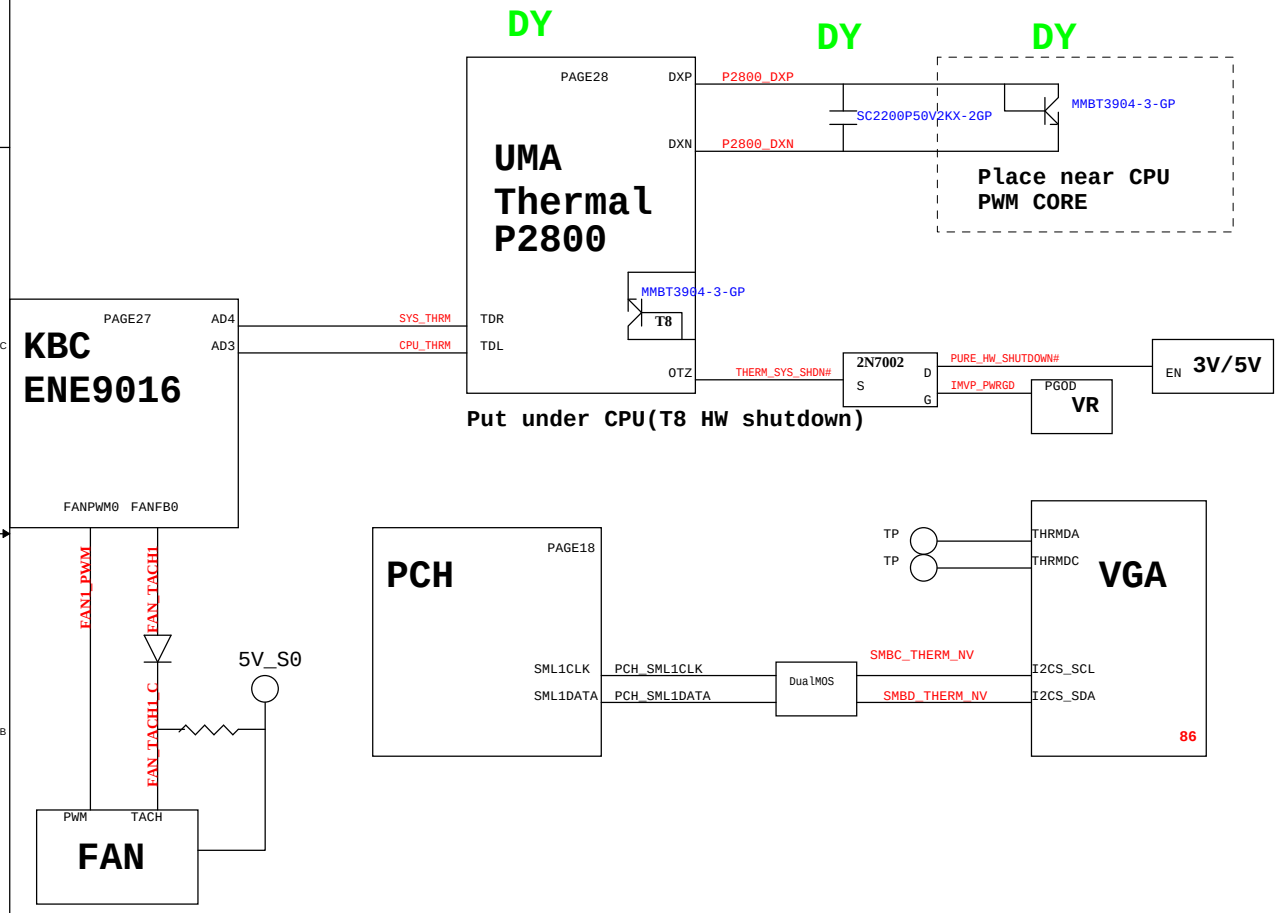
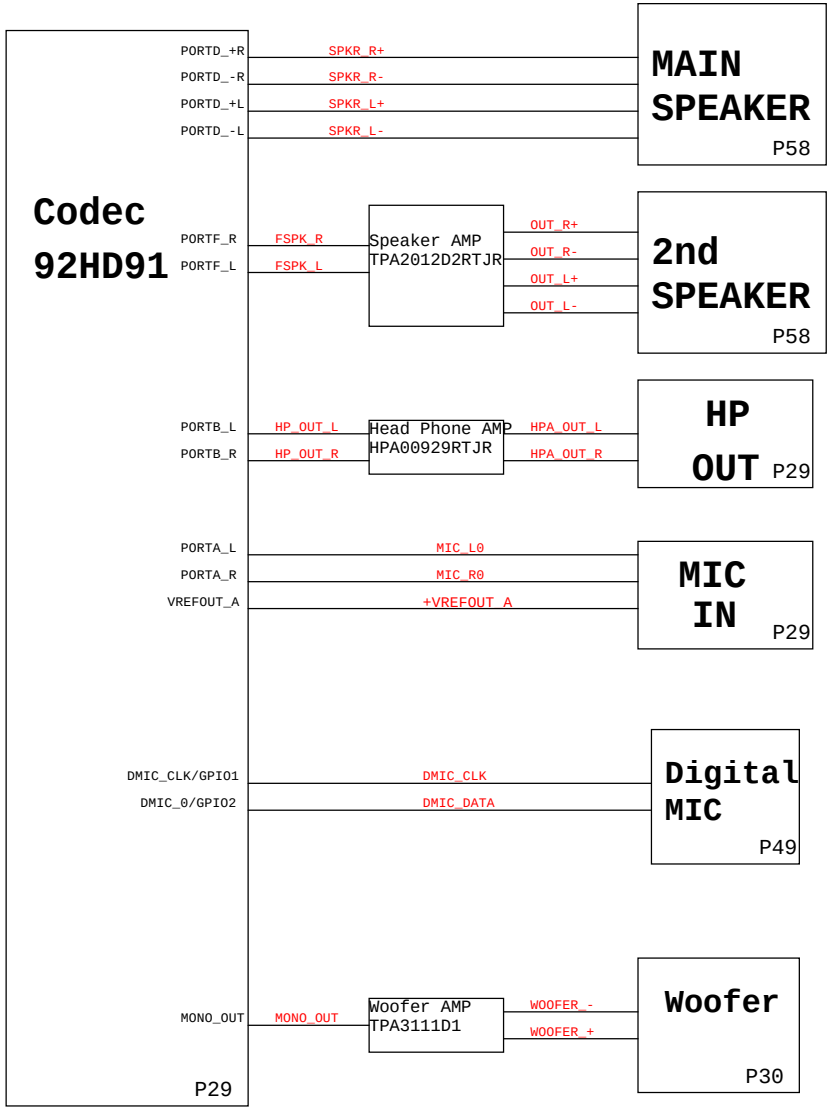
Thermal Block Diagram



Audio Block Diagram



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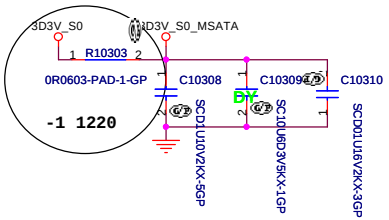
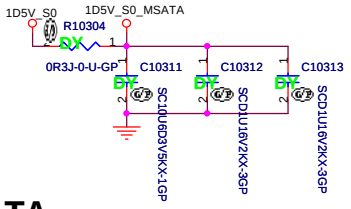
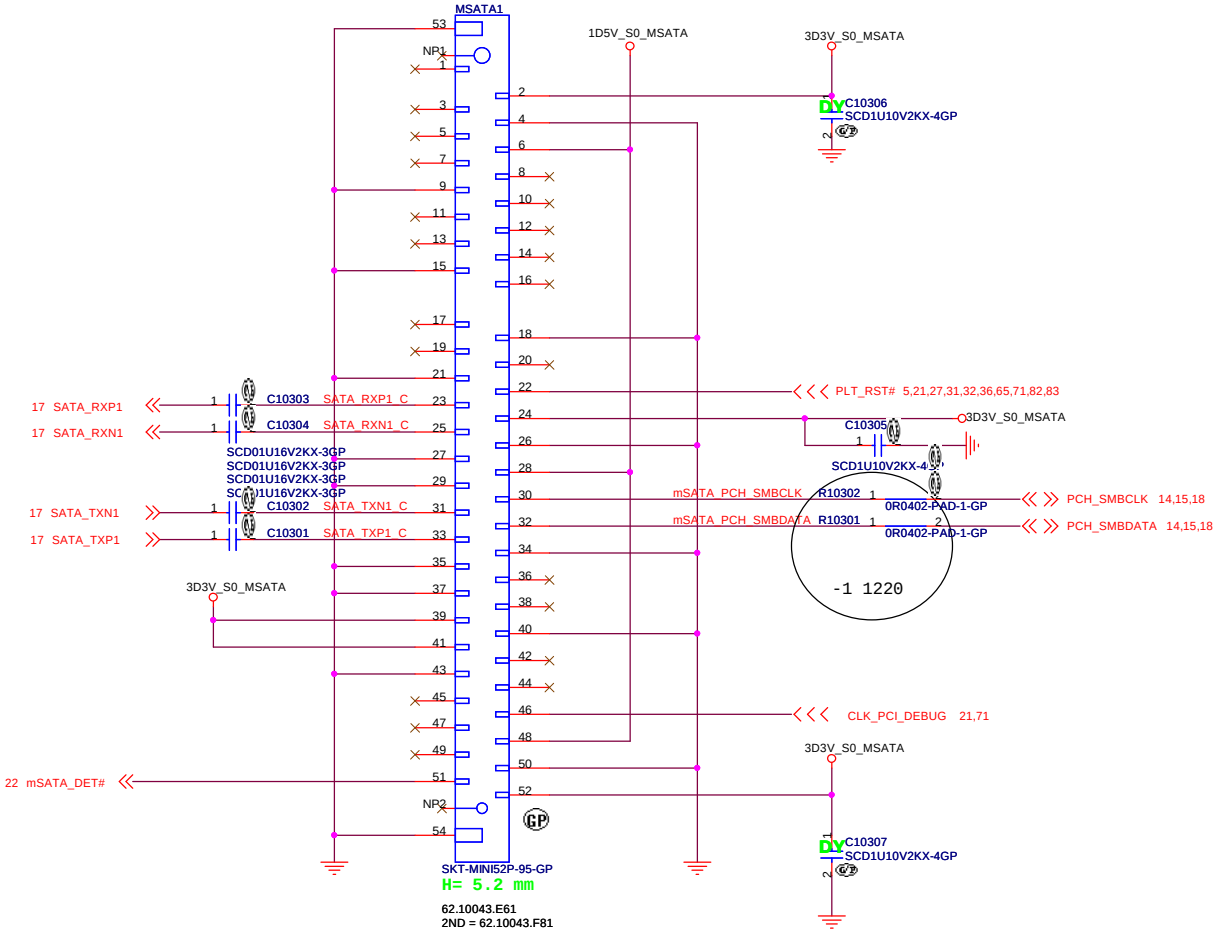




mSATA



677867-FM5

Pin #	Name	Description		Pin #	Name	Description
1	Reserved	NC		2	V33	3.3V power
3	Reserved	NC		4	GND	Return Current Path
5	Reserved	NC		6	V15	1.5V power (Unused)
7	Reserved	NC		8	Reserved	NC
9	GND	Return Current Path		10	Reserved	NC
11	Reserved	NC		12	Reserved	NC
13	Reserved	NC		14	Reserved	NC
15	GND	Return Current Path		16	Reserved	NC
Key						
17	Reserved	NC		18	GND	Return Current Path
19	Reserved	NC		20	Reserved	NC
21	GND	Return Current Path		22	Reserved	NC
23	B+	Differential Signal Pair B (Device Tx)		24	V33	3.3V power
25	B-			26	GND	Return Current Path
27	GND	Return Current Path		28	V15	1.5V power (Unused)
29	GND	Return Current Path		30	Reserved	NC
31	A-	Differential Signal Pair A (Device Rx)		32	Reserved	NC
33	A+			34	GND	Return Current Path
35	GND	Return Current Path		36	Reserved	NC
37	GND	Return Current Path		38	Reserved	NC
39	V33	3.3V power		40	GND	Return Current Path
41	V33	3.3V power		42	Reserved	NC
43	GND	Return Current Path		44	Reserved	NC
45	Vendor	No connect at Host side		46	Reserved	NC
47	Vendor	No connect at Host side		48	V15	1.5V power (Unused)
49	DAS/DSS*1	Drive Activity Signal		50	GND	Return Current Path
51	Presense*2	Device Presense		52	V33	3.3V power

Note: *1: DAS/DSS signal is not use for this drive. (DAS Signal output is optional)

*2: Presense pin is Connected to GND by device side. (220Ω Pull Down)

1st	677867-FM5
2nd	677867-AM5
3rd	677867-BM5
4th	677867-LM5

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Title: mSATA

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