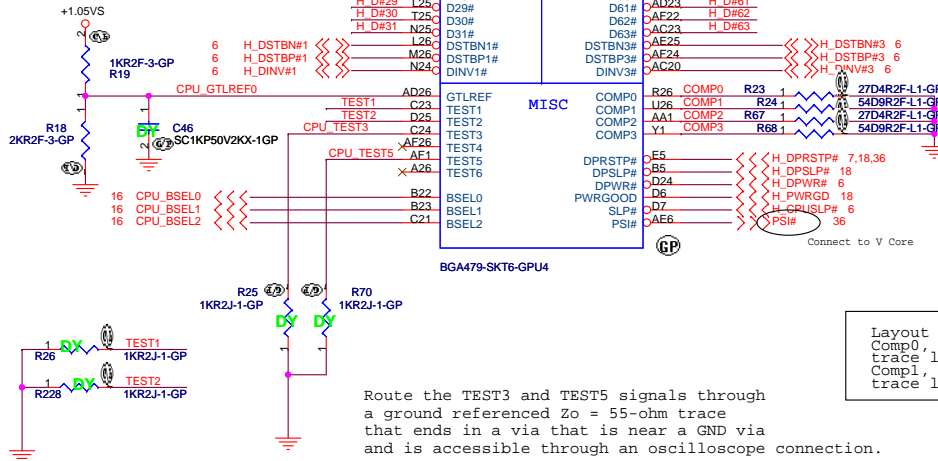


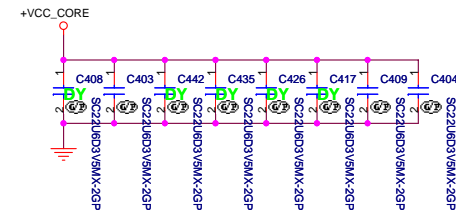
Title			
CPU (1 of 2)			
Size	Document Number	Rev	
	Warrior	SC	
Date:	Monday, January 07, 2008	Sheet 3 of 42	

H_DINV#3..0] << >> H_DINV#3..0] 6
H_DSTBN#3..0] << >> H_DSTBN#3..0] 6
H_DSTBP#3..0] << >> H_DSTBP#3..0] 6
H_D#63..0] << >> H_D#63..0] 6

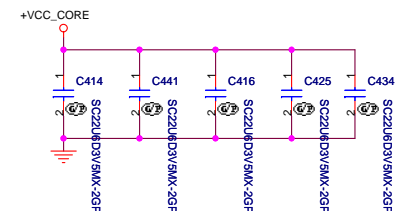
Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF



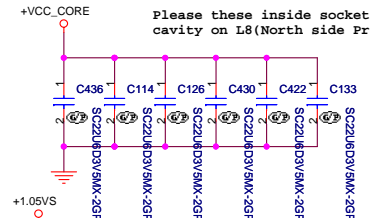
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (3 of 2)			
Size	Document Number	Rev	SC
Warrior			
Date: Monday, January 07, 2008	Sheet 4	of 42	



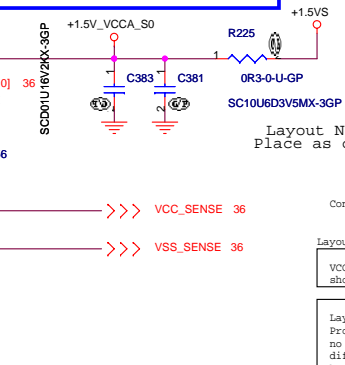
Please these inside socket cavity on L8(South side Secondary)



Please these inside socket
cavity on L8(North side Primary)



layout note: "1D5V_V
as short as possible



Layout Note:
Place as close as possible to the CPU VCCA pin.

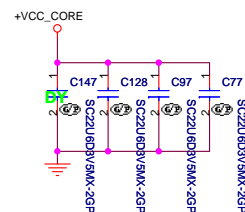
Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Please these inside socket
cavity on L8(North side Secondary)

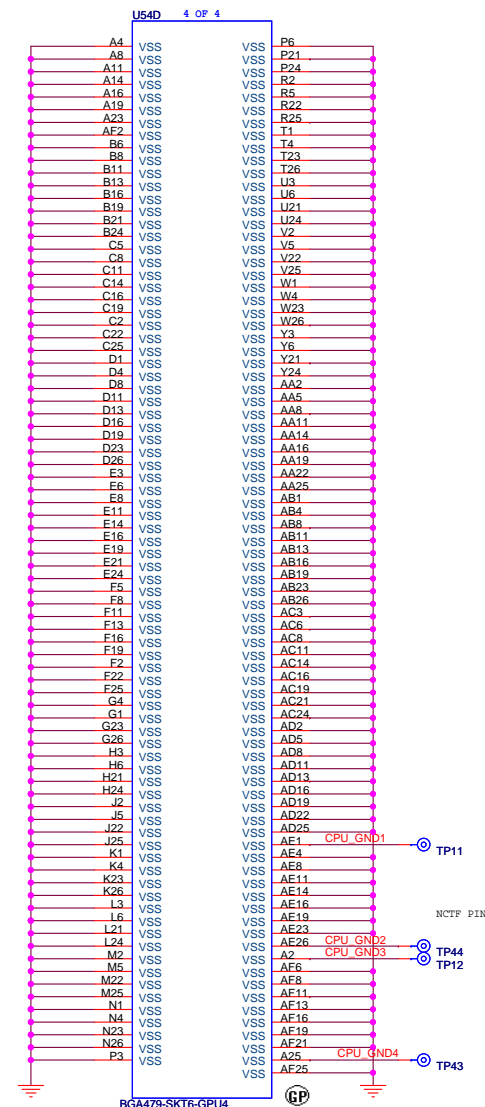
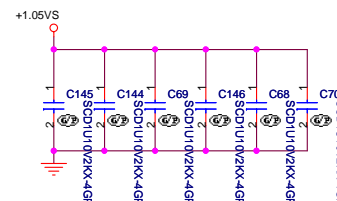
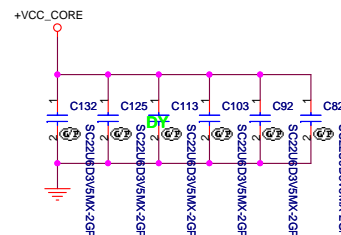
Please these outside socket
cavity on L8(North side Secondary)




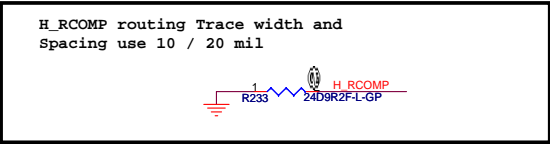
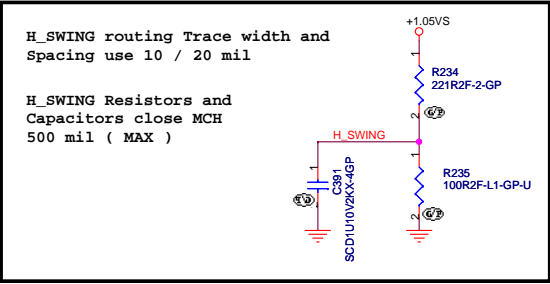
A circuit diagram showing a 100pF capacitor connected between the +VCC_CORE supply and ground. The capacitor is represented by two parallel blue lines, with the value '100pF' written next to it. The top terminal is connected to a red circle labeled '+VCC_CORE', and the bottom terminal is connected to a red ground symbol.

Please these outside socket
cavity on L8(South side Secondary)

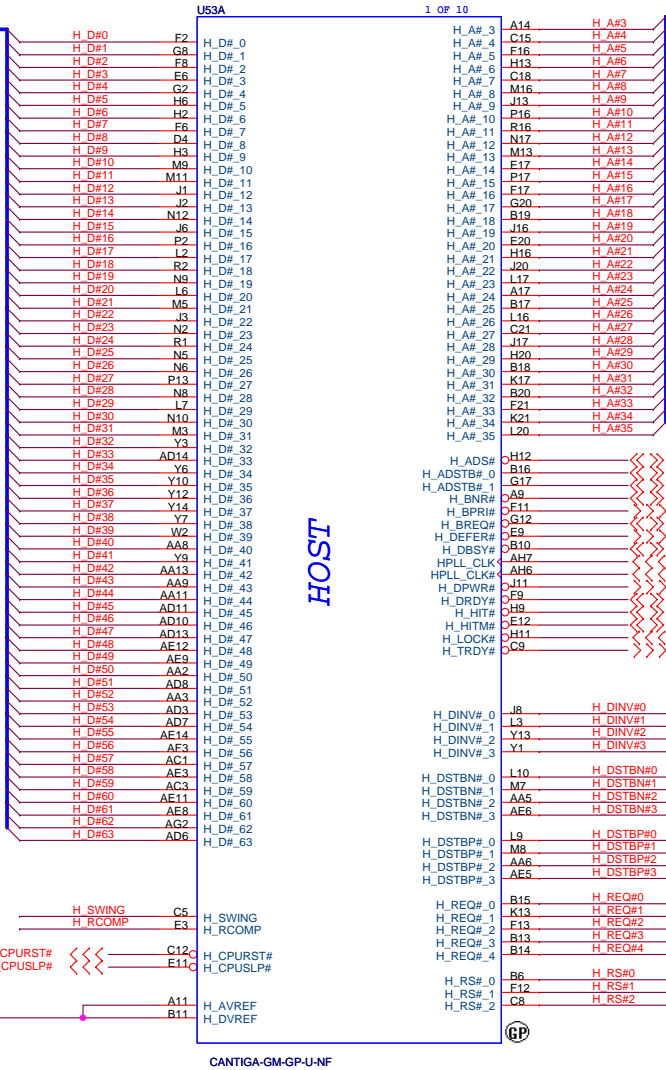
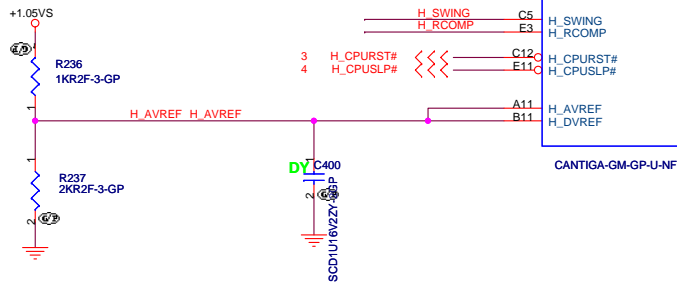
Please these inside socket
cavity on L8(South side Primary)

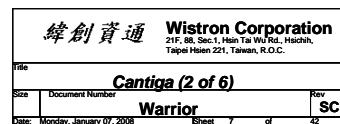


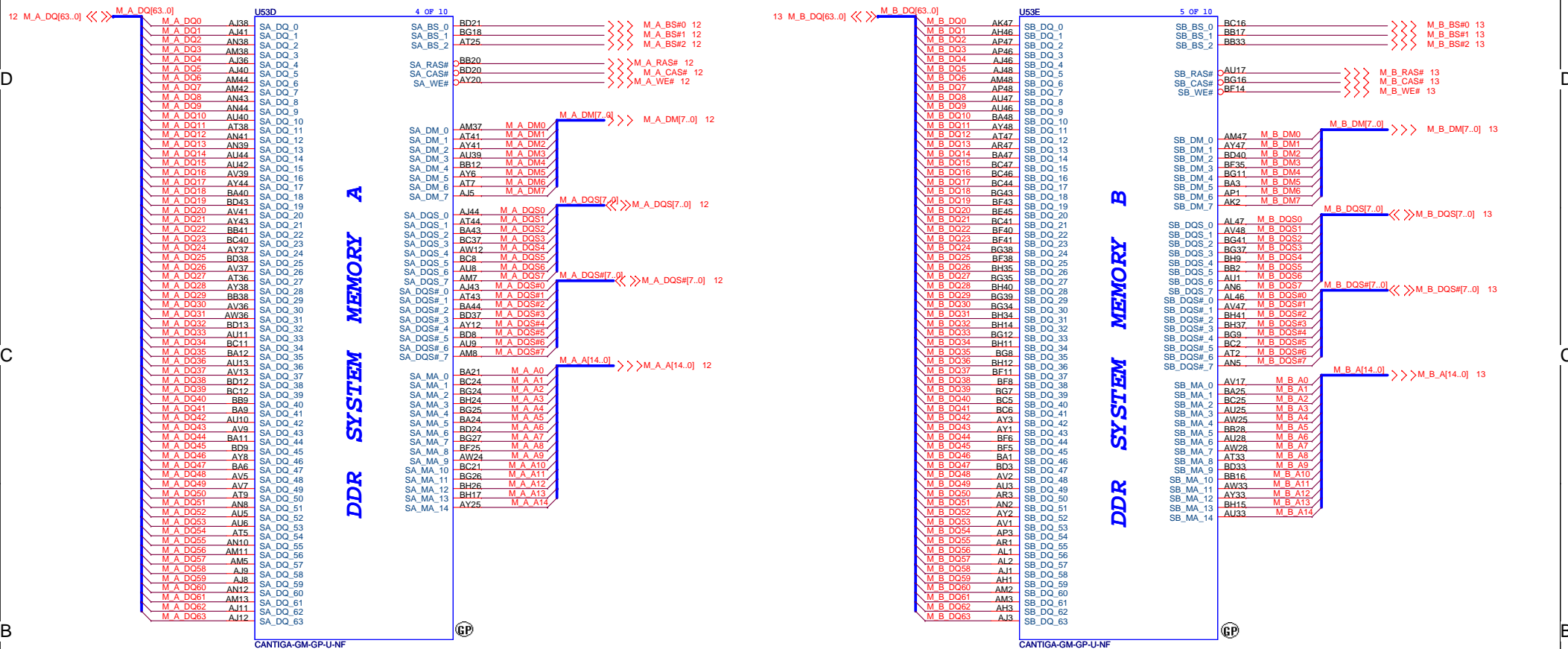
 <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div>	
Title	
<div>CPU (3 of 3)</div>	
Size	Document Number
<div>Warrior</div>	
Date: Monday, January 07, 2008	Sheet 5 of 42
<div>SC</div>	



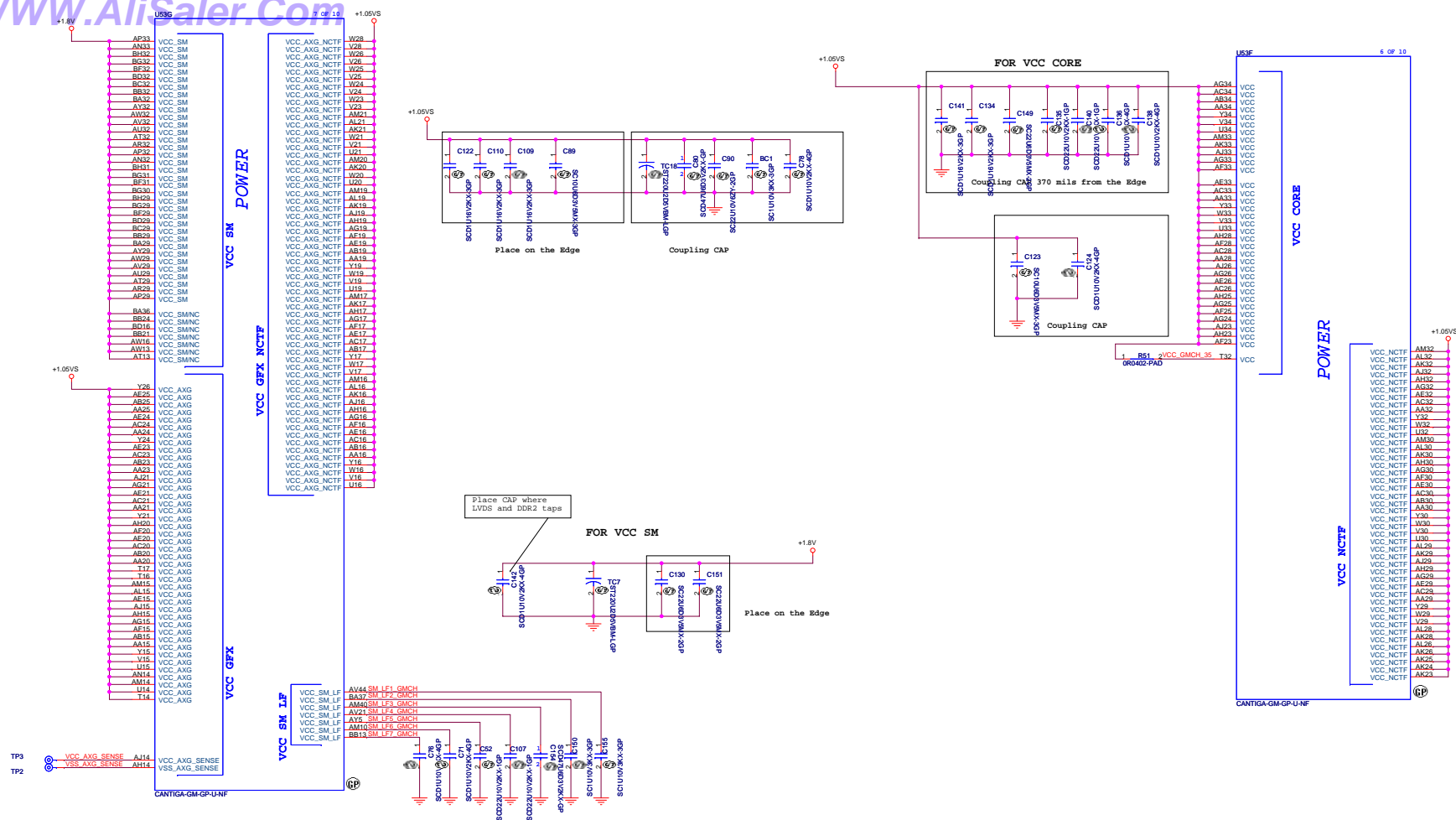
Place them near to the chip (< 0.5")

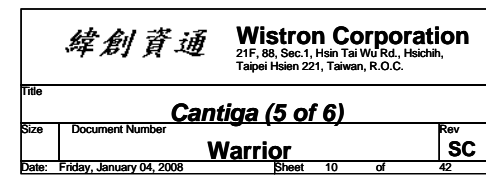


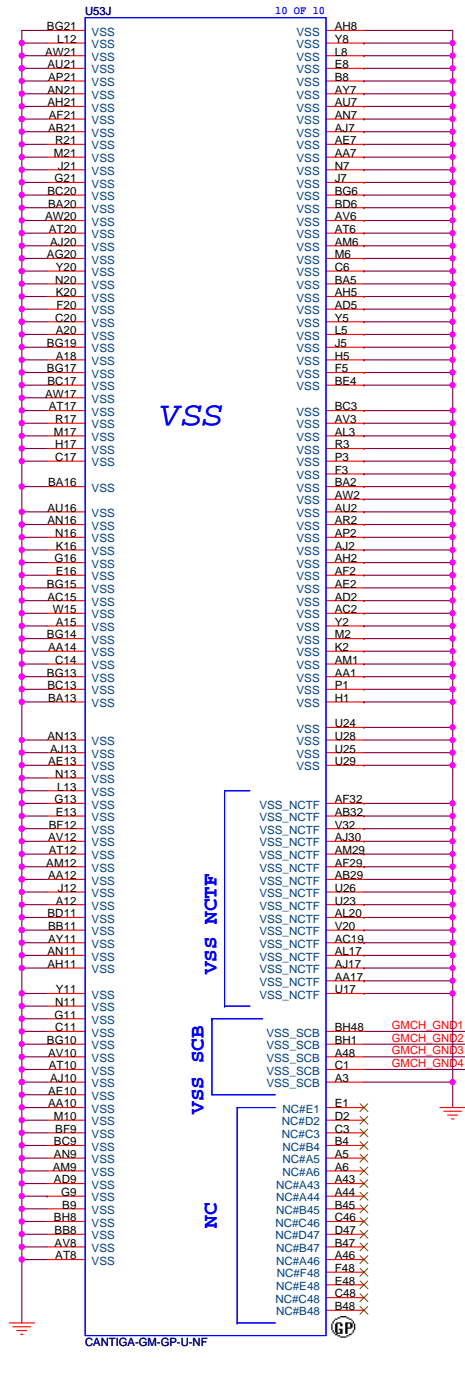
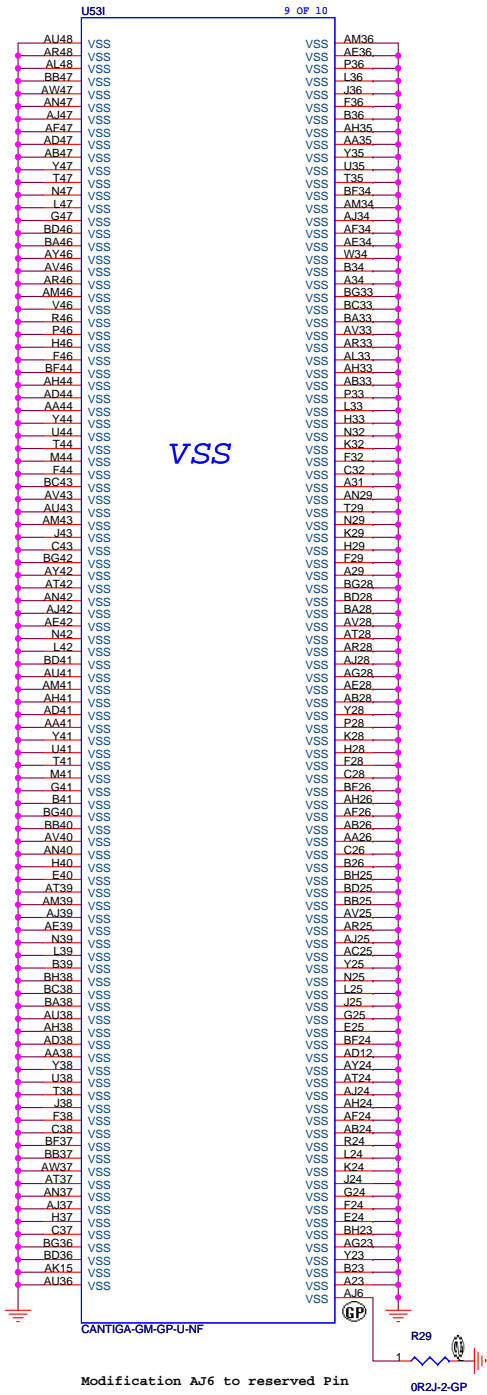




緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Cantiga (3 of 6)	
Size	Document Number
Date: Monday, January 07, 2008	Rev
Sheet 8 of 42	SC





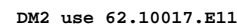


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga (6 of 6)

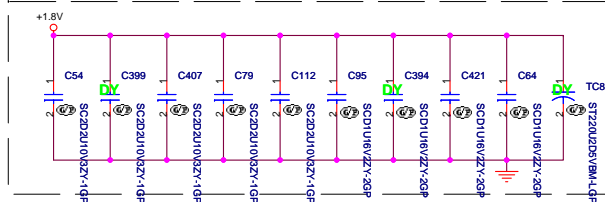
Size: Document Number Rev: SC

Date: Friday, January 04, 2008 Sheet 11 of 42

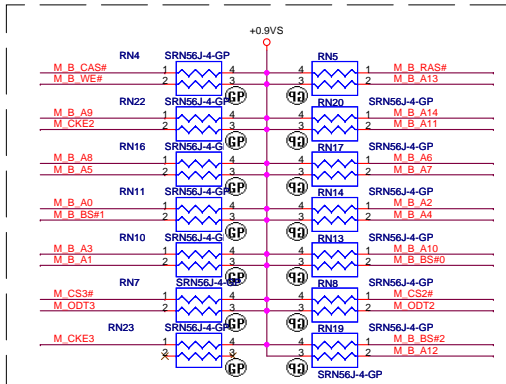
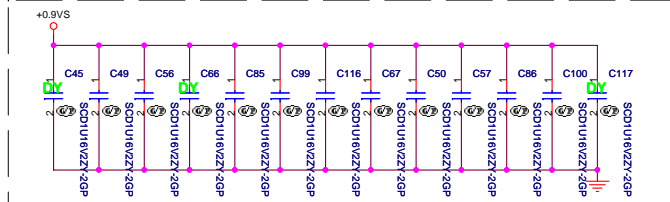


8 M_B_DQS#(7..0) <<>>
8 M_B_DQ(63..0) <<>>
8 M_B_DM(7..0) <<>>
8 M_B_DQS(7..0) <<>>
8 M_B_A[14..0] <<>>

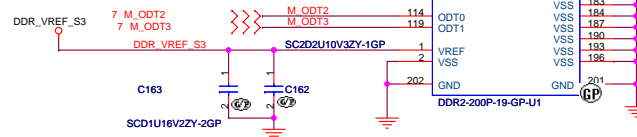
Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"



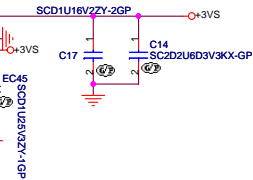
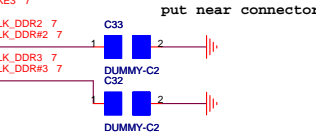
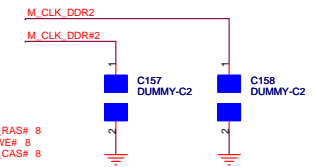
8 M_B_BS#2
8 M_B_BS#0
8 M_B_BS#1

>>>
>>>

M_B_A0	102	A0	/RAS	108	M_B_RAS# 8
M_B_A1	101	A1	/WE	108	M_B_WE# 8
M_B_A2	100	A2	/CAS	113	M_B_CAS# 8
M_B_A3	99	A3	/CS0	110	M_CS2# 7
M_B_A4	98	A4	/CS1	115	M_CS3# 7
M_B_A5	97	A5			
M_B_A6	96	A6			
M_B_A7	95	A7			
M_B_A8	94	A8			
M_B_A9	93	A9			
M_B_A10	92	A10			
M_B_A11	91	A11			
M_B_A12	90	A12			
M_B_A13	89	A13			
M_B_A14	88	A14			
M_B_BS#2	85	A15			
M_B_BS#0	107	BA0			
M_B_BS#1	106	BA1			
M_B_DQ0	5	DQ0			
M_B_DQ1	7	DQ1			
M_B_DQ2	17	DQ2			
M_B_DQ3	19	DQ3			
M_B_DQ4	6	DQ4			
M_B_DQ5	14	DQ5			
M_B_DQ6	16	DQ6			
M_B_DQ7	23	DQ7			
M_B_DQ8	25	DQ8			
M_B_DQ9	35	DQ9			
M_B_DQ10	37	DQ10			
M_B_DQ11	47	DQ11			
M_B_DQ12	22	DQ12			
M_B_DQ13	22	DQ13			
M_B_DQ14	38	DQ14			
M_B_DQ15	38	DQ15			
M_B_DQ16	43	DQ16			
M_B_DQ17	45	DQ17			
M_B_DQ18	55	DQ18			
M_B_DQ19	57	DQ19			
M_B_DQ20	44	DQ20			
M_B_DQ21	46	DQ21			
M_B_DQ22	56	DQ22			
M_B_DQ23	58	DQ23			
M_B_DQ24	61	DQ24			
M_B_DQ25	63	DQ25			
M_B_DQ26	73	DQ26			
M_B_DQ27	75	DQ27			
M_B_DQ28	62	DQ28			
M_B_DQ29	64	DQ29			
M_B_DQ30	74	DQ30			
M_B_DQ31	76	DQ31			
M_B_DQ32	123	DQ32			
M_B_DQ33	125	DQ33			
M_B_DQ34	135	DQ34			
M_B_DQ35	137	DQ35			
M_B_DQ36	124	DQ36			
M_B_DQ37	126	DQ37			
M_B_DQ38	134	DQ38			
M_B_DQ39	136	DQ39			
M_B_DQ40	141	DQ40			
M_B_DQ41	143	DQ41			
M_B_DQ42	151	DQ42			
M_B_DQ43	153	DQ43			
M_B_DQ44	140	DQ44			
M_B_DQ45	142	DQ45			
M_B_DQ46	152	DQ46			
M_B_DQ47	154	DQ47			
M_B_DQ48	157	DQ48			
M_B_DQ49	159	DQ49			
M_B_DQ50	173	DQ50			
M_B_DQ51	175	DQ51			
M_B_DQ52	158	DQ52			
M_B_DQ53	160	DQ53			
M_B_DQ54	174	DQ54			
M_B_DQ55	176	DQ55			
M_B_DQ56	179	DQ56			
M_B_DQ57	181	DQ57			
M_B_DQ58	189	DQ58			
M_B_DQ59	191	DQ59			
M_B_DQ60	180	DQ60			
M_B_DQ61	182	DQ61			
M_B_DQ62	192	DQ62			
M_B_DQ63	194	DQ63			
M_B_DQS#0	11	DQS0			
M_B_DQS#1	29	DQS1			
M_B_DQS#2	49	DQS2			
M_B_DQS#3	68	DQS3			
M_B_DQS#4	129	DQS4			
M_B_DQS#5	146	DQS5			
M_B_DQS#6	167	DQS6			
M_B_DQS#7	188	DQS7			
M_B_DQSO	31	DQSO			
M_B_DQS1	51	DQS1			
M_B_DQS2	70	DQS2			
M_B_DQS3	131	DQS3			
M_B_DQS4	148	DQS4			
M_B_DQS5	169	DQS5			
M_B_DQS6	188	DQS6			
M_B_DQS7	114	DQS7			
M_ODT2	114	ODT0			
M_ODT3	119	ODT1			
M_ODT2	114	ODT0			
M_ODT3	119	ODT1			

DM1 use 62.10017.B51

1206 SI

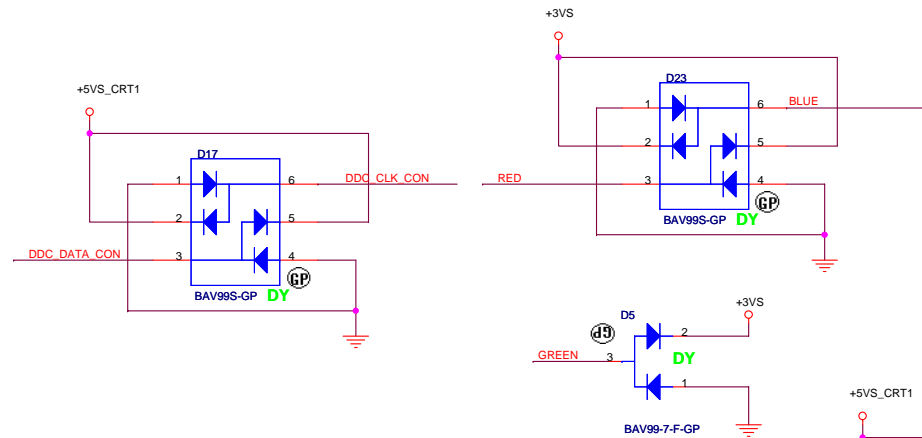


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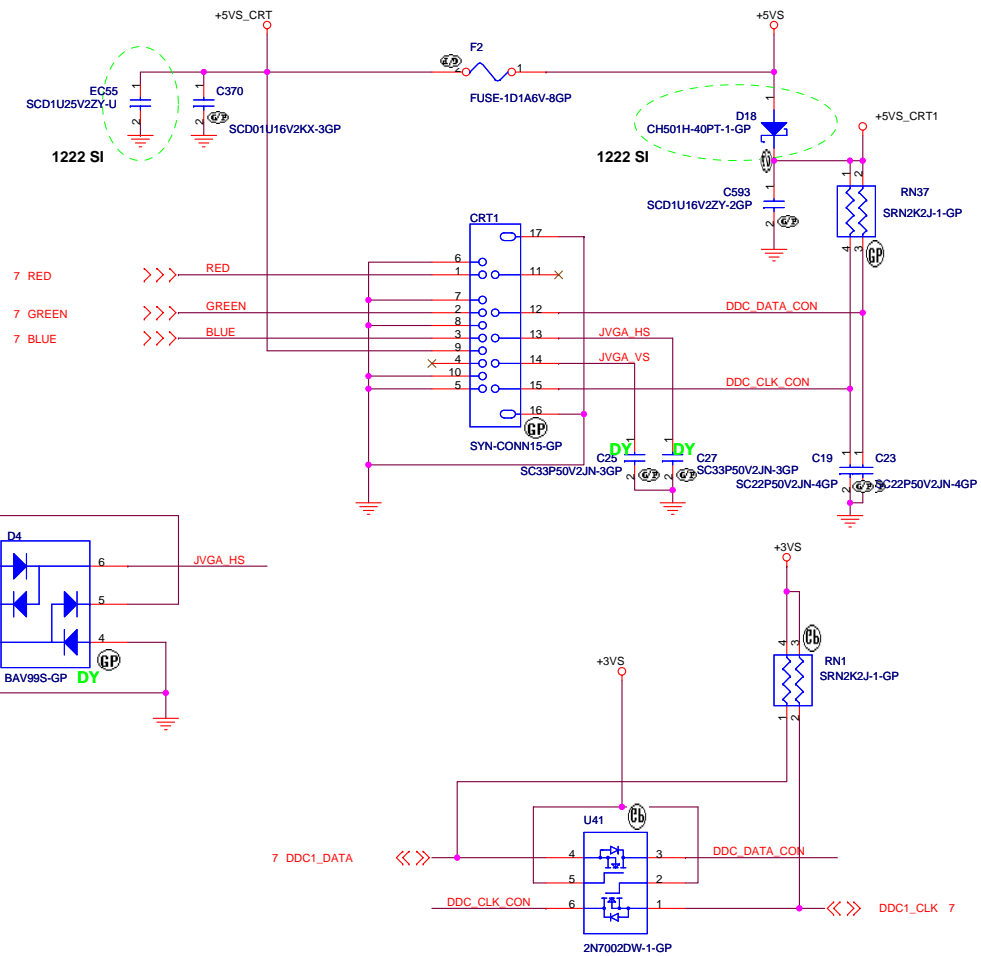
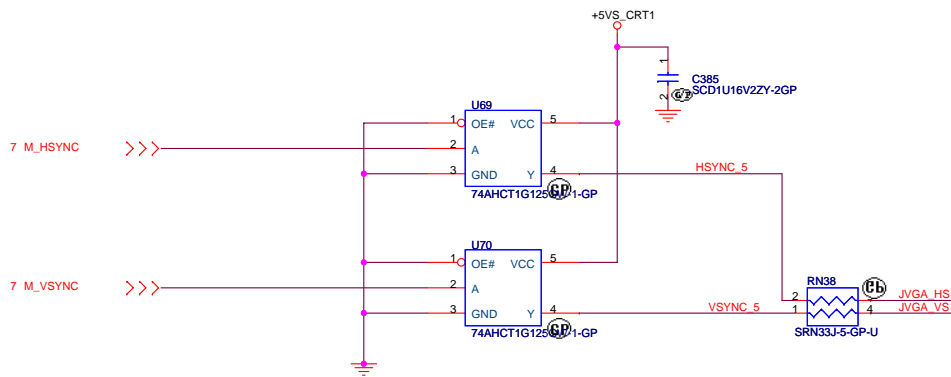
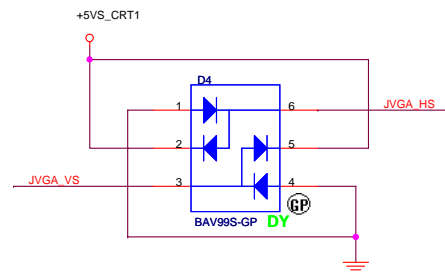
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		DDR2-SODIMM SLOT2	
Size	Document Number	Warrior	Rev
Custom			SC
Date:	Monday, January 07, 2008	Sheet 13 of 42	

CRT I/F & CONNECTOR



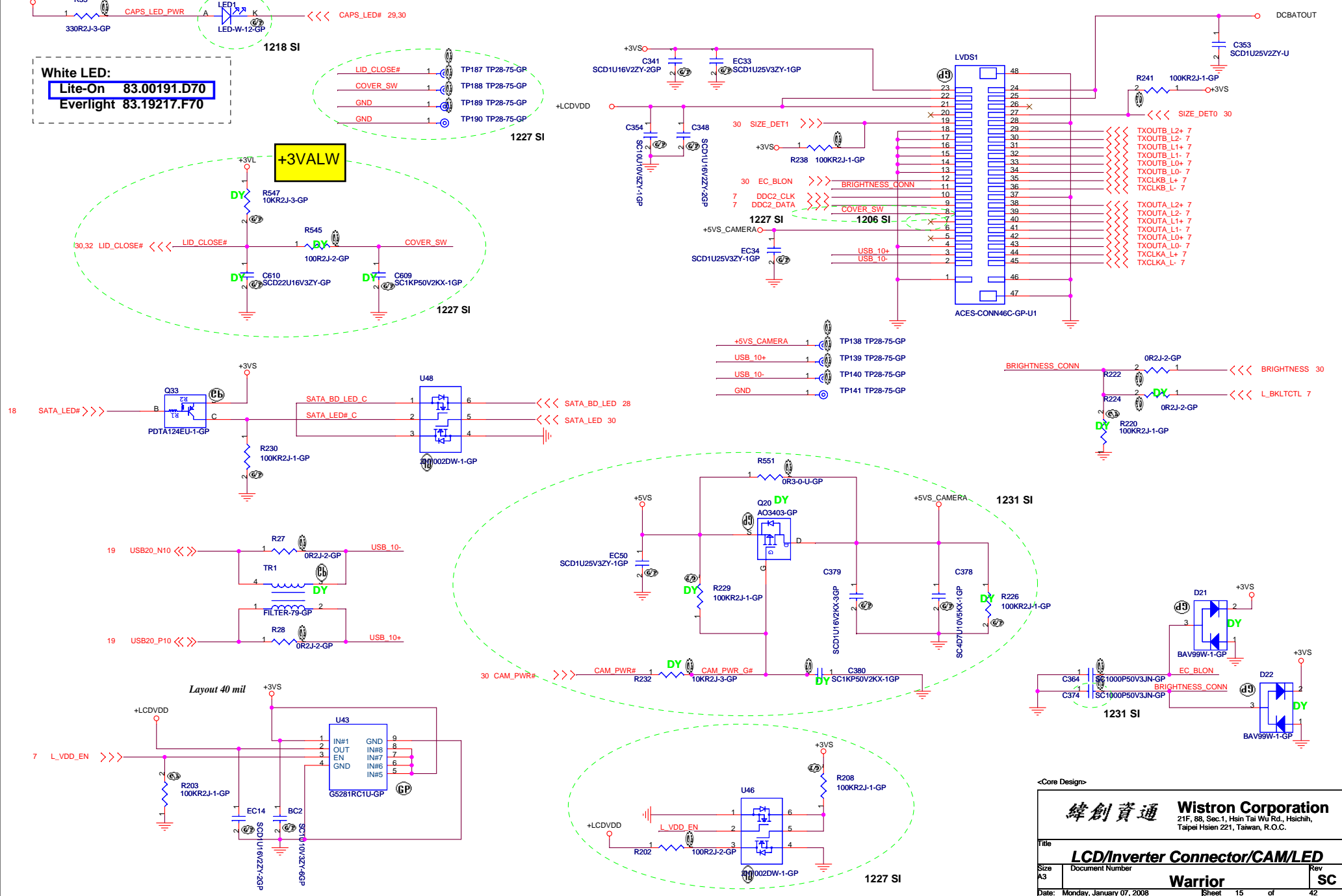
Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

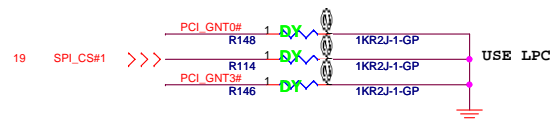
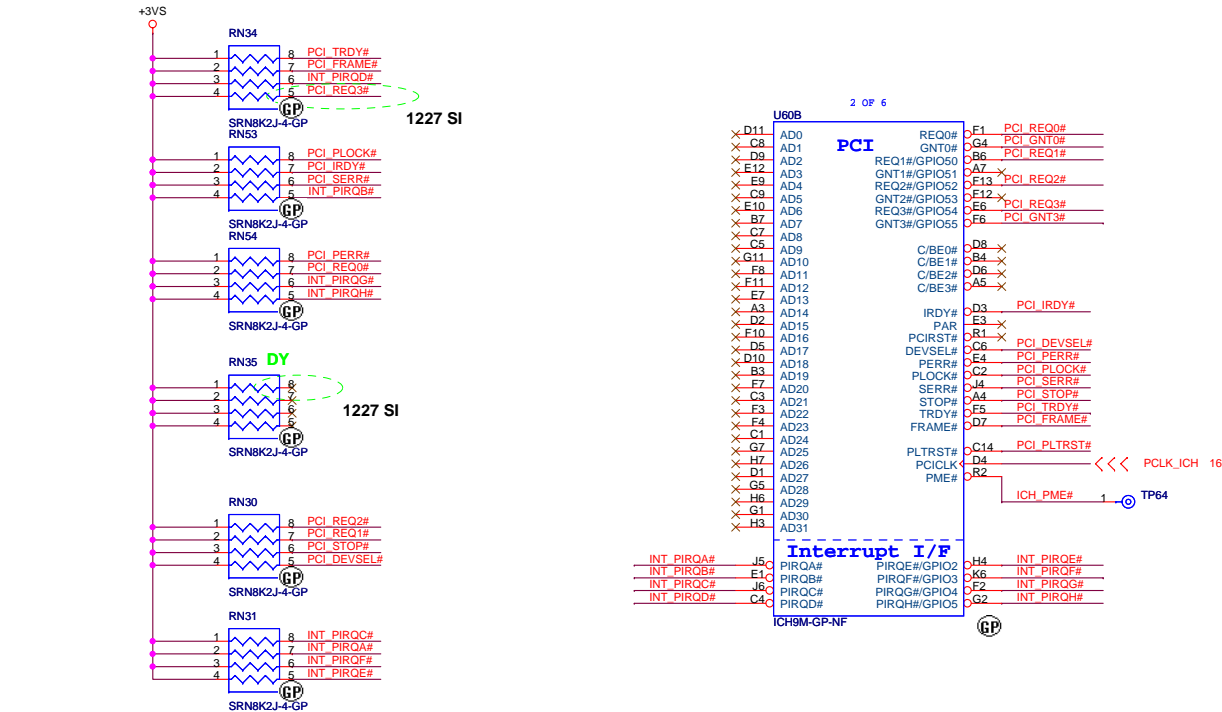


5V @ ext. CRT side

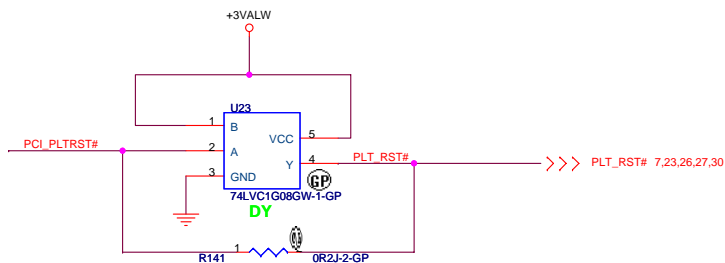
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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT Connector	
Size A3	Document Number Warrior
Date: Monday, January 07, 2008	Sheet 14 of 42
Rev	SC

LCD / INVERTER INTERFACE / CAMERA





BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ICH9-M (1 of 5)			
Size	Document Number		Rev
	Warrior		SC
Date: Monday, January 07, 2008	Sheet 17	of 42	

82.30001.731 EPSON MC-306
32.768Khz 6pf 10ppm

GLAN_COMP place within 500 mil of ICH9M

7.28 HDA_RST#_CODEC
7.28 HDA_BITCLK_CODEC
7.28 HDA_SYNC_CODEC
7.28 HDA_SDOUT_CODEC

HDD

ODD

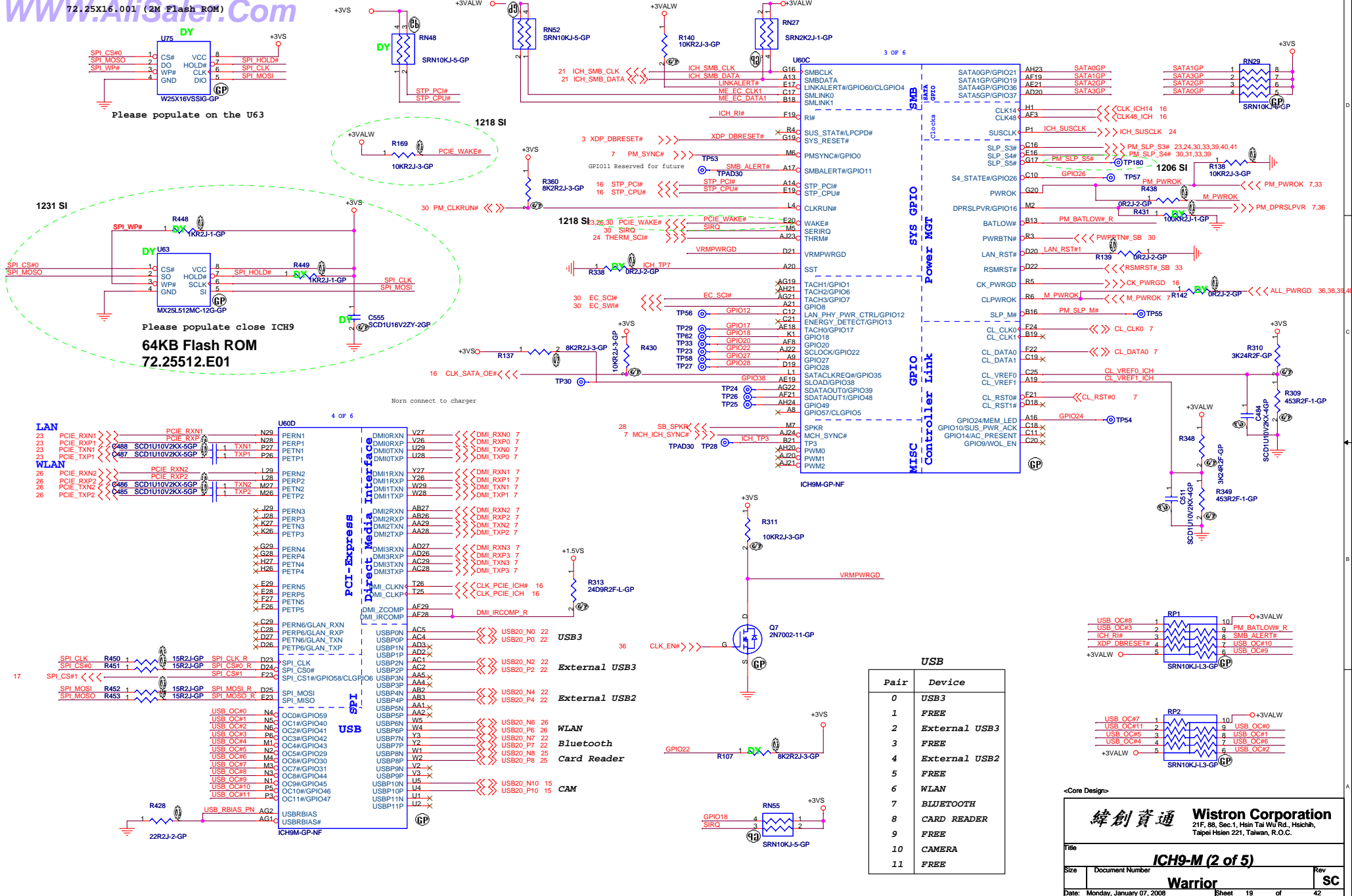
ICH9M-GP-NF

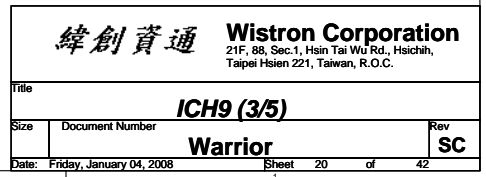
Integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

<Core Design>

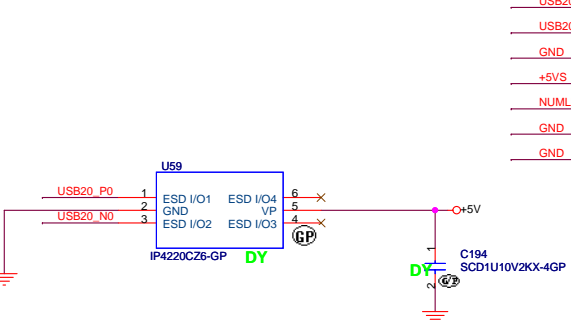
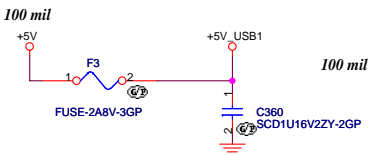
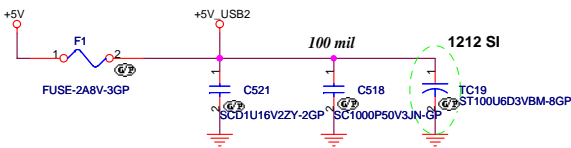
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File			
ICH9-M (2 of 5)			
Size	Document Number	Rev	SC
Warrior			
Date: Monday, January 07, 2008	Sheet 18	of 42	

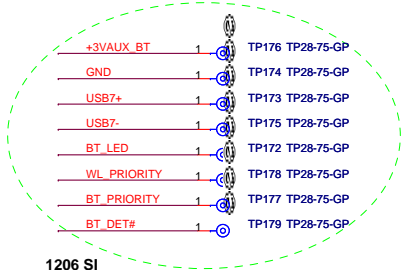
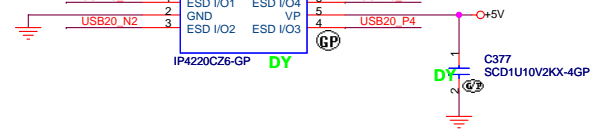
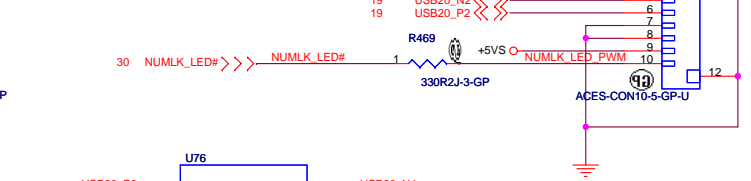
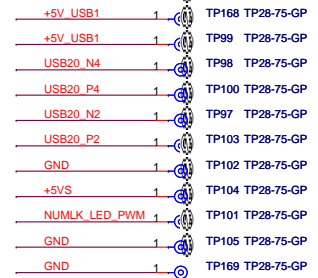
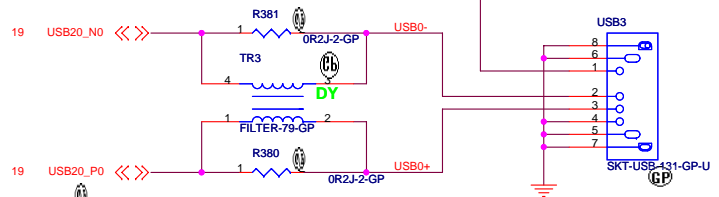
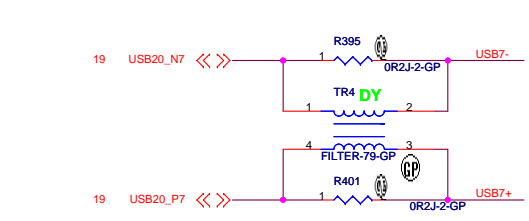
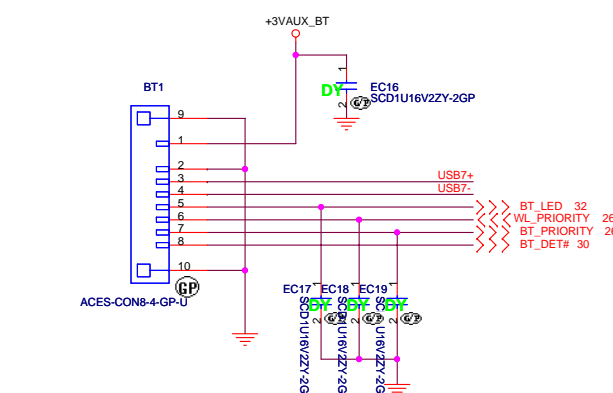




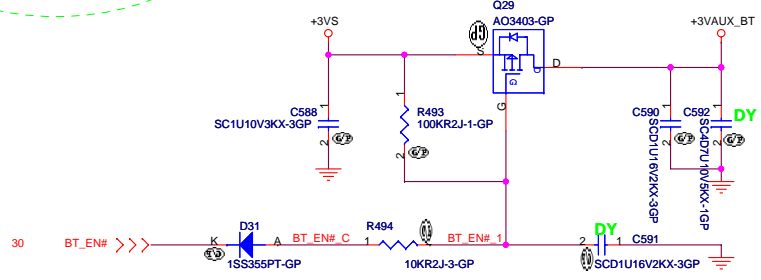
A



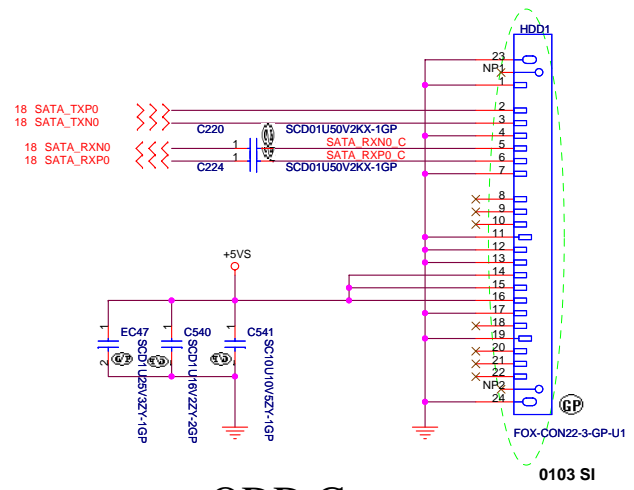
BLUETOOTH



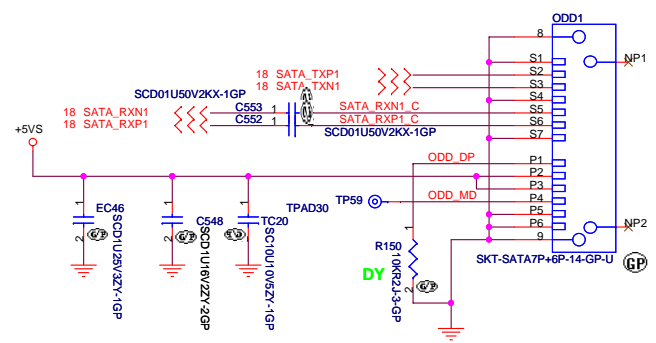
1206 SI



SATA HD Connector



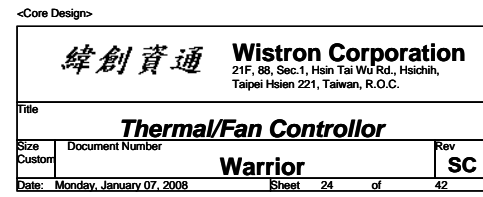
ODD Connector



<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD/CDROM/USB/BT			
Size A3	Document Number	Warrior	Rev SC
Date: Monday, January 07, 2008	Sheet 22	of 42	



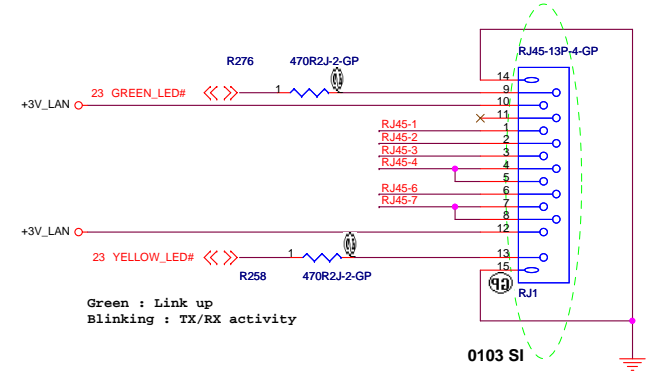
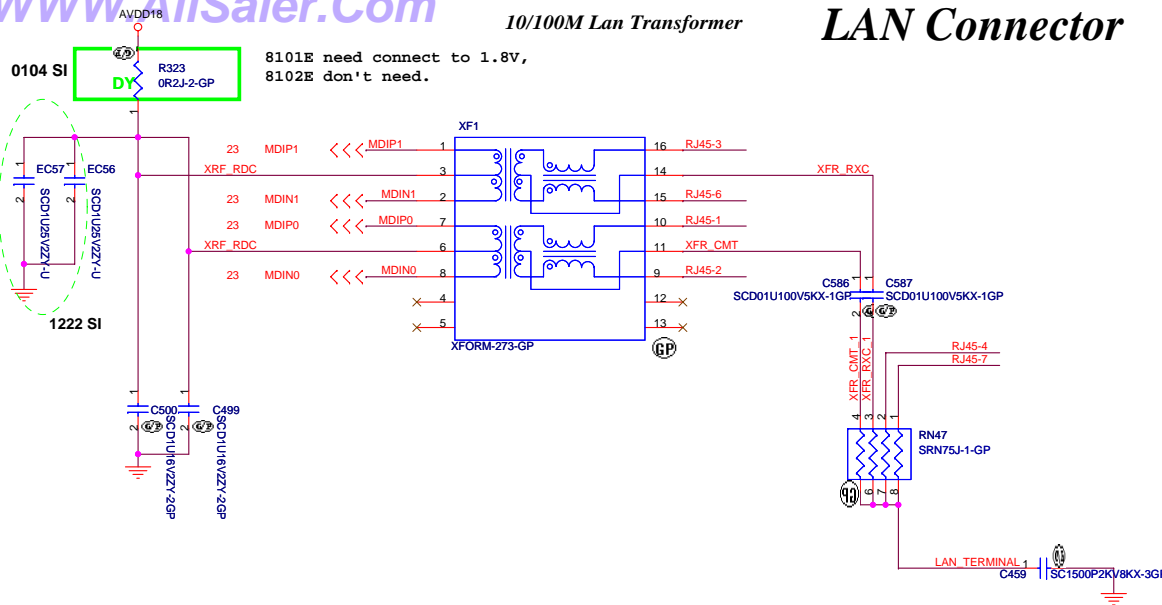




Title USB Card Reader Controller - RTS5158			
Size	Document Number Warrior		Rev S
Date	Monday, January 07, 2008	Sheet	26 of 42

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Green : Link up
Blinking : TX/RX activity

Remark:
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

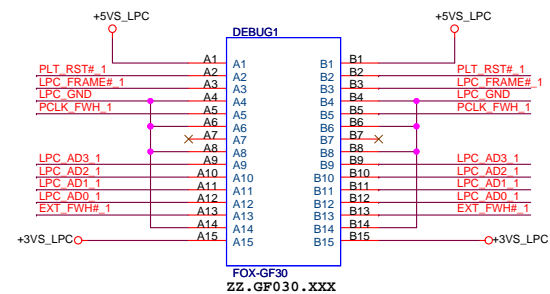
Golden Finger for Debug Board

TOP VIEW (A)

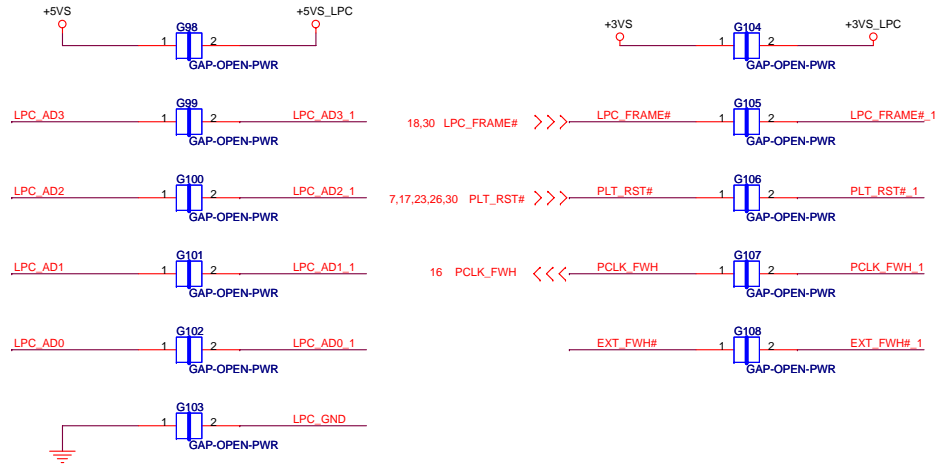
A15 (B1)
A14 (B2)
:
:
:
A2 (B14)
A1 (B15)

BOTTOM VIEW (B)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



Please put near board edge.



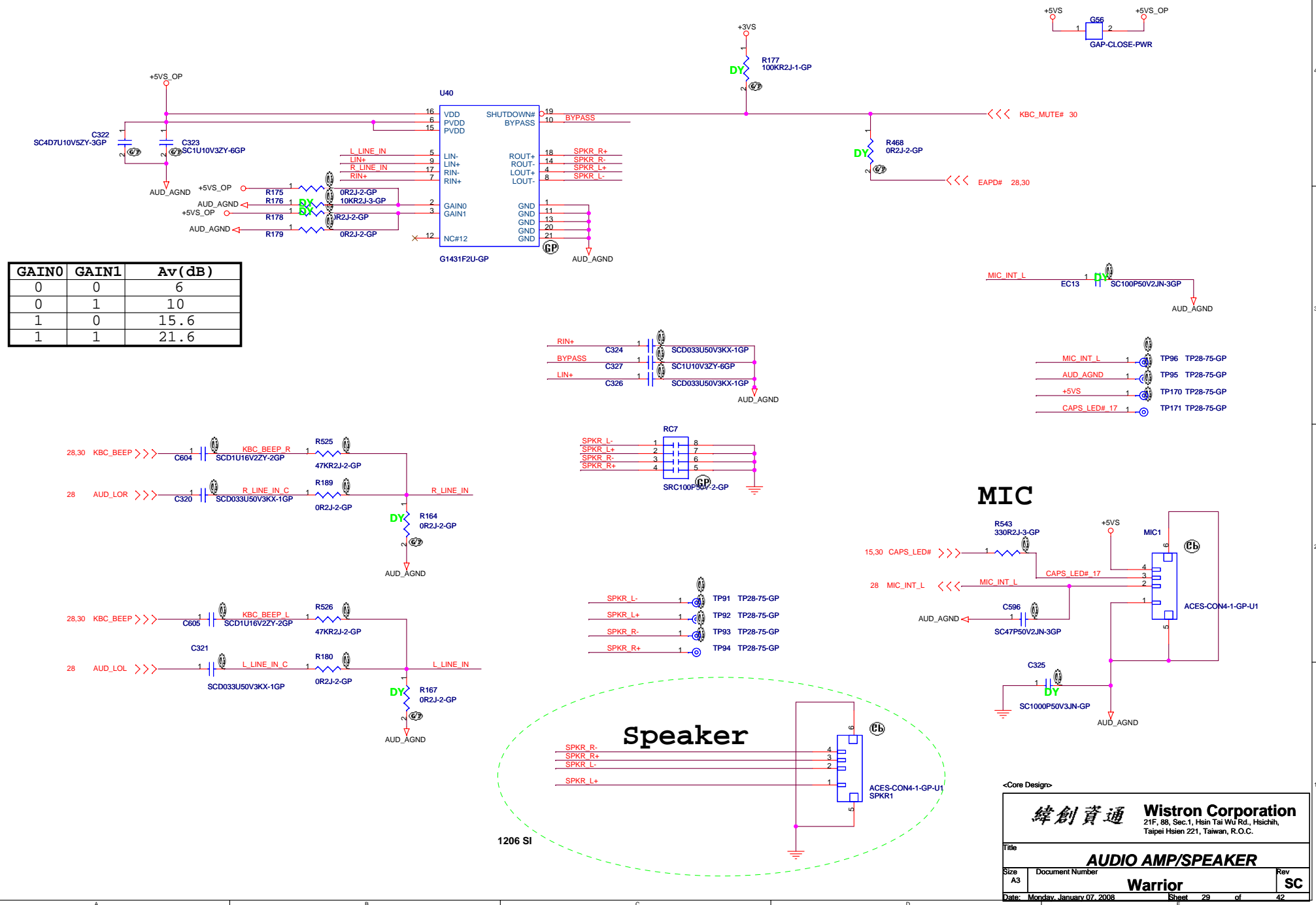
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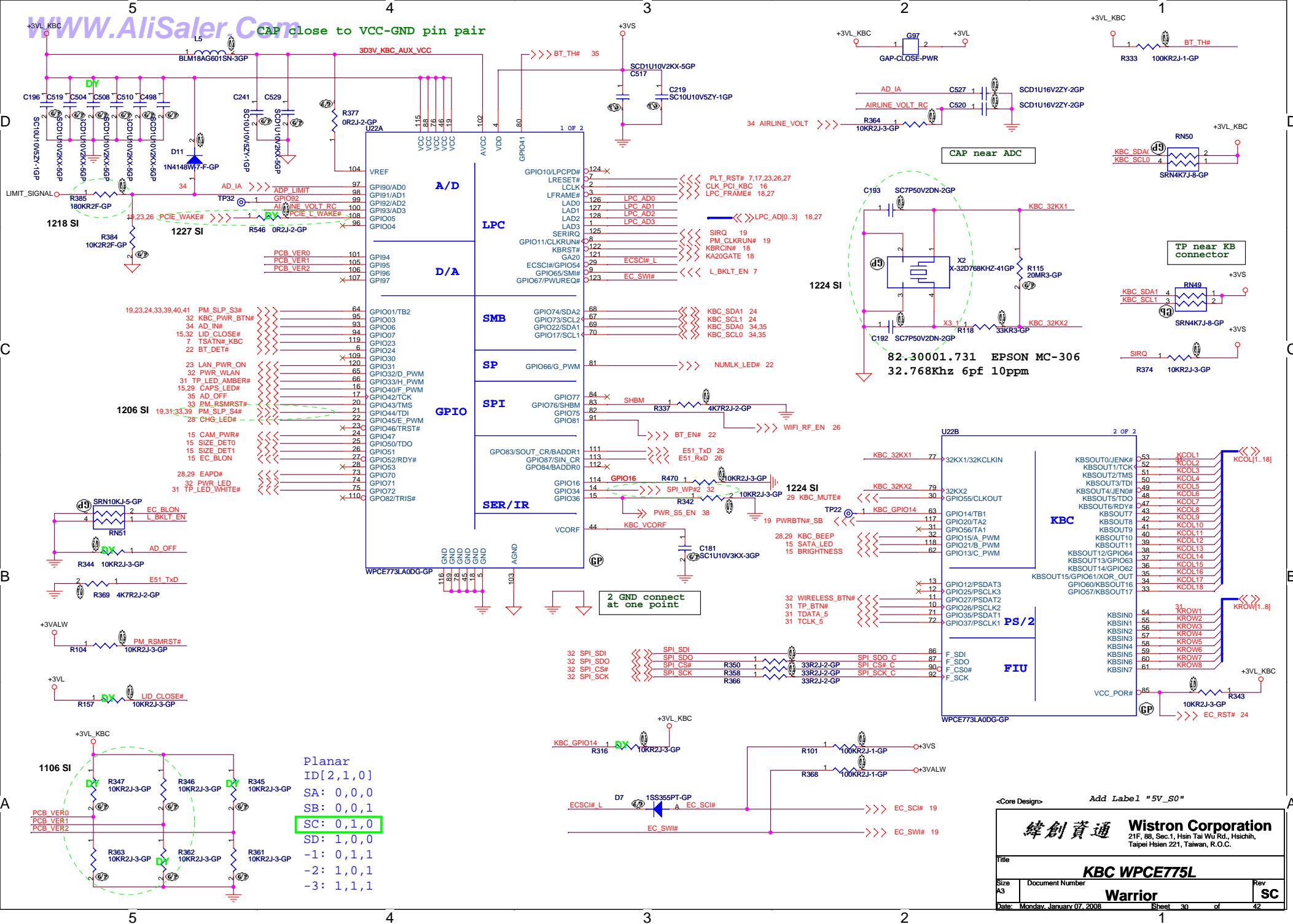
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN/Debug**

Size: A3 Document Number: **Warrior** Rev: **SC**

Date: Monday, January 07, 2008 Sheet 27 of 42

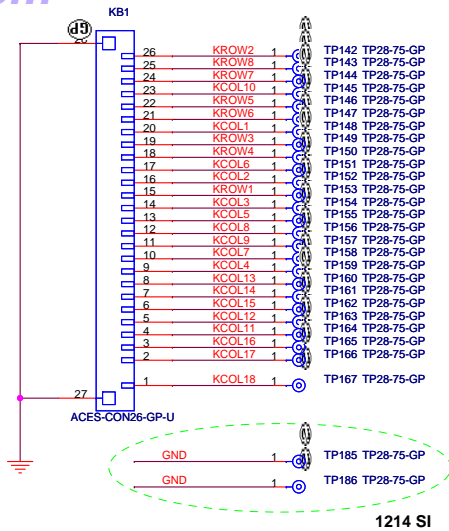
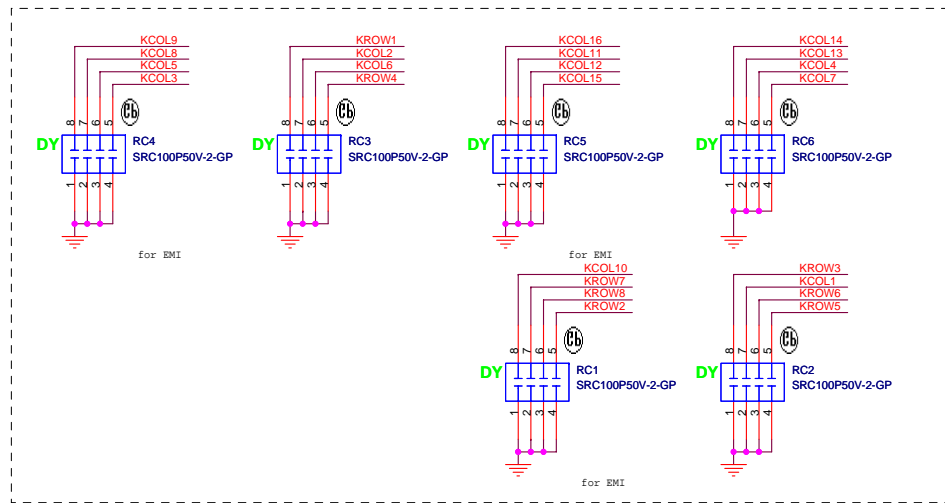
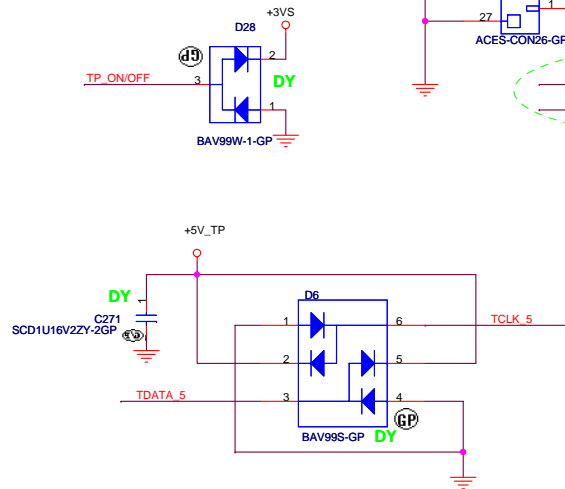




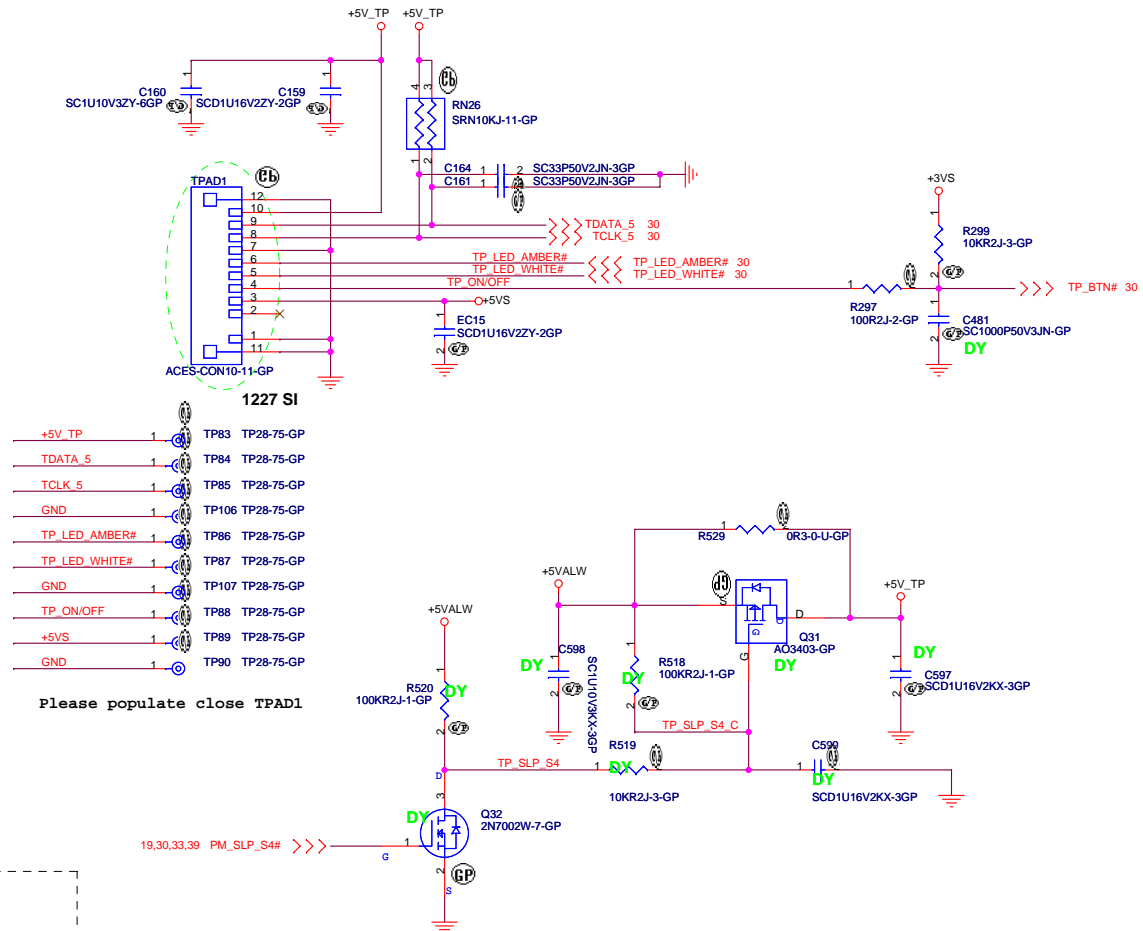
Internal KeyBoard Connector

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



TouchPad Connector

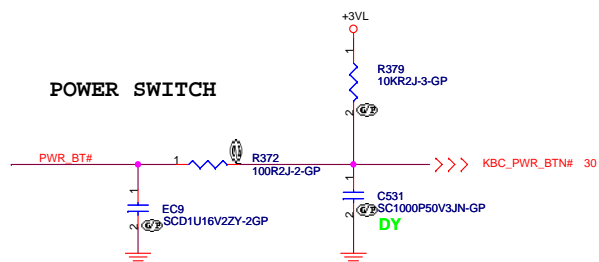
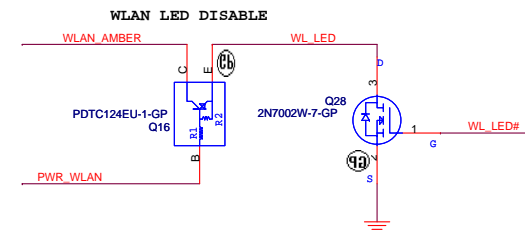
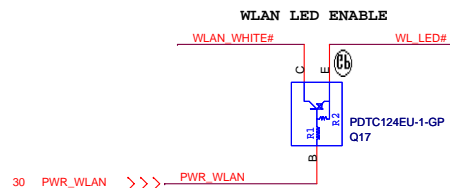
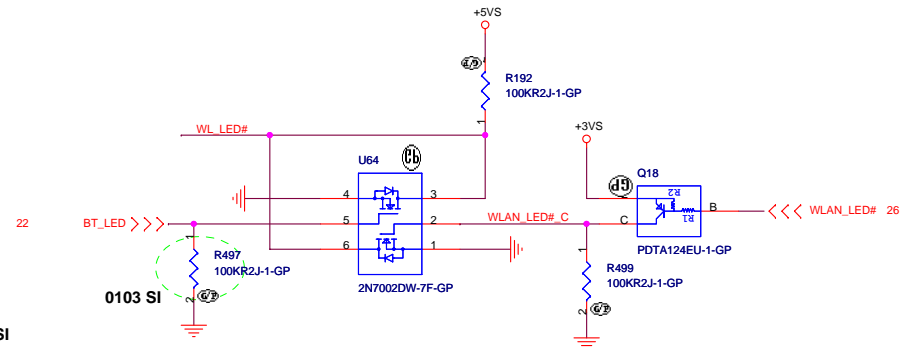
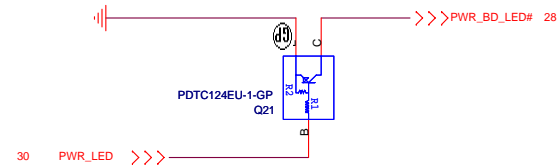


Please populate close TPAD1

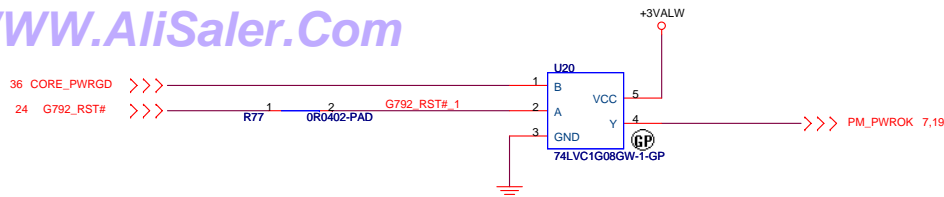
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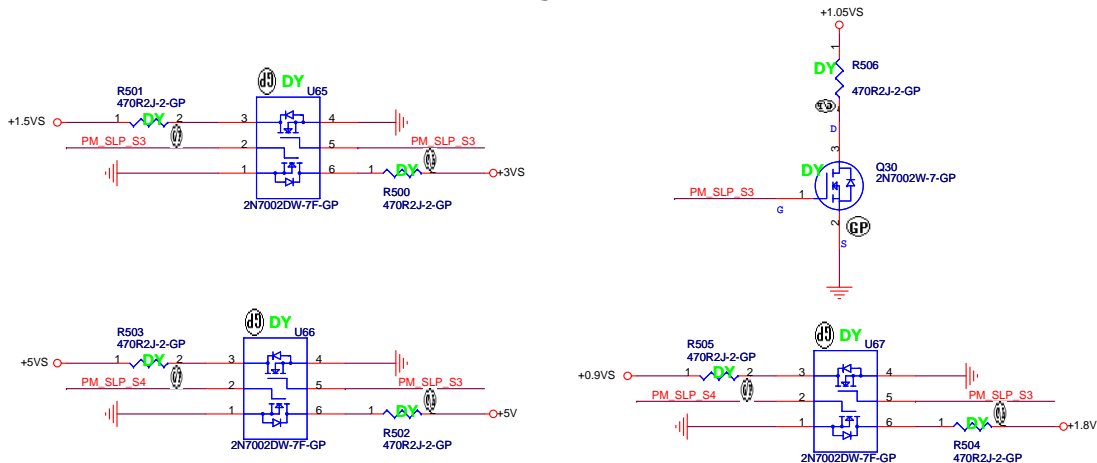
Title	KeyBoard-CONN		
Size A3	Document Number	Warrior	Rev SC
Date: Monday, January 07, 2008	Sheet	31	of 42



<Core Design>			
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Title			
<i>FWH and CONN.</i>			
Size A3	Document Number		Rev
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Discharge Circuit

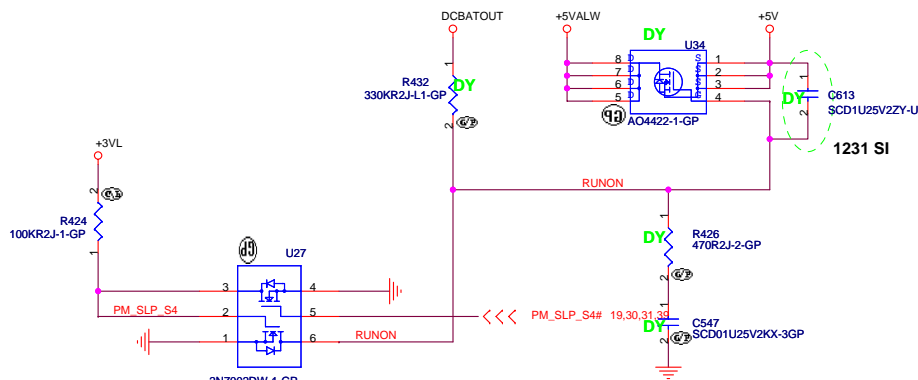
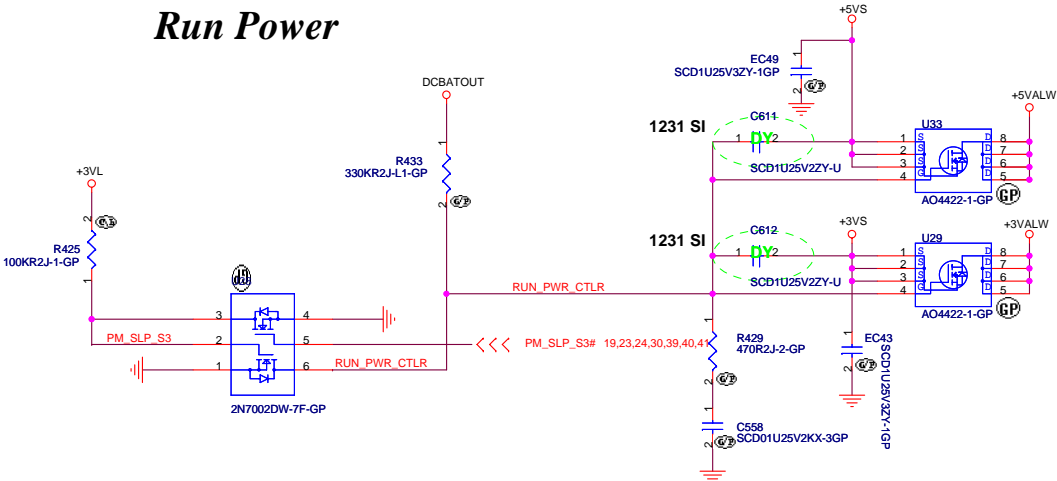


Populate close U34

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

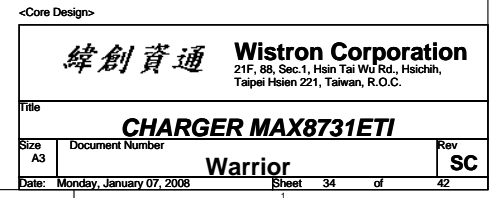
+5VALW to +5V Transfer

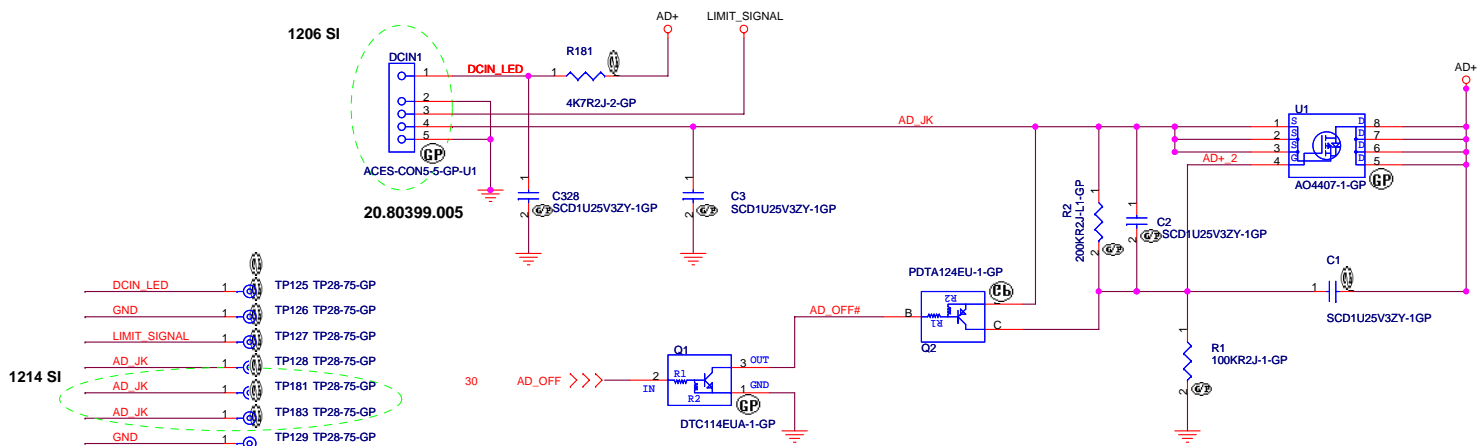
Run Power



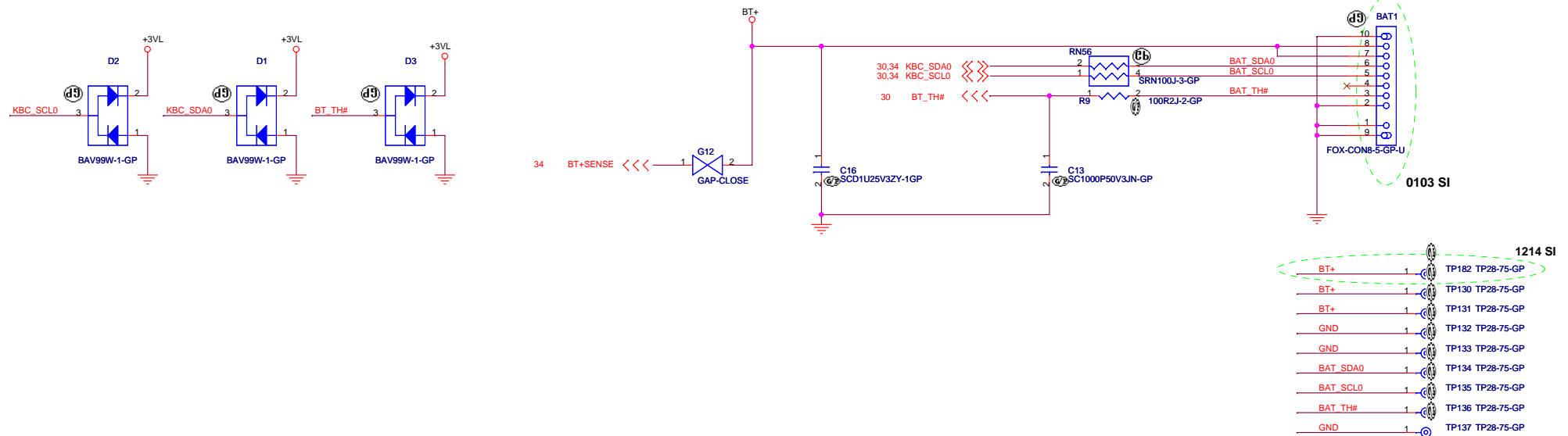
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Title	PWRPLANE	
Size A3	Document Number	Rev
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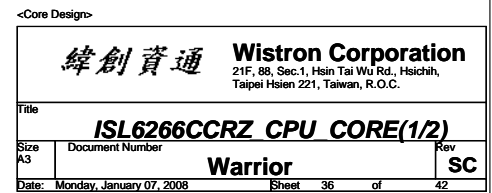


BATTERY CONNECTOR



<Core Design>

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Title	AD/BATT CONN
Size A3	Document Number
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Title

ISL6260CCRZ CPU CORE(2/2)

Size
A3

Document Number

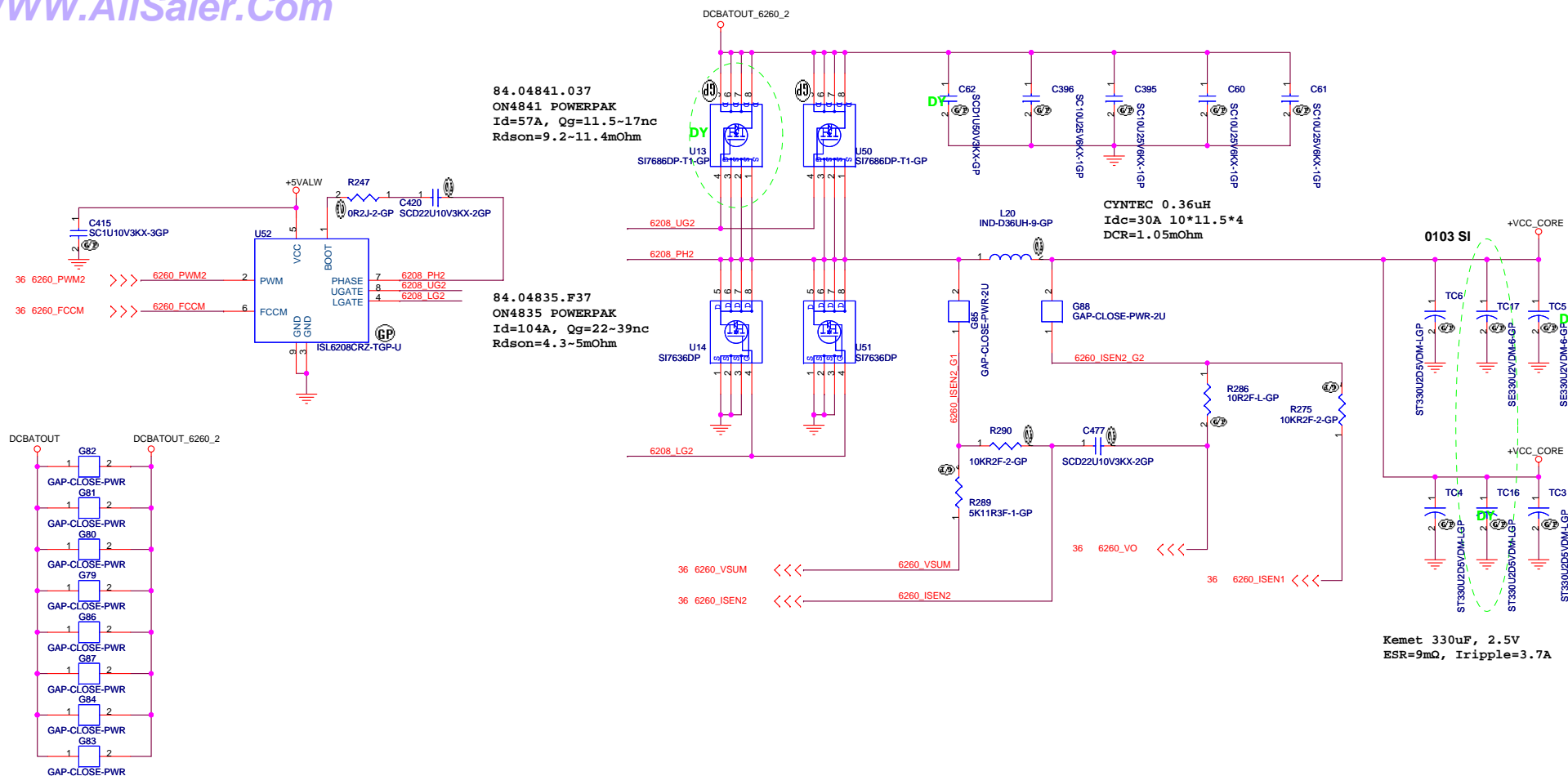
Warrior

Rev	S
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Date: Monday, January 07, 2008

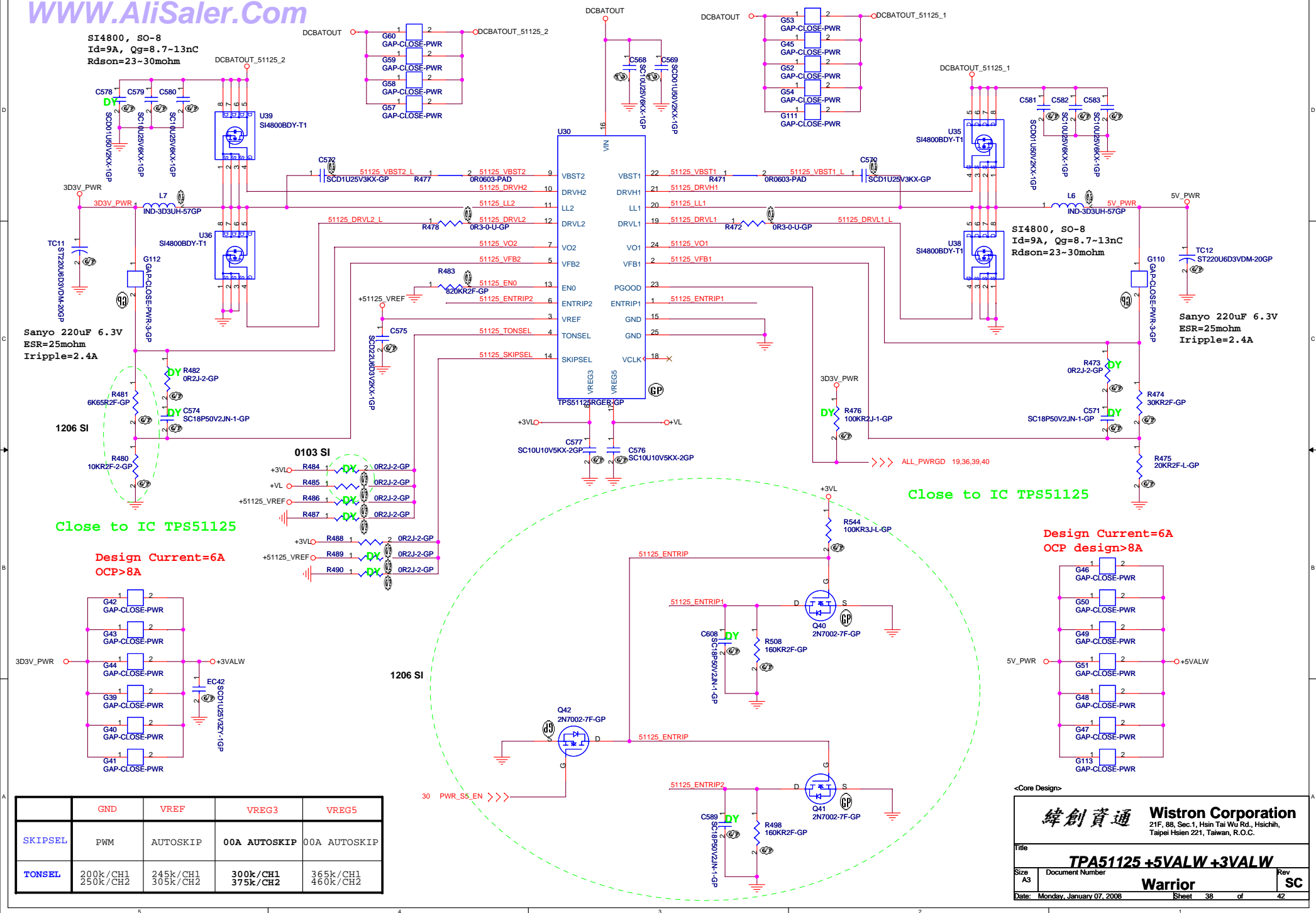
Sheet 3

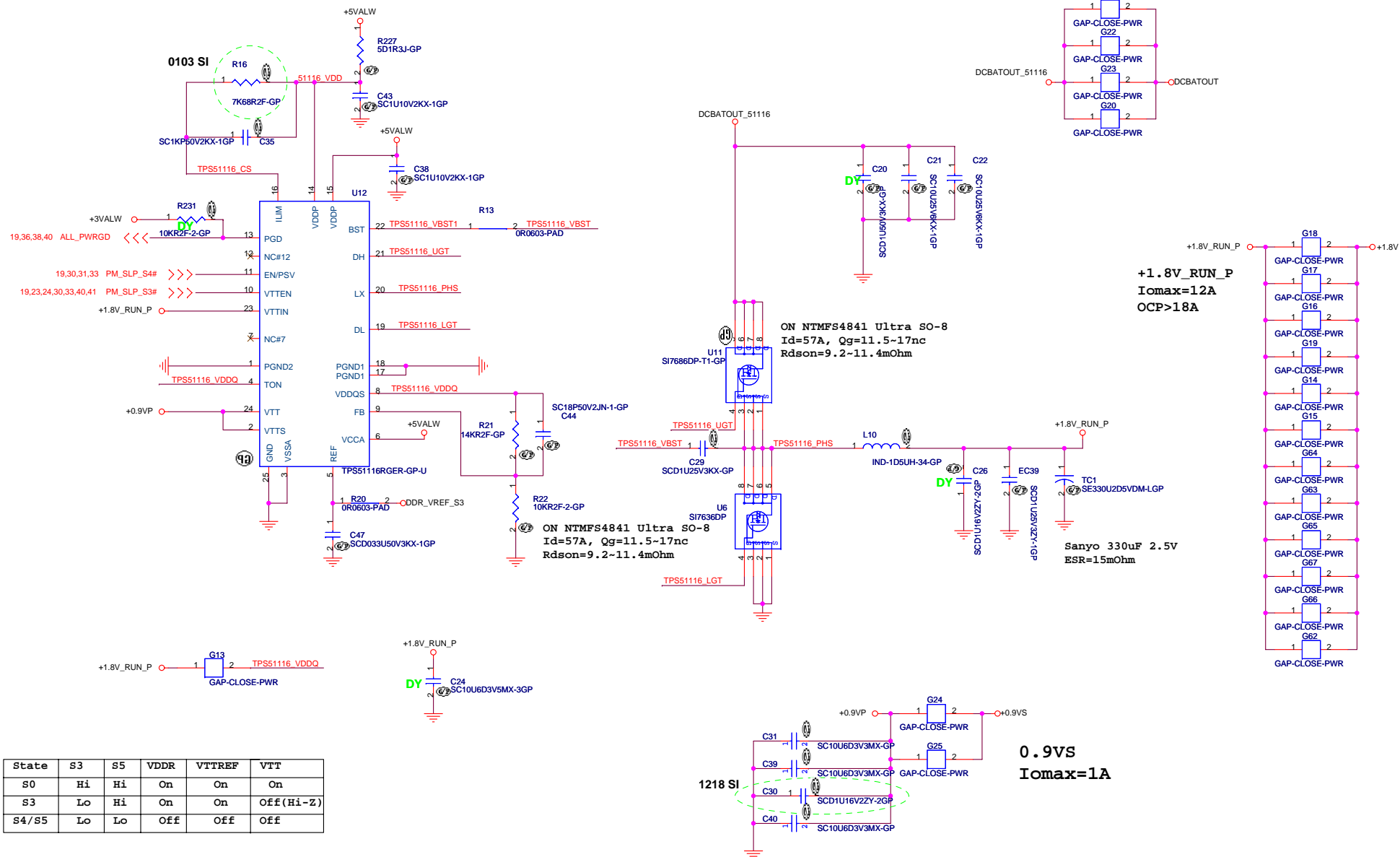
37 of 42

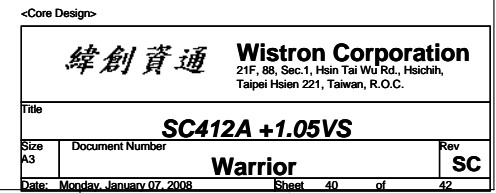


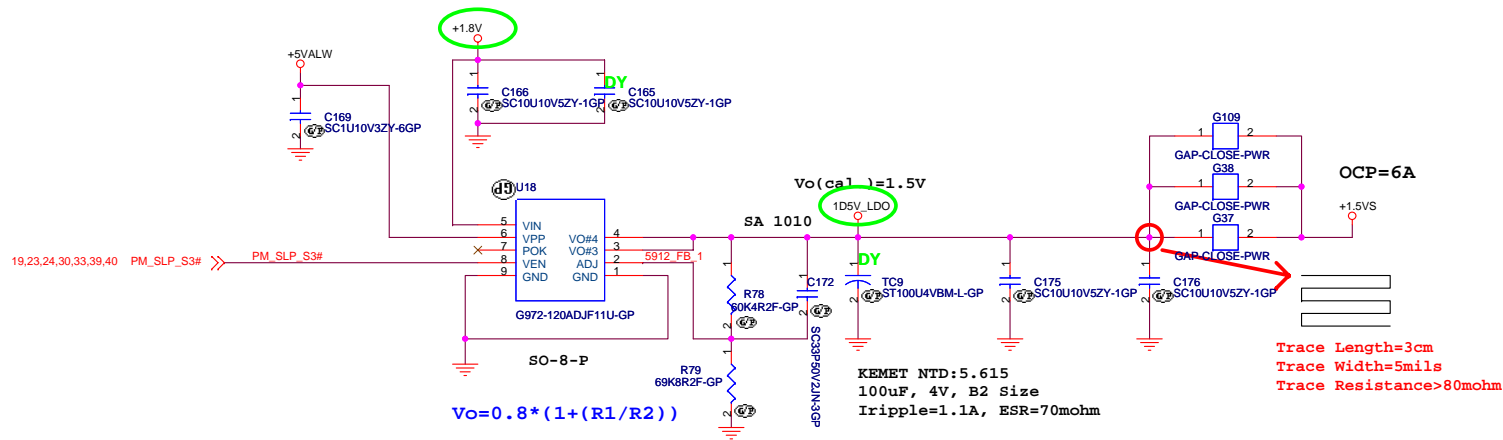
Kemet 330uF, 2.5V
ESR=9mΩ, Iripple=3.7A

SI4800, SO-8
Id=9A, Qg=8.7~13nC
Rdson=23~30mohm









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Title

GMT 1D5V LDO

Size
A3

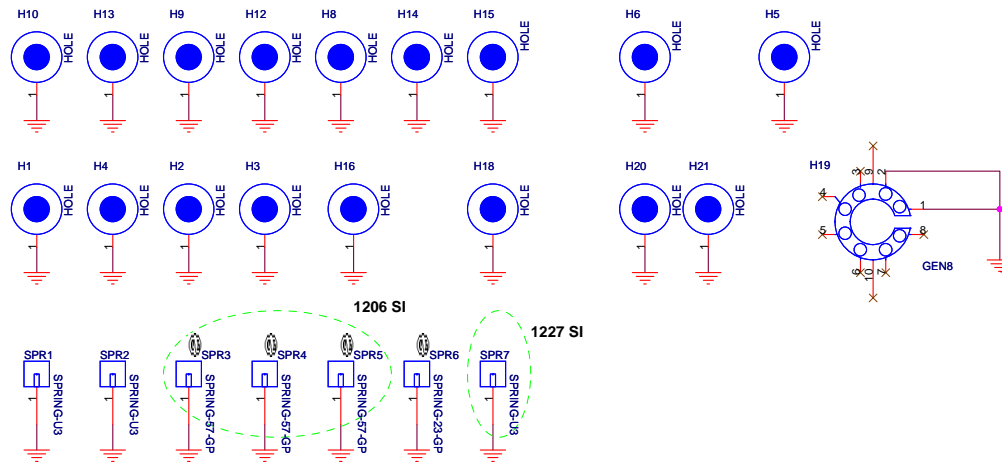
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SPR1-2: 34.40U07.001
 SPR3-5: 34.42T14.002
 SPR6 : 34.39S07.003
 SPR7 : 34.40U07.001

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Title	MISC
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