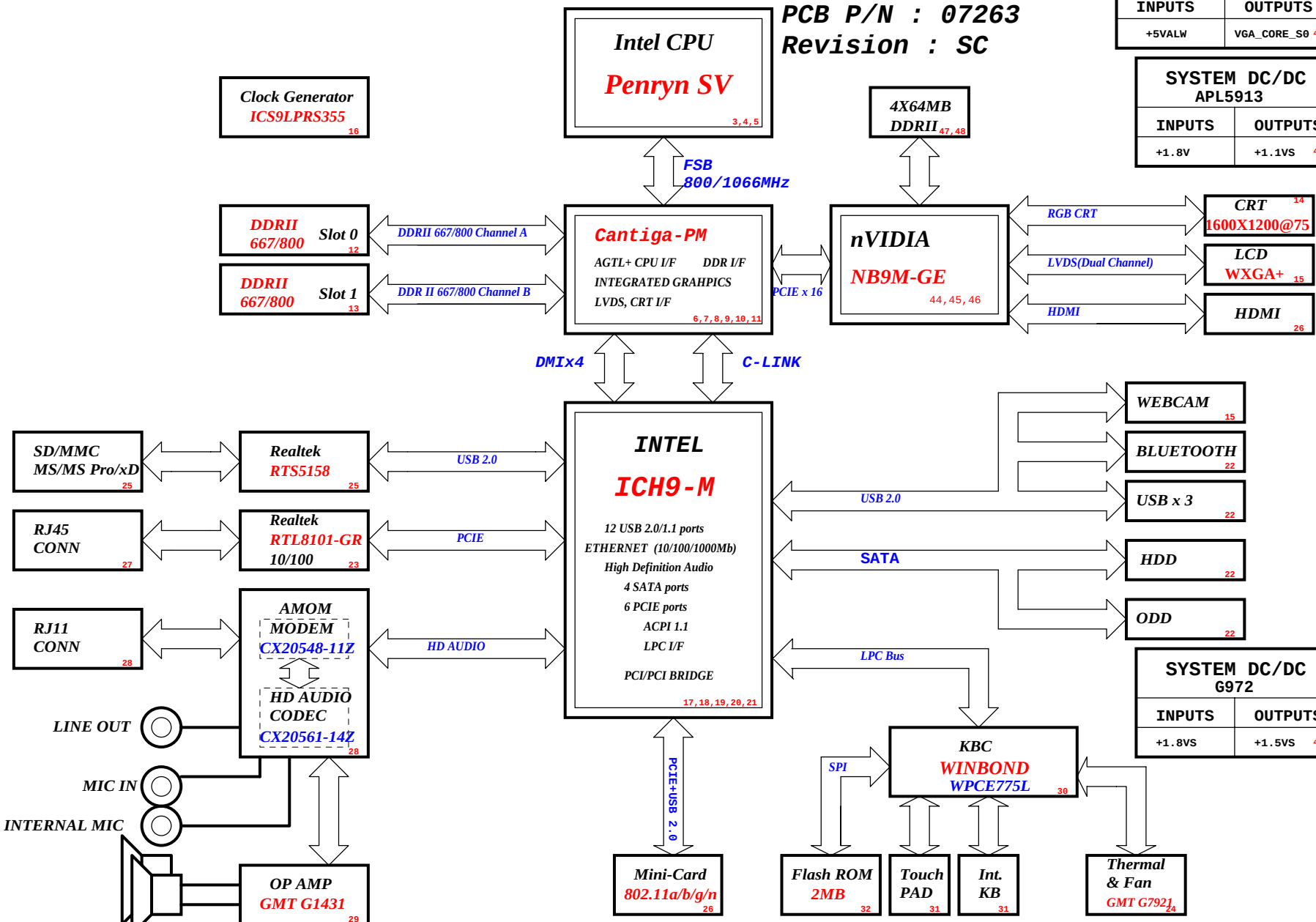
VITAS Block Diagram

Project code : 91.4I501.001
PCB P/N : 07263
Revision : SC



VGA DC/DC
SC421A

INPUTS	OUTPUTS
+5VALW	VGA_CORE_S0 42

SYSTEM DC/DC
APL5913

INPUTS	OUTPUTS
+1.8V	+1.1VS 42

SYSTEM DC/DC
G972

INPUTS	OUTPUTS
+1.8VS	+1.5VS 41

SYSTEM DC/DC
TPA51125

INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 38

SYSTEM DC/DC
TPS51116

INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 39

SYSTEM DC/DC
SC412A

INPUTS	OUTPUTS
+5VALW	+1.05V 40

MAXIM CHARGER
MAX8731

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 34

CPU DC/DC
ISL6260CCRZ

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 36,37

PCB LAYER

L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

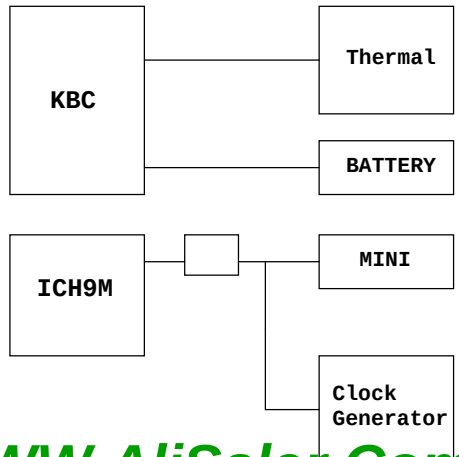
PCIE Routing page 19

LANE1	**LAN**
LANE2	**MiniCard WLAN**

USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



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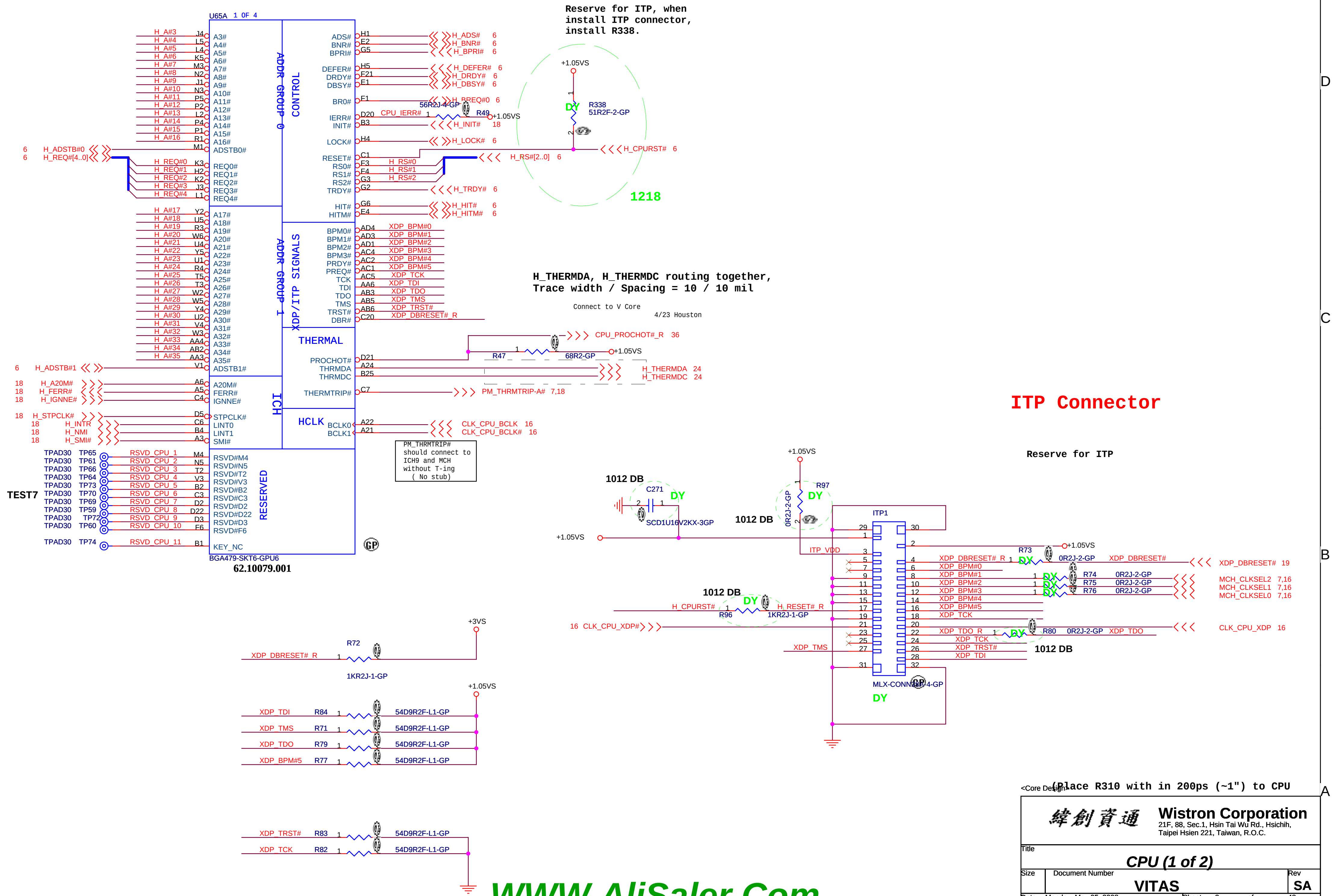

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Title		
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H_DINV#[3..0] H_DINV#[3..0] 6
H_DSTBN#[3..0] H_DSTBN#[3..0] 6
H_DSTBP#[3..0] H_DSTBP#[3..0] 6
H_D#[63..0] H_D#[63..0] 6

U65B 2 OF 4

DATA GRP0 / DATA GRP2

H_D#0	E22	D0#	D32#	Y22	H_D#32
H_D#1	E24	D1#	D33#	AB24	H_D#33
H_D#2	E26	D2#	D34#	V24	H_D#34
H_D#3	G22	D3#	D35#	V26	H_D#35
H_D#4	F23	D4#	D36#	V23	H_D#36
H_D#5	G25	D5#	D37#	T22	H_D#37
H_D#6	E25	D6#	D38#	U25	H_D#38
H_D#7	E23	D7#	D39#	U23	H_D#39
H_D#8	K24	D8#	D40#	Y25	H_D#40
H_D#9	G24	D9#	D41#	W22	H_D#41
H_D#10	J24	D10#	D42#	Y23	H_D#42
H_D#11	J23	D11#	D43#	W24	H_D#43
H_D#12	H22	D12#	D44#	W25	H_D#44
H_D#13	F26	D13#	D45#	AA23	H_D#45
H_D#14	K22	D14#	D46#	AA24	H_D#46
H_D#15	H23	D15#	D47#	AB25	H_D#47
6 H_DSTBN#0	J26	DSTBN0#	DSTBN2#	Y26	H_DSTBN#2 6
6 H_DSTBP#0	H26	DSTBP0#	DSTBP2#	AA26	H_DSTBP#2 6
6 H_DINV#0	H25	DINV0#	DINV2#	U22	H_DINV#2 6

DATA GRP1 / DATA GRP3

H_D#16	N22	D16#	D48#	AE24	H_D#48
H_D#17	K25	D17#	D49#	AD24	H_D#49
H_D#18	P26	D18#	D50#	AA21	H_D#50
H_D#19	R23	D19#	D51#	AB22	H_D#51
H_D#20	L23	D20#	D52#	AB21	H_D#52
H_D#21	M24	D21#	D53#	AC26	H_D#53
H_D#22	L22	D22#	D54#	AD20	H_D#54
H_D#23	M23	D23#	D55#	AE22	H_D#55
H_D#24	P25	D24#	D56#	AF23	H_D#56
H_D#25	P23	D25#	D57#	AC25	H_D#57
H_D#26	P22	D26#	D58#	AE21	H_D#58
H_D#27	T24	D27#	D59#	AD21	H_D#59
H_D#28	R24	D28#	D60#	AC22	H_D#60
H_D#29	L25	D29#	D61#	AD23	H_D#61
H_D#30	T25	D30#	D62#	AE22	H_D#62
H_D#31	N25	D31#	D63#	AC23	H_D#63
6 H_DSTBN#1	L26	DSTBN1#	DSTBN3#	AE25	H_DSTBN#3 6
6 H_DSTBP#1	M26	DSTBP1#	DSTBP3#	AF24	H_DSTBP#3 6
6 H_DINV#1	N24	DINV1#	DINV3#	AC20	H_DINV#3 6

MISC

	AD26	GTLREF	COMP0	R26	COMP0 R360 1 27D4R2F-L1-GP
TEST1	C23	TEST1	COMP1	U26	COMP1 R361 1 54D9R2F-L1-GP
TEST2	D25	TEST2	COMP2	AA1	COMP2 R78 1 27D4R2F-L1-GP
CPU_TEST3	C24	TEST3	COMP3	Y1	COMP3 R81 1 54D9R2F-L1-GP
	AF26	TEST4			
CPU_TEST5	AF1	TEST5	DPRSTP#	E5	H_DPRSTP# 7,18,36
	A26	TEST6	DPSLP#	B5	H_DPSLP# 18
			DPWR#	D24	H_DPWR# 6
			PWRGOOD	D6	H_PWRGD 18
			SLP#	D7	H_CPUSLP# 6
			PSI#	AE6	PSI# 36
16 CPU_BSEL0	B22	BSEL0			
16 CPU_BSEL1	B23	BSEL1			
16 CPU_BSEL2	C21	BSEL2			

BGA479-SKT6-GPU6

Connect to V Core

Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF

+1.05VS
1KR2F-3-GP R362
CPU_GTLREF0
R363 2KR2F-3-GP
C508 SC1KP50V2KX-1GP
R39 1KR2J-1-GP
R70 1KR2J-1-GP
R43 1KR2J-1-GP TEST1
R359 1KR2J-1-GP TEST2

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

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Please these inside socket cavity on L8(North side Secondary)

Please these inside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(North side Primary)

Please these outside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)

Please these inside socket cavity on L8(North side Secondary)

0128 DB

0429 PV

U65C 3 0F 4

BGA479-SKT6-GPU6

U65D 4 0F 4

BGA479-SKT6-GPU6

layout note: "1D5V_VCCA_S0" as short as possible

Layout Note:
Place as close as possible to the CPU VCCA pin.

Connect to V Core

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

NCTF PIN

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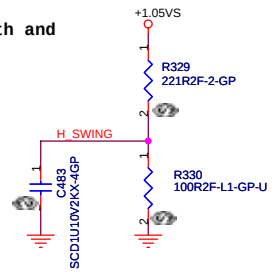
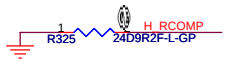
H_SWING routing Trace width and Spacing use 10 / 20 mil

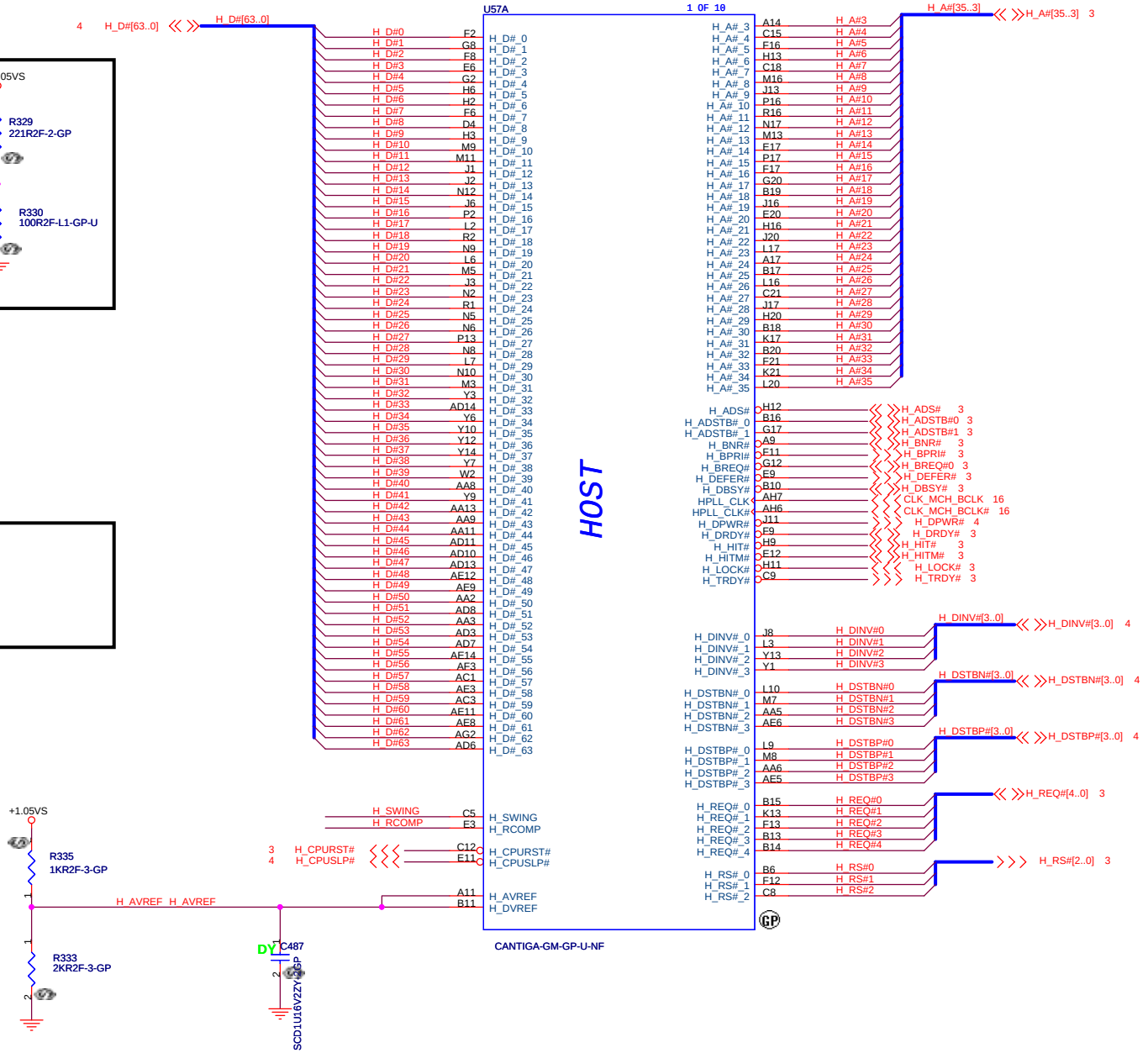
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

FSB setting

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

1011 DB

1113 DB

1015 DB

1107 DB

DDPC/SDVO for HDMI used

Please Close GMCH

Please Close to U22

CL_VREF ~= 0.35V

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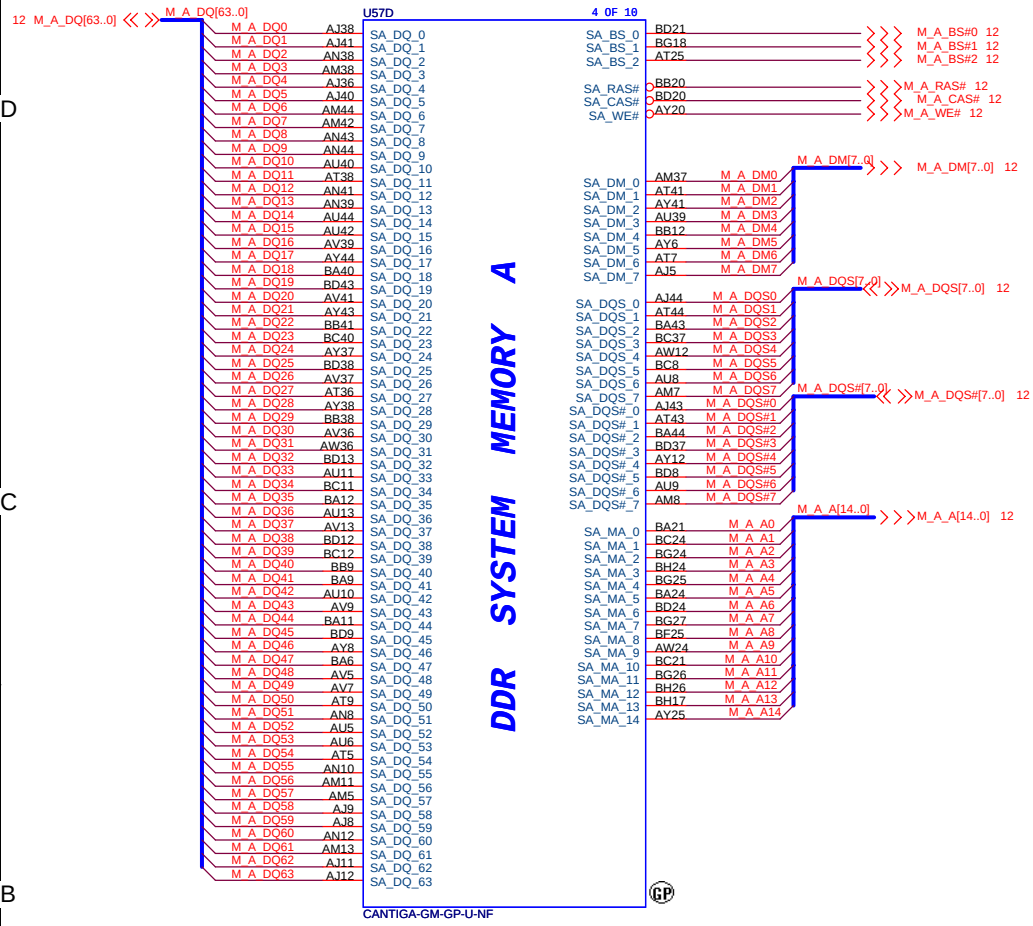

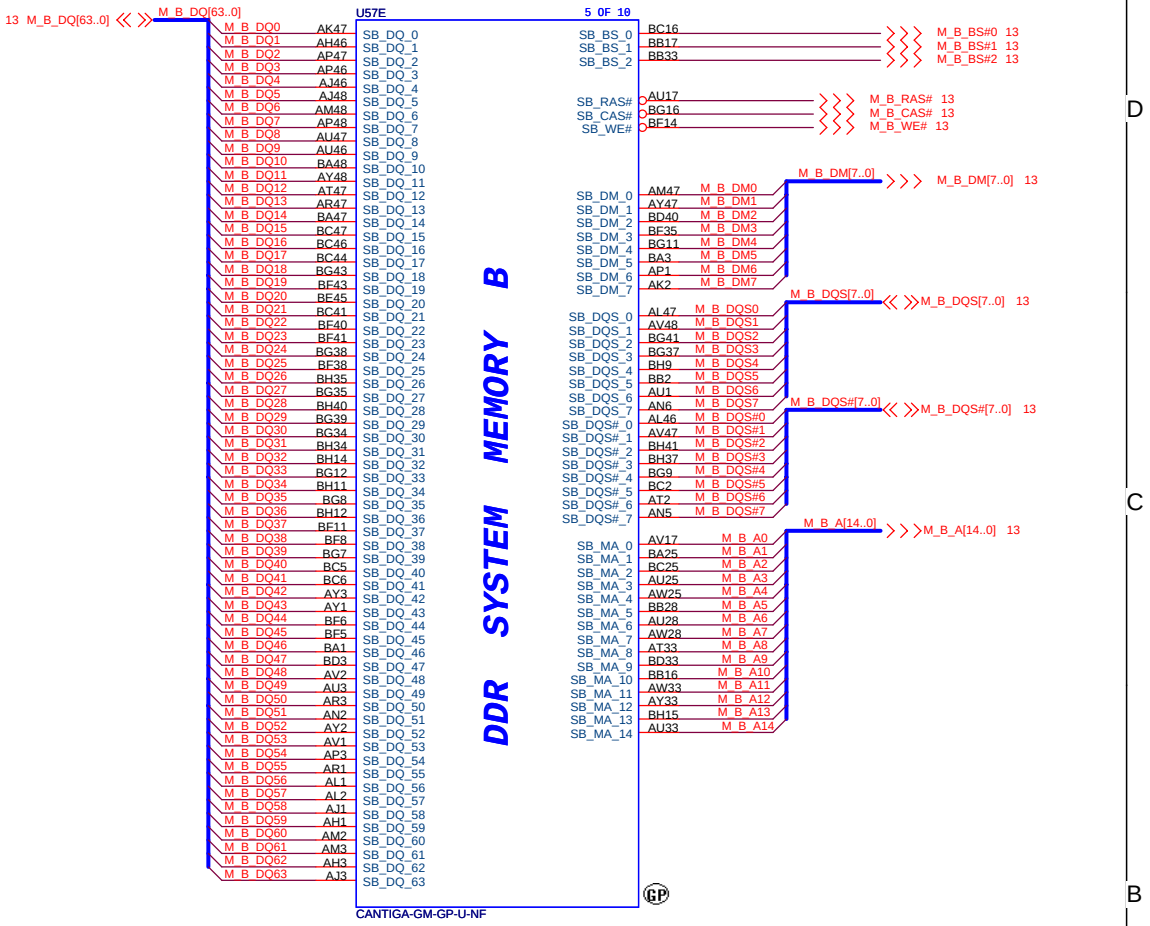

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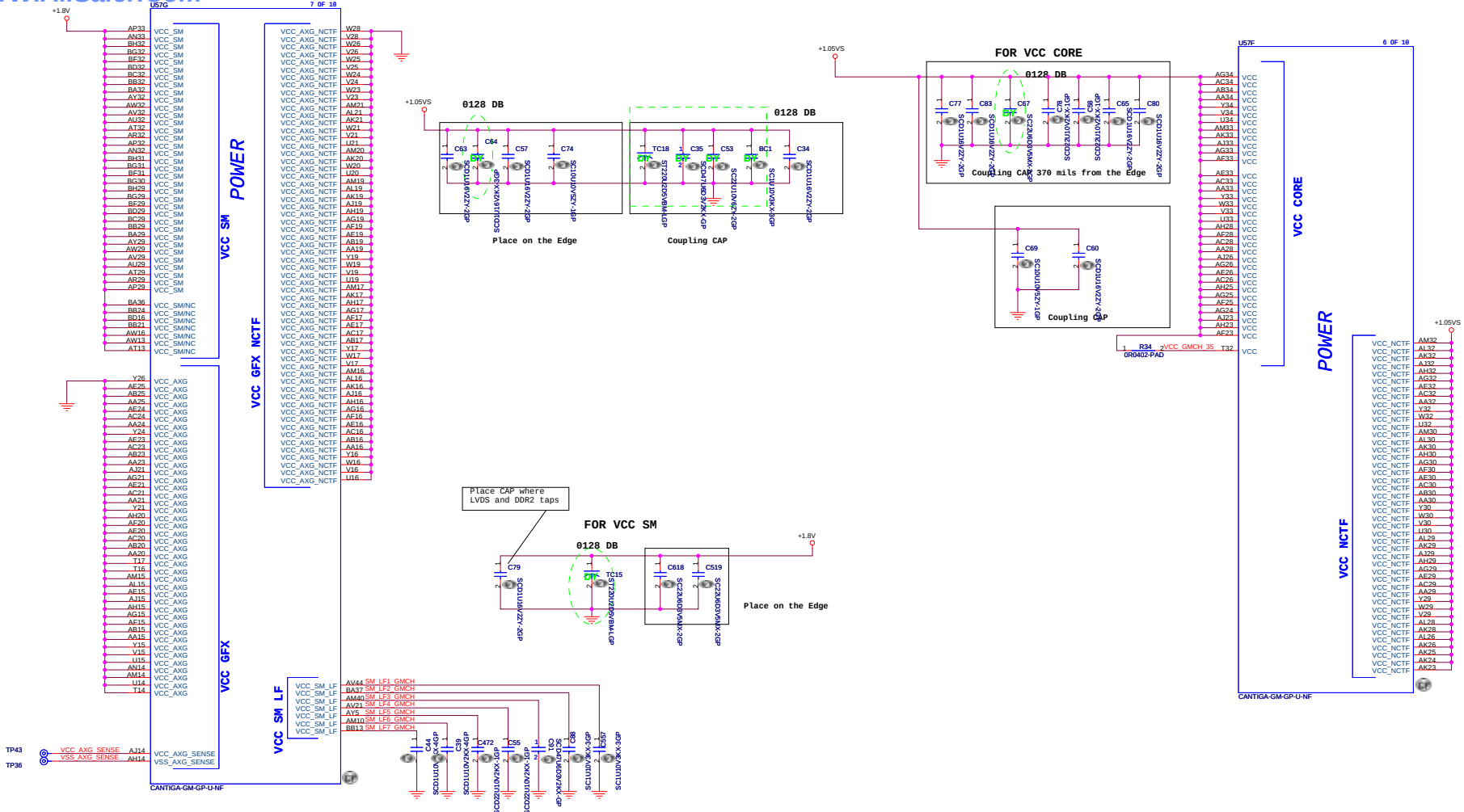

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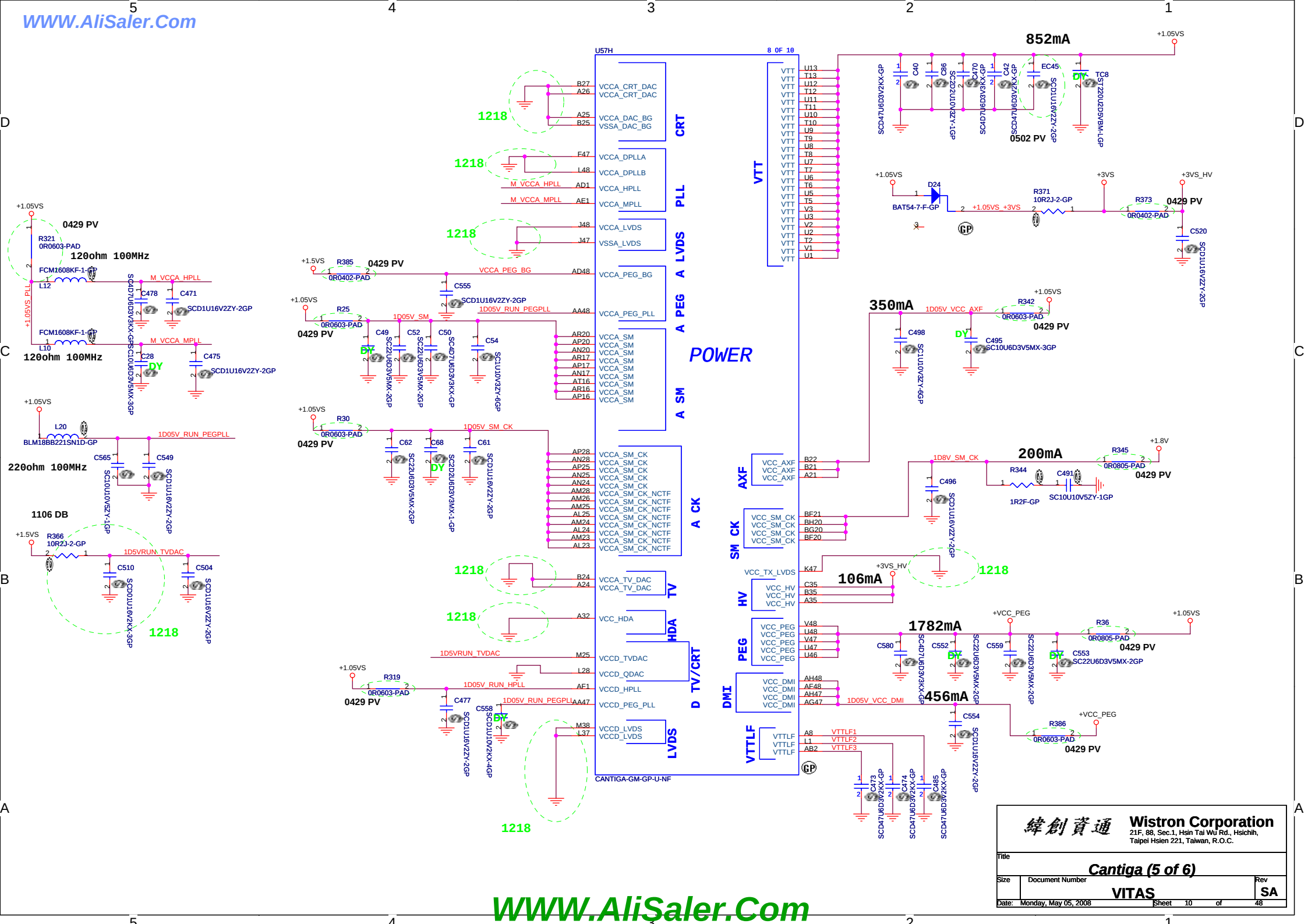

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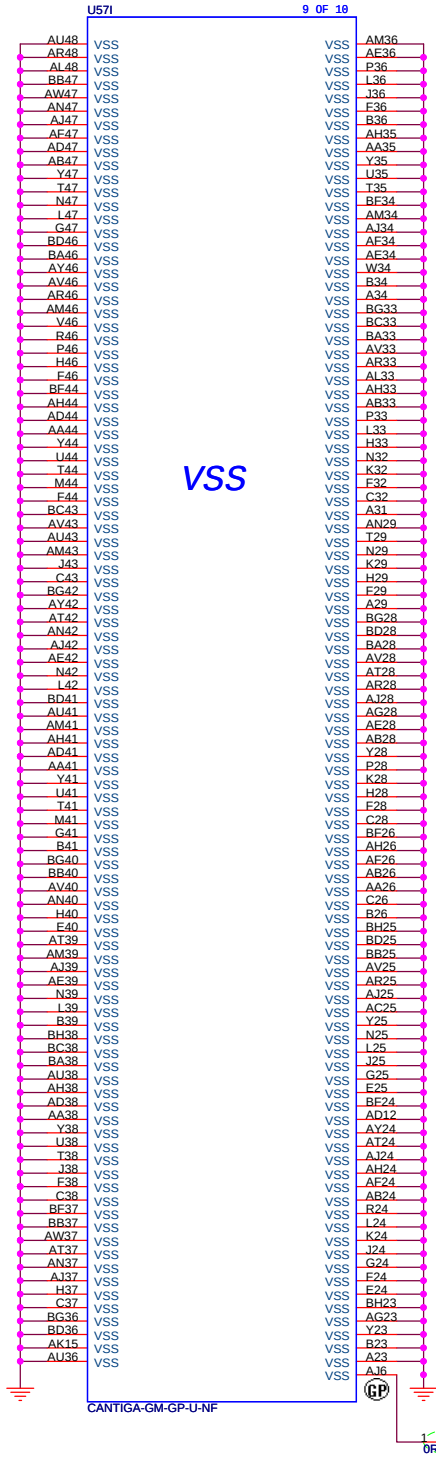

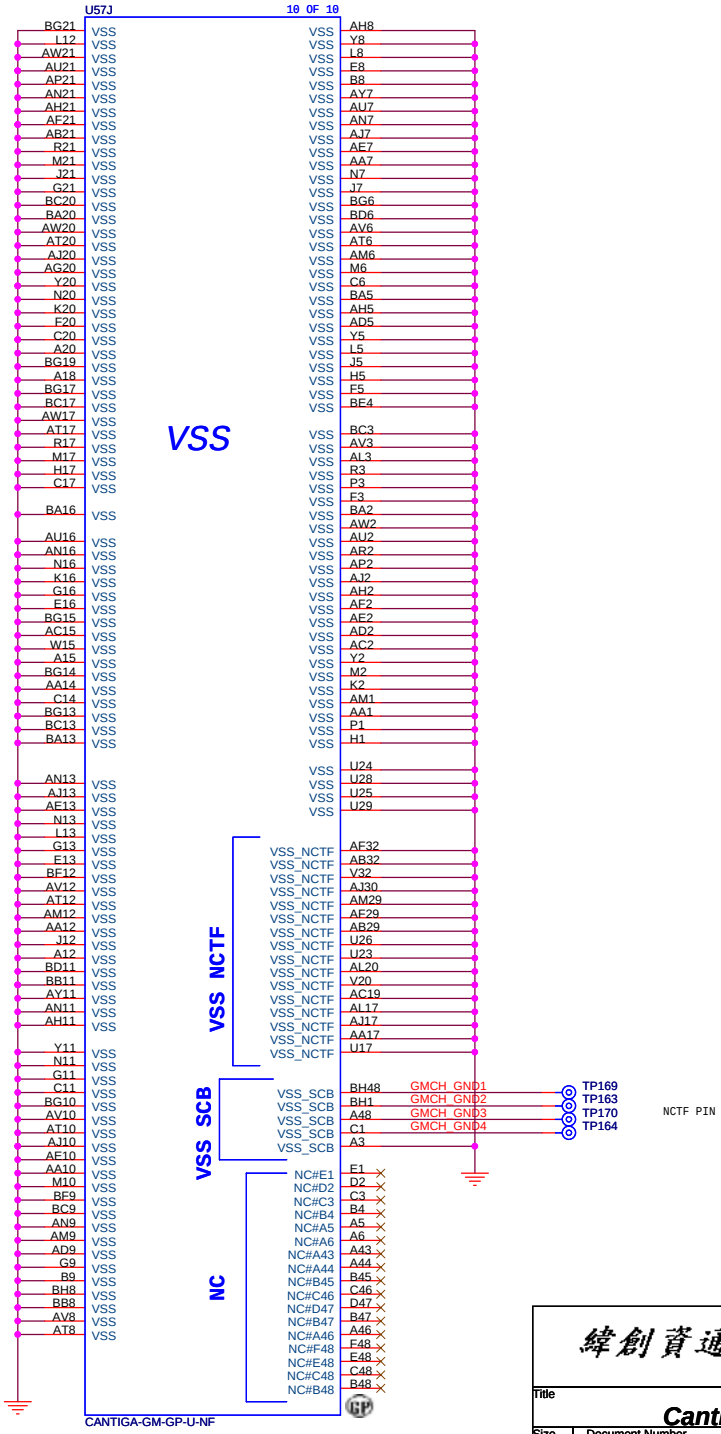

R19
0R0402-PAD

Modification AJ6 to reserved Pin

0429 PV

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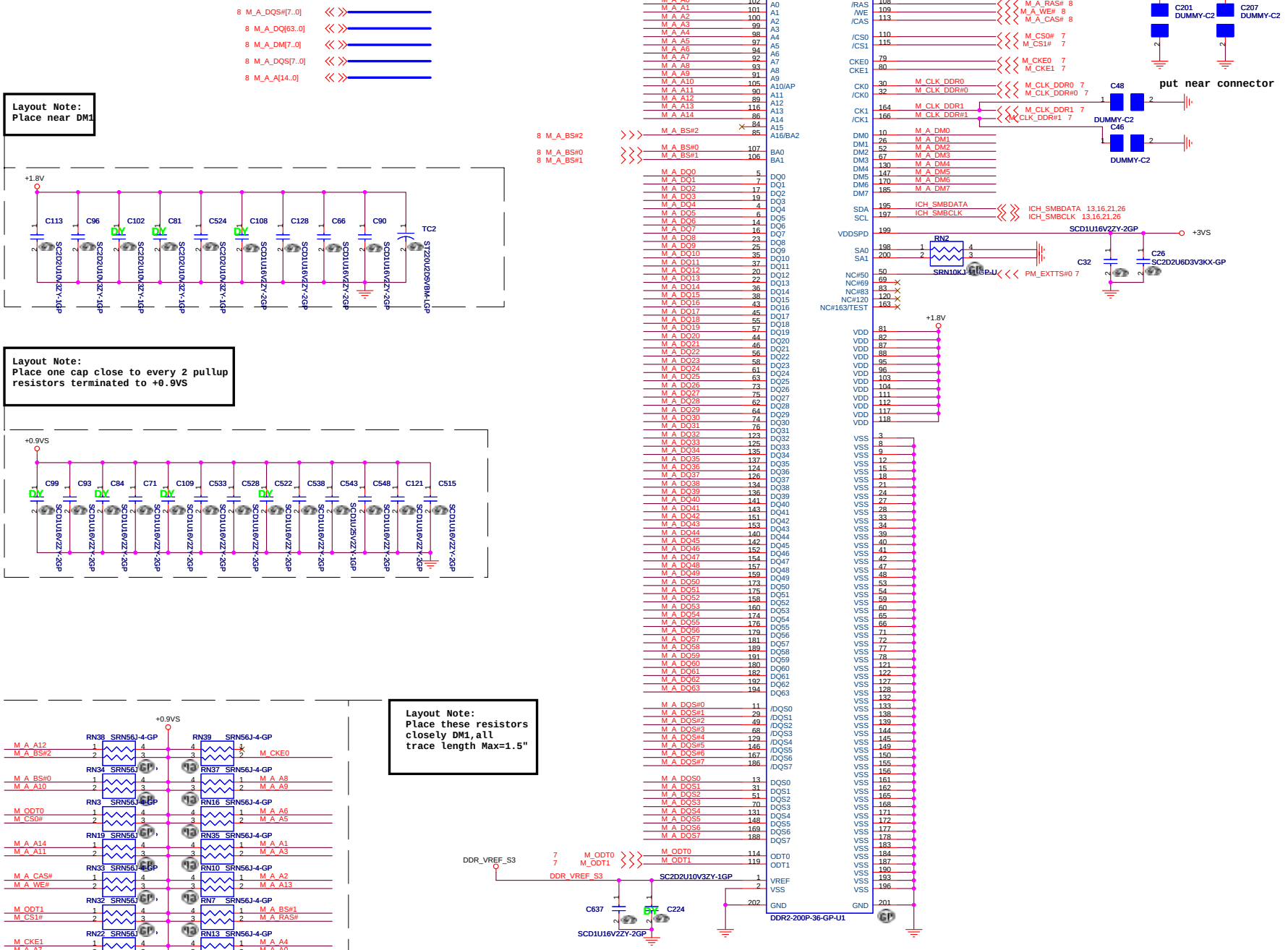

DM2 use 62.10017.E11

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Title: DDRII-SODIMM SLOT1

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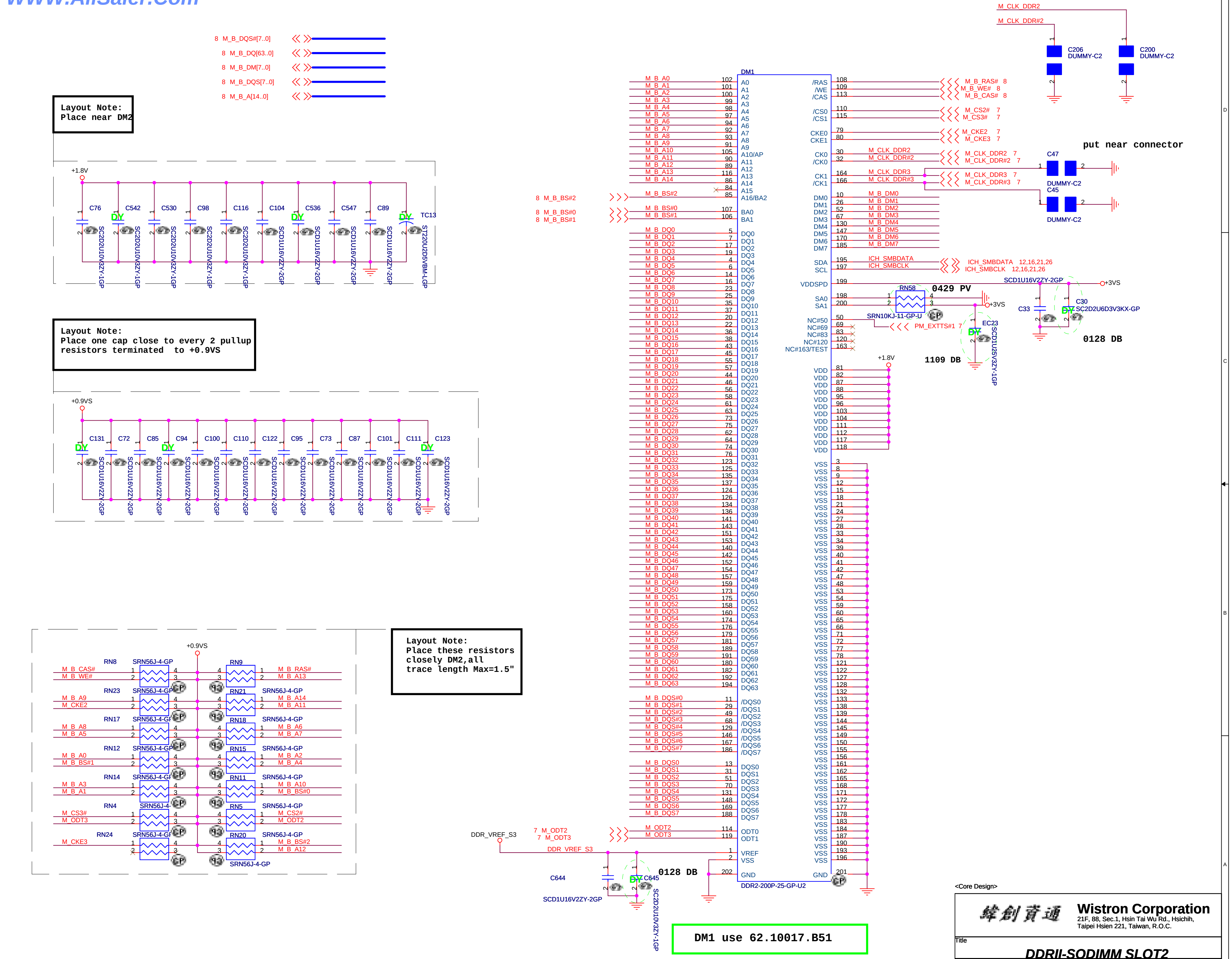

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Title: DDRII-SODIMM SLOT2

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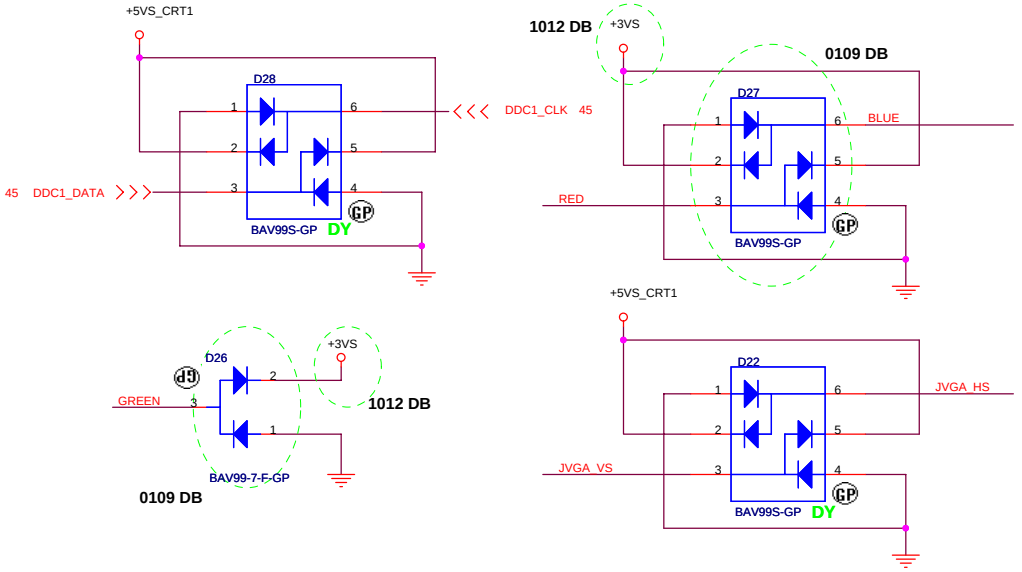
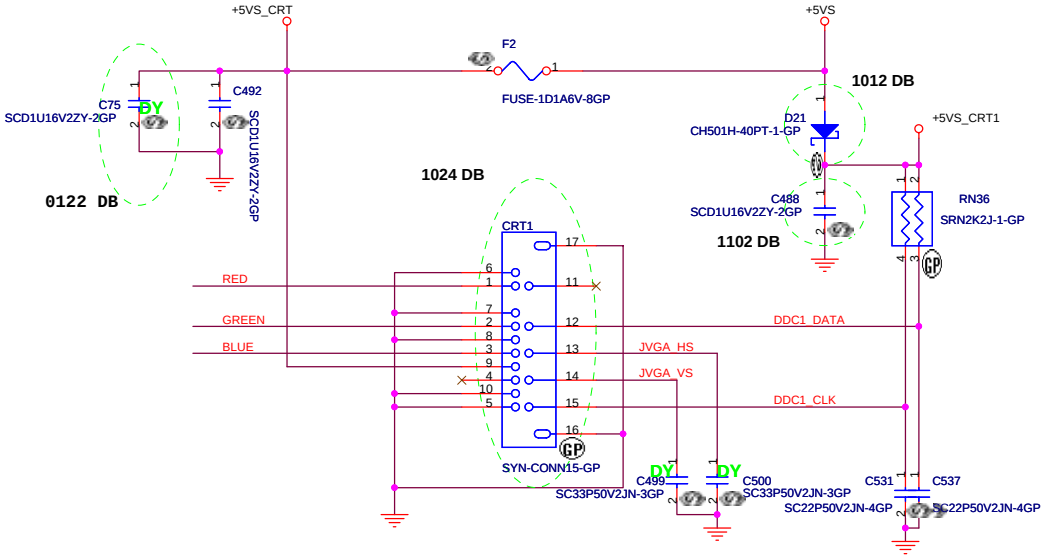
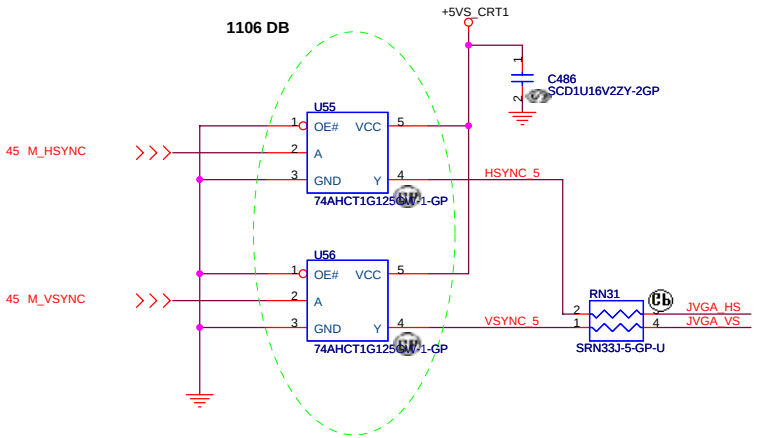
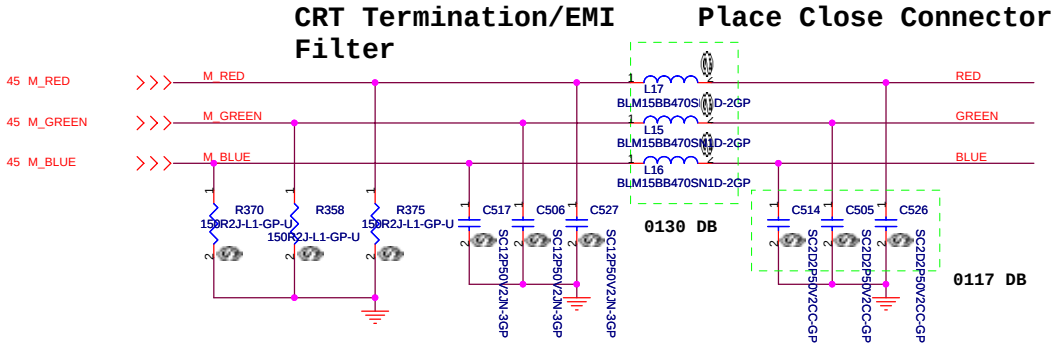
CRT I/F & CONNECTOR





Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





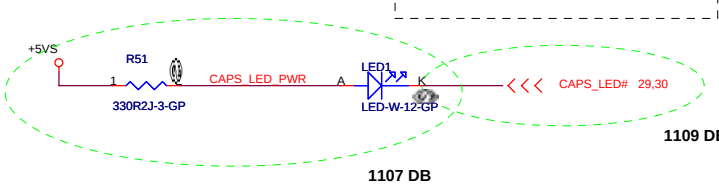
<Core Design>

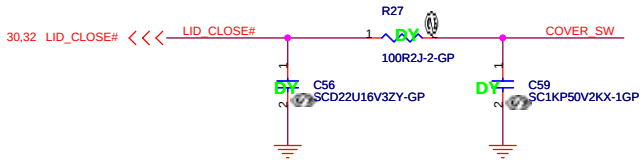
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

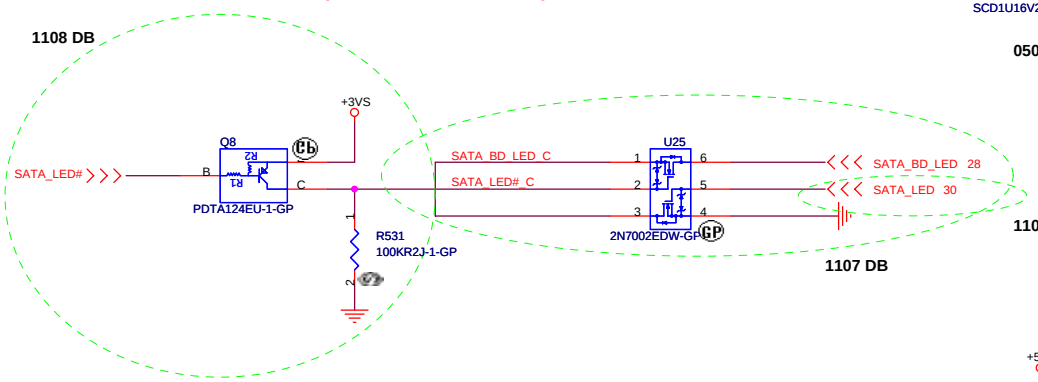
Title: CRT Connector		
Size: A3	Document Number: VITAS	Rev: SA
Date: Monday, May 05, 2008	Sheet 14 of 48	

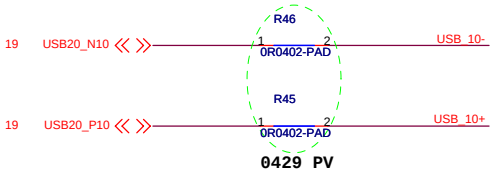
LCD / INVERTER INTERFACE / CAMERA

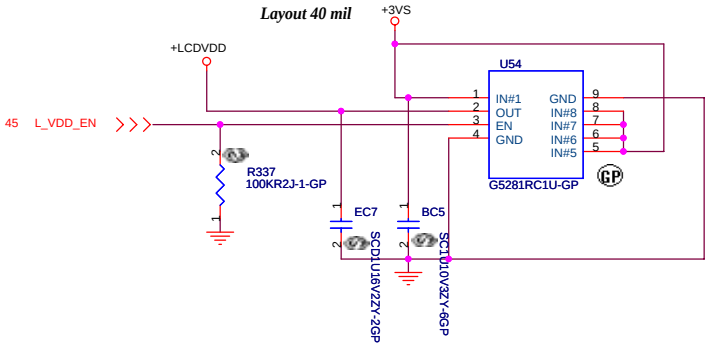
White LED:
Lite-On 83.00191.D70
Everlight 83.19217.F70

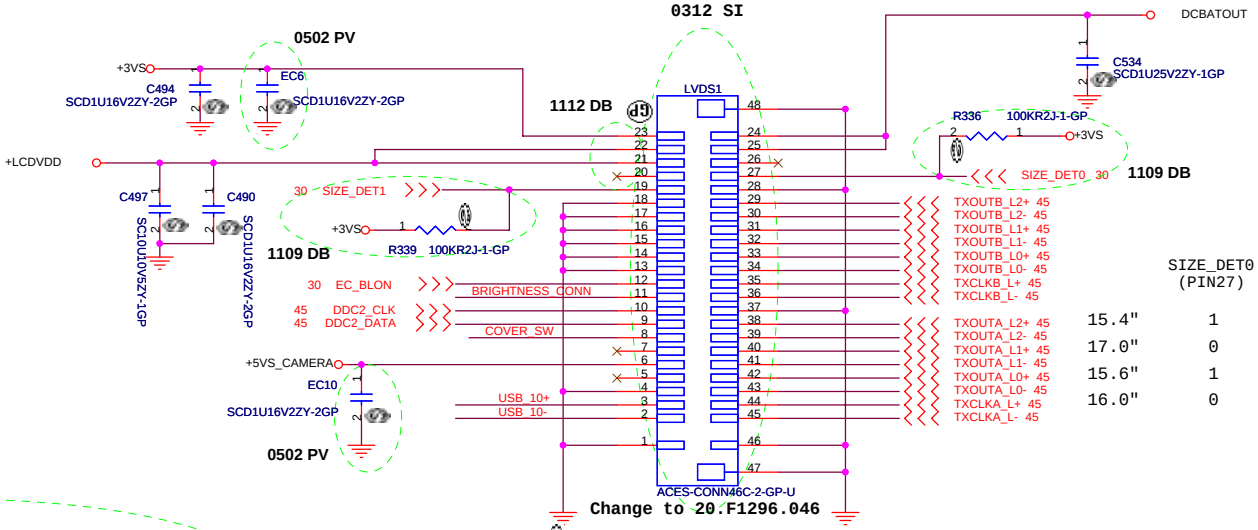




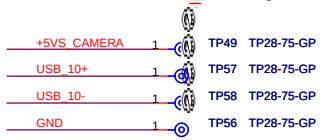


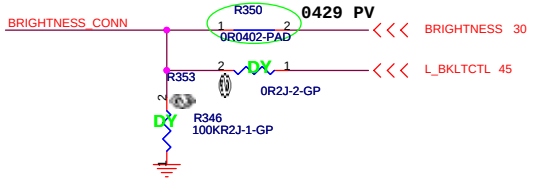


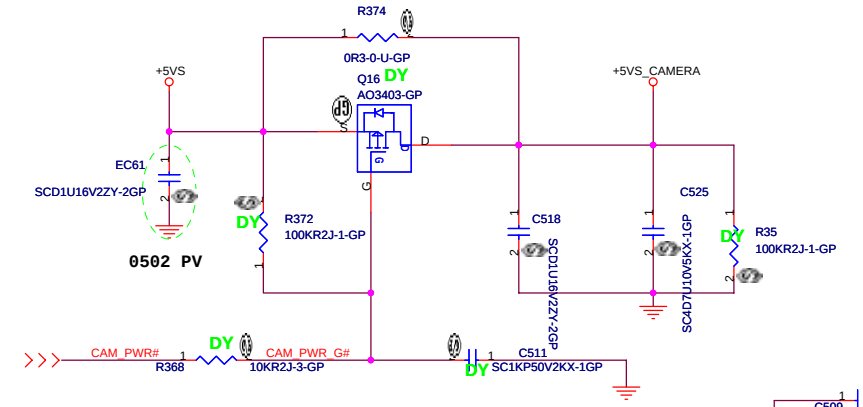


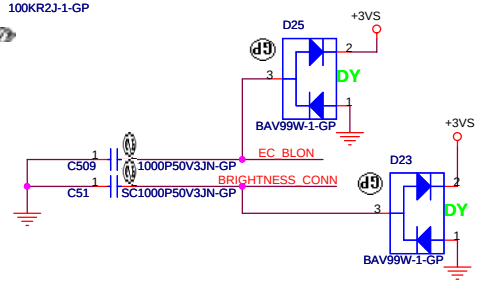


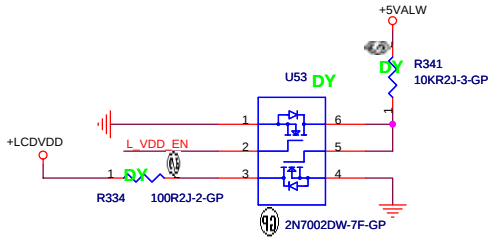
	SIZE_DET0 (PIN27)	SIZE_DET1 (PIN19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0







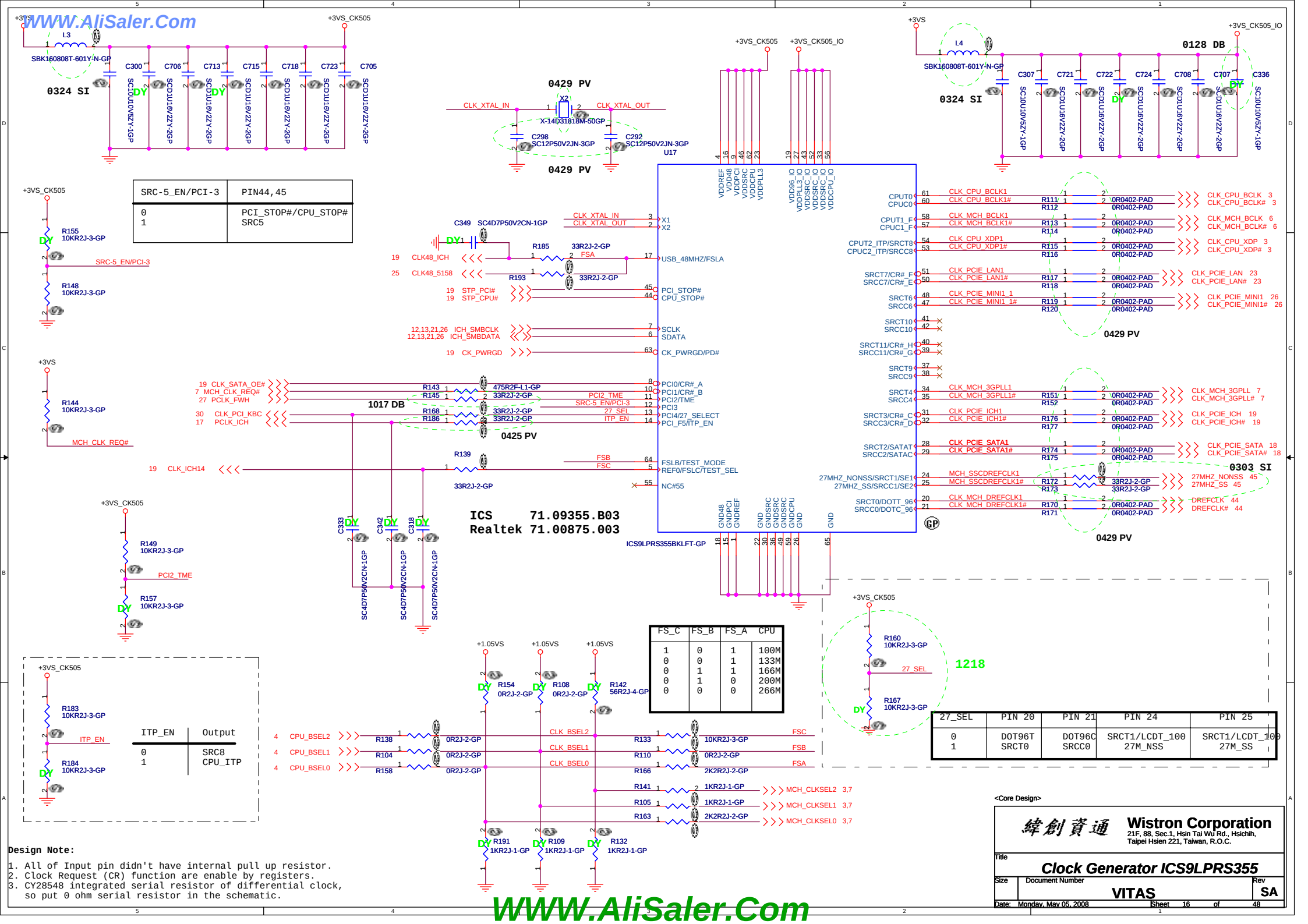




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector/CAM/LED
Size: A3 | Document Number: VITAS | Rev: SA
Date: Monday, May 05, 2008 | Sheet 15 of 48



SRC-5_EN/PCI-3	PIN44,45
0	PCI_STOP#/CPU_STOP#
1	SRC5

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M
0	0	0	266M

ITP_EN	Output
0	SRC8
1	CPU_ITP

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

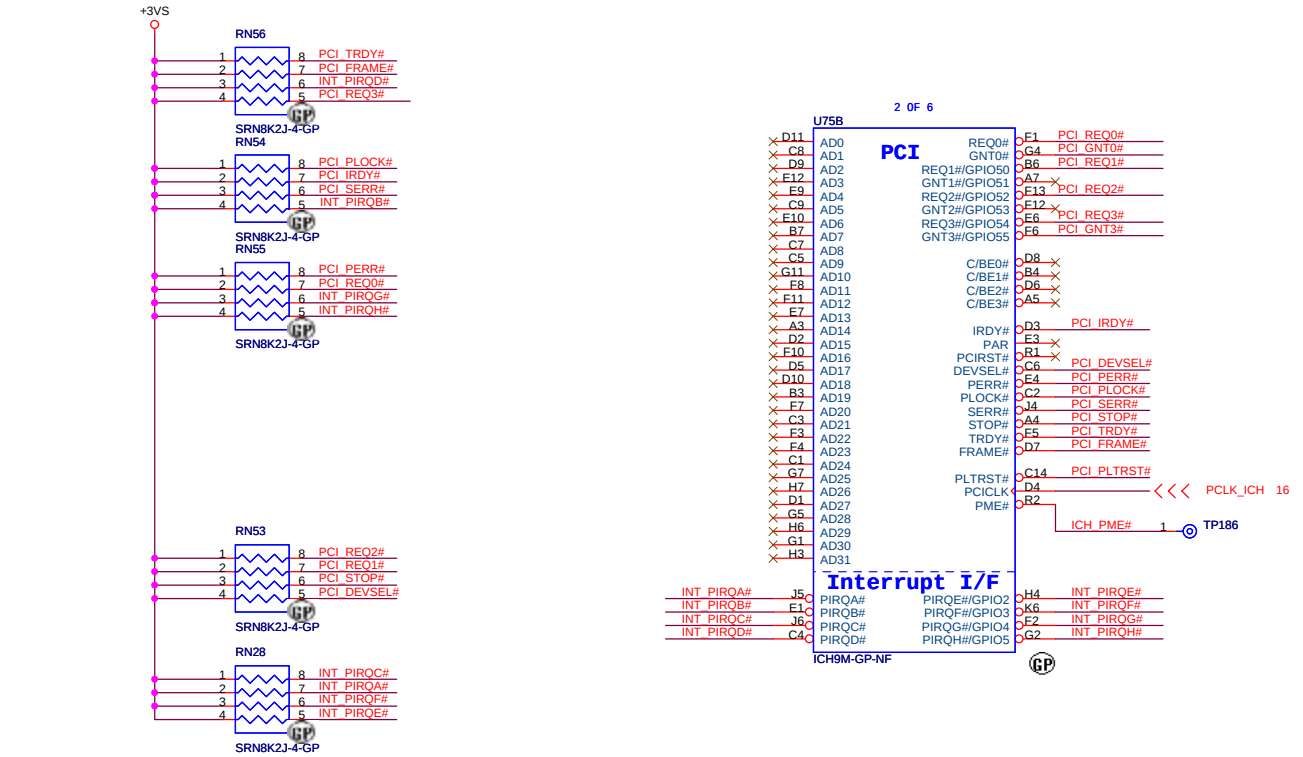
<Core Design>

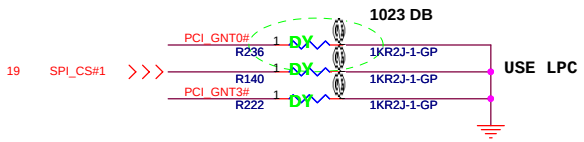
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

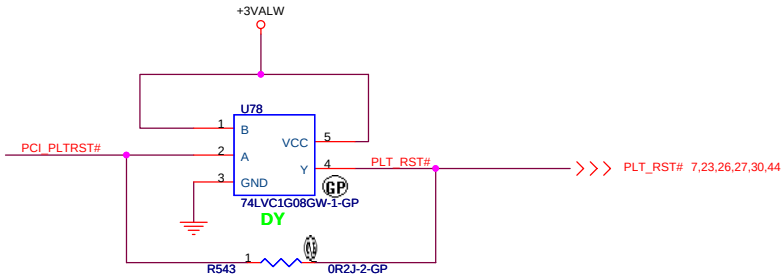
Title: Clock Generator ICS9LPRS355

Size: | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 16 of 48







BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

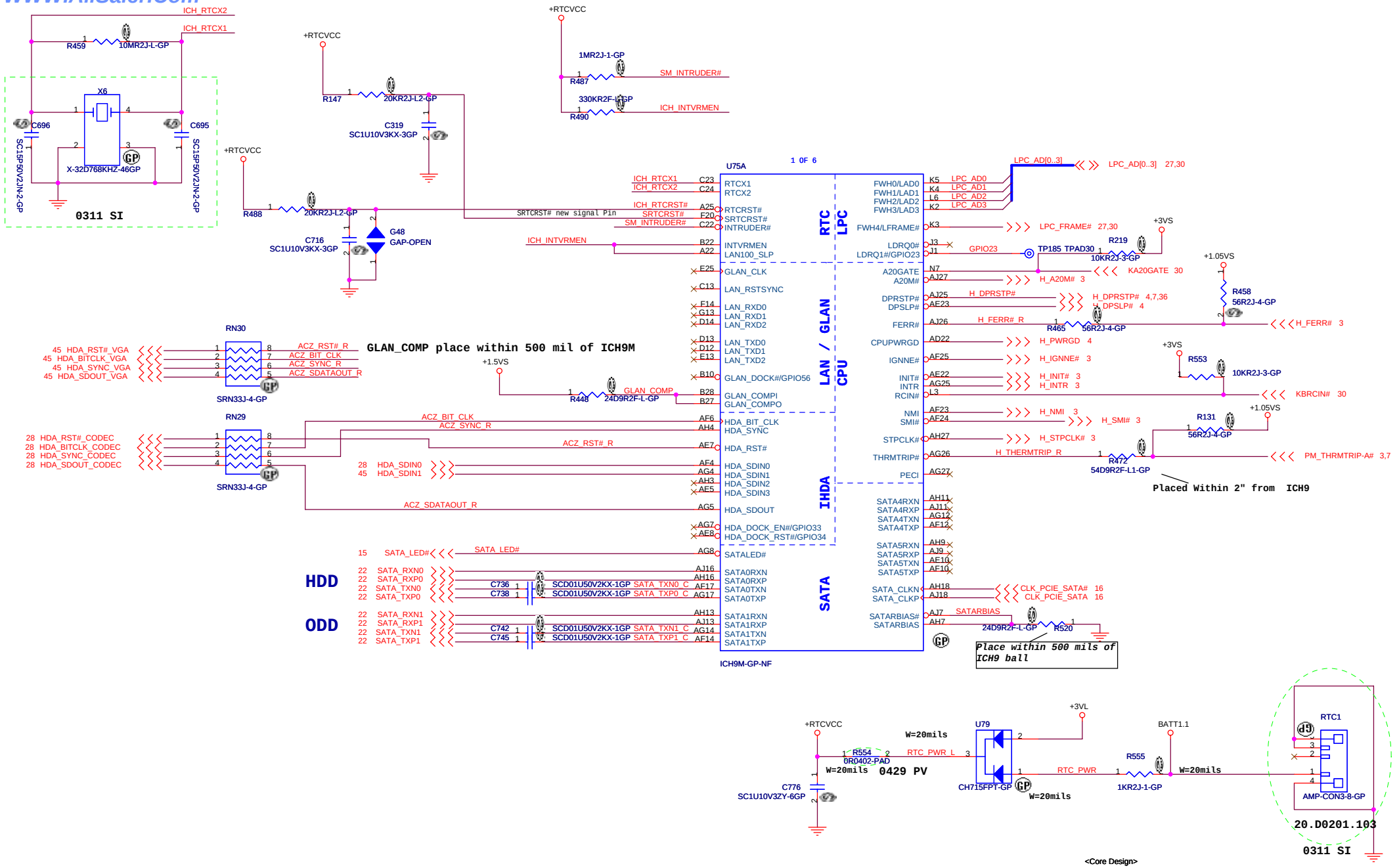
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 5)

Size | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 17 of 48



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

<Core Design>

緯創資通 Wistron Corporation
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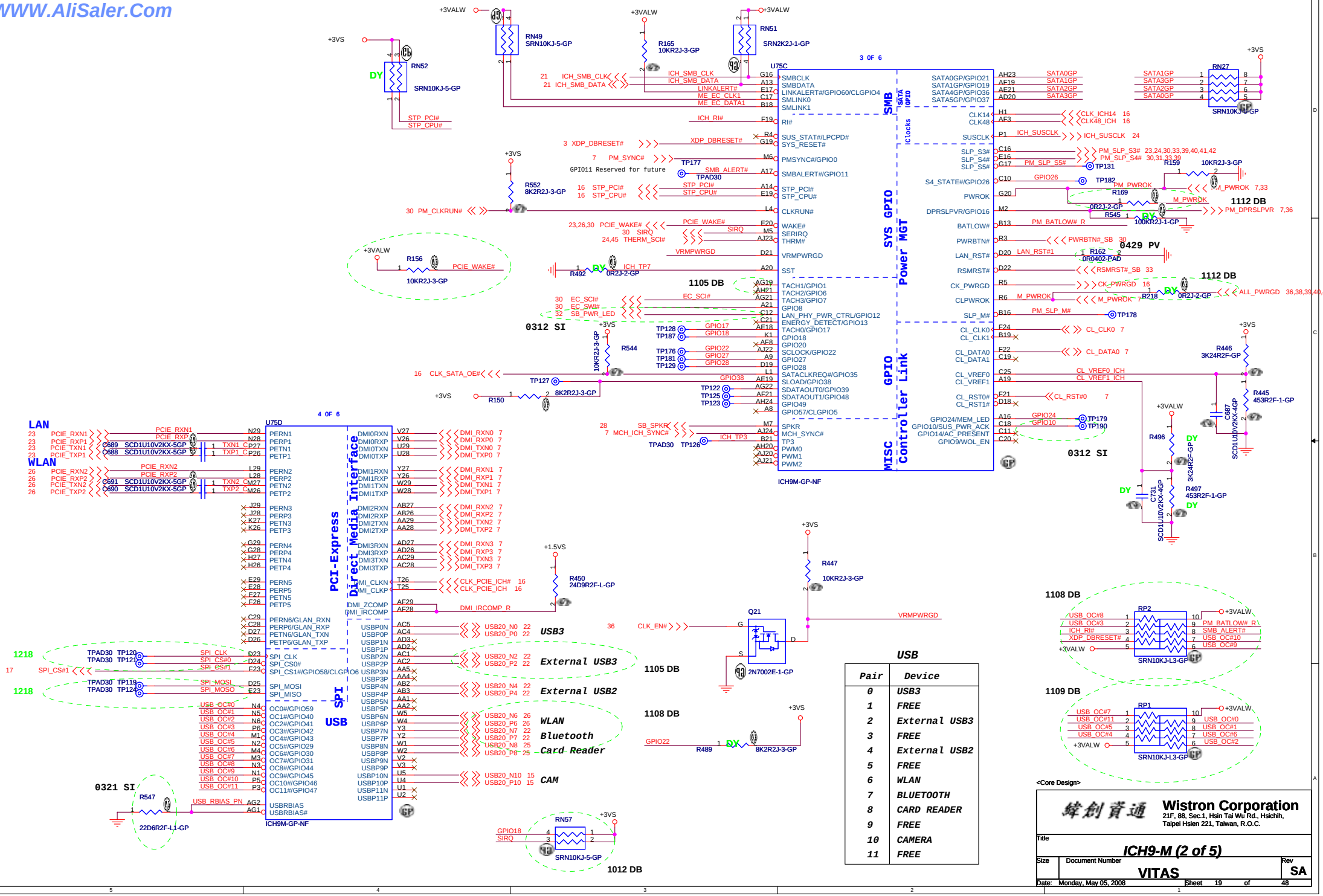
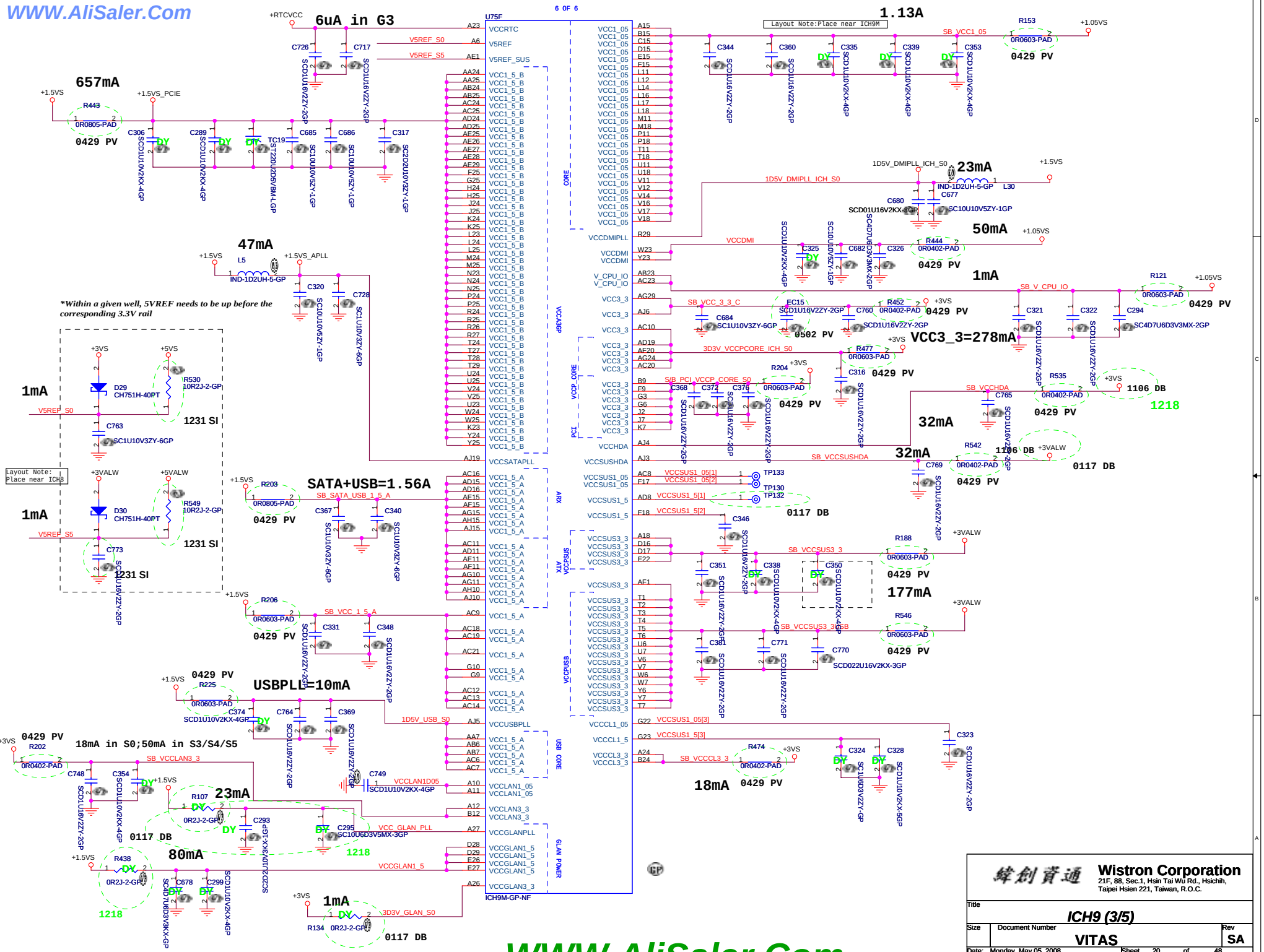
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ICH9-M (2 of 5)		
Size	Document Number	Rev
	VITAS	SA
Date: Monday, May 05, 2008	Sheet 18 of 48	





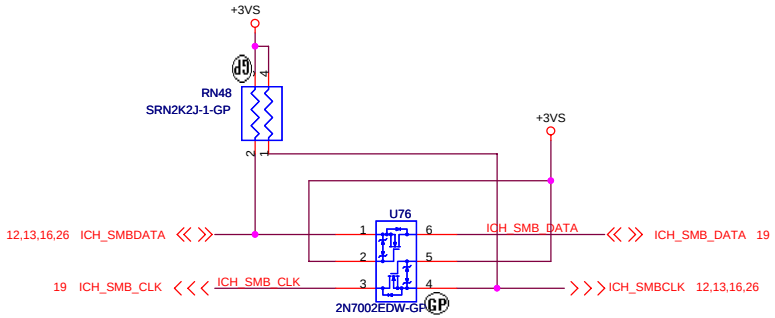
5 OF 6

U75E

AA26	VSS	VSS	H5
AA27	VSS	VSS	J23
AA3	VSS	VSS	J26
AA6	VSS	VSS	J27
AB1	VSS	VSS	AC22
AA23	VSS	VSS	K28
AB28	VSS	VSS	K29
AB29	VSS	VSS	L13
AB4	VSS	VSS	L15
AB5	VSS	VSS	L2
AC17	VSS	VSS	L26
AC26	VSS	VSS	L27
AC27	VSS	VSS	L5
AC3	VSS	VSS	L7
AD1	VSS	VSS	M12
AD10	VSS	VSS	M13
AD12	VSS	VSS	M14
AD13	VSS	VSS	M15
AD14	VSS	VSS	M16
AD17	VSS	VSS	M17
AD18	VSS	VSS	M23
AD21	VSS	VSS	M28
AD28	VSS	VSS	M29
AD29	VSS	VSS	N11
AD4	VSS	VSS	N12
AD5	VSS	VSS	N13
AD6	VSS	VSS	N14
AD7	VSS	VSS	N15
AD9	VSS	VSS	N16
AE12	VSS	VSS	N17
AE13	VSS	VSS	N18
AE14	VSS	VSS	N26
AE16	VSS	VSS	N27
AE17	VSS	VSS	P12
AE2	VSS	VSS	P13
AE20	VSS	VSS	P14
AE24	VSS	VSS	P15
AE3	VSS	VSS	P16
AE4	VSS	VSS	P17
AE6	VSS	VSS	P2
AE9	VSS	VSS	P23
AF13	VSS	VSS	P28
AF16	VSS	VSS	P29
AF18	VSS	VSS	P4
AF22	VSS	VSS	P7
AH26	VSS	VSS	R11
AF26	VSS	VSS	R12
AF27	VSS	VSS	R13
AF5	VSS	VSS	R14
AF7	VSS	VSS	R15
AF9	VSS	VSS	R16
AG13	VSS	VSS	R17
AG16	VSS	VSS	R18
AG18	VSS	VSS	R28
AG20	VSS	VSS	T12
AG23	VSS	VSS	T13
AG3	VSS	VSS	T14
AG6	VSS	VSS	T15
AG9	VSS	VSS	T16
AH12	VSS	VSS	T17
AH14	VSS	VSS	T23
AH17	VSS	VSS	B26
AH19	VSS	VSS	U12
AH2	VSS	VSS	U13
AH22	VSS	VSS	U14
AH25	VSS	VSS	U15
AH28	VSS	VSS	U16
AH5	VSS	VSS	U17
AH8	VSS	VSS	AD23
AJ12	VSS	VSS	U26
AJ14	VSS	VSS	U27
AJ17	VSS	VSS	U3
AJ8	VSS	VSS	V1
B11	VSS	VSS	V13
B14	VSS	VSS	V15
B17	VSS	VSS	V23
B2	VSS	VSS	V28
B20	VSS	VSS	V29
B23	VSS	VSS	V4
B5	VSS	VSS	V5
B8	VSS	VSS	W26
C26	VSS	VSS	W27
C27	VSS	VSS	W3
E11	VSS	VSS	Y1
E14	VSS	VSS	Y28
E18	VSS	VSS	Y29
E2	VSS	VSS	Y4
E21	VSS	VSS	Y5
E24	VSS	VSS	AG28
E5	VSS	VSS	AH6
E8	VSS	VSS	AF2
F16	VSS	VSS	B25
F28	VSS		
F29	VSS	A1	ICH_GND1 — TP184
G12	VSS	A2	
G14	VSS	A28	
G18	VSS	A29	ICH_GND2 — TP175
G21	VSS	AH1	
G24	VSS	AH29	
G26	VSS	AJ1	ICH_GND3 — TP183
G27	VSS	AJ2	
G8	VSS	AJ28	
H2	VSS	AJ29	ICH_GND4 — TP174
H23	VSS	B1	
H28	VSS	B29	
H29	VSS		

ICH9M-GP-NF

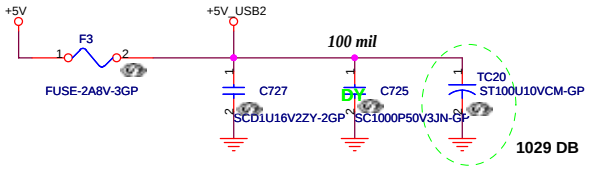
NCTF PIN

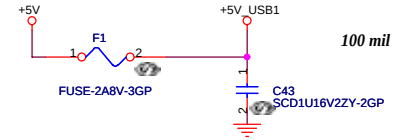


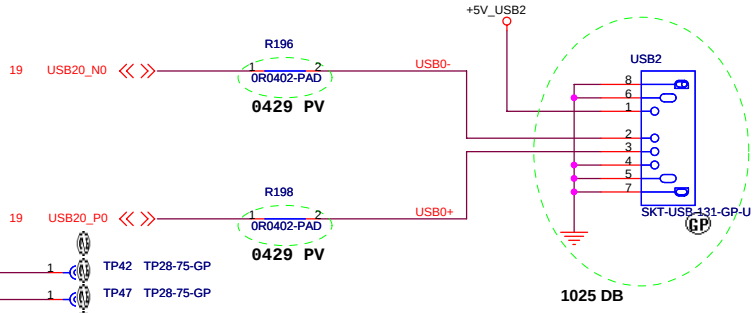
SMBUS

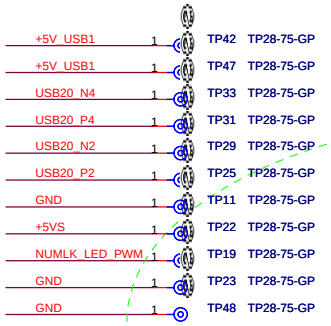
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	ICH9-M (4 of 4)		
Size	Document Number: VITAS		Rev: SA
Date: Monday, May 05, 2008	Sheet 21 of 48		

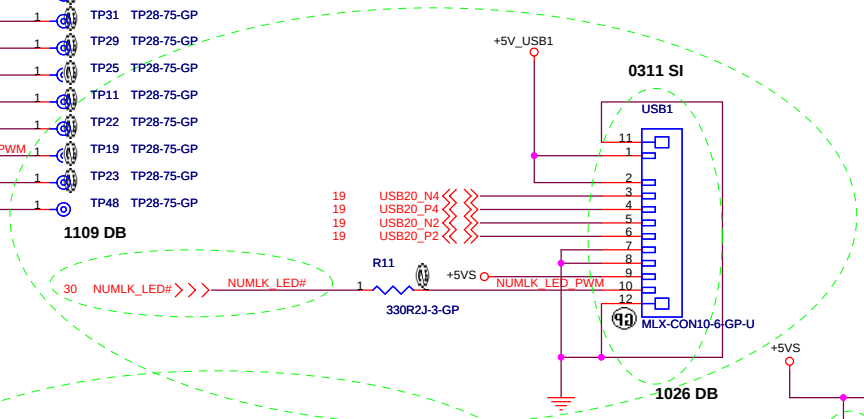
USB PORT

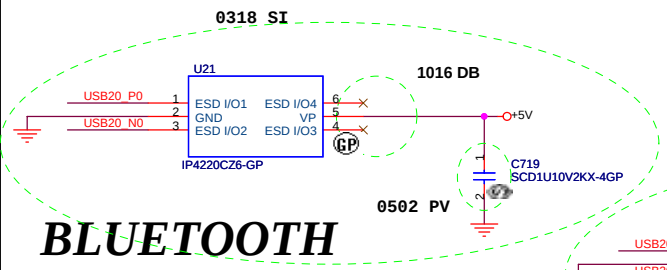




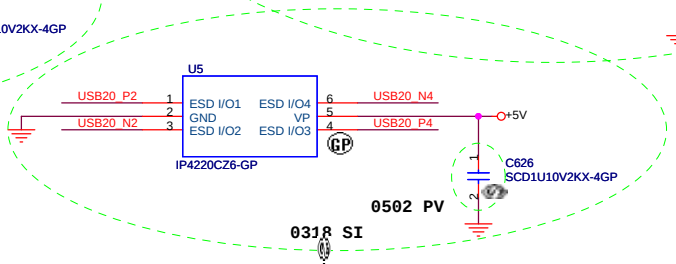


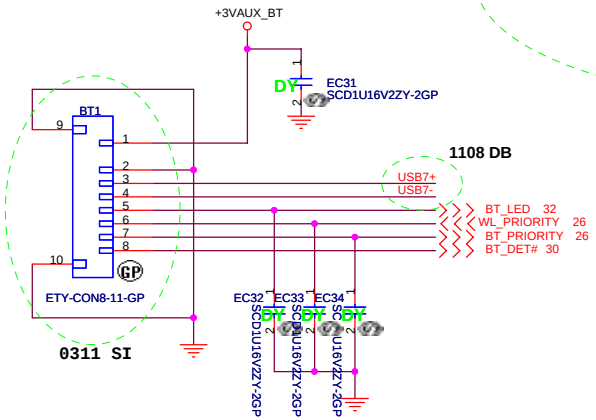


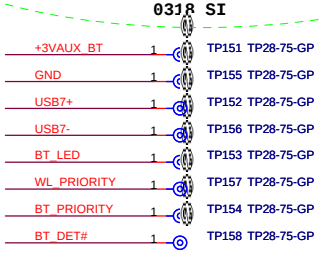


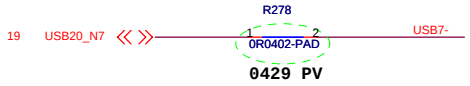


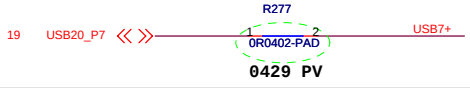
BLUETOOTH



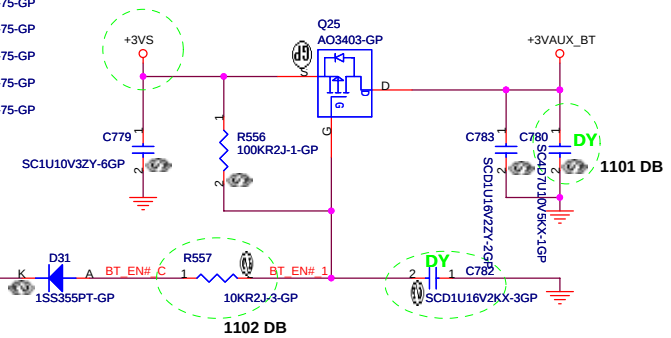




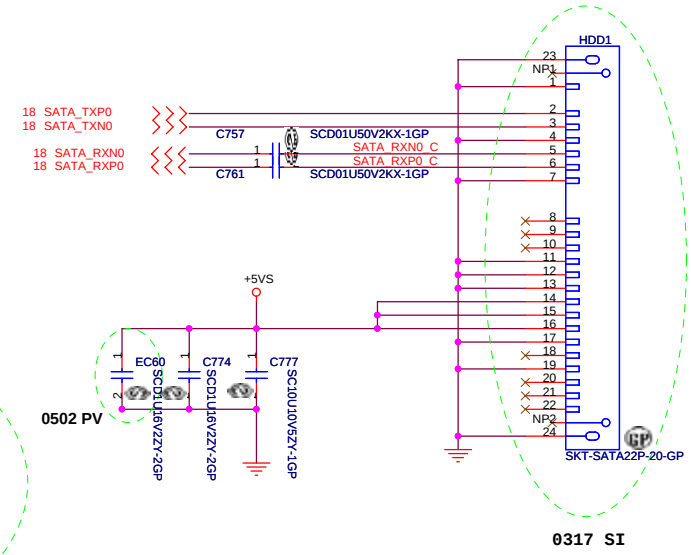




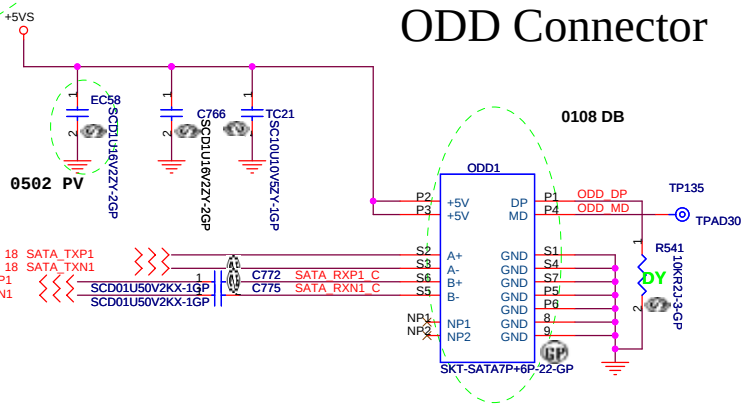
MAX 150mA



SATA HD Connector



ODD Connector



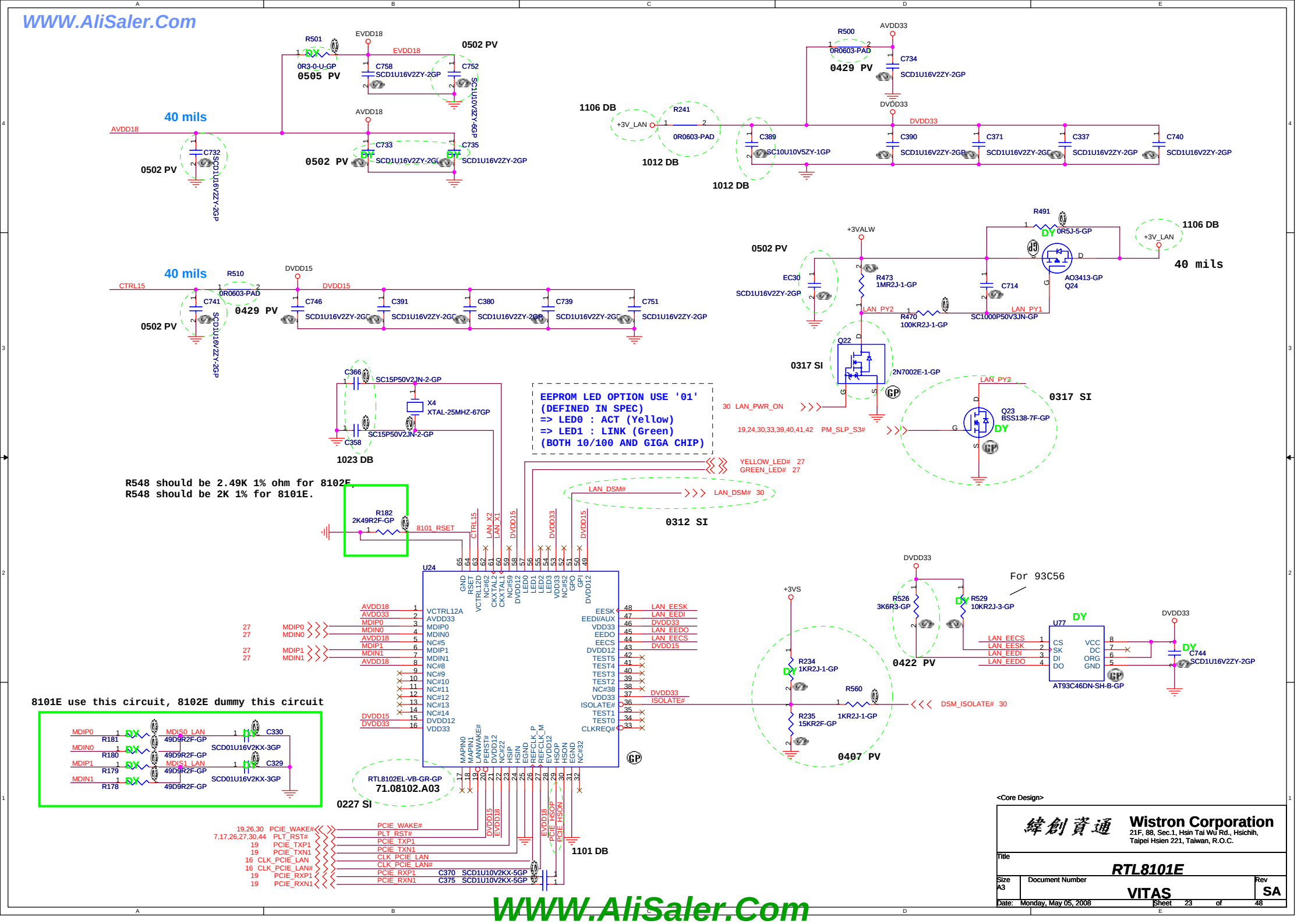
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/CDROM/USB/BT

Size	Document Number	Rev
A3	VITAS	SA

Date: Monday, May 05, 2008 Sheet 22 of 48

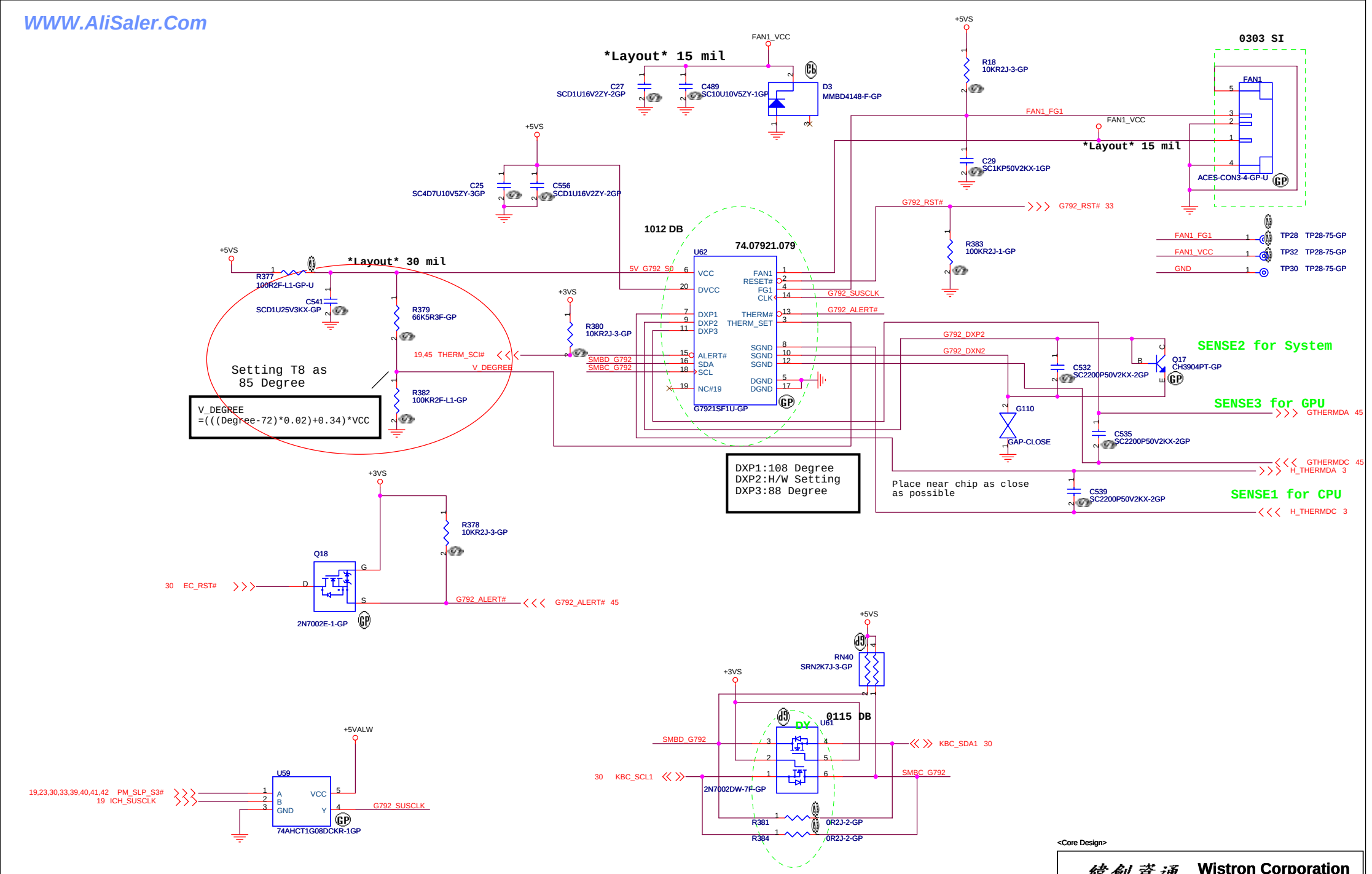


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8101E**

Size	Document Number	Rev
A3	VITAS	SA

Date: Monday, May 05, 2008 Sheet 23 of 48



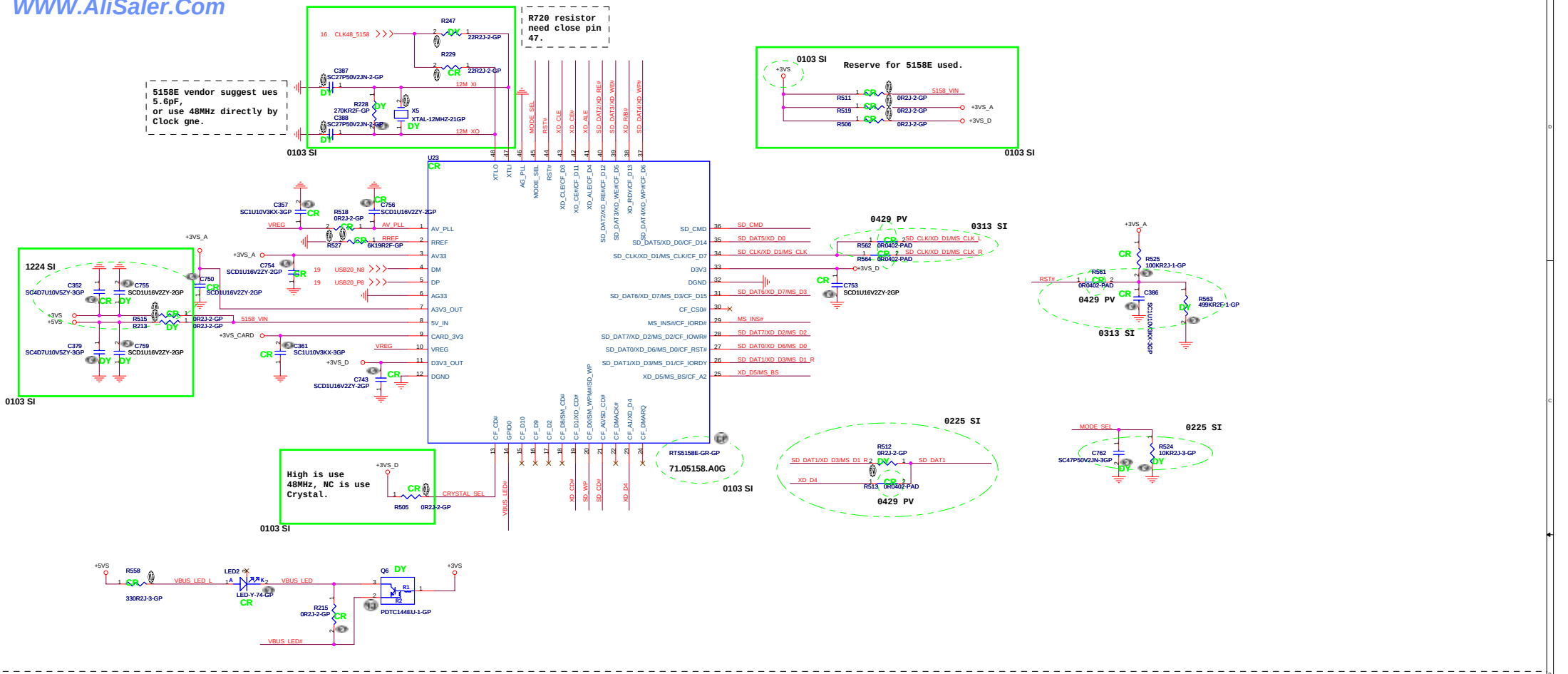
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

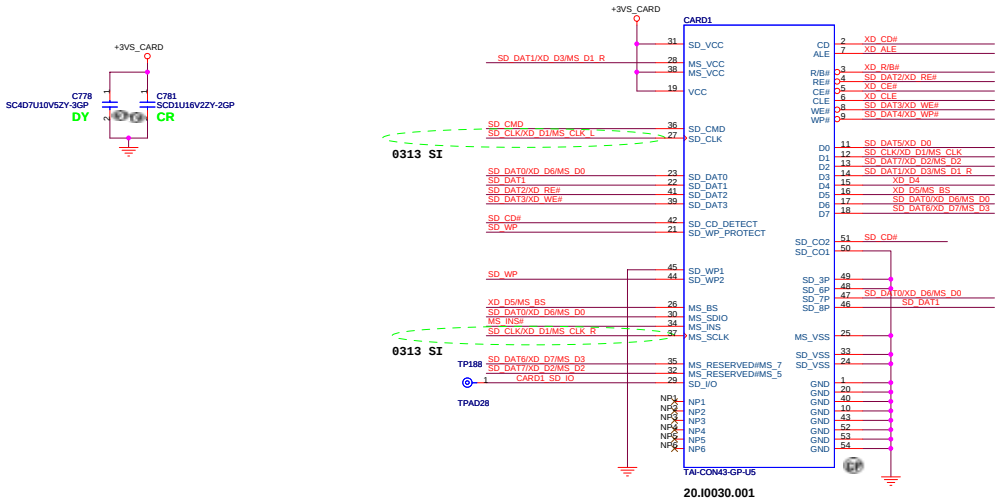
Title: Thermal/Fan Controllor

Size	Document Number	Rev
Custom	VITAS	SA

Date: Monday, May 05, 2008 Sheet 24 of 48



4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Card Reader Controller - RTS5158**

Size	Document Number	Rev
	Warrior	SC

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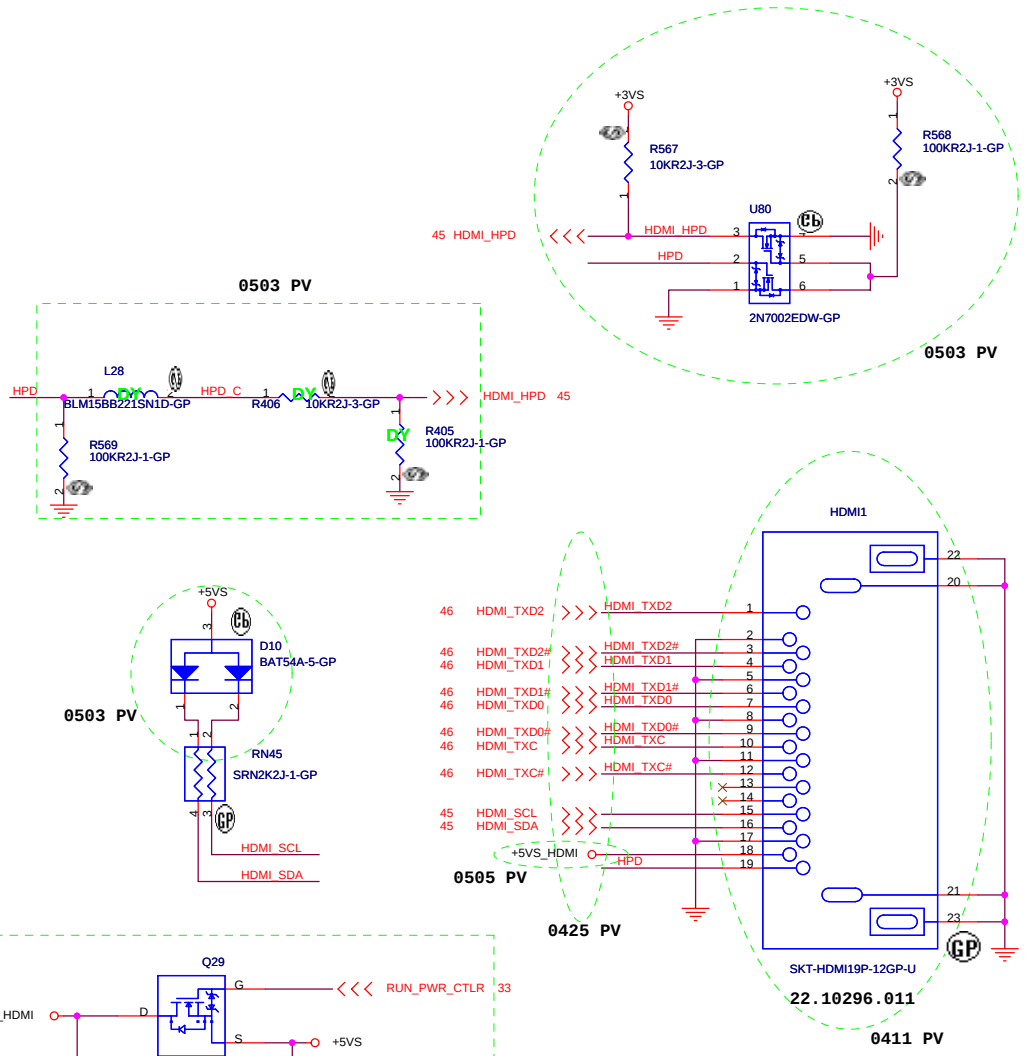
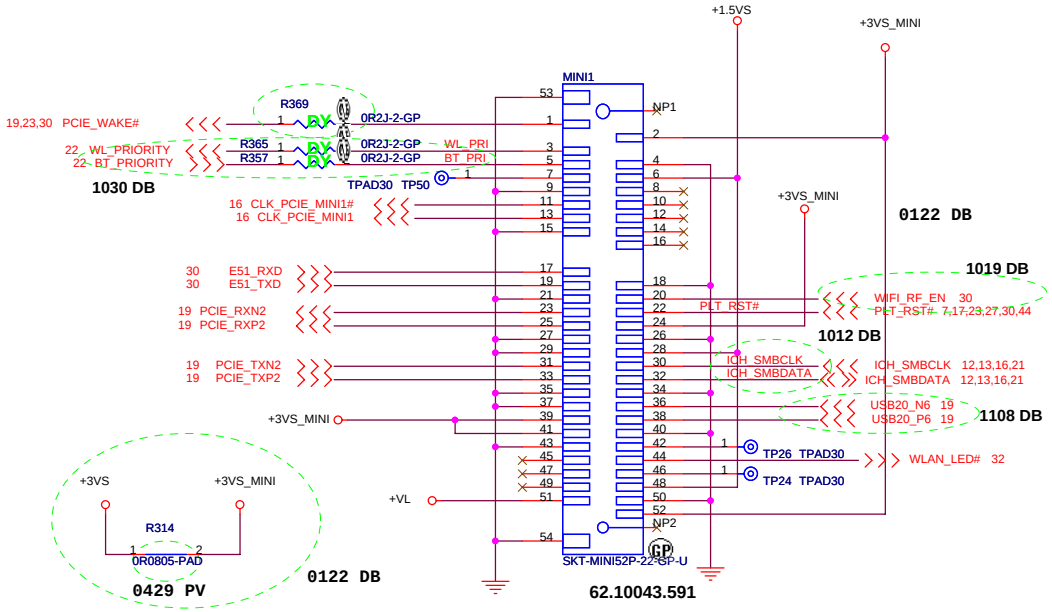
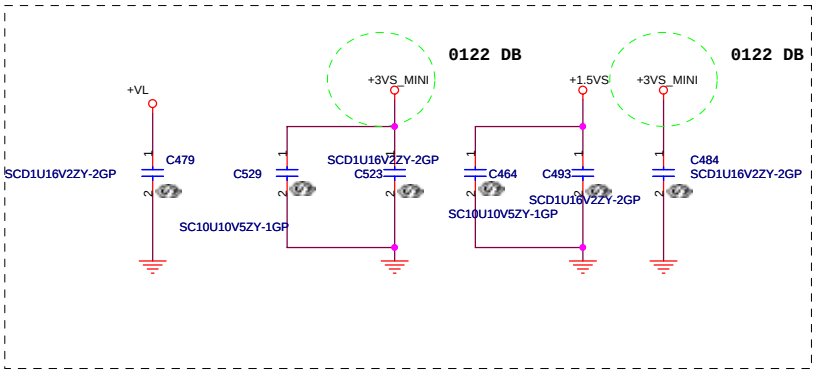
HDMI Connector



Mini Card Connector1(802.11a/b/g)





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD/HDMI CONN .

Size: A3 | Document Number: VITAS | Rev: SA

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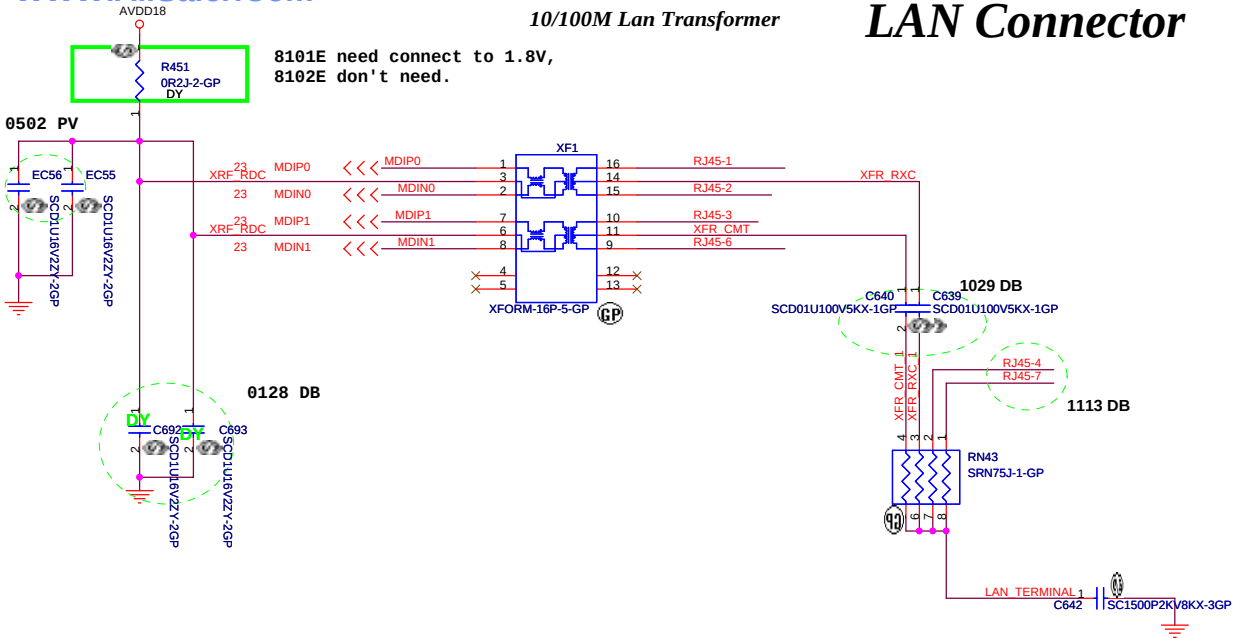
LAN Connector

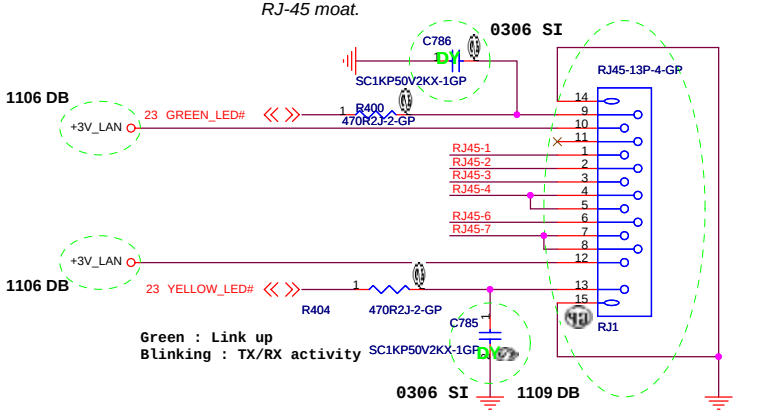
10/100M Lan Transformer

8101E need connect to 1.8V,
8102E don't need.



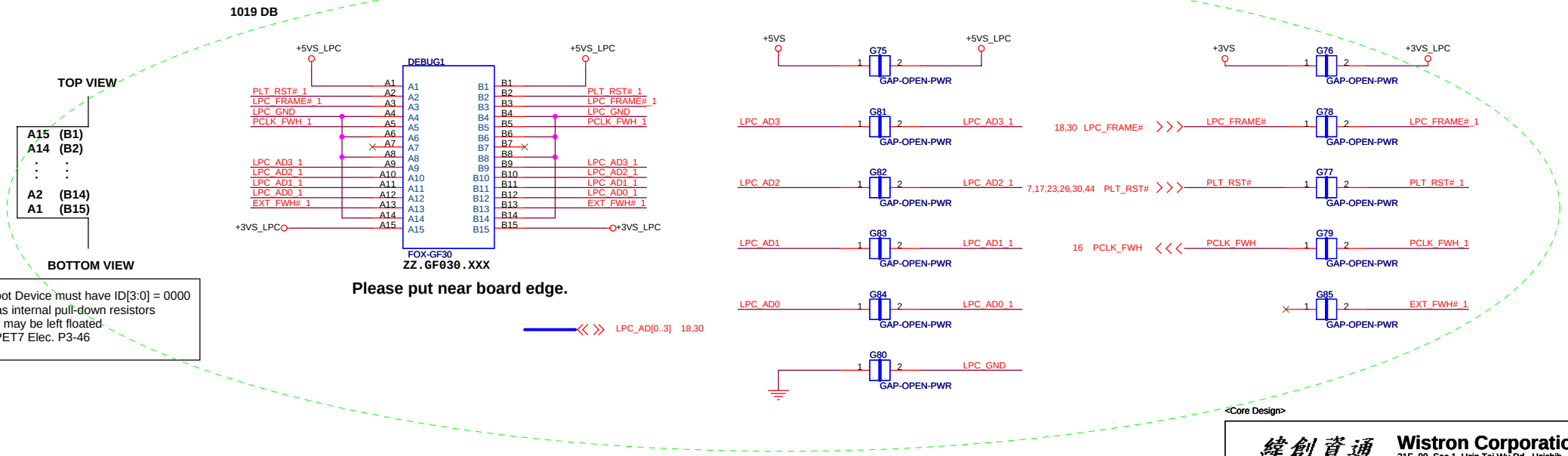
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:
Add trace width to 20mils for RJ1 pin4, 5 and pin 7, 8.

Golden Finger for Debug Board



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

<Core Design>

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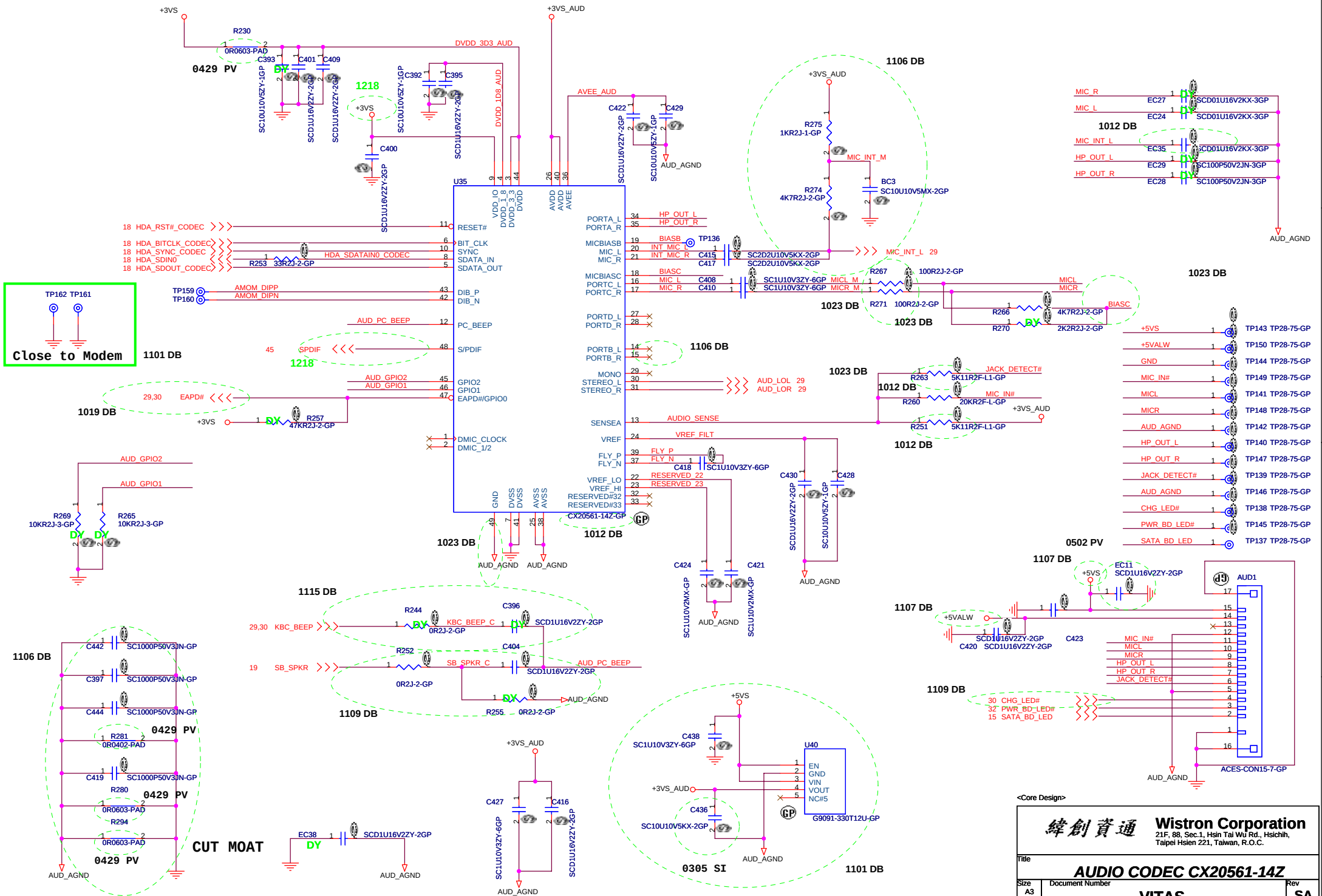
Title	LAN CONN/Debug	
Size A3	Document Number VITAS	Rev SA
Date: Monday, May 05, 2008	Sheet 27 of 48	



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC CX20561-14Z

Size: A3 | Document Number: VITAS | Rev: SA

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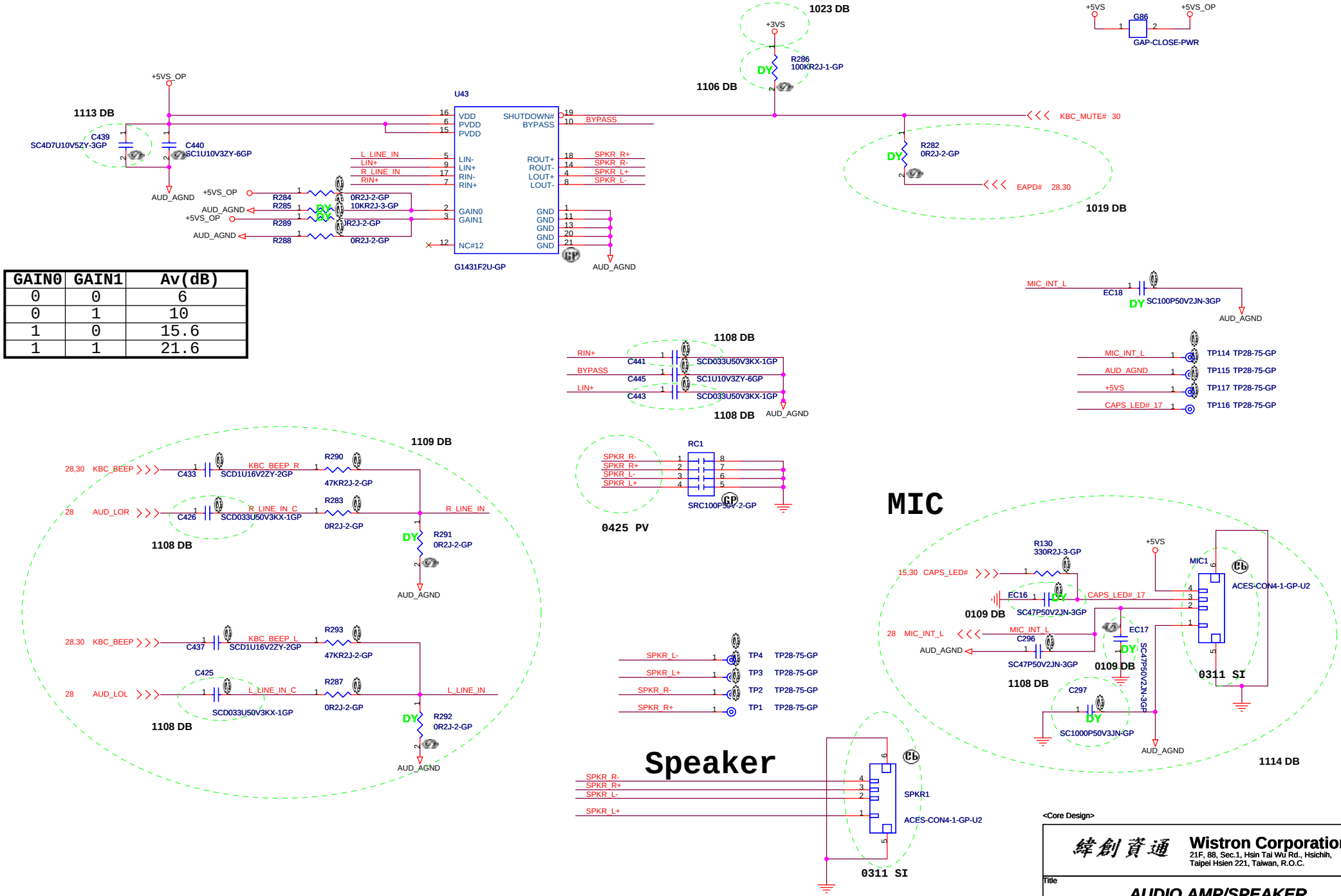

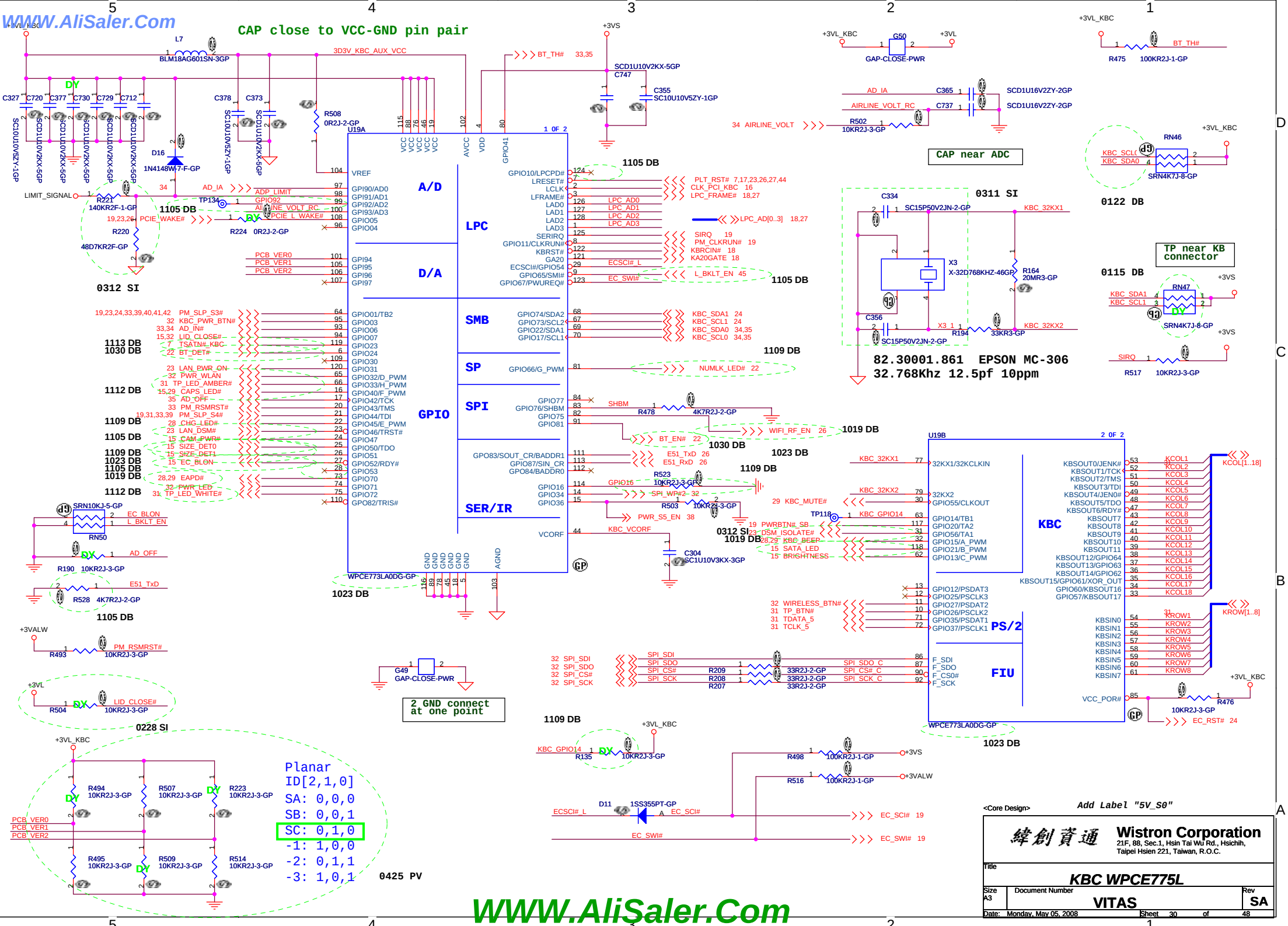

Internal KeyBoard Connector

30 KROW[1..8]
30 KCOL[1..18]

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

KB1 ACES-CON26-GP

1011 DB

1	KROW2	TP113 TP28-75-GP
2	KROW8	TP98 TP28-75-GP
3	KROW7	TP112 TP28-75-GP
4	KCOL10	TP97 TP28-75-GP
5	KROW5	TP111 TP28-75-GP
6	KROW6	TP96 TP28-75-GP
7	KCOL1	TP110 TP28-75-GP
8	KROW3	TP95 TP28-75-GP
9	KROW4	TP109 TP28-75-GP
10	KCOL6	TP94 TP28-75-GP
11	KCOL2	TP108 TP28-75-GP
12	KROW1	TP93 TP28-75-GP
13	KCOL3	TP107 TP28-75-GP
14	KCOL5	TP92 TP28-75-GP
15	KCOL8	TP106 TP28-75-GP
16	KCOL9	TP91 TP28-75-GP
17	KCOL7	TP105 TP28-75-GP
18	KCOL4	TP90 TP28-75-GP
19	KCOL13	TP104 TP28-75-GP
20	KCOL14	TP89 TP28-75-GP
21	KCOL15	TP103 TP28-75-GP
22	KCOL12	TP88 TP28-75-GP
23	KCOL11	TP102 TP28-75-GP
24	KCOL16	TP87 TP28-75-GP
25	KCOL17	TP101 TP28-75-GP
26	KCOL18	TP86 TP28-75-GP

Change to 20.K0545.026

0310 SI

D7 BAV99W-1-GP
TP_ON/OFF
+3VS
DY

GND TP99 TP28-75-GP
GND TP100 TP28-75-GP

1108 DB
+5V_TP
C233 SCD1U16V2ZY-2GP
D8 BAV99S-GP
TCLK_5
TDATA_5
0408 PV

0228 SI

+5V_TP	TP83 TP28-75-GP
TDATA_5	TP77 TP28-75-GP
TCLK_5	TP76 TP28-75-GP
GND	TP78 TP28-75-GP
TP_LED_AMBER#	TP81 TP28-75-GP
TP_LED_WHITE#	TP75 TP28-75-GP
GND	TP84 TP28-75-GP
TP_ON/OFF	TP80 TP28-75-GP
+5VS	TP79 TP28-75-GP
GND	TP82 TP28-75-GP

Please populate close TPAD1

TouchPad Connector

1107 DB
+5V_TP +5V_TP
C253 SC1U10V3ZY-6GP
C258 SCD1U16V2ZY-2GP
RN25 SRN10KJ-11-GP-U
C221 SC33P50V2JN-3GP
C220 SC33P50V2JN-3GP
TPAD1 ACES-CON10-11-GP
TDATA_5 30
TCLK_5 30
TP_LED_AMBER# 30
TP_LED_WHITE# 30
TP_ON/OFF
+5VS
EC14 SCD1U16V2ZY-2GP
0228 SI

1112 DB
+3VS
R67 10KR2J-3-GP
100R2J-2-GP R85
TP_BTN# 30
C343 SC1000P50V3JN-GP
DY

R437 0R3-0-U-GP
+5VALW
R408 100KR2J-1-GP
C649 SCU10V3KX-3GP
R425 100KR2J-1-GP
Q20 AO3403-GP
C672 SCD1U16V2KX-3GP
TP_SLP_S4_C
TP_SLP_S4
R411 10KR2J-3-GP
C674 SCD1U16V2KX-3GP
Q19 2N7002E-1-GP
19,30,33,39 PM_SLP_S4#
1109 DB
1112 DB

RC4 SRC100P50V-2-GP KCOL9 KCOL8 KCOL5 KCOL3
RC5 SRC100P50V-2-GP KROW1 KCOL2 KCOL6 KROW4
RC2 SRC100P50V-2-GP KCOL16 KCOL11 KCOL12 KCOL15
RC3 SRC100P50V-2-GP KCOL14 KCOL13 KCOL4 KCOL7
for EMI
RC7 SRC100P50V-2-GP KCOL10 KROW7 KROW8 KROW2
RC6 SRC100P50V-2-GP KROW3 KCOL1 KROW6 KROW5
for EMI

0408 PV

<Core Design>

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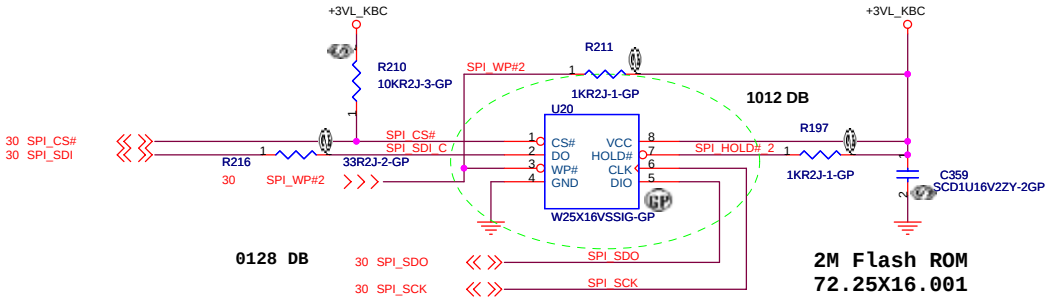
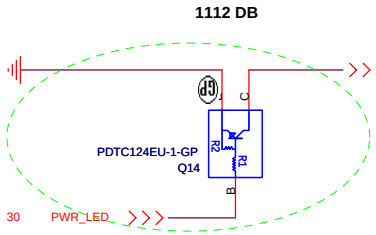
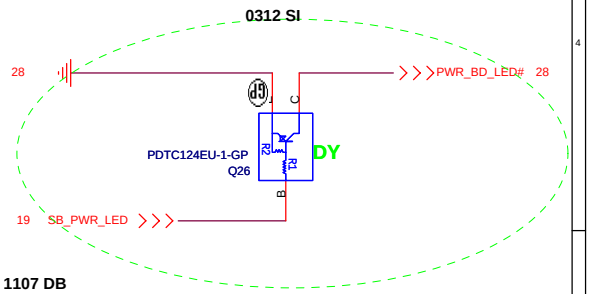
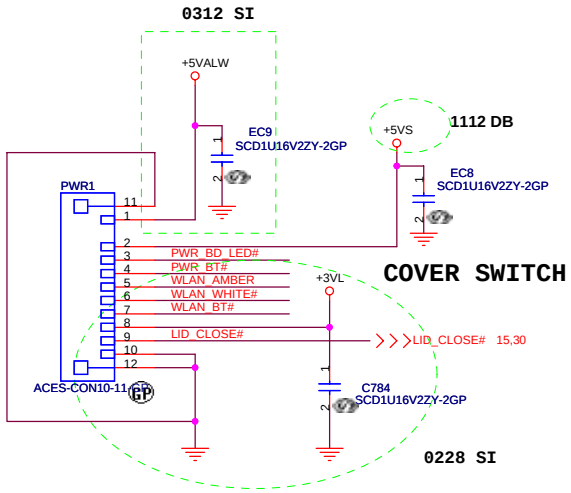
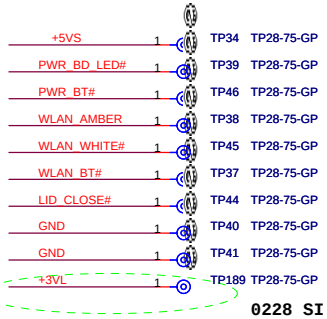
Title: KeyBoard-CONN
Size: A3
Document Number: VITAS
Rev: SA
Date: Monday, May 05, 2008
Sheet 31 of 48

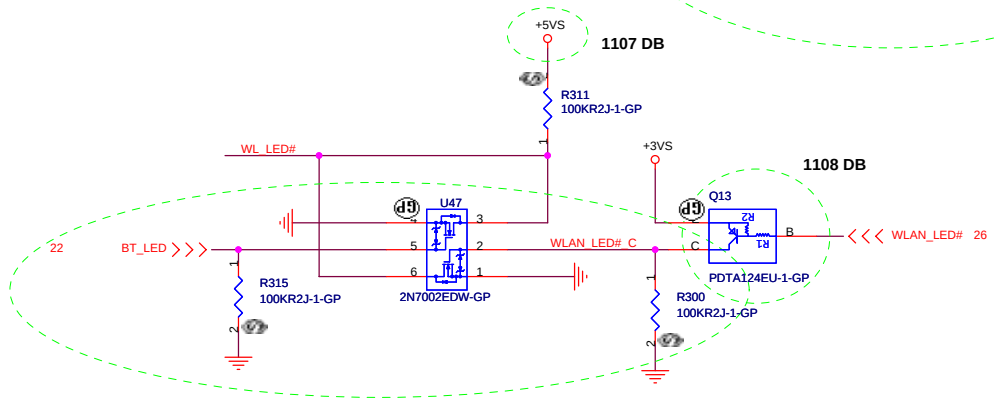


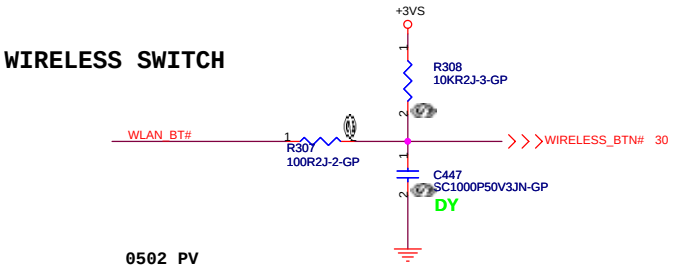


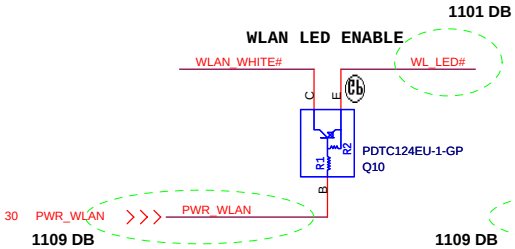


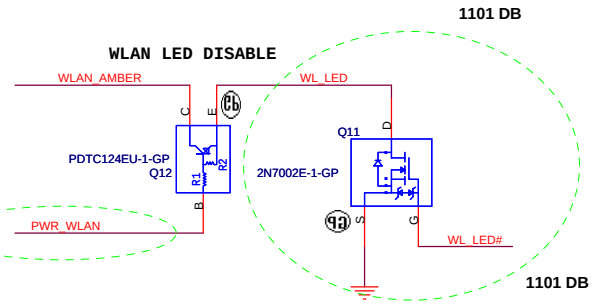


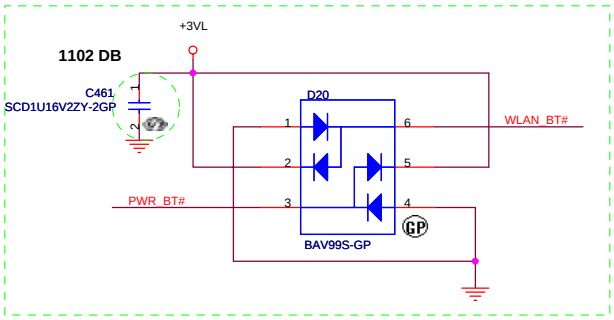


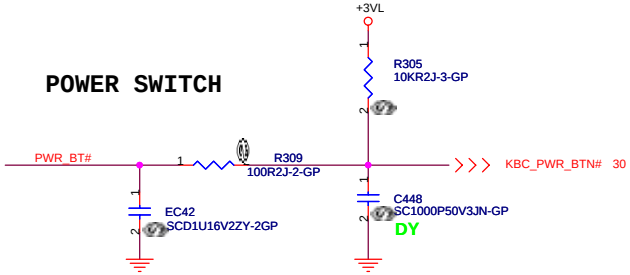












<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***FWH and CONN.***
Size: A3	Document Number: **VITAS**
Rev:	**SA**
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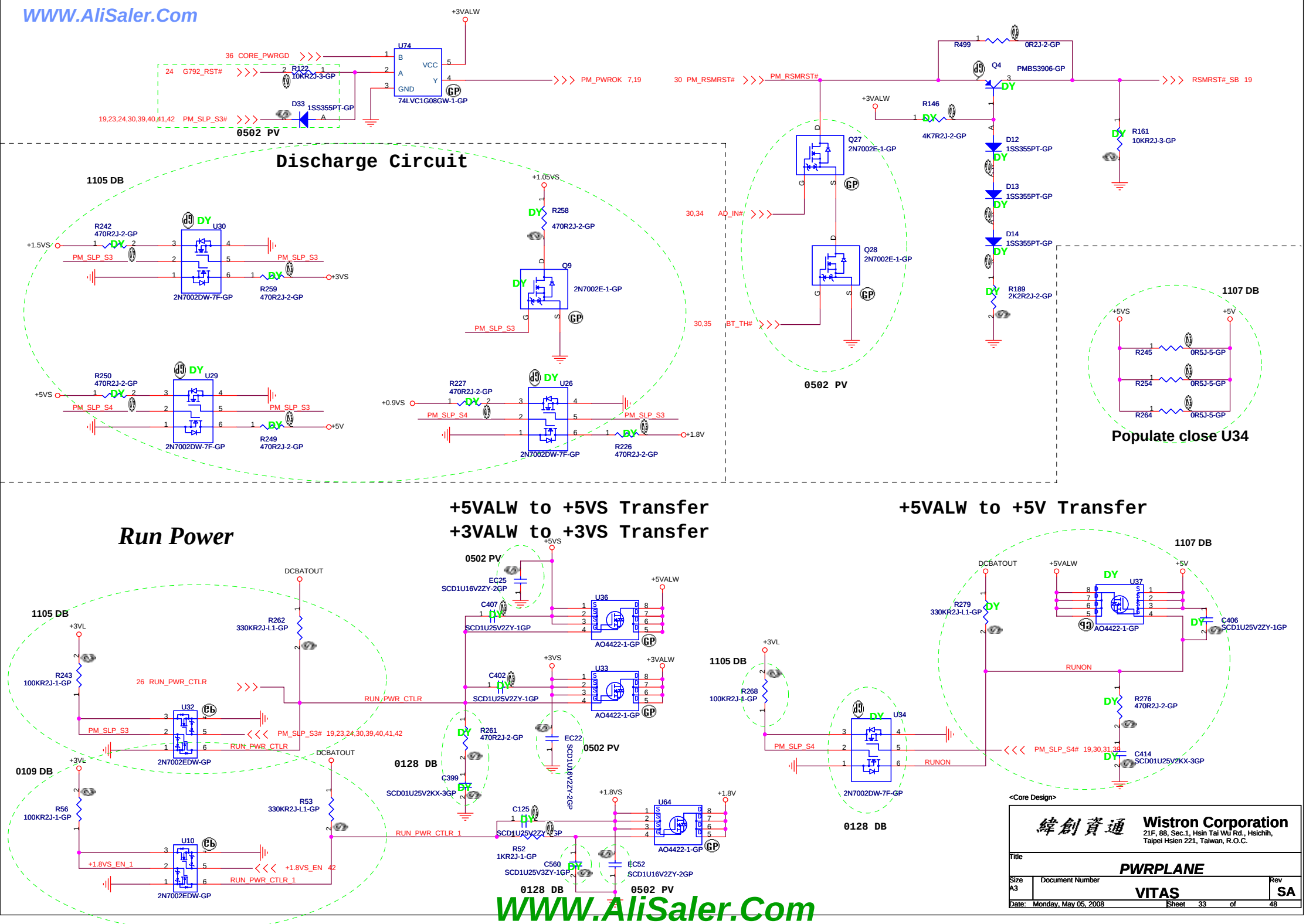
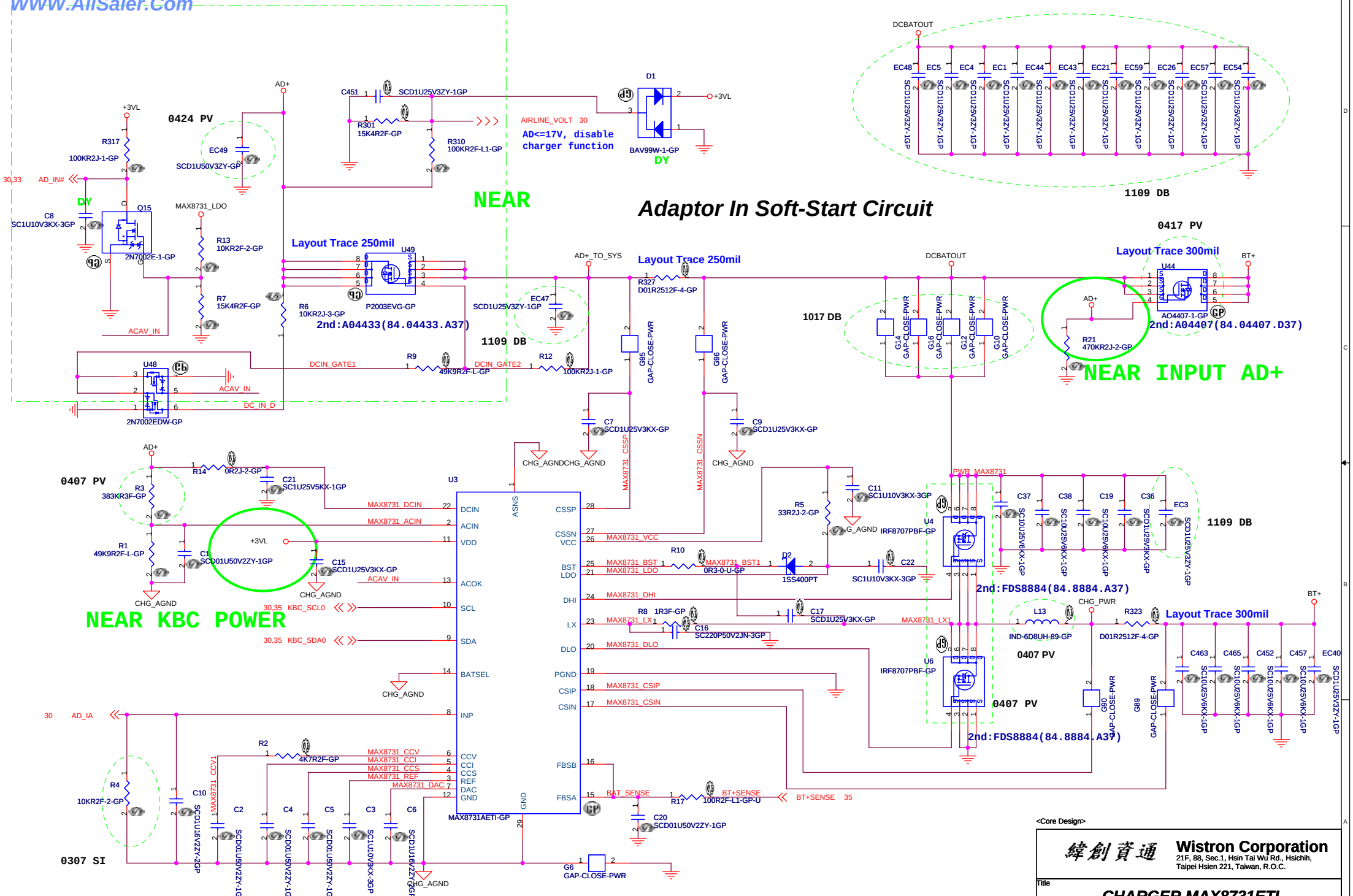


Adaptor In Soft-Start Circuit



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Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731ETI

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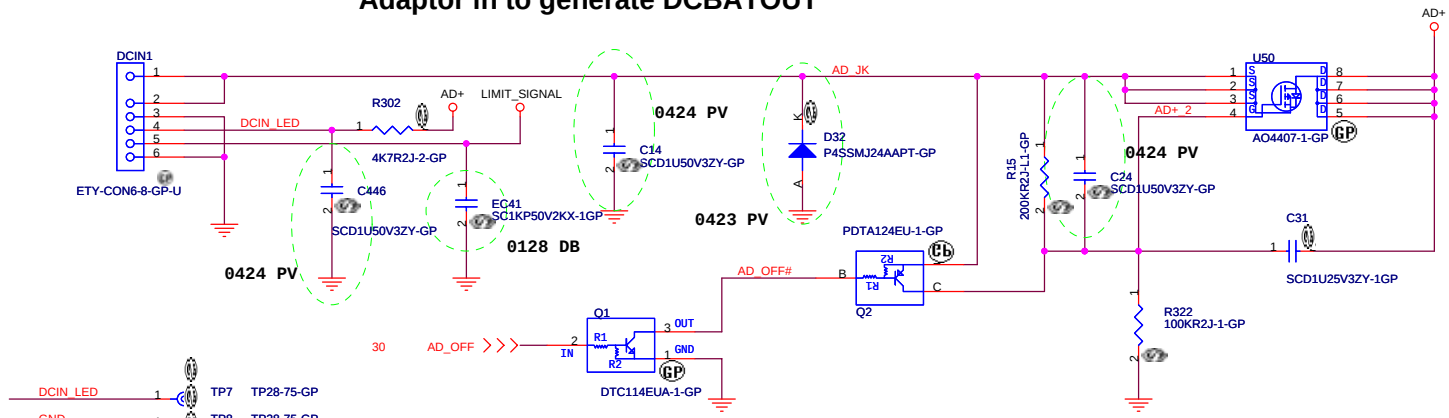
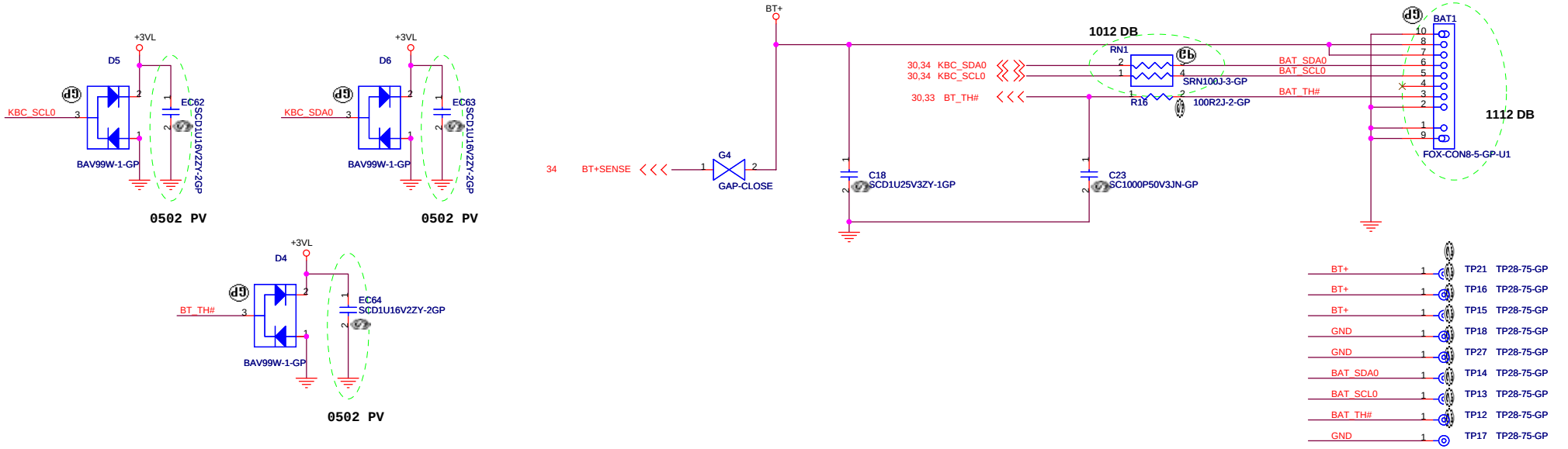
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number VITAS	Rev SA
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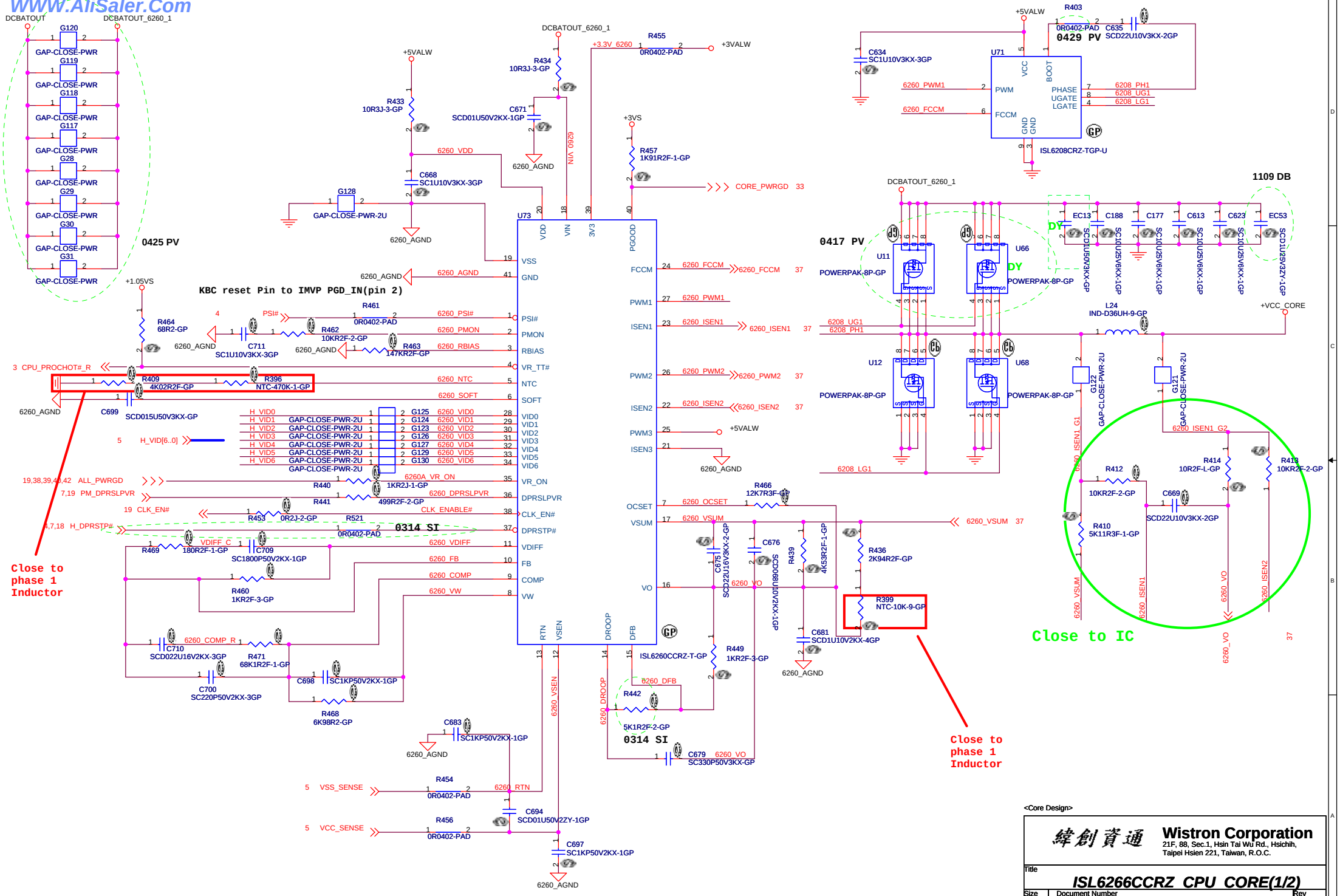


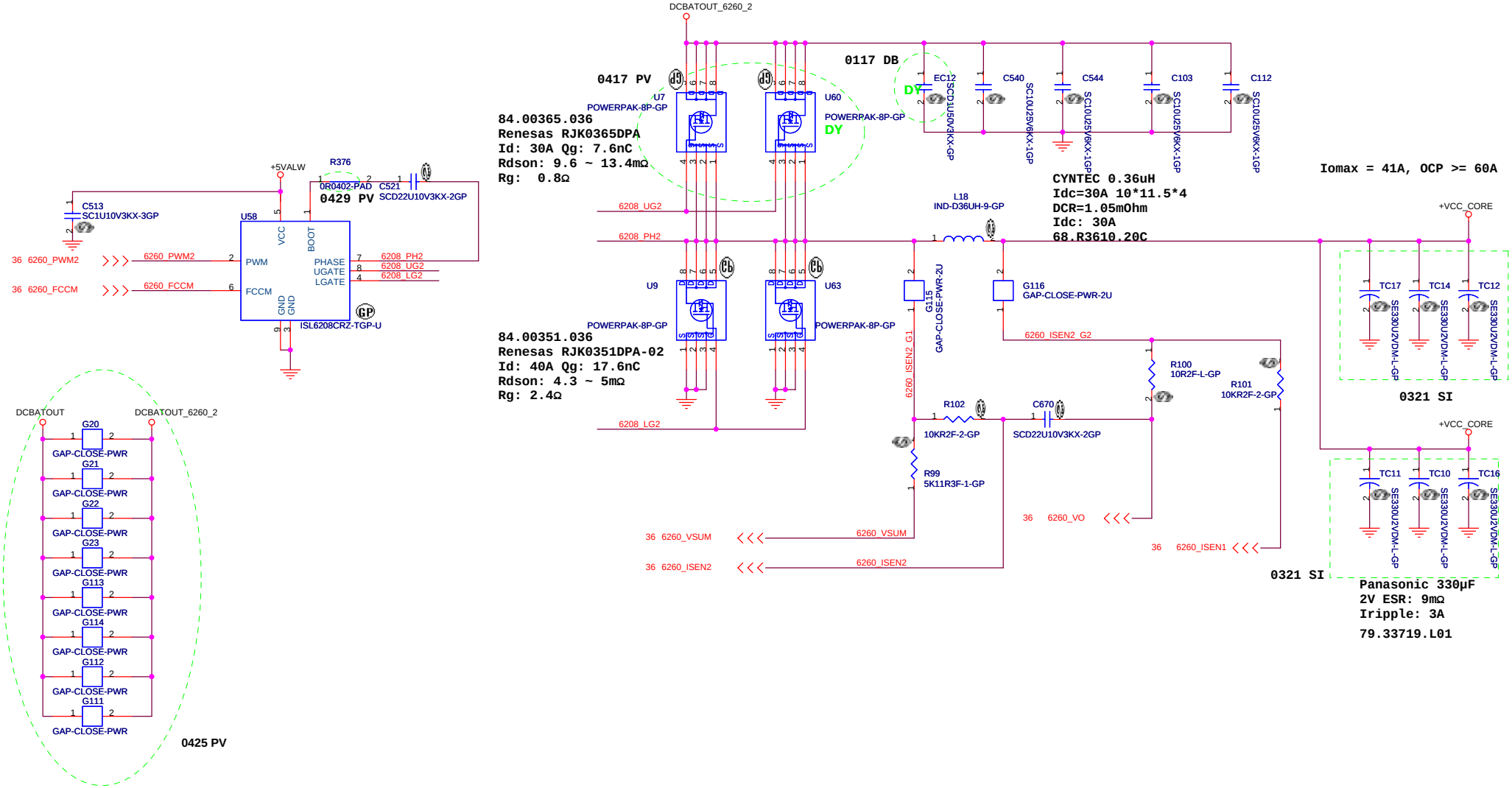
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6266CCRZ CPU CORE(1/2)

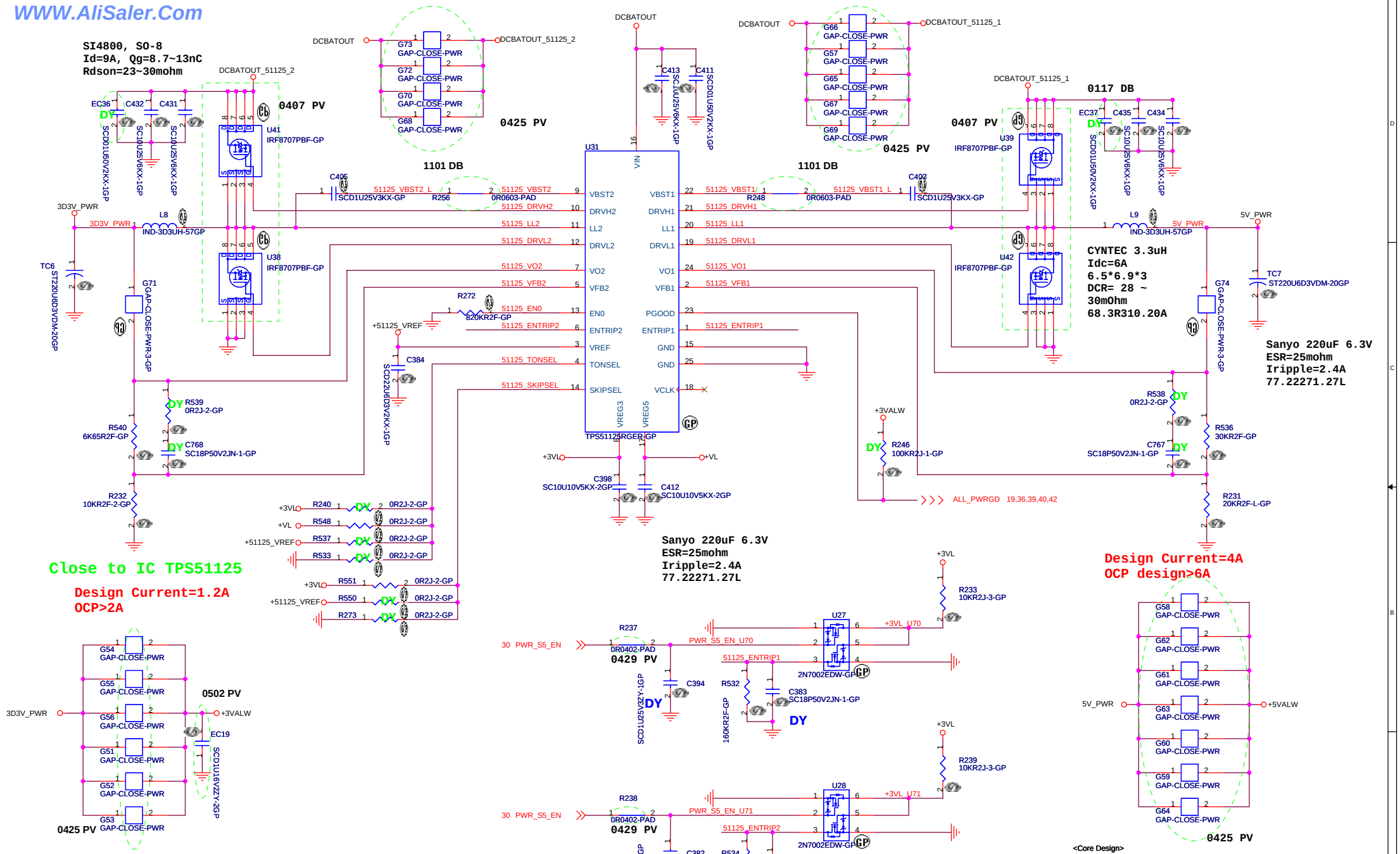
Size: A3 | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 36 of 48



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*ISL6260CCRZ CPU CORE(2/2)*
Size A3	Document Number: VITAS — Rev: SA
Date: Monday, May 05, 2008	Sheet 37 of 48



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	**00A AUTOSKIP**	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	**300k/CH1** **375k/CH2**	365k/CH1 460k/CH2

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPA51125 +5VALW +3VALW

Size: A3 | Document Number: VITAS | Rev: SA

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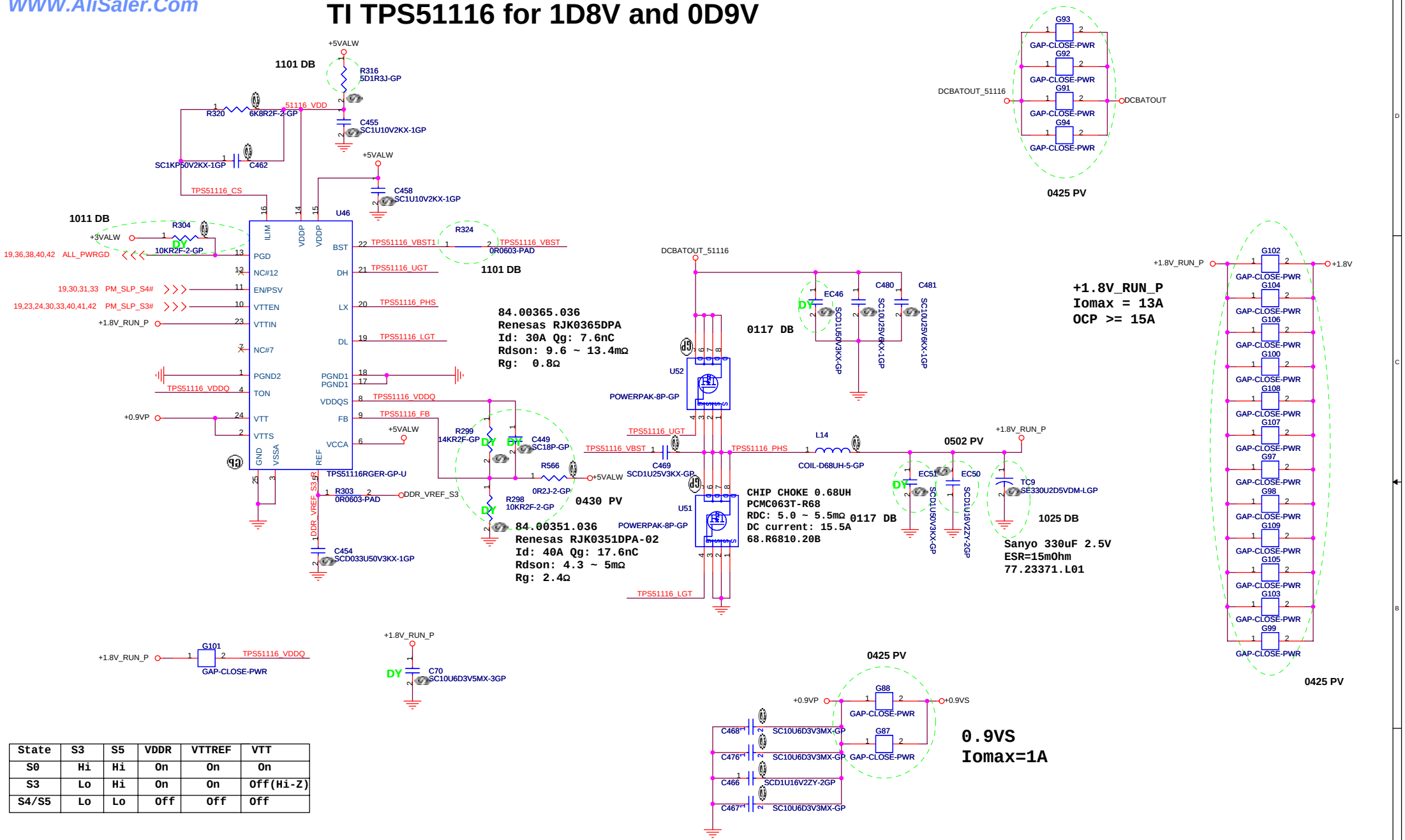
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: VITAS | Rev: SA

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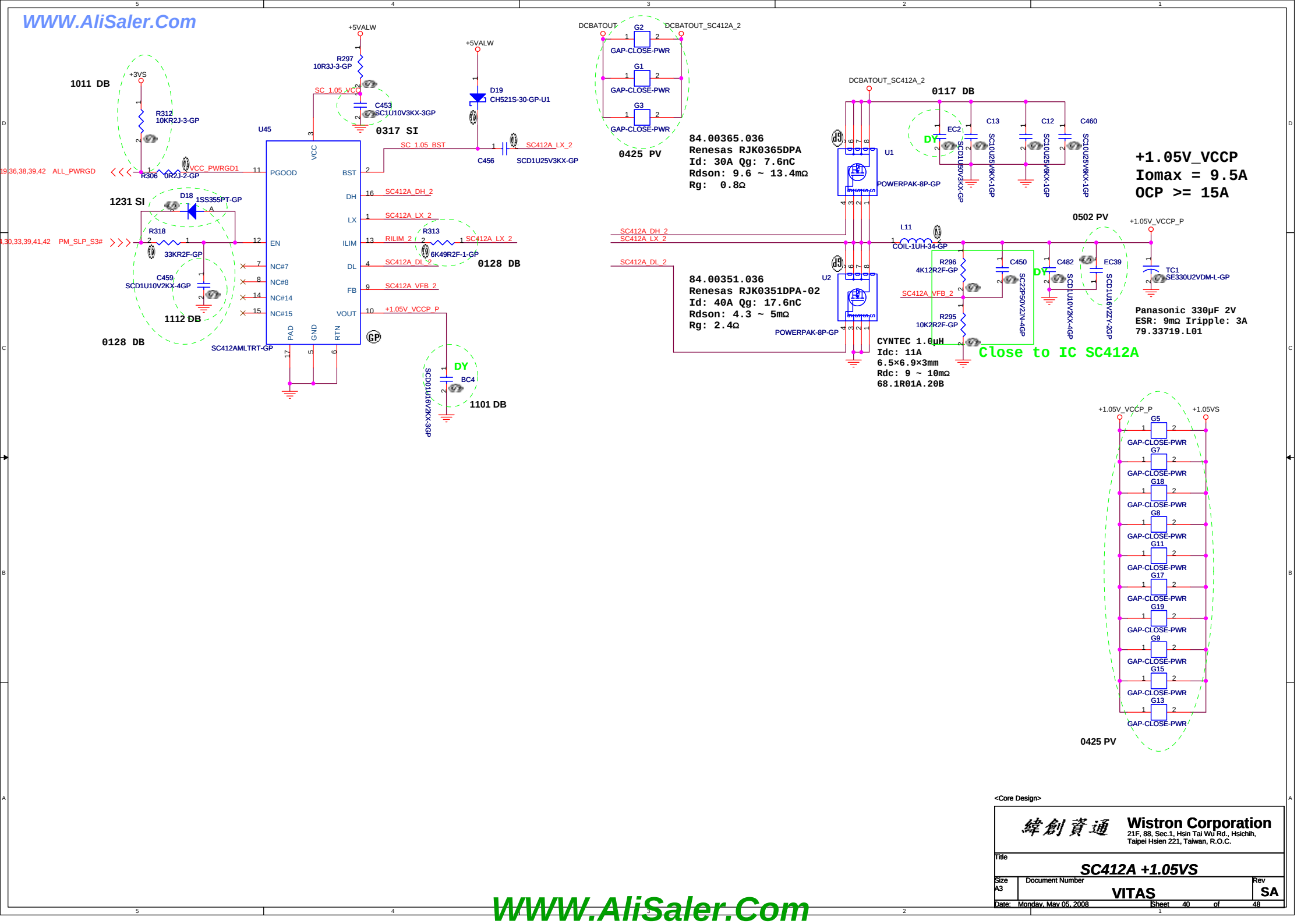

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC412A +1.05VS

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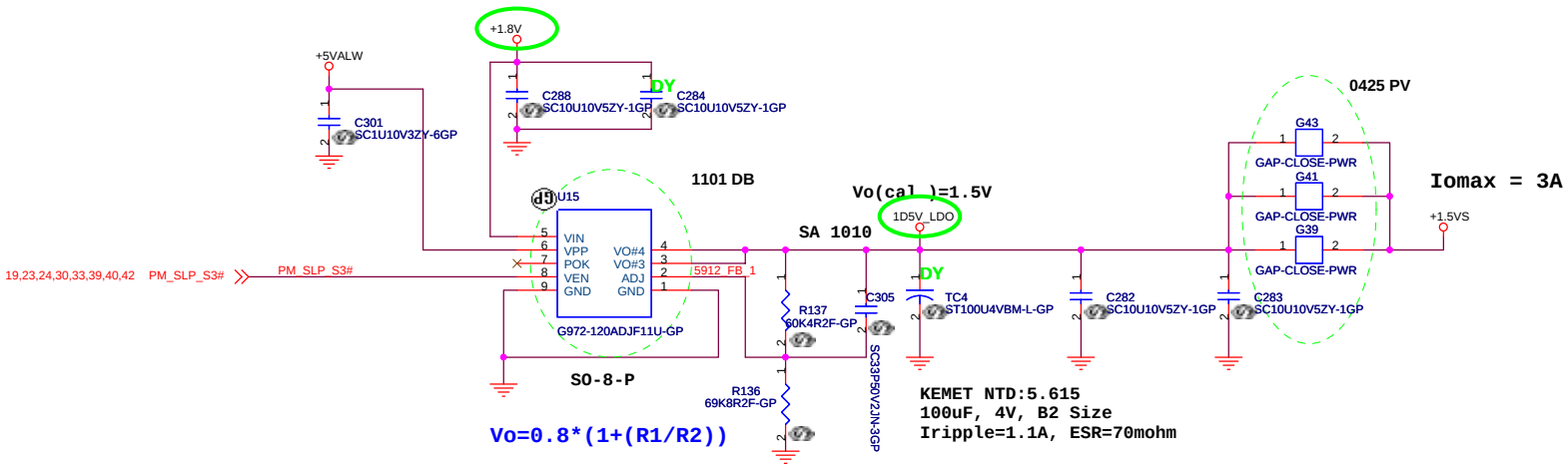

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMT 1D5V LDO

Size	Document Number	Rev
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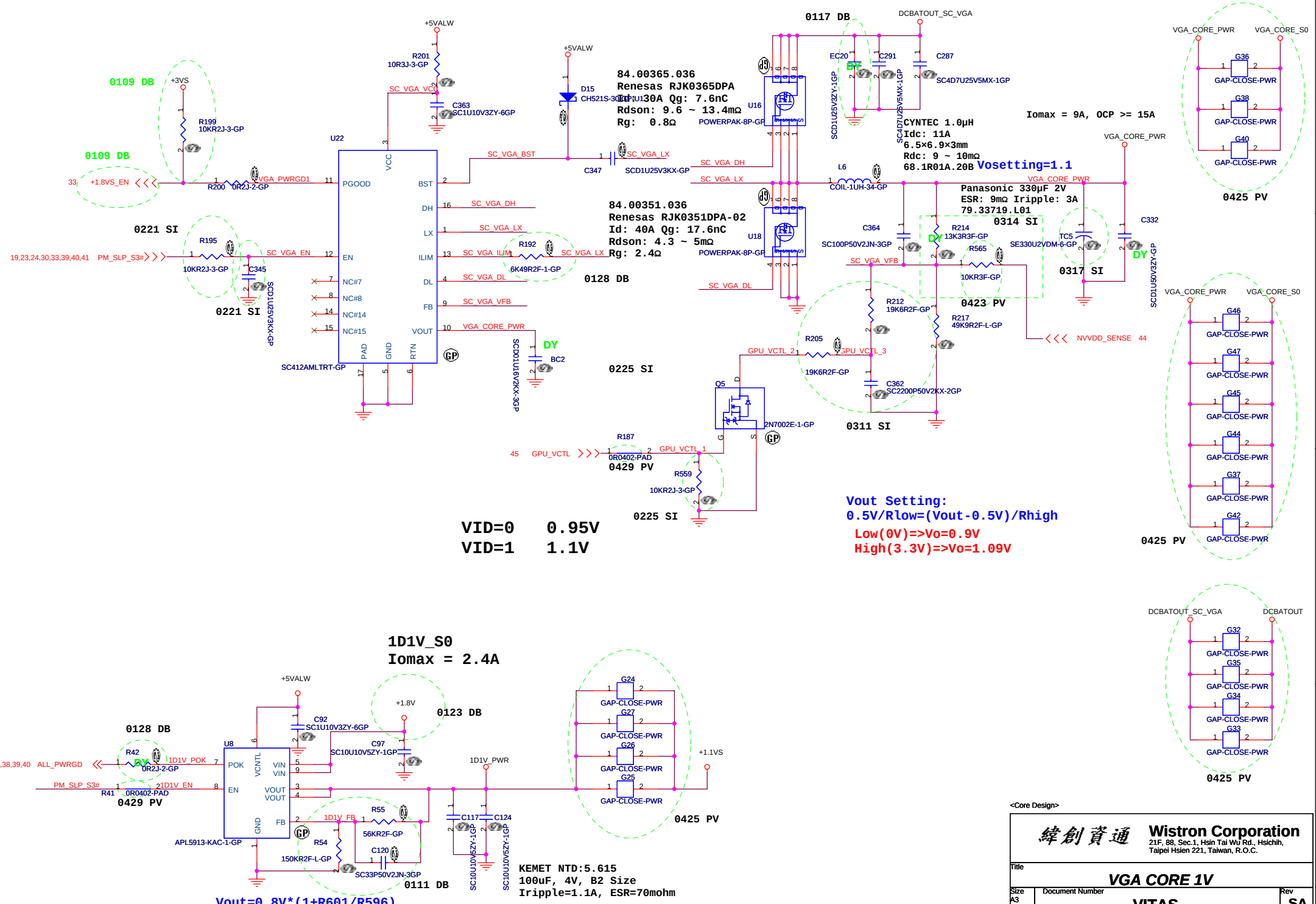

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA CORE 1V

Size	Document Number	Rev
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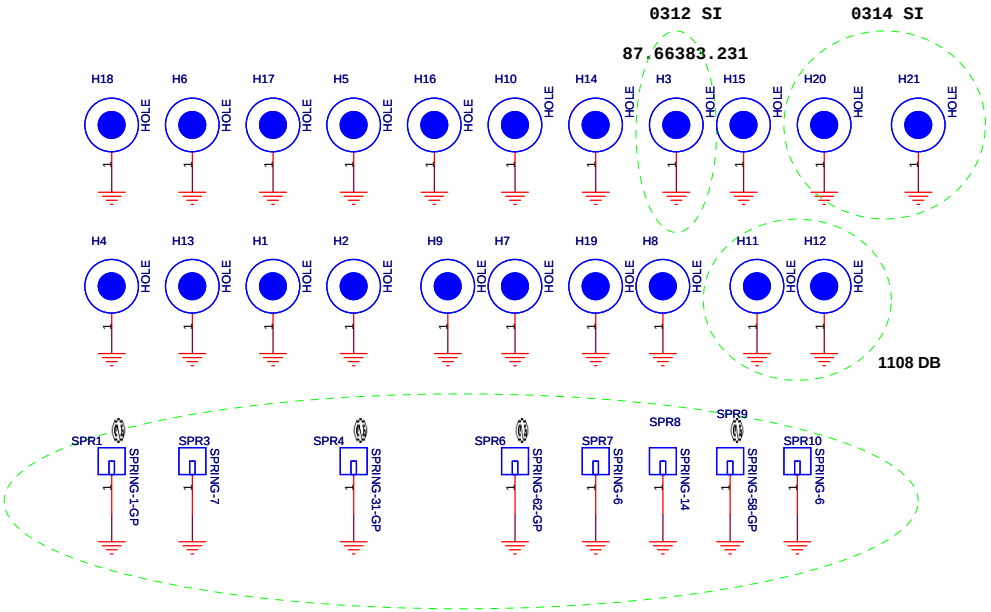

SPR1	34.40V16.001
SPR3	34.49U26.001
SPR4	34.49U24.001
SPR6	34.39S07.003
SPR7	34.13B01.001
SPR8	34.41V01.001
SPR9	34.4B312.002
SPR10	34.13B01.001

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC

Size: A3 | Document Number: VITAS | Rev: SA

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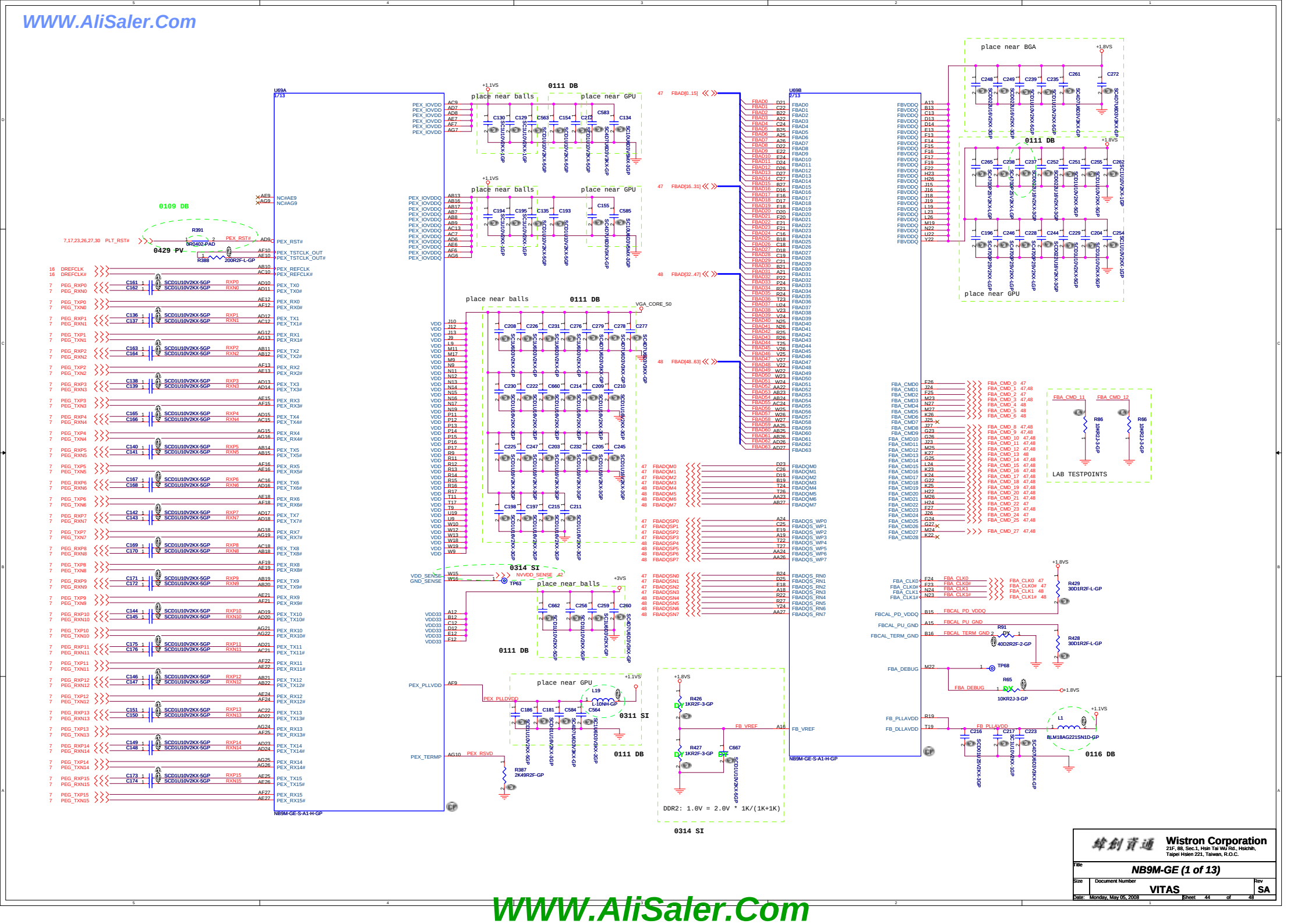

Title: NB9M-GE (1 of 13)

Size: | Document Number: VITAS | Rev: SA

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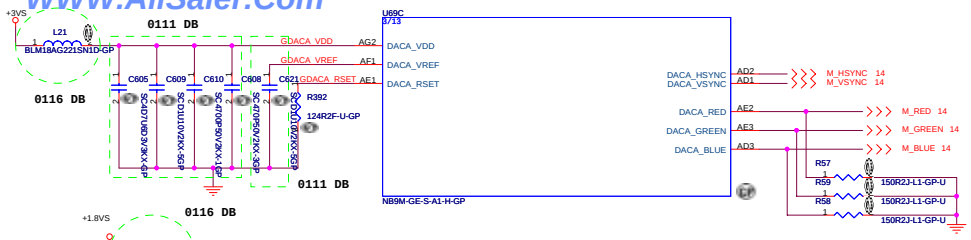

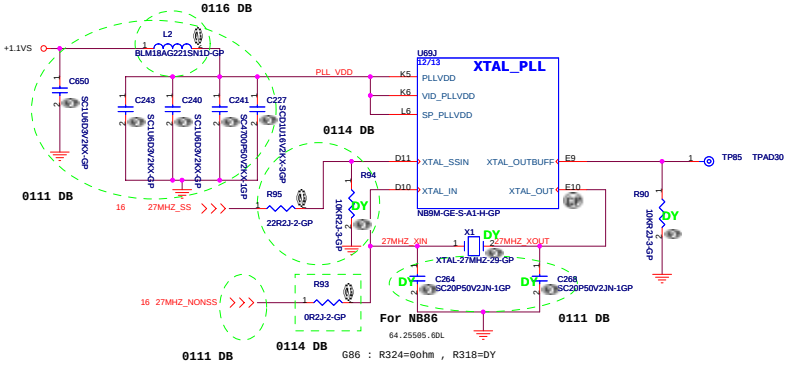

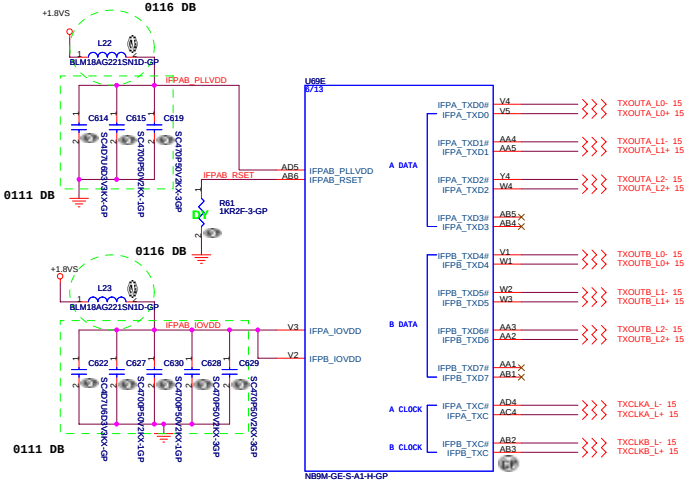

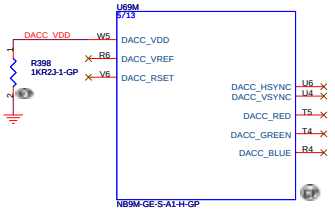

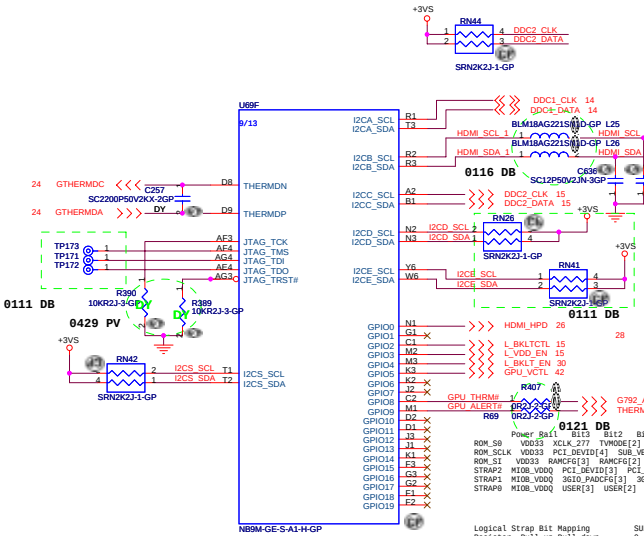

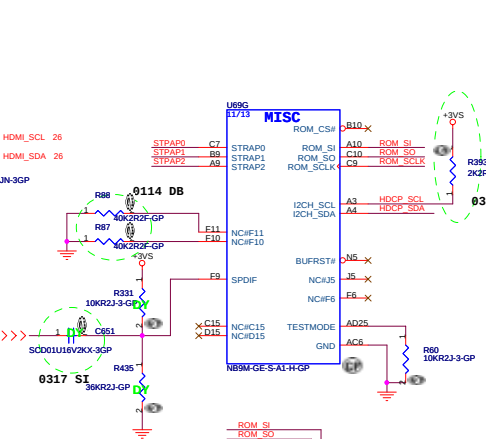

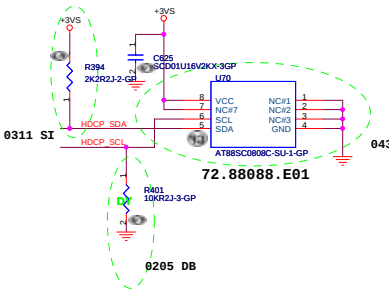

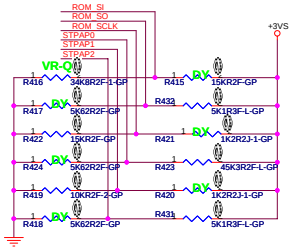

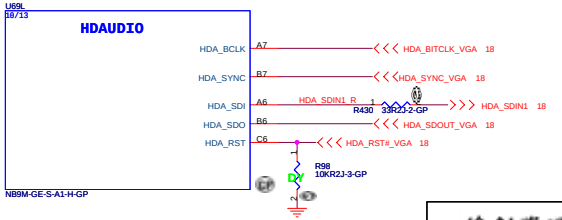

0121 DB

Power Rail	Bit3	Bit2	Bit1	Bit0
ROM_S0	VDD33	XCLK_277	TVMODE[2]	TVMODE[0]
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCCFG[1]
STRAP2	MIOB_VDDQ	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]
STRAP1	MIOB_VDDQ	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP0	MIOB_VDDQ	USER[3]	USER[2]	USER[1]

NB9M-GE	NB9M-GE	NB9M-GE
0x06E8	0x06E8	0x06E8
256MB	256MB	256MB
32M16 DDR2	32M16 DDR2	32M16 DDR2
K4N51163QG-HC25	HYB18TS12161B2F-25	HY5PS121621CFP-25
Samsung	Qimonda	Hynix
ROM_SI 0101	0110	0111

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

SUB_VENDOR
0 No VBIOS ROM
1 BIOS ROM present

XCLK_277
0 Reserved
1 27MHz(POR)

USER[3:0]
1111 Use EDID to detect panel settings

PLL Termination Settings
PEX_PLL_EN_TERM
0 Disable (POR)
1 Enable

3GIO_PADCFG
0000 Desktop
0001 Notebook (POR)

SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

蜂創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	NB9M-GE (2 of 3)
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Rev	SA
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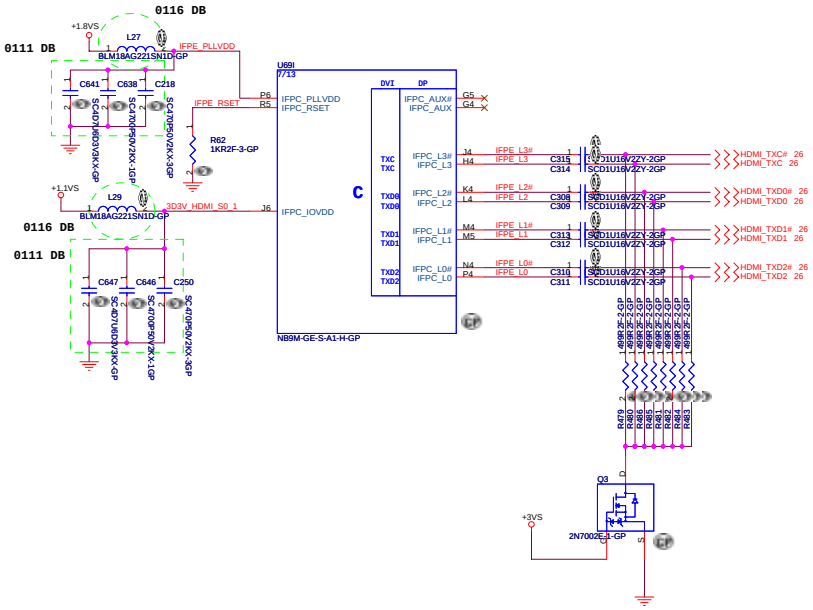
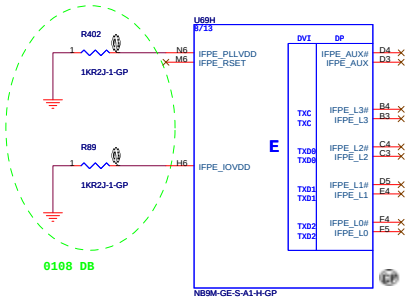
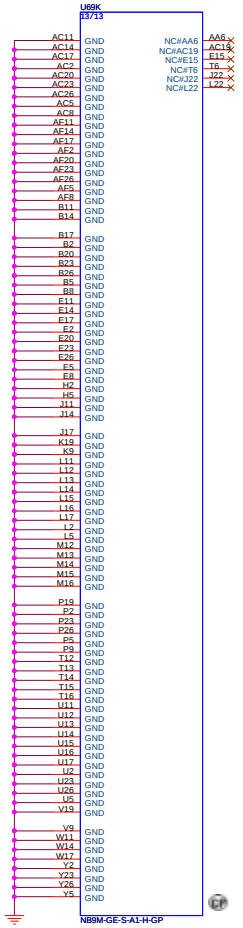
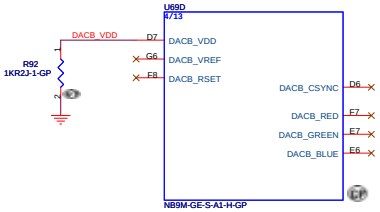
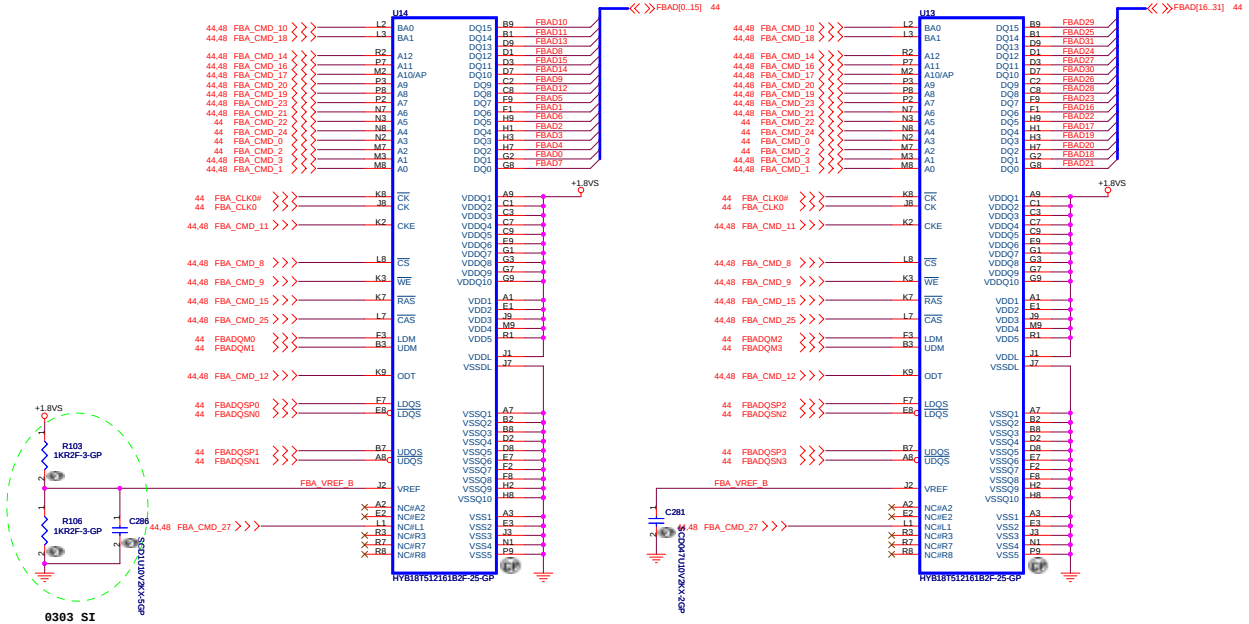








緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	NB9M-GE (3 of 3)		
Size	Document Number	Rev	
	VITAS	SA	
Date: Monday, May 05, 2008	Sheet 46 of 48		



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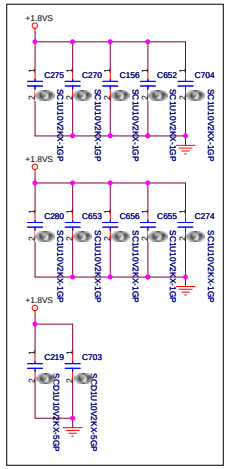
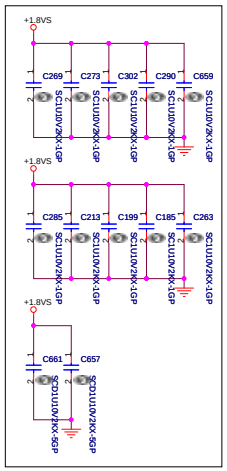
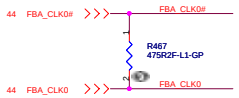
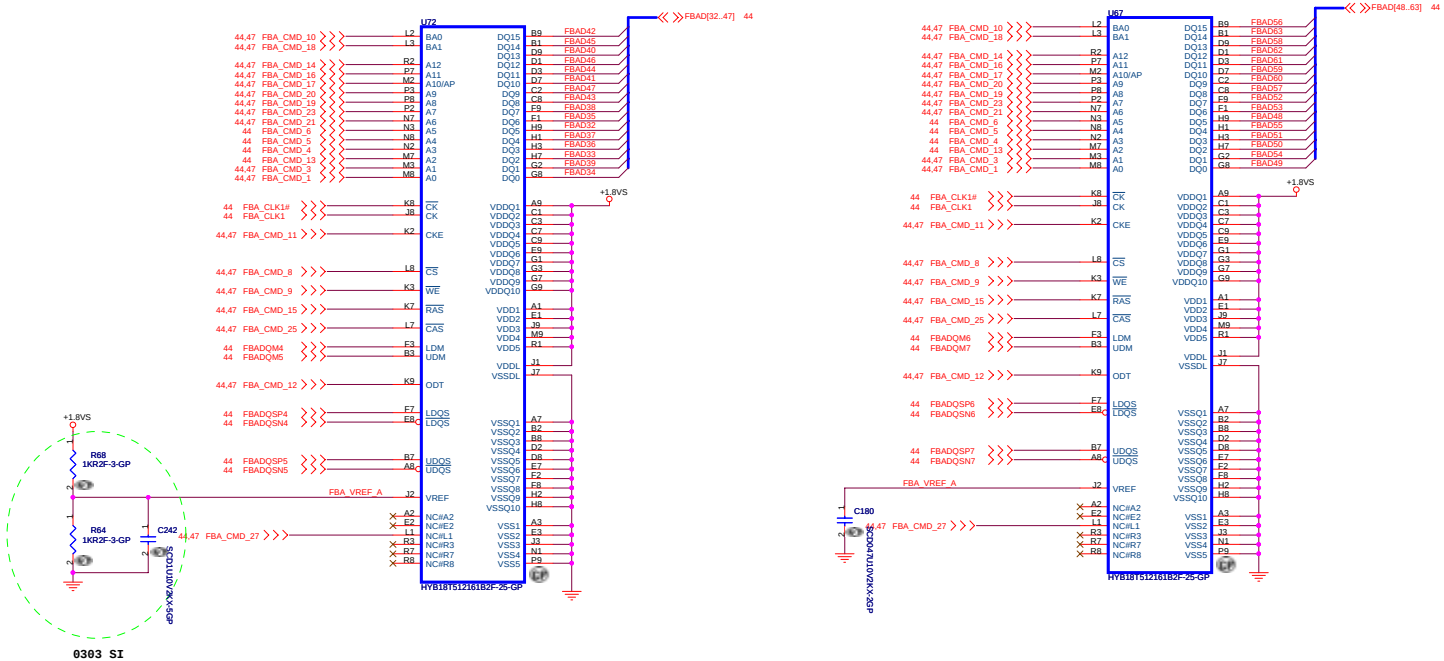


X - cap for CMD

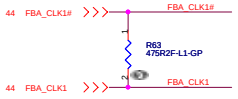




緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM1		
Size	Document Number: VITAS	Rev: SA
Date: Monday, May 05, 2008	Sheet 47 of 48	



0303 SI



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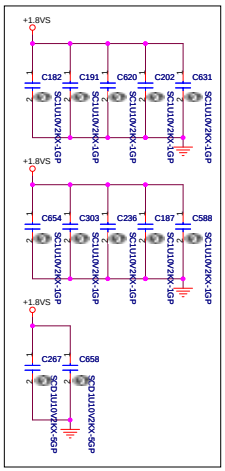
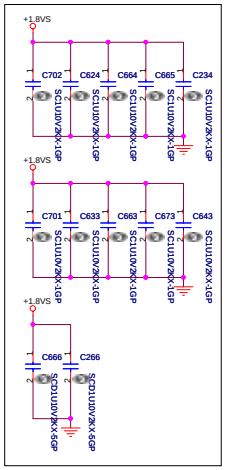


X - cap for CMD



緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM2		
Size	Document Number: VITAS	Rev: SA
Date: Monday, May 05, 2008	Sheet 48 of 48	