

Compal confidential

Schematics Document

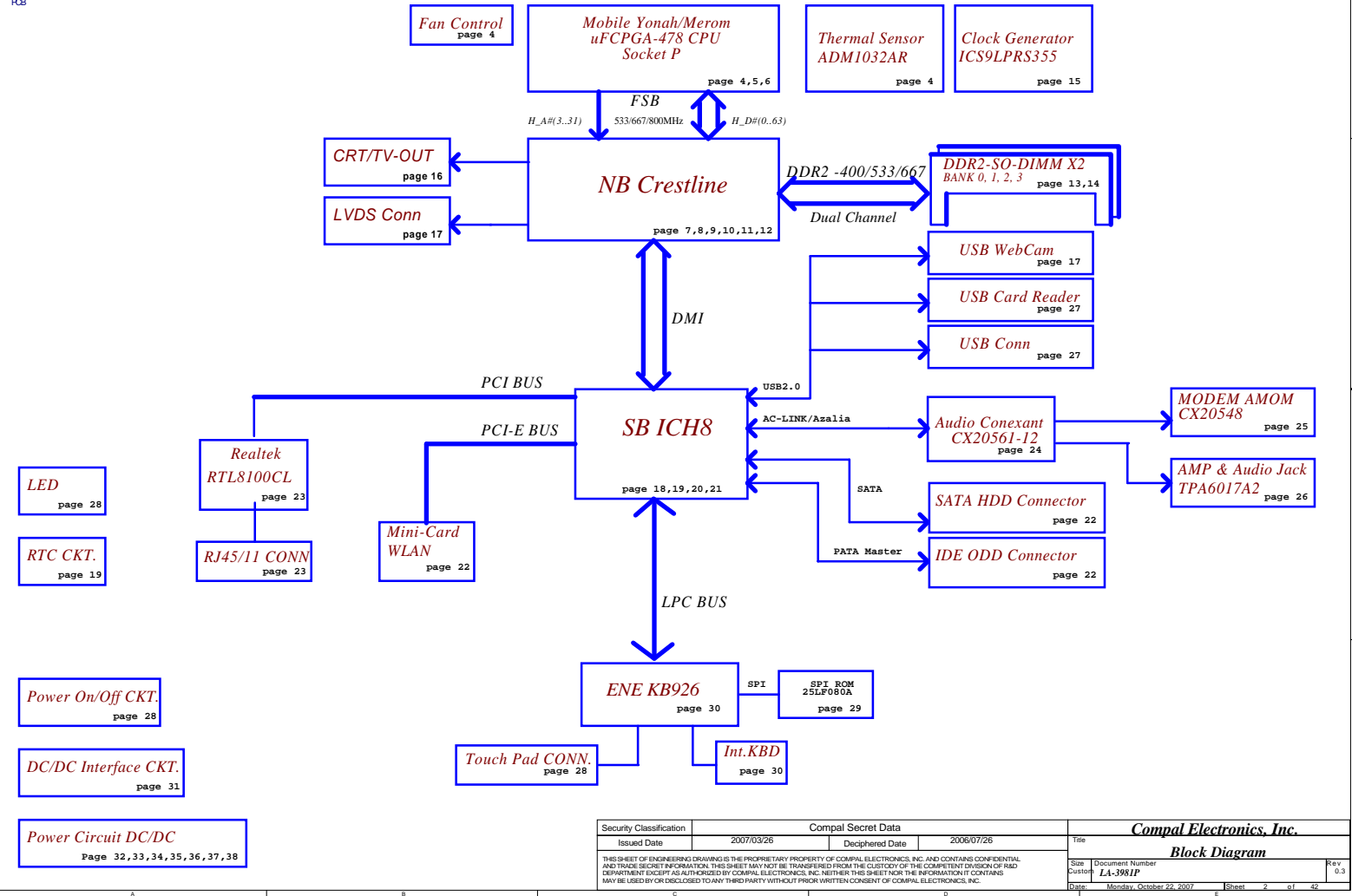
Mobile Merom uFCPGA with Satna Rosa Platform

2007-08-02
REV:0.2

Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	
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LEON 1.0 (Merom +Crestline+ICH8)

ZZZ1
PCB



Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

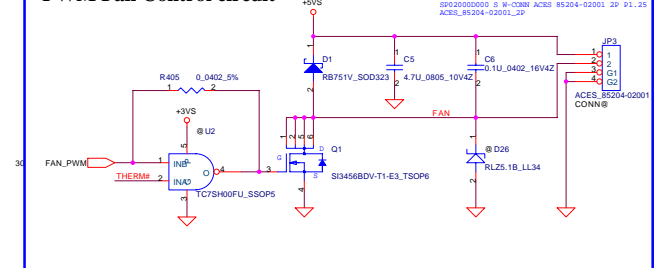
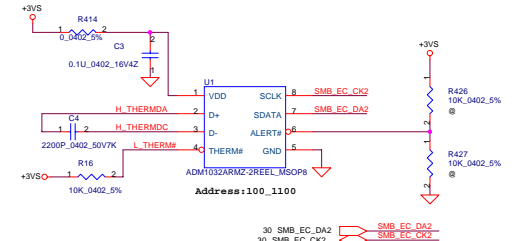
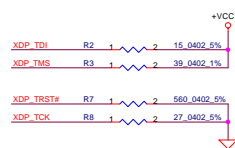
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43151732L01(965GM) & 443151732L02(960GML) with card reader

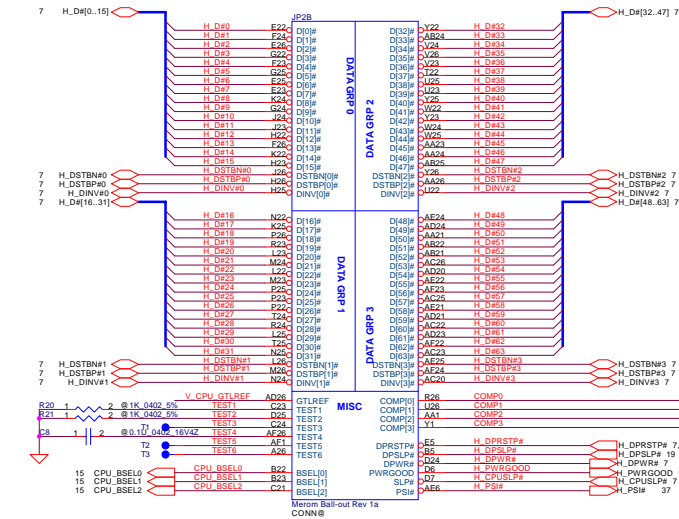
BOM: 43151732L03(965GM) & 43151732L04(960GML) without card reader

Jump-Short: PJP?

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				Size	Document Number	Rev
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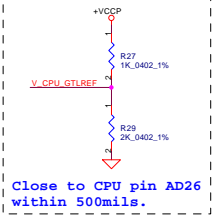


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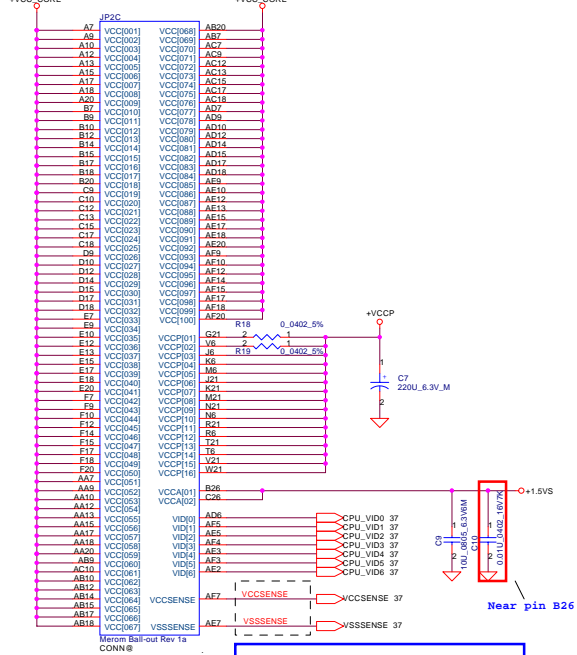


layout note: Route TEST3 and TEST5 traces on ground referenced layer to the TPs

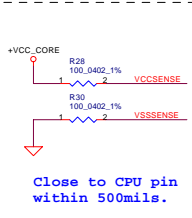
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0



Close to CPU pin AD26 within 500mils.



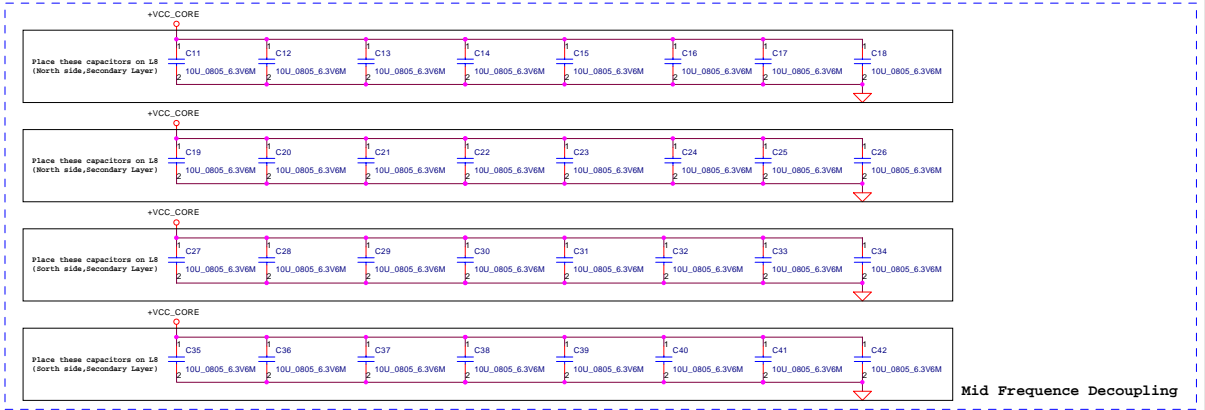
Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

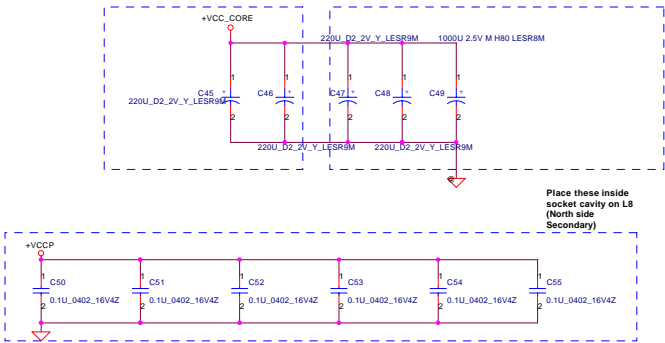
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JP20		
A4	VSS001	VSS082
A5	VSS002	VSS083
A6	VSS003	VSS084
A7	VSS004	VSS085
A8	VSS005	VSS086
A9	VSS006	VSS087
A10	VSS007	VSS088
A11	VSS008	VSS089
A12	VSS009	VSS090
A13	VSS010	VSS091
A14	VSS011	VSS092
A15	VSS012	VSS093
A16	VSS013	VSS094
A17	VSS014	VSS095
A18	VSS015	VSS096
A19	VSS016	VSS097
A20	VSS017	VSS098
A21	VSS018	VSS099
A22	VSS019	VSS100
A23	VSS020	VSS101
A24	VSS021	VSS102
A25	VSS022	VSS103
A26	VSS023	VSS104
A27	VSS024	VSS105
A28	VSS025	VSS106
A29	VSS026	VSS107
A30	VSS027	VSS108
A31	VSS028	VSS109
A32	VSS029	VSS110
A33	VSS030	VSS111
A34	VSS031	VSS112
A35	VSS032	VSS113
A36	VSS033	VSS114
A37	VSS034	VSS115
A38	VSS035	VSS116
A39	VSS036	VSS117
A40	VSS037	VSS118
A41	VSS038	VSS119
A42	VSS039	VSS120
A43	VSS040	VSS121
A44	VSS041	VSS122
A45	VSS042	VSS123
A46	VSS043	VSS124
A47	VSS044	VSS125
A48	VSS045	VSS126
A49	VSS046	VSS127
A50	VSS047	VSS128
A51	VSS048	VSS129
A52	VSS049	VSS130
A53	VSS050	VSS131
A54	VSS051	VSS132
A55	VSS052	VSS133
A56	VSS053	VSS134
A57	VSS054	VSS135
A58	VSS055	VSS136
A59	VSS056	VSS137
A60	VSS057	VSS138
A61	VSS058	VSS139
A62	VSS059	VSS140
A63	VSS060	VSS141
A64	VSS061	VSS142
A65	VSS062	VSS143
A66	VSS063	VSS144
A67	VSS064	VSS145
A68	VSS065	VSS146
A69	VSS066	VSS147
A70	VSS067	VSS148
A71	VSS068	VSS149
A72	VSS069	VSS150
A73	VSS070	VSS151
A74	VSS071	VSS152
A75	VSS072	VSS153
A76	VSS073	VSS154
A77	VSS074	VSS155
A78	VSS075	VSS156
A79	VSS076	VSS157
A80	VSS077	VSS158
A81	VSS078	VSS159
A82	VSS079	VSS160
A83	VSS080	VSS161
A84	VSS081	VSS162
A85	VSS082	VSS163

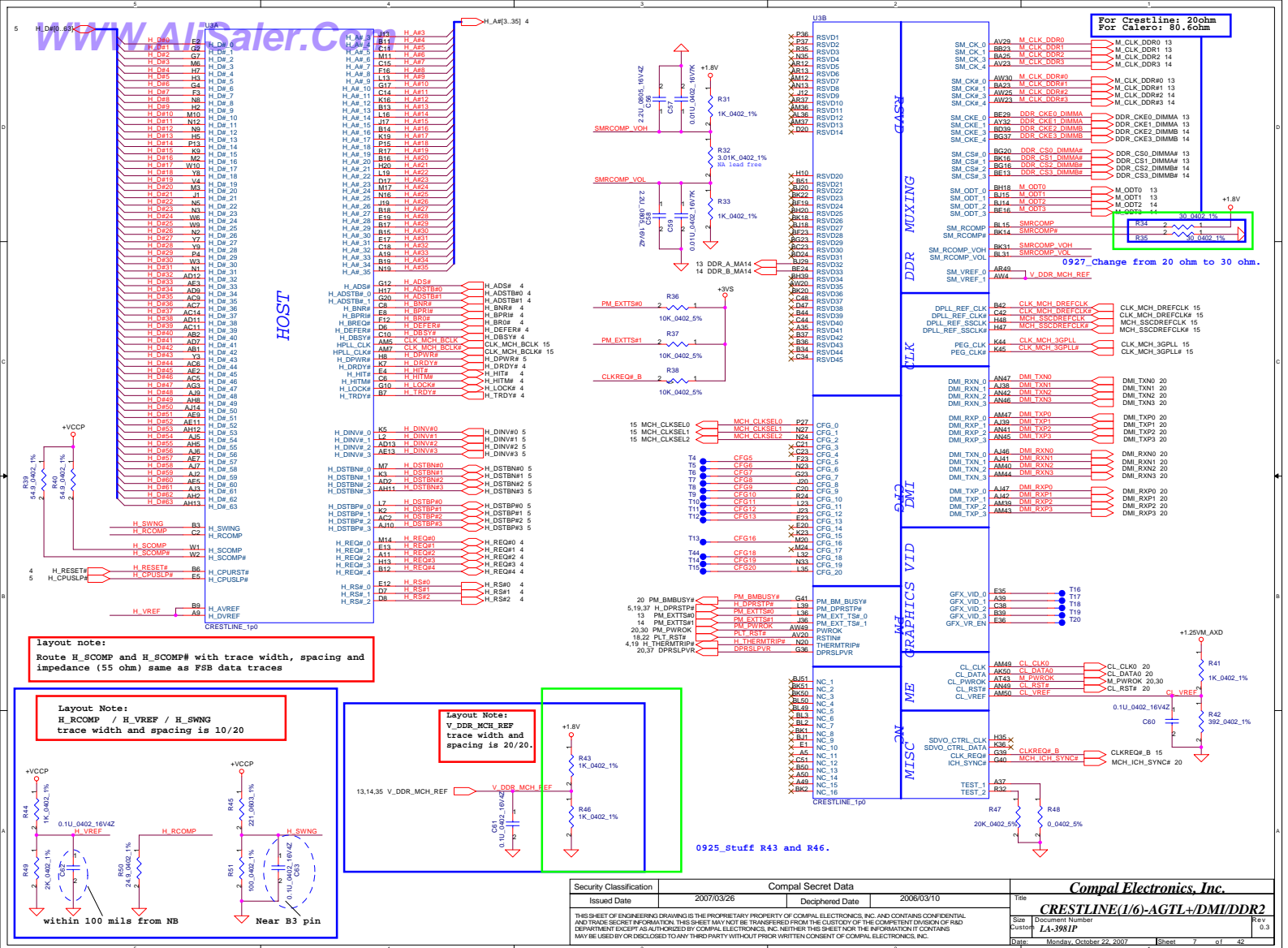


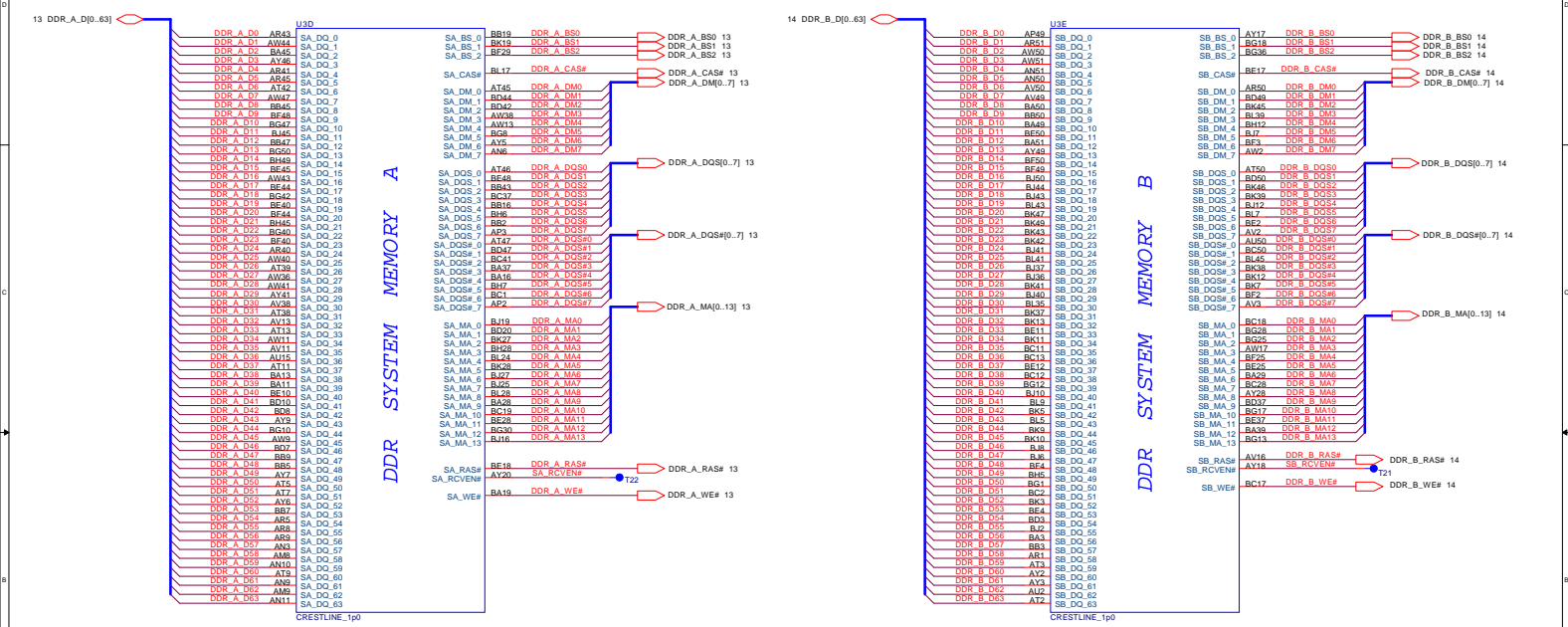
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

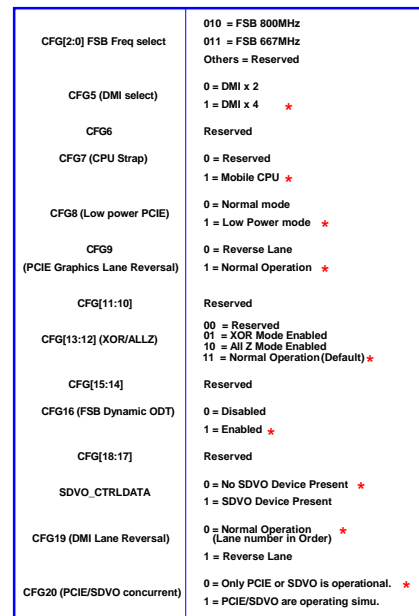


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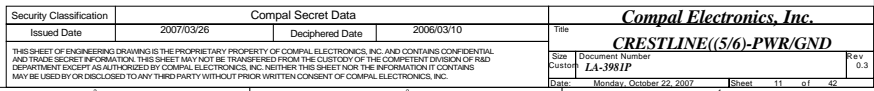
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2007/03/26		2006/03/10		CRESTLINE((2/6)-DDR2 A/B CH	
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```
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
```

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CRESTLINE((3/6)-VGA/LVDS/TV			LA-3981P	Sheet 9 of 42







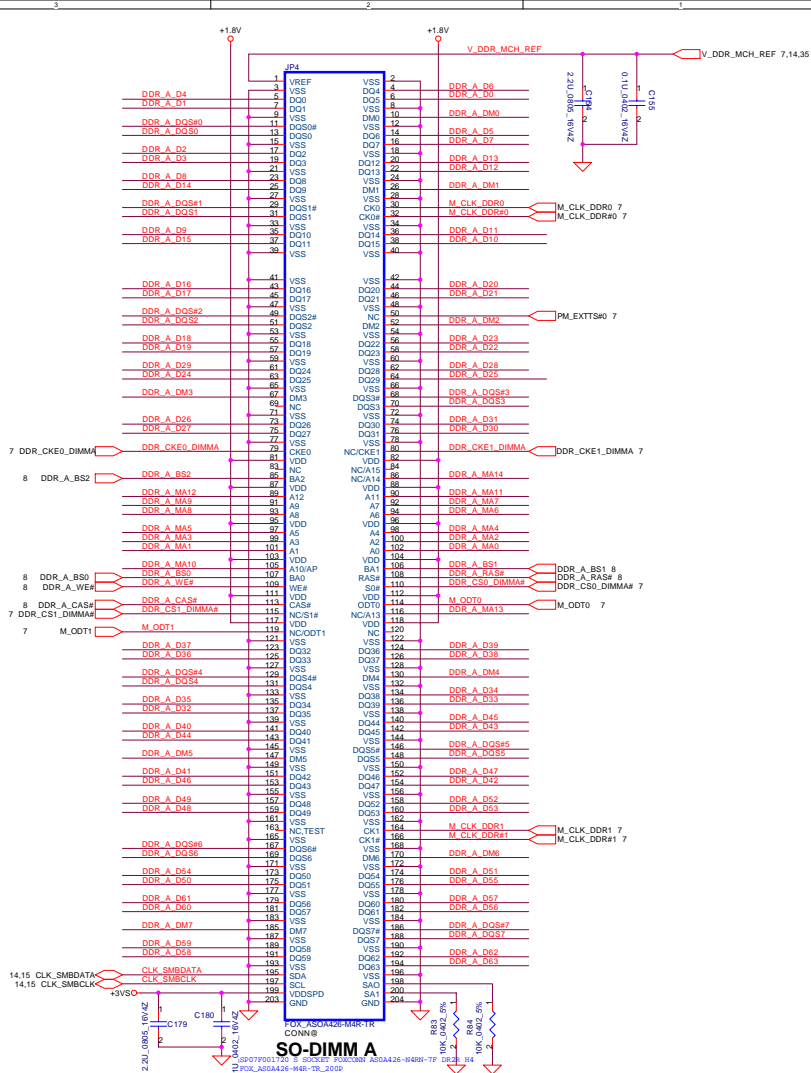
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The circuit diagram for Example 1.10 shows a ladder network with 10 resistors and a voltage source. The resistors are labeled as follows:

- $R_1 = 10\ \Omega$ (top horizontal)
- $R_2 = 20\ \Omega$ (vertical, after R_1)
- $R_3 = 10\ \Omega$ (top horizontal, after R_2)
- $R_4 = 20\ \Omega$ (vertical, after R_3)
- $R_5 = 10\ \Omega$ (top horizontal, after R_4)
- $R_6 = 20\ \Omega$ (vertical, after R_5)
- $R_7 = 10\ \Omega$ (top horizontal, after R_6)
- $R_8 = 20\ \Omega$ (vertical, after R_7)
- $R_9 = 10\ \Omega$ (top horizontal, after R_8)
- $R_{10} = 20\ \Omega$ (vertical, after R_9)

A voltage source of $10\ \text{V}$ is connected in series with R_1 on the left. A red arrow indicates the current i flowing through R_{10} from top to bottom.

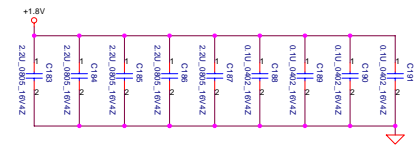
Figure 1: Schematic diagram of the proposed 16-to-1 multiplexer. The diagram shows a hierarchical structure of 2-to-1 multiplexers. At the top, a 2-to-1 MUX selects between R1 and R2 based on control signal S0. Below this, there are four stages of 2-to-1 MUXes. The first stage has inputs R1, R2, R3, and R4, controlled by S0 and S1. The second stage has inputs R5, R6, R7, and R8, controlled by S0 and S2. The third stage has inputs R9, R10, R11, and R12, controlled by S0 and S3. The fourth stage has inputs R13, R14, R15, and R16, controlled by S0 and S4. The final output is selected by S5. The diagram is labeled with '0.9V' at the top and '0V' at the bottom. The inputs are labeled with their corresponding data bus values: R1 (DDR_A_M13, DDR_A_M10), R2 (DDR_A_M12, DDR_A_M9), R3 (DDR_A_M8, DDR_A_M5), R4 (DDR_A_M7, DDR_A_M4), R5 (DDR_A_M6, DDR_A_M3), R6 (DDR_A_M2, DDR_A_M1), R7 (DDR_A_M12, DDR_A_M9), R8 (DDR_A_M11, DDR_A_M8), R9 (DDR_A_M10, DDR_A_M7), R10 (DDR_A_M6, DDR_A_M3), R11 (DDR_A_M5, DDR_A_M4), R12 (DDR_A_M2, DDR_A_M1), R13 (DDR_A_M12, DDR_A_M9), R14 (DDR_A_M11, DDR_A_M8), R15 (DDR_A_M10, DDR_A_M7), R16 (DDR_A_M6, DDR_A_M3).



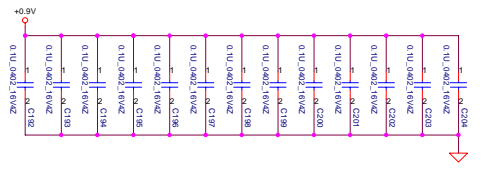
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8 DDR_B_D0#(0.7)
8 DDR_B_D0(0.69)
8 DDR_B_DM0(0.7)
8 DDR_B_DS0(0.7)
7.8 DDR_B_MA(0.14)

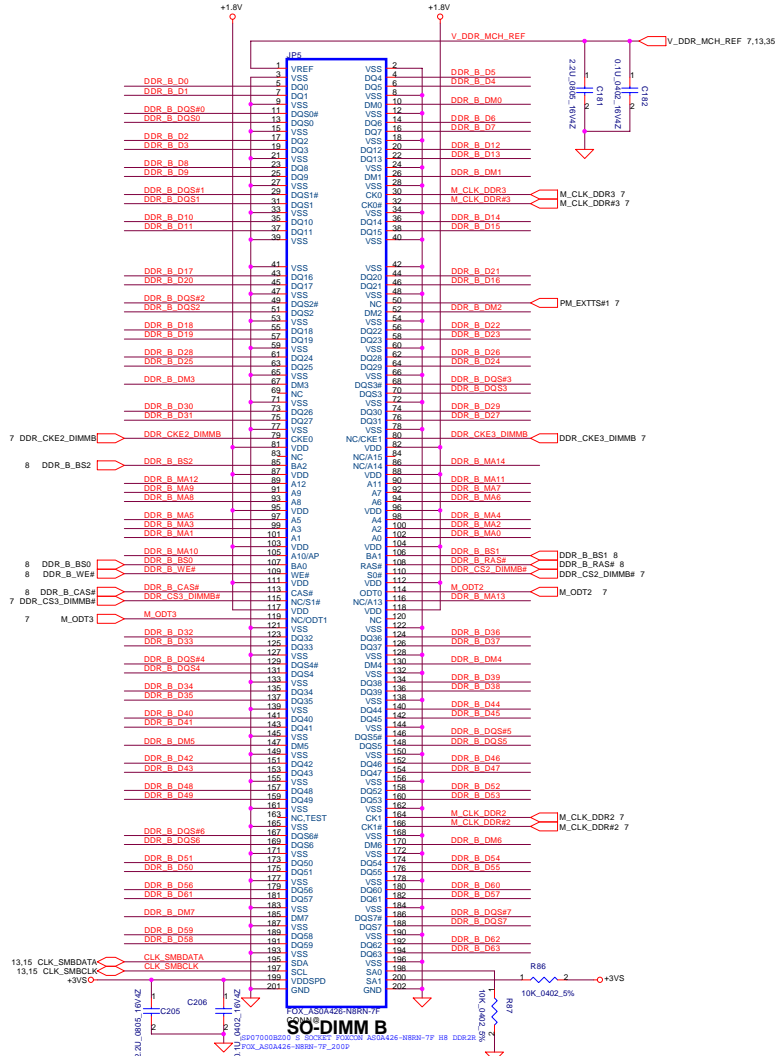
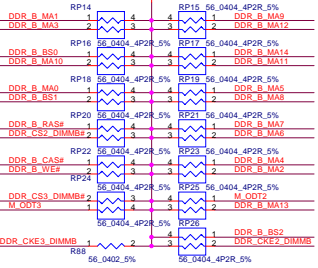
Layout Note:
Place near JP10

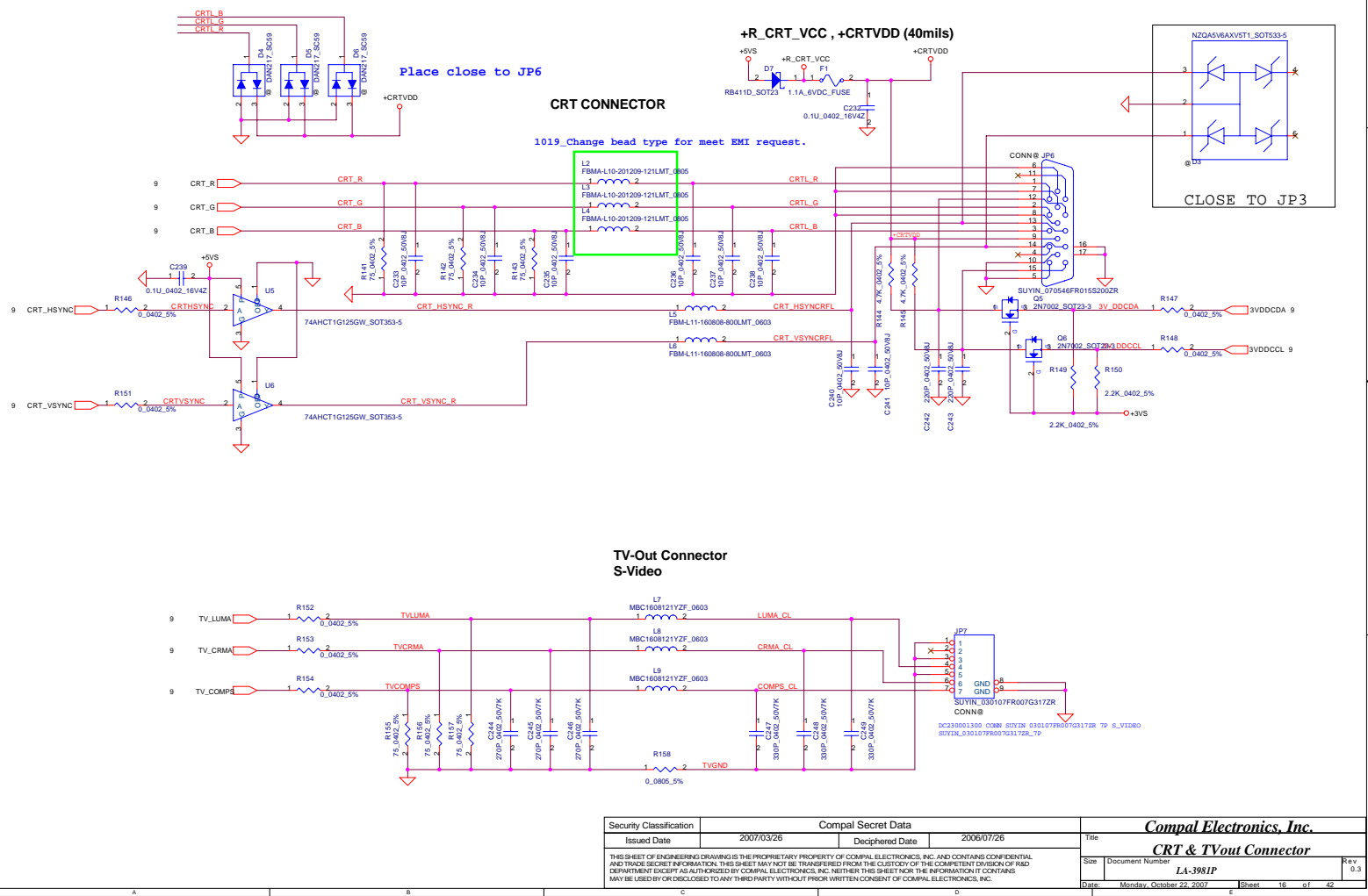


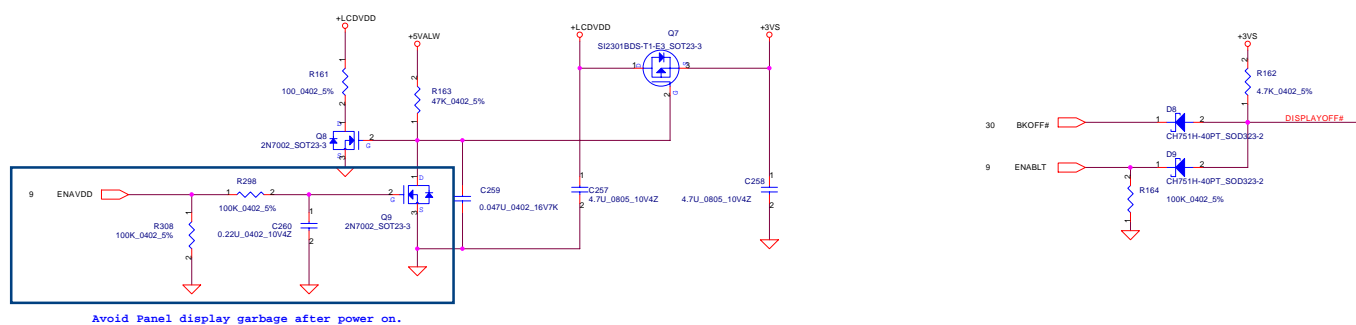
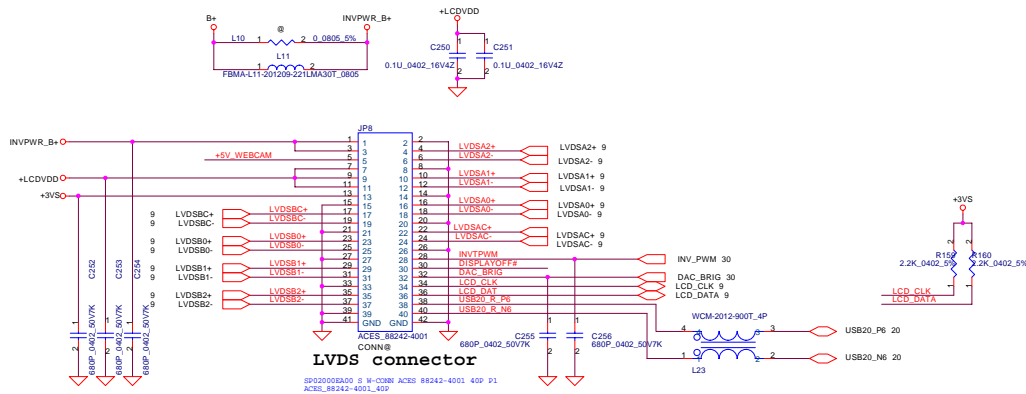
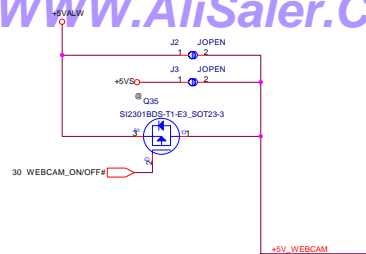
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



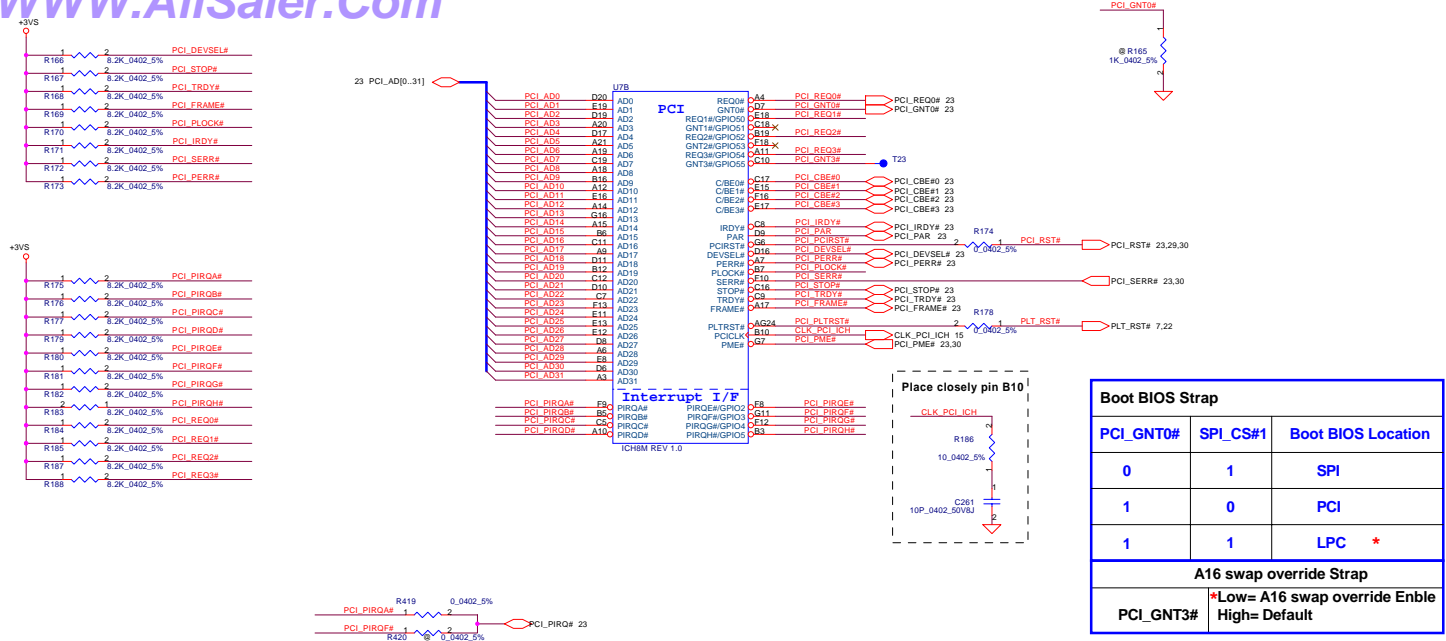
Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



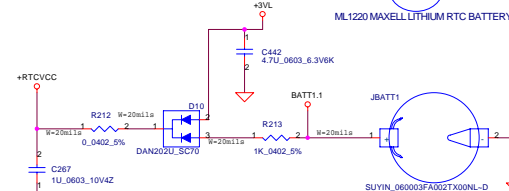




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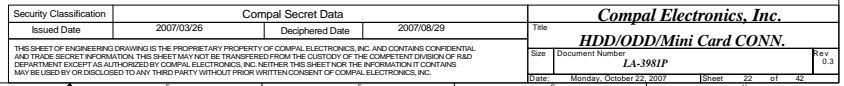


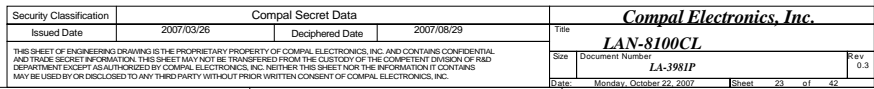
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Issued Date	2007/03/26	Deciphered Date	2006/03/10	IC88(1/4)-PCI/INT	
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Placea caps. near ODD CONN.

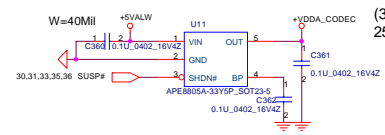




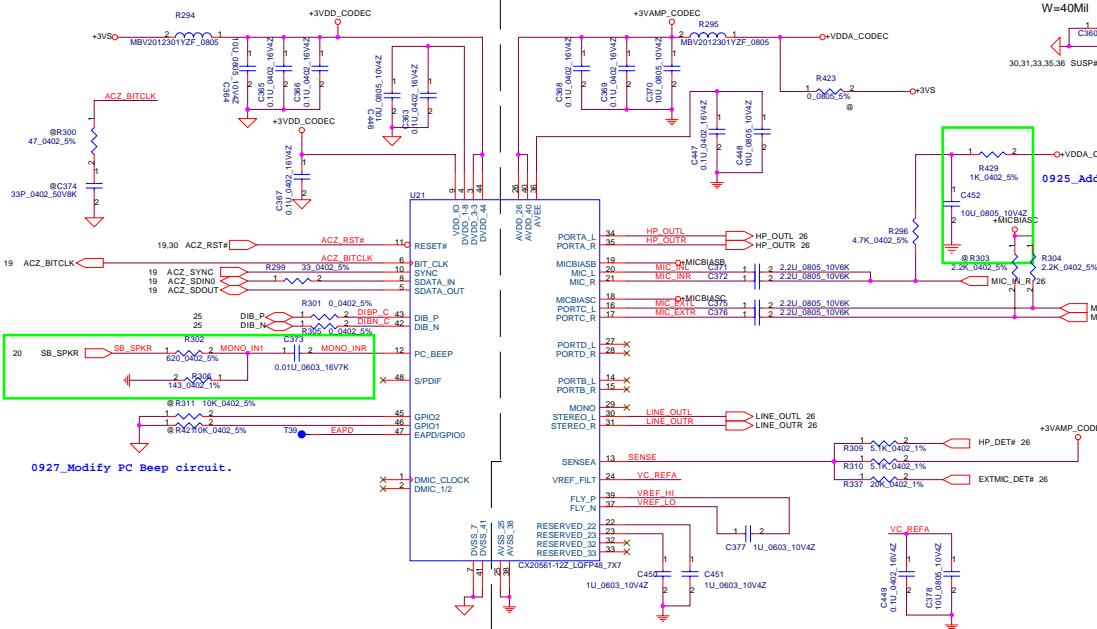
CODEC POWER

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

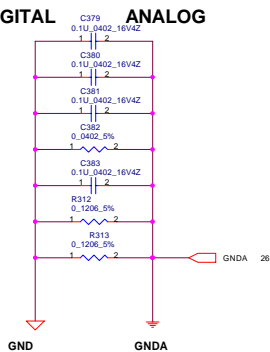
(3.33V)
250mA



02_5% 0925_Add LPF to reduce INT. MIC noise.

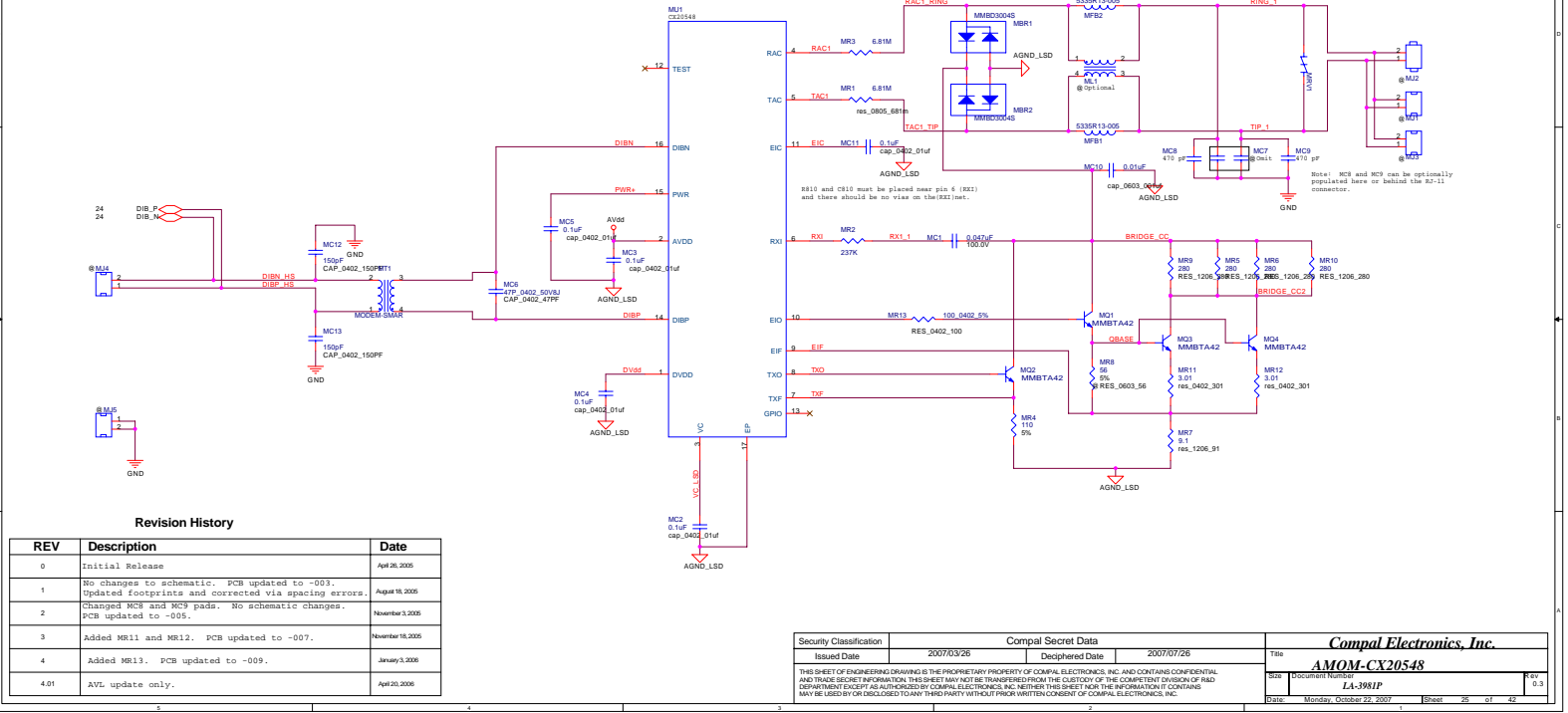


DIGITAL C379 **ANALOG**
0.11L 0402 18V47

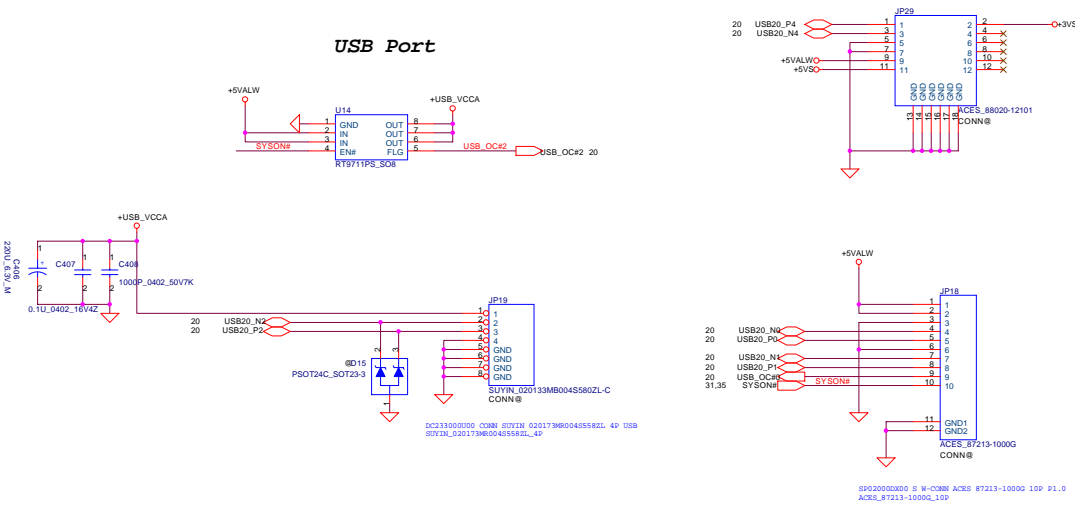


HP_DET#	MIC_DET	LINEOUT	PORT-A <Rearphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

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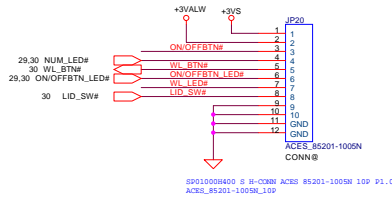
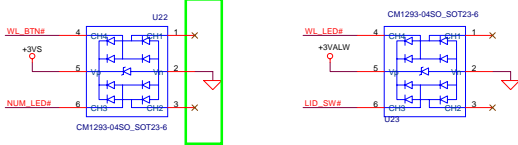




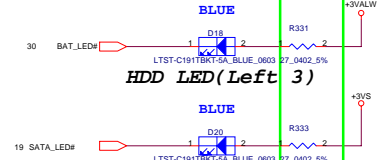
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1		27		42	

M/BtoS/B

1005_Disconnect ON/OFFBTN# and ON/OFFBTN_LED# from U22.



Battery Charge LED(Left 2)

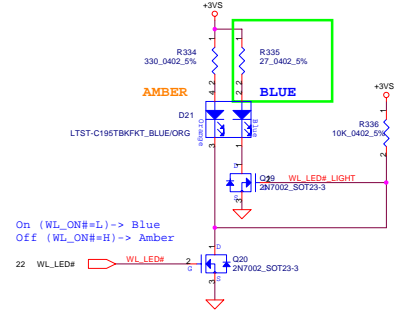


HDD LED(Left 3)

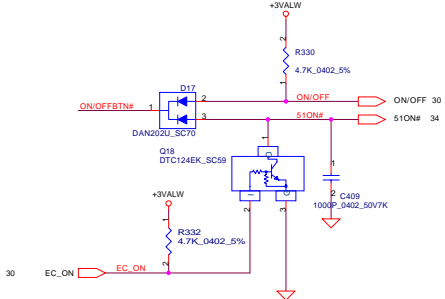


0927_Change R329, R331, R333 (75 ohm), R335 (33 ohm) to 27 ohm.

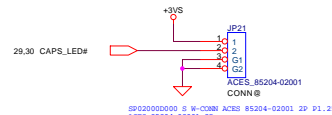
Wireless ON/OFF LED(Left 4)



Power ON/OFF

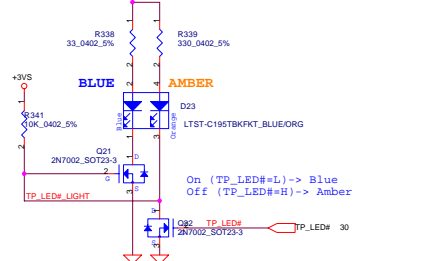


M/B to SB(Caps Lock LED)

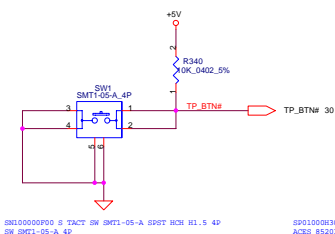


D21, D25, D23 Footprint can not match part number.

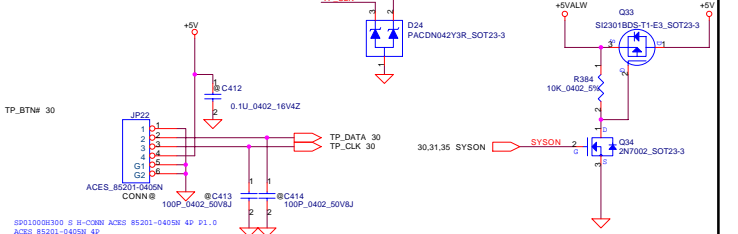
TouchPAD ON/OFF LED



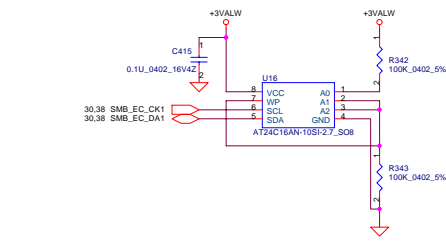
TP ON/OFF



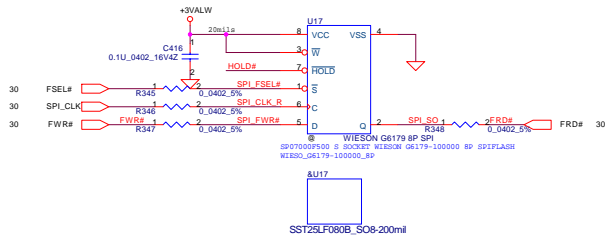
T/P Board



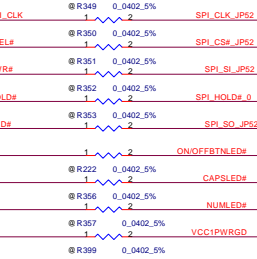
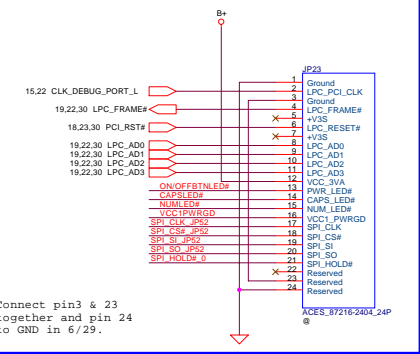
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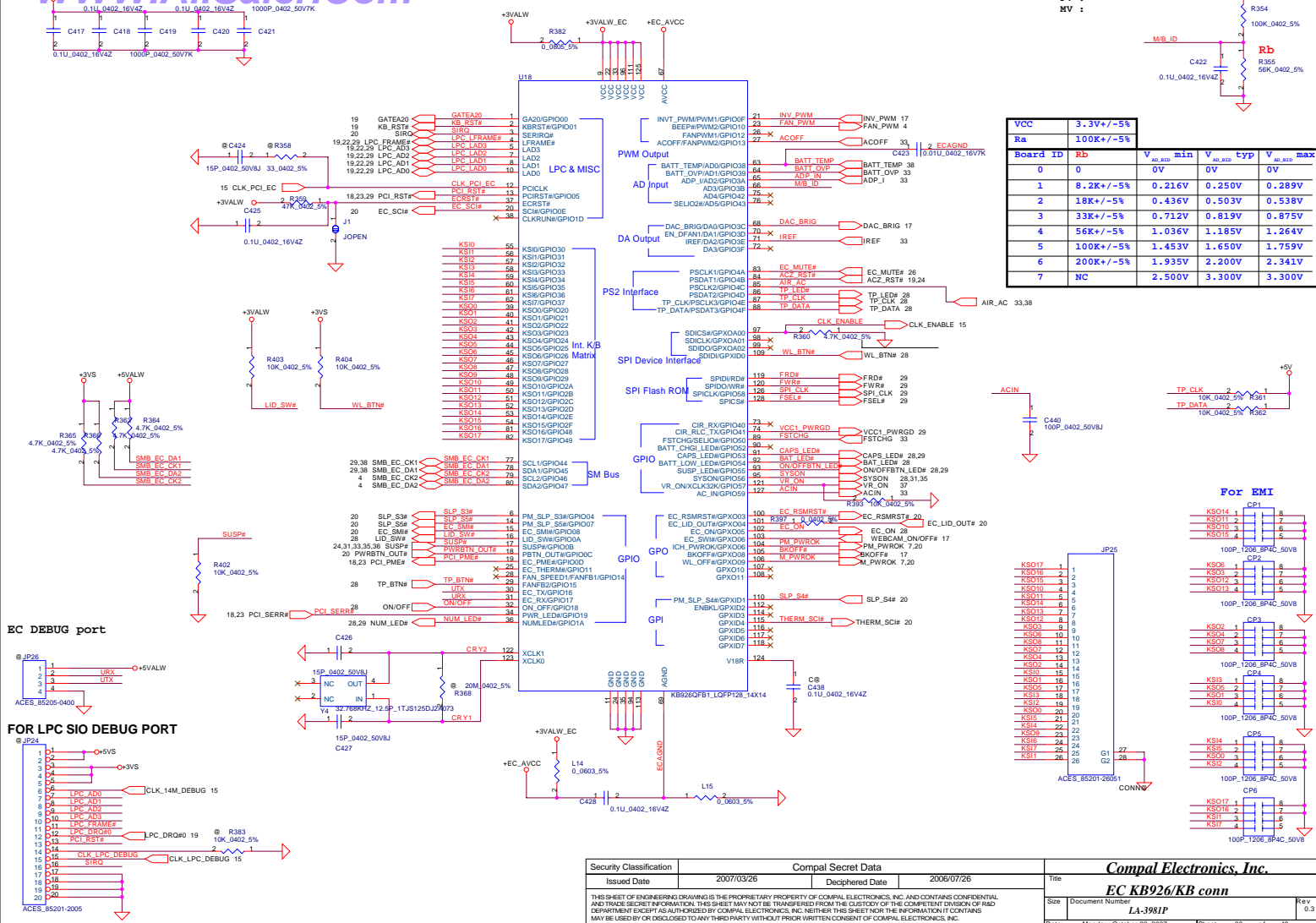
SPI ROM

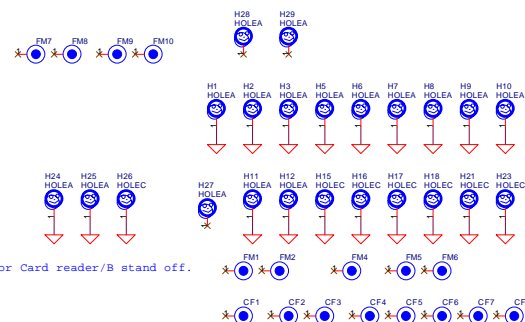
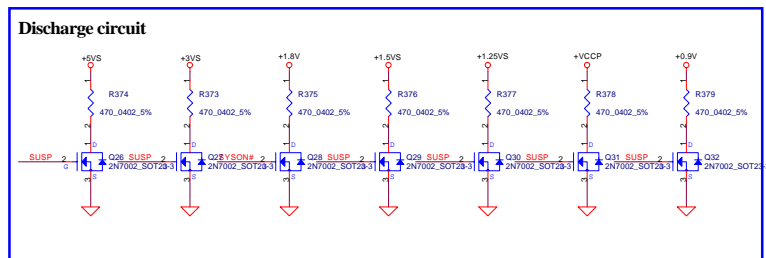
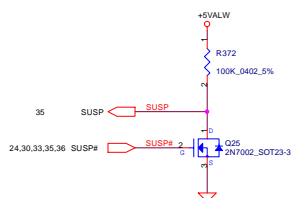
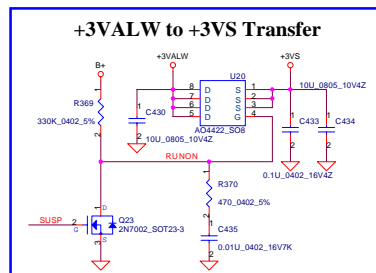


LPC Debug Port

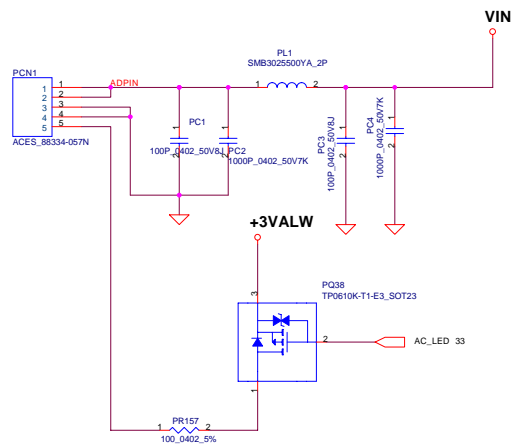


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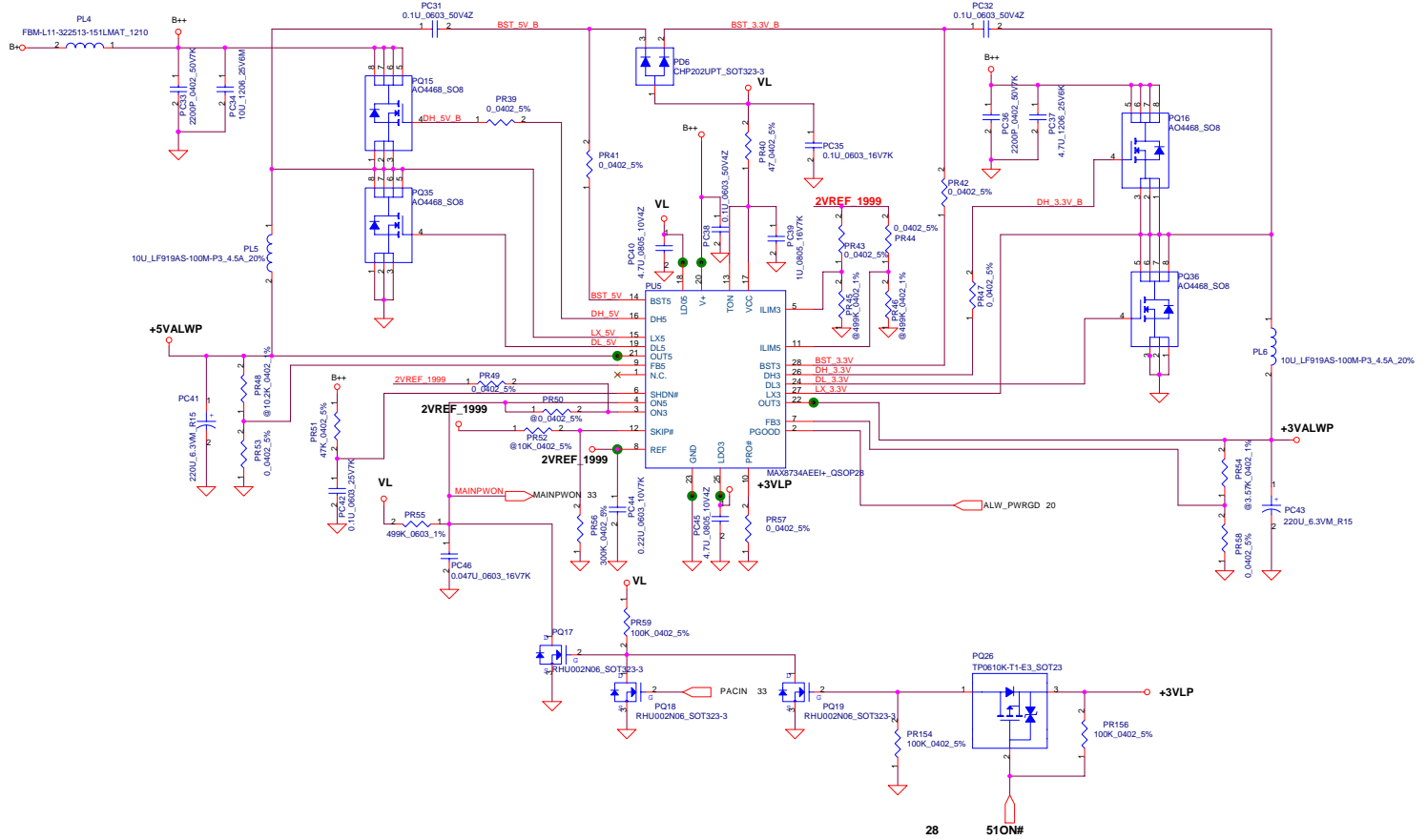


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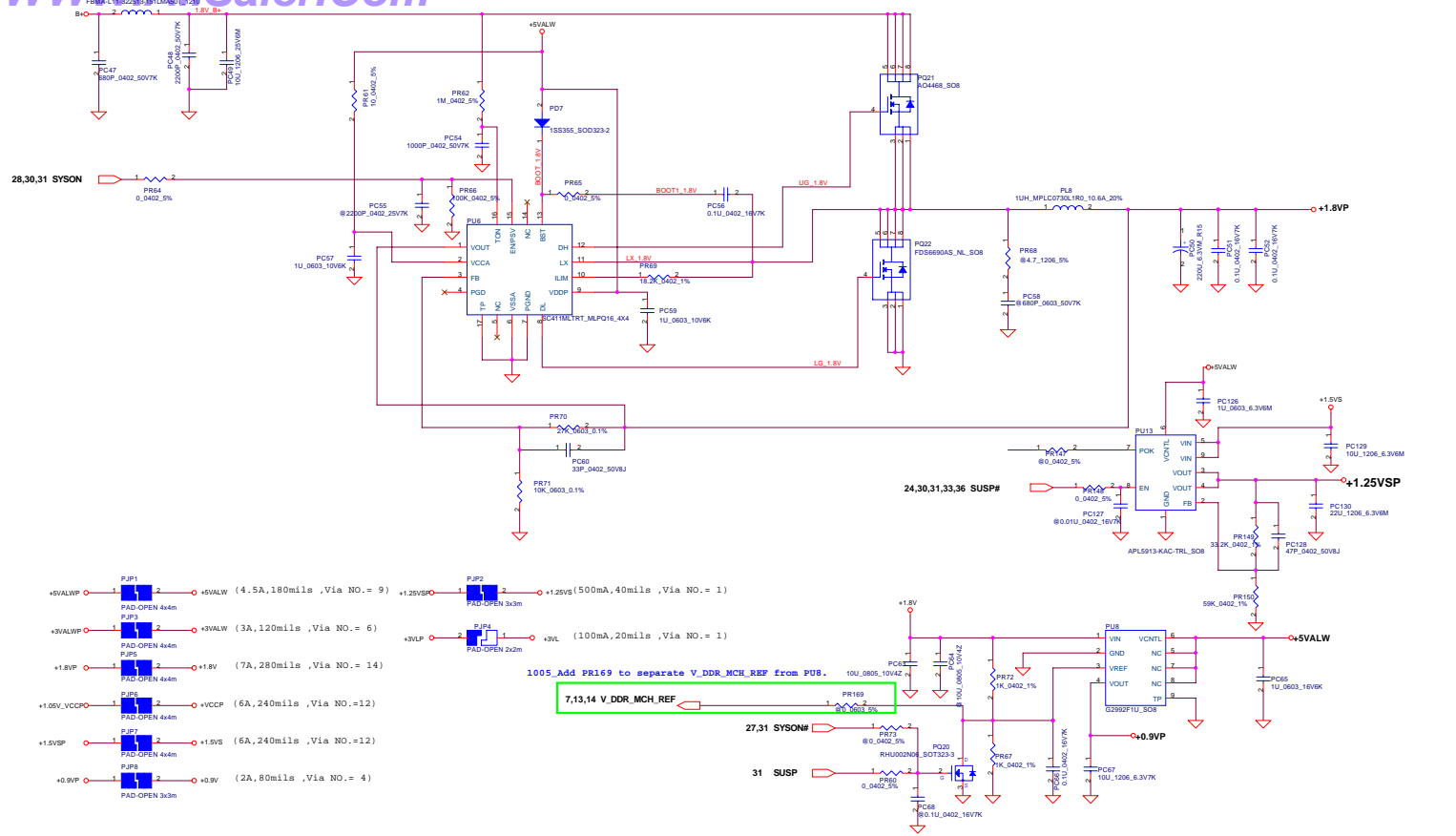


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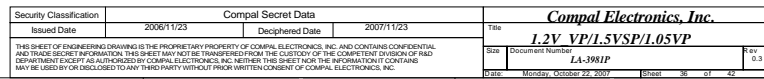


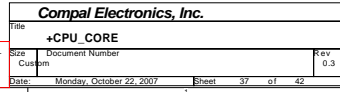


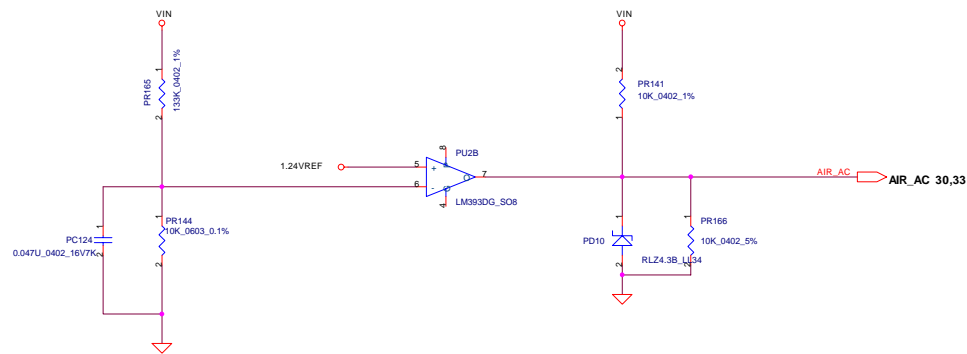
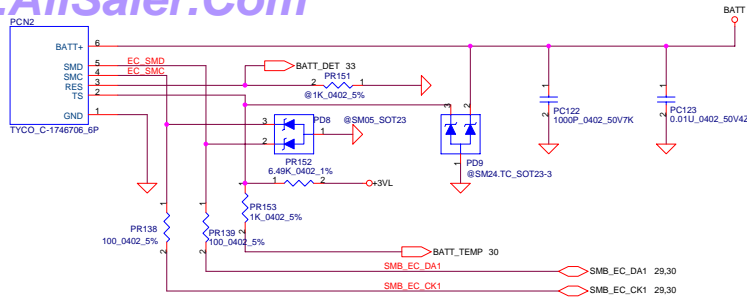
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Item	Reason for change	PG#	Modify List	Date	Phase
1			1009_PL8 change to 1uH.		
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					




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Item	Change Item	Page	Date	Phase
1	Change C262 and C263 from 15pF to 12pF	19	7/16	DB --> SI
2	Reserved R245 and Add R422	20	7/16	DB --> SI
3	Add D29 prevent leakage issue	22	7/16	DB --> SI
4	Reserved diode D30 D31 for ESD	26	7/16	DB --> SI
5	Reserved R423 for coat down plan	24	7/24	DB --> SI
6	Remove Q12-Q17,R323 R324 R327 R328 R417 R418	26	7/30	DB --> SI
7	Change EXT MIC port B to port C	24	7/31	DB --> SI
8				DB --> SI
9				DB --> SI
10				DB --> SI
11				DB --> SI
12				DB --> SI
13				DB --> SI
14				DB --> SI
15				DB --> SI
16				DB --> SI
17				DB --> SI
18				DB --> SI
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29				DB --> SI

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Item	Change item	Page		Date	Phase
1	Change R296 R337 R value	24	Follow conexant new design rule	8/6	SI --> PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	Follow conexant new design rule	8/6	SI --> PV
3	Change PIRQ from F to A	18	Choose R419 then control PIRQ A	8/14	SI --> PV
4	Connect PCI_SERR# to EC GPIO pin.	18	Connect PCI_SERR# to EC GPIO pin.	8/31	SI --> PV
5	Modify PC BEEP circuit.	20	Modify PC BEEP circuit.	8/31	SI --> PV
6	For support Intel Penryn CPU.	04	Reserve R426 and R427 for support Intel Penryn CPU.	9/3	SI --> PV
7	For ESD request.	28	Add U22 and U23 for ESD request.	9/3	SI --> PV
8	For EMI request.	26	Add L24-L27	9/5	SI --> PV
9	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	9/7	SI --> PV
10	Add R417 and R418 to fine-tune Vp-p.	26	Add R417 and R418 to fine-tune Vp-p.	9/7	SI --> PV
11	For ESD request.	20	Add U22 and U23 for ESD request.	9/7	SI --> PV
12					SI --> PV
13					SI --> PV
14					SI --> PV
15					SI --> PV
16					SI --> PV
17					SI --> PV
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38					SI --> PV

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