

MODEL NAME : *BBV00/BBV10*PCB NO : *LA-D993P*

BOM P/N :

# Dell/Compal Confidential

## Schematic Document

### KABYLAKE-H

2016-11-01

Rev: 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

EMC@ : Pop of EMI parts

S4G@ : Samsung GDDR5 4G for GPU

M4G@ : Micron GDDR5 4G for GPU

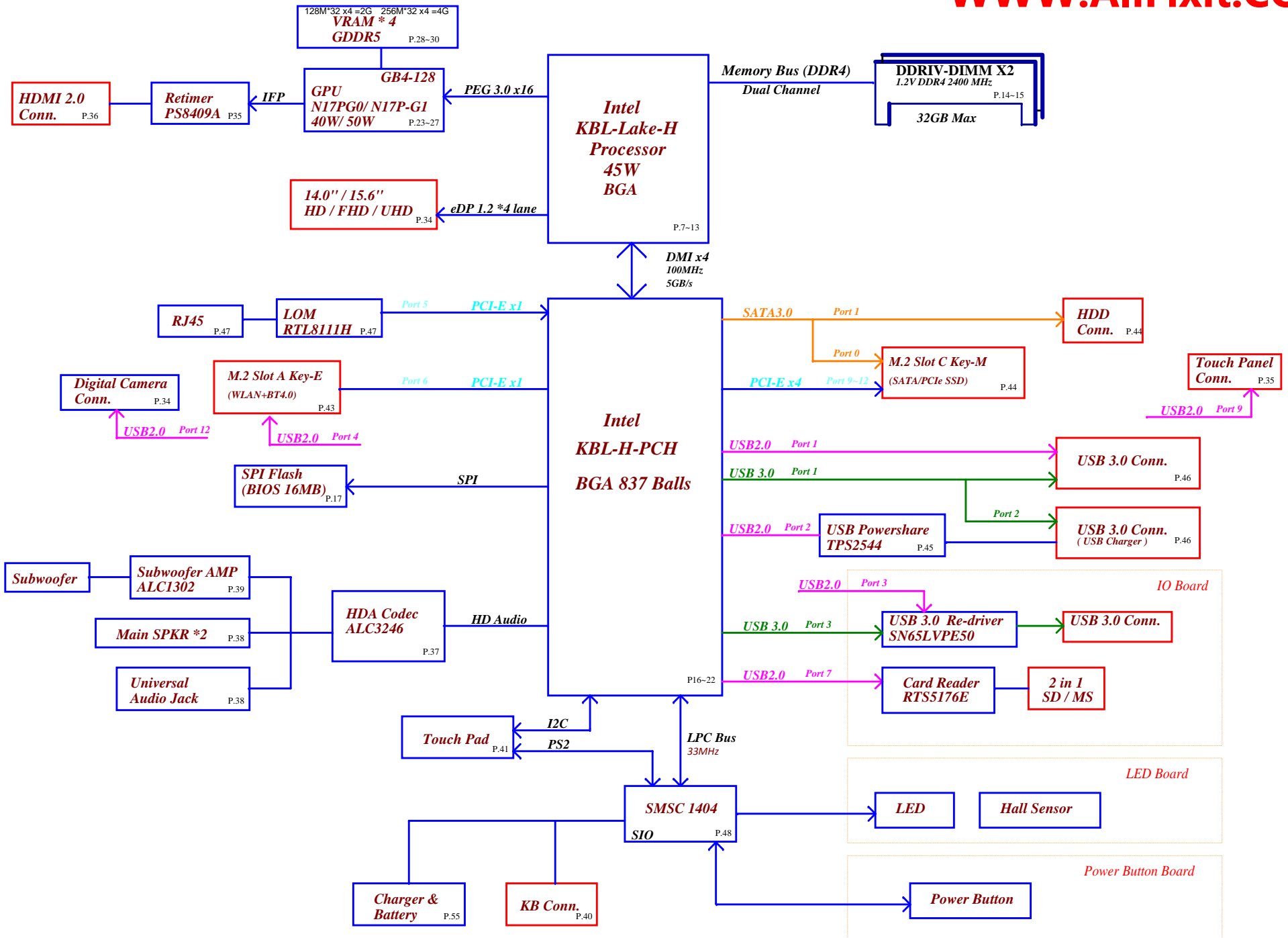
H4G@ : Hynix GDDR5 4G for GPU

BreakDown@ : For measure power consumption

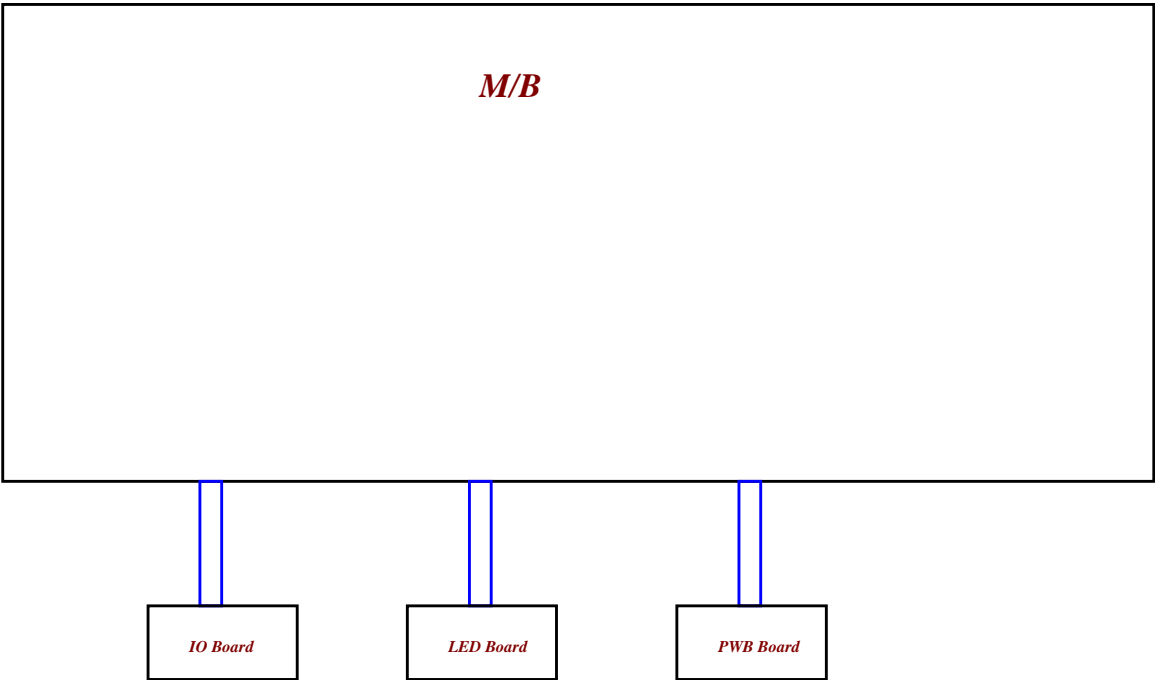
14G0@ : 14" N17P-G0

15G1@ : 15" N17P-G1

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Issued Date	2011/08/25	Deciphered Date	2011/08/25	Title
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			Document Number	0.1000
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Project Code :  
File Name :



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Board ID	Resistor
X00	N/A
X01	
X02	
X03	
X04	22.1K
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None	SATA	DESTINATION
Lane 9	SSD	0A	SSD
Lane 10	SSD	1A	N/A
Lane 11	SSD	N/A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	None	0B	None
Lane 14	None	1B	HDD
Lane 15	Alpine Ridge	2	None
Lane 16		3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

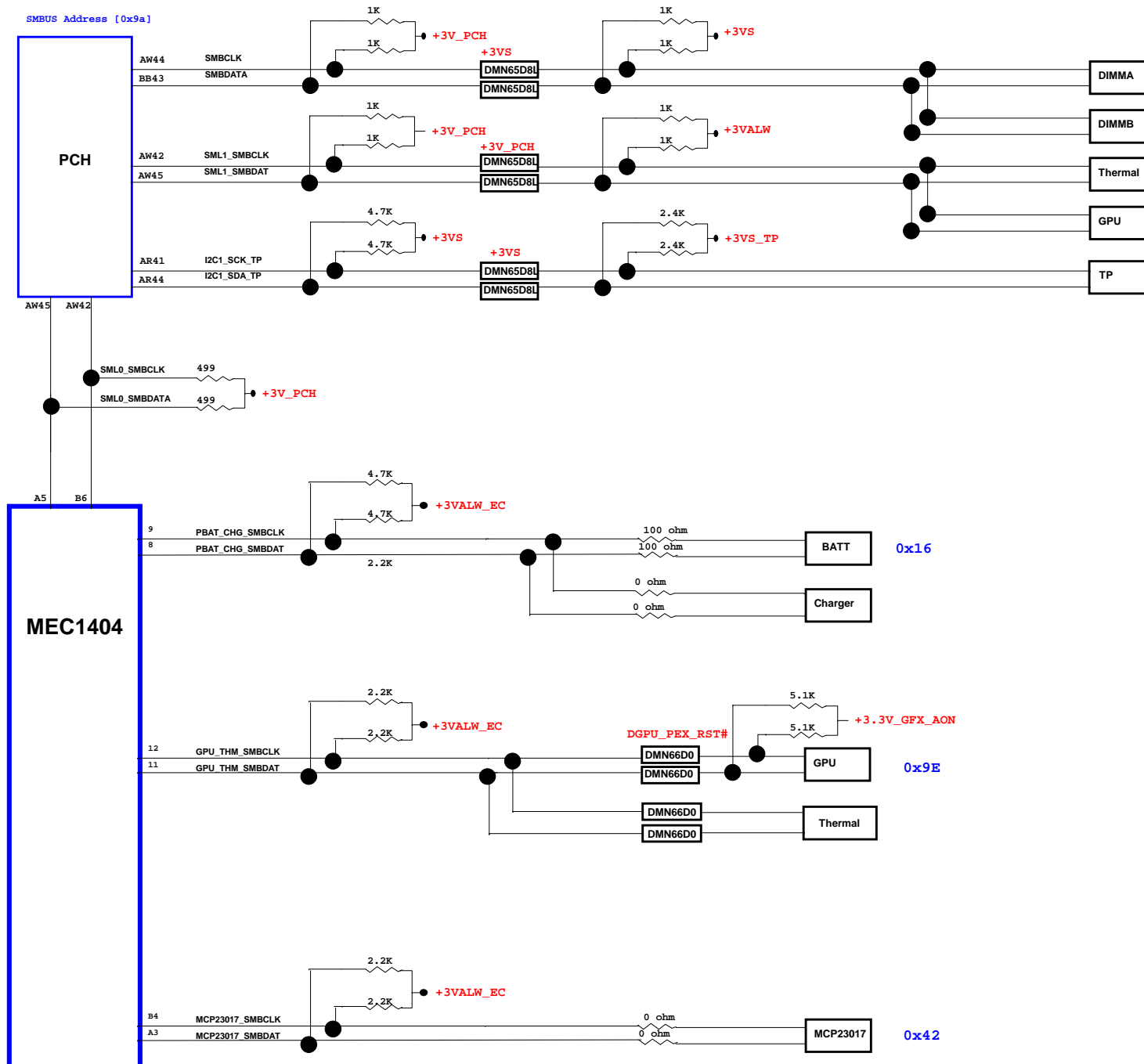
Symbol Note :



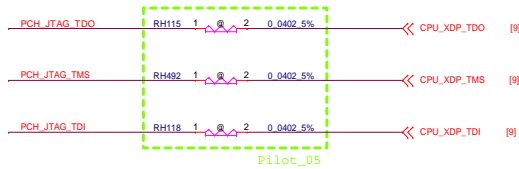
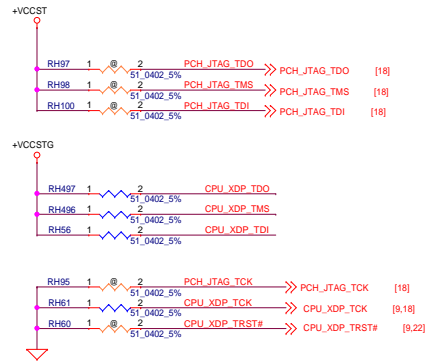
: means Digital Ground



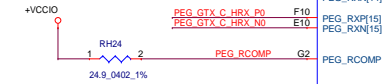
: means Analog Ground



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2012/07/15				Title				SMBus Block Diagram			
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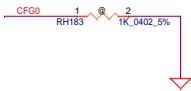


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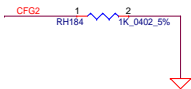
0.1(X100)



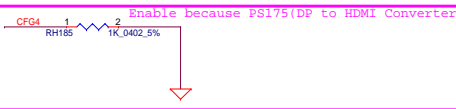
Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	<ul style="list-style-type: none"><li>* 1 = (Default) Normal Operation; No stall.</li><li>0 = Stall.</li></ul>



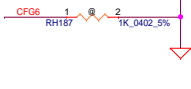
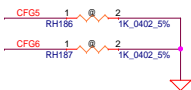
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<ul style="list-style-type: none"><li>1: Normal Operation; Lane # definition matches socket pin map definition</li><li>* 0: Lane Reversed</li></ul>



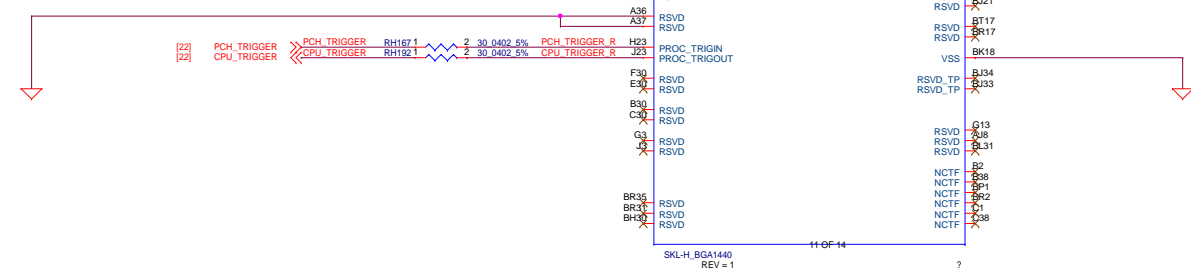
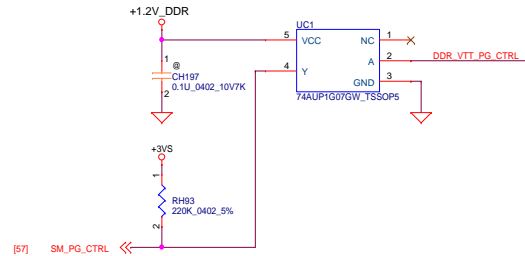
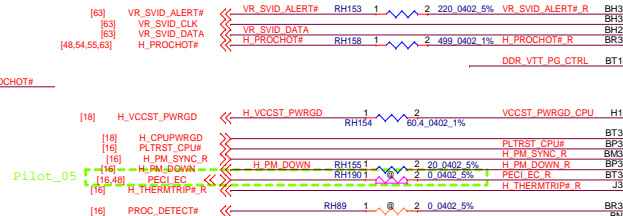
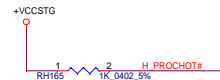
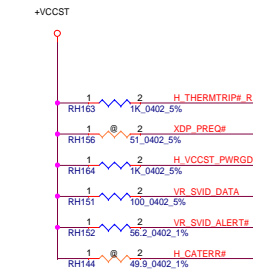
Display Port Presence Strap	
CFG4	<ul style="list-style-type: none"><li>1 : Disabled; No Physical Display Port attached to Embedded Display Port</li><li>* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</li></ul>

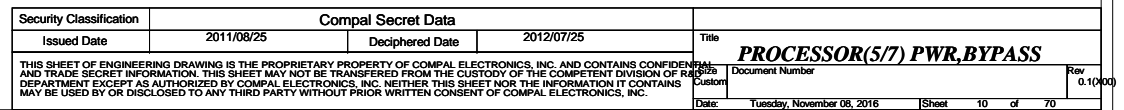


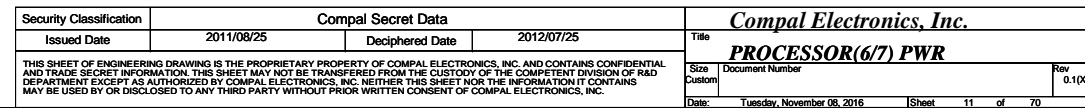
PCIe Port Bifurcation Straps	
CFG[6:5]	<ul style="list-style-type: none"><li>* 11: (Default) x16 - Device 1 functions 1 and 2 disabled</li><li>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</li><li>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</li><li>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</li></ul>

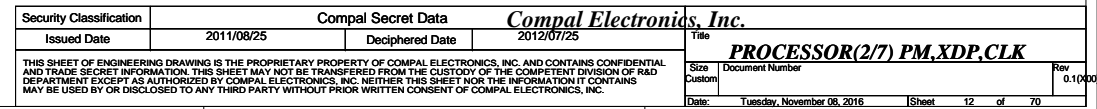


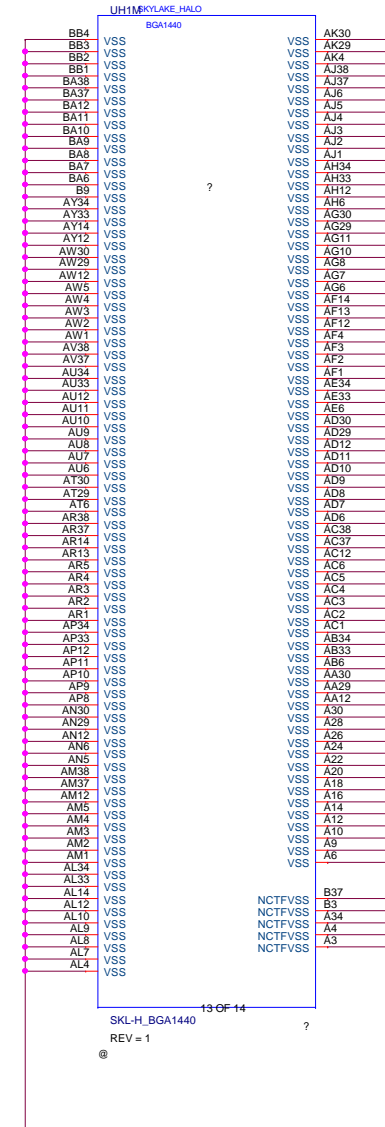
PEG DEFER TRAINING	
CFG7	<ul style="list-style-type: none"><li>* 1: (Default) PEG Train immediately following xxRESETB de assertion</li><li>0: PEG Wait for BIOS for training</li></ul>



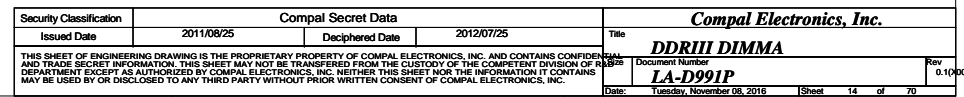


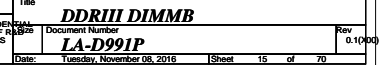


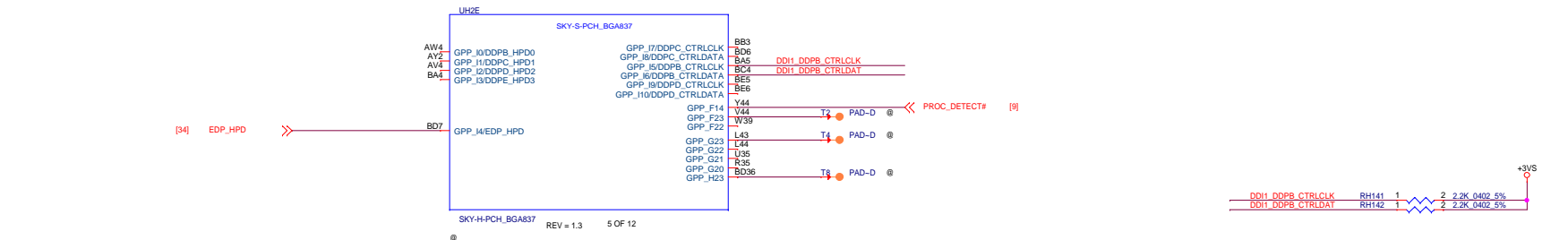




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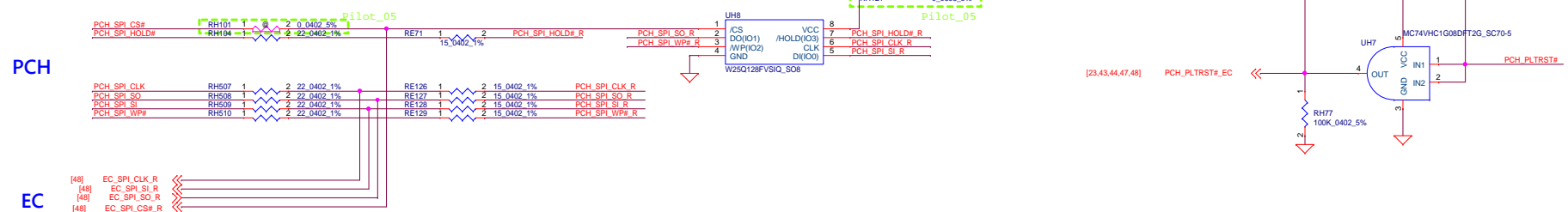
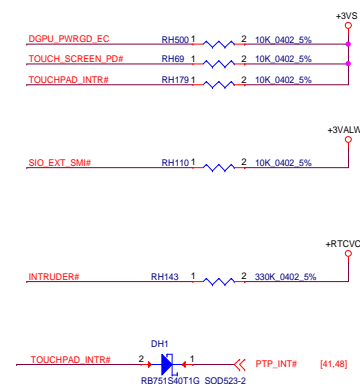
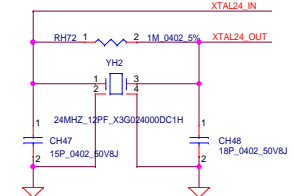
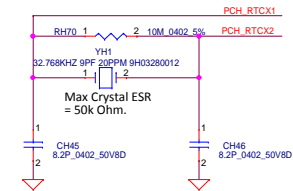




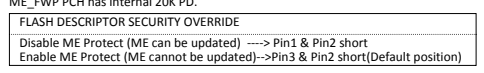
Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k $\Omega$ $\pm$ 5% resistor	No Connect

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						Size	Document Number	Rev
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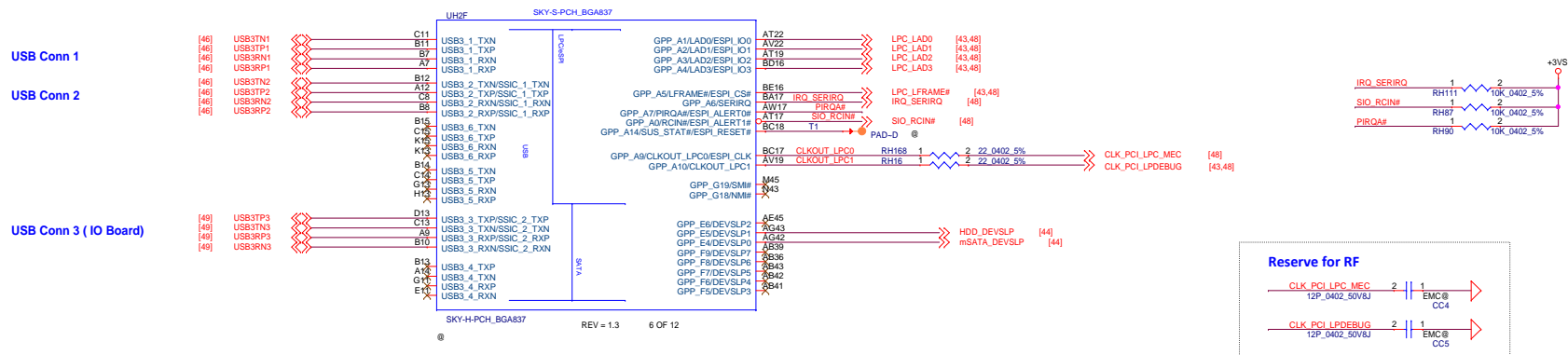
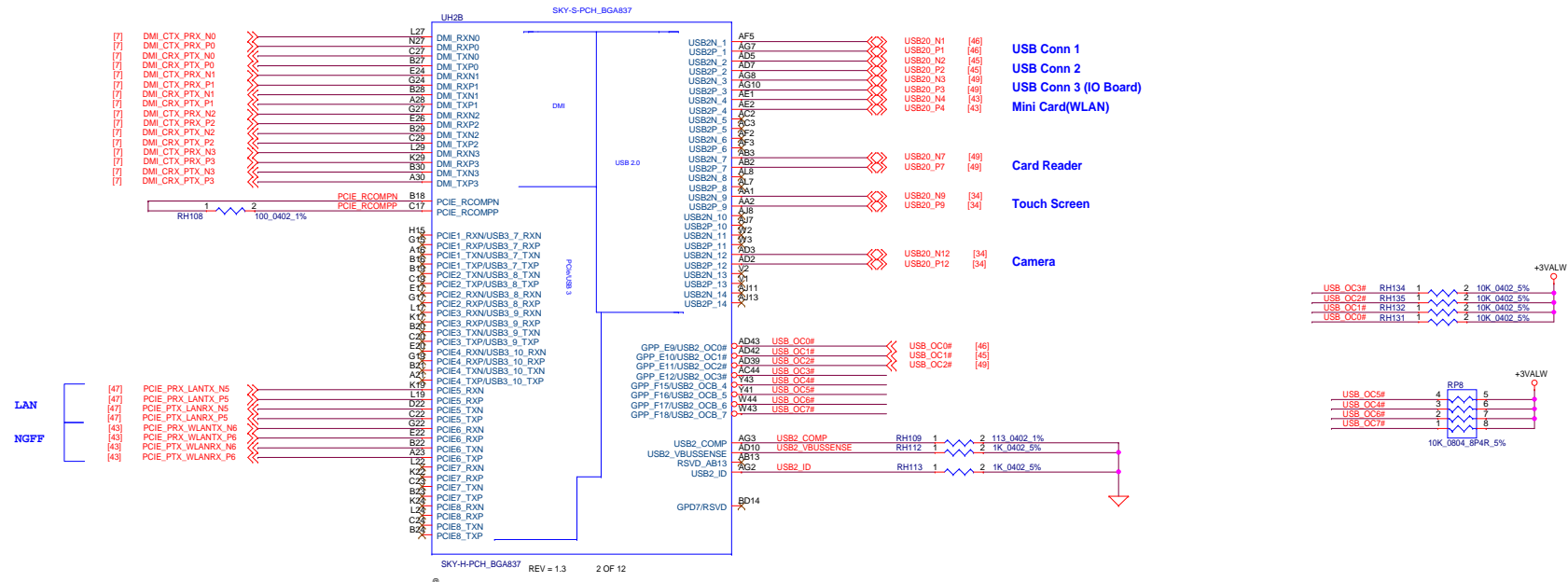




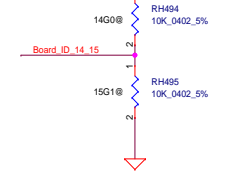
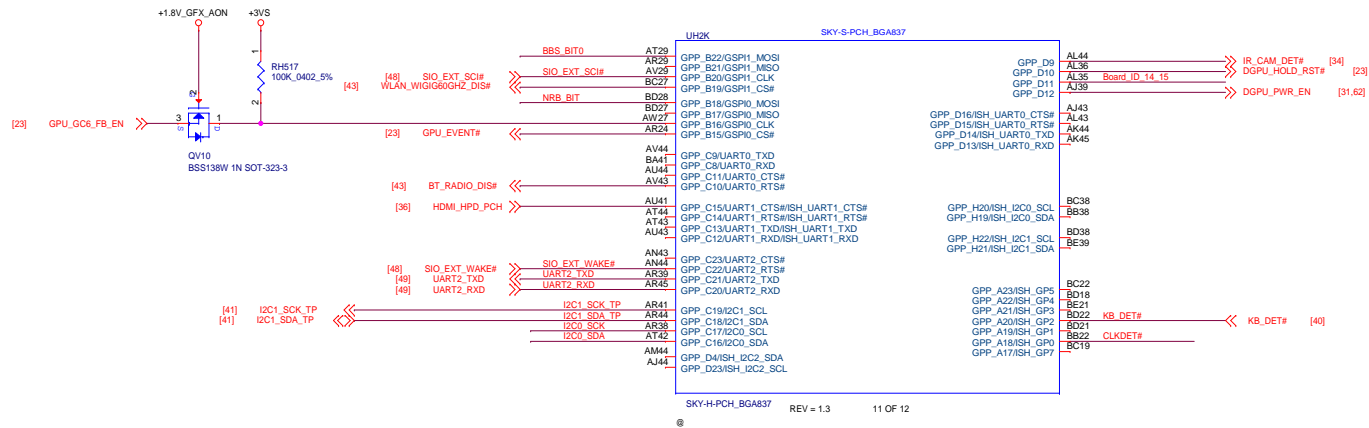
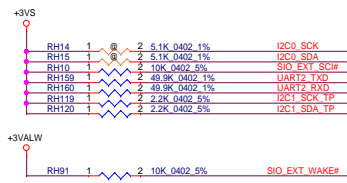
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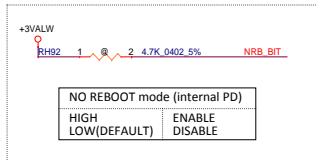
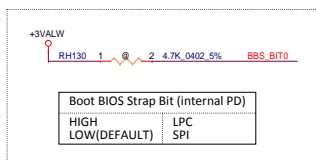
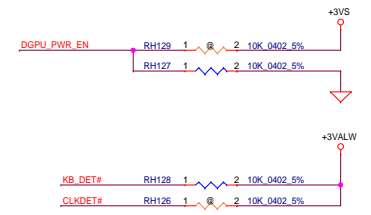
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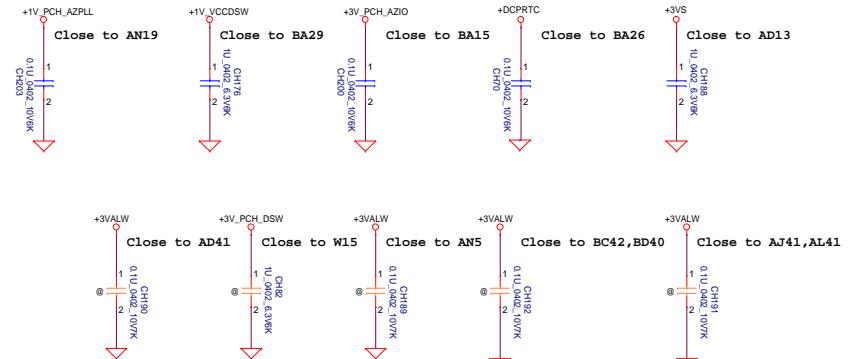
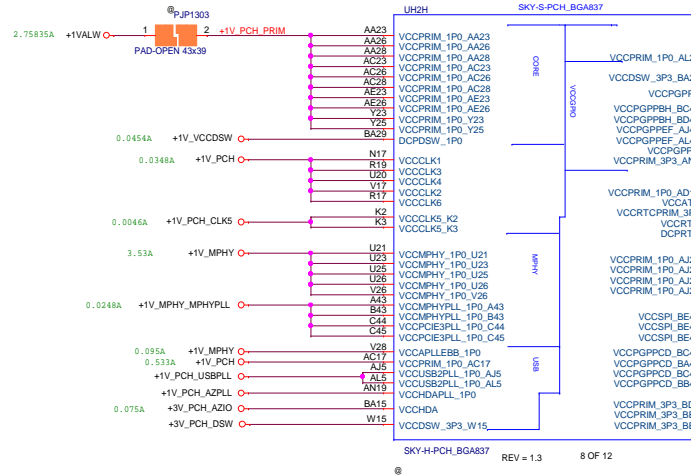
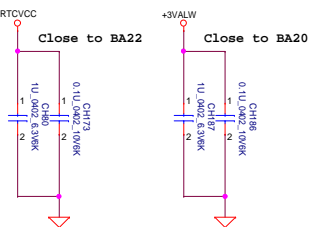
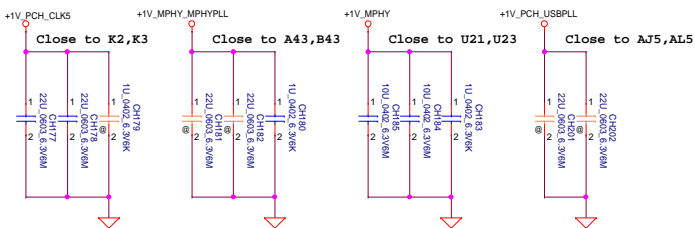
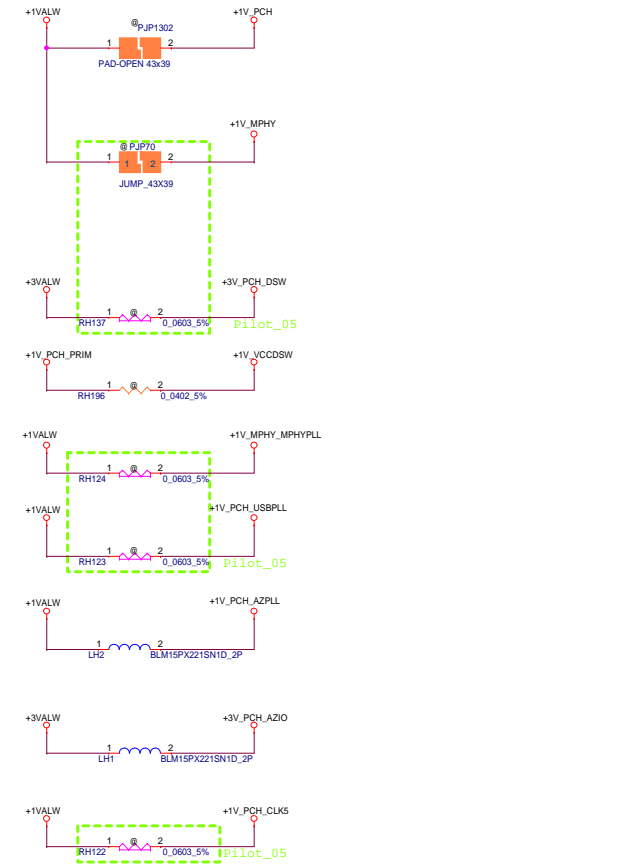
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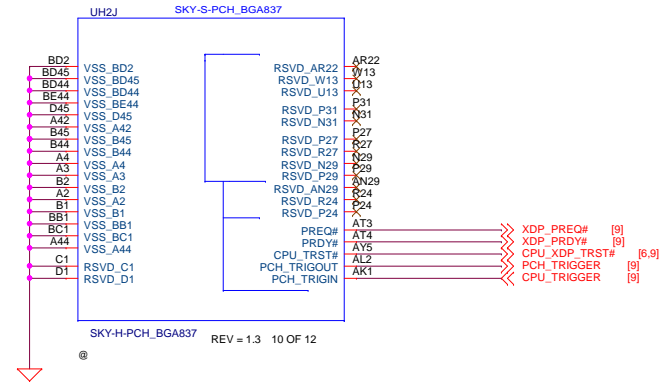
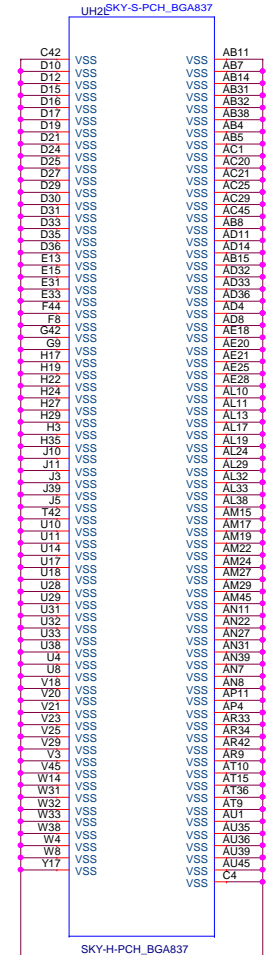
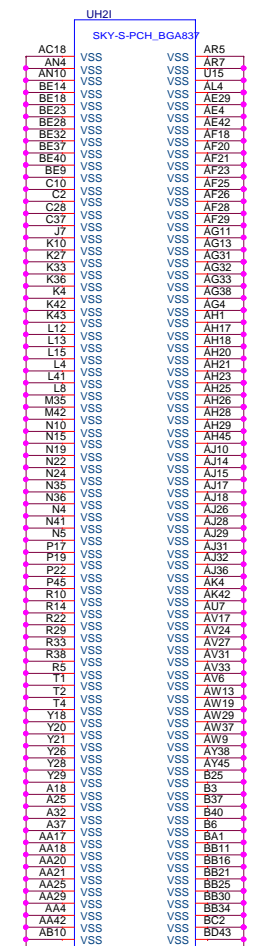


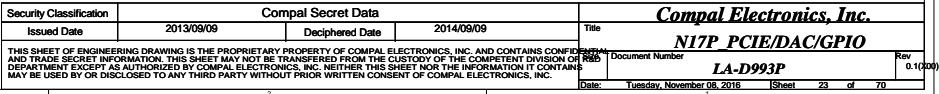
SYSTEM ID	
HIGH	14" & N16P_GT
LOW	15" & N16P_GX



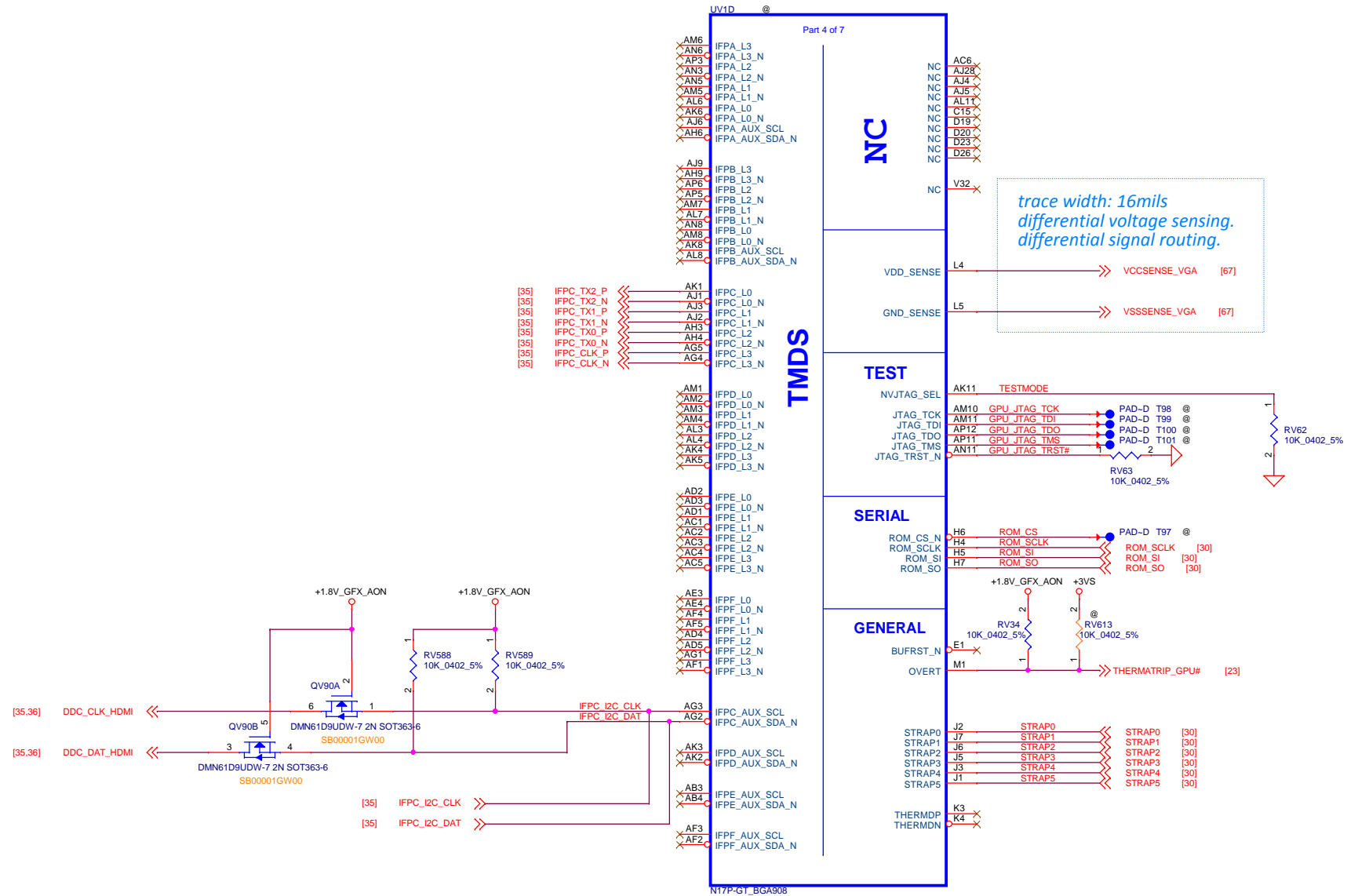
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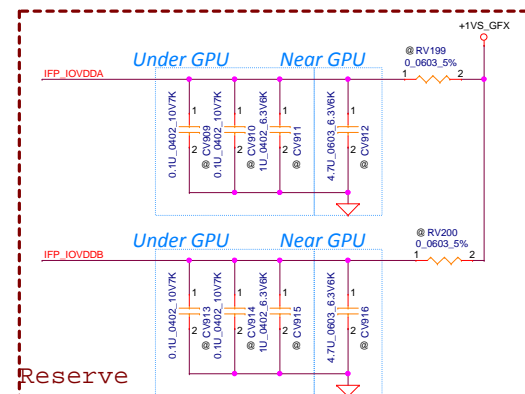






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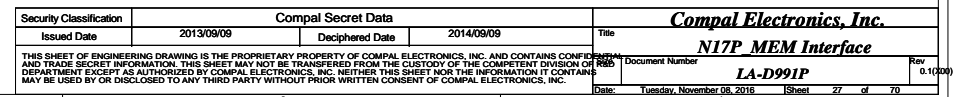


CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB CAL xTERM GND	60.4 ohm

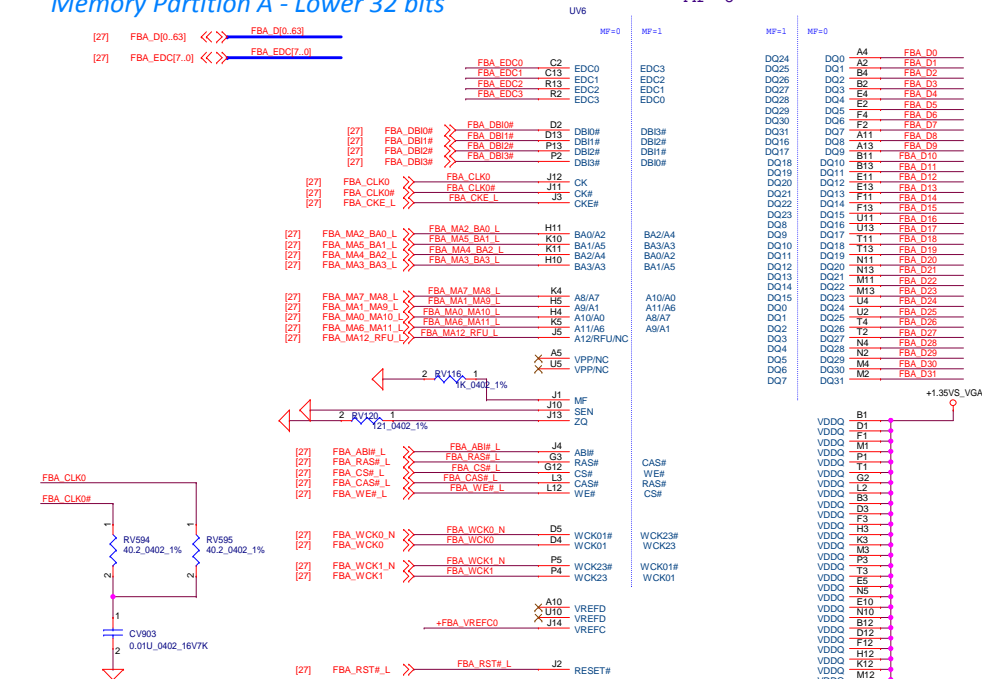


N17P-GT\_BGA908

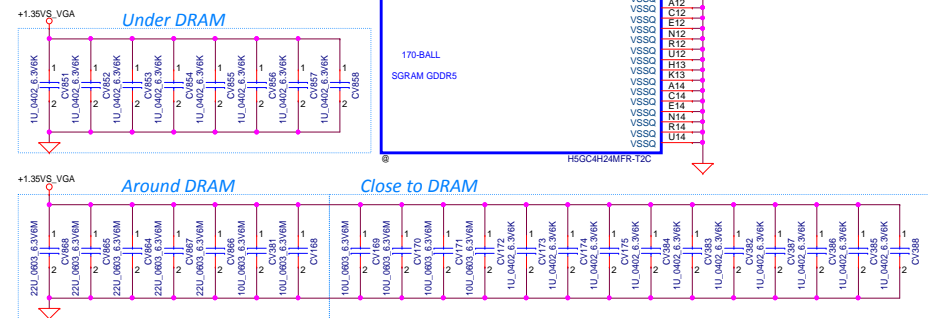
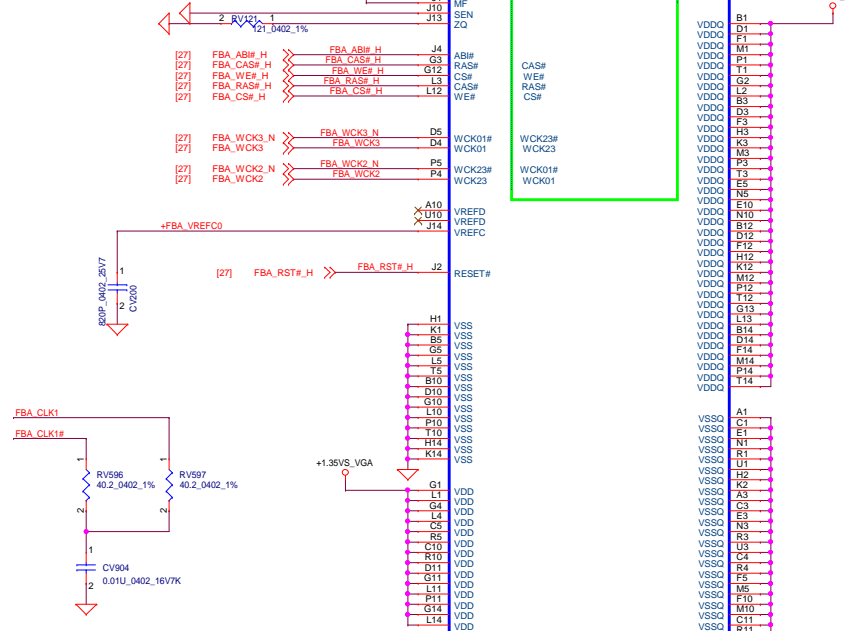
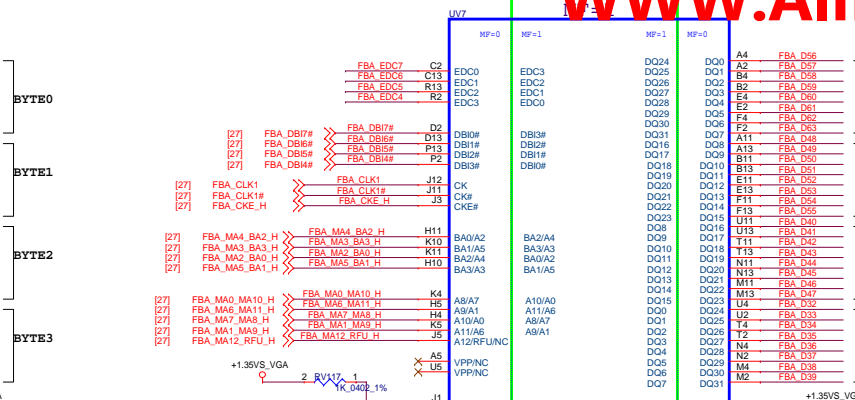
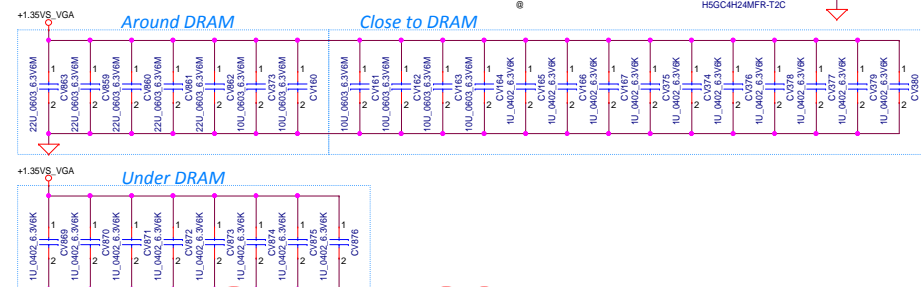
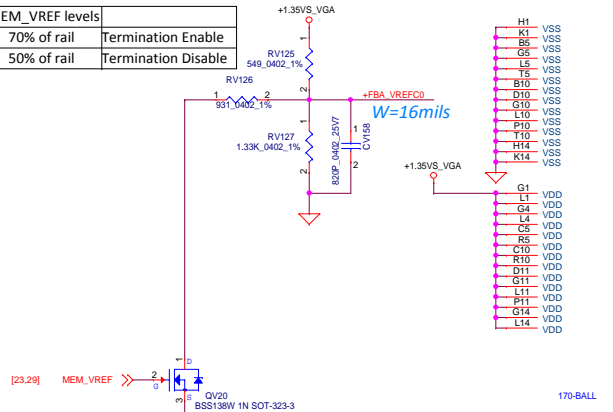
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Memory Partition A - Lower 32 bits

$$MF=0$$


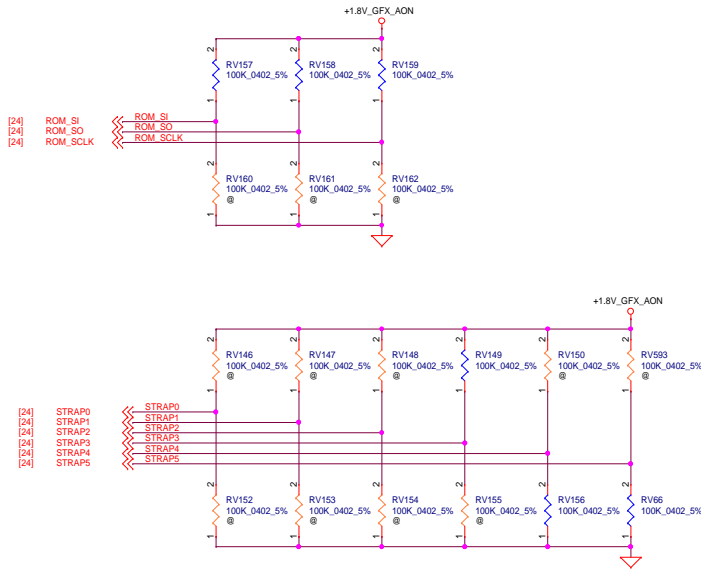
MEM_VREF levels	
70% of rail	Termination Enable
50% of rail	Termination Disable



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SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 1. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Allowed Memory Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V and 1.5V/ 1.5V See Note 2	8 Gb	256Mx32	Samsung	K4G80325FB-HC28	B-die	0x0	3500	N/A	Production candidate
				Micron	MT51J256M32HF-70-A	A-die	0x1	3500	N/A	Production candidate
				Hynix	H5GQ8H24MJR-R0C	M-die	0x2	3500	N/A	Post-production candidate

**Note:**

- For N17P-Gx, the maximum allowable memory case temperature is 85 °C.
- N17P-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. DVS is required to run WCLK > 3000 MHz.

Table 5.5 SMB ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

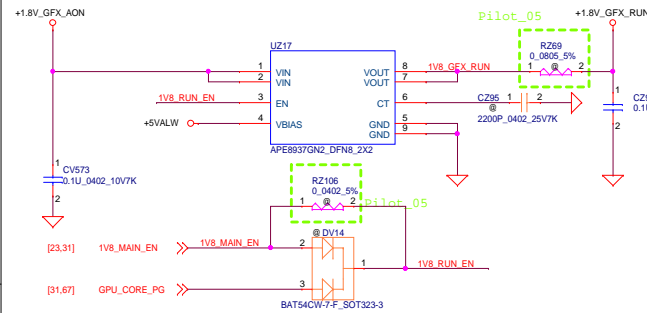
Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
8	H	H	H	ENABLED	disabled	disabled	disabled

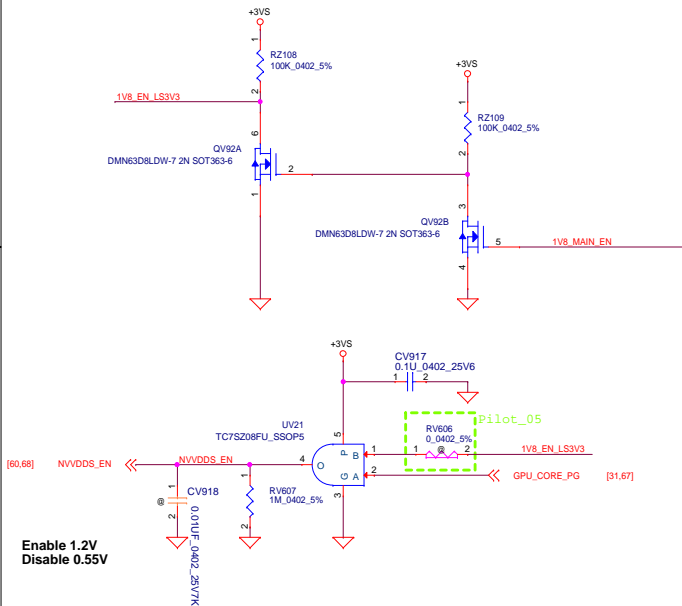
Total Display Links (HDMI, DP or DVI)					See This Row of Table 5.5
	Total Enabled for Audio (HDMI, DP or DVI)				
		Is eDP Supported on:			
		IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
1	1	--	--	--	8

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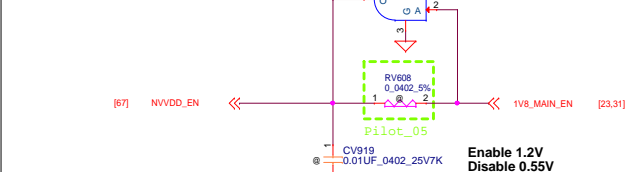
## +1.8V\_GFX\_RUN



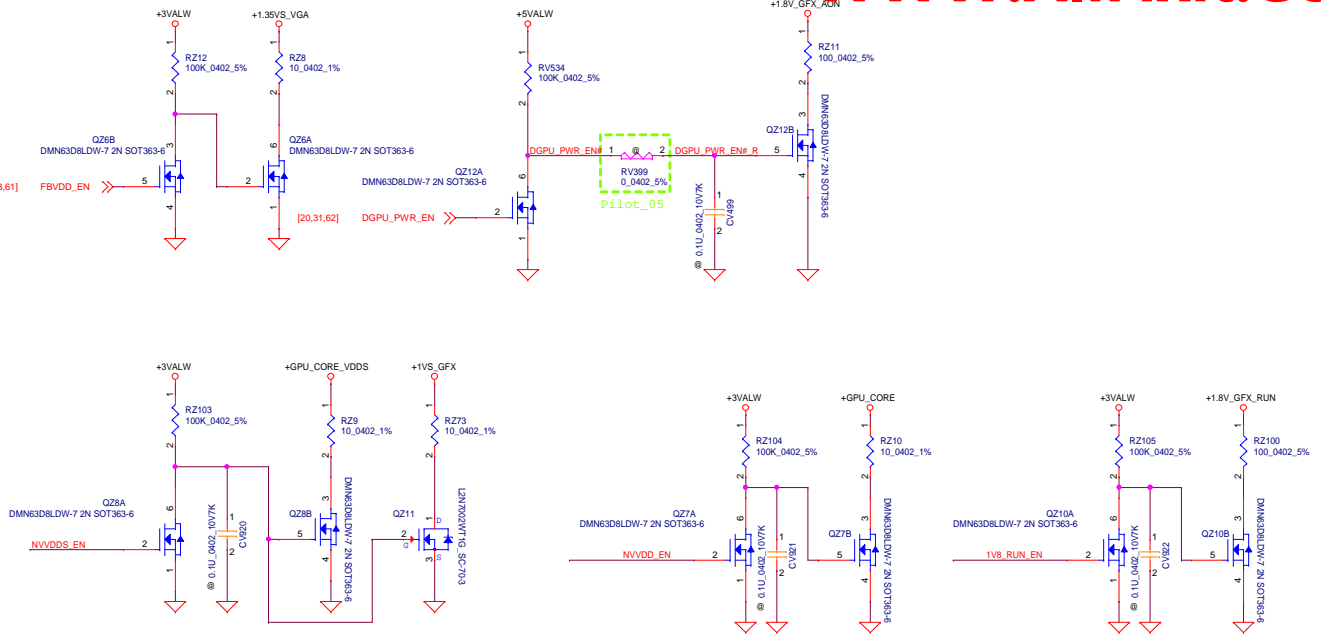
## NVDDDS Enable



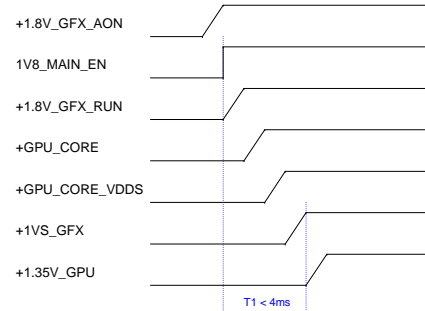
## NVDD Enable



## Discharge

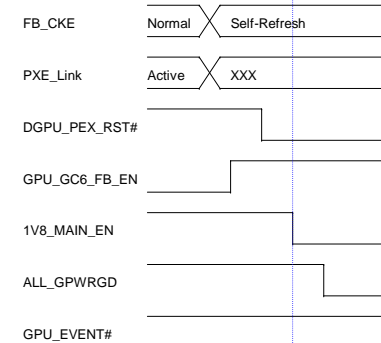


## GPU Power Up Sequence



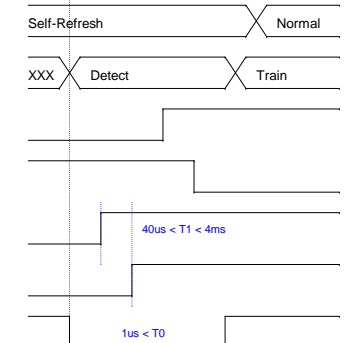
The ramp time for any rail must be more than 40us and less than 2ms.

## GPU GC6 Entry Sequence

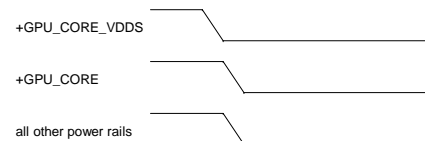


The entire entry/exit sequence must complete within 200 ms.

## GPU GC6 Exit Sequence

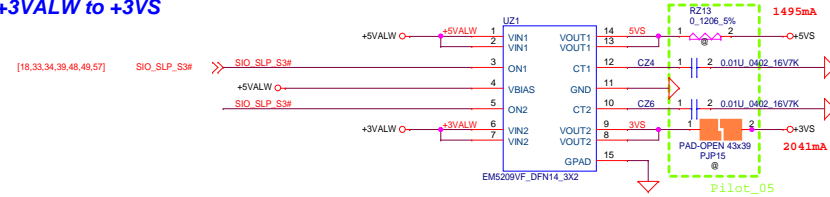


## GPU Power Down Sequence

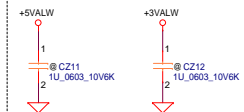


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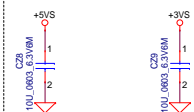
**+5VALW to +5VS**  
**+3VALW to +3VS**



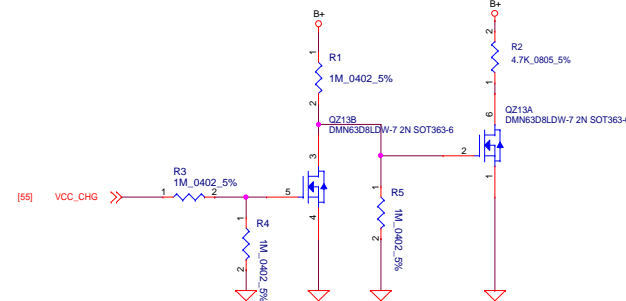
Close UZ1



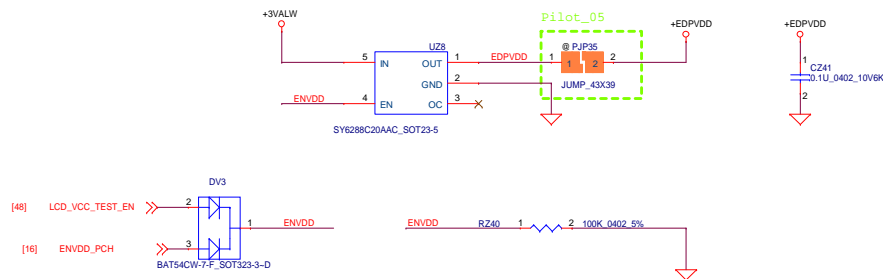
Close UZ1



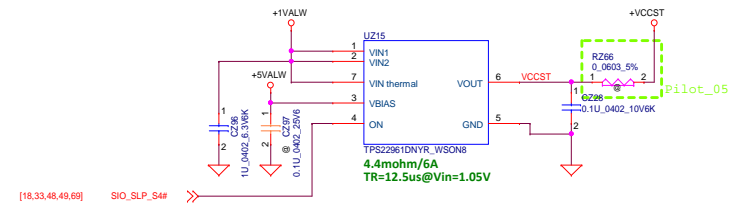
**B+ Discharge**



**eDP & Camera Load Switch**

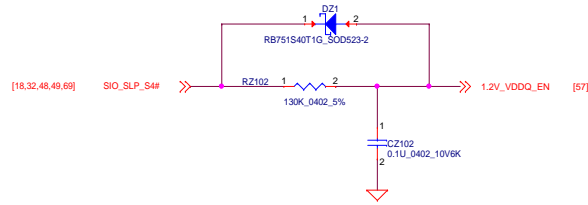


**+VCCST Load Switch**

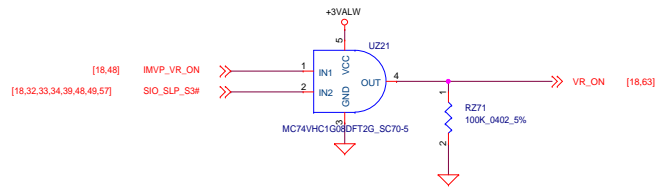
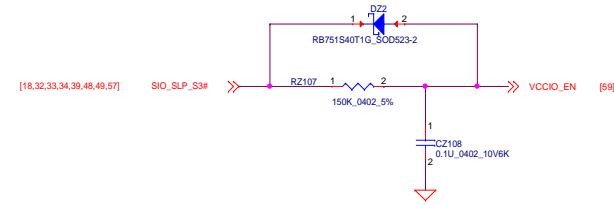




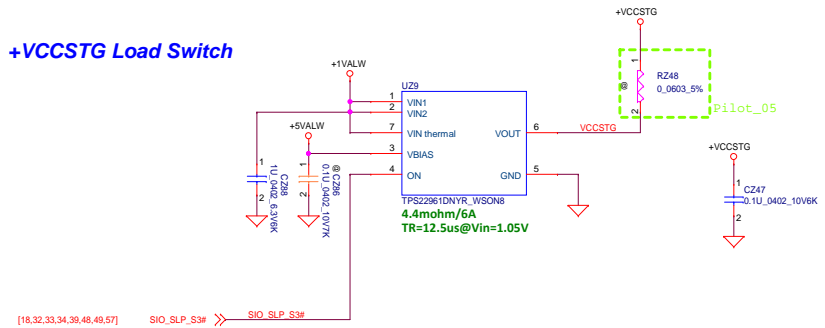
### +1.2V\_DDR Enable



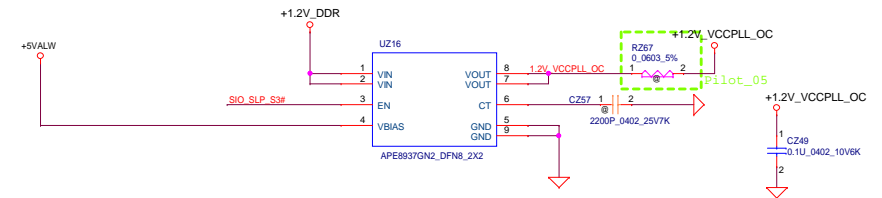
### +VCCIO Enable



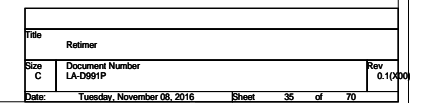
### +VCCSTG Load Switch



### +VCCPLL\_OC Load Switch

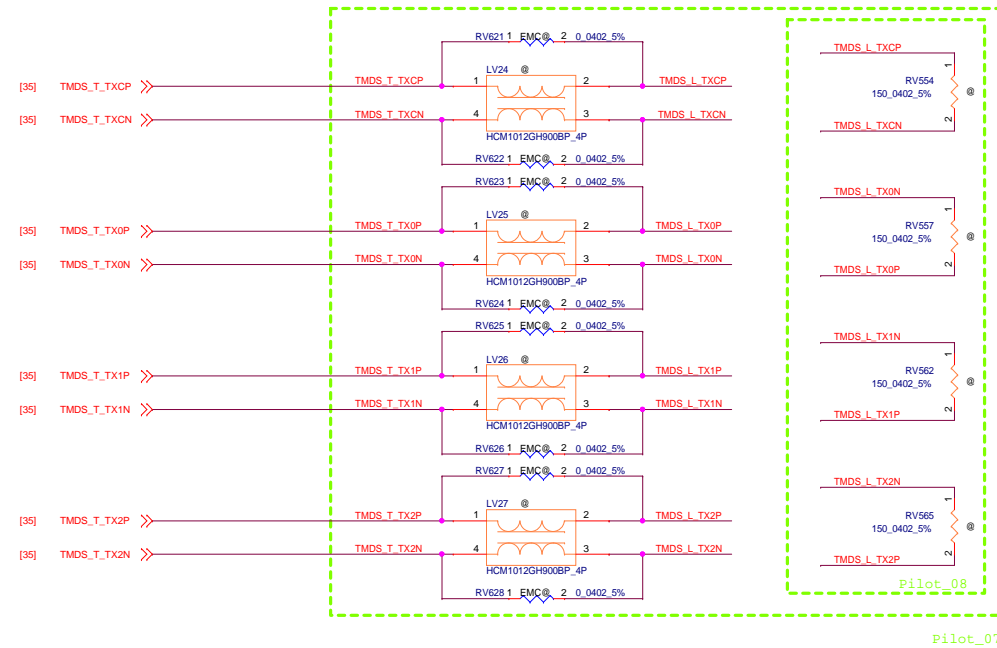


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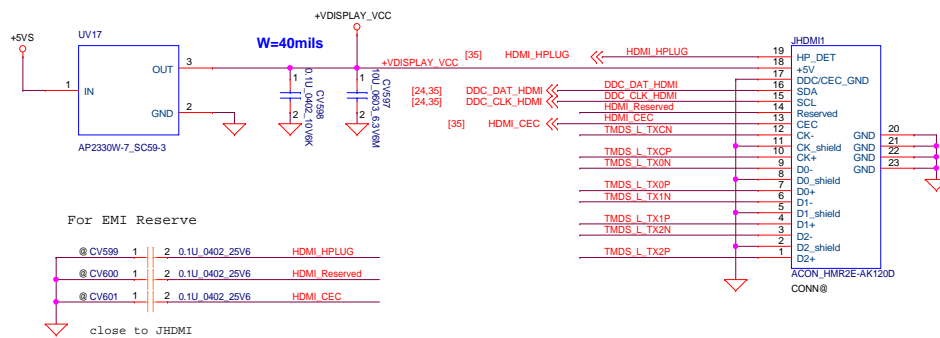


Place close to JHDMI1

Place between ESD and CM-Choke

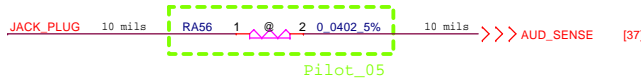
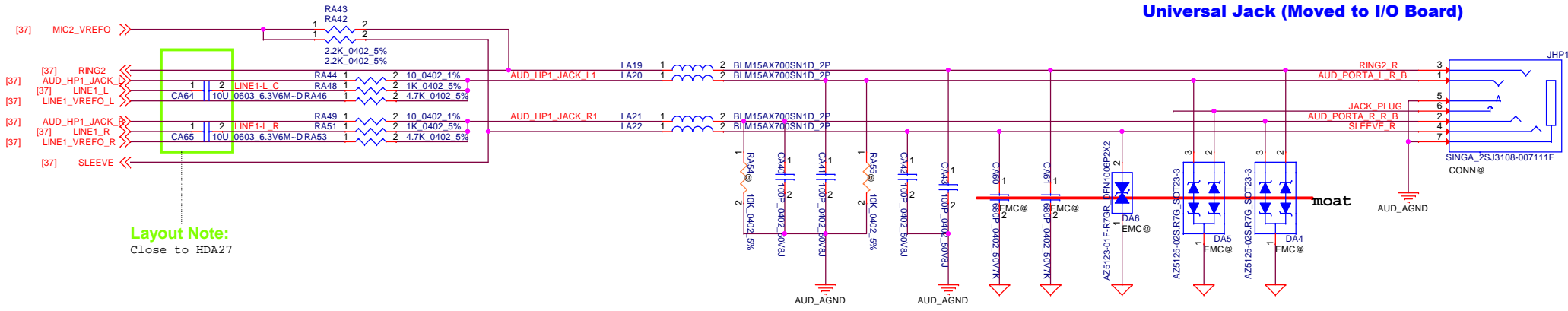
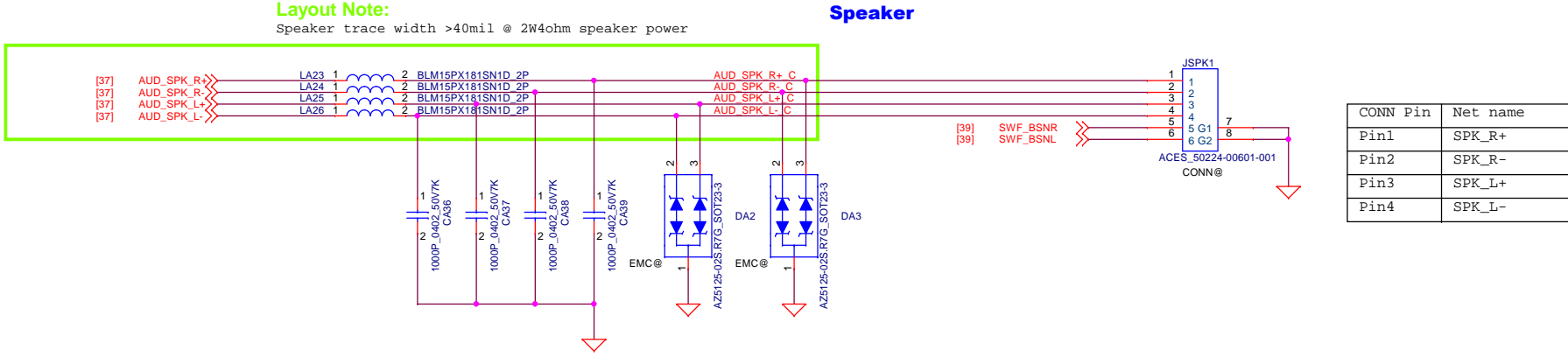


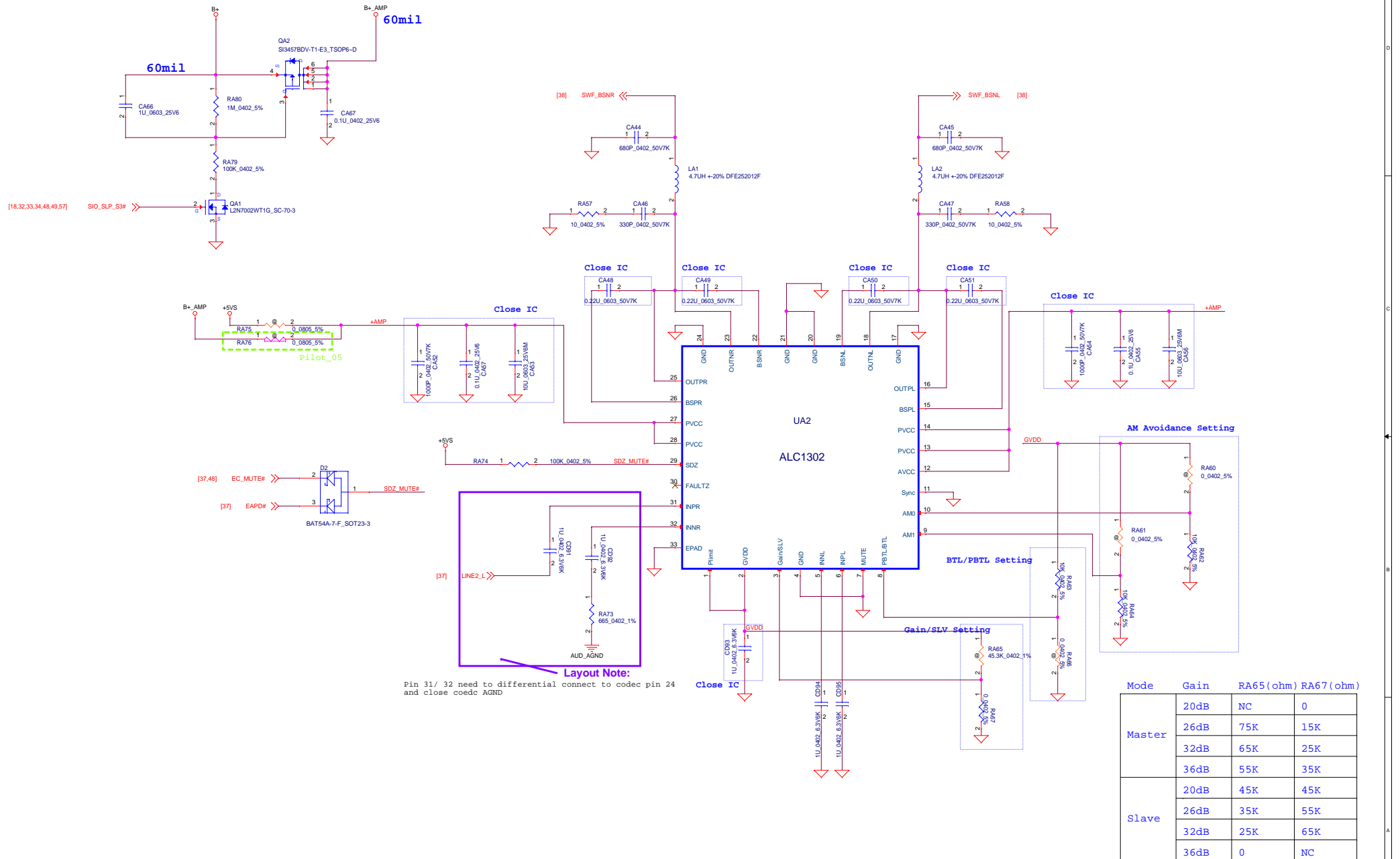
## HDMI conn



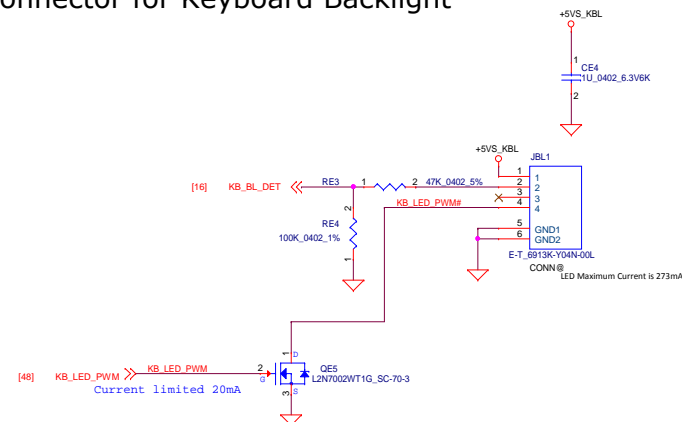
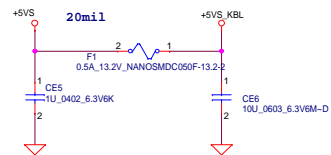
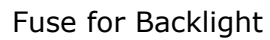
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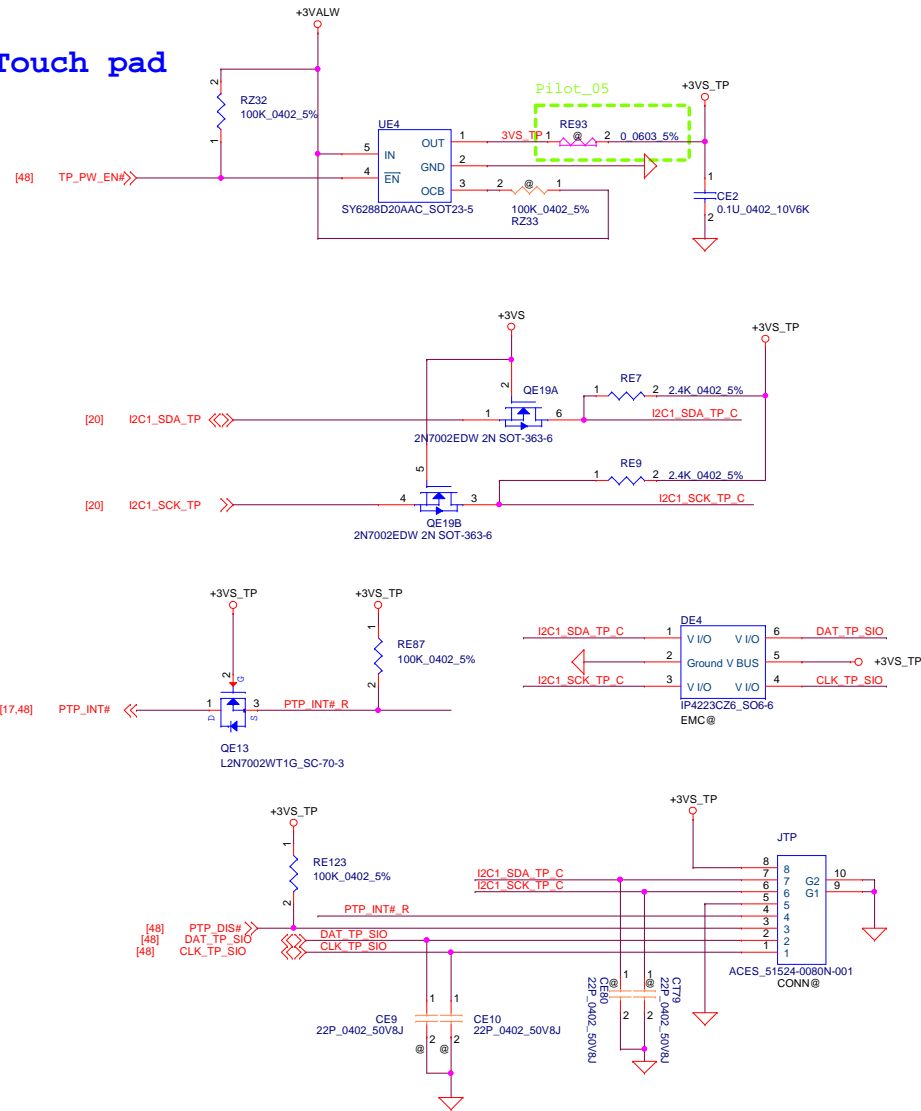
## Connector for Keyboard Backlight



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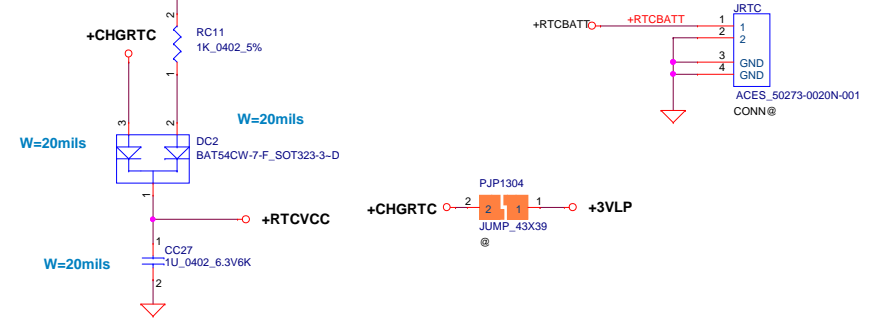


# Touch pad

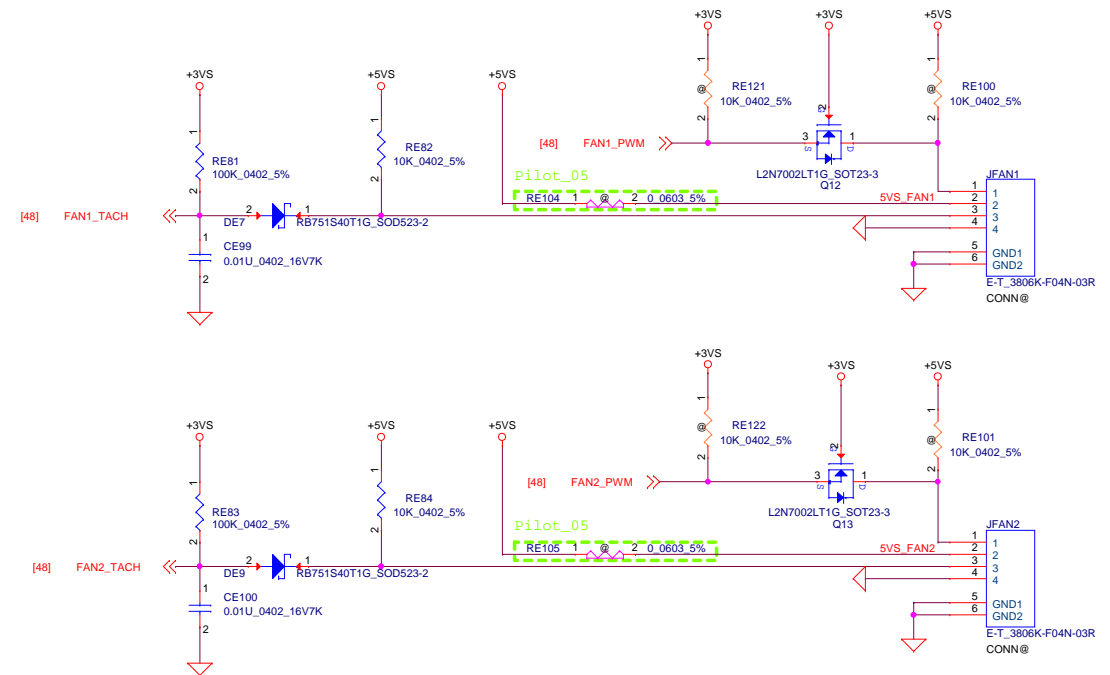


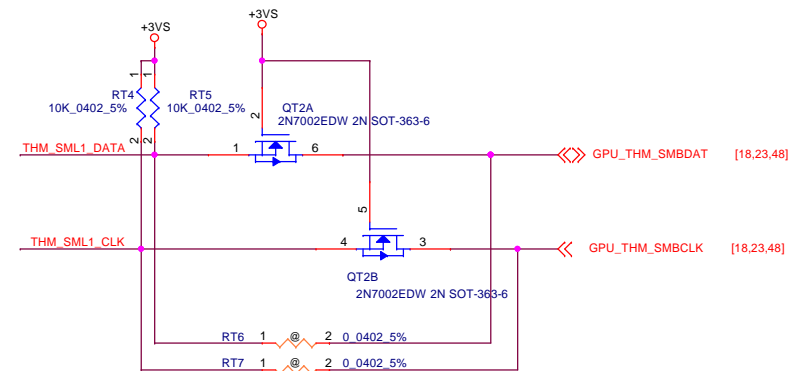
# RTC Battery non- Charge Function

## RTC Battery +RTCBATT



## PWM FAN

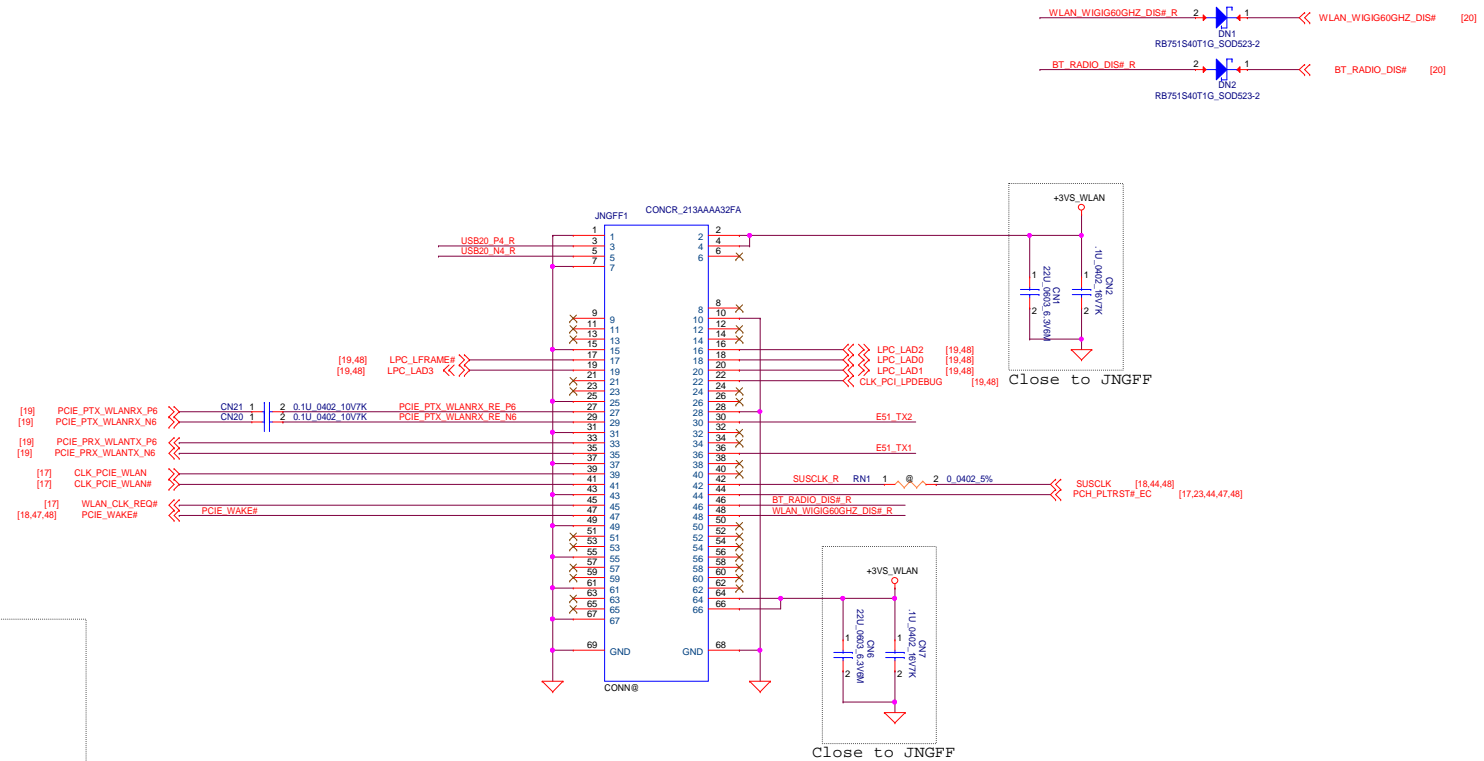
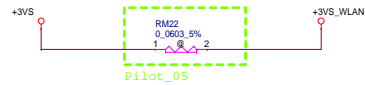




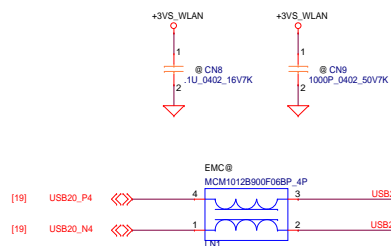
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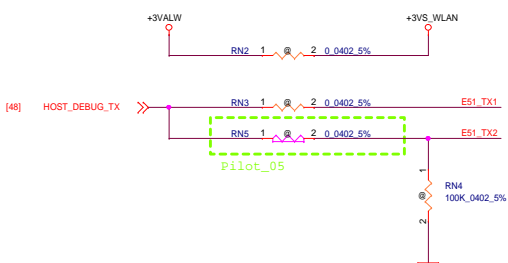
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Reserve for EMI

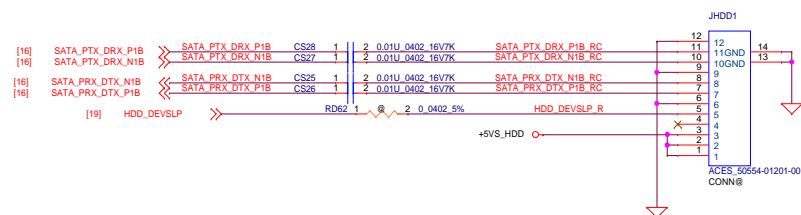
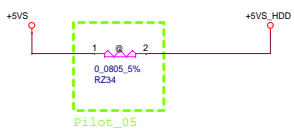


Reserve for NGFF Debug Card



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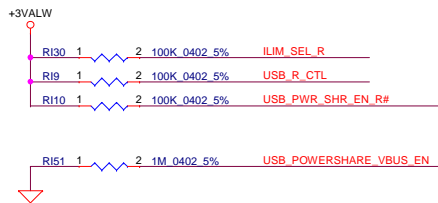
**HDD CONN**



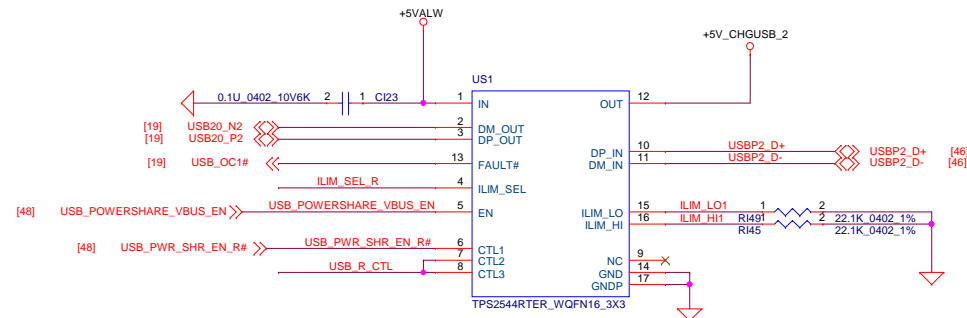
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					0.1(000)
Size	Document Number				
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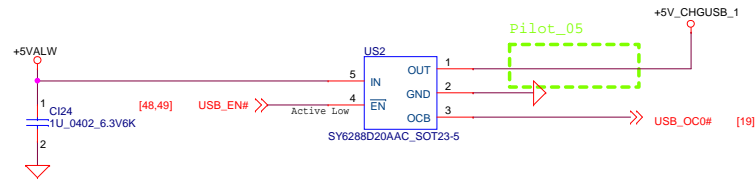
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

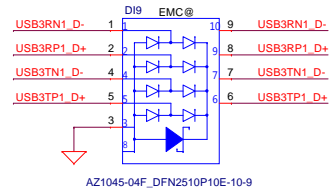
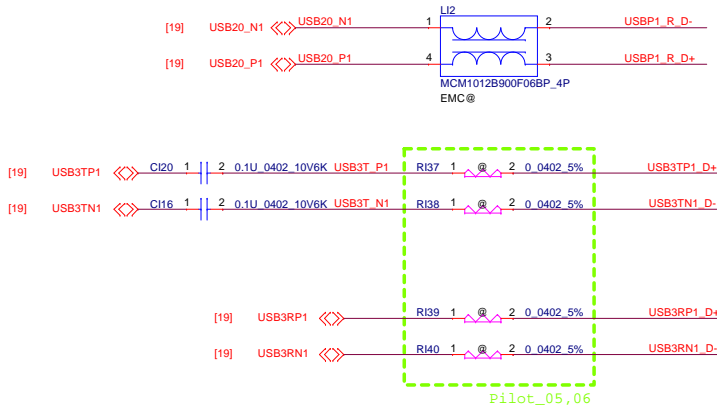


## USB3.0 / USB2.0 Port1

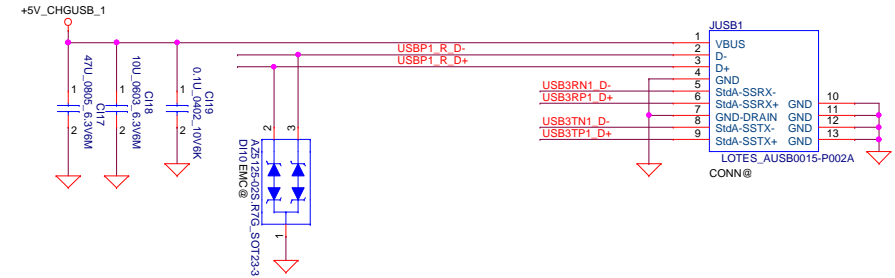




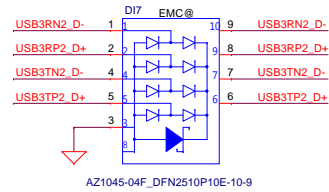
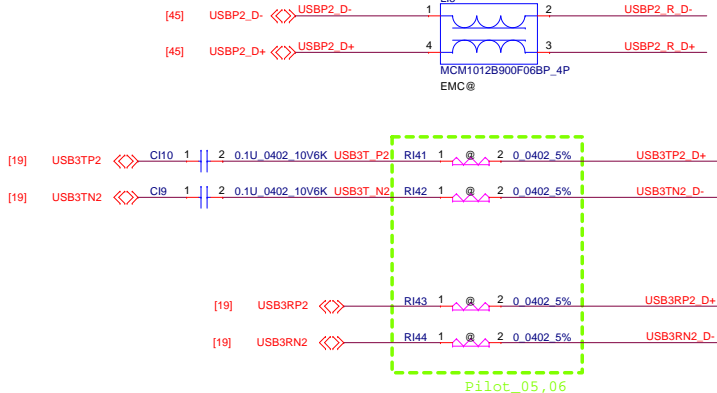
## USB3.0 / USB2.0 Port1



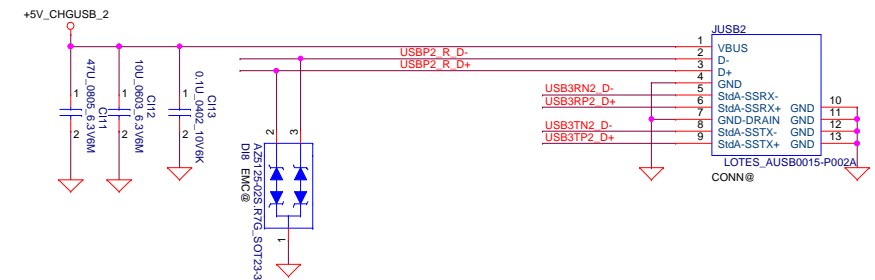
Place close to JUSB1



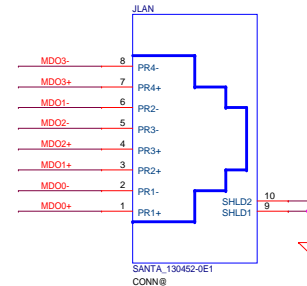
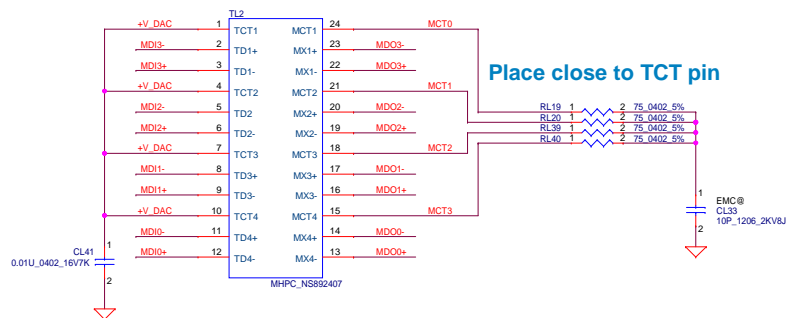
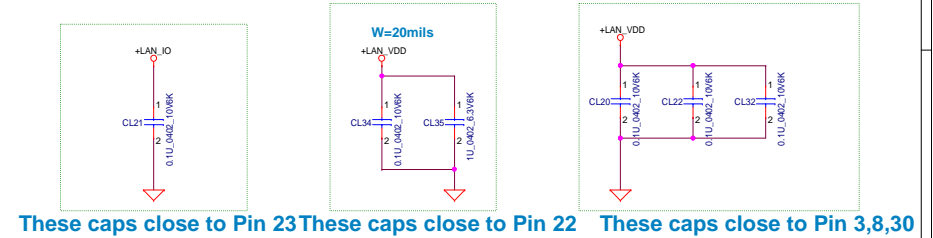
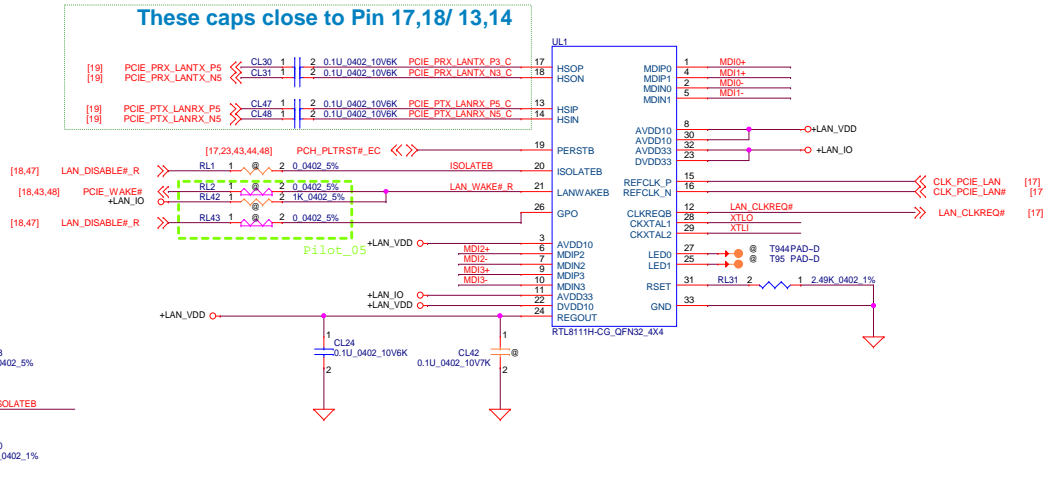
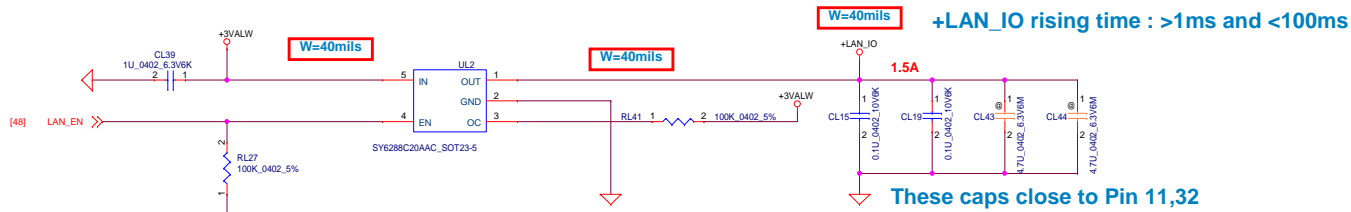
## USB3.0 / USB2.0 Port2 (Power share)



Place close to JUSB2



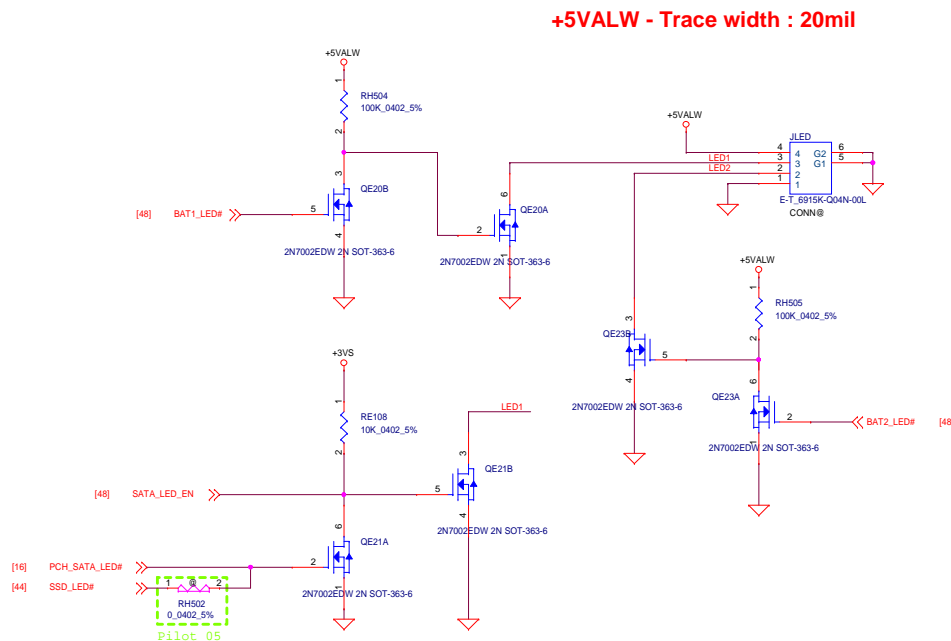
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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	USB conn.
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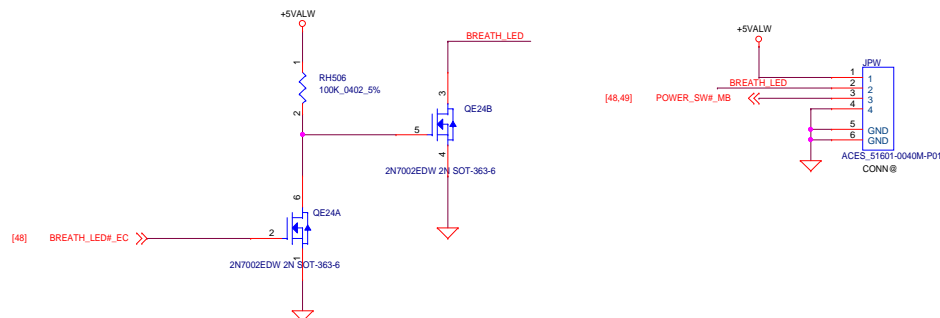




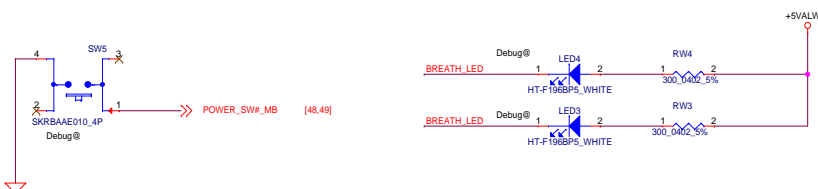
## LED Board Connector



TO PWR BOARD

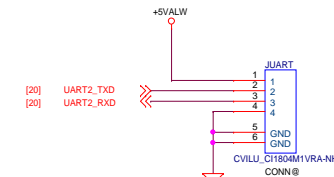


## Power Button & LED (Reserve)

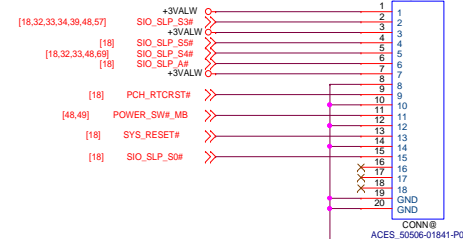


## I/O & APS & UART CONN

## UART CONN

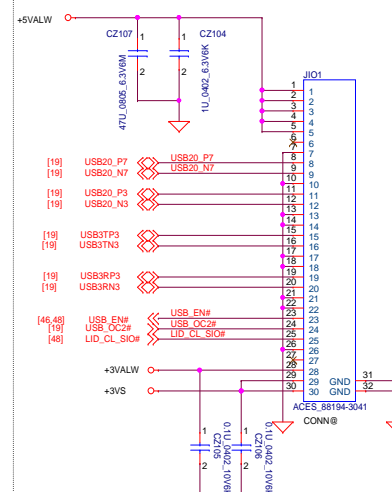


APS CONN

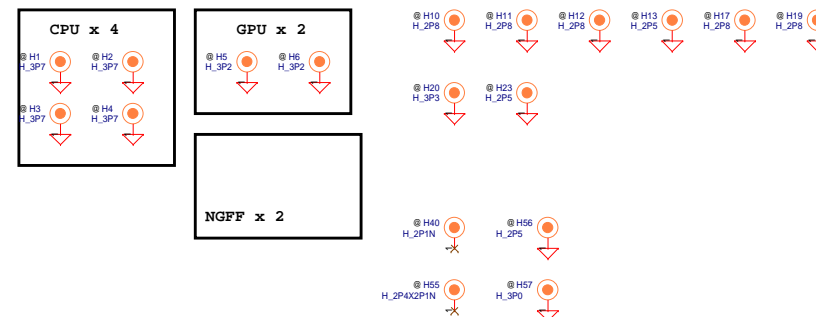


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## I/O CONN



## Screw Hole

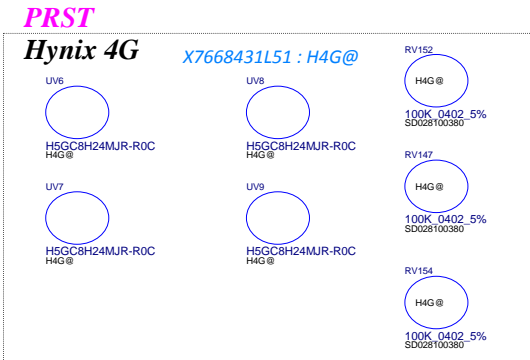
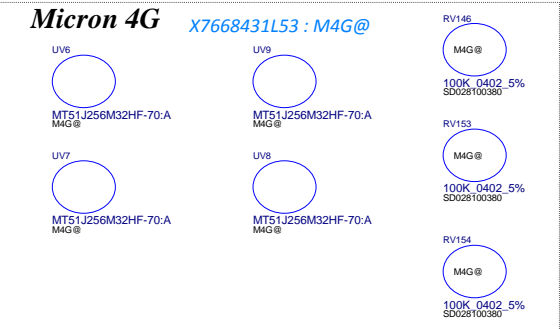
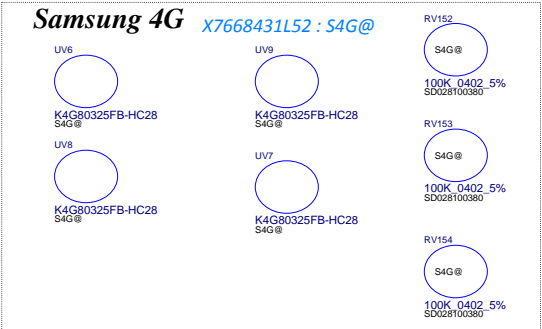
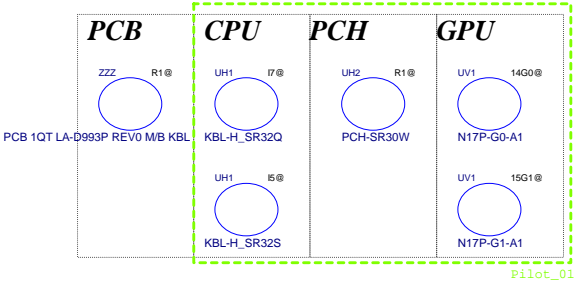


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				Size	Document Number	Rev
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MODEL NAME : *BBV00/ BBV10*  
PCB NO : *LA-D993P*

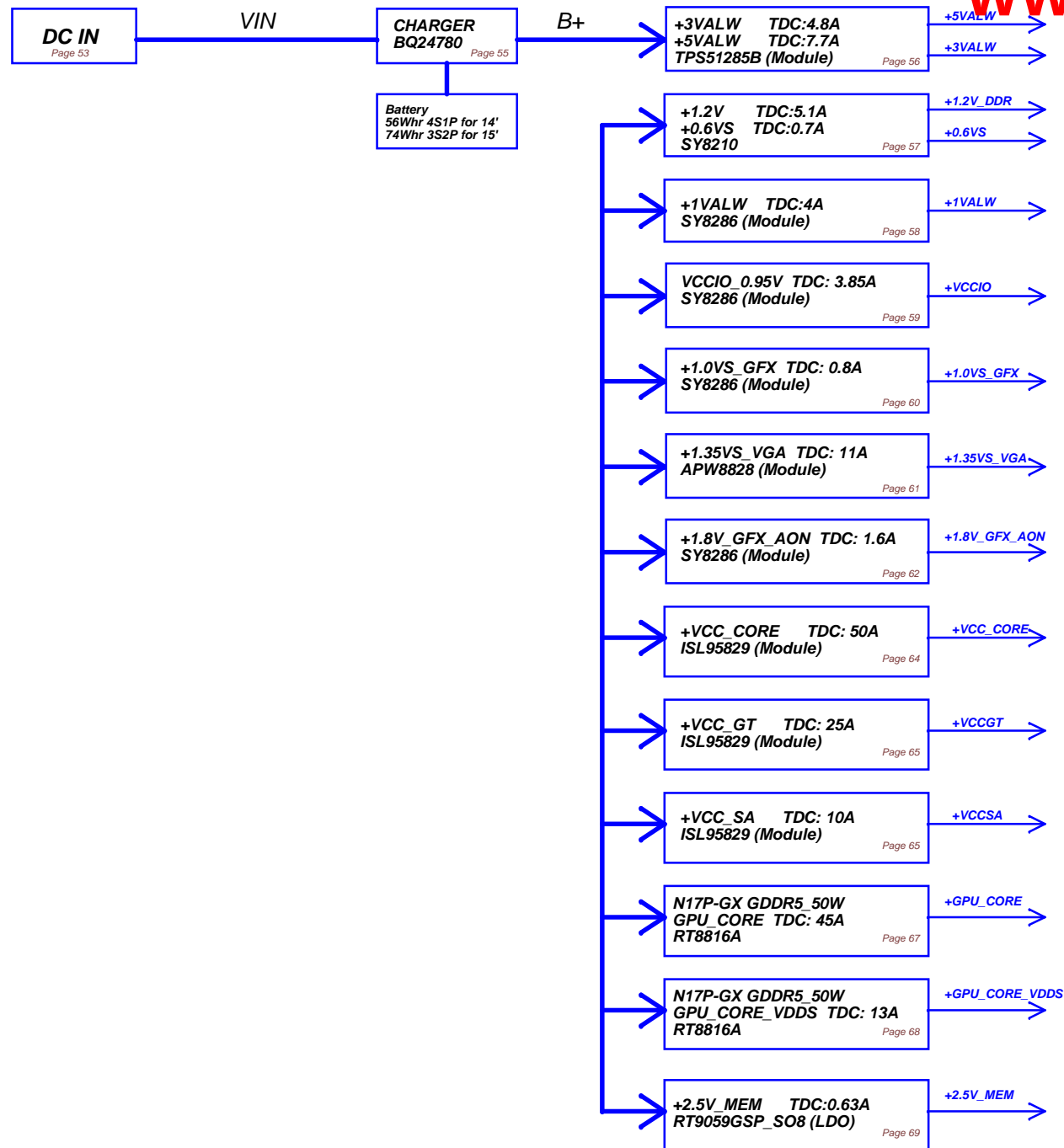
Bom Structure

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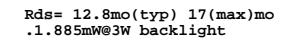
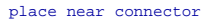


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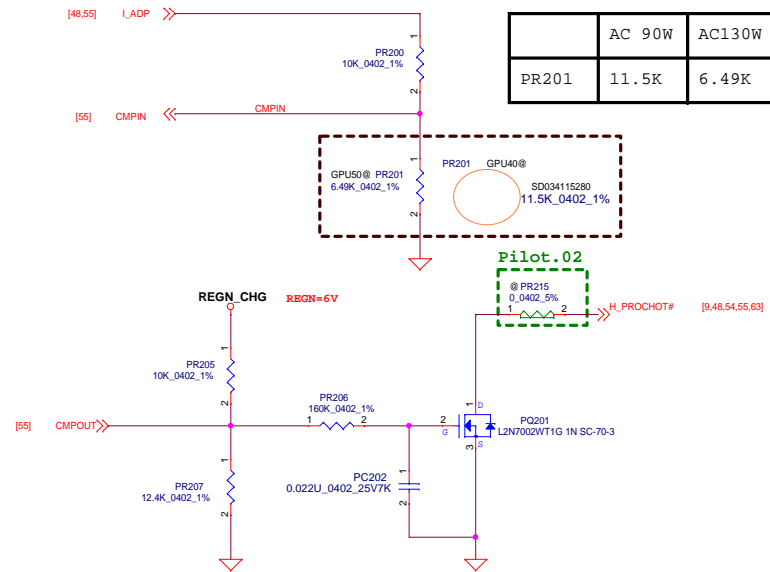
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	Power Block Diagram
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				Date	Tuesday, November 06, 2018
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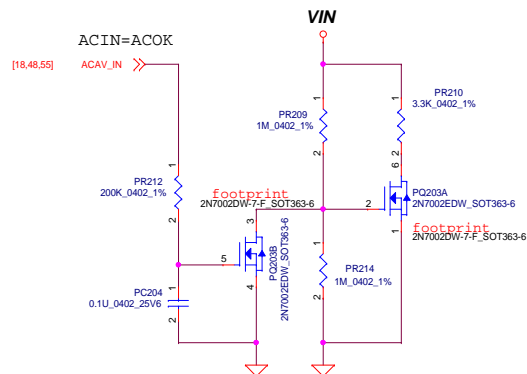
## Smart Adapter circuit (39.1)

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				Size	Document Number	Rev
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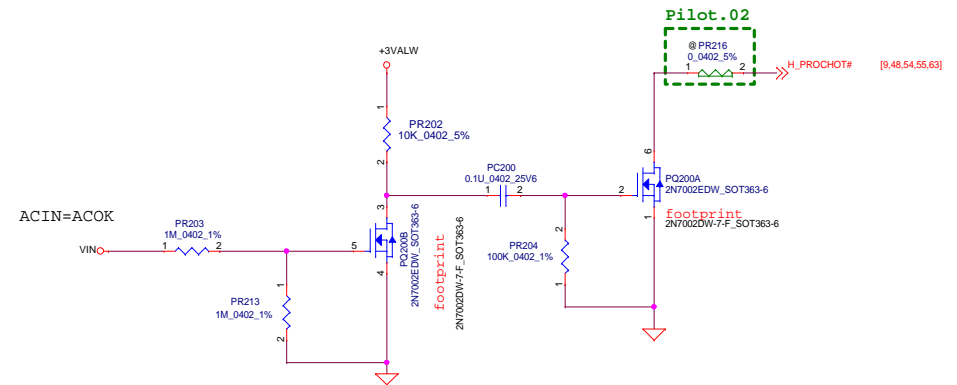
When  $CMPIN > V_{ref}(2.3V/1.3V)$   
CMPOUT=floating



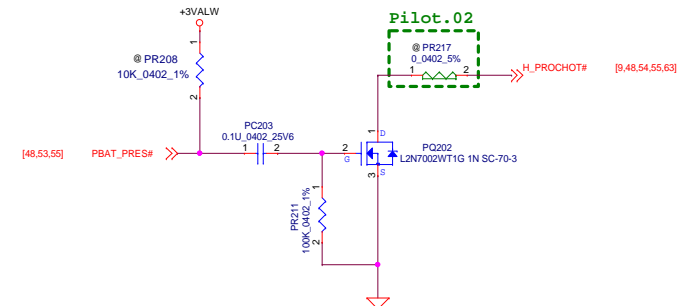
ENG0012879 Circuit-1  
Delay Adapter OC H\_PROCHOT# 2ms while  
Hybrid power transition



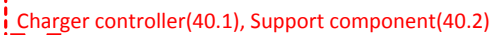
## Erp lot 6 circuit



Ref ENG0012879 Circuit-2  
HW Asserts H\_PROCHOT# when ac adapter  
is being unplugged and keep low for 10ms  
until SW prochot# is issued by EC



Ref ENG0012879 Circuit-4  
HW Asserts H\_PROCHOT# when battery  
is being unplugged and keep low for 10ms  
until SW prochot# is issued by EC

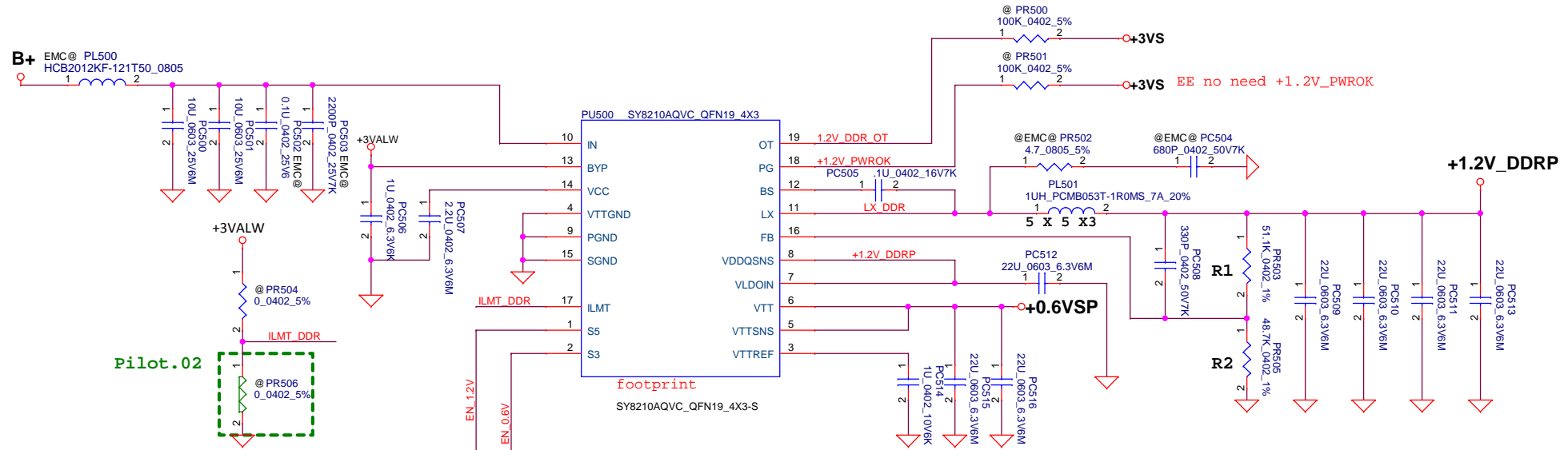


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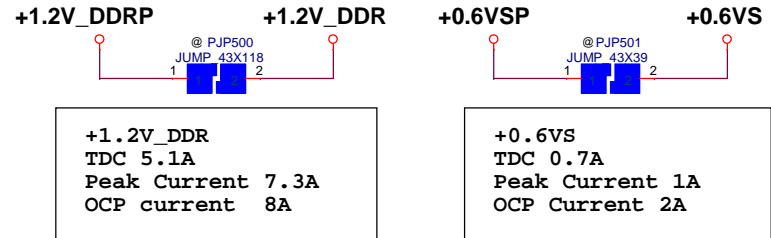


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high +1.2V\_DDR OCP set 8A

VFB=0.6V  
 $V_{out}=0.6V * (1+R1/R2)$   
 $V_{out}=1.2V$   
 $F_{sw}=600KHz$   
 600Khz  
 $I_{coul}=0.542A@19.5V$   
 $IL=1.88A@19.5V$   
 $ripple=6.32mV@19.5V$

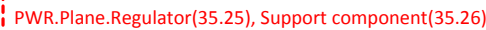
Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Standby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off



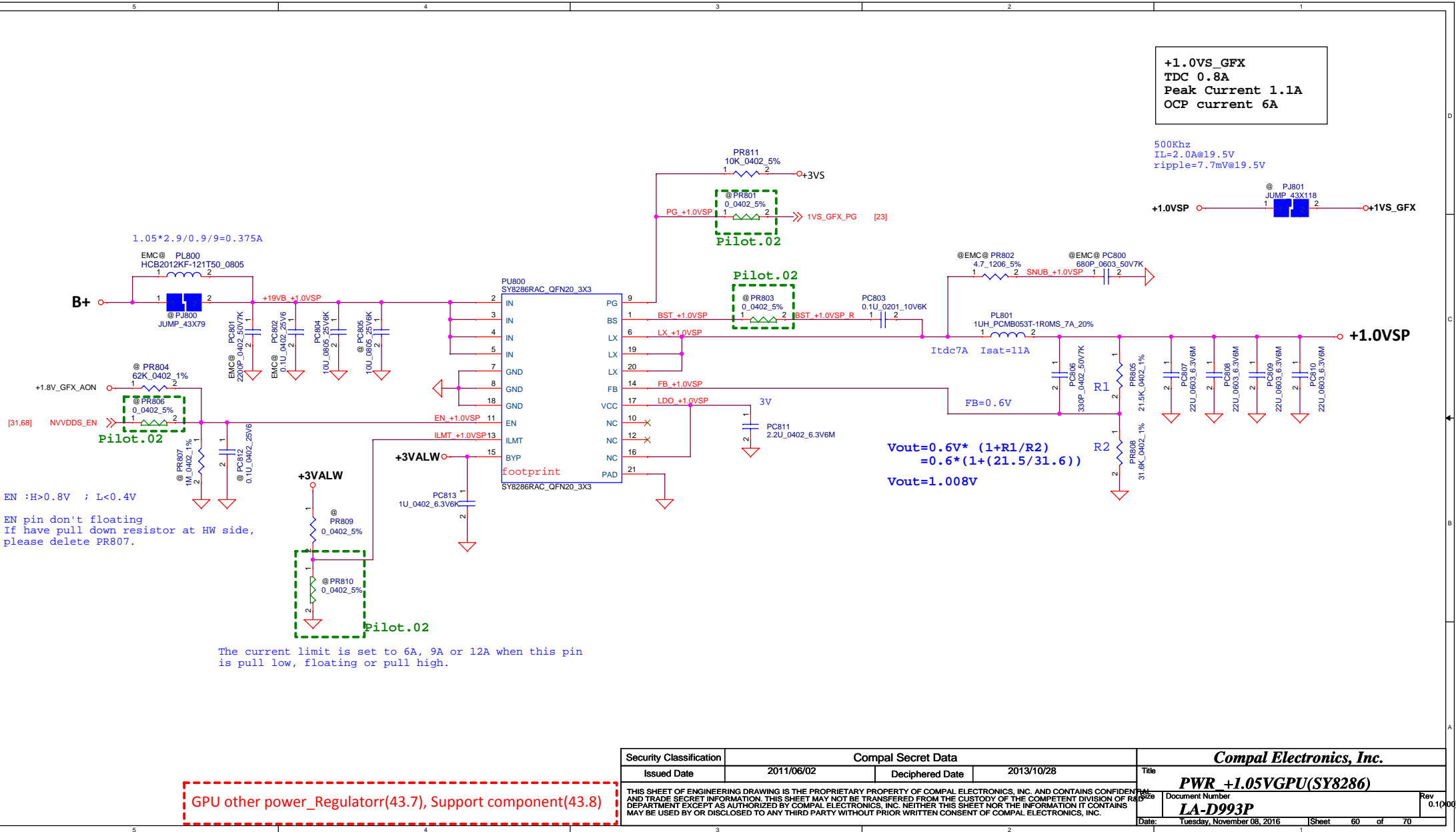
DDR controller(35.3), Support component(35.4)

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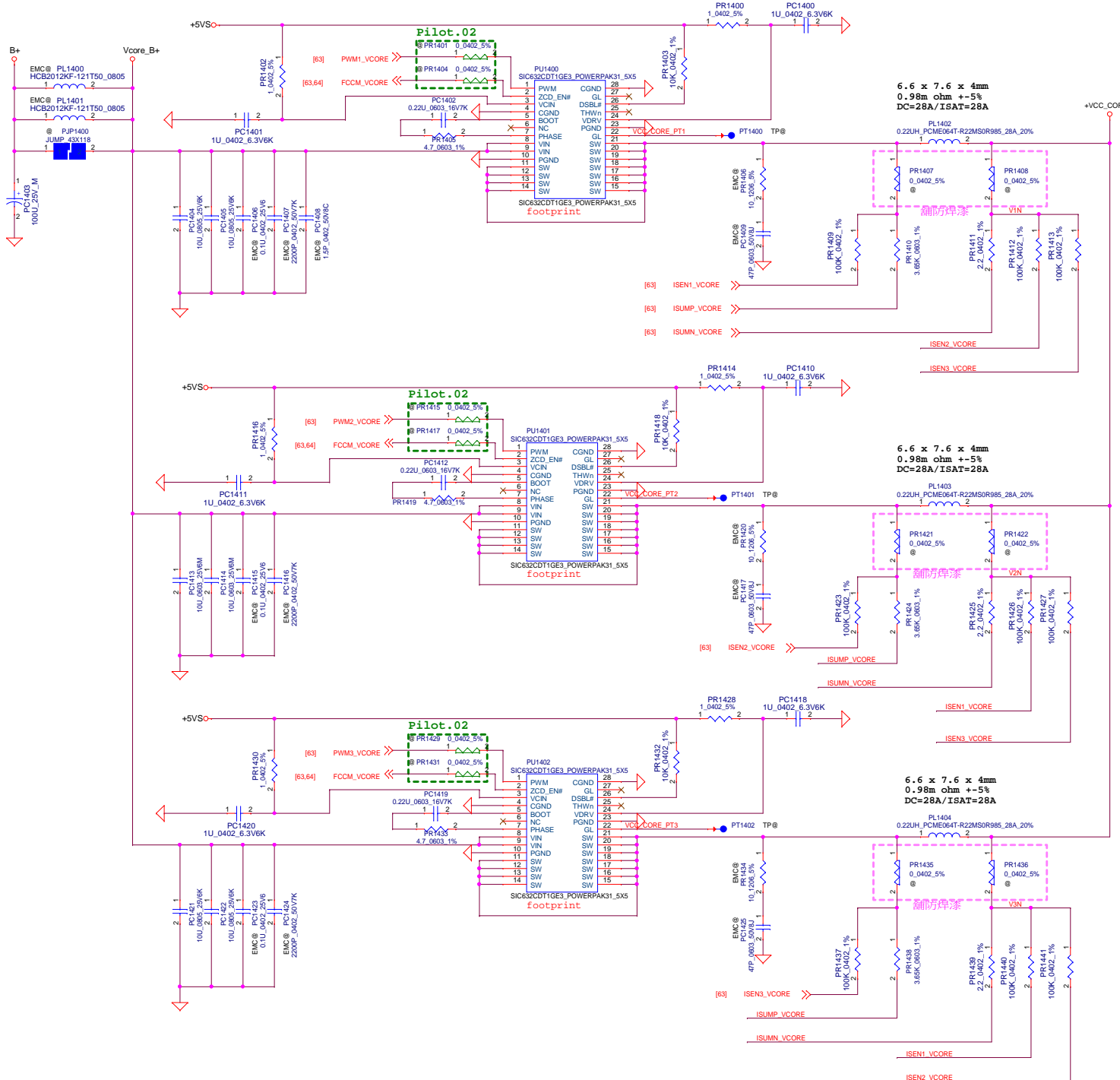






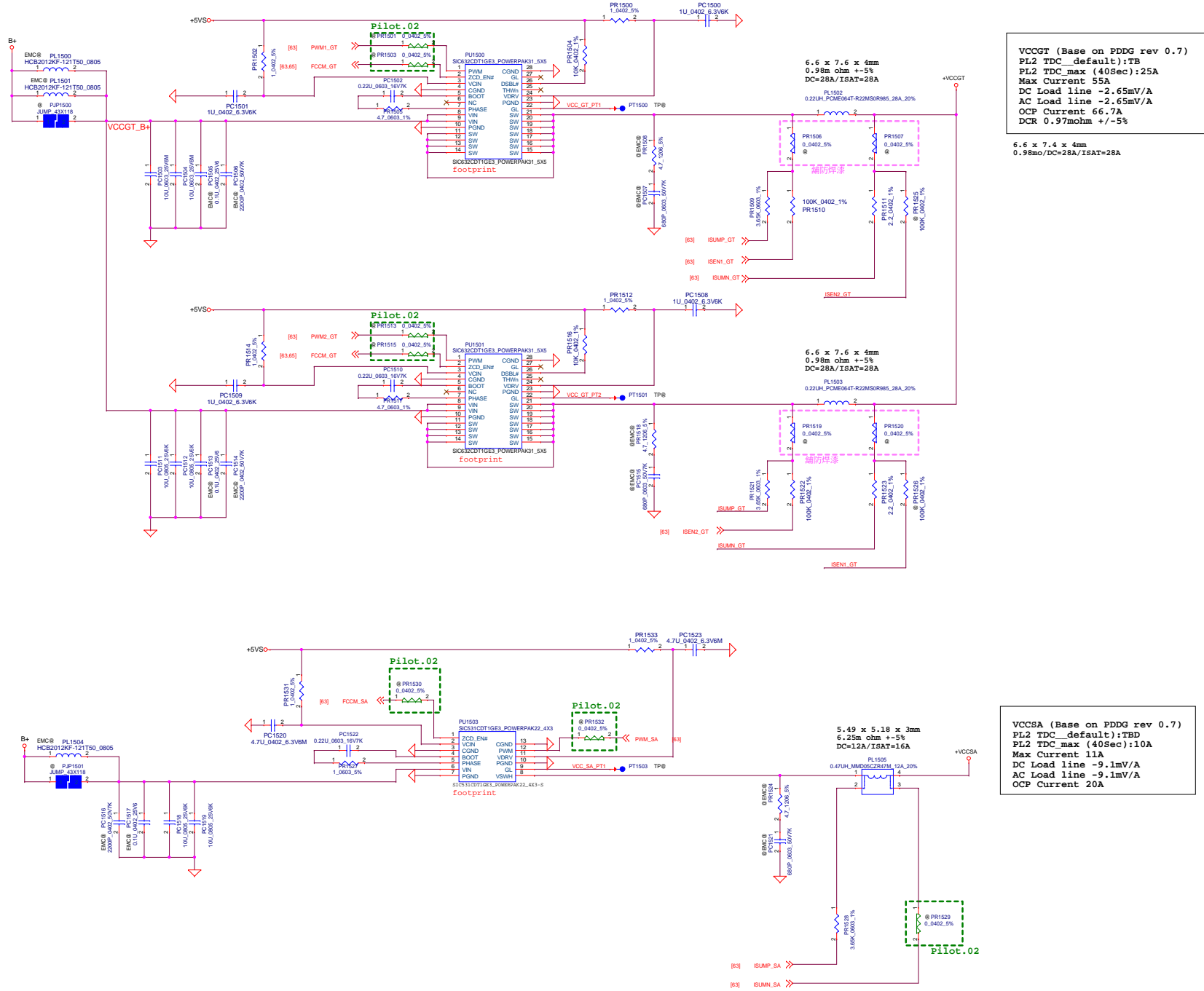




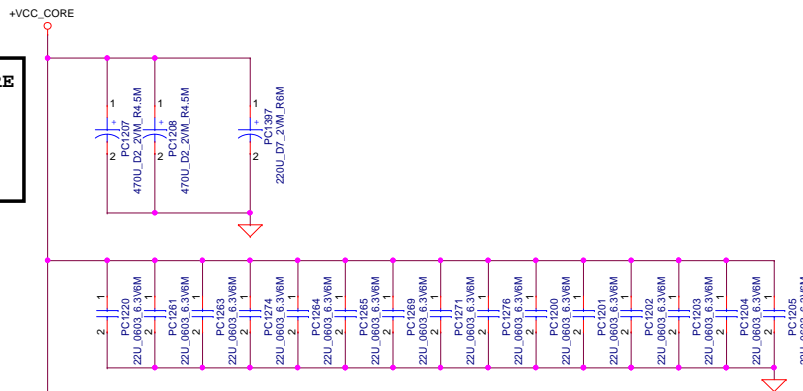


VCC\_core (Base on PDBG rev 0.7)  
 PL2 TDC\_default):TB  
 PL2 TDC\_max (40sec):50A  
 Peak Current 68A  
 DC Load line -1.8mV/A  
 AC Load line -1.8mV/A  
 OCP Current 83.2A  
 DCR 0.97mohm +/-5%



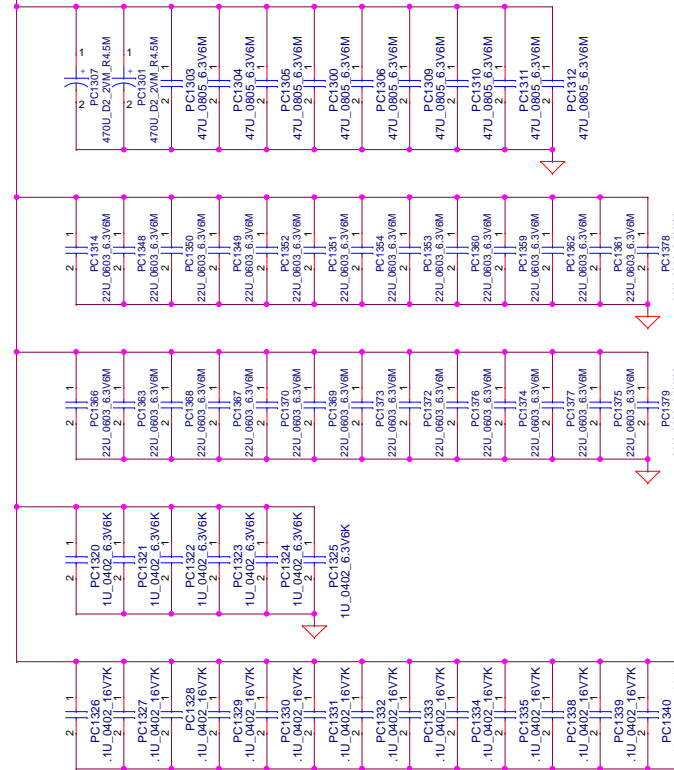


**+VCC\_CORE**  
 470uF\*2  
 22uF\*15  
 220uF\*1  
 1uF\*6  
 .1uF\*15



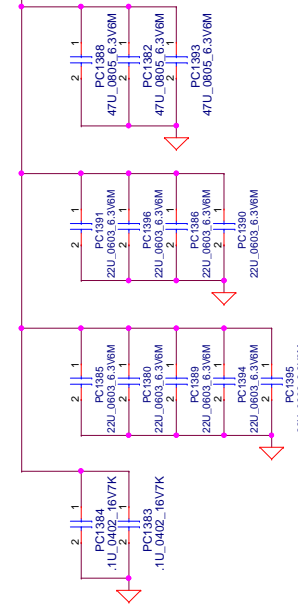
+VCCGT

**+VCCGT**  
 470uF\*2  
 47uF\*9  
 22uF\*26  
 1uF\*6  
 .1uF\*15



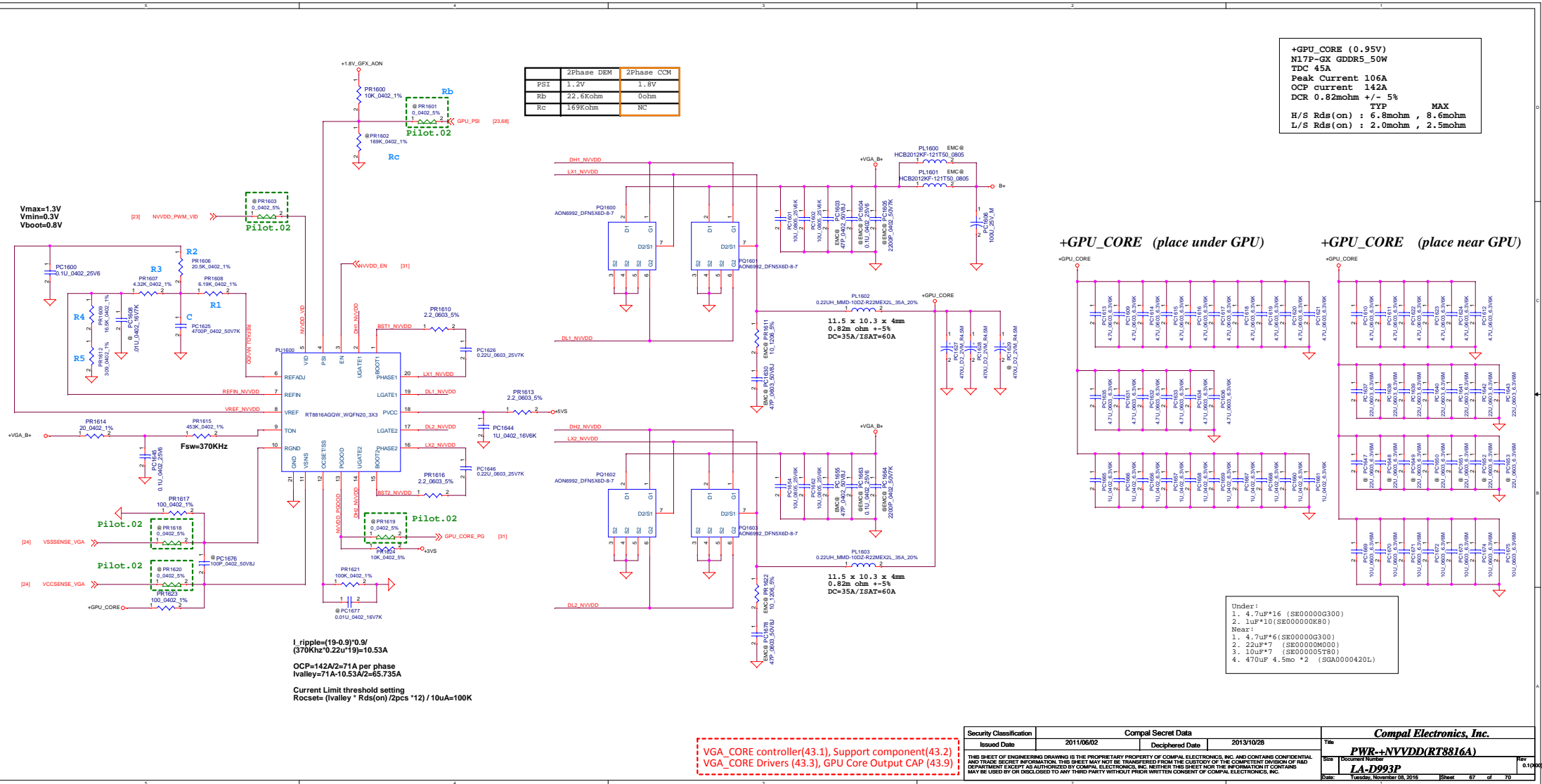
+VCCSA

**+VCCSA**  
 47uF\*3  
 22uF\*9  
 .1uF\*2



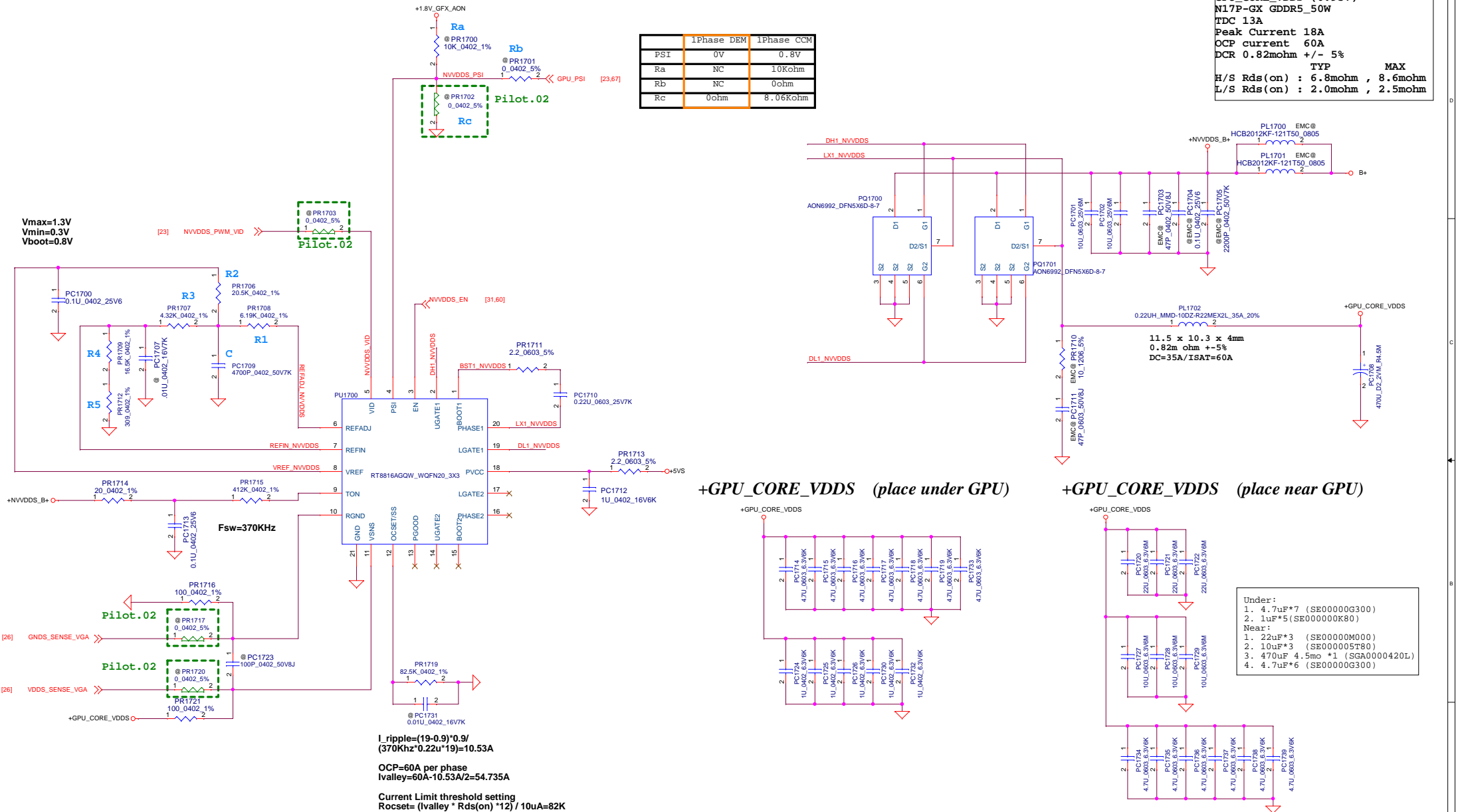
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Vcc\_CORE output CAP(36.4), Vcc\_GT output CAP(36.5),  
 Vcc\_SA output CAP(36.6)



GPU\_CORE\_VDD5 (0.95V)  
N17P-GX GDDR5\_50W  
TDC 13A  
Peak Current 18A  
OCP current 60A  
DCR 0.82mohm +/- 5%  
H/S Rds(on) : 6.8mohm , 8.6mohm  
L/S Rds(on) : 2.0mohm , 2.5mohm

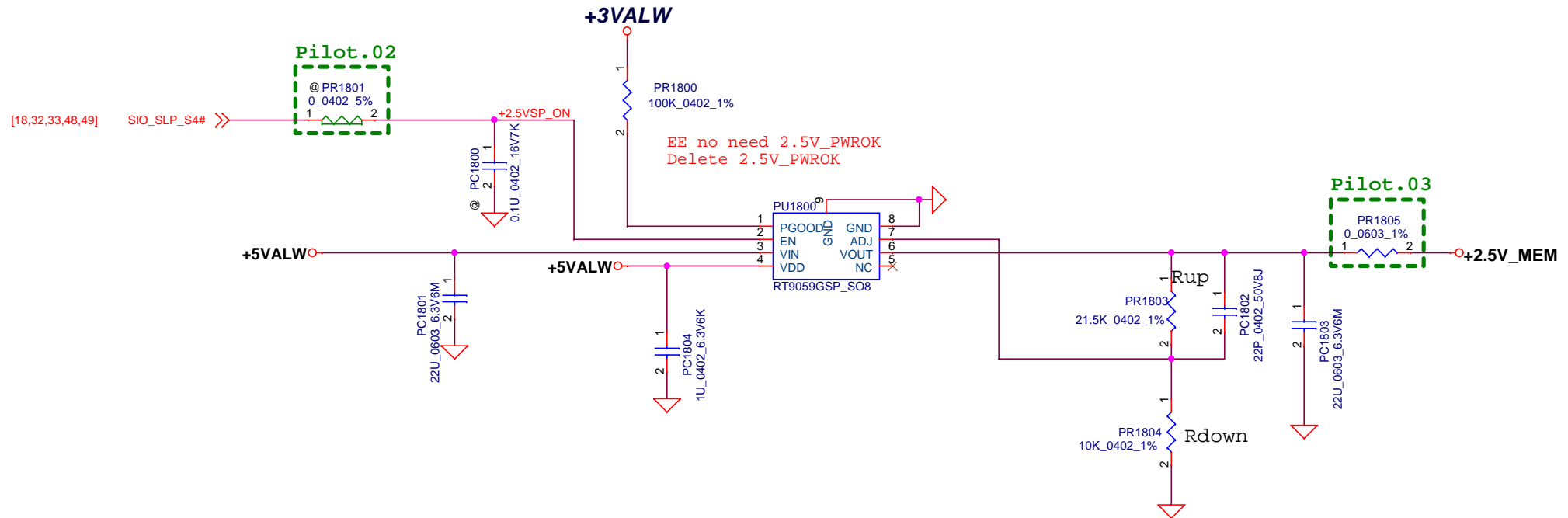
	1Phase DEM	1Phase CCM
PSI	0V	0.8V
Ra	NC	10Kohm
Rb	NC	0ohm
Rc	0ohm	8.06Kohm



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2.5V\_MEM controller(35.13), Support component(35.14)

+2.5V\_MEM  
TDC 0.63A  
Peak Current 0.9A  
OCP Current 3.5A



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				Size	Document Number
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