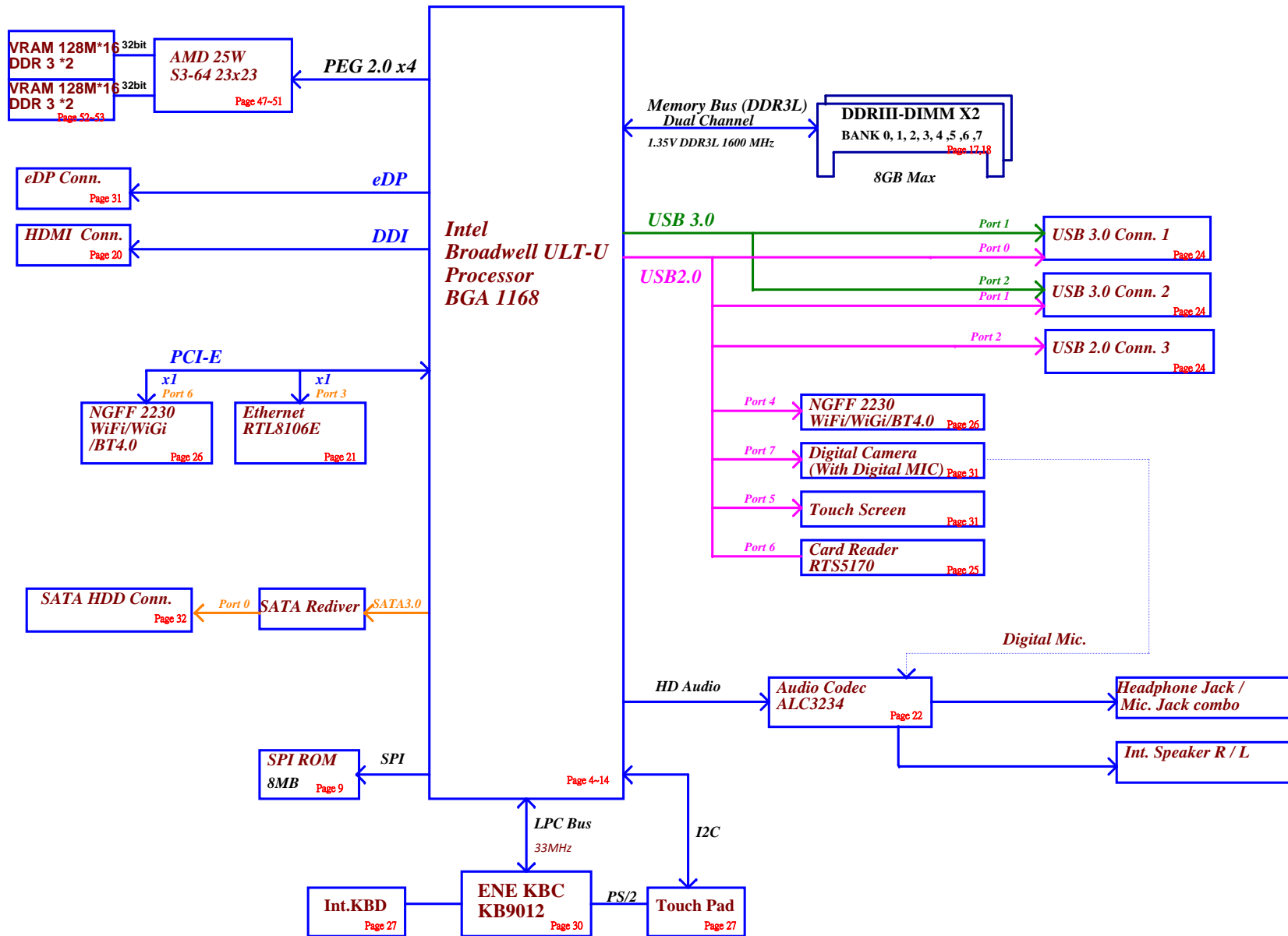


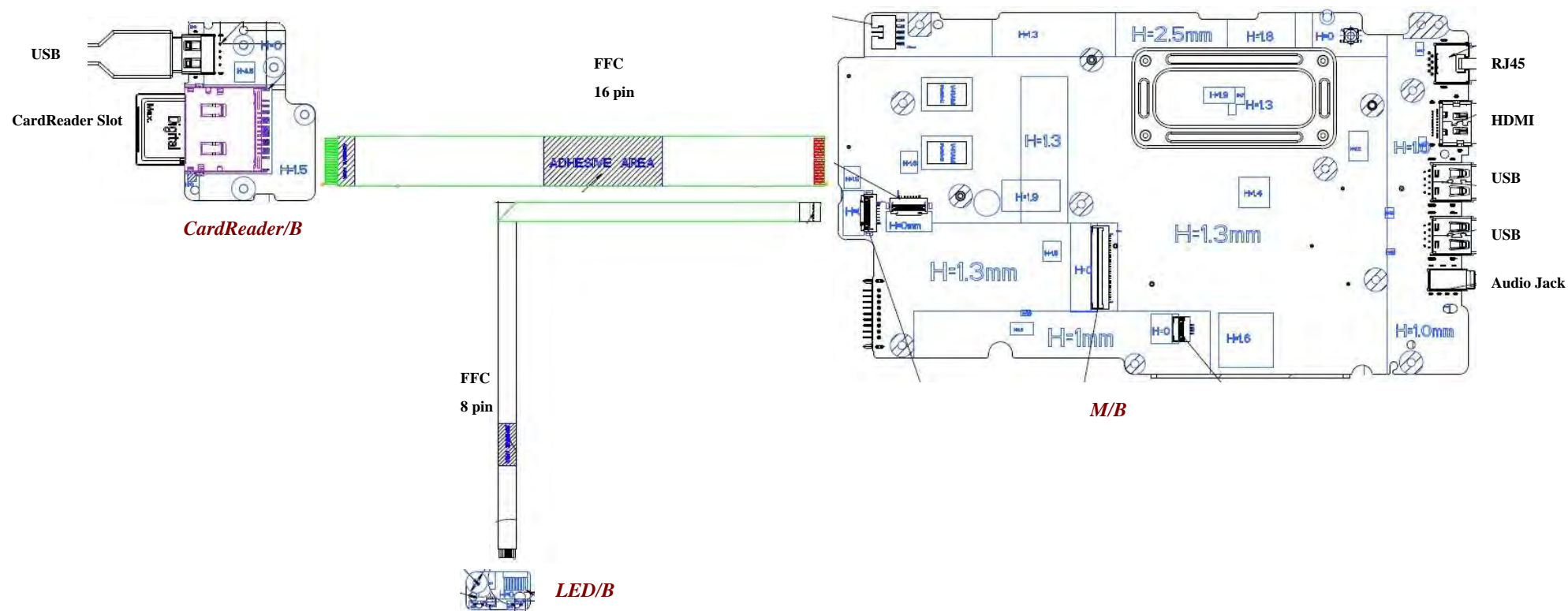
PROJECT :ZAVA1/ZAVC1
PCB NO : DA60018A000 LA-B016P-R1.0

Compal Confidential
Schematic Document

Intel Shark Bay ULT
UMA / DIS AMD 25W/S3+DDR3x4

2014-10-20 Rev: 1.0





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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XD	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V	V		V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

BDW 3D BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)
0	Pre-SSI		
1		Pre-SSI	
2			Pre-SSI
3	SSI		
4		SSI	
5			SSI
6	PT		
7		PT	
8			PT
9	ST		
10		ST	
11			ST
12	1.0		
13		1.0	
14			1.0

Link

CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

Symbol Note :



: means Digital Ground



: means Analog Ground

ULT

USB3.0

Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	

USB2.0

Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (D/B)
Port3	
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera

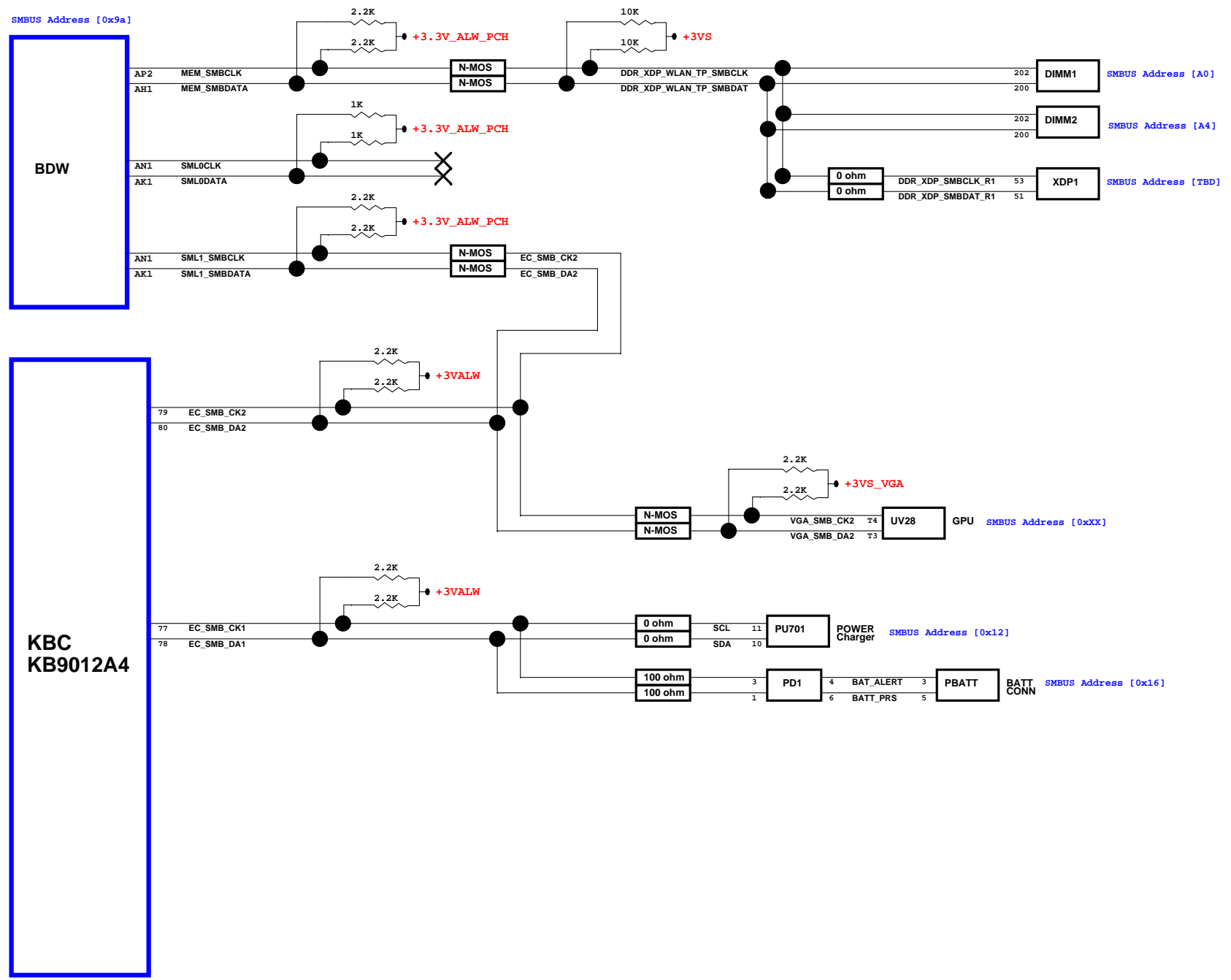
PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (AMD JET/TOBAZ)
Lane 6	

SATA

SATA0	HDD
SATA1	
SATA2	
SATA3	

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I3-4020U-15W-GT2-MP

UC1 I3R1@
CL8064701552800 QE25 D0 1.8G
SA00007MGOL

UC1 I3R3@
CL8064701478202 SR16Q C1 1.7G A31!
SA00006SX2L TBD

I5-4210U-15W-GT2-MP

UC1 I5R1@
CL8064701477802 QEAK D0 1.7G
SA00007LOOL

UC1 I5R3@
CL8064701477702 SR170 C1 1.6G A31!
SA00006SM3L TBD

i7-4510U-15W-GT2-MP

UC1 I7R1@
CL8064701477301 QEAF D0 2G BGA
SA00007M7OL

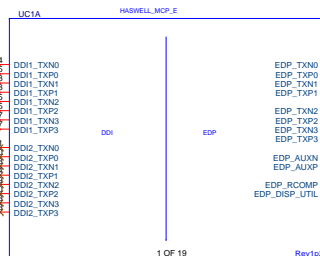
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SA00006SL2L TBD

UC1 QFSY@
CL8064701614813 QFSY C0 1.6G
SA00007AMOL

UC1 QG21@
CL8065801674128 QG21 C0 1.2G
SA00007OSOL

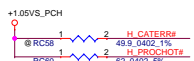
UC1 QG22@
CL8065801675027 QG22 C0 1.2G
SA00007OTOL

Broadwell



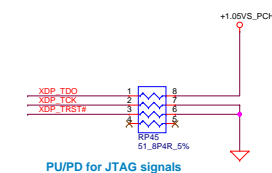
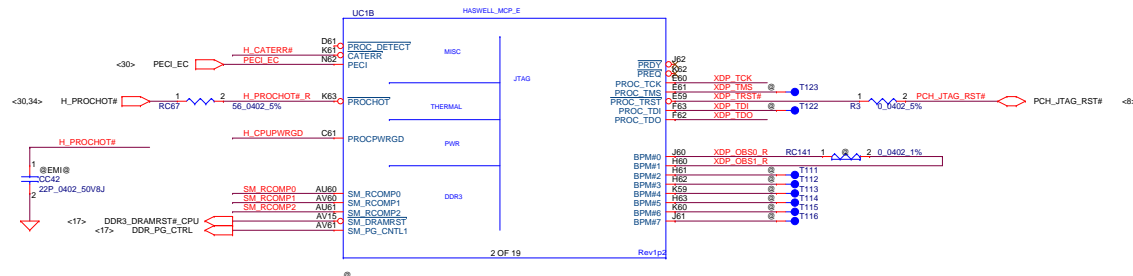
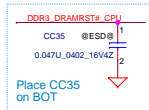
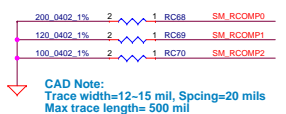
COMPENSATION PU FOR eDP

CAD Note: Trace width=20 mils, Spacing=25mil, Max length=100 mils.



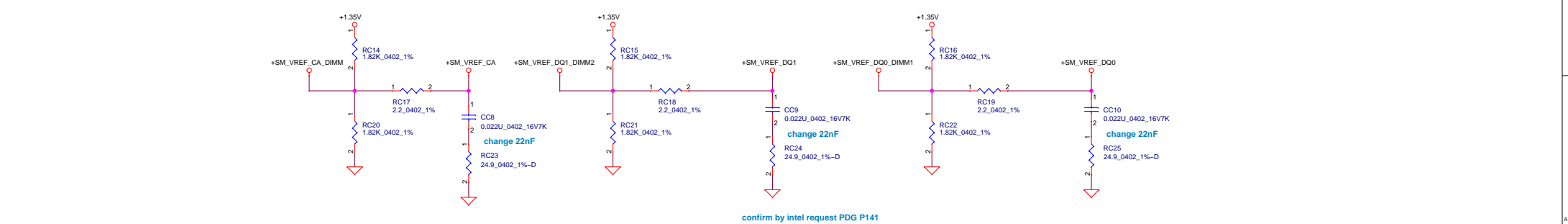
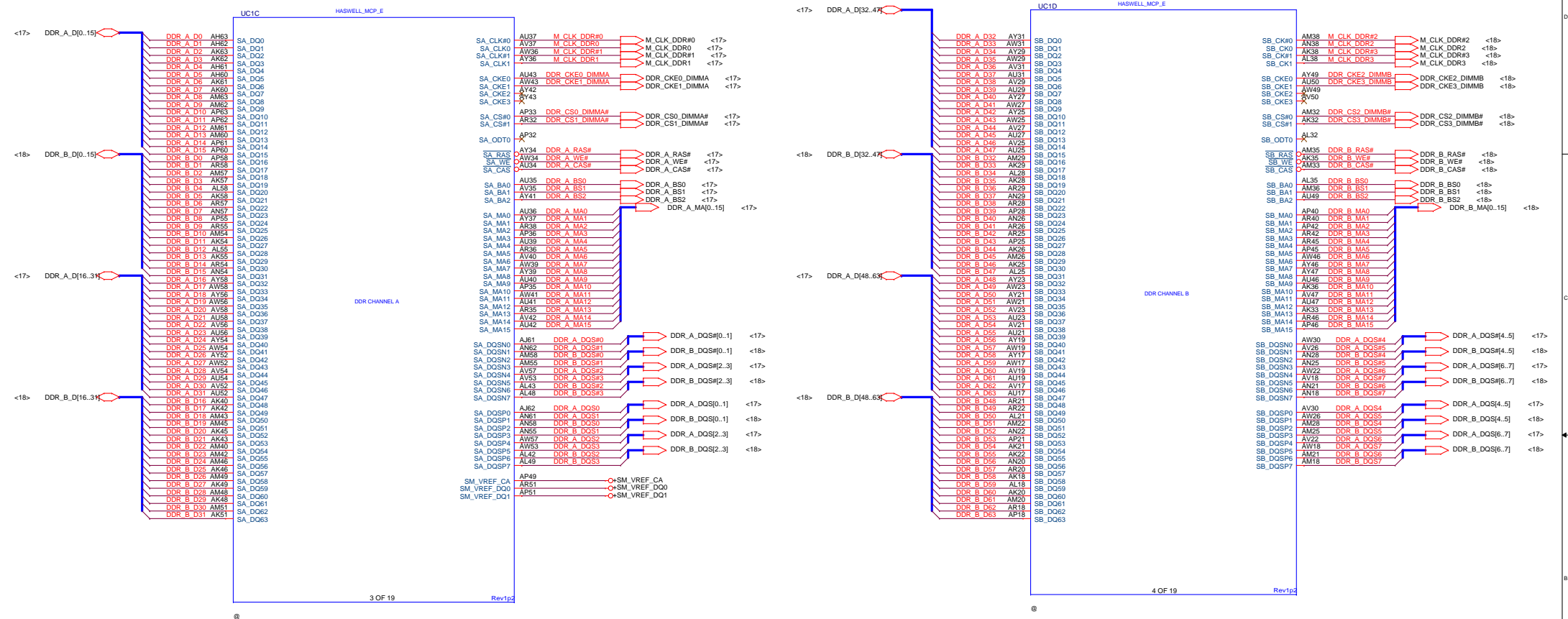
CAD Note: Avoid stub in the PWRGD path while placing resistors RC115

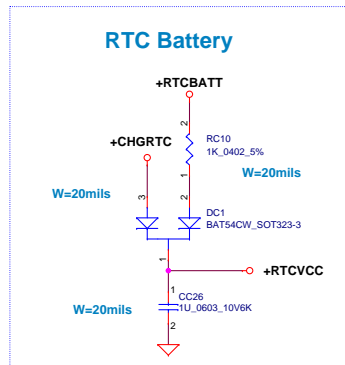
DDR3 COMPENSATION SIGNALS



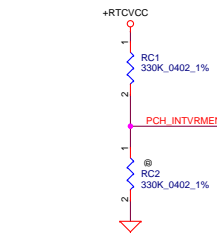
PU/PD for JTAG signals

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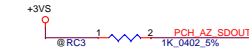




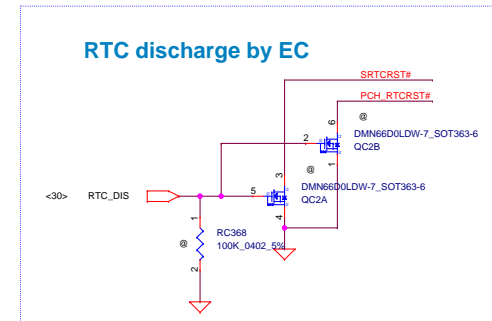
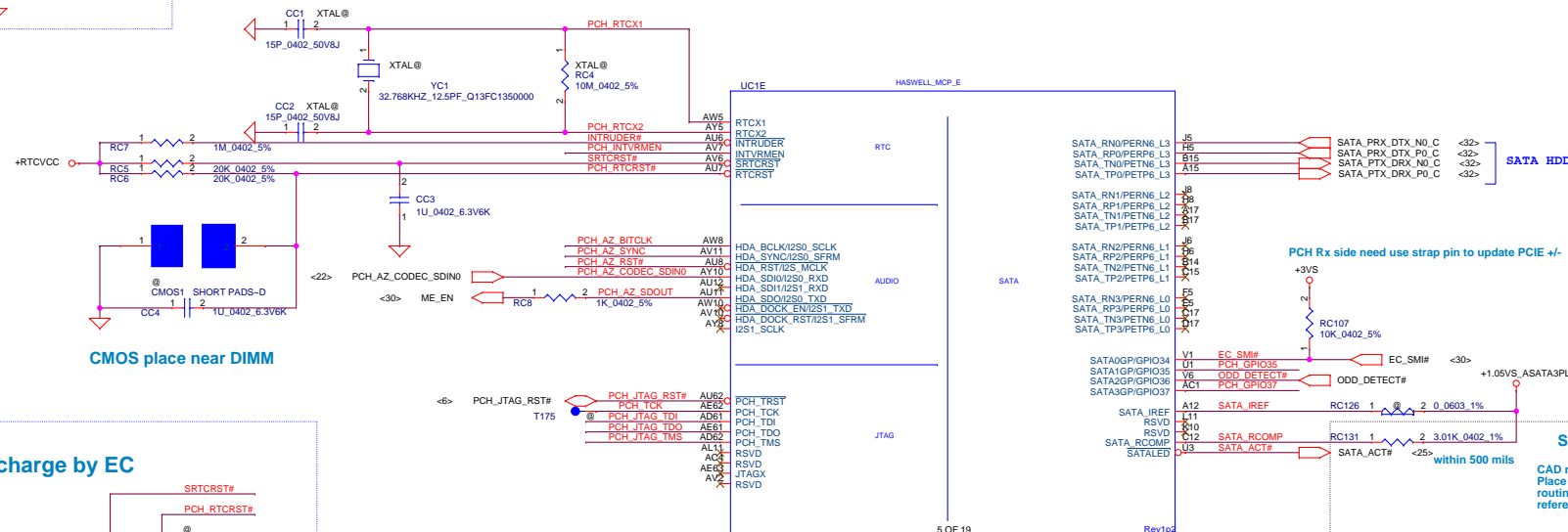
For GCLK



INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
 High - Enable Internal VRs
 Low - Enable External VRs

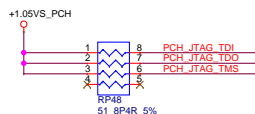
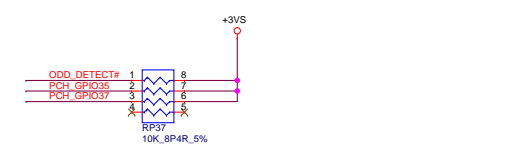
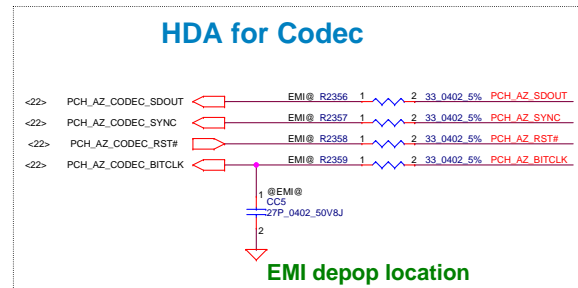


FLASH DESCRIPTOR SECURITY OVERRIDE
 LOW = DISABLED (DEFAULT)
 HIGH = ENABLED



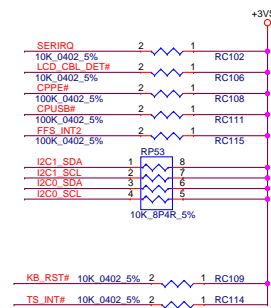
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

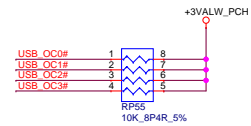
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



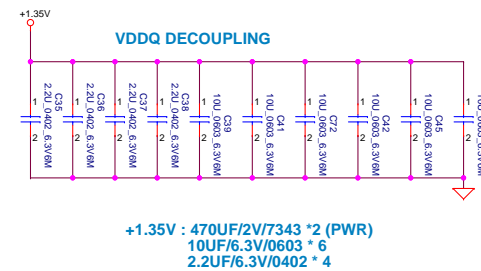
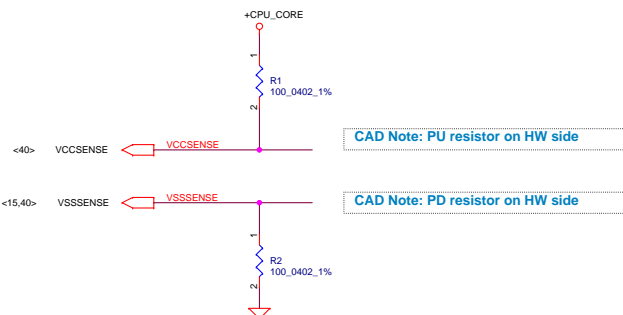
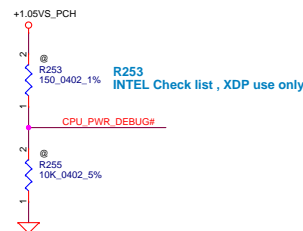
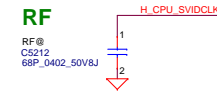
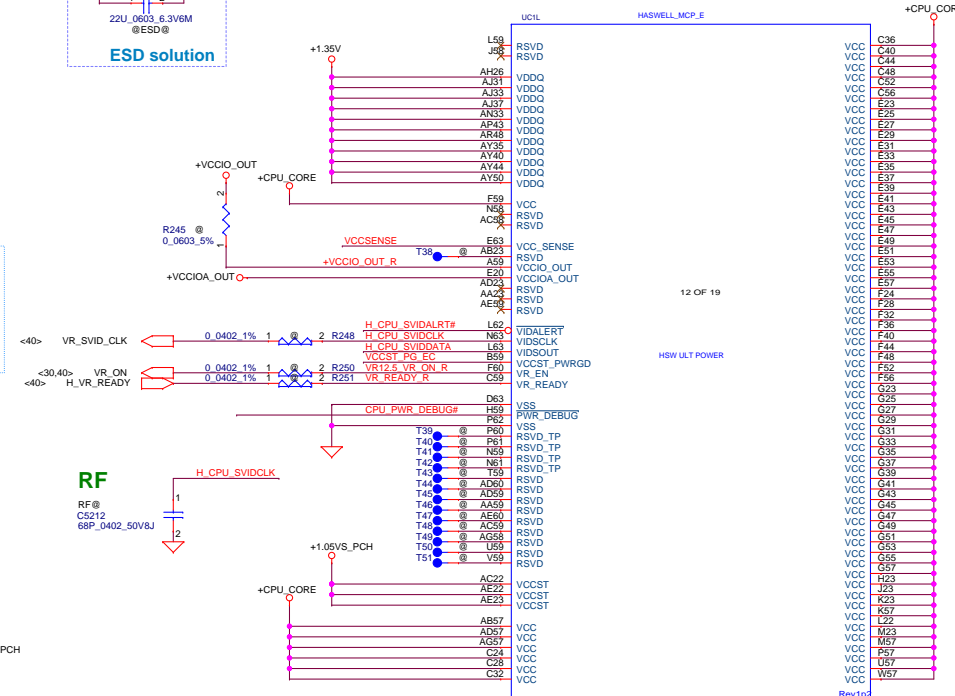
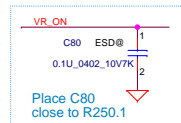
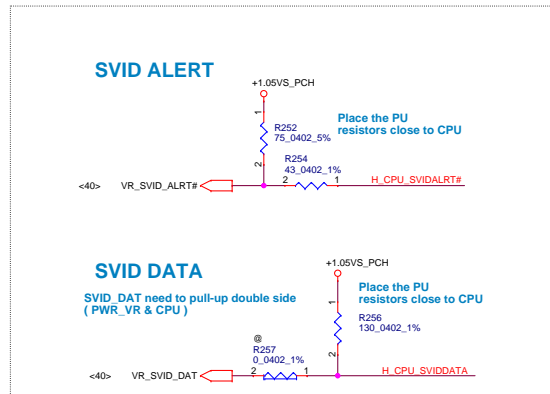
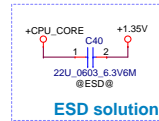
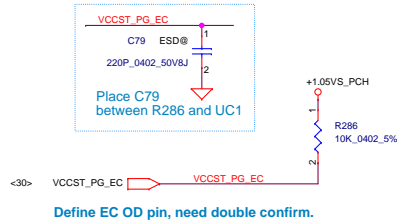


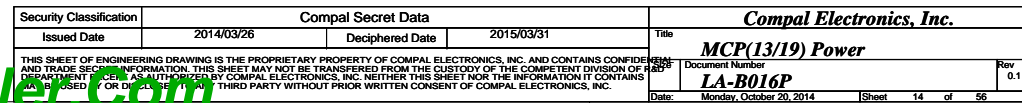
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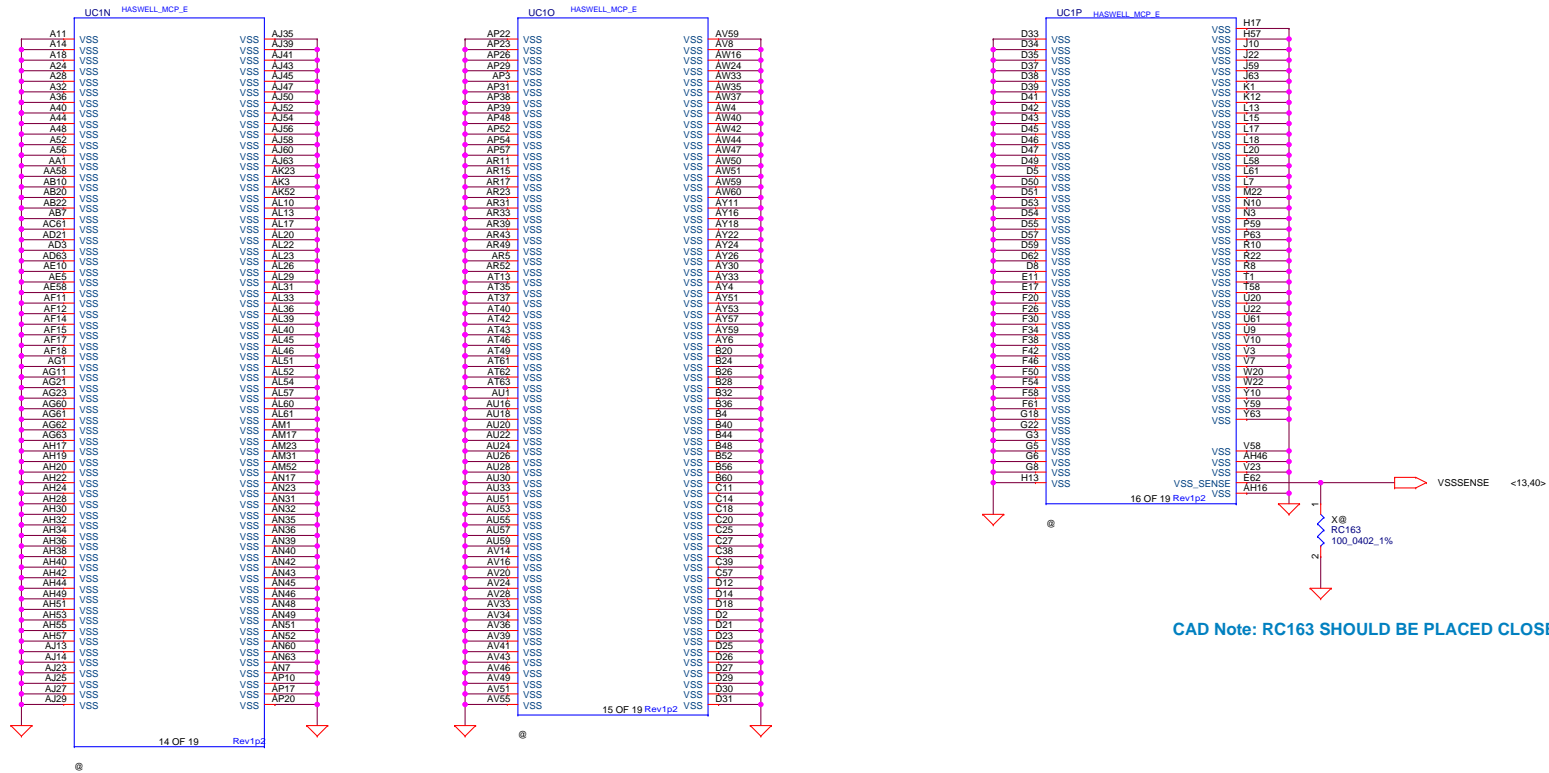


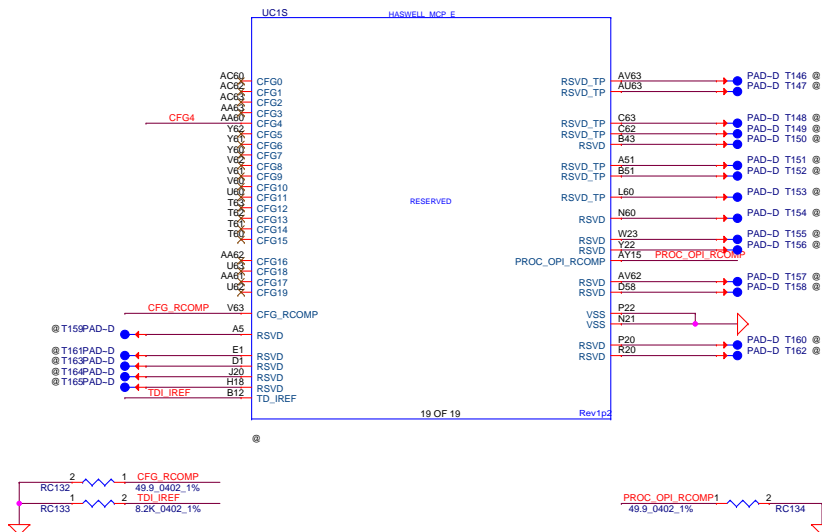
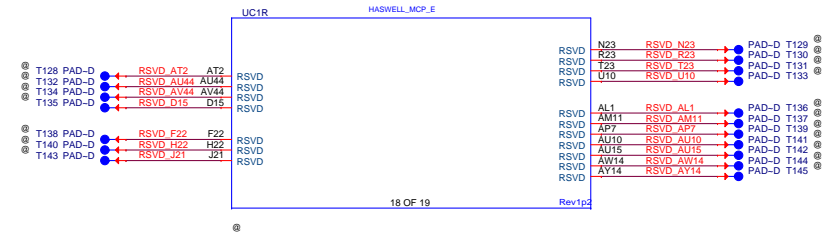
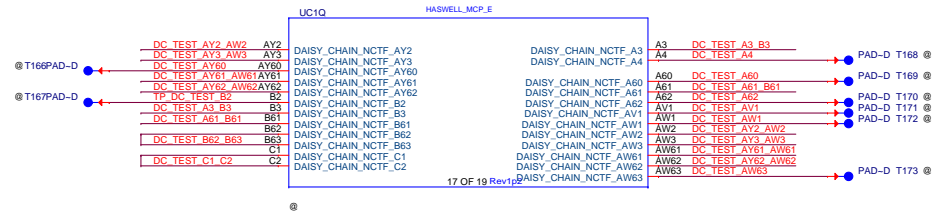


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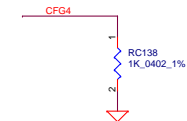








CFG STRAPS for CPU



Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

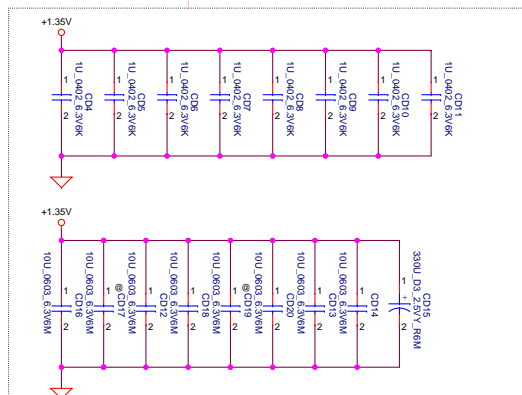
<7> DDR_A_DQS#(0..7)
<7> DDR_A_DQ(0..63)
<7> DDR_A_DQS(0..7)
<7> DDR_A_MA(0..15)

All VREF traces should have 10 mil trace width

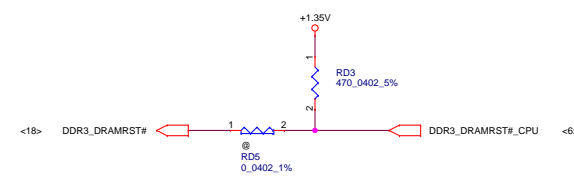
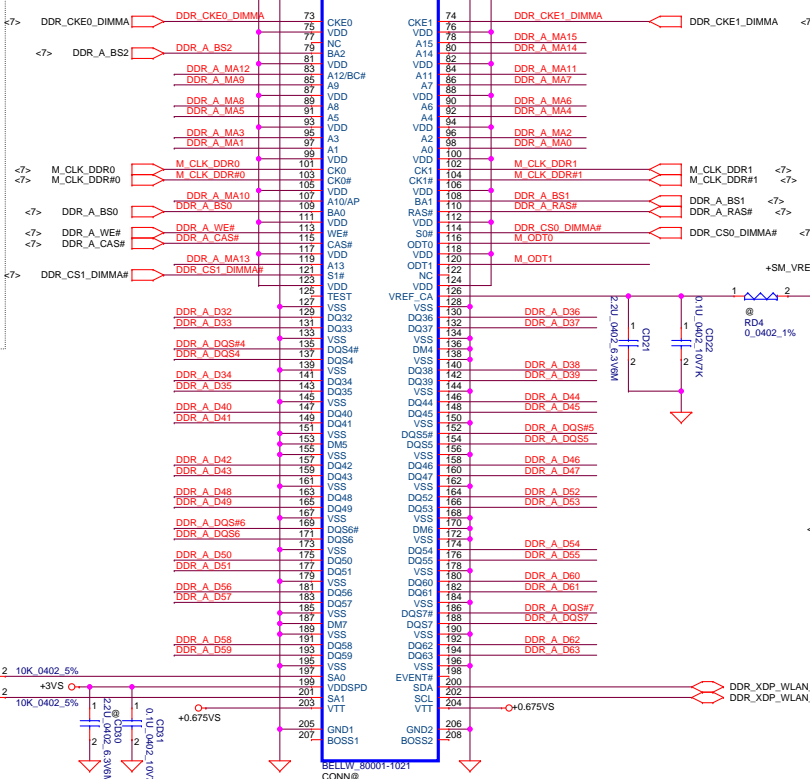
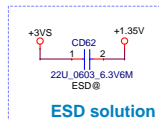
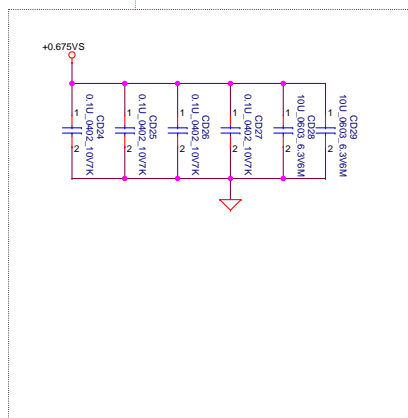
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

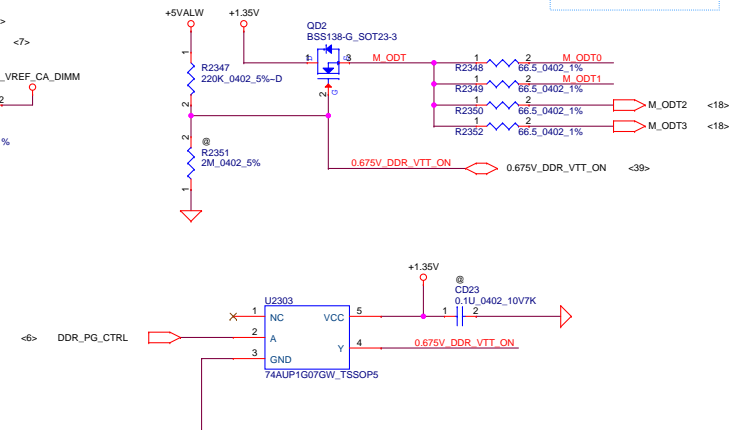
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

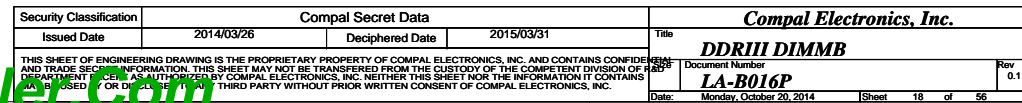


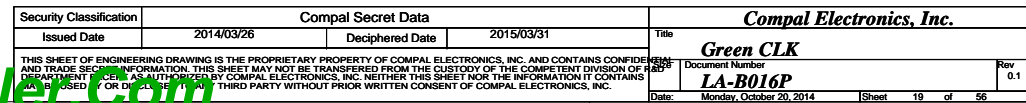
Layout Note:
Place near JDIMM1.203,204

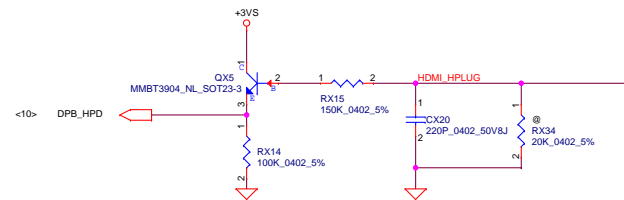
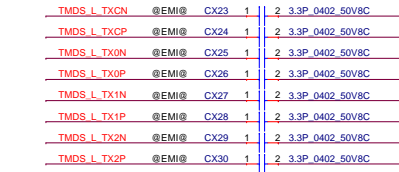
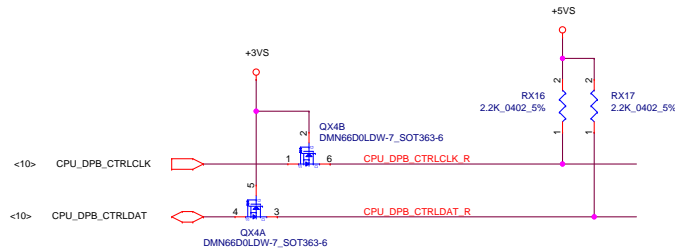
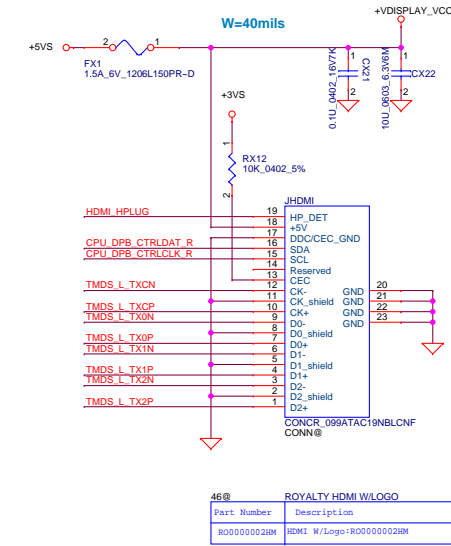
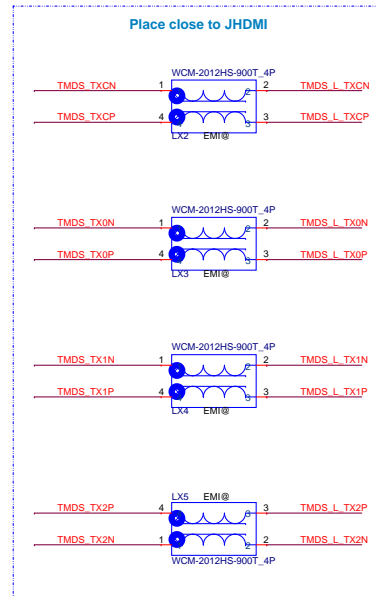
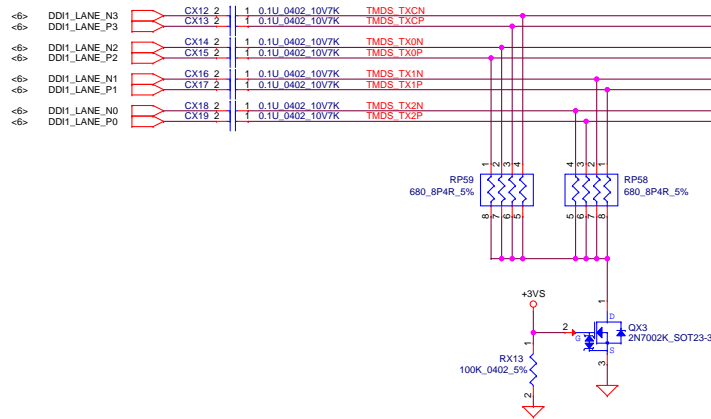


DDR3L SODIMM ODT GENERATION

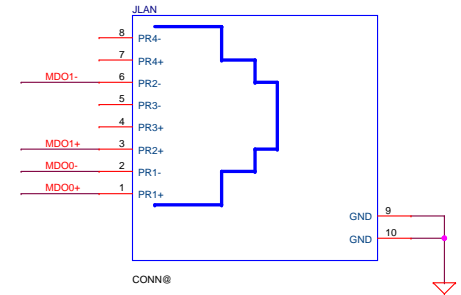
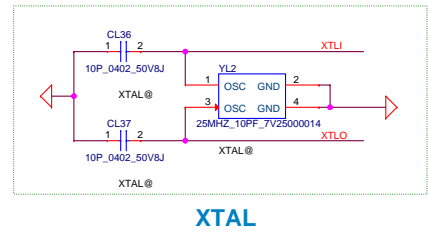
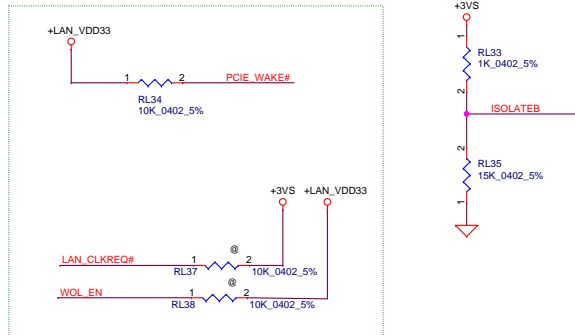
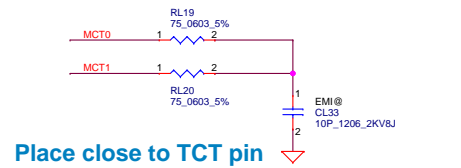
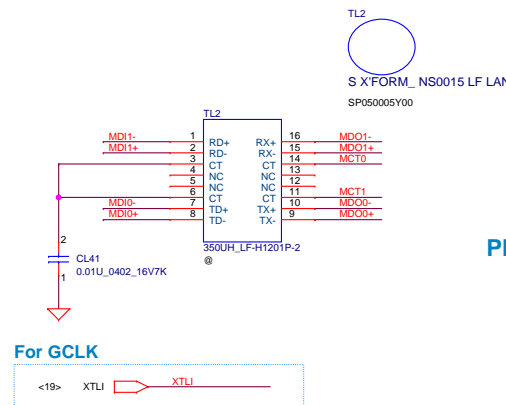
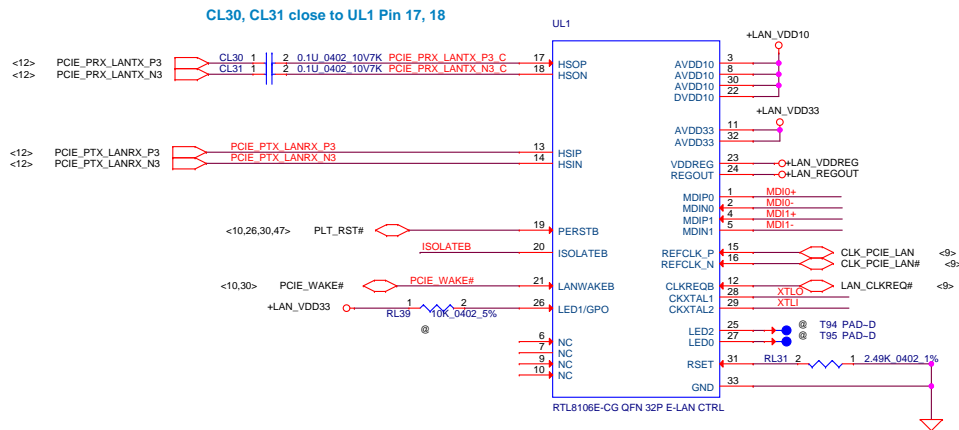
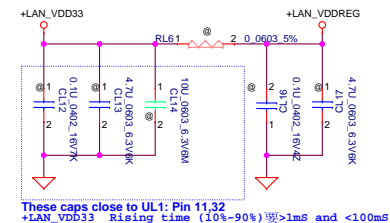
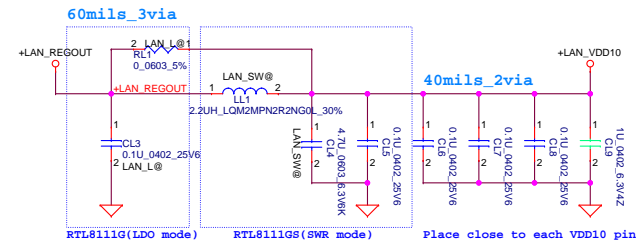
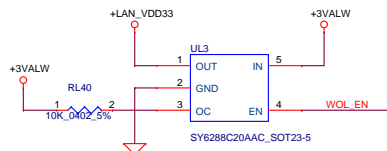
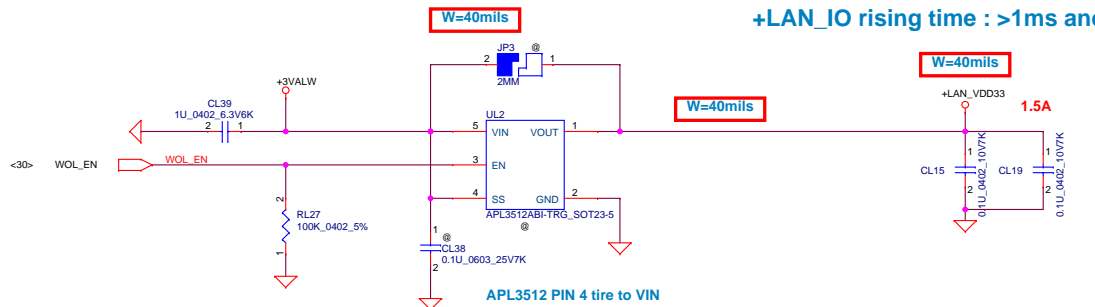




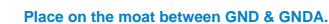


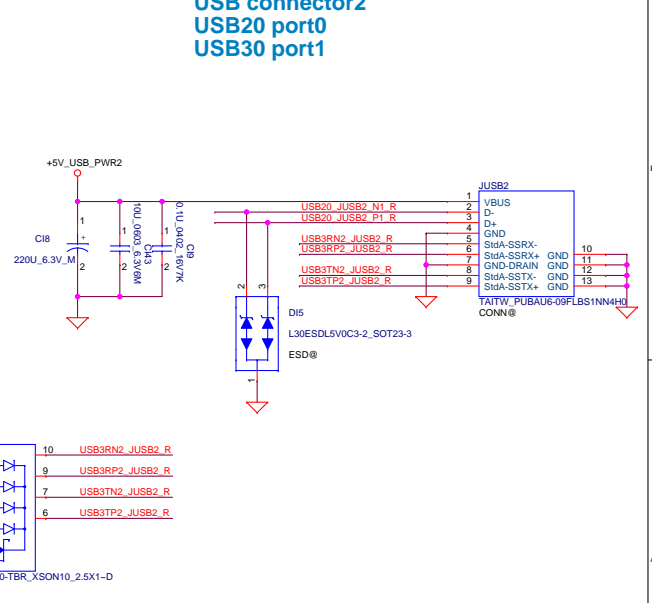
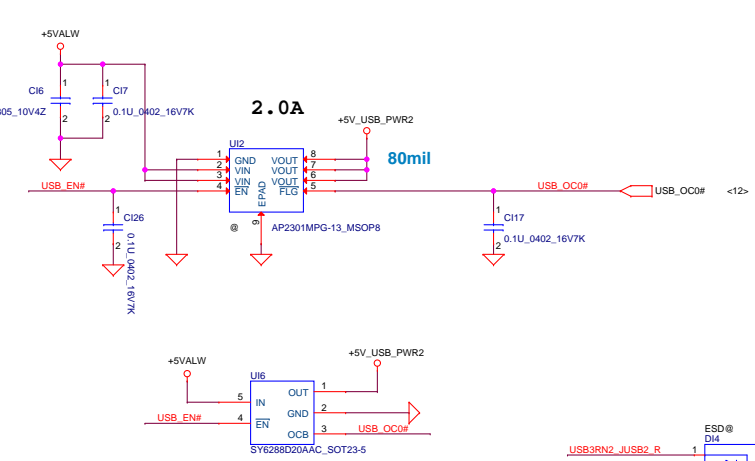
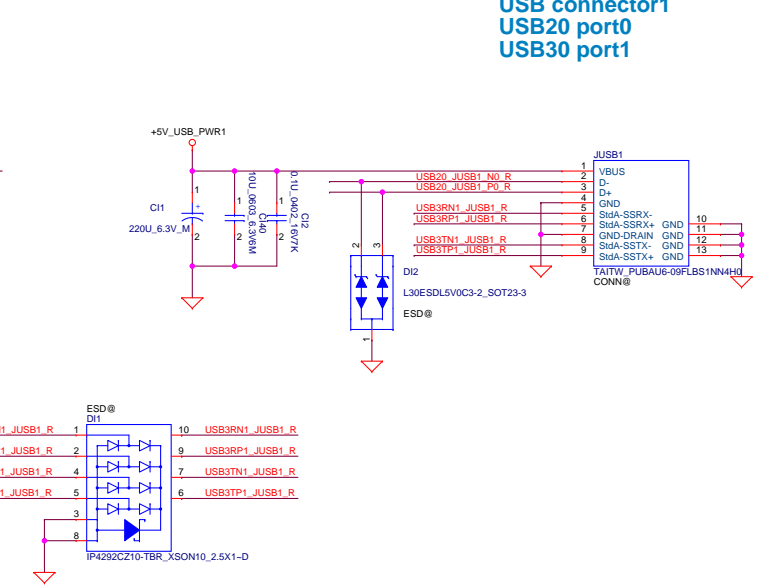
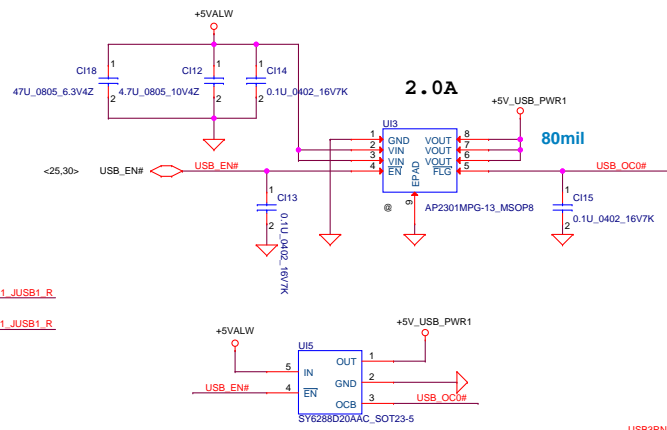
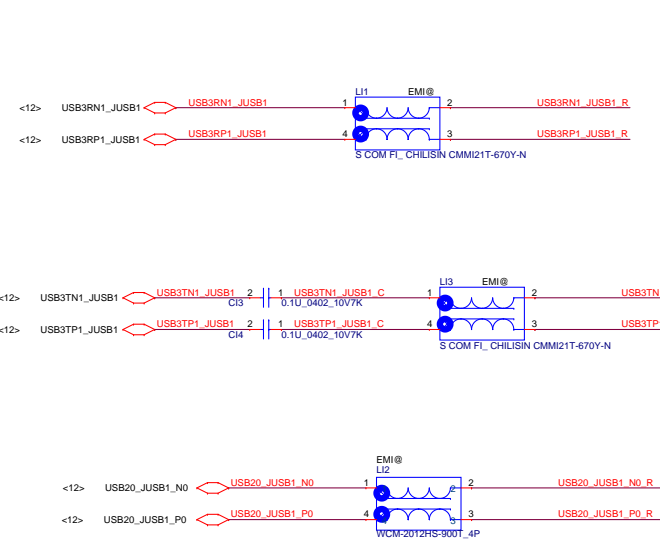


+LAN_IO rising time : >1ms and <100ms

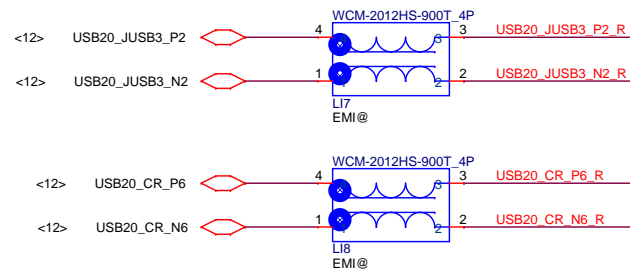
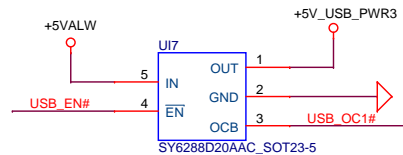
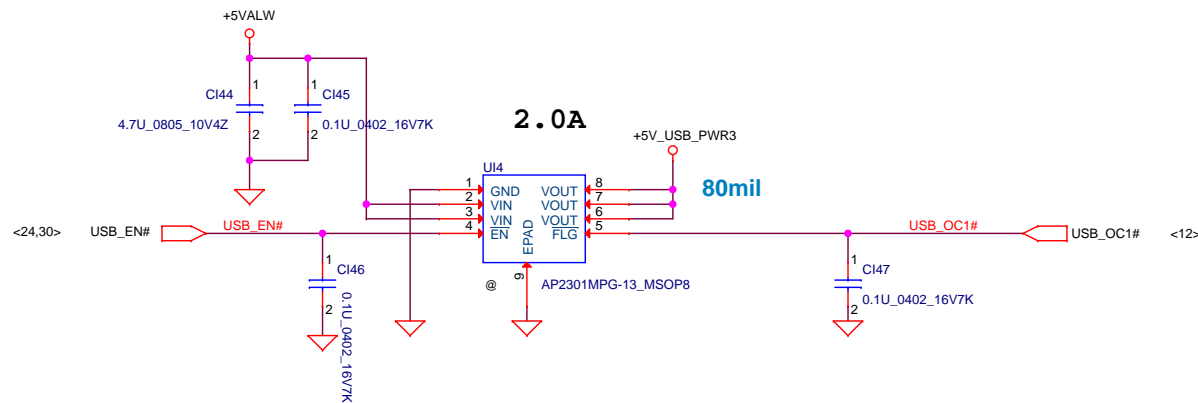


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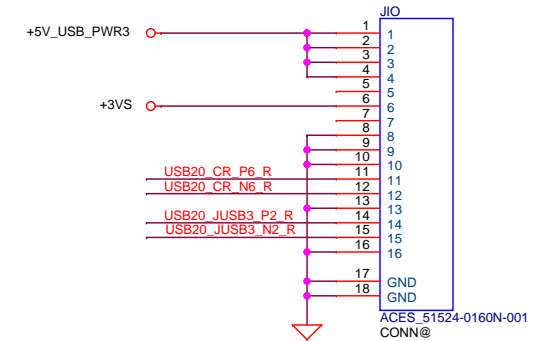




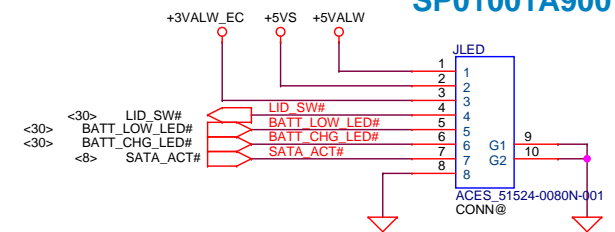
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Issued Date	2014/03/26	Deciphered Date	2015/03/31	Document Number	USB3.0
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IO to MB CONN Substitute:SP01001FS00

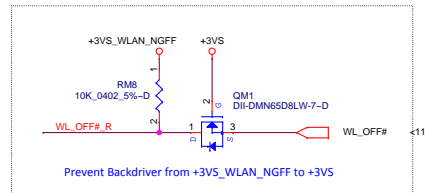
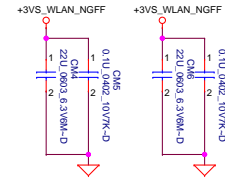


LED/B TO M/B SP01001A900



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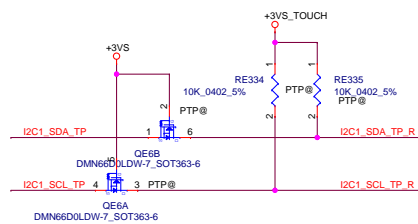
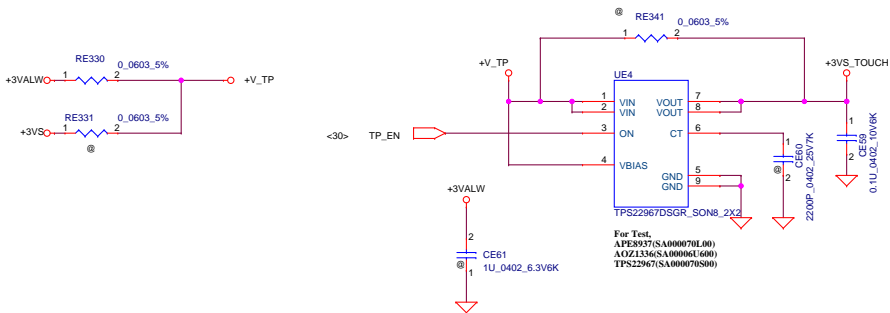
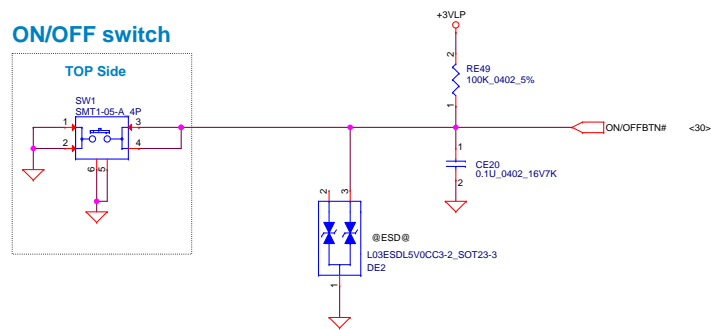
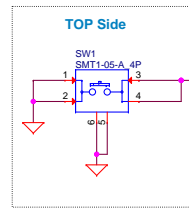
closed to pin 2, 4 closed to pin 64, 66



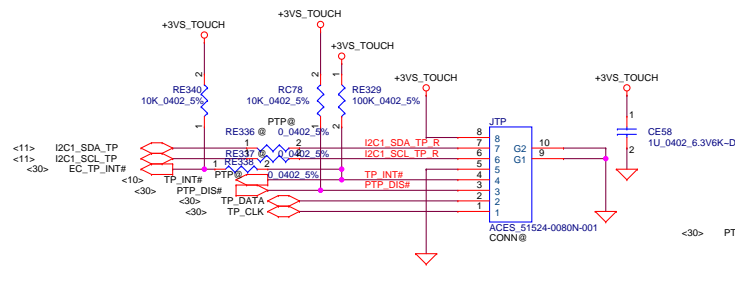
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Date: Monday, October 20, 2014				Sheet	26 of 56

Power ON Circuit

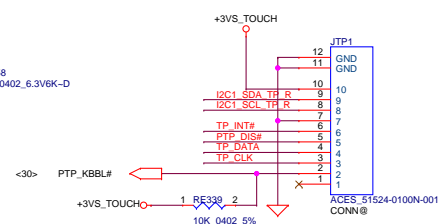
ON/OFF switch



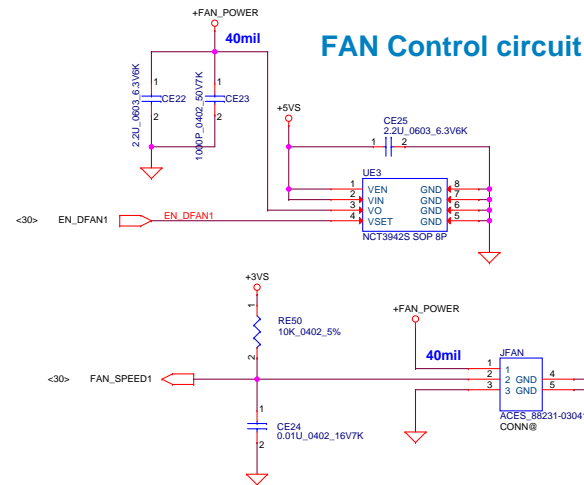
Touch pad



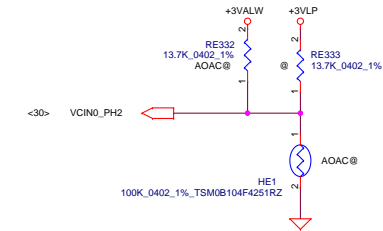
PTP



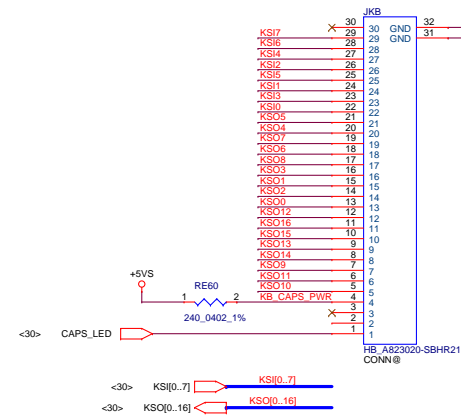
FAN Control circuit



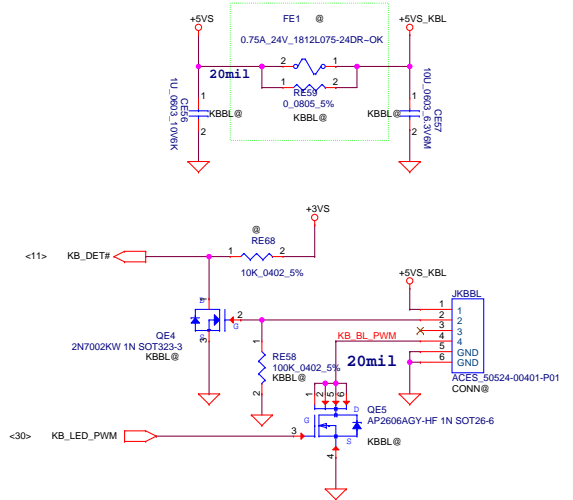
HE1 place around FAN area.



INT_KBD Connector

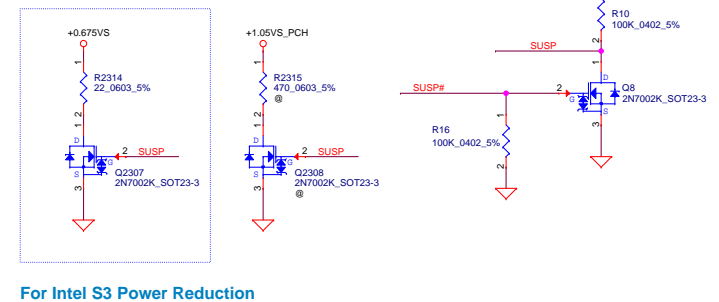
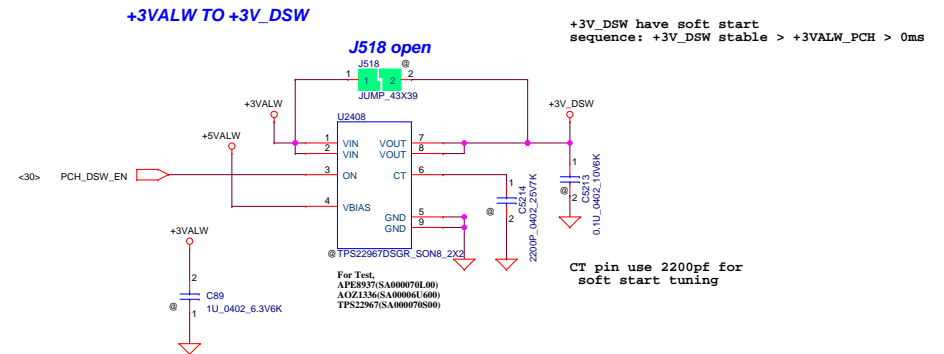


* Key Board Back Light



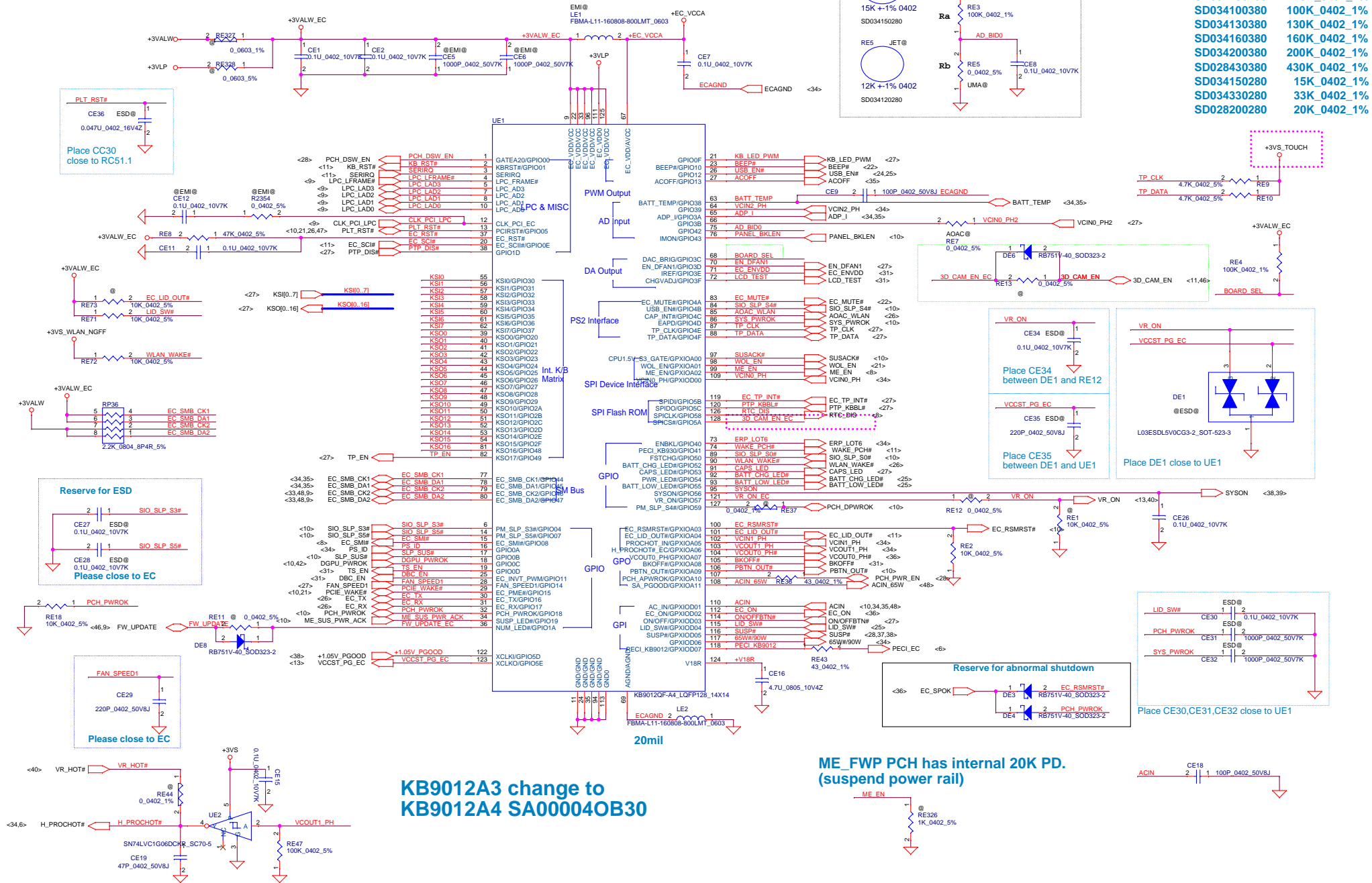
Security Classification		Compal Secret Data		Title	
Issued Date	2014/03/26	Deciphered Date	2015/03/31	FAN / TP / PWR SW / KBBL	
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+3VALW_PCH switch



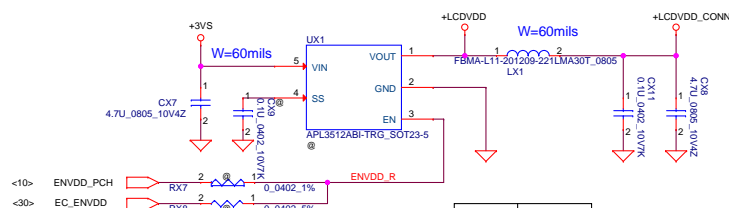
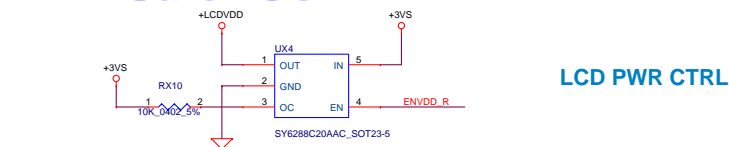
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				2015/03/31	
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				DC/DC Interface	
				Document Number	
				LA-B016P	
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				Sheet	29 of 56

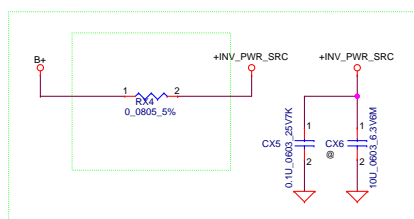


KB9012A3 change to
KB9012A4 SA00004OB30

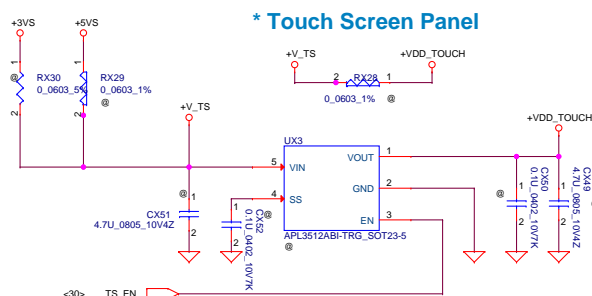
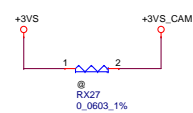
ME_FWP PCH has internal 20K PD.
(suspend power rail)



Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



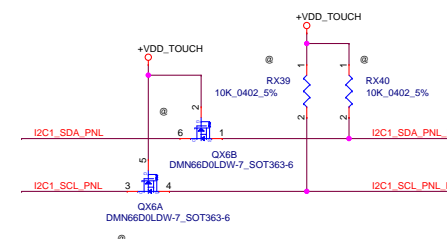
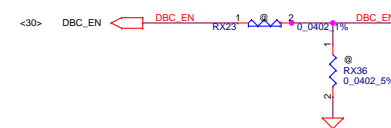
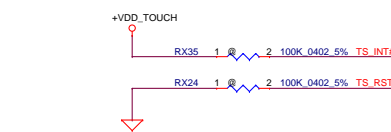
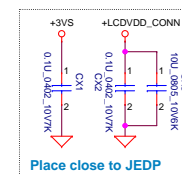
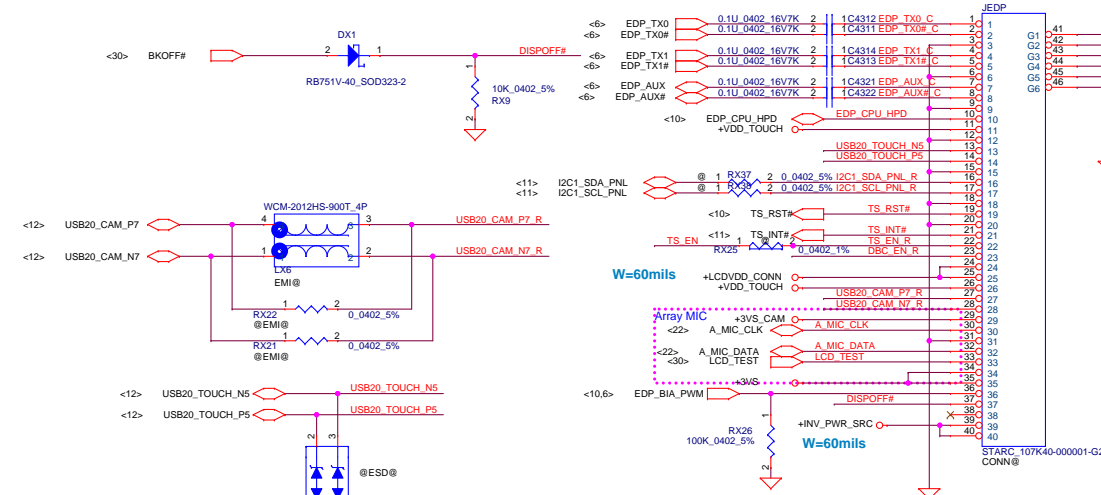
Webcam PWR CTRL

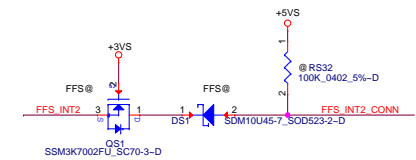
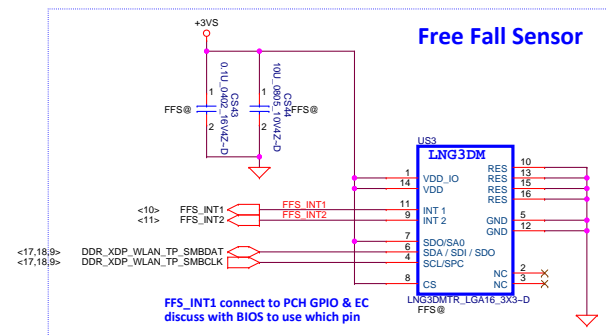
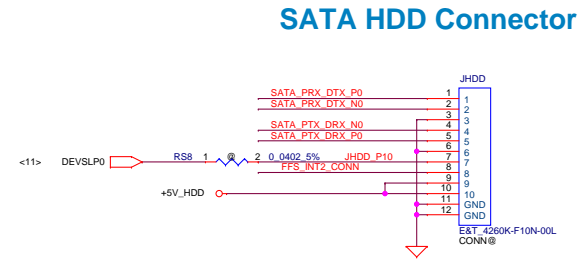


Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

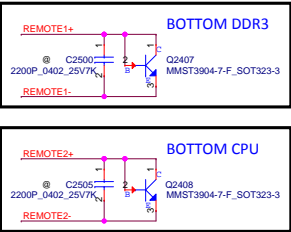
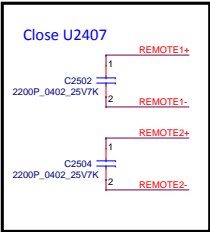
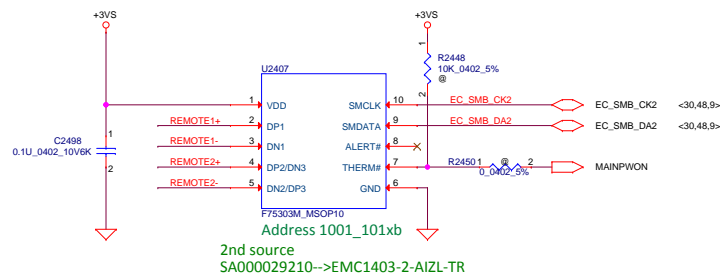
SS table

eDP Connector

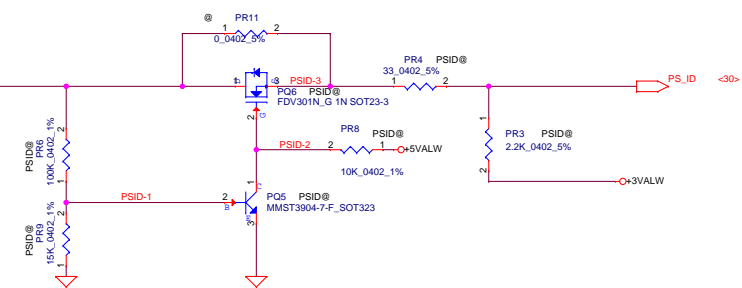
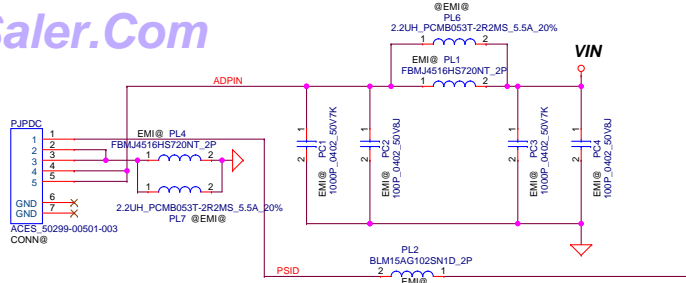




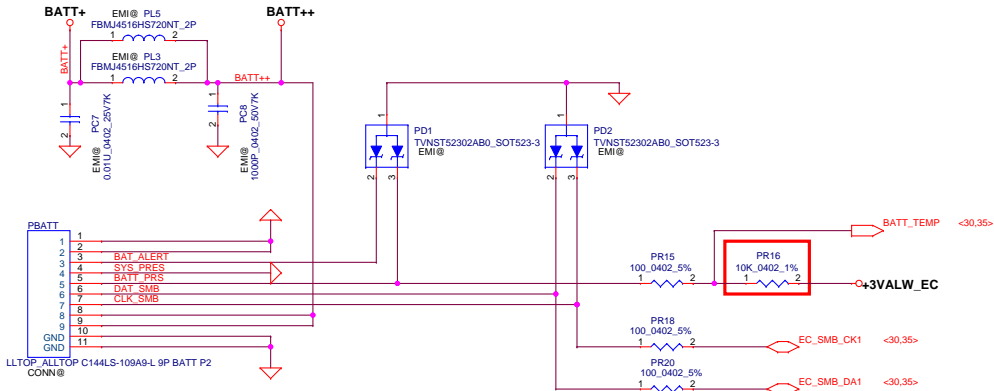
Fintek thermal sensor
placed near by TOP DDR3



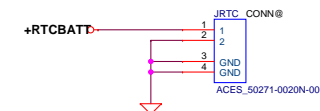
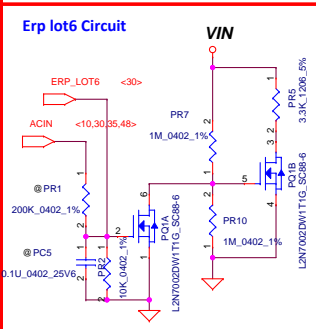
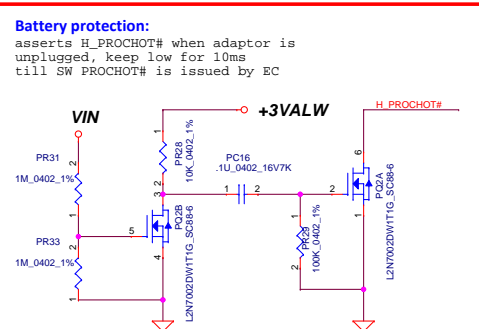
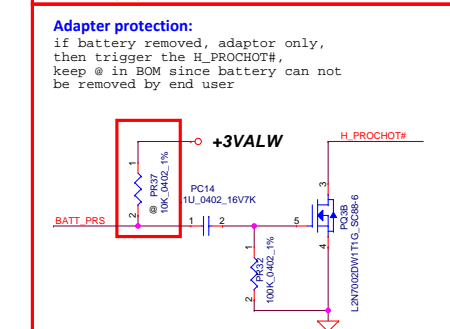
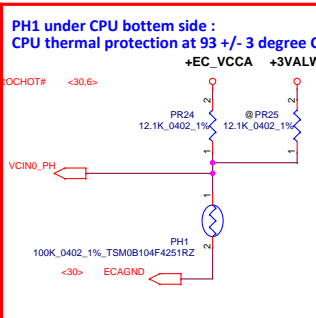
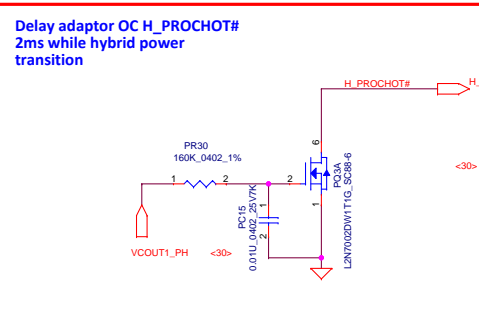
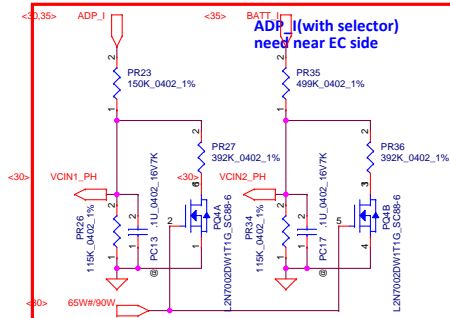
REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"



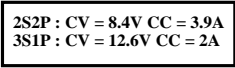
SMART Battery:
 01.GND1
 02.GND2
 03.BATT_ALERT
 04.SYS_PRES
 05.BATT_PRS
 06.DAT_SMB
 07.CLK_SMB
 08.BATT1+
 09.BATT2+




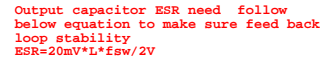
Other component (37.1)



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				Date	Monday, October 20, 2014
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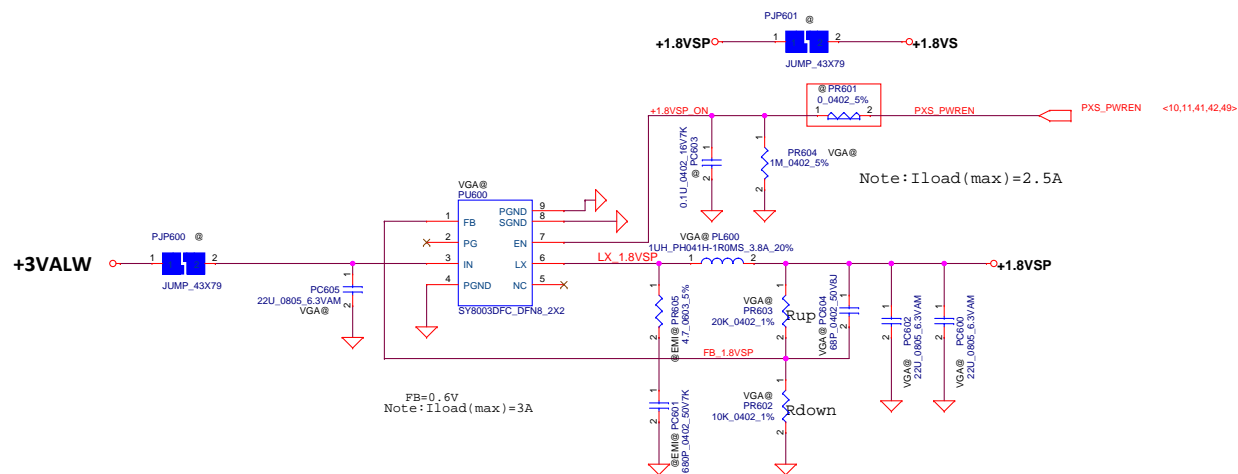
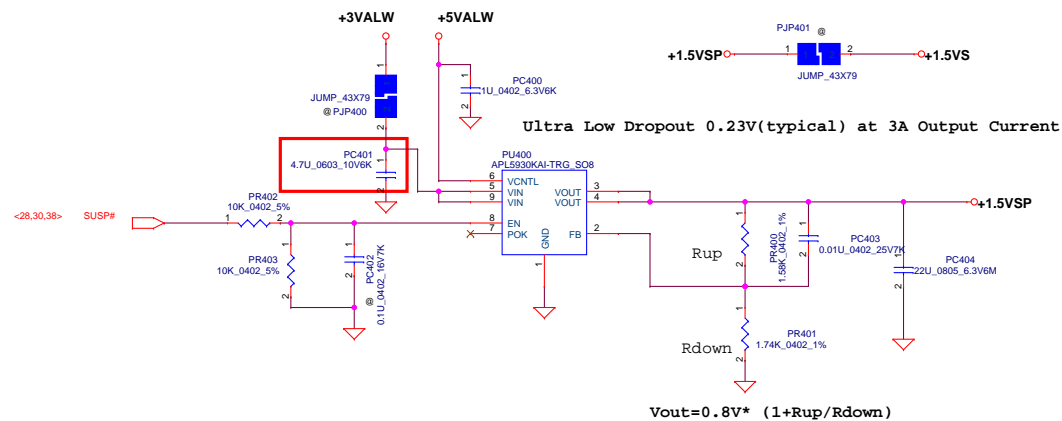


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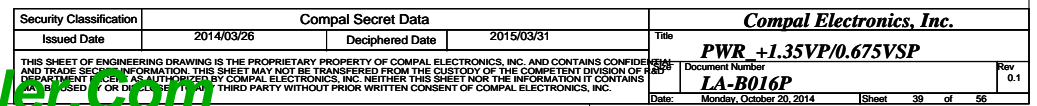
5VALWP	
TDC 5.96A	
Peak Current 8.51A	
OCP current 10.2A	
TYP	MAX
H/S Rds(on) : 22mohm ,	30mohm
L/S Rds(on) : 10.8mohm ,	13.6mohm

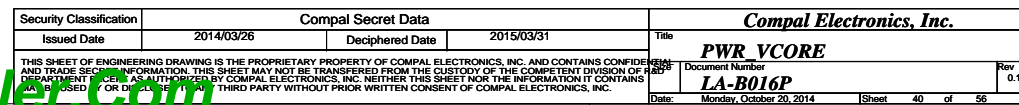
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Issued Date		2014/03/26	Deciphered Date		2015/03/31
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		Document Number		LA-B016P	
Date:		March, October 20, 2014		Sheet 36 of 56	



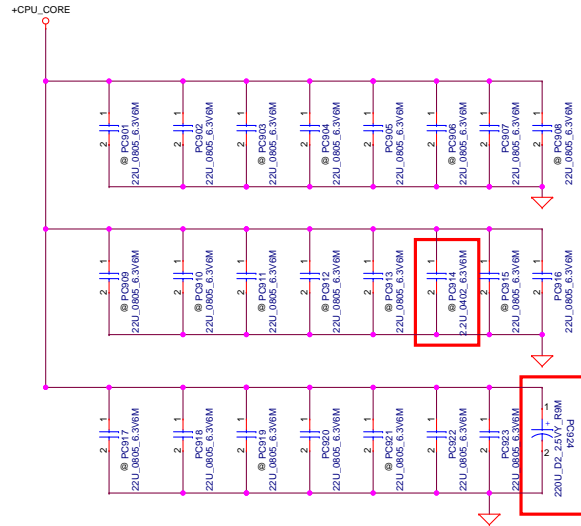


A vertical number line with points A, B, C, and D. Point A is at the bottom, followed by B, then C, and D at the top. The segments AB, BC, and CD are marked with single tick marks, indicating they are equal in length.

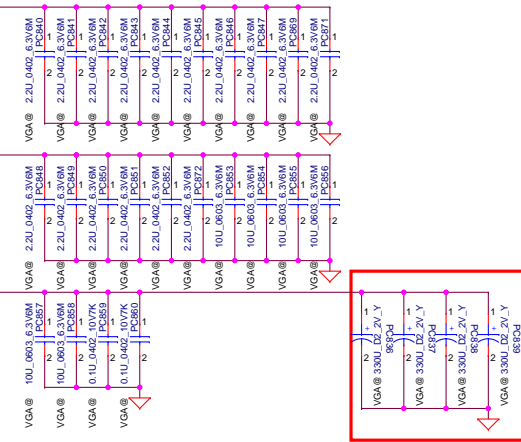




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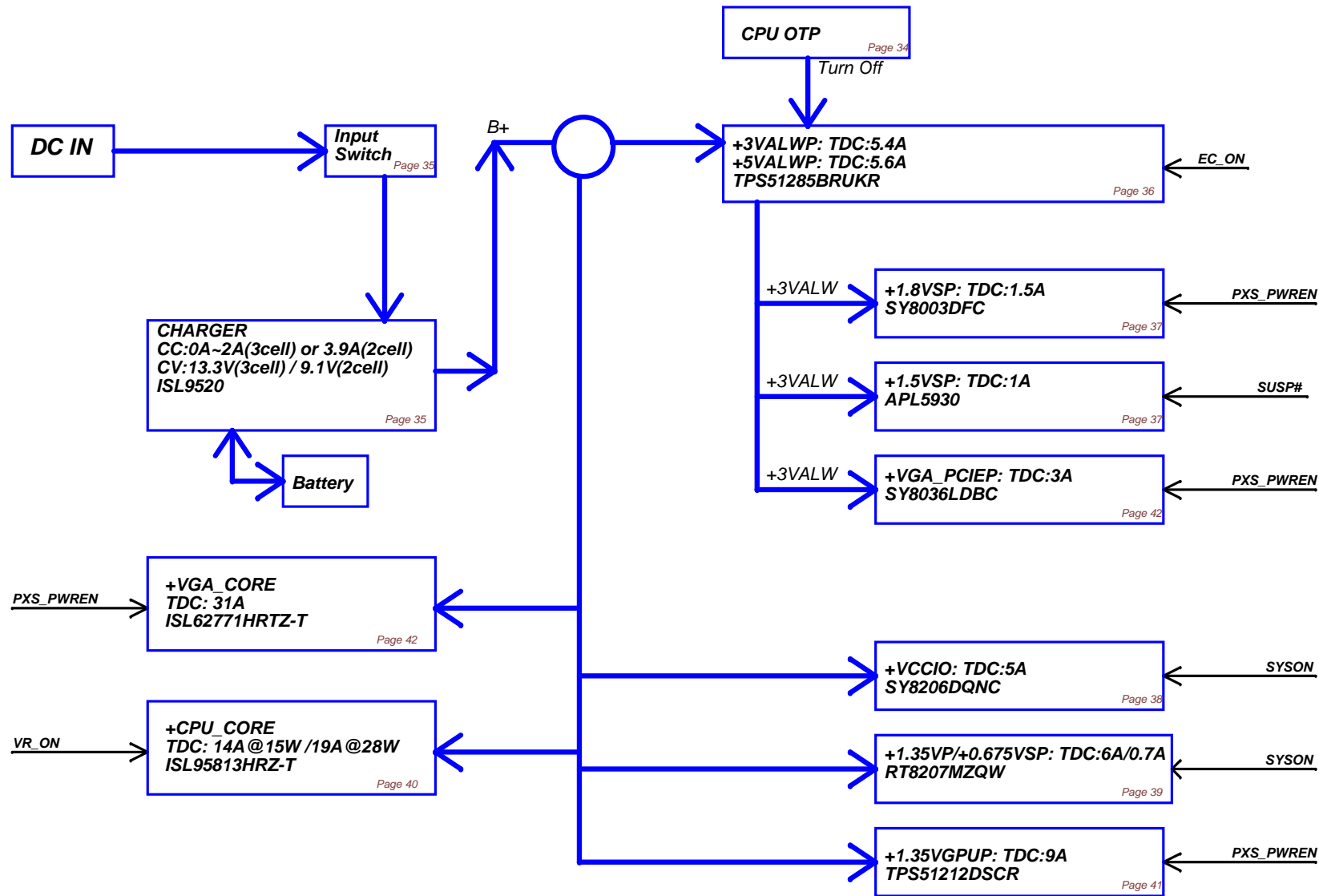


+VGA_CORE



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Power block



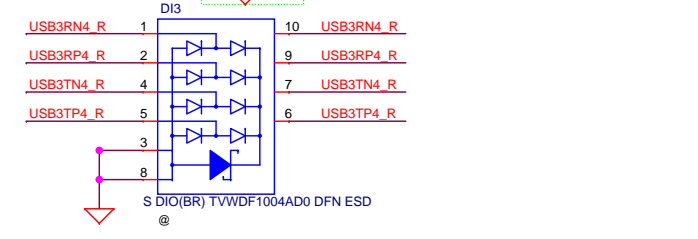
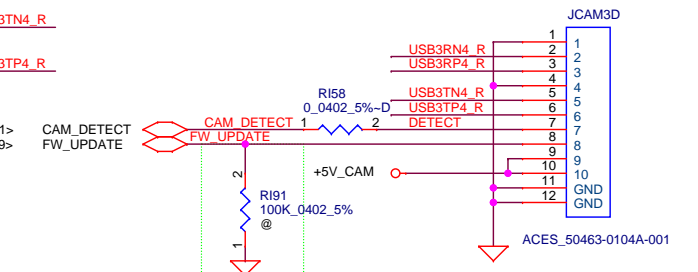
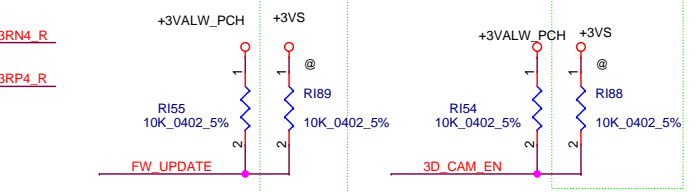
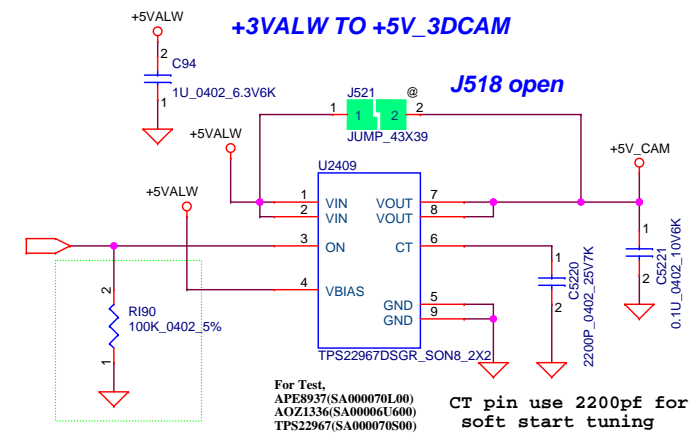
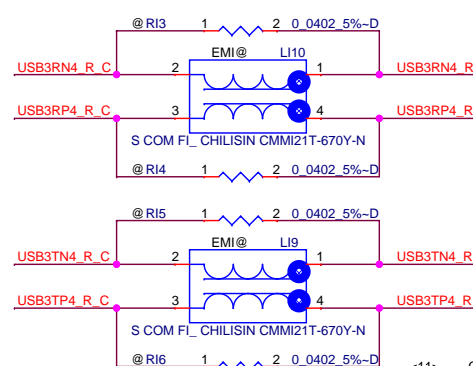
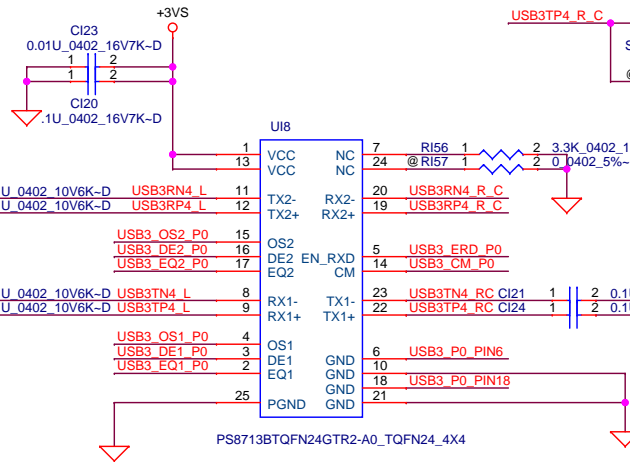
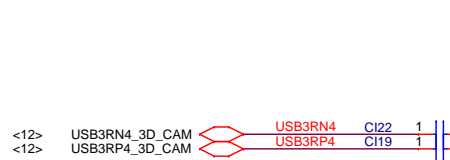
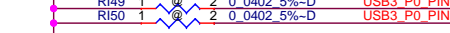
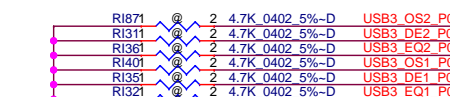
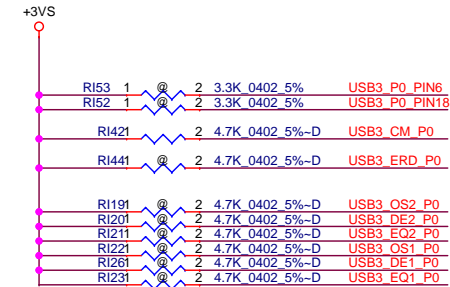
Version Change List (P. I. R. List)

Page 1

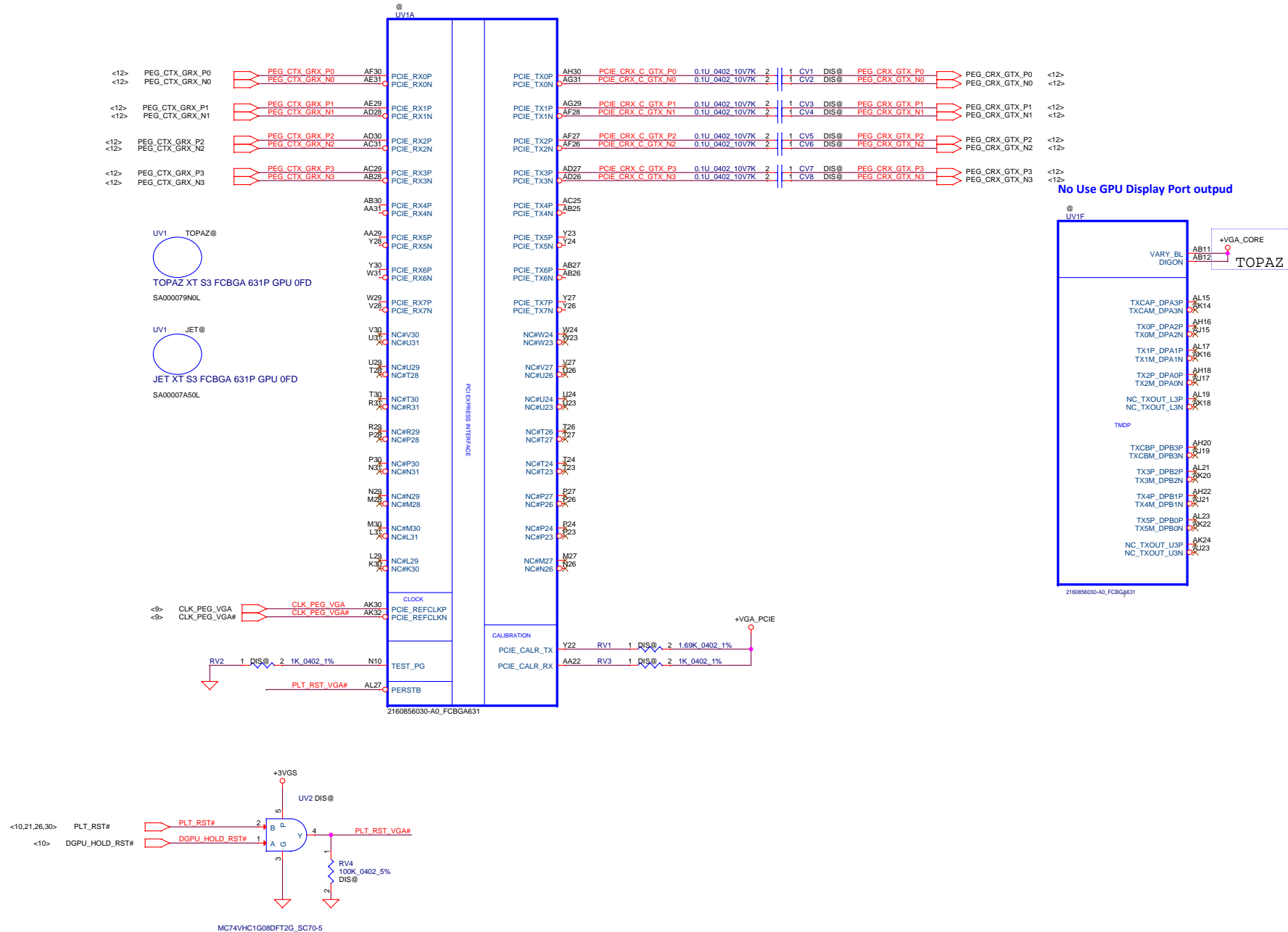
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF0000005100 to SF0000004M00 change PL502 from SH000000NM00 to SH000000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

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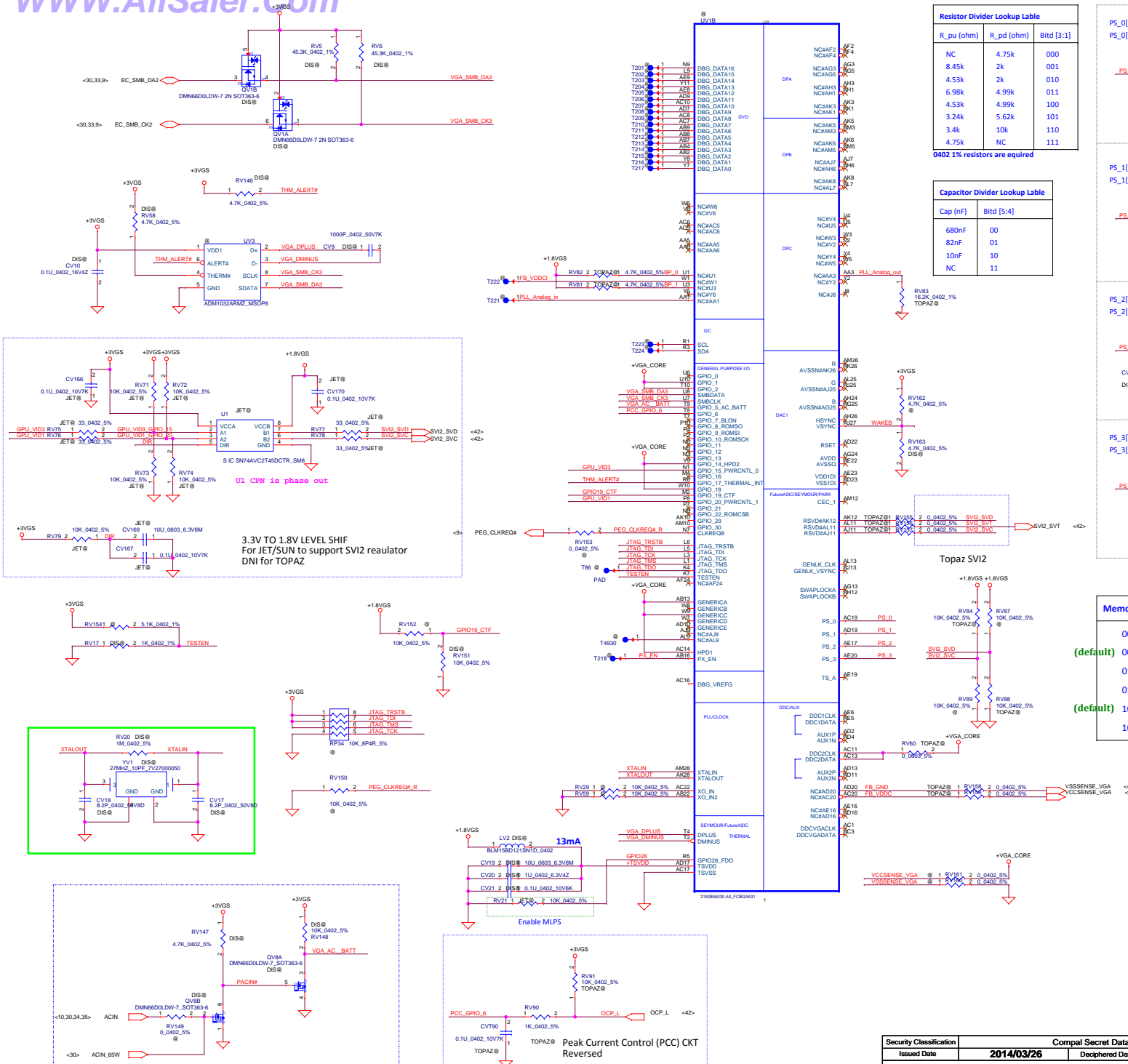
Vendor	Part	TI	Spec	schematic netname	3Vs	GND
1	YD0	YCC	Same			
2	B_EQ0	EQ1	LL: 9.5dB (default) LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_EQ1_P0	RI23	@ RI32
3	DE0	DE1	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE1_P0	RI26	@ RI35
4	EQ1	OS1	LL: 9.5dB LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_OS1_P0	RI22	@ RI40
5	PD#	EN_RXD	it can be left open	USB3_ERD_P0	RI44	@ RI48
6	B_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN6	RI53	@ RI49
7	REXT	NC	4.99K			RI56 4.99K
8	B_Inp	RX1-	Same			
9	B_Inp	RX1+	Same			
10	GND	GND	Same			
11	A_OUTa	TX2-	Same			
12	A_OUTp	TX2+	Same			
13	VDD	VCC	Same			
14	TS1/NC	CM	4.7K ohm resistor for performance adjustment	USB3_CM_P0	RI42	@ RI40
15	A_EQ1	OS2	LL: 9.5 dB (default) LH: 13 dB	USB3_OS2_P0	RI19	@ RI87
16	A_DE0	DE2	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE2_P0	RI20	@ RI31
17	A_EQ0	EQ2	LL: 9.5 dB (default) LH: 13 dB	USB3_EQ2_P0	RI21	@ RI36
18	A_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN18	RI52	@ RI50
19	A_Inp	RX2-	Same			
20	A_Inp	RX2+	Same			
21	GND	GND	Same			
22	B_OUTp	TX1+	Same			
23	B_OUTa	TX1-	Same			
24	I2C_EN	NC	this pin can be NC or connected to GND	NC		RI57 @



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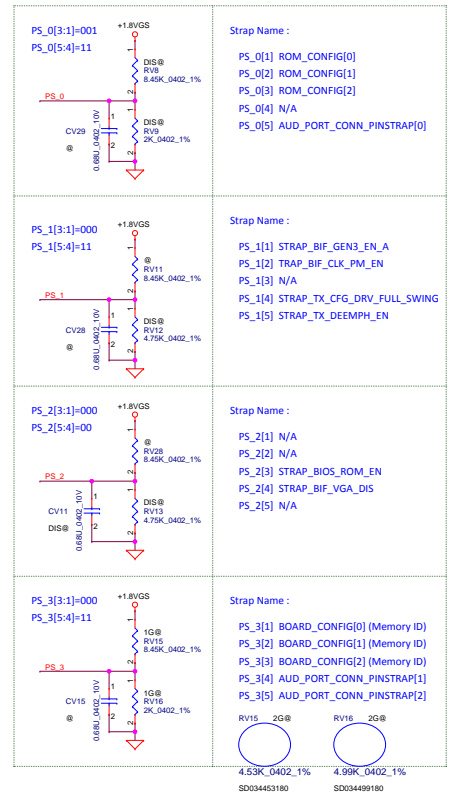
Resistor Divider Lookup Table

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

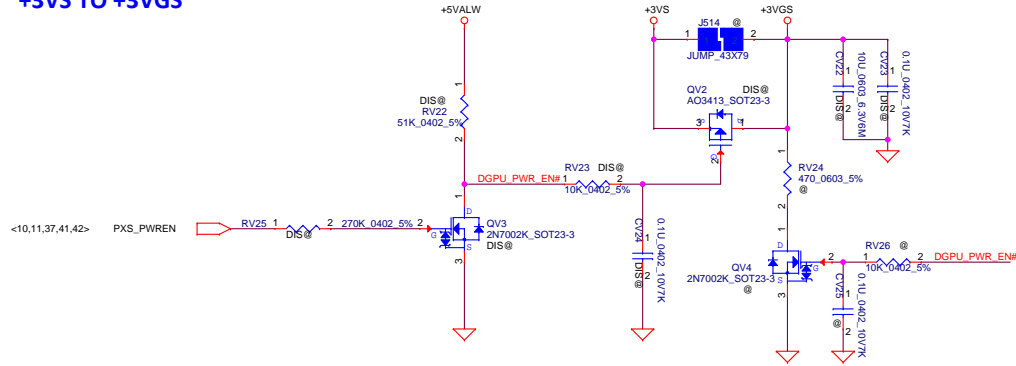
0402 1% resistors are required

Capacitor Divider Lookup Table

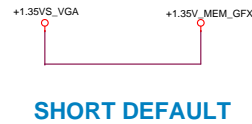
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



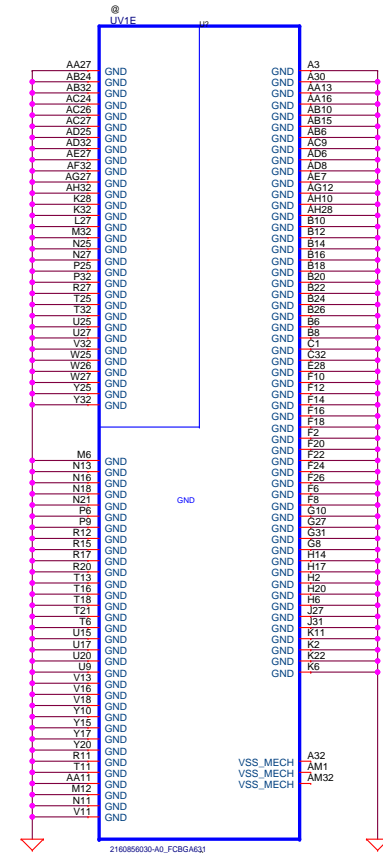
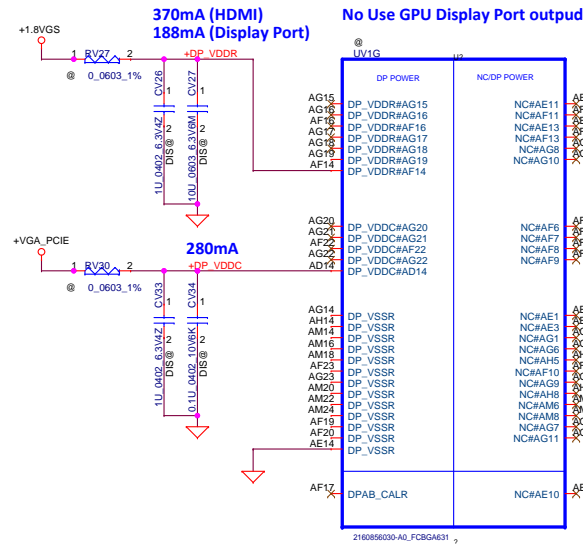
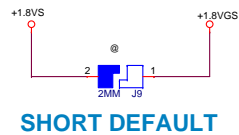
Memory ID	P/N	Vendor	Configuration	Size
(default) 000	SA000068UOL	SAMSUNG	K4W2G1646Q-BC1A	1GB
001	SA00006H4OL	HYNIX	H5TC2G63FFR-11C	1GB
010	SA0000675OL	Micron	MT41J128M16JT-093G	1GB
011	SA000076POL	SAMSUNG	K4W4G1646B-HC11	2GB
(default) 100	SA00006E8OL	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077KOL	Micron	MT41J256M16HA-093G	2GB



+1.35VS_VGA TO +1.35V_MEM_GFX

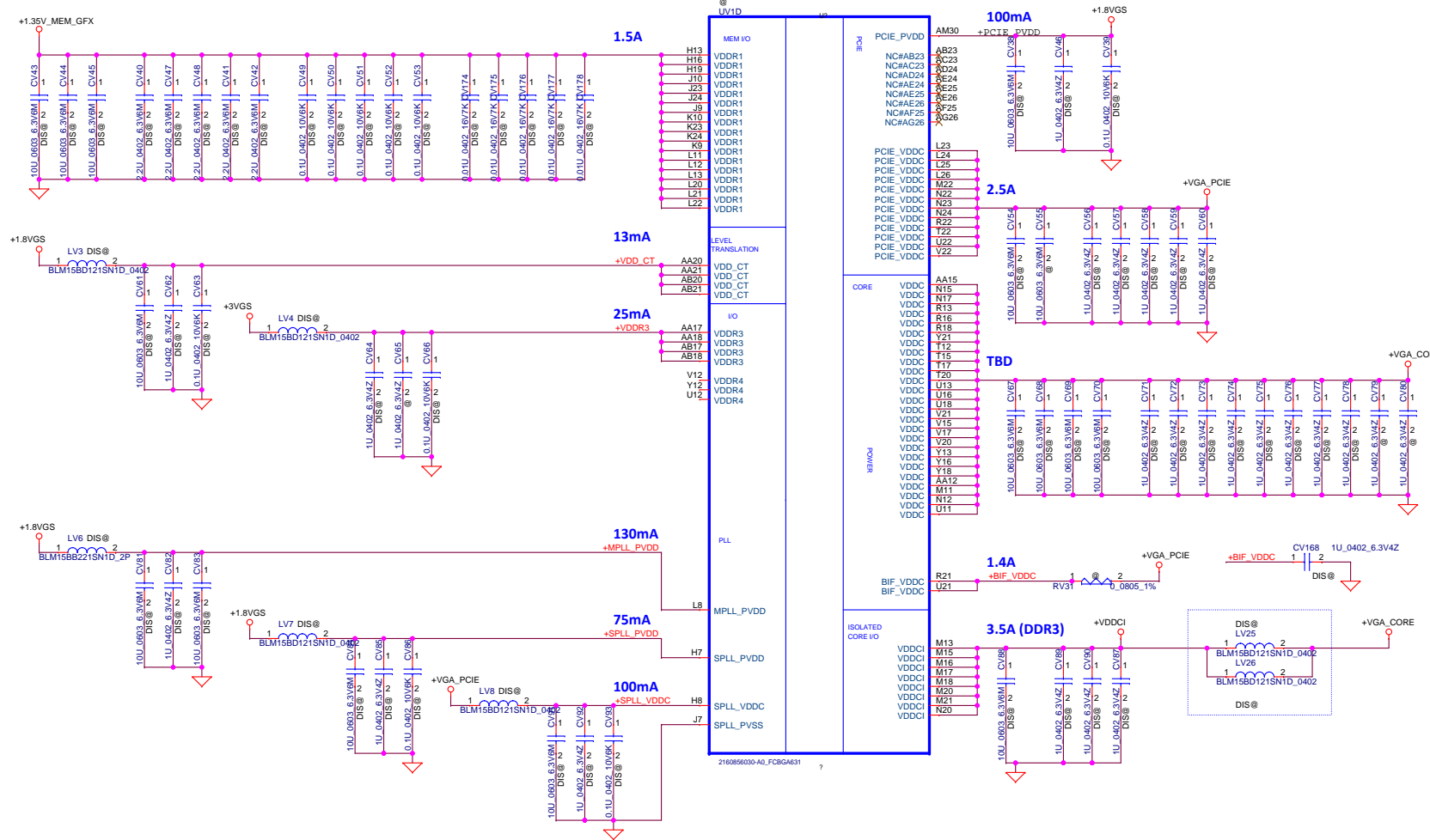


+1.8VS TO +1.8VGS

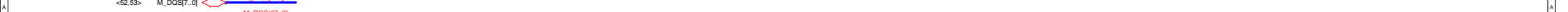


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+3VGS	10uF	1uF	0.1uF
VDDR3 25mA	0	2 (1@)	1



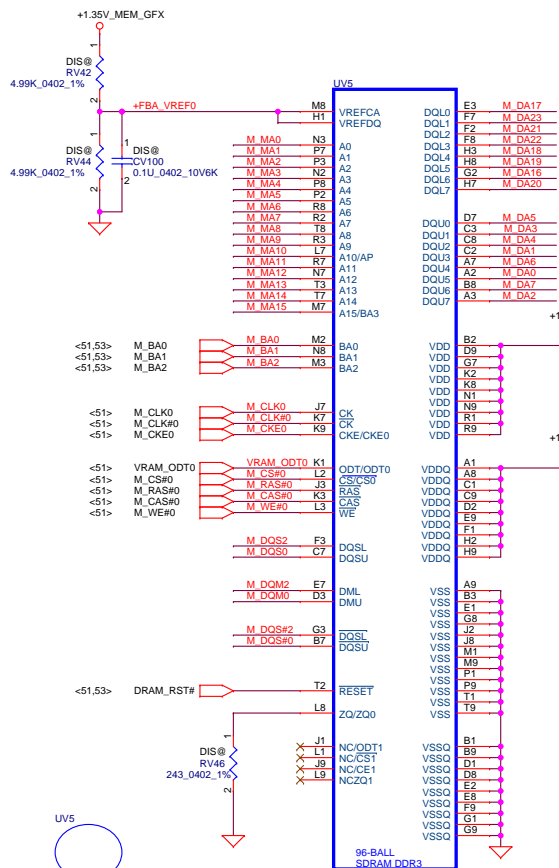
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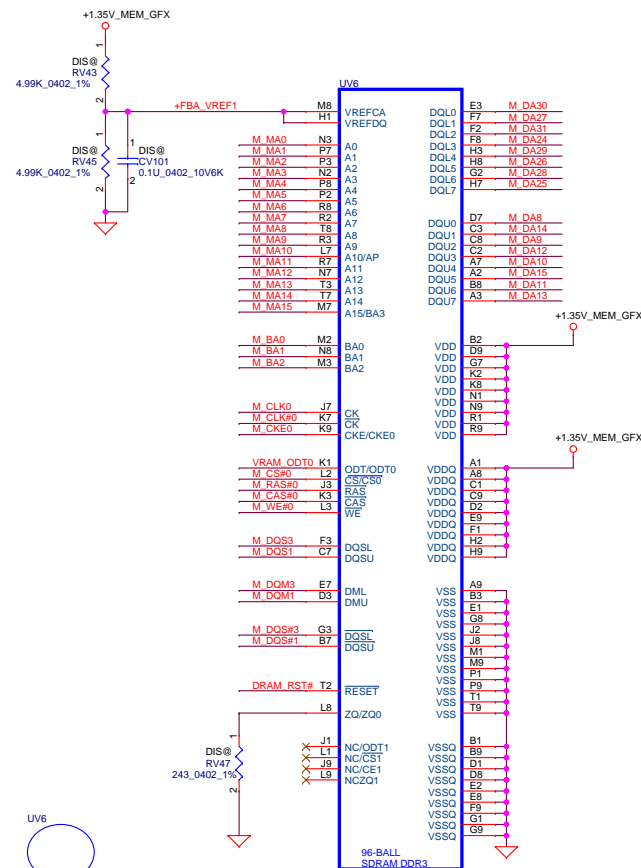
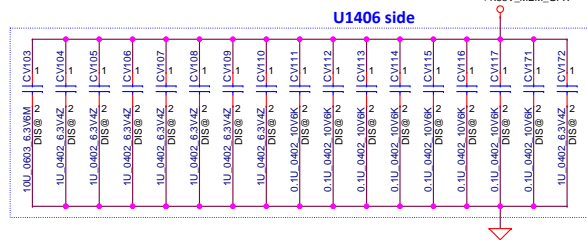
M_DA61	J1	QDA1_29	CASA0B	D19	M_CAS#0	M_CAS#0	<52>
M_DA62	J3	QDA1_20	CASA0B	G16	M_CAS#1	M_CAS#4	<63>

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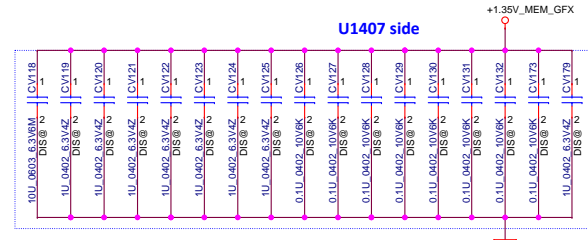
<51,53> M_DA[63..0] M_DA[63..0]
 <51,53> M_MA[15..0] M_MA[15..0]
 <51,53> M_DQM[7..0] M_DQM[7..0]
 <51,53> M_DQS[7..0] M_DQS[7..0]
 <51,53> M_DQS[7..0] M_DQS[7..0]



U1406
 256MX16 H5TC4G63AFR-11C FBGA 96P
 SA00006E80L
 2G@

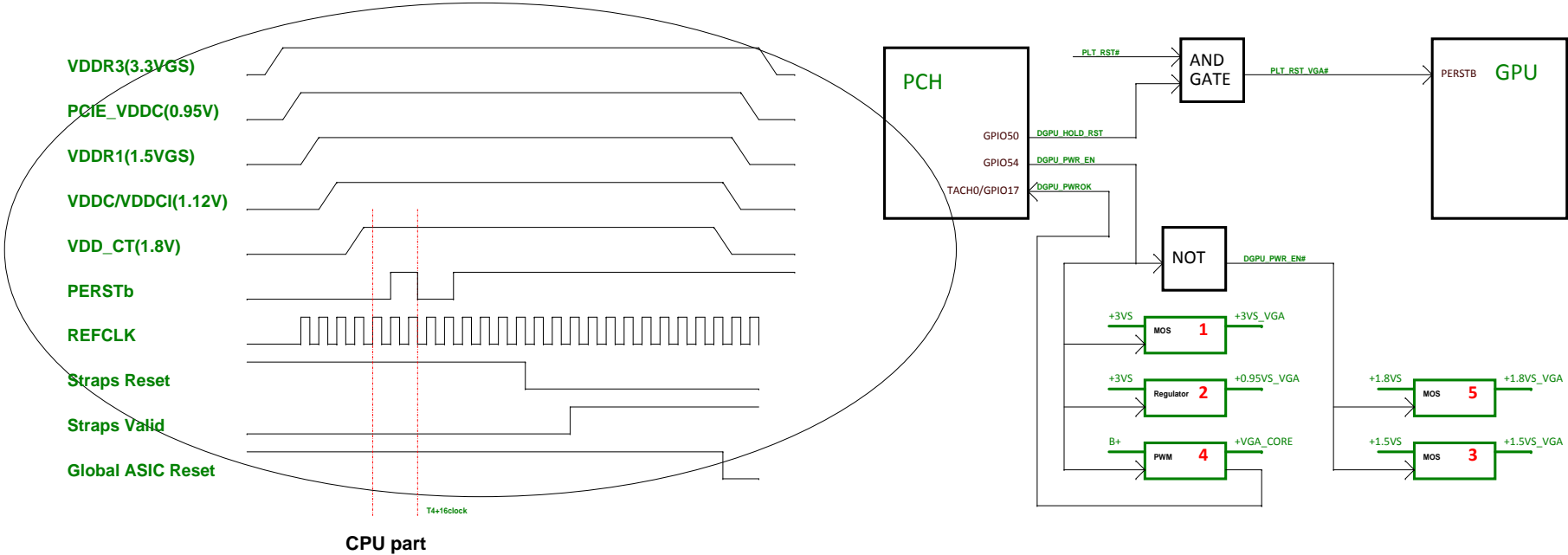


U1407
 256MX16 H5TC4G63AFR-11C FBGA 96P
 SA00006E80L
 2G@



Power-Up/Down Sequence

- 1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- 2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- 3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- 4. For power down, reversing the ramp-up sequence is recommended.



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