

MODEL NAME : Maple  
PCB NO : DA8000WL000 LA-B012PR01

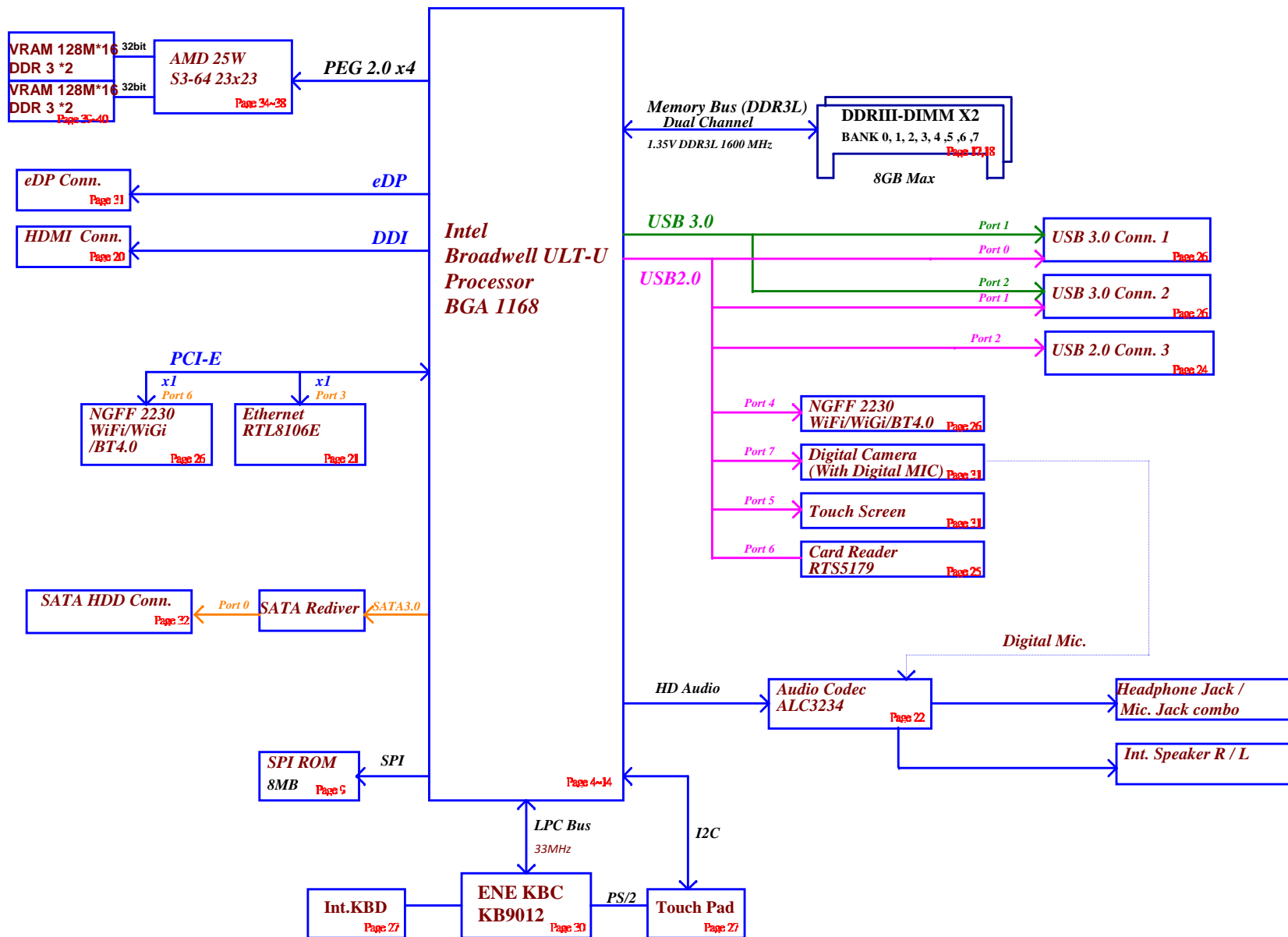
# Dell / Compal Confidential

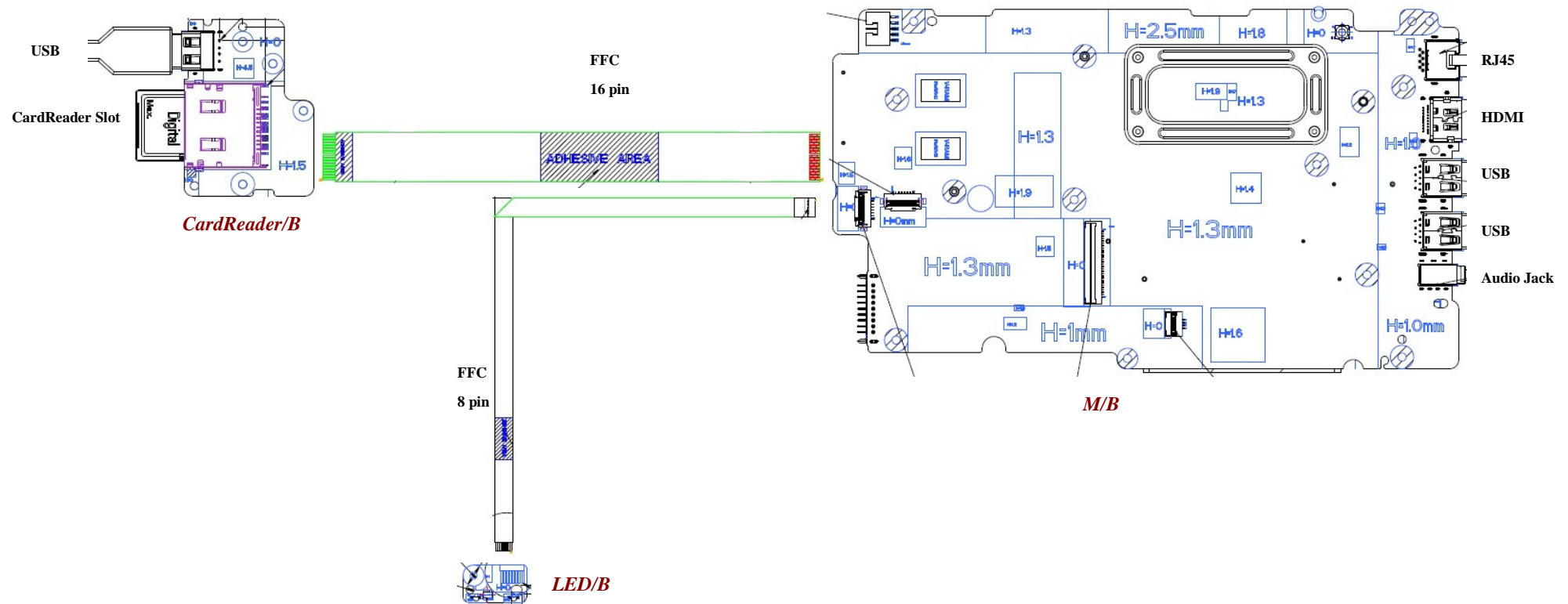
## Schematic Document

Intel Shark Bay ULT  
Maple 14"/15" Value  
UMA / DIS AMD 25W/S3+DDR3x4

2014-01-21      Rev: 1.0

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# Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XD	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V	V		V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

## HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)
0	SSI		
1		SSI	
2			SSI
3	PT		
4		PT	
5			PT
6	ST		
7		ST	
8			ST
9	1.0		
10		1.0	
11			1.0

## BDW BOARD ID Table

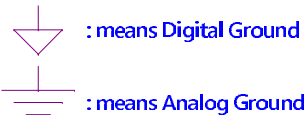
Board ID	UMA	DIS(JET)	DIS(Topaz)
0	Pre-SSI		
1		Pre-SSI	
2			Pre-SSI
3	SSI		
4		SSI	
5			SSI
6	PT		
7		PT	
8			PT
9	ST		
10		ST	
11			ST
12	1.0		
13		1.0	
14			1.0

Link

## CLOCK SIGNAL

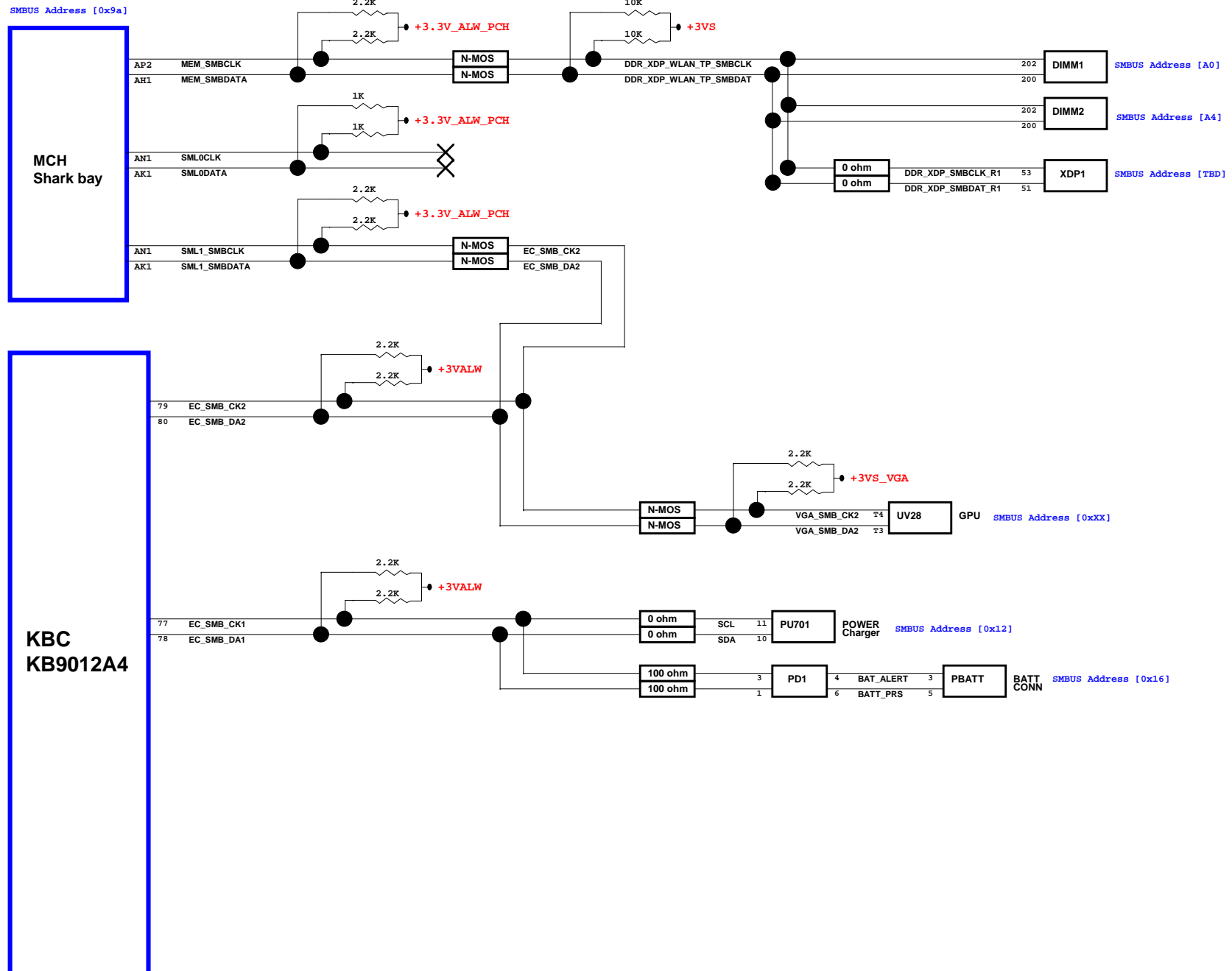
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

Symbol Note :



ULT

USB3.0	
Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	
USB2.0	
Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (D/B)
Port3	
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (AMD JET/TOBAZ)
Lane 6	
SATA	
SATA0	HDD
SATA1	
SATA2	
SATA3	



I3-4020U-15W-GT2-MP

UC1 IR10  
CL8064701552800 QEZ5 D0 1.8G  
SA00007MGOL

UC2 IR300  
CL8064701478202 SR16Q C1 1.7G A31!  
SA00006SX2L TBD

I5-4210U-15W-GT2-MP

UC4 IR10  
CL8064701477802 QEAK D0 1.7G  
SA00007LOOL

UC5 IR300  
CL8064701477702 SR170 C1 1.6G A31!  
SA00006SM3L TBD

I7-4510U-15W-GT2-MP

UC7 IR10  
CL8064701477301 QEAF D0 2G BGA  
SA00007M7UL

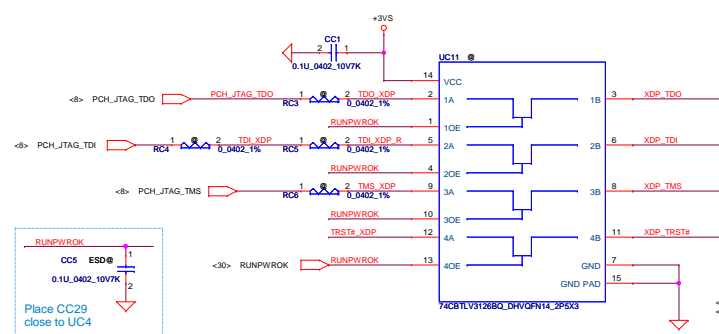
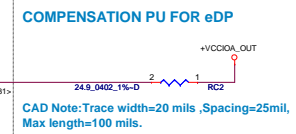
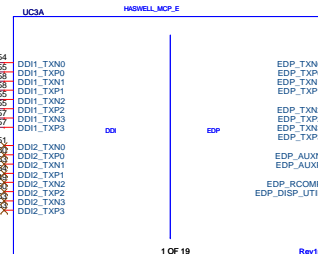
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CL8064701477202 SR16Z C1 1.8G A31!  
SA00006SL2L TBD

UC9 QFSY0  
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SA00007AMXL

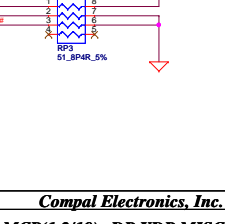
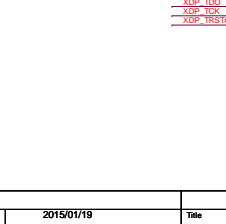
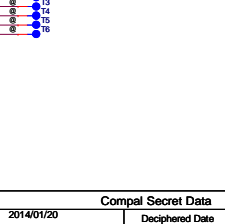
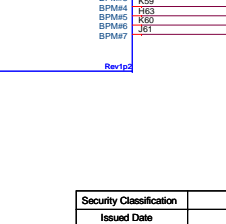
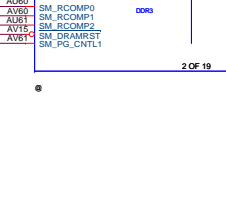
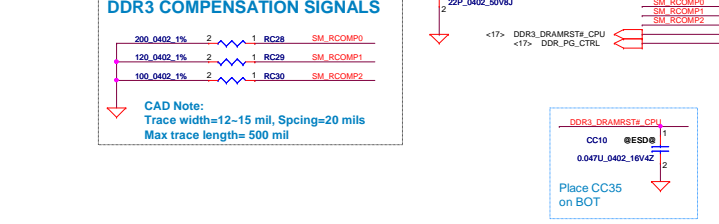
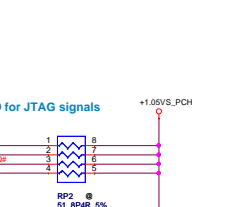
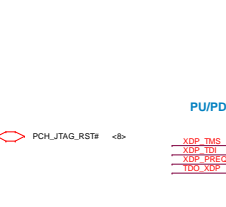
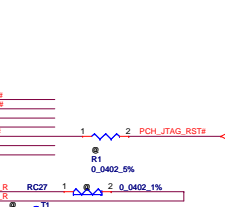
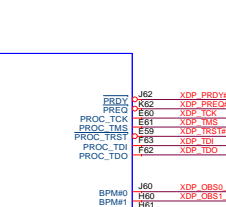
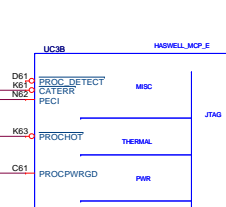
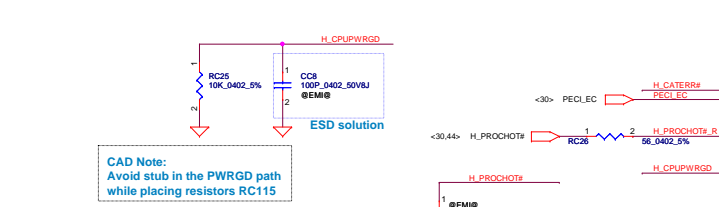
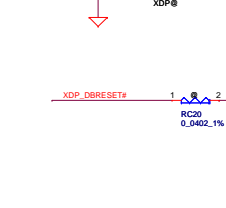
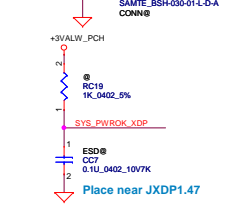
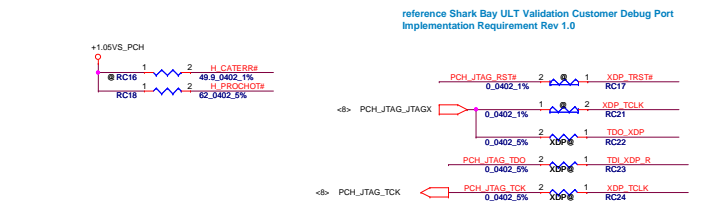
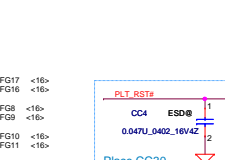
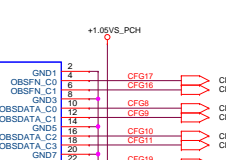
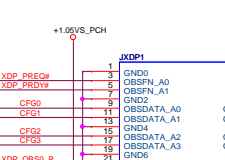
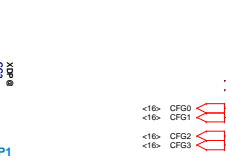
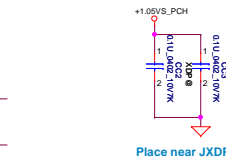
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SA00007OTOL

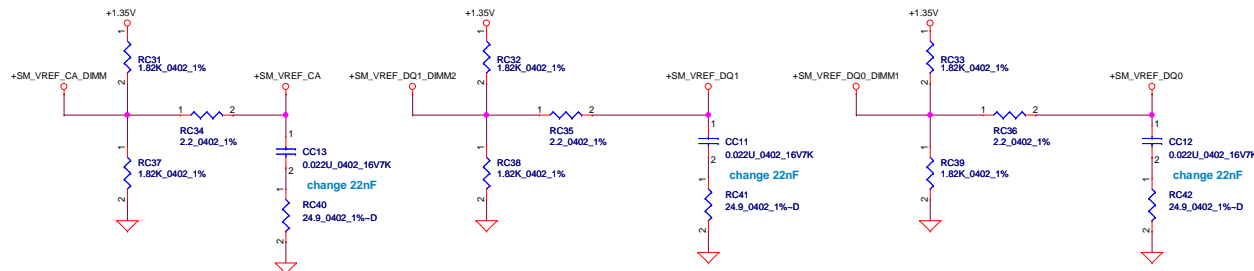
Broadwell



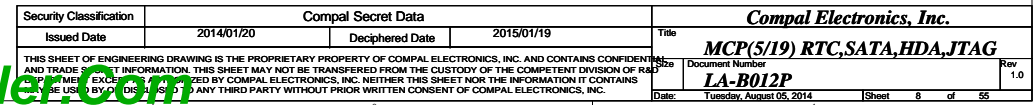
reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0



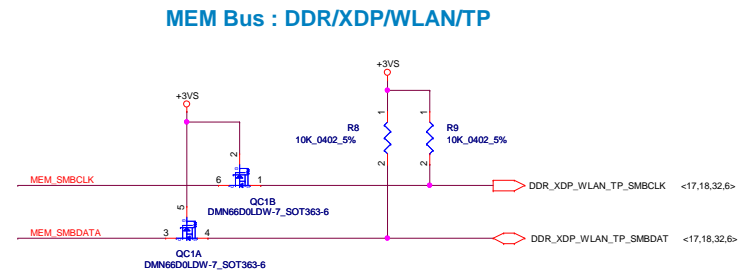
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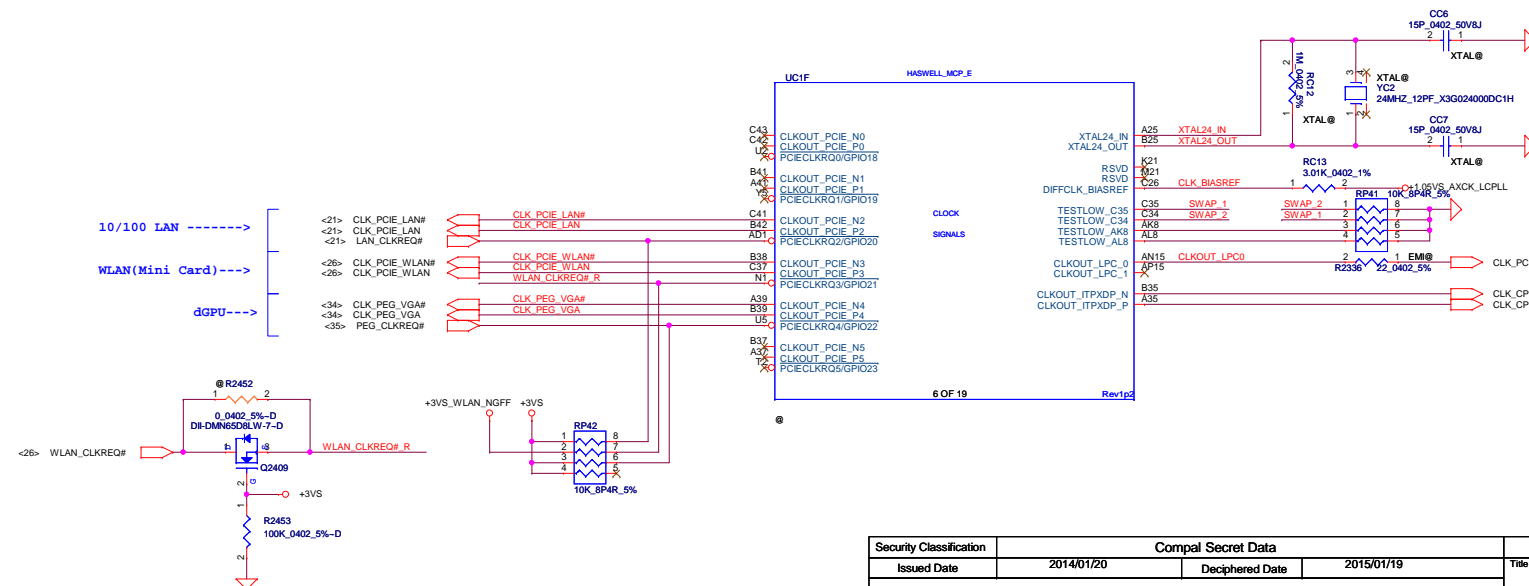
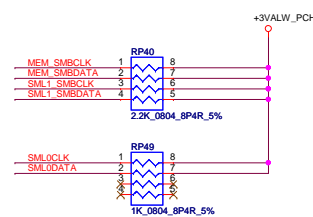
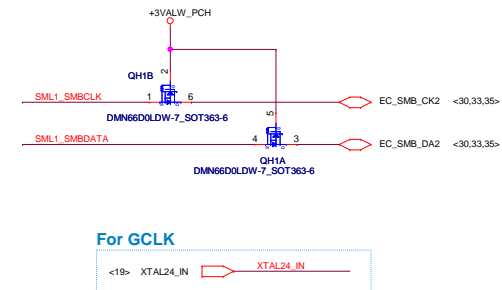
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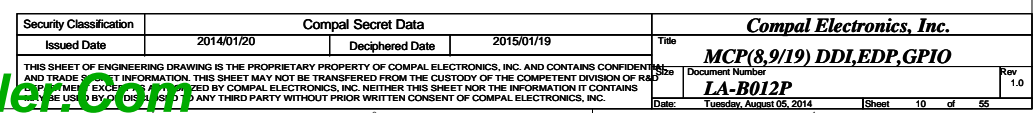


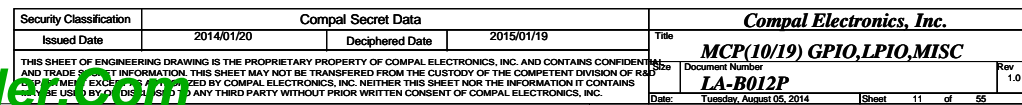


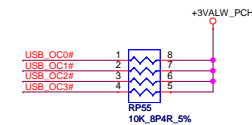
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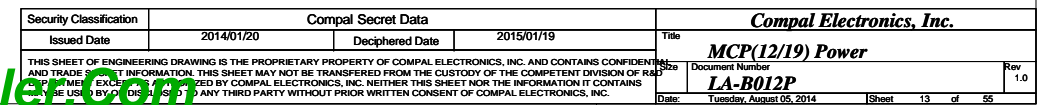
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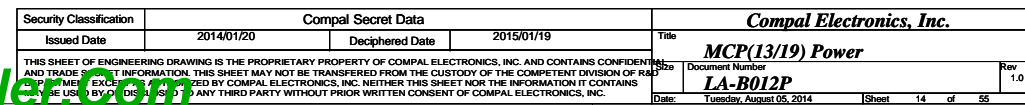


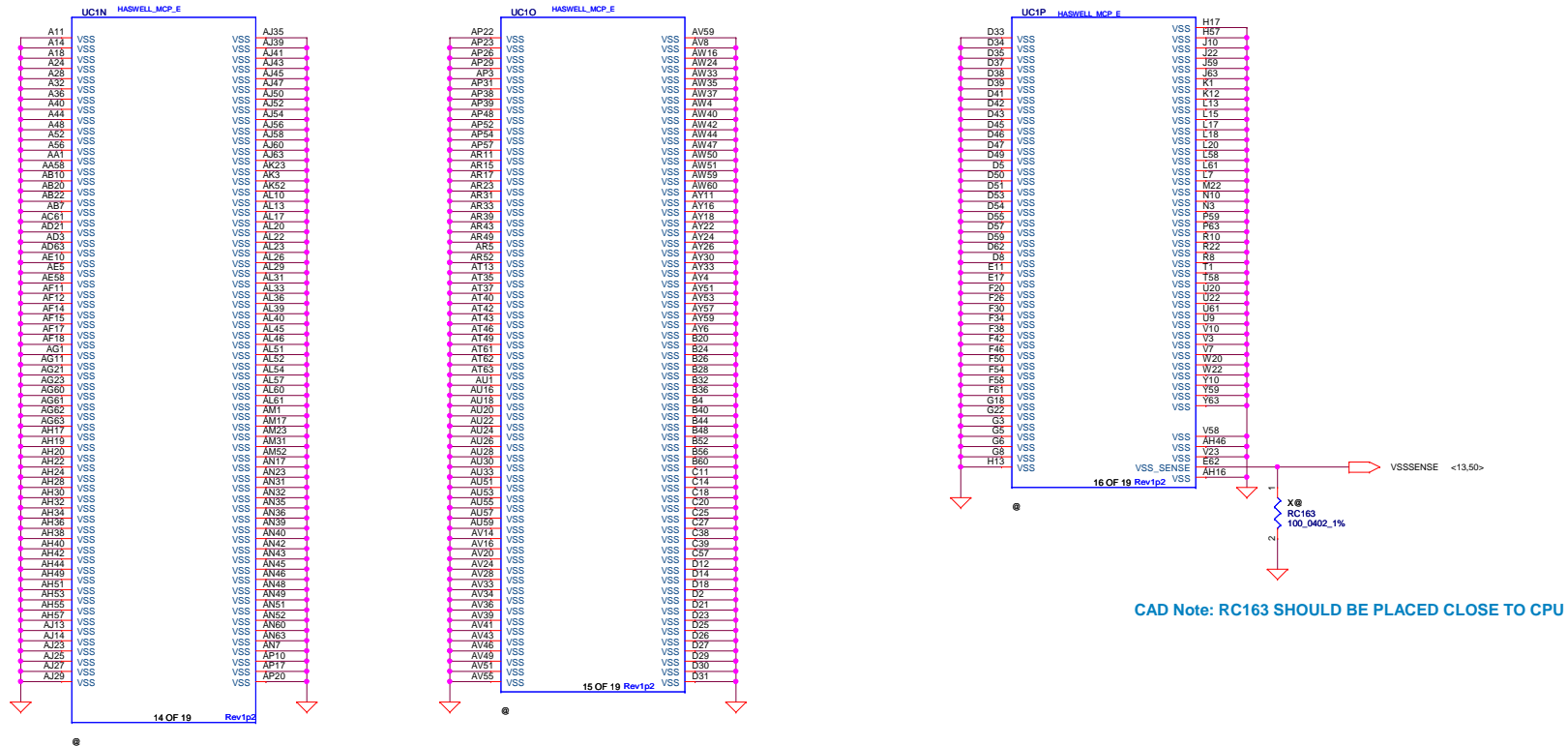


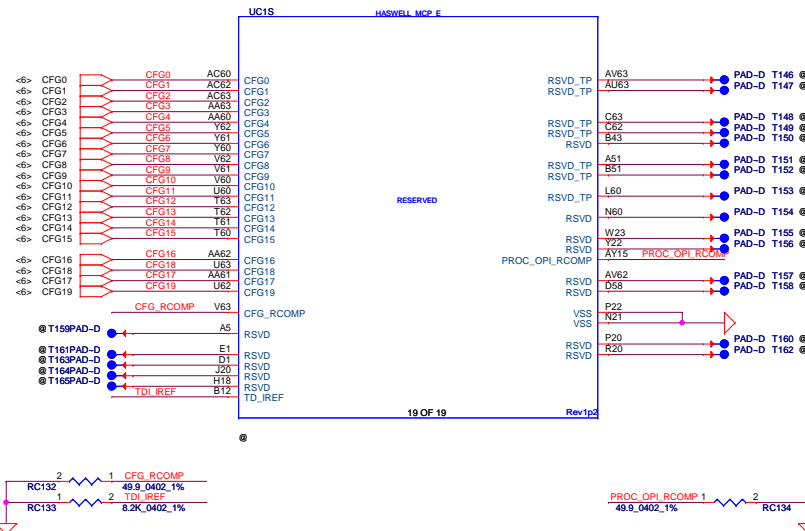
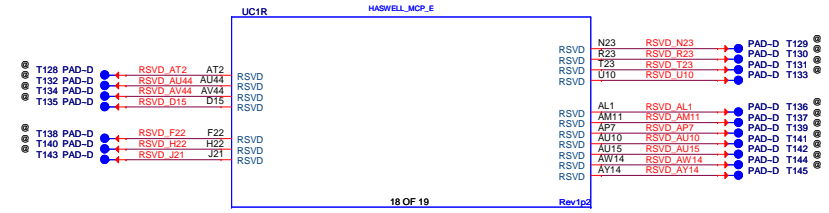
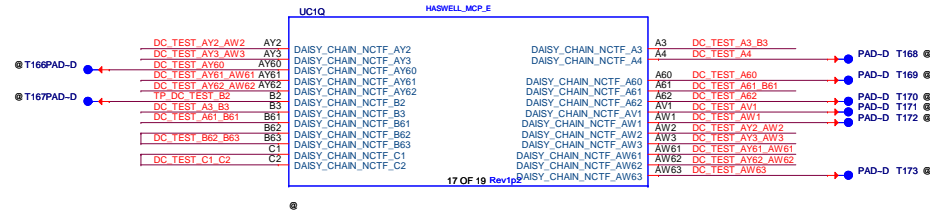


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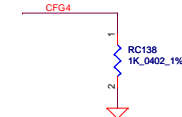






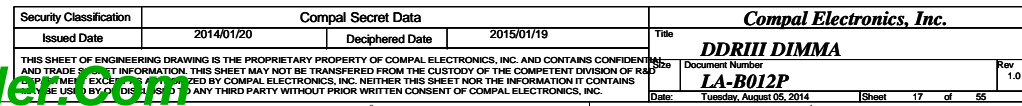


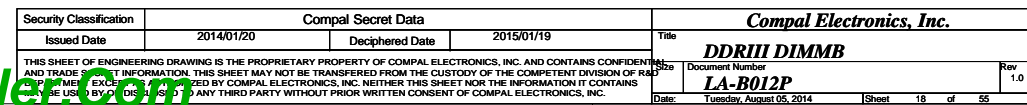
## CFG STRAPS for CPU

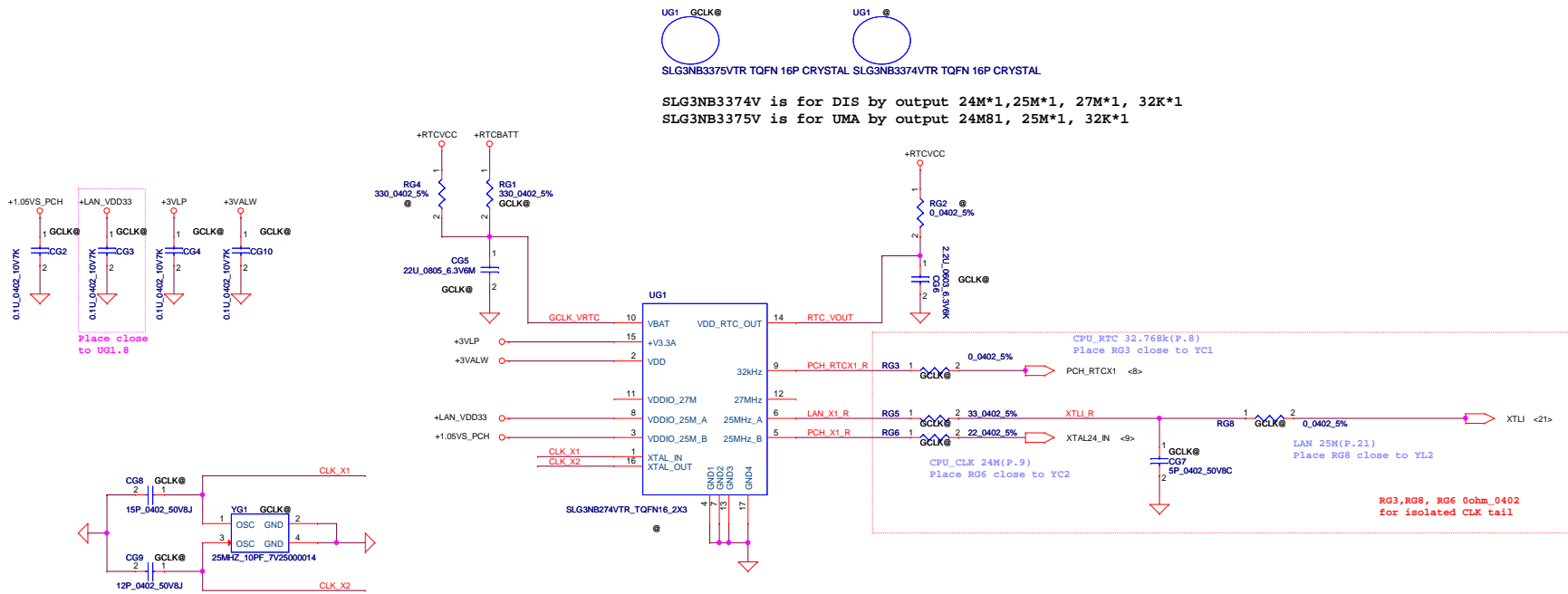


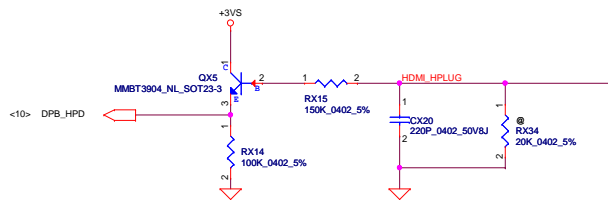
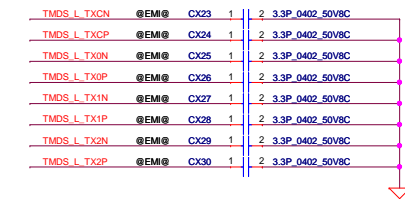
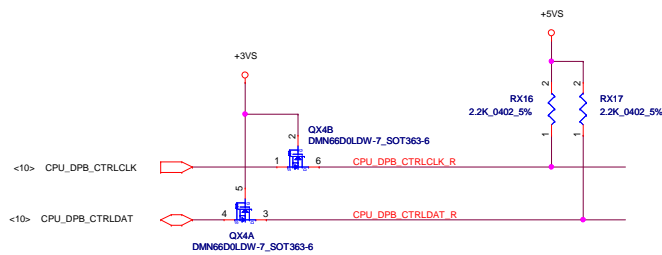
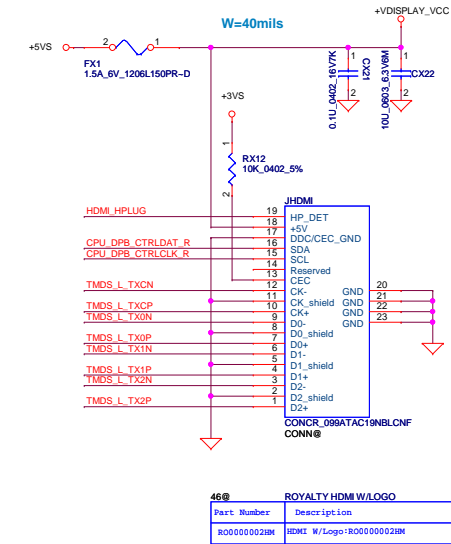
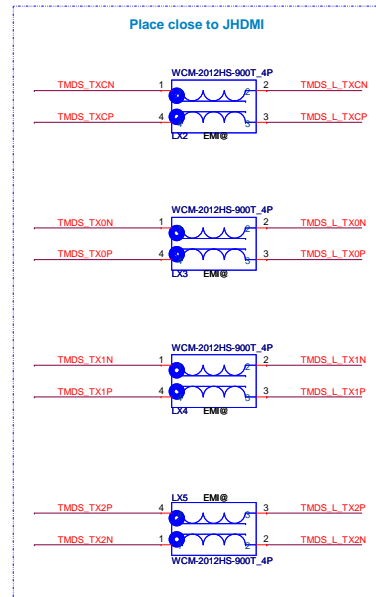
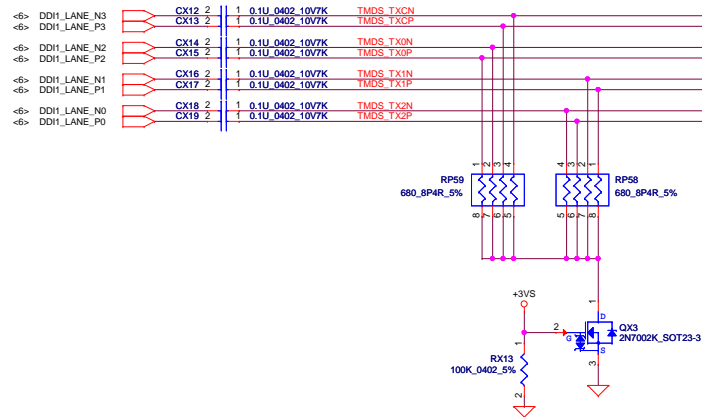
Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

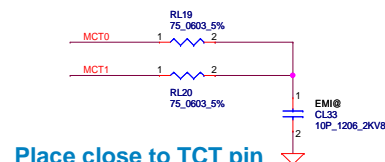
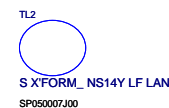
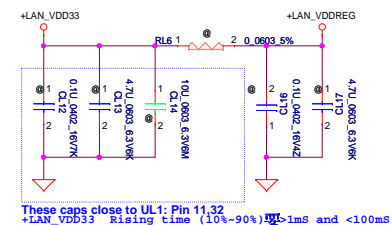
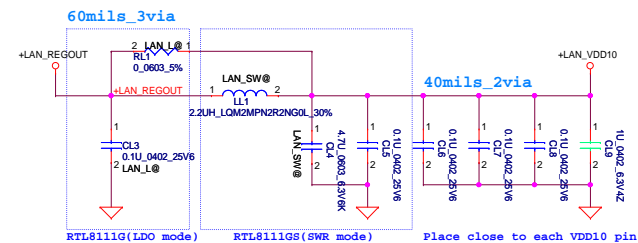




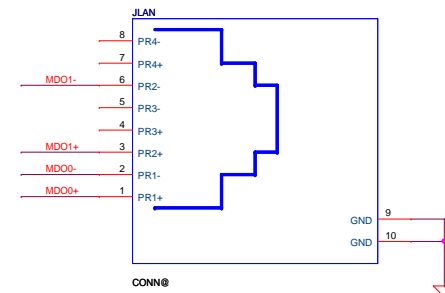
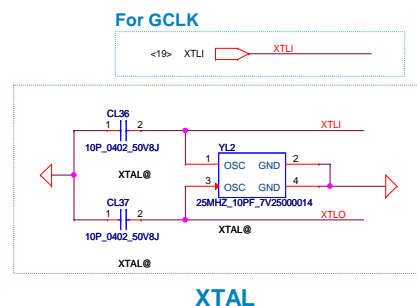






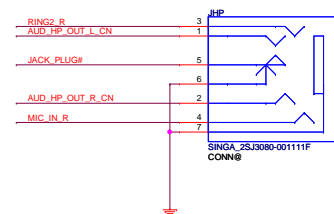


**Place close to TCT pin**

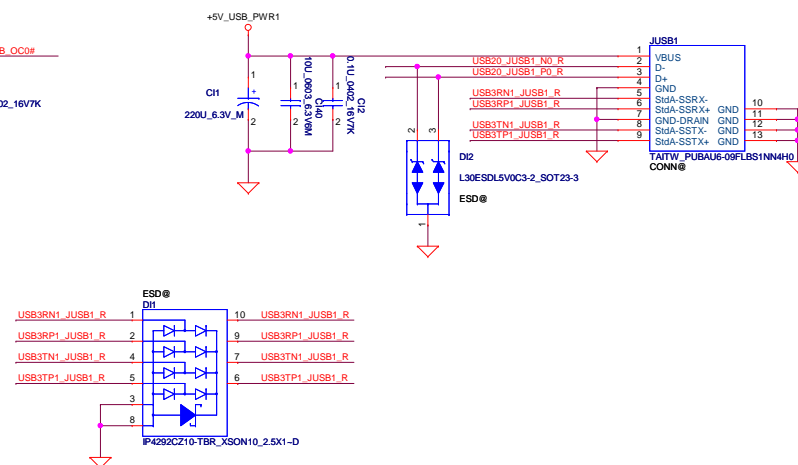
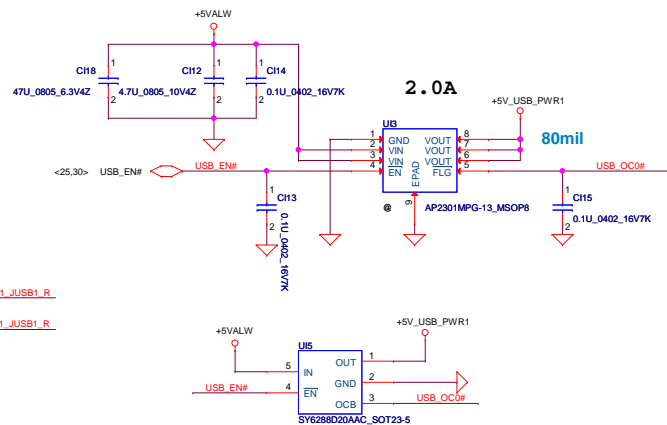


## Reserve 10K pull LAN\_IO

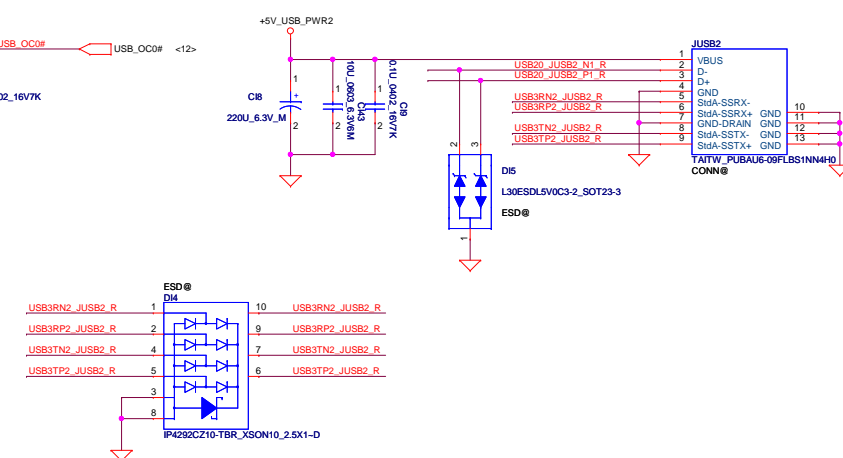
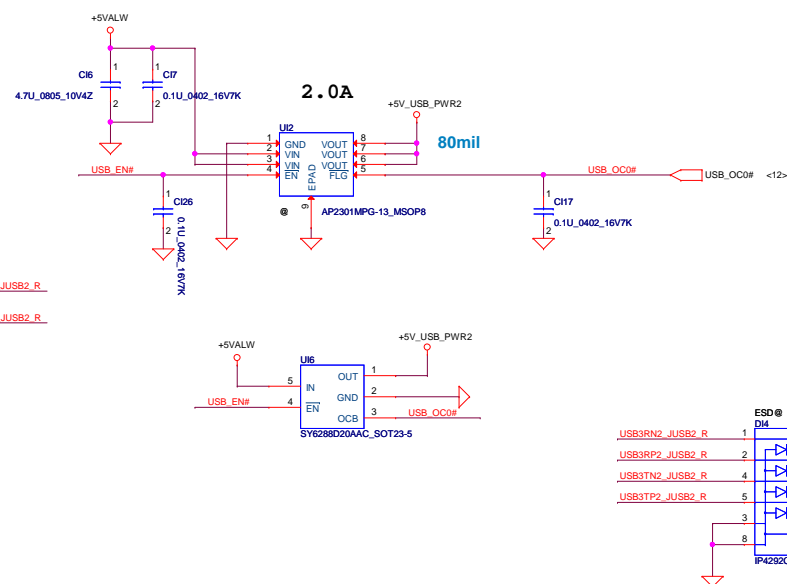
WWW.AliSaler.Com



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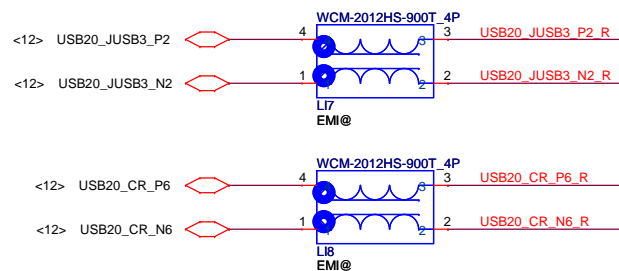
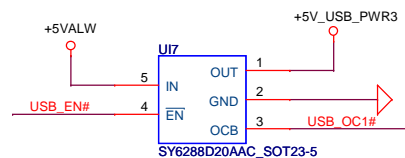
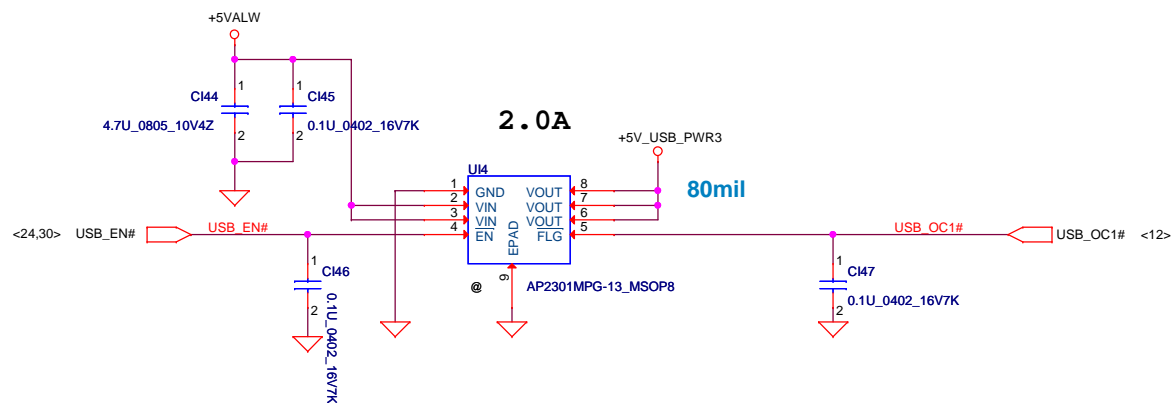


USB connector2  
USB20 port0  
USB30 port1

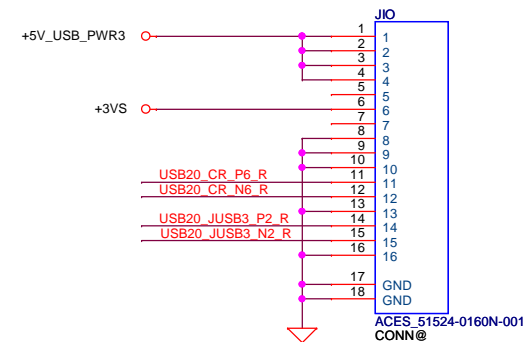


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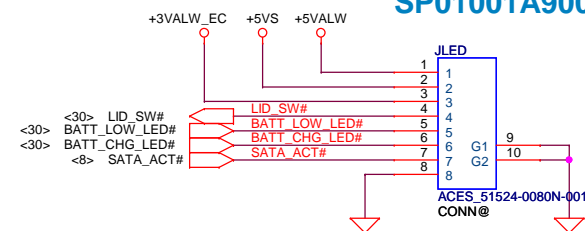




## IO to MB CONN Substitute:SP01001FS00

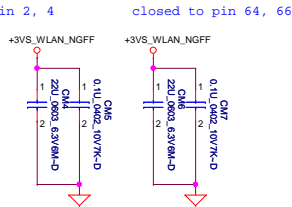
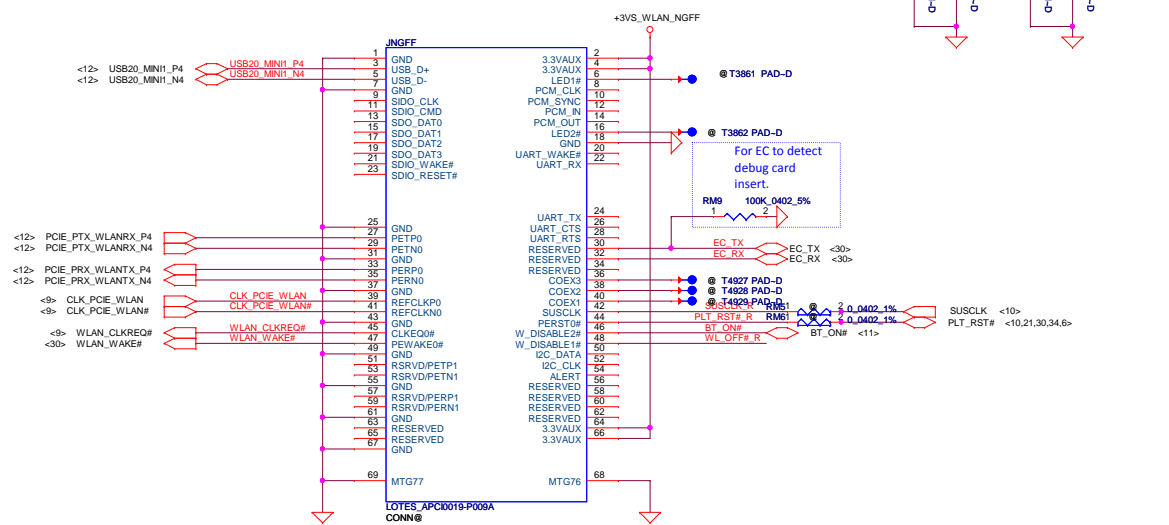


## LED/B TO M/B SP01001A900

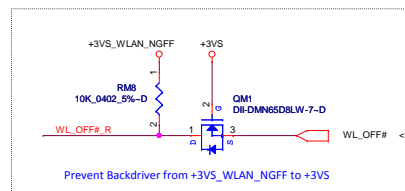
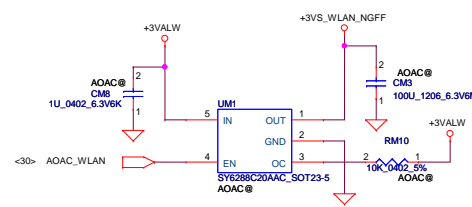
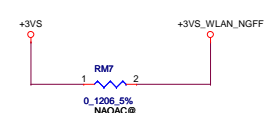


Security Classification		Compal Secret Data								
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								Size	Document Number	Rev
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# NGFF WL Con (E Key)



## +3VALW TO +3VS\_WLAN\_NGFF

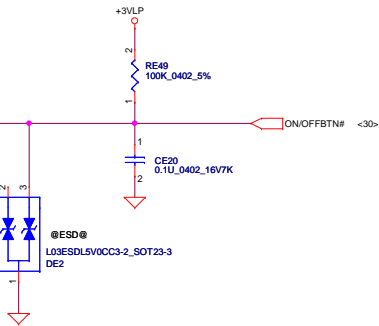
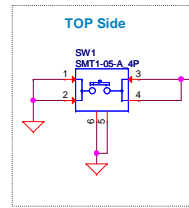


Prevent Backdriver from +3VS\_WLAN\_NGFF to +3VS

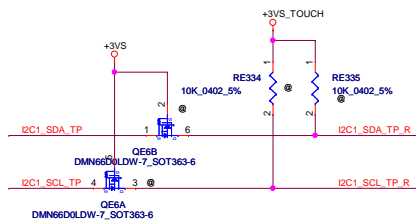
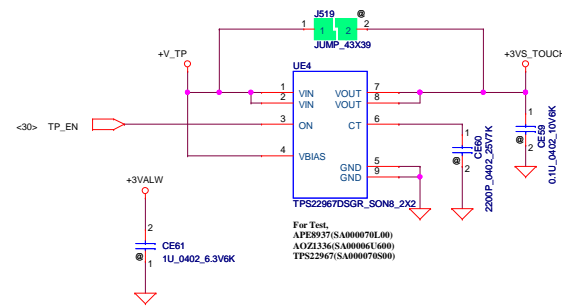
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Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	
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				Document Number	Rev
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## Power ON Circuit

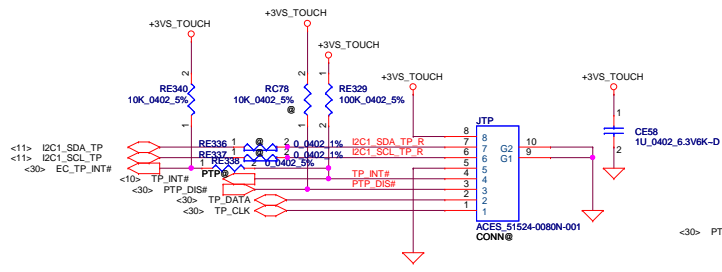
### ON/OFF switch



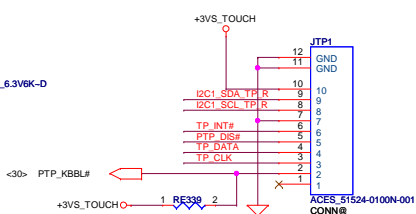
### J519 short



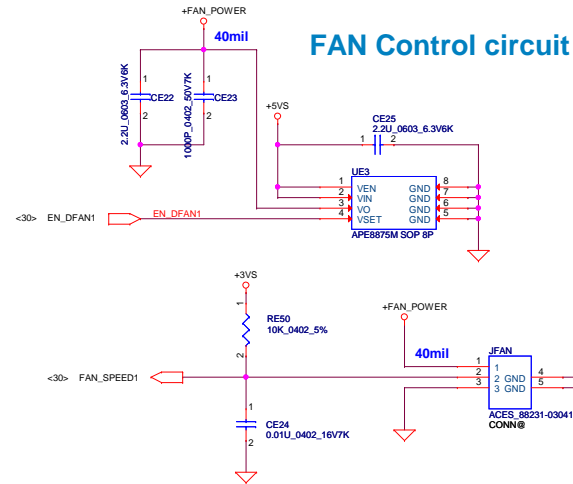
## Touch pad



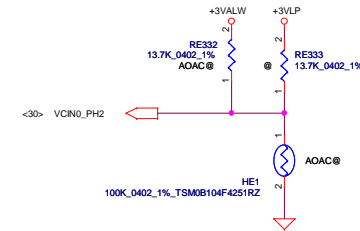
## PTP



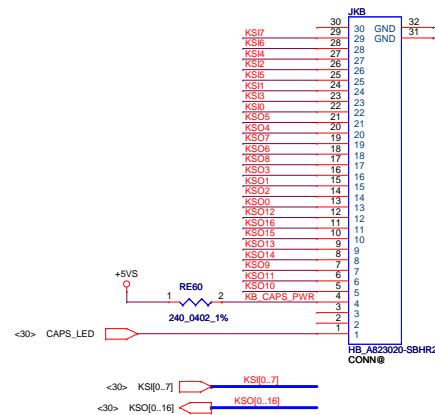
## FAN Control circuit



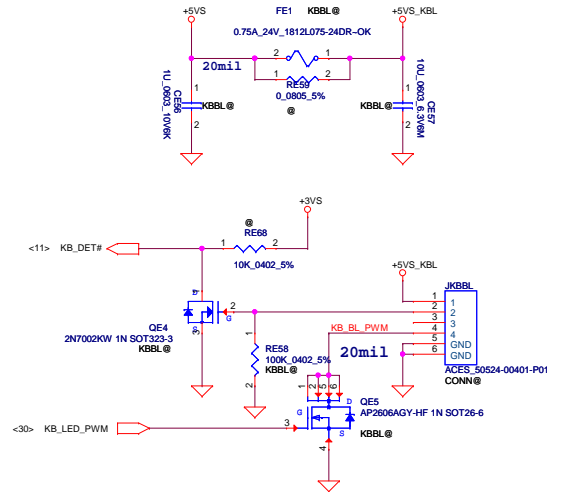
HE1 place around FAN area.



## INT\_KBD Connector

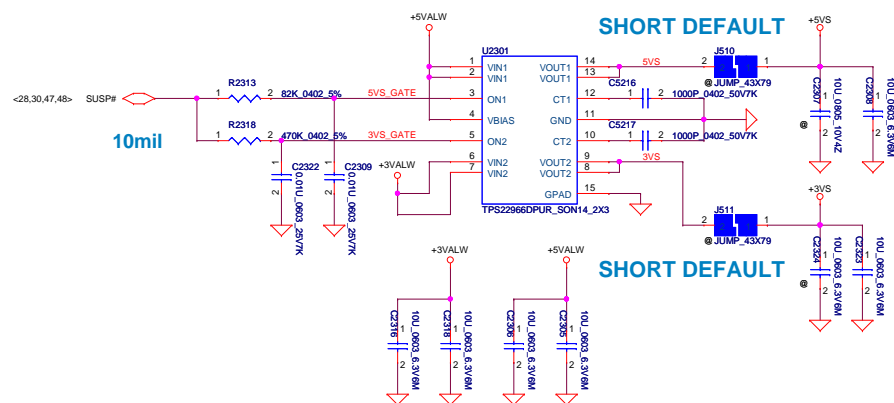


## \* Key Board Back Light

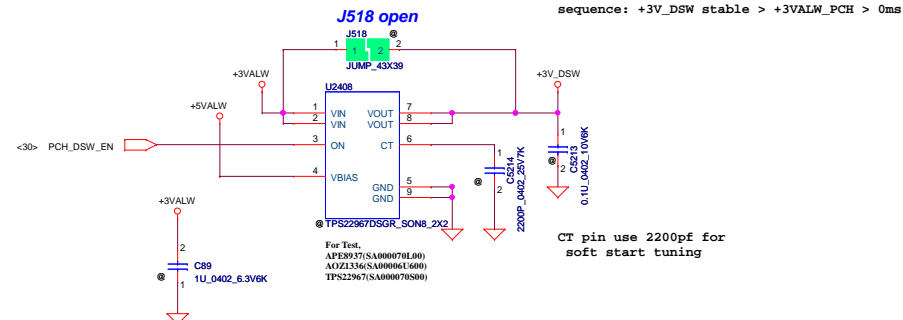


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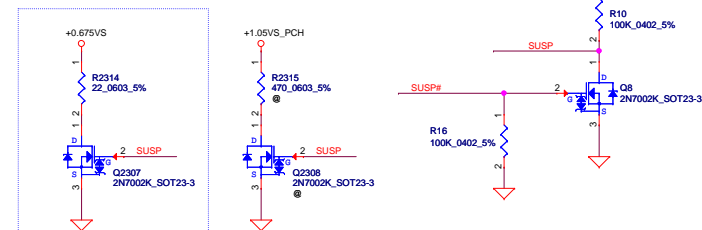
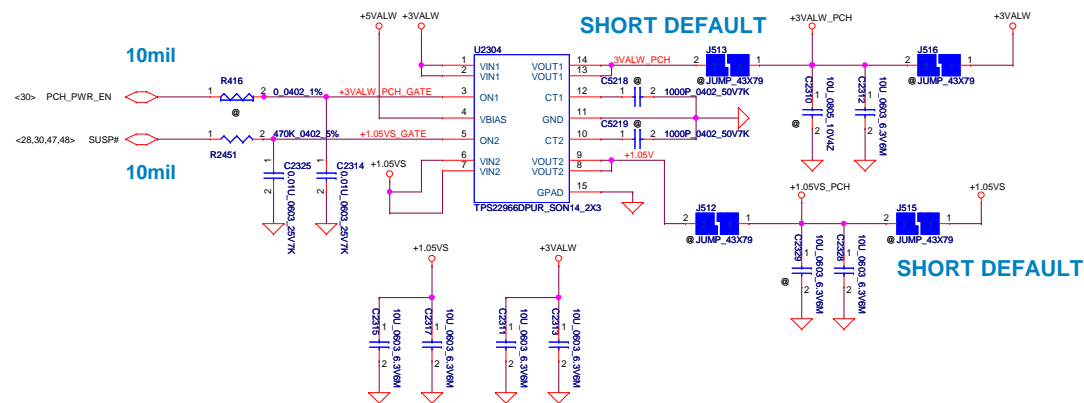
## +5VS and +3VS switch



## +3VALW TO +3V\_DSW



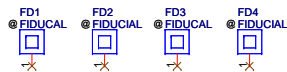
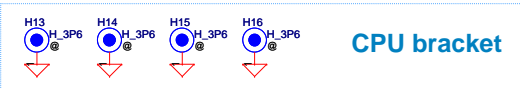
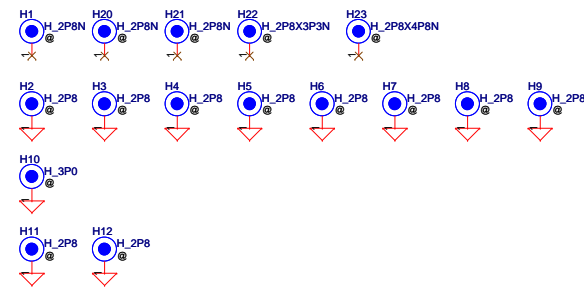
## +3VALW\_PCH switch



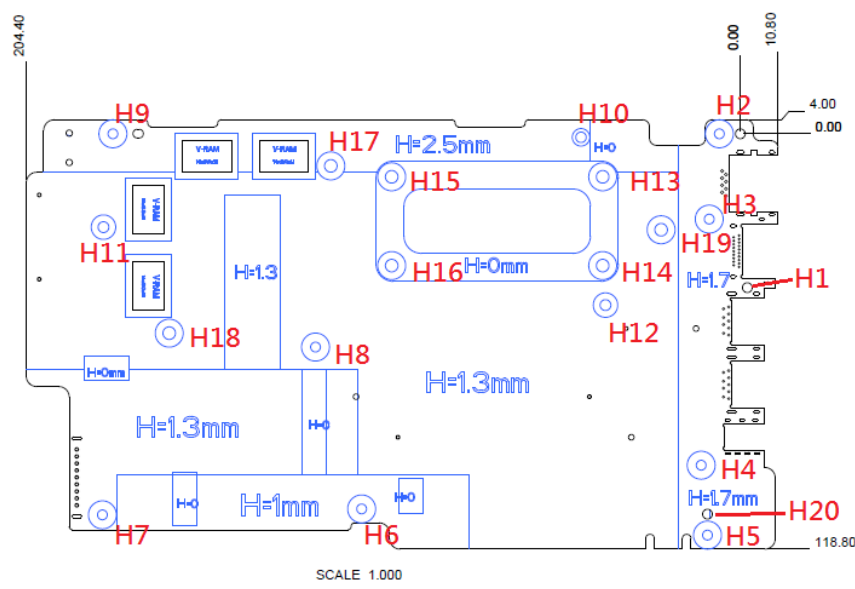
For Intel S3 Power Reduction

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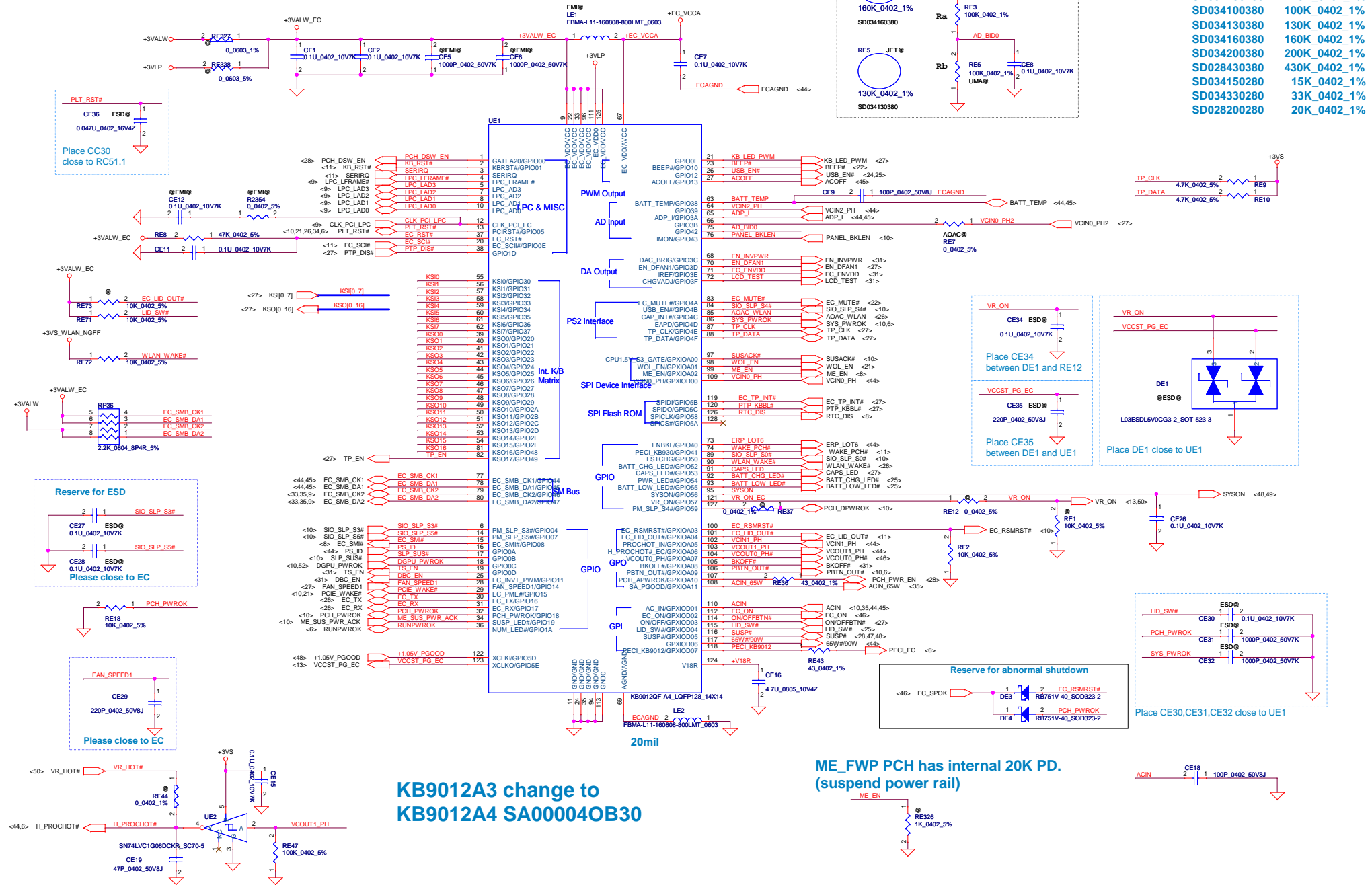
Screw Hole

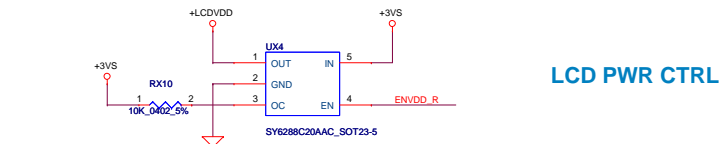


ZZZ  
PCB 13P LA-B011P REV0 M/B  
DA60013U000

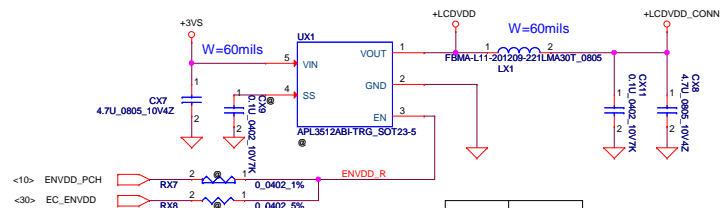


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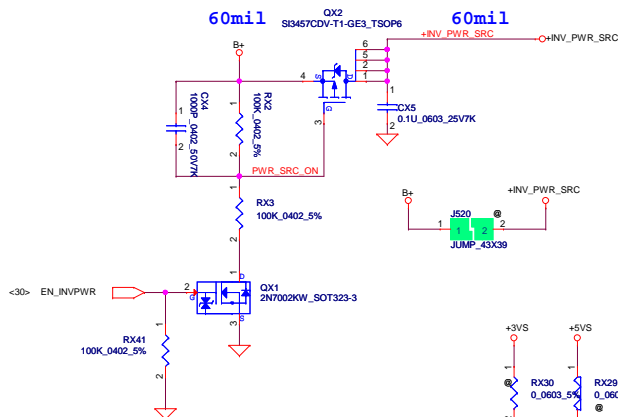


LCD PWR CTRL

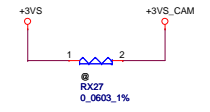


SS table

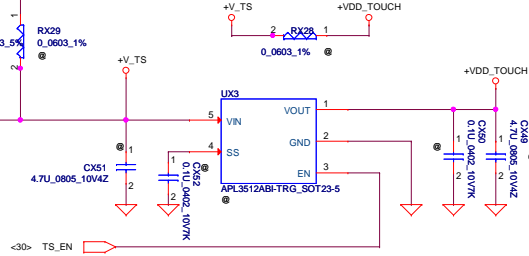
LCD backlight PWR CTRL



Webcam PWR CTRL

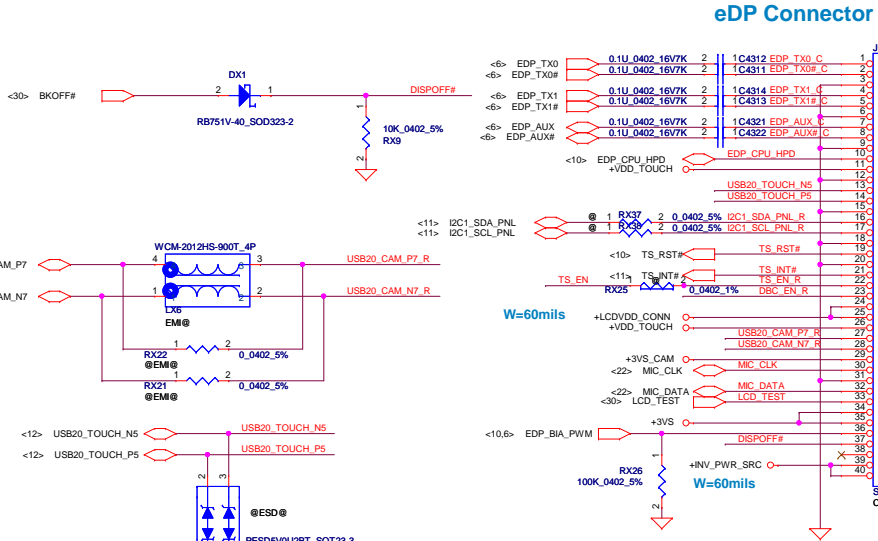


\* Touch Screen Panel

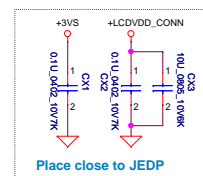
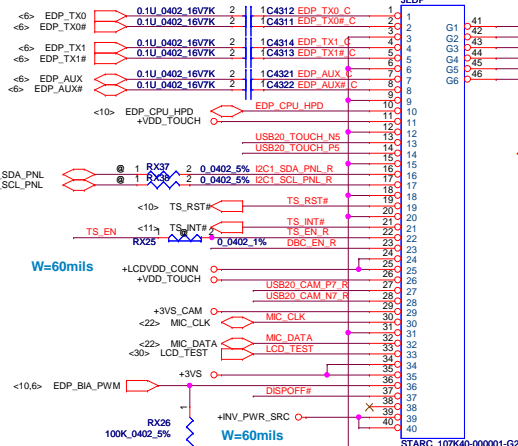


SS table

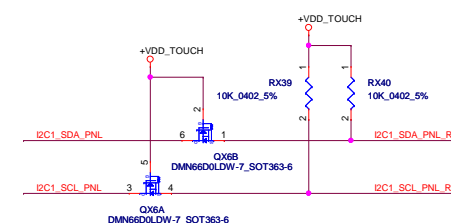
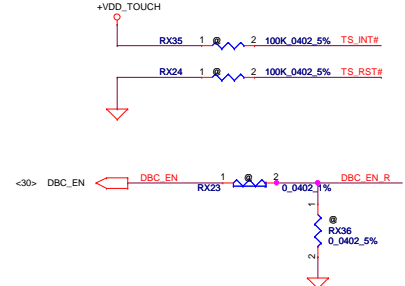
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

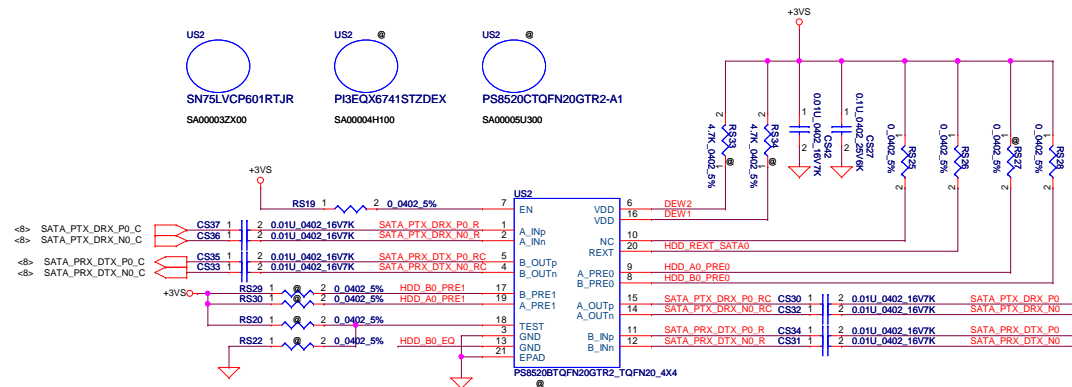


eDP Connector



Place close to JEDP





Pin 20:  
PARADE PS8250B:  
Depop RS26

PERICOM PI3EQX6741ST:  
Pop RS26

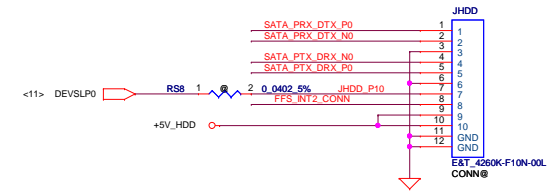
ASMEDIA ASM1466:  
Pop RS26

Pin 9:  
PARADE PS8250B:  
Depop RS24

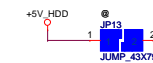
PERICOM PI3EQX6741ST:  
Depop RS24

ASMEDIA ASM1466:  
Pop RS24 to pull down

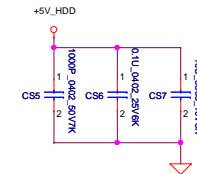
## SATA HDD Connector



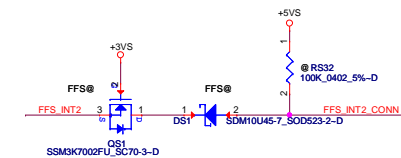
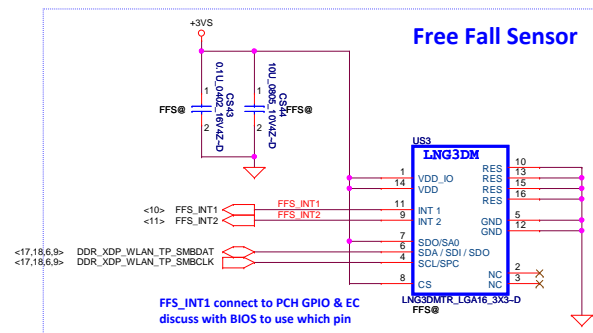
## +5V\_HDD Source



## SHORT DEFAULT



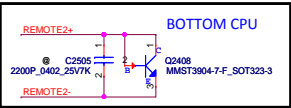
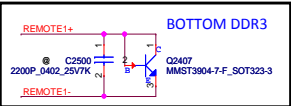
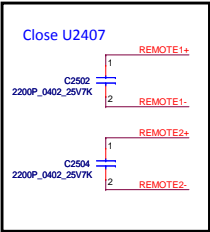
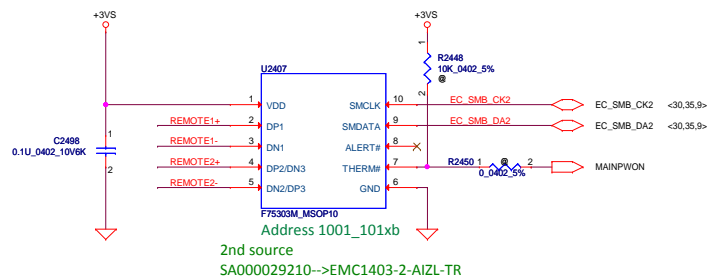
## Free Fall Sensor



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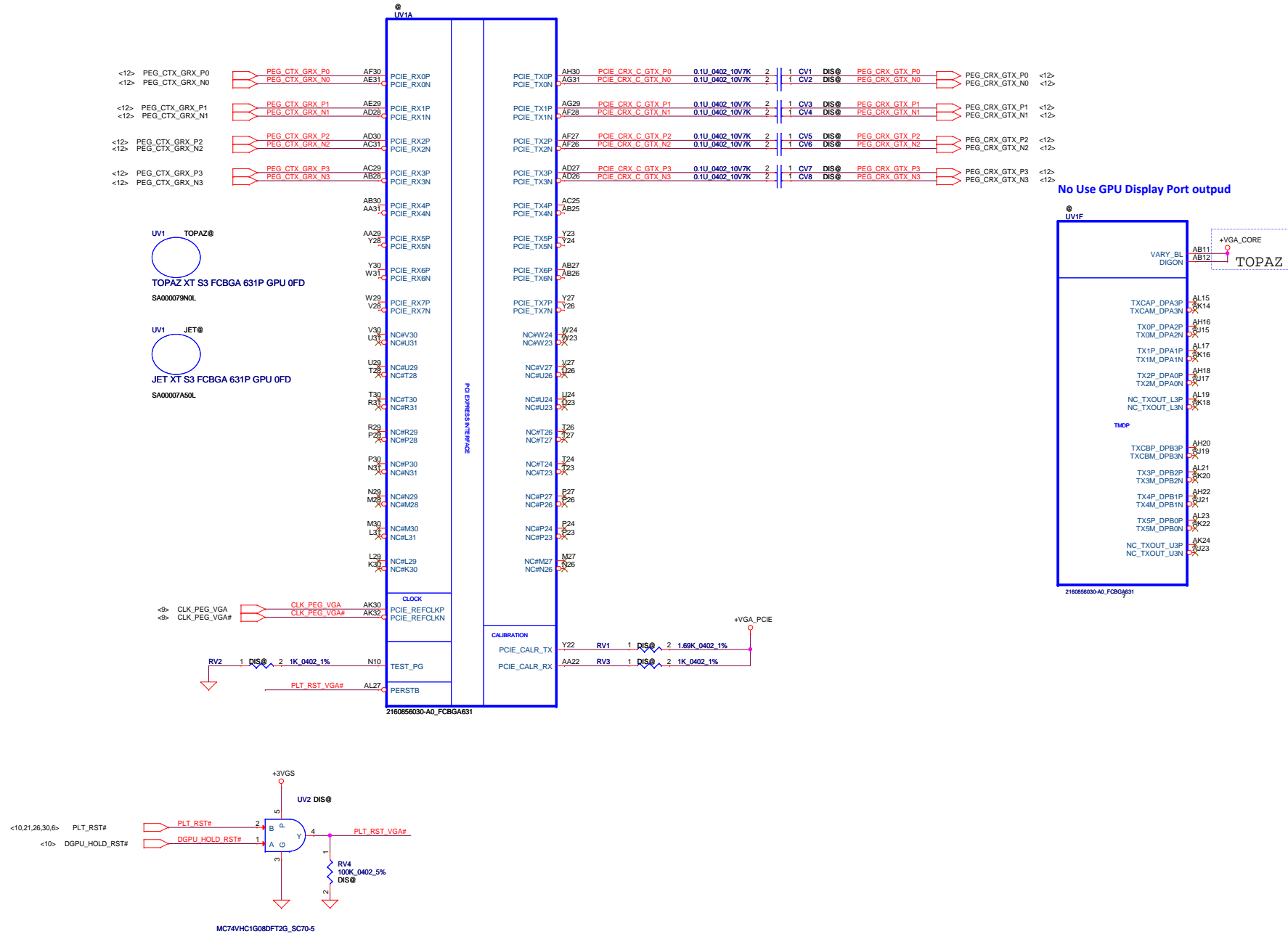


Fintek thermal sensor  
placed near by TOP DDR3

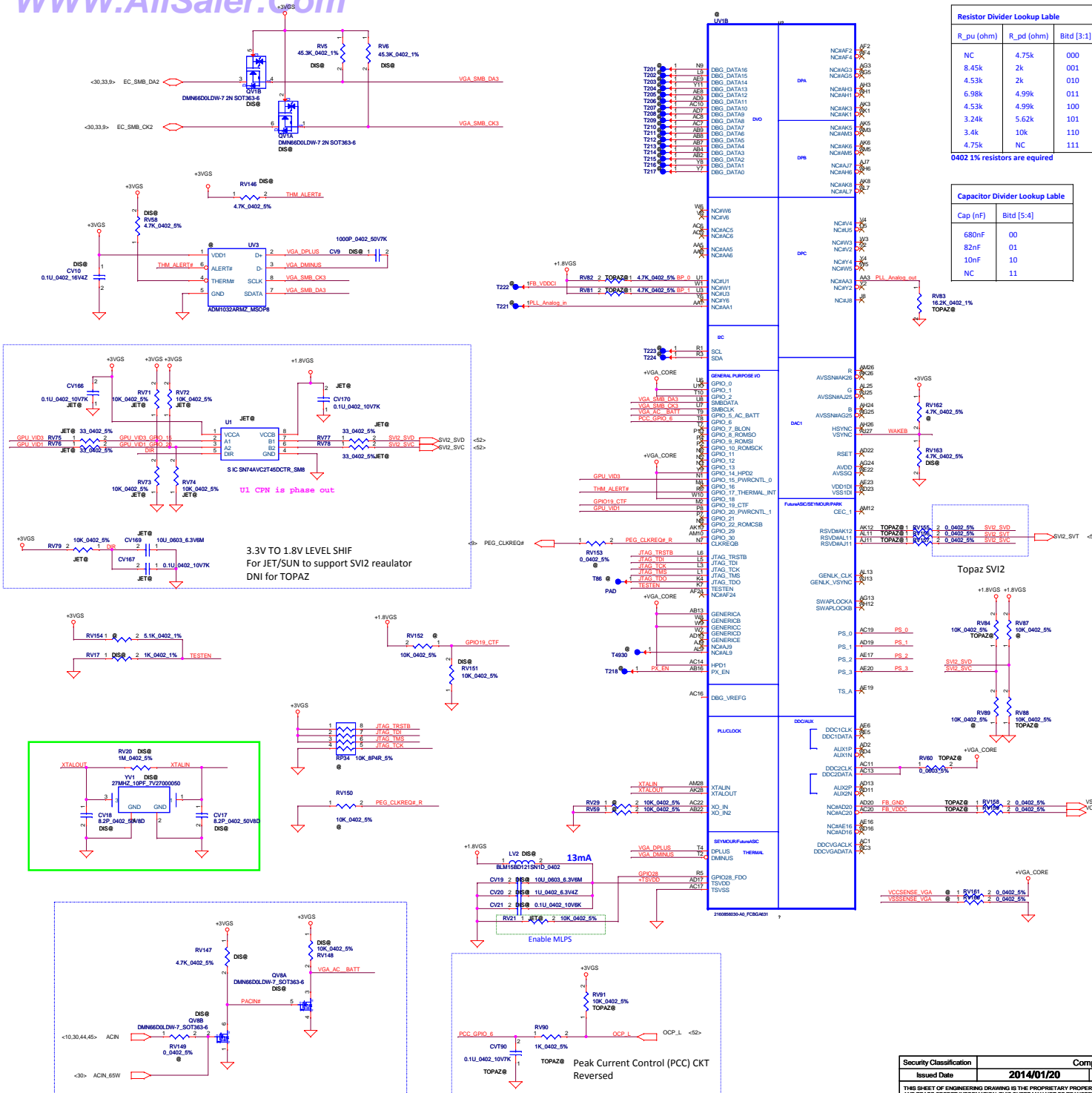


REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"

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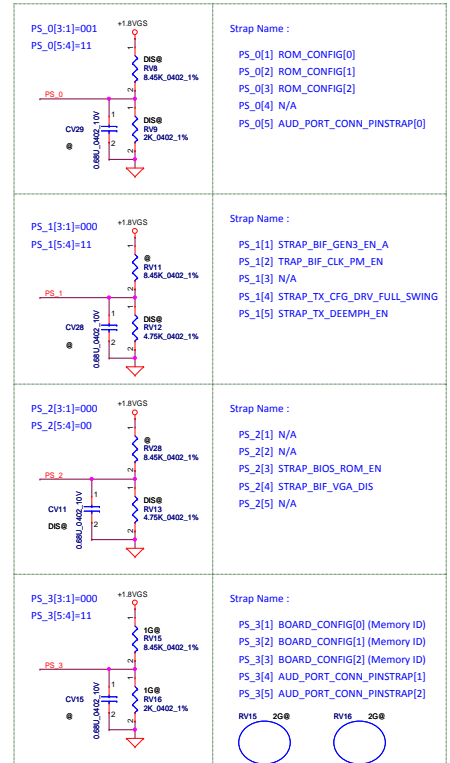
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Issued Date	2014/01/20	Deciphered Date	2015/01/19	Size	Custom
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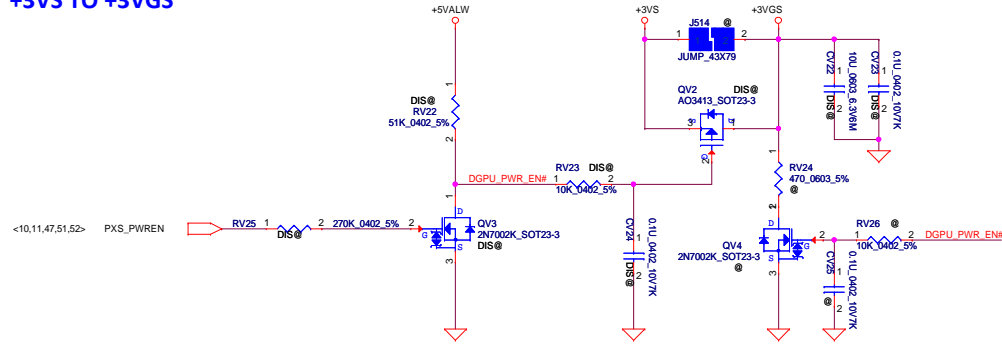
Resistor Divider Lookup Table			
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

0402 1% resistors are required

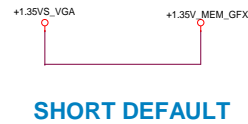
Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



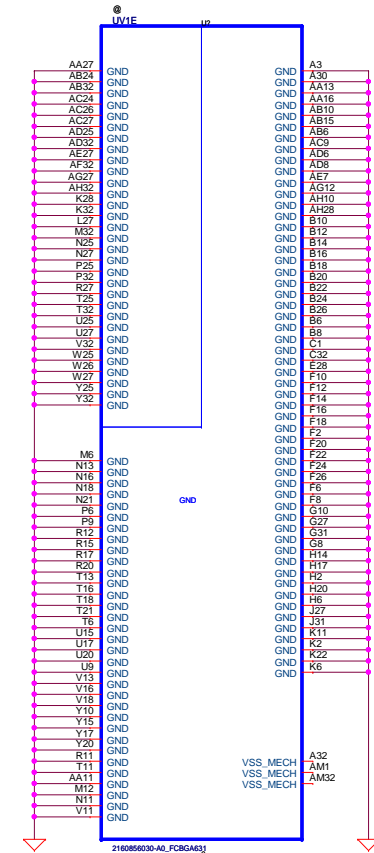
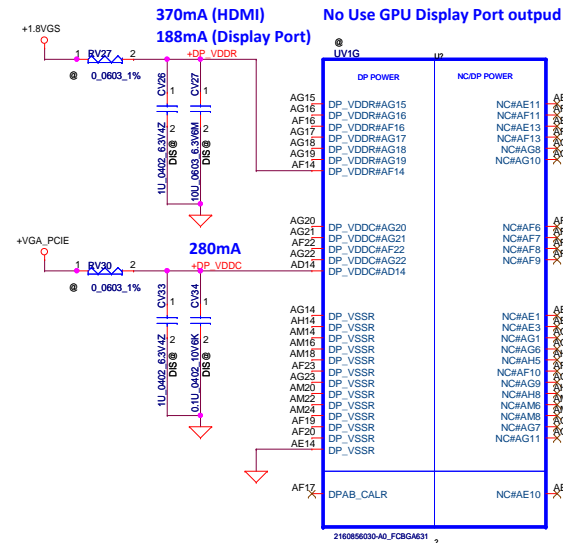
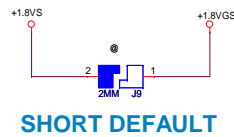
Memory ID	P/N	Vendor	Configuration	Size
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001	SA00006H40L	HYNIX	H5TC2G63FFR-11C	1GB
010	SA00006750L	Micron	MT41J128M16/T-093G	1GB
011	SA000076POL	SAMSUNG	K4W4G1646B-HC11	2GB
(default) 100	SA00006E80L	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077K0L	Micron	MT41J256M16HA-093G	2GB



## +1.35VS\_VGA TO +1.35V\_MEM\_GFX

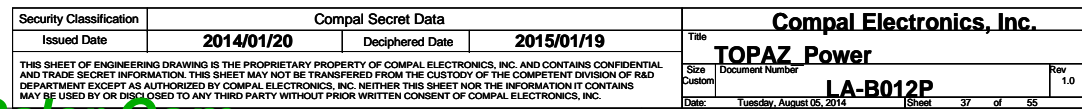


## +1.8VS TO +1.8VGS

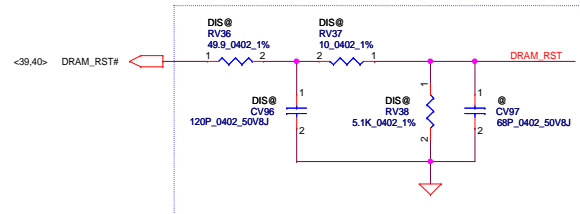
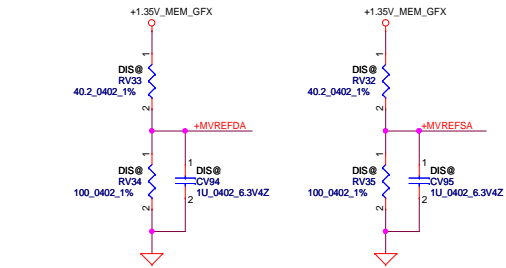


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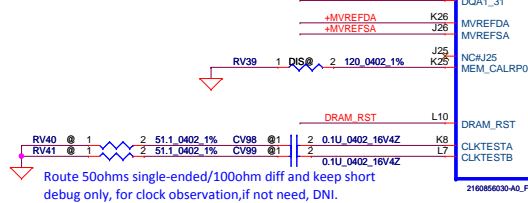
+3VGS	10uF	1uF	0.1uF
VDDR3 25mA	0	2 (1@)	1



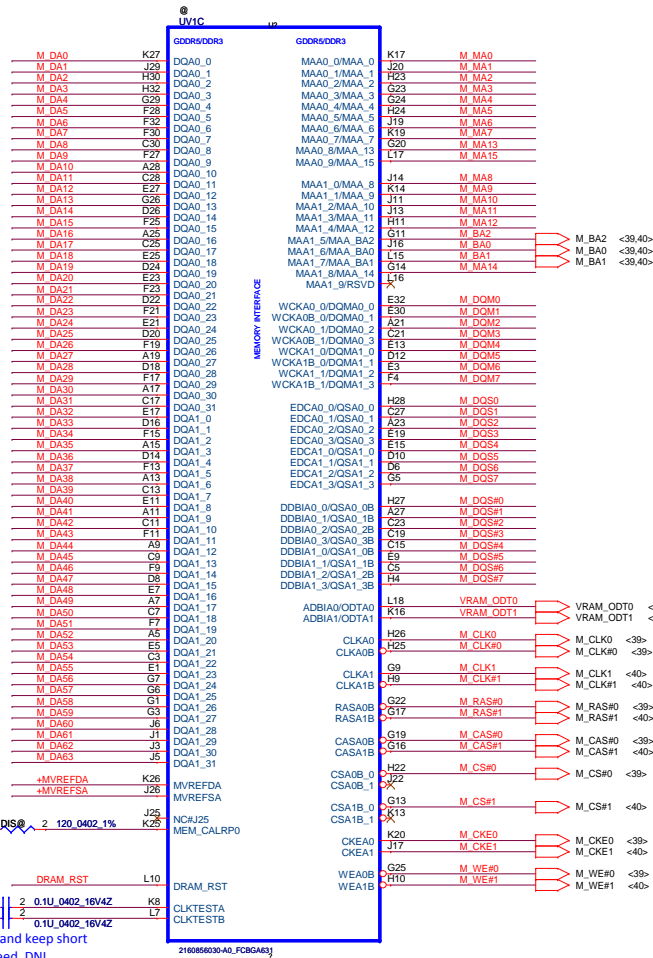
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<39,40> M\_MA[15..0] M\_MA[15..0]  
<39,40> M\_DM[7..0] M\_DM[7..0]  
<39,40> M\_DS[7..0] M\_DS[7..0]  
<39,40> M\_DS#7..0 M\_DS#7..0



Place close to GPU (within 25mm)  
and place component close to each other

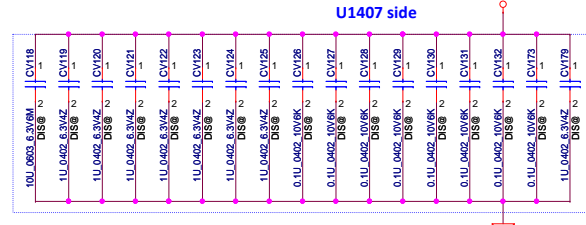
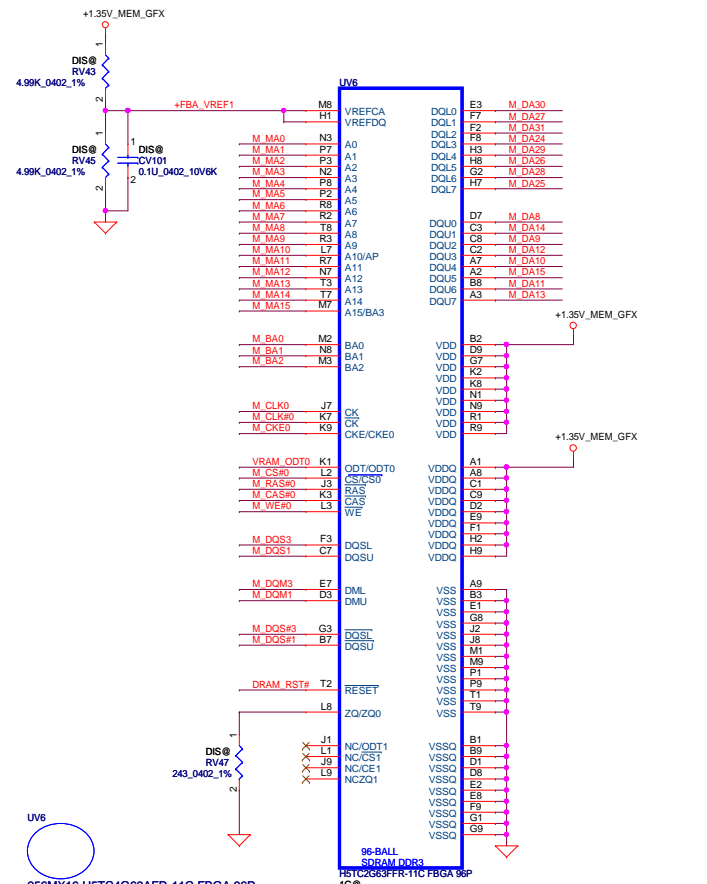
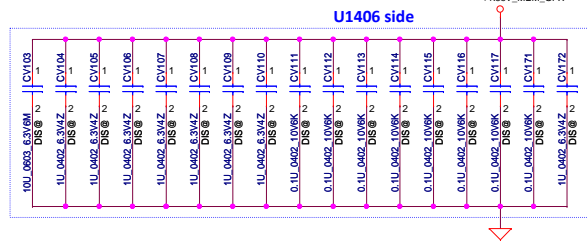
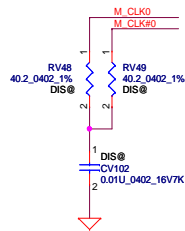
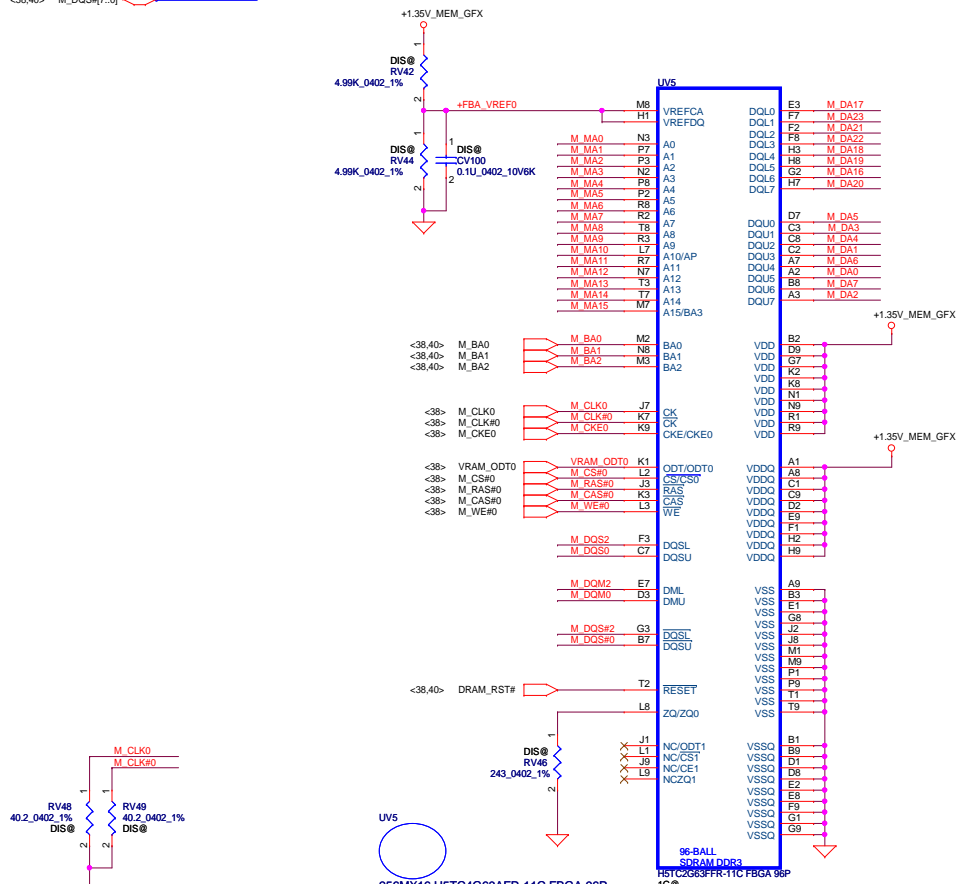


Route 50ohms single-ended/100ohm diff and keep short  
debug only, for clock observation, if not need, DNI.

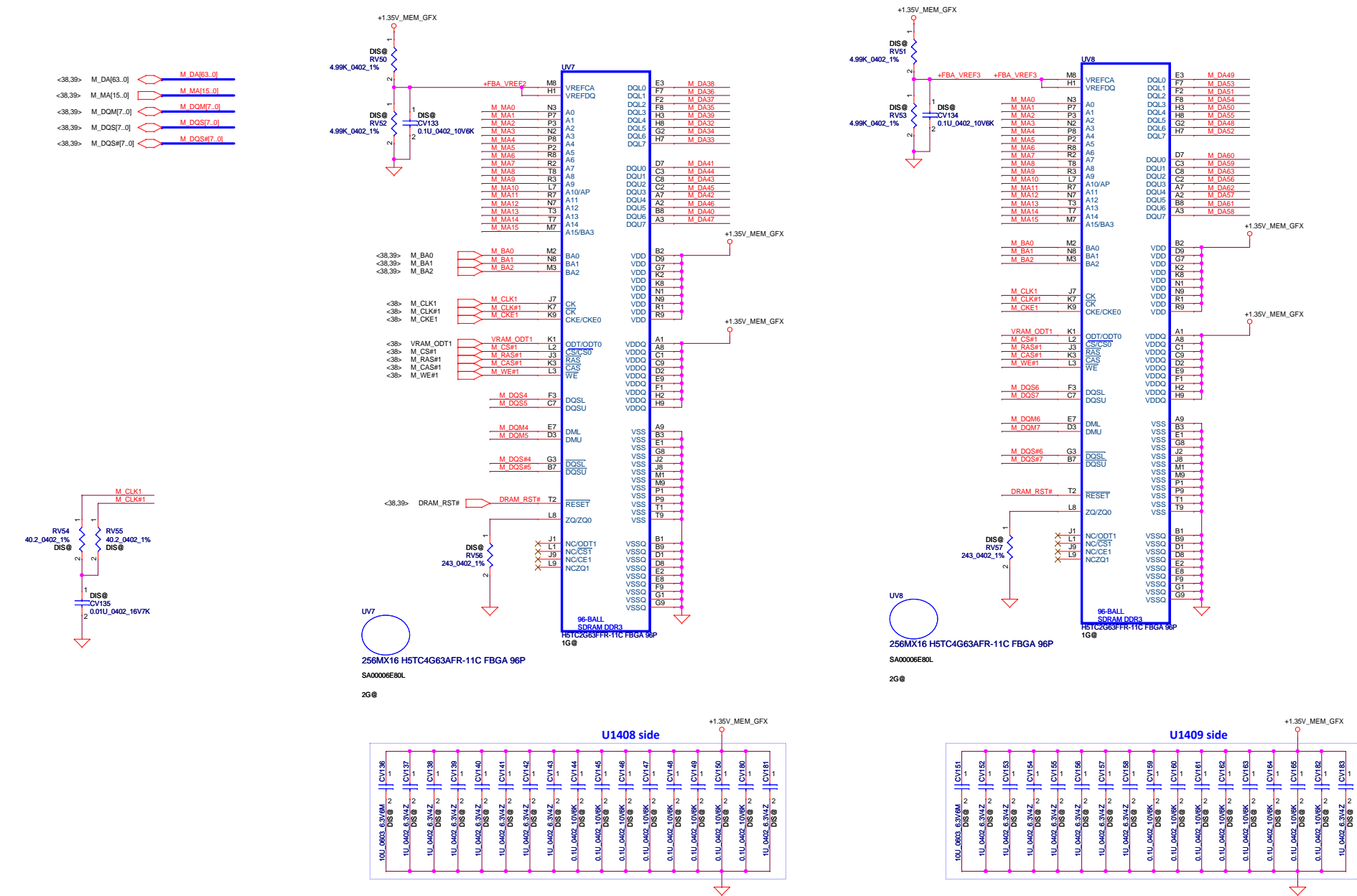


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<38,40> M\_DA[63..0] M\_DA[63..0]  
 <38,40> M\_MA[15..0] M\_MA[15..0]  
 <38,40> M\_DQM[7..0] M\_DQM[7..0]  
 <38,40> M\_DQS[7..0] M\_DQS[7..0]  
 <38,40> M\_DQS#[7..0] M\_DQS#[7..0]



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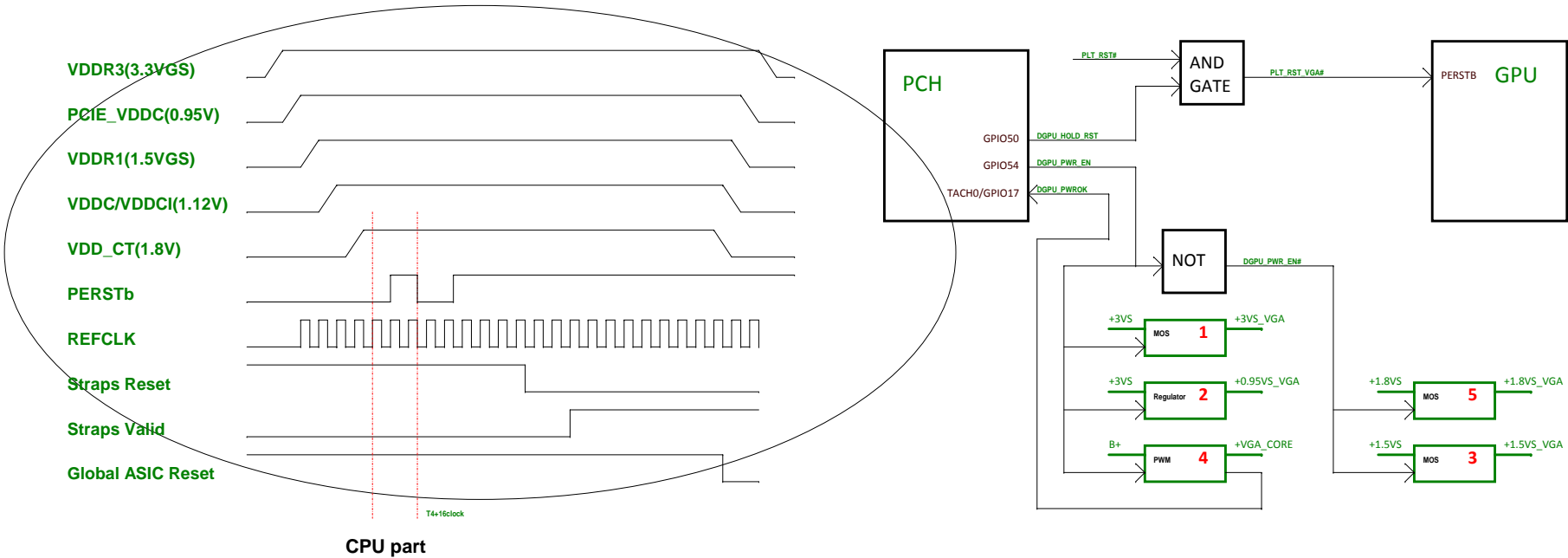


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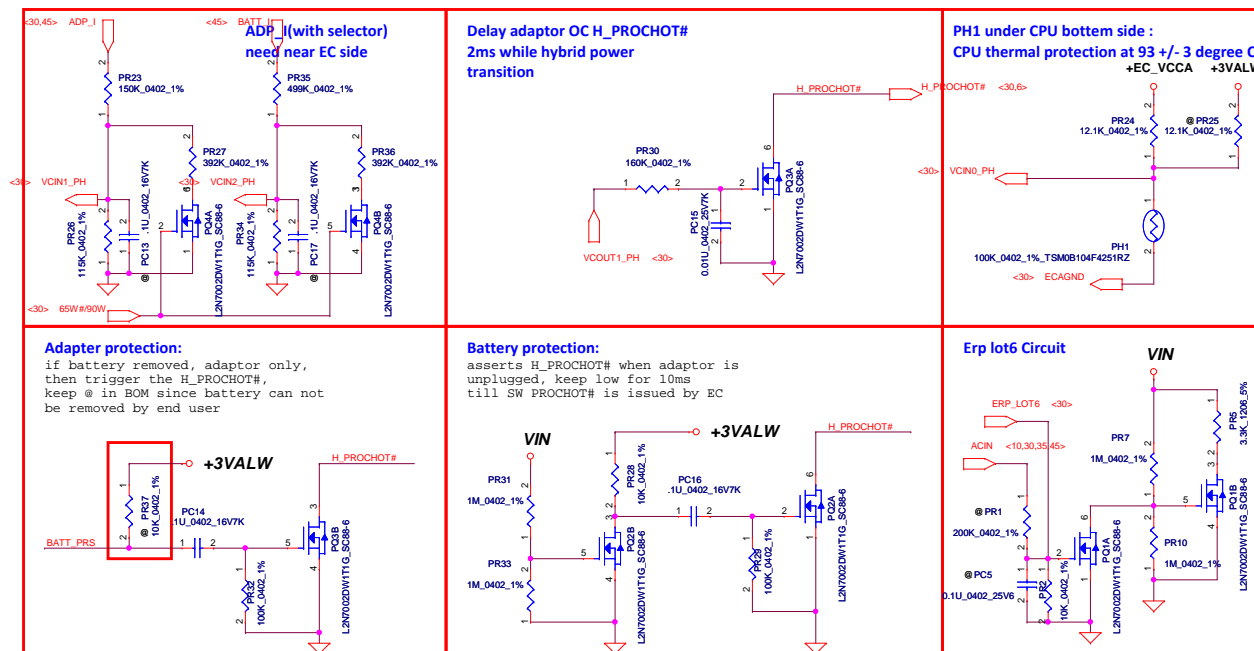
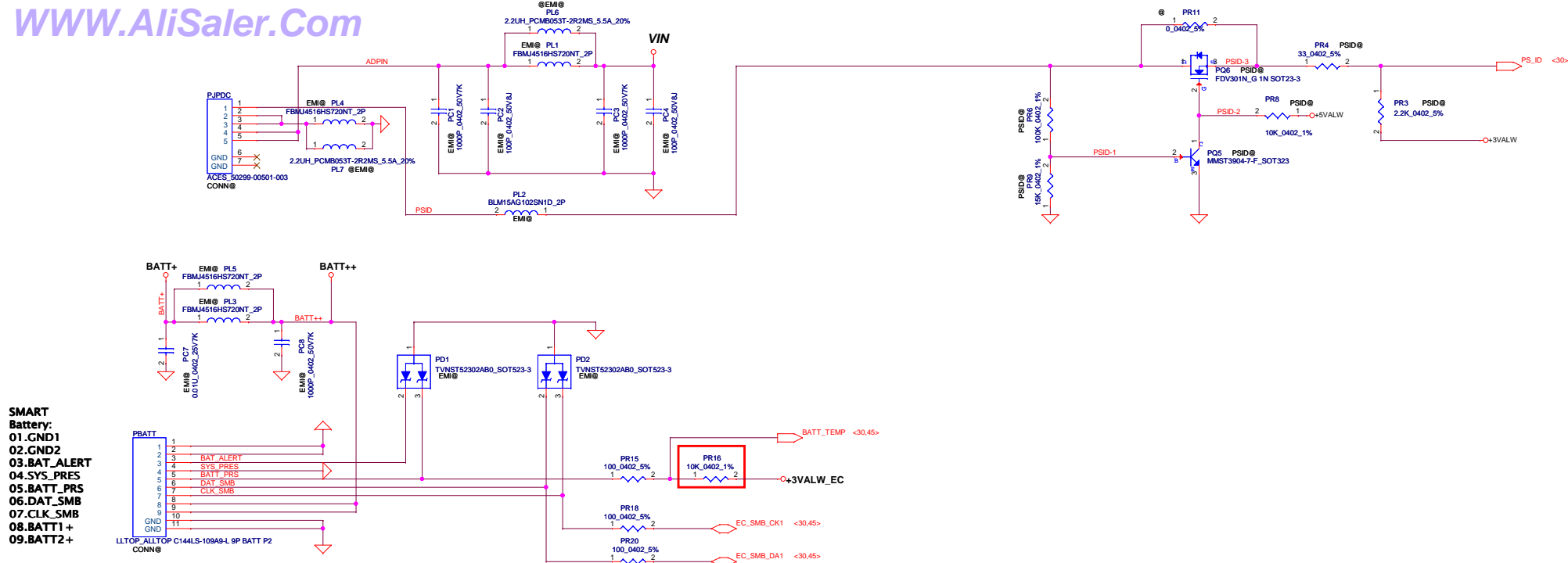
Power-Up/Down Sequence

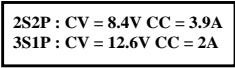
- 1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.
- 2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- 3. VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- 4. For power down, reversing the ramp-up sequence is recommended.



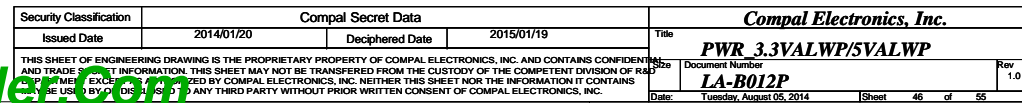
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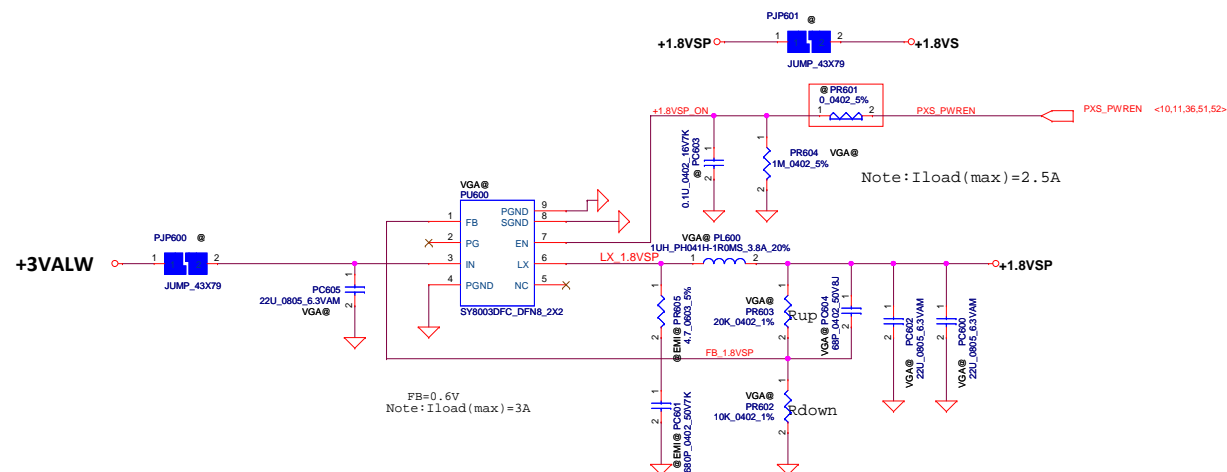
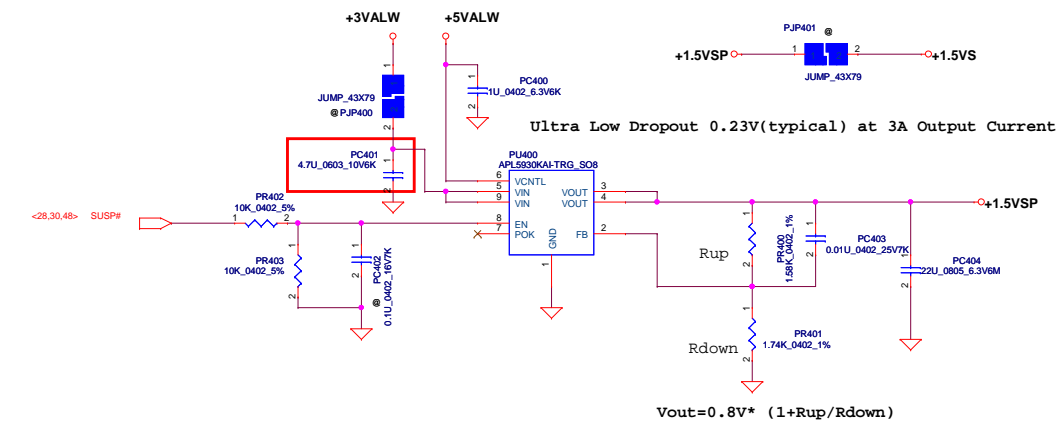
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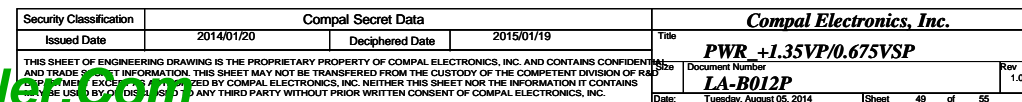
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						Document Number
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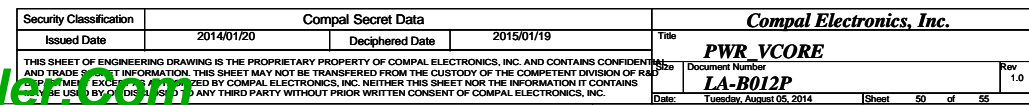




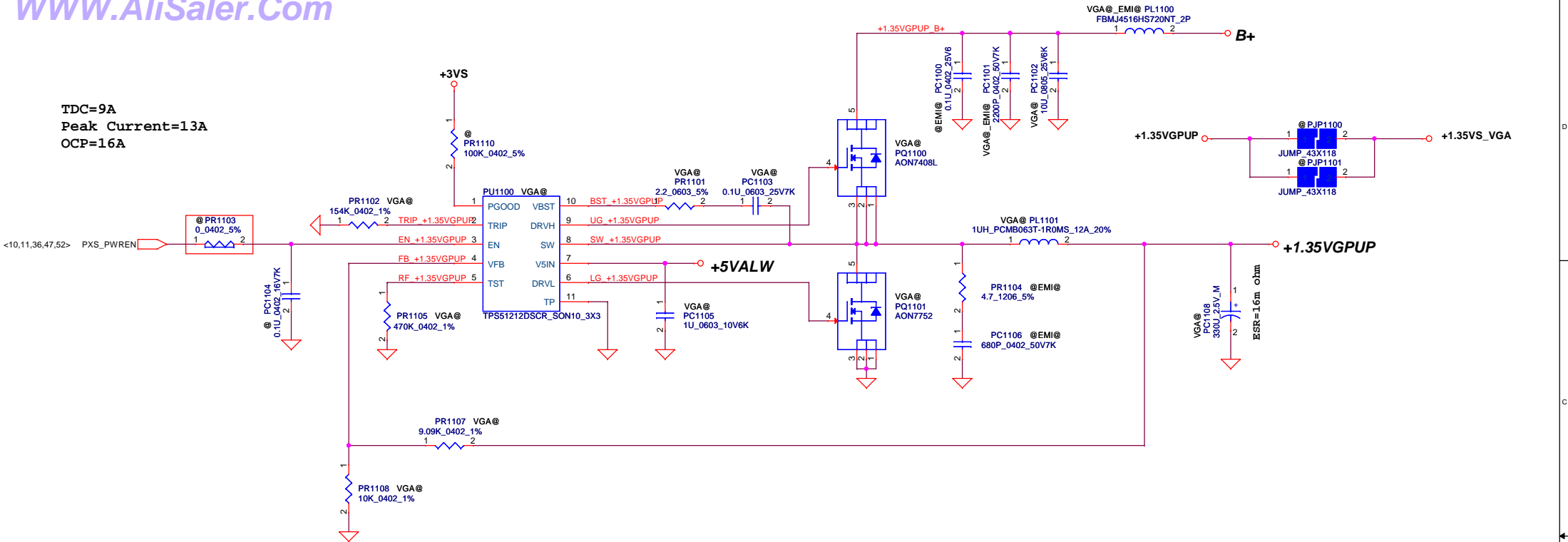




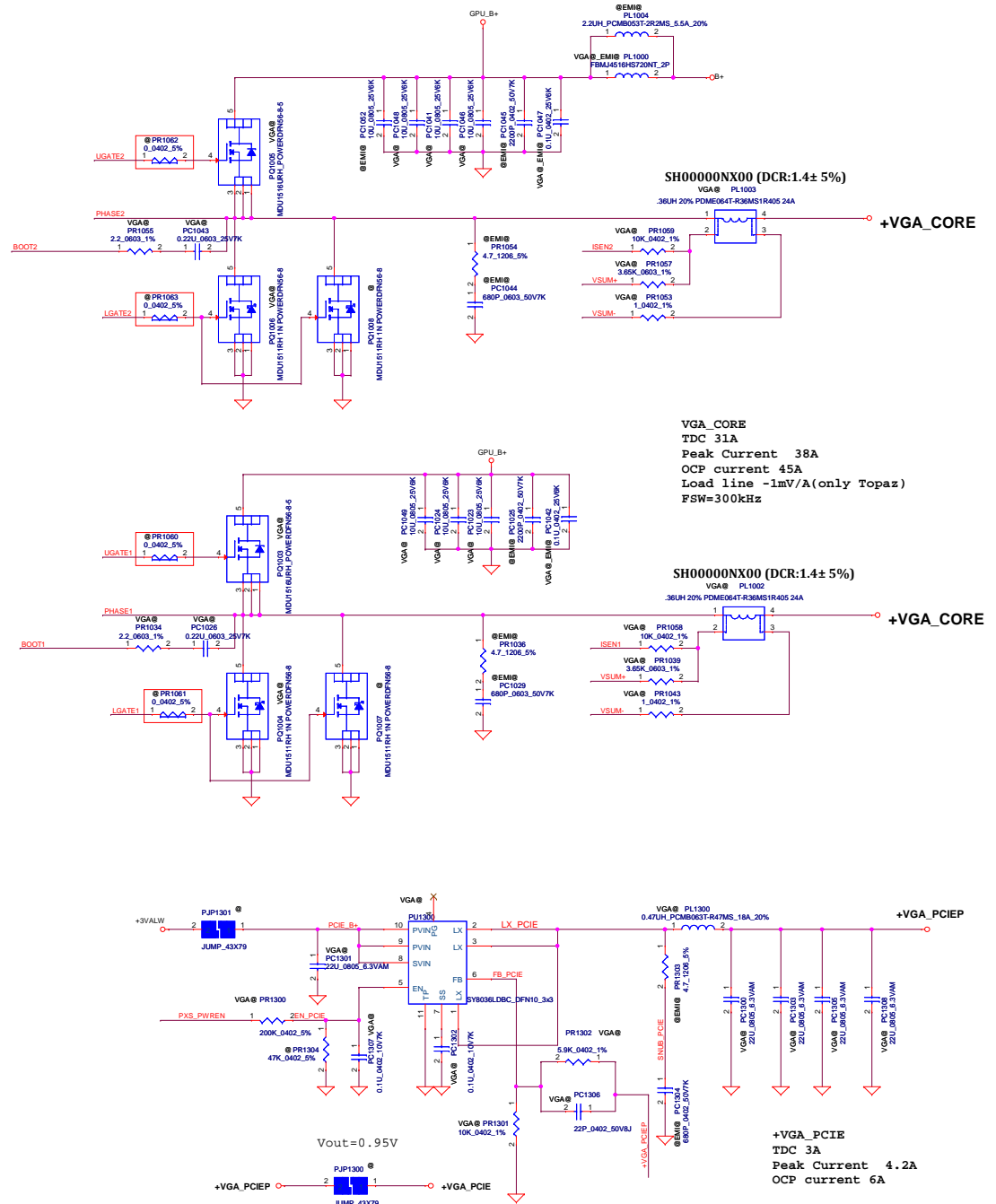
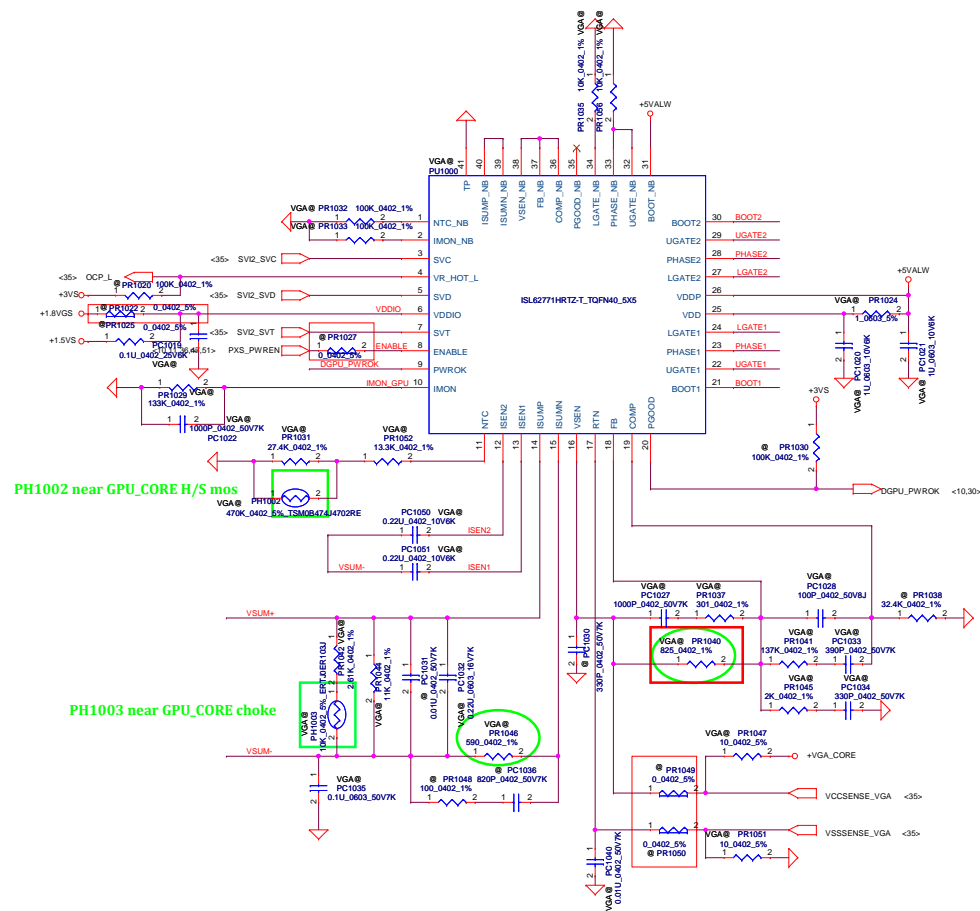


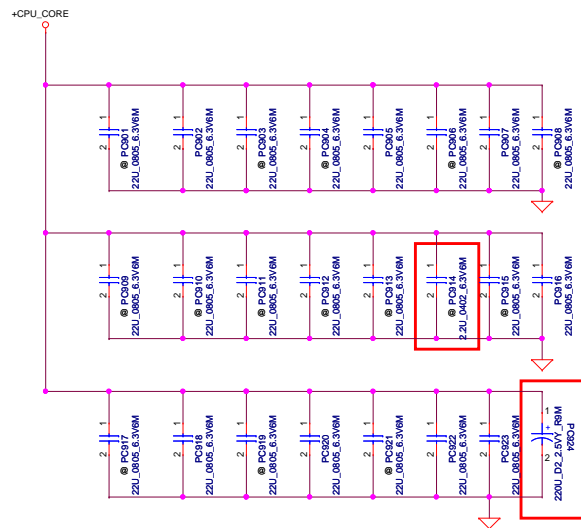


TDC=9A  
Peak Current=13A  
OCP=16A

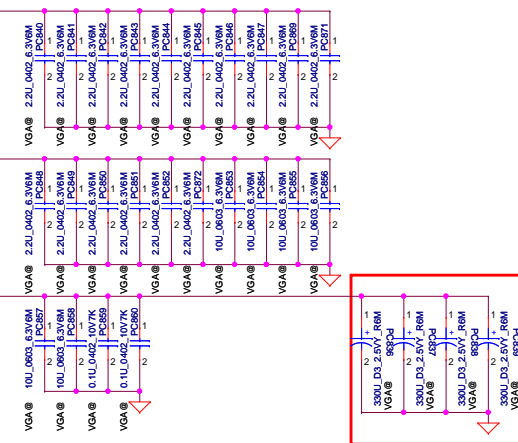


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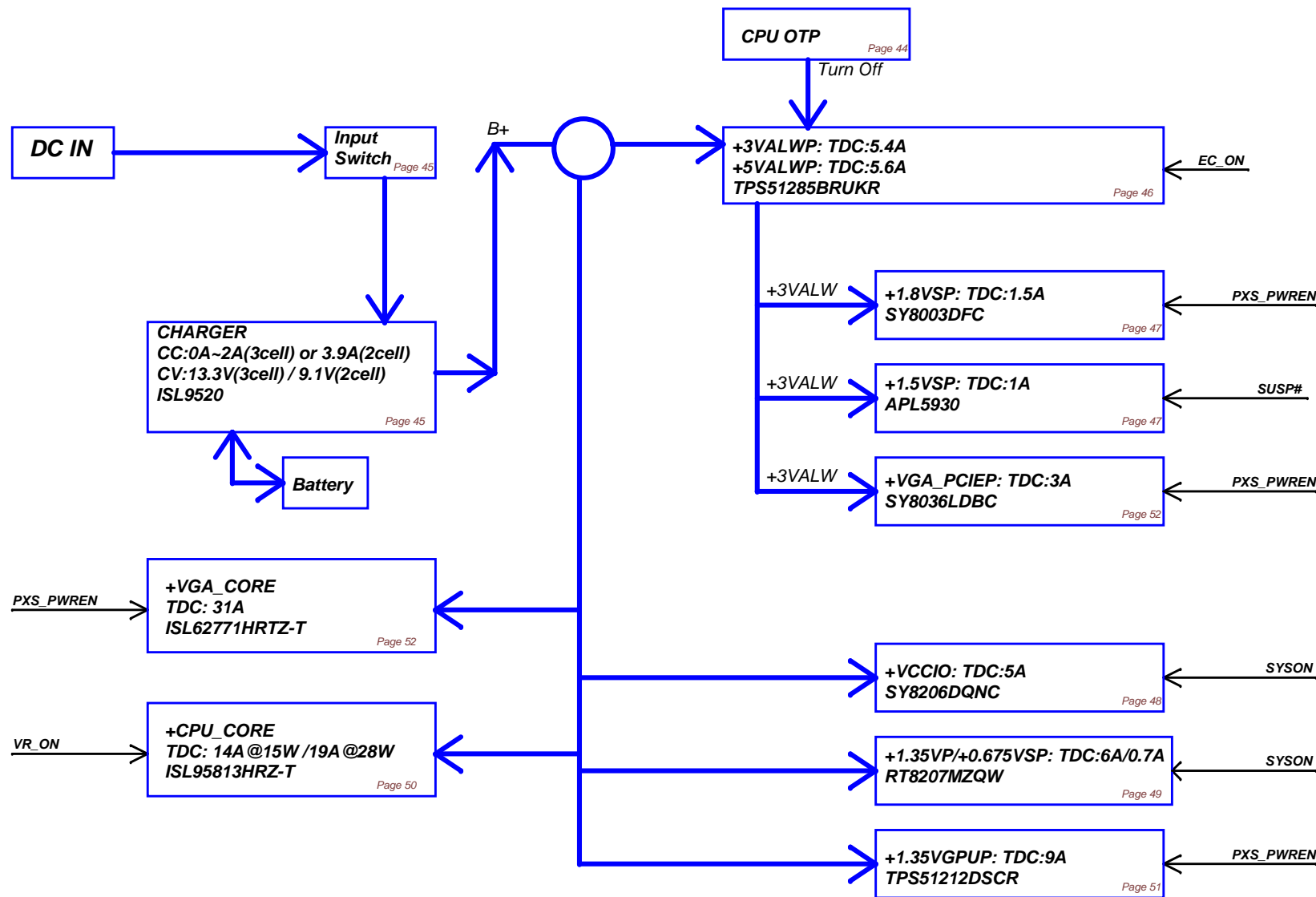


+VGA\_CORE



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# Power block



Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF0000005100 to SF0000004M00 change PL502 from SH000000NM00 to SH000000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0