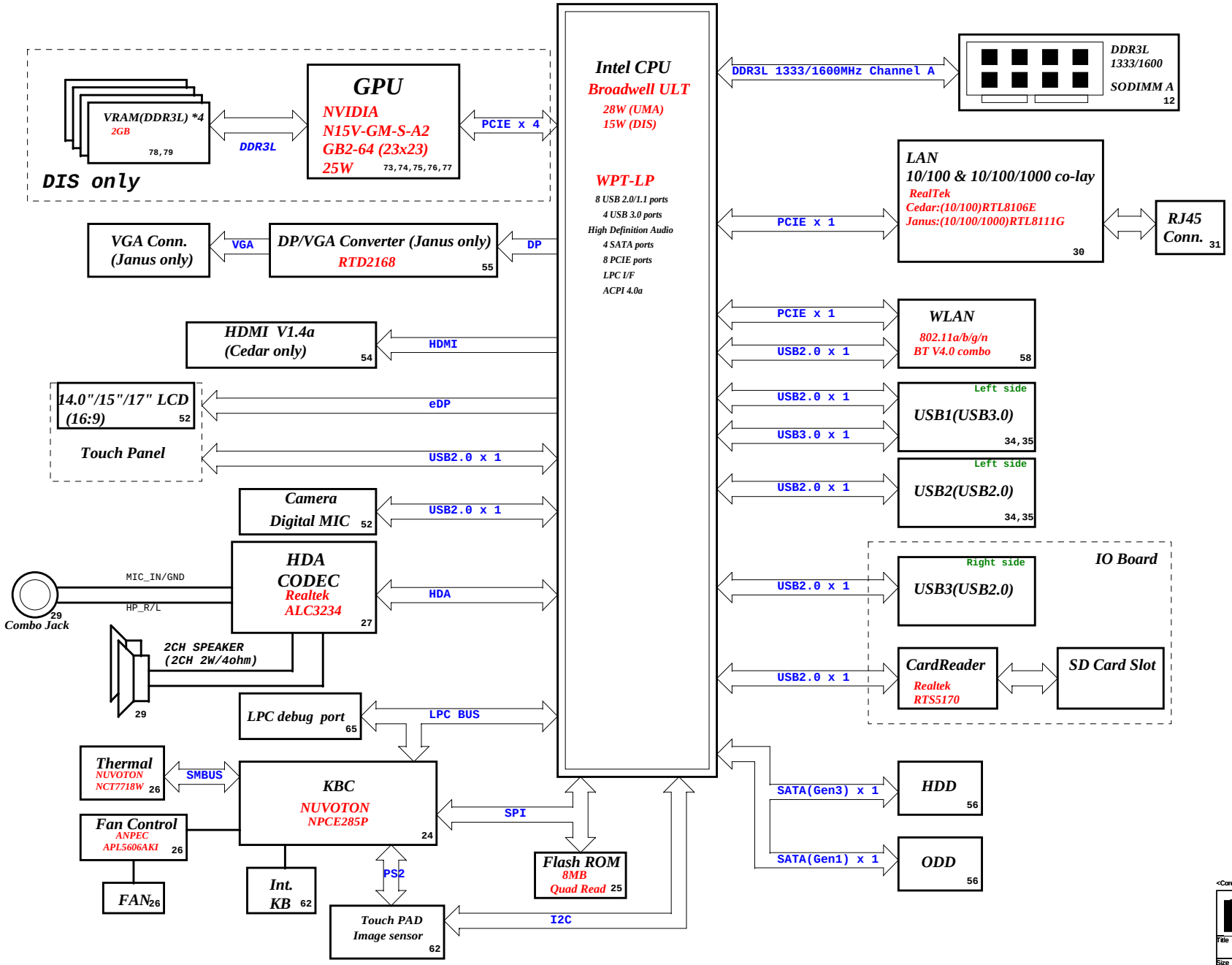
Project code:4PD00I010001
PCB P/N: 13269-1
Revision: X02

Cedar/Janus Block Diagram



CHARGER	
HPA02224RGRR-1-GP	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	
ISL95813HRZ-GP	46,47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU 1.05V	
RT8237CZQW-2-GP	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU 1D5V_S0	
TLV70215DBVR-GP	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

Switches	36 83
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D05V_S0	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
C	Janus HSW 40/50/70	X02

Date: Friday, February 07, 2014 Sheet 2 of 104

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Janus HSW 40/50/70*	*A00*

Date: Friday, February 07, 2014 Sheet 3 of 104

SSID = CPU

1D05S_VCCST

RN401
XDP_TMS 1 8
XDP_TDI 2 7
3 DY 6
XDP_TDO 4 5
SRN51J-1-GP

XDP_TRST# R402 1 DY 2 51R2J-2-GP
XDP_TCLK R406 1 1 51R2J-2-GP

1D05S_VCCST

Remove TP401 for TP604 spacing.

R401
62R2J-GP

Layout Note:
Impedance control:50 ohm

[24,42,44,46] H_PROHOT#

TP402
H_PECI
H_CATERR#
H_PROCHOT# R
R403
56R2J-4-GP

TP403
DY
R411
0R2J-2-GP
[36] H_THERMTRIP_EN

Layout Note: Close to CPU

H_CPUPWRGD
R405
10KR2J-3-GP

SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
SM_DRAMRST#
DDR_PG_CTRL
[12] DDR_PG_CTRL

CPU1B HSW_ULT_DDR3L 2 OF 19

PROC_DETECT#	D61	MISC
CATERR#	K62	
PECI	N62	
PROCHOT#	K63	THERMAL
PROCPWRGD	C61	PWR
SM_RCOMP0	AU60	DDR3L
SM_RCOMP1	AV60	
SM_RCOMP2	AU61	
SM_DRAMRST#	AV15	
SM_PG_CNTL1	AV61	

JTAG

PRDY#	J62	XDP_PRDY# [96]
PREQ#	K62	XDP_PREQ# [96]
PROC_TCK	E60	XDP_TCLK [96]
PROC_TMS	E61	XDP_TMS [96]
PROC_TRST#	E59	XDP_TRST# [96]
PROC_TDI	F63	XDP_TDI [96]
PROC_TDO	F62	XDP_TDO [96]

BPM#0	J60	XDP_BPM0
BPM#1	H60	XDP_BPM1
BPM#2	H61	XDP_BPM2
BPM#3	H62	XDP_BPM3
BPM#4	K59	XDP_BPM4
BPM#5	H63	XDP_BPM5
BPM#6	K60	XDP_BPM6
BPM#7	J61	XDP_BPM7

XDP_BPM[7:0] XDP_BPM[7:0] [96]

HASWELL-6-GP-U

71.HASWE.G0U

R407 1 2 200R2F-L-GP SM_RCOMP_0
R408 1 121R2F-GP SM_RCOMP_1
R409 1 2 100R2F-L1-GP-U SM_RCOMP_2

Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

1D35V_S3
R410
470R2J-2-GP
SM_DRAMRST# 1 R404 2 DDR3_DRAMRST# [12]
0R0402-PAD

Layout Note:
Place close to DIMM

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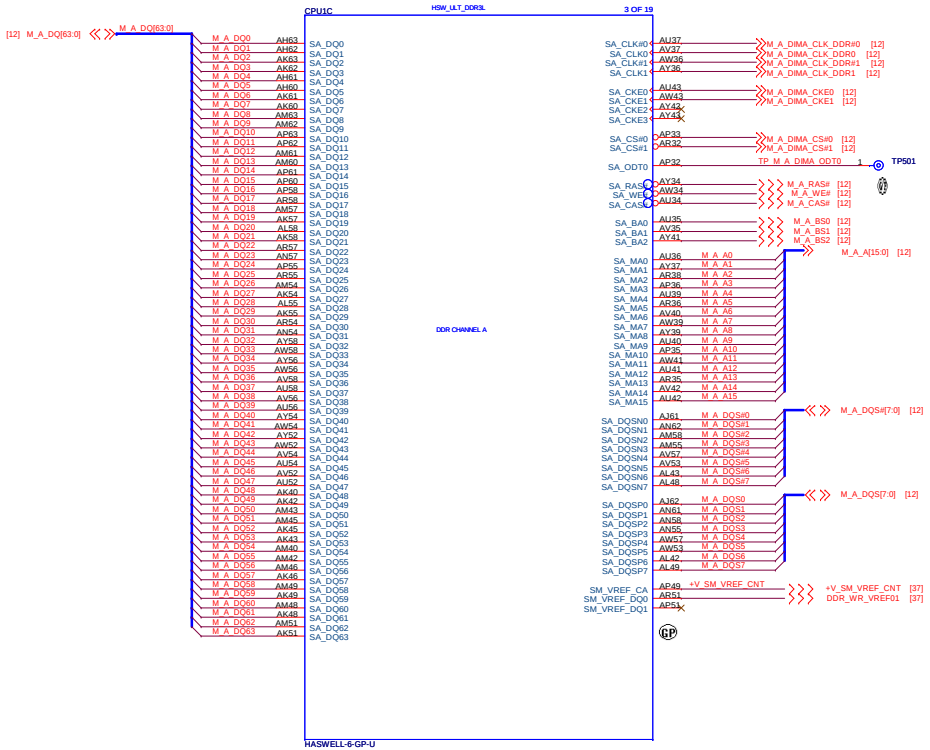
Title: CPU (THERMAL/MISC/PM)

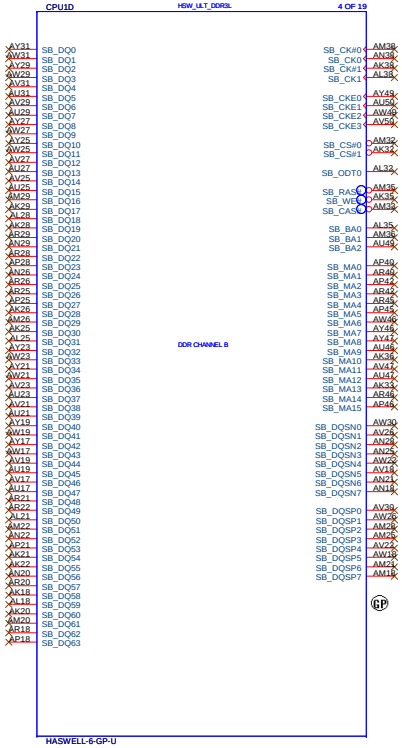
Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 4 of 104

SSID = CPU

DDR3L ball type: Non-Interleaved Type





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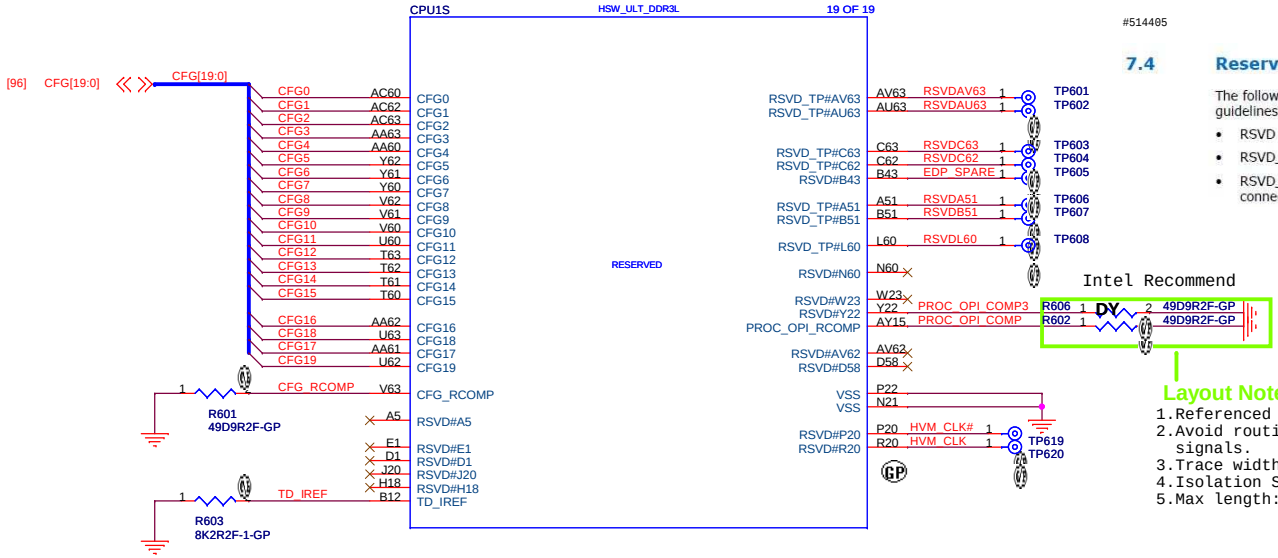
Title: CPU (DDR)

Size	Document Number	Rev
A2	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 5 of 104

SSID = CPU



#514405

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

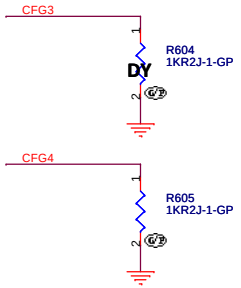
- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 **PCH strap pin:**

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired. • **CFG[2:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[3]: MSR Privacy Bit Feature** – 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting – 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • **CFG[4]: eDP enable** – 1 = Disabled – 0 = Enabled • **CFG[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

<Core Design>

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Title: CPU (CFG)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 6 of 104

SSID = CPU

1D05S_VCCST

R703 1 75R2F-2-GP VR_SVID_ALERT#

R704 1 130R2F-1-GP H_CPU_SVIDDAT

#487822

Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

VCC_CORE — R702 100R2F-L1-GP-U — [46] VCC_SENSE

TP701 TP_VCCIO_OUT — +VCCIOA_OUT

R701 43R2J-GP — H_CPU_SVIDALRT#

[46] VR_SVID_ALERT#
[46] H_CPU_SVIDCLK
[46] H_CPU_SVIDDAT
H_VCCST_PWRGD
[46] H_VR_ENABLE

R710 1 DY 2 10KR2J-3-GP — IMVP_PWRGD_R

[96] PWR_DEBUG — R705 150R2J-L1-GP-U — 1D05S_VCCST

TP702 RSVDP60
TP703 RSVDP61
TP704 RSVDN59
TP705 RSVDN61

3D3V_S5 — C702 SCD1U16Y2KX-3GP DY — 1D05S_VCCST

U701 74LVC1G07GW-GP 73.01G07.0HG
NC#1 VCC / A DY / GND Y

[36,48] 1D05V_VTT_PWRGD

R706 10KR2J-3-GP DY

H_VCCST_PWRGD [96]

EC701 SCD1U16V2KX-3GP DY

R707 100KR2F-L1-GP

R709 47KR2F-GP

Need to fine tune to 1.05V.

1D05V_S0 — R711 0R0603-PAD-1GP-U — 1D05S_VCCST 0.1A

C701 SC22U6D3V5MX-2GP DY

C703 SC1U10V2KX-1GP DY

[24,46] IMVP_PWRGD

R713 100KR2F-L1-GP — IMVP_PWRGD_R

R712 47KR2F-GP

EC702 SCD1U16V2KX-3GP DY

CPU1L — HSW_ULT_DDR3L — 12 OF 19 — HSW ULT POWER — HASWELL-6-GP-U

1D35V_S3: AH26 AJ31 AJ33 AJ37 AN33 AP43 AR48 AY35 AY40 AY44 AY50 VDDQ

VCC_CORE: F59 N58 AC58 E63 AB23 A59 E20 AD23 AA23 AE59 VCC RSVD#N58 RSVD#AC58 VCC_SENSE RSVD#AB23 VCCIO_OUT VCCIOA_OUT RSVD#AD23 RSVD#AA23 RSVD#AE59

L59 J58 RSVD#L59 RSVD#J58

VIDALERT# L62 — VIDSCLK N63 — VIDSOUT L63 — VCCST_PWRGD B59 — VR_EN F60 — VR_READY C59

D63 H59 P62 P60 P61 N59 N61 T59 AD60 AD59 AA59 AE60 AC59 AG58 U59 V59 VSS PWR_DEBUG# VSS RSVD_TP#P60 RSVD_TP#P61 RSVD_TP#N59 RSVD_TP#N61 RSVD#T59 RSVD#AD60 RSVD#AD59 RSVD#AA59 RSVD#AE60 RSVD#AC59 RSVD#AG58 RSVD#U59 RSVD#V59

1D05S_VCCST: AC22 AE22 AE23 VCCST

VCC_CORE: AB57 AD57 AG57 C24 C28 C32 VCC

VCC_CORE: C36 C40 C44 C48 C52 C56 E23 E25 E27 E29 E31 E33 E35 E37 E39 E41 E43 E45 E47 E49 E51 E53 E55 E57 F24 F28 F32 F36 F40 F44 F48 F52 F56 G23 G25 G27 G29 G31 G33 G35 G37 G39 G41 G43 G45 G47 G49 G51 G53 G55 G57 H23 J23 K23 K57 L22 M23 M57 P57 U57 W57 VCC

<Core Design>

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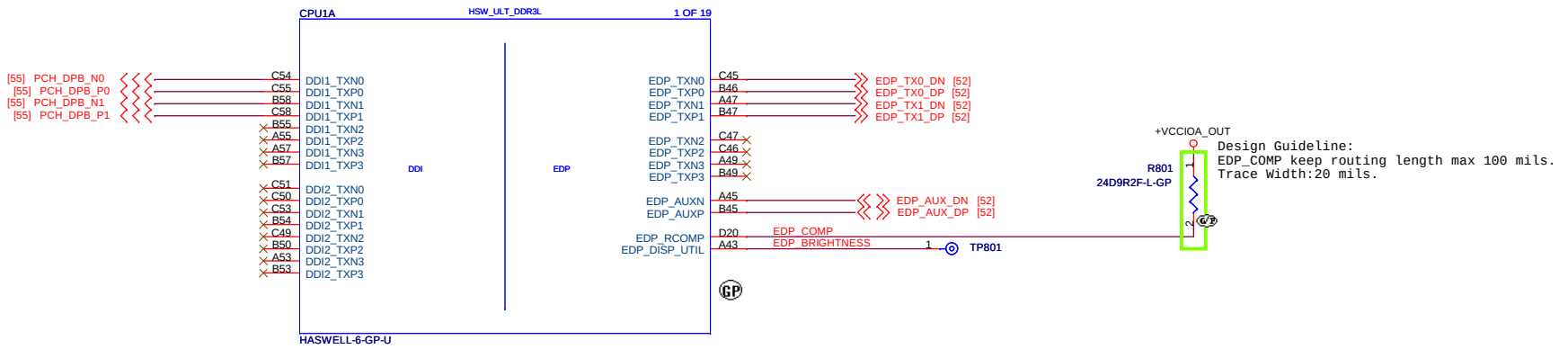
Title: CPU (VCC CORE)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 7 of 104

SSID = CPU

DP to VGA Converter



<Core Design>

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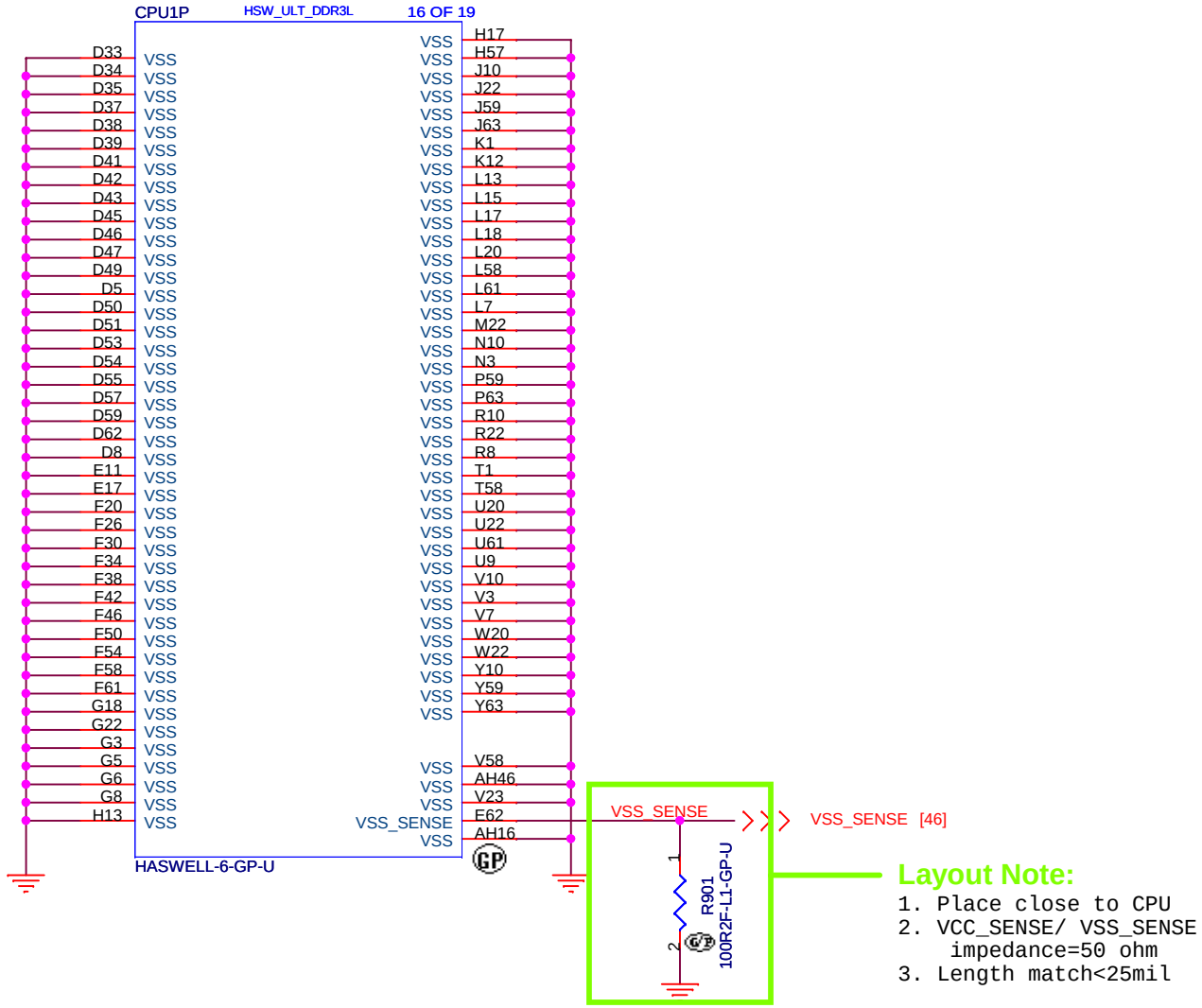
Title: CPU (DDI/EDP)

Size	Document Number	Rev
A3	Janus HSW 40/50/70	X02

Date: Friday, February 07, 2014 Sheet 8 of 104

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title: CPU (VSS)

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

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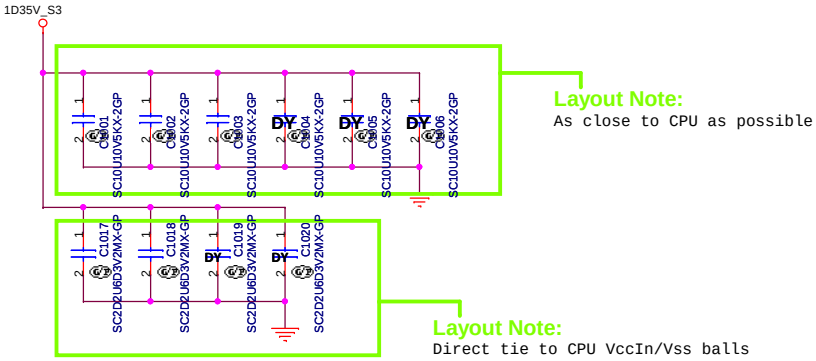
SCD - CPU



<Core Design>

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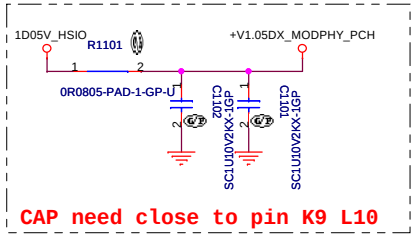
Title: CPU (Power CAP1)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

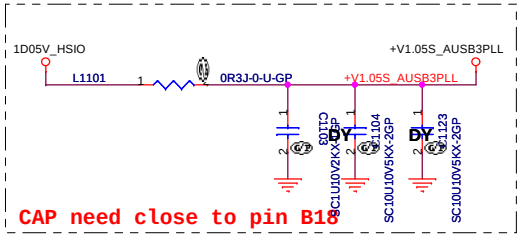
Date: Friday, February 07, 2014 | Sheet 10 of 104

MAX: 1.92A

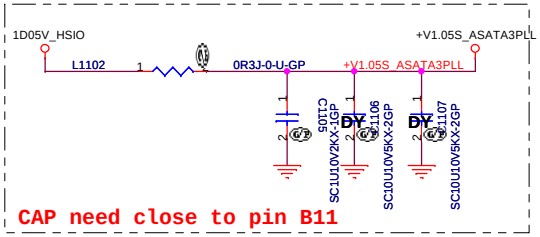
1.838A



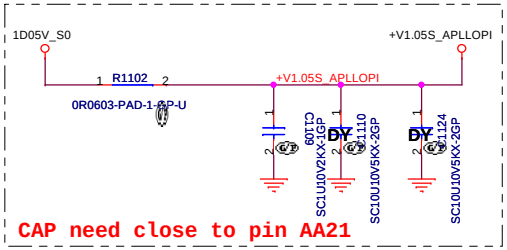
41mA



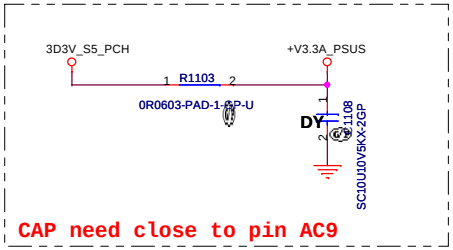
42mA



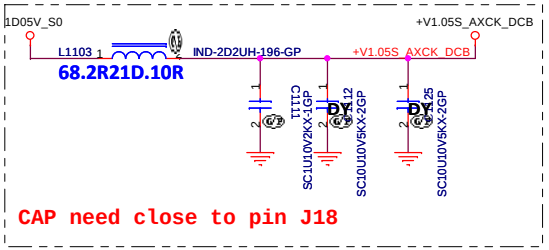
57mA



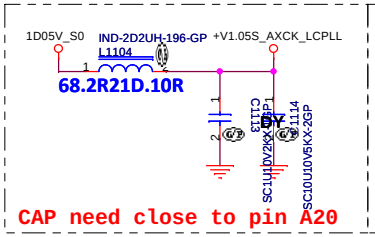
62mA



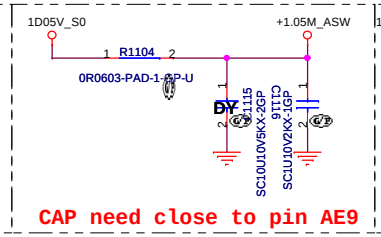
185mA



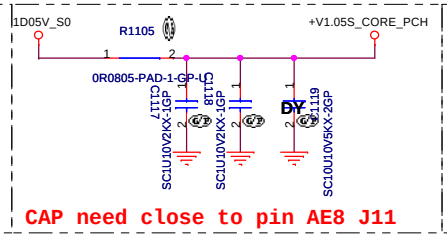
31mA



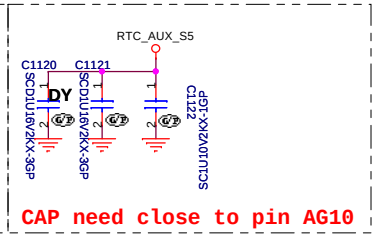
658mA



1.632A



1mA



<Core Design>

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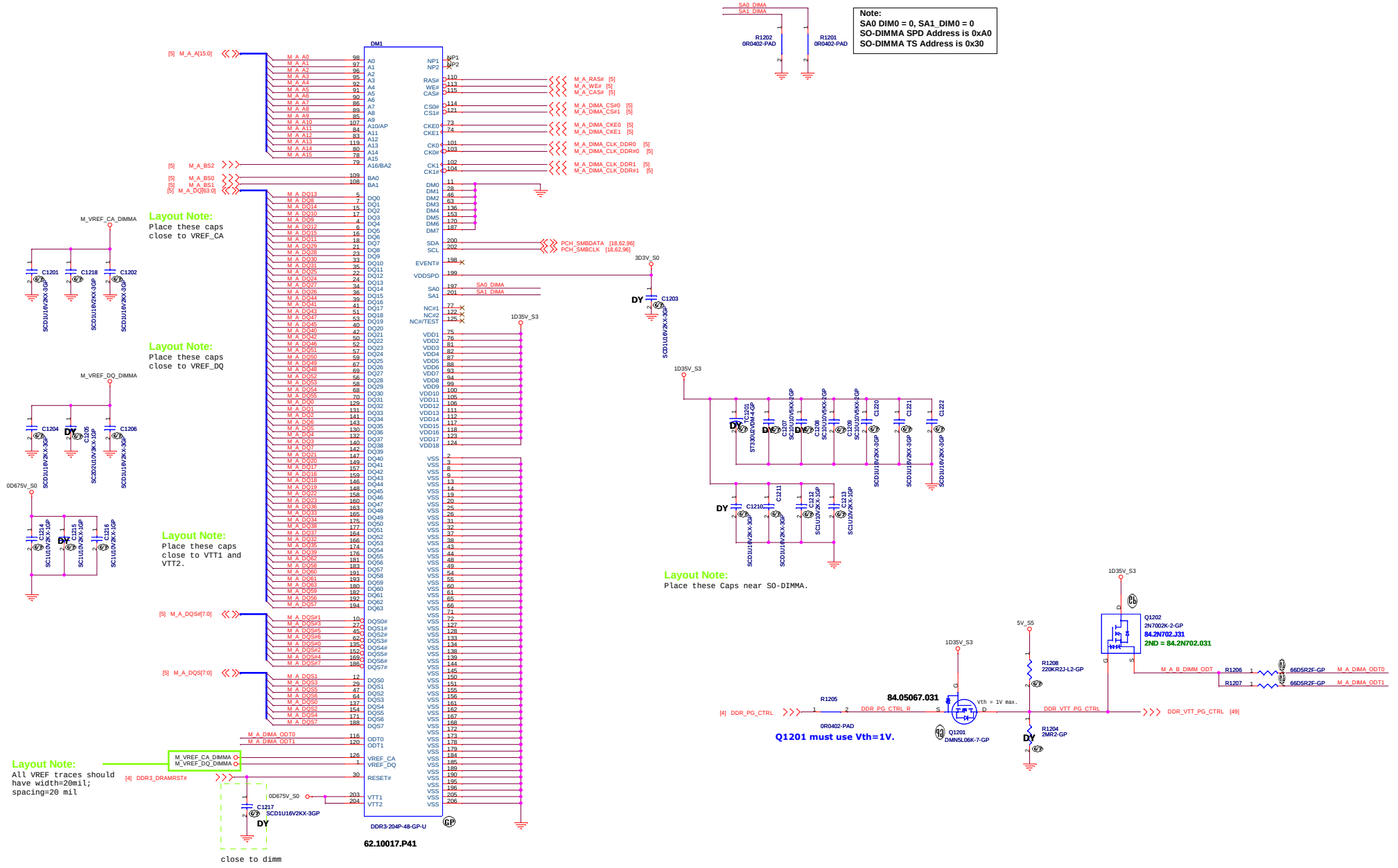
Title: CPU (Power CAP2)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 11 of 104

SSID = MEMORY



<Core Design>

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Title: DDR3-SODIMM1

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 12 of 104

(Blanking)

<Core Design>

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Title: (Reserved)DDR3-SODIMM2		
Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet 13 of 104	

(Blanking)

<Core Design>

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Title: *(Reserved)_SODIMM _SODIMM4*

Size	Document Number	Rev
A4	*Janus HSW 40/50/70*	*A00*

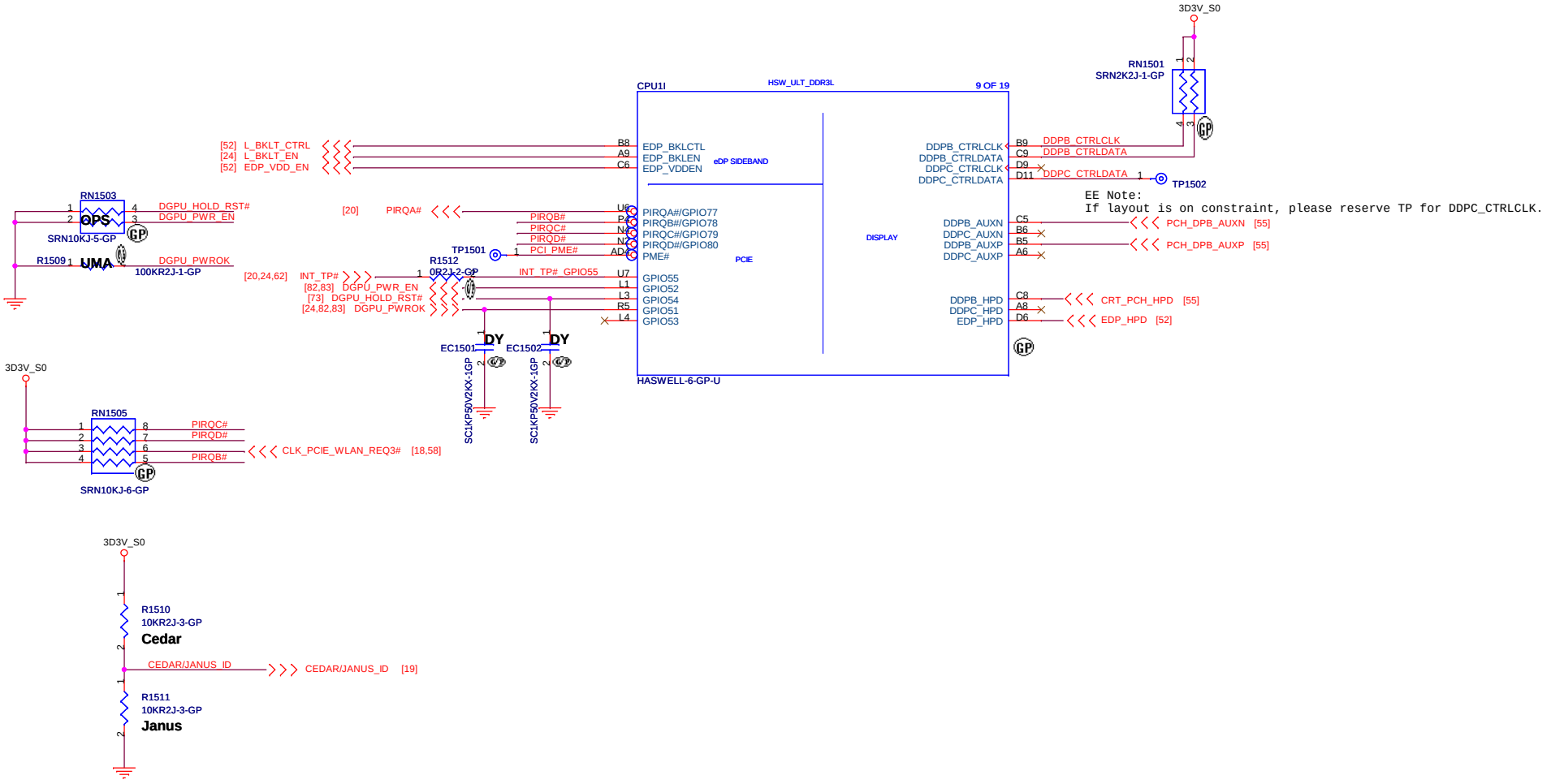
Date: Friday, February 07, 2014 Sheet 14 of 104

SSID = CPU

PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	Low = Disable Port B (default) * High = Enable Port B
DDPC_CTRLDATA	* Low = Disable Port C (default) High = Enable Port C

The internal pull-down is disabled after PLTRST# deasserts



EE Note:
If layout is on constraint, please reserve TP for DDPC_CTRLCLK.

<Core Design>

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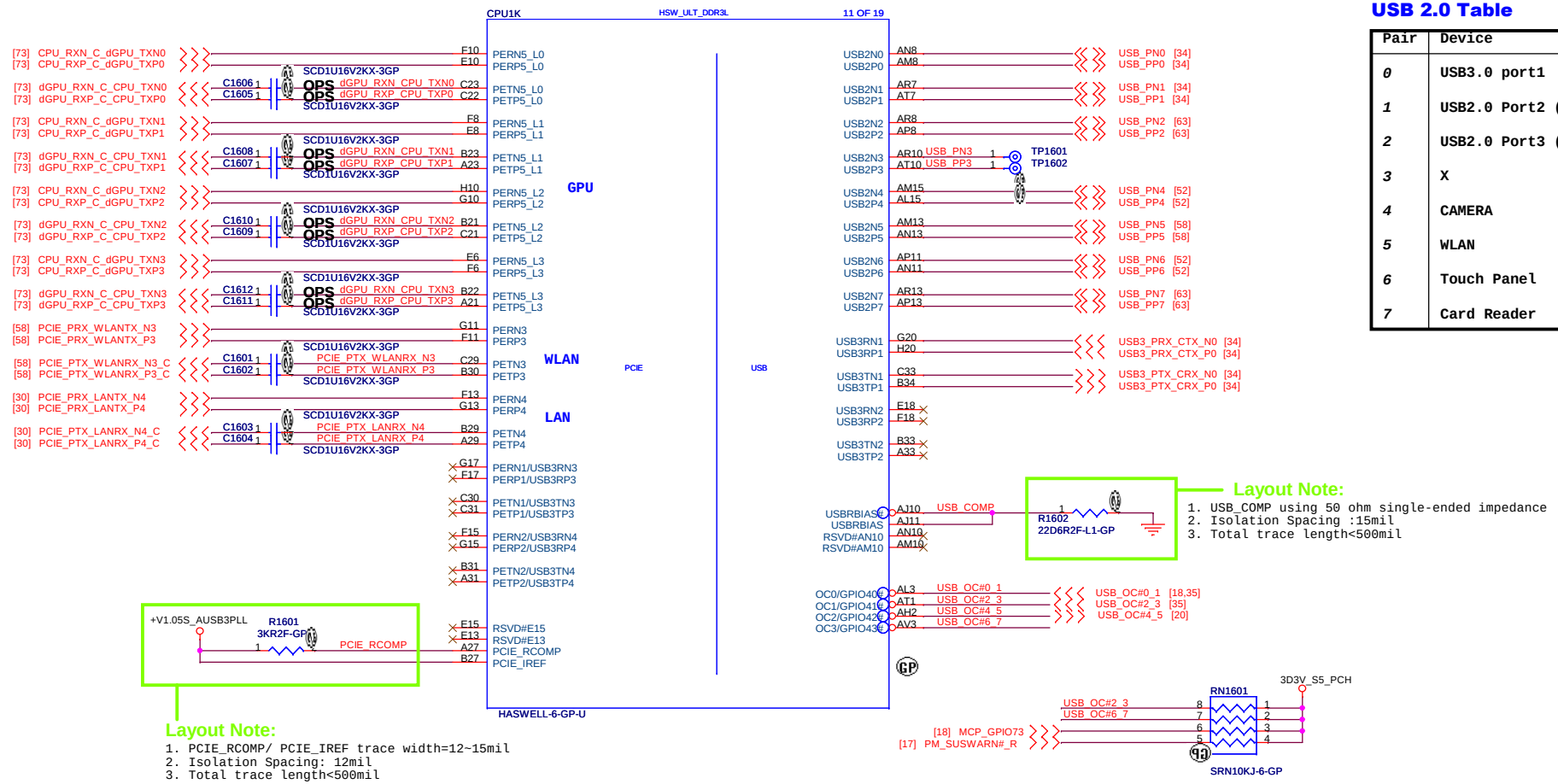
Title	PCH (EDP/GPIO/DDI)	
Size: A3	Document Number: Janus HSW 40/50/70	Rev: X02
Date: Friday, February 07, 2014	Sheet 15 of 104	

SSID = PCH



Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB2.0 Port2 (Debug Port)
2	USB2.0 Port3 (IOBD)
3	X
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0~L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	ODD	SATA1
6(L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3	USB 3.0 Port4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	SATA 6Gb/s Port 3 PCIe* Port 6 Lane 0 SSD	SATA 6Gb/s Port 2 PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1 PCIe* Port 6 Lane 2	SATA 6Gb/s Port 0 PCIe* Port 6 Lane 3
			PCIe* Port 1 SSD	PCIe* Port 2 SSD										
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3	USB 3.0 Port4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD										

<Core Design>

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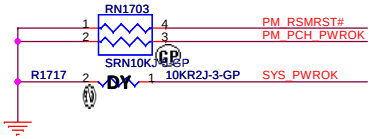
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCIE/USB)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 16 of 104

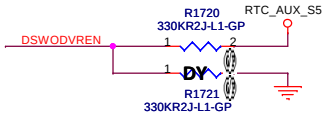
SSID = PCH

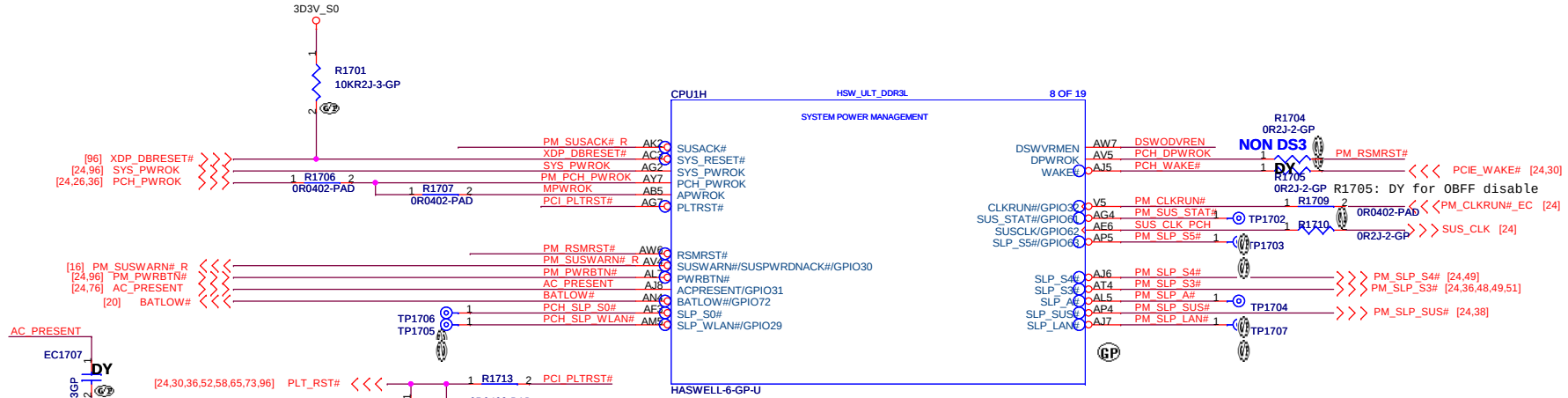


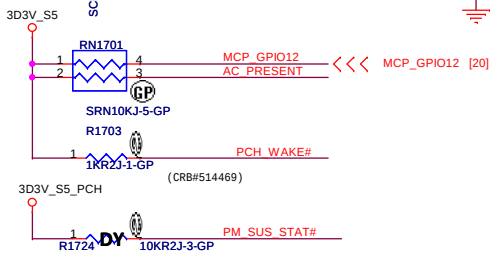
PCH strap pin:

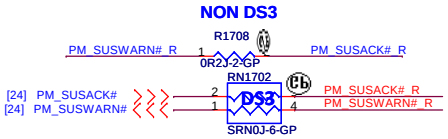
On Die DSW VR Enable	
DSWVRMEN	* Low = Disable High = Enable (default)

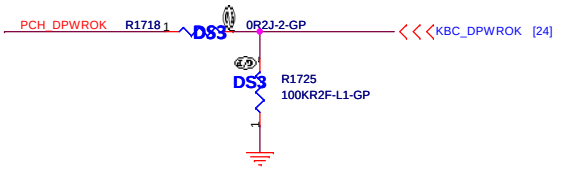
This signal has no integrated pull-up/pull-down.

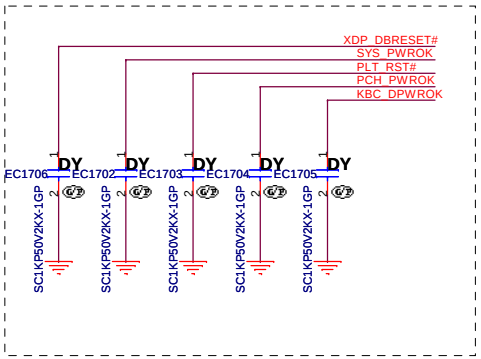


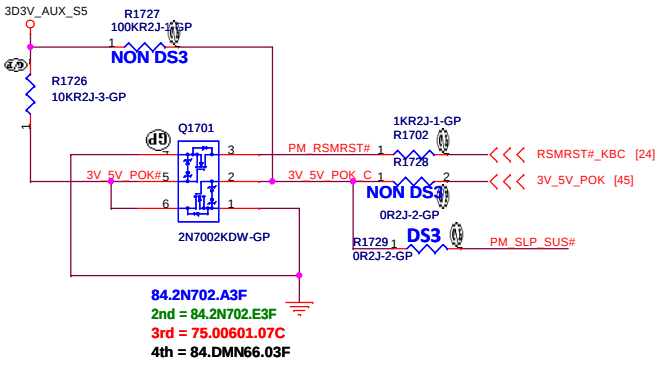


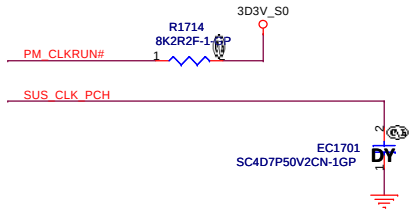












<Core Design>

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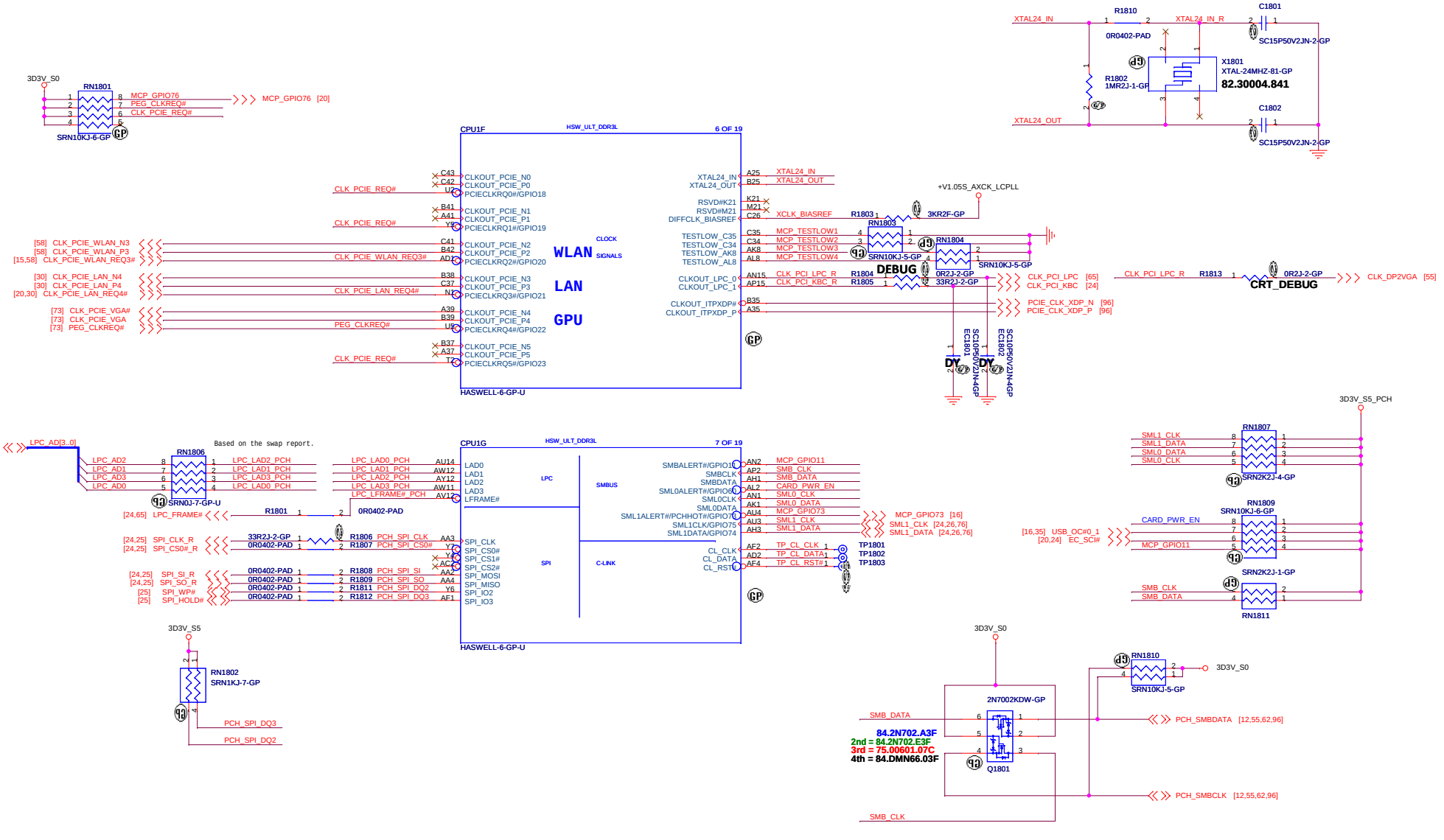
Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (PM)		
Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet 17 of 104	

SSID = PCH



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLOCK/SMBUS/CL/LPC/SPI)

Size	Document Number	Rev
Custom	Janus HSW 40/50/70	X02

Date: Friday, February 07, 2014 Sheet 18 of 104

SSID = CPU

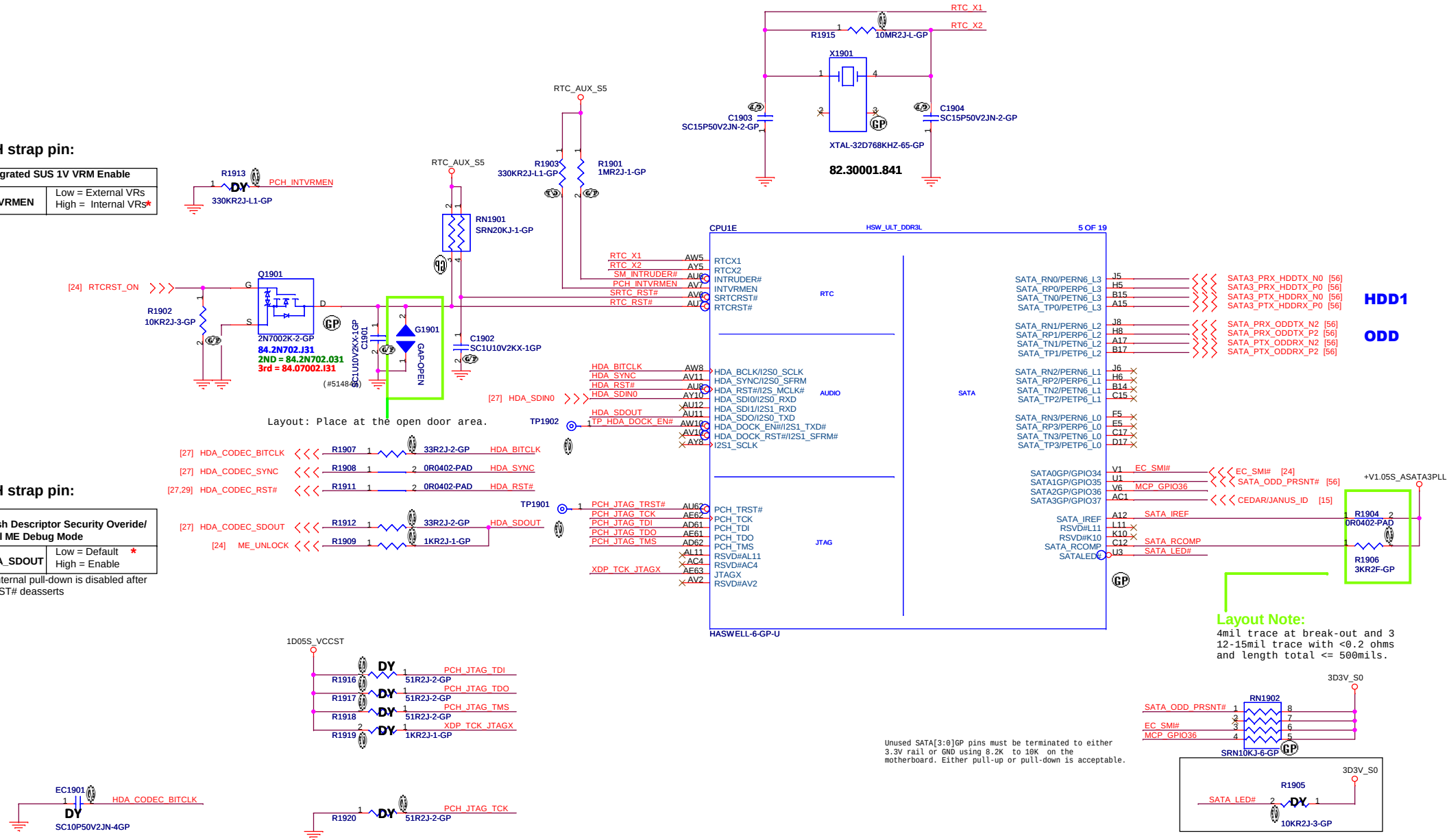
PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

Wistron Corporation
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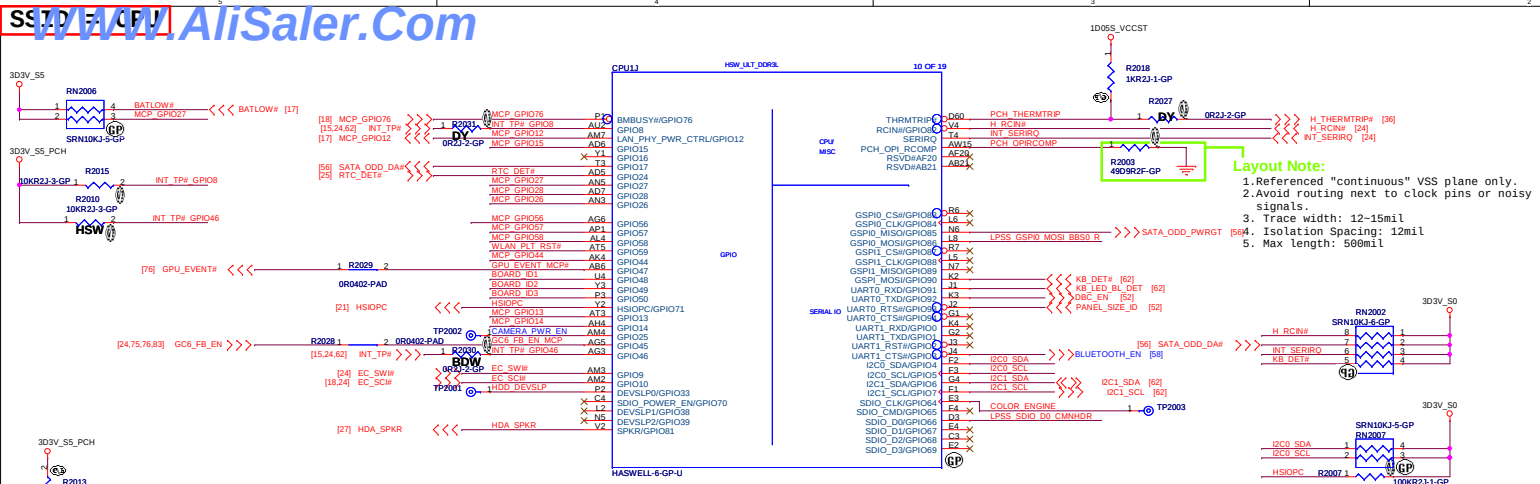
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (RTC/SATA/HDA/JTAG)

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 19 of 104



PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode * Low = Disable "Top-Block swap" mode (Default)

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

PCH strap pin:

TLS Confidentiality	
GPIO15	*Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI (Default) High = LPC

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

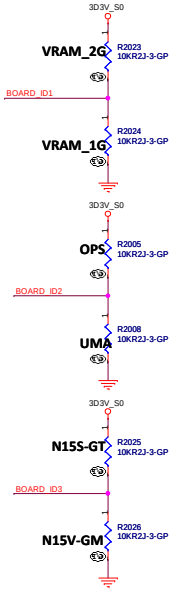
BIOS VRAM Size Strap pin	BOARD_ID1
1G	0
2G	1

BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM-S(DVC40/50)	0
N15S-GT (DVC70)	1



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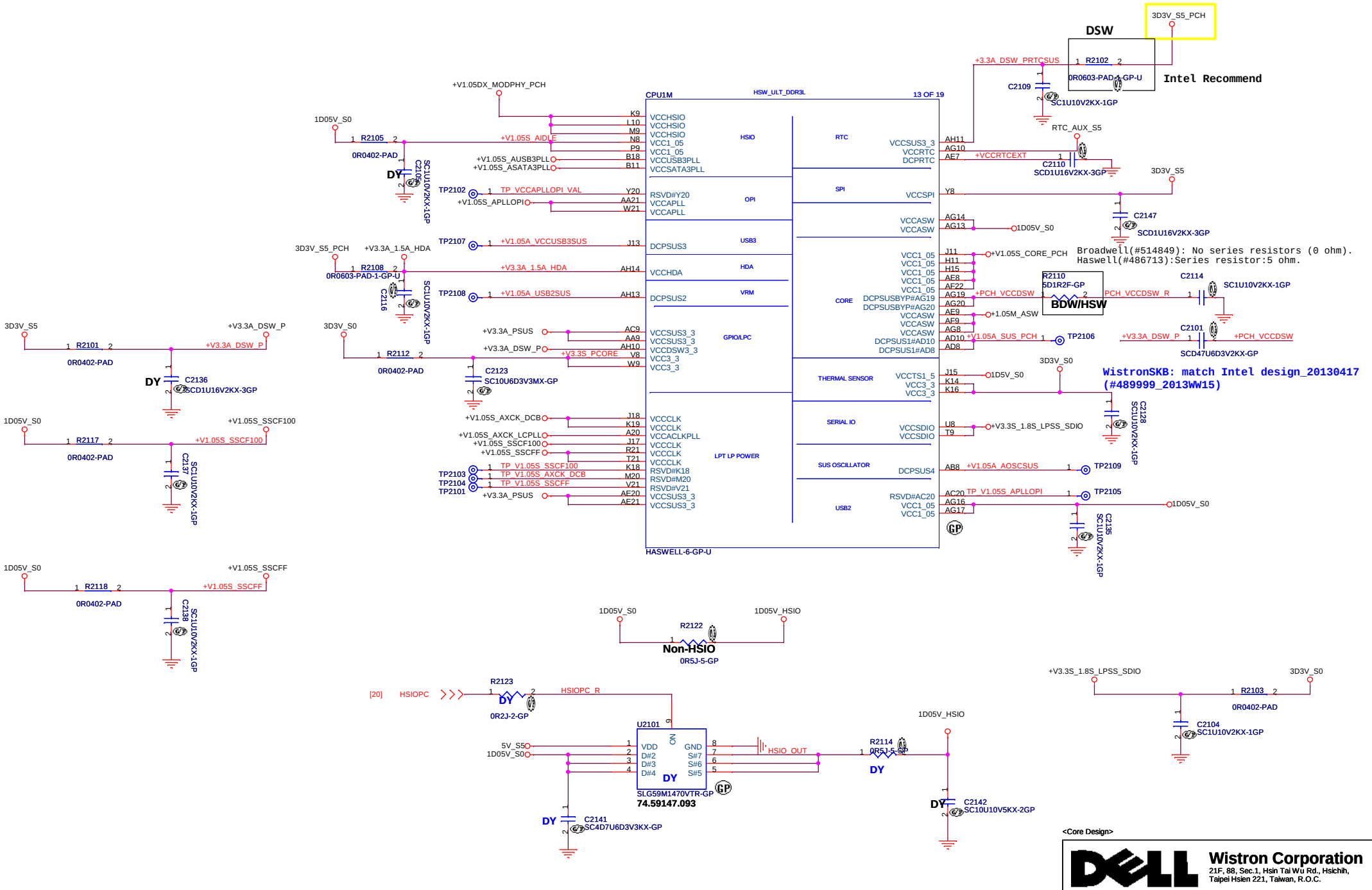
Title: CPU (GPIO/MISC)

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 20 of 104



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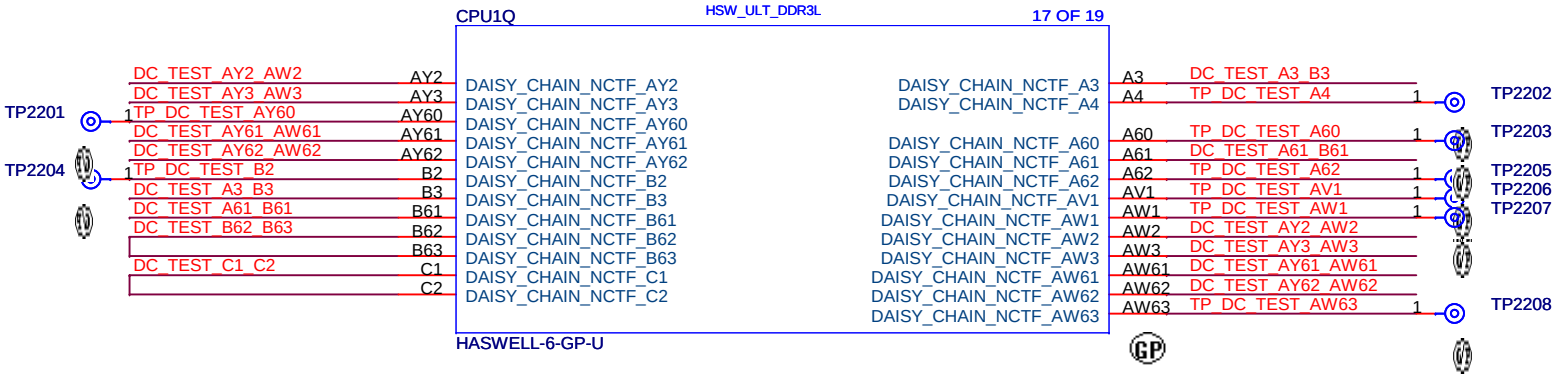
Taipei Hsien 221, Taiwan, R.O.C.

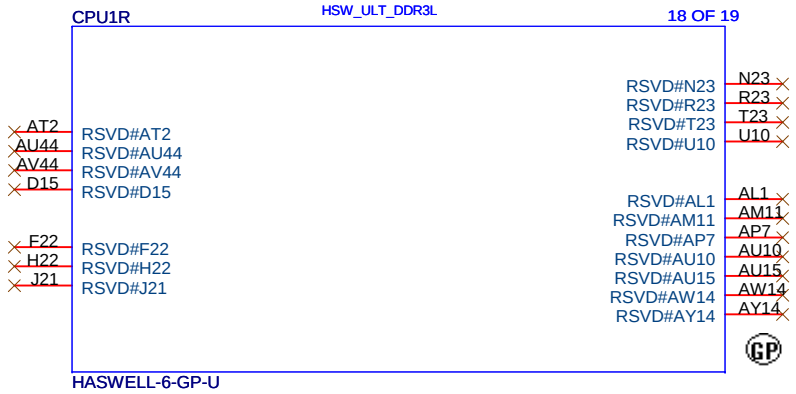
Title: CPU (POWER2)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 21 of 104

SSID = PCH





<Core Design>

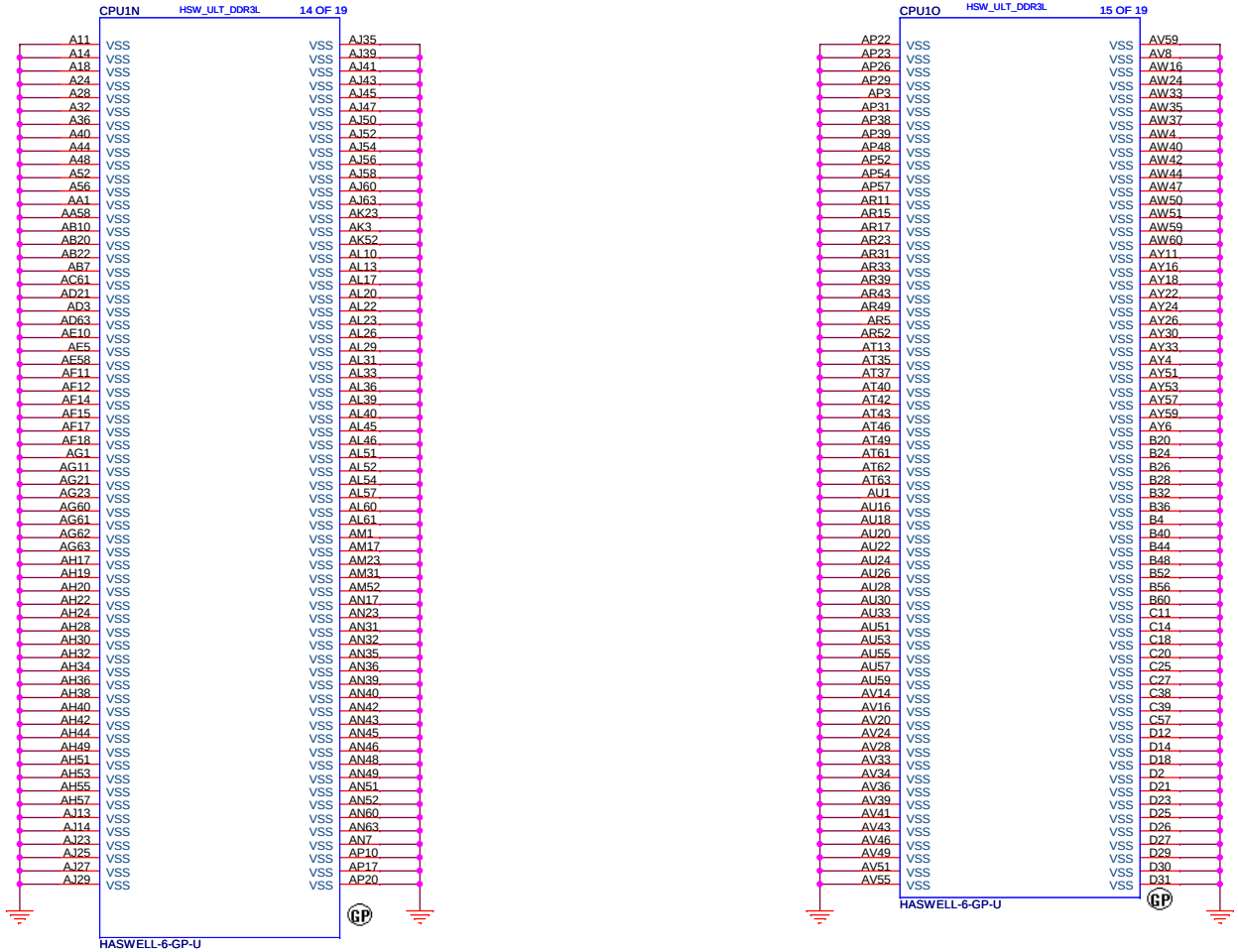
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RSVD)

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 22 of 104

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VSS)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 23 of 104

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO67)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Janus-DPS	100.0K	10.0K/64.10025.6D1	3.6V
Janus-UMA	100.0K	13.7K/64.13725.6D1	2.962V
TBD	100.0K	17.8K/64.17825.6D1	2.801V
TBD	100.0K	22.1K/64.22125.6D1	2.702V
TBD	100.0K	27.0K/64.27025.6D1	2.598V
TBD	100.0K	32.4K/64.32425.6D1	2.491V
TBD	100.0K	37.4K/64.37425.6D1	2.402V
TBD	100.0K	41.2K/64.41225.6D1	2.364V
TBD	100.0K	49.9K/64.49925.6D1	2.291V
Cedar-DPS	100.0K	57.6K/64.57625.6D1	2.051V
Cedar/UMA	100.0K	64.9K/64.64925.6D1	2.001V
TBD	100.0K	73.2K/64.73225.6D1	1.961V
TBD	100.0K	82.5K/64.82525.6D1	1.898V
TBD	100.0K	93.1K/64.93125.6D1	1.789V
TBD	100.0K	107K/64.10735.6D1	1.594V
TBD	100.0K	120K/64.12035.6D1	1.459V
TBD	100.0K	137K/64.13735.6D1	1.192V
TBD	100.0K	154K/64.15435.6D1	1.05V
TBD	100.0K	200K/64.20035.6D1	1.695V
TBD	100.0K	232K/64.23235.6D1	0.951V

Layout Note:
Need very close to EC

ALL_SYS_PWRGD assert, delay 10ms; PCH_PWROK assert.

ALL_SYS_PWRGD de-assert, delay 100ms; SYS_PWROK assert.

LVDS backlight Control from PS8625

eDP backlight Control from PCH

071.00285.000G

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

Power Switch Logic(PSL)

EC_GPIO47 High Active

83.R2004.H8F

83.R2004.H8F

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

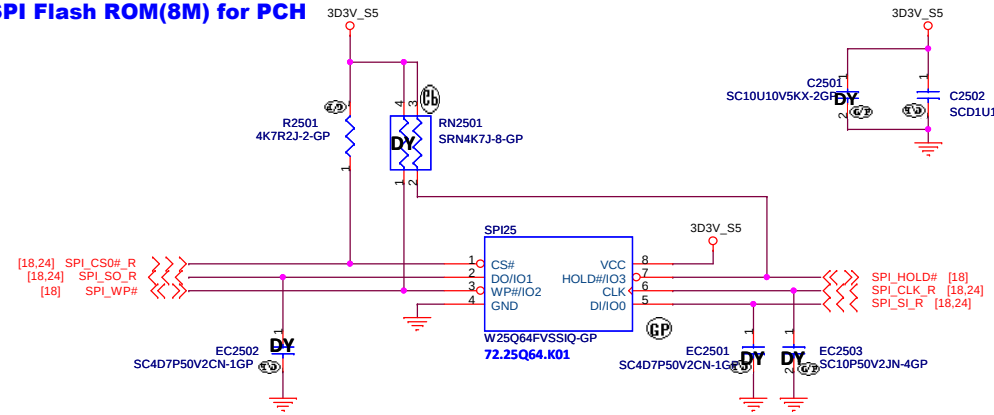
Title: KBC Nuvoton NPCE885

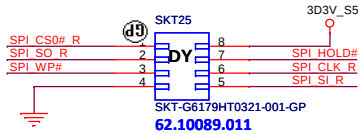
Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 01, 2013 | Sheet 24 of 38

SSID = Flash.ROM

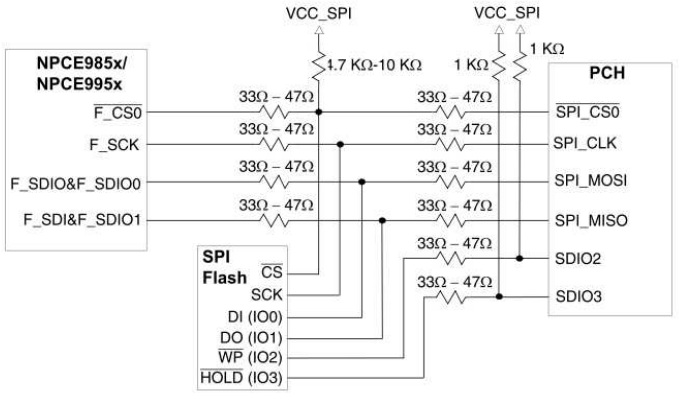
SPI Flash ROM(8M) for PCH





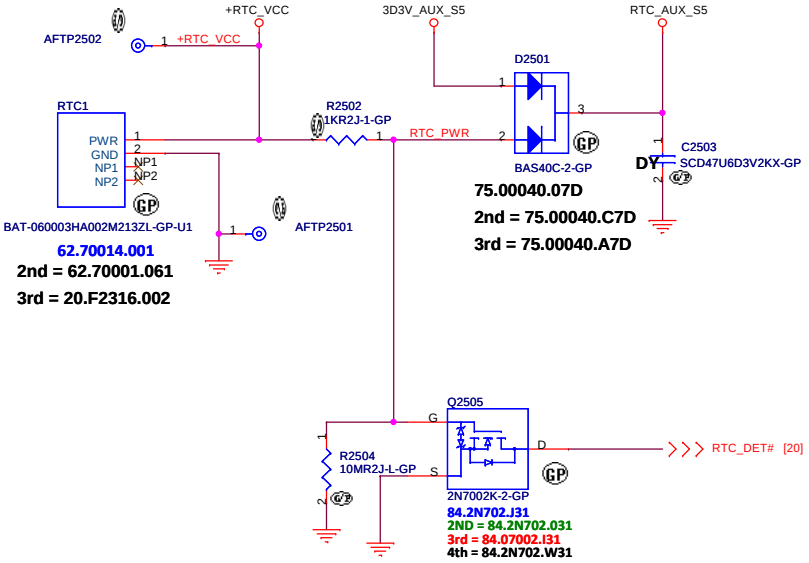
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O
072.25B64.0001	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 25 of 104

SSID = Thermal

Fan controller1

R2605 0R2J-2-GP (DY) 5V_S0 FAN_VCC1 FON# [24] FAN1_DAC_1

FAN261 AP2113MTR-G1-GP 74.02113.0E1

5V_S0 C2605 SCD1U16V2KX-3GP C2611 SC4D7U6D3V3KX-GP

Layout Note:
Need 10 mil trace width.

[24] FAN_TACH1 R2606 0R0402-PAD FAN_TACH1_C FAN_VCC1

FAN1 ETY-CON3-8-GP 20.F1841.003 2nd = 20.F1295.00 AFTP2803

C2604 SC4D7U6D3V3KX-GP (DY) D2601 RB551V30-GP C2603 SC2200P50V2KX-2GP (DY) 83.R5003.H8H

Layout Note:
Signal Routing Guideline:
Trace width = 15mil

AFTP2802 FAN_TACH1_C
AFTP2801 FAN_VCC1

3D3V_S0 R2603 18K7R2F-GP ALERT#
R2604 2KR2F-3-GP T_CRIT#

3D3V_AUX_KBC R2607 2KR2F-3-GP R2602 THERM_SYS_SHDN# 0R2J-2-GP VD_OUT1# [24]

Close to Thermal sensor

Close to KBC
VD_IN1 for system thermal sensor

3D3V_AUX_S5 R2609 24K9R2F-L-GP
3D3V_AUX_KBC R2608 24K9R2F-L-GP
VD_IN1 [24]
R2610 NTC-100K-8-GP C2612 SCD1U16V2KX-3GP C2613 SC100P50V2JN-3GP
VD_IN1_C R2611 0R0402-PAD

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

3D3V_S0 C2601 SC10U6D3V3MX-GP (DY) C2602 SCD1U16V2KX-3GP

[18,24,76] SML1_DATA 84.2N702.A3F 2nd = 84.2N702.E3F 3rd = 75.00601.07C 4th = 84.DMN66.03F
2N7002KDW-GP Q2601 (DY)
RN2602 SRN2K2J-1-GP
THM_SML1_DATA
THM_SML1_CLK
[18,24,76] SML1_CLK

84.T3904.H11
Q2603 LMBT3904LT1G-GP
NCT7718_DXP NCT7718_DXN
C2606 SC470P50V3JN-2GP (DY) C2607 SC2200P50V2KX-2GP
T_CRIT#

THM26 NCT7718W-GP 74.07718.0B9
VDD D+ D- T_CRIT# SCL SDA ALERT# GND
THM_SML1_CLK THM_SML1_DATA ALERT#
C2608 SCD1U16V2KX-3GP (DY) C2609 SCD1U16V2KX-3GP (DY)

2.System Sensor, Put on palm rest

Layout Note:
C2812 close U2801

R2601 0R2J-2-GP (DY)
[17,24,36] PCH_PWROK
THERM_SYS_SHDN#

Q2602 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31
C2610 SCD1U16V2KX-3GP (DY)

PURE_KBCT8 R2612 0R2J-2-GP VD_OUT1#
PURE_HW_SHUTDOWN# [24,36,76]

FAN_TACH1 FAN_VCC1
EC2602 SC10P50V2JN-4GP (DY) EC2601 SCD1U16V2KX-3GP (DY)

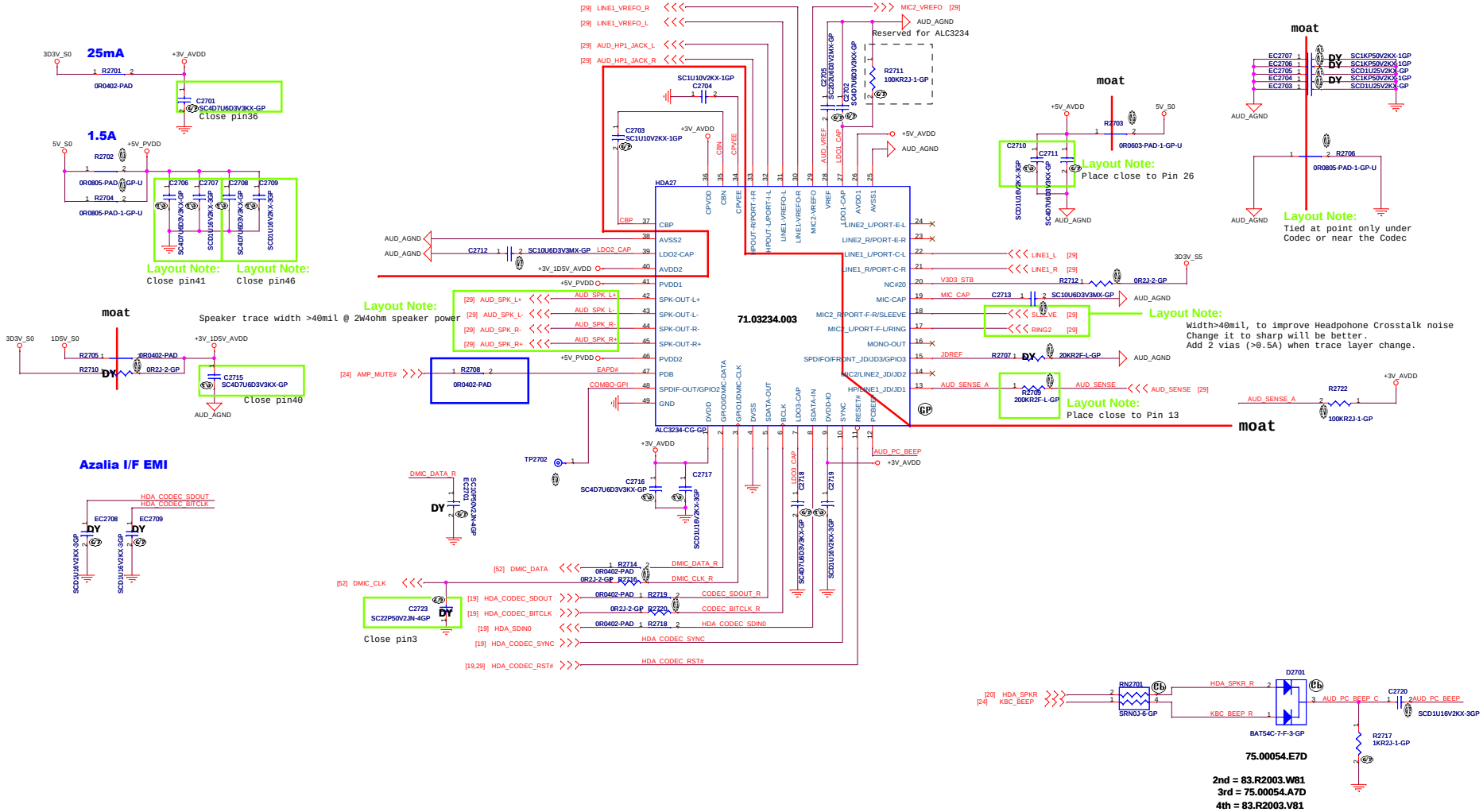
Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan
Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00
Date: Friday, February 07, 2014 | Sheet 26 of 104

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3234

Size	Document Number	Rev
A2	Janus HSW 40/50/70	A00

Date: Monday, February 10, 2014 Sheet 27 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

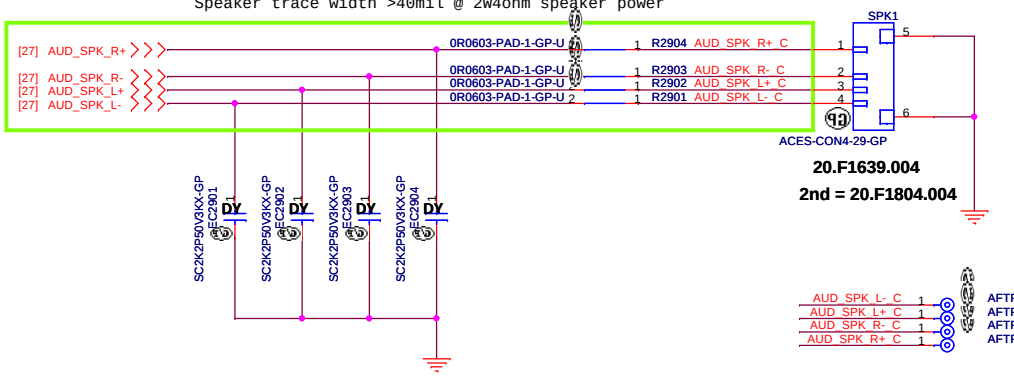
Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 28 of 104

SSID = AUDIO

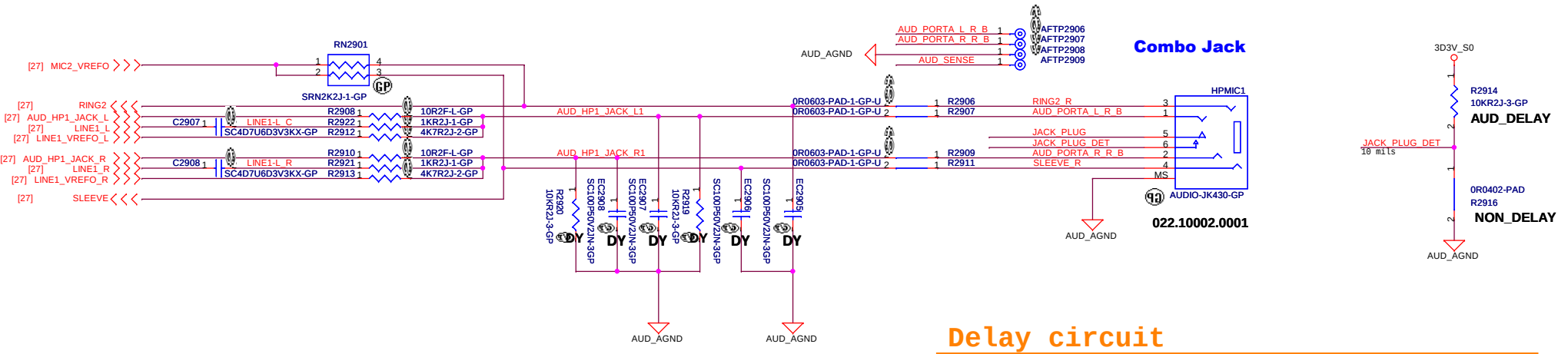
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

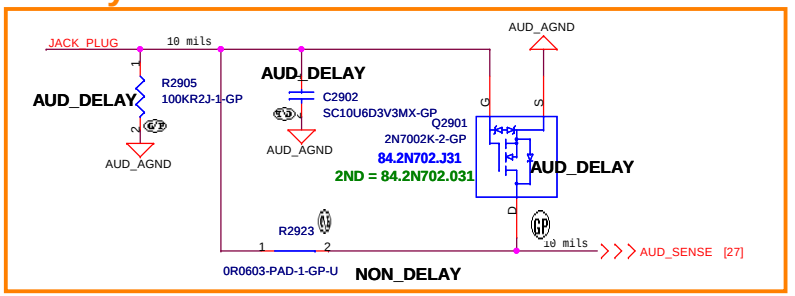


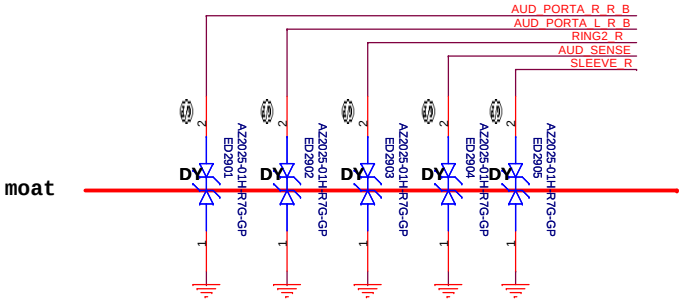
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

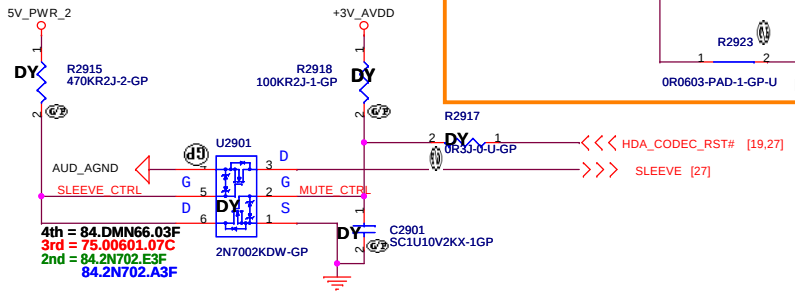
Combo Jack



Delay circuit





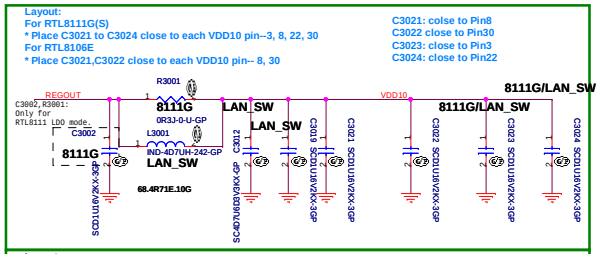


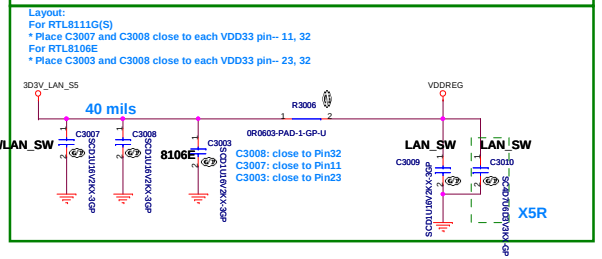
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

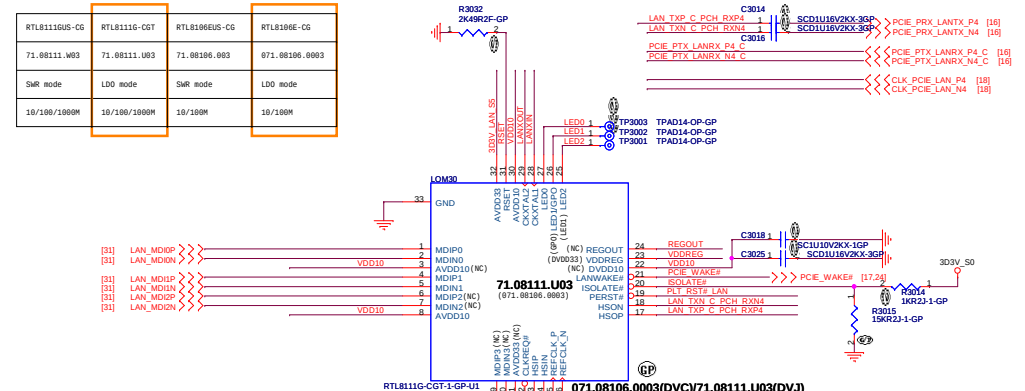
Title: Speaker/HPMIC
Size: A3
Document Number: Janus HSW 40/50/70
Rev: A00
Date: Friday, February 07, 2014
Sheet 29 of 104

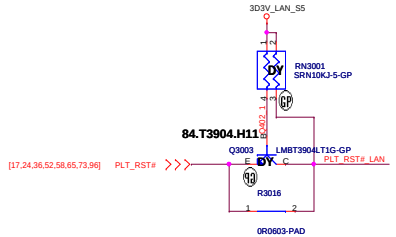
LAN CHIP (10/100/1000M & 10/100M co-lay)

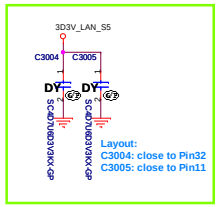




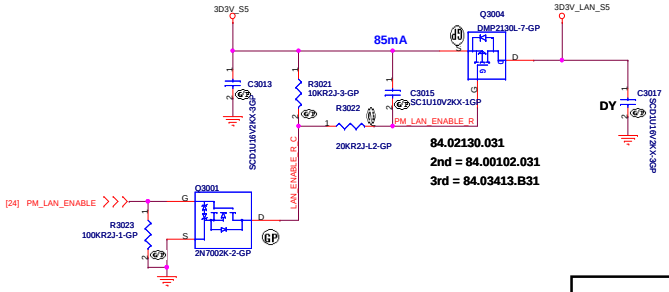
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

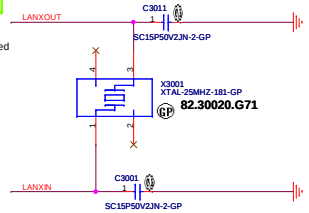


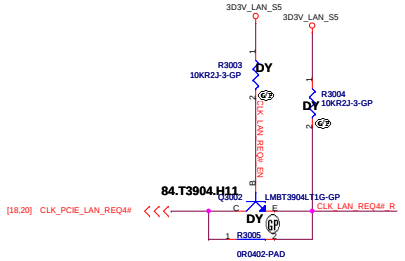




3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.







	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	0	0	0	0	0	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	SWR	X	X	0	0	0	0	0	0	0	0	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	0

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: LAN RTL8111/RTL8106
Size: A2
Document Number: Janus HSW 40/50/70
Rev: A00
Date: Friday, February 07, 2014
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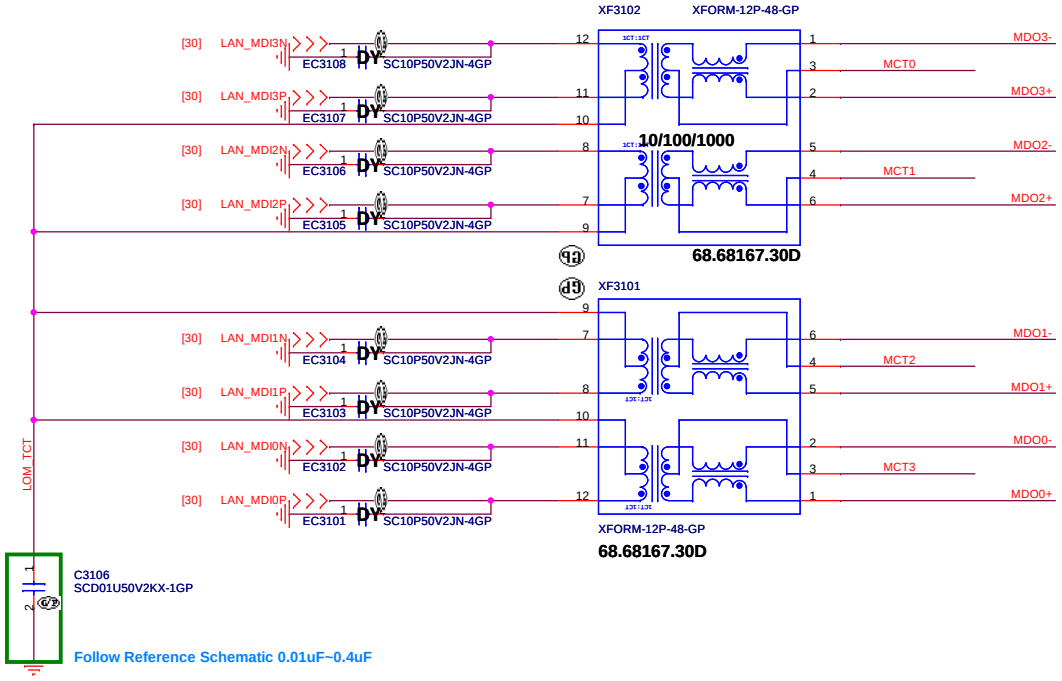
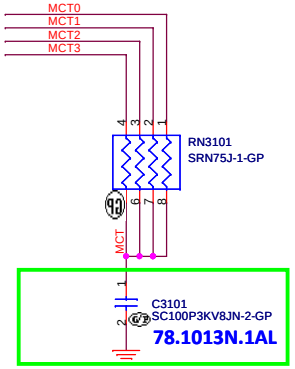
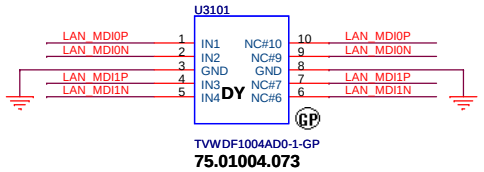
SSID = LOM

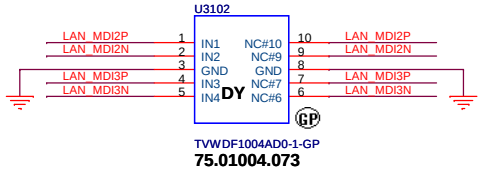
LAN TransFormer (10/100/1000M & 10/100M co-lay)

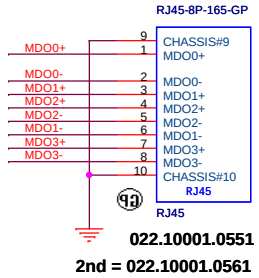
Layout note:
30 mil spacing between MDI differential pairs.



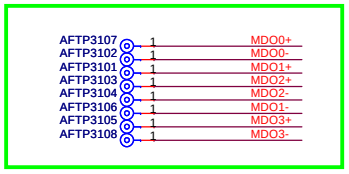








Layout:
Place near RJ45



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

Date: Monday, February 10, 2014 Sheet 31 of 104

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)Card Reader

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 32 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

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SSID = USB

[16] USB_PN1
[16] USB_PP1
TR3401
FILTER-4P-6-GP
69.10103.041
USB_PN1_R
USB_PP1_R

U3401
USB_PN1_R
USB_PP1_R
I/O1
GND
I/O2
I/O4
VDD
I/O3
USB20_VCCA
DY
C3406
SCD1U16V2KX-3GP
75.09904.07C
AZC099-04S-1-GP

USB20_VCCA
USB_PN1_R
USB_PP1_R
AFTP6205
AFTP6204
AFTP6209

USB2.0 Port2
USB20_VCCA
USB2
USB_PN1_R
USB_PP1_R
SKT-USB8-14-GP
22.10321.E91

[16] USB_PN0
[16] USB_PP0
TR3404
FILTER-4P-6-GP
69.10103.041
USB_PN0_C
USB_PP0_C

U3402
USB3_PRX_CTX_N0_C
USB3_PRX_CTX_P0_C
USB3_PTX_CRX_N0_C
USB3_PTX_CRX_P0_C
IN1
IN2
GND
IN3
IN4
NC#10
NC#9
GND
NC#7
NC#6
DY
TVWDF1004AD0-1-GP
75.01004.073

U3403
USB_PN0_C
USB_PP0_C
I/O1
GND
I/O2
I/O4
VDD
I/O3
DY
AZC099-04S-1-GP
75.09904.07C
USB30_VCCC
DY
C3405
SCD1U16V2KX-3GP

USB3.0 Port1
USB30_VCCC
USB_PN0_C
USB_PP0_C
AFTP6210
AFTP6211
AFTP6212
USB1
USB3_PTX_CRX_P0_C
USB30_VCCC
USB3_PTX_CRX_N0_C
USB_PN0_C
USB_PP0_C
USB3_PRX_CTX_P0_C
USB3_PRX_CTX_N0_C
SKT-USB13-151-GP
AFTP6217
22.10341.Q21

[16] USB3_PTX_CRX_P0
C3404
SCD1U16V2KX-3GP
USB3_PTX_CRX_P0_R
R3408
0R0402-PAD
USB3_PTX_CRX_P0_C

[16] USB3_PRX_CTX_P0
R3410
0R0402-PAD
USB3_PRX_CTX_P0_C

[16] USB3_PTX_CRX_N0
C3403
SCD1U16V2KX-3GP
USB3_PTX_CRX_N0_R
R3409
0R0402-PAD
USB3_PTX_CRX_N0_C

[16] USB3_PRX_CTX_N0
R3411
0R0402-PAD
USB3_PRX_CTX_N0_C

USB3_PTX_CRX_P0_C
USB3_PTX_CRX_N0_C
C3402
C3401
DY
DY
SC4D7H50V2CN-1GP
SC4D7H50V2CN-1GP

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0
Size: Custom
Document Number: Janus HSW 40/50/70
Rev: A00
Date: Monday, February 10, 2014
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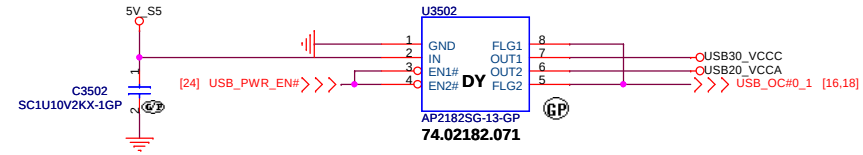
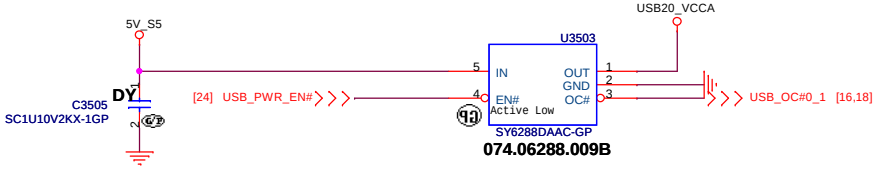
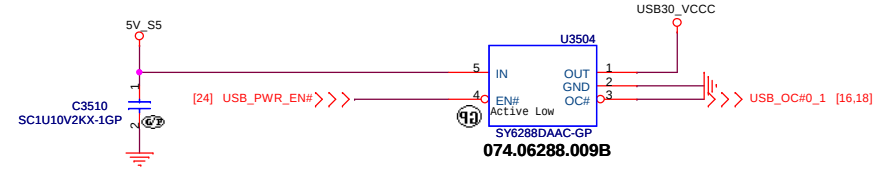
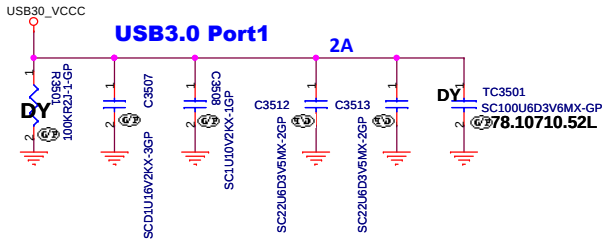
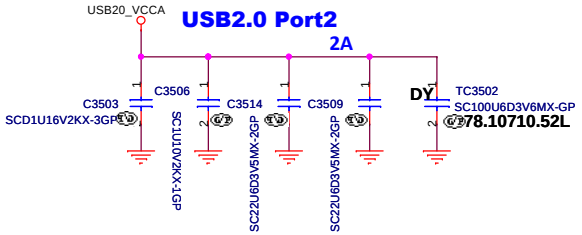


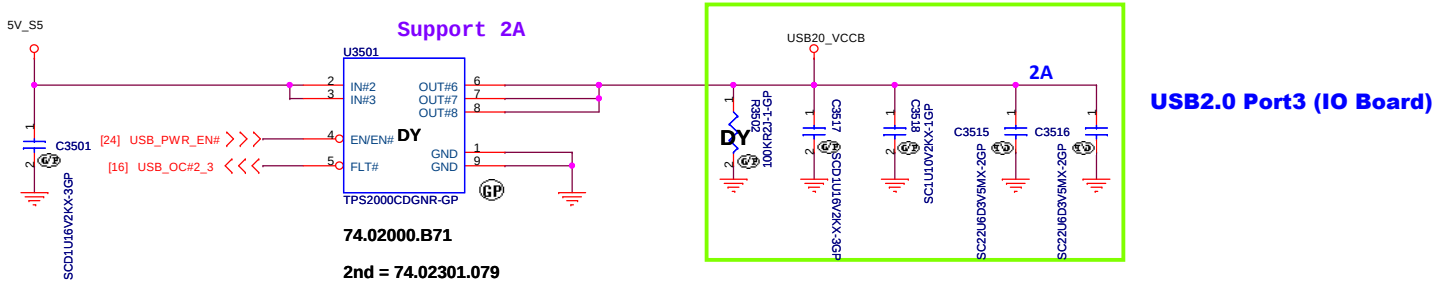




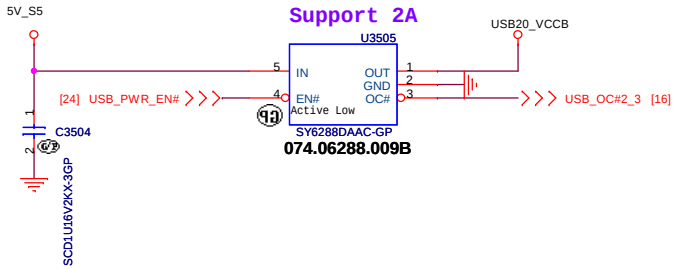




Layout Note: Close CON1



USB2.0 Port3 (IO Board)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size | Document Number: Janus HSW 40/50/70 | Rev: A00

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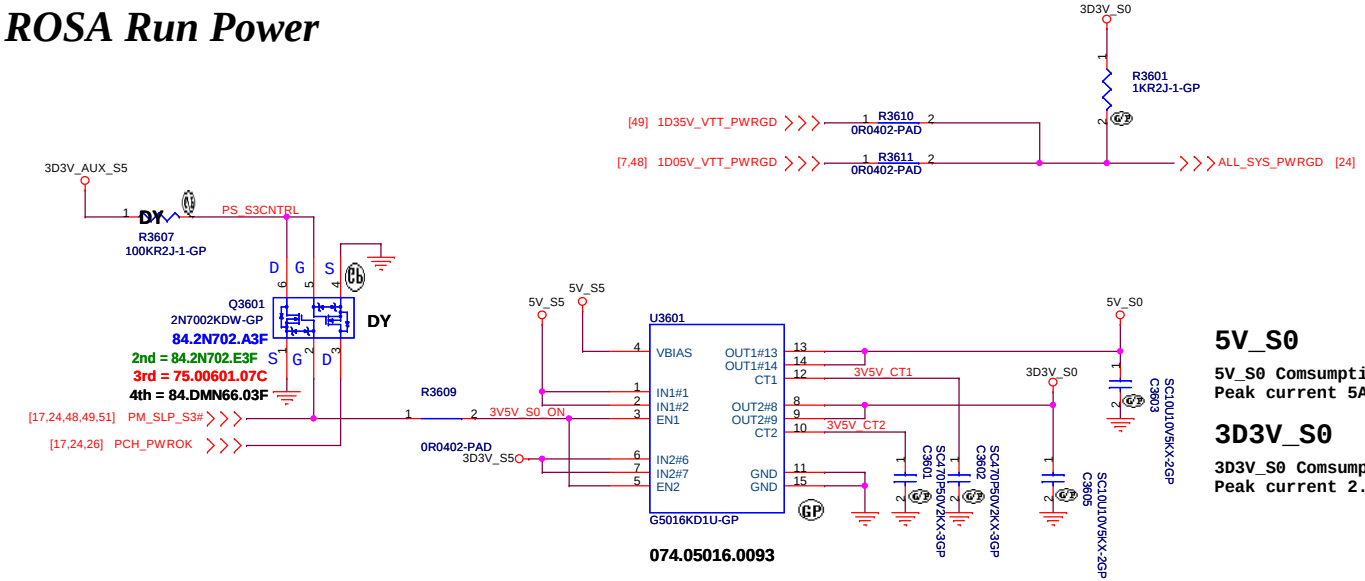
SSID = Reset.Suspend

Power Good

ROSA Run Power

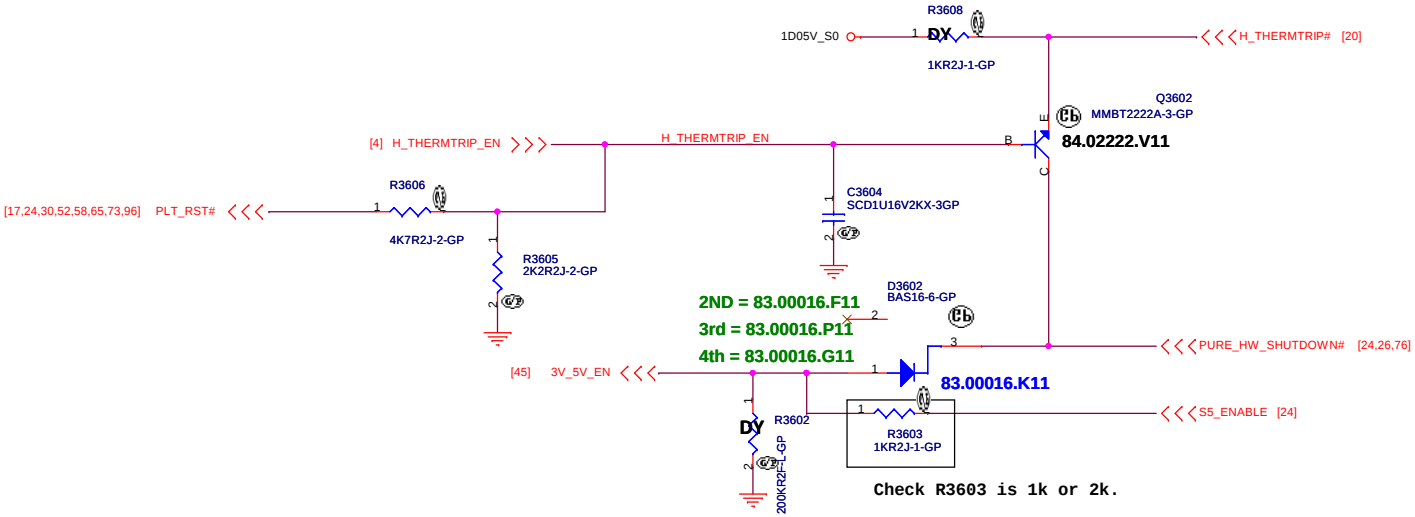


5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A



Check R3603 is 1k or 2k.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

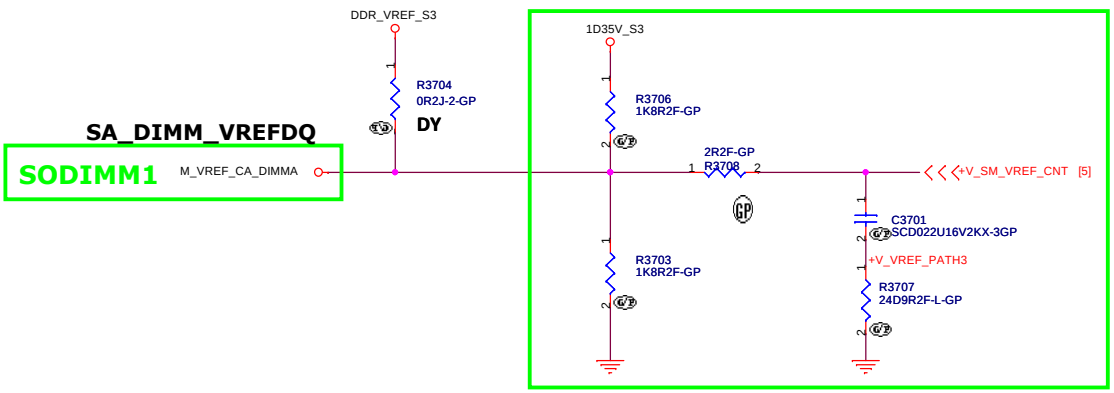
Title: Power Plane Enable

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

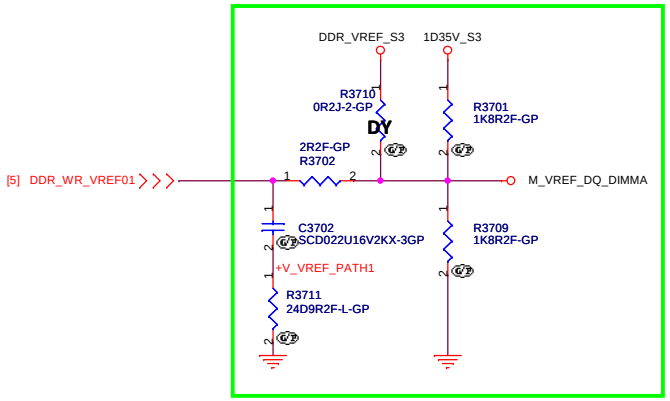
Date: Monday, February 10, 2014 Sheet 36 of 104

SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMM1



Layout Note:
Place Close SO-DIMM1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *S3 Reduction Circuit*

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

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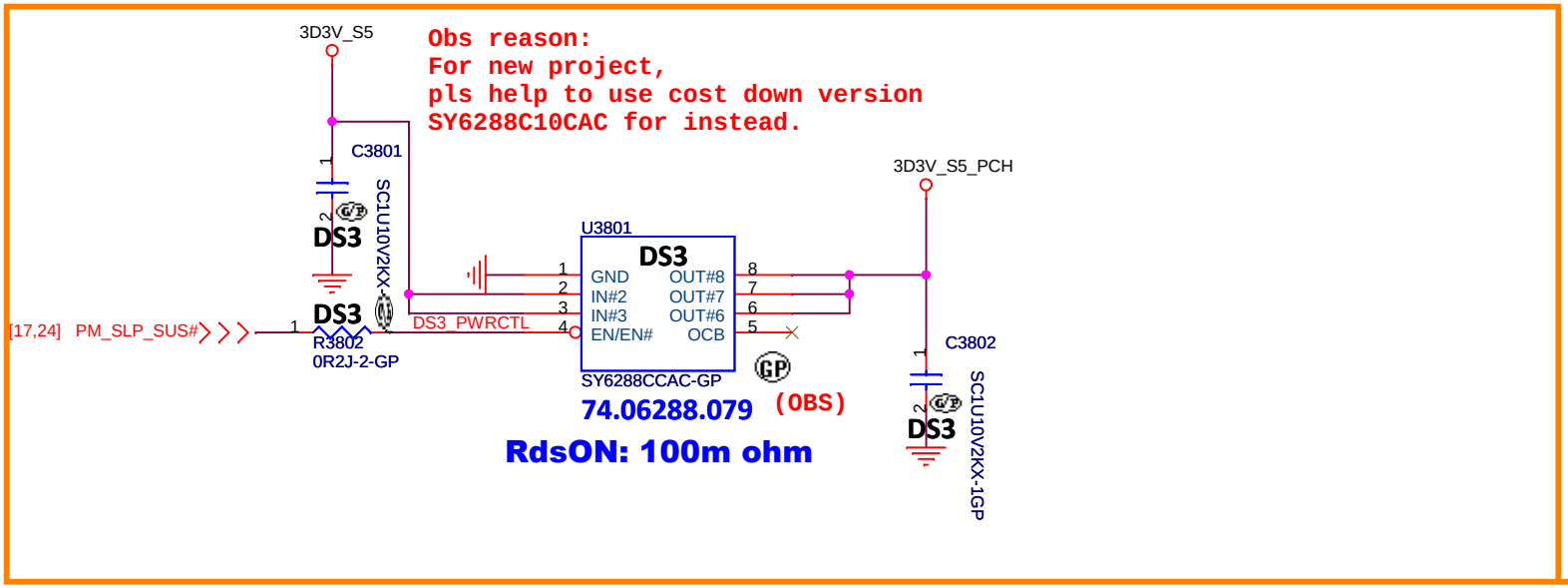

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DSW

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 38 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved) 1D05_M

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 39 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	*Janus HSW 40/50/70*	*A00*

Date: Friday, February 07, 2014 Sheet 40 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

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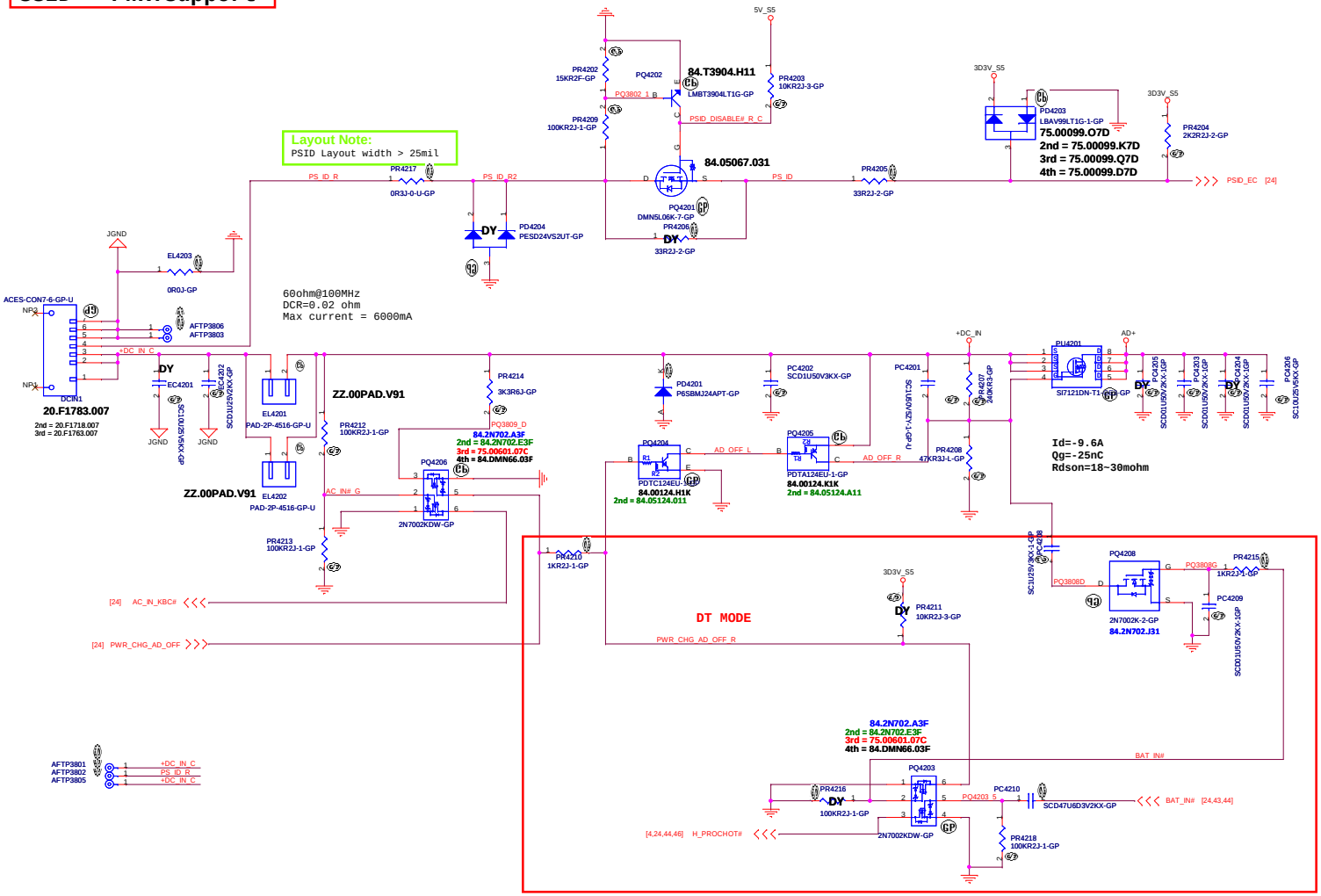
SSID = PWR.Support



<Core Design>

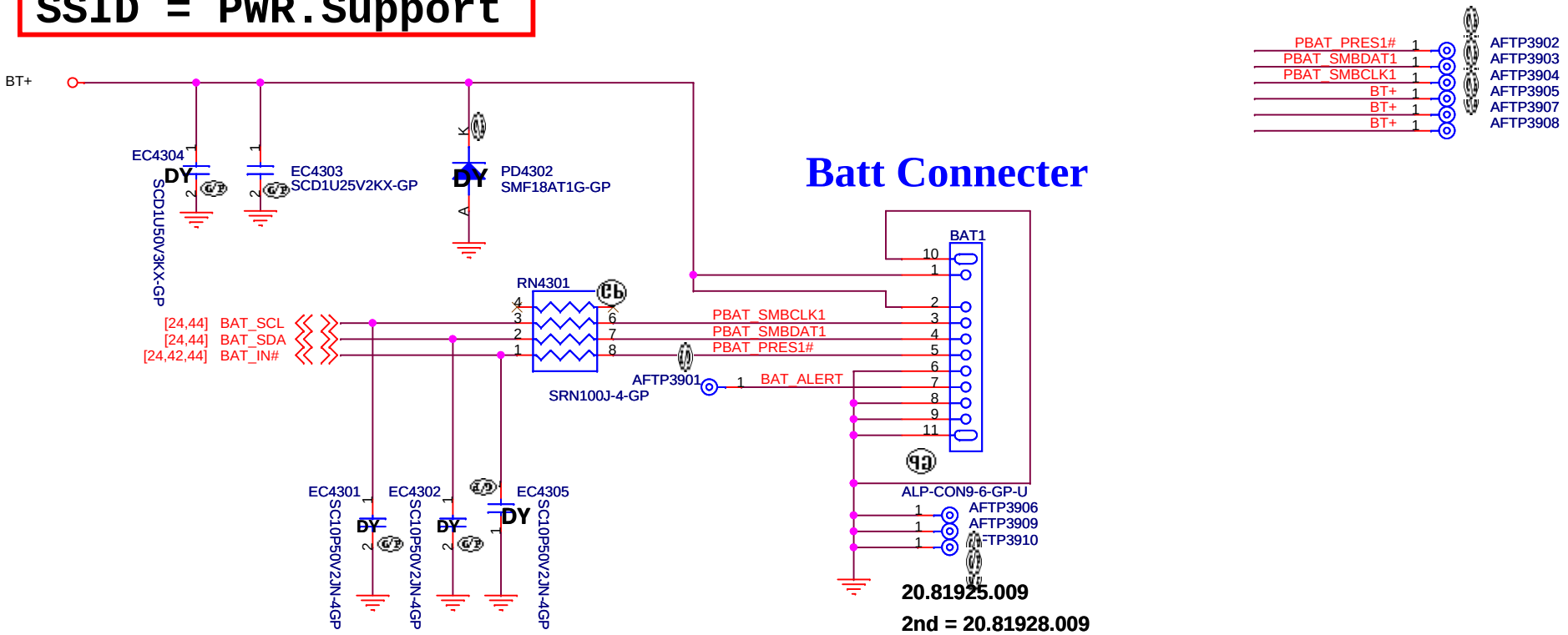
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN

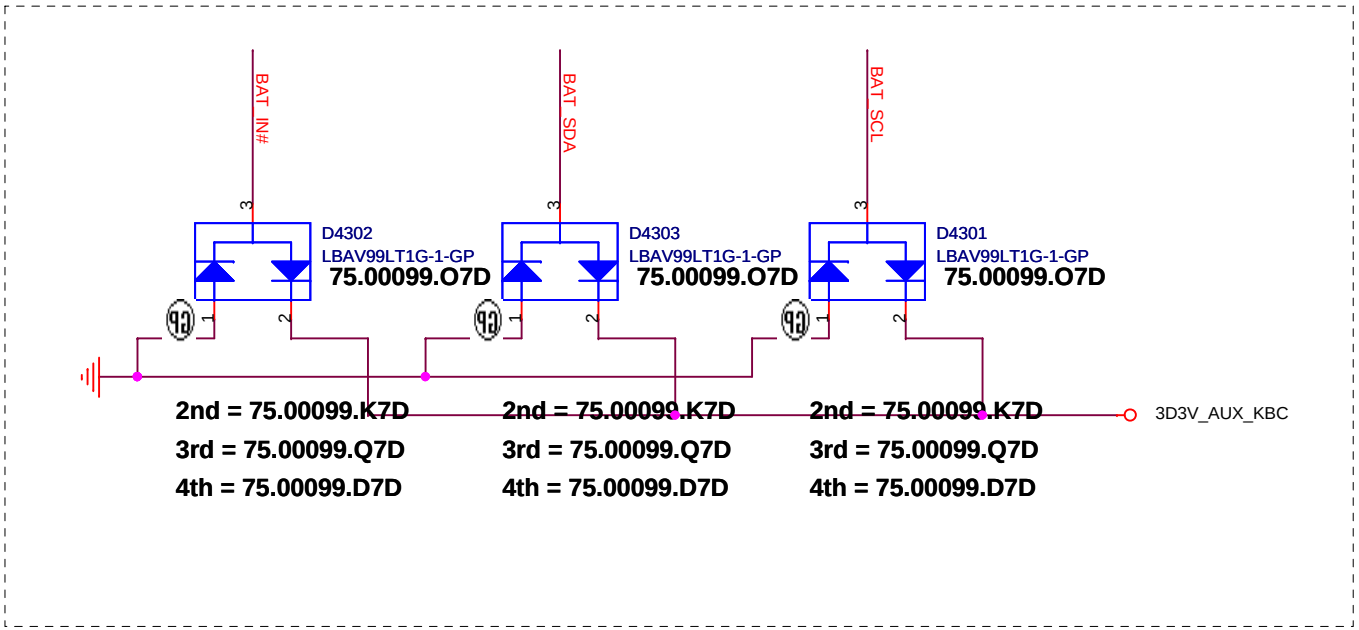
Size	Document Number	Rev
A2	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 42 of 104

SSID = PWR.Support



Placement: Close to Batt Connector



<Core Design>

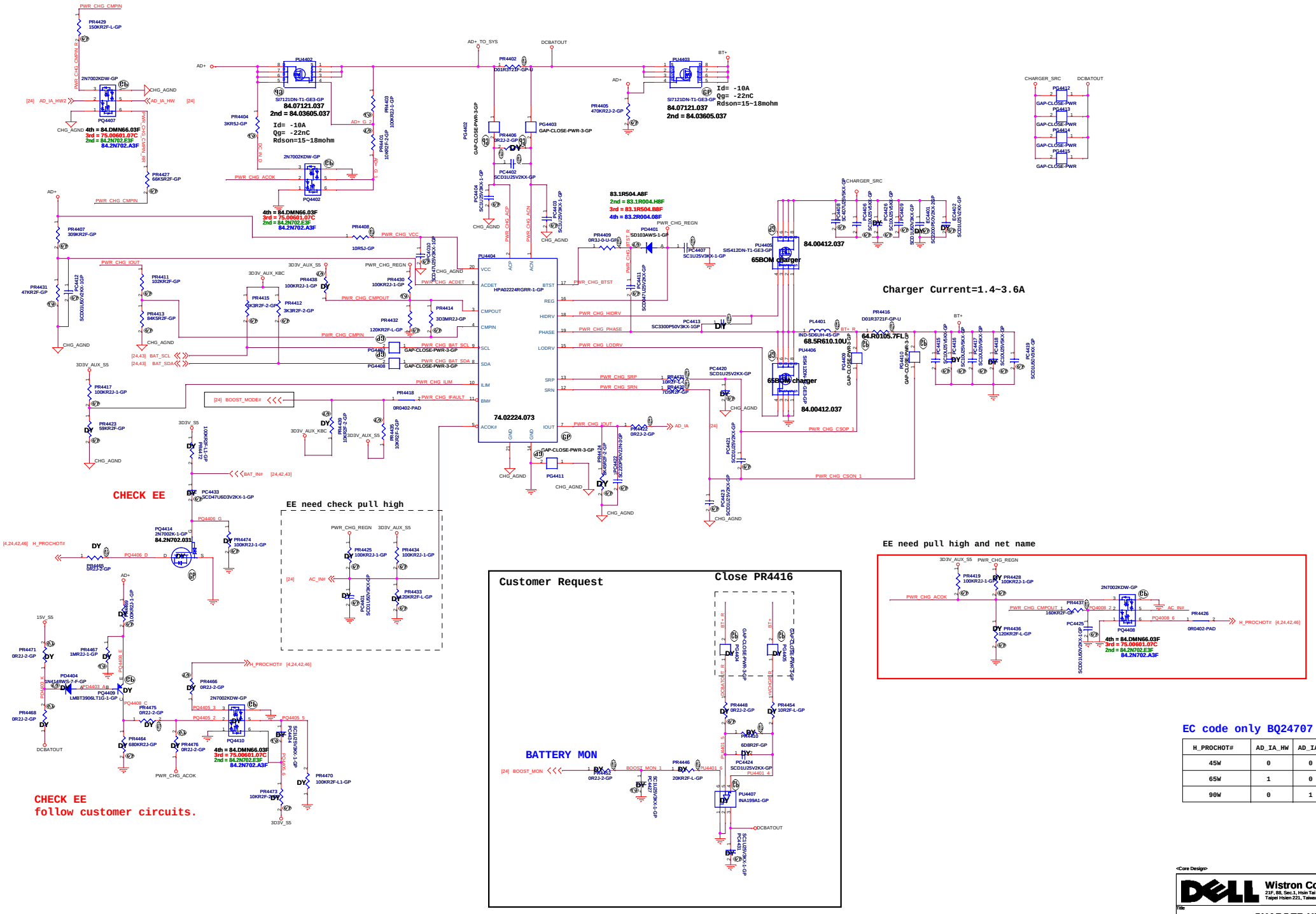
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 43 of 104

SSID = Charger



H_PROCHOT#	AD_IA_HW	AD_IA_HW2
45W	0	0
65W	1	0
90W	0	1

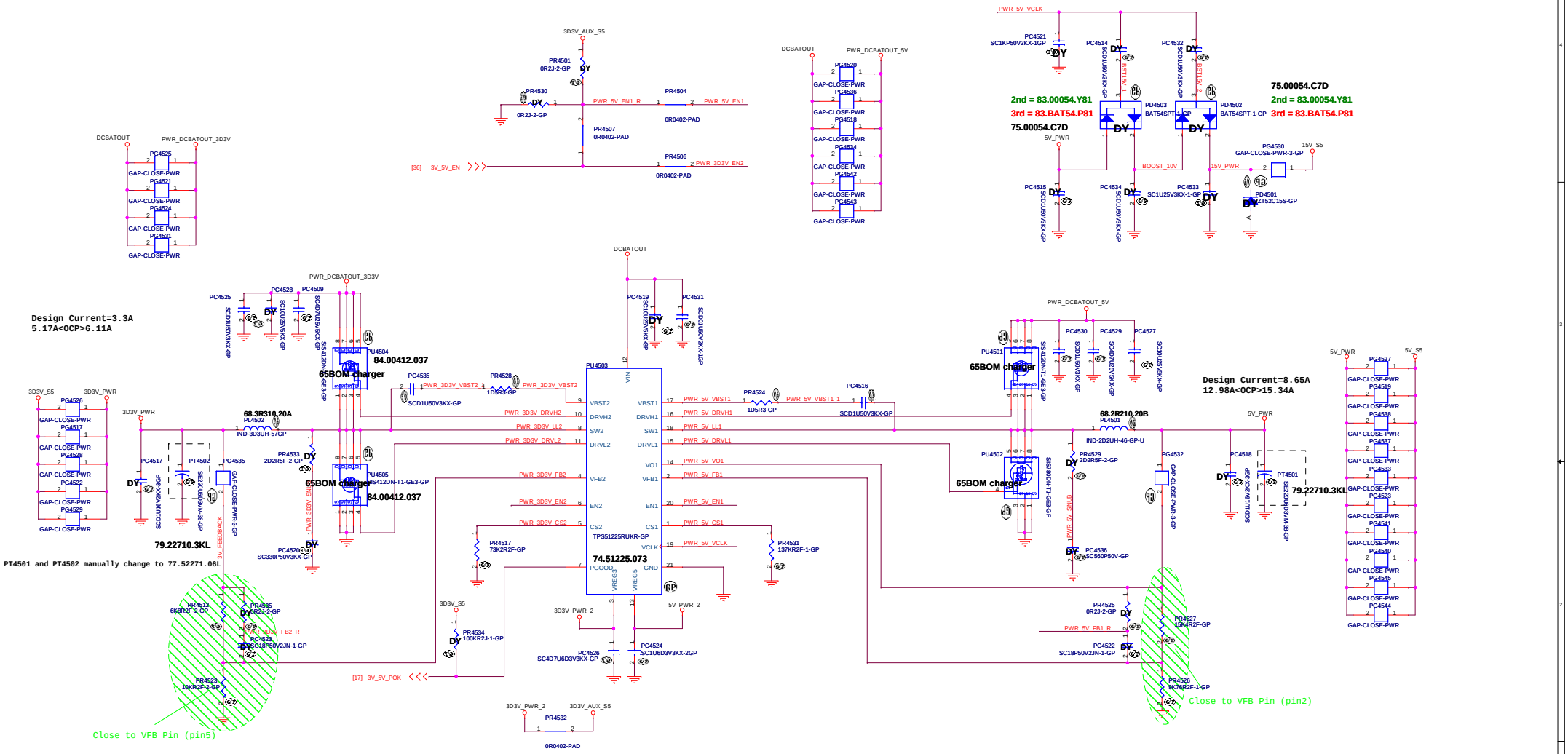
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER HPA02224

Size: Custom | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 44 of 104

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

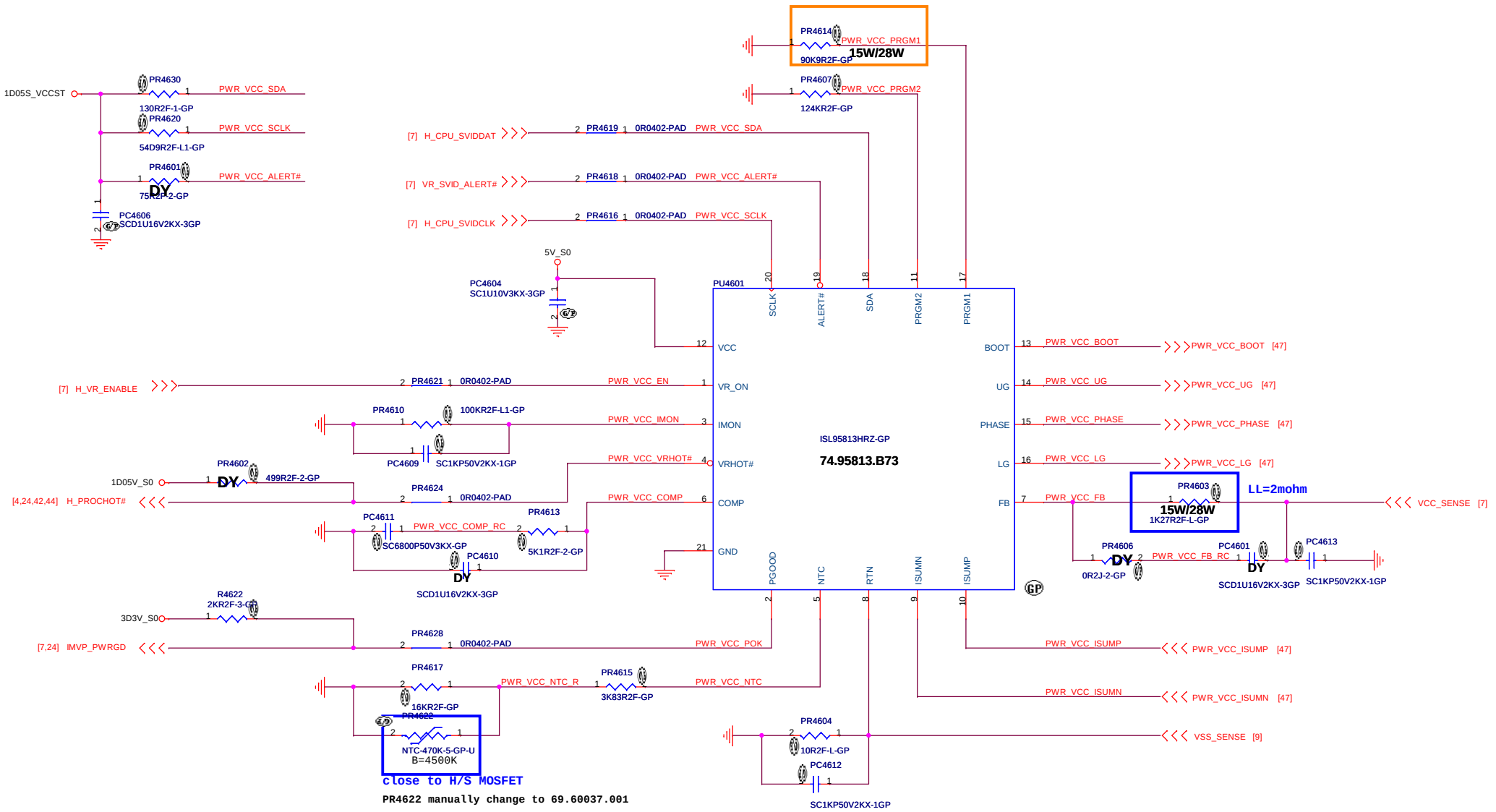
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51225

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

Date: Friday, February 07, 2014 | Sheet 45 of 104

SSID = CPU.Regulator



	PR4603	PR4614
15W	1.27K 64.12715.6DL	90.9K 64.90925.6DL
28W	1.58K 64.15815.6DL	113K 64.11335.6DL

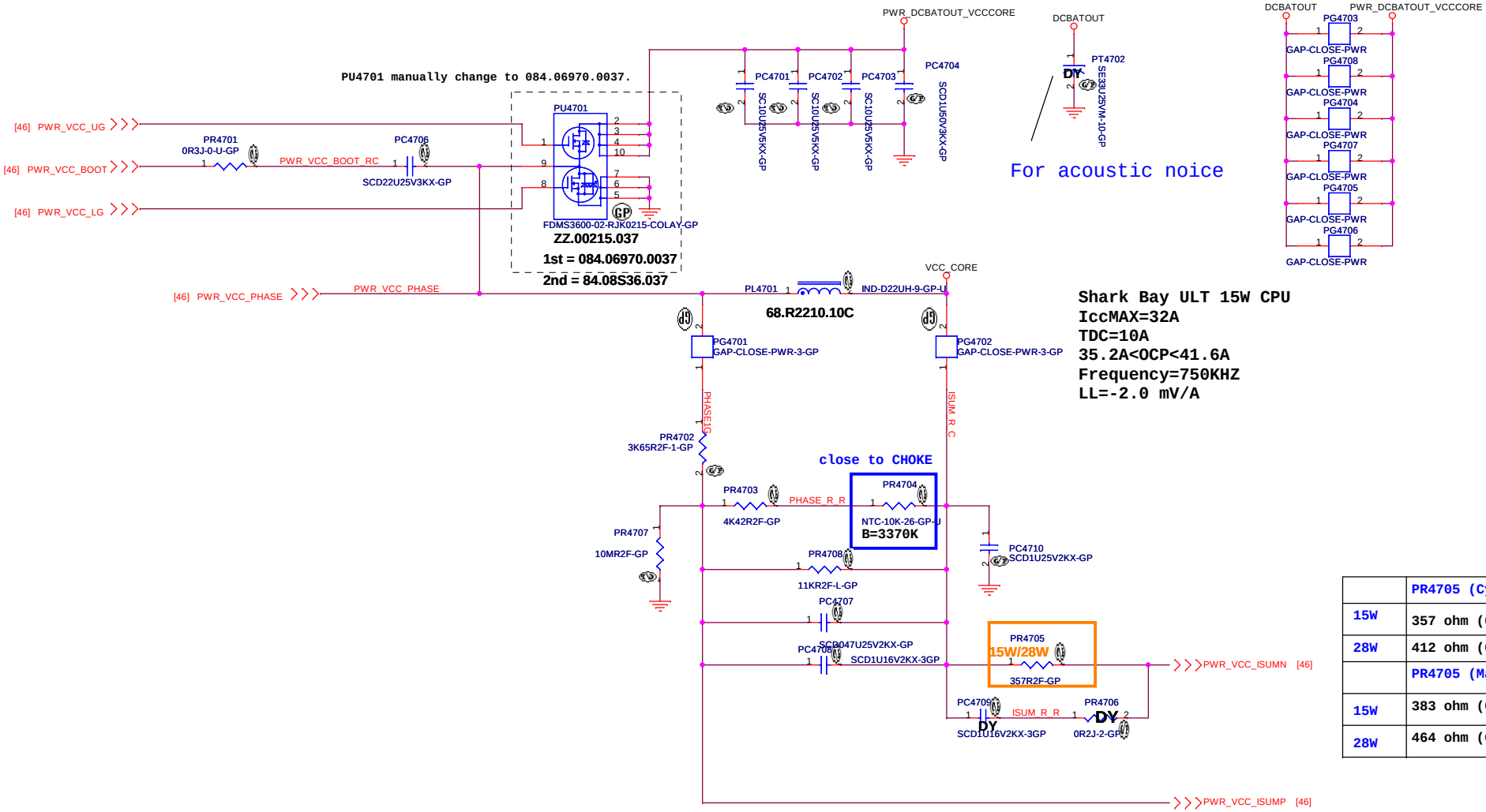
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95813_CPUCORE(1/2)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

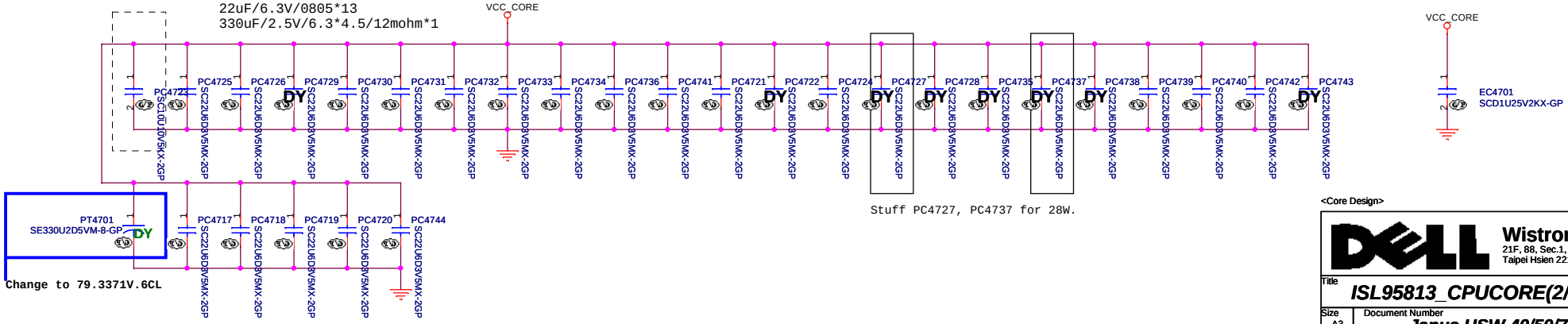
Date: Friday, February 07, 2014 | Sheet 46 of 104



Shark Bay ULT 15W CPU
IccMAX=32A
TDC=10A
35.2A<OCP<41.6A
Frequency=750KHZ
LL=-2.0 mV/A

	PR4705 (Cyntec)	OCP
15W	357 ohm (64.35705.6DL)	38A
28W	412 ohm (64.41205.6DL)	48A
	PR4705 (Maglayers)	
15W	383 ohm (64.38305.6DL)	38A
28W	464 ohm (64.46405.6DL)	48A

Change PC4723 to 10U from 22U based on PI Simulation.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95813_CPUCORE(2/2)
Size: A3
Document Number: Janus HSW 40/50/70
Rev: A00
Date: Friday, February 07, 2014
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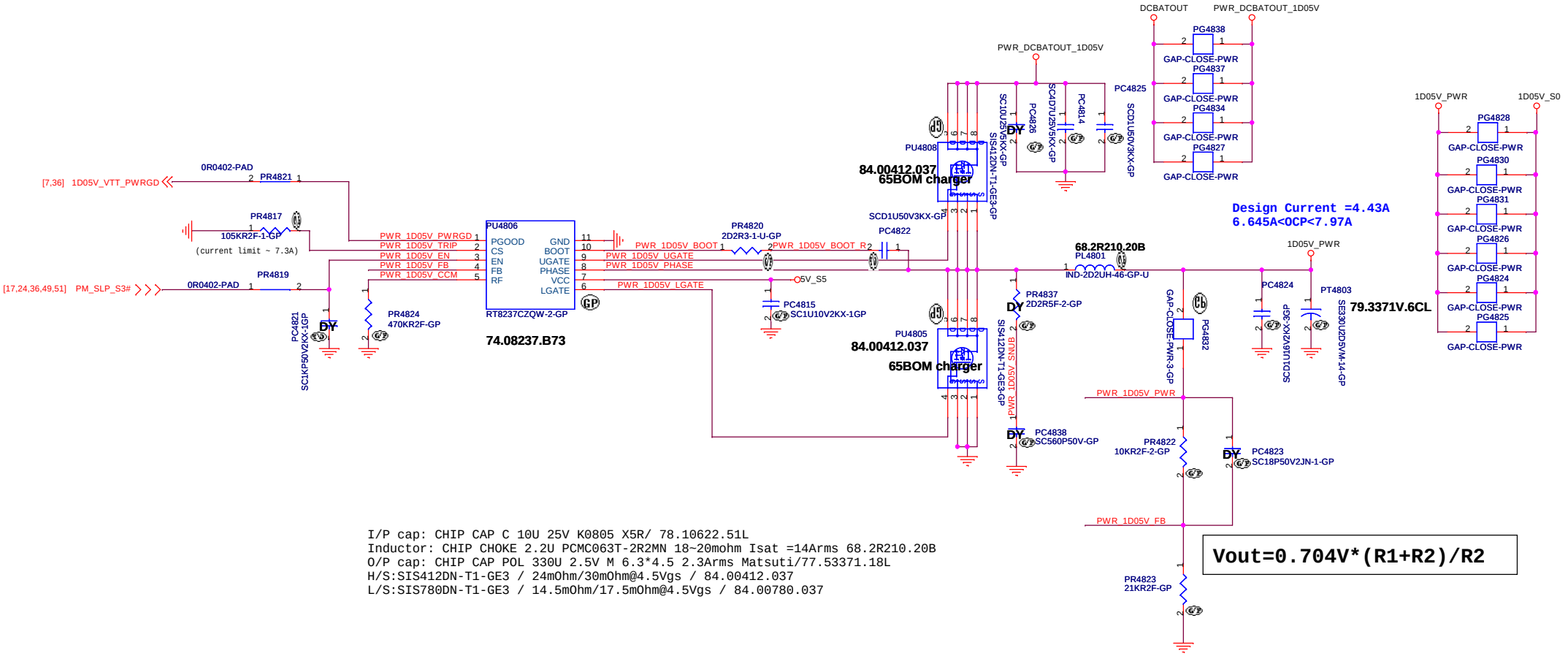
SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Vout=0.704V*(R1+R2)/R2

<Core Design>

Wistron Corporation
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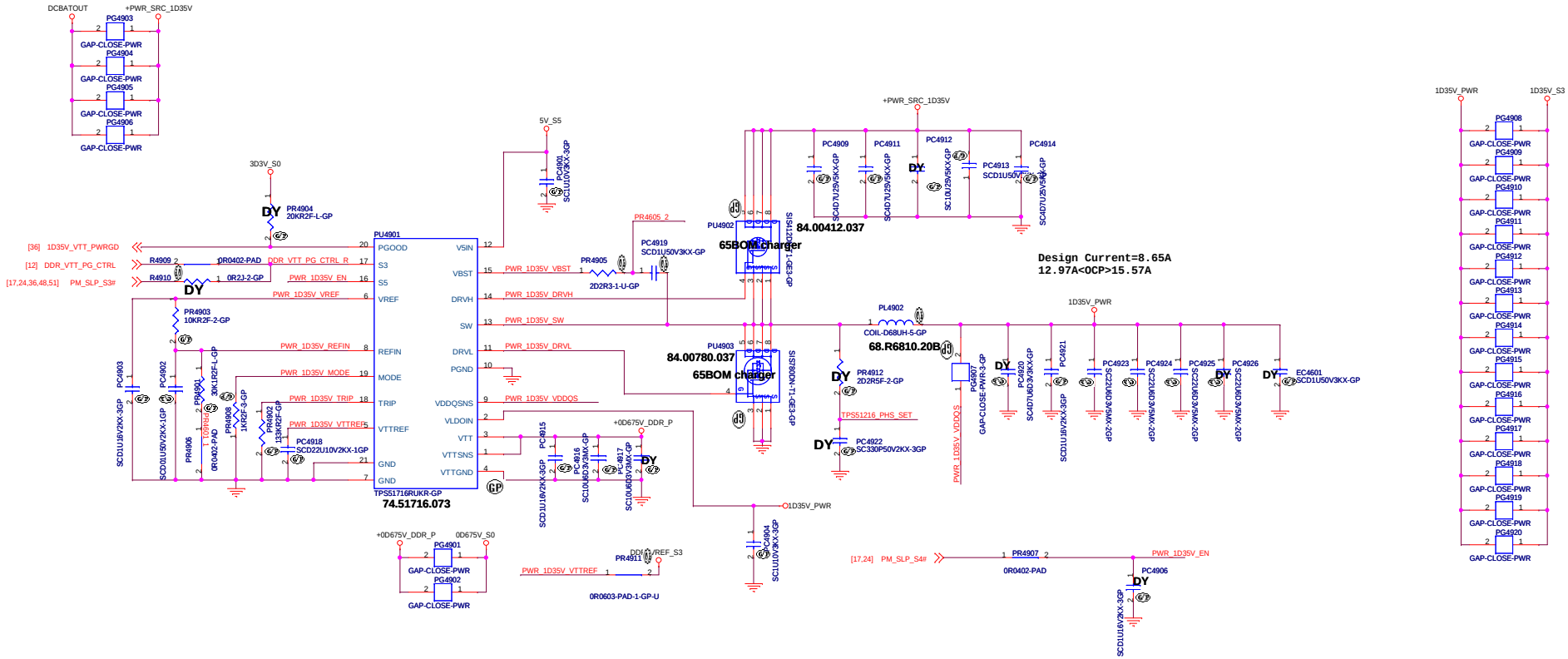
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8237_1D05V	
Size A3	Document Number Janus HSW 40/50/70	Rev A00
Date: Friday, February 07, 2014	Sheet 48 of 104	

SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5~1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
MOS: FET MOS FDMS3664S NC POWER56 / 84.03664.037 / Q1: 8.5~11mohm @Vgs=4.5V Q2: 2.6~3.2mohm @Vgs=4.5V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51716_1D35V_S3
Size: C
Document Number: Janus HSW 40/50/70
Rev: A00
Date: Monday, February 10, 2014
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(Blanking)

<Core Design>

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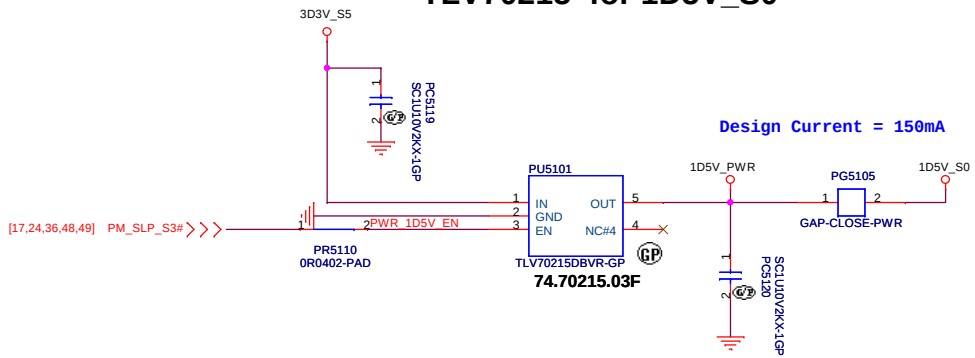
Title: Reserved

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

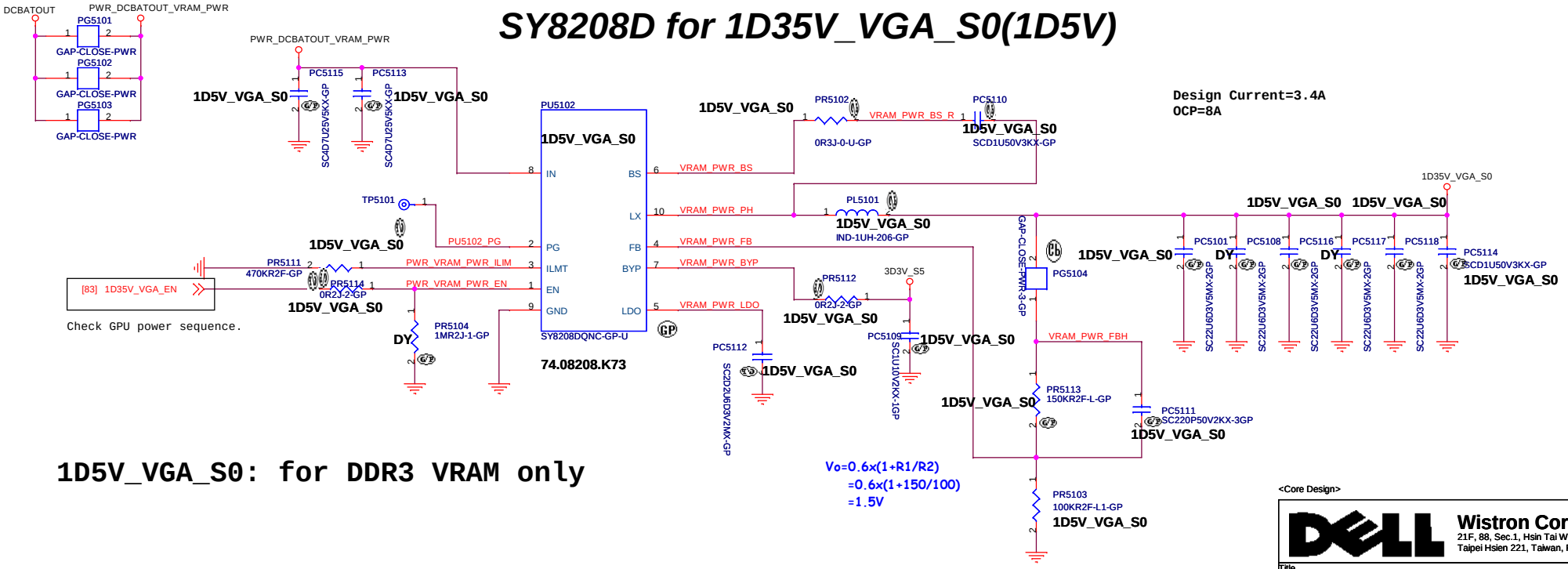
Date: Friday, February 07, 2014 | Sheet 50 of 104

SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



1D5V_VGA_S0: for DDR3 VRAM only

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TLV70215_1D5V / SY8208D_1D5V(VGA)

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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INVERTER POWER

CAM1

EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201

LCD1 — ACES-CON40-18-GP — 20.K0678.040

Trace width = 80mil

DCBATOUT_LCD, LCDVDD_LCD

C5201 SCD1U16V2KX-3GP
C5206 SC1U10V2KX-1GP

EE note: Never change R5211 to short pad after MP

R5211 0R5J-5-GP

DBC_EN_R — R5224 0R0402-PAD — DBC_EN [20]

F5201 800mA POLYSW-1D1A24V-2-GP 69.60040.001
C5205 SCD1U50V3KX-GP
C5202 SC33P50V2KX-1GP

LCD

DBC_EN_R
EDP_HPD_CONN
LCD_TST_C
EDP_AUX
EDP_AUX#
EDP_TX0#
EDP_TX0
EDP_TX1#
EDP_TX1
LCD_BRIGHTNESS
BLON_OUT_C
PANEL_SIZE_ID_CONN

Camera

DMIC_CLK_EDP
DMIC_DATA_EDP
MIC_GND
USB_CAMERA_EDP#
USB_CAMERA_EDP
3D3V_CAMERA_S0

Touch Panel

USB_PN6_TPNL
USB_PP6_TPNL
TP_RS
TP_RESET
OTPAN_VDD

R5201 0R0402-PAD — MIC_GND

TP_RS — R5205 0R0402-PAD — TOUCH_PANEL_INTR# [24]
C5208 SC10P50V2JN-4GP

TP_RESET — R5212 0R0402-PAD — PLT_RST# [17,24,30,36,58,65,73,96]
C5214 SC10P50V2JN-4GP

USB_PN6_TPNL — R5203 0R0402-PAD — USB_PN6 [16]

USB_PP6_TPNL — R5204 0R0402-PAD — USB_PP6 [16]

3D3V_S0 — R5208 10KR2J-3-GP
PANEL_SIZE_ID_CONN — R5210 100R2J-2-GP (For ESD) — PANEL_SIZE_ID — PANEL_SIZE_ID [20]
R5209 0R2J-2-GP

For AUDIO Grade B or C selection.

CCD1 — DM-ACES-CON8-44-GP-01 — ZZ.F2191.00801

3D3V_CAMERA_S0 — R5229 0R3J-0-U-GP — EC5210 SC33P50V2JN-3GP — C5207 SC4D7U6D3V3KX-GP

DMIC_CLK_C
DMIC_DATA_C
USB_CAMERA#
USB_CAMERA
CAM1_MIC_GND

R5207 0R2J-2-GP — CAM1_MIC_GND

RN5202 SRN33J-5-GP-U
DMIC_CLK_C — DMIC_CLK [27]
DMIC_DATA_C — DMIC_DATA [27]
EC5205 SC68P50V2JN-2GP
EC5206 SC68P50V2JN-2GP

RN5204 SRN33J-5-GP-U
DMIC_CLK_EDP
DMIC_DATA_EDP
CAM_EDP

Layout Note: Reduce the stubs.

TRS208 FILTER-4P-6-GP — 69.10103.041
USB_CAMERA# — USB_PN4 CAM# — RN5205 SRN0J-6-GP — USB_PN4 [16]
USB_CAMERA — USB_PP4 CAM — USB_PP4 [16]

TRS209 FILTER-4P-6-GP — 69.10103.041
USB_CAMERA_EDP# — USB_PN4 EDP — RN5206 SRN0J-6-GP — USB_PN4 [16]
USB_CAMERA_EDP — USB_PP4 EDP — USB_PP4 [16]
CAM_EDP

Layout Note: Reduce the stubs.

RN5203 SRN100KJ-5-GP
BKLT_CTRL
BLON_OUT_C
EDP_HPD

RN5201 SRN100J-4-GP
LCD_TST_C
LCD_BRIGHTNESS
BLON_OUT_C
BKLT_CTRL — LCD_TST [24]
BLON_OUT [24]

R5222 0R2J-2-GP — D5202 BAT54C-7-F-3-GP — eDP_BKLT_CTRL — EC_BRIGHTNESS [24]

EC (BIST MODE)
75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D
4th = 83.R2003.V81

EDP_HPD_CONN — 100R2J-2-GP — R5233 — EDP_HPD [15]

3D3V_S0 — R5231 0R2J-2-GP
5V_S0 — R5230 0R0603-PAD-1-GP-U
TPAN_VDD_F — R5232 0R3J-0-U-GP
TPAN_VDD — R5203 69.60040.001 POLYSW-1D1A24V-2-GP

EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201

LCDVDD

[15] EDP_VDD_EN — D5201 BAT54C-7-F-3-GP — LCDVDD_EN
[24] LCD_TST_EN — R5202 100KR2J-1-GP — LCDVDD

75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D
4th = 83.R2003.V81

Layout Note:
Trace width = 80mil

3D3V_S0 — C5204 SC4D7U6D3V3KX-GP
US201 RT9724GB-GP — 74.09724.09F
EN, GND, VOUT, VIN#5, VIN#4

Brightness

[15] L_BKLT_CTRL — R5206 0R0402-PAD — eDP_BKLT_CTRL

AFTP5203 LCD_BRIGHTNESS
AFTP5205 BLON_OUT_C
AFTP5207 LCD_TST_C
AFTP5206 EDP_AUX
AFTP5208 EDP_AUX#
AFTP5213 EDP_TX0#
AFTP5210 EDP_TX0
AFTP5211 EDP_TX1#
AFTP5212 EDP_TX1
AFTP5222 DMIC_CLK_C
AFTP5228 DMIC_DATA_C
AFTP5225 USB_CAMERA#
AFTP5226 USB_CAMERA
AFTP5227 3D3V_CAMERA_S0

AFTP5201 EDP_HPD_CONN
AFTP5202 LCDVDD_LCD
AFTP5204 DCBATOUT_LCD
AFTP5209 TP_RS
AFTP5214 TP_RESET

[8] EDP_TX0_DN — C5203 SCD1U16V2KX-3GP — EDP_TX0#
[8] EDP_TX0_DP — C5210 SCD1U16V2KX-3GP — EDP_TX0
[8] EDP_TX1_DN — C5211 SCD1U16V2KX-3GP — EDP_TX1#
[8] EDP_TX1_DP — C5213 SCD1U16V2KX-3GP — EDP_TX1
[8] EDP_AUX_DN — C5209 SCD1U16V2KX-3GP — EDP_AUX#
[8] EDP_AUX_DP — C5212 SCD1U16V2KX-3GP — EDP_AUX

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter CONN
Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00
Date: Monday, February 10, 2014 | Sheet 52 of 104

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A3	*Janus HSW 40/50/70*	*A00*

Date: Friday, February 07, 2014 Sheet 53 of 104

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Janus HSW 40/50/70	X02

Date: Friday, February 07, 2014 Sheet 54 of 104

CRT Board Connector

CRT1
D-SUB 15P
D-SUB-15-252-GP
020.20020.0015

CRT RGB
CRT H/VSYNC
CRT SMBUS

F5501 POLYSW-1D1A6V-9-GP-U
D5501 RB551V30-GP
83.R5003.H8H
69.48001.081
2ND = 69.50011.081
3RD = 69.50013.101

U5501D U5501C U5501A U5501B
TC74VHCT125AFTQK2M-GP

Hsync & Vsync level shift

L5503 L5501 L5502 BLM18BB220SN-GP
68.00084.A11
2nd = 68.00245.011

RN5501 SRN2K2J-1-GP
RN5502 SRN0J-6-GP
R5511 R5507 33R2J-2-GP

Layout note:
All cap need close to chip

U5502
RTD2168-CGT-GP
071.02168.0003

CRT DEBUG
CAT24C128WI-GT3-GP
72.24128.J01

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

1	0	1	0	A_2	A_1	A_0	R/W

DEVICE ADDRESS

Figure 3. Slave Address Bits

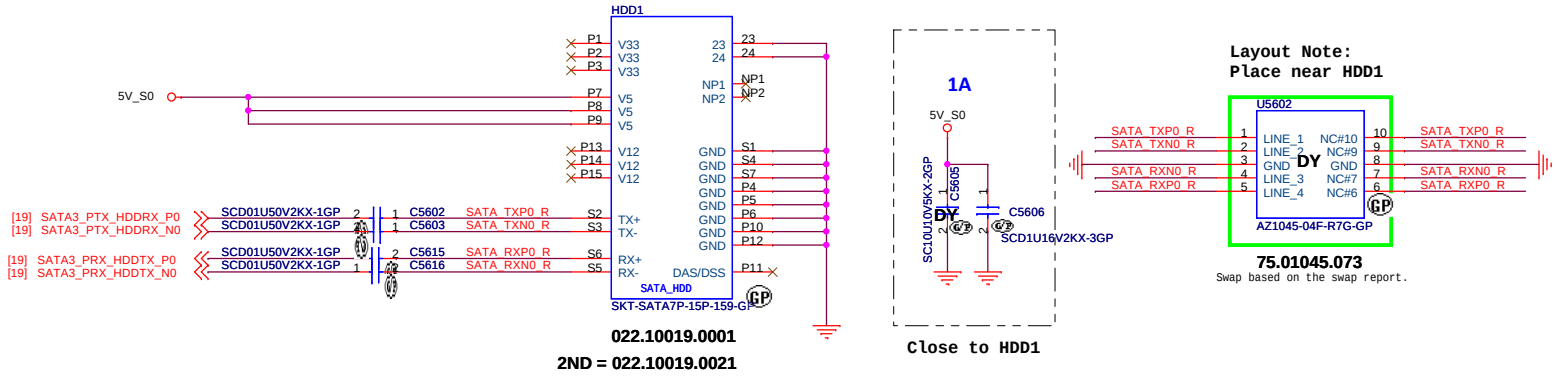
	POL1_SDA(PIN22) 0	POL1_SDA(PIN22) 1
POL2_SCL(PIN23) 0	X	EP MODE
POL2_SCL(PIN23) 1	ROM ONLY MODE	EEPROM MODE

	LDO_EN(PIN21) 0	LDO_EN(PIN21) 1
	VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: (Reserved)DP to VGA Converter
Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: X02
Date: Friday, February 07, 2014 | Sheet 55 of 104

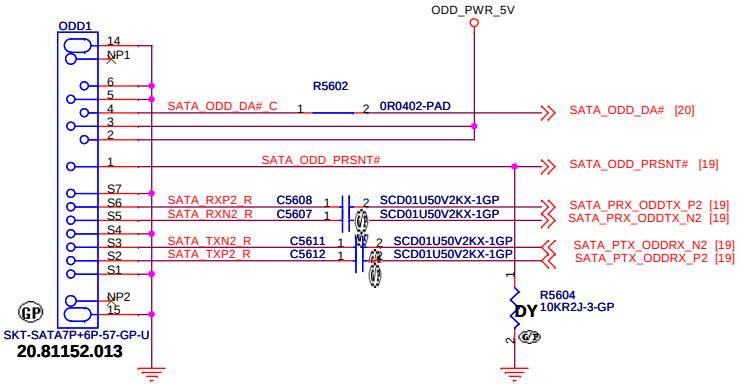
SSID = SATA

SATA HDD Connector

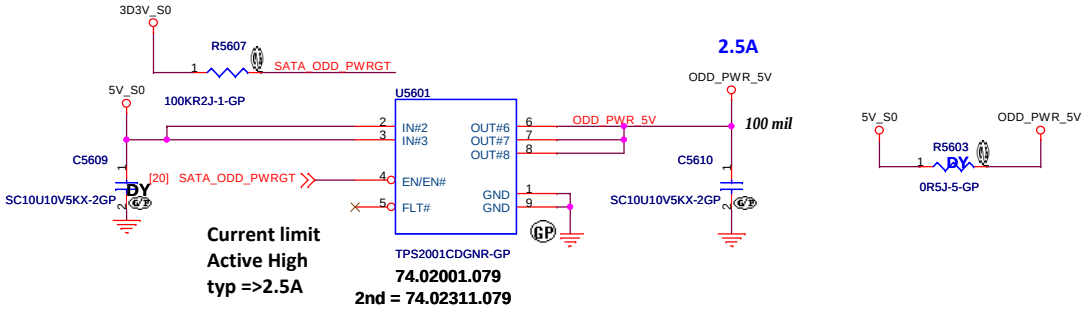


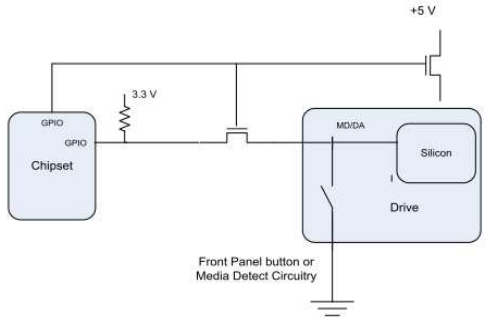
ME Note: New HDD conn symbol is not ready,
we will use original OAK HDD conn (22.10300.991) and shift to the correct position.

ODD Connector



SATA Zero Power ODD





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 56 of 104

SSID = ESATA

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<Core Design>

Wistron Corporation
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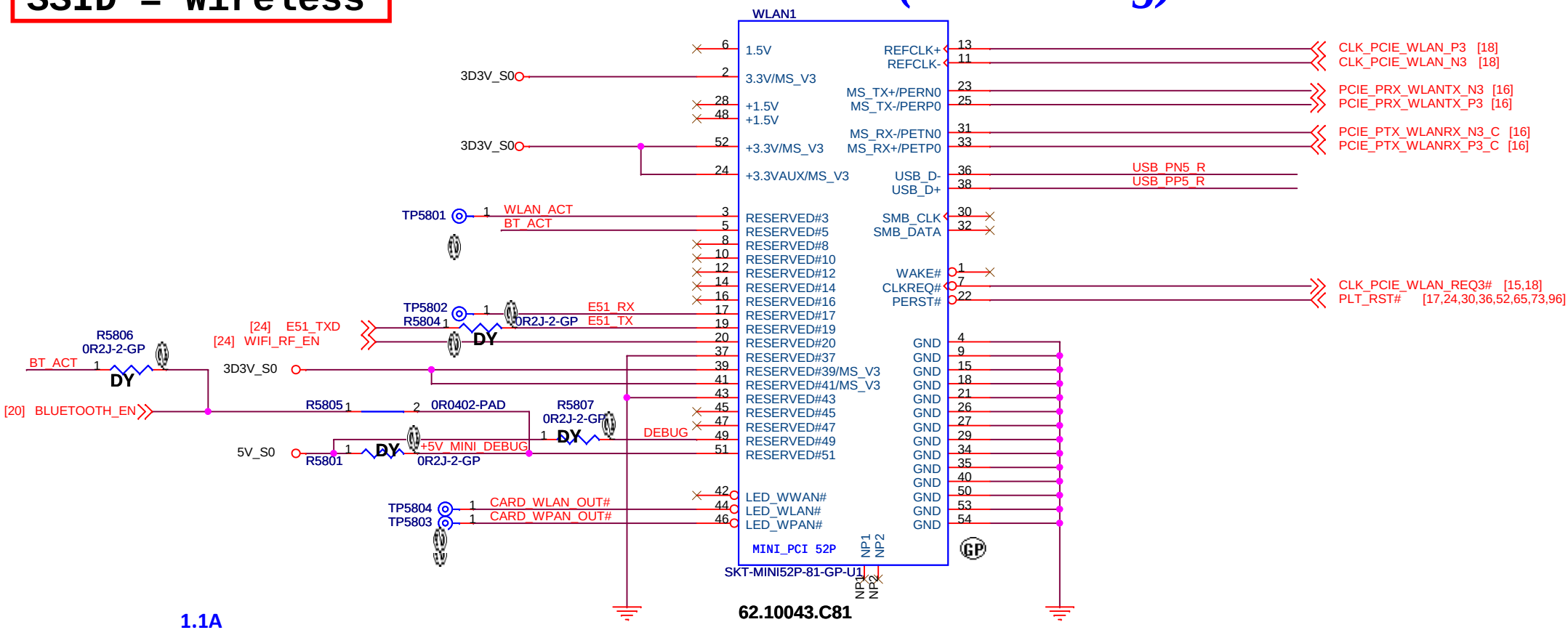
Taipei Hsien 221, Taiwan, R.O.C.

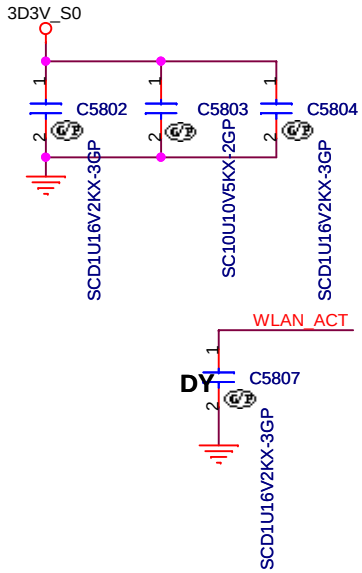
Title: ESATA		
Size: A3	Document Number: Janus HSW 40/50/70	Rev: A00
Date: Friday, February 07, 2014	Sheet 57 of 104	

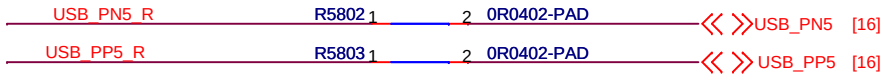
SSID = Wireless

Mini Card Connector(802.11a/b/g)



1.1A





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card (WLAN)

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 58 of 104

(Blanking)

<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 59 of 104

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

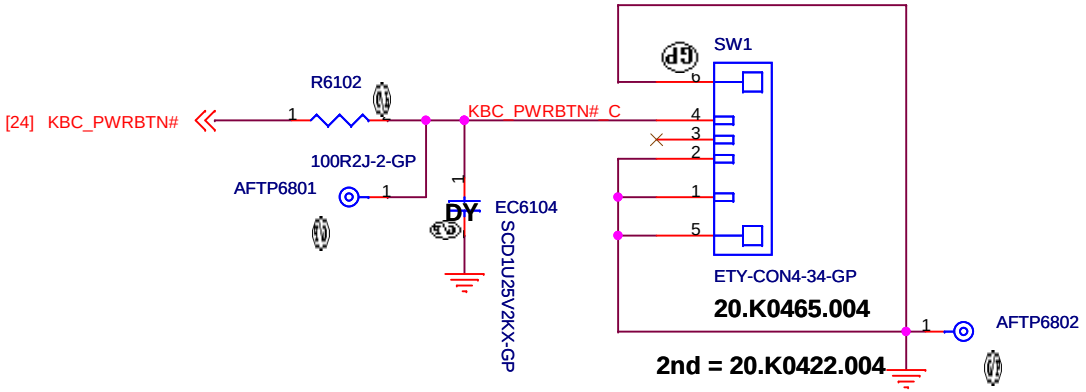
Title: *(Reserved)*

Size	Document Number	Rev
A4	*Janus HSW 40/50/70*	*A00*

Date: Friday, February 07, 2014 Sheet 60 of 104

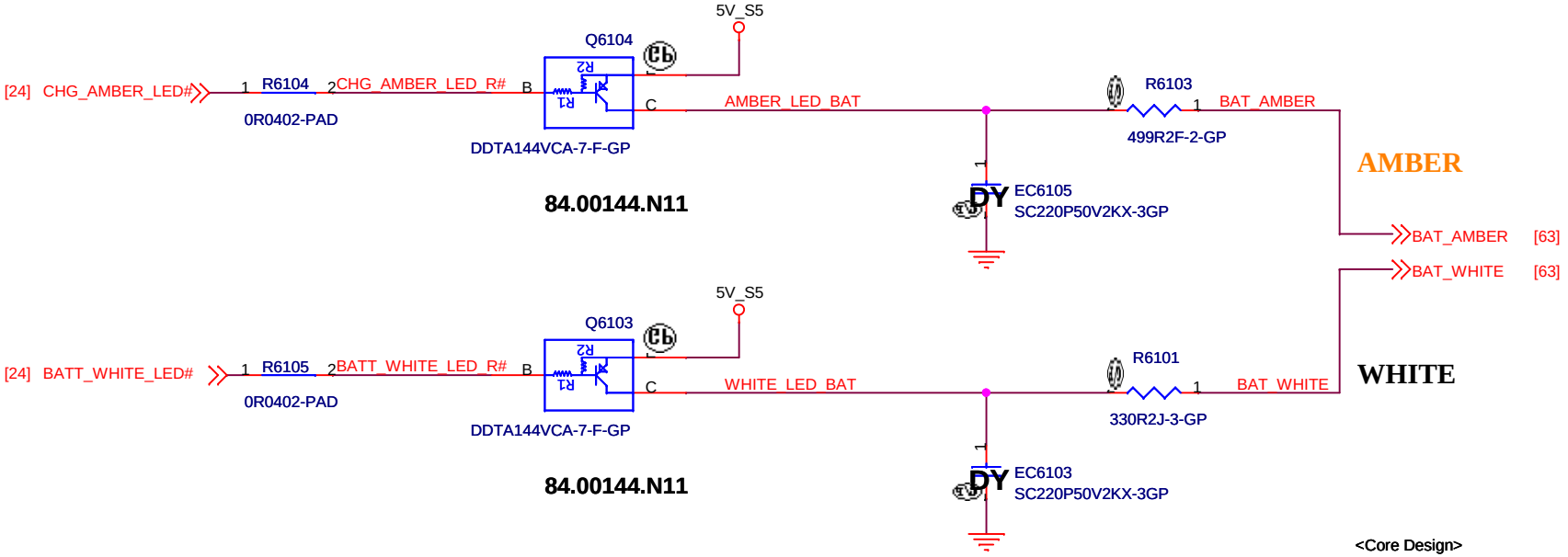
SSID = User.Interface

Power button



Battery LED1 (AMBER_LED)

Low actived from KBC GPIO



Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

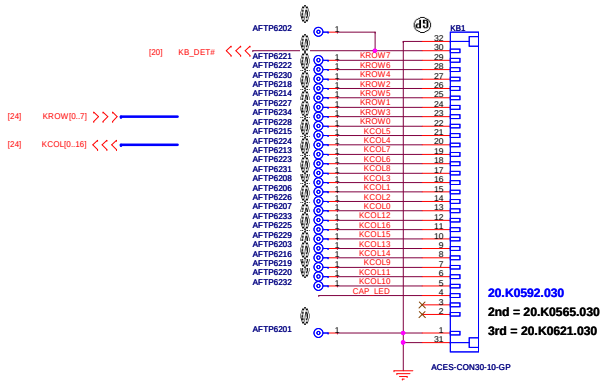
Title: LED Bard/Power Button

Size	Document Number	Rev
A4	Janus HSW 40/50/70	A00

Date: Friday, February 07, 2014 Sheet 61 of 104

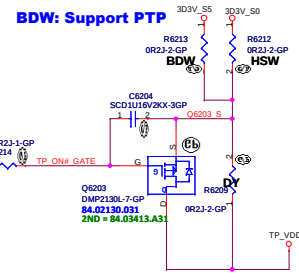
SSID = KBC

Internal Keyboard Connector (DVC40)



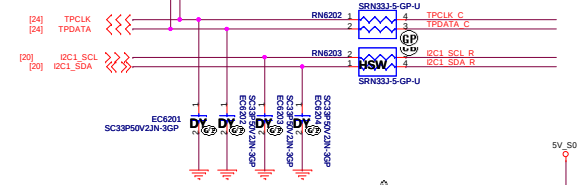
SSID = Touch.Pad

BDW: Support PTP

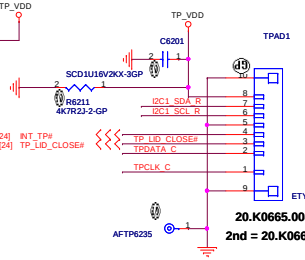


PS2

I2C



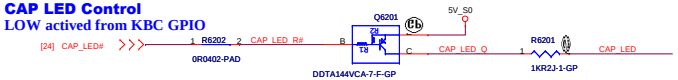
Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

CAP LED Control

LOW actived from KBC GPIO

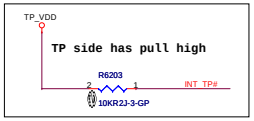


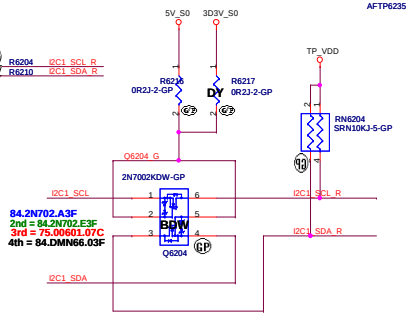
84.00144.N11

SMBUS

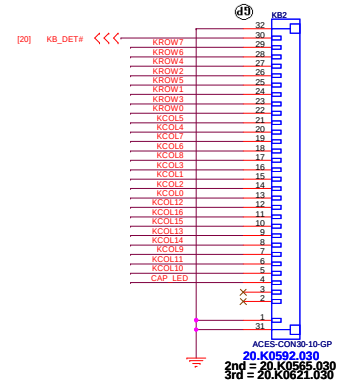
Need to check with SW.

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

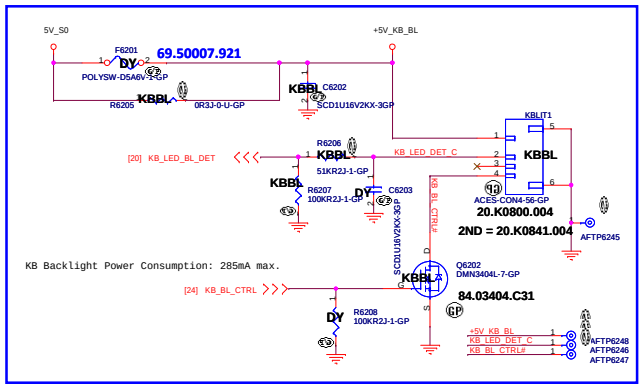




Internal Keyboard Connector (DVC50/DVC70)



Keyboard Backlight (DVC70)



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Title: Key Board/Touch Pad

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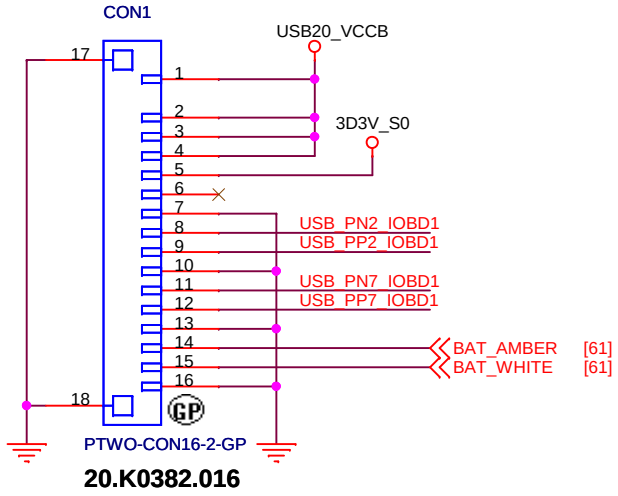
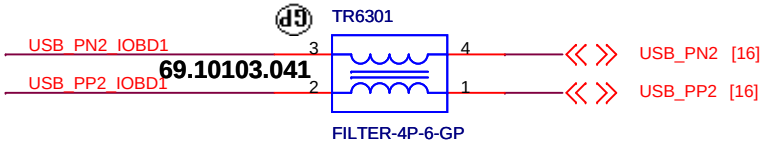
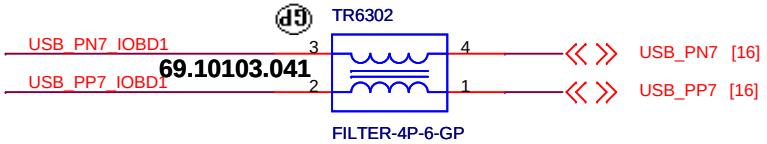


USB2.0 Port3

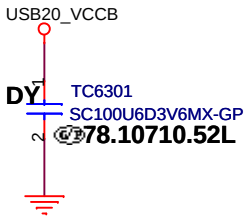
Card Reader

LED





The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



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Title: ***IO Board Connector***

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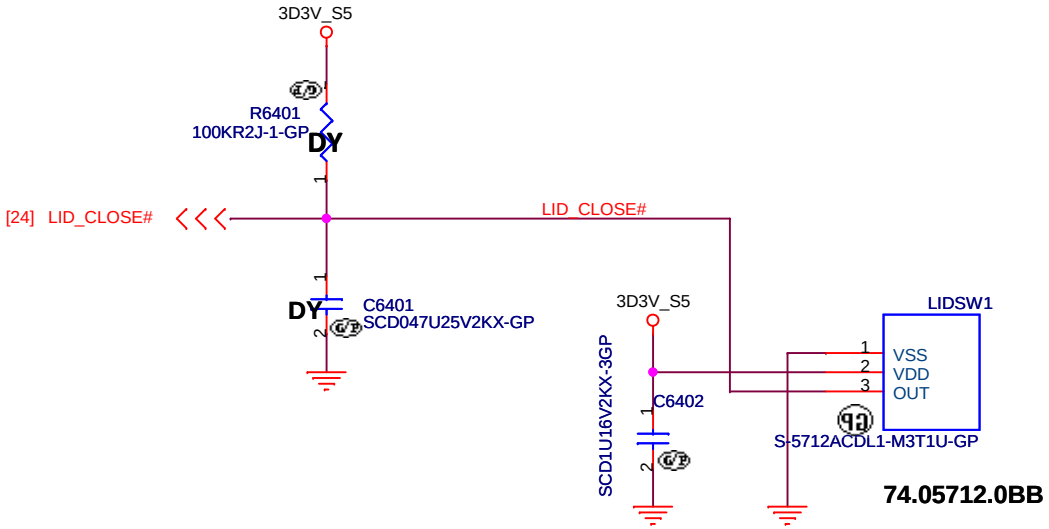
SSID = User.Interface



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Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***Janus HSW 40/50/70***	***A00***

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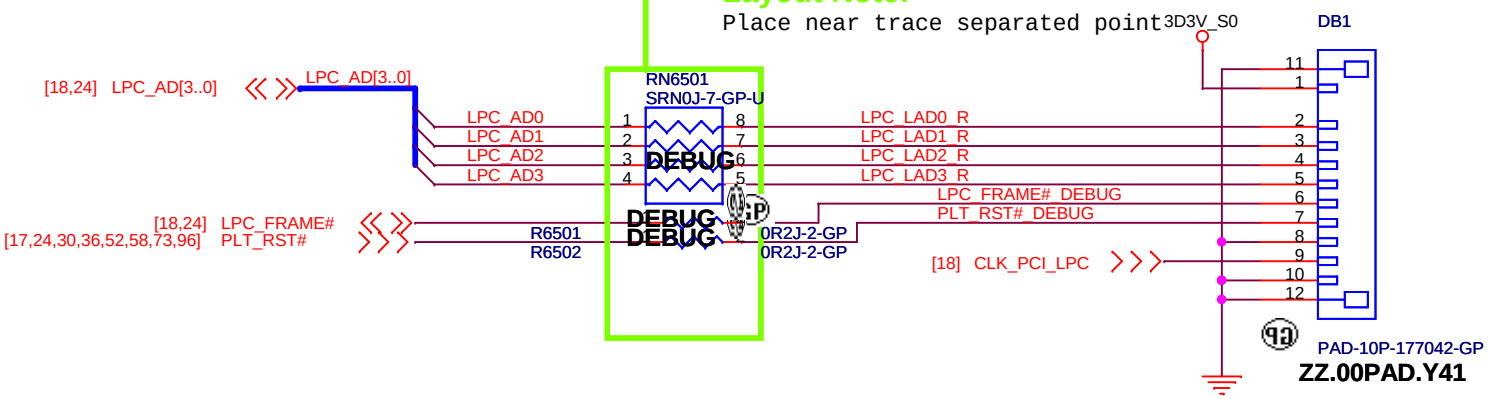
SSID = DEBUG PORT

Debug Connector

Layout Note:
Place near trace separated point



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

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Title: *Dubug connector*		
Size: A4	Document Number: *Janus HSW 40/50/70*	Rev: *A00*
Date: Friday, February 07, 2014	Sheet 65 of 104	

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Title

Reserved

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Title: *Reserved*

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Title: USB3.0 PORT

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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Title: Reserved

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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Title: Reserved

Size	Document Number	Rev
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Date: Friday, February 07, 2014 Sheet 71 of 104

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Title: Reserved

Size	Document Number	Rev
A3	Janus HSW 40/50/70	A00

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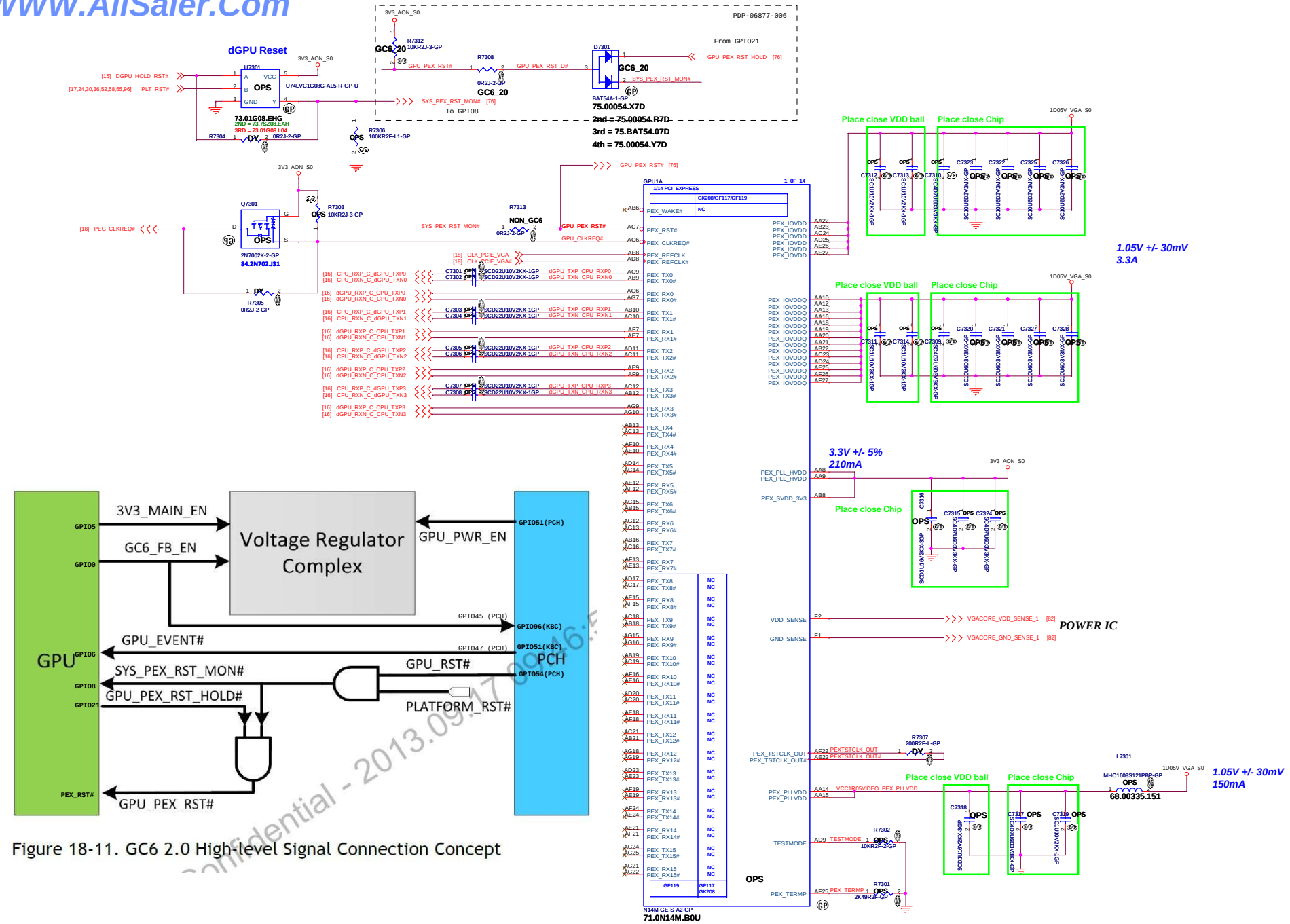

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

N15V-GM-S-A2: 071.0N15V.0A0U
N15V-GM-S is GF117.
N15S-GT is GM108.

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Title: GPU_PCIE/STRAPPING(1/5)

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

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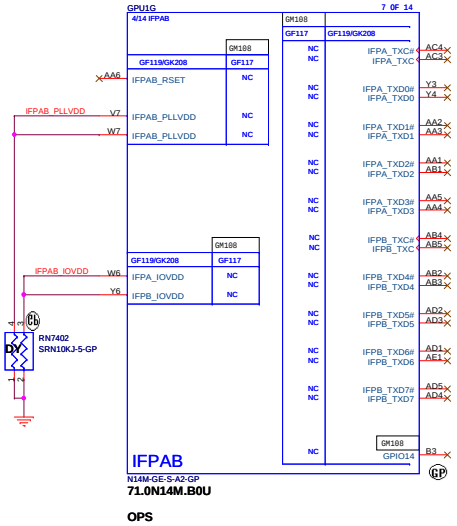
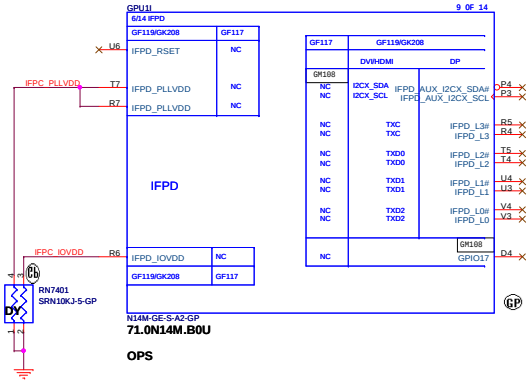
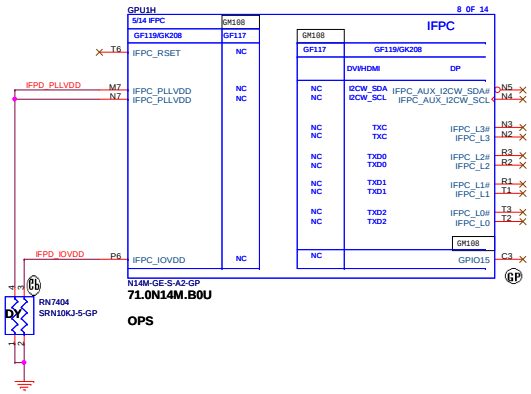
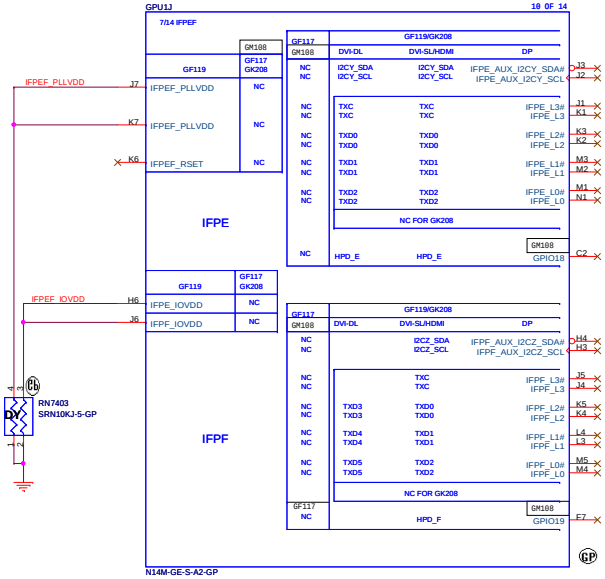
LVDS Interface





HDMI Interface





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Title: GPU Memory(2/5)

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

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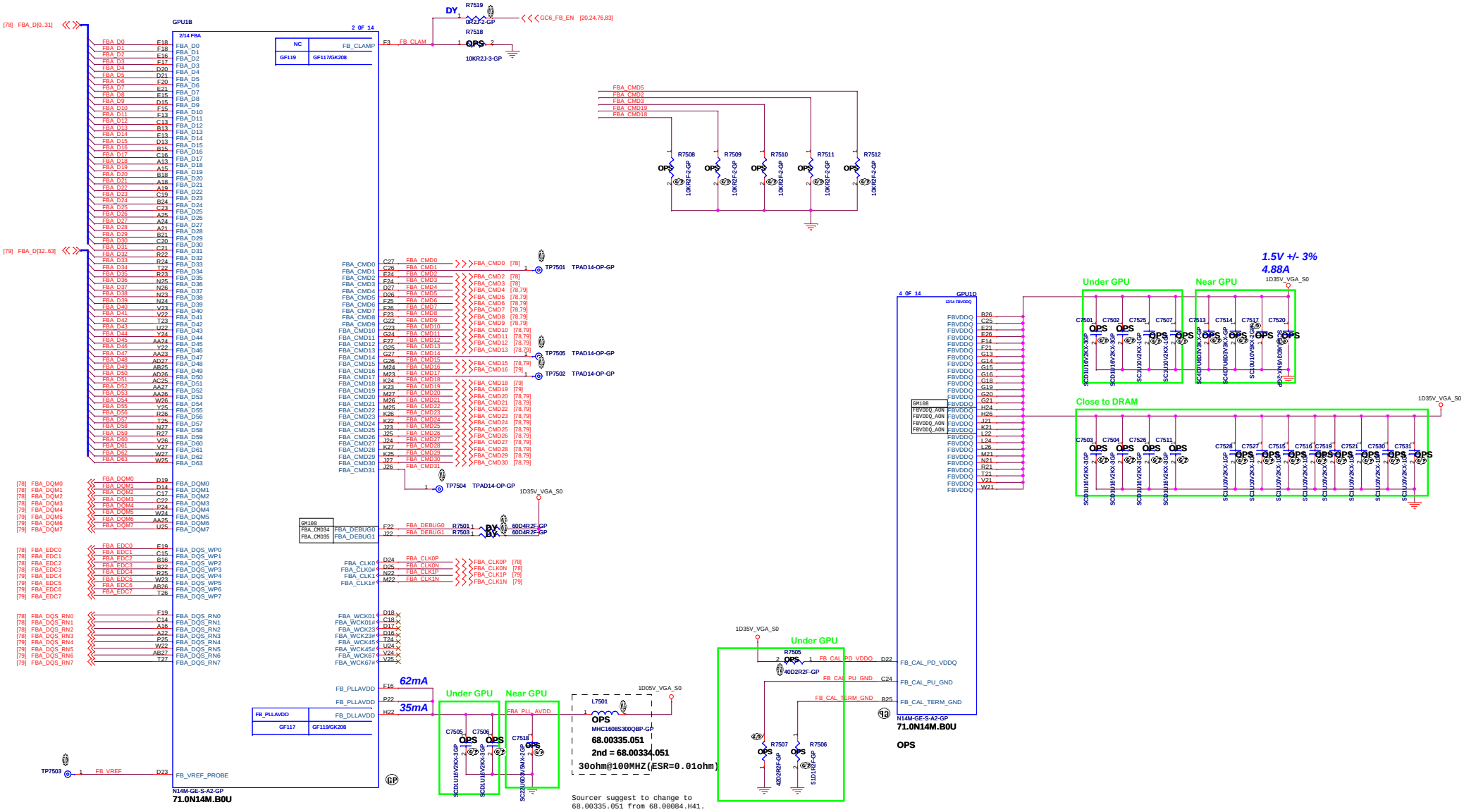


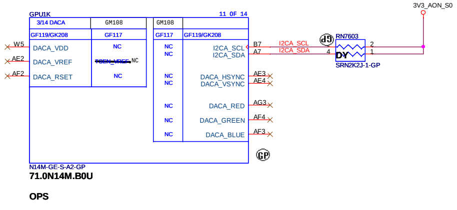
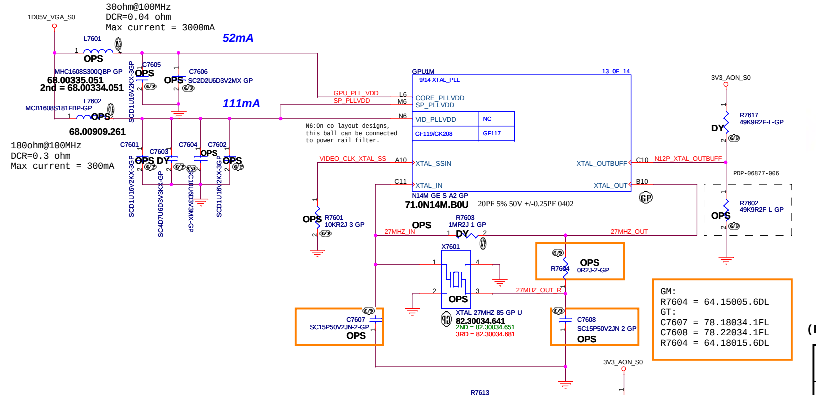


Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05)		0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	SP_PLLVDD = VID_PLLVDD	0.1 µF	X7R	0402	1 per ball	Under GPU
		4.7 µF	X5R	0603	1	Near GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)		0603	1	Near GPU



Straps

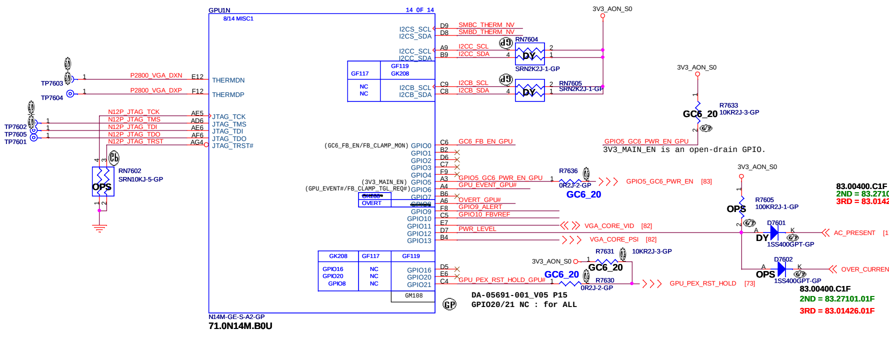
(DS-06814-001)

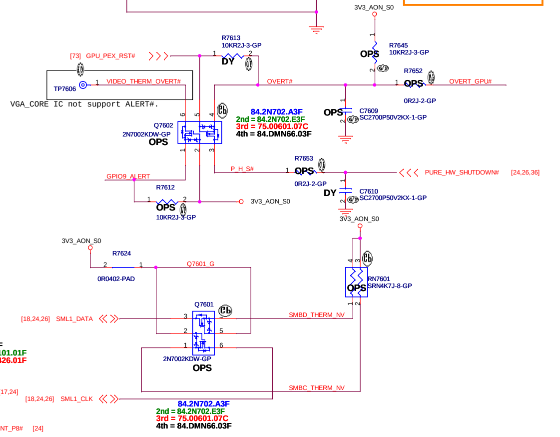
Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VENDOR	10kΩ	•Pull-up to 3V3 if VBIOS ROM exists •Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

(RVL-06891-001)N15V- GM -S DDR3L Recommended Memories

		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1





(DS-06814-001)

Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	N15S-GV	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	N15S-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	All GB2-64 N14 and GB2B-64 N15	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	N15S-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	N15S-GM/-GT	DEVID_SEL	PCIE_CFG		
STRAP0	N15S-GV	USER[3]	USER[2]	USER[1]	USER[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)			
STRAP1	N15S-GV	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP2	N15S-GV	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP3	N15S-GV	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	N15S-GV	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

(RVL-06891-001)N15V- GT -S DDR3L Recommended Memories

		Strap	
128Mx16 DDR3L	Hynix	0x9	H5TC2G63FFR-11C
	Micron	0xA	MT41K128M16JT-107G:K
	Samsung	0xB	K4W2G1646E-BY11
256Mx16 DDR3L	Hynix	0x3	H5TC4G63AFR-11C
	Micron	0x4	MT41K256M16HA-107G:E
	Samsung	0x5	K4W4G1646D-BC1A

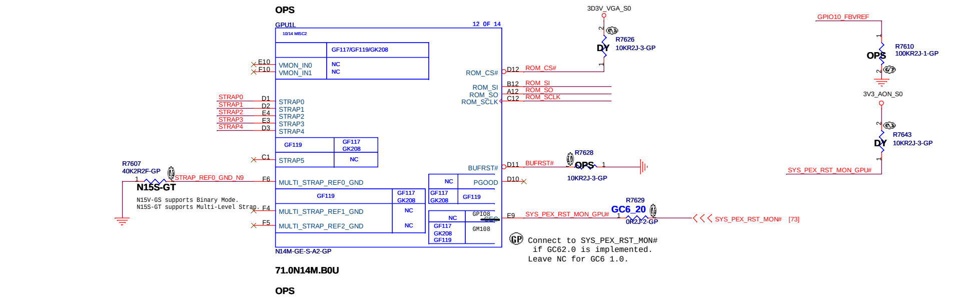
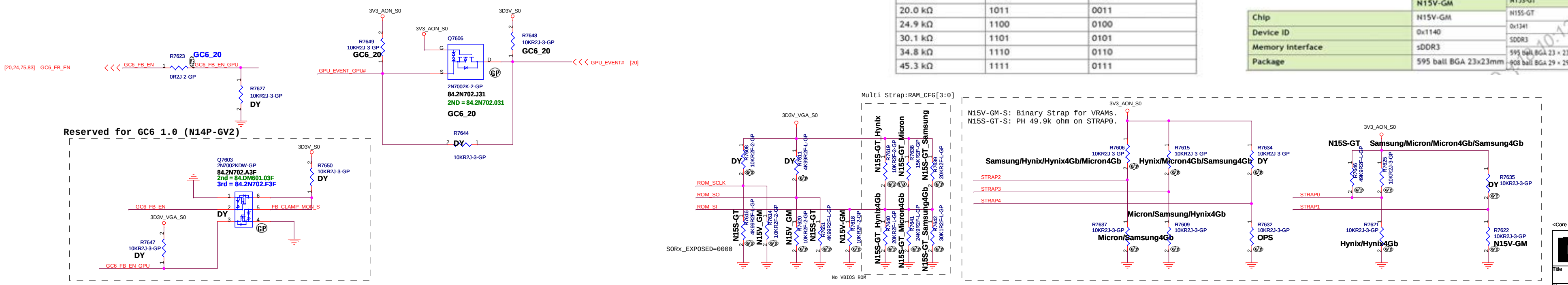


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

	NPN-06912 N15V-GM	NPN-06975 N15S-GT
Chip	N15V-GM	N15S-GT
Device ID	0x1140	0x1341
Memory interface	sDDR3	SDDR3
Package	595 ball BGA 23x23mm	595 ball BGA 23 × 23 mm 908 ball BGA 29 × 29 mm



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Title	GPU_POWER(4/5)
Size: Custom	Document Number: Janus HSW 40/50/70
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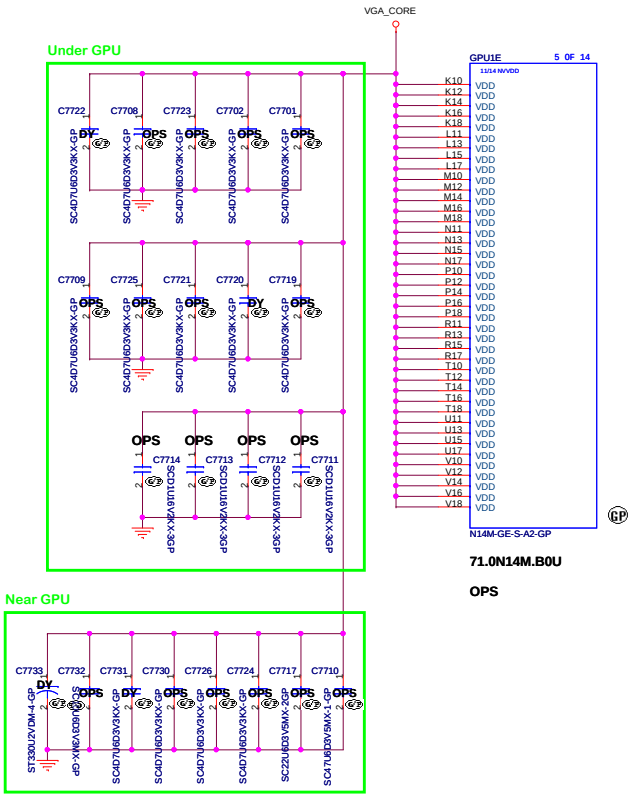
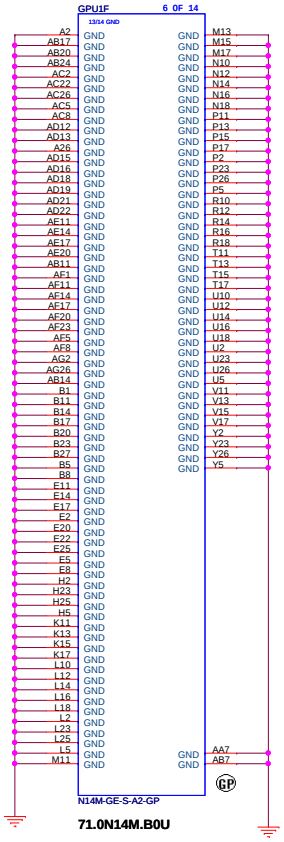
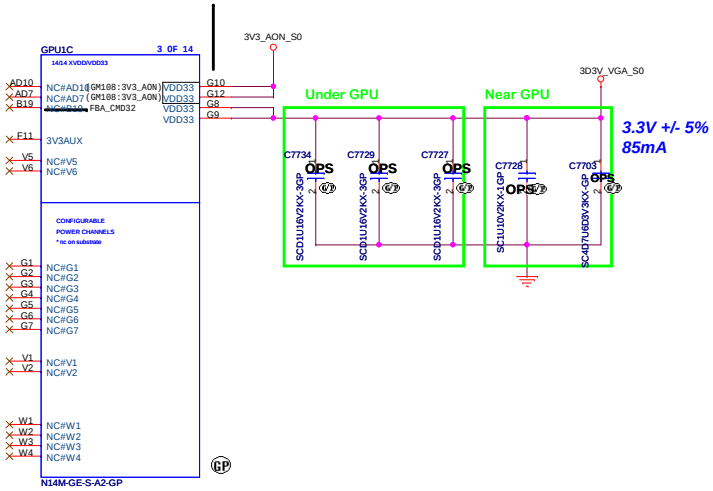
Date: Monday, February 10, 2014	Sheet 76 of 104





G10,G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.



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Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
Custom	Janus HSW 40/50/70	A00

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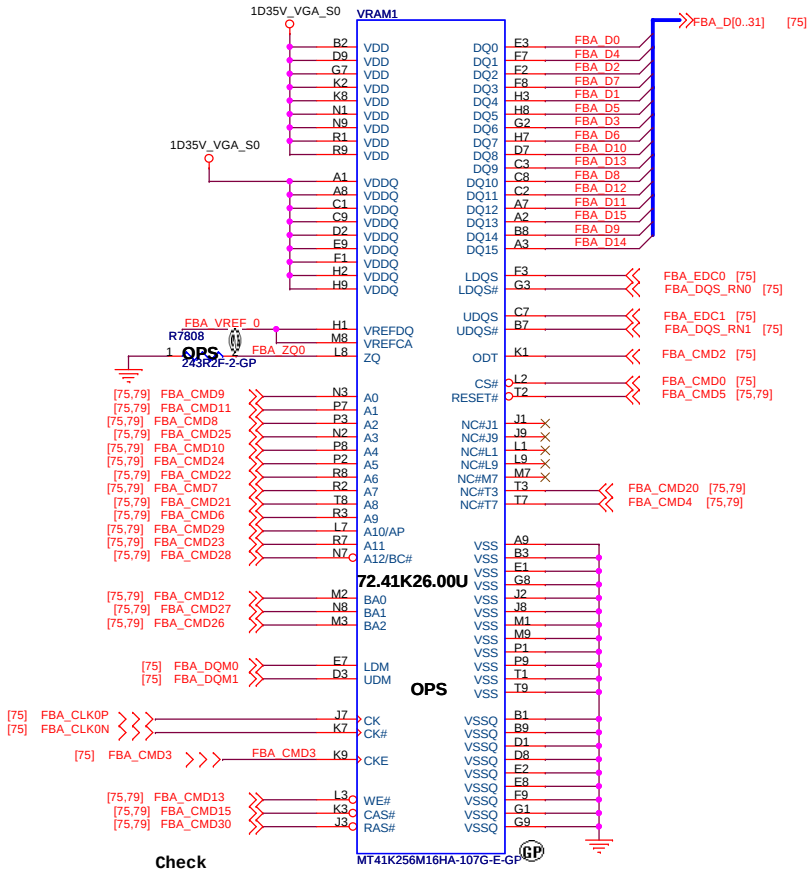
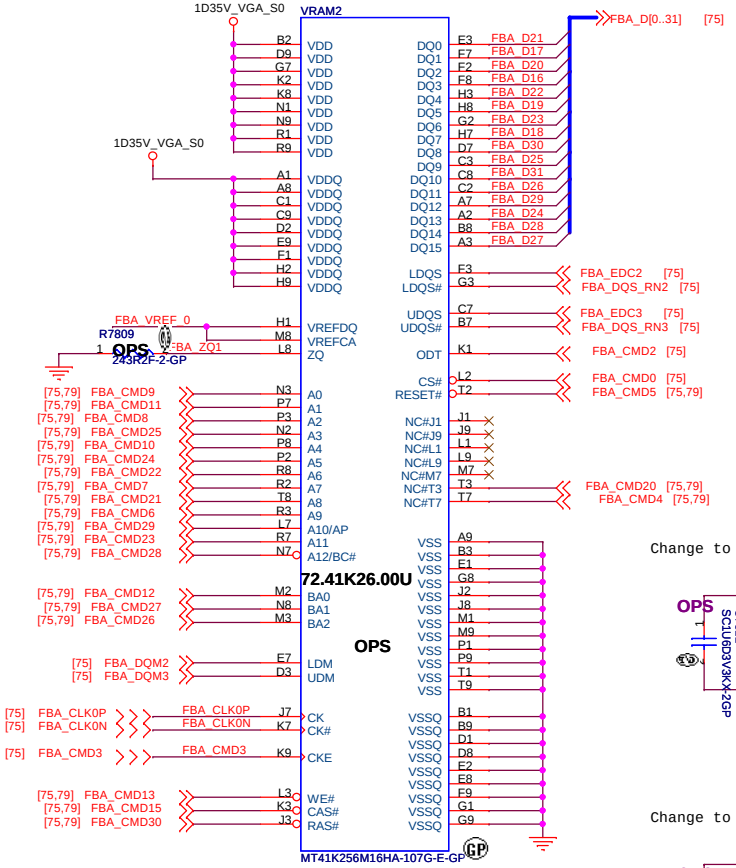
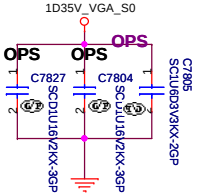
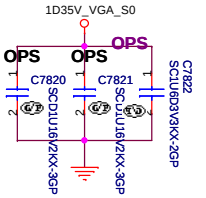




Place close VRAM1 VDD ball

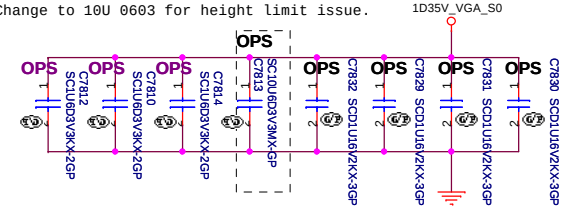


Place close VRAM2 VDD ball



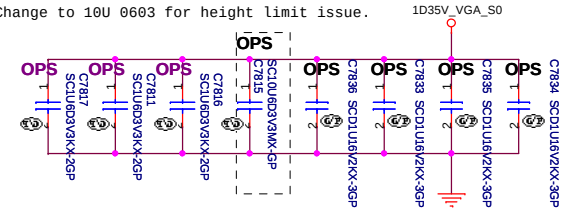
Place close VRAM1VDDQ ball

Change to 10U 0603 for height limit issue.

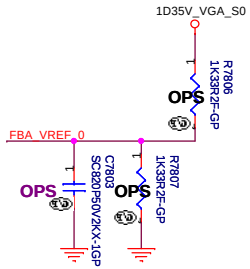


Place close VRAM1VDDQ ball

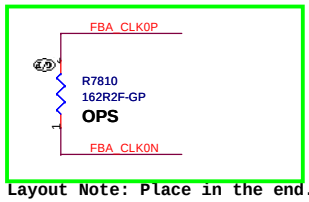
Change to 10U 0603 for height limit issue.



Frame Buffer Patition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

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Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

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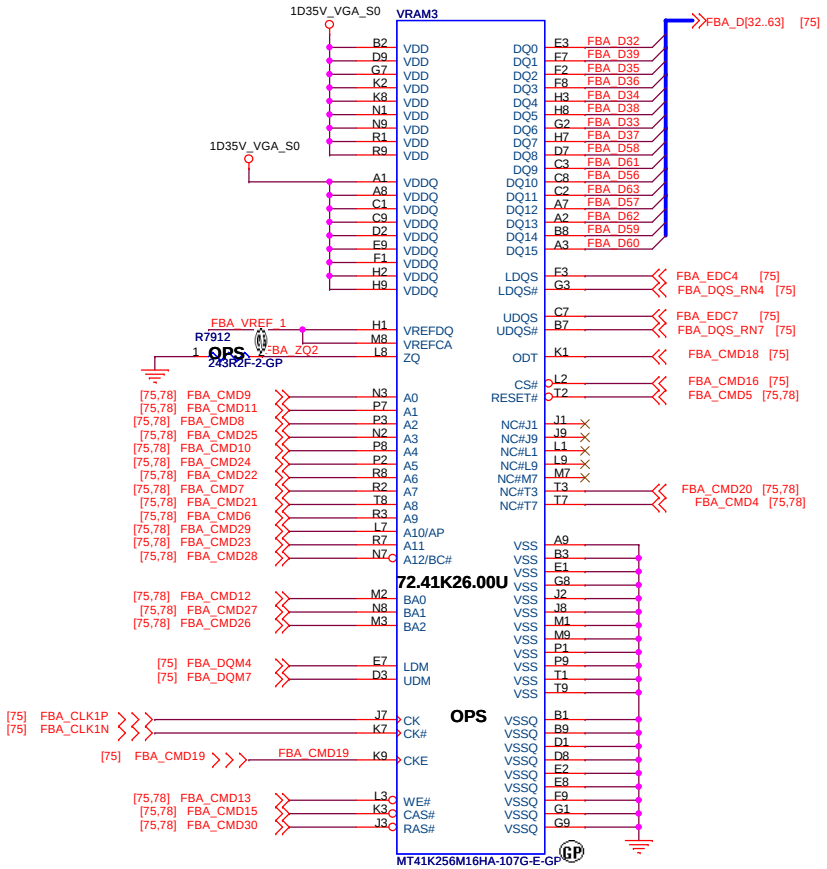
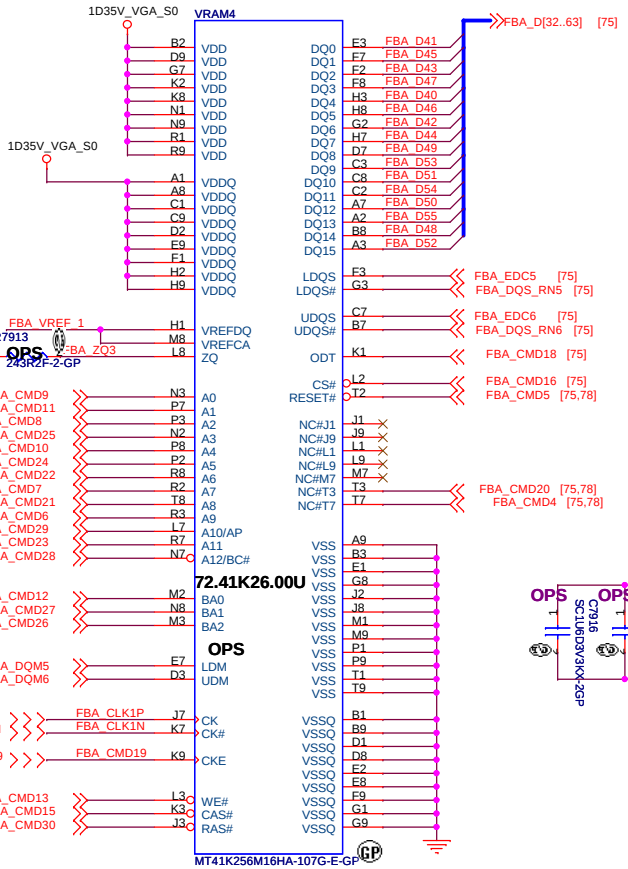
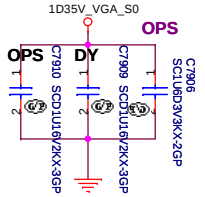
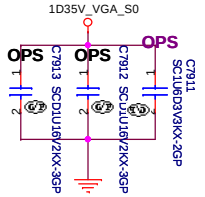




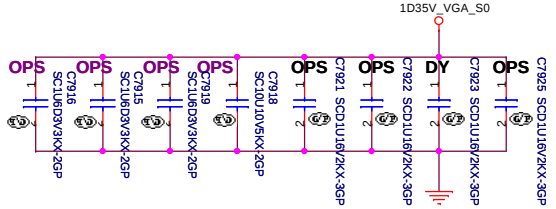
Place close VRAM3 VDD ball



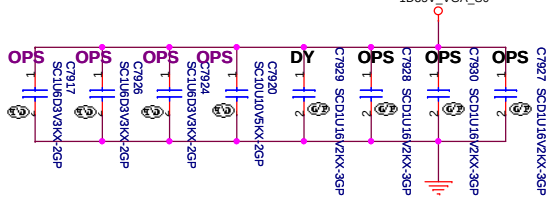
Place close VRAM4 VDD ball



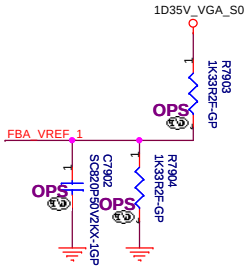
Place close VRAM3 VDDQ ball



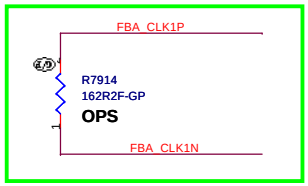
Place close VRAM4 VDDQ ball



Frame Buffer Patition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
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Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
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Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
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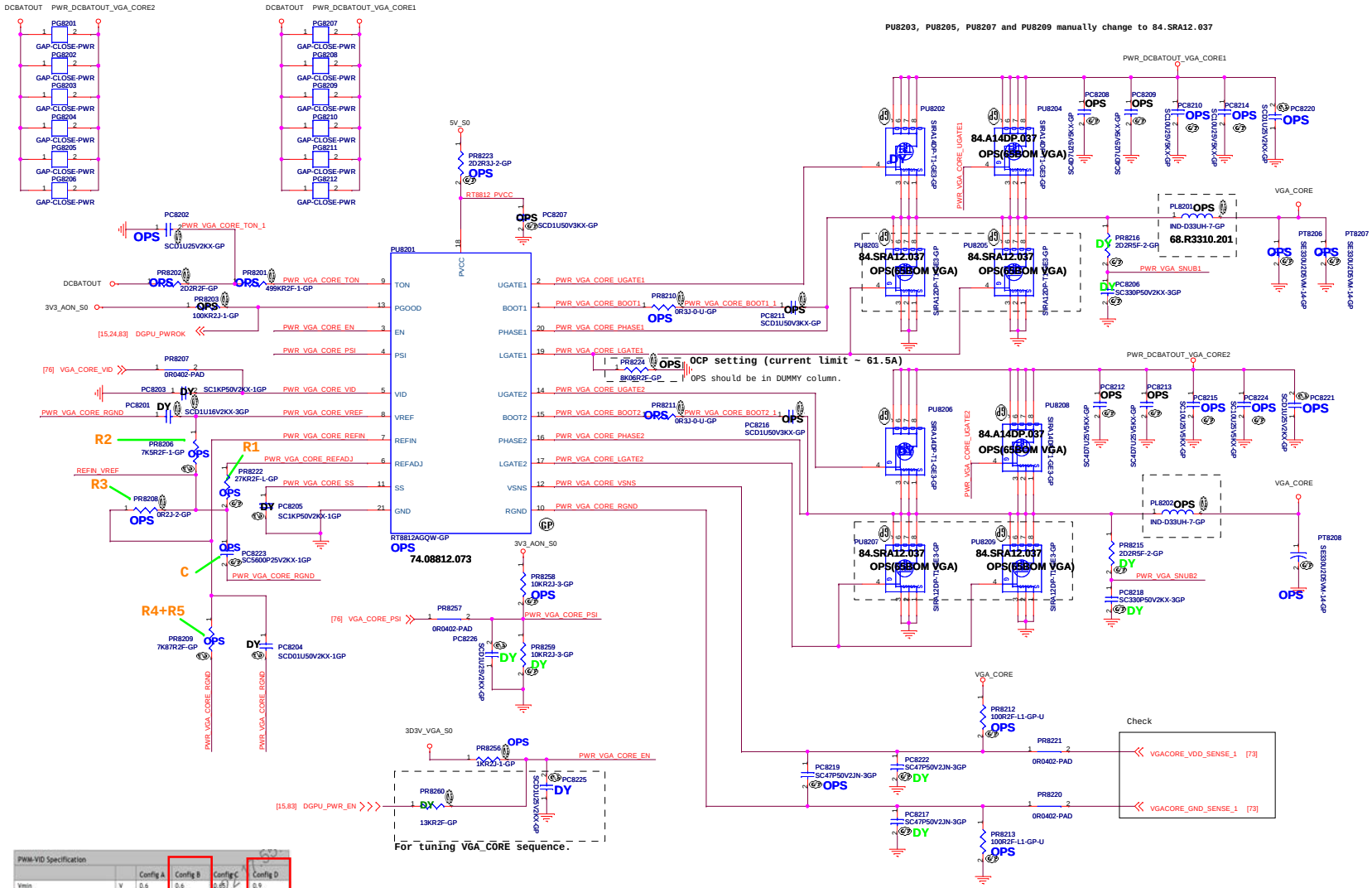

N15V_GM_S
Config D

Design Current=33.5A
56.65A <OCP< 66.7A

Component value	N15V-GM-S Config D	N15-S-GT-S Config B
R1 (PR8222)	27K 64.27025.6DL	29K 64.29025.6DL
R2 (PR8206)	7.5K 64.75815.6DL	28K 64.29025.6DL
R3 (PR8208)	0 63.R0034.1DL	2K 64.20015.6DL
R4+R5 (PR8209)	7.87K 64.78715.6DL	18K 64.18025.6DL
C (PC8223)	5.6nF 78.56222.2FL	2.7nF 78.27224.2FL

PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	0.676	0.676	0.676
PWM Minimum Pulse Width T_{pwm}	ns	9.26	9.26	74	74
VID Transient Time T		<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	30	39	27
R2 (1%)	KΩ	39	30	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S:SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06.037

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Title: RT8812 VGACORE

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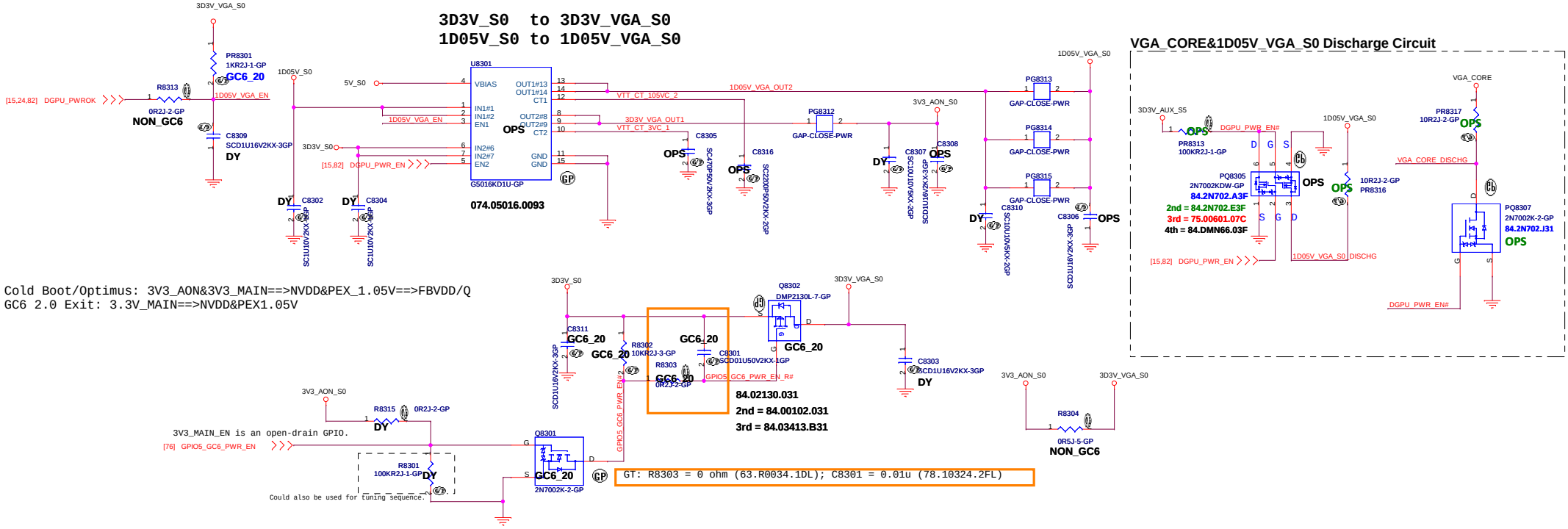
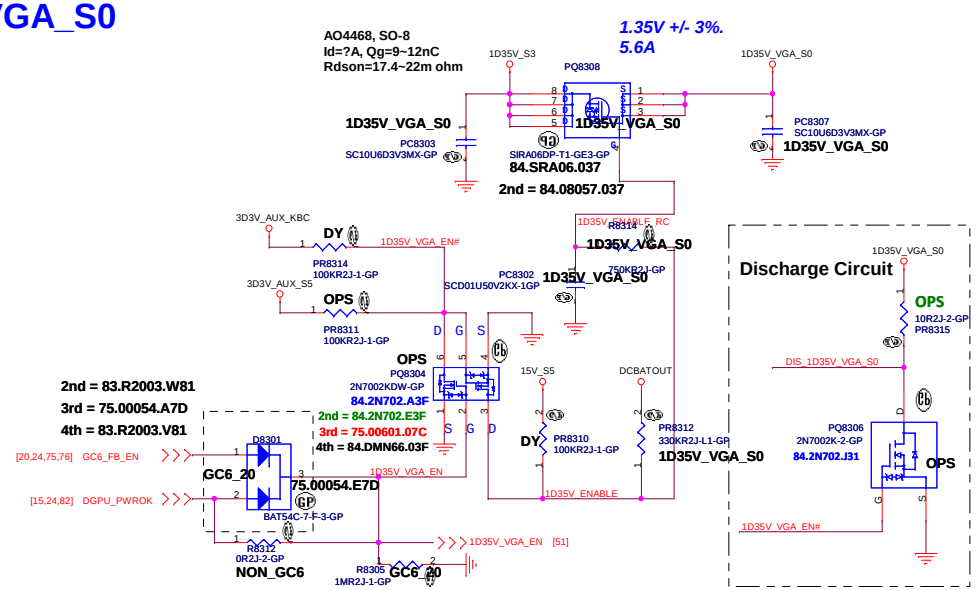
3D3V_VGA_S0
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0



1D35V_VGA_S0



CTx (pF)	Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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Title: DISCRETE VGA POWER
Size: Custom | Document Number: Janus HSW 40/50/70 | Rev: A00
Date: Monday, February 10, 2014 | Sheet 83 of 104

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Title: Reserved

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Title: Reserved

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SSID = Mechanical

S1
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.601
3rd = 34.4CK01.501

S2
STF237R117H83-1-GP
34.4CK01.001
2nd = 34.4CK01.601
3rd = 34.4CK01.501

H2
HOLE335R115-GP
ZZ.00PAD.D01

H5
HT85BE85R29-U-5-GP
ZZ.00PAD.D41

H6
HT85BE85R29-U-5-GP
ZZ.00PAD.D41

H1
HOLE335R115-GP
ZZ.00PAD.D01

H3
HOLE335R115-GP
ZZ.00PAD.D01

H4
HOLE256R115-GP
ZZ.00PAD.D11

SPR2
SPRING-102-GP
34.41V01.001

SPR3
SPRING-102-GP
34.41V01.001

SPR5
SPRING-63-GP
34.4Y806.001

SPR4
SPRING-43-GP-U
34.15J03.001

C1
HOLE197R166-1-GP
ZZ.00PAD.V71

C2
HOLE197R166-1-GP
ZZ.00PAD.V71

C3
HOLE197R166-1-GP
ZZ.00PAD.V71

SSID = EMI

Mind the voltage rating of the caps.

DCBATOUT
EC9701 EC9702 EC9703 EC9704 EC9708 EC9705 EC9706 EC9707 EC9709 EC9710
EC9717 EC9711 EC9712 EC9713 EC9716 EC9715 EC9714

1D35V_VGA_S0
EC9727 EC9725 EC9726 EC9730 EC9728 EC9729 EC9731

AUD_AGND
EC9739 EC9744 EC9743 EC9745

DCBATOUT
EC9740 EC9741 EC9742 EC9747 EC9748 EC9749

5V_S0
EC9720 EC9719 EC9718 EC9723 EC9721 EC9722 EC9724

3D3V_S0
EC9737 EC9735 EC9736 EC9738

5V_S5
EC9734 EC9732 EC9733

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Title: UNUSED PARTS/EMI Capacitors
Size: A3
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Rev: A00
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Title: *(Reserved)Finger Print*

Size	Document Number	Rev
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<Core Design>

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Title: Free Fall Sensor

Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00

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Title: Reserved

Size	Document Number	Rev
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Title: Reserved

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Title: Express Card

Size	Document Number	Rev
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<Core Design>

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Title: *LVDS_Switch*

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<Core Design>

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Title: CRT_Switch

Size	Document Number	Rev
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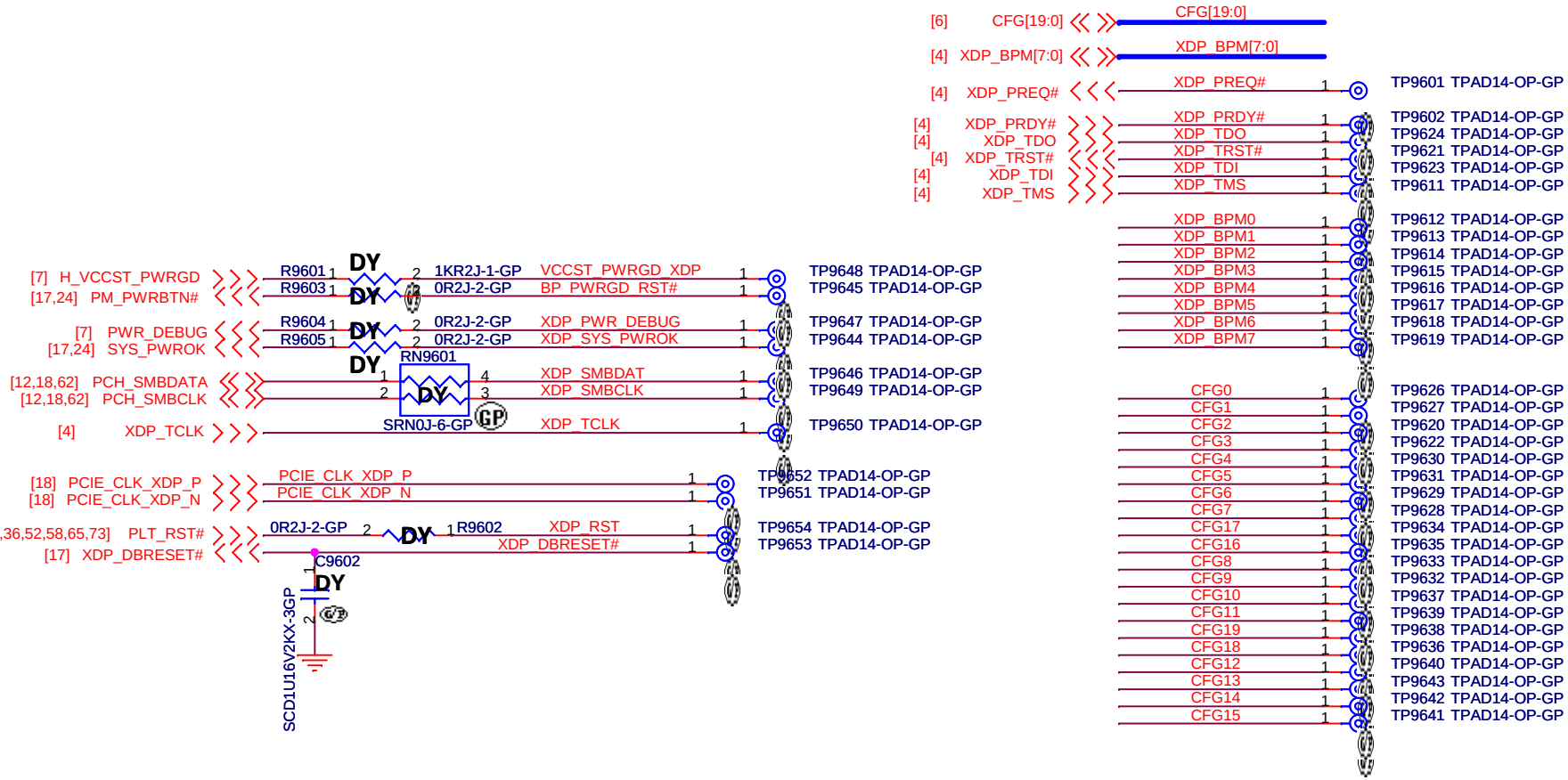
SSID = XDP

CPU XDP



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Title: *CPU/PCH XDP*

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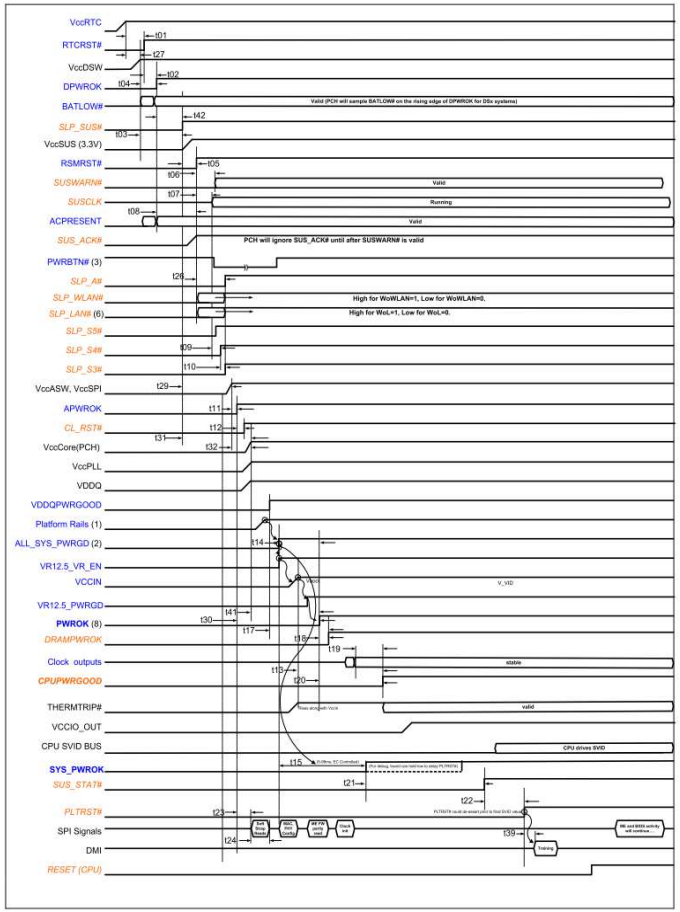
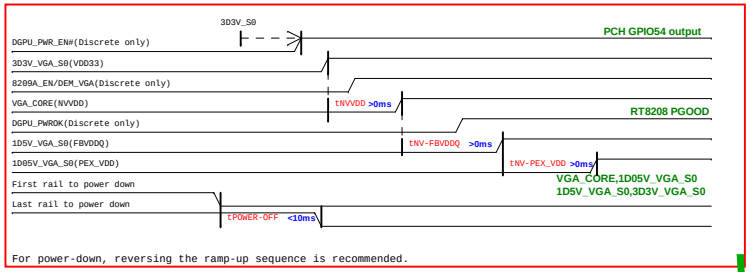
Shark Bay Platform Power Sequence

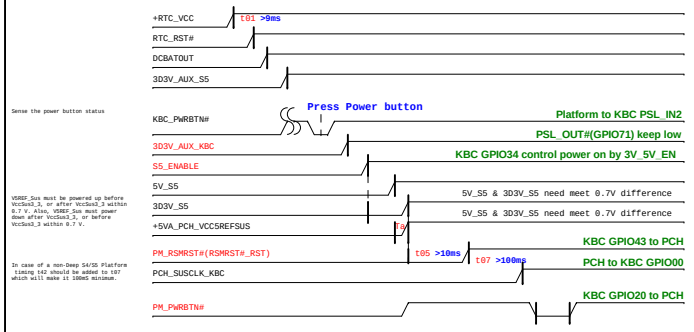


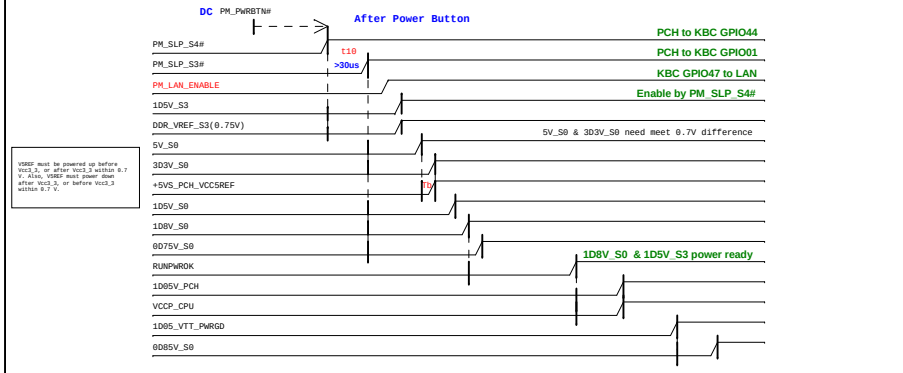
N14P-GT Power-Up/Down Sequence

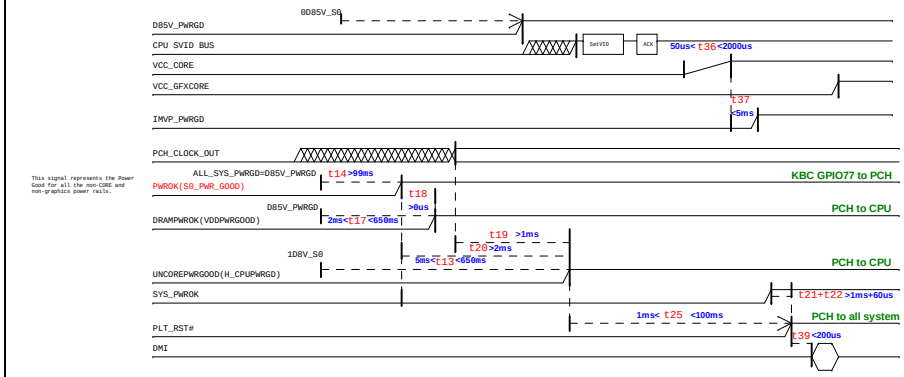


(DC mode)

Red Words: Controlled by EC GPIO







<Core Design>
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Title: Power Sequence
Size: A1 | Document Number: Janus HSW 40/50/70 | Rev: A00
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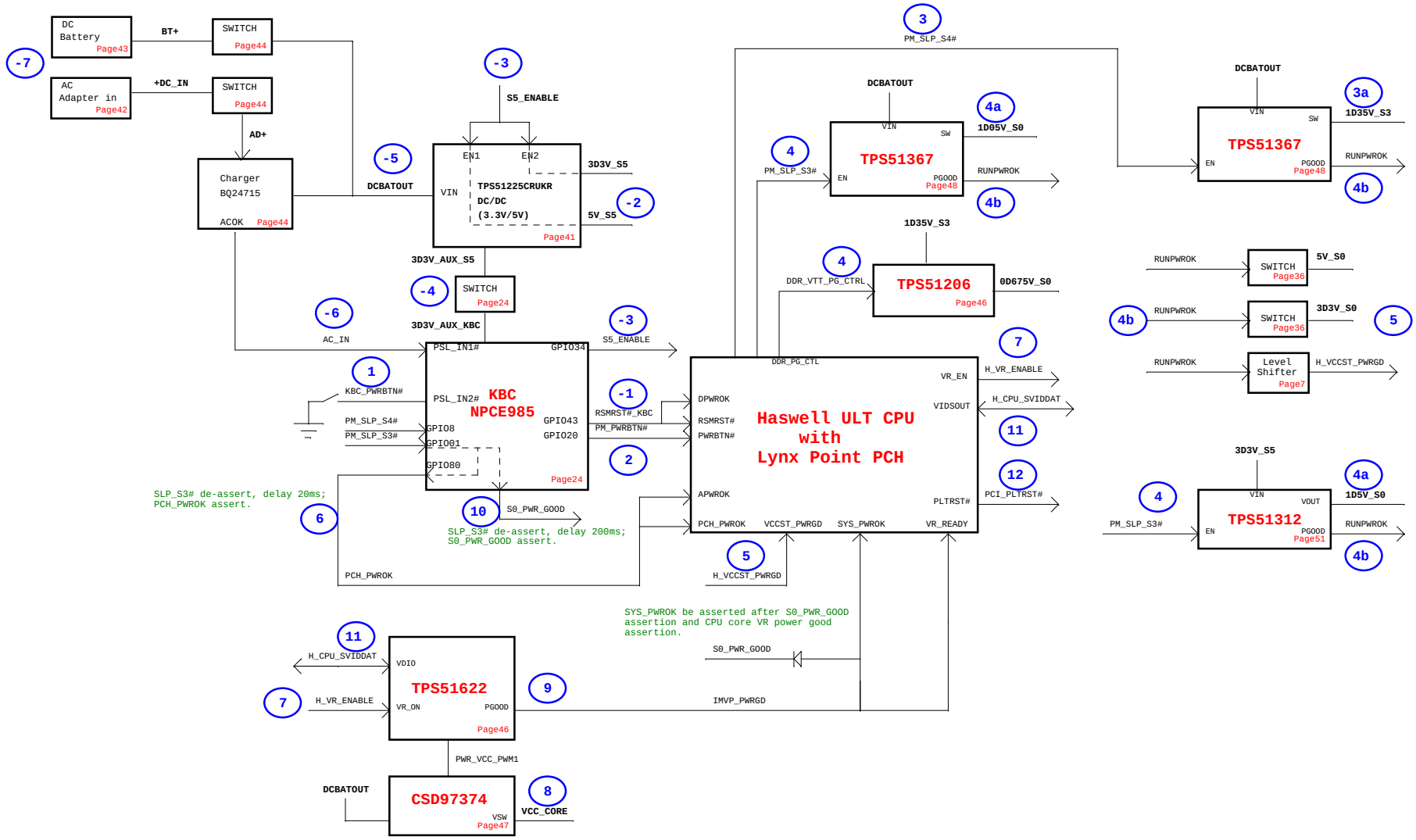
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



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Title: Power Sequence Diagram

Size: A2 | Document Number: Janus HSW 40/50/70 | Rev: A00

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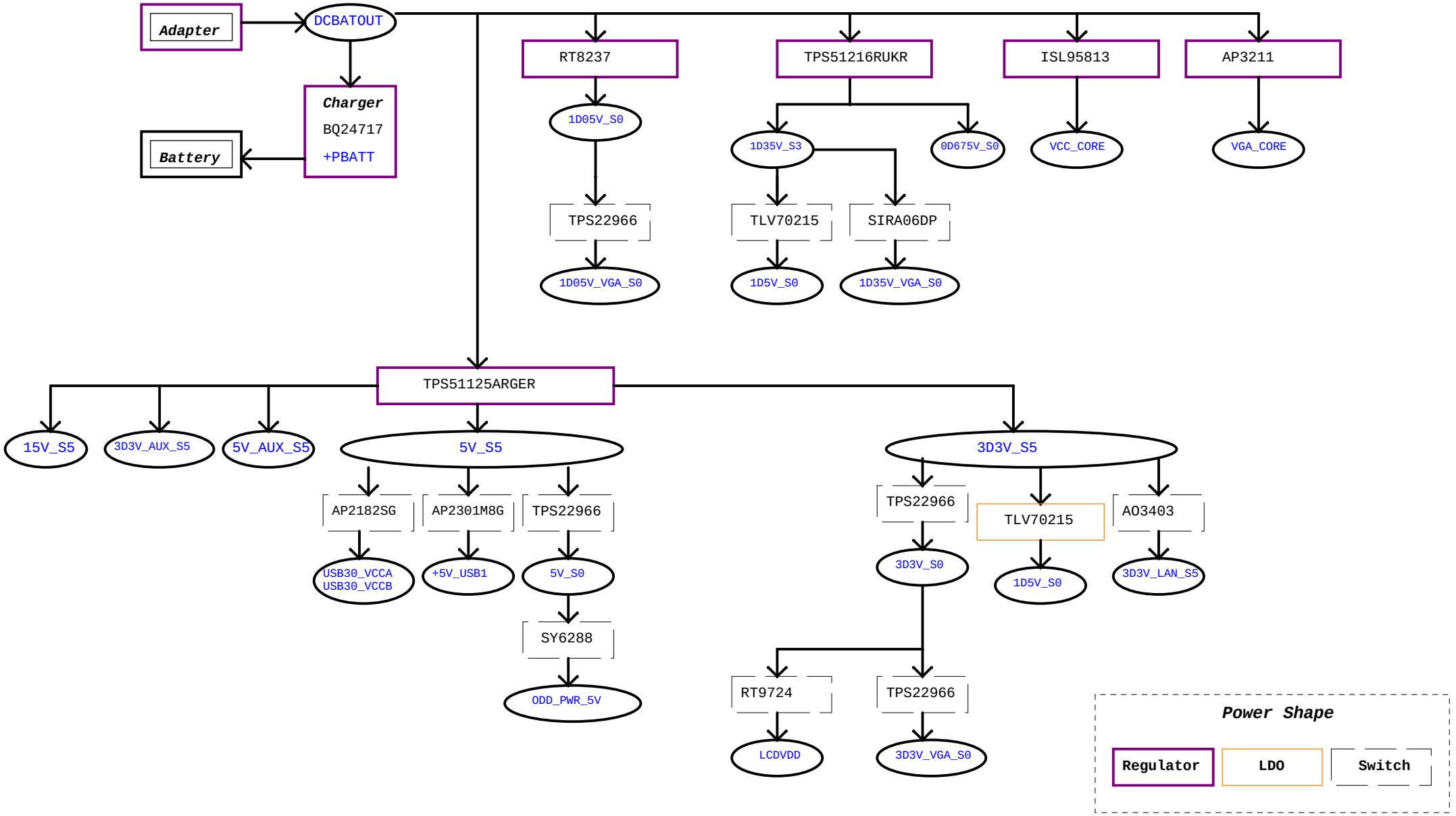

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Title: Power Block Diagram

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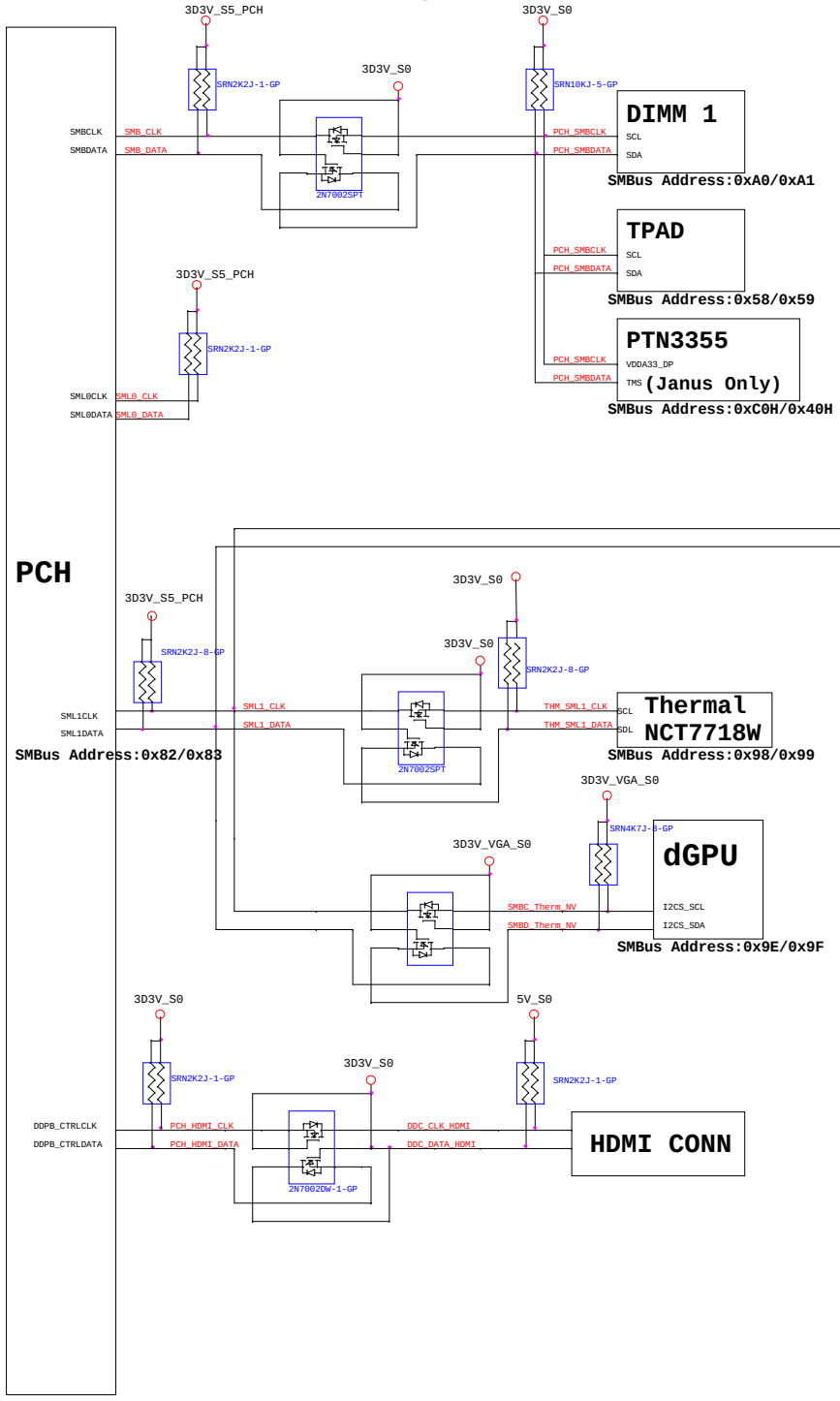
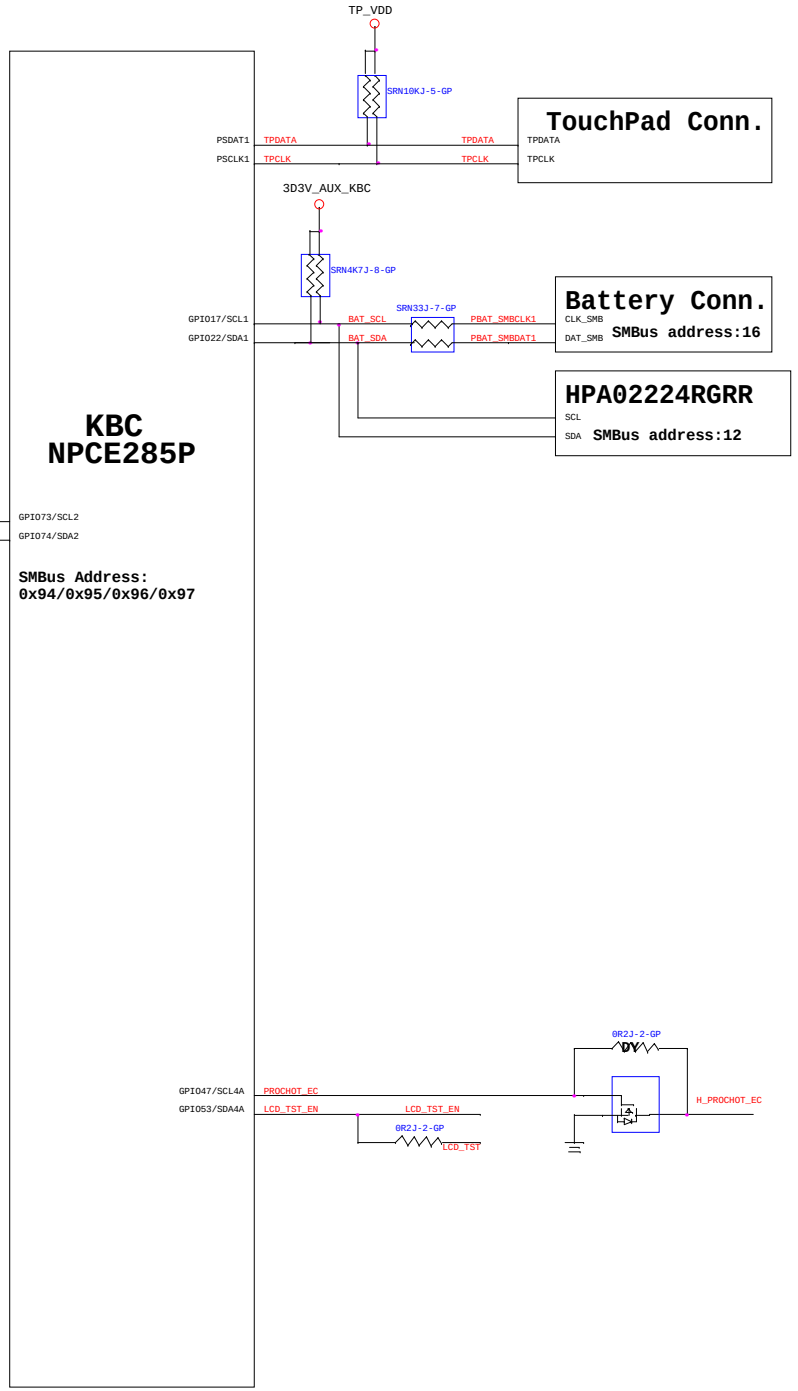
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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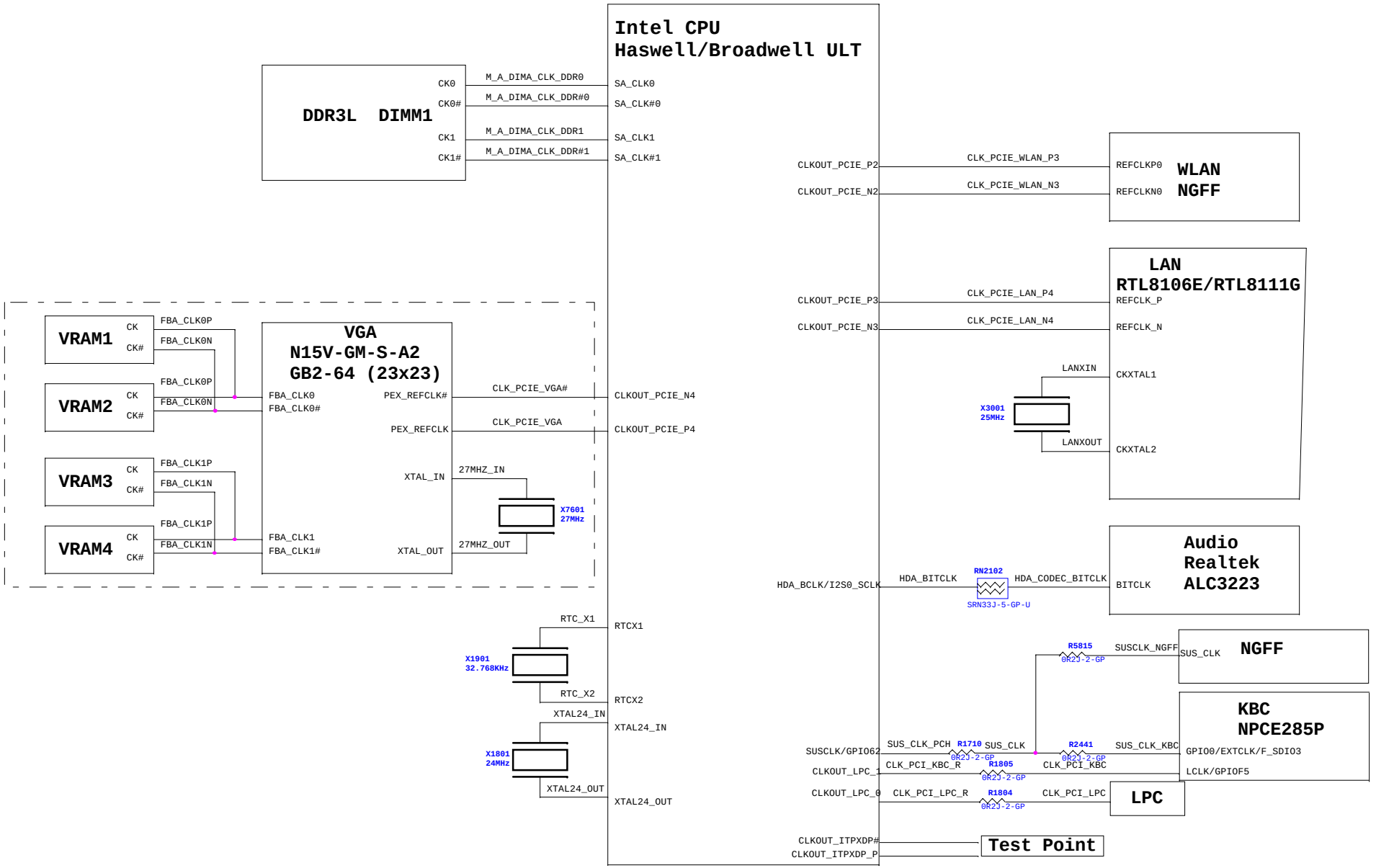
CLK Block Diagram



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Title: CLK Block Diagram
Size: A2
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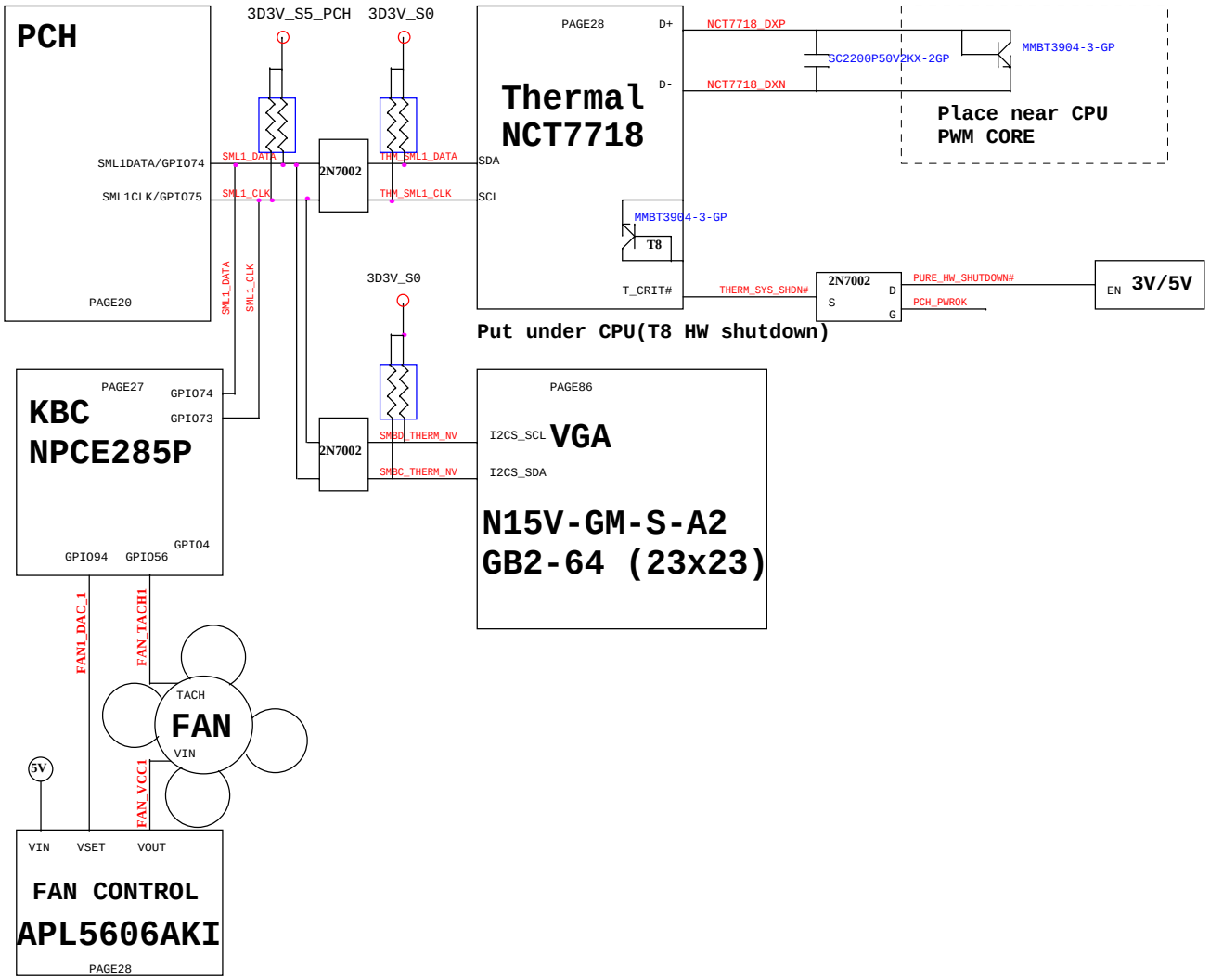
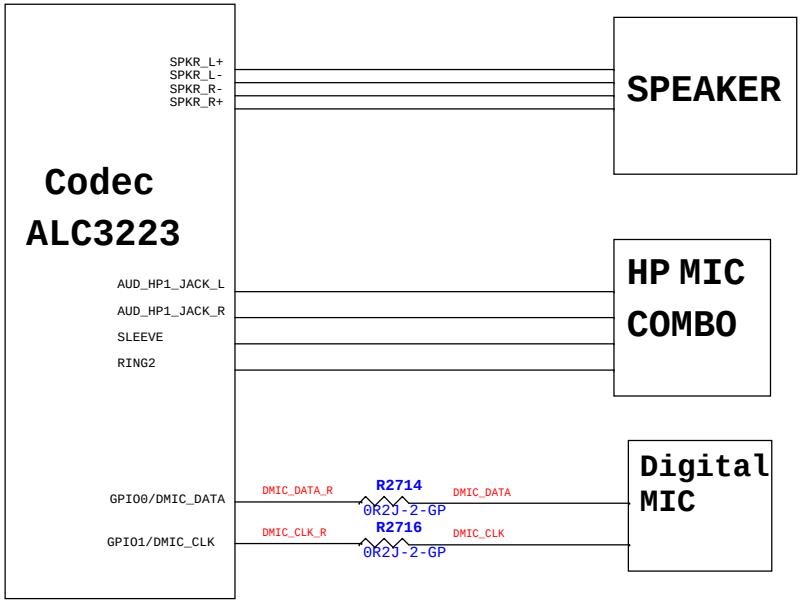
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Janus HSW 40/50/70 | Rev: A00

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Change notes :

DATE	VERSON	DATE	Page	Modify List	OWNER

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Wistron Corporation
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Title: Change History

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VERSION	DATA	PAGE	Change Iteam

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Title: Change History

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