

# Compal confidential

## Schematics Document

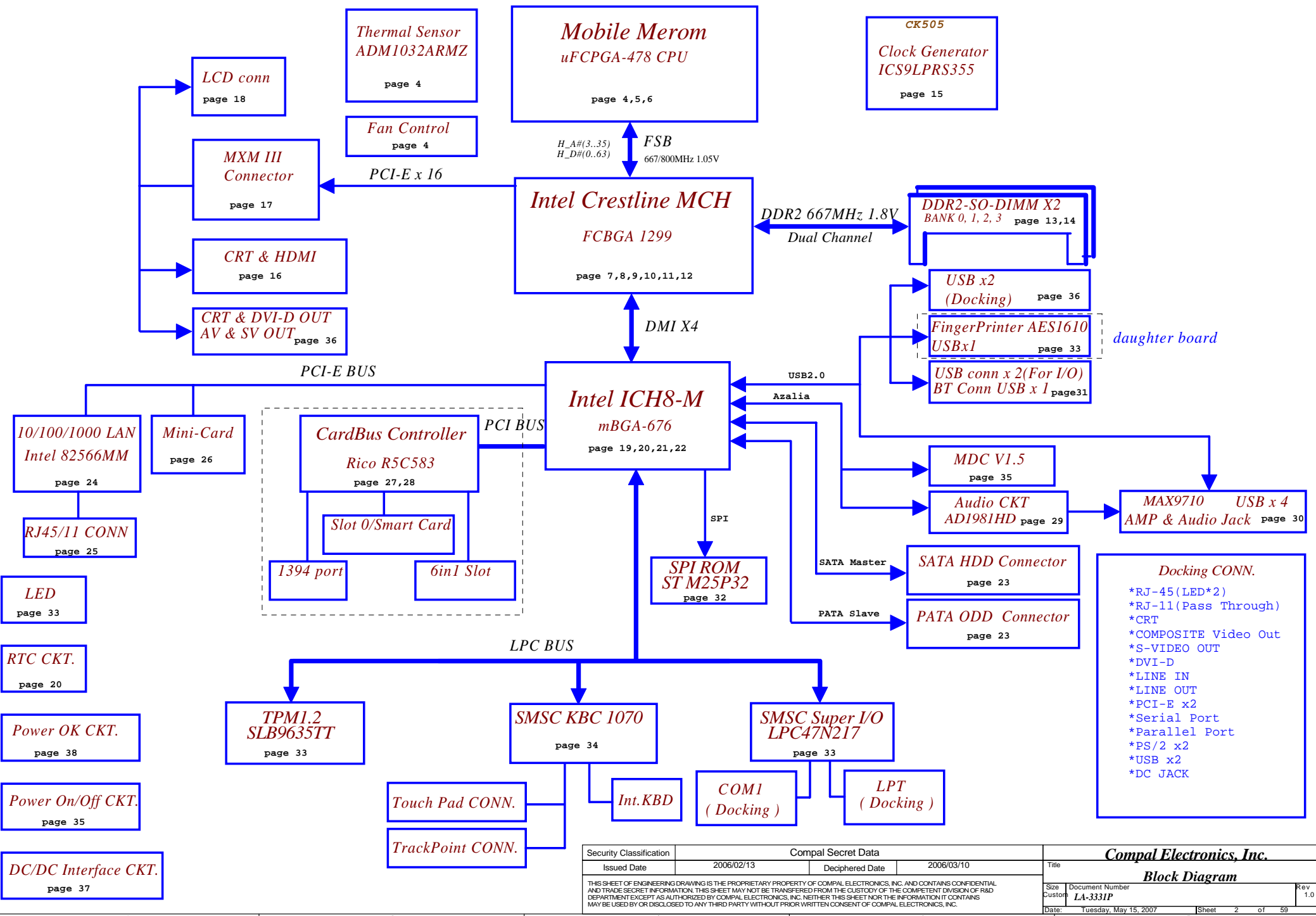
Mobile Merom uFCPGA with Intel  
Crestline\_PM+ICH8-M core logic

2007-05-15

REV:1.0

Security Classification		Compal Secret Data		Title	
Issued Date	2006/04/13	Deciphered Date	2006/06/30	Cover Sheet	
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# ABITA



## Voltage Rails

power plane State	+B LDO3 LDO5	+5VALW +3VALW	+3VM +1.25VM +1.05VM	+5V +1.8V +0.9V	+5VS +3VS +1.8VS +1.5VS +1.25VS +CPU_CORE +VCCP
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON X MEANS OFF

## PCI Devices

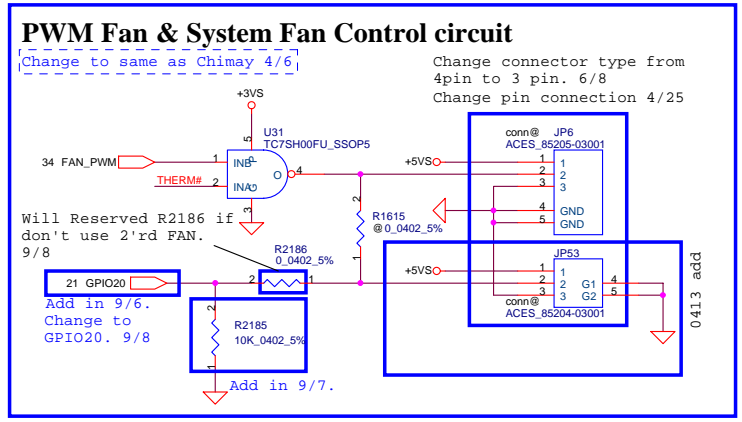
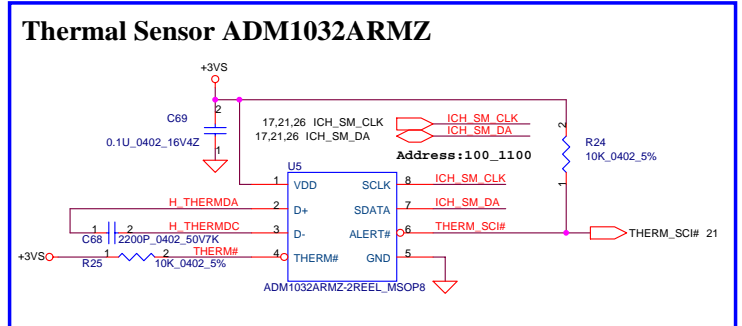
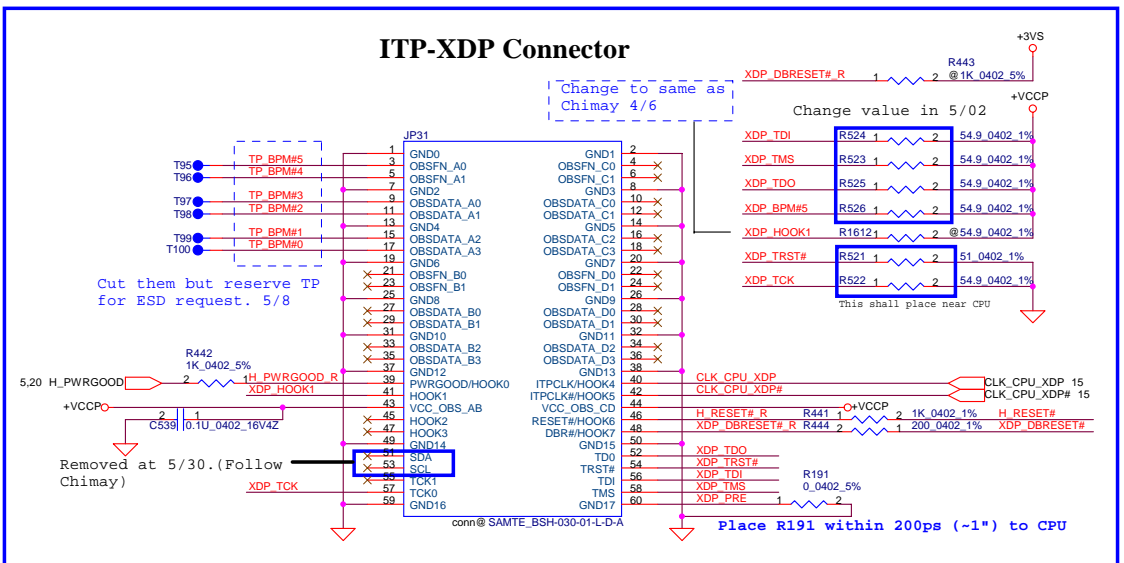
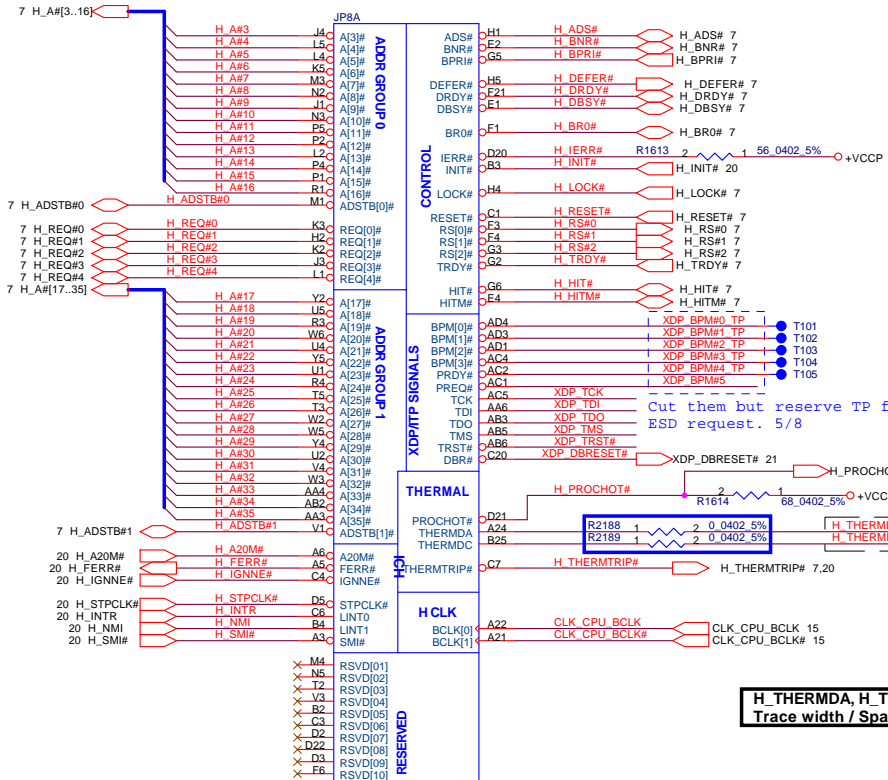
EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

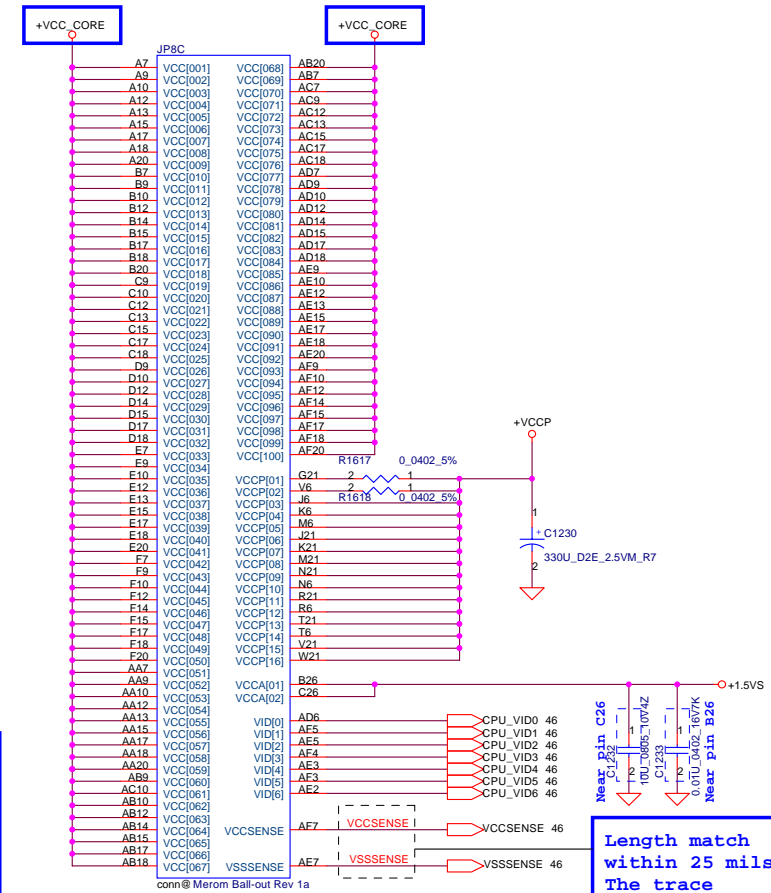
USB PORT#	Destination
0	M/B
1	Finger Printer
2	M/B
3	On Audio Board
4	On Audio Board
5	On Audio Board
6	Blut Tooth
7	Docking
8	On Audio Board
9	Docking

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	<del>Floppy</del>
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass storagage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

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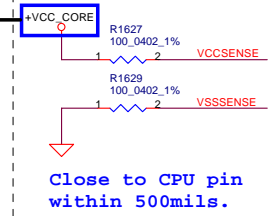


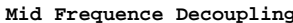
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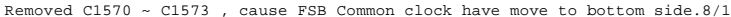
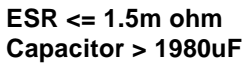
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match  
within 25 mils.  
The trace  
width/space/other  
is 20/7/25.

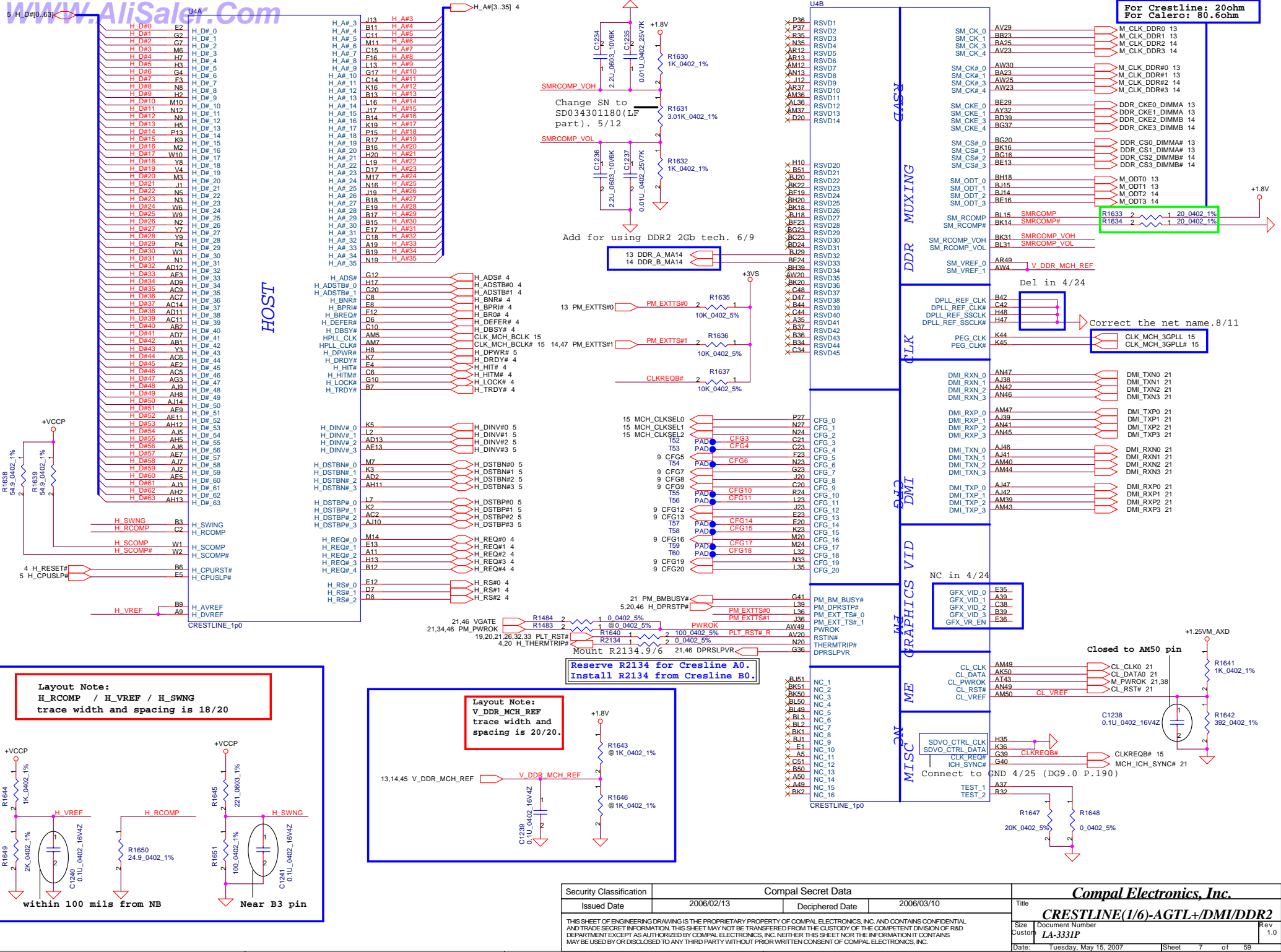




South Side Secondary	North Side Secondary
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
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96	96
97	97
98	98
99	99
100	100



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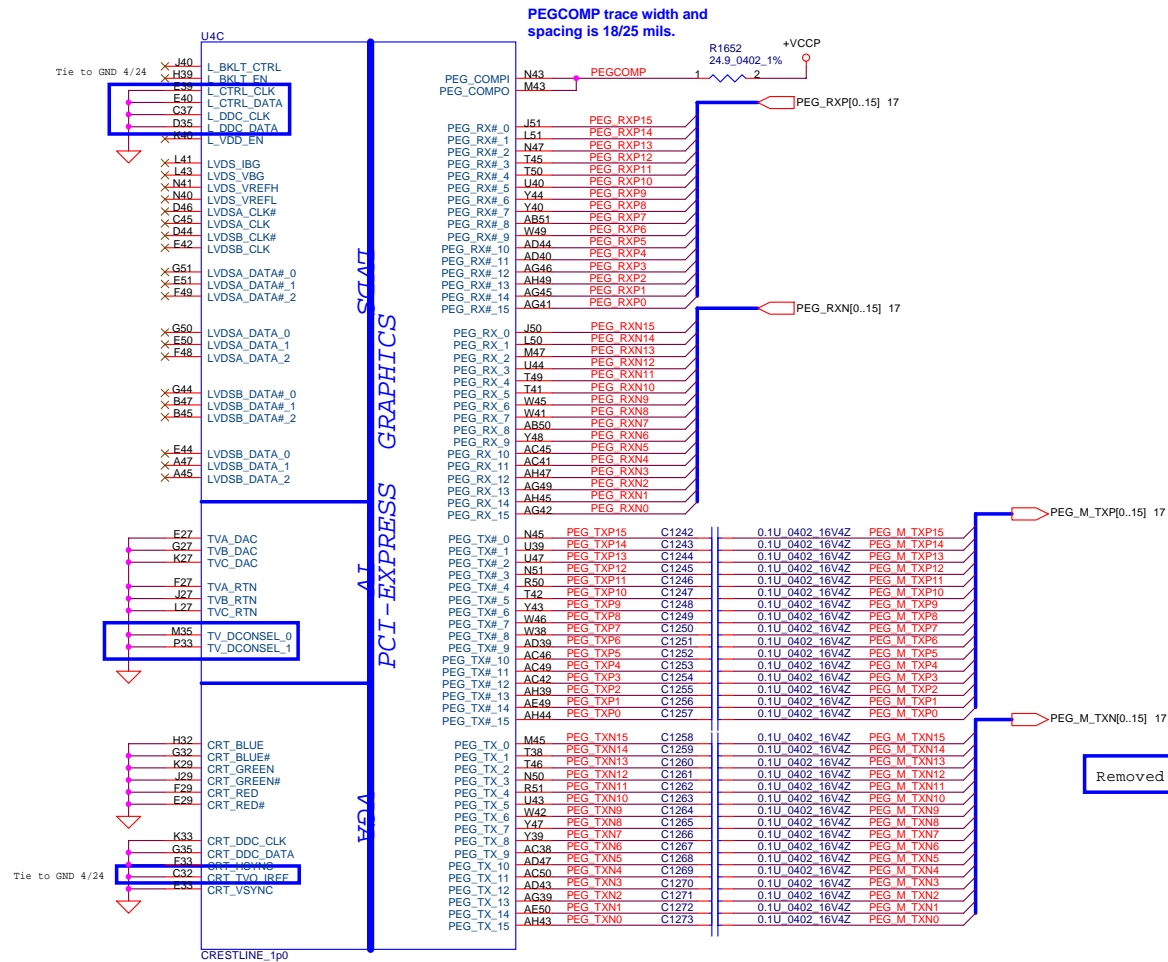
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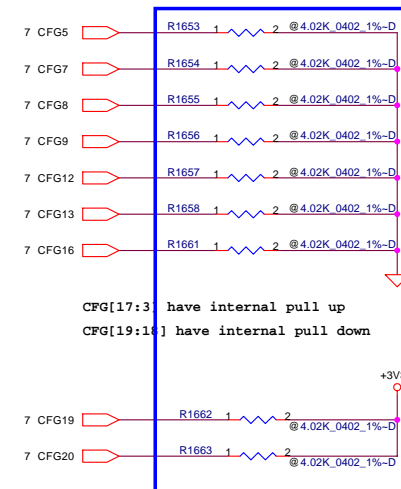




## Strap Pin Table

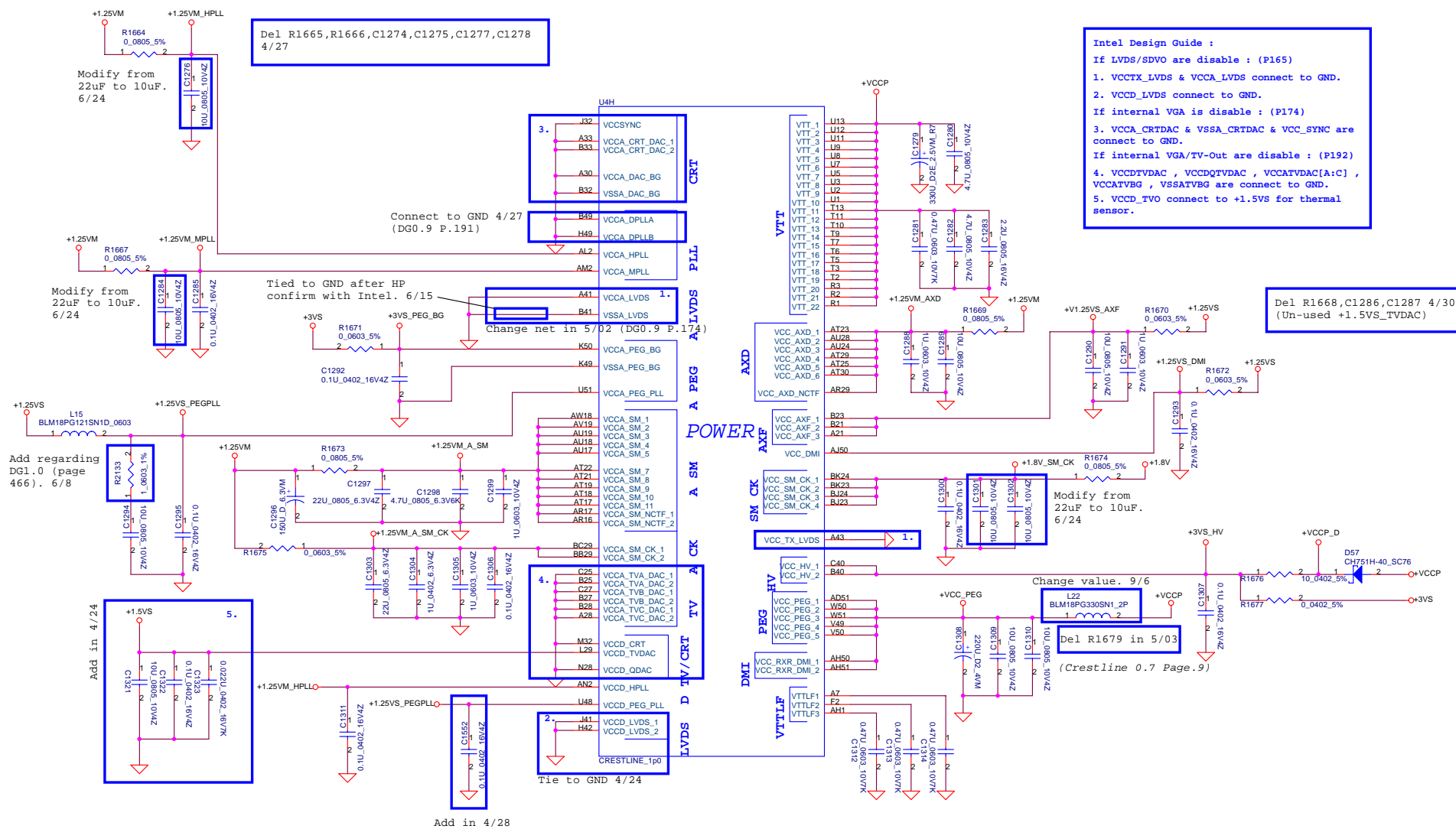


CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present *
	1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) *
	1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu.



Change Value  
—form 2.2K to  
4.02K.

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Intel Design Guide :

If LVDS/SDVO are disable : (P165)

1. VCCTX\_LVDS & VCCA\_LVDS connect to GND.

2. VCCD\_LVDS connect to GND.

If internal VGA is disable : (P174)

3. VCCA\_CRTDAC & VSSA\_CRTDAC & VCC\_SYNC are connect to GND.

If internal VGA/TV-Out are disable : (P192)

4. VCCDQTVDAC , VCCDQTVDAC , VCCATVDAC[A:C] , VCCATVBG , VSSATVBG are connect to GND.

5. VCCD\_TV0 connect to +1.5VS for thermal sensor.

Del R1668,C1286,C1287 4/30  
(Un-used +1.5VS\_TVDAC)

Modify from  
22uF to 10uF.  
6/24

Change value. 9/  
L22  
BLM18PG330SN1 2P

Del R1679 in 5/03

(Crestline 0.7 Page.

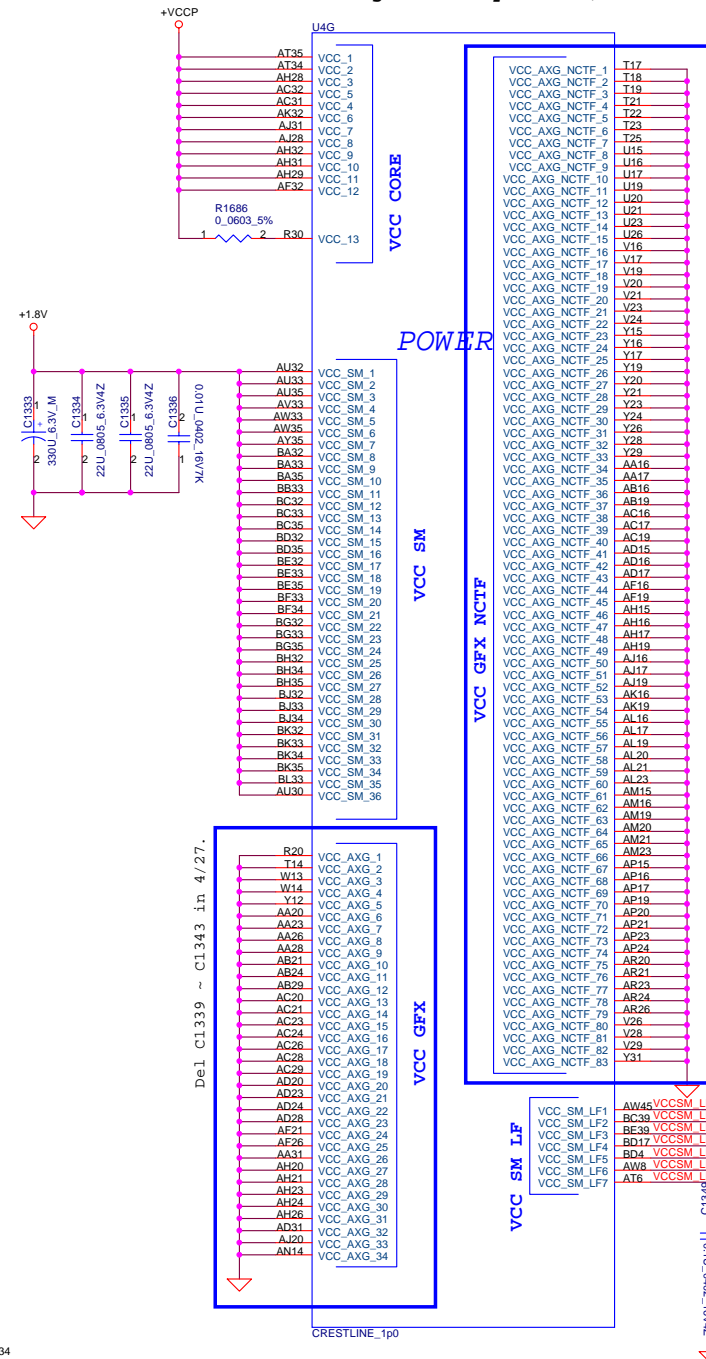
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title		
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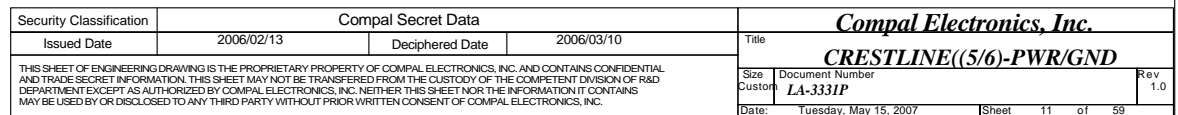
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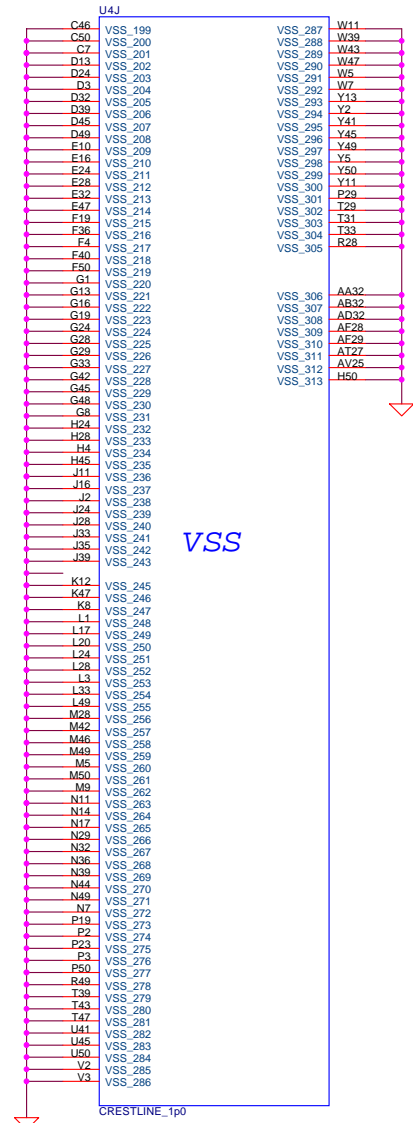
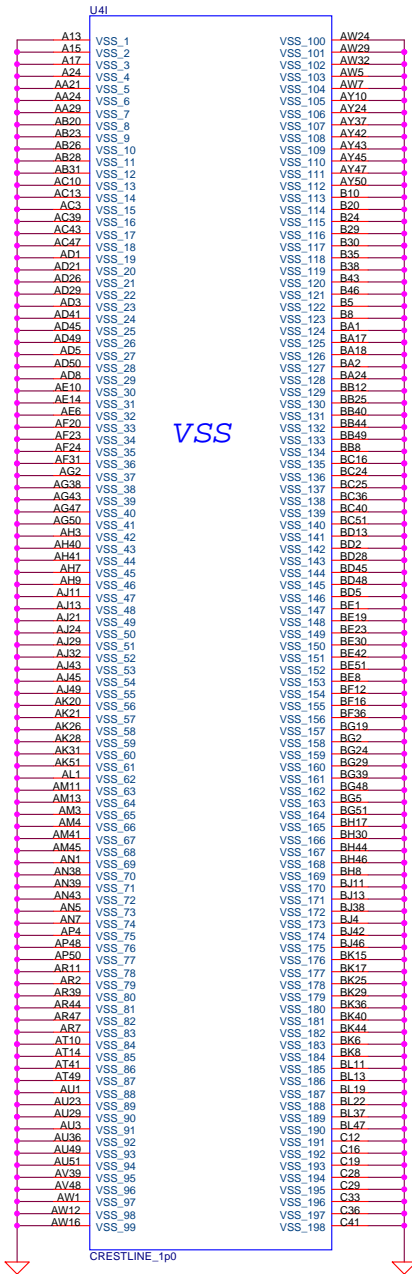
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Del C1325 ~ C1327 in 4/27.



Del C1339 ~ C1343 in 4/27.





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								Size			
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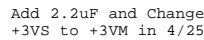
[illegible][illegible]

Diagram illustrating the connection of DDR2 memory banks (RP11 to RP16) to a central bus. The diagram shows the connection of various signals (DDR A MA5, DDR A MA8, DDR A MA1, DDR A MA3, DDR A RAS#, DDR CS0 DIMMA#, DDR A BS0, DDR A MA10, DDR A CAS#, DDR A WE#, DDR CS1 DIMMA#, M\_ODT1, DDR A MA14, R2135, and 56\_0402.5) to the memory banks. A +0.9V supply is indicated at the top.

Legend:

- RP11: DDR A MA5, DDR A MA8, DDR A MA1, DDR A MA3, DDR A RAS#, DDR CS0 DIMMA#, DDR A BS0, DDR A MA10, DDR A CAS#, DDR A WE#, DDR CS1 DIMMA#, M\_ODT1, DDR A MA14
- RP12: 56\_0404\_4P2R\_5%, DDR A BS2, DDR CKEO DIMMA, DDR A MA7, DDR A MA6, DDR A MA9, DDR A MA12, DDR A MA2, DDR A MA0, DDR A MA4, DDR A MA3, DDR A MA1, DDR A MA0, DDR A MA4, DDR A MA3
- RP13: 56\_0404\_4P2R\_5%, DDR A BS2, DDR CKEO DIMMA, DDR A MA7, DDR A MA6, DDR A MA9, DDR A MA12, DDR A MA2, DDR A MA0, DDR A MA4, DDR A MA3, DDR A MA1, DDR A MA0, DDR A MA4, DDR A MA3
- RP14: 56\_0404\_4P2R\_5%, DDR A BS2, DDR CKEO DIMMA, DDR A MA7, DDR A MA6, DDR A MA9, DDR A MA12, DDR A MA2, DDR A MA0, DDR A MA4, DDR A MA3, DDR A MA1, DDR A MA0, DDR A MA4, DDR A MA3
- RP15: 56\_0404\_4P2R\_5%, DDR A BS2, DDR CKEO DIMMA, DDR A MA7, DDR A MA6, DDR A MA9, DDR A MA12, DDR A MA2, DDR A MA0, DDR A MA4, DDR A MA3, DDR A MA1, DDR A MA0, DDR A MA4, DDR A MA3
- RP16: 56\_0404\_4P2R\_5%, DDR A BS2, DDR CKEO DIMMA, DDR A MA7, DDR A MA6, DDR A MA9, DDR A MA12, DDR A MA2, DDR A MA0, DDR A MA4, DDR A MA3, DDR A MA1, DDR A MA0, DDR A MA4, DDR A MA3

Additional labels: R2135, 56\_0402.5, Add for using DDR2 2Gb tech. 6/9



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The schematic shows a 10-bit DAC implemented with a R-2R ladder network. The circuit is powered by a +0.9V supply. The ladder consists of resistors labeled C65 through C71, each with a value of 0.11U 0402, 16k42. The output of the ladder is connected to a 0V ground symbol.

[illegible]

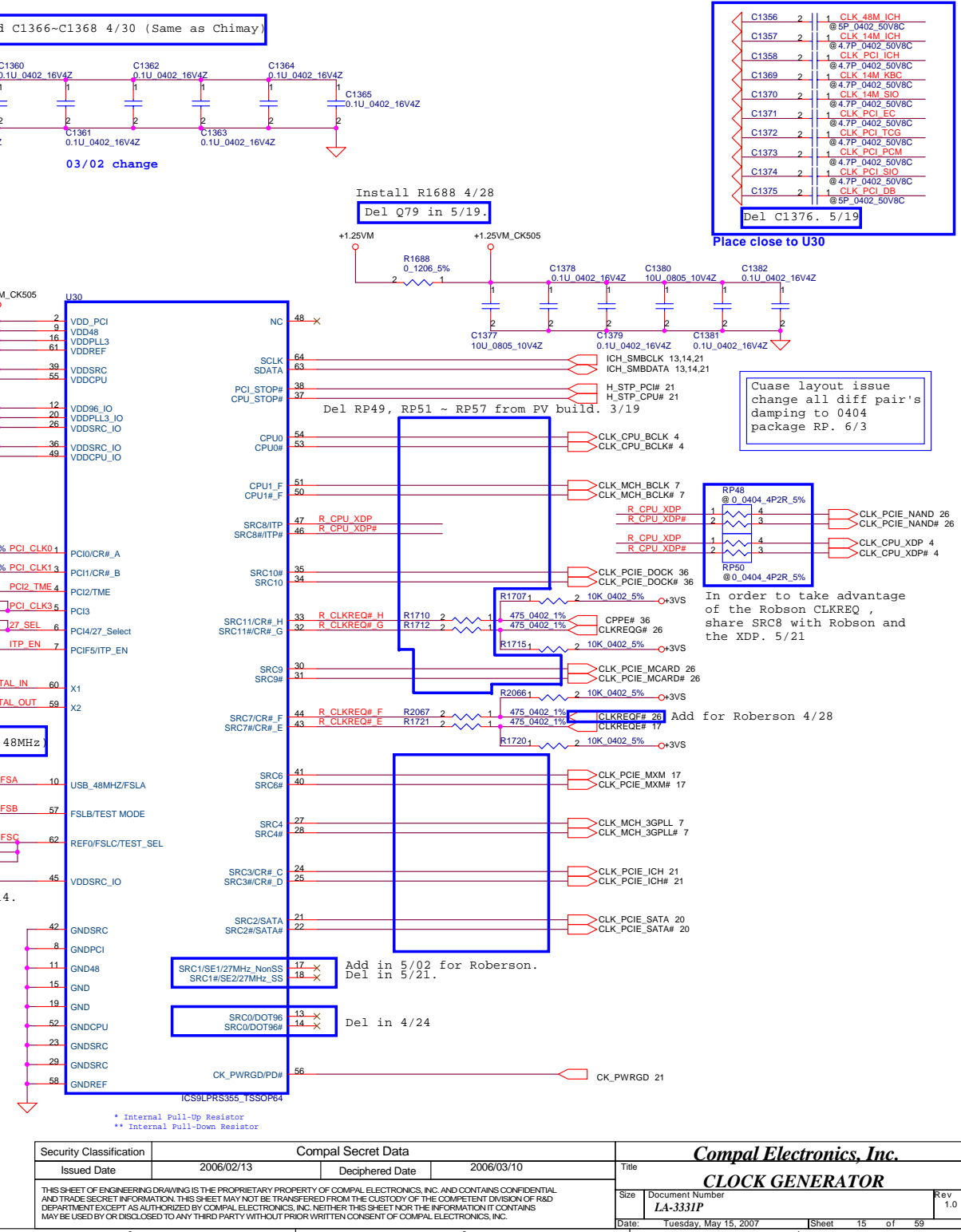
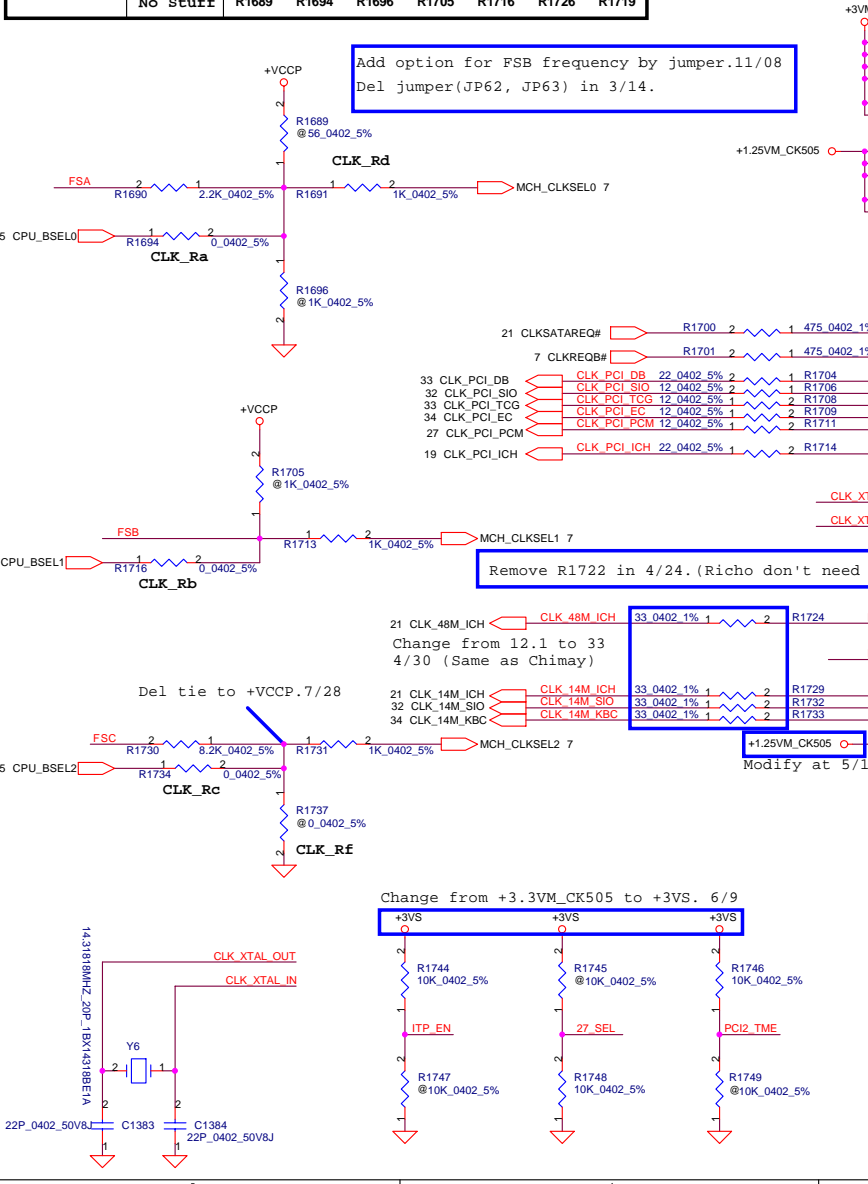
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Issued Date		2006/02/13		Title <b>DDRII-SODIMM SLOT2</b>	
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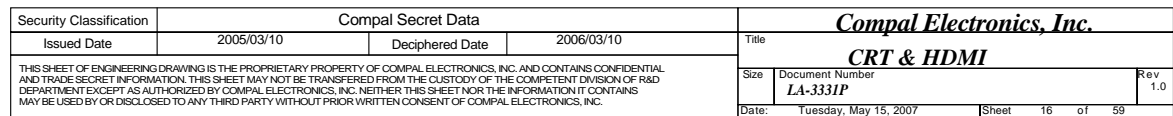
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

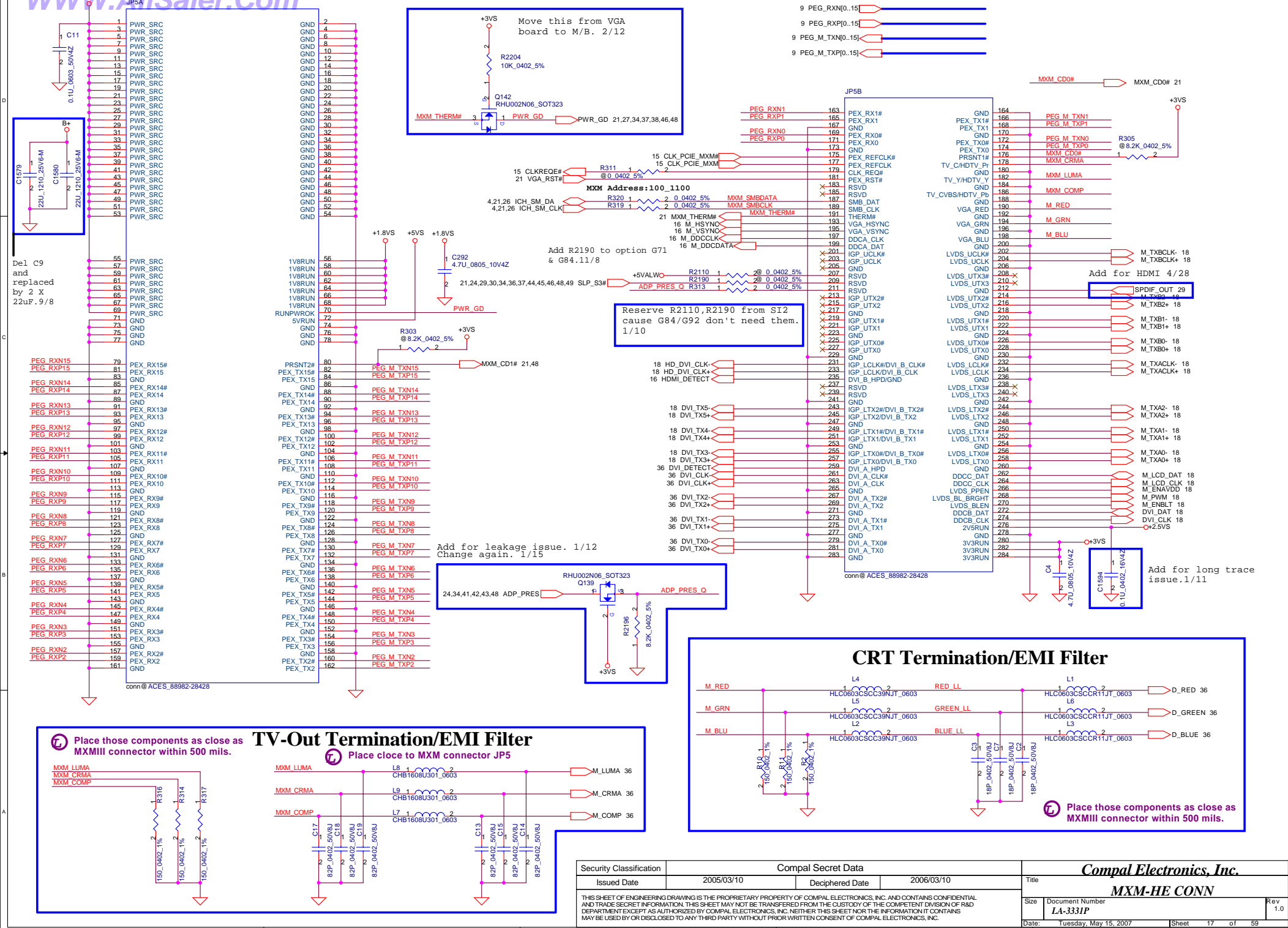
FSB Frequency Selet:

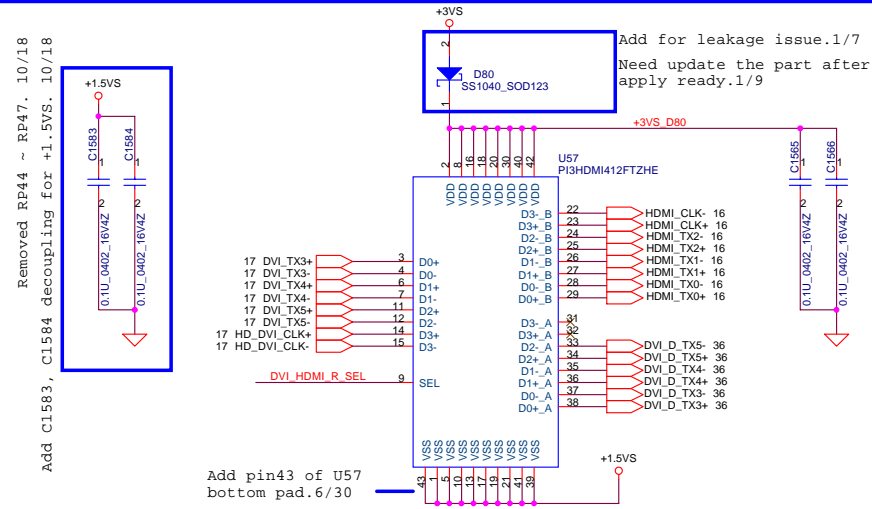
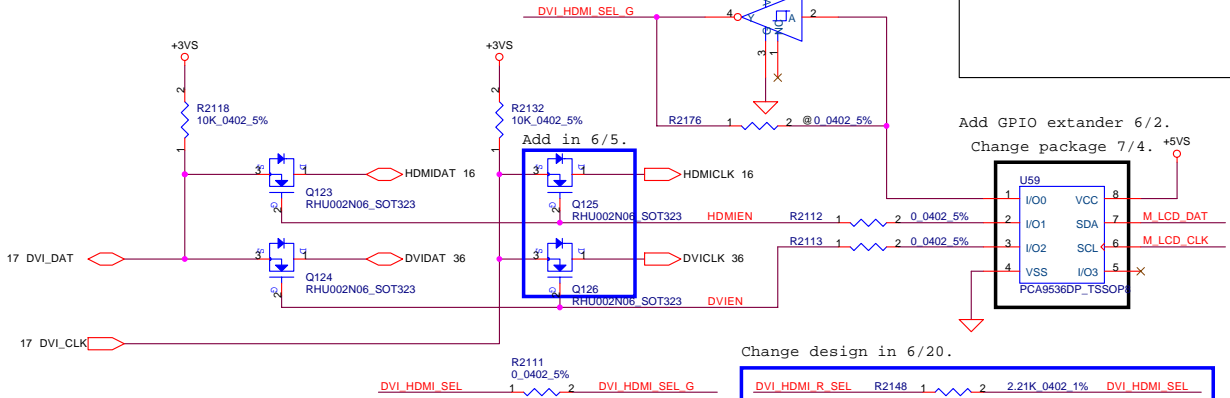
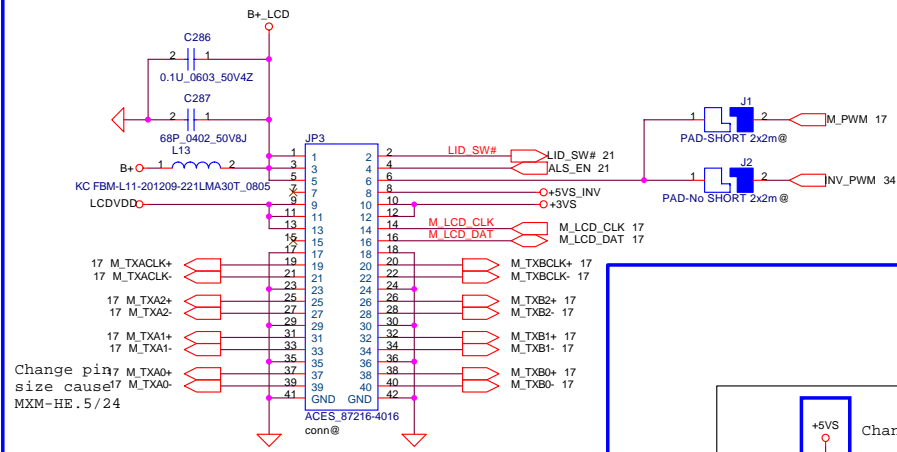
CPU Driven	Stuff	R1694	R1716	R1734			
* (Default)	No Stuff	R1689	R1696	R1705	R1719	R1726	R1737
667MHz	Stuff	R1689	R1696	R1734	R1737		
	No Stuff	R1694	R1705	R1716	R1719	R1726	
800MHz	Stuff			R1734	R1737		
	No Stuff	R1689	R1694	R1696	R1705	R1716	R1726 R1719



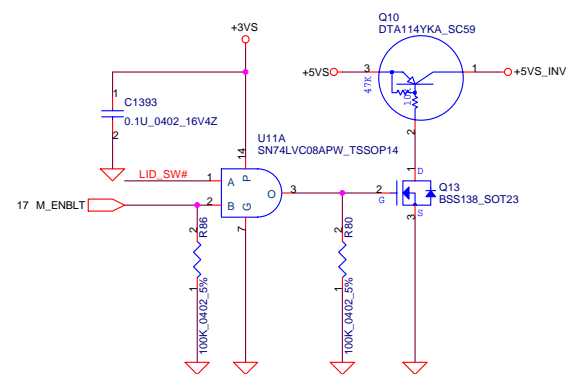
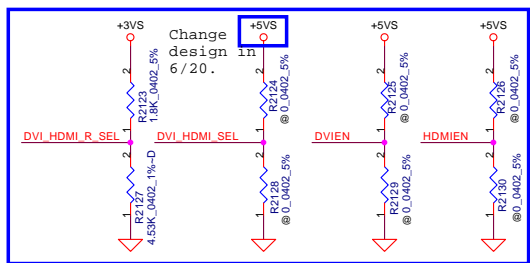
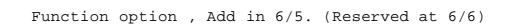
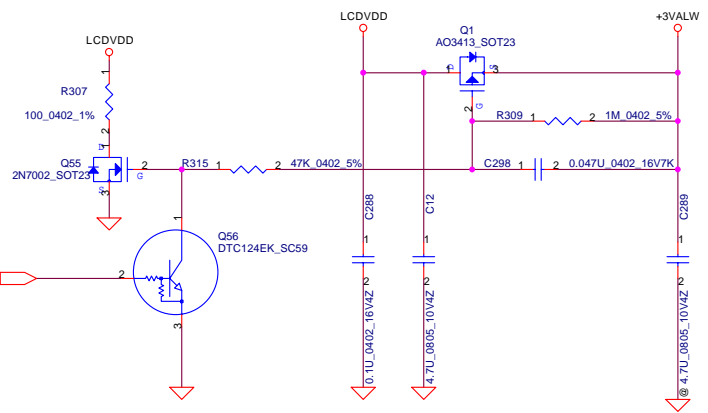
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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				Date: Tuesday, May 15, 2007	Sheet 15 of 59



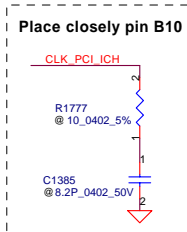




## LCD POWER CIRCUIT



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>LCD CONN &amp; Q-Switch &amp; GPIO Ext.</b>		
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					LA-3331P	1.0
				Date:	Tuesday, May 15, 2007	Sheet 18 of 59



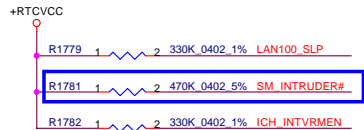
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



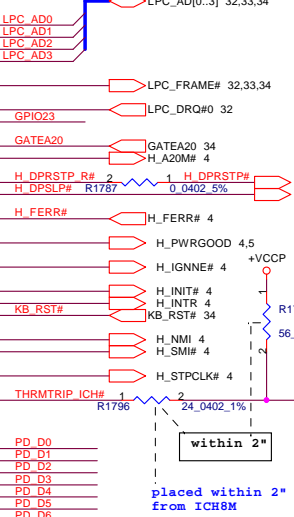
PCI_GNT3#	Low= A16 swap override Enble High= Default *
-----------	---

PCI\_GNT3#  
Del R2054. 5/12  
(According to ICH8 EDS  
1.5 P.86) R1774  
@1K\_0402\_5%

**Place closely pin B10**



Change from 1M to 470K. 6/14  
Del Kensington support. 10/18

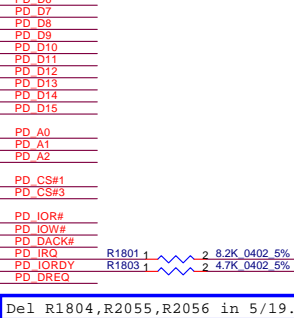


```
Add 2nd STAT in 4/19.
Del 2nd SATA in 6/1.
Del JP54 , C1387~C1390.6/1
```

Change PLT\_RST\_B# to  
PLT\_RST#. 6/15

change from ODD\_RST# to  
PLT\_RST\_B#. 5/19

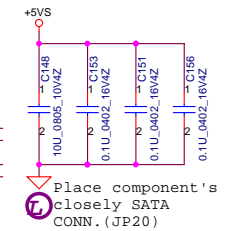
placed within 2"  
from ICH8M



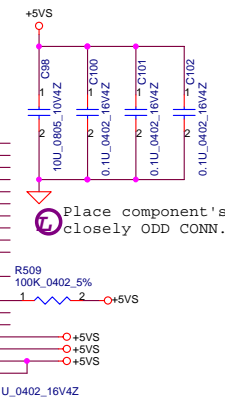
Del R1804,R2055,R2056 in 5/19.



XOR CHAIN ENTRANCE STRAP:RSVD

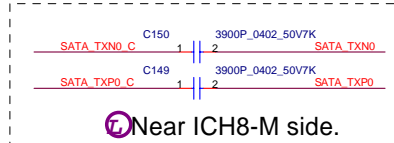
**SATA CONN**

Place component's  
closely SATA  
CONN. (JP20)



- Place component's closely ODD CONN.

Del U52.6/15  
Del C1394~C1397.6/1

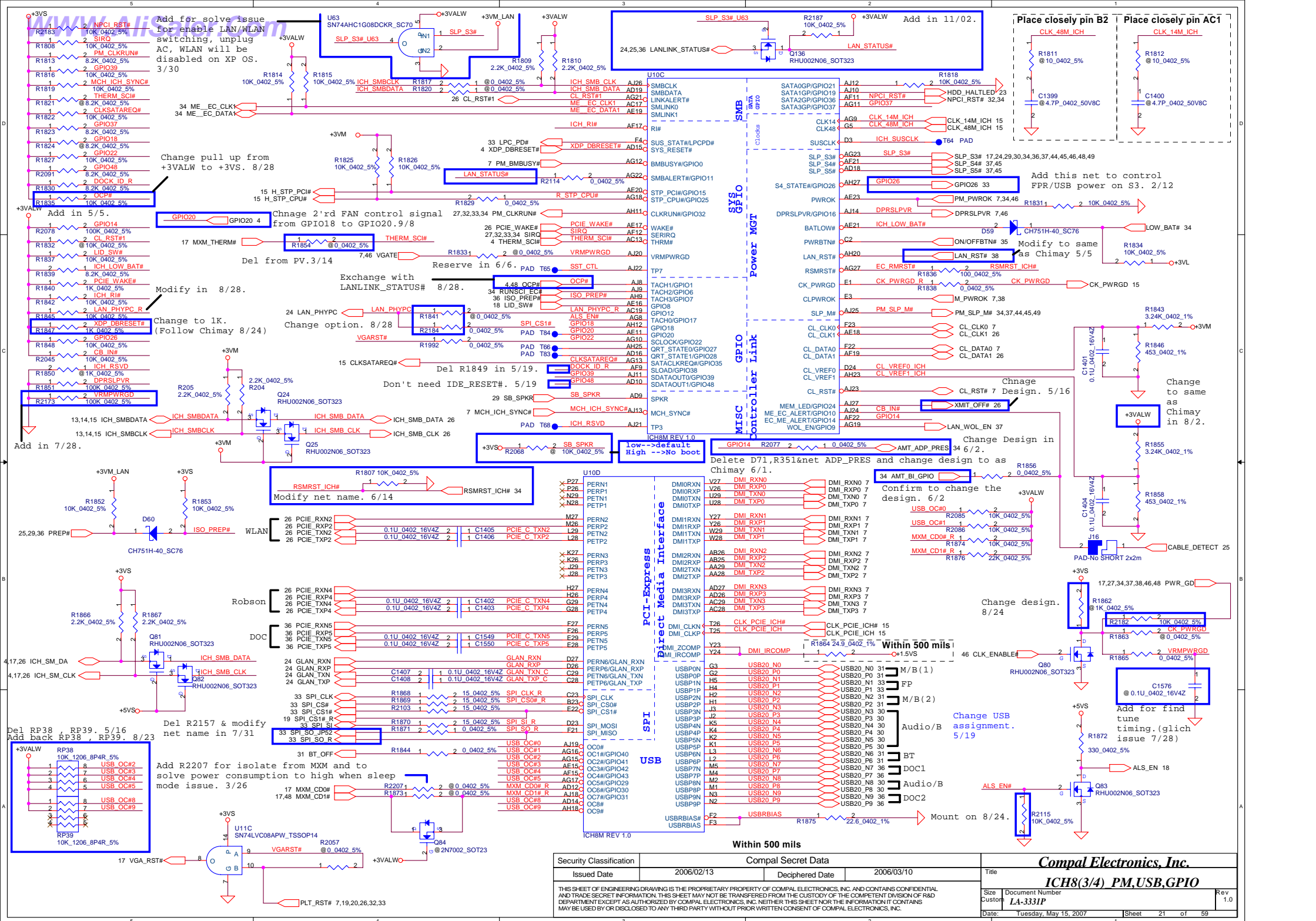


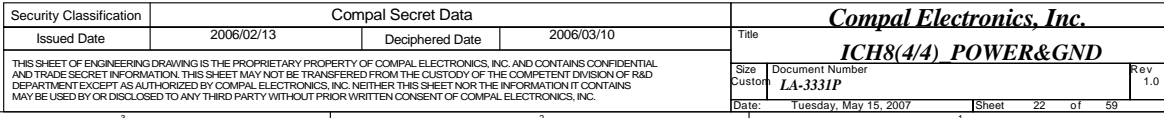
 Near Device side.

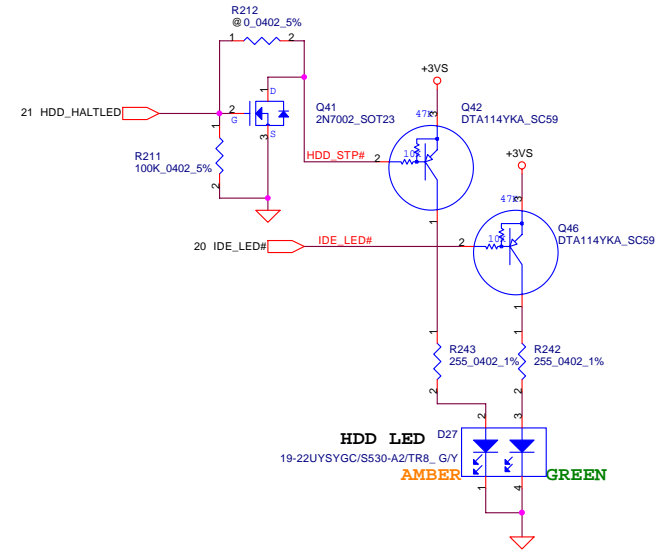
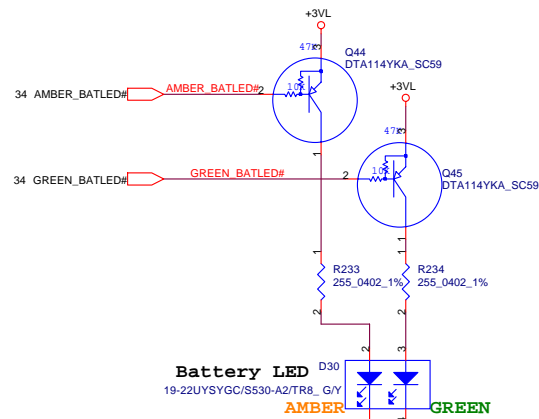
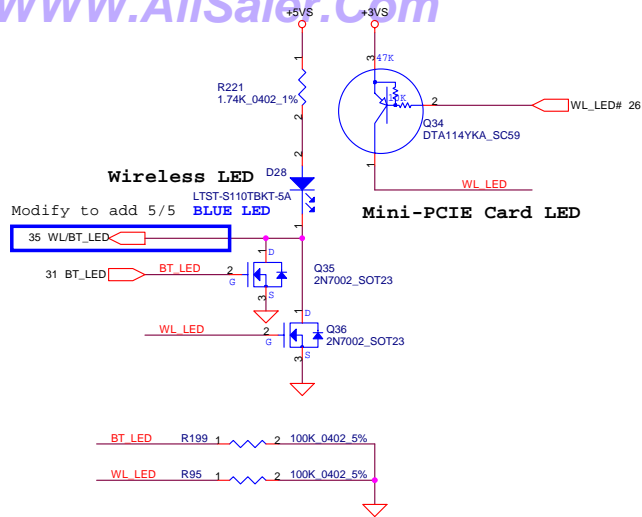
④ Near ICH8-M side.

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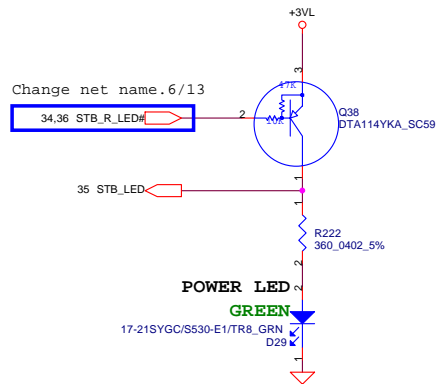








Del R2109. 6/14  
 Add the kill circuit.5/25  
 Update design. 5/14  
 Reserved Space for Kensington 4/27  
 Removed Kensington 10/18.



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ACBS support :  
Mount Q85, R2072.  
Remove Q87, Q88, R1877

Remove Q90 and C1436 ~ C1440. 3/28

Follow Design  
Guide in 6/11.

Change design 5/01 (Follow Chimay)  
Change design. 5/14(Intel check result)

EMI request to add for 150MHz/200MHz  
issue close to U25.1/4

Add in 5/17.(Follow  
DG P.430)

Cause something wrong , add 1V  
supply back. 5/14

Removed +V1.0M\_LAN 5/01 (Follow Chimay)

Cause something  
wrong , add 1V  
supply back.  
5/14

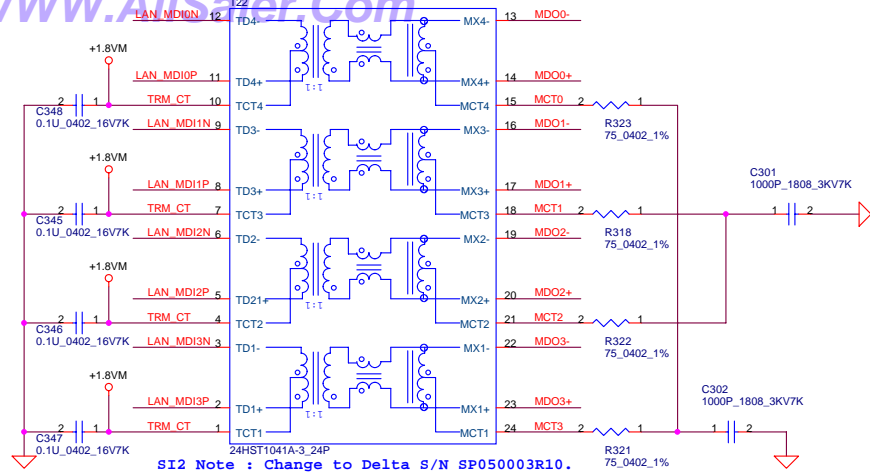
Add in 5/17.(Follow  
DG P.430)

Add in 5/24.

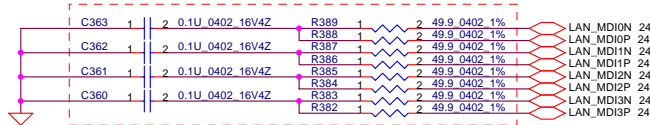
EMI request to change C1421 to 680P  
and close to U25. 1/5

EMI request to add for 150MHz/200MHz  
issue close to R1894.1/4

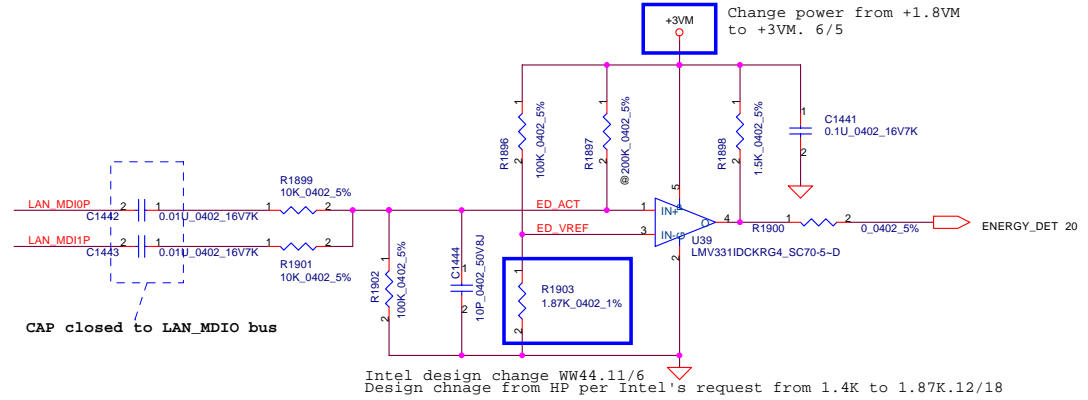
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Layout Notice : Place termination as close as Intel 82566 as possible

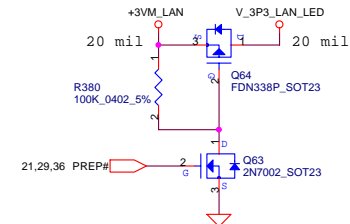
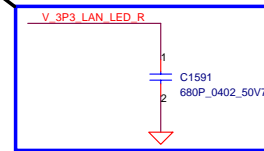
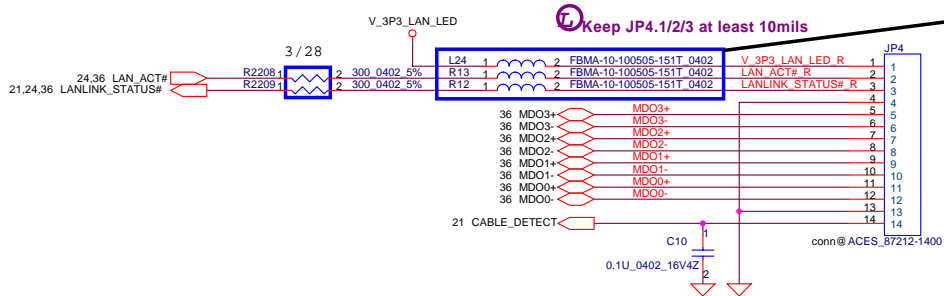


## LAN ENERGY DET



## To RJ-45 CONN.

- EMI request :
1. Add L24 and C1591.
  2. Change R12-R13 to FBMA-10-100505-151T\_0402.
  3. Add R2208, R2209 to have current limit for E-star. 3/28

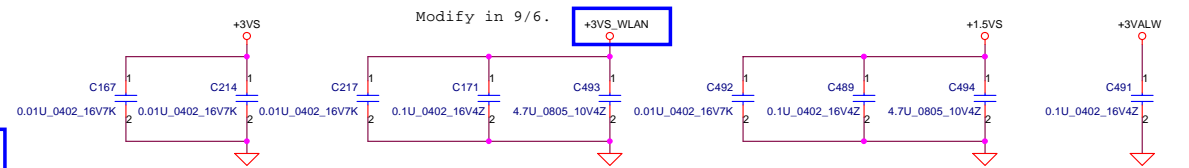
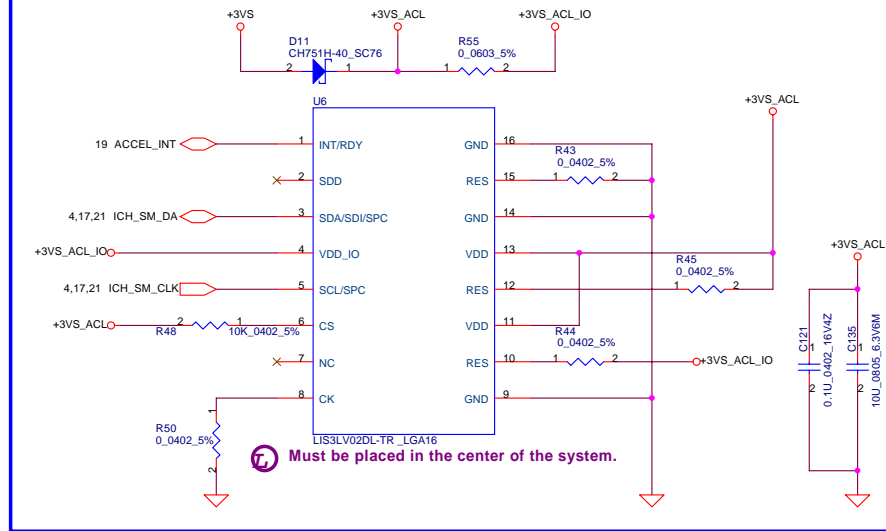


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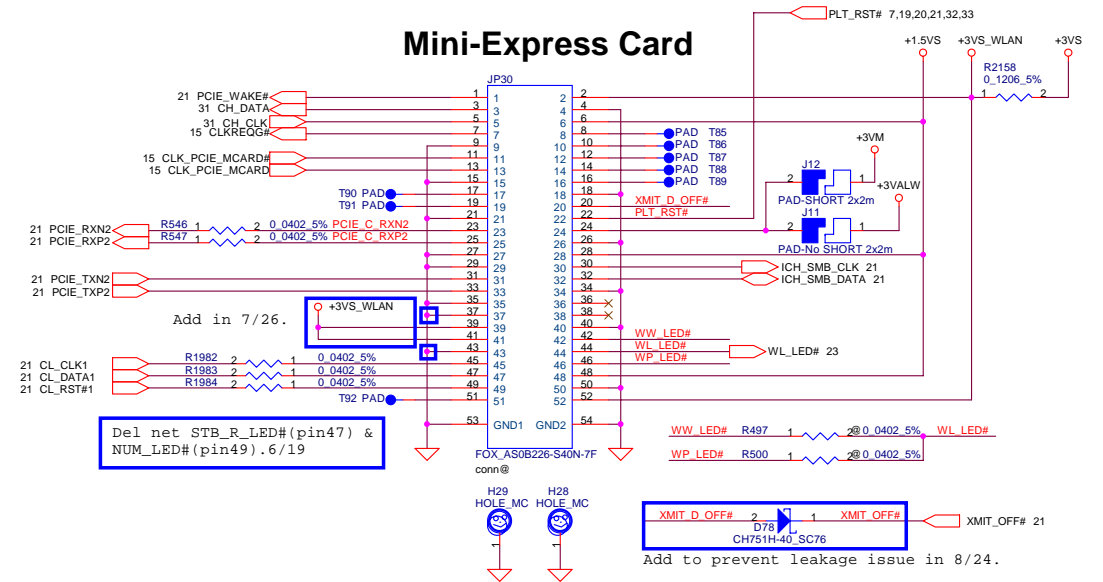


Change U6 to same as Chimay. 7/27

## ACCELEROMETER



## Mini-Express Card



Chnage Design , Del R92 , R104 , R112 , Q17. 5/16

Del +3VL from JP30 pin 45. 6/15

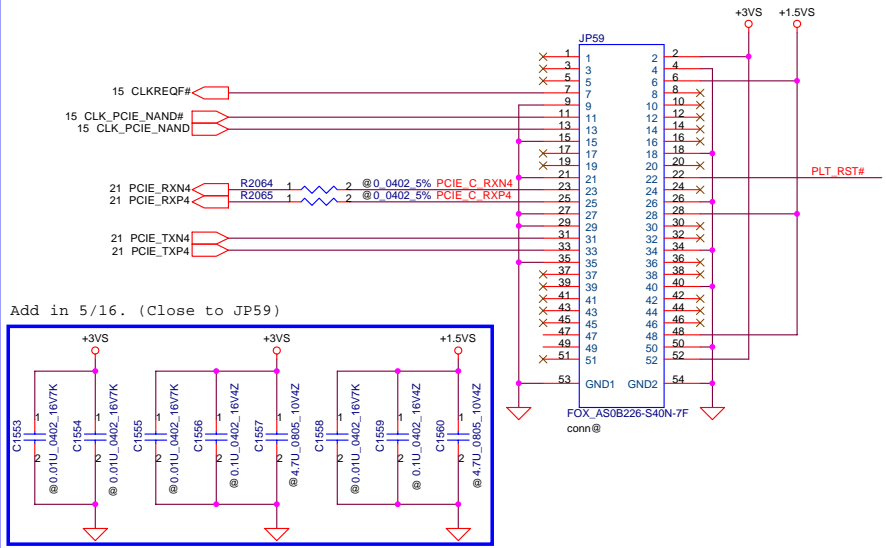
Del net of JP30 pin 8, 10, 12, 14, 16, 17, 19, 51. 6/15

Del resistors & bypass all net as shown in below picture. 5/24

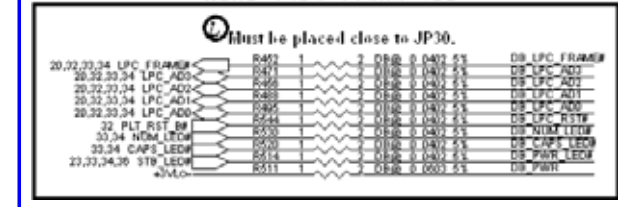
## NAND mini Card(Robson support)

Add in 4/27.

Rerserve from PV build. 3/23

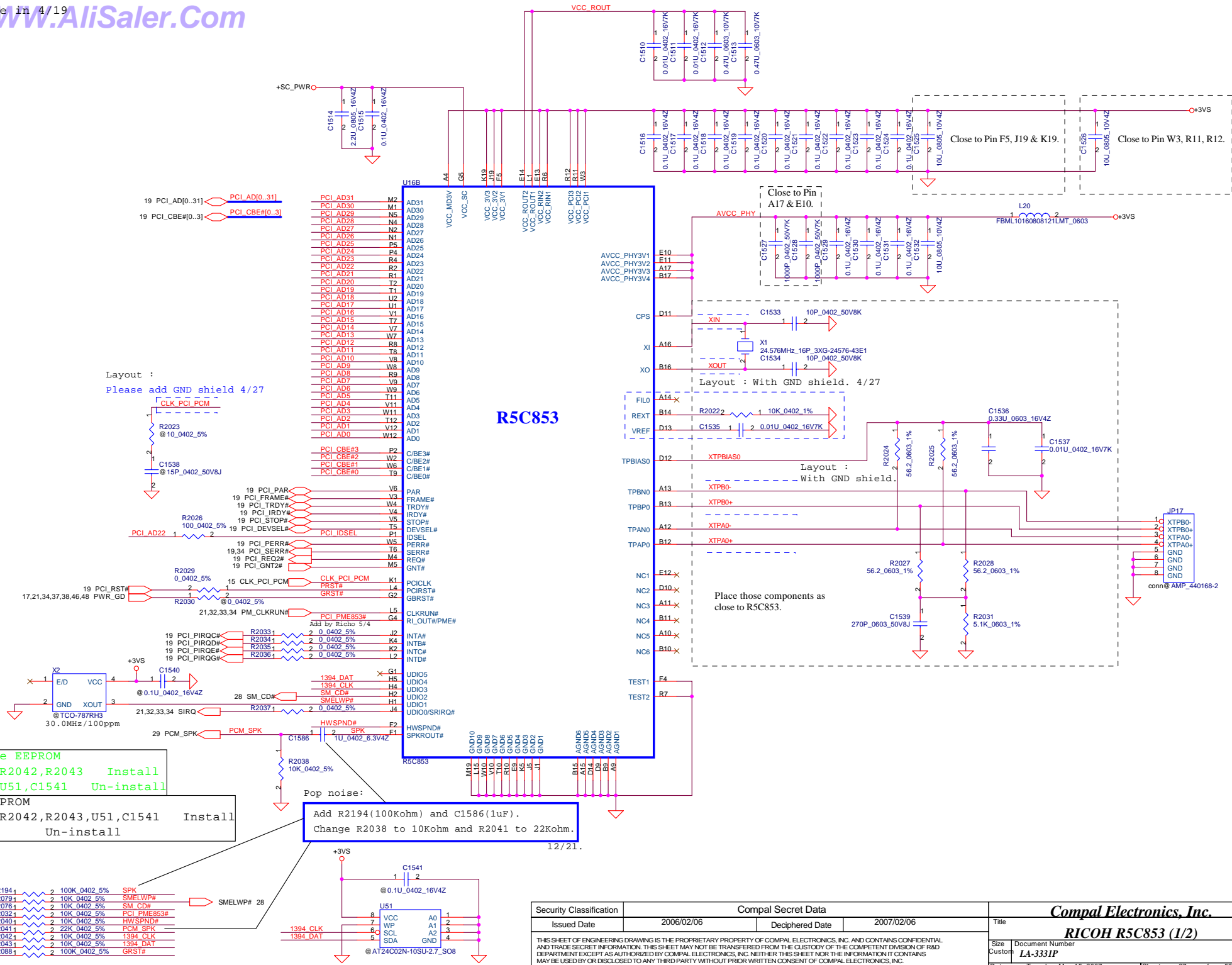


## Mini-Card Stand Off

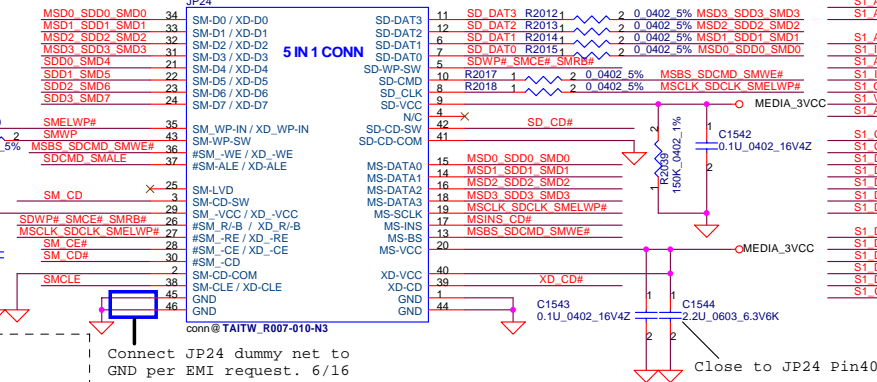
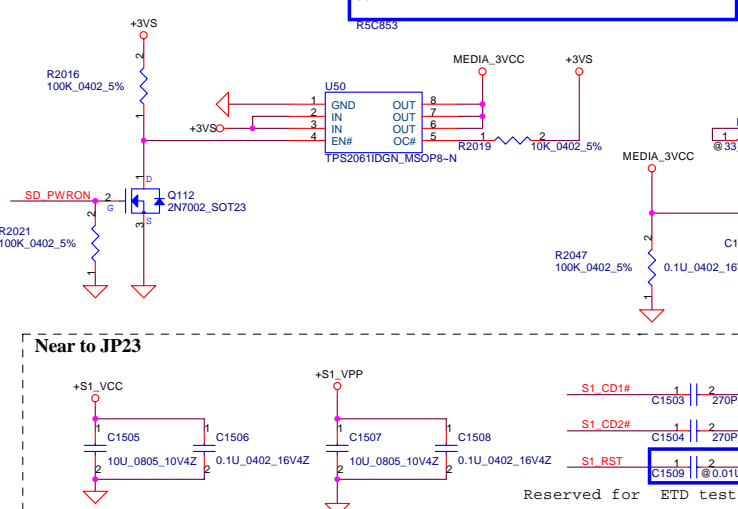
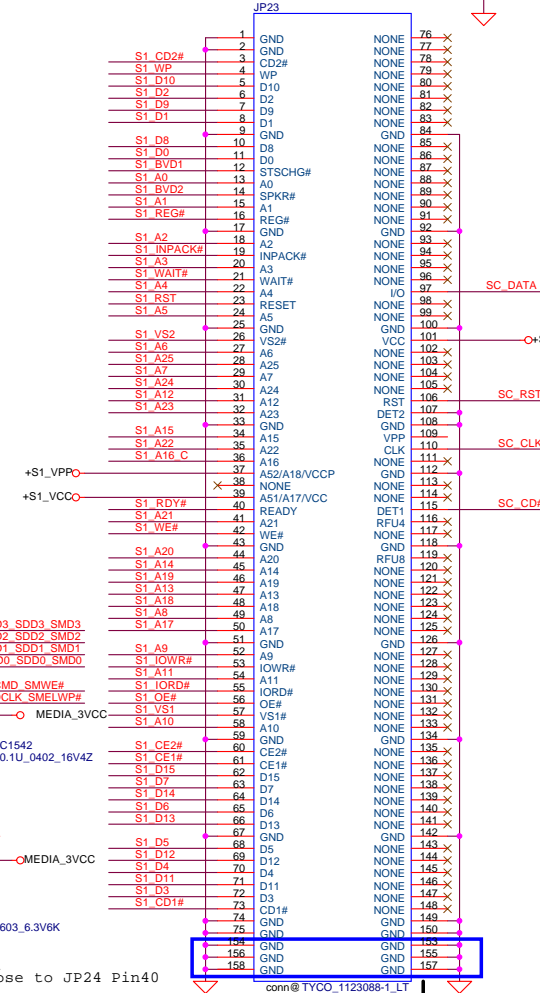
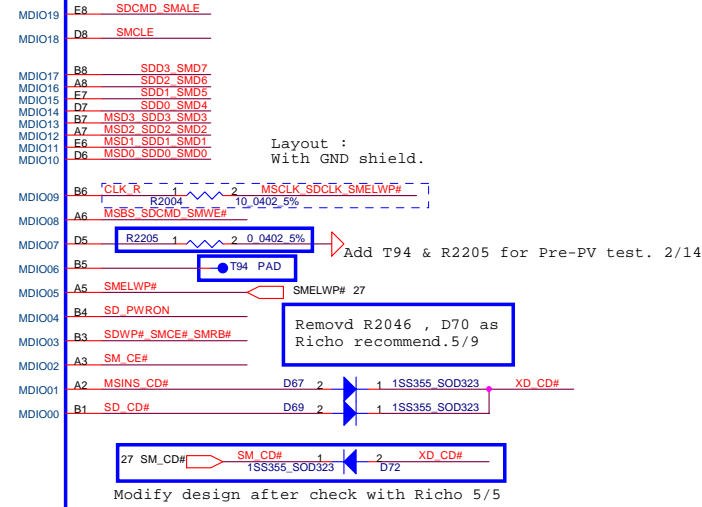
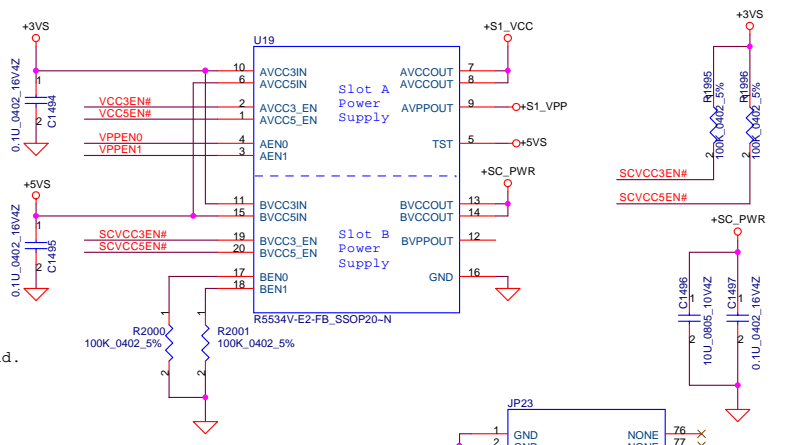
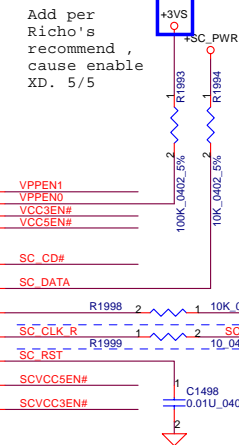
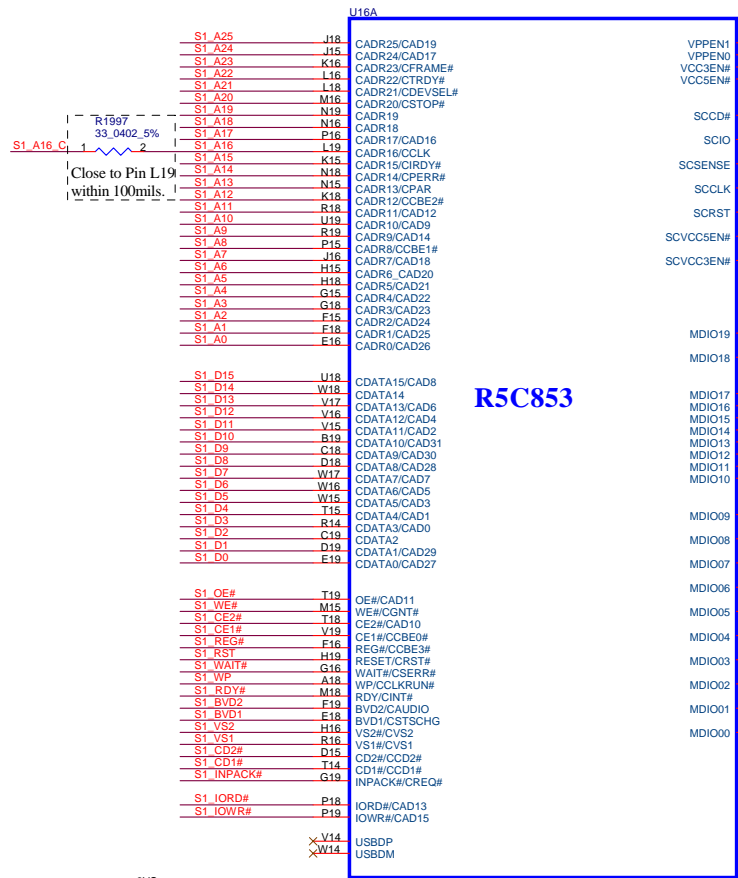


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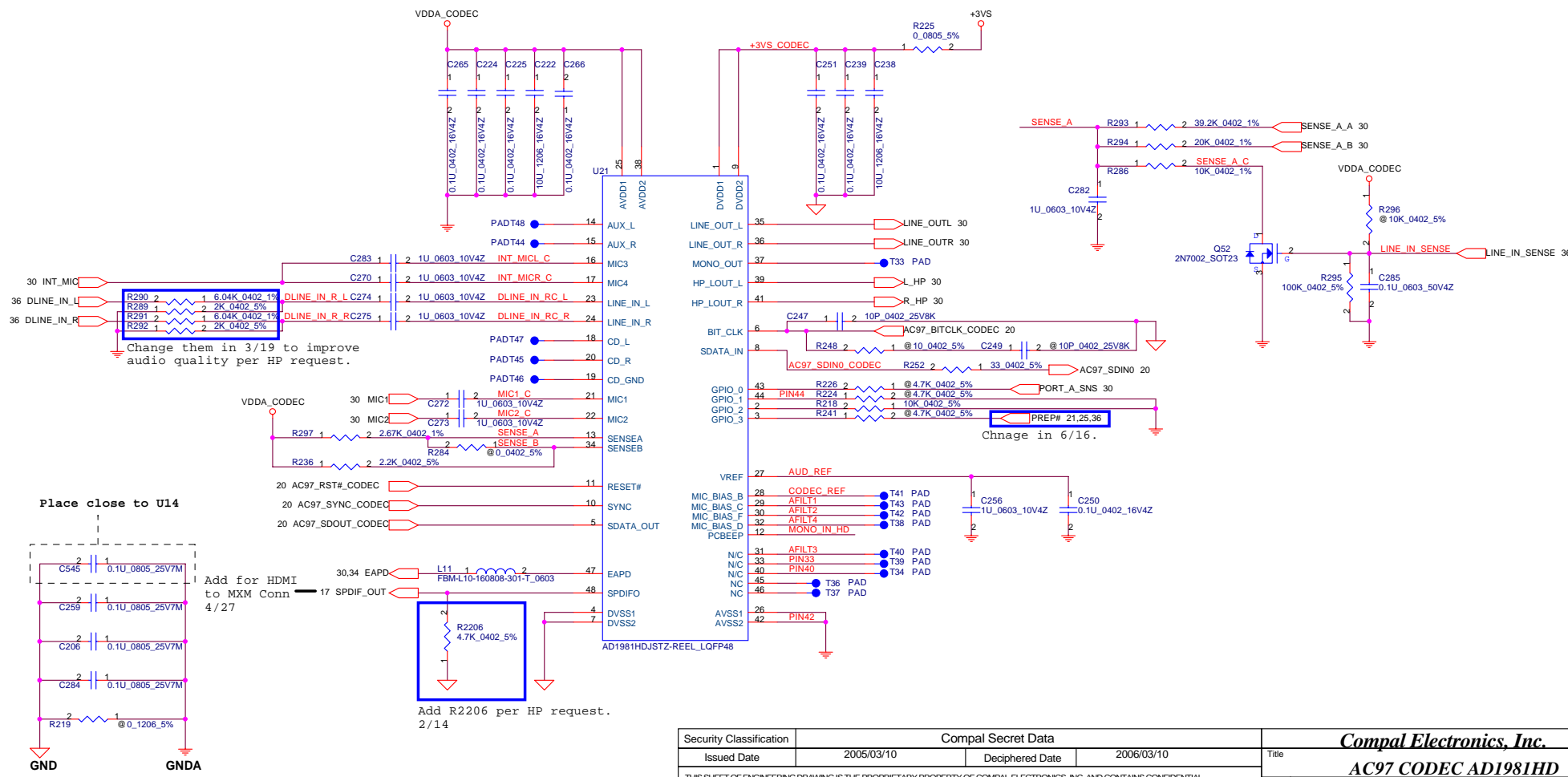
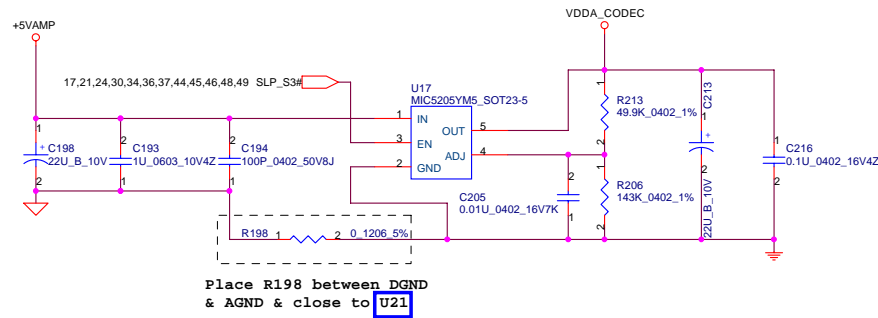
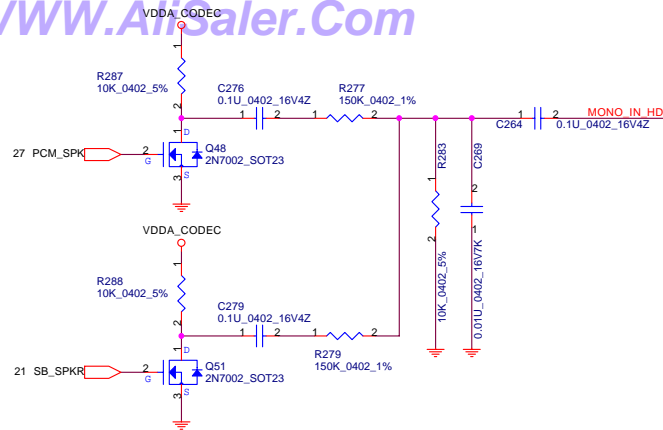


Connect JP24 dummy net to  
GND per EMI request. 6/16

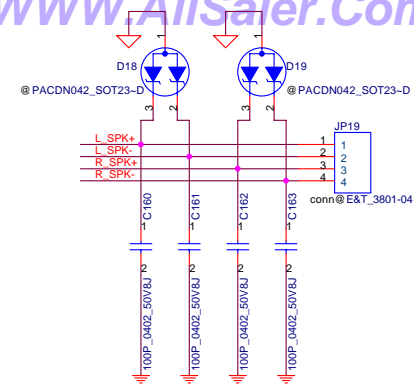
Close to JP24 Pin40

Connect JP23 dummy net to  
GND per EMI request. 6/16

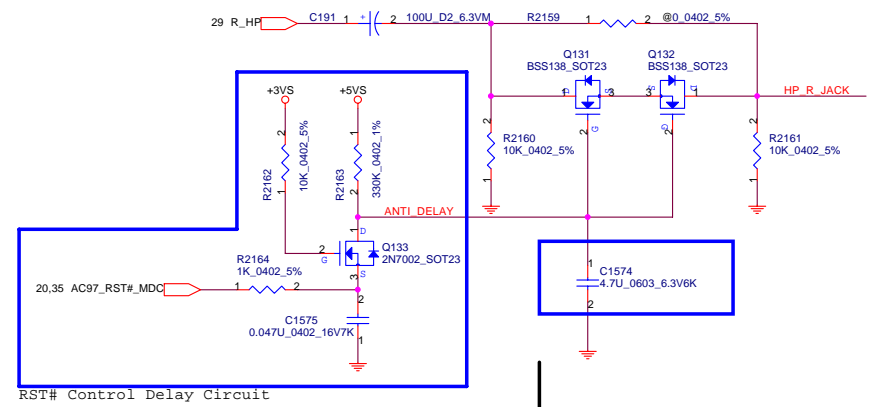
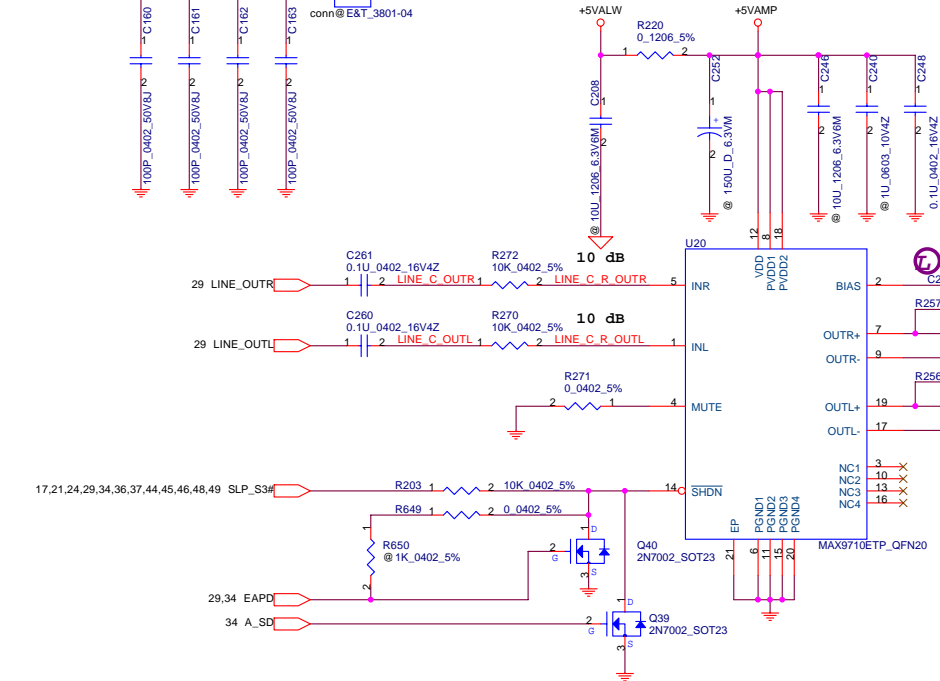
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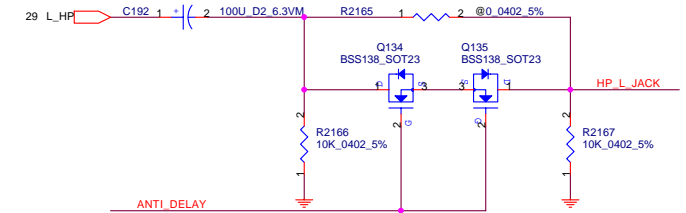
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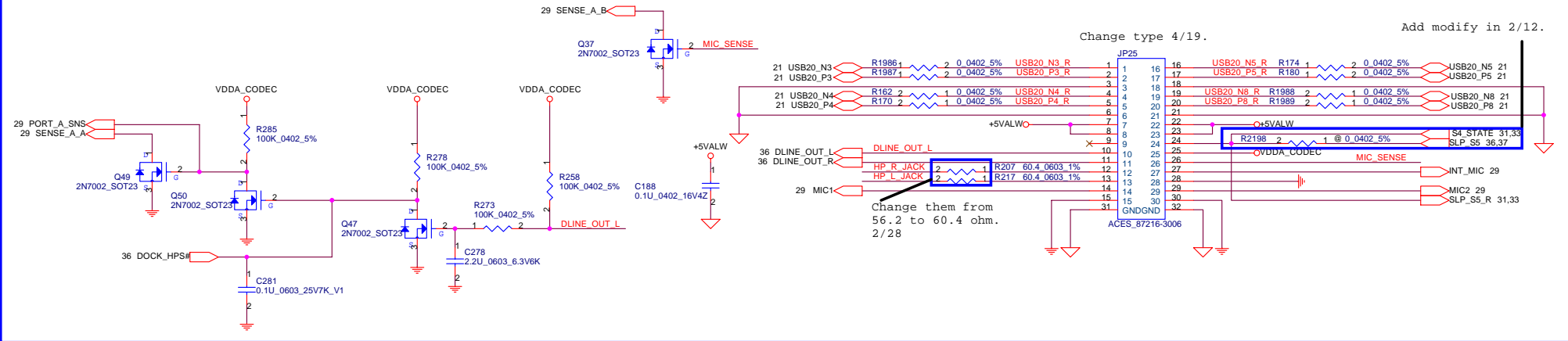
## AMP. FOR INTERNAL SPEAKER



## ANTI POP Circuit (Add in 7/26)

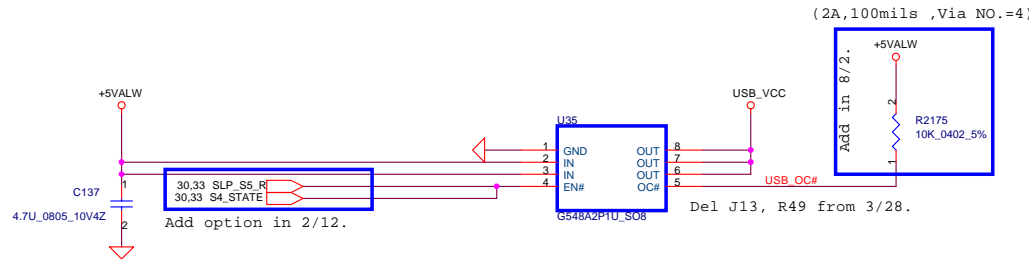
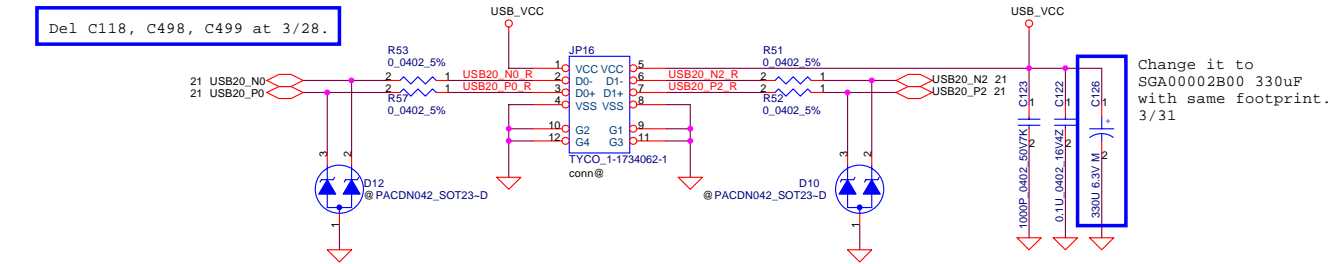


## To Audio / USB Board CONN

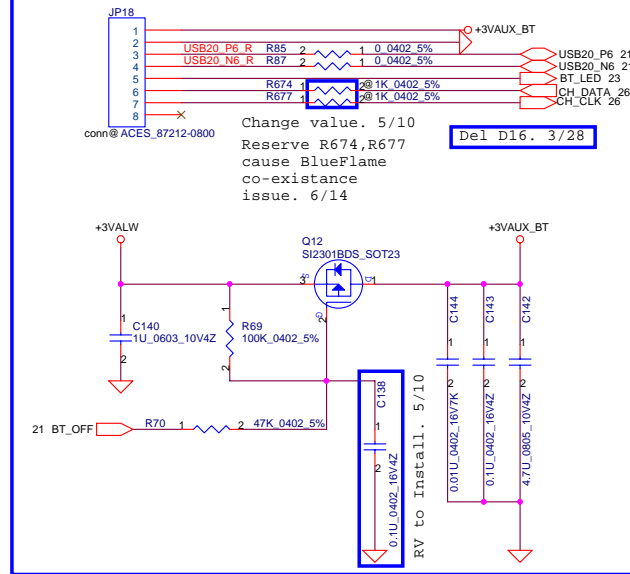


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# USB CONNECTOR 1



## BT Connector



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Date: Tuesday, May 15, 2007				Sheet 31	of 59

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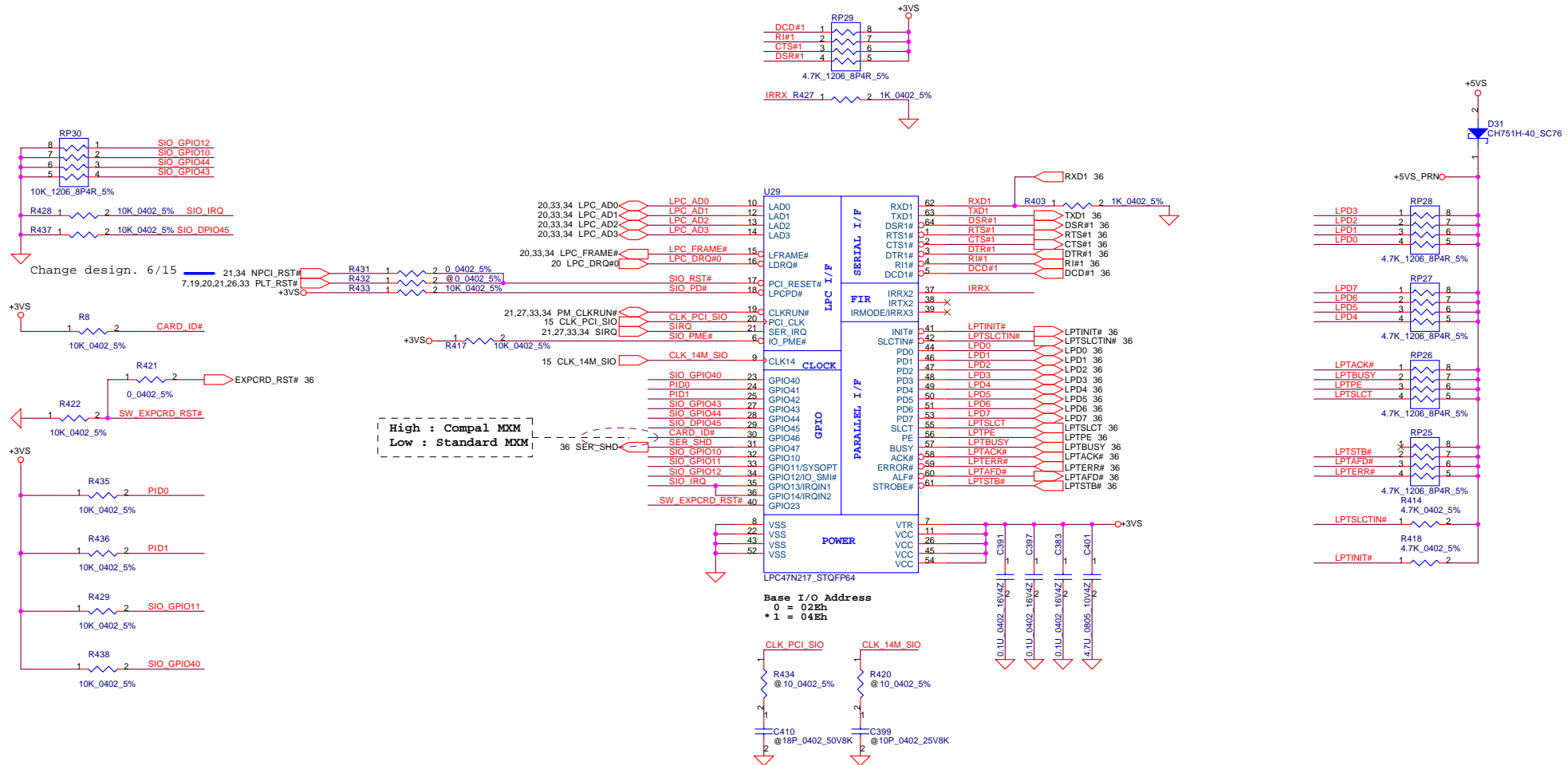
Compal Secret Data

***Compal Electronics, Inc.***

***SUPER I/O LPC47N217***

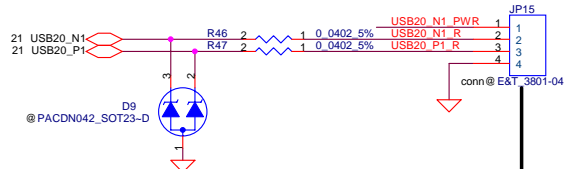
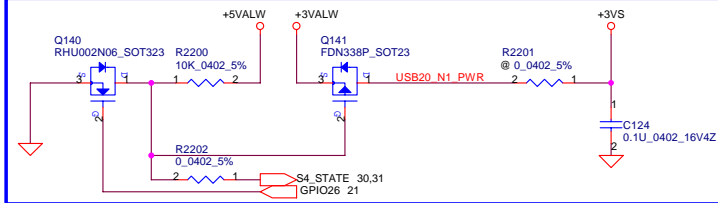
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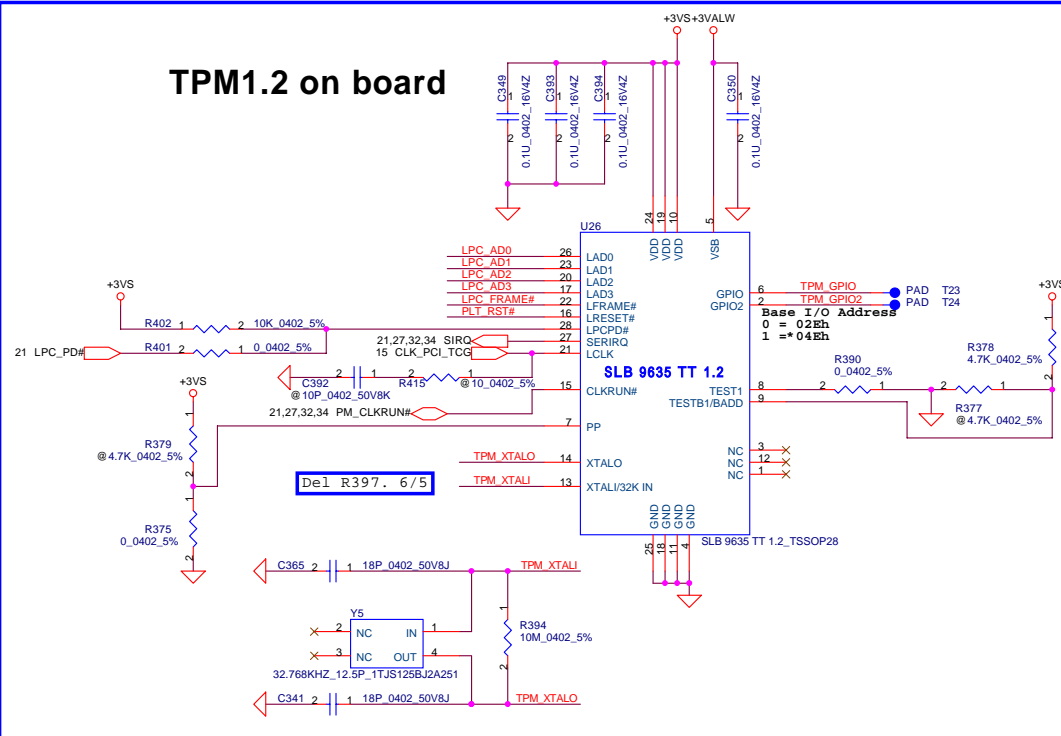


Add change per request for FPR resume in S3. 2/12



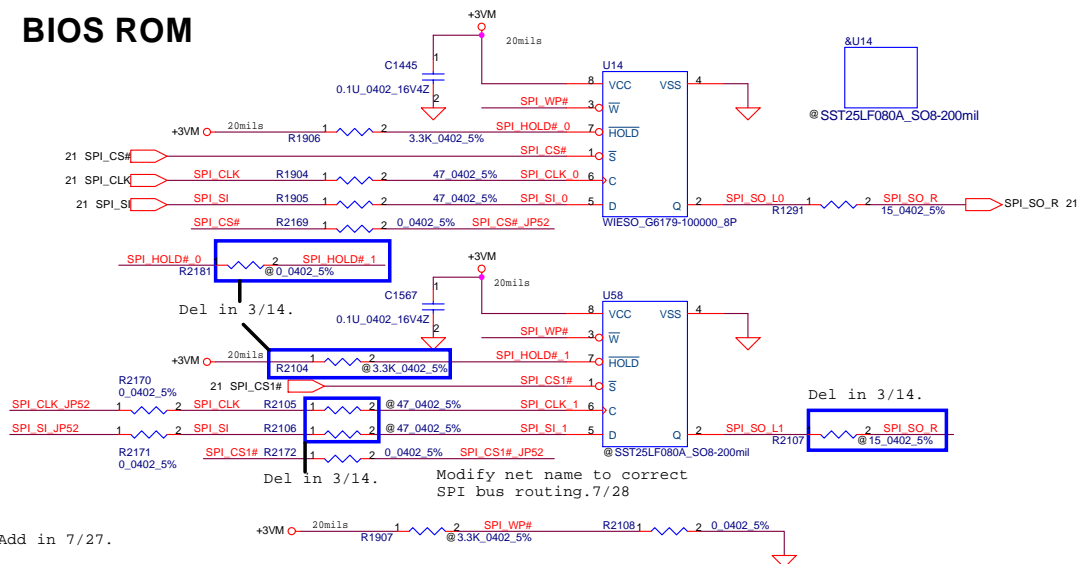
Change connector to same as JP58 per  
ME request. 12/18

## TPM1.2 on board

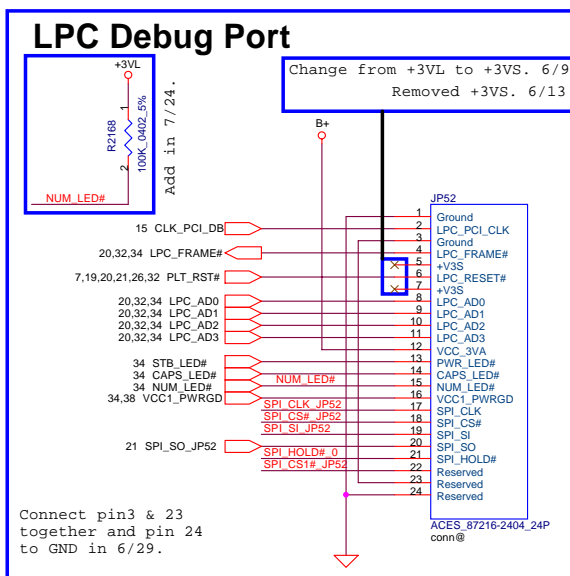


```
# Change SPI ROM to 8Mbit(SA00001JX00) from SI2.
```

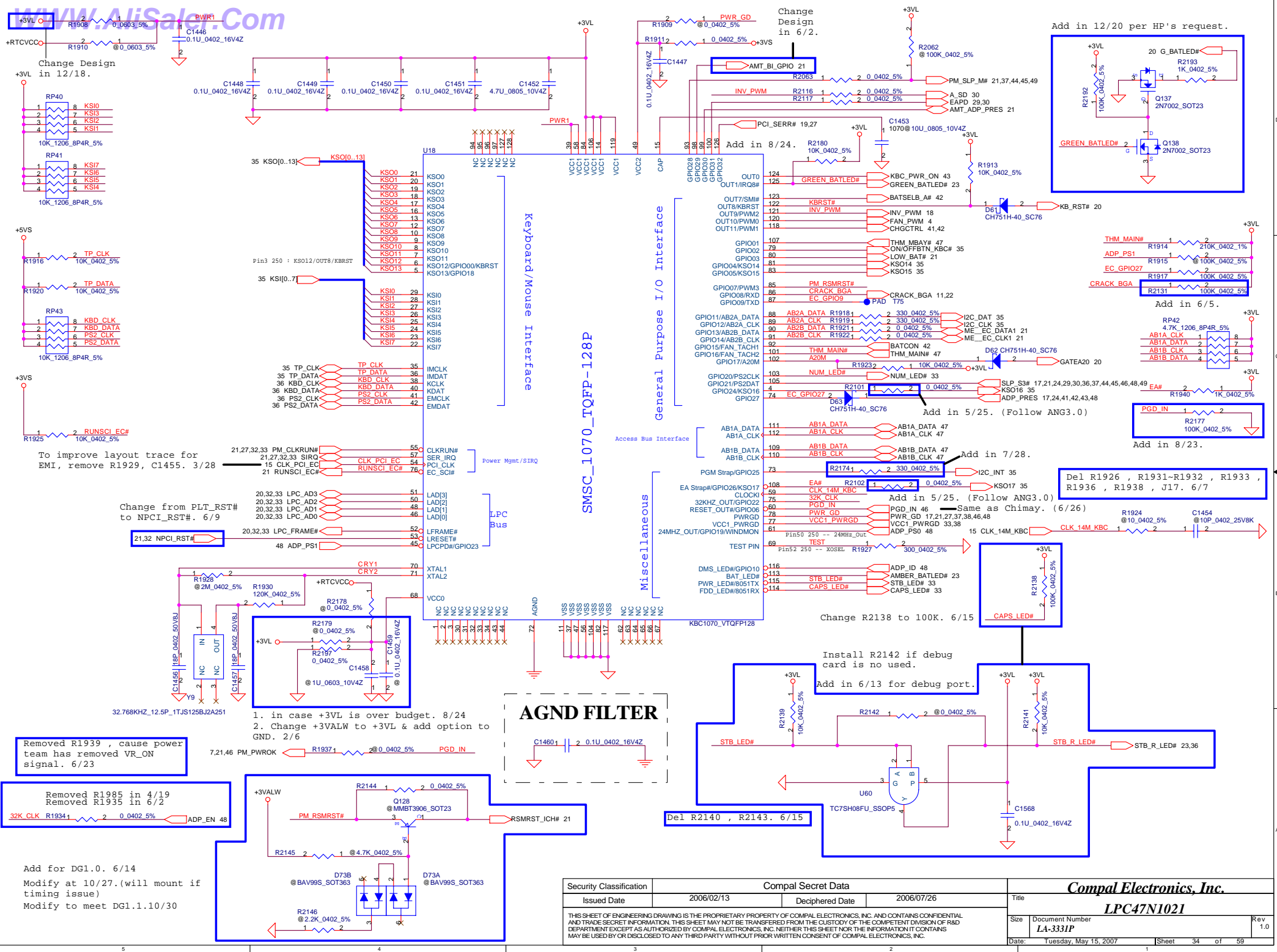
## BIOS ROM



## LPC Debug Port

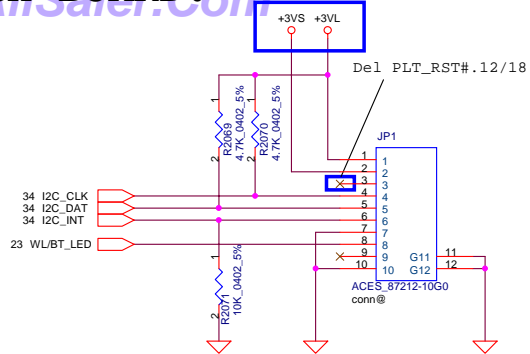


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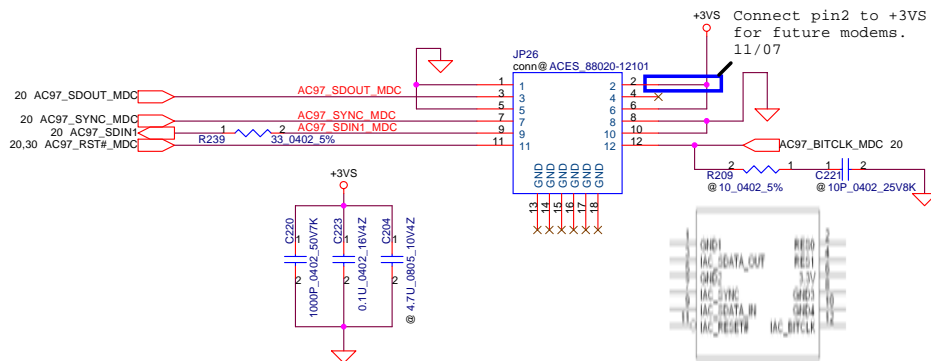


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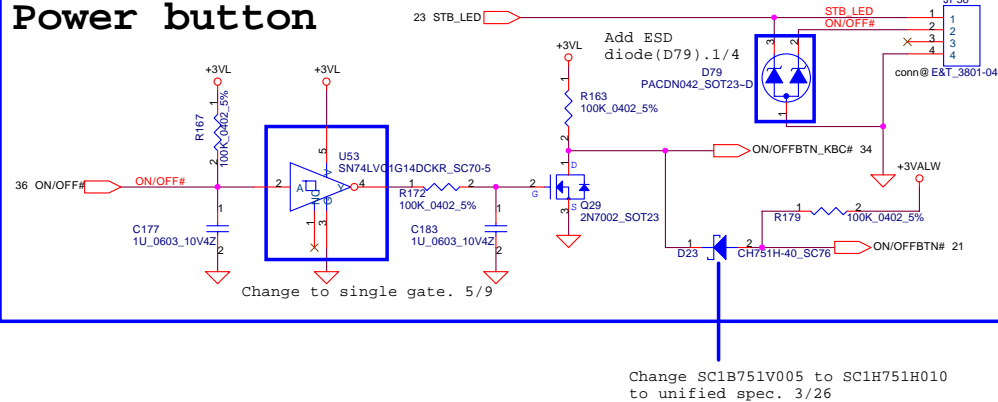
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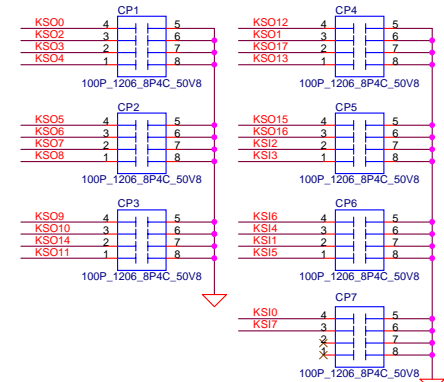
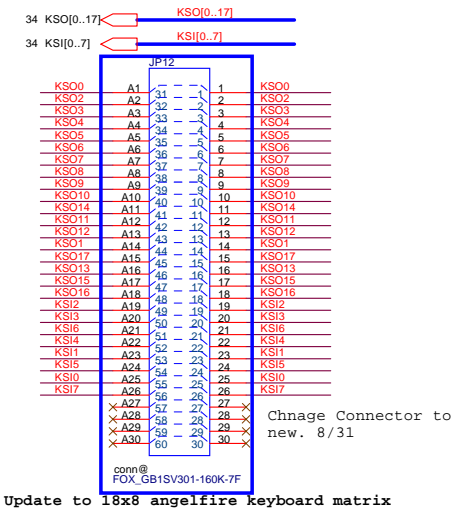
## MDC 1.5 Conn.



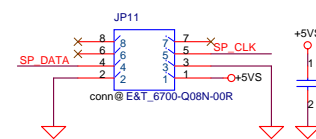
## Power button



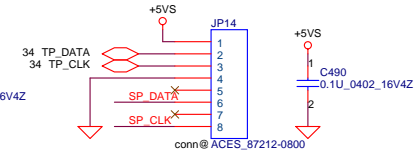
## INT\_KBD CONN.



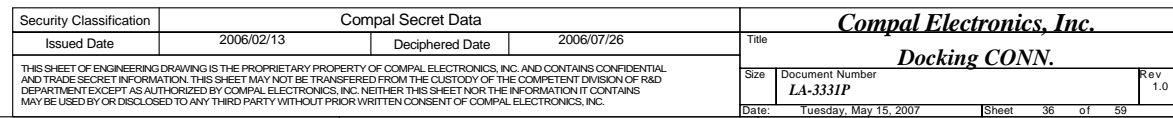
## TrackPoint CONN.



## T/P BOARD.

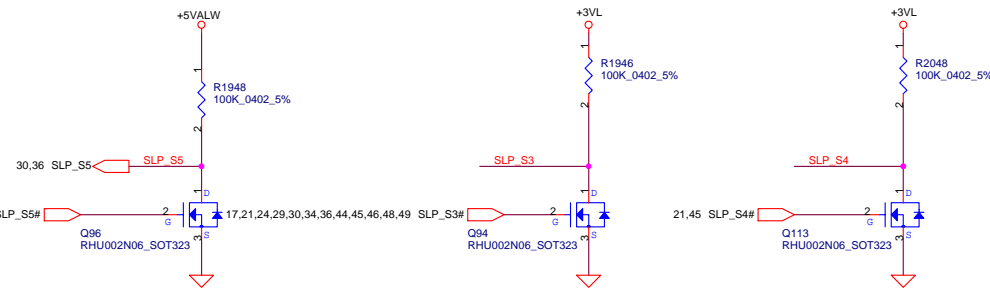


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### Discharge circuit-2 for V-M

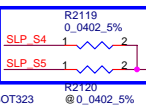


The schematic diagram illustrates the control logic for the motor. It features two comparators, U15D and U15E, and two NAND gates, U11B and U11D. U15D compares the motor speed feedback signal (14) with the reference speed (3VL). U15E compares the motor speed feedback signal (14) with the reference speed (3VL). The outputs of U15D (8) and U15E (10) are connected to the inputs of U11B and U11D respectively. The outputs of U11B (6) and U11D (4) are connected to the inputs of the motor driver (12).

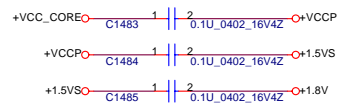
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Change to same as Chimay. 6/2

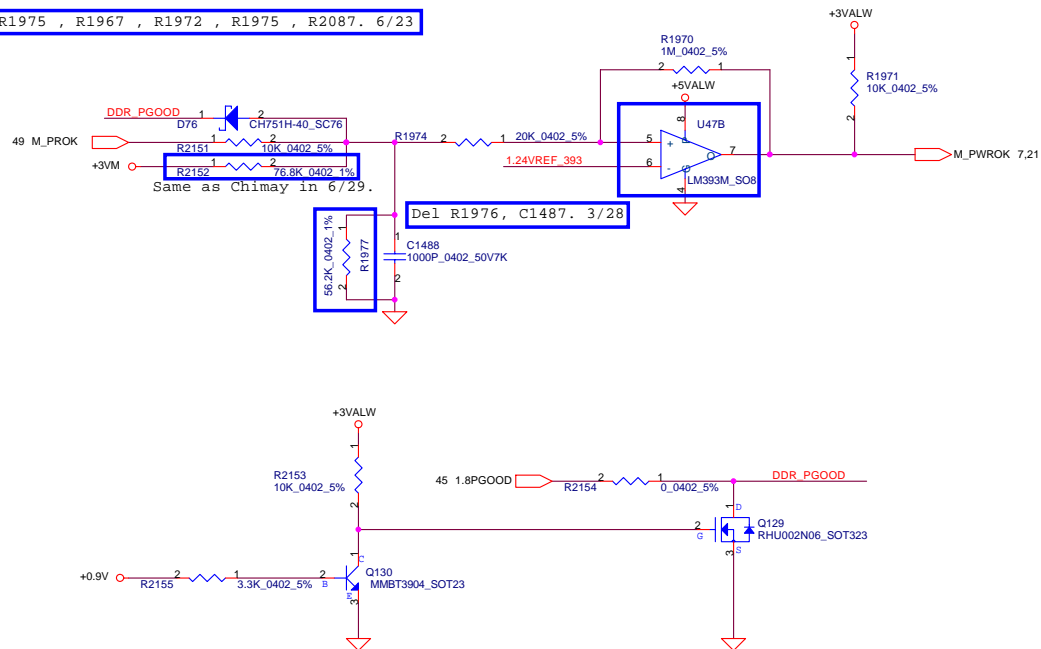
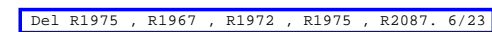
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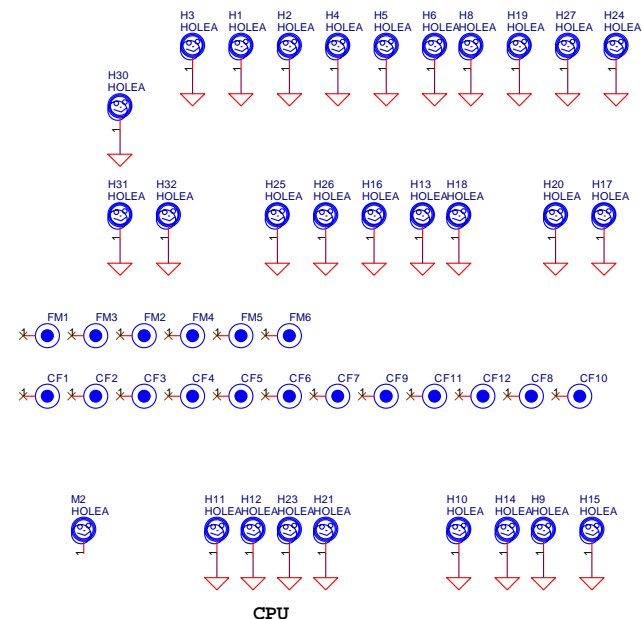
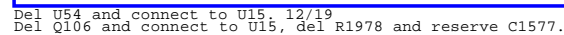
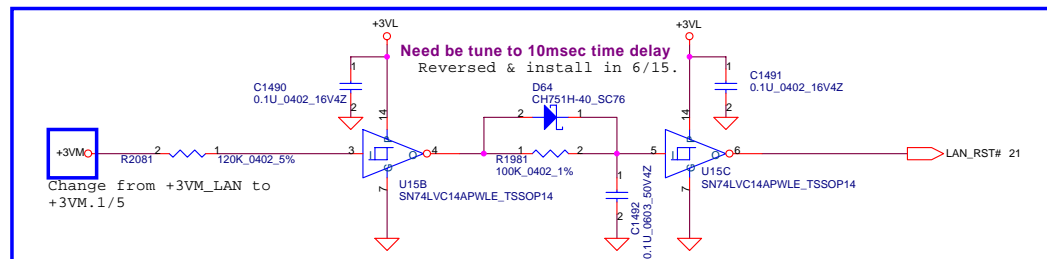
▼ RUNON



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C		D		E		

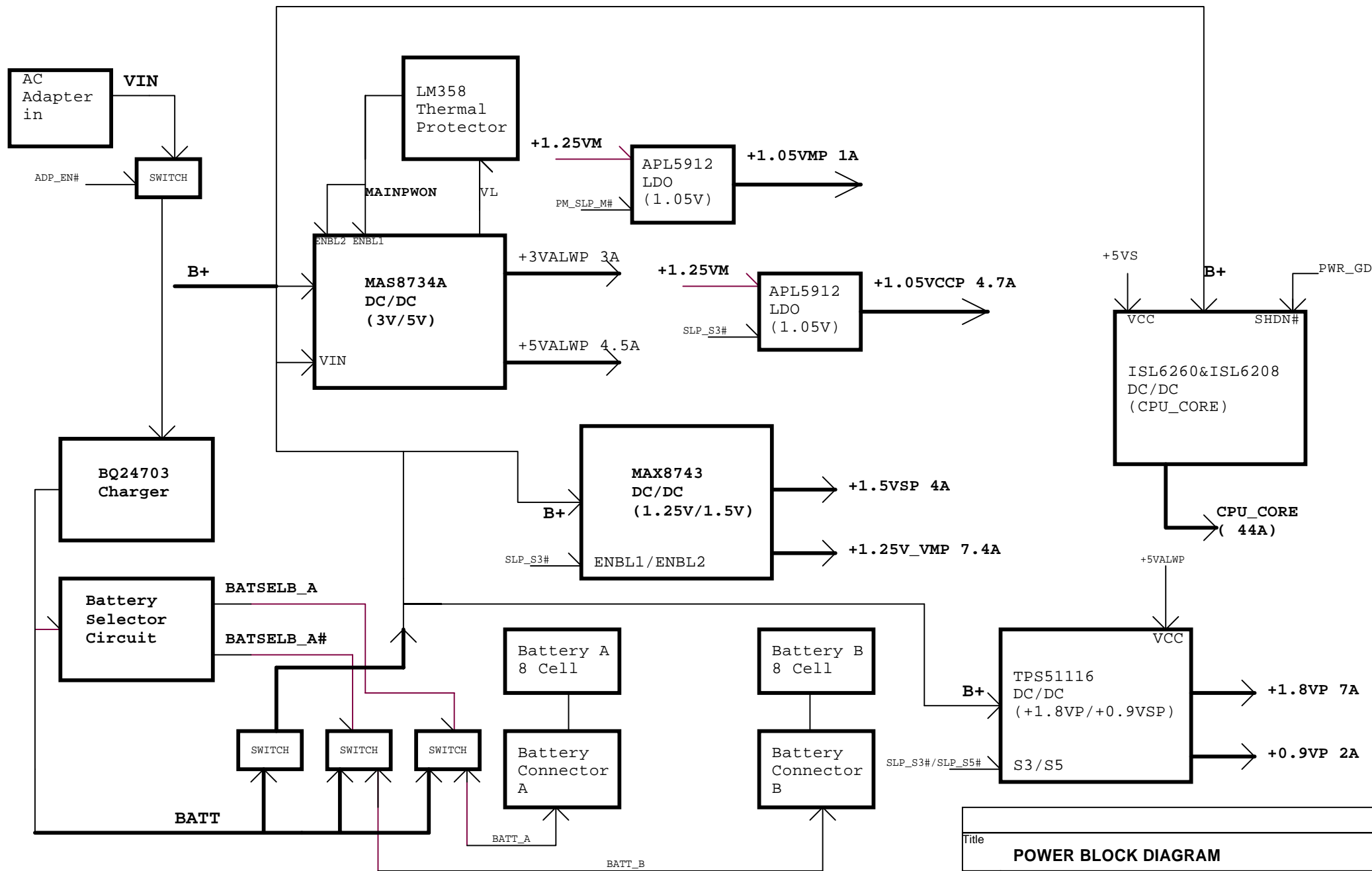


Change to same as Chimay (Del  
R2080 , R1980 , R2082. 6/23  
Modify to same as Chimay 5/5

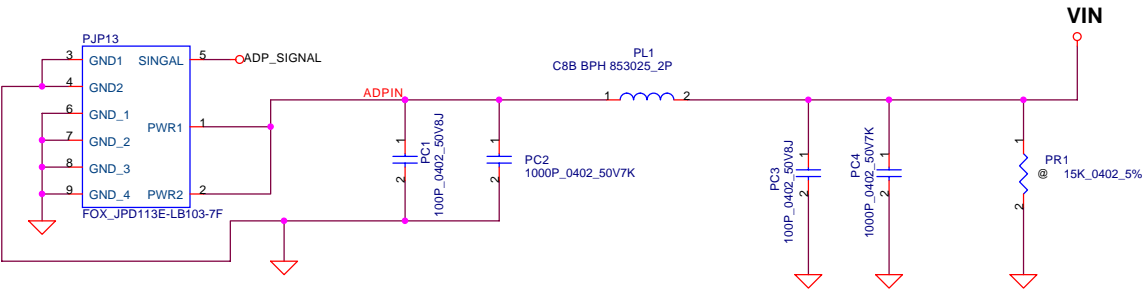


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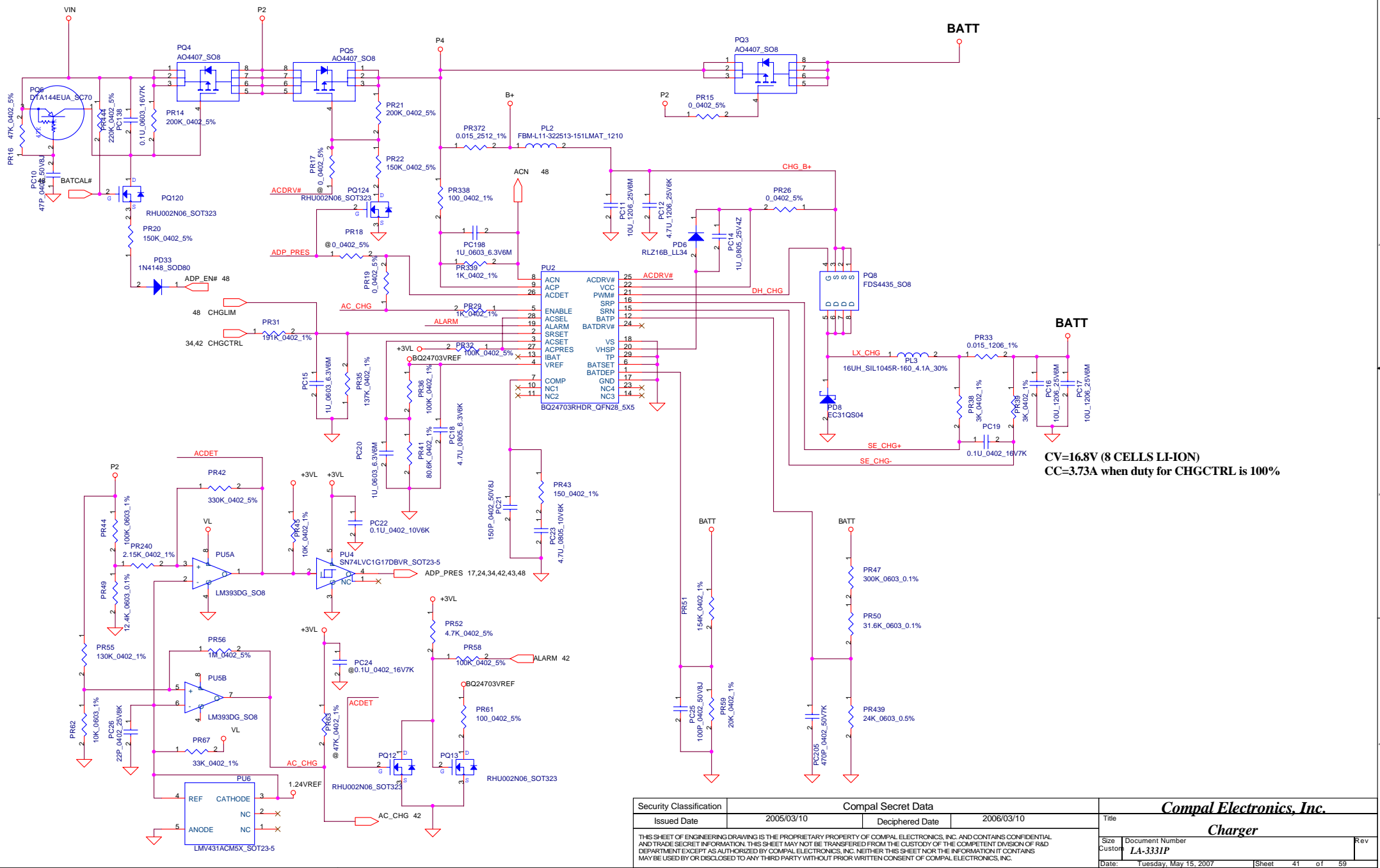




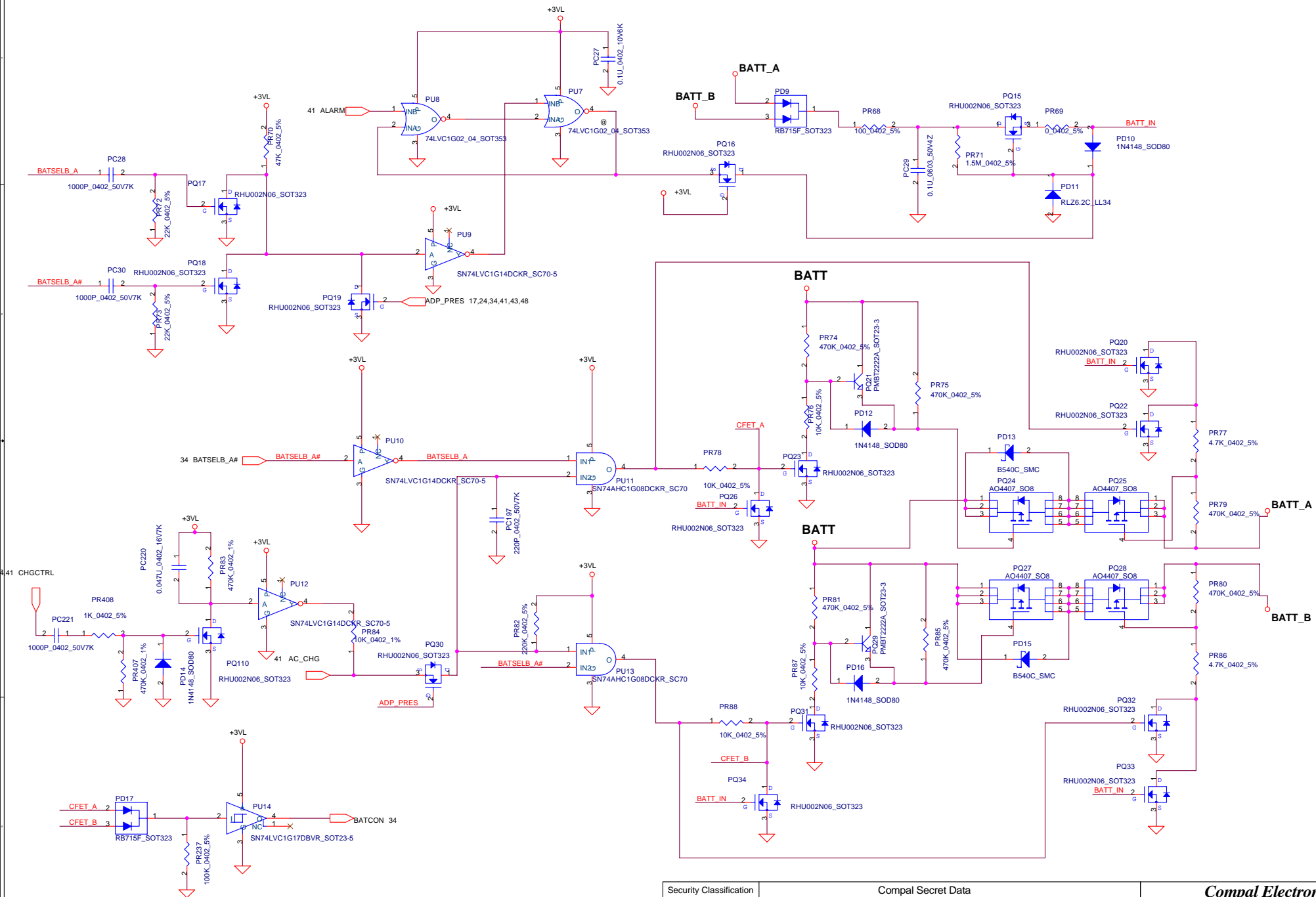
Title		
POWER BLOCK DIAGRAM		
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				Custom	LA-333IP
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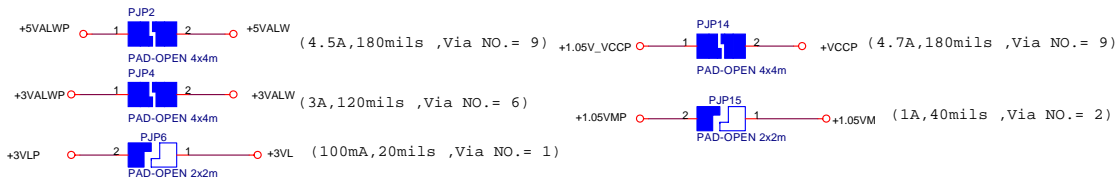
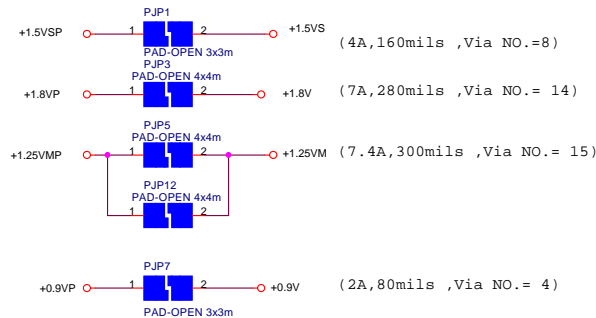


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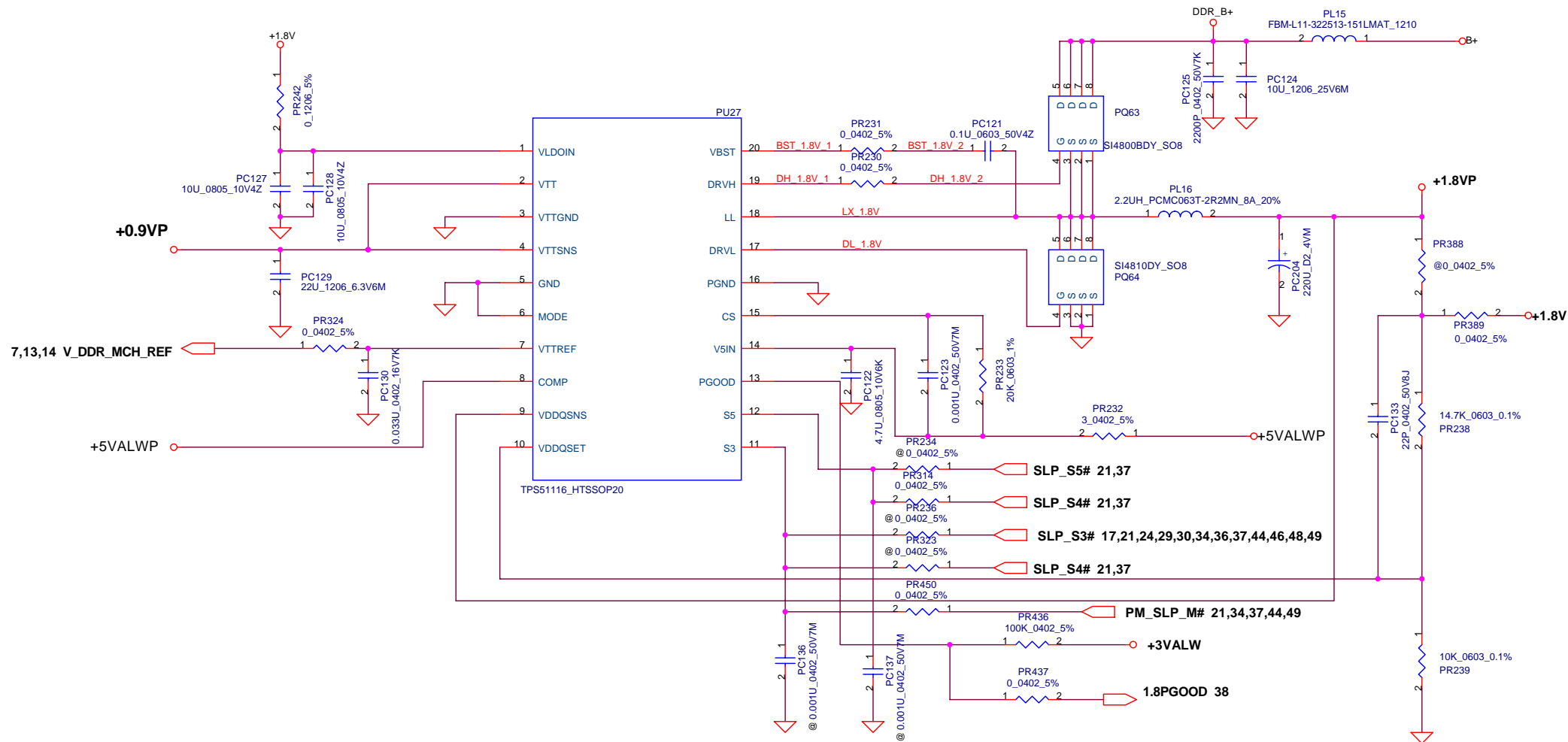
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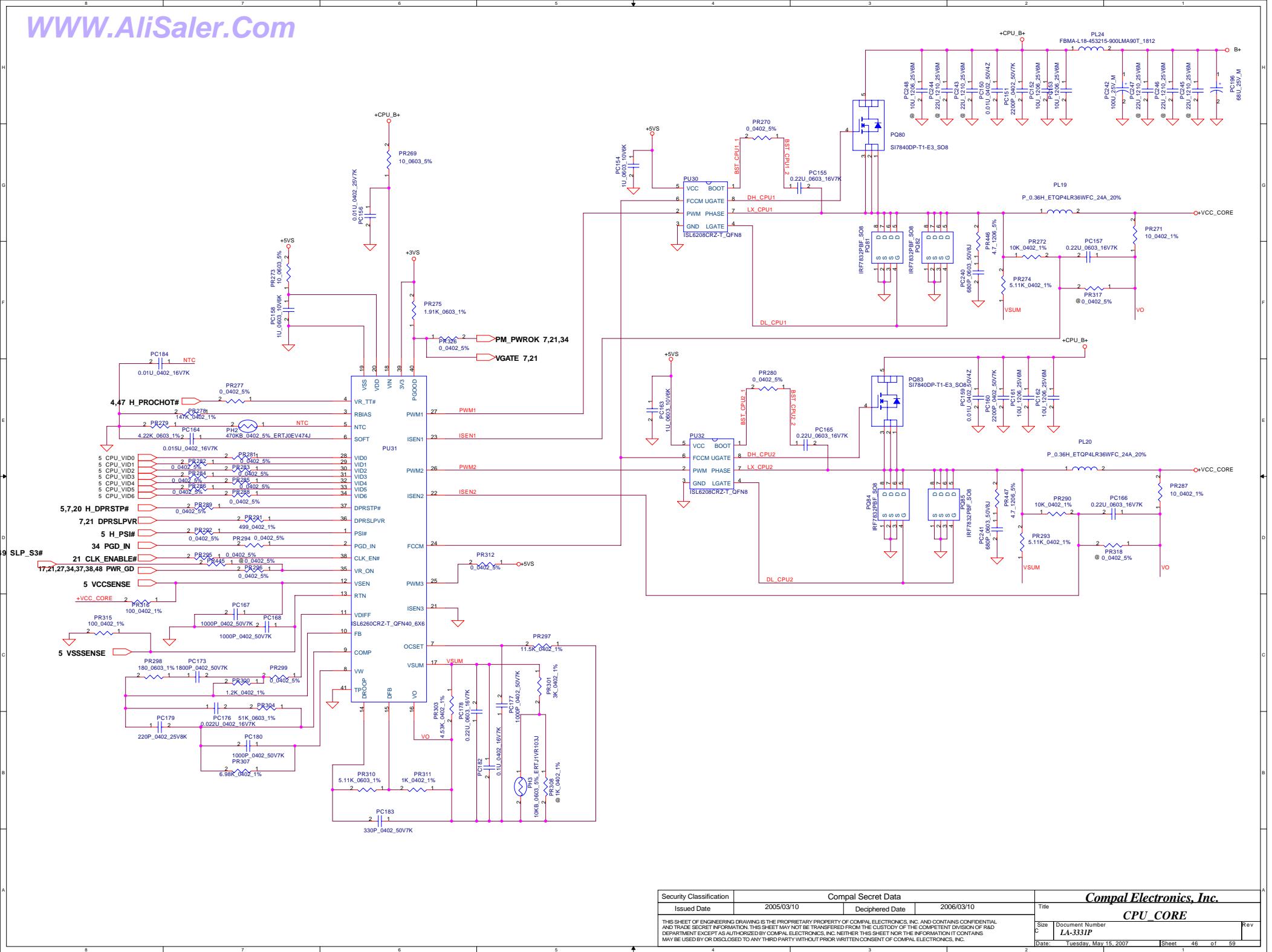


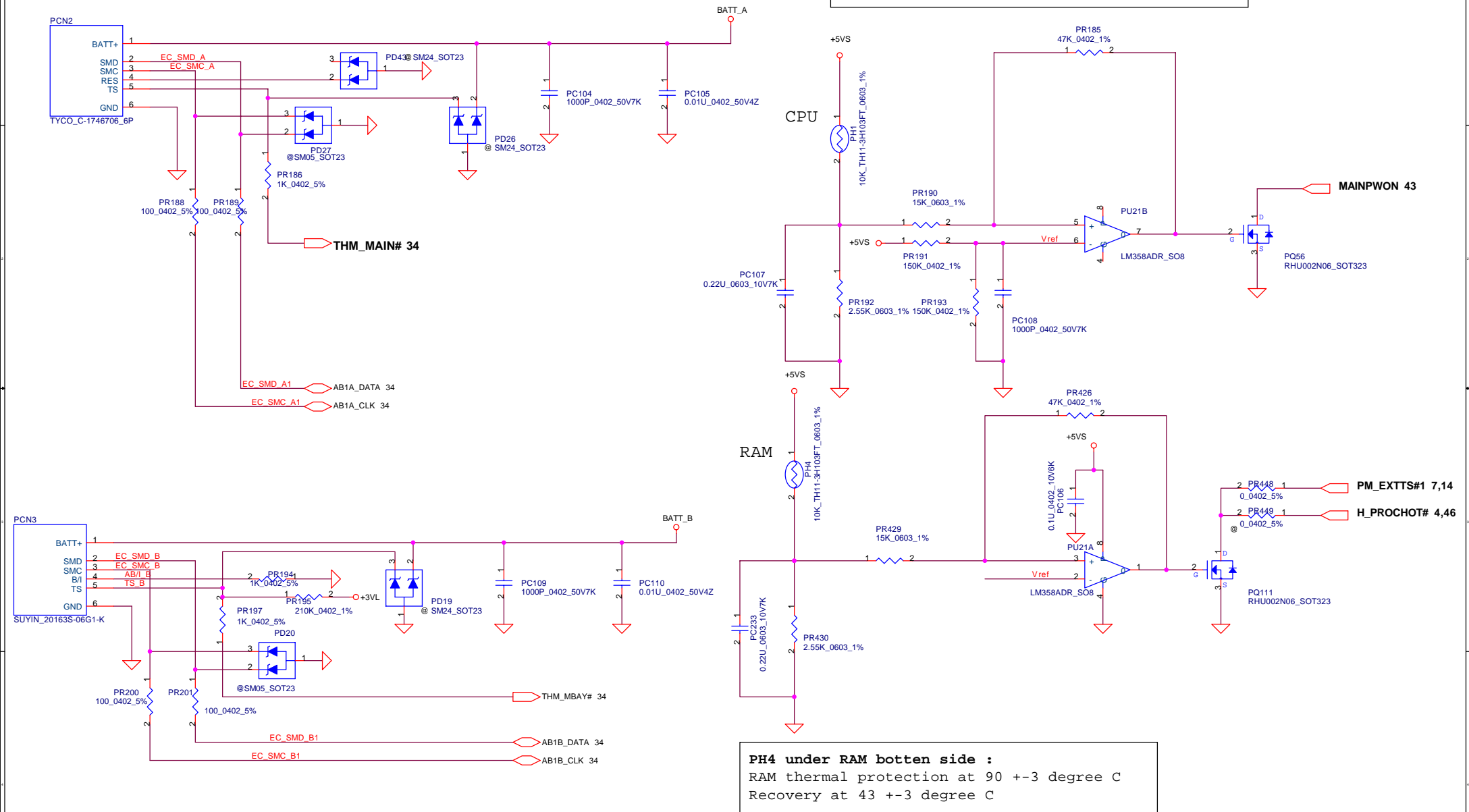
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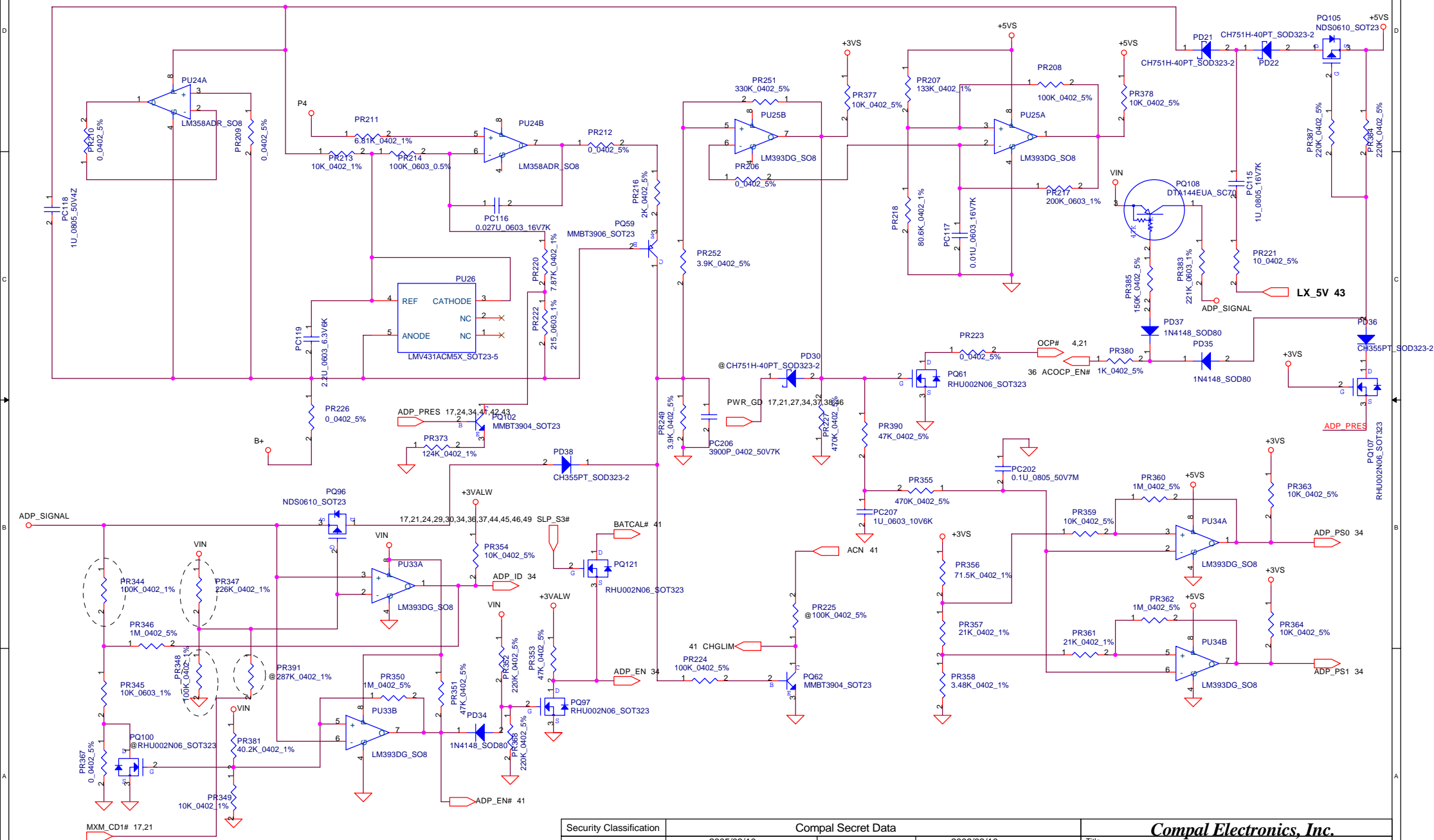


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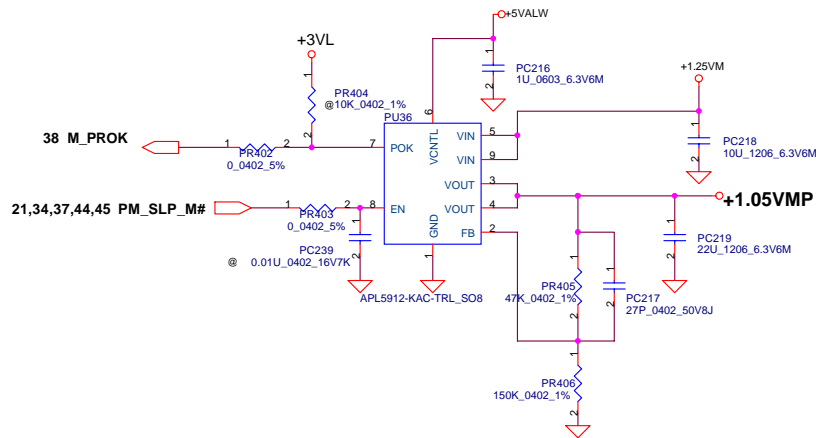
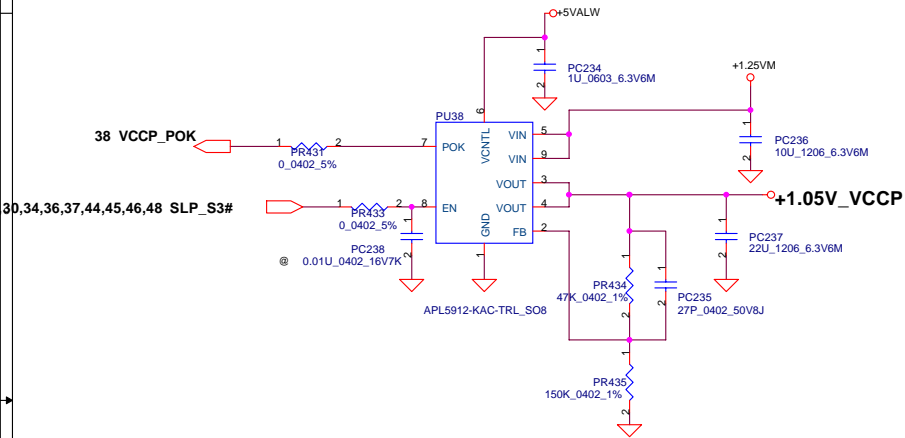




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# Version Change List ( P. I. R. List ) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	Charger	5/9	HP	Remove PQ91,PD32,PR376	Remove PQ91,PD32,PR376	Rev.
2	42	Battery Selector	5/9	HP	Modify battery selector design.	PU12 Change from SN74LVC1G17DBVR_SOT23-5 to SN74LVC1G14DCKR_SC70-5 Add new location PC220 as 0.047uF Add new location PC221 as 1000PF Add new location PR407 as 470K ohm. Add new location PR408 as 1K ohm.	
3	43	3.3VALW/5VALW	5/9	HP	Modify 3.3VALW/5VALW solution	Change solution from TPS51020 to MAX8734A	
4	44	2.5VALW/1.5VS/1.05VCCP	5/9	Compal	Remove 2.5VALW, H/W no need!	Remove PU20, PC72, PC73	
5	47	BATTERY CONN	5/9	Compal Thermal team	Add RAM thermal protection schematic.	Add new location PH4,PC233,PR430,PR429,PR426,PQ111	
6	48	ADP_OCP	5/9	HP	Modify ADP_OCP design	Delete PR379,PQ103,PQ104,PR386,PR382,PQ106	
7	43	3.3VALW/5VALW	5/9	Compal	Modify 3.3VALW/5VALW location for layout.	Swap location PC33, PC44 Swap location PC34, PC45 Swap location PQ37, PQ38, PL5 PL6, PR100, PR104, PC39 , PC199.	
8	44	1.25VM/1.5VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution	
9	49	1.05V_VCCP/1.05VS	5/29	Compal	Layout concern.	Modify 1.05V_VCCP/1.25VM solution.	
10	45	1.8V/0.9VS	6/2	HP	HP request to follow Chimay.	Modify 1.8V/0.9VS schematic.	
11	41	Charger	6/6	HP	HP request!	Modify Charger schematic.	
12	42	Battery selector	6/6	HP	HP request!	Modify selector schematic.	
13	47	BATTERY CONN	6/6	HP	HP request!	Modify main battery power in schematic.	
14	45	1.8V/0.9VS	6/7	HP	At S3 mode, 0.9V need exist, so connect PR242 to 1.8V	Modify PR242 connect to 1.8V	
15	46	CPU_CORE	6/21	HP	HP request.	Modify PU31.35 pin connect to SLP_S3#, originally is connect to VR_ON.	

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# Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	41	Charger	5/9	HP	Change PQ114 to BSS138.	Change PQ114 to BSS138.	
17	47	BATTERY CONN	9/7	Compal	Intel Document for the DDR Module Thermal Diode design	Change the PQ111.1 connection from H_PROCHOT# to PM_EXTTS#1	
18	43/44		11/1	Compal	Dual N MOSFET has failure rate at other project, to reduce Dual N MOS useage.	Change 3V, 1.5V solution, to single N Mos FET solution.	
19	41	Charger	03/29	Compal	Reserve some components for EPA.	Reserve PR21, PR22, PQ124 and PR19.	
20			03/30	Compal	DFx request modify footprint to prevent shift issue.	Modlfy PD10,PD12,PD14,PD16,PD33,PD34,PD35,PD37(SC11N414880) footprint from SOD80 to LL34.	
21			04/02	Compal	For Energy star	Unlstaill UnInstall PR1, PR17 and PR18.And Install PR19,PR21,PR22,PQ124.	
22			04/02	Compal	For ADP OCP setting.	Change PC116 from 0.22U_0603_16V_X7R to 0.027U_0603_16V_X7R.	
23			04/02	Compal	For ADP OCP setting.	Change PR222 from 422 ohm 1% to 215 ohm 1%.	
24			04/02	Compal	For ADP OCP setting.	Change PC117 form 0.027U_0603_16V_X7R to 0.01U_0603_16V_X7R.	
25			04/02	Compal	For ADP OCP setting.	Change PR217 from 604K_0603_1% to 200K_0603_1%	
					Security Classification	Compal Secret Data	
					Issued Date	2006/02/28	Deciphered Date 2007/02/28
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							Changed-List History-1
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# Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	20, 34	BATTERY LED	10/2	HP	GREEN_BATLED# keep high when AC/DC exist.	Change connection between SB & EC.	0.4
2	21	SM Bus	10/3	Compal	SM Bus connection is not correct.	Correct connection of SM bus and reserved R1817, R1820.	0.4
3	35	Function Connector	10/5	HP	Wireless LED always on.	Make change of JP1, pin1-> +3VL, pin2 -> +3VS.	0.4
4	20, 23	Kensington support	10/18	HP	Removed Kensington support.	Remove JP60, Q122, R2084.	0.4
5	18	Quick-Switch	10/18	Nvidia	We will change Quick switch to PI3HDMI412FT-A	Don't need pull up, removed RP44 ~ RP47.	0.4
6	18	Quick-Switch	10/18	HP	Don't have decoupling for U57 1.5VS.	Add C1583, C1584.	0.4
7	34	KBC Debug port	10/18	HP	Don't need use JP55, JP56 for debug.	Removed JP55, JP56 from SI1.	0.4
8	34	RUMRST# timing	10/18	HP	It may don't need these circuit.	Reserve them at SI1.(Install R2144, RV : Q128, D73, R2145~2146)	0.4
9	34	RUMRST# timing	10/18	HP	It different to desg n guide 1.1.	Change R2145 to 4.7k, pull up to +3VALW and connect to Q128 base pin.	0.4
10	34	VCC1 Power	11/02	HP	Chnage Design.	Chnage VCC1 power option to +3VALW or +RTCVCC.	0.4
11	21	LANSTATUS#	11/02	HP	System auto power on after plug AC in.	Add Q136 to isolation U10 directly link to NIC, and add PU R2187.	0.4
12	31	USB Switch	11/03	Compal	Don't need dual layout for USB power switch.	Remove U7, U36.	0.4
13	30	Audio	11/03	HP	To pass Vista test of Audio.	Change R207, R217 from 15ohm to 56.2ohm.	0.4
14	25	LAN	11/06	Intel	Intel Santa Rosa Platform Message of the WW44	Change R1903 from 3.92Kohm to 1.4Kohm.	0.4
15	24	LAN Connector	11/06	Compal	EMI issue for LANLINK_STATUS#, LAN_ACT#.	Mount C1581, C1582 --> 680pF(0402).	0.4
16	17	MXM Connector	11/08	HP	Need BOM option of SLP_S3# for use G71 or G84.	Add R2190(0ohm).	0.4
17	4	Thermal Senser	11/08	HP	Abita will chnage to new Thermal senser in the future.	Add R2188, R2189(0ohm).	0.4
18	35	MDC	11/08	HP	Implement new MDC future.	Connect JP26.2 to +3VS.	0.4
19	15	FSB Freq Selector	11/09	HP	Need HW option for 667MHz or 800MHz	Add JP62, JP63 and install R1689,R1696,R1705,R1737 and reserve R1694,R1716,R1734.	0.4
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21	37	M-Power discharge	11/10	Compal	It's wrong connection of discharge control circuit.	Correct Q97, Q98, Q99 pin2 connect to LAN_WOL_EN#.	0.4
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# Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	33	FP Connector	12/18	Compal	ME ask to change FP connector.	Change FP connector(JP15) to same as JP58.	0.5
2	34	KBC	12/18	HP	System can't power on.(PWR1 connect to +3VALW)	PWR1 will modify connect to +3VL(R1908.2).	0.5
3	35	PLTRST/CBB	12/18	HP	Capacitive Button Board may not need PLTRST.	Disconnect PLT_RST# from JP1.3.	0.5
4	38	KBC Power good	12/19	HP	VCC1_PWRGD have glitch when plug AC/DC power.	Del U54, Q106 and R1978, replace by U15.	0.5
5	25	LAN ENERGY DET	12/19	Intel	Intel request chnage value of R1903.	Change R1903 from 1.4K to 1.87Kohm.	0.5
6	38	PWR_GD	12/19	HP	Ripple noise to cause system auto shutdown issue.	Add C1585(0.1uF) and R2191(1Kohm).	0.5
7	34	KBC	12/20	HP	Current design may possible to damage the KBC.	Change design to add Q137, Q138(2N7002) and R2192(100Kohm), R2193(1Kohm).	0.5
8	27	Card bus Controller	12/21	Compal	There is pop noise when plug some PCMCIA card.	Add R2194 and C1586 and change value for R2038 and R2041.	0.5
9	24	NIC	12/21	Intel	82566MM may have start-up issue with Crystal.	Modify layout and add R2195(0ohm).	0.5
10	24	ACBS	01/02	Intel	To enable IAMT and support ACBS.	Mount Q85 and R2072 but remove Q87~Q88 and R1877.	0.5
11	35	Power Buttom	01/04	Compal	ESD test is not good for Switch board.	Add ESD diode(D79) to M/B and add ME solution.	0.5
12	24	NIC	01/05	Compal	EMI test is fail from NIC.	Add C1587~C1590, L24 and change C1421 to 820pF, R12~R13 to FBMA-10-100505-151T.	0.5
13	38	LAN Reset	01/05	HP	HP request to modify.	Change this power rail from +3VM_LAN to +3VM.	0.5
14	18	Quick-Switch	01/07	HP	There is leakage issue of Q-Switch.	Add D80 for this issue.	0.5
15	37	MXM	01/10	HP	MXM board need external +2.5VS power rail.	Add U62, C1592, C1593 for this issue.	0.5
16	37	MXM	01/11	HP	2.5VS for MXM is too long.	Reserve C1594(0.1uF) close to pin.	0.5
17	37	MXM	01/12	HP	Leakage issue from MXM pin211(ADP_PRES)	Add Q139(RHU002N06) & R2196(8.2K).	0.5
18							0.5
19							0.5
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# Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	USB Connector	02/07	Compal	Not need 40 pin connector for USB/Audio connector.	Change JP25 from 40pin to 30pin.	0.6
2	34	KBC VCC0	02/07	Compal	Can't power on and AC power LED always light.	Change R2179 connect to +3VL, and add option R2197 to GND.	0.6
3	33	FPR/USB S3/S4	02/12	HP	Change control method for FPR/USB power in S3/S4.	Add R2198, R2200~R2202, Q140~Q141.	0.6
4	37	WOL control	02/14	HP	Add 100K pull up for LAN_WOL_EN.	Add R2203(100Kohm).	0.6
5	29	SPDIF	02/14	HP	HP request to add 4.7K pull down on SPDIF out.	Add R2206(4.7Kohm).	0.6
6	29	Card reader	02/14	HP	Need reserve some test point.	Add R2205(0ohm) and T94.	0.6
7	17	MXM thermal pin	02/14	HP	Isolation MXM_THERM# and PWR_GD use MOSFET.	Add Q142 and R2204 for the modify.	0.6
8	30	USB Connector	02/28	HP	Couple mV over the 150mV GS limits.	Change R207, R217 from 56.2 ohm to 60.4 ohm.	0.6
9	21	THERM_SCI#	02/28	HP	HP request to design change.	Remove R1854 from BOM list.	0.6
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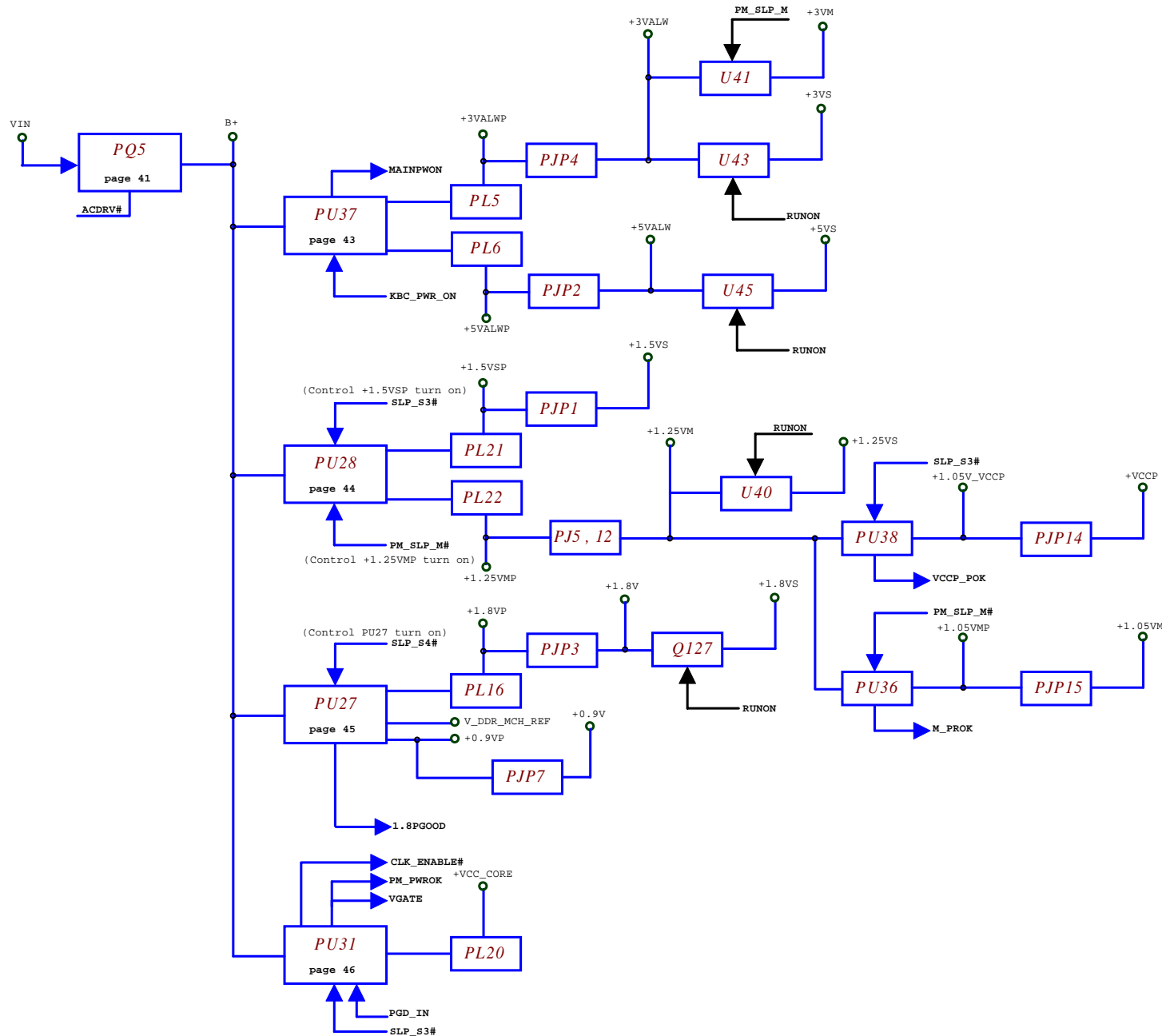


# Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	15	Clock Gen	03/19	HP	Remove Ohm damping of differential clock pair.	Remove RP49, RP51~RP57, reserve RP48.	0.8
2	15	FSB selector	03/19	HP	Remove FSB selection function. Remove JP62, JP63, Reserve R1689, R1696, R1705, R1737, install R1694, R1716, R1734.		0.8
3	29	Audio Codec	03/19	HP	To improve audio quality of docking.	Change R290~R291 to 6.04K and R289, R292 to 2K.	0.8
4	20	GPU Thermal	03/19	HP	Design change for MXM board.	Reserve R1854.	0.8
5	26	NAND Card	03/23	HP	Don't need this function for MP.	Reserve R2064, R2065, C1553 ~ C1560.	0.8
6	21	OC6#/GPIO30	03/23	HP	This pin is not long use for MXM.	Reserve R2207 for isolation.	0.8
7	38	POK CKT	03/28	Compal	For schematic leverage to Chimay.	Change LMV331(U47,U48) to LM393(U47), and remove R1976, C1487	
8	24	NIC power	03/28	Compal	Don't need +V1.0M_LAN power regulator.	Remove Q90, C1436 ~ C1440.	0.8
9	31	USB Port	03/28	Compal	To correct schematic and make layout smooth.	Remove C118, C498, C499, R49 and change C126 to 330uF.	0.8
10	31	BT	03/28	Compal	To make layout smoothly.	Remove D16.	0.8
11	34	KBC Clock	03/28	Compal	To make layout smoothly and EMI request.	Remove R1929, C1455.	0.8
12	21	LAN/WLAN Switch	03/30	HP	Unplug AC, WLAN will be disabled on XP OS.	Add U63 for slove leakage issue of enable ACBS.	0.8
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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	NB Crack detect	05/02	HP	Reserve BGA crack detect function	Remove Q114~Q117, R2049~R2052, install R111, R113, R122, R132.	1.0
2	22	SB Crack detect	05/02	HP	Reserve BGA crack detect function	Remove Q118~Q121, R2058~R2061, install R138~R141.	1.0
3	22	Audio Codec	05/02	HP	To improve ICH_V5REF_RUN of SB.	Change C1190 from 0.1uF to 1uF.	1.0
4	36	Easy crack Issue	05/14	HP	To prevent crack issue for L14	Change L14 material to SM010008E10.	1.0
5	14	DDR DIMM B	5/15	HP	To solve OTS issue OTS 265441 and 261307.	Change R33 pin2 connect to +3VM.	1.0
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