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# Intel Skylake-U Platform

## Skylake-U CPU (TDP 15W) SoC

**Project Information**

**Phase: EVT**

| PCB AND SILKSCREEN COLOR | | |
|---|---|---|
| **Program Phase** | **Color of PCB** | **Silkscreen** |
| **EVT** | **RED** | **YELLOW** |
| **DVT** | **LIGHT BLUE** | **YELLOW** |
| **PVT/MVB / PRODUCTION** | **GREEN** | **WHITE** |



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PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
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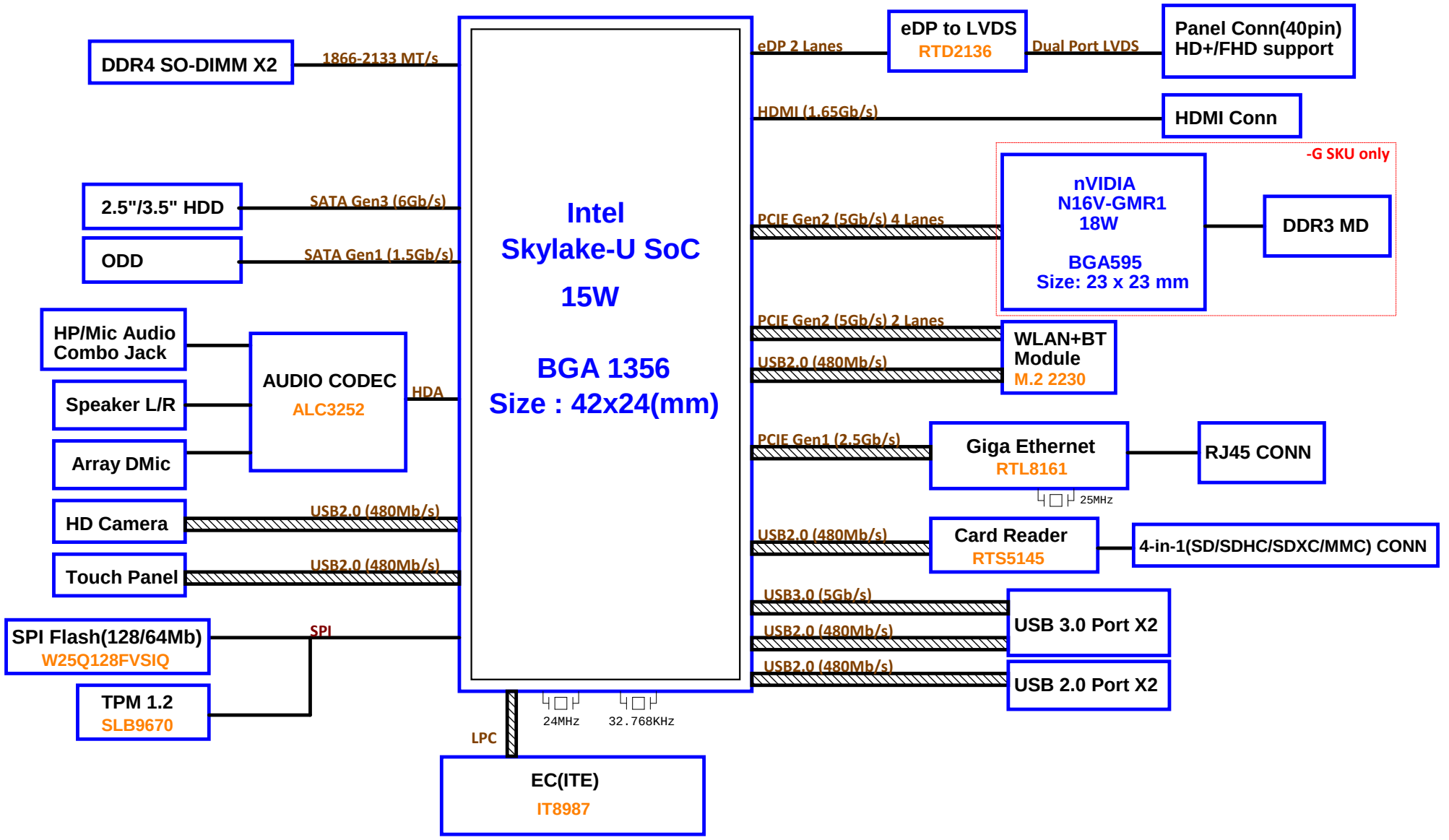
# Intel Skylake-U Platform Block Diagram (Hawaii-G/-U)



[5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[5,7,17,46,48] +VCCIO
[5,6,7,10,43,46] +VCCSTPLL

HDMI

U21A SKL_ULT ?

[22] IN_D2# → E55 DDI1_TXN[0]
[22] IN_D2 → F55 DDI1_TXP[0]
[22] IN_D1# → E58 DDI1_TXN[1]
[22] IN_D1 → F58 DDI1_TXP[1]
[22] IN_D0# → F53 DDI1_TXN[2]
[22] IN_D0 → G53 DDI1_TXP[2]
[22] IN_CLK# → F56 DDI1_TXN[3]
[22] IN_CLK → G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI

EDP

DISPLAY SIDEBANDS

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 [20]
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 [20]
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 [20]
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 [20]
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN [20]
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP [20]

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

[22] SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
[22] SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

+3V R208 2.2K_4 → NZ N8 GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA

TP22 → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO R116 24.9/F_4 → EDP_RCOMP E52 EDP_RCOMP

GPP_E13/DDPB_HPD0 L9 → PCH_HDMI_HPD → PCH_HDMI_HPD [22]
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L8
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 → EDP_HPD → EDP_HPD [20]

EDP_BKLTEN R12 → PCH_LVDS_BLON → PCH_EDP_BLON [21]
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM [20]
EDP_VDDEN U13 → PCH_LCDVCC_EN → PCH_LCDVCC_EN [21]

SKL_ULT
REV = 1

1 OF 20

?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

**Reserve EDP_HPD opposites circuit!**

+3V
R505 *10K_4 → EDP_HPD
R504 100K_4

U21D SKL_ULT ?

TP45 → CATERR# D63
[29] EC_PECI → EC_PECI A54
[29,43,47] H_PROCHOT# → R408 499/F_4 → PROCHOT# C65
PM_THRMTRIP# C63
THERMTRIP# A65
SKTOCC#

CPU MISC

[17] XDP_BPM0 → C55 BPM#[0]
[17] XDP_BPM1 → D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

[26] RF_OFF → A6 GPP_E3/CPU_GP0
A7 GPP_E7/CPU_GP1
BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3

R170 49.9/F_4 → PROC_POPIRCOMP AT16
R164 49.9/F_4 → PCH_OPI_RCOMP AU16
R79 49.9/F_4 → EDRAM_OPIO_RCOMP H66
R80 49.9/F_4 → EOPIO_RCOMP H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG

PROC_TCK B61 → XDP_TCK0 → XDP_TCK0 [17]
PROC_TDI D60 → XDP_TDI_CPU → XDP_TDI_CPU [17]
PROC_TDO A61 → XDP_TDO_CPU → XDP_TDO_CPU [17]
PROC_TMS C60 → XDP_TMS_CPU → XDP_TMS_CPU [17]
PROC_TRST# B59 → XDP_TRST#_CPU → XDP_TRST#_CPU [17]

PCH_JTAG_TCK B56 → JTAG_TCK_PCH → JTAG_TCK_PCH [17]
PCH_JTAG_TDI D59 → JTAG_TDI_PCH → JTAG_TDI_PCH [17]
PCH_JTAG_TDO A56 → JTAG_TDO_PCH → JTAG_TDO_PCH [17]
PCH_JTAG_TMS C59 → JTAG_TMS_PCH → JTAG_TMS_PCH [17]
PCH_TRST# C61 → XDP_TRST#_CPU
JTAGX A59 → JTAGX_PCH → JTAGX_PCH [17]

SKL_ULT
REV = 1

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+VCCSTPLL
PM_THRMTRIP# R422 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL . 470 OHM IS FOR I/P

PLACE NEAR CPU

+VCCIO
XDP_TMS_CPU R435 *51_4
XDP_TDI_CPU R436 *51_4
XDP_TDO_CPU R427 *51_4

+VCCSTPLL
H_PROCHOT# R406 1K_4
XDP_TCK0 R430 51_4
XDP_TRST#_CPU R439 51_4

EC-PV-01

+VCCIO R428 *0/S_4 →
R431 *51_4 → JTAGX_PCH
R440 51_4 → JTAG_TMS_PCH
R444 51_4 → JTAG_TDI_PCH
R448 51_4 → JTAG_TDO_PCH
R443 51_4 → JTAG_TCK_PCH

**Close to Chipset**

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|---|---|---|
| Custom | SKL CPU eDP/DDI/MISC | 1A |

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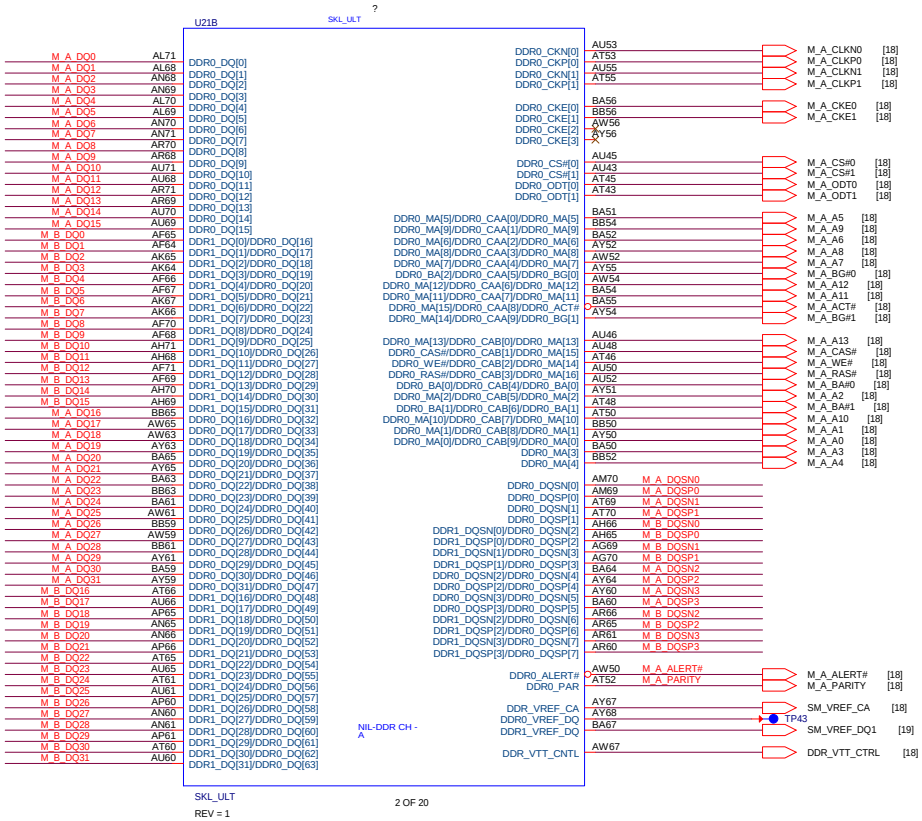
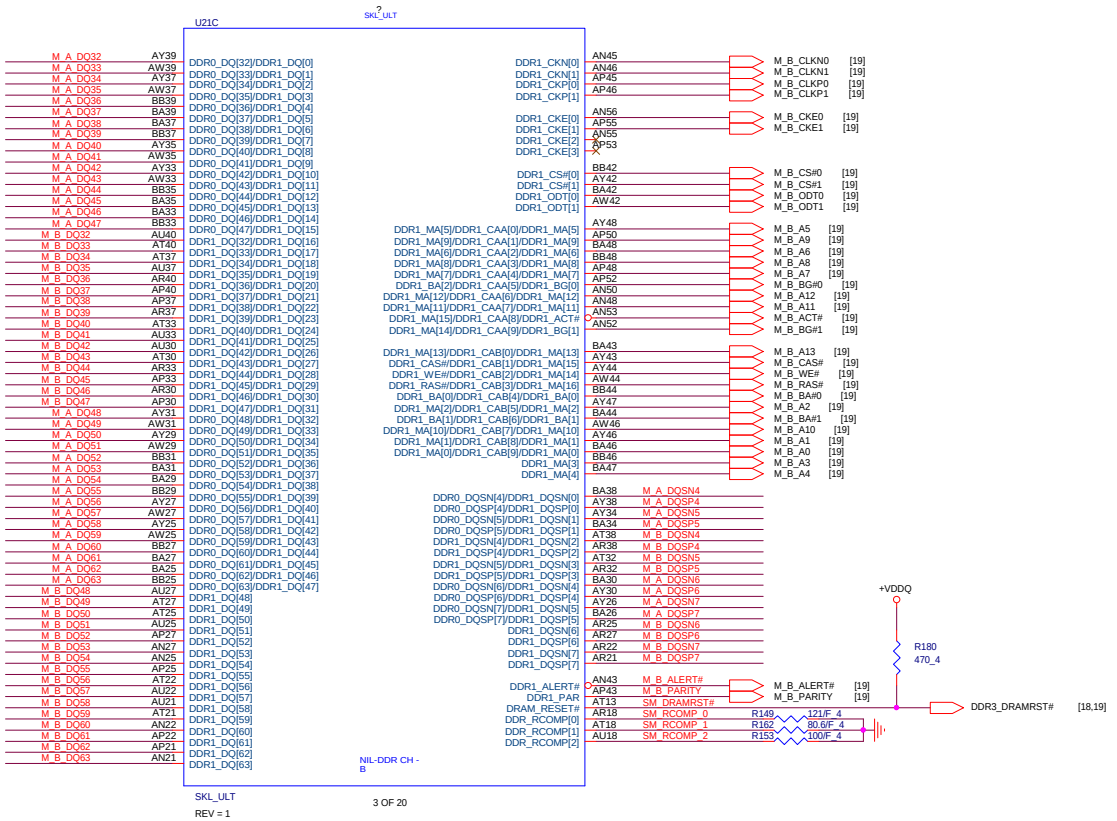
# SkyLake ULT Processor (DDR4 IL)



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[11,12,13,15,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[3,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[21,23,27,28,32,39,40,41,43,45,46,47,48,52] +5V_S5
[3,7,17,46,48] +VCCIO
[3,6,7,10,43,46] +VCCSTPLL
[14,16] +3V_RTC_2

U21K SKL_ULT ?
SYSTEM POWER MANAGEMENT

[24,26,29,31,33] PLTRST#
[17] SYS_RESET#
[17,29] RSMRST#
R485 *0/S_4 RSMRST#_R
R403 *10K_4 H_VCCST_PWRGD
EC-PV-01
[17,29] HWPG R484 *0/S_4
[29] EC_SUSPWRACK
[29] EC_SUSACK#
*0_4 R580
*0_4 R192
[24,26] PCIE_WAKE#
TP23
TP58
TP18

PLTRST# AN10
SYS_RESET# B5
RSMRST# AY17
PROCPWRGD A68
H_VCCST_PWRGD B65
SYS_PWROK B6
PCH_PWROK BA20
DPWROK BB20
SUSWARN# AR13
SUSACK# AP11
PCIE_WAKE# BB15
PCIE_LAN_WAKE# AM15
LAN_DIS# AW17
AT15

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD

GPP_B12/SLP_S0# AT11 PM_SLP_S0#
GPD4/SLP_S3# AP15
GPD5/SLP_S4# BA16
GPD10/SLP_S5# AY16
SLP_SUS# AN15
SLP_LAN# AW15 SLP_LAN#
GPD9/SLP_WLAN# BB17 SLP_WLAN#
GPD6/SLP_A# AN16
GPD3/PWRBTN# BA15 DNBSWON#
GPD1/ACPRESENT AY15 AC_PRESENT_EC
GPD0/BATLOW# AU13 PM_BATLOW_N_EC
GPP_A11/PME# AU11
INTRUDER# AP16 INTRUDER#_R R177 1M_4 +3V_RTC_2
GPP_B11/EXT_PWR_GATE# AM10 EXT_PWR_GATE#
GPP_B2/VRALERT# AM11

PM_SLP_S0# [17,29]
SUSB# [17,29]
SUSC# [17,29]
SLP_S5# [17,29]
PM_SLP_SUS# [29]
TP62
TP60
SLP_A# [17]
TP31
DNBSWON# [17,29]
AC_PRESENT_EC [29]
TP27

SKL_ULT
REV = 1
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?

## PCH Pull-high/low(CLG)

+3V_S5
SUSWARN# R189 *10K_4
SUSACK# R191 *10K_4
PM_BATLOW_N_EC R181 10K_4

+3V_S5
PCIE_WAKE# R493 1K_4
AC_PRESENT_EC R490 10K_4
PCIE_LAN_WAKE# R187 10K_4
EXT_PWR_GATE# R186 *20K/F_4

+3V
SYS_RESET# R500 10K_4
PLTRST# R222 *10K/F_4
R223 100K/F_4
RSMRST# R487 10K_4
DPWROK R481 *100K/F_4

RSMRST#
SYS_RESET#
PLTRST#
EC5 *220P/50V_4
C554 *220P/50V_4
C549 *220P/50V_4

[29] EC_DPWROK
RSMRST# R483 *0_4 DPWROK
EC_DPWROK R538 *0/S_4
EC-PV-01

**Close to CPU side**
**H_VCCST_PWRGD trace 0.3" - 1.5"**

+VCCIO +VCCSTPLL
R401 1K_4
R405 *1K_4
HWPG D14 1 2 RB500V-40 H_VCCST_PWRGD_R R404 60.4_4 H_VCCST_PWRGD
C512 *10P/50V_4

+VCCIO +5V_S5 +3V_S5
R478 15K_4
R479 100K_4
R476 10K_4
HWPG
+1.0V_PWRGD_G2 2 Q31 2N7002K
R475 100K_4
+1.0V_PWRGD_G1 2 Q32 METR3904-G
C530 0.1U/16V_4
R480 100K_4

**System PWR_OK(CLG)**

SYS_PWROK
EC-PV-01
R496 *0/S_4
EC_PWROK
EC_PWROK [29]
C552 *0.1U/16V_4
R497 100K/F_4

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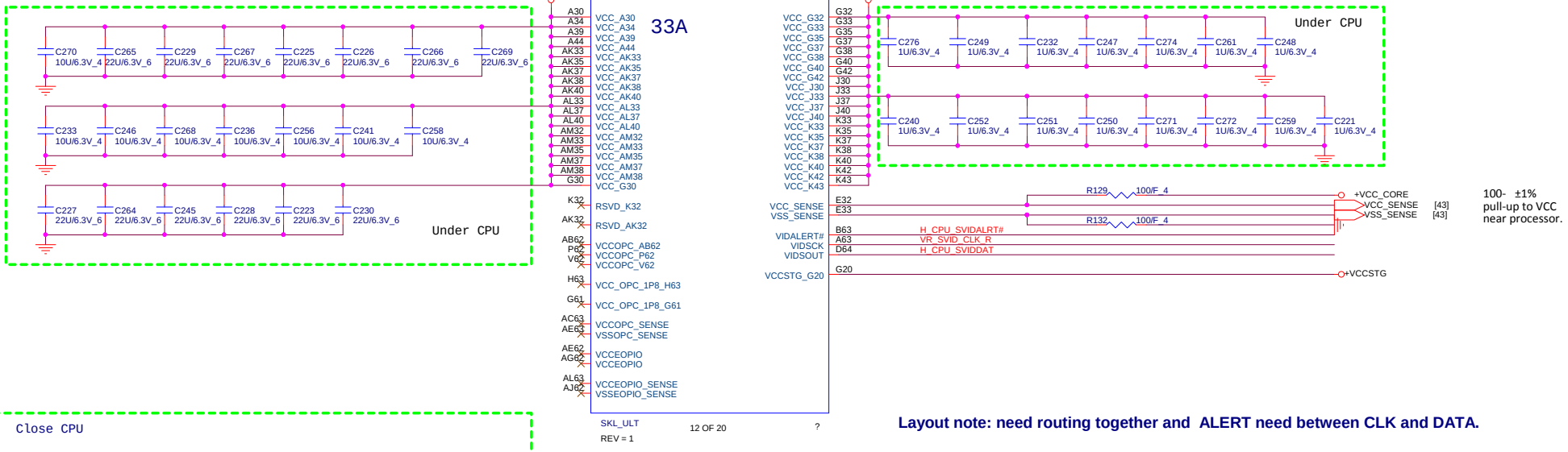
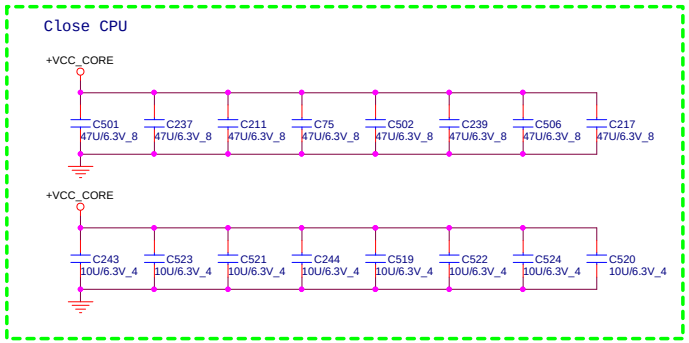
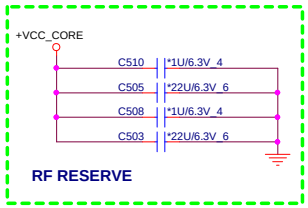
[32,43,44] +VCC_CORE
[7] +VCCSTG
[3,5,7,10,43,46] +VCCSTPLL

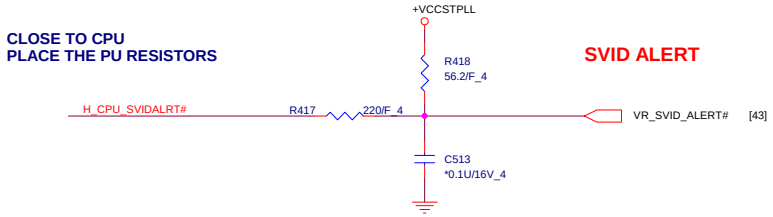


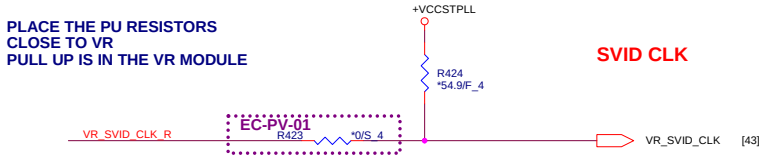

100- ±1% pull-up to VCC near processor.

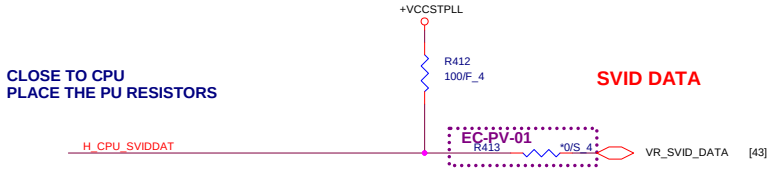



**Layout note: need routing together and ALERT need between CLK and DATA.**

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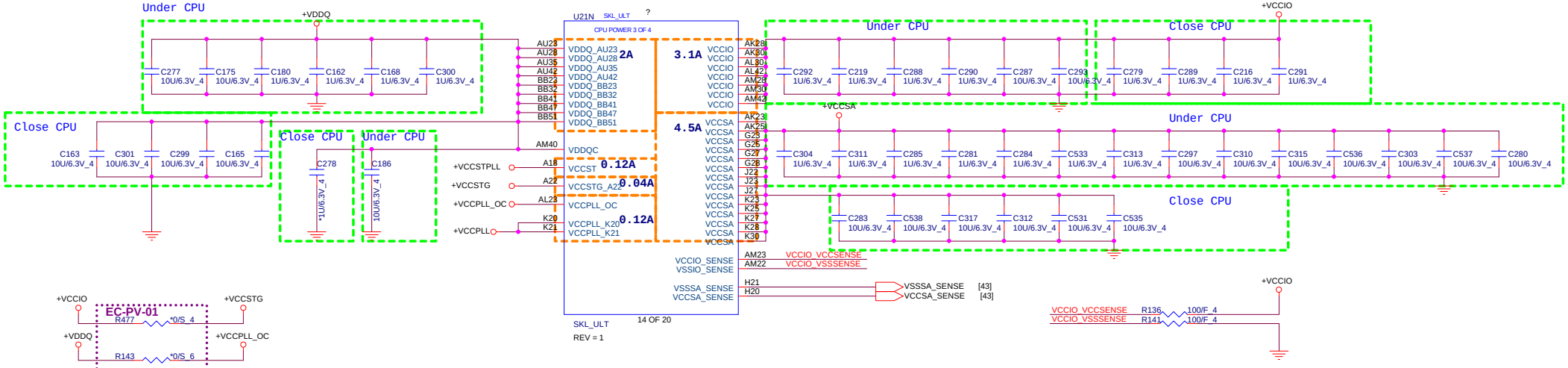
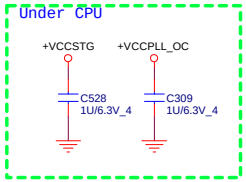
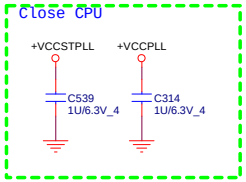
[3,5,17,46,48] +VCCIO
[43,45] +VCCSA
[4,18,19,32,40] +VDDQ
[3,5,6,10,43,46] +VCCSTPLL
[6] +VCCSTG

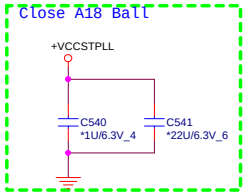


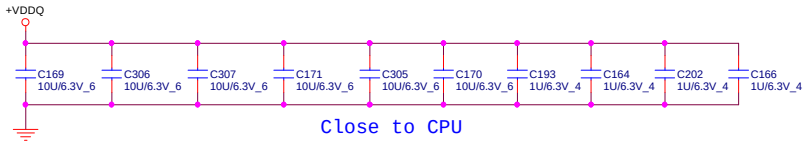




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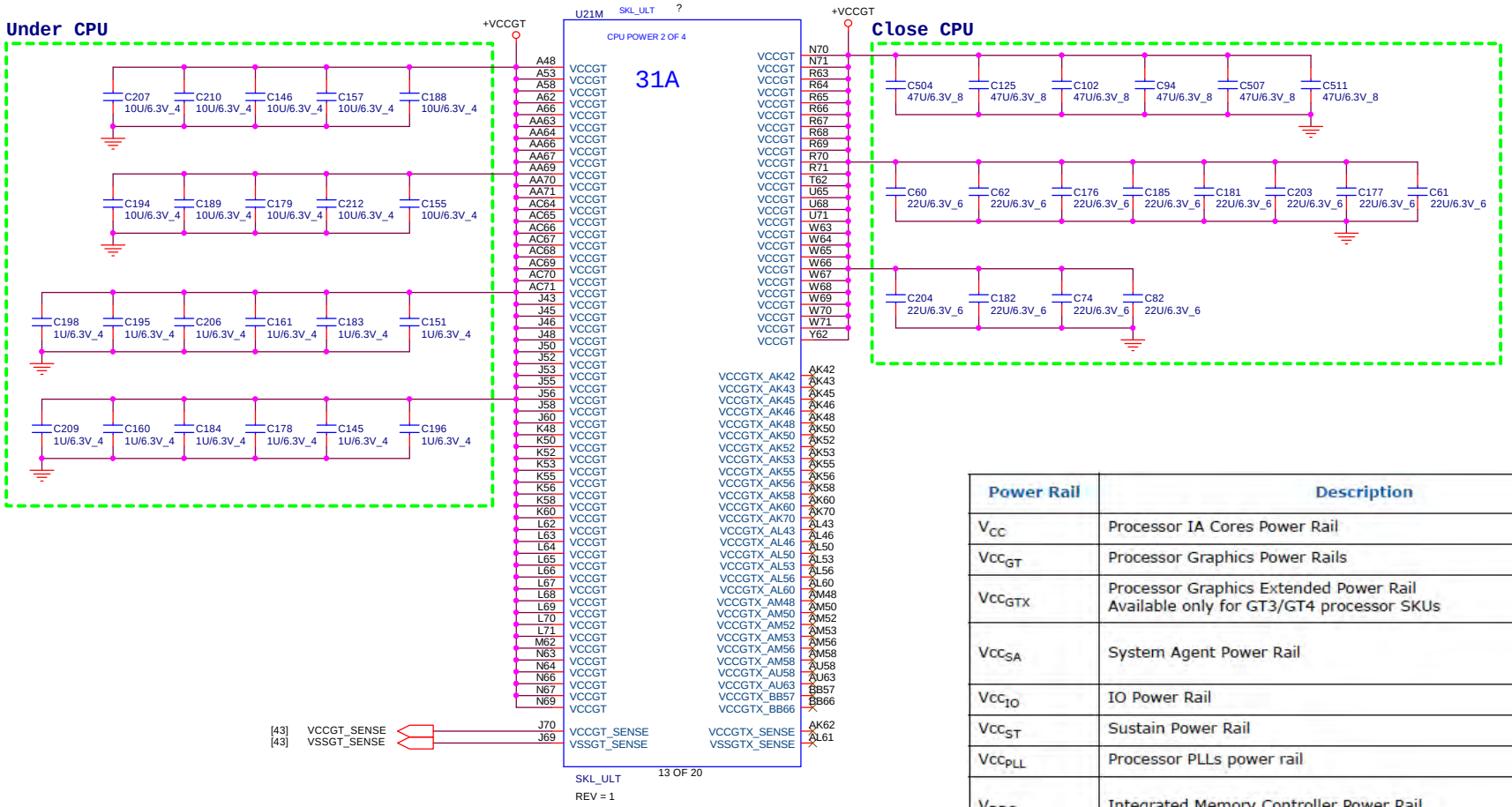
+VCCGT [43,44]




| Power Rail | Description | Control |
|---|---|---|
| $V_{CC}$ | Processor IA Cores Power Rail | SVID |
| $Vcc_{GT}$ | Processor Graphics Power Rails | SVID |
| $Vcc_{GTX}$ | Processor Graphics Extended Power Rail<br>Available only for GT3/GT4 processor SKUs | SVID |
| $Vcc_{SA}$ | System Agent Power Rail | SVID/Fixed (SKU dependent) |
| $Vcc_{IO}$ | IO Power Rail | Fixed |
| $Vcc_{ST}$ | Sustain Power Rail | Fixed |
| $Vcc_{PLL}$ | Processor PLLs power rail | Fixed |
| $V_{DDQ}$ | Integrated Memory Controller Power Rail | Fixed (Memory technology dependent) |
| $Vcc_{OPC}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $Vcc_{OPC\_1P8}$ | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| $Vcc_{EOPIO}$ | Processor EOPIO power rail (available only in SKU's with OPC) | Fixed |

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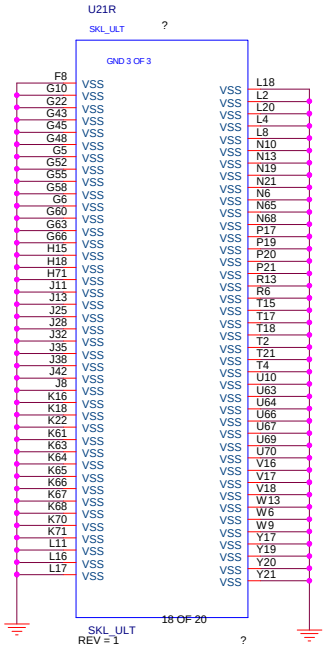


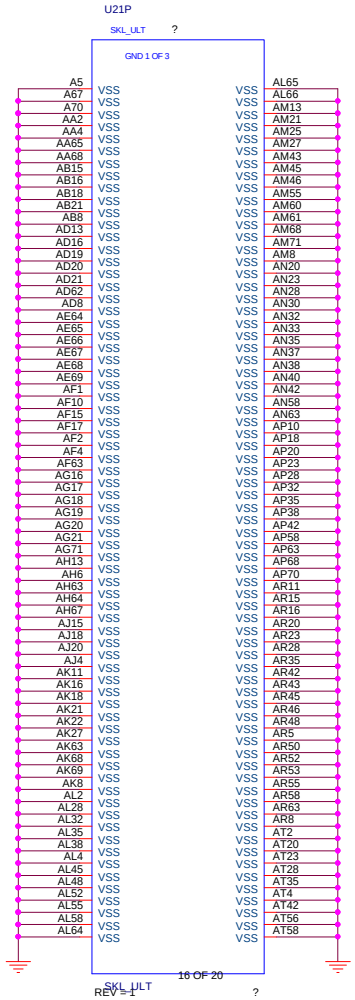


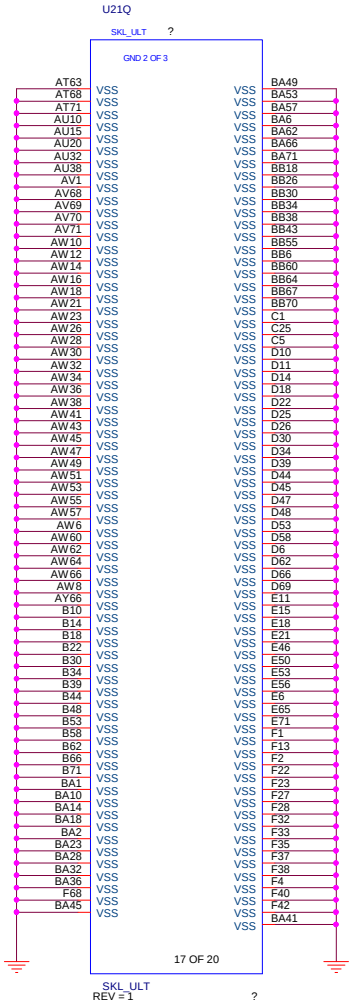




| | | |
|---|---|---|
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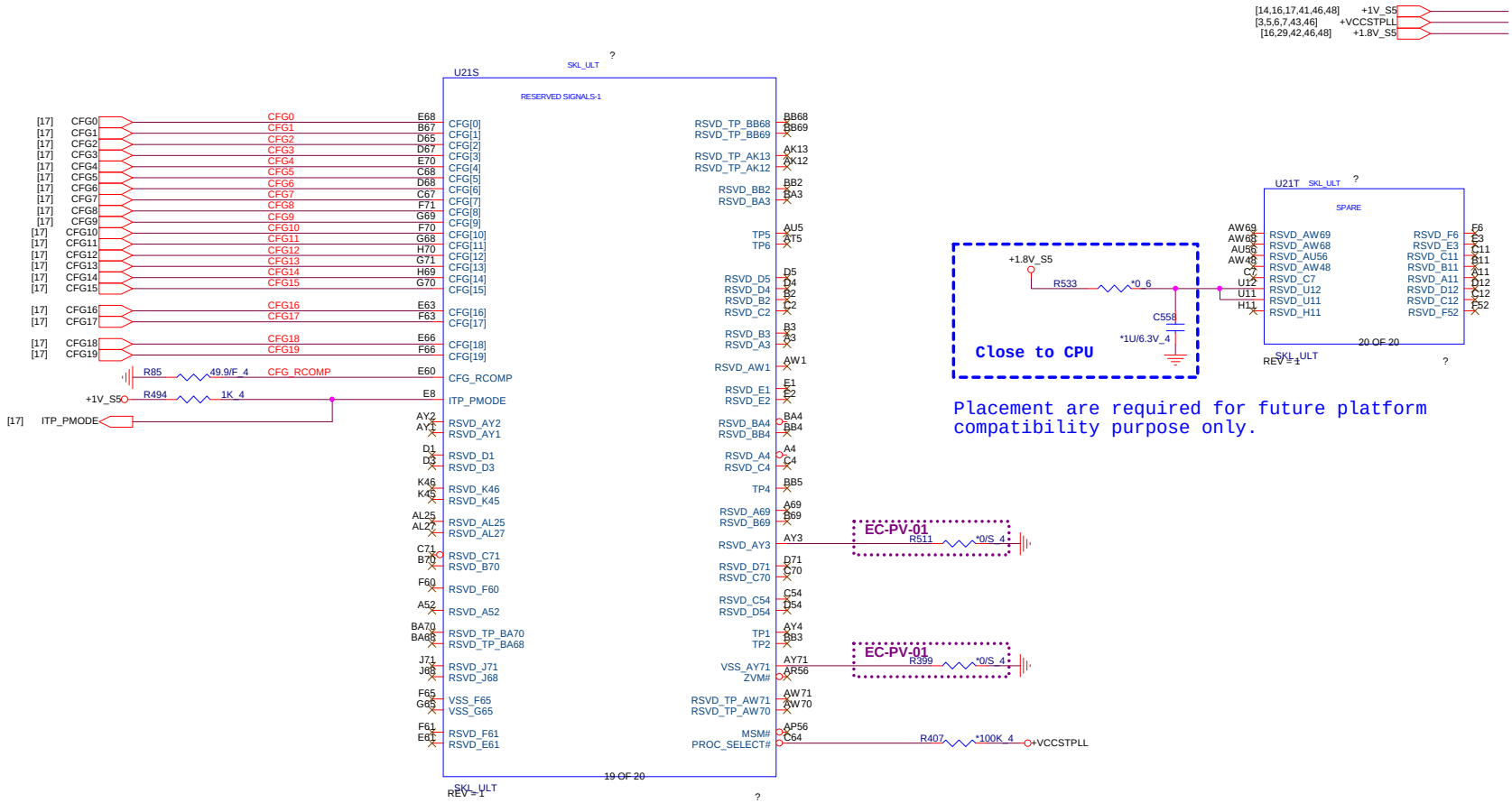


## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 | Circuit |
|---|---|---|---|
| CFG3 (Physcial Debug Enable) DFX Privacy | Disable: | Enable: Set DFX Enable in DFX interface MSR | CFG3 R400 *1K_4 |
| CFG4 (DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP | CFG4 R402 1K_4 |
| | | | |

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| Custom | SKL CPU RSVD | 1A |

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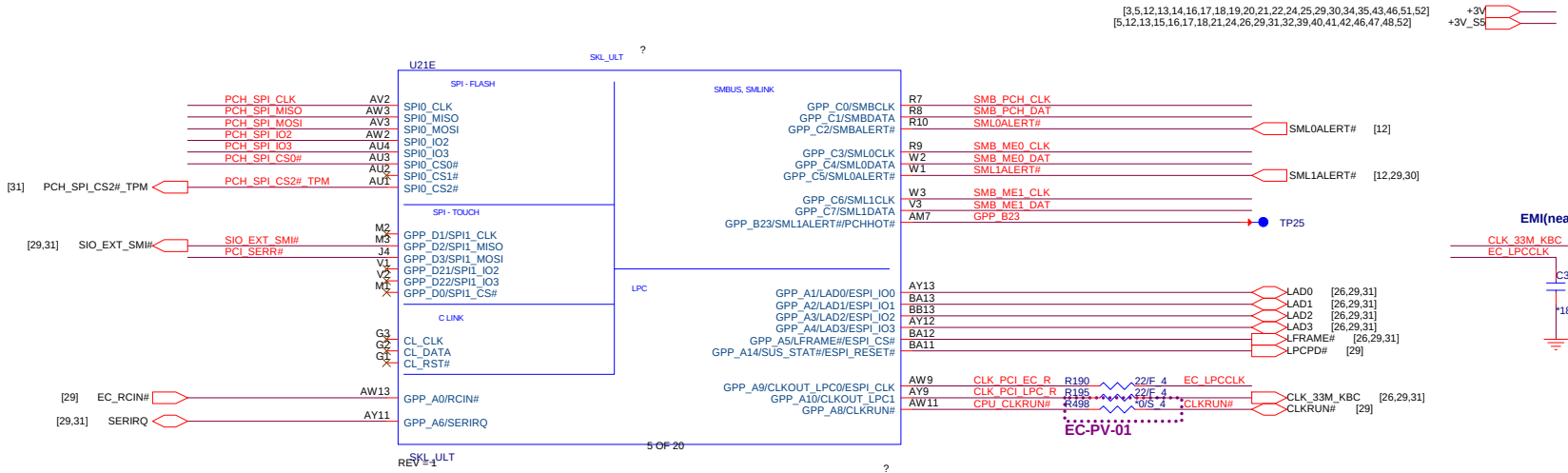
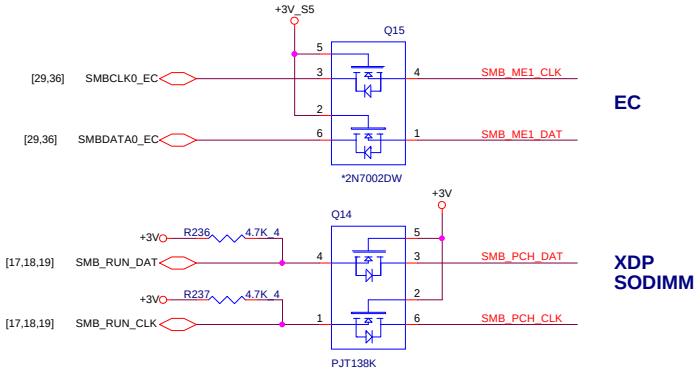
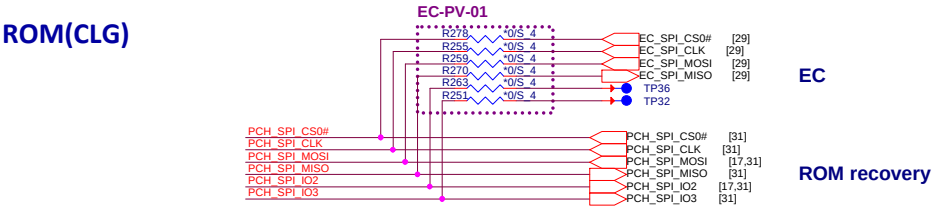


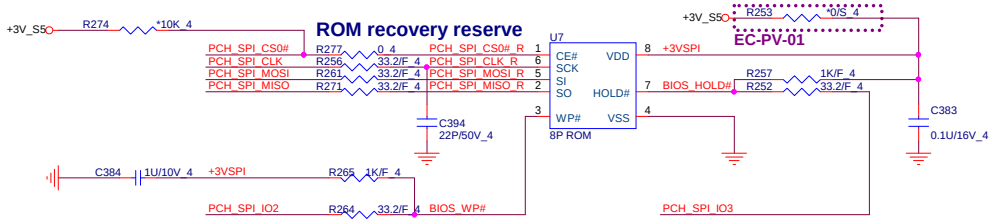

## GPIO Pull UP


## SMBus/Pull-up(CLG)




## PCH SPI ROM(CLG)




| Vender | Size | P/N |
|---|---|---|
| Winbond | 8MB | AKE3EFP0N07 (W25Q64FVSSIQ) |
| GD | 8MB | AKE2EZN0Q00 (GD25B64CSIGR) |
| Socket | | DFHS08FS023 |
| | | |


HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

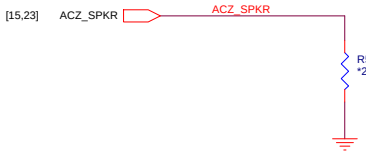
| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL CPU SPI/LPC/SMB | 1A |

Date: Tuesday, March 15, 2016 Sheet 11 of 58

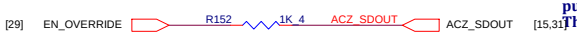
[3,5,11,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V

# Functional Strap Definitions

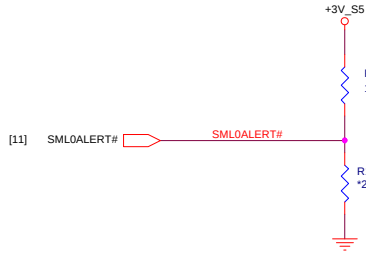
**DESIGN NOTE:**
**WEAK PULL UP RESISTOR PRESENT ON THIS NET**



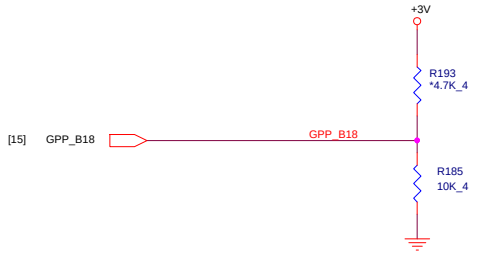

**TOP SWAP OVERRIDE**
**HIGH - TOP SWAP ENABLE**
**LOW-DISABLED**
**HIGH: LPC SELECTED FOR SYSTEM FLASH**
**WEAK INTERNAL PD**




**No Boot:**
**The signal has a weak internal pull-down.**
**0 = Enable security measures defined in the Flash Descriptor.**
**1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.**
**This function is useful when running ITP/XDP.**



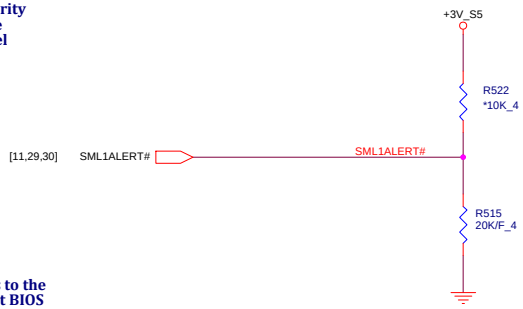

**No Boot:**
**The signal has a weak internal pull-down.**
**0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).**
**1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.**




**No Boot:**
**The signal has a weak internal pull-down.**
**0 = Disable No Reboot mode.**
**1 = Enable No Reboot mode**
**(PCH will disable the TCO Timer system reboot feature).**
**This function is useful when running ITP/XDP.**


**No Boot:**
**The signal has a weak internal pull-down.**
**This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.**

| Bit 10 | Boot BIOS Destination |
|---|---|
| 0 | SPI |
| 1 | LPC |




**No Boot:**
**The signal has a weak internal pull-down.**
**0 = LPC Is selected for EC.**
**1 = eSPI Is selected for EC.**

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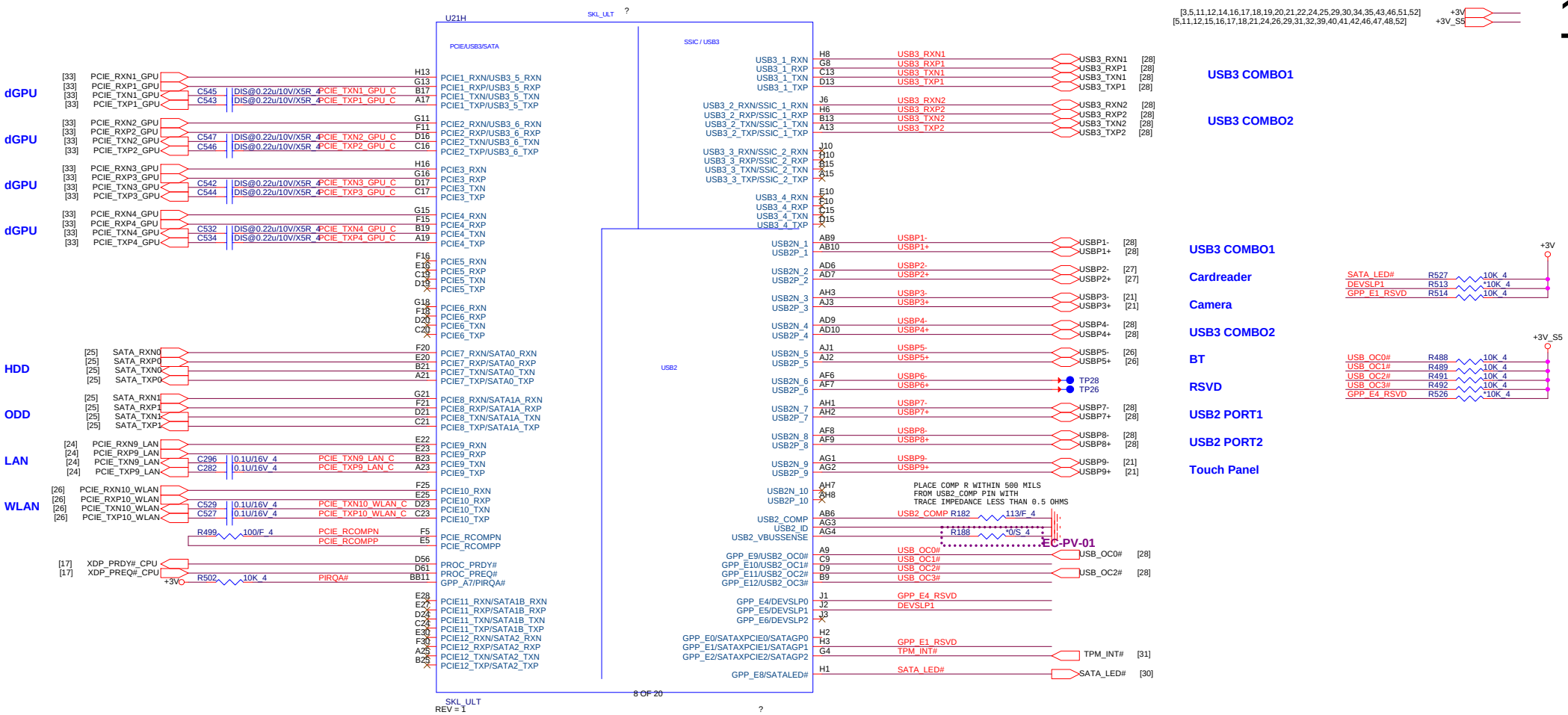
Quanta Computer Inc.
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL CPU Strap | 1A |

Date: Wednesday, March 09, 2016 Sheet 12 of 58




## PCI-E Port Mapping Table

| PCI-E | Function | CLK REQ | Function |
|---|---|---|---|
| PORT-1 | dGPU | PORT-0 | dGPU |
| PORT-2 | dGPU | PORT-1 | |
| PORT-3 | dGPU | PORT-2 | WLAN |
| PORT-4 | dGPU | PORT-3 | LAN |
| PORT-5 | | PORT-4 | |
| PORT-6 | | PORT-5 | |
| PORT-7 | HDD | | |
| PORT-8 | ODD | | |
| PORT-9 | LAN | | |
| PORT-10 | WLAN | | |
| PORT-11 | | | |
| PORT-12 | | | |

## USB3.0 Port Mapping Table

| USB3.0 | Function |
|---|---|
| PORT-1 | USB3 COMBO1 |
| PORT-2 | USB3 COMBO2 |
| PORT-3 | NC |
| PORT-4 | NC |

## USB2.0 Port Mapping Table

| USB2.0 | Function |
|---|---|
| PORT-1 | USB3 COMBO1 |
| PORT-2 | Cardreader |
| PORT-3 | Camera |
| PORT-4 | USB3 COMBO2 |
| PORT-5 | BT |
| PORT-6 | NC |
| PORT-7 | USB2 PORT1 |
| PORT-8 | USB2 PORT2 |
| PORT-9 | Touch Panel |
| PORT-10 | NC |



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| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL CPU PCIE/USB/SATA | 1A |

Date: Wednesday, March 09, 2016 Sheet 13 of 58

[5,16] +3V_RTC_2
[3,5,11,12,13,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,16,17,41,46,48] +1V_S5

U21J SKL_ULT ?

CLOCK SIGNALS

WLAN
LAN

[33] CLK_GFX_N → CLK_GFX_N → D42 CLKOUT_PCIE_N0
[33] CLK_GFX_P → CLK_GFX_P → C42 CLKOUT_PCIE_P0
[33] PCIE_CLKREQ_VGA# → PCIE_CLKREQ_VGA# → AR10 GPP_B5/SRCCLKREQ0#

B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
PCIE_CLKREQ1# → AT7 GPP_B6/SRCCLKREQ1#

[26] CLK_PCIE_WLANN → CLK_PCIE_WLANN → D41 CLKOUT_PCIE_N2
[26] CLK_PCIE_WLANP → CLK_PCIE_WLANP → C41 CLKOUT_PCIE_P2
[26] PCIE_CLKREQ_WLAN# → PCIE_CLKREQ_WLAN# → AT8 GPP_B7/SRCCLKREQ2#

[24] CLK_PCIE_LANN → CLK_PCIE_LANN → D40 CLKOUT_PCIE_N3
[24] CLK_PCIE_LANP → CLK_PCIE_LANP → C40 CLKOUT_PCIE_P3
[24] PCIE_CLKREQ_LAN# → PCIE_CLKREQ_LAN# → AT10 GPP_B8/SRCCLKREQ3#

B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
PCIE_CLKREQ4# → AU8 GPP_B9/SRCCLKREQ4#

E40 CLKOUT_PCIE_N5
E39 CLKOUT_PCIE_P5
PCIE_CLKREQ5# → AU7 GPP_B10/SRCCLKREQ5#

10 OF 20

SKL_ULT REV = 1 ?

CLKOUT_ITPXDP_N → F43 CK_XDP_N_R
CLKOUT_ITPXDP_P → E43 CK_XDP_P_R

**RP1 install for XDP**

*0_4P2R_4 RP1: 4, 3, 2, 1
CK_XDP_N [17]
CK_XDP_P [17]

GPD8/SUSCLK → BA17 PCH_SUSCLK → TP59

XTAL24_IN → E37 XTAL24_IN
XTAL24_OUT → E35 XTAL24_OUT → +1V_S5

XCLK_BIASREF → E42 XCLK_BIASREF
R461 2.7K/F_4
R462 *60.4/F_4

Co-lay 60ohm 1% to GND for Cannonlake use

RTCX1 → AM18 RTC_X1
RTCX2 → AM20 RTC_X2

SRTCRST# → AN18 SRTC_RST#
RTCRST# → AM16 RTC_RST# → RTC_RST# [17]

## CLK_REQ/Strap Pin(CLG)

+3V
10K_4 R212 PCIE_CLKREQ4#
10K_4 R197 PCIE_CLKREQ_WLAN#
10K_4 R196 PCIE_CLKREQ_LAN#
10K_4 R211 PCIE_CLKREQ1#
10K_4 R210 PCIE_CLKREQ5#
10K_4 R213 PCIE_CLKREQ_VGA#

U21I SKL_ULT ?

CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C36 CSI2_DN1
D36 CSI2_DP1
C35 CSI2_DN2
D35 CSI2_DP2
A35 CSI2_DN3
B35 CSI2_DP3

C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 C32
CSI2_CLKP1 D32
CSI2_CLKN2 C29
CSI2_CLKP2 D29
CSI2_CLKN3 B26
CSI2_CLKP3 A26

CSI2_COMP → E13 CSI2_RCOMP → R165 100/F_4
GPP_D4/FLASHTRIG → B7 GPP_D4 → TP61

EMMC

GPP_F13/EMMC_DATA0 AP2
GPP_F14/EMMC_DATA1 AP1
GPP_F15/EMMC_DATA2 AP3
GPP_F16/EMMC_DATA3 AN3
GPP_F17/EMMC_DATA4 AN1
GPP_F18/EMMC_DATA5 AN2
GPP_F19/EMMC_DATA6 AM4
GPP_F20/EMMC_DATA7 AM1

GPP_F21/EMMC_RCLK AM2
GPP_F22/EMMC_CLK AM3
GPP_F12/EMMC_CMD AP4

EMMC_RCOMP → AT1 EMMC_RCOMP → R184 200/F_4

9 OF 20

SKL_ULT REV = 1 ?

## RTC Clock 32.768KHz

EC-SI-12

C355 12P/50V_4 — RTC_X1
Y3 32.768KHz
R224 10M_4
C356 12P/50V_4 — RTC_X2

## External Crystal

EC-SI-12

C360 12P/50V_4
XTAL24_IN
XTAL24_OUT
R130 1M_4
24MHz +-30PPM Y2
C273 12P/50V_4

## RTC Circuitry(RTC)

RTC Power trace width 20mils.

+3V_ALW
R554 1.5K_4
+3V_RTC_0
+3V_RTC_2
R567 20K/F_4
RTC_RST#
C589 1U/6.3V_4
C590 *220P/50V_4
R555 45.3K_4
D18 RB500V-40
R553 1K_4 +3V_RTC_1
D17 RB500V-40
R566 20K/F_4
SRTC_RST#
C581 1U/6.3V_4
C588 1U/6.3V_4
CN20 CONNDIPHOUSING2P

RTC_RST#
Q35 2N7002K
EC_RTC_RST
EC_RTC_RST [29]
R561 10K_4

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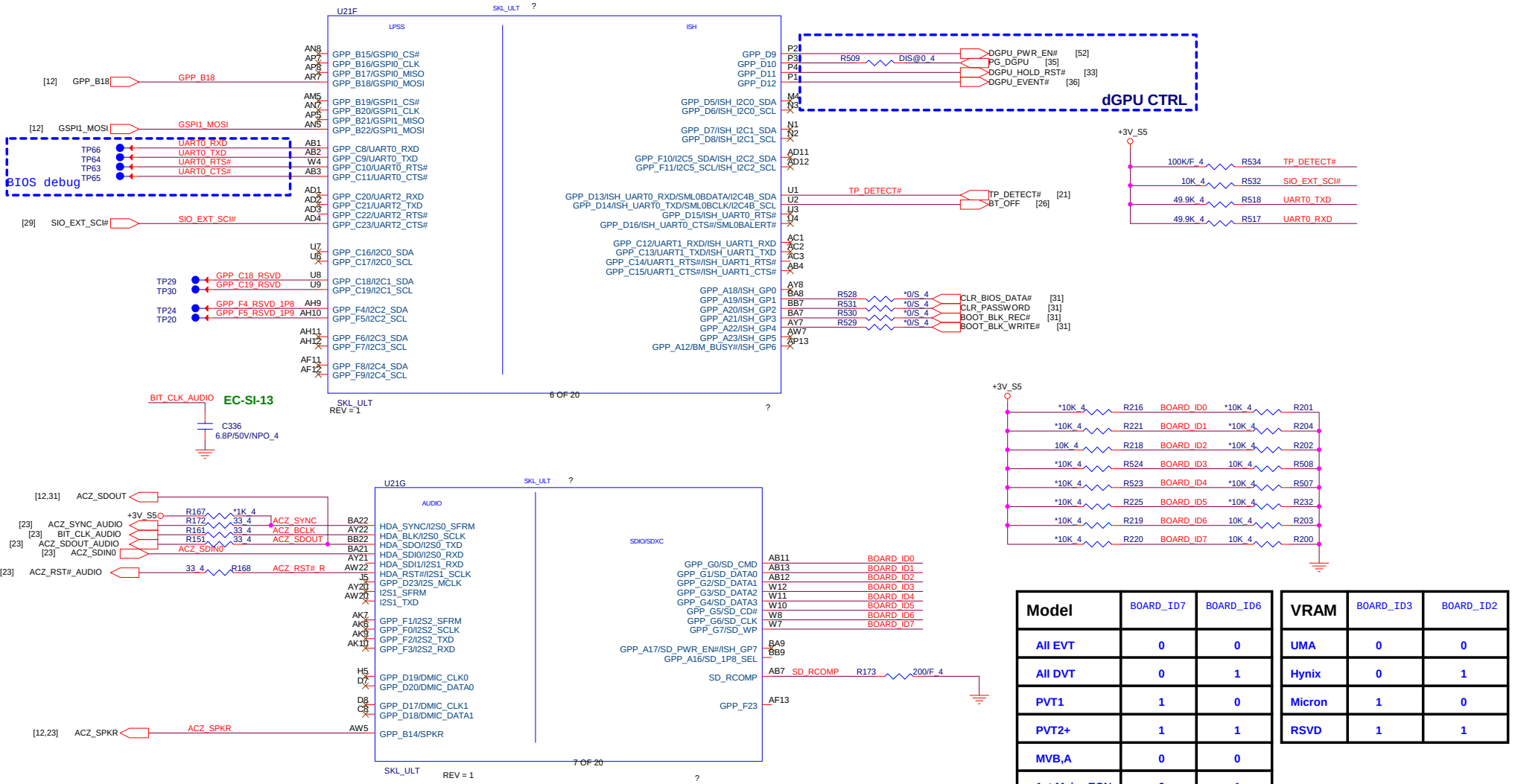
Quanta Computer Inc.
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL CPU CLK/eMMC | 1A |
| Date: Tuesday, March 15, 2016 | Sheet 14 of 58 | |

[5,11,12,13,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52]
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52]
+3V_S5
+3V




| Model | BOARD_ID7 | BOARD_ID6 |
|---|---|---|
| All EVT | 0 | 0 |
| All DVT | 0 | 1 |
| PVT1 | 1 | 0 |
| PVT2+ | 1 | 1 |
| MVB,A | 0 | 0 |
| 1st Major ECN | 0 | 1 |
| 2nd Major ECN | 1 | 0 |
| 3rd Major ECN | 1 | 1 |

| VRAM | BOARD_ID3 | BOARD_ID2 |
|---|---|---|
| UMA | 0 | 0 |
| Hynix | 0 | 1 |
| Micron | 1 | 0 |
| RSVD | 1 | 1 |

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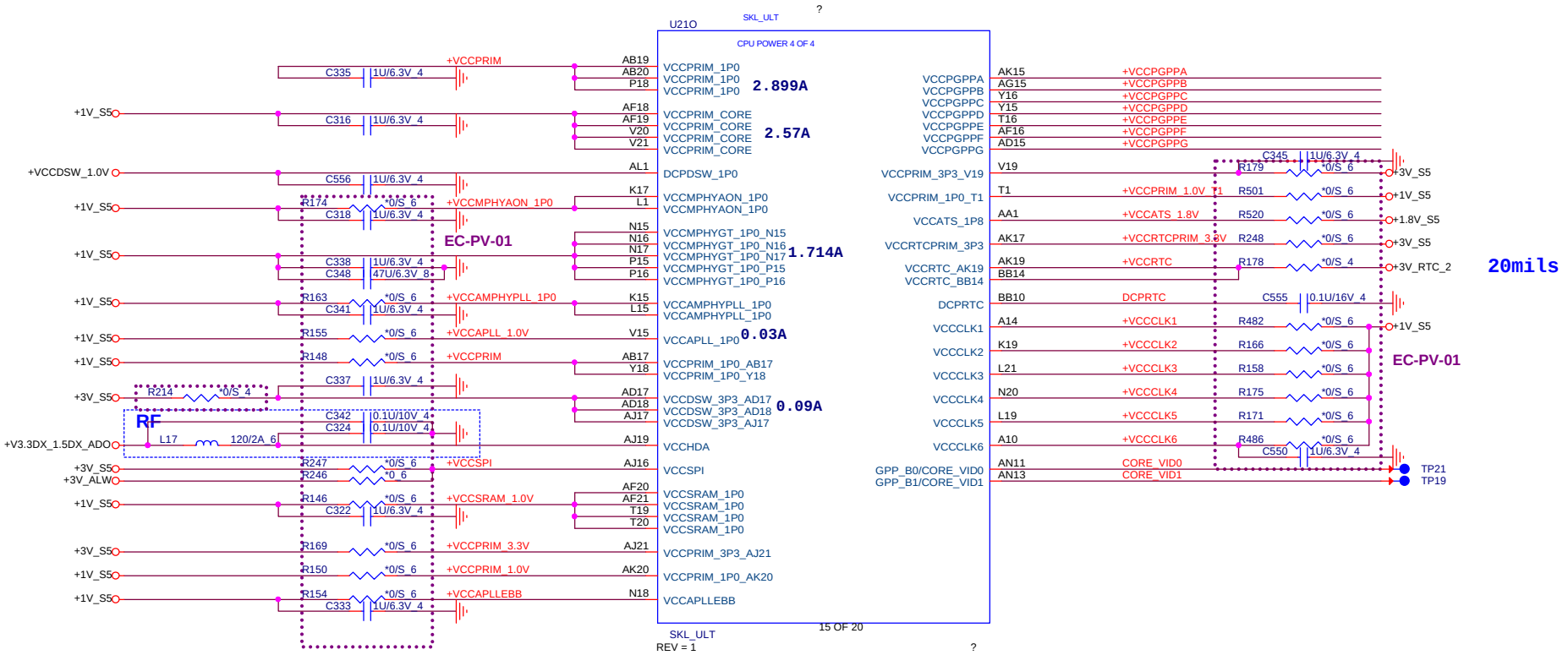
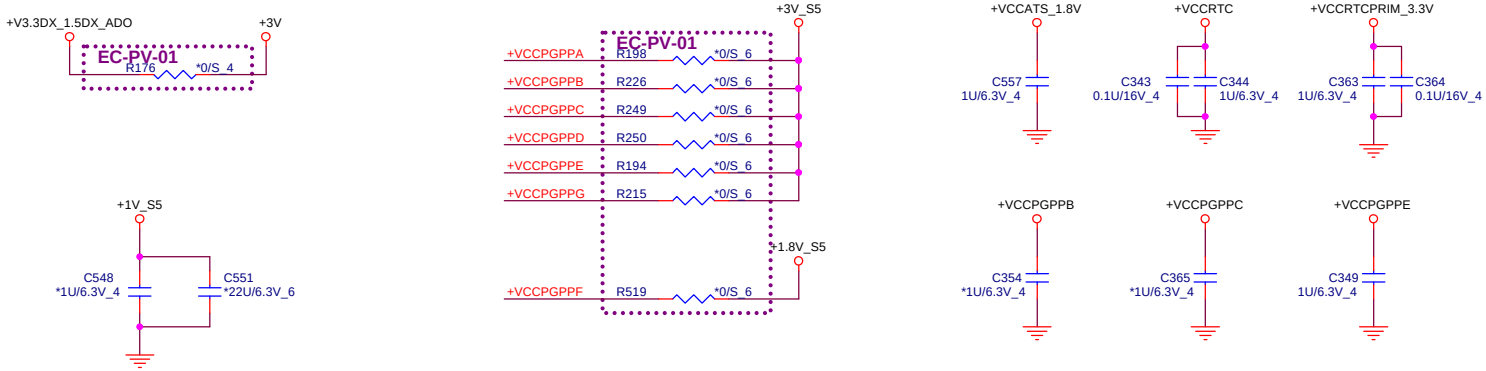
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL CPU HDA/GPIO | 1A |

Date: Thursday, March 10, 2016 Sheet 15 of 58

[10,14,17,41,46,48] +1V_S5
[10,29,42,46,48] +1.8V_S5
[5,11,12,13,15,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[5,14] +3V_RTC_2
[3,5,11,12,13,14,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V






Quanta Computer Inc.
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL CPU Power (PCH) | 1A |

Date: Wednesday, March 09, 2016 Sheet 16 of 58

[3,5,11,12,13,14,16,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,14,16,41,46,48] +1V_S5
[3,5,7,46,48] +VCCIO
[5,11,12,13,15,16,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5

# CPU XDP

CN1 *Samtec BSH-030-01

EC-PV-01

*0_4 R70 CFG3 1K_4 R69
[10] CFG3
[13] XDP_PREQ#_CPU
[13] XDP_PRDY#_CPU
[10] CFG0
[10] CFG1
[10] CFG2
TP44
CFG0 R78 1K_4 CFG1 CFG2 CFG3
[3] XDP_BPM0
[3] XDP_BPM1
[10] CFG4
[10] CFG5
[10] CFG6
[10] CFG7
[5,29] RSMRST#
[5,29] DNBSWON#
1K_4 R67
+1V_S5
CFG0 R65 *0/S_4 PWR_DEBUG
HOOK3
[11,18,19] SMB_RUN_DAT
[11,18,19] SMB_RUN_CLK
R57 *0/S_4 SMB_RUN_DAT_XDP
R54 *0/S_4 SMB_RUN_CLK_XDP
XDP_TCK1
XDP_TCK0
[3] XDP_TCK0

| | | | |
|---|---|---|---|
| 1 | XDP_PRESENT# | GND1 | 60 |
| 2 | PROC_PREQ# | OBSFN_C0 | 59 |
| 3 | OBSFN_A1 | OBSFN_C1 | 58 |
| 4 | GND2 | GND3 | 57 |
| 5 | OBSDATA_A0 | OBSDATA_C0 | 56 |
| 6 | OBSDATA_A1 | OBSDATA_C1 | 55 |
| 7 | GND4 | GND5 | 54 |
| 8 | OBSDATA_A2 | OBSDATA_C2 | 53 |
| 9 | OBSDATA_A3 | OBSDATA_C3 | 52 |
| 10 | GND6 | GND7 | 51 |
| 11 | OBSFN_B0 | OBSFN_D0 | 50 |
| 12 | OBSFN_B1 | OBSFN_D1 | 49 |
| 13 | GND8 | GND9 | 48 |
| 14 | OBSDATA_B0 | OBSDATA_D0 | 47 |
| 15 | OBSDATA_B1 | OBSDATA_D1 | 46 |
| 16 | GND10 | GND11 | 45 |
| 17 | OBSDATA_B2 | OBSDATA_D2 | 44 |
| 18 | OBSDATA_B3 | OBSDATA_D3 | 43 |
| 19 | GND12 | GND13 | 42 |
| 20 | HOOK0 | ITPCLK/HOOK4 | 41 |
| 21 | HOOK1 | ITPCLK#/HOOK5 | 40 |
| 22 | VCC_OBS_AB | VCC_OBS_CD | 39 |
| 23 | HOOK2 | HOOK6/RESET# | 38 |
| 24 | HOOK3 | HOOK7/DBR# | 37 |
| 25 | GND14 | GND15 | 36 |
| 26 | XDP_SDA | XDP_TDO | 35 |
| 27 | XDP_SCL | XDP_TRSTn | 34 |
| 28 | XDP_TCK1 | XDP_TDI | 33 |
| 29 | XDP_TCK0 | XDP_TMS | 32 |
| 30 | GND16 | GND(XDP_PRESENT#) | 31 |

CFG17 CFG16 CFG8 CFG9 CFG10 CFG11 CFG19 CFG18 CFG12 CFG13 CFG14 CFG15
ITP_PMODE SYS_RESET# XDP_TDO XDP_TRST# XDP_TDI XDP_TMS XDP_PRS

CFG17 [10] CFG16 [10] CFG8 [10] CFG9 [10] CFG10 [10] CFG11 [10] CFG19 [10] CFG18 [10] CFG12 [10] CFG13 [10] CFG14 [10] CFG15 [10]
CK_XDP_P [14] CK_XDP_N [14] +1V_S5 ITP_PMODE [10] TP2

XDP_PRS R52 *0/S_4 R53 *0_4 PCH_SPI_IO2 [11,31]
EC-PV-01

[11,31] PCH_SPI_MOSI R61 *0_4 HOOK3 R62 *1K_4 +3V_S5

+3V *1K_4 R59 SYS_RESET#
C85 *0.1U/16V_4

+VCCIO
R398 150/F_4
PWR_DEBUG
R64 *10K_4

+1V_S5
C99 0.1U/16V_4
C97 0.1U/16V_4

## APS

CN2 *50501-0180N-001

EC-PV-01 R205 *0/S_4
+3V_S5
SUSB# [5,29]
SLP_S5# [5,29]
SUSC# [5,29]
SLP_A# [5]
RTC_RST# [14]
DNBSWON#
SYS_RESET# [5]
R199 *0_4_S PM_SLP_S0# [5,29]

C515 0.1U/16V_4
+3V R463 *0_4_S XDP_TDO
[5,29] HWPG
XDP_TDI
XDP_TMS
XDP_TRST#

U19 *SN74CBTLV3126RGYR

| | | | |
|---|---|---|---|
| 14 | VCC | | |
| 2 | 1A | 1B | 3 |
| 1 | 1OE | | |
| 5 | 2A | 2B | 6 |
| 4 | 2OE | | |
| 9 | 3A | 3B | 8 |
| 10 | 3OE | | |
| 12 | 4A | 4B | 11 |
| 13 | 4OE | | |
| | DPAD | | 15 |
| | GND | | 7 |

XDP_TDO_CPU [3] XDP_TDI_CPU [3] XDP_TMS_CPU [3] XDP_TRST#_CPU [3]

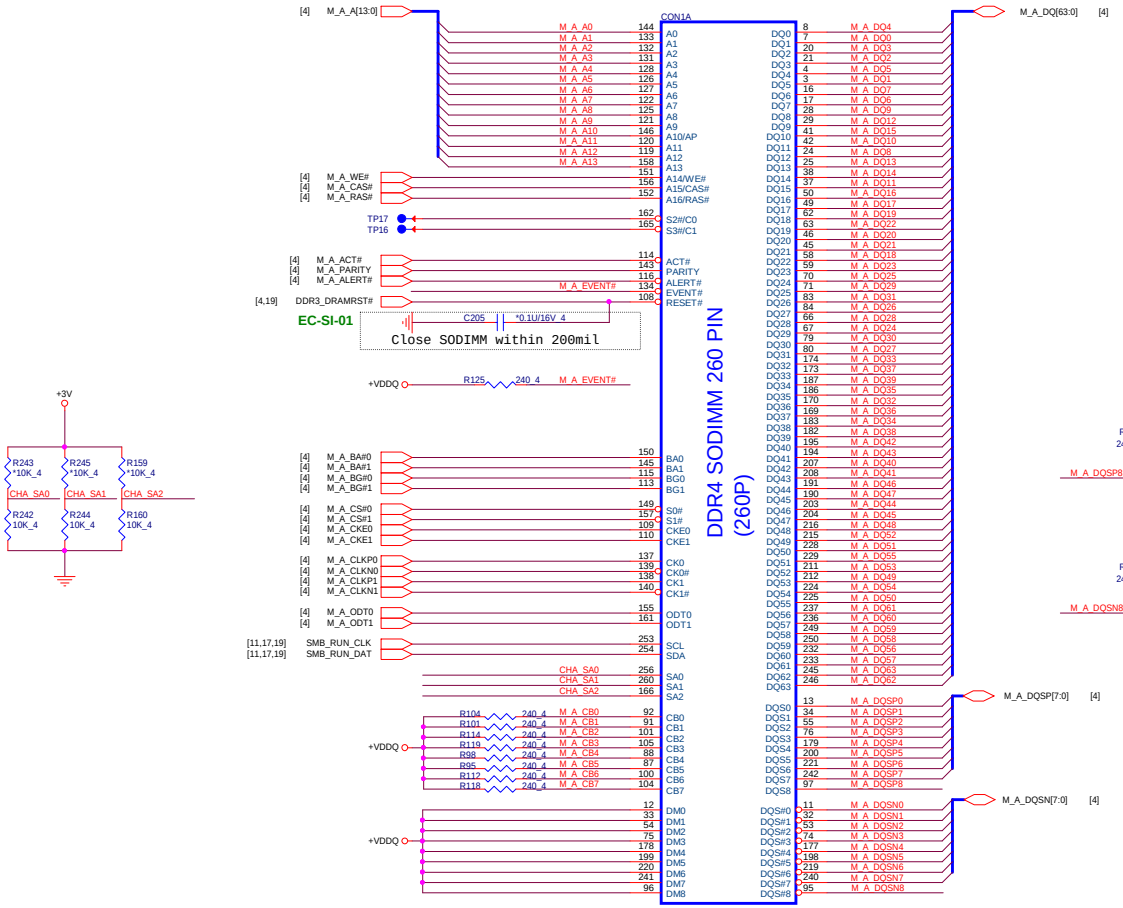
[3] JTAGX_PCH
[3] JTAG_TMS_PCH
[3] JTAG_TDI_PCH
[3] JTAG_TDO_PCH
[3] JTAG_TCK_PCH

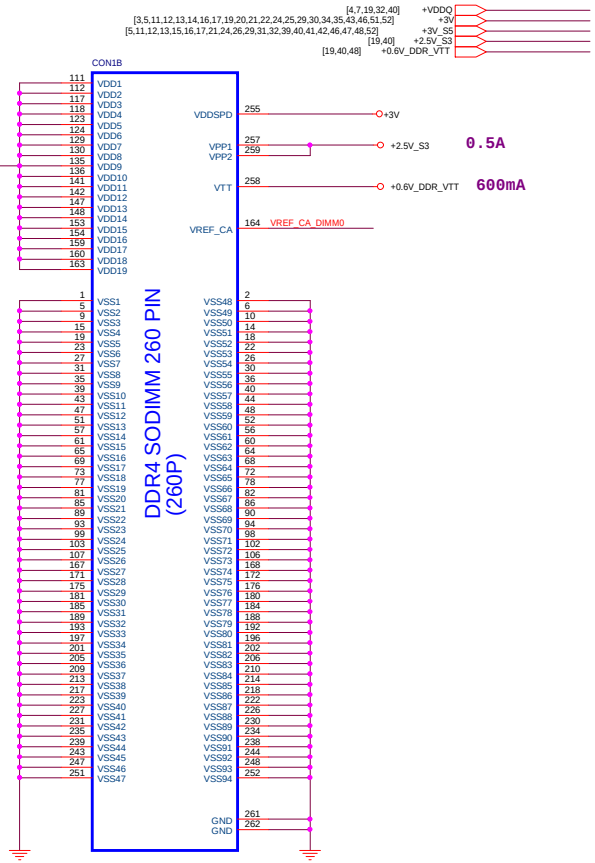
+VCCIO R450 51_4
R449 *0_4 XDP_TDO
XDP_TCK0
XDP_TMS
XDP_TDI
XDP_TDO
R446 *0_4 XDP_TDI
R445 *0_4 XDP_TCK0
XDP_TCK1

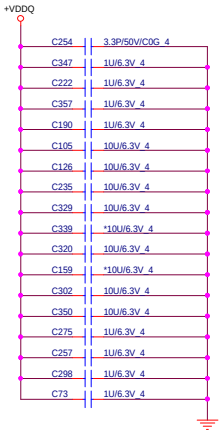
HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

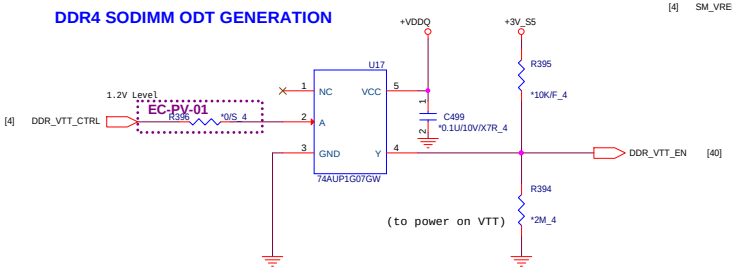
| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL CPU XDP/APS | 1A |
| Date: Wednesday, March 09, 2016 | Sheet 17 of 58 | |



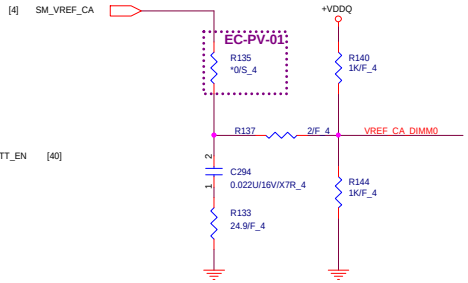




## DDR4 SODIMM ODT GENERATION




## VREF CA DIMM0 Solution



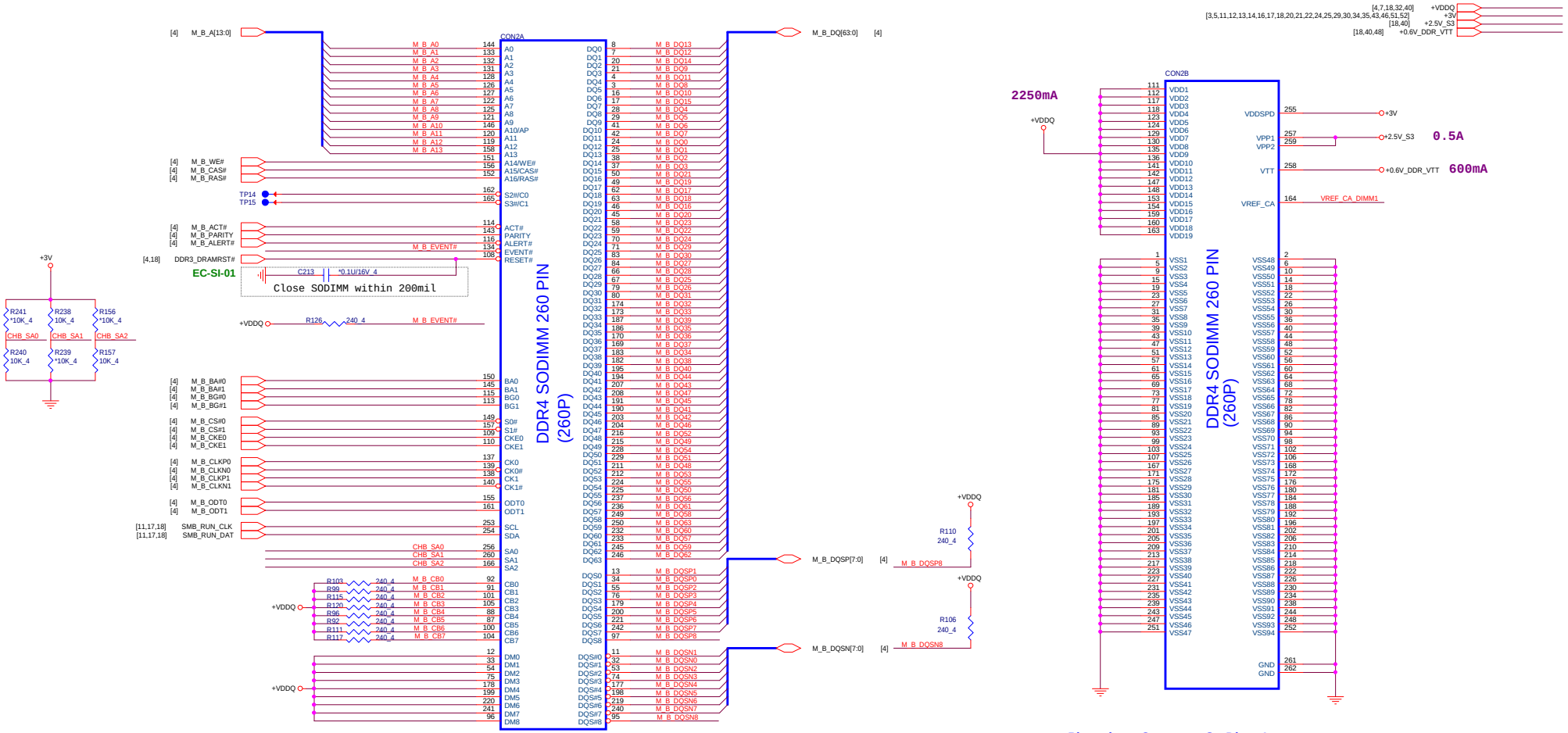

HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR4 SODIMM H=8 | 1A |

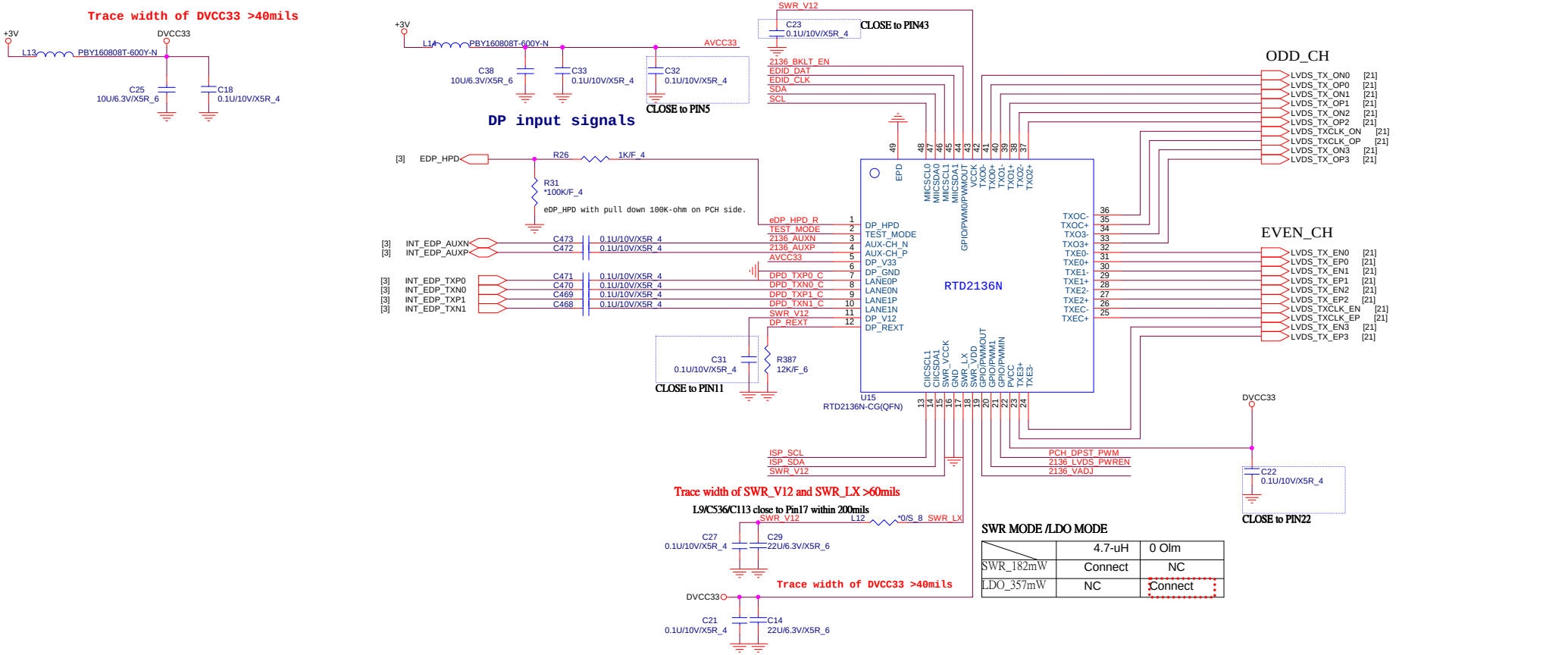
Date: Tuesday, February 02, 2016 Sheet 18 of 58


CON2A
DDR4 SODIMM 260 PIN
(260P)
EC-SI-01
Close SODIMM within 200mil
CON2B
2250mA
0.5A
600mA
VREF_CA_DIMM1
Place these Caps near So-Dimm1
VREF CA DIMM1 Solution
EC-PV-01
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
DDR4 SODIMM H=4

# eDP to LVDS (RTD2136N-CG)



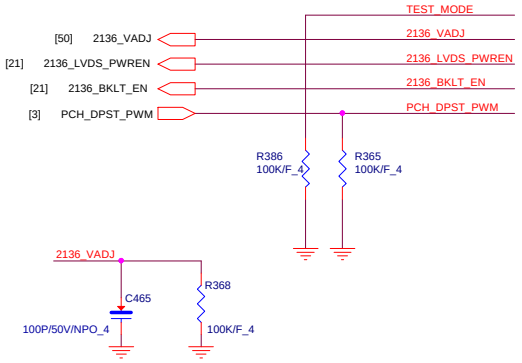
[3,5,11,12,13,14,16,17,18,19,21,22,24,25,29,30,34,35,43,46,51,52] +3V




SWR MODE /LDO MODE

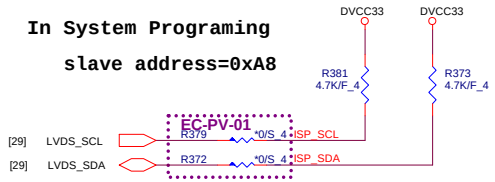
| | 4.7-uH | 0 Olm |
|---|---|---|
| SWR_182mW | Connect | NC |
| LDO_357mW | NC | Connect |

## GPIO & TESTing signals




## In System Programing

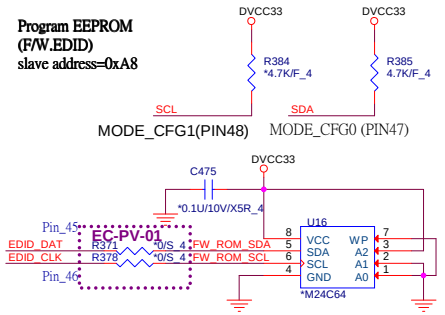
slave address=0xA8




| RTD2136N: Mode Selestion | | MODE_CFG0 (PIN47) | |
|---|---|---|---|
| | | 0 | 1 |
| MODE_CFG1(PIN48) | 0 | X | EP MODE |
| | 1 | ROM ONLY MODE | EEPROM MODE |

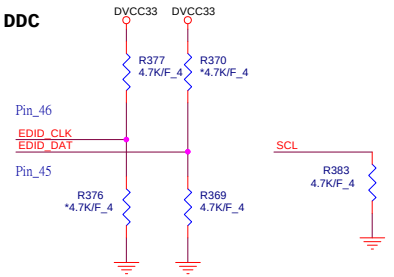
## Program EEPROM (F/W.EDID)

slave address=0xA8




The Program EEPROM must be 2 byte addressing device

## DDC




Reserve pull down for EPMODE

HP Restricted Secret

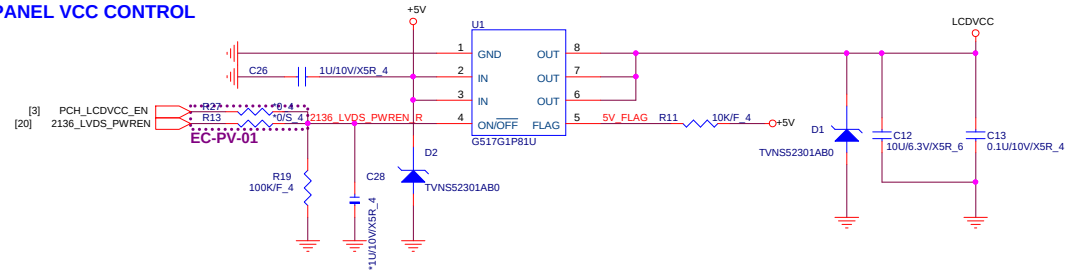
Quanta Computer Inc.

PROJECT: HP-Hawaii

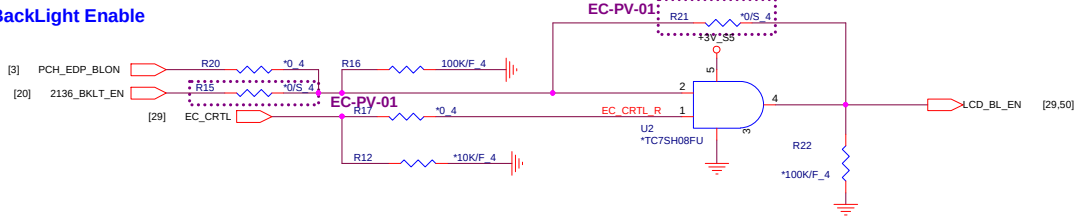
| Size | Document Number | Rev |
|---|---|---|
| Custom | eDP to LVDS converter | 1A |

Date: Thursday, January 28, 2016 Sheet 20 of 58

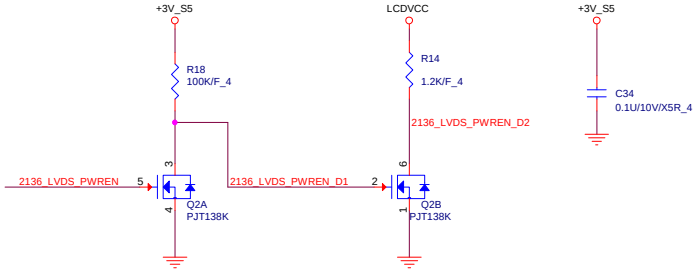
## PANEL VCC CONTROL



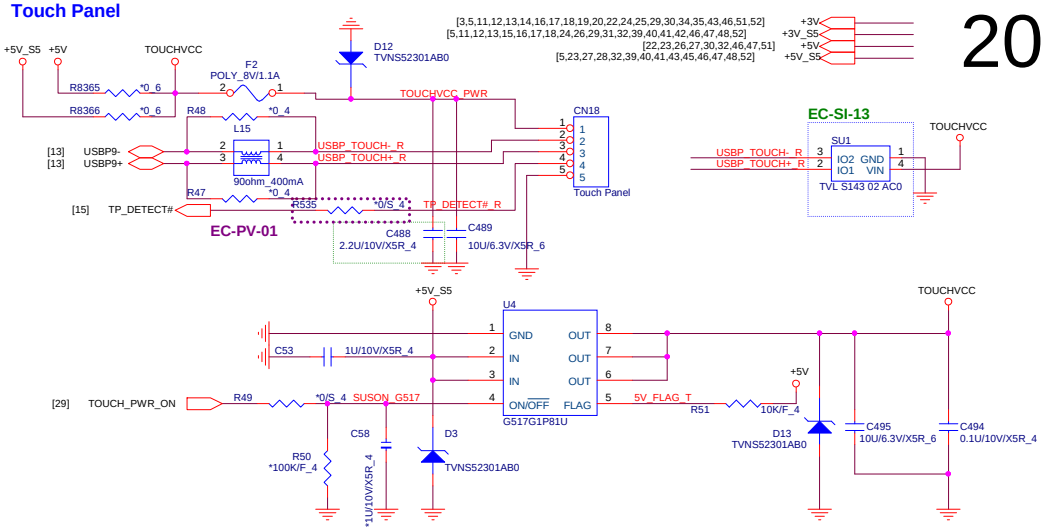

## BackLight Enable



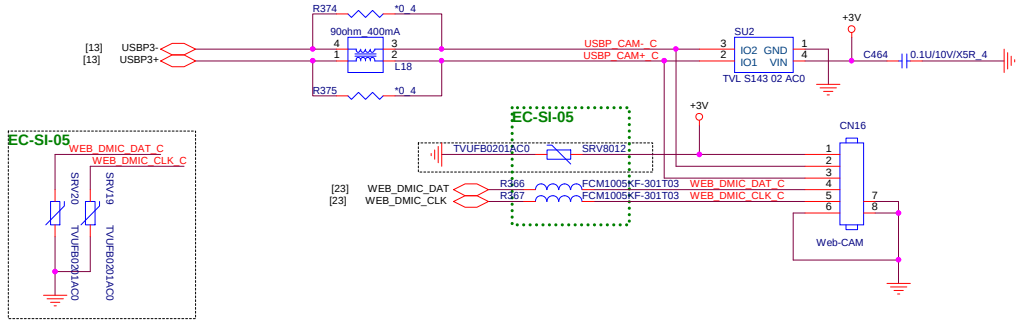

## LCDVCC Discharge Circuit

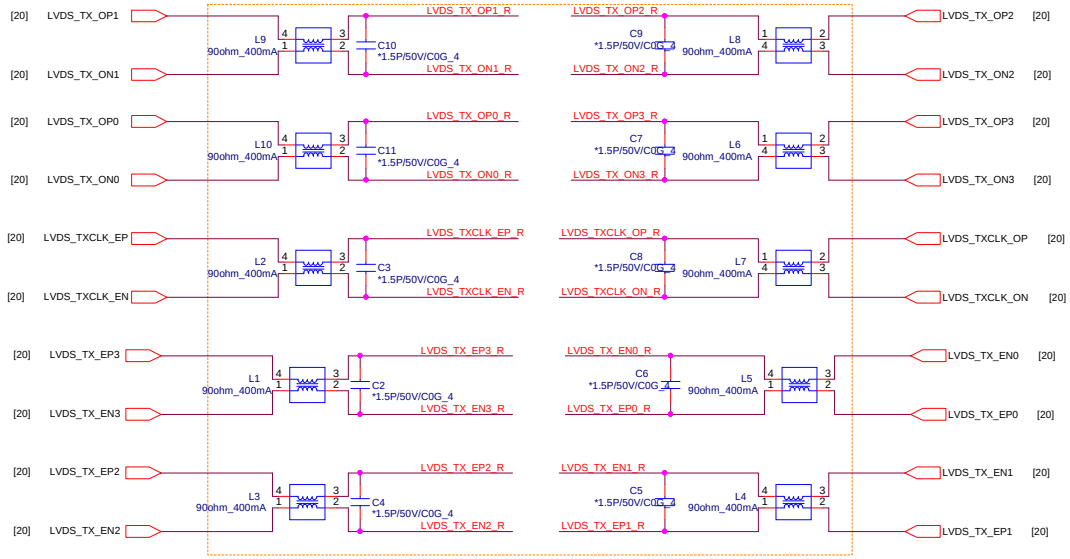



## Touch Panel

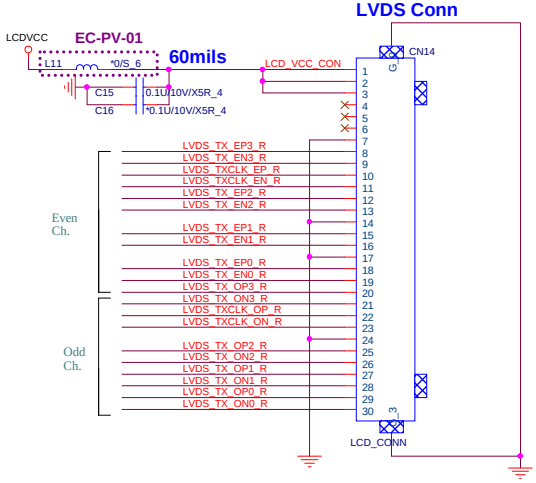



## CCD CONN




## LVDS Conn




HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

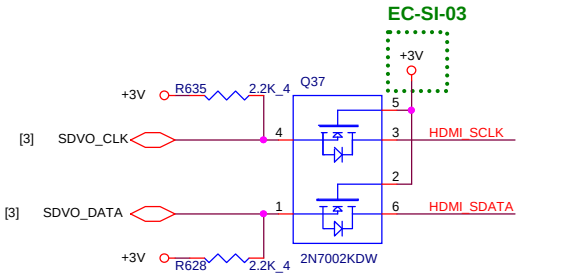
| Size | Document Number | Rev |
|---|---|---|
| Custom | LVDS CONN/DDC/Touch Panel | 1A |
| Date: Thursday, March 17, 2016 | Sheet 21 of 58 | |

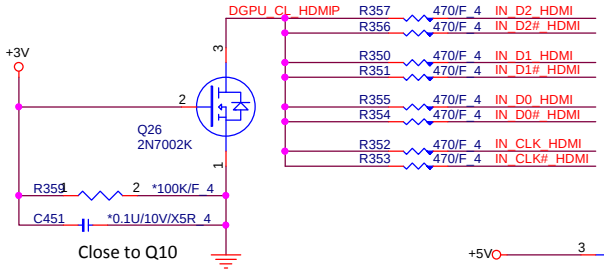
# HDMI CONN

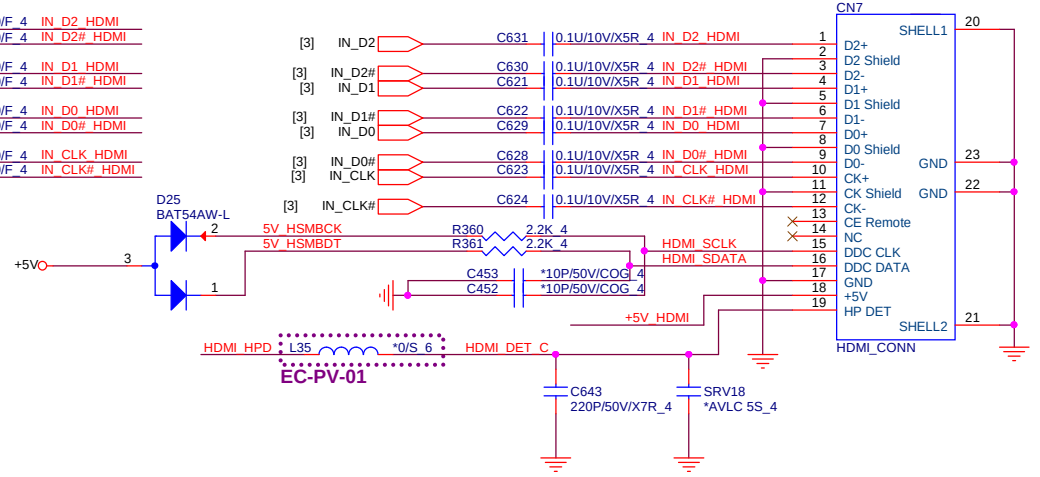


[3,5,11,12,13,14,16,17,18,19,20,21,24,25,29,30,34,35,43,46,51,52]
[21,23,26,27,30,32,46,47,51]
+3V
+5V

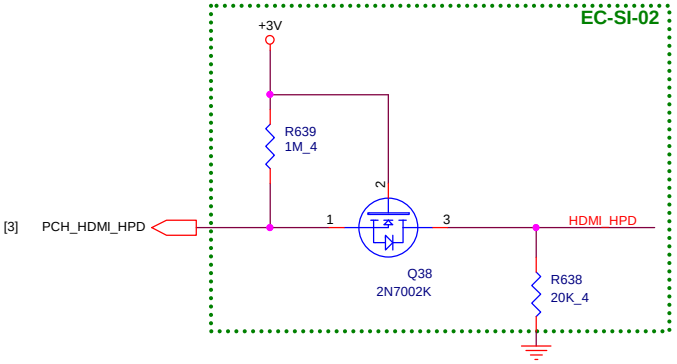
EC-SI-03



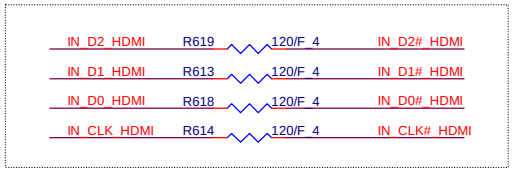



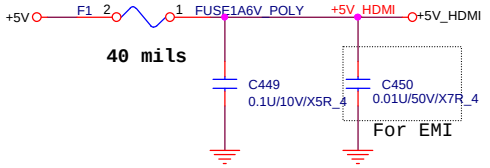




EC-SI-02

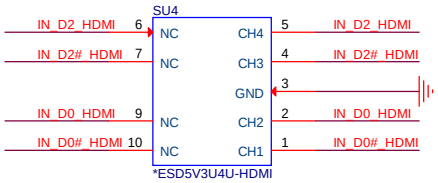


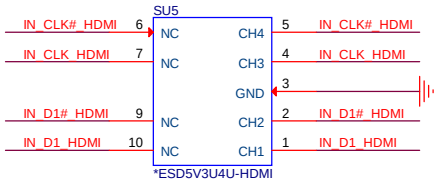

For EMI

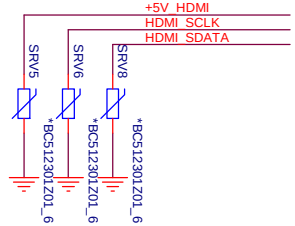



For ESD



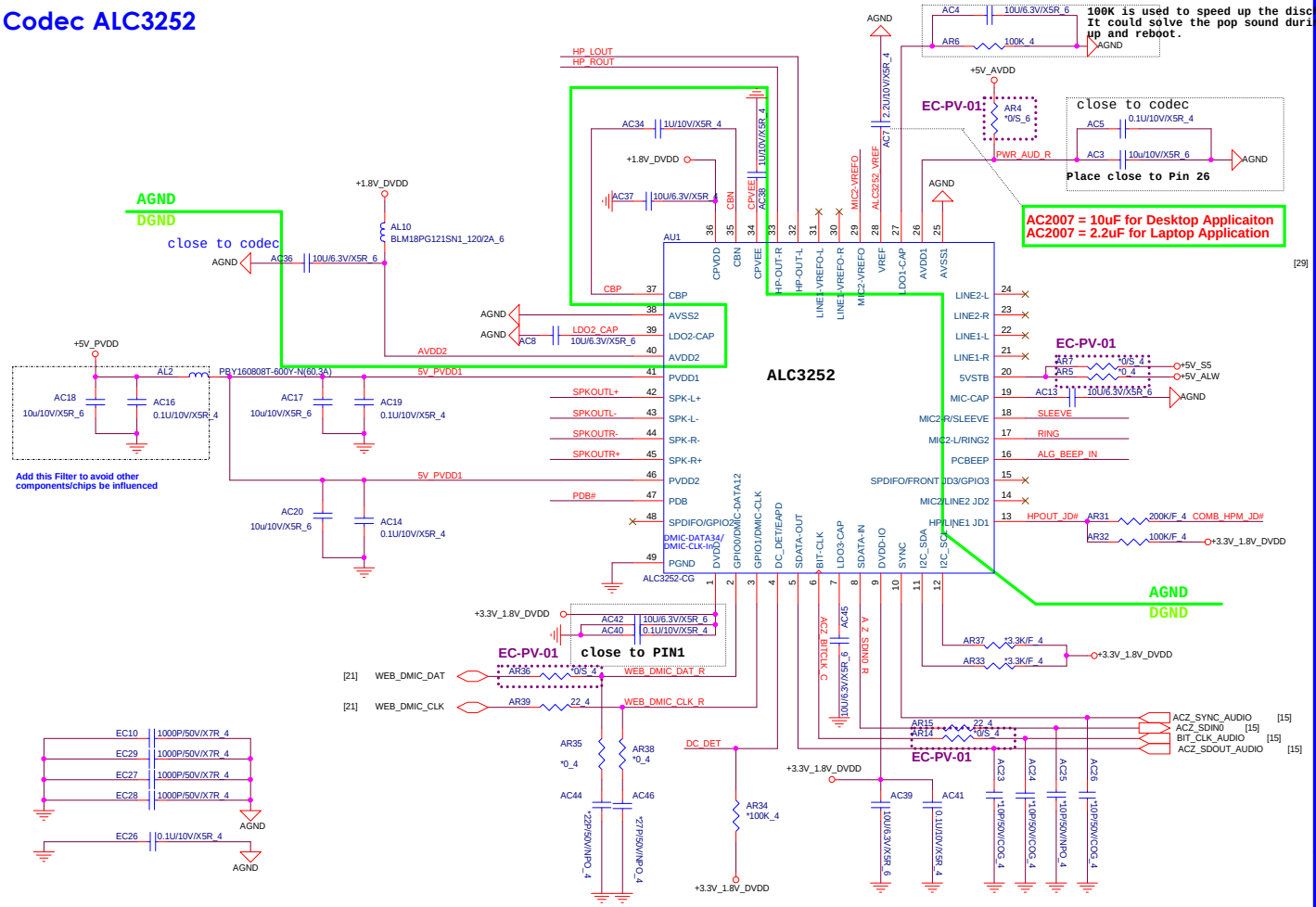

Layout note:Place close to HDMI Conn



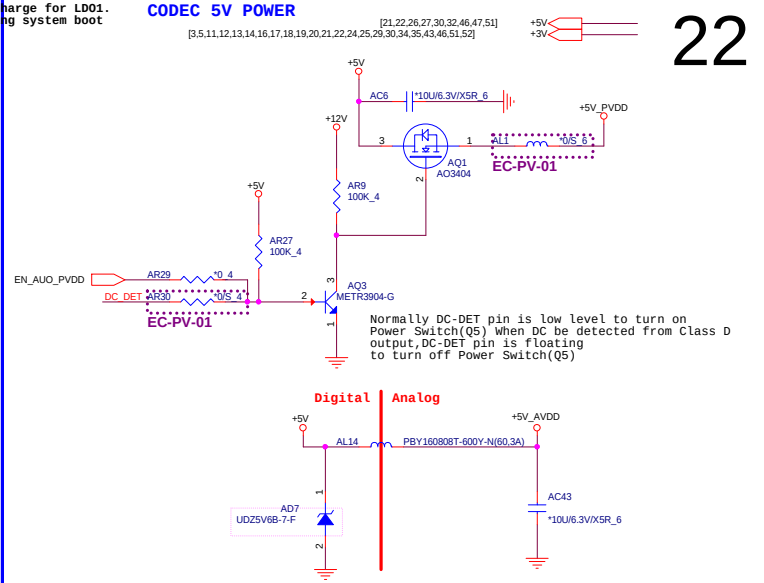
Quanta Computer Inc.
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | HDMI | 1A |
| Date: Monday, February 15, 2016 | Sheet 22 of 58 | |

# Codec ALC3252

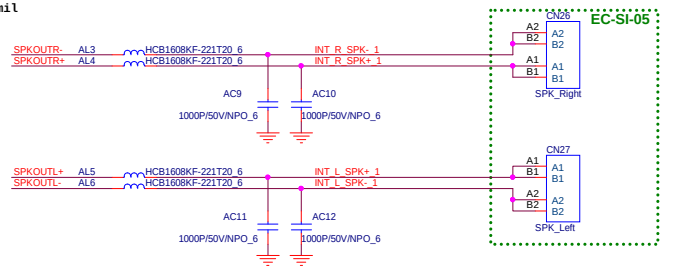



# CODEC 5V POWER

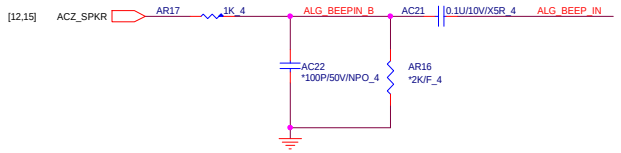



# Internal Speaker (2W, 4 ohm)

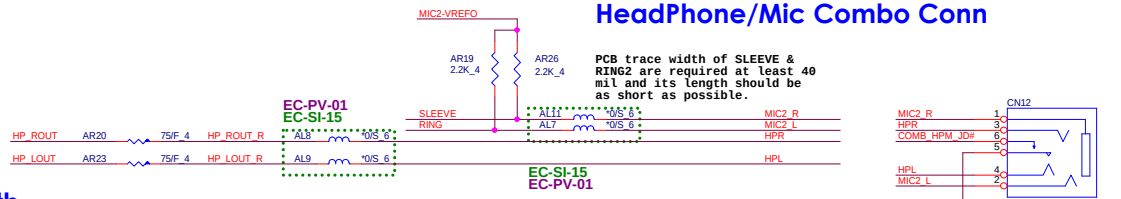
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
4 ohm : 40mil
8 ohm : 20mil



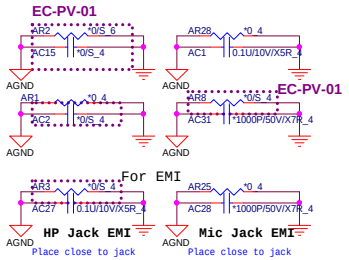

# PC BEEP

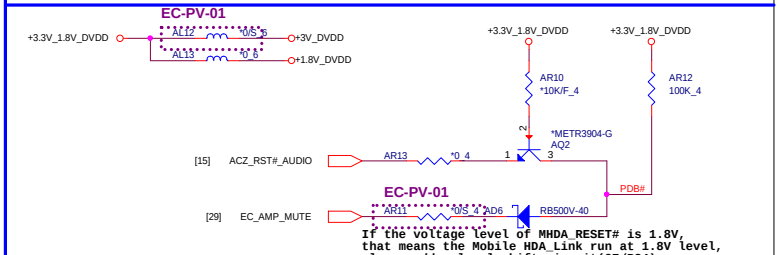


# HeadPhone/Mic Combo Conn




# CODEC Return Path




HP Restricted Secret

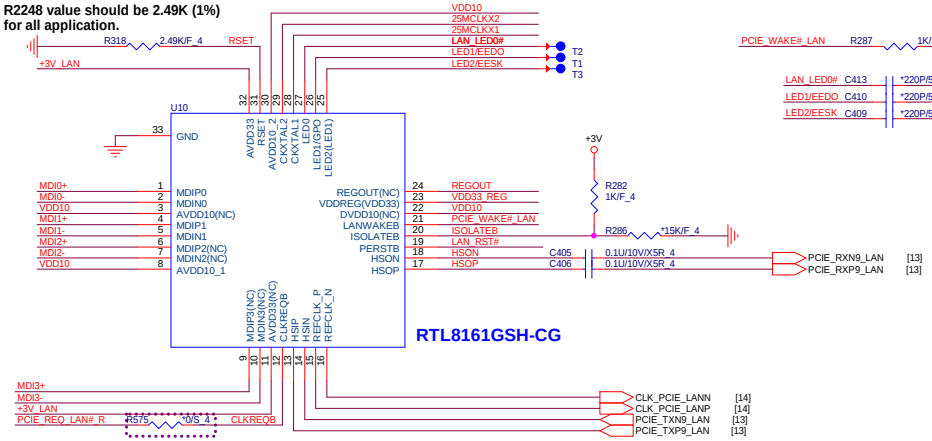
Quanta Computer Inc.

PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | Audio CODEC | 1A |

Date: Tuesday, March 22, 2016 Sheet 23 of 58

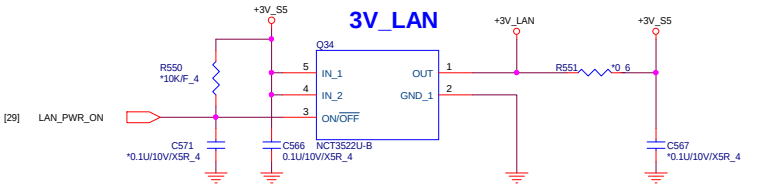
R2248 value should be 2.49K (1%) for all application.





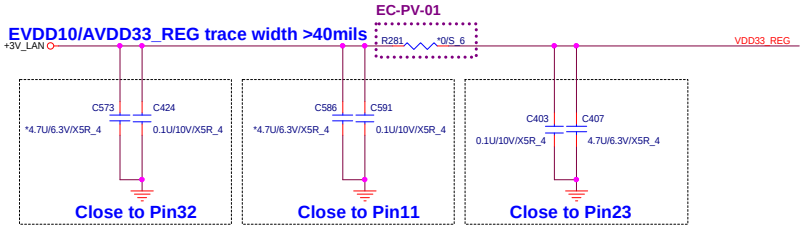


## 3V_LAN

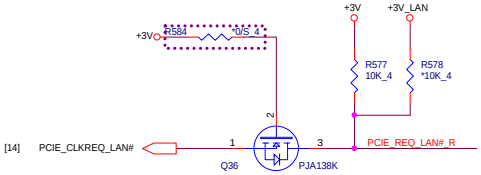


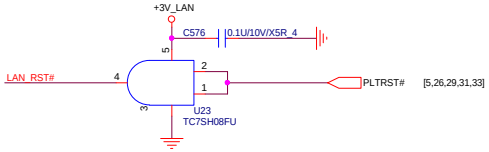

EC-PV-01

## EVDD10/AVDD33_REG trace width >40mils

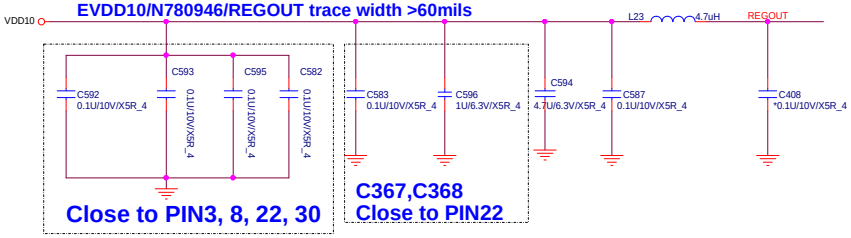



EC-PV-01

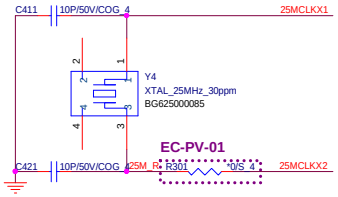


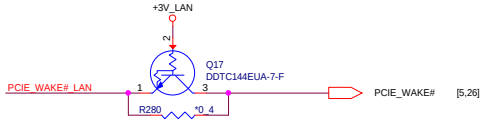

## EVDD10/N780946/REGOUT trace width >60mils



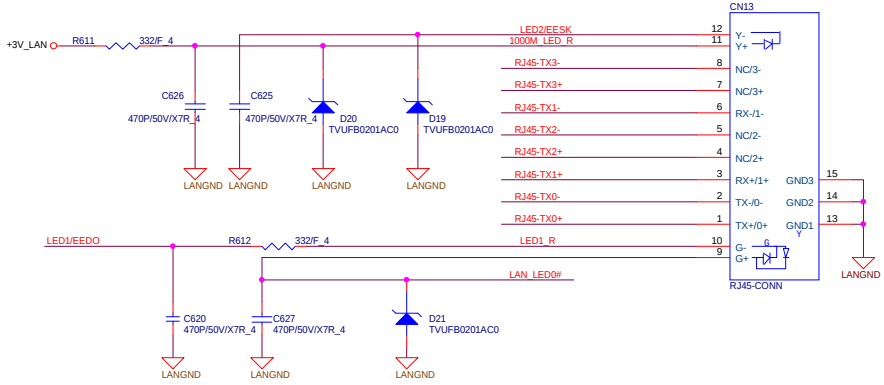

## X'tal 25MHz

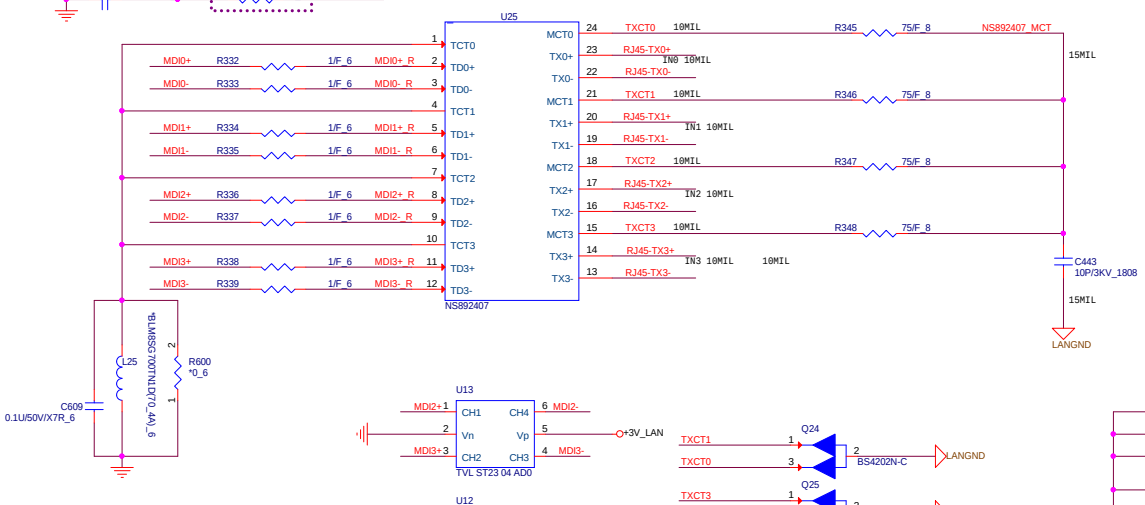



EC-PV-01




## LAN Conn

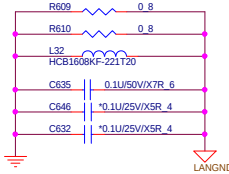









HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | LAN/RJ45 | 1A |

Date: Wednesday, March 09, 2016 Sheet 24 of 58

# HDD REDRIVER

C44,C45,C46,C47 CLOSE TO RE-DRIVER IC

[13] SATA_TXP0 — C616 *0.01U/50V/X7R_4, R341 *0/S_4 — SATA_TX0_P_RE — SATA_TX0_P_CON [26]
[13] SATA_TXN0 — C614 *0.01U/50V/X7R_4, R340 *0/S_4 — SATA_TX0_N_RE — SATA_TX0_N_CON [26]
[13] SATA_RXN0 — C612 *0.01U/50V/X7R_4, R331 *0/S_4 — SATA_RX0_N_RE — SATA_RX0_N_CON [26]
[13] SATA_RXP0 — C610 *0.01U/50V/X7R_4, R330 *0/S_4 — SATA_RX0_P_RE — SATA_RX0_P_CON [26]

3 PAD DESIGN

EC-PV-01

[3,5,11,12,13,14,16,17,18,19,20,21,22,24,29,30,34,35,43,46,51,52] +3V

+3V — R592 *0/S_4 — +3V_HDD_REDRIVER

EC-PV-01

+3V
R607 *4.7K_4 — HDD_A_EQ1
R606 *4.7K_4 — HDD_A_EQ2
R608 *4.7K_4 — HDD_B_EQ2
R605 *4.7K_4 — HDD_B_EQ1
R603 *4.7K_4
R602 *4.7K_4
R604 *4.7K_4
R601 *4.7K_4

+3V_HDD_REDRIVER
C618 *4.7U/6.3V/X5R_4
C619 *0.1U/10V/X5R_4
C602 *4.7U/6.3V/X5R_4
C604 *0.1U/10V/X5R_4

U24 *PS8527BTQFN20GTR2-A2

| | | | |
|---|---|---|---|
| 6 VCC | | | |
| 16 VCC | | REXT | 10 U21_REXT R598 *4.99K/F_4 |
| HDD_A_EQ1 18 A_EQ1 | | B_EQ2 | 17 HDD_B_EQ2 |
| HDD_A_EQ2 19 A_EQ2 | | B_EQ1 | 20 HDD_B_EQ1 |
| SATA_TX0_P_RE 1 IN0P | | OUT0P | 15 SATA_TXP0+_R [26] |
| SATA_TX0_N_RE 2 IN0M | | OUT0M | 14 SATA_TXN0-_R [26] |
| SATA_RX0_N_RE 4 OUT1N | | IN1N | 12 SATA_RXN0-_R [26] |
| SATA_RX0_P_RE 5 OUT1P | | IN1P | 11 SATA_RXP0+_R [26] |
| +3V R593 *10K/F_4 U21_EN 7 EN | | GND | 3, 13, 22 |
| +3V R597 *4.7K_4 U21_A_DE 9 A_DE | | EP_AGND | 23 |
| R595 *4.7K_4 U21_B_DE 8 B_DE | | EP | 24 |
| R594 *4.7K_4 | R596 *4.7K_4 | 21 | 25 |

# ODD REDRIVER

C53,C57,C58,C59 CLOSE TO RE-DRIVER IC

[13] SATA_TXP1 — C417 *0.01U/50V/X7R_4, R573 *0/S_4 — SATA_TX1_P_RE — SATA_TX1_P_CON [26]
[13] SATA_TXN1 — C416 *0.01U/50V/X7R_4, R572 *0/S_4 — SATA_TX1_N_RE — SATA_TX1_N_CON [26]
[13] SATA_RXN1 — C415 *0.01U/50V/X7R_4, R571 *0/S_4 — SATA_RX1_N_RE — SATA_RX1_N_CON [26]
[13] SATA_RXP1 — C414 *0.01U/50V/X7R_4, R570 *0/S_4 — SATA_RX1_P_RE — SATA_RX1_P_CON [26]

3 PAD DESIGN

EC-PV-01

+3V — R599 *0/S_4 — +3V_ODD_REDRIVER

EC-PV-01

+3V
R583 *4.7K_4 — ODD_A_EQ1
R576 *4.7K_4 — ODD_A_EQ2
R586 *4.7K_4 — ODD_B_EQ2
R574 *4.7K_4 — ODD_B_EQ1
R322 *4.7K_4
R319 *4.7K_4
R324 *4.7K_4
R305 *4.7K_4

+3V_ODD_REDRIVER
C427 *4.7U/6.3V/X5R_4
C426 *0.1U/10V/X5R_4
C422 *4.7U/6.3V/X5R_4
C418 *0.1U/10V/X5R_4

U11 *PS8527BTQFN20GTR2-A2

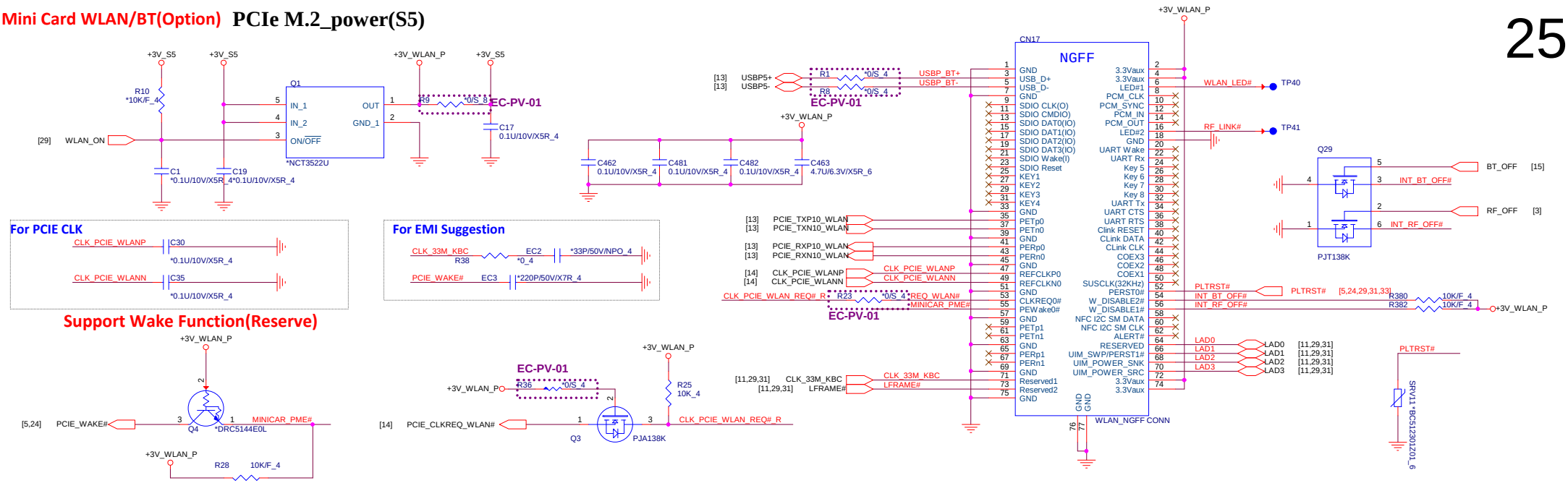
| | | | |
|---|---|---|---|
| 6 VCC | | | |
| 16 VCC | | REXT | 10 U19_REXT *4.99K/F_4 R329 |
| ODD_A_EQ1 18 A_EQ1 | | B_EQ2 | 17 ODD_B_EQ2 |
| ODD_A_EQ2 19 A_EQ2 | | B_EQ1 | 20 ODD_B_EQ1 |
| SATA_TX1_P_RE 1 IN0P | | OUT0P | 15 SATA_TXP1+_R [26] |
| SATA_TX1_N_RE 2 IN0M | | OUT0M | 14 SATA_TXN1-_R [26] |
| SATA_RX1_N_RE 4 OUT1N | | IN1N | 12 SATA_RXN1-_R [26] |
| SATA_RX1_P_RE 5 OUT1P | | IN1P | 11 SATA_RXP1+_R [26] |
| +3V R320 *10K/F_4 U19_EN 7 EN | | GND | 3, 13, 22 |
| +3V R328 *4.7K_4 U19_A_DE 9 A_DE | | EP_AGND | 23 |
| R325 *4.7K_4 U19_B_DE 8 B_DE | | EP | 24 |
| R323 *4.7K_4 | R326 *4.7K_4 | 21 | 25 |

HP Restricted Secret

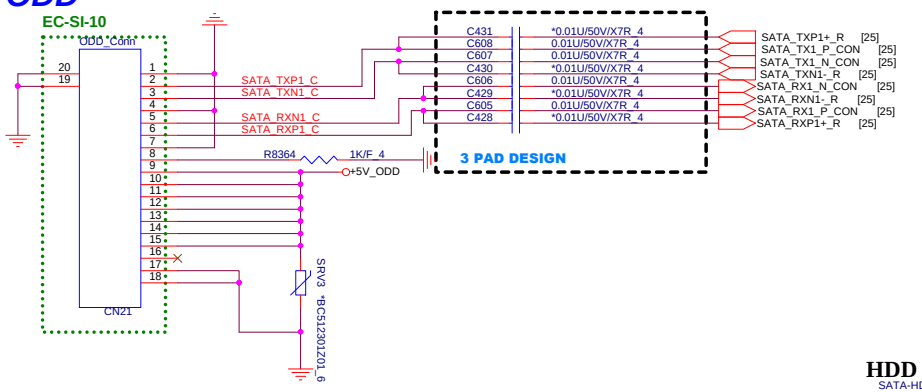
Quanta Computer Inc.
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | SATA Re-driver | 1A |
| Date: Wednesday, January 27, 2016 | Sheet 25 of 58 | |

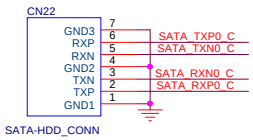
## Mini Card WLAN/BT(Option) PCIe M.2_power(S5)

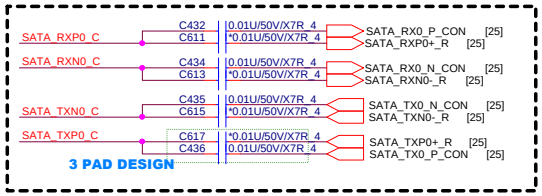



## ODD

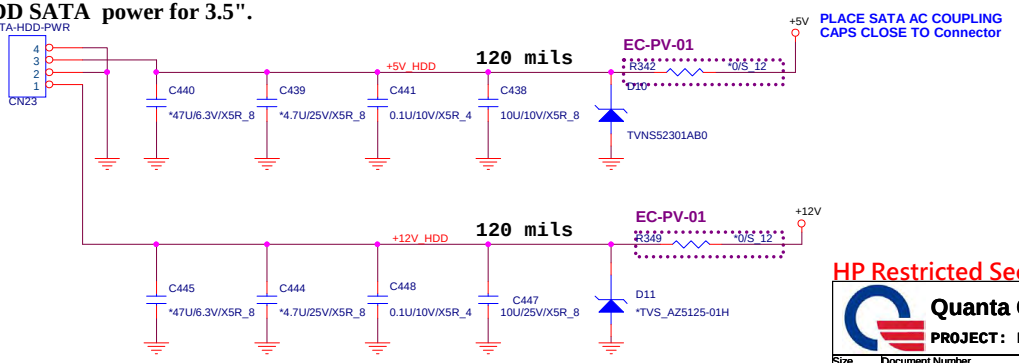


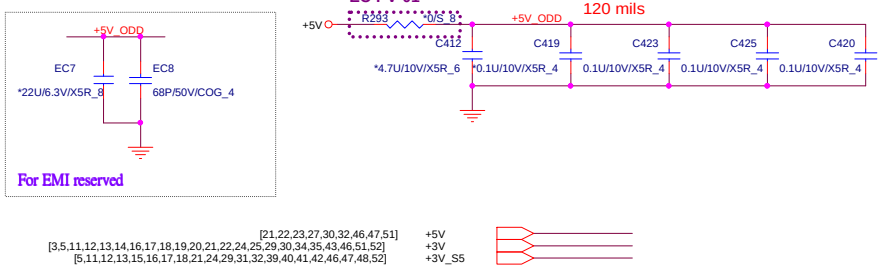

### HDD SATA signal for 3.5".




### HDD SATA power for 3.5".




[21,22,23,27,30,32,46,47,51] +5V
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[5,11,12,13,15,16,17,18,21,24,29,31,32,39,40,41,42,46,47,48,52] +3V_S5

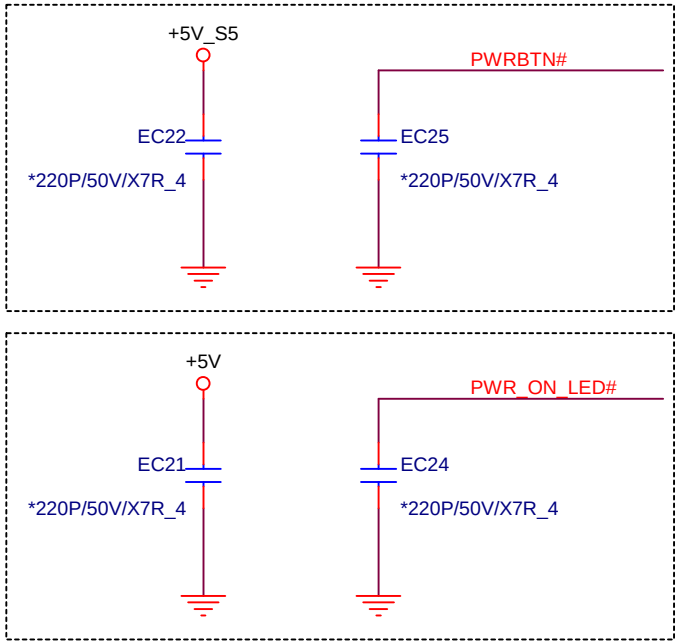
HP Restricted Secret

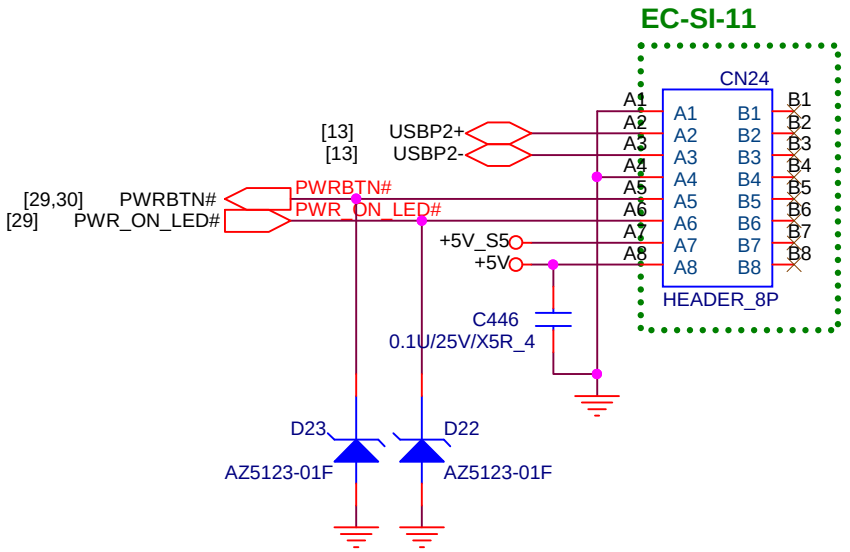
Quanta Computer Inc.
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | WLAN/HDD/ODD | 1A |
| Date: Tuesday, March 22, 2016 | Sheet 26 of 58 | |

# Card reader/Power button conn





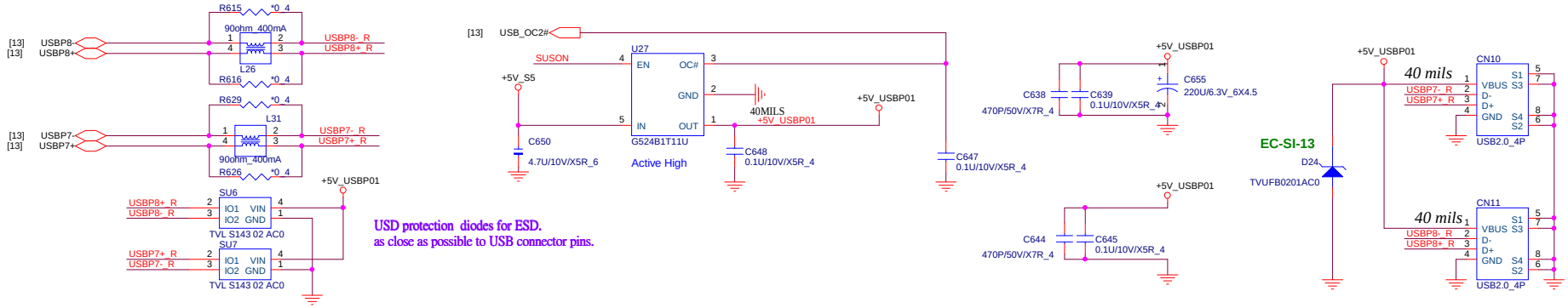

HP Restricted Secret

Quanta Computer Inc.

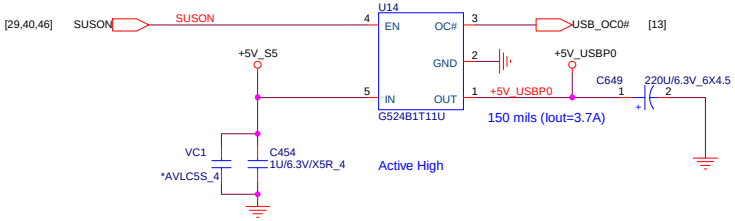
PROJECT: HP-Hawaii

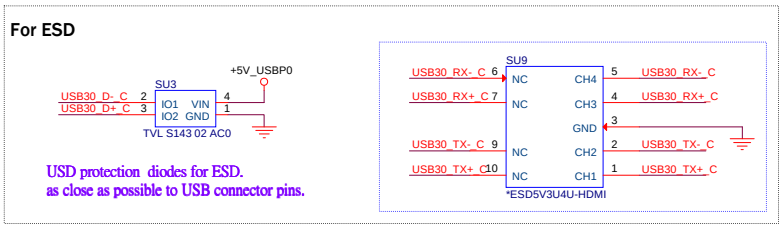
| Size | Document Number | Rev |
|---|---|---|
| A | Card reader/PWR BTN CONN | 1A |
| Date: Tuesday, March 08, 2016 | Sheet 27 of 58 | |

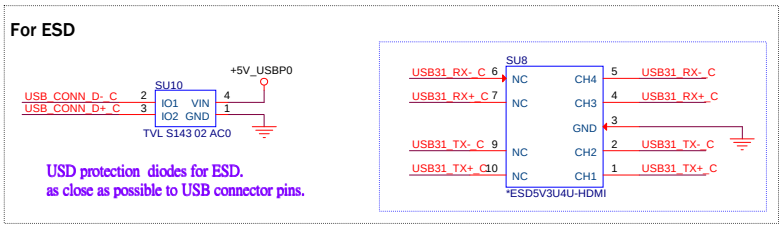
## USB 2.0

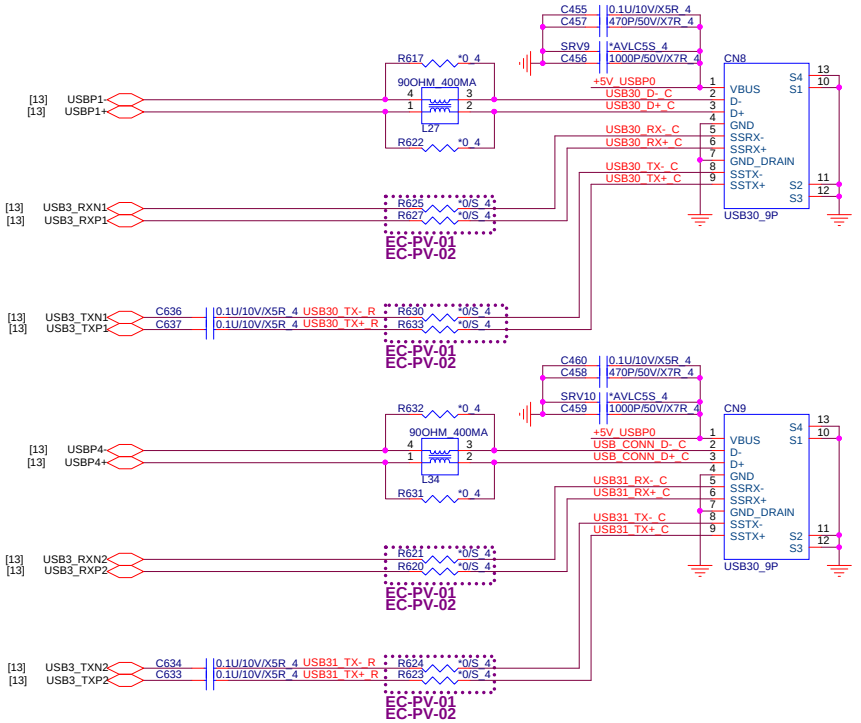



## USB 2.0/3.0 Combo




[5,21,23,27,32,39,40,41,43,45,46,47,48,52] +5V_S5

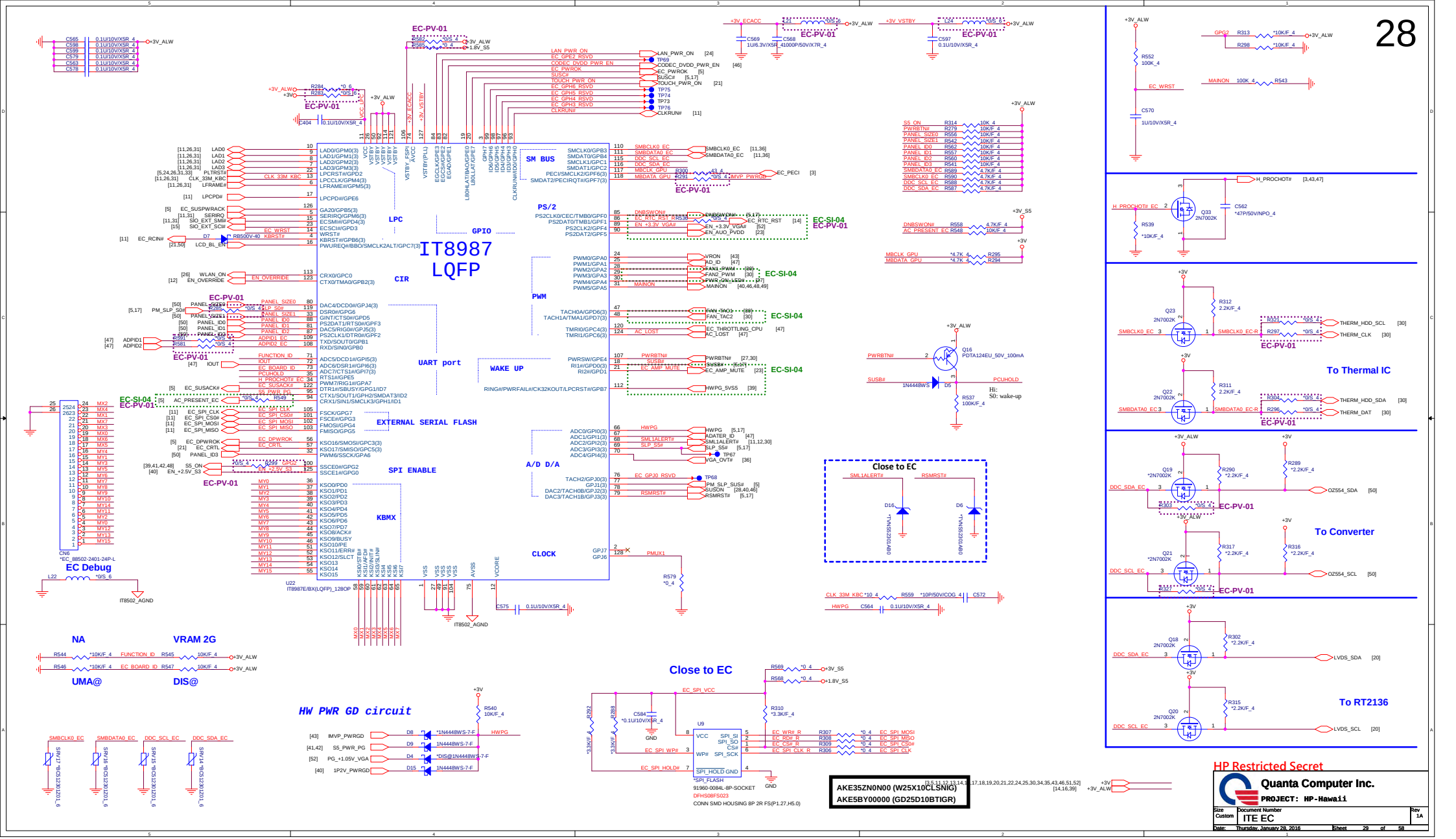
HP Restricted Secret

Quanta Computer Inc.

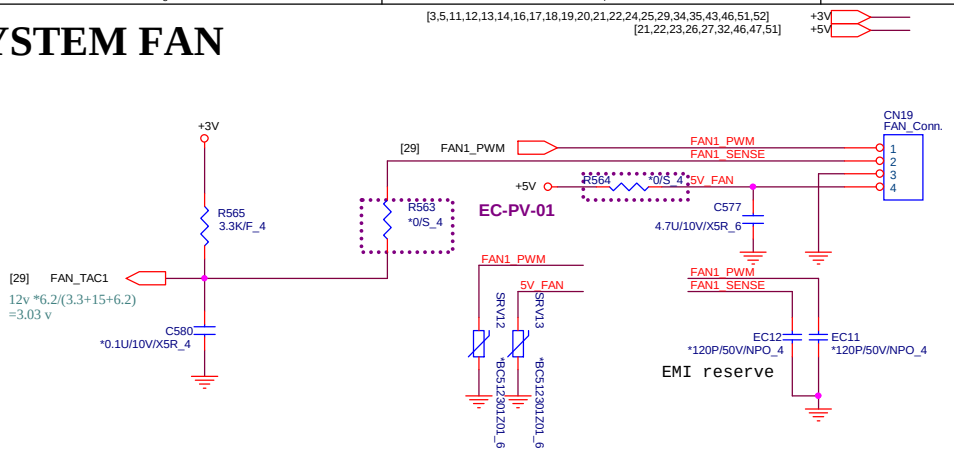
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | USB2.0/USB3.0/Hole/EMI | 1A |

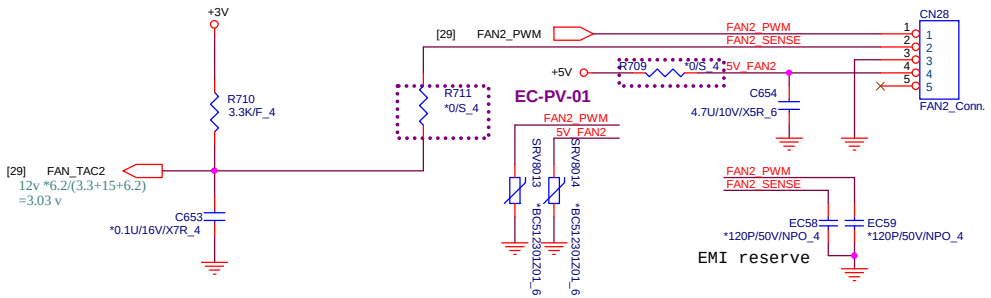
Date: Tuesday, January 26, 2016 Sheet 28 of 58


28
IT8987
LQFP
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
EC Debug
NA
VRAM 2G
UMA@
DIS@
HW PWR GD circuit
Close to EC
Close to EC
To Thermal IC
To Converter
To RT2136
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
ITE EC
AKE35ZN00N00 (W25X10CLSNIG)
AKE5BY00000 (GD25D10BTIGR)

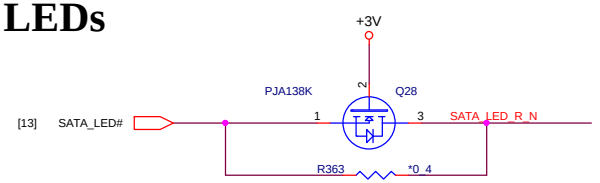
# SYSTEM FAN

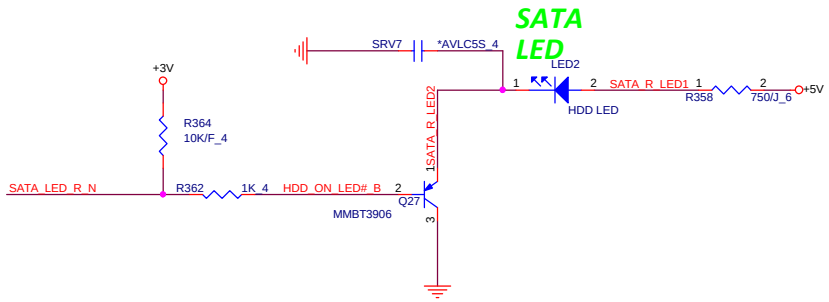


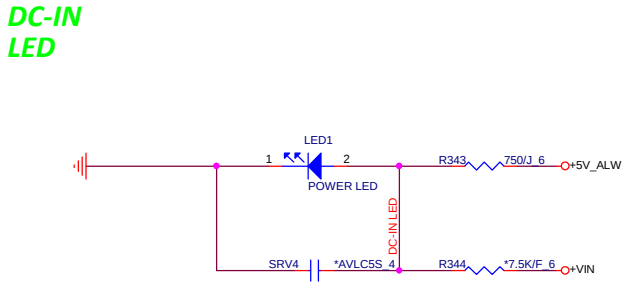

# 2nd SYSTEM FAN (RSVD)



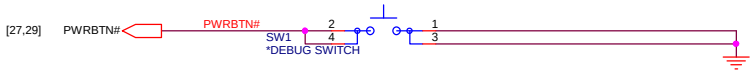

# LEDs



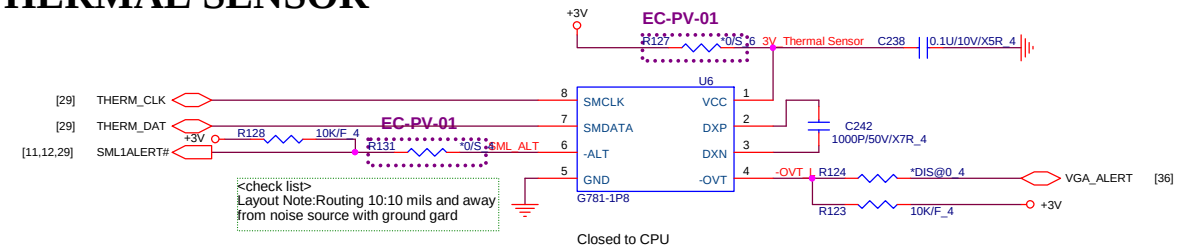




## SW1 For Debug.MP will remove it.



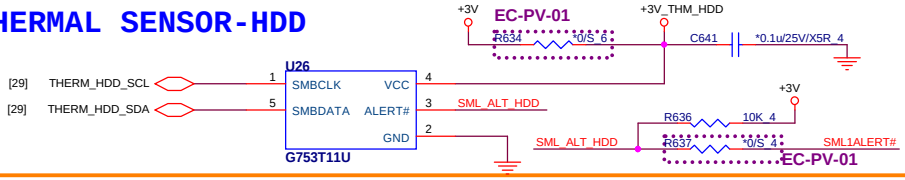

# THERMAL SENSOR




## Ambient

| Slave Adress | | | | | | |
|---|---|---|---|---|---|---|
| A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |

## THERMAL SENSOR-HDD




HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

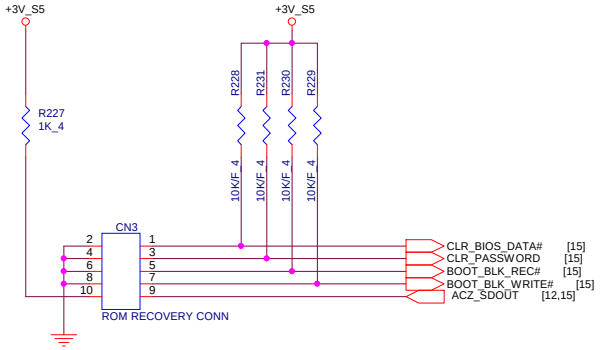
| Size | Document Number | Rev |
|---|---|---|
| Custom | Thermal/Fan/LED | 1A |

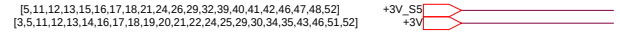
Date: Wednesday, March 09, 2016 Sheet 30 of 58

## CLR_CMOS

| Jumper | Pre-production | Production |
|---|---|---|
| BOOT_BLK_Recovery | X | X |
| BOOT_BLK_Enable | O | X |

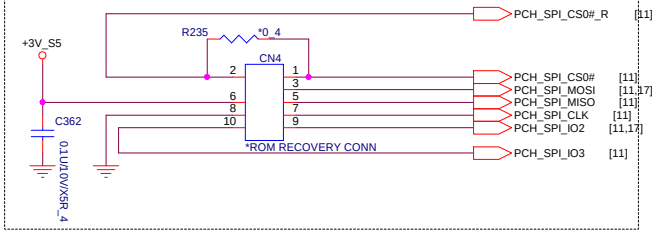
| Jumper | Type |
|---|---|
| Pop | CLR_BIOS_DAT |
| Pop | CLR_PASSWD |
| Pop | BOOT_BLK_Recovery |
| Pop | BOOT_BLK_Enable |



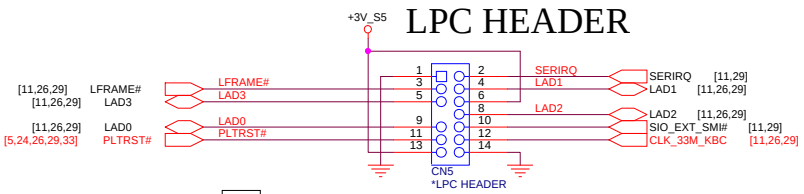




ON Chip select:Default:iinsatall (PROTO only)
CONN MINI JUMPER 2P FS (P2.0,H5.0)

## ROM recovery (for pre-production only)

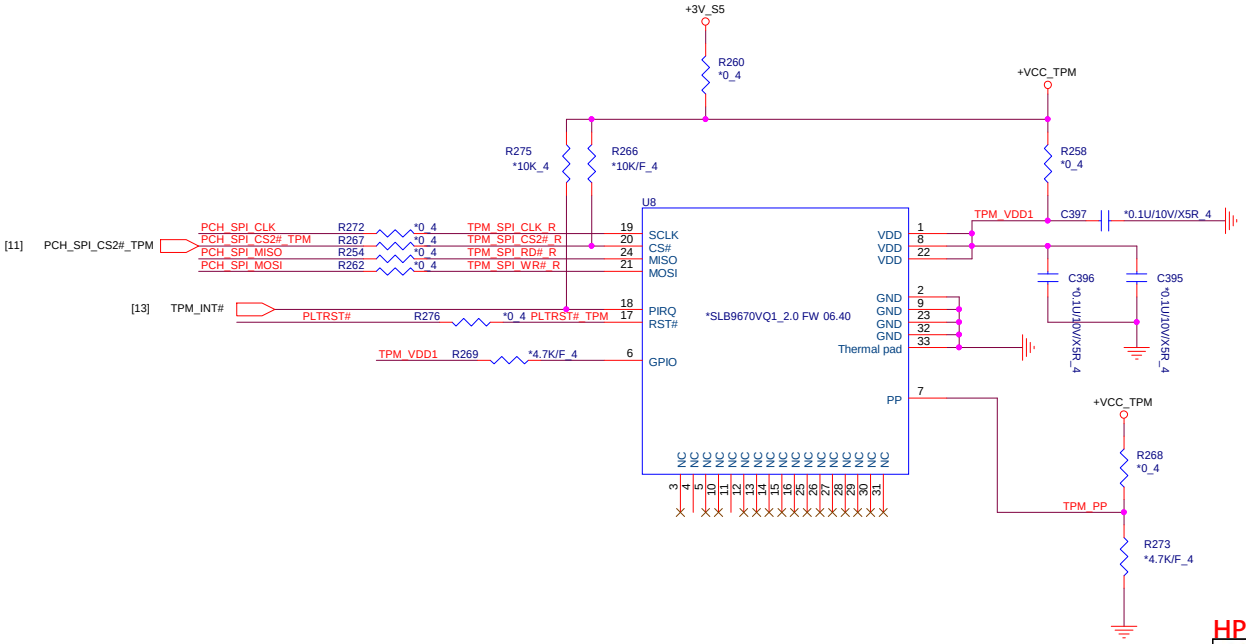



## LPC HEADER




CLR_PASSWORD Default:install
CONN MINI JUMPER 2P FS (P2.0,H5.0)

## TPM (1.2 or 2.0)




HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

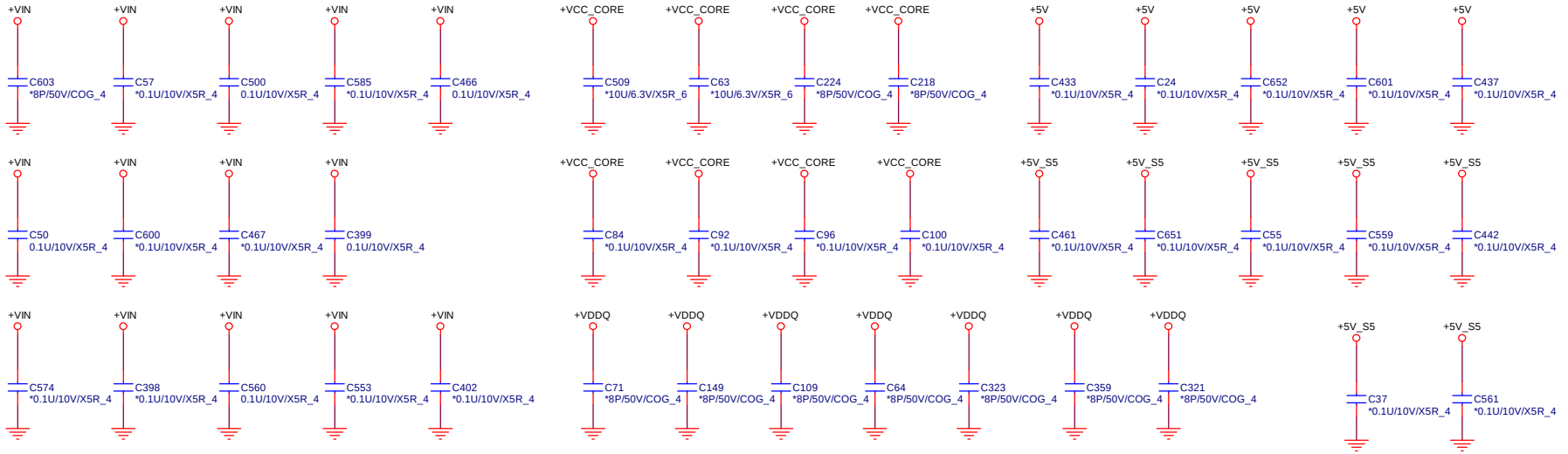
| Size | Document Number | Rev |
|---|---|---|
| Custom | Jumper/LPC Header | 1A |

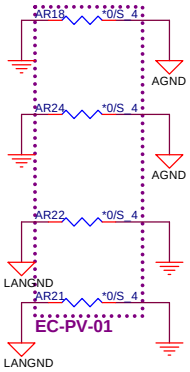
Date: Friday, December 18, 2015 Sheet 31 of 58

# RF/EMI Suggestion

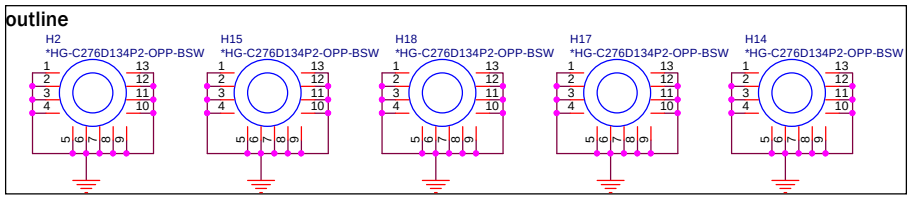


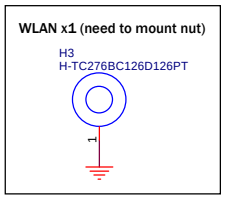
[4,7,18,19,40] +VDDQ
[6,43,44] +VCC_CORE
[30,39,40,41,43,44,45,46,47,48,49,50,51,52] +VIN

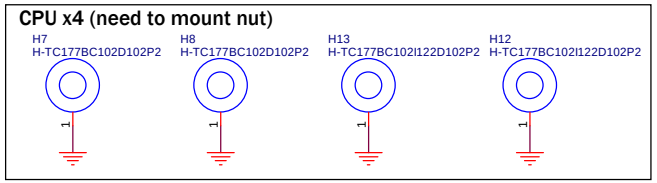


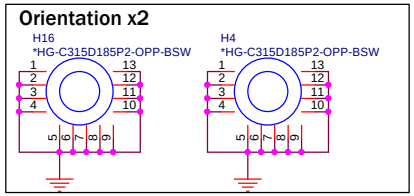



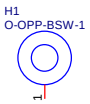

# Holes

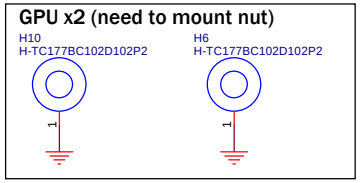


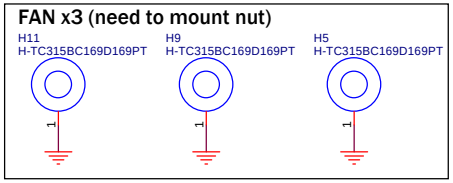



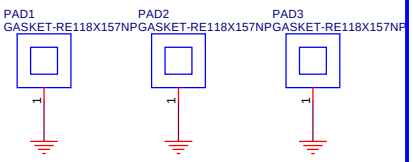



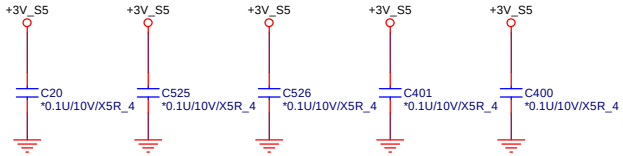

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Quanta Computer Inc.
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | EMI/RF/Holes | 1A |
| Date: Thursday, March 17, 2016 | Sheet 32 of 58 | |

[34,35,52] +1.05V_VGA
[35,36,37,51,52] +3.3V_VGA

U18A

1/14 PCI_EXPRESS

## PEX_IOVDD + PEX_IOVDDQ = 1.042A

+1.05V_VGA

Near GPU
C70 DIS@22U/6.3VS_6
C69 *DIS@22U/6.3VS_6
C65 *DIS@10U/6.3VS_6
C68 DIS@10U/6.3VS_6
C93 DIS@4.7U/6.3V_6

C88 DIS@1U/6.3V_4
C83 *DIS@1U/6.3V_4

Under GPU

AA22 AB23 AC24 AD25 AE26 AE27 — PEX_IOVDD

C119 DIS@22U/6.3VS_6
C95 *DIS@22U/6.3VS_6
C80 *DIS@10U/6.3VS_6
C103 DIS@10U/6.3VS_6
C79 DIS@4.7U/6.3V_6

Near GPU

C72 DIS@1U/6.3V_4
C66 *DIS@1U/6.3V_4

Under GPU

AA10 AA12 AA13 AA16 AA18 AA19 AA20 AA21 AA22 AC23 AD24 AE25 AF26 AF27 — PEX_IOVDDQ

## PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

+3.3V_VGA

C134 DIS@0.1U/16V_4
C143 DIS@4.7U/6.3V_6
C154 DIS@4.7U/6.3V_6

Near GPU

AA8 AA9 — PEX_PLL_HVDD
AB8 — PEX_SVDD_3V3

[51] VGA_VDD_SEN — F2 — VDD_SENSE
[51] VGA_GND_SEN — F1 — GND_SENSE

*DIS@200/F_4 R397
PEX_TSTCLK AF22 — PEX_TSTCLK_OUT
PEX_TSTCLK# AE22 — PEX_TSTCLK_OUT
CX300T30001 Change to 0ohm

+1.05V_VGA R68 DIS@0_6

Near GPU
DIS@4.7U/6.3V_6 C106
DIS@1U/6.3V_4 C114
PEX_PLLVDD AA14 AA15 — PEX_PLLVDD

DIS@0.1U/16V_4 C115
Under GPU

## PEX_PLLVDD = 130mA

DIS@10K/F_4 R102 TESTMODE AD9 — TESTMODE

DIS@2.49K/F_4 R55 PEX_TERMP AF25 — PEX_TERMP

PEX_WAKE AB6 — C173 *DIS@0.1U/16V_4
PEX_RST AC7 VGA_RST# — R86 *DIS@0/short_4 — PEGX_RST# [36]
PEX_CLKREQ AC6 PEX_CLKREQ# — R453 DIS@10K/F_4 — +3.3V_VGA
PEX_REFCLK AE8 — CLK_GFX_P [14]
PEX_REFCLK AD8 — CLK_GFX_N [14]

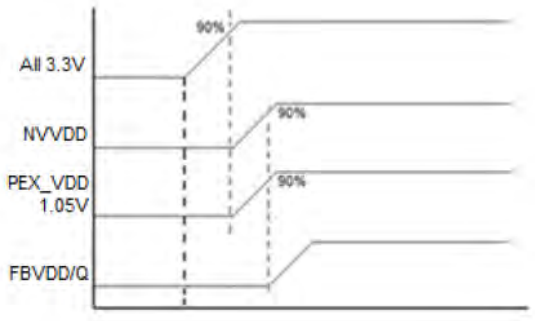
| | | | | |
|---|---|---|---|---|
| PEX_TX0 | AC9 | C_PCIE_RXP1_GPU C142 | DIS@0.22u/10V/X5R_4 | PCIE_RXP1_GPU [13] |
| PEX_TX0 | AB9 | C_PCIE_RXN1_GPU C147 | DIS@0.22u/10V/X5R_4 | PCIE_RXN1_GPU [13] |
| PEX_RX0 | AG6 | PCIE_TXP1_GPU | | PCIE_TXP1_GPU [13] |
| PEX_RX0 | AG7 | PCIE_TXN1_GPU | | PCIE_TXN1_GPU [13] |
| PEX_TX1 | AB10 | C_PCIE_RXP2_GPU C123 | DIS@0.22u/10V/X5R_4 | PCIE_RXP2_GPU [13] |
| PEX_TX1 | AC10 | C_PCIE_RXN2_GPU C128 | DIS@0.22u/10V/X5R_4 | PCIE_RXN2_GPU [13] |
| PEX_RX1 | AF7 | PCIE_TXP2_GPU | | PCIE_TXP2_GPU [13] |
| PEX_RX1 | AE7 | PCIE_TXN2_GPU | | PCIE_TXN2_GPU [13] |
| PEX_TX2 | AD11 | C_PCIE_RXP3_GPU C130 | DIS@0.22u/10V/X5R_4 | PCIE_RXP3_GPU [13] |
| PEX_TX2 | AC11 | C_PCIE_RXN3_GPU C135 | DIS@0.22u/10V/X5R_4 | PCIE_RXN3_GPU [13] |
| PEX_RX2 | AE9 | PCIE_TXP3_GPU | | PCIE_TXP3_GPU [13] |
| PEX_RX2 | AF9 | PCIE_TXN3_GPU | | PCIE_TXN3_GPU [13] |
| PEX_TX3 | AC12 | C_PCIE_RXP4_GPU C116 | DIS@0.22u/10V/X5R_4 | PCIE_RXP4_GPU [13] |
| PEX_TX3 | AB12 | C_PCIE_RXN4_GPU C118 | DIS@0.22u/10V/X5R_4 | PCIE_RXN4_GPU [13] |
| PEX_RX3 | AG9 | PCIE_TXP4_GPU | | PCIE_TXP4_GPU [13] |
| PEX_RX3 | AG10 | PCIE_TXN4_GPU | | PCIE_TXN4_GPU [13] |

PEX_TX4 AB13 AC13
PEX_RX4 AF10 AE10
PEX_TX5 AD14 AC14
PEX_RX5 AE12 AF12
PEX_TX6 AC15 AB15
PEX_RX6 AG12 AG13
PEX_TX7 AB16 AC16
PEX_RX7 AF13 AE13
PEX_TX8 AD17 AC17
PEX_RX8 AE15 AF15
PEX_TX9 AC18 AB18
PEX_RX9 AG15 AG16
PEX_TX10 AB19 AC19
PEX_RX10 AF16 AE16
PEX_TX11 AD20 AC20
PEX_RX11 AE18 AF18
PEX_TX12 AC21 AB21
PEX_RX12 AG18 AG19
PEX_TX13 AD23 AE23
PEX_RX13 AF19 AE19
PEX_TX14 AF24 AE24
PEX_RX14 AE21 AF21
PEX_TX15 AG24 AG25
PEX_RX15 AG21 AG22

NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC

GF117 GF119

bga595-nvidia-n13p-gv2-s-a2 COMMON




+3.3V_VGA

U5
DIS@TC7SH08FU
C215
DIS@0.1U/16V_4

[5,24,26,29,31] PLTRST#
[15] DGPU_HOLD_RST#
SYS_PEX_RST_R466
*DIS@0_4 SYS_PEX_RST_MON#
[36] GPU_PEX_RST_HOLD#
R473 *DISG@0/short_4

U20
*DIS@TC7SH08FU
C517
*DIS@0.1U/16V_4
PEGX_RST#
R474
DIS@100K/F_4

+3.3V_VGA

R90
DIS@10K/F_4
Q12
DIS@2N7002K
Q8
DIS@2N7002K
PEX_CLKREQ#
PCIE_CLKREQ_VGA# [14]

R464
*DIS@100K/F_4
SYS_PEX_RST_MON# [36]

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PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | N16V-GMR PCIE | 1A |

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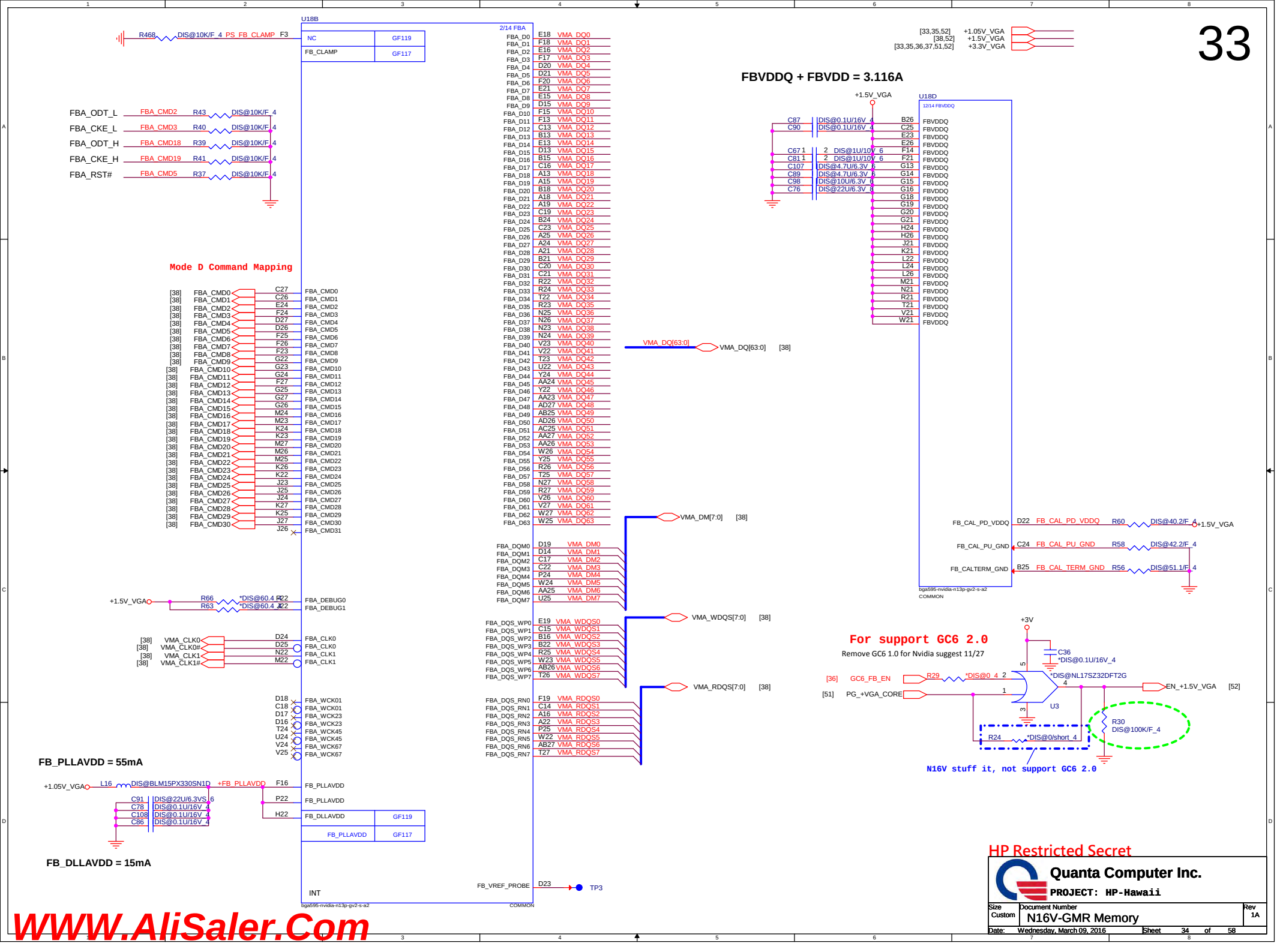

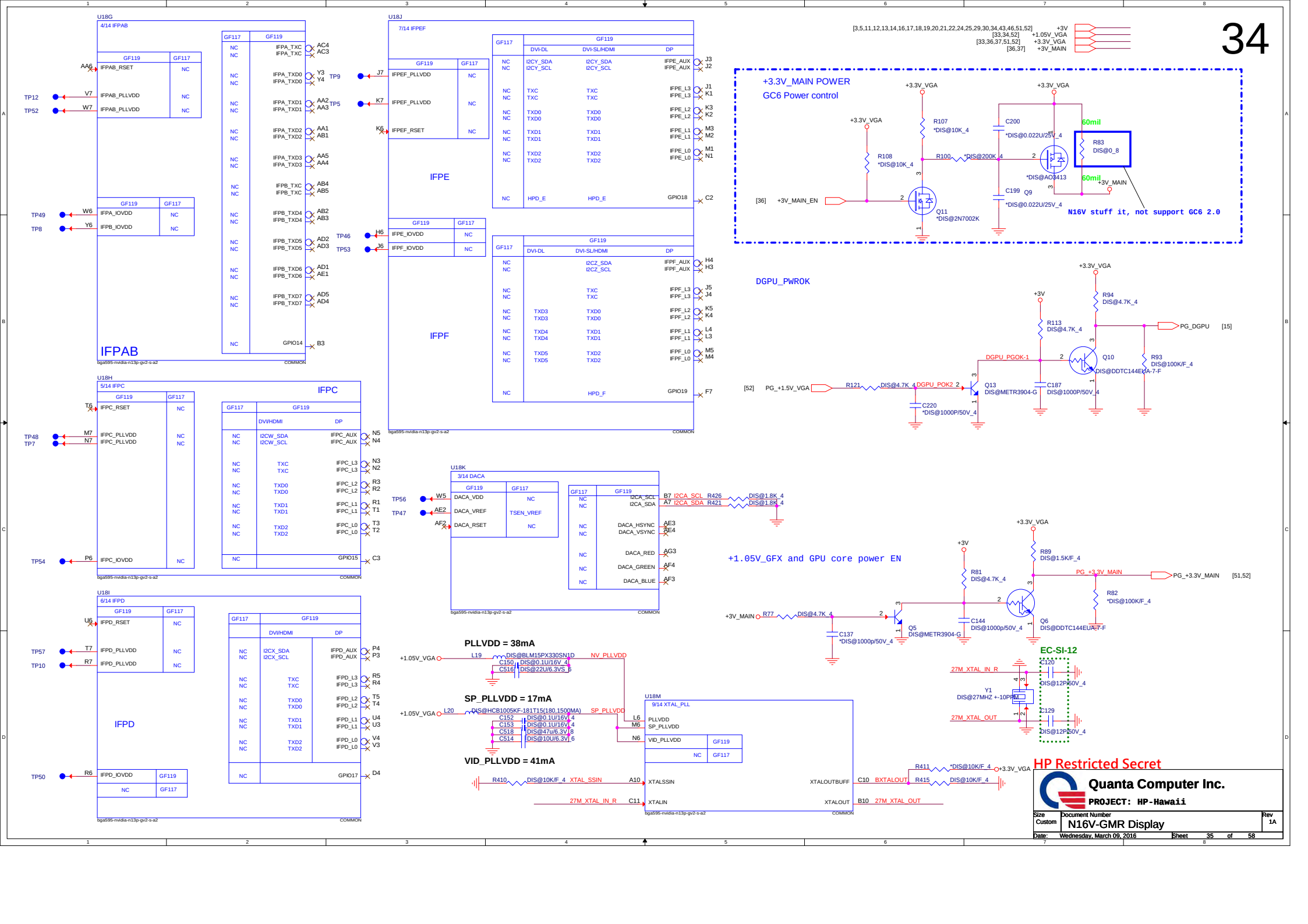
U18G
4/14 IFPAB
IFPAB
U18J
7/14 IFPEF
IFPE
IFPF
U18H
5/14 IFPC
IFPC
U18K
3/14 DACA
U18I
6/14 IFPD
IFPD
U18M
9/14 XTAL_PLL
+3.3V_MAIN POWER
GC6 Power control
N16V stuff it, not support GC6 2.0
DGPU_PWROK
+1.05V_GFX and GPU core power EN
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
EC-SI-12
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
N16V-GMR Display
Size Custom
Rev 1A
Date: Wednesday, March 09, 2016
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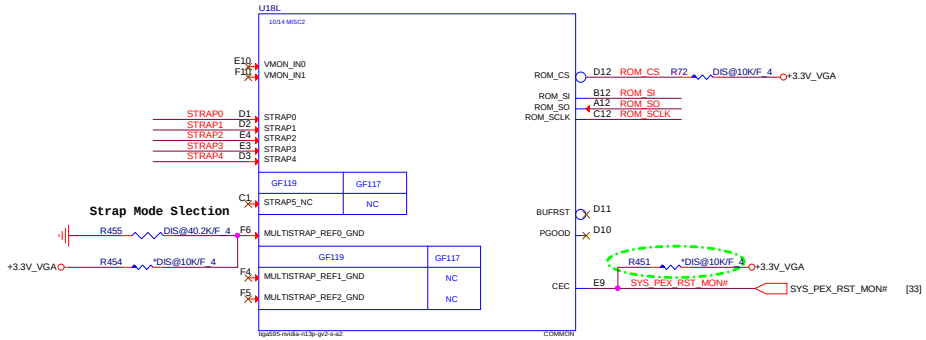


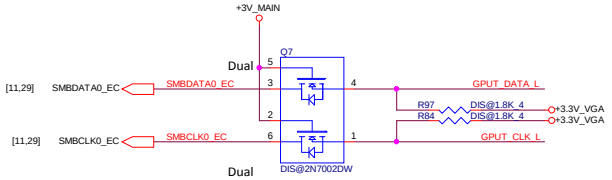


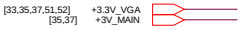


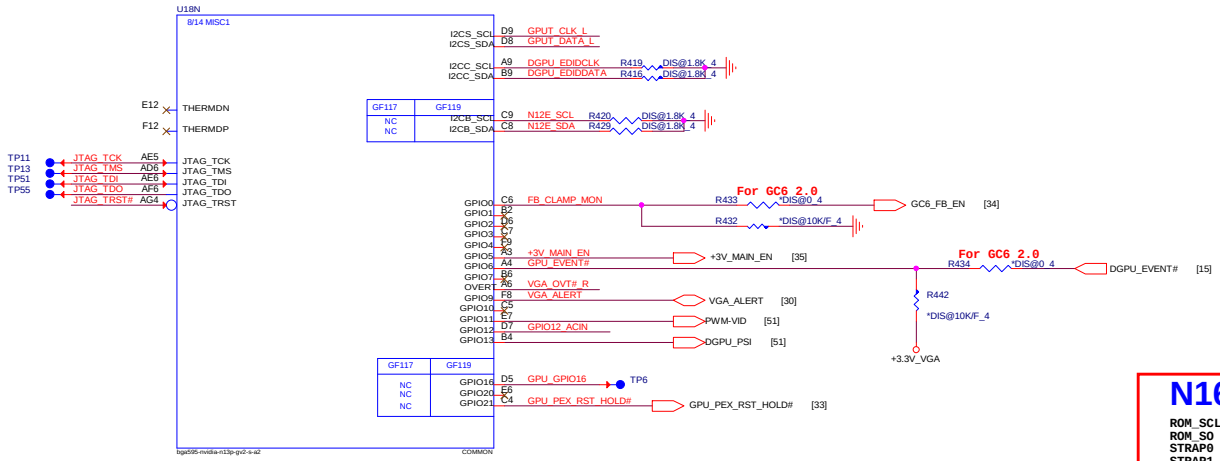


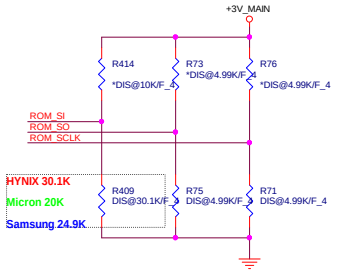


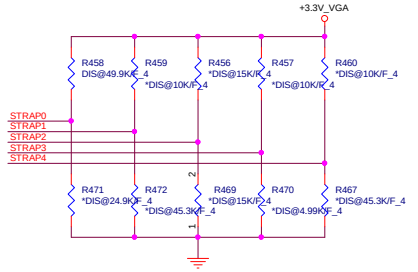


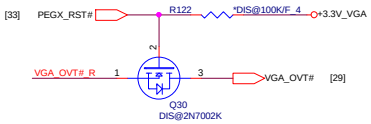


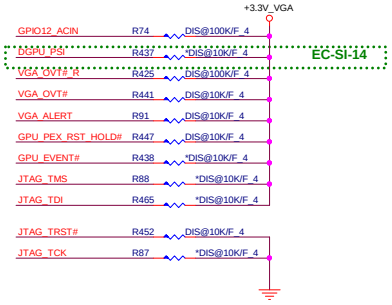


## GPIO ASSIGNMENTS

| GPIO | I/O | PIN | USAGE |
|---|---|---|---|
| 0 | IN | FB_CLAMP_MON | FB Clamp monitor (GC6 1.0) |
| 0 | OUT | GC6_FB_EN | GC6 FB Enable (GC6 2.0) |
| 5 | OUT | +3V_MAIN_EN | Enable GC6 +3V_MAIN |
| 6 | OUT | FB_CLAMP_REQ# | Active low FB Clamp toggle request (GC6 1.0) |
| 6 | IN | DGPU_EVENT# | DGPU EVENT from CPU (GC6 2.0) |
| 8 | OUT | VGA_OVT# | ACTIVE LOW THERMAL OVER TEMP |
| 9 | OUT | ALERT | ACTIVE LOW THERMAL ALERT |
| 11 | OUT | PWR_VID | GPU CORE_VDD PWM Control signal |
| 12 | IN | PWR_LEVEL | AC Power detect or power supply overdraw input |
| 13 | OUT | PSI | Phase Shedding |

## N16V-GMR1 DID=0x134F

GB2B-64

```
ROM_SCLK = Stuff 4.99K pull down
ROM_SO   = Stuff 4.99K pull down
STRAP0   = Stuff 49.9K pull up
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
ROM_SI   = VRAM Configuration follow below table
```

## Logical Strap Bit Mapping

| | PU-VDD | PD | QCI P/N |
|---|---|---|---|
| 4.99K | 1000 | 0000 | CS24992FB26 |
| 10K | 1001 | 0001 | CS31002FB26 |
| 15K | 1010 | 0010 | CS31502FB24 |
| 20K | 1011 | 0011 | CS32002FB29 |
| 24.9K | 1100 | 0100 | CS32492FB16 |
| 30.1K | 1101 | 0101 | CS33012FB18 |
| 34.8K | 1110 | 0110 | CS33482FB06 |
| 45.3K | 1111 | 0111 | CS34532FB18 |

## ROM_SI

| RAMCFG [3:0] | DESCRIPTION 1.5V DDR3 | Vendor | Vendor P/N | ROM_SI | STN B/S | Configuration |
|---|---|---|---|---|---|---|
| | 256Mx16 | | | | | |
| 0011 | DDR3 256Mx16, 64bit, 4Gb,1000MHz | Micron | MT41J256M16LY-091G:N | PD 20K ohm | AKD59GSTL02 | Single Rank or |
| 1001 | DDR3 256Mx16, 64bit, 4Gb,1000MHz | HYNIX | H5TC4G63CFR-N0C | PD 30.1K ohm | AKD5PZDTW03 | Single Rank stuffing |
| 1000 | DDR3 256Mx16, 64bit, 4Gb,1000MHz | Samsung | K4W4G1646E-BC1A | PD 24.9K ohm | AKD5PGDT502 | for Dual Rank |

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| Size | Document Number | Rev |
|---|---|---|
| Custom | N16V-GMR GPIO/Strap | 1A |

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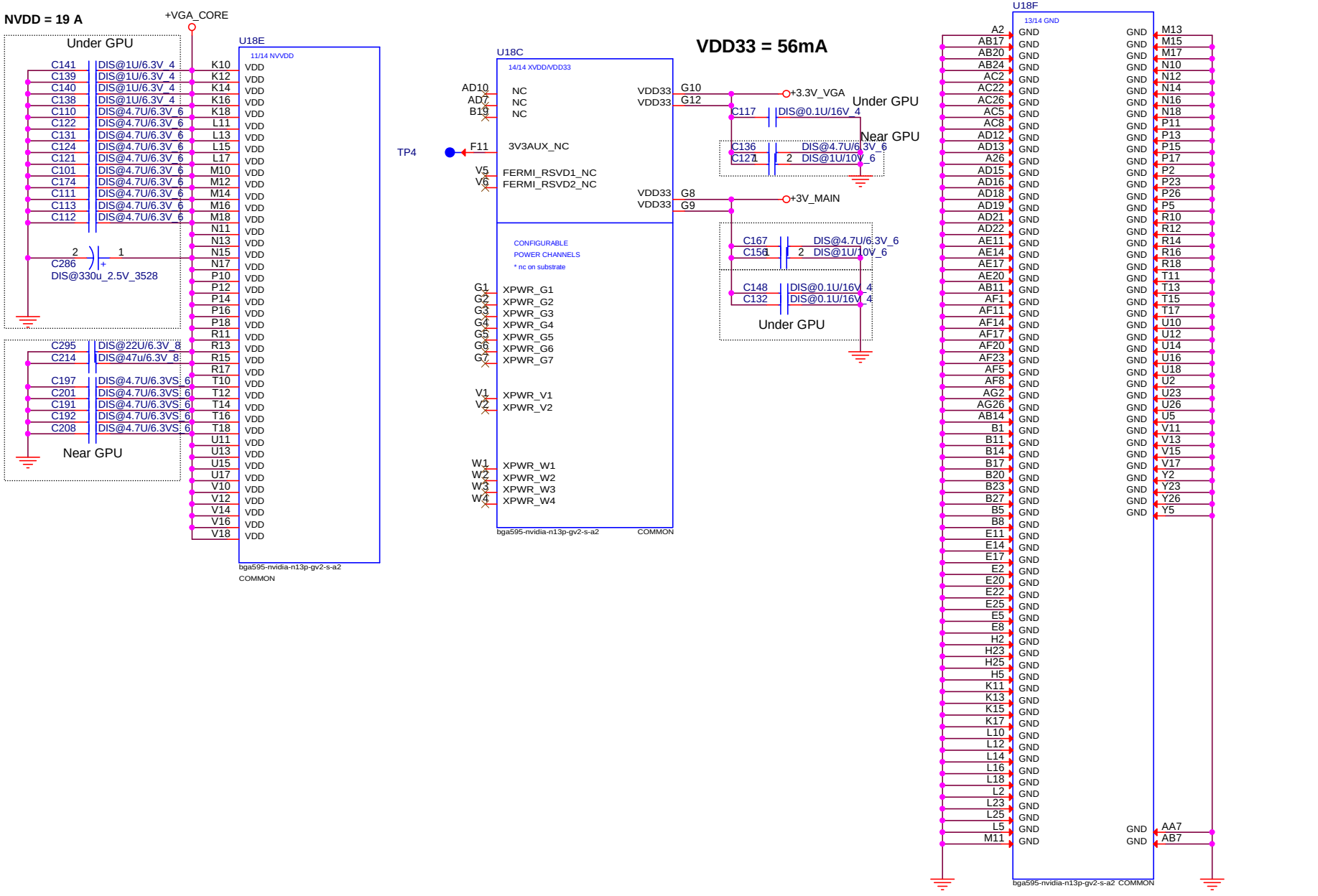


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| Size | Document Number | Rev |
|---|---|---|
| Custom | N16V-GMR Power/GND | 1A |

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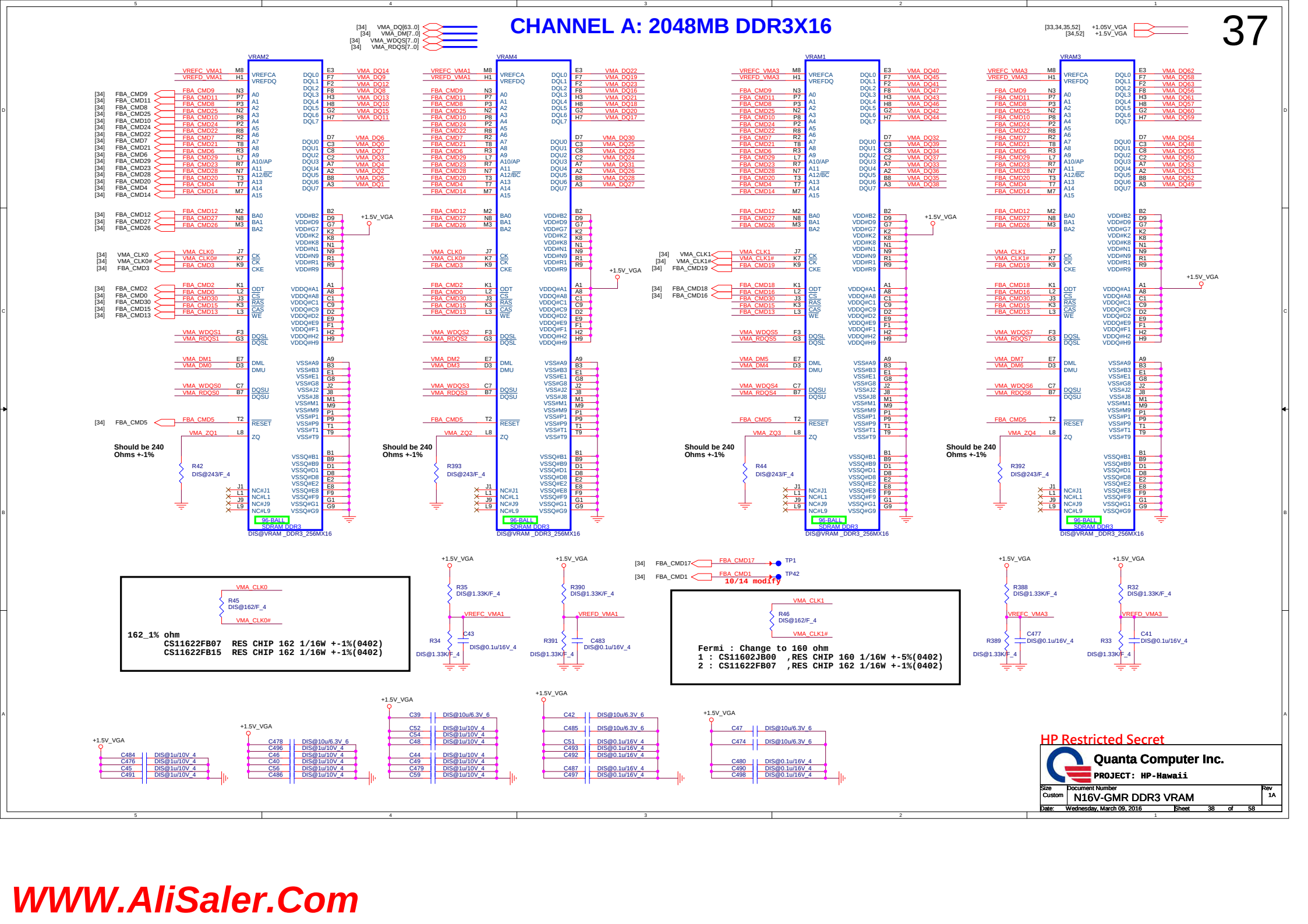
# CHANNEL A: 2048MB DDR3X16



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| Size | Document Number | Rev |
|---|---|---|
| Custom | N16V-GMR DDR3 VRAM | 1A |

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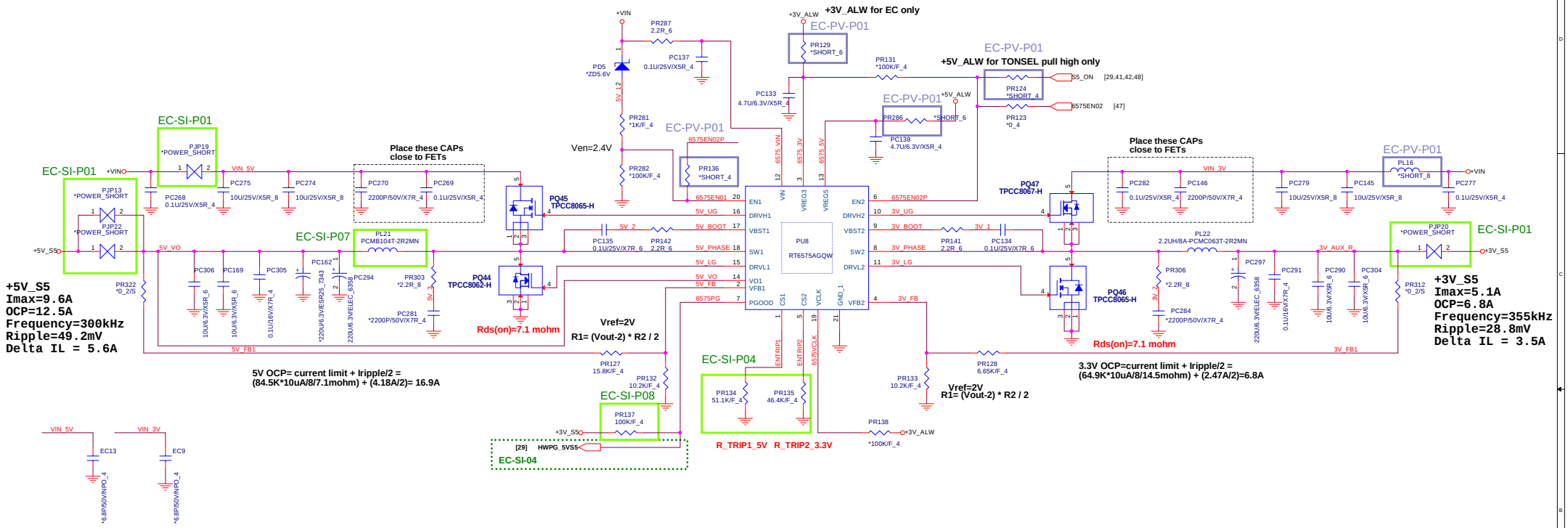


**L/S Mosfet parameter**

| MOSFET | Package | ID (Ta=25C) | Rds_on_max |
|---|---|---|---|
| TPCC8067-H | DFN3x3 | 9A | 26m |
| TPCC8062-H | DFN3x3 | 27A | 7.1m |

**Power On sequencing**

| EN0 | ENC | REF | VREG3 | VREG5 | SMPS1 | SMPS2 |
|---|---|---|---|---|---|---|
| LOW | LOW | OFF | OFF | OFF | OFF | OFF |
| > 2.4V | LOW | ON | ON | ON | OFF | OFF |
| > 2.4V | > 2.4V | ON | ON | ON | ON | ON |

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| Size | Document Number | Rev |
|---|---|---|
| Custom | System +3V_S5/+5V_S5 | 1A |

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+VDDQ [4,7,18,19,32]

**+VDDQ**
**Imax= 9.7A**
**OCP=12.7A**
**Frequency=400kHz**
**Ripple=31.4mV**
**Delta IL = 2.8 A**

## +0.6V_DDR_VTT ( 0.75A )
PEAK :0.75A

[29] 1P2V_PWRGD — PR122 *SHORT_4 — PR119 *SHORT_4 — EC-PV-P01
[28,29,46] SUSON
PR407 10K/F_4 — +3V_S5 — EC-SI-P08
PC126 *0.1U/16V/X7R_4
[18] DDR_VTT_EN
[29,46,48,49] MAINON
PR116 *0_4 — PR117 *SHORT_4
PC125 *0.1U/16V/X7R_4
PR126 120K/F_4
1P2V_S3 1P2V_S5 1P2V_PGOOD 1P2V_CS
1P2V_TON
PR121 620K/F_4

PU7 RT8231BGQW
VTT VTTSNS VTTGND VTTREF VLDOIN
UGATE BOOT1 PHASE LGATE VDD
S3 S5 PGOOD CS TON
LPMB VID PGND FB VDDQ PAD

+0.6V_DDR_VTT — +0.6V_DDR_VTT_R — PR112 *SHORT_6 — PC122 10U/6.3V/X5R_6 — EC-PV-P01
+VTTREF — PR111 100/F_4 — PC121 0.1U/16V/X7R_4 — PC123 0.033U/10V/X7R_4 — PC124 10U/6.3V/X5R_6
+1.2VSUS_S — PR115 *SHORT_6 — 1P2_VLDOIN — EC-PV-P01
PR113 *0_2S — 1P2V_VID
+5V_S5 — PR125 *0_2S — 1P2V_FB
1P2V_VDDQ
R1 PR110 7.68K/F_4
R2 PR114 10K/F_4
VO=(0.675(R1+R2)/R2)

PQ11 TPCA8064-H — PC110 0.1U/25V/X5R_4 — PC106 4.7U/25V/X5R_8 — PC262 4.7U/25V/X5R_8 — PC109 2200P/50V/X7R_4 — PC104 0.1U/25V/X5R_4
+VIN_DDR — PL5 *SHORT_8 — +VIN — EC-PV-P01
PQ13 TPCA8059-H — EC-SI-P09
PC131 1U/6.3V/X5R_4
PR120 2.2/J_6 — PC129 0.1U/25V/X5R_4
PL7 1UH/11A(PCMC063T-1R0MN)
PR280 *2.2/J_6 — PC263 *2200P/50V/X7R_4
+1.2VSUS_S — PR90 *0_2S — PC91 0.1U/16V/X7R_4 — PC95 22U/6.3V/X5R_6 — PC103 390U/2.5V/ELEC_6358
PJP5 *POWER_SHORT — PJP4 *POWER_SHORT — EC-SI-P01 — +VDDQ

+VIN_DDR — EC6 *6.8P/50V/NPO_4
1P2V_VID — SRV1 *BC5123ZOZ01_6
1P2V_VDD — SRV2 *BC5123ZOZ01_6

## +2.5V_S3 +/- 5%
**Imax = 1A**
**OCP = 3A**
**Pd: 0.8W**
**Ripple=10mV**

+3V_S5 — PR103 10K_4 — PR102 *SHORT_4 — 1P2V_PWRGD — EC-PV-P01
+5V_S5 — PC107 1U/6.3V/X5R_4
PU5 G9661-25ADJF12U
VPP PGOOD VEN VO VIN GND GND ADJ NC
+2.5V_VIN — +2.5V_EN — +3V_S5 — PR105 *SHORT_6 — EC-PV-P01
PC115 10U/6.3V/X5R_6 — PC114 0.1U/16V/X7R_4
+2.5V_PG — +2.5V_S3_P
FB_+2.5V — PR91 *0_2S
+2.5V_ADJ
R1 PR92 21.5K/F_4
R2 PR93 10K/F_4
Vout =0.8(1+R1/R2)
PJP6 *POWER_SHORT — +2.5V_S3 — EC-SI-P01
PC94 0.1U/16V/X7R_4 — PC96 10U/6.3V/X5R_6 — PC97 10U/6.3V/X5R_6

[29] EN_+2.5V_S3 — SUSON — PR106 *0_4 — EN_+2.5V_S3 — PR107 *SHORT_4 — +2.5V_EN — PC113 1U/10V/X5R_4 — EC-PV-P01

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| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR4 +VDDQ/+2.5V_S3 | 1A |
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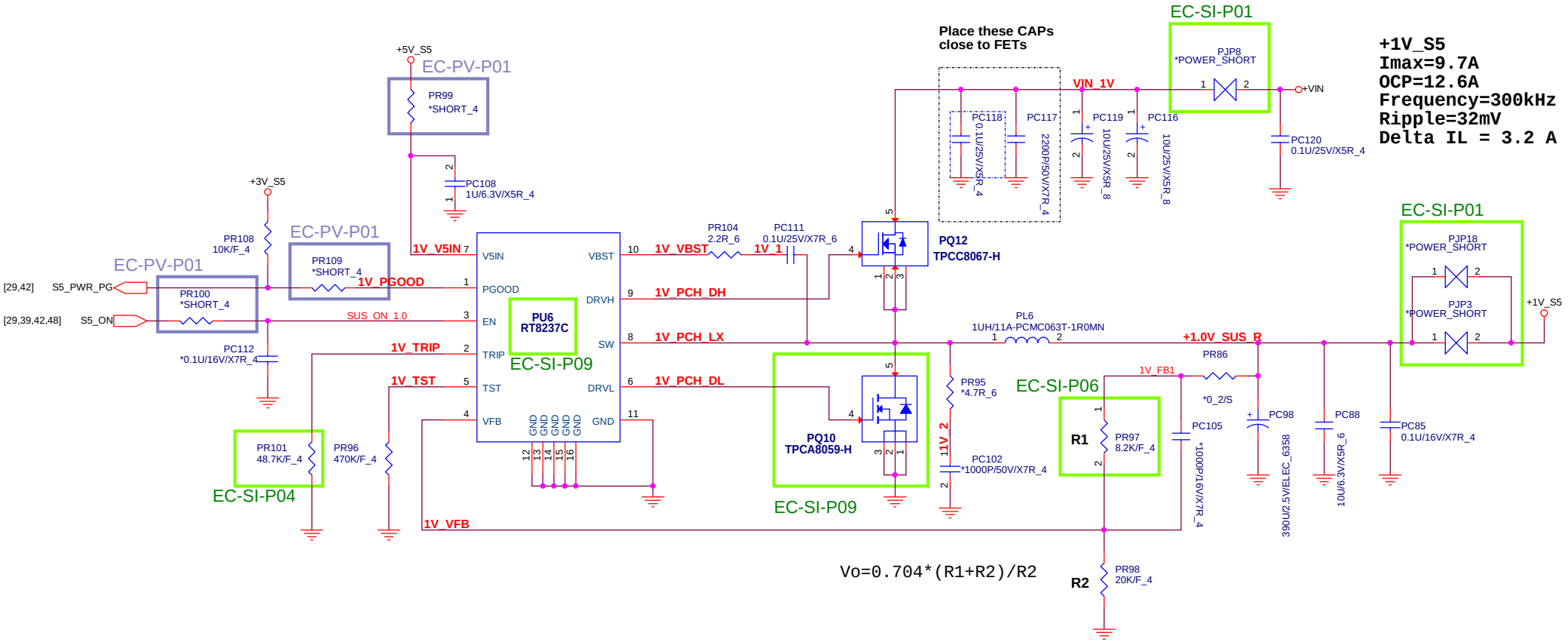




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| Size | Document Number | Rev |
|---|---|---|
| B | +1V_S5 | 1A |

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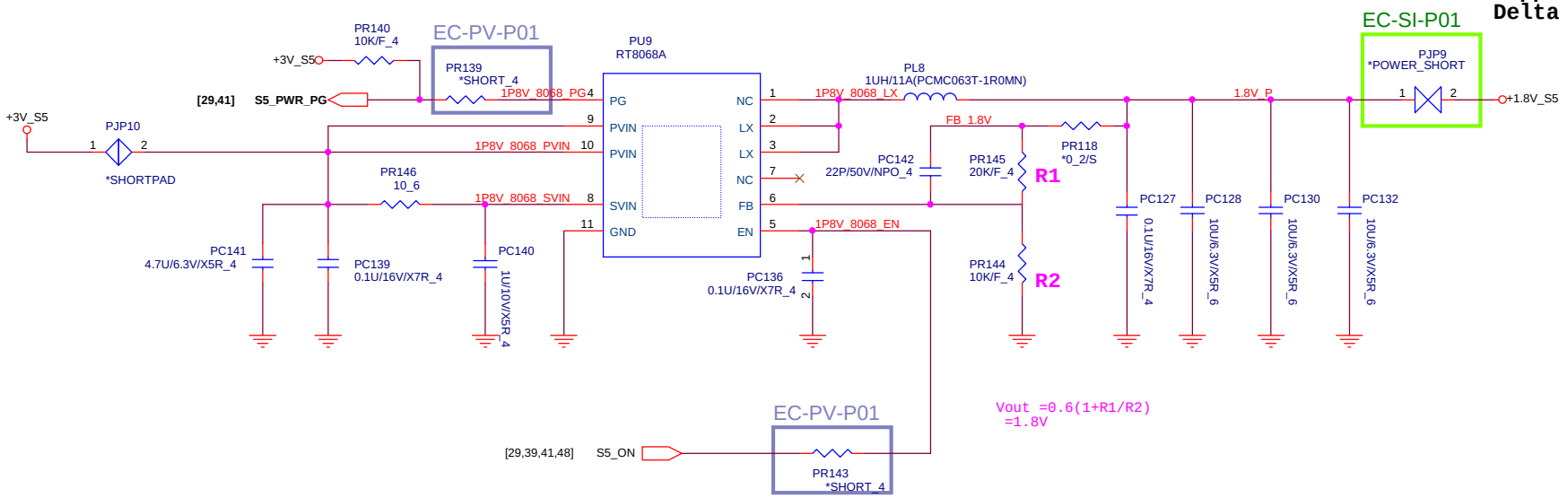
# V1P8A (RT8068A)



**+1.8V_S5**
**Imax=1.2A**
**OCP=4A**
**Frequency=1MHz**
**Ripple=12mV**
**Delta IL = 0.8A**

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| Size | Document Number | Rev |
|---|---|---|
| B | +1.8V_S5 | 1A |

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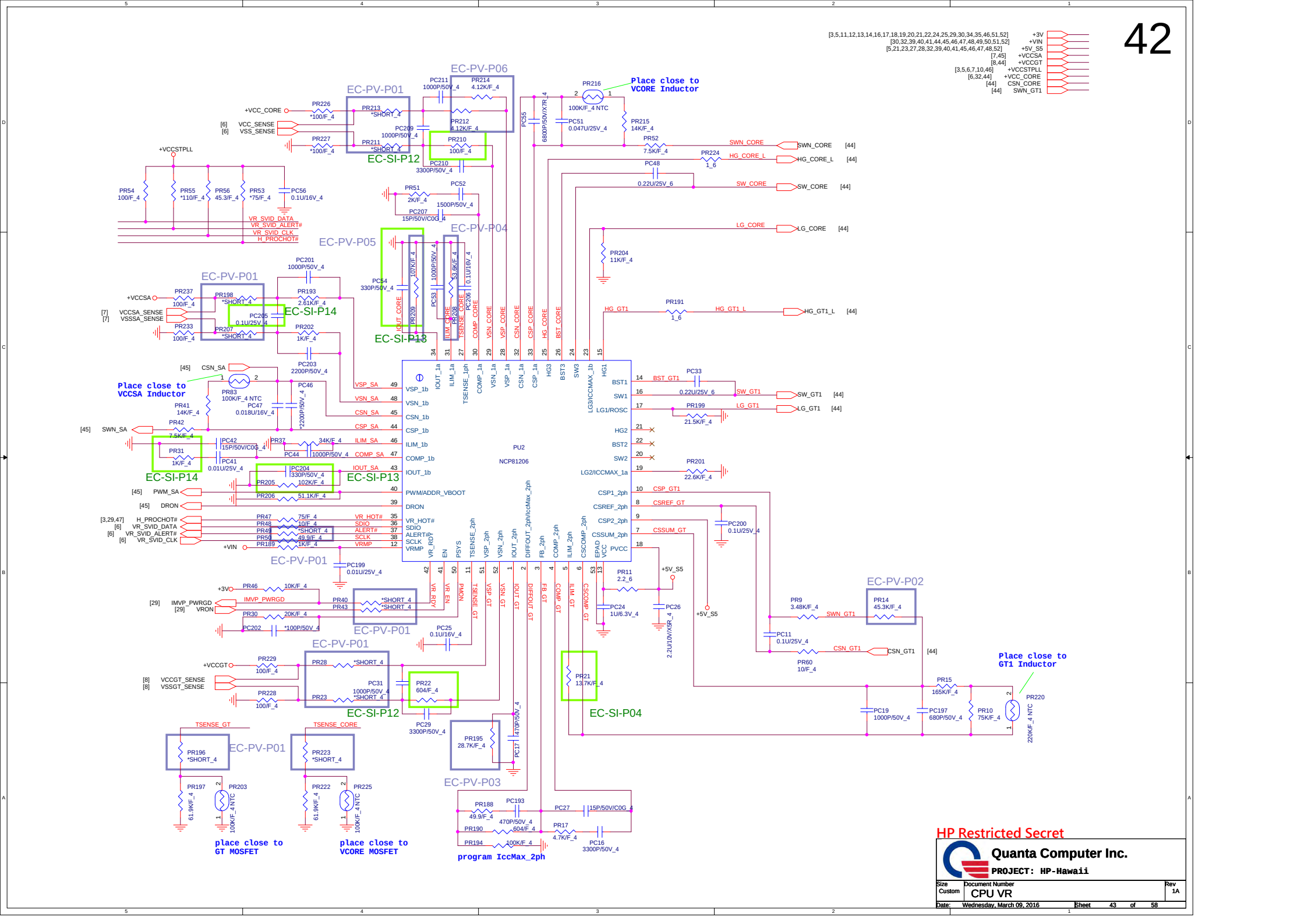


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PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | CPU VR | 1A |

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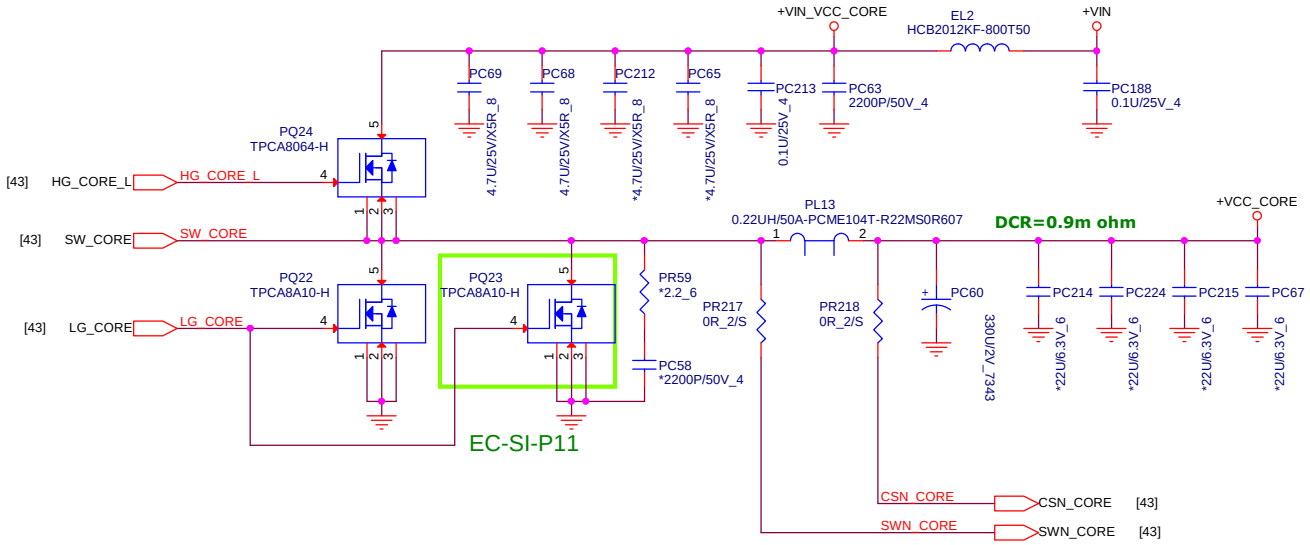
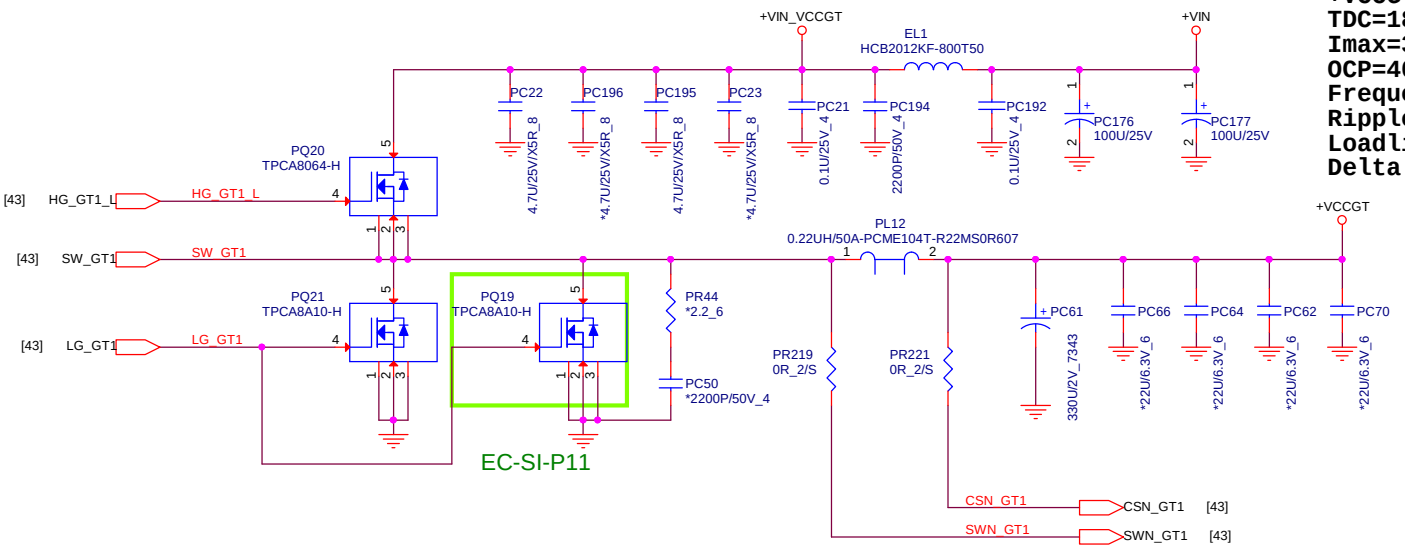
**+VCC_CORE**
**TDC=21A**
**Imax=29A**
**OCP=36A**
**Frequency=450kHz**
**Ripple=13mV**
**Loadline: -2.4m ohm**
**Delta IL = 9.6A**




**+VCCGT**
**TDC=18A**
**Imax=31A**
**OCP=40A**
**Frequency=450kHz**
**Ripple=13mV**
**Loadline: -3.1m ohm**
**Delta IL = 9.6A**

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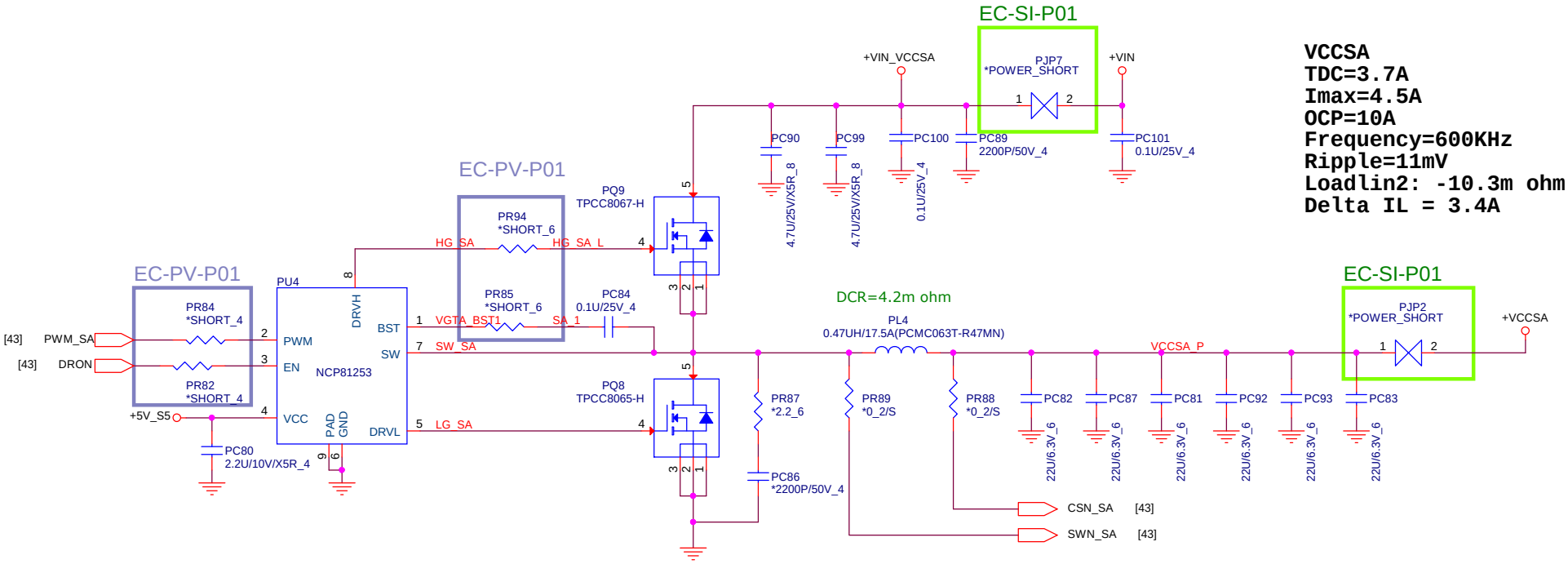
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| B | CPU +VCC_CORE/+VCCGT | 1A |

Date: Wednesday, March 09, 2016 Sheet 44 of 58

[30,32,39,40,41,43,44,46,47,48,49,50,51,52] +VIN
[5,21,23,27,28,32,39,40,41,43,46,47,48,52] +5V_S5
[7,43] +VCCSA

# VCCSA




**VCCSA**
**TDC=3.7A**
**Imax=4.5A**
**OCP=10A**
**Frequency=600KHz**
**Ripple=11mV**
**Loadlin2: -10.3m ohm**
**Delta IL = 3.4A**

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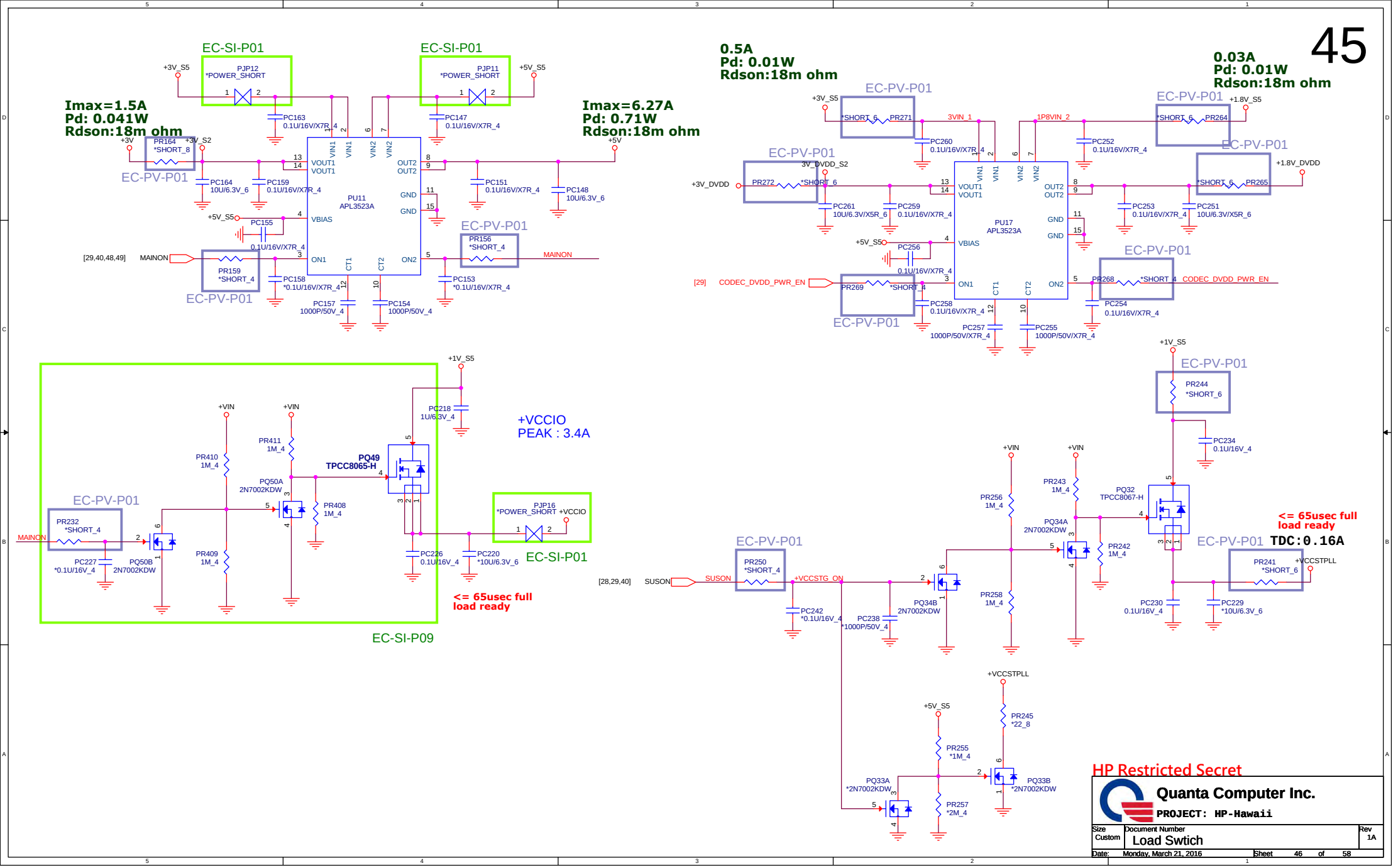
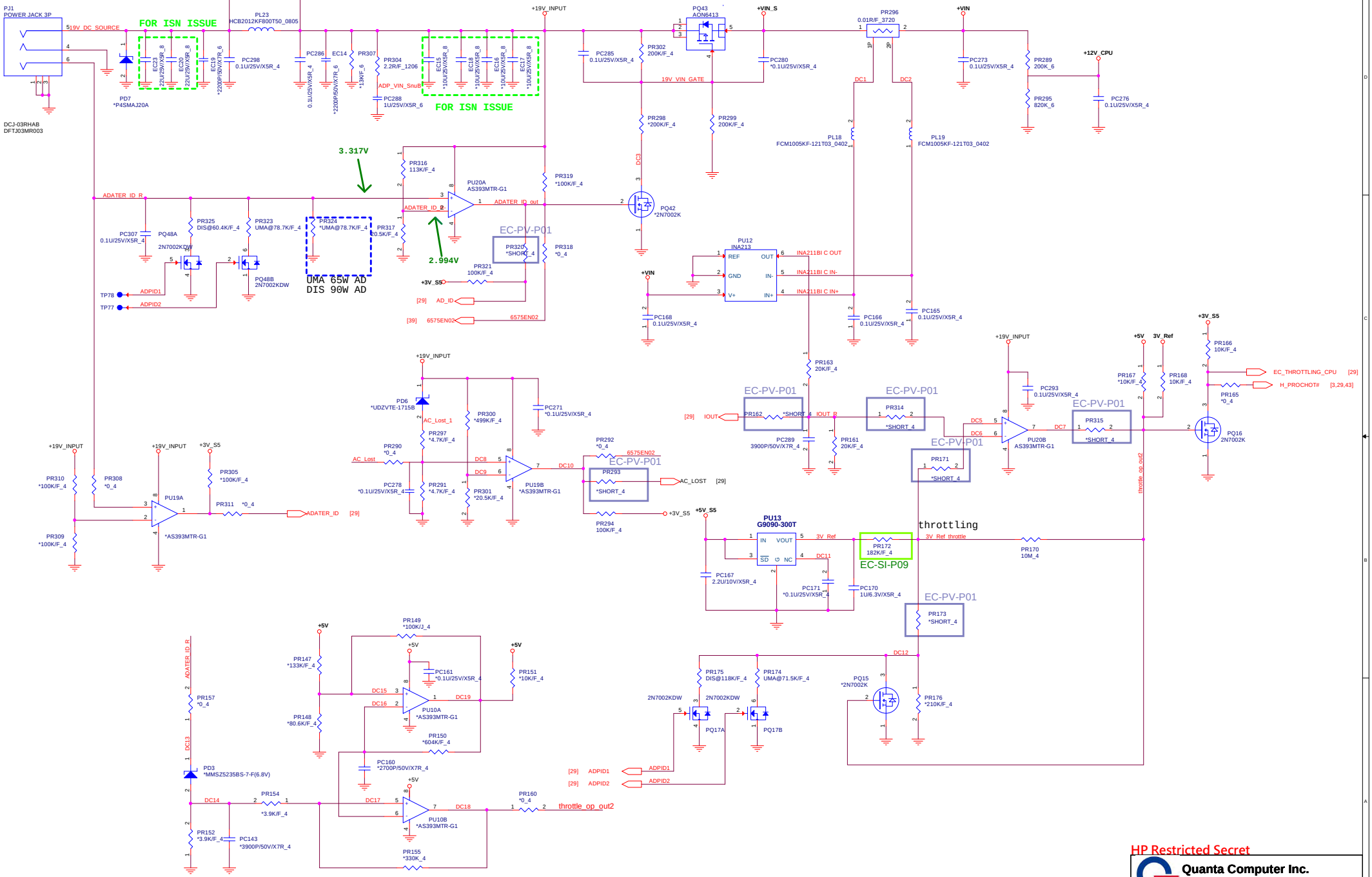
**PROJECT: HP-Hawaii**

| Size | Document Number | Rev |
|---|---|---|
| Custom | CPU +VCCSA | 1A |
| Date: Wednesday, March 09, 2016 | Sheet 45 of 58 | |



Id=16A
Qg=41~58nC
Rdson=6.9~8.5mOHM

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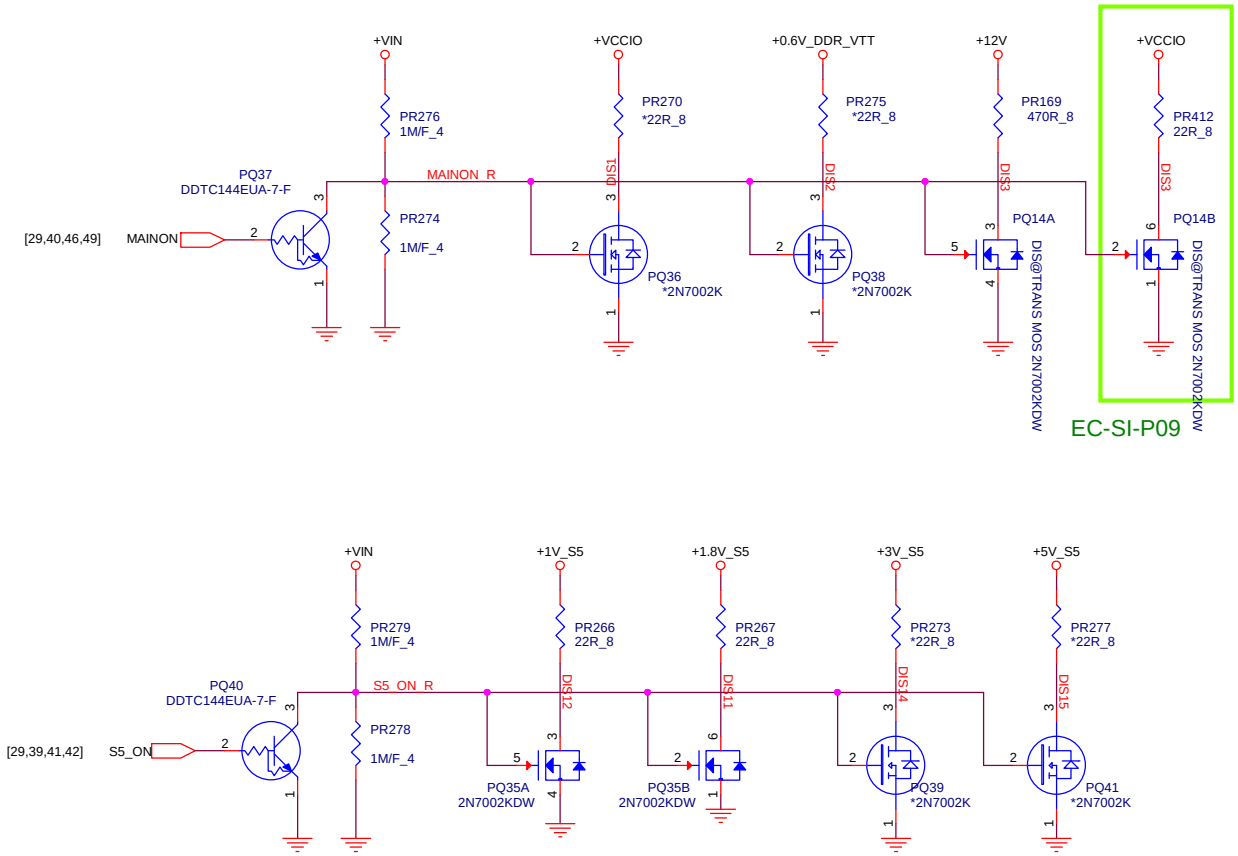
| Size | Document Number | Rev |
|---|---|---|
| Custom | DC IN | 1A |
| Date: Wednesday, March 09, 2016 | Sheet 47 of 56 | |

CONFIDENTIAL

# DISCHARGE









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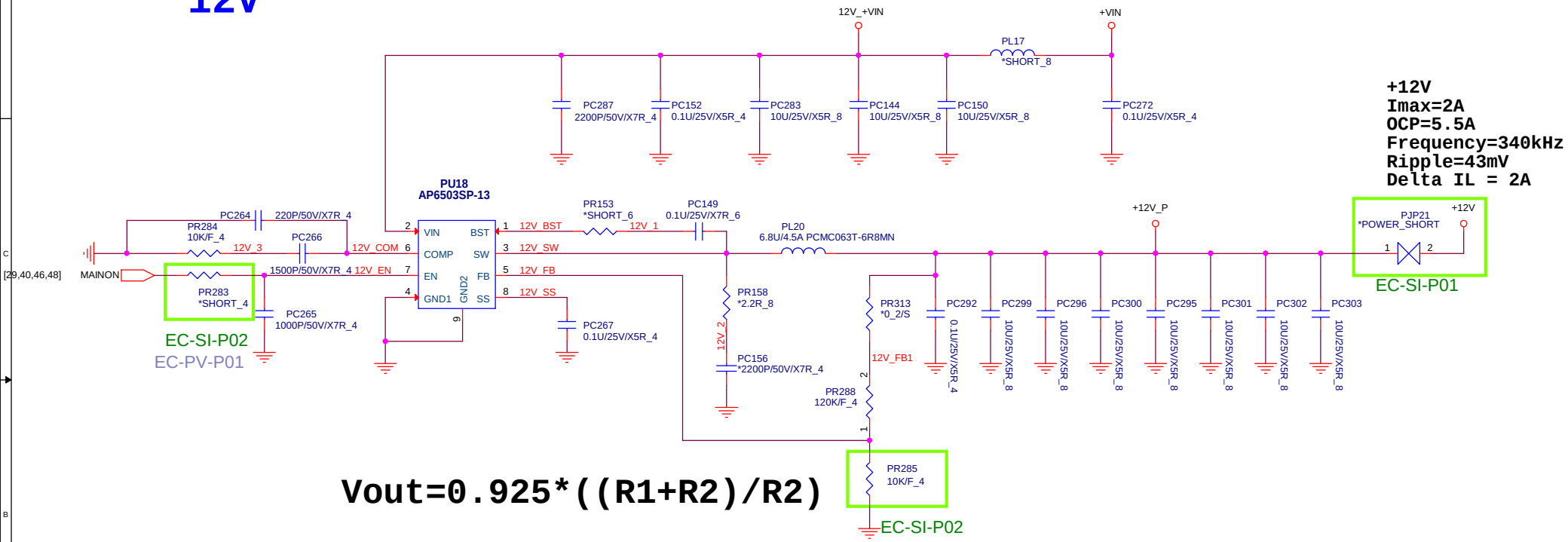
| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT: HP-Hawaii | | |
| Size: B | Document Number: Discharge | Rev: 1A |
| Date: Wednesday, March 09, 2016 | Sheet 48 of 58 | |

# 12V




**+12V**
**Imax=2A**
**OCP=5.5A**
**Frequency=340kHz**
**Ripple=43mV**
**Delta IL = 2A**

**Vout=0.925*((R1+R2)/R2)**

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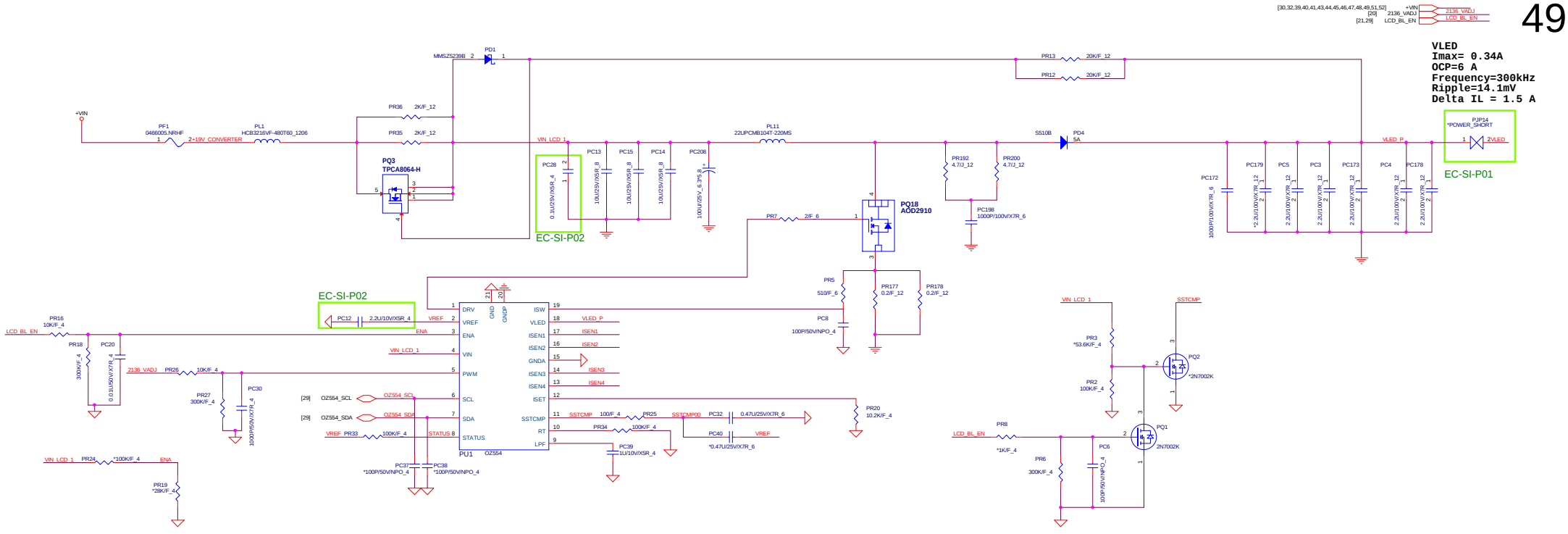
| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT: HP-Hawaii | | |
| Size: B | Document Number: +12V | Rev: 1A |
| Date: Wednesday, March 09, 2016 | Sheet 49 of 58 | |




**PANEL_SIZE Table**

| PANEL_Size[1:0] | Size |
|---|---|
| 00 | 19.5/9.53" |
| 01 | 21.5" |
| 10 | 23.6"/23.8" |
| 11 | Reserve |

**19.45" /19.53" PANEL_ID Table**

| PANEL_ID[3:0] | Panel model |
|---|---|
| 1111 | No Connect |
| 1110 | INX M200HJJ-L20 FHD |
| 1101 | AUO M195RTN01.0 HD+ |
| 1100 | LGD LM195WD1-TLA1 HD+ |
| 1010 | Reserve |

**21.5" PANEL_ID Table**

| PANEL_ID[3:0] | Panel model |
|---|---|
| 1111 | No Connect |
| 1110 | INX M215HJK-L3B FHD eDP |
| 1101 | SDC LTM215HL01 FHD |
| 1100 | LGD LM215WF3-SLN1 FHD |
| 1011 | Reserve |

**23.6" /23.8" PANEL_ID Table**

| PANEL_ID[3:0] | Panel model |
|---|---|
| 1111 | No Connect |
| 1110 | INX M236HJK-L5B FHD eDP |
| 1101 | AUO M238HAN01.0 FHD |
| 1100 | LGD LM238WF1-SLE1 FHD |
| 1011 | SDC LTM238HL02 FHD |
| 1010 | Reserve |

Panel_ID[3:0] = 1111 & Panel_Size[1:0] = 11 is reserved for cabling detection by "No connection".



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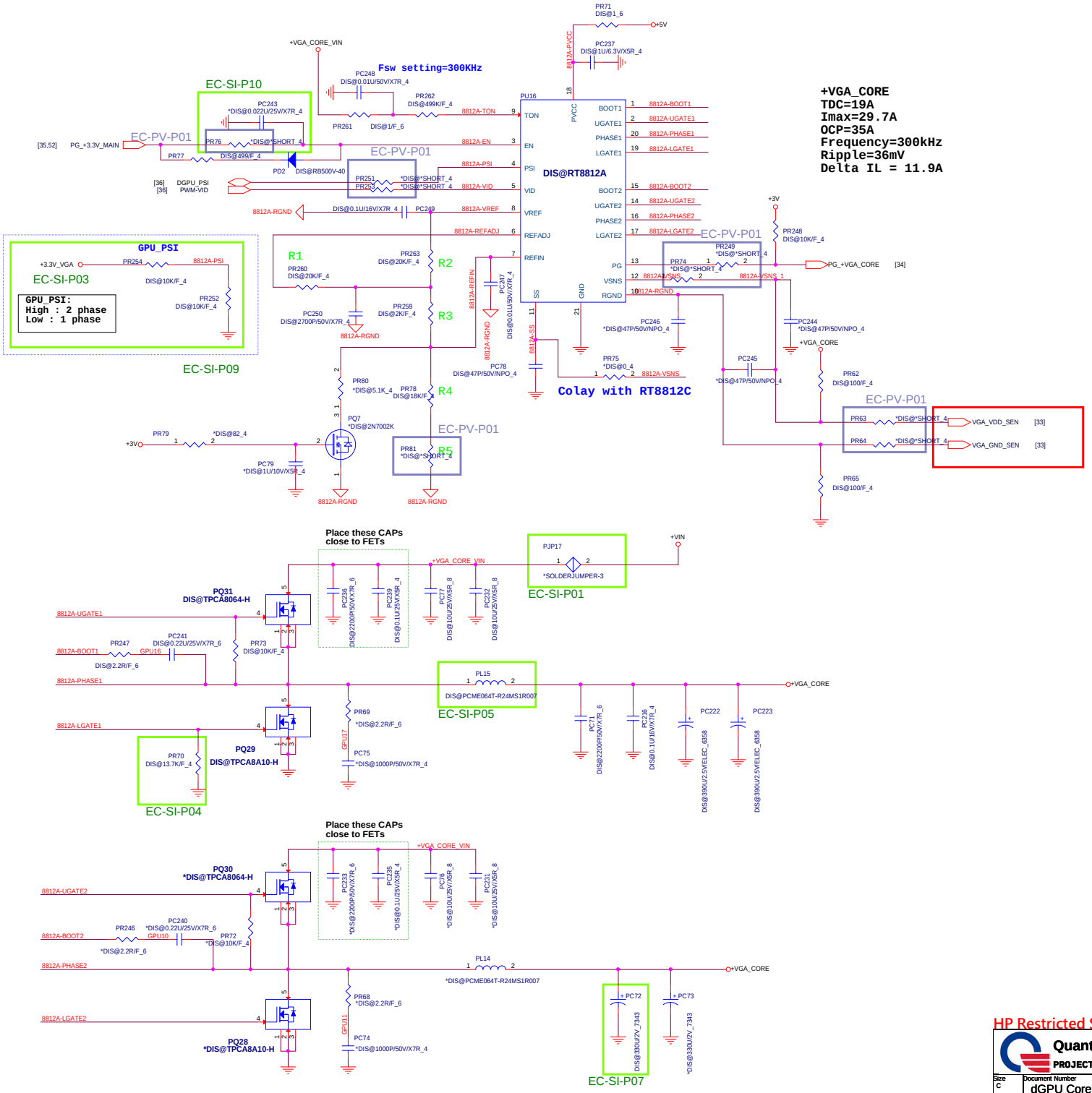
Size: Custom | Document Number: OZ554 | Rev: 1A
Date: Thursday, March 17, 2016 | Sheet 50 of 58

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PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| C | dGPU Core | 1A |

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# VGA POWER

51

AO6402A
Rdson=24m ohm
Imax=0.2A
Pd: 0.01W

+1.05V_VGA
Imax=1.5A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL = 0.8A

+1.5V_VGA
Imax=4.7A
OCP=8A
Frequency=500KHz
Ripple=22mV
Delta IL = 2.8A

## +1.05V VGA

40mil

V0=0.6*(R1+R2)/R2

VREF=0.604V

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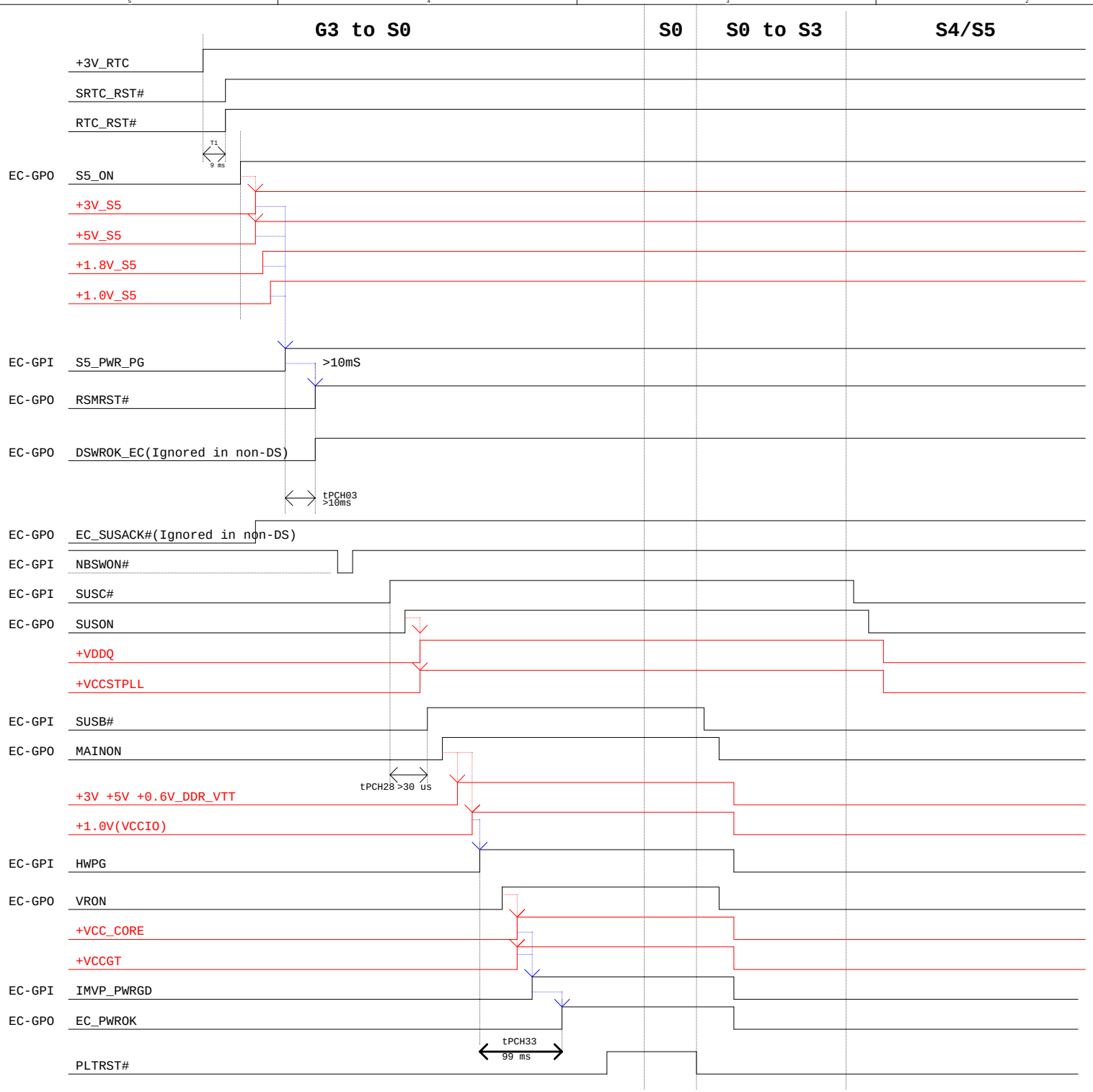
PROJECT: HP-Hawaii

Size: Custom | Document Number: dGPU +1.05V/+1.5V | Rev: 1A
Date: Wednesday, March 09, 2016 | Sheet 52 of 58

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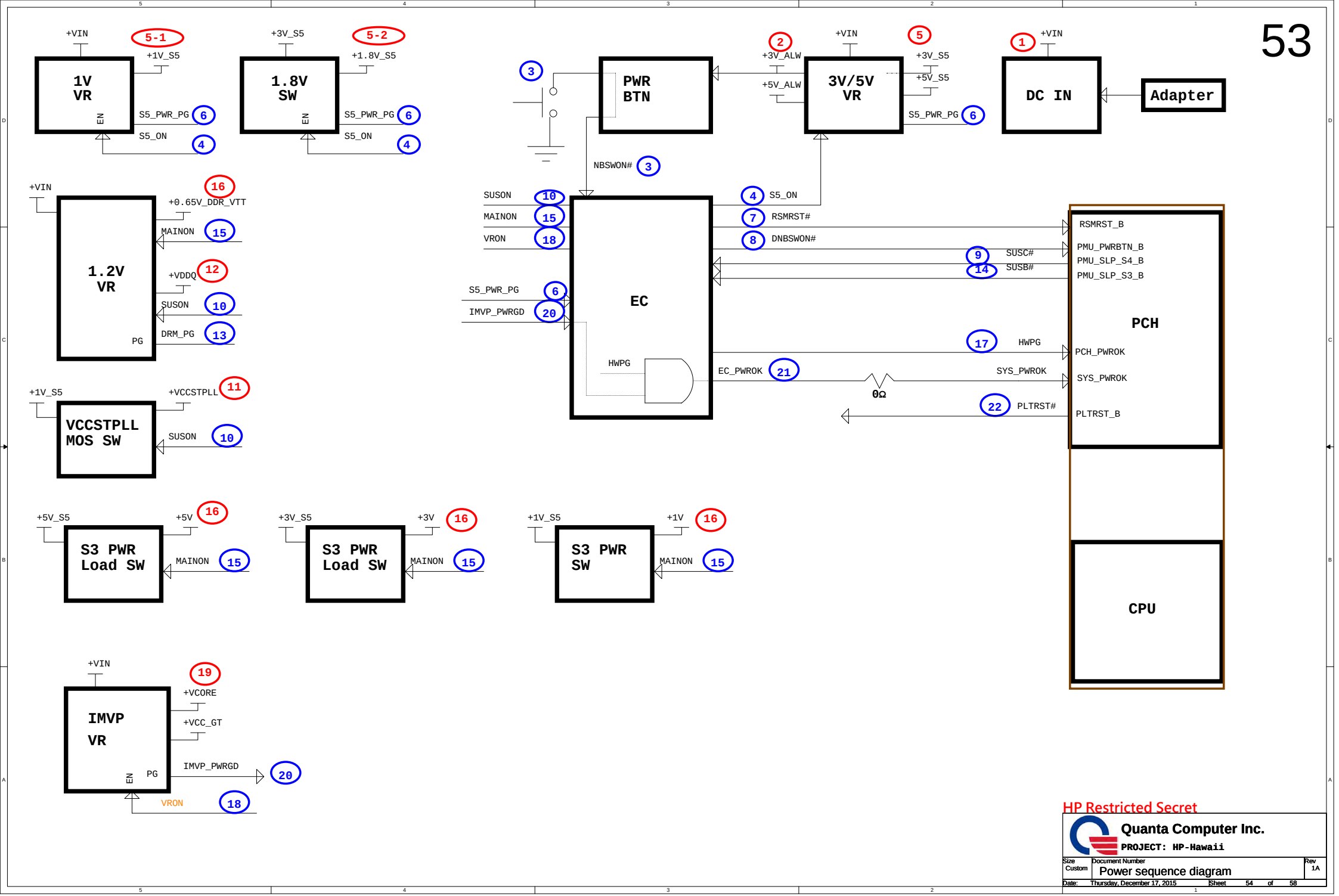
PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| C | Power Sequence | 1A |

Date: Thursday, December 17, 2015 Sheet 53 of 58

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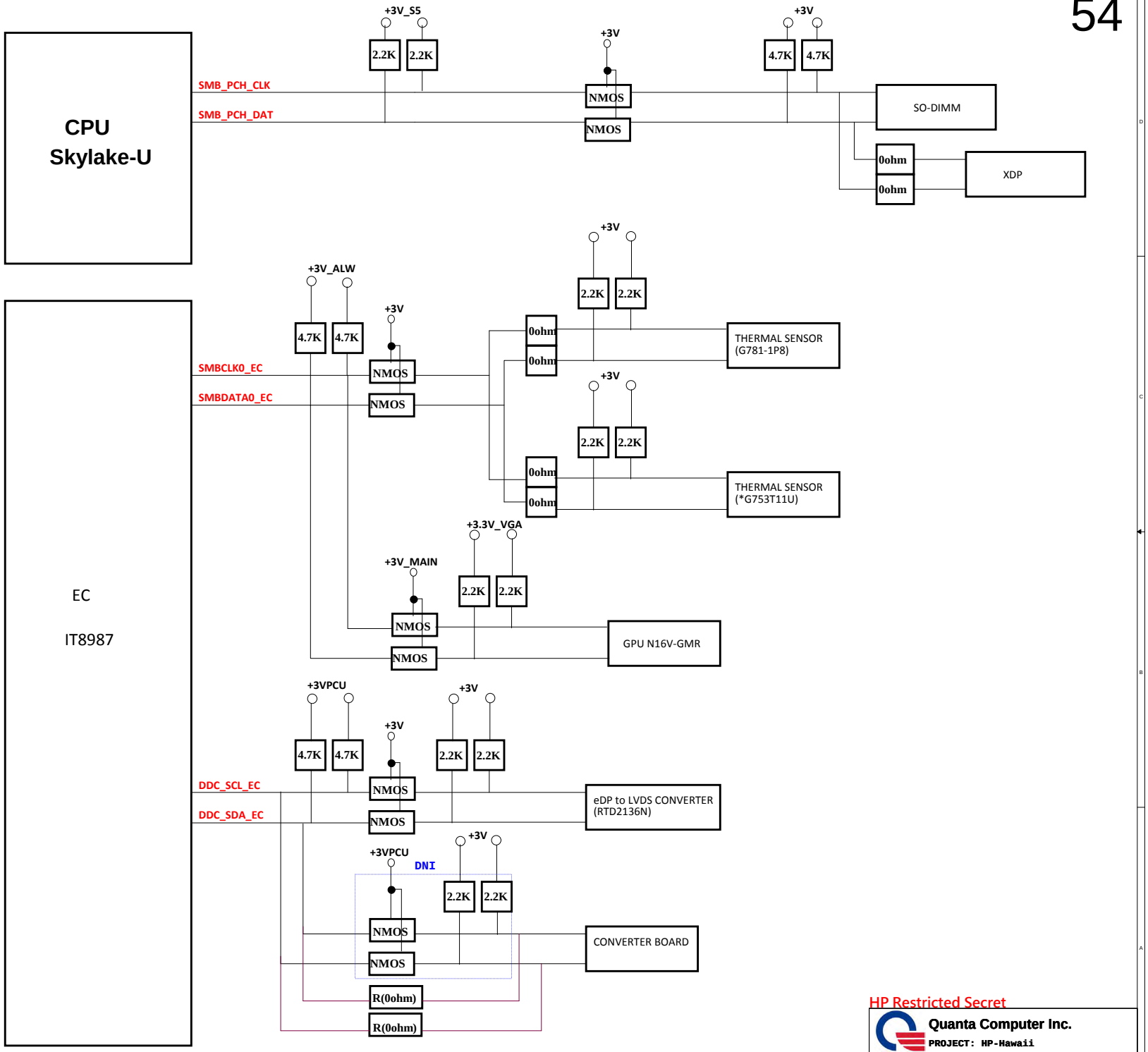
Quanta Computer Inc.

PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| Custom | Power sequence diagram | 1A |

Date: Thursday, December 17, 2015 Sheet 54 of 58

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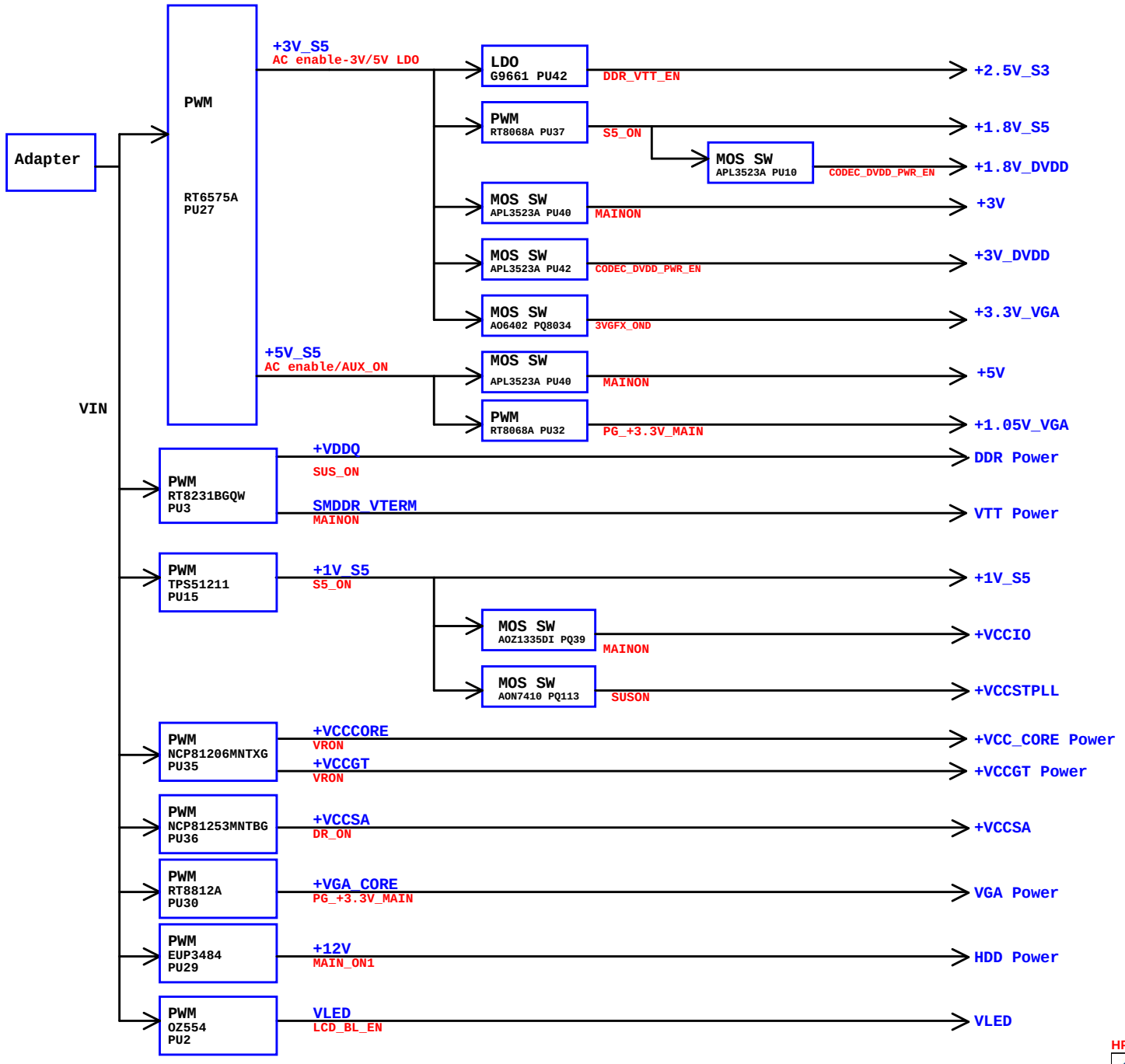
| Size | Document Number | Rev |
|---|---|---|
| Custom | SMBUS map | 1A |

Date: Thursday, December 17, 2015 Sheet 55 of 58

# Power Delivery Map



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PROJECT: HP-Hawaii

| Size | Document Number | Rev |
|---|---|---|
| C | Power Delivery Map | 1A |

Date: Thursday, January 28, 2016 Sheet 56 of 58

## N91 EE Schematic DB to SI Change List

| EC# | Page | Description | Part Affected |
|---|---|---|---|
| EC-SI-01 | 17,18 | Unstuff C205/C213 for DDR4 Issue | C205,C213 |
| EC-SI-02 | 21 | Change HDMI HPD signal from low active to high active | Q38,R638,R639 |
| EC-SI-03 | 21 | Modify Q37 MOSFET gate power source from +5V to +3V | Q37 |
| EC-SI-04 | 28 | Swap EC GPIO for reserving 2nd fan control | |
| EC-SI-05 | 22 | Separate L/R channels for spkeaker connector | CN26,CN27 |
| EC-SI-06 | 20 | Add ESD protection for CCD | |
| EC-SI-07 | 29 | Reserve 2nd FAN | |
| EC-SI-08 | 49 | Reserve 100pF for CN15 (EMI suggestion) | |
| EC-SI-09 | 31 | Add 2 GND pad for EMI | |
| EC-SI-10 | 25 | Change ODD connector | CN21 |
| EC-SI-11 | 26 | Change connector of card reader daughter board | CN24 |
| EC-SI-12 | 13,34 | Change load cap for 32.768K/24M/27M due to vendor suggest | |
| EC-SI-13 | All | Stuff EMC/ESD/RF materials | |
| EC-SI-14 | 35 | Unstuff R437 for correct PSI setting | R437 |
| EC-SI-15 | 22 | Change AL7/AL8/AL9/AL11 as 0ohm from Realtek suggest | AL7,AL8,AL9,AL11 |

## N91 EE Schematic SI to PV Change List

| EC# | Page | Description | Part Affected |
|---|---|---|---|
| EC-PV-01 | All | Change 0ohm resistor to be short pad | |
| EC-PV-02 | 27 | Remove reserved CMC of USB3.0 | L28,L29,L30,L33 |

## N91 Power Schematic DB to SI Change List

| EC# | Page | Description | Part Affected |
|---|---|---|---|
| EC-SI-P01 | 38~51 | Change default open to default short | PJP1~PJP22 |
| EC-SI-P02 | 48,49,51 | Downsize components | PR283, PR285, PC12, PC28, PC184, PC185, PC174, PL3 |
| EC-SI-P03 | 50, 51 | Correct connection | |
| EC-SI-P04 | 38,40,42,50 | Fine tune OCP function | PR134, PR135, PR101, PR21, PR70 |
| EC-SI-P05 | 50 | Change choke for transient | PL15 |
| EC-SI-P06 | 40,51 | Fine tune offset voltage | PR97, PR186 |
| EC-SI-P07 | 38, 50 | Change components for ripple voltage | PL21, PC72 |
| EC-SI-P08 | 38,39 | Add components for PG function | PR137, PR122 |
| EC-SI-P09 | 39,40,45~47,50,51 | Change components for common part using | PU6, PQ10, PQ13, PQ14, PQ49, PQ50, PR408~PR412, PR254, PR252, PQ4, PQ5, PQ26, PR172 |
| EC-SI-P10 | 50 | Fine tune soft start | PR76, PC243 |
| EC-SI-P11 | 43 | Add components for Efficiency | PQ19, PQ23 |
| EC-SI-P12 | 42 | Fine tune DVID setting | PR210, PR22 |
| EC-SI-P13 | 42 | Fine tune Iout function | PR205, PR209, PC54, PC204 |
| EC-SI-P14 | 42 | Fine tune compensation | PR31, PC205 |

## N91 EE Schematic SI to PV Change List

| EC# | Page | Description | Part Affected |
|---|---|---|---|
| EC-PV-P01 | All | Change 0ohm resistor to short pad | |
| EC-PV-P02 | 42 | Fine tune +VCCGT load line | PR14 |
| EC-PV-P03 | 42 | Fine tune +VCCGT Iout function | PR195 |
| EC-PV-P04 | 42 | Fine tune Vcore OCP | PR208 |
| EC-PV-P05 | 42 | Fine tune Vcore Iout function | PR209 |
| EC-PV-P06 | 42 | Fine tune Vcore Loadline | PR212,PR214 |