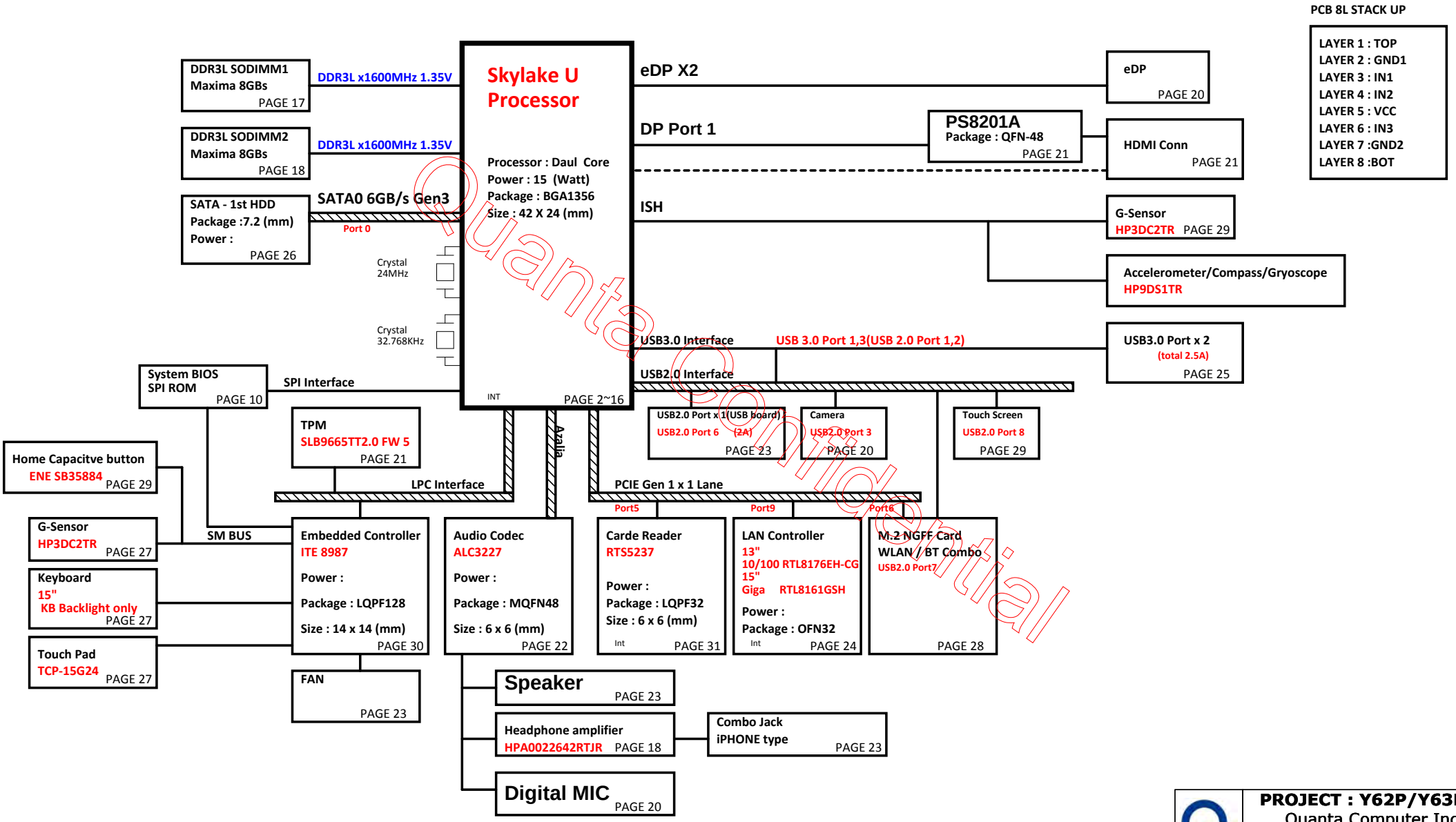
13"/15"
Intel Skylake ULT Platform Block Diagram



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Wednesday, May 20, 2015 Sheet 1 of 42

+3V 4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+1.0V 4,6,16,30,36
+VCCIO 6,16,36
+VCCSTPLL 4,5,6,9,36,37

HDMI

21 IN_D2# → E55 DDI1_TXN[0]
21 IN_D2 → F55 DDI1_TXP[0]
21 IN_D1# → E58 DDI1_TXN[1]
21 IN_D1 → F58 DDI1_TXP[1]
21 IN_D0# → G53 DDI1_TXN[2]
21 IN_D0 → F56 DDI1_TXP[2]
21 IN_CLK# → G56 DDI1_TXN[3]
21 IN_CLK → DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

U17A SKL_ULT ? **Need apply PN**

DDI → EDP

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 20
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 20
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 20
EDP_TXP[1] C45 INT_EDP_TXP1 → INT_EDP_TXP1 20
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN 20
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP 20

EDP_DISP_UTIL B52 → TP107

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E13/DDPB_HPD0 L9 HDMI_HPD_CON → HDMI_HPD_CON 21
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 ULT_EDP_HPD → ULT_EDP_HPD 20

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON 20
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM 20
EDP_VDDEN U13 PCH_DISP_ON → PCH_DISP_ON 20

DISPLAY SIDEBANDS

21 SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
21 SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

TP23 DDPC_CTRLDATA → N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA

TP21 DDPD_CTRLDATA → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO R220 24.9/F_4 EDP_RCOMP → E52 EDP_RCOMP

SKL_ULT
REV = 1
1 OF 20
?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R30 10K_4
ULT_EDP_HPD
R51 100K_4

U17D SKL_ULT ? **Need apply PN**

CPU MISC

30,32,37 H_PROCHOT# → R463 499/F_4 30 EC_PECI
30 PM_THRMTRIP#

TP117 CATERR# → D63 CATERR#
EC_PECI → A54 PECI
PROCHOT# → C65 PROCHOT#
PM_THRMTRIP# → C63 THERMTRIP#
A65 SKTOCC#

16 XDP_BPM0 → C55 BPM#[0]
16 XDP_BPM1 → D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

TP94 CPU_GP0 → A6 GPP_E3/CPU_GP0
TP92 CPU_GP1 → A7 GPP_E7/CPU_GP1
TP55 CPU_GP2 → BA5 GPP_B3/CPU_GP2
TP56 CPU_GP3 → AY5 GPP_B4/CPU_GP3

R109 49.9/F_4 PROC_POPIRCOMP → AT16 PROC_POPIRCOMP
R108 49.9/F_4 PCH_OPI_RCOMP → AU16 PCH_OPIRCOMP
R273 49.9/F_4 EDRAM_OPIO_RCOMP → H66 OPCE_RCOMP
R272 49.9/F_4 EOPIO_RCOMP → H65 OPC_RCOMP

JTAG

PROC_TCK B61 XDP_TCK0 → XDP_TCK0 16
PROC_TDI D60 XDP_TDI_CPU → XDP_TDI_CPU 16
PROC_TDO A61 XDP_TDO_CPU → XDP_TDO_CPU 16
PROC_TMS C60 XDP_TMS_CPU → XDP_TMS_CPU 16
PROC_TRST# B59 XDP_TRST#_CPU → XDP_TRST#_CPU 2,16

PCH_JTAG_TCK B56 JTAG_TCK_PCH → JTAG_TCK_PCH 16
PCH_JTAG_TDI D59 JTAG_TDI_PCH → JTAG_TDI_PCH 16
PCH_JTAG_TDO A56 JTAG_TDO_PCH → JTAG_TDO_PCH 16
PCH_JTAG_TMS C59 JTAG_TMS_PCH → JTAG_TMS_PCH 16
PCH_TRST# C61 XDP_TRST#_CPU → XDP_TRST#_CPU 2,16
JTAGX A59 JTAGX_PCH → JTAGX_PCH 16

SKL_ULT
REV = 1
4 OF 20

+VCCSTPLL
R470 *49.9/F_4 CATERR#

+1.0V
R335 0_4
R326 *51_4 JTAGX_PCH
R322 51_4 JTAG_TMS_PCH
R329 51_4 JTAG_TDI_PCH
R327 51_4 JTAG_TDO_PCH
R328 51_4 JTAG_TCK_PCH

Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R469 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R336 *51_4
XDP_TDI_CPU R323 *51_4
XDP_TDO_CPU R324 *51_4

+1.0V
H_PROCHOT# R471 1K_4
XDP_TCK0 R325 51_4
XDP_TRST#_CPU R331 51_4

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/20(eDP/DDI)	1A
Date: Wednesday, May 20, 2015	Sheet 2 of 42	

SkyLake ULT Processor (DDR3L)

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.35VSUS 6,17,18,34,36

Need apply PN

U17B — SKL_ULT — 2 OF 20

U17C — SKL_ULT — 3 OF 20

Need apply PN

NIL-DDR CH - A

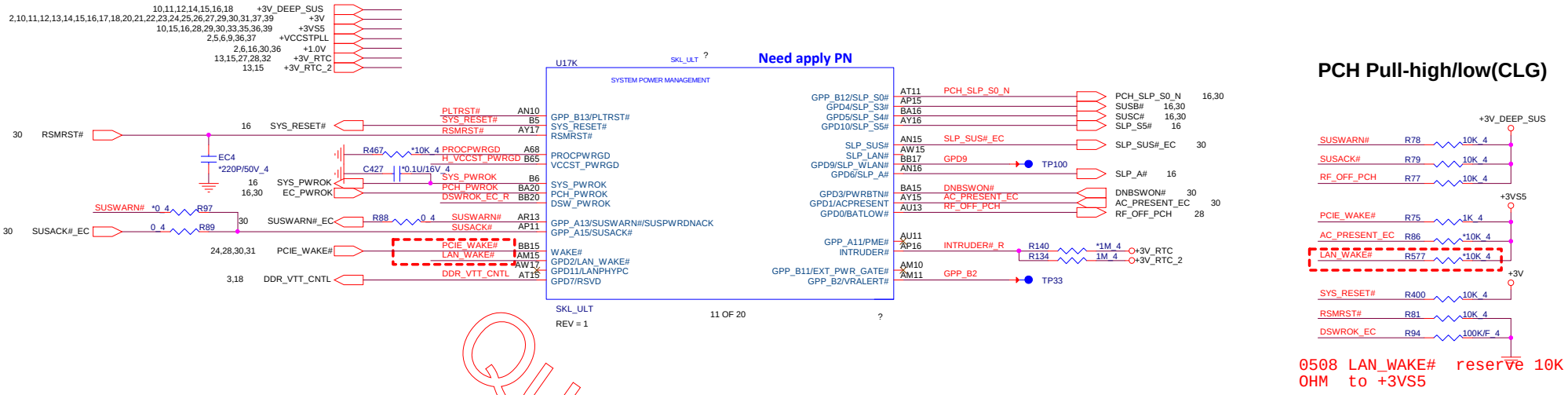
NIL-DDR CH - B

20mils width

SKL_ULT REV = 1

PROJECT : Y62P/Y63P
Quanta Computer Inc.

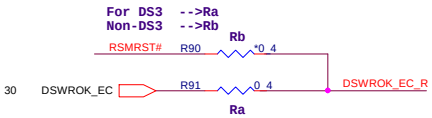
Size	Document Number	Rev
Custom	03 -- SKYPAKE 3/20(DDR3-A I/F)	1A
Date: Wednesday, May 20, 2015	Sheet 3 of 42	



PCH Pull-high/low(CLG)

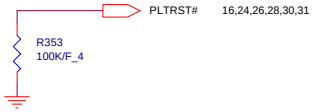
0508 LAN_WAKE# reserve 10K OHM to +3VS5

For DS3 Sequence

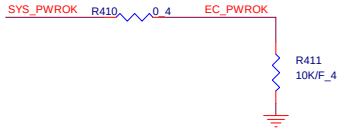


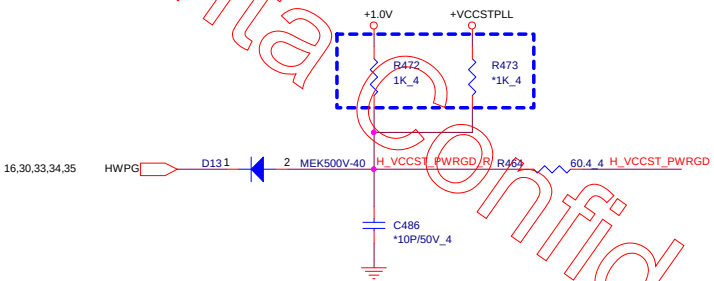
PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns

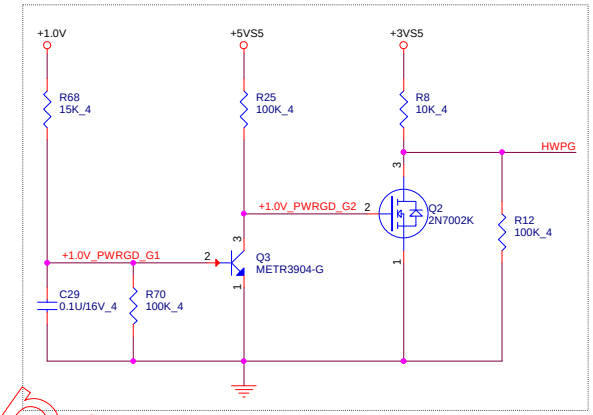


System PWR_OK(CLG)



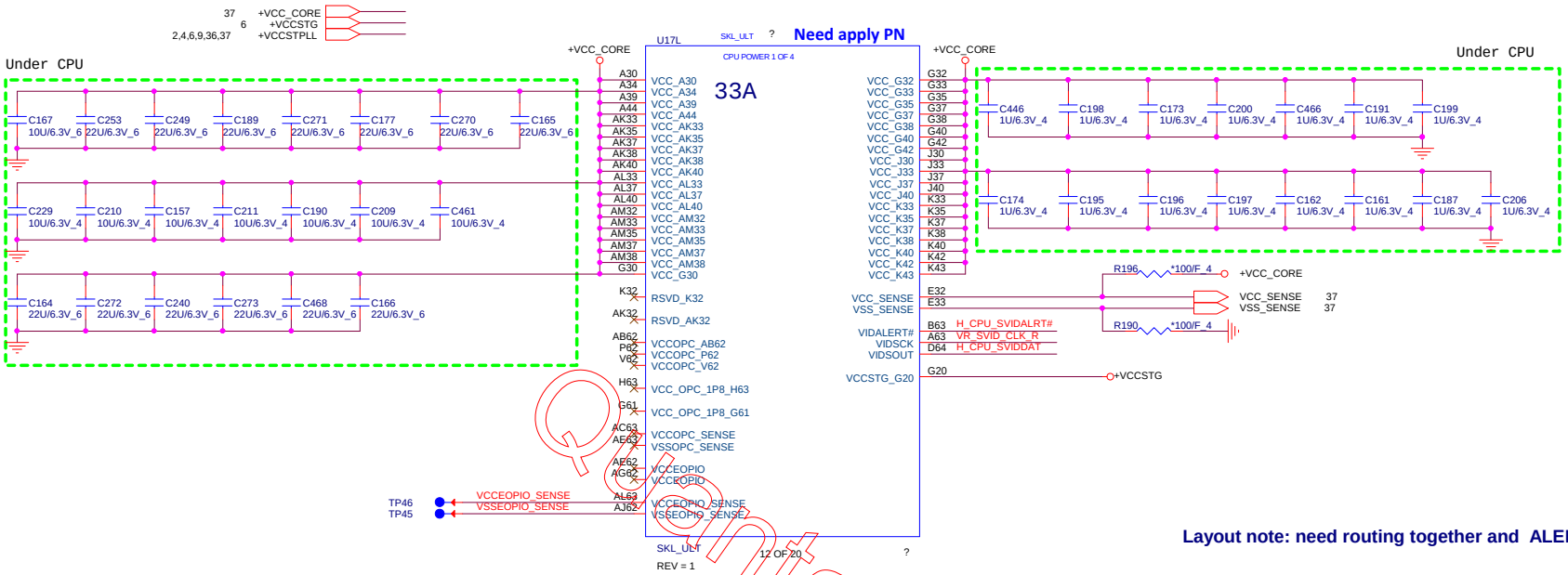


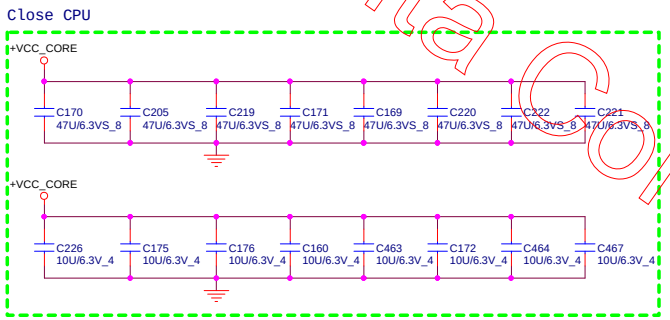
Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



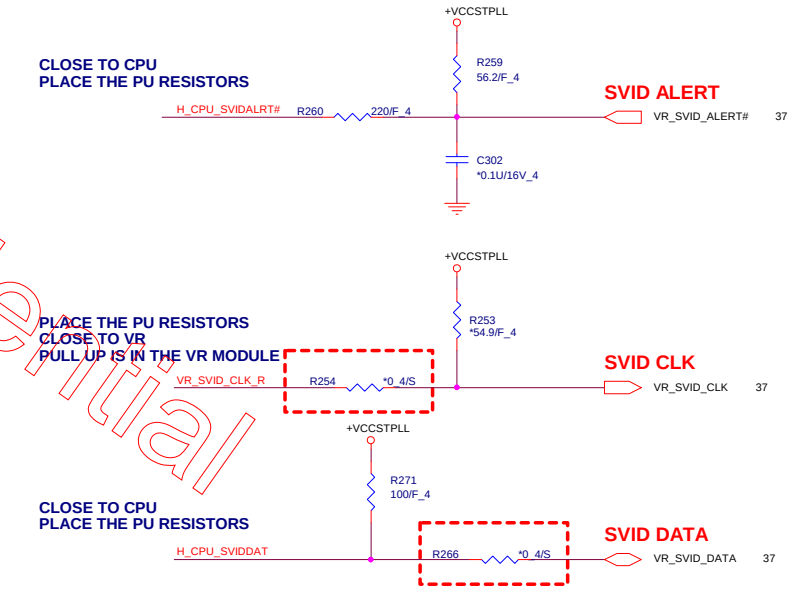
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 -- SKYPAKE 5/20(Power Manger)	1A
Date: Wednesday, May 20, 2015	Sheet 4 of 42	





Layout note: need routing together and ALERT need between CLK and DATA.

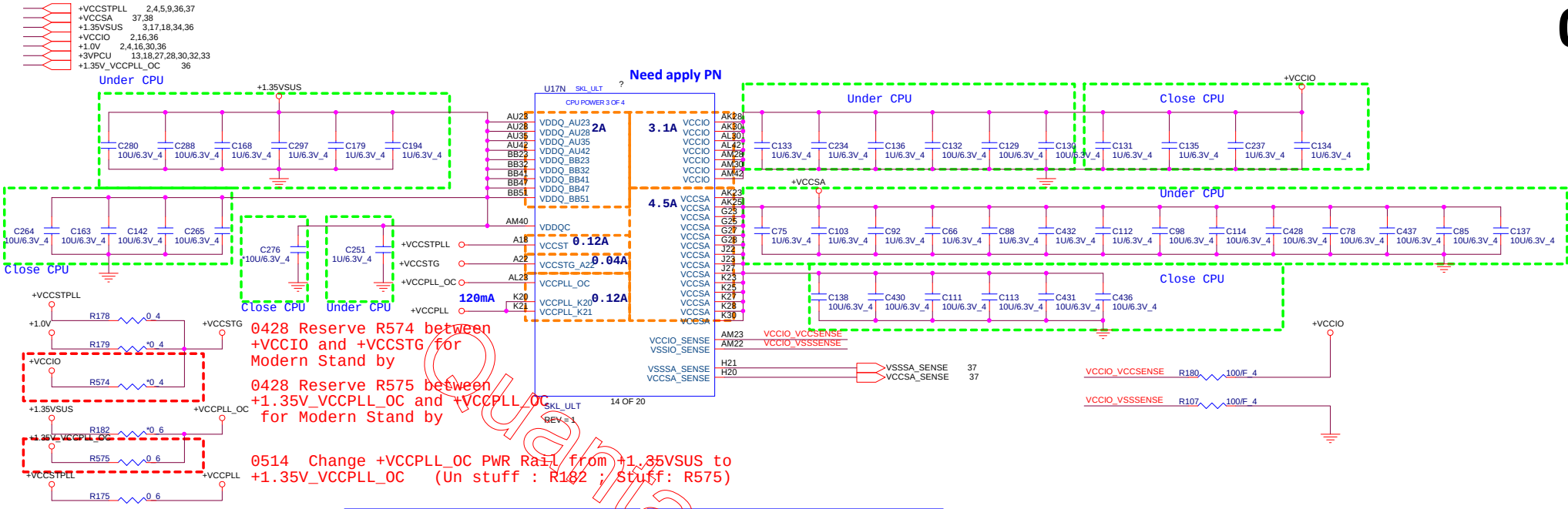


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

0506 Change R254, R266 from 0 OHM to shurtpad

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYPAKE 6/20 (POWER-1)	1A
Date: Wednesday, May 20, 2015	Sheet 5 of 42	



IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

Close to FAN PIPE BOT Side

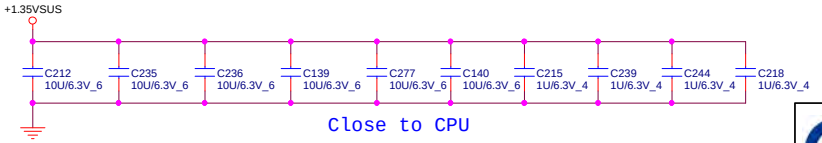
CPU VR Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

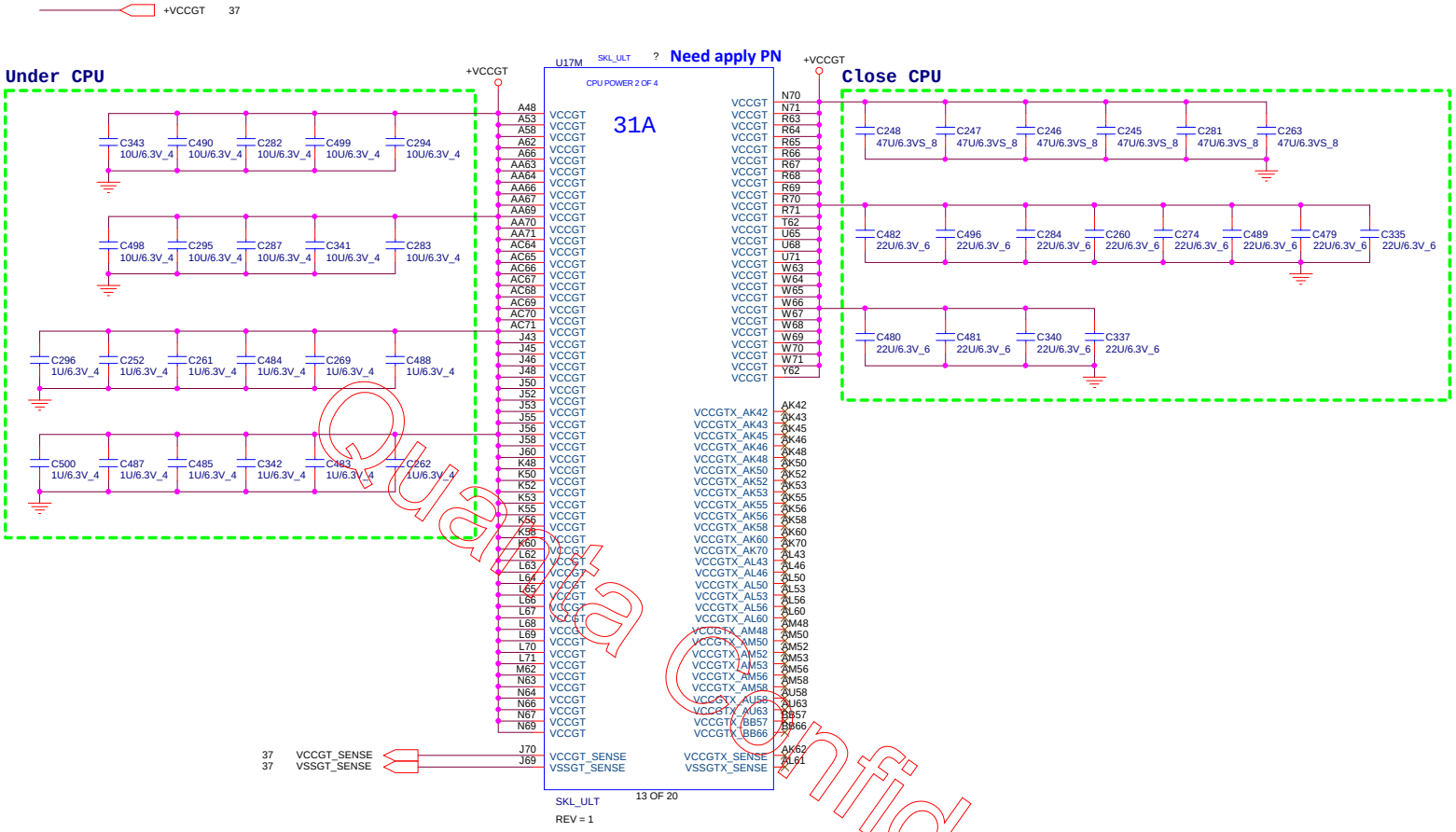
Close to VCORE Choke BOT Side

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

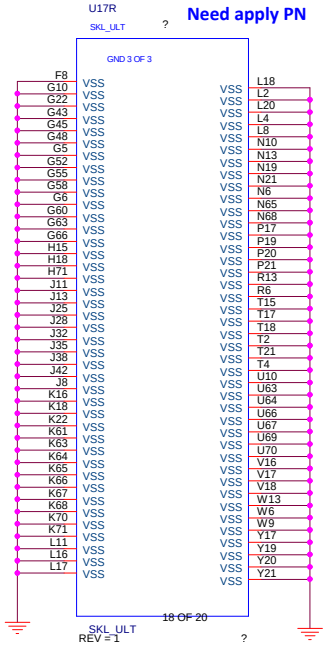


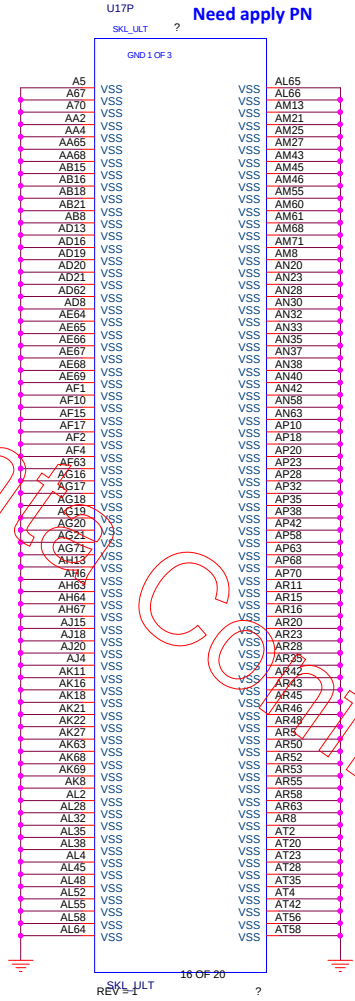
PROJECT : Y62P/Y63P
Quanta Computer Inc.

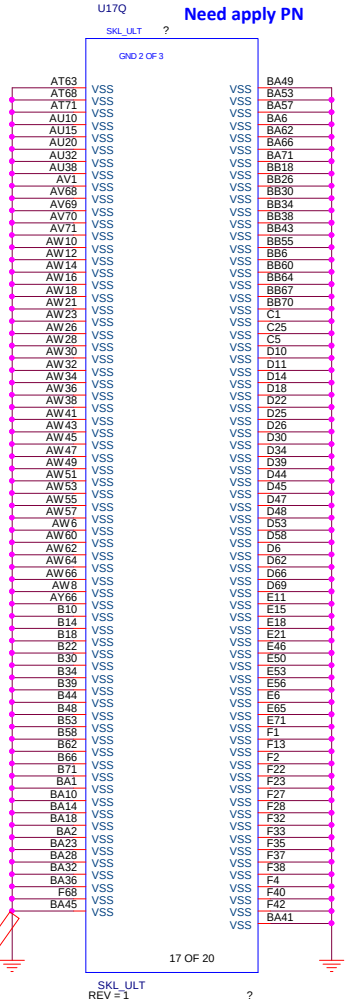
Size	Document Number	Rev
Custom	06 -- SKYPAKE 7/20 (POWER-2)	1A
Date: Wednesday, May 20, 2015	Sheet 6 of 42	



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



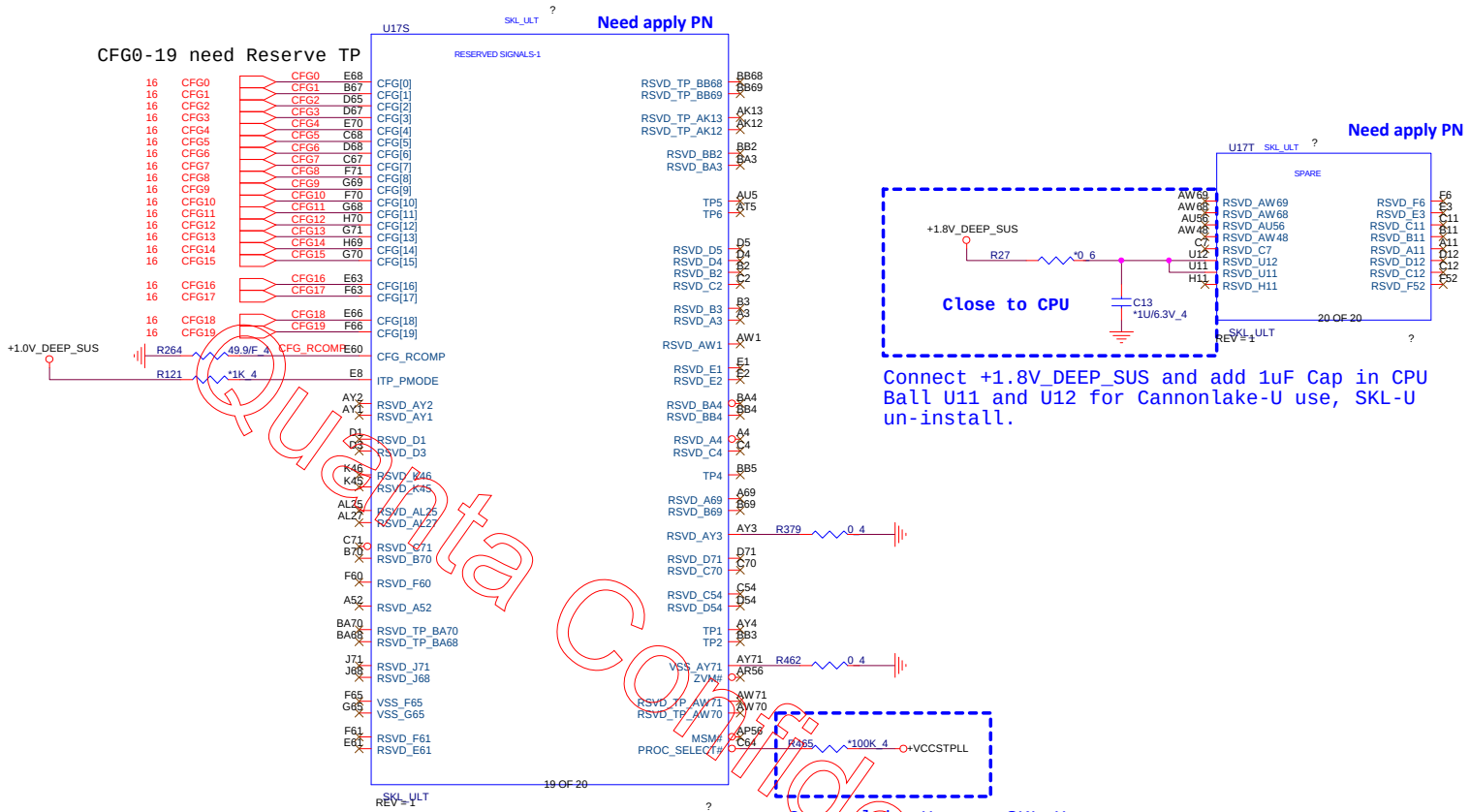




PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	8 -- SKYPAKE 9/20 (GND-1)	1A
Date: Wednesday, May 20, 2015	Sheet 8 of 42	

+1.0V_DEEP_SUS 13,15,16,35,36
+VCCSTPLL 2,4,5,6,36,37



Processor Strapping

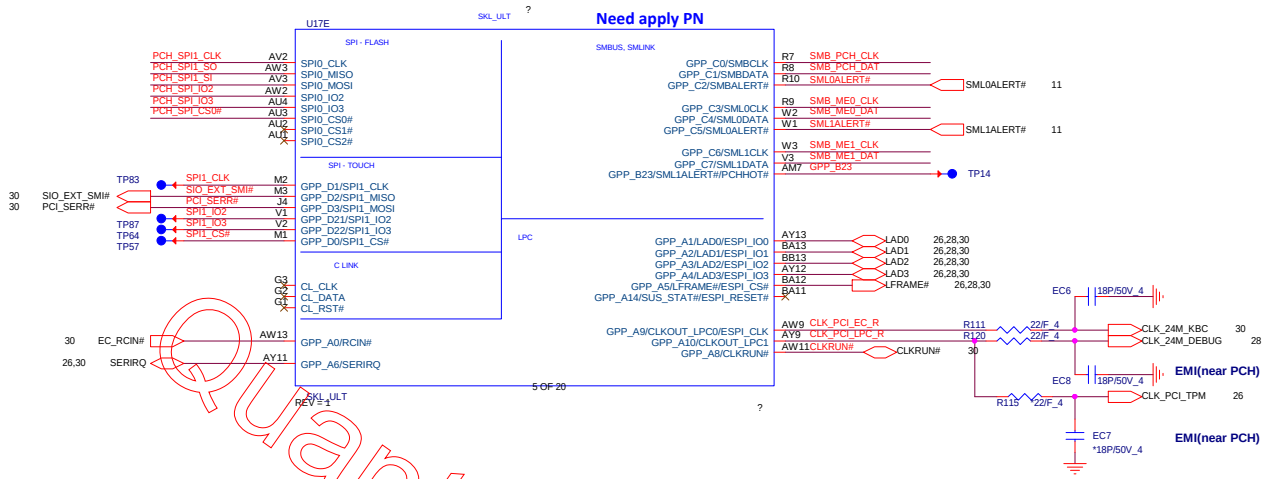
The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R466 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R468 1K_4

PROJECT : Y62P/Y63P
Quanta Computer Inc.

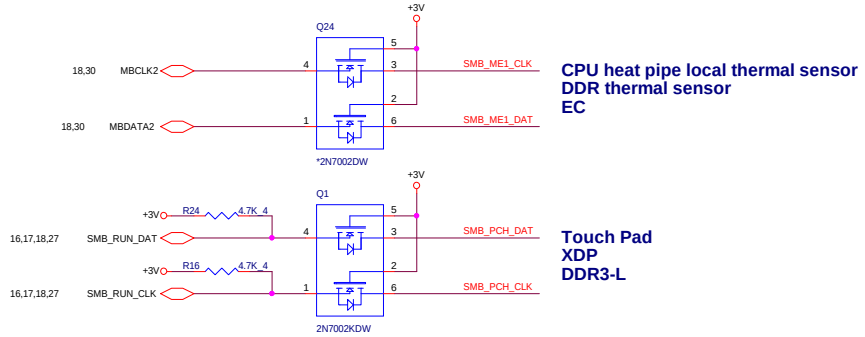
Size	Document Number	Rev
Custom	9 -- SKYPAKE 12/20 (RSV-1)	1A
Date: Wednesday, May 20, 2015	Sheet 9 of 42	

+3V_DEEP_SUS 4,11,12,14,15,16,18
+3V 2,4,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+3VS5 4,15,16,28,29,30,33,35,36,39



GPIO Pull UP

SMBus/Pull-up(CLG)



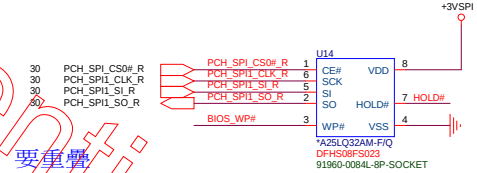
CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR3-L

PCH SPI ROM(CLG)

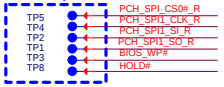
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

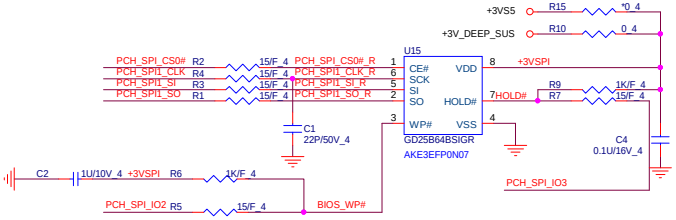


U14 &U15 footprint 要重疊

Need place to TOP



PCH SPI ROM(CLG)



R1/R2/R3/R4/R5/R7 close to U15 pin

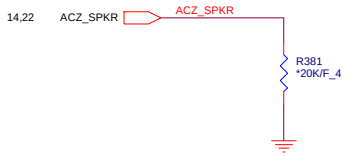
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)	1A
Date: Wednesday, May 20, 2015	Sheet 10of 42	

+3V_DEEP_SUS 4,10,12,14,15,16,18
+3V 2,4,10,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39

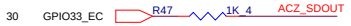
Functional Strap Definitions

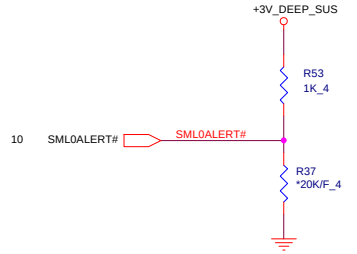
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



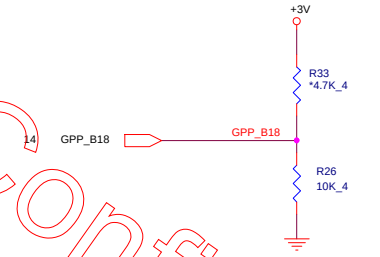
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.





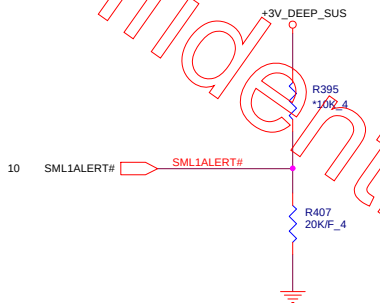
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

PROJECT : Y62P/Y63P Quanta Computer Inc.		
Size: Custom	Document Number: 11 -- SKYPAKE 15/20(HDA)	Rev: 1A
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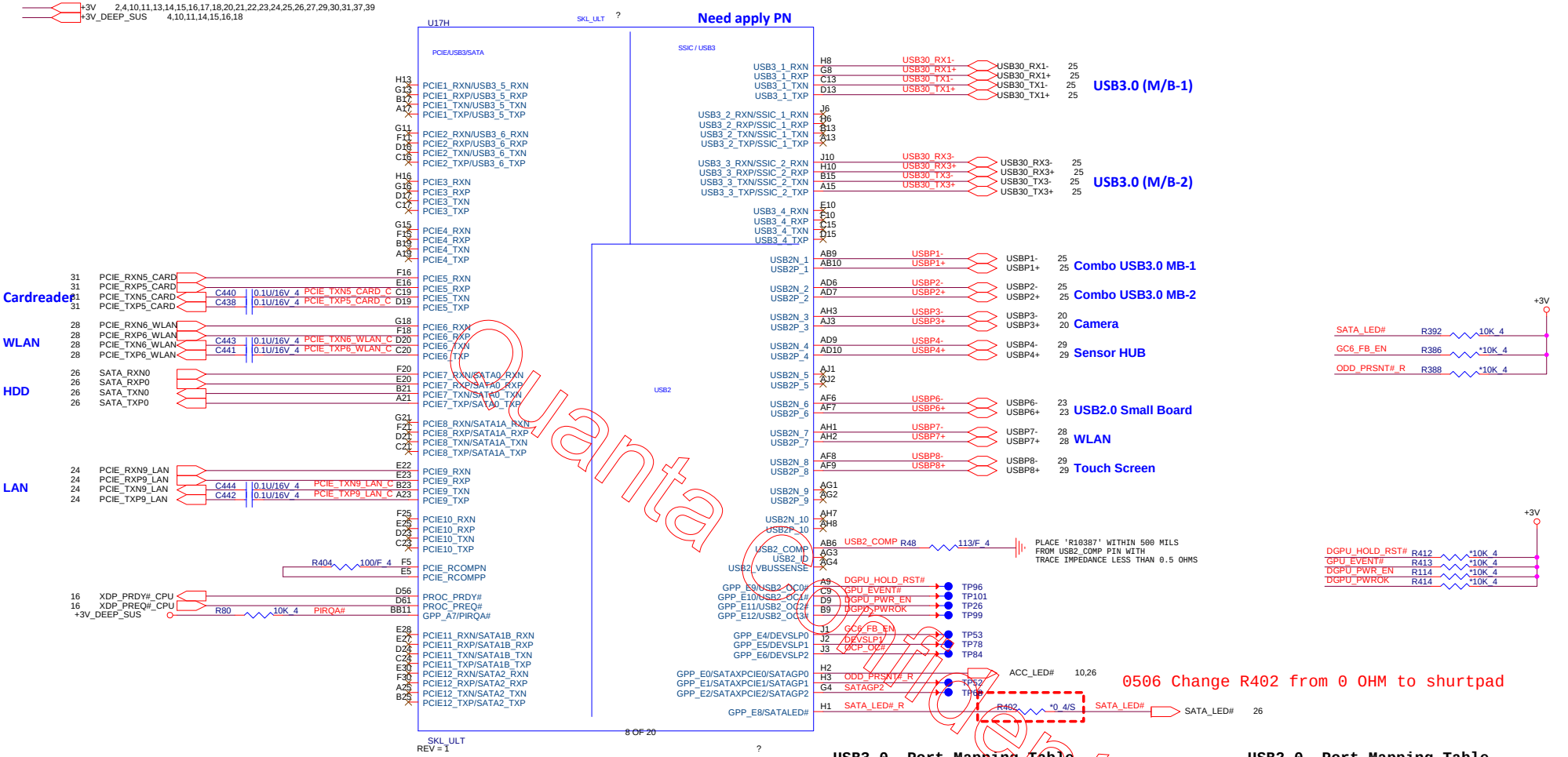

0506 Change R402 from 0 OHM to shurtpad

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	Un-used	Port1	CardReader
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	LAN
Port5	CardReader	Port4	Un-used
Port6	WLAN	Port5	Un-used
Port7	HDD		
Port8	Un-used		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	USB3.0 MB-2
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 MB-2
PORT-3	Camera
PORT-4	Sensor HUB
PORT-5	NC
PORT-6	USB2.0 Small Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- SKYPAKE 16/20 (PCIE/USB)	1A
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+3V_RTC_2 4,15
+3V_RTC 4,15,27,28,32
+3V 2,4,10,11,12,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+1.0V_DEEP_SUS 9,15,16,35,36

Need apply PN

U17J SKL_ULT ?

CLOCK SIGNALS

Cardreader	31	CLK_PCIE_CRN	PCIE_CLKREQ0#
	31	CLK_PCIE_CRP	CLK_PCIE_CRN
	31	PCIE_CLKREQ_CR#	CLK_PCIE_CRP / PCIE_CLKREQ_CR#
WLAN	28	CLK_PCIE_WLANN	CLK_PCIE_WLANN
	28	CLK_PCIE_WLANP	CLK_PCIE_WLANP
	28	PCIE_CLKREQ_WLAN#	PCIE_CLKREQ_WLAN#
LAN	24	CLK_PCIE_LANN	CLK_PCIE_LANN
	24	CLK_PCIE_LANP	CLK_PCIE_LANP
	24	PCIE_CLKREQ_LAN#	PCIE_CLKREQ_LAN#

D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5
E38 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#

PCIE_CLKREQ0# PCIE_CLKREQ_VGA# PCIE_CLKREQ5#

CLKOUT_ITPXDP_N F43 CK_XDP_N_R
CLKOUT_ITPXDP_P E43 CK_XDP_P_R
RP1 2 4 1 3 *0_4P2R_4
CK_XDP_N 16
CK_XDP_P 16

GPD8/SUSCLK BA17 PCH_SUSCLK TP41

XTAL24_IN E37 XTAL24_IN
XTAL24_OUT E35 XTAL24_OUT

XCLK_BIASREF E42 XCLK_BIASREF
+1.0V_DEEP_SUS
R444 2.7K/F_4
R445 *60.4/F_4

RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2 TP60

SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST#
RTC_RST# 16

TBT

10 OF 20

SKL_ULT REV = 1

RP5002 install for XDP

Co-lay 60ohm 1% to GND for Cannonlake use

CLK_REQ/Strap Pin(CLG)

+3V
PCIE_CLKREQ_VGA# R73 10K_4
PCIE_CLKREQ_WLAN# R93 10K_4
PCIE_CLKREQ_LAN# R104 10K_4
PCIE_CLKREQ_CR# R92 10K_4
PCIE_CLKREQ5# R82 10K_4
PCIE_CLKREQ0# R96 10K_4

Need apply PN

U17I SKL_ULT ?

CSI2

A39 CSI2_DN0
B36 CSI2_DP0
C39 CSI2_DN1
D38 CSI2_DP1
C36 CSI2_DN2
D36 CSI2_DP2
A36 CSI2_DN3
B38 CSI2_DP3
C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A33 CSI2_DN6
B33 CSI2_DP6
A31 CSI2_DN7
B31 CSI2_DP7
A29 CSI2_DN8
B29 CSI2_DP8
C29 CSI2_DN9
D29 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 C32
CSI2_CLKP1 D32
CSI2_CLKN2 C29
CSI2_CLKP2 D29
CSI2_CLKN3 C26
CSI2_CLKP3 D26

CSI2_COMP E13 R136 100/F_4
GPP_D4/FLASHTRIG B7 GPP_D4 TP95

EMMC

GPP_F13/EMMC_DATA0 AP2 GPP_F13 TP77
GPP_F14/EMMC_DATA1 AP1 GPP_F14 TP67
GPP_F15/EMMC_DATA2 AP3 GPP_F15 TP86
GPP_F16/EMMC_DATA3 AN3 GPP_F16 TP75
GPP_F17/EMMC_DATA4 AN1 GPP_F17 TP66
GPP_F18/EMMC_DATA5 AN2 GPP_F18 TP80
GPP_F19/EMMC_DATA6 AM4 GPP_F19 TP85
GPP_F20/EMMC_DATA7 AM1 GPP_F20 TP59

GPP_F21/EMMC_RCLK AM2 EMMC_RCLK TP62
GPP_F22/EMMC_CLK AM3 EMMC_CLK TP73
GPP_F12/EMMC_CMD AP4 EMMC_CMD TP78

EMMC_RCOMP AT1 EMMC_RCOMP R393 200/F_4

9 OF 20

SKL_ULT REV = 1

RTC Clock 32.768KHz

C421 12P/50V_4 C422 12P/50V_4 Y2 32.768KHZ NC NC R403 10M_4 RTC_X1 RTC_X2

0506 Change C421, C422 from 18P to 12P for vendor suggest

RTC Circuitry(RTC)

30mils

+3V_RTC_2 +3V_RTC R291 0_4 R292 *0_4 J1 *SOLDERJUMPER-2 R278 20K/F_4 RTC_RST#

RTC Power trace width 20mils.

+3V_RTC_0 CN20 RTC SOCKET R251 1K +3V_RTC_1 +3VPCU D7 MEK500V-40 D6 MEK500V-40 R267 20K/F_4 SRTC_RST# C310 1U/6.3V_4 C311 1U/6.3V_4 C306 1U/6.3V_4

RTC_RST# R277 *0_6 SRTC_RST#

RTC_RST# Q16 2N7002K EC_RST# R298 10K_4 EC_RST#

External Crystal and Green Clock

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

XTAL24_IN XTAL24_OUT R442 1M_4 TP103 C460 33P/50V_4 24MHZ +-30PPM Y3 C453 33P/50V_4 TP102

0512 Change Y3 from BG624000044 to BG624000107
0512 Change C456, C460 from 12pF to 22pF
0514 Change C456, C460 from 22pF to 27pF
0520 Change C456, C460 from 27pF to 33pF

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYPAKE 17/20 (CLK)	1A
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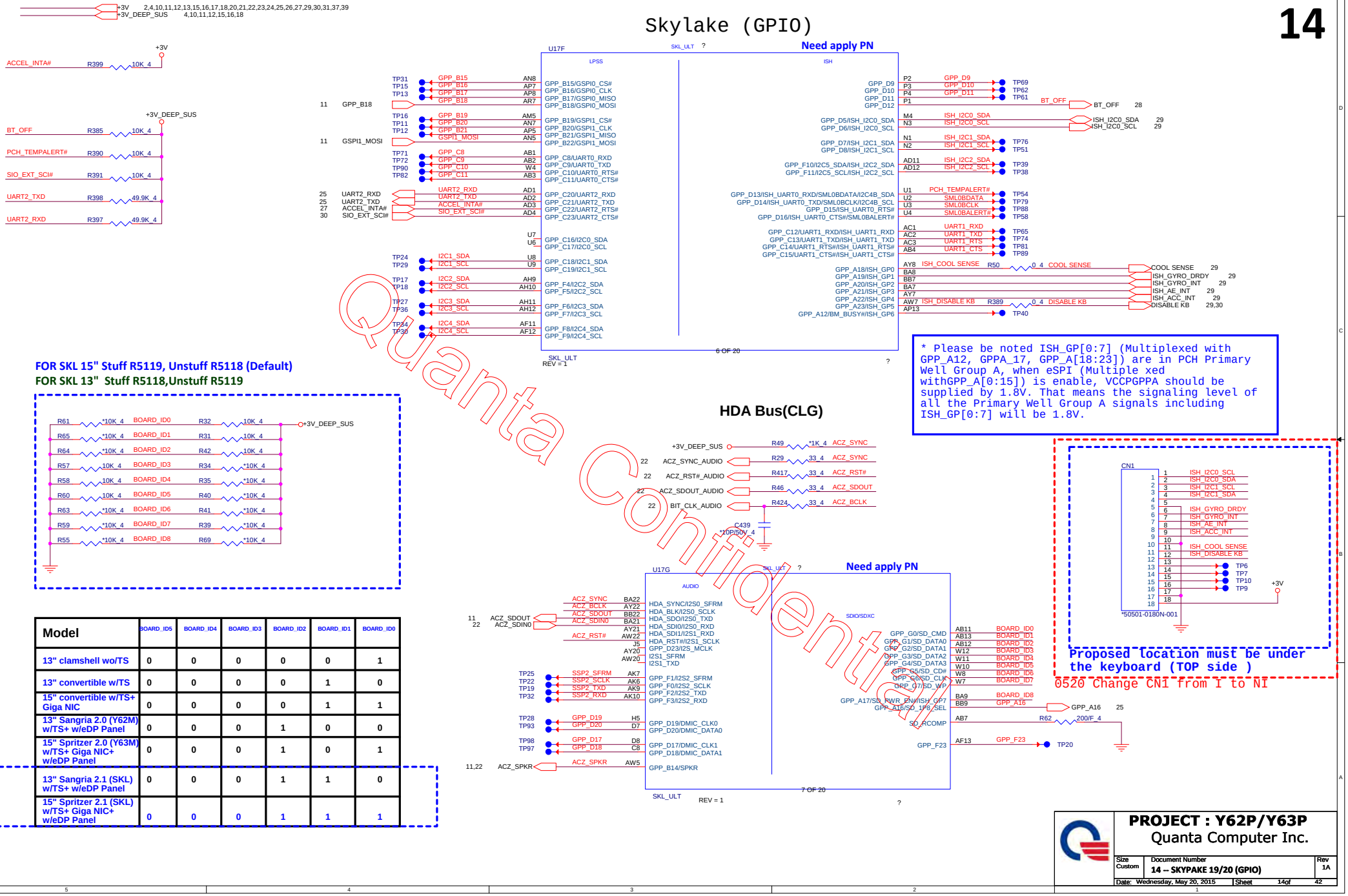
Skylake (GPIO)



FOR SKL 15" Stuff R5119, Unstuff R5118 (Default)
FOR SKL 13" Stuff R5118,Unstuff R5119

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
13" clamshell wo/TS	0	0	0	0	0	1
13" convertible w/TS	0	0	0	0	1	0
15" convertible w/TS+ Giga NIC	0	0	0	0	1	1
13" Sangria 2.0 (Y62M) w/TS+ w/eDP Panel	0	0	0	1	0	0
15" Spritzer 2.0 (Y63M) w/TS+ Giga NIC+ w/eDP Panel	0	0	0	1	0	1
13" Sangria 2.1 (SKL) w/TS+ w/eDP Panel	0	0	0	1	1	0
15" Spritzer 2.1 (SKL) w/TS+ Giga NIC+ w/eDP Panel	0	0	0	1	1	1

HDA Bus(CLG)

* Please be noted ISH_GP[0:7] (Multiplexed with GPP_A12, GPPA_17, GPP_A[18:23]) are in PCH Primary Well Group A, when eSPI (Multiple xed withGPP_A[0:15]) is enable, VCCPGPPA should be supplied by 1.8V. That means the signaling level of all the Primary Well Group A signals including ISH_GP[0:7] will be 1.8V.

Proposed location must be under the keyboard (TOP side)

0520 Change CN1 from I to NI

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 – SKYPAKE 19/20 (GPIO)	1A
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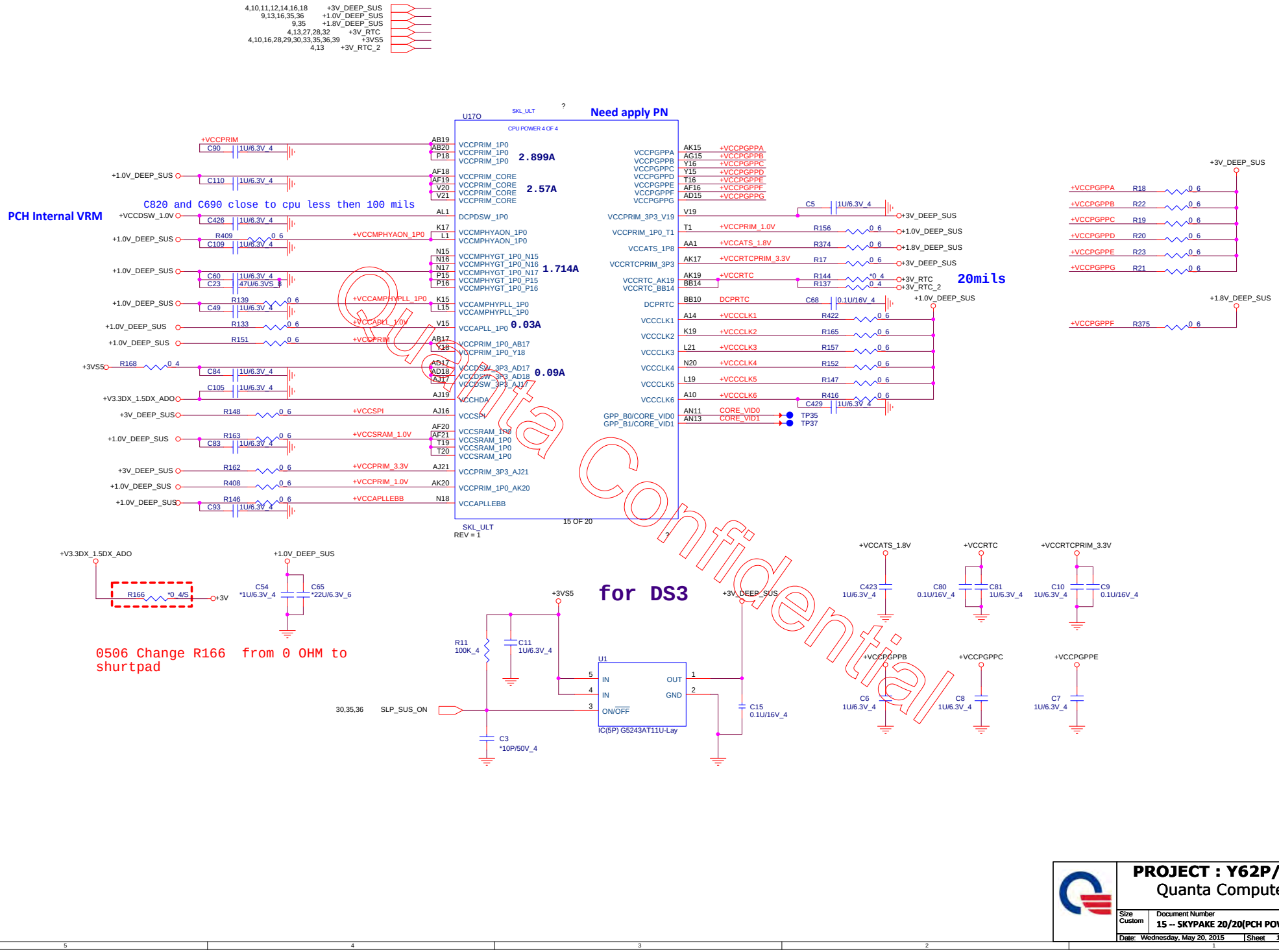
4,10,11,12,14,16,18 +3V_DEEP_SUS
9,13,16,35,36 +1.0V_DEEP_SUS
9,35 +1.8V_DEEP_SUS
4,13,27,28,32 +3V_RTC
4,10,16,28,29,30,33,35,36,39 +3VSS
4,13 +3V_RTC_2
U17O
SKL_ULT
CPU POWER 4 OF 4
Need apply PN
PCH Internal VRM
C820 and C690 close to cpu less then 100 mils
2.899A
2.57A
1.714A
0.03A
0.09A
20mils
15 OF 20
SKL_ULT
REV = 1
for DS3
0506 Change R166 from 0 OHM to shurtpad
IC(5P) G5243AT11U-Lay
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PROJECT : Y62P/Y63P
Quanta Computer Inc.
Size Custom
Document Number
15 -- SKYPAKE 20/20(PCH POWER)
Rev 1A
Date: Wednesday, May 20, 2015
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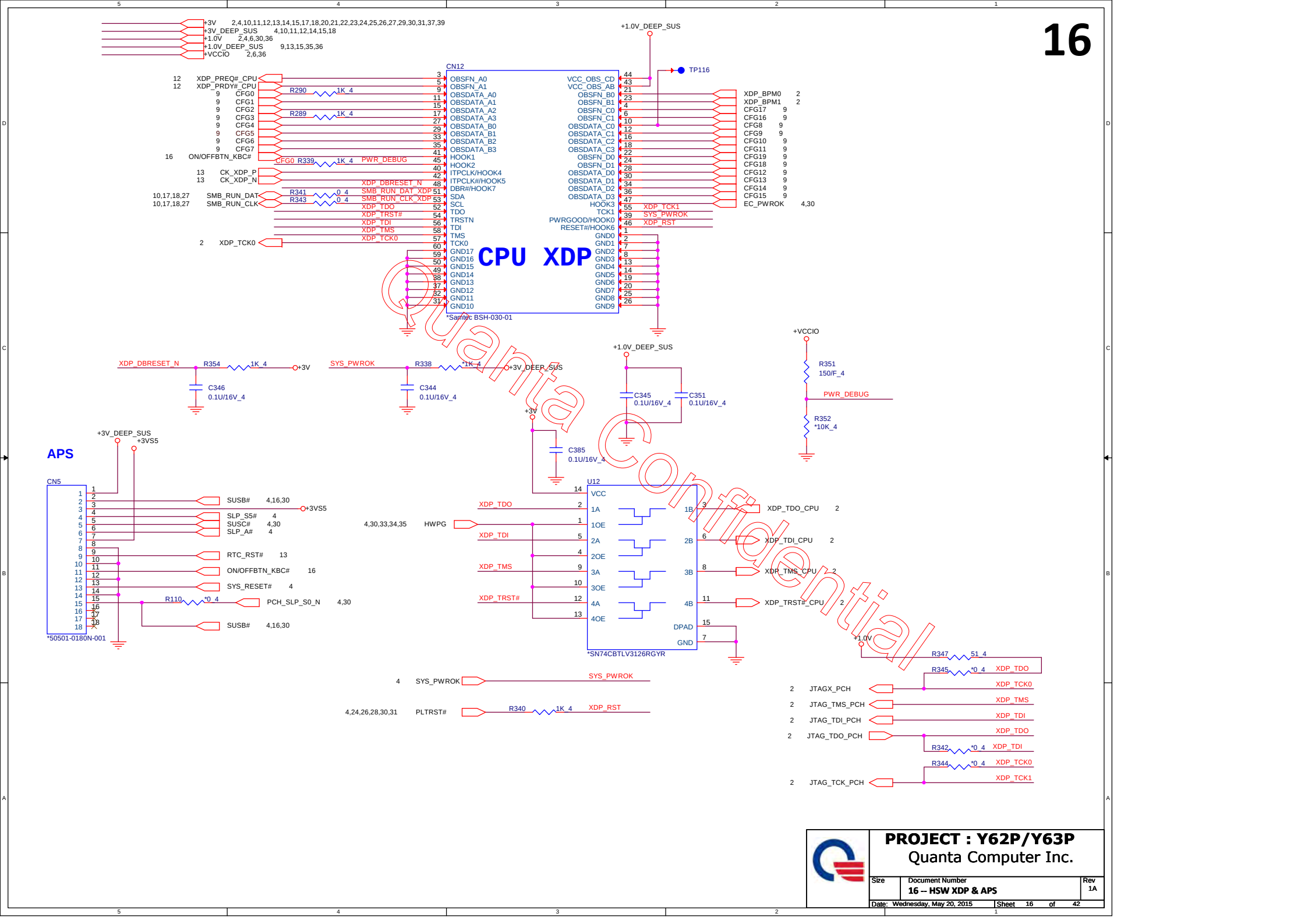
WWW.AliSaler.Com


16
CPU XDP
APS
CN12
*Samtec BSH-030-01
CN5
*50501-0180N-001
U12
*SN74CBTLV3126RGYR
TP116
+3V 2,4,10,11,12,13,14,15,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+3V_DEEP_SUS 4,10,11,12,14,15,18
+1.0V 2,4,6,30,36
+1.0V_DEEP_SUS 9,13,15,35,36
+VCCIO 2,6,36
+1.0V_DEEP_SUS
+3V_DEEP_SUS
+3VS5
+3V
+VCCIO
+1.0V
XDP_PREQ#_CPU
XDP_PRDY#_CPU
CFG0
CFG1
CFG2
CFG3
CFG4
CFG5
CFG6
CFG7
ON/OFFBTN_KBC#
CK_XDP_P
CK_XDP_N
SMB_RUN_DAT
SMB_RUN_CLK
XDP_TCK0
R290 1K_4
R289 1K_4
R339 1K_4 PWR_DEBUG
R341 0_4
R343 0_4
XDP_DBRESET_N
SMB_RUN_DAT_XDP
SMB_RUN_CLK_XDP
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_TCK0
OBSFN_A0
OBSFN_A1
OBSDATA_A0
OBSDATA_A1
OBSDATA_A2
OBSDATA_A3
OBSDATA_B0
OBSDATA_B1
OBSDATA_B2
OBSDATA_B3
HOOK1
HOOK2
ITPCLK/HOOK4
ITPCLK#/HOOK5
DBR#/HOOK7
SDA
SCL
TDO
TRSTN
TDI
TMS
TCK0
GND17
GND16
GND15
GND14
GND13
GND12
GND11
GND10
VCC_OBS_CD
VCC_OBS_AB
OBSFN_B0
OBSFN_B1
OBSFN_C0
OBSFN_C1
OBSDATA_C0
OBSDATA_C1
OBSDATA_C2
OBSDATA_C3
OBSFN_D0
OBSFN_D1
OBSDATA_D0
OBSDATA_D1
OBSDATA_D2
OBSDATA_D3
HOOK3
TCK1
PWRGOOD/HOOK0
RESET#/HOOK6
GND0
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
XDP_BPM0
XDP_BPM1
CFG17
CFG16
CFG8
CFG9
CFG10
CFG11
CFG19
CFG18
CFG12
CFG13
CFG14
CFG15
EC_PWROK
XDP_TCK1
SYS_PWROK
XDP_RST
XDP_DBRESET_N R354 1K_4 +3V
C346 0.1U/16V_4
SYS_PWROK R338 *1K_4 +3V_DEEP_SUS
C344 0.1U/16V_4
C345 0.1U/16V_4
C351 0.1U/16V_4
C385 0.1U/16V_4
R351 150/F_4
PWR_DEBUG
R352 *10K_4
SUSB# 4,16,30
SLP_S5# 4
SUSC# 4,30
SLP_A# 4
RTC_RST# 13
ON/OFFBTN_KBC# 16
SYS_RESET# 4
R110 *0_4 PCH_SLP_S0_N 4,30
SUSB# 4,16,30
4,30,33,34,35 HWPG
XDP_TDO
XDP_TDI
XDP_TMS
XDP_TRST#
1OE
2OE
3OE
4OE
1A
2A
3A
4A
1B
2B
3B
4B
DPAD
GND
XDP_TDO_CPU 2
XDP_TDI_CPU 2
XDP_TMS_CPU 2
XDP_TRST#_CPU 2
4 SYS_PWROK
4,24,26,28,30,31 PLTRST#
R340 1K_4 XDP_RST
R347 51_4
R345 *0_4 XDP_TDO
2 JTAGX_PCH XDP_TCK0
2 JTAG_TMS_PCH XDP_TMS
2 JTAG_TDI_PCH XDP_TDI
2 JTAG_TDO_PCH XDP_TDO
R342 *0_4 XDP_TDI
R344 *0_4 XDP_TCK0
2 JTAG_TCK_PCH XDP_TCK1
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Quanta Computer Inc.
Size
Document Number
16 -- HSW XDP & APS
Rev 1A
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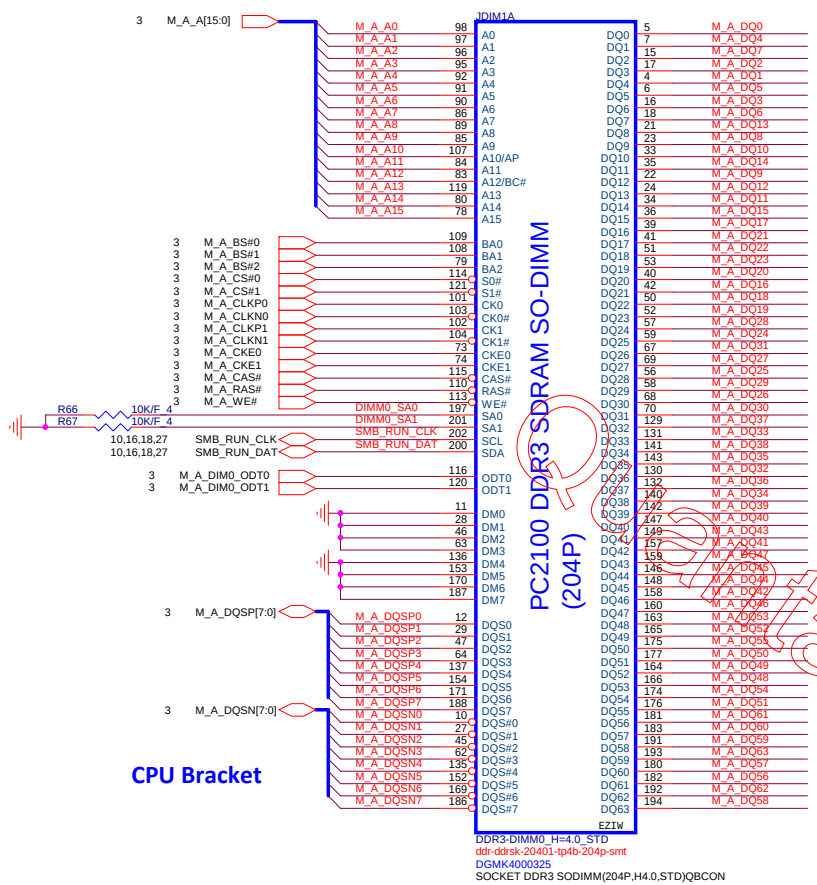
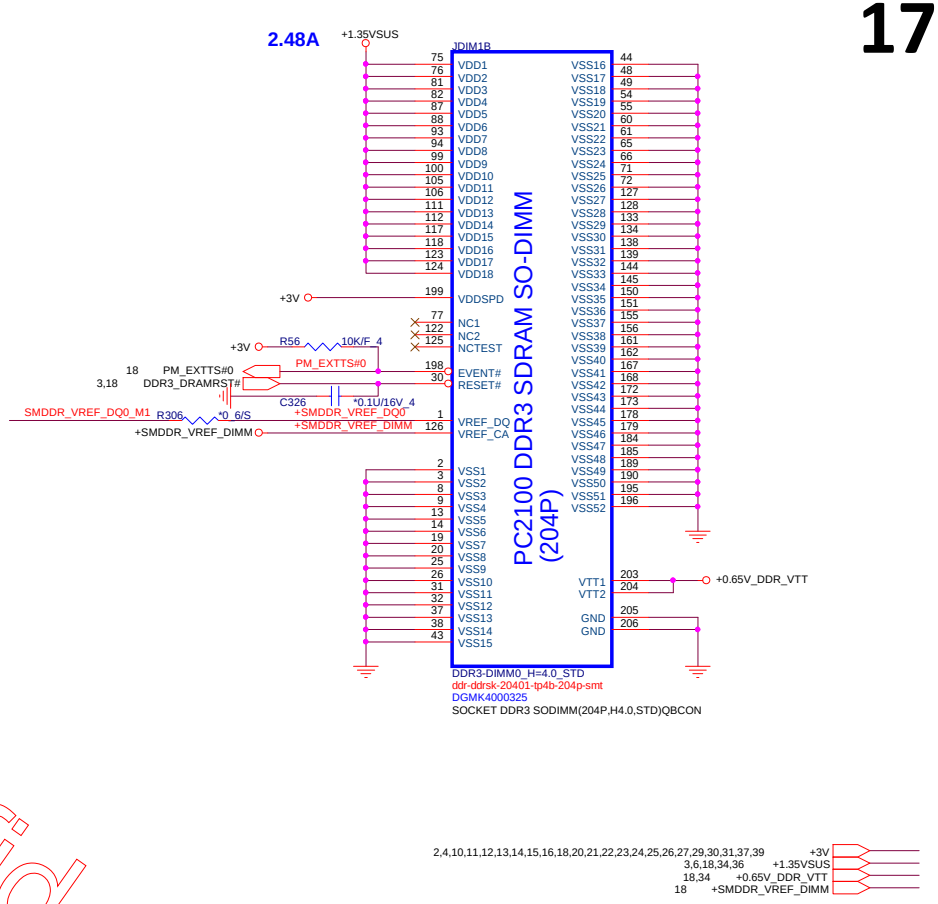
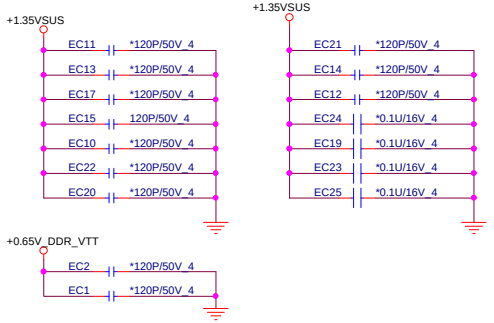




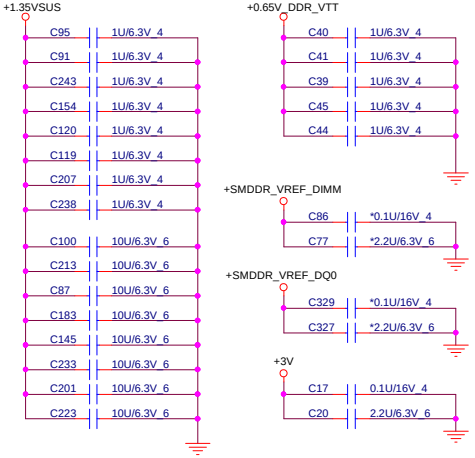
2,4,10,11,12,13,14,15,16,18,20,21,22,23,24,25,26,27,29,30,31,37,39 +3V
3,6,18,34,36 +1.35VSUS
18,34 +0.65V_DDR_VTT
18 +SMDDR_VREF_DIMM

For EMI RESERVE

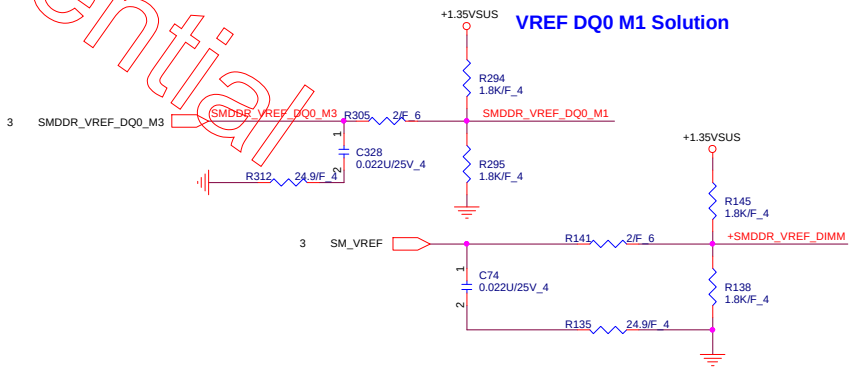


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	17 -- DDR3 DIMM0-STD(4.0H)	1A
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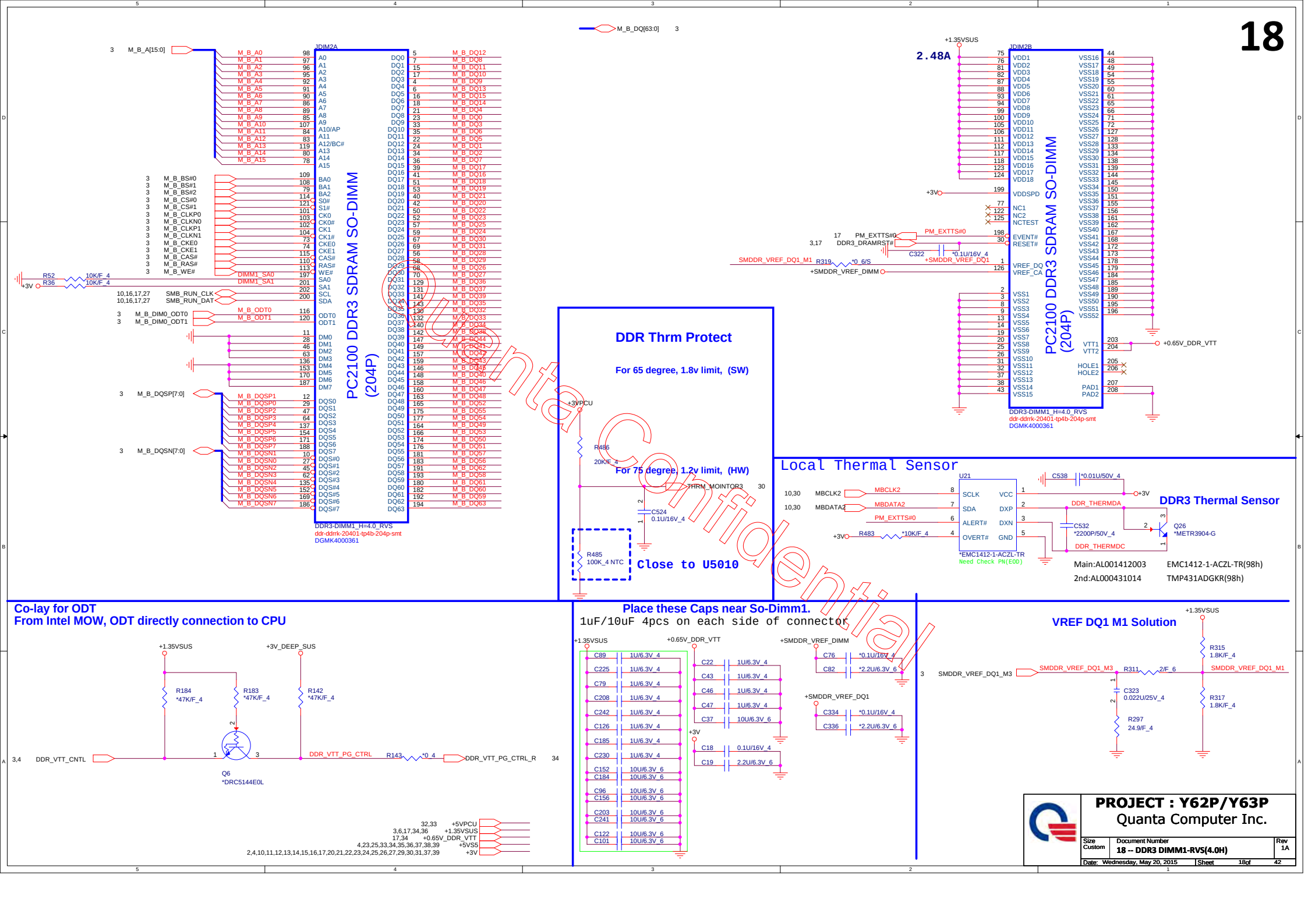
M_B_DQ[63:0] 3
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
M_B_A[15:0]
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_CS#0
M_B_CS#1
M_B_CLKP0
M_B_CLKN0
M_B_CLKP1
M_B_CLKN1
M_B_CKE0
M_B_CKE1
M_B_CAS#
M_B_RAS#
M_B_WE#
DIMM1_SA0
DIMM1_SA1
SMB_RUN_CLK
SMB_RUN_DAT
M_B_ODT0
M_B_ODT1
M_B_DQSP[7:0]
M_B_DQSN[7:0]
M_B_DQ[63:0]
DDR3-DIMM1_H=4.0_RVS
ddr-ddrk-20401-tp4b-204p-smt
DGMK4000361
R52 10K/F_4
R36 10K/F_4
+3V
DDR Thrm Protect
For 65 degree, 1.8v limit, (SW)
+3VPCU
R486
20K/F_4
For 75 degree, 1.2v limit, (HW)
THRM_MOINTOR3 30
C524
0.1U/16V_4
R485
100K_4 NTC
Close to U5010
Local Thermal Sensor
U21
*EMC1412-1-ACZL-TR
Need Check PN(EOD)
MBCLK2
MBDATA2
PM_EXTTS#0
C538 *0.01U/50V_4
DDR_THERMDA
DDR_THERMDC
C532 *2200P/50V_4
Q26 *METR3904-G
DDR3 Thermal Sensor
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU
+1.35VSUS
+3V_DEEP_SUS
R184 *47K/F_4
R183 *47K/F_4
R142 *47K/F_4
DDR_VTT_CNTL
DDR_VTT_PG_CTRL
R143 *0_4
DDR_VTT_PG_CTRL_R
Q6 *DRC5144E0L
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
+0.65V_DDR_VTT
+SMDDR_VREF_DIMM
+SMDDR_VREF_DQ1
C89 1U/6.3V_4
C225 1U/6.3V_4
C79 1U/6.3V_4
C208 1U/6.3V_4
C242 1U/6.3V_4
C126 1U/6.3V_4
C185 1U/6.3V_4
C230 1U/6.3V_4
C152 10U/6.3V_6
C184 10U/6.3V_6
C96 10U/6.3V_6
C156 10U/6.3V_6
C203 10U/6.3V_6
C241 10U/6.3V_6
C122 10U/6.3V_6
C101 10U/6.3V_6
C22 1U/6.3V_4
C43 1U/6.3V_4
C46 1U/6.3V_4
C47 1U/6.3V_4
C37 10U/6.3V_6
C18 0.1U/16V_4
C19 2.2U/6.3V_6
C76 *0.1U/16V_4
C82 *2.2U/6.3V_6
C334 *0.1U/16V_4
C336 *2.2U/6.3V_6
VREF DQ1 M1 Solution
SMDDR_VREF_DQ1_M3
SMDDR_VREF_DQ1_M1
R311 2/F_6
R315 1.8K/F_4
R317 1.8K/F_4
C323 0.022U/25V_4
R297 24.9/F_4
+5VPCU
+1.35VSUS
+0.65V_DDR_VTT
+5VS5
+3V
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
2.48A
PM_EXTTS#0
DDR3_DRAMRST#
C322 *0.1U/16V_4
SMDDR_VREF_DQ1_M1
R319 *0_6/S
+SMDDR_VREF_DIMM
+SMDDR_VREF_DQ1
+0.65V_DDR_VTT
DDR3-DIMM1_H=4.0_RVS
ddr-ddrk-20401-tp4b-204p-smt
DGMK4000361
Intel Confidential
PROJECT : Y62P/Y63P
Quanta Computer Inc.
Size Custom
Document Number 18 -- DDR3 DIMM1-RVS(4.0H)
Rev 1A
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Size Custom	Document Number **RTD2136**	Rev 1A
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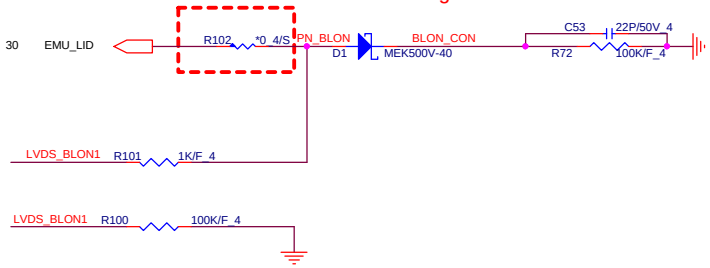
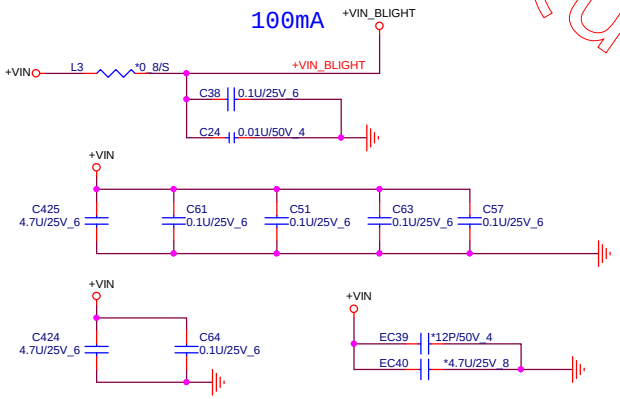
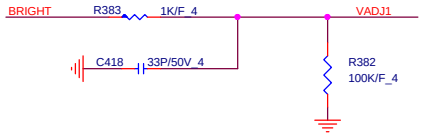
LID Switch

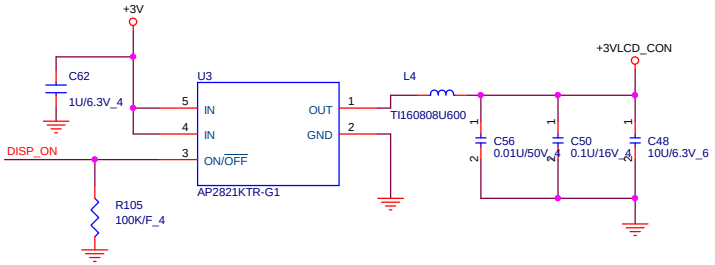
0506 ChangeR102 from 0 OHM to shurtpad



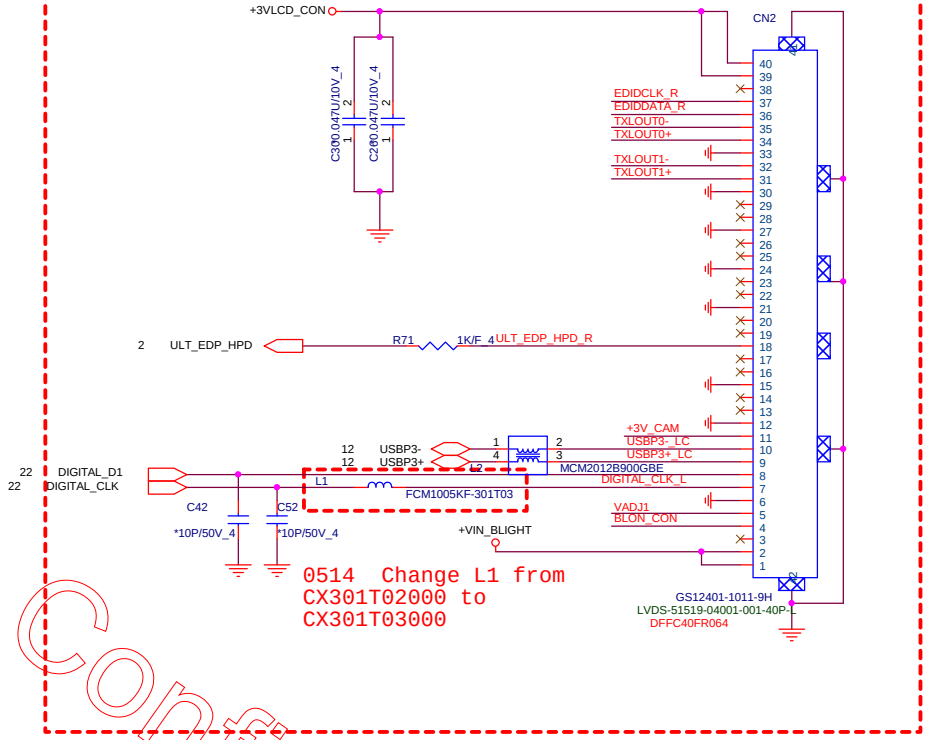
100mA





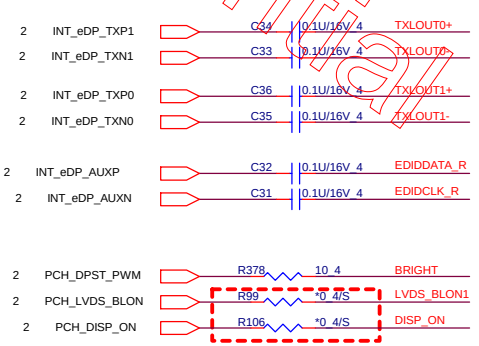


eDP Conn.

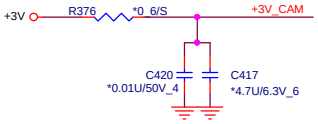


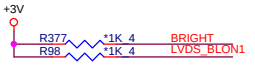
0514 Change L1 from CX301T02000 to CX301T03000

0506 Change CN2 footprint from lvds-50671-04041-001-40p-l to LVDS-51519-04001-001-40P-L



0506 Change R99, R106 from 0 OHM to shurtpad





2,4,10,11,12,13,14,15,16,17,18,21,22,23,24,25,26,27,29,30,31,37,39 +3V
6,13,18,27,28,30,32,33 +3VPCU
21,22,23,26,27,39 +5V
27,32,33,34,35,37,38 +VIN

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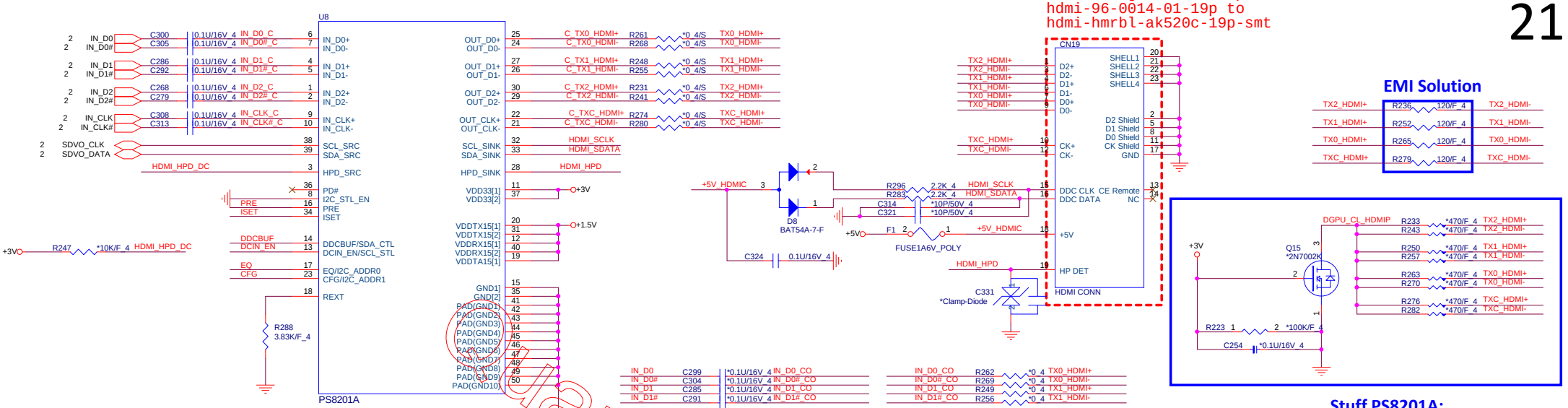
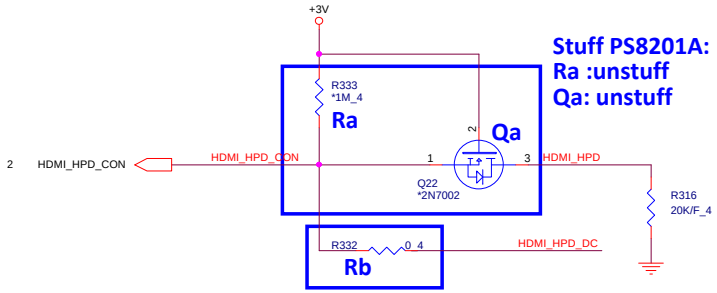
0415 Change CN19 footprint from
hdmi-96-0014-01-19p to
hdmi-hmrbl-ak520c-19p-smt



EMI Solution

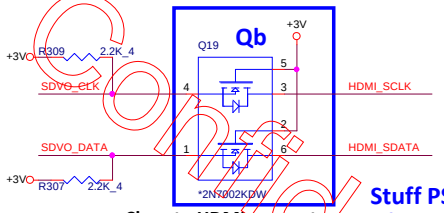
Stuff PS8201A:
DEL ALL

Stuff PS8201A:
Ra :unstuff
Qa: unstuff



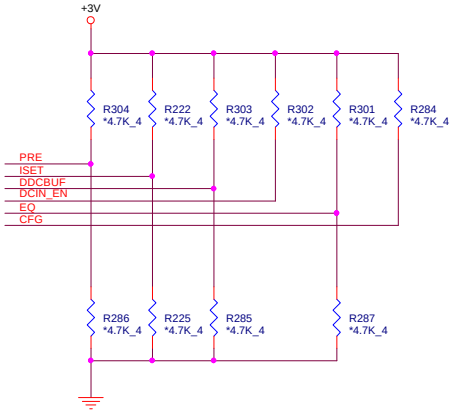
Stuff PS8201A
Rb: stuff

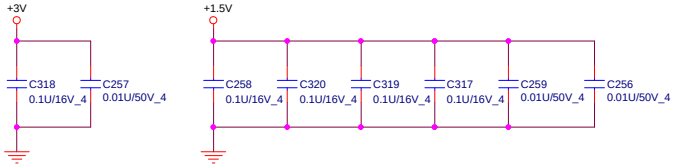
HDMI SMBus Isolation



Close to HDMI connector

Stuff PS8201A:
Qb:unstuff





2,4,10,11,12,13,14,15,16,17,18,20,22,23,24,25,26,27,29,30,31,37,39 +3V
22,35 +1.5V
22,23,26,27,39 +5V

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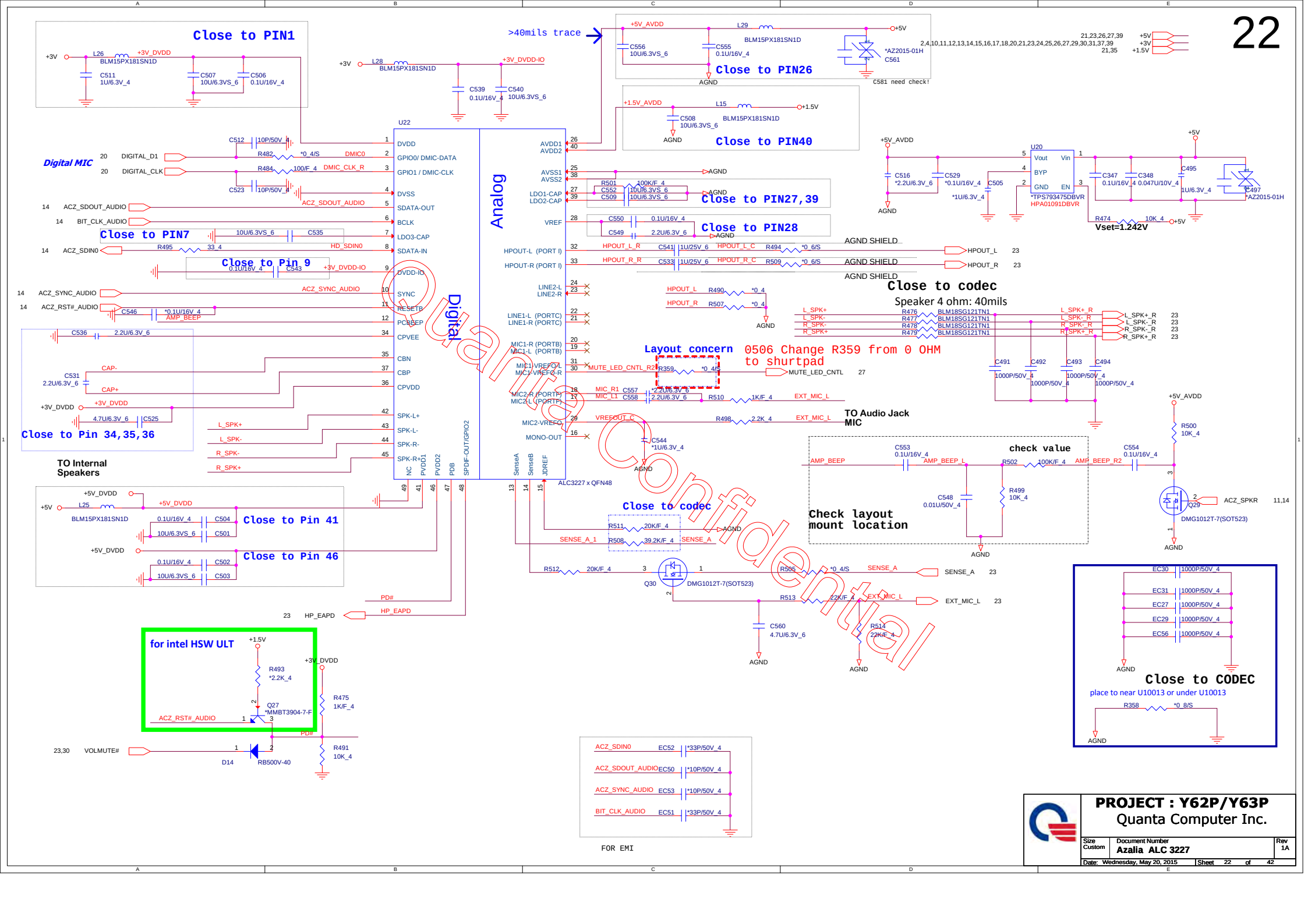

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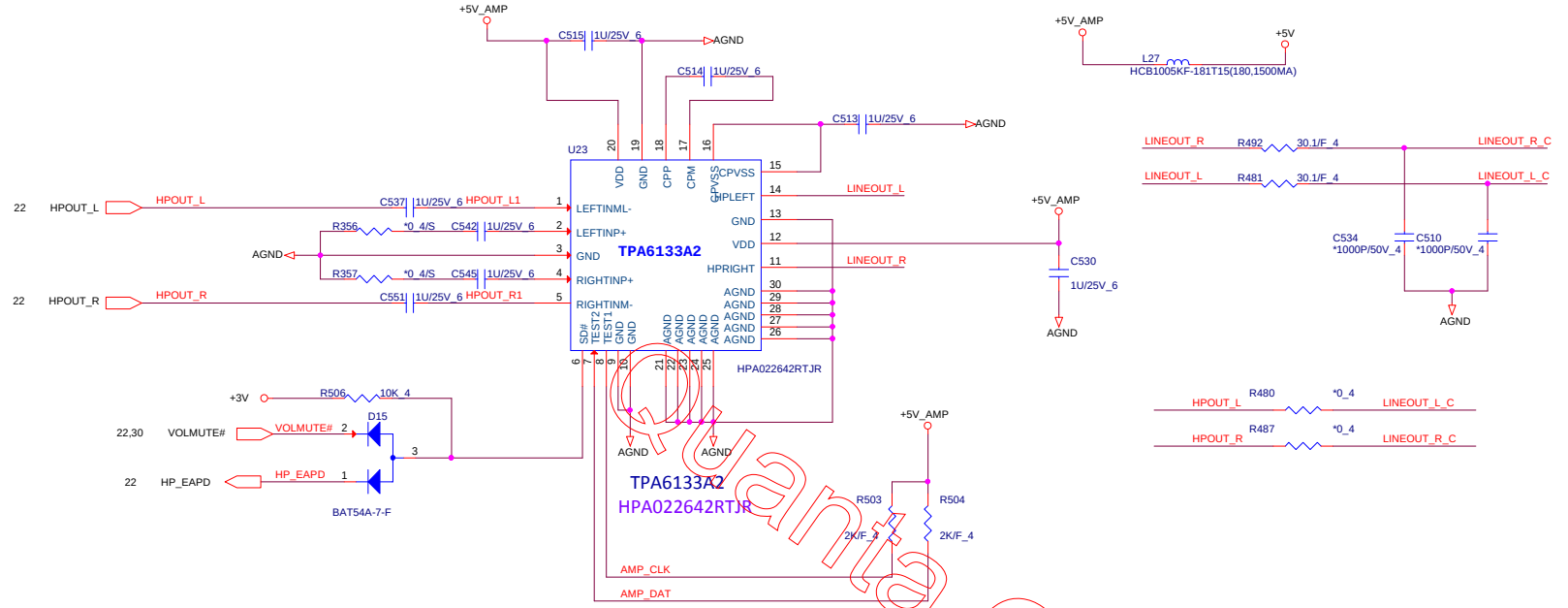
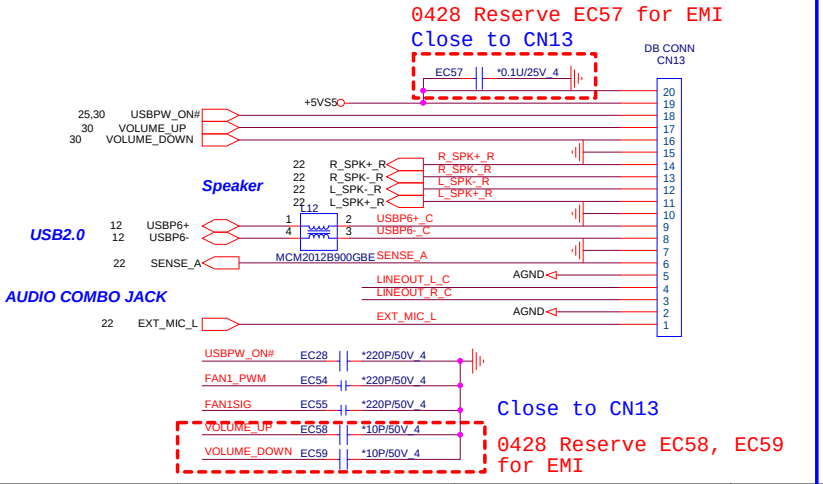
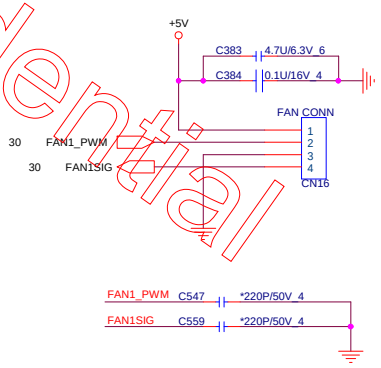
Head Phone out



Audio Board



FAN



2,4,10,11,12,13,14,15,16,17,18,20,21,22,24,25,26,27,29,30,31,37,39 +3V
21,22,26,27,39 +5V
4,25,33,34,35,36,37,38,39 +5VS5

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For EMI 0 ~ 22 ohm

R208 10/F_4

LAN_XTAL1 — XTAL1

Y1 25MHZ +-10PPM

XTAL2

C232 10P/50V_4

C231 10P/50V_4

Trace<30 mil
Width > 60 mil

Power trace Layout 寬度> 60mil

>60mil

+1.05V_LAN_REGOUT

4.7UH,+-20%,650MA_1210 L21 La

>60mil

R206 *0_8

Cb C178 4.7U/6.3V_6

Ca C180 0.1U/16V_4

Cc C450 0.1U/16V_4

Cd C216 0.1U/16V_4

Ce C458 0.1U/16V_4

Cf C456 0.1U/16V_4

Cg C455 *1U/6.3V_4

C182 0.1U/16V_4

C447 *1U/6.3V_4 Cf

C181 *0.1U/16V_4

+1.05V_LAN

Close to Choke La
SWR mode need stuff Ca & Cb

Place Cg & C128 close to each VDD10 pin22

For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)

13 PCIE_CLKREQ_LAN#

LED1:
FOR GIGA 8161: Stuff Ra, DEL Rb (Default)
FOR 10/100 8176: Stuff Rb,DEL Ra

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

+1.05V_LAN

R443 2.49K/F_4 LANRSET

+3V_LAN

LAN_AMBLED# TP43

Ra

R210 0_4 LAN_WLED#

Rb R209 *0_4

+3V

R441 1K_4

ISOLATEB

R440 15K/F_4

U6

RTL8176EH

Please add 9 GND VIAs connection with thermal PAD

MDI0+ MDI0- VDD10 MDI1+ MDI1- MDI2+ MDI2- VDD10

MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10

REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

+1.05V_LAN_REGOUT +3V_LAN +1.05V_LAN PCIE_WAKE# ISOLATEB PCIE_RXN9_LAN_L PCIE_RXP9_LAN_L

C127 0.1U/16V_4 C128 0.1U/16V_4

PCIE_WAKE# 4,28,30,31
PLTRST# 4,16,26,28,30,31
PCIE_RXN9_LAN 12
PCIE_RXP9_LAN 12

RTL8161GSH-CG

FOR GIGA: 8161GSH: AL008161004 (Default)
FOR 10/100: 8176EH: AL008176000

MDI3+ MDI3-

+3V_LAN

PCIE_CLKREQ_LAN# R167 *0_4/S LAN_CLKRQ

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN9_LAN PCIE_TXP9_LAN

CLK_PCIE_LANN 13
CLK_PCIE_LANP 13
PCIE_TXN9_LAN 12
PCIE_TXP9_LAN 12

10/100 only

U16

MDI1-_1 MDI1+_1 LAN_MCT2 MDI0-_1 MDI0+_1 LAN_MCT1

TD+ TD- CT RD+ RD- CT

TX+ CMT TX- RX- CT RX+

MDI1- V_DAC MDI1+ MDI0+ V_DAC MDI0-

*NS681684

BOT: DB0LE6LAN00
FCE: DB0LE6LAN20

Reserve for Reltek FAE request.

+3V_LAN

+3VLANVCC

C117 0.1U/16V_4 C217 0.1U/16V_4 C214 *0.1U/16V_4 C459 *4.7U/6.3V_6 C116 *4.7U/6.3V_6

close to each VDD33 pin-- 11, 32

Place Cc and Cd close to each VDD33 pin-- 23

C202 4.7U/6.3V_6 Cc

C457 0.1U/16V_4 Cd

Remove For Not Using SWR mode

2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,25,26,27,29,30,31,37,39

39 +3V +3VLANVCC

Giga only

Swap pin for Layout

U18

MDI2+ MDI2- MDI3- MDI3+ MDI0+ MDI0- MDI1+ MDI1-

TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-

MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-

MDI2+_1 MDI2-_1 MDI3-_1 MDI3+_1 MDI0+_1 MDI0-_1 MDI1+_1 MDI1-_1

V_DAC V_DAC V_DAC V_DAC

TCT1 TCT2 TCT3 TCT4

MCT1 MCT2 MCT3 MCT4

LAN_MCT1 LAN_MCT2 LAN_MCT3 LAN_MCT4

75_4 R217 R155 R205 R204

C102 0.01U/50V_4

NS892407

Stuff for Giga only

BOT: DB0Z06LAN00
FCE: DB0LL1LAN00 (Default)

C433 10P/3KV_1808

LAN conn

RJ45

CN18

LAN_AMBLED LAN_AMBLED# (Amber)

LED_AMBER_P LED_AMBER_N

MDI3-_1 MDI3+_1 MDI1-_1 MDI2-_1 MDI2+_1 MDI1+_1 MDI0-_1 MDI0+_1

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

GND1 GND

LAN_WLED LAN_WLED# (White)

LED_WHITE_P LED_WHITE_N

R415 *0_6/S

R450 *0_6/S

RJ45_CONN

0224
Need check P/N

+3VLANVCC R161 330_4 C97 1000P/50V_4 LAN_AMBLED

+3VLANVCC R212 330_4 C224 1000P/50V_4 LAN_WLED

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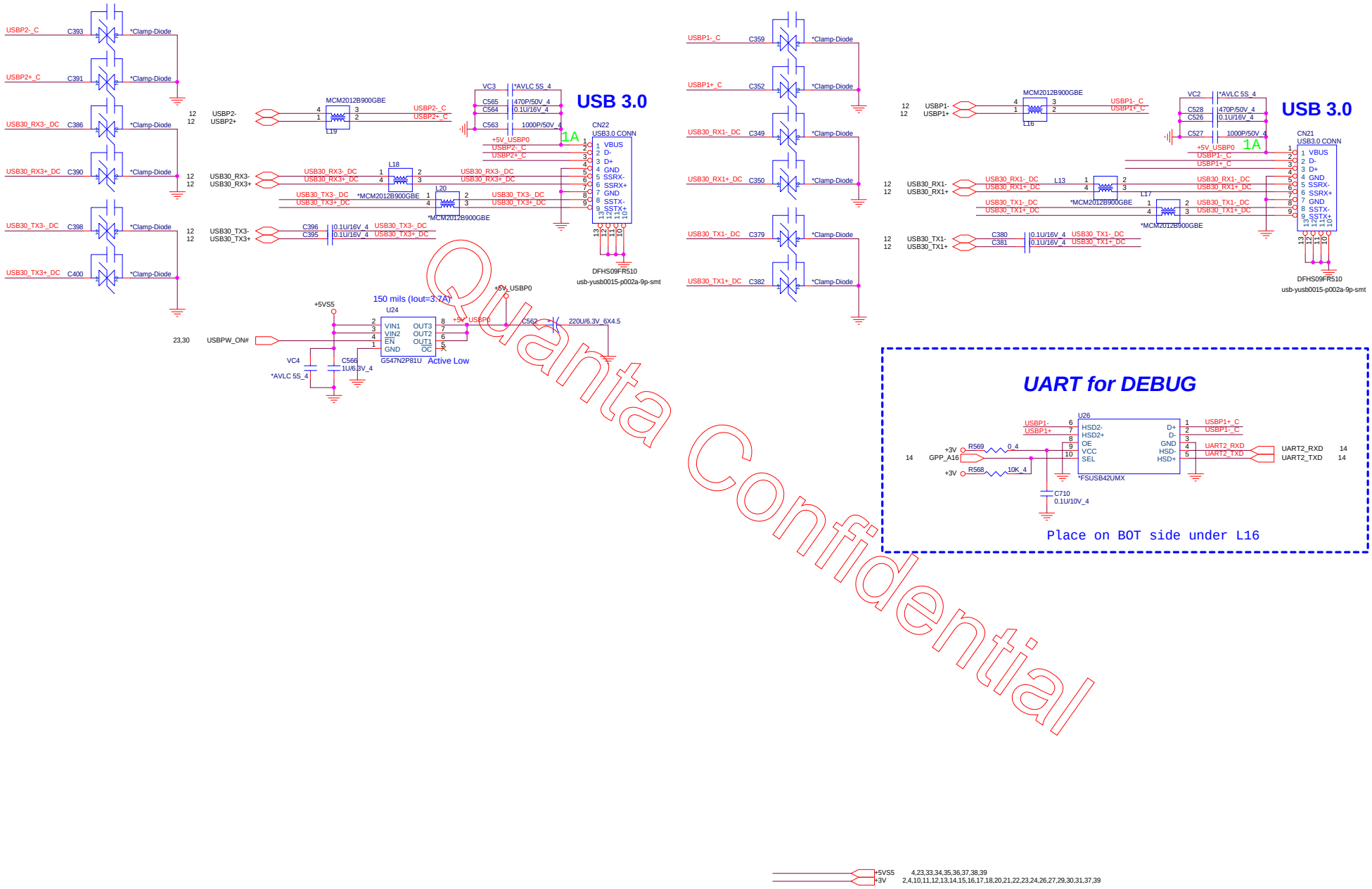
USB 2.0/3.0 Combo



UART for DEBUG

Place on BOT side under L16

+5VS5 4,23,33,34,35,36,37,38,39
+3V 2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,26,27,29,30,31,37,39

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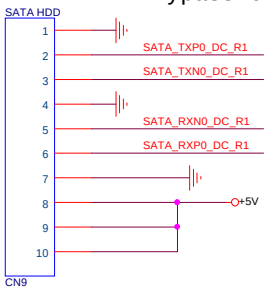
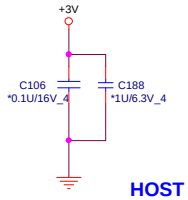
SATA HDD Connector(Cable type)

Bypass CAP close conn

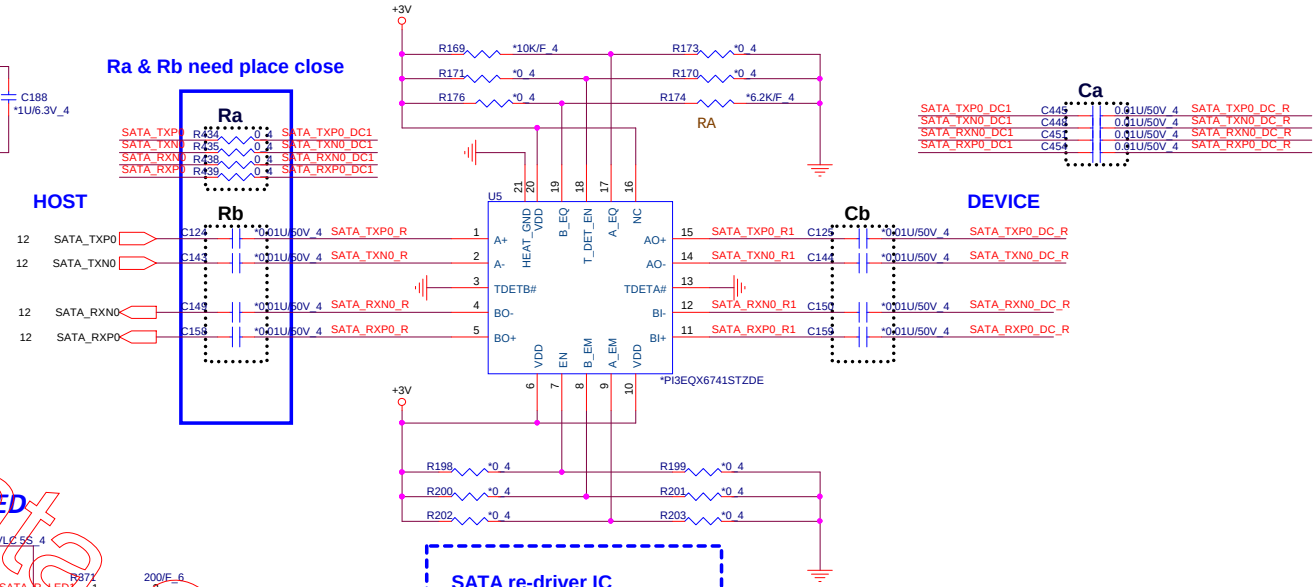




LED1	PN	
Dual Color	BEWY0009ZA0	stuff R370, unstuff R573
Single Color	BEWH0046Z00	stuff R573, unstuff R370

SATA Re-driver

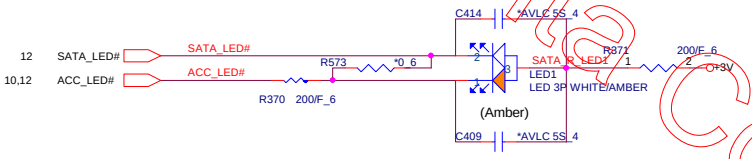
Ra & Rb need place close



SATA re-driver IC
stuff Rb,Cb , unstuff Ra,Ca

unstuff SATA re-driver IC
stuff Ra,Ca , unstuff Rb,Cb

SATA LED



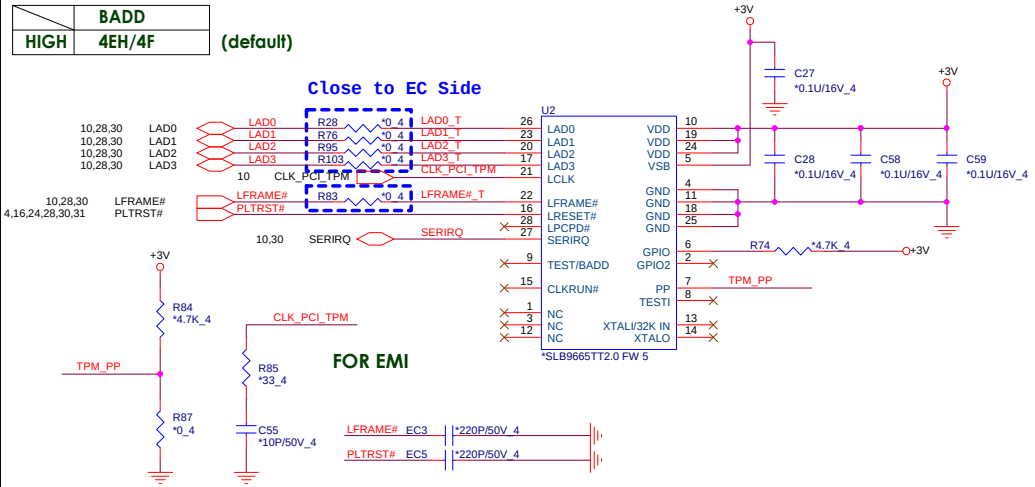
TPM (2.0)

Address

	BADD
HIGH	4EH/4F

(default)

Close to EC Side



2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,27,29,30,31,37,39 +3V
21,22,23,27,39 +5V

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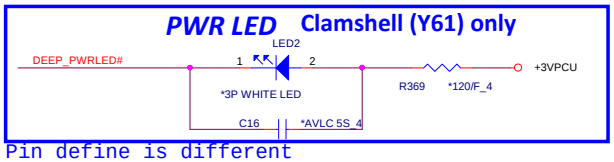
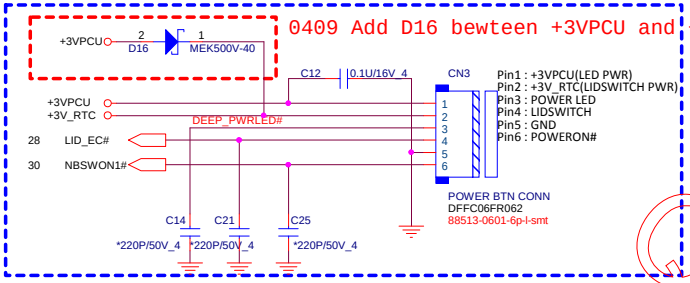
Power Botton Connector

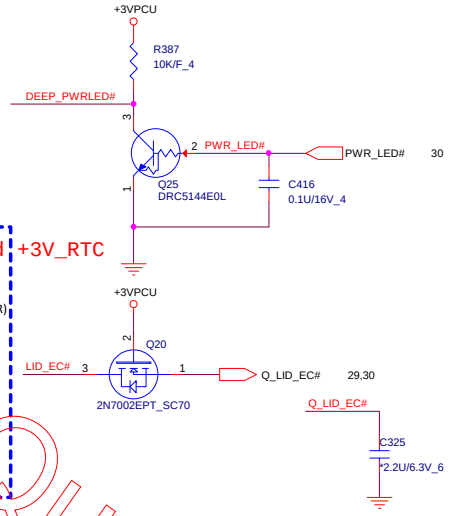
PWR LED Clamshell (Y61) only



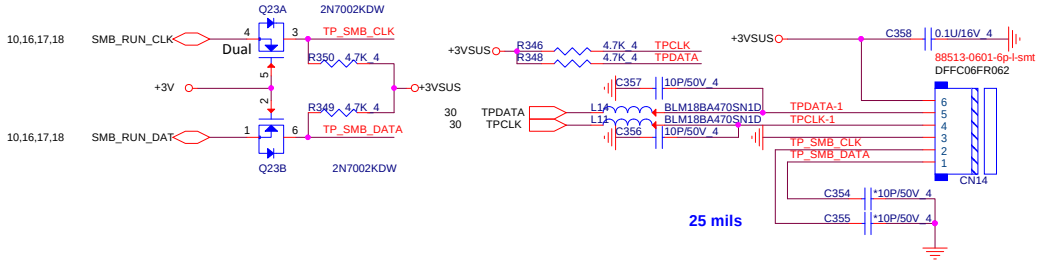
Pin define is different
Power Board does not shared with Y6x !!

0409 Add D16 bewteen +3VPCU and +3V_RTC

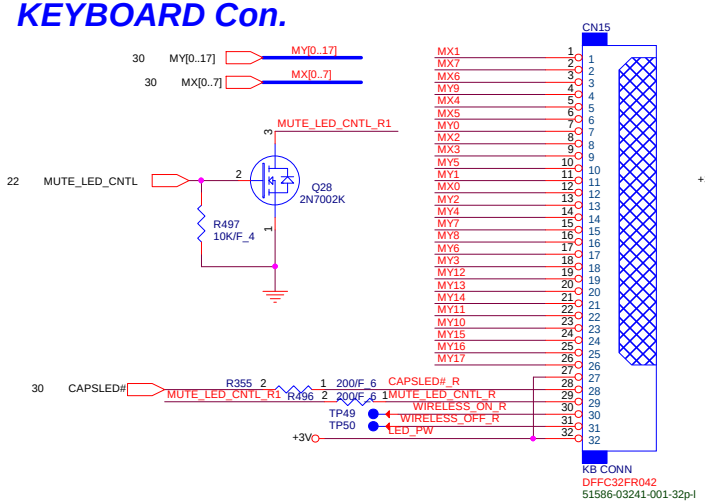




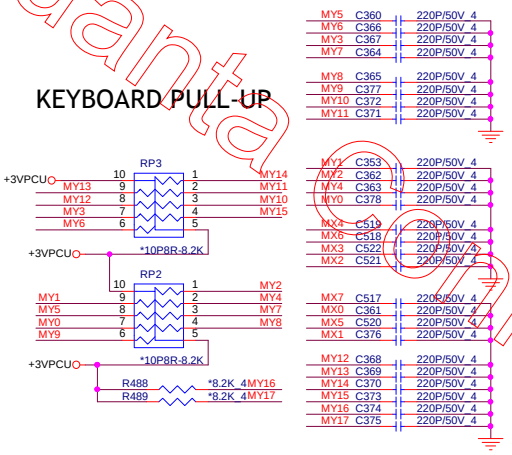
Touch Pad Connector



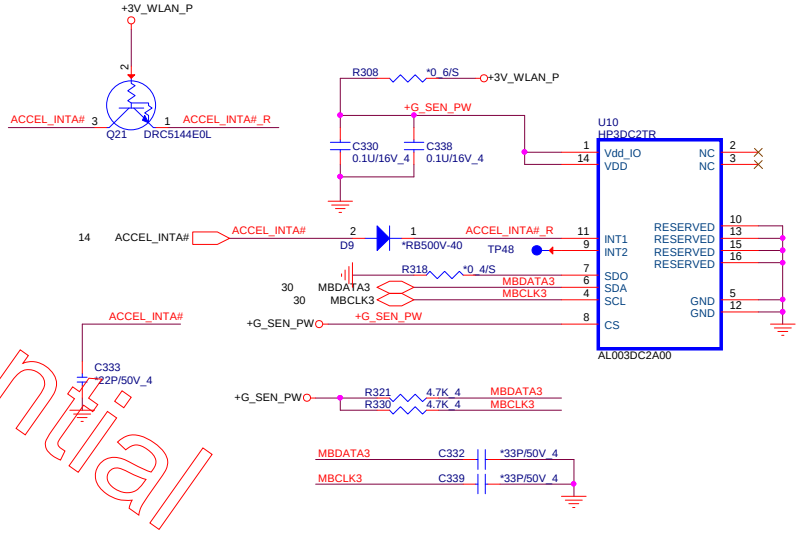
KEYBOARD Con.



KEYBOARD PULL-UP

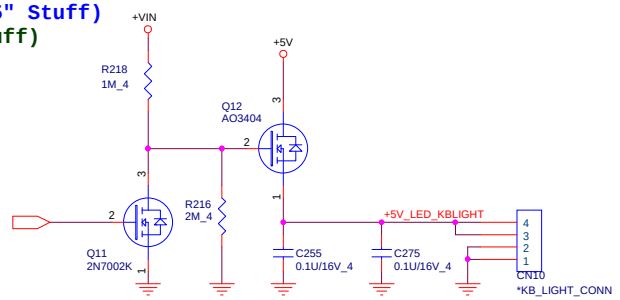


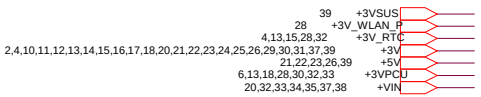
Accelerometer Sensor



15" KB backlight only

(Default 15" Stuff)
(13" Un-Stuff)





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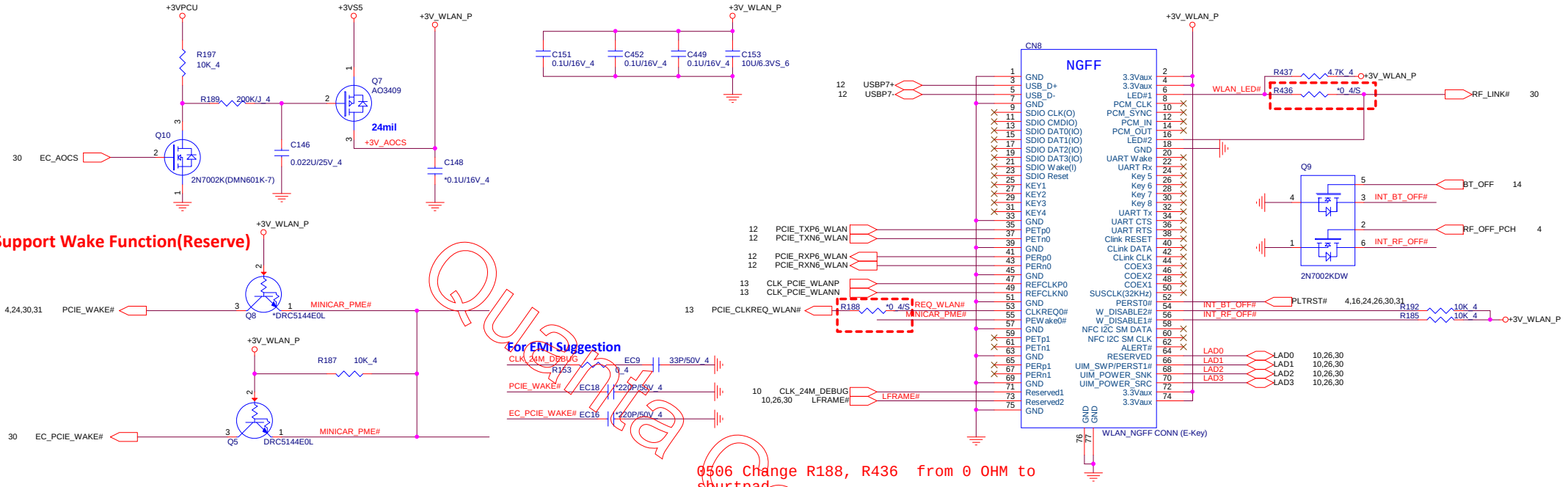
Mini Card
WLAN/BT(Option)

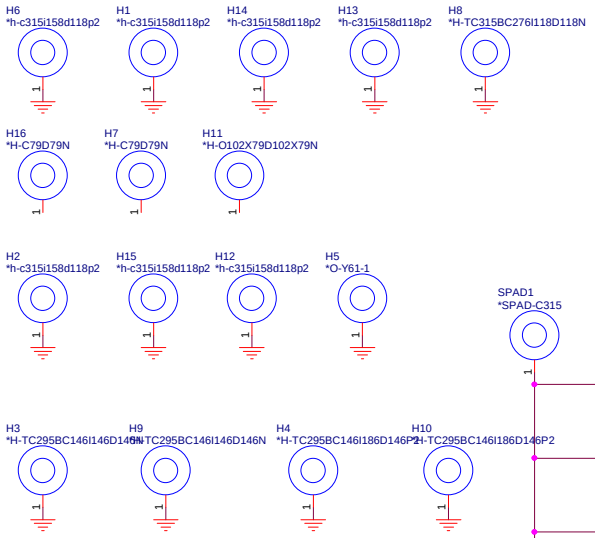


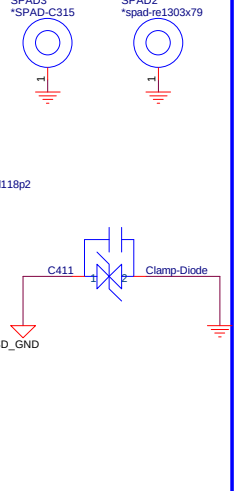
Support Wake Function(Reserve)

0506 Change R188, R436 from 0 OHM to shurtpad

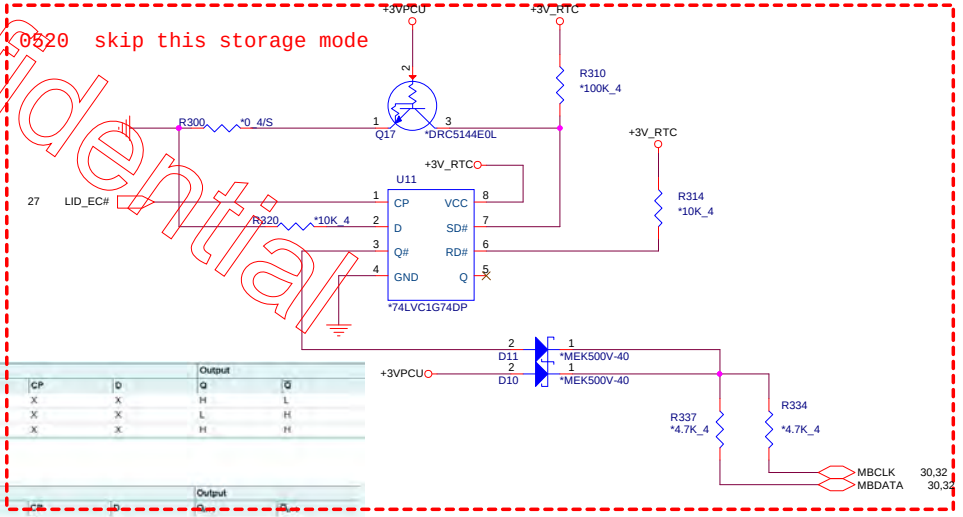
Quanta Confidential

Hole





0520 skip this storage mode



Input				Output	
SD	RD	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output	
SD	RD	CP	D	Q	Q
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition

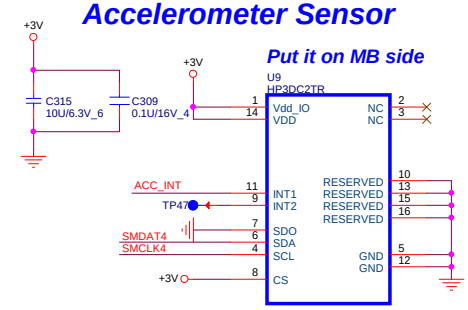
4,10,15,16,29,30,33,35,36,39 +3VSS
27 +3V_WLAN_P
4,13,15,27,32 +3V_RTC
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39 +3V
21,22,23,26,27,39 +5V
6,13,18,27,30,32,33 +3VPCU

PROJECT : Y62P/Y63P
Quanta Computer Inc.

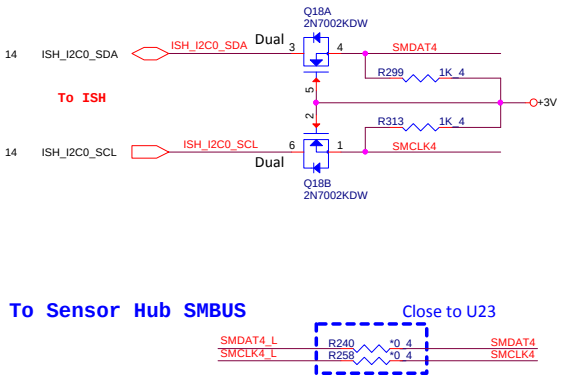
Size	Document Number	Rev
Custom	WLAN/G-Sensor/G-CLK/TS	1A
Date: Wednesday, May 20, 2015	Sheet 28of 42	

Accelerometer Sensor

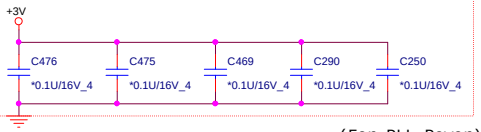
Put it on MB side



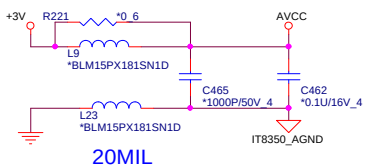
Close to U9



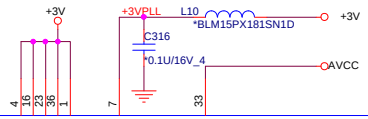
Note: Place all capacitors close to IT8350.

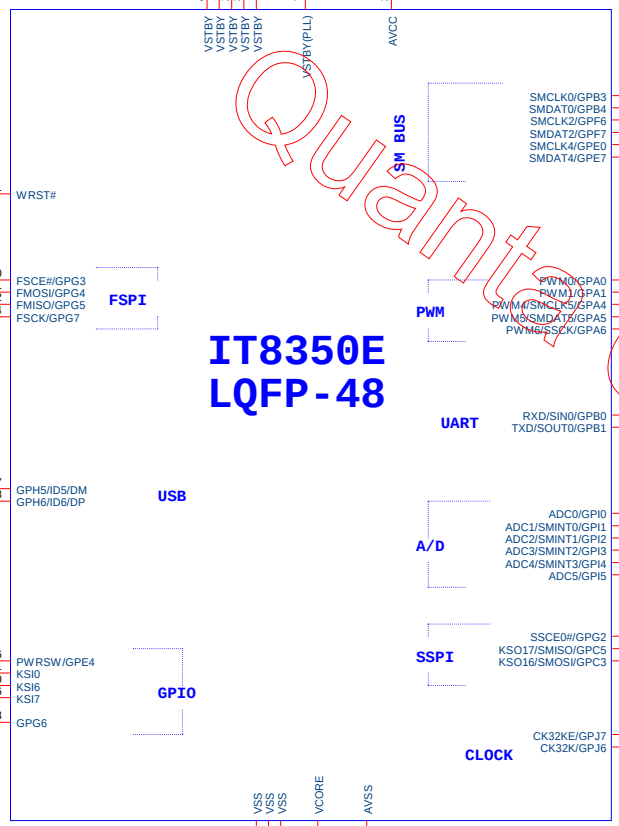


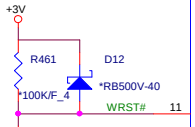
20MIL

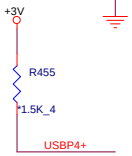


20MIL 10MIL (For PLL Power)

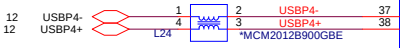


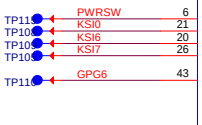


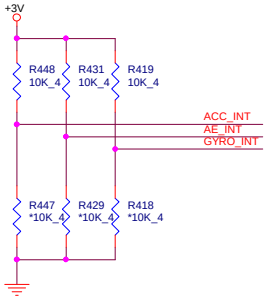


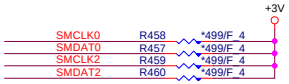


USB for Host

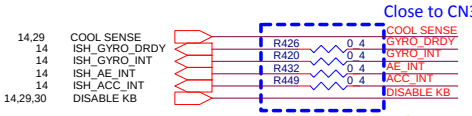


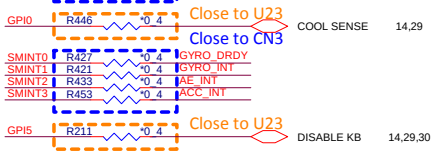


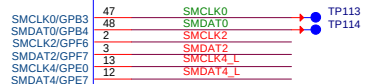




Close to CN3







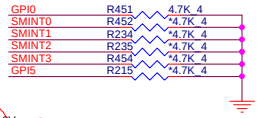
Reserved SMBus channel 0 for debugging & updating FW

Reserved

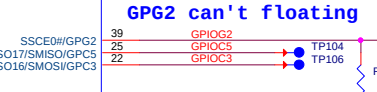
SMbus channel 4 for connecting the Sensor (G-sensor)

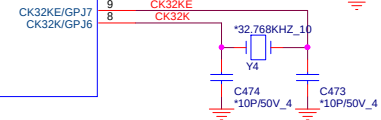
Reserved TX/RX for debugging

if no use ADC function,
please pull down to GND
SMINTx for sensor interrupt

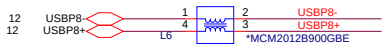


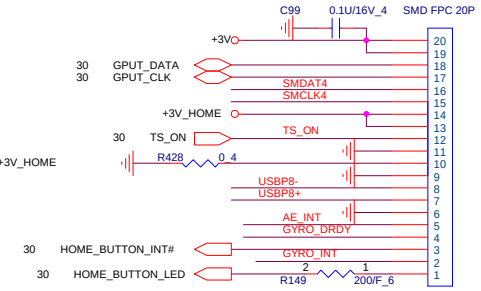
GPG2 can't floating





External crystal is must be item
when USB func. is used !



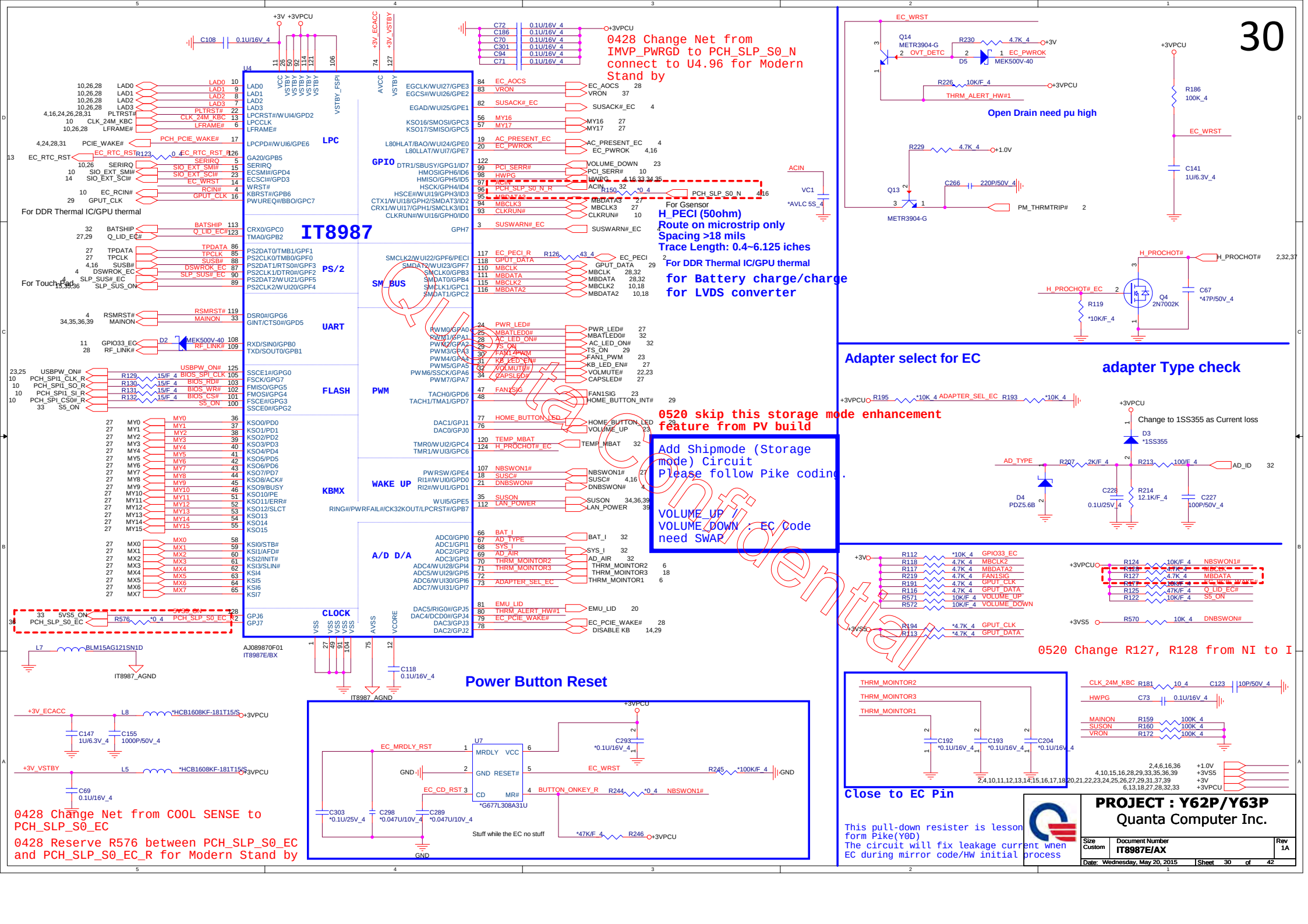


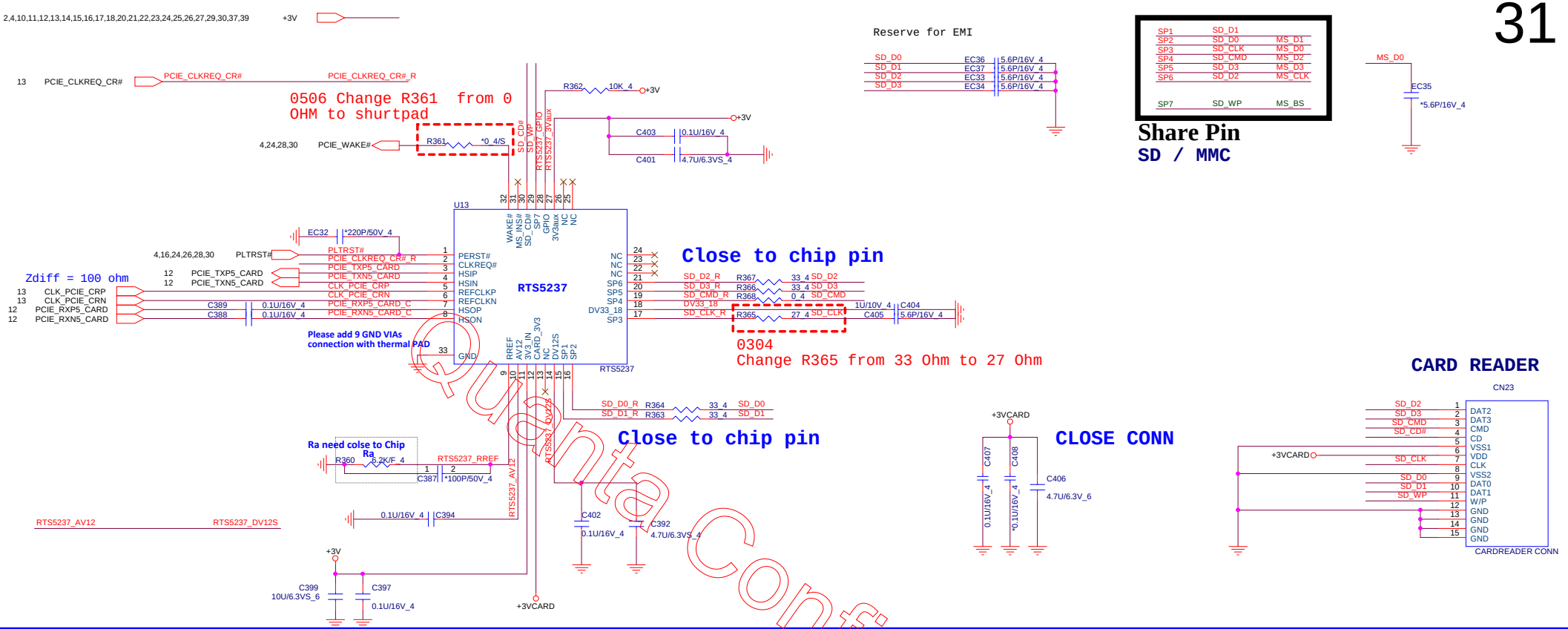
0415 Del TS Co-Lay CN6

32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

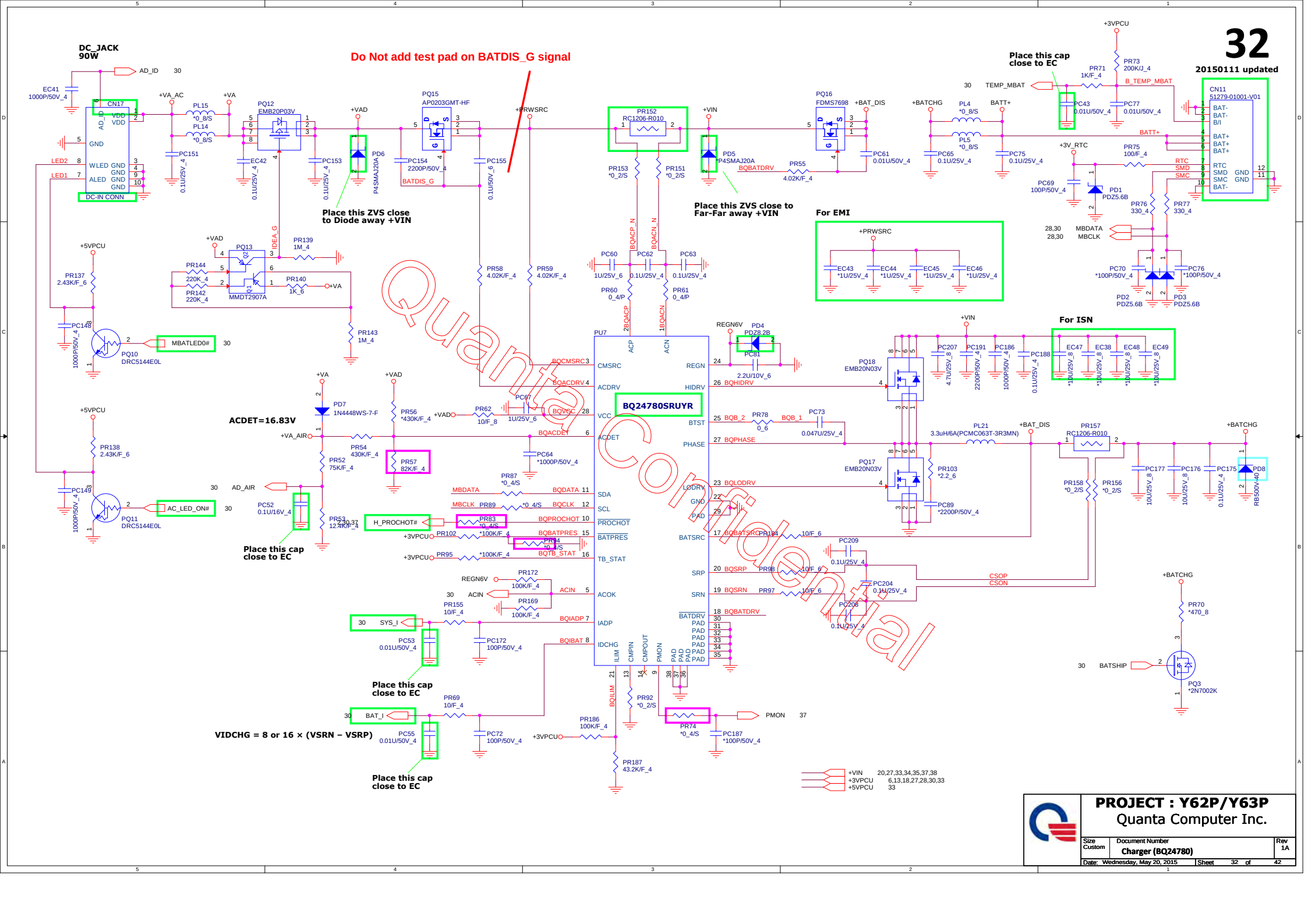
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ITE8350/HP9DS0/HP3DC2	1A
Date: Wednesday, May 20, 2015	Sheet 29 of 42	


IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
0428 Change Net from IMVP_PWRGD to PCH_SLP_S0_N connect to U4.96 for Modern Stand by
For DDR Thermal IC/GPU thermal
For Touch Pad
For Gsensor
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
For DDR Thermal IC/GPU thermal
for Battery charge/charge
for LVDS converter
0520 skip this storage mode enhancement
feature from PV build
Add Shipmode (Storage mode) Circuit
Please follow Pike coding.
VOLUME_UP / VOLUME_DOWN : EC Code need SWAP
Open Drain need pu high
Adapter select for EC
adapter Type check
Change to 1SS355 as Current loss
0520 Change R127, R128 from NI to I
Power Button Reset
0428 Change Net from COOL SENSE to PCH_SLP_S0_EC
0428 Reserve R576 between PCH_SLP_S0_EC and PCH_SLP_S0_EC_R for Modern Stand by
Close to EC Pin
This pull-down resister is lesson form Pike(Y0D)
The circuit will fix leakage current when EC during mirror code/HW initial process
Quanta Confidential
PROJECT : Y62P/Y63P
Quanta Computer Inc.
Size Custom
Document Number IT8987E/AX
Rev 1A
Date: Wednesday, May 20, 2015
Sheet 30 of 42



PROJECT : Y62P/Y63P Quanta Computer Inc.		
Size: Custom	Document Number: CR RTS5237 & HOLE	Rev: 1A
Date: Wednesday, May 20, 2015	Sheet 31 of 42	

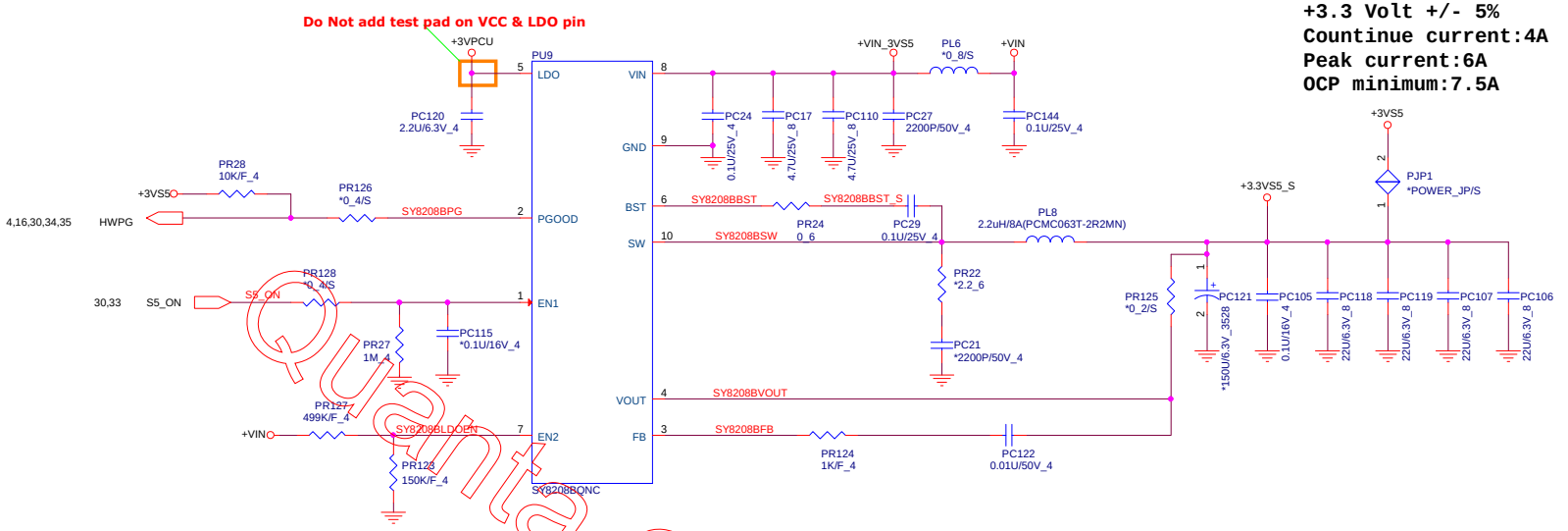

32
20150111 updated
DC_JACK
90W
Do Not add test pad on BATDIS_G signal
Place this cap close to EC
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
For EMI
For ISN
ACDET=16.83V
VIDCHG = 8 or 16 × (VSRN – VSRP)
BQ24780SRUYR
Quanta Confidential
PROJECT : Y62P/Y63P
Quanta Computer Inc.
Charger (BQ24780)
Wednesday, May 20, 2015
Sheet 32 of 42

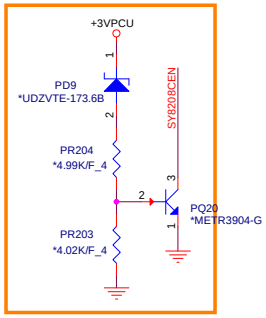
DC/DC +3VS5/+5VS5

+3VS5 4,10,15,16,28,29,30,35,36,39
+5VS5 4,23,25,34,35,36,37,38,39

Do Not add test pad on VCC & LDO pin

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

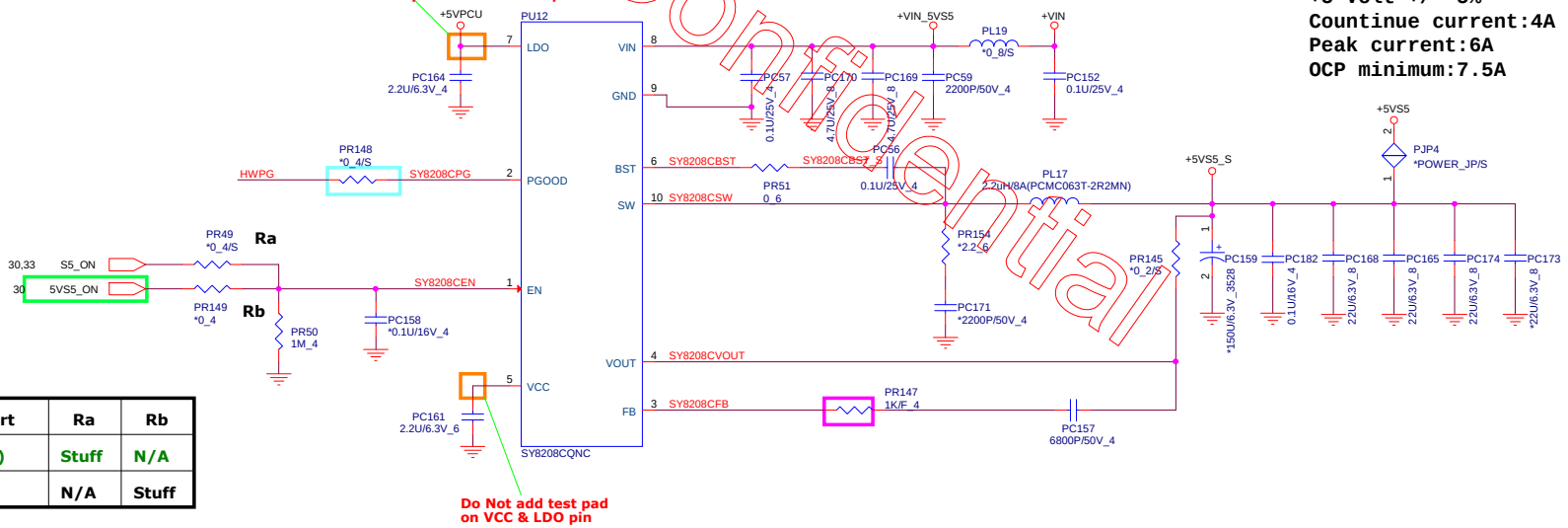




2014/12/17 updated

Do Not add test pad on VCC & LDO pin

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

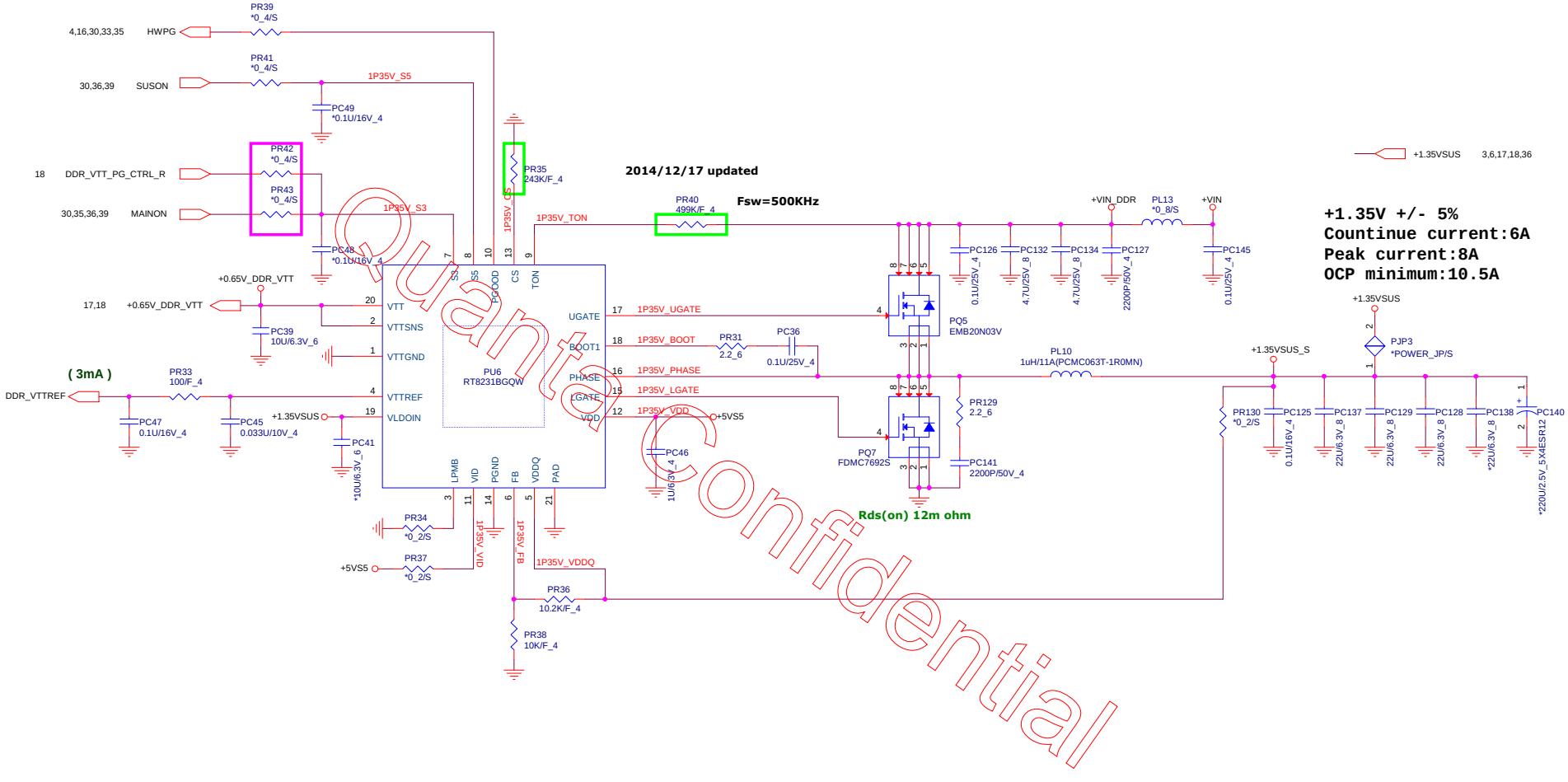


Do Not add test pad on VCC & LDO pin

USB charge support	Ra	Rb
Napa (No support)	Stuff	N/A
Whisky (Support)	N/A	Stuff

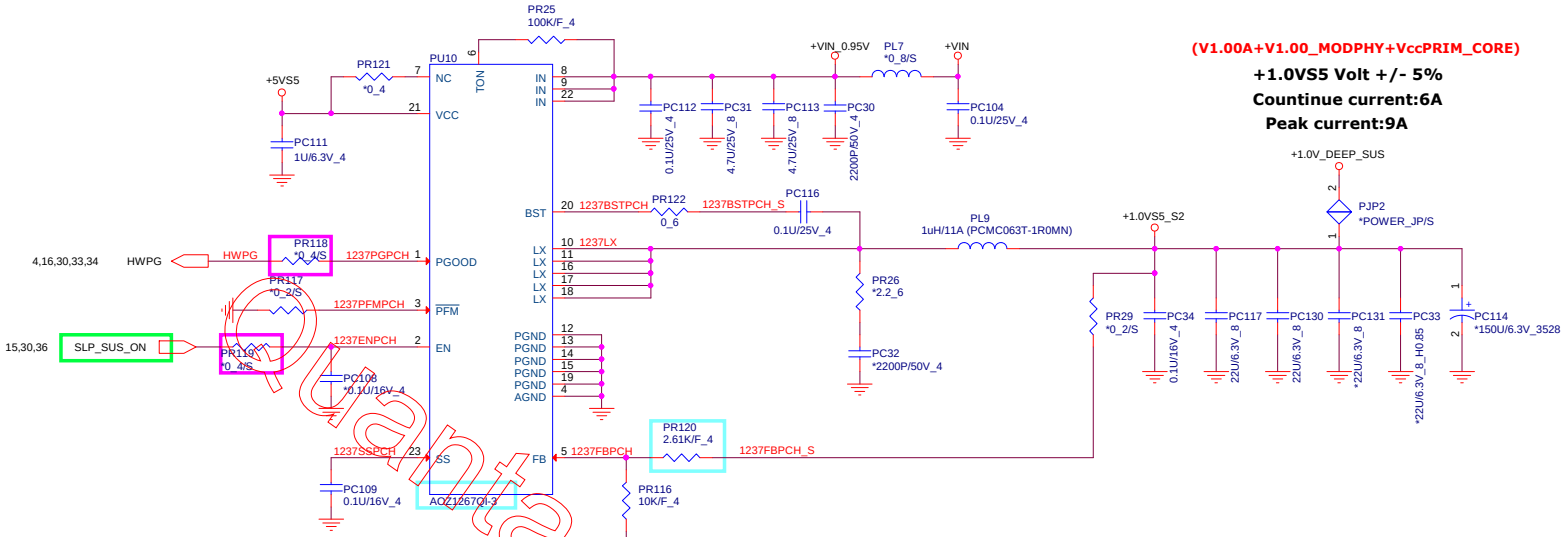
PROJECT : Y62P/Y63P
Quanta Computer Inc.

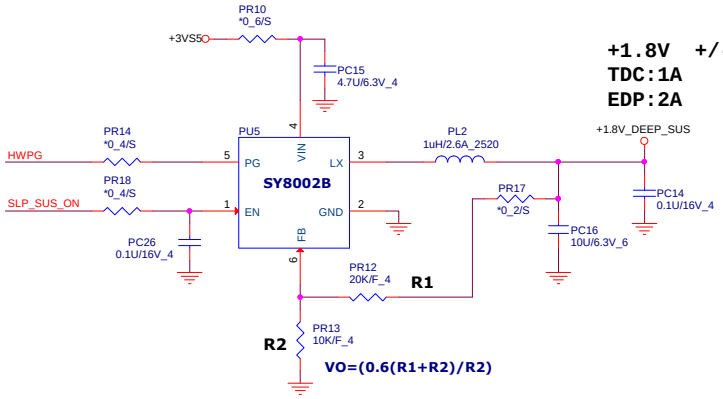
Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Wednesday, May 20, 2015	Sheet 33 of 42	



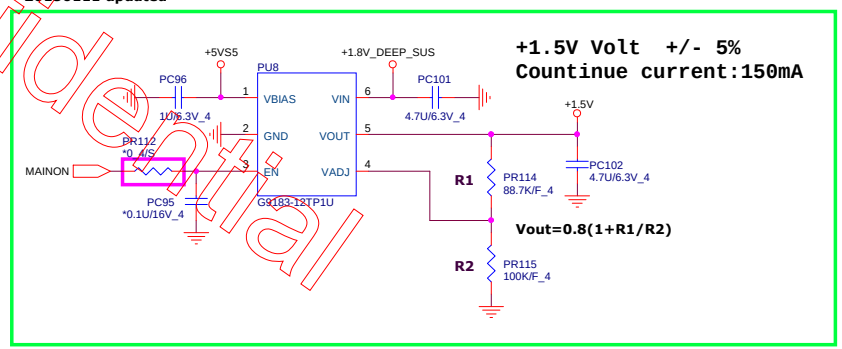
	PROJECT : Y62P/Y63P Quanta Computer Inc.	
Size Custom	Document Number DDR3 (RT8231B)	Rev 1A
Date: Wednesday, May 20, 2015	Sheet 34 of 42	

+VIN 20,27,32,33,34,37,38
+3VS5 4,10,15,16,28,29,30,33,36,39
+5VS5 4,23,25,33,34,36,37,38,39
+1.0V_DEEP_SUS 9,13,15,16,36
+1.8V_DEEP_SUS 9,15





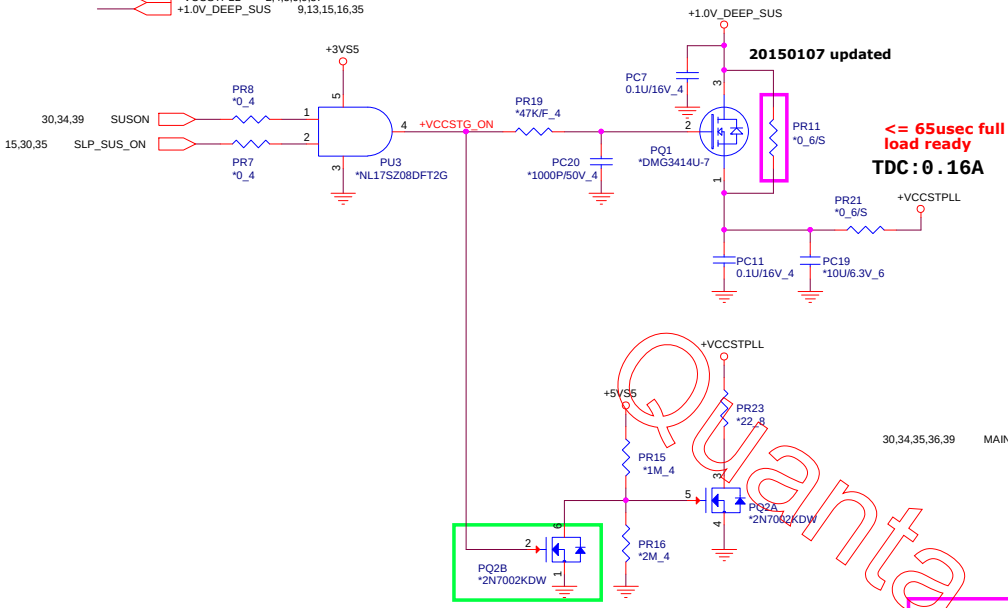
20150111 updated

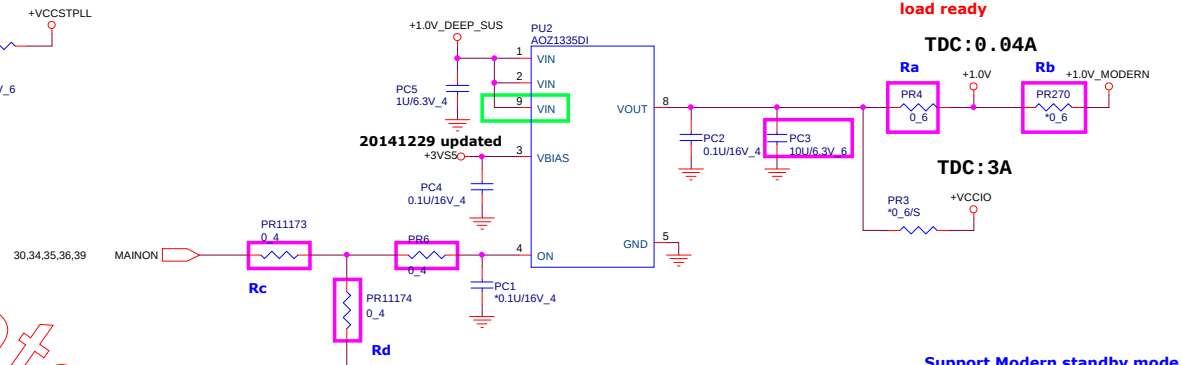


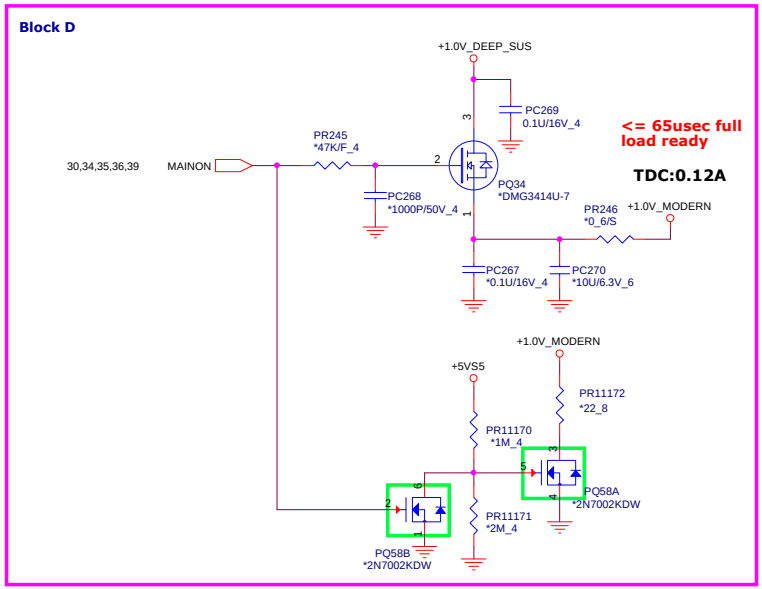
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Wednesday, May 20, 2015	Sheet 35 of 42	

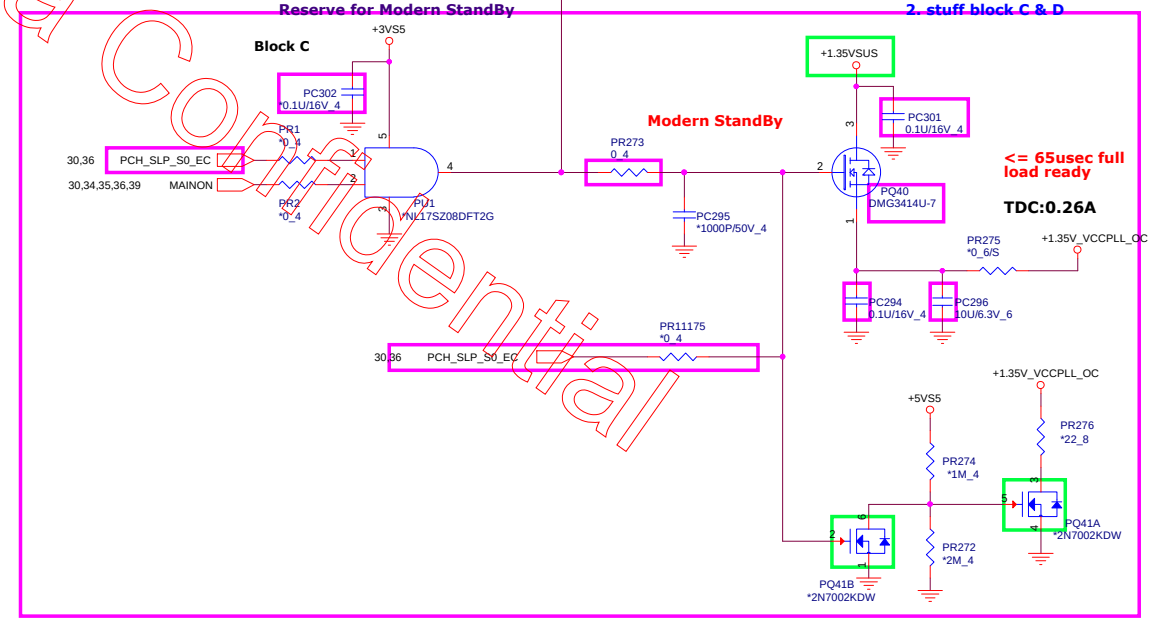
+1.0V 2,4,6,16,30
+3VS5 4,10,15,16,28,29,30,33,35,39
+5VS5 4,23,25,33,34,35,37,38,39
+VCCIO 2,6,16
+VCCSTPLL 2,4,5,6,9,37
+1.0V_DEEP_SUS 9,13,15,16,35







Reserve for Modern StandBy



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
Date: Wednesday, May 20, 2015	Sheet 36 of 42	

CPU CORE
TDC:25A
EDP:40A

VCCGT
TDC:22A
EDP:45A

DCR=0.48m ohm

Place close to VCORE Inductor

Place close to VCCSA Inductor

Place close to GT1 Inductor

place close to GT MOSFET

place close to VCORE MOSFET

program IccMax_2ph

PU14 NCP81206

PQ14 FDMS7698

PQ9 FDMS0308AS

PQ8 FDMS0308AS

PQ19 FDMS3664S

PQ4 FDMS3664S

PL16 0.15uH/40A(PCMB104T-R15MS0R487)

PL24 0.15uH/40A(PCMB104T-R15MS0R487)

PL22 *0_8/S

PL18 *0_8/S

For Acoustic

+VCCSTPLL
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
H_PROCHOT#

+VCC_CORE
VCC_SENSE
VSS_SENSE

+VCCSA
VCCSA_SENSE
VSSSA_SENSE

+VCCGT
VCCGT_SENSE
VSSGT_SENSE

+VIN_VCC_CORE
+VIN_VCCGT
+VIN
+3V
+5VS5

IMVP_PWRGD
VRON
PMON

PWM_SA
DRON
SWN_SA
CSN_SA

CSN_CORE
SWN_CORE
CSN_GT1
SWN_GT1

+VCC_CORE 5
+3V 2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,39
+VIN 20,27,32,33,34,35,38
+5VS5 4,23,25,33,34,35,36,38,39
+VCCSA 6,38
+VCCGT 7
+VCCSTPLL 2,4,5,6,9,36

PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU VR IC (NCP81206)	1A

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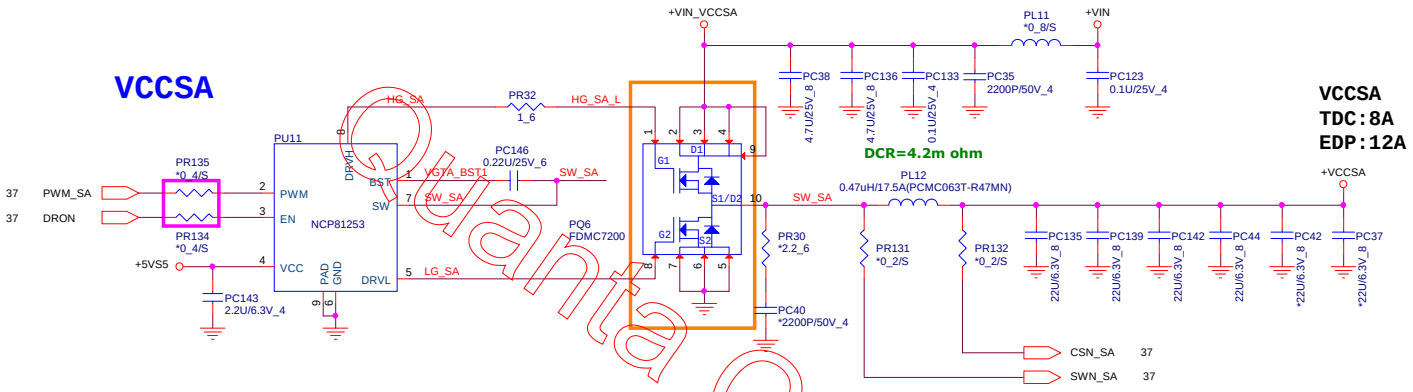
+VIN 20,27,32,33,34,35,37
+5VS5 4,23,25,33,34,35,36,37,39
+VCCSA 6,37



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	1A

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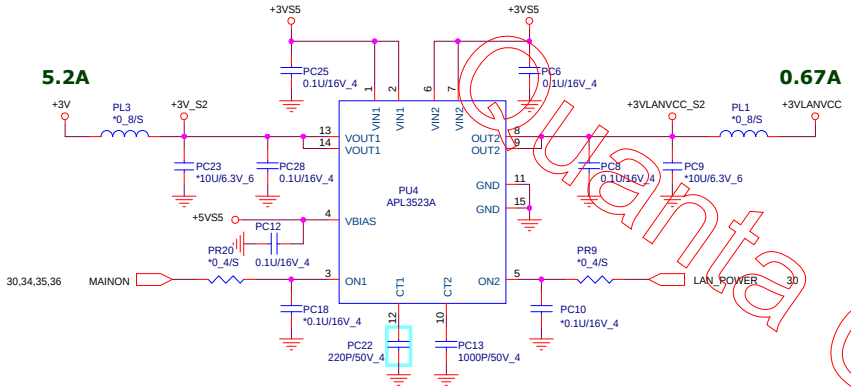
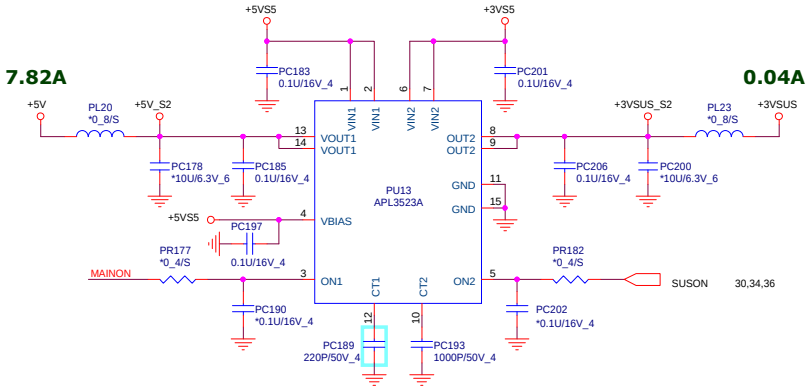


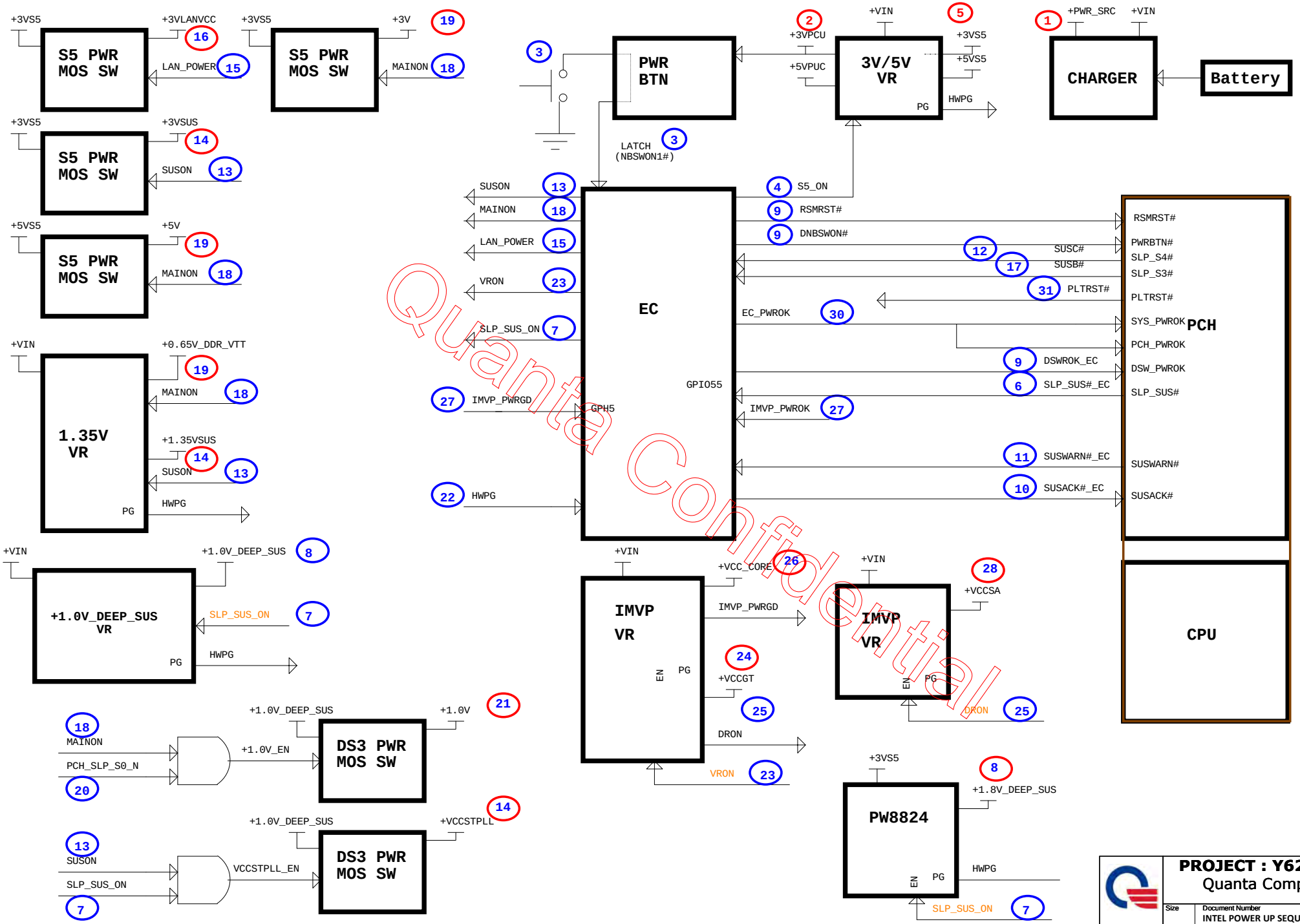


27 +3VSUS
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37 +3V
21,22,23,26,27 +5V
4,10,15,16,28,29,30,33,35,36 +3VS5
4,23,25,33,34,35,36,37,38 +5VS5
24 +3VLANVCC

PROJECT : Y62P/Y63P
Quanta Computer Inc.

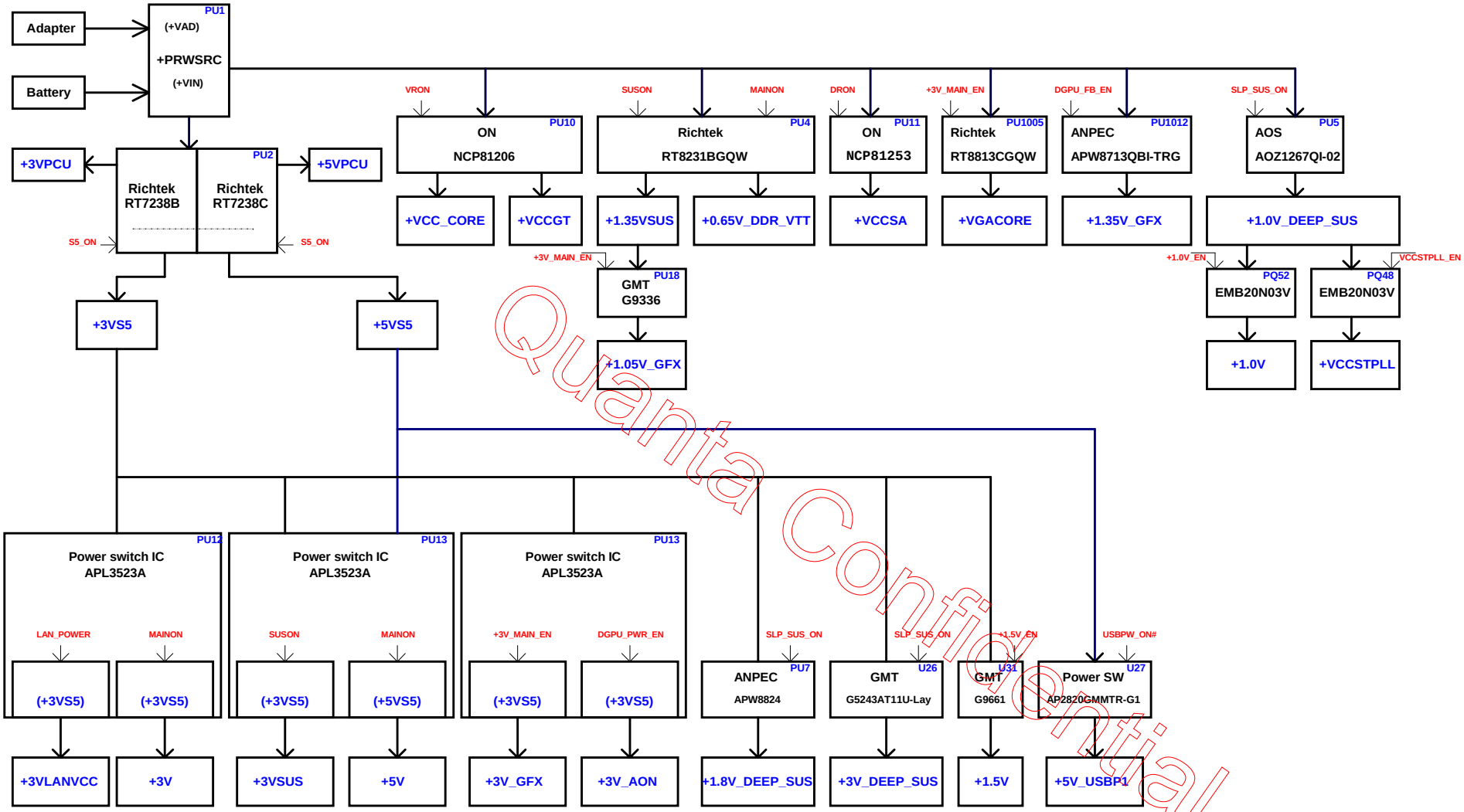
Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A

Date: Wednesday, May 20, 2015 Sheet 39 of 42



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
	INTEL POWER UP SEQUENCE	1A
Date: Wednesday, May 20, 2015	Sheet 40 of 42	



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
	Power Block Diagram	1A
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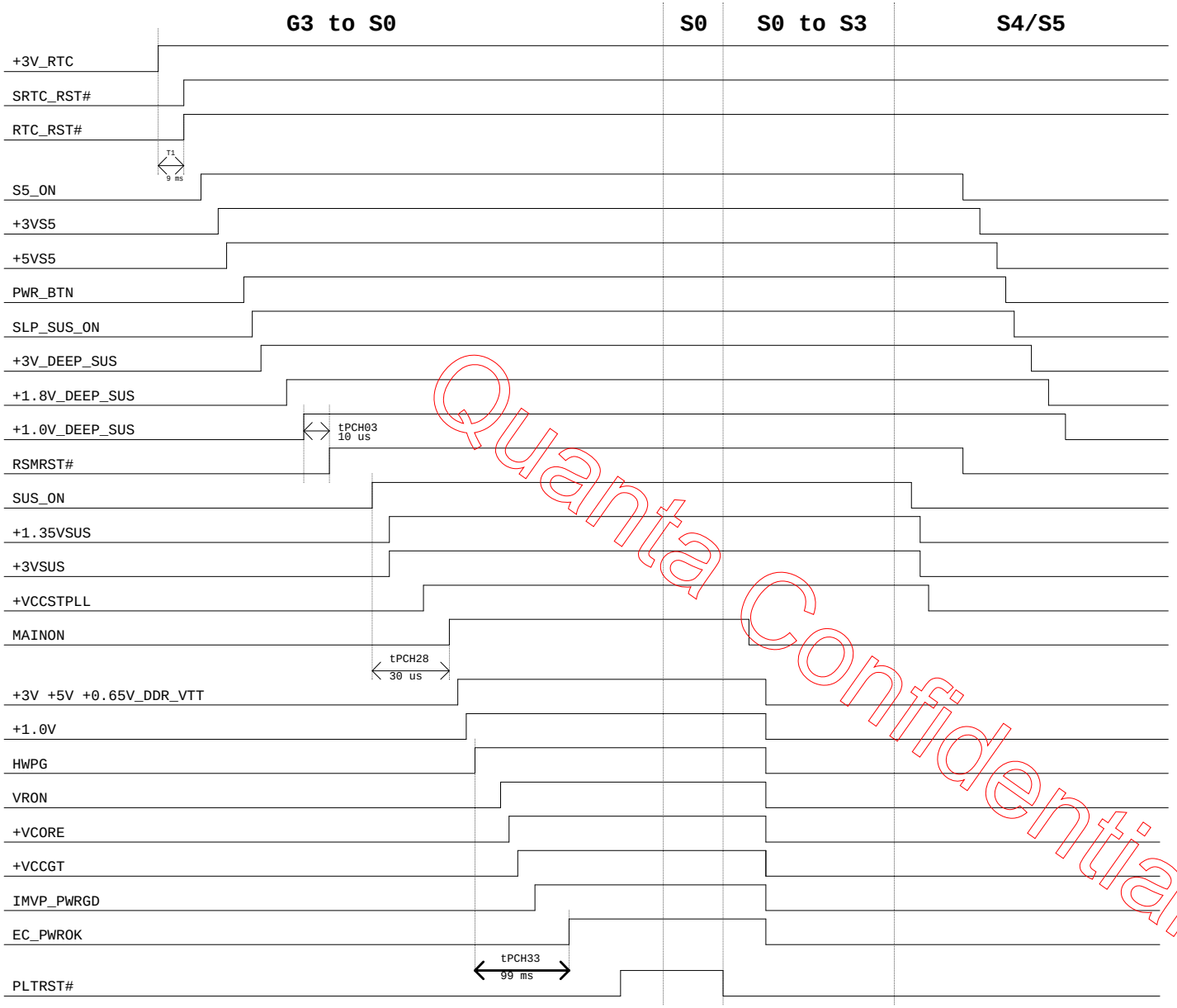

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