

MODEL NAME : *PALB0*

PCB NO : *LA-6801P ( DAB00000400 )*

BOM P/N : *46198531L01*  
*46198531L02*

# Dell/Compal Confidential

## Schematic Document

Specter (Huron River)

Sandy Bridge (PGA) + Cougar Point (standard)

DISCRETE VGA N12E-GE-B (optimus)

2010-12-06

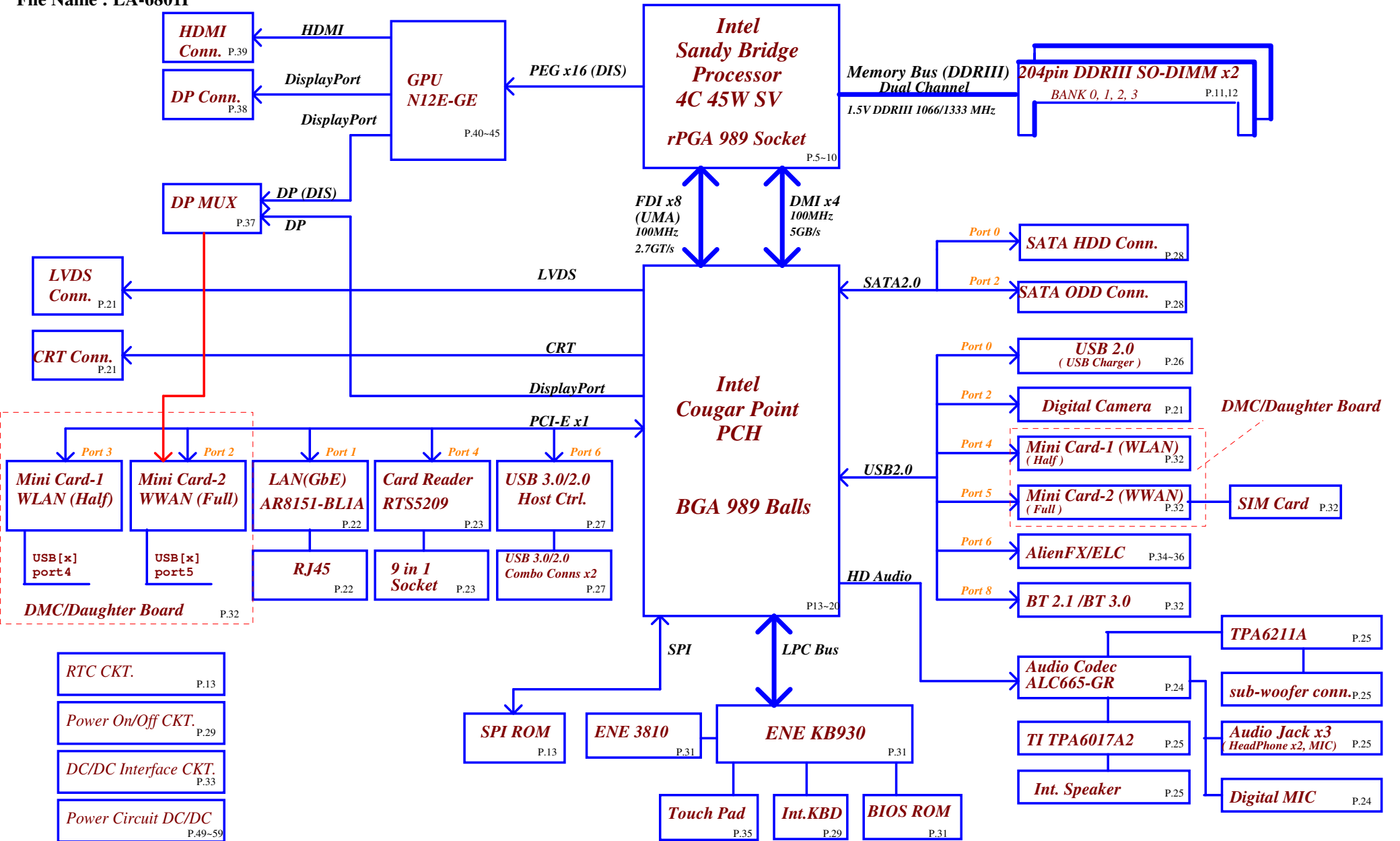
Rev: 0.3

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				<i>LA-6801P</i>	0.3
				Date: Monday, December 06, 2010	Sheet 1 of 60

Project Code : PALB0

File Name : LA-6801P

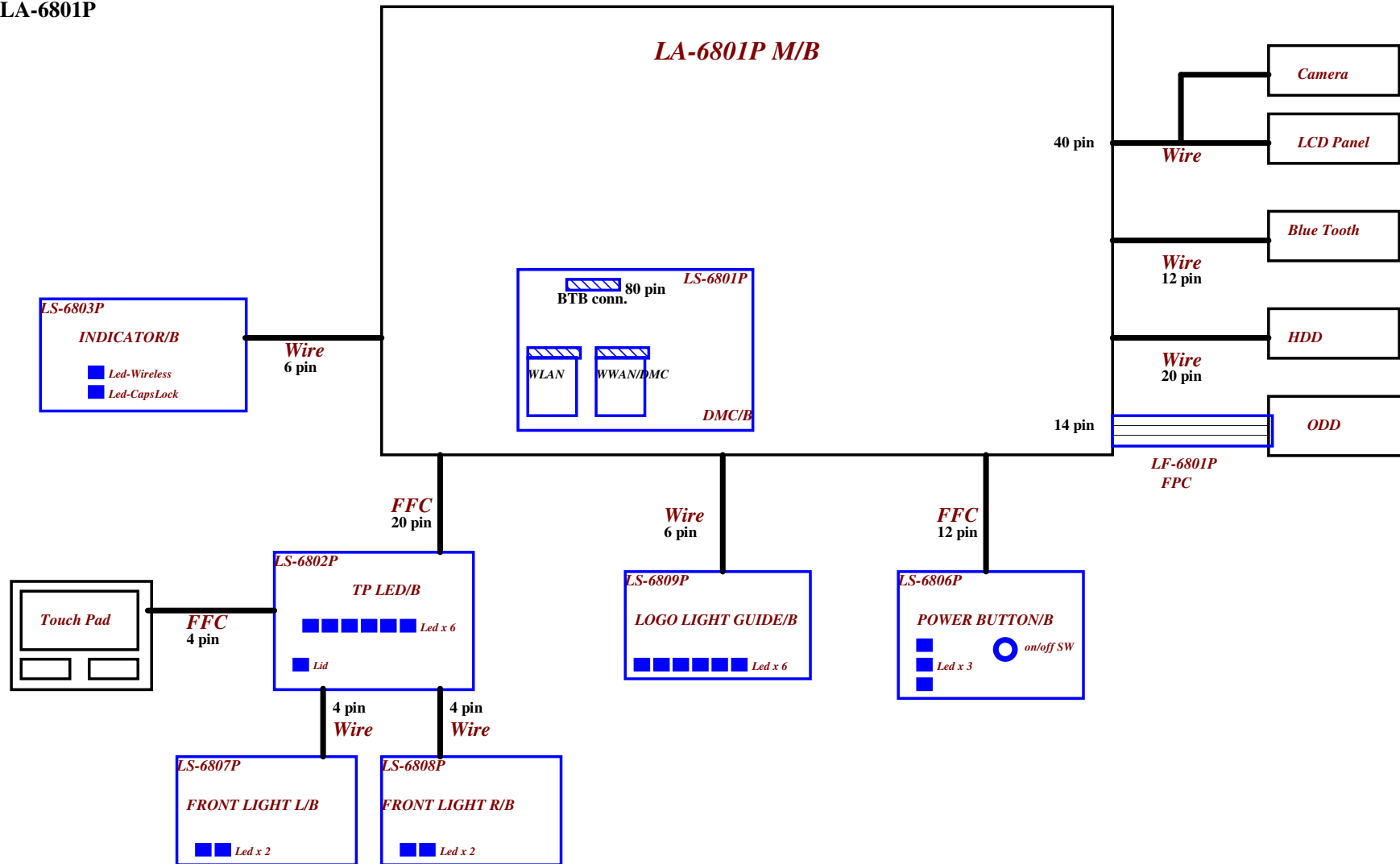
FFS P.28 Fan Control P.30 CPU XDP Conn. P.6



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Date: Monday, December 06, 2010				Rev	0.3
Sheet				2	of 60

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Date: Monday, December 06, 2010				Sheet 3	of 60

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

Link

PCH

USB PORT#	DESTINATION
0	None
1	JUSB1 (2.0 Ext Left Side)
2	Bluetooth
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN/DMC)
6	ELC 8051
7	None
8	None
9	None
10	None
11	None
12	None
13	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

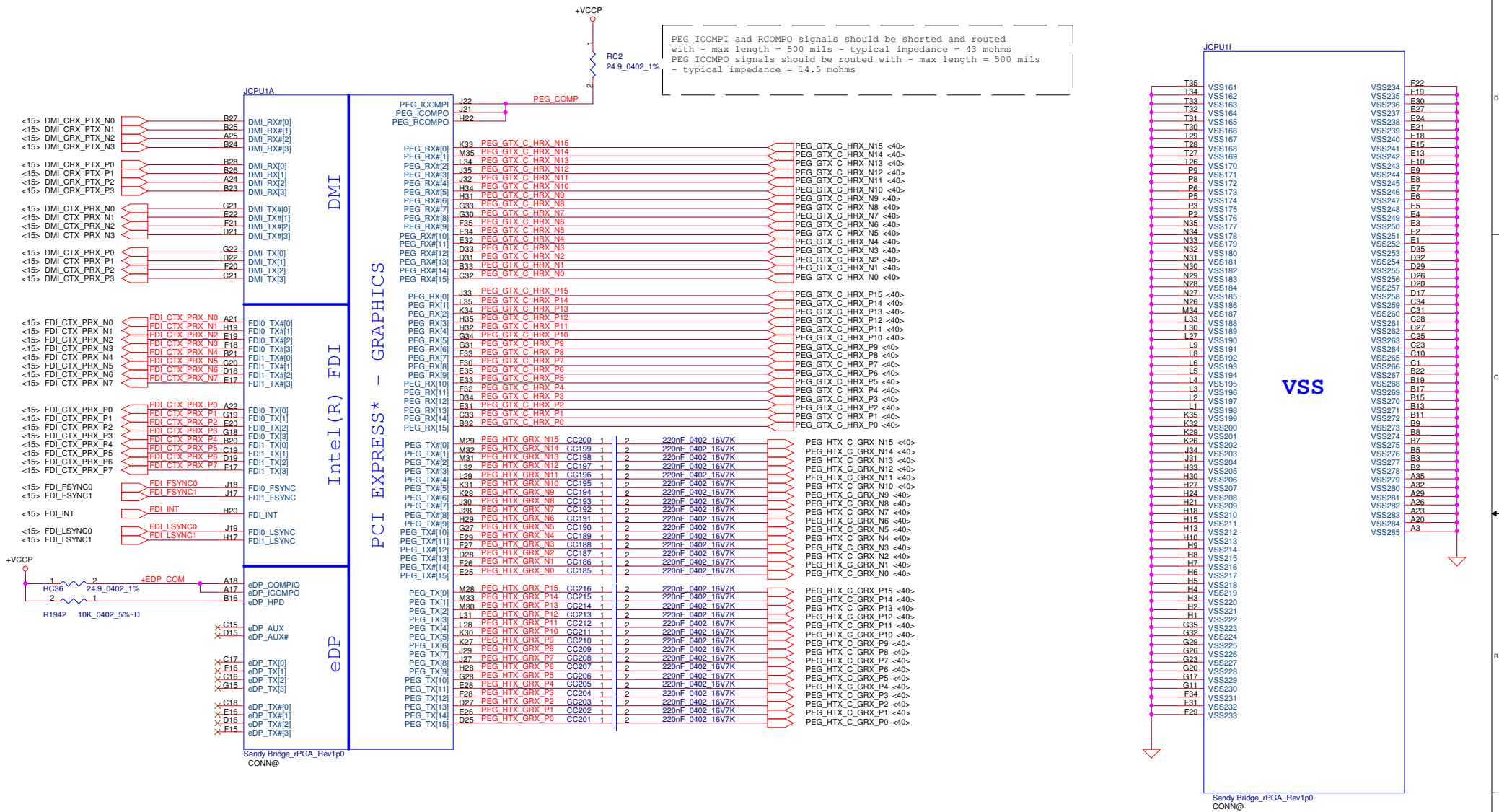


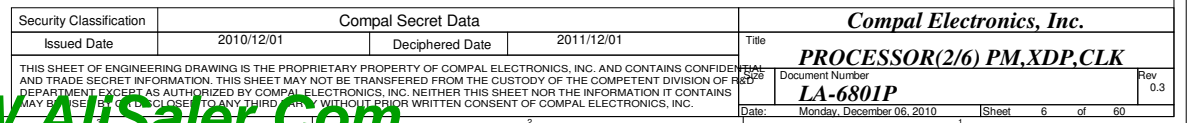
: means Digital Ground

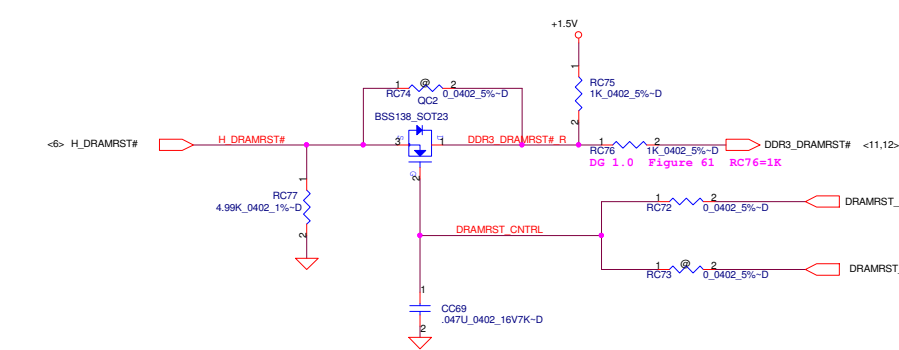
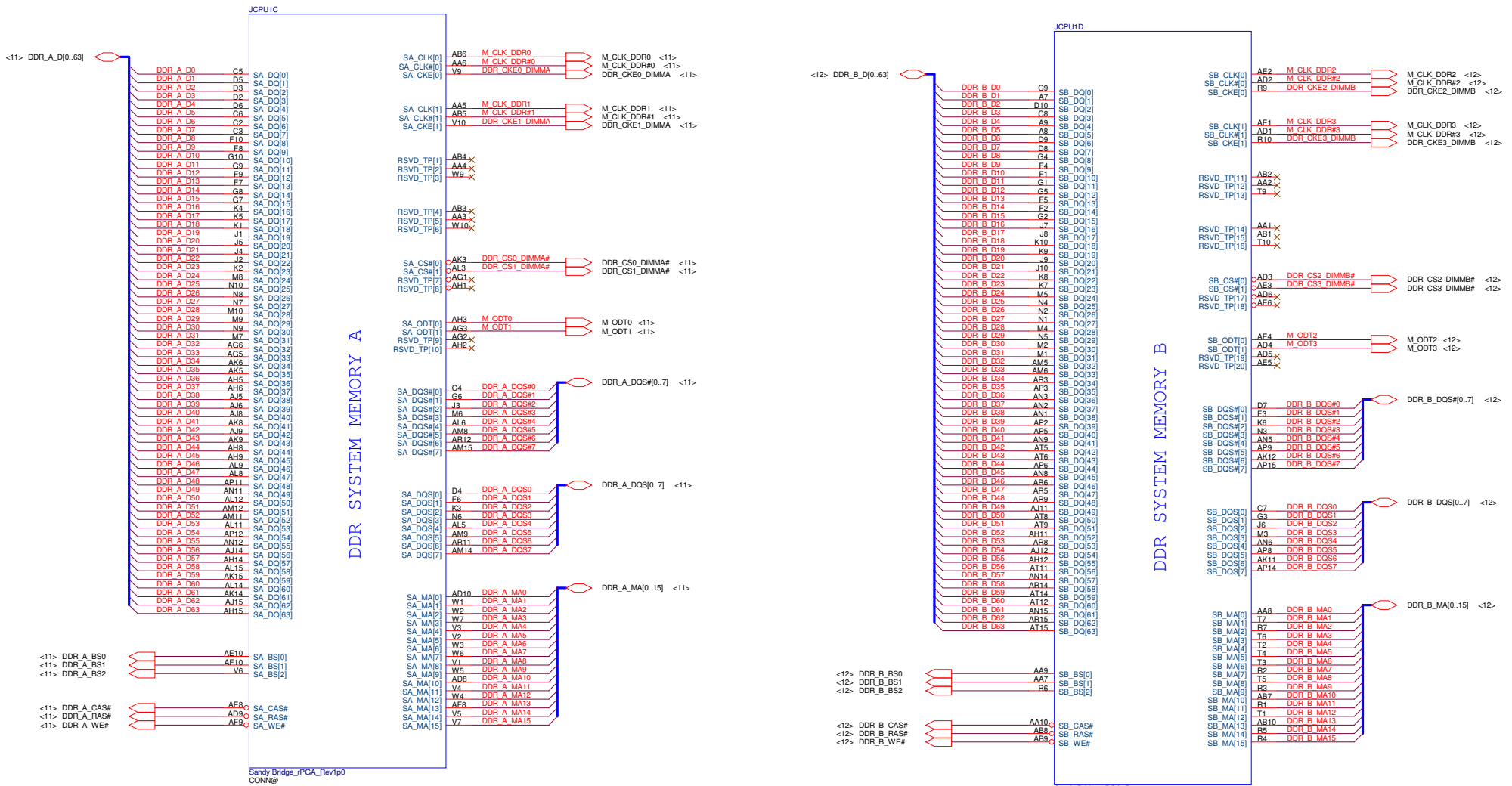


: means Analog Ground

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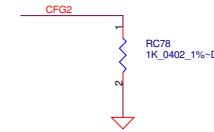




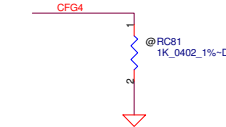
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				Rev	0.3
				Date	Monday, December 06, 2010
				Sheet	7 of 60



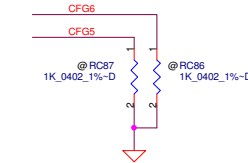
## CFG Straps for Processor



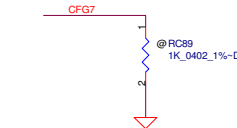
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed



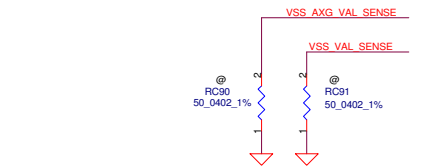
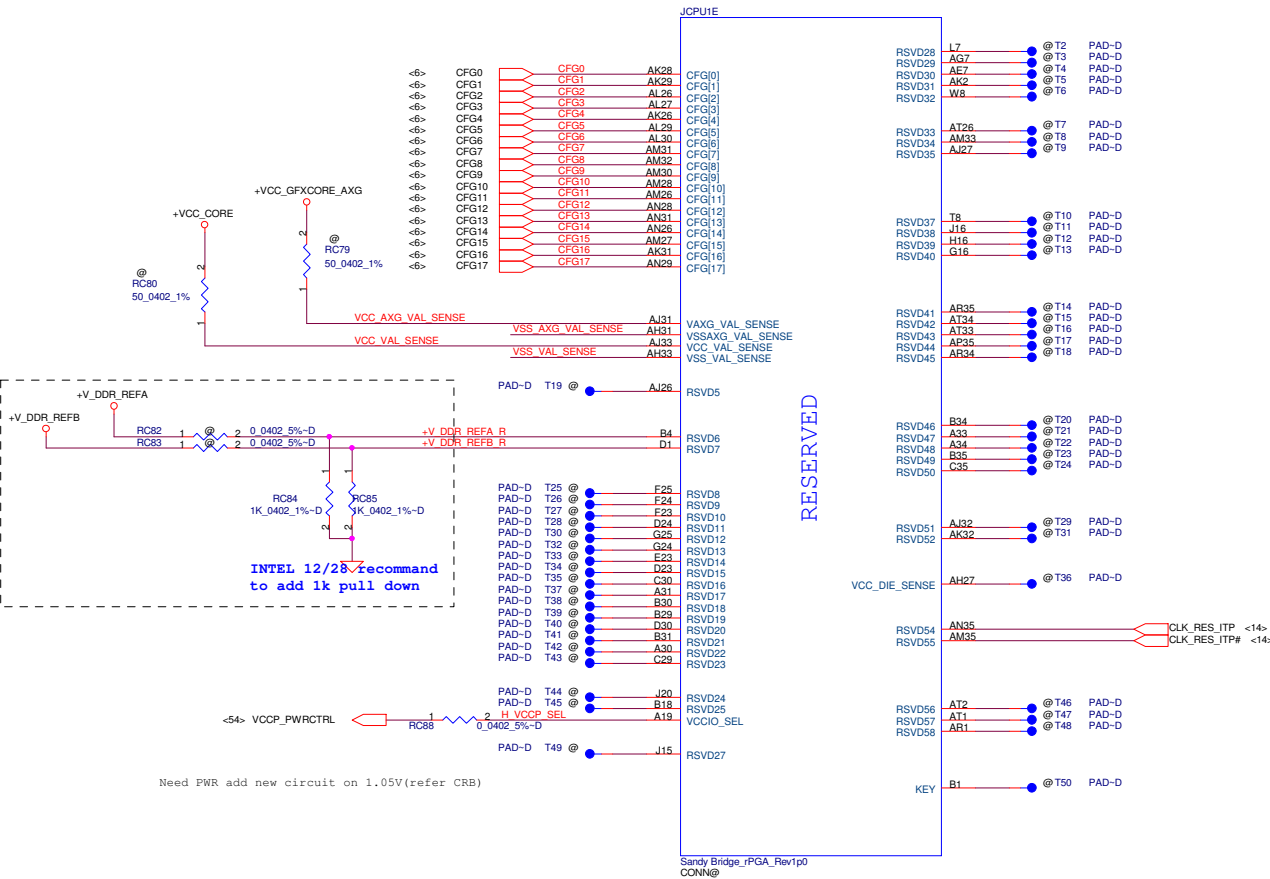
Display Port Presence Strap	
CFG4	*1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training



INTEL 12/28 recommend  
to add RC120, RC121, RC122, RC123  
Please place as close as JCPU1





QC=94A  
DC=53A

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PEG AND DDR

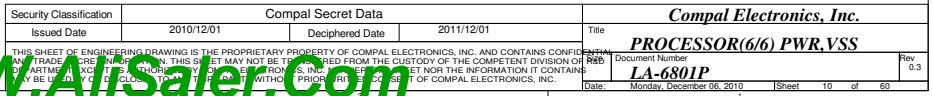
## CORE SUPPLY

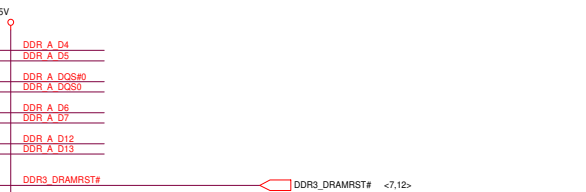
SVID

SENSE LINES

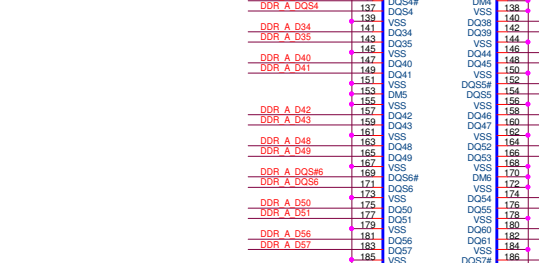
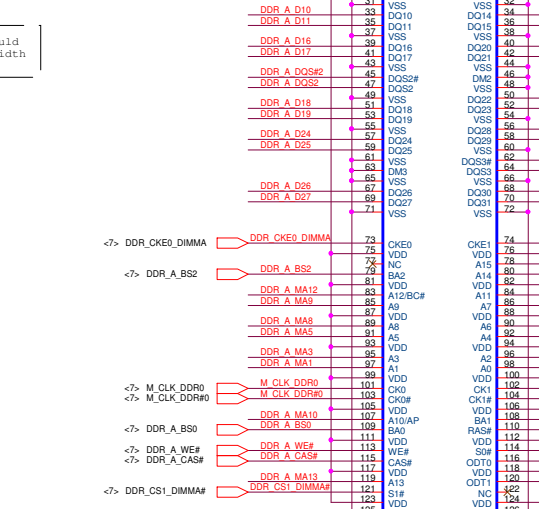
Sandy Bridge\_rPGA\_Rev1p0  
CONN@

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					LA-6801P	0.3
Date:				Monday, December 06, 2010		Sheet 9 of 60





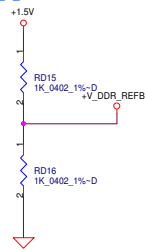
All VREF traces should  
have 10 mil trace width



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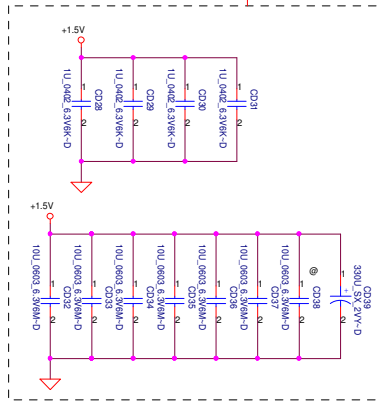
<7> DDR\_B\_DQS#[0..7]  
 <7> DDR\_B\_DQS#[0..7]  
 <7> DDR\_B\_DQ[0..63]  
 <7> DDR\_B\_MA[0..15]



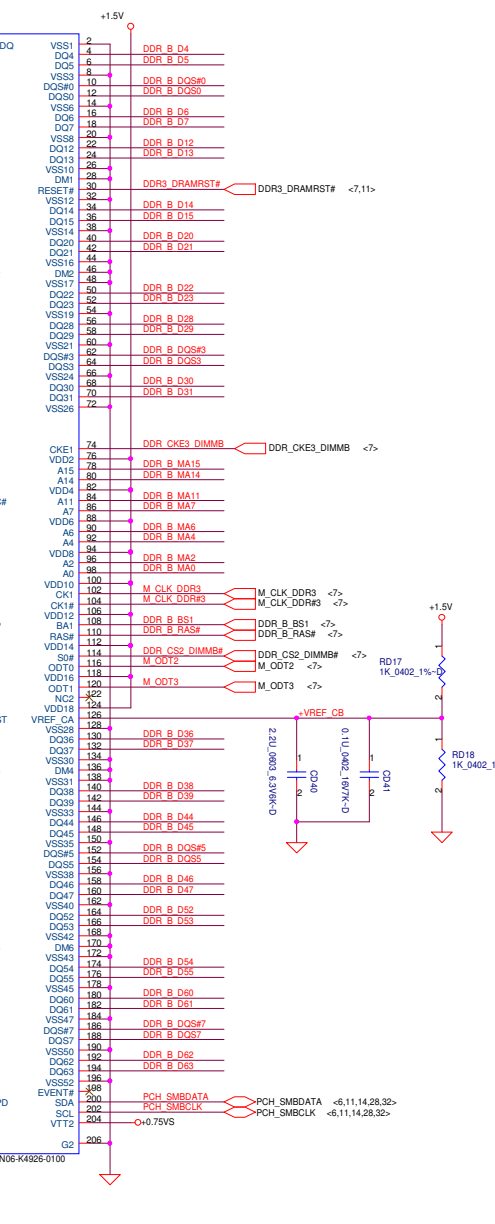
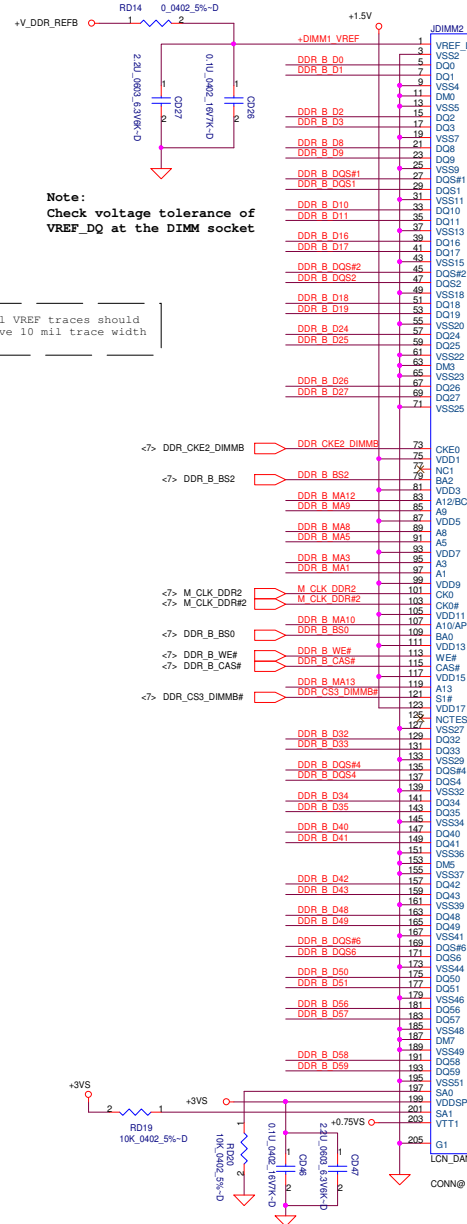
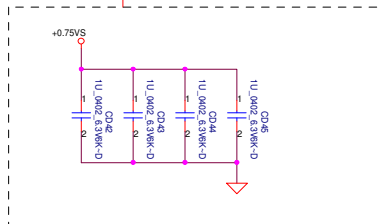
Note:  
 Check voltage tolerance of  
 VREF\_DQ at the DIMM socket

All VREF traces should  
 have 10 mil trace width

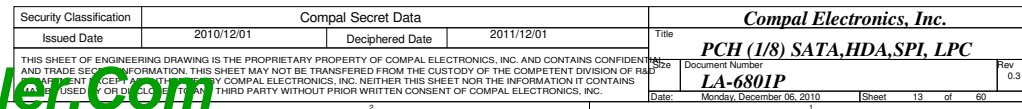
Layout Note:  
 Place near JDIMMB

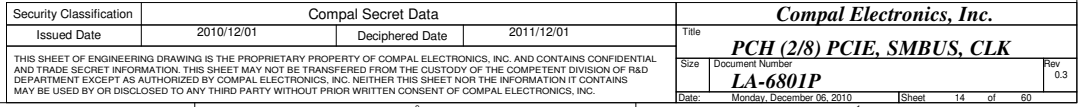


Layout Note:  
 Place near JDIMMB.203,204

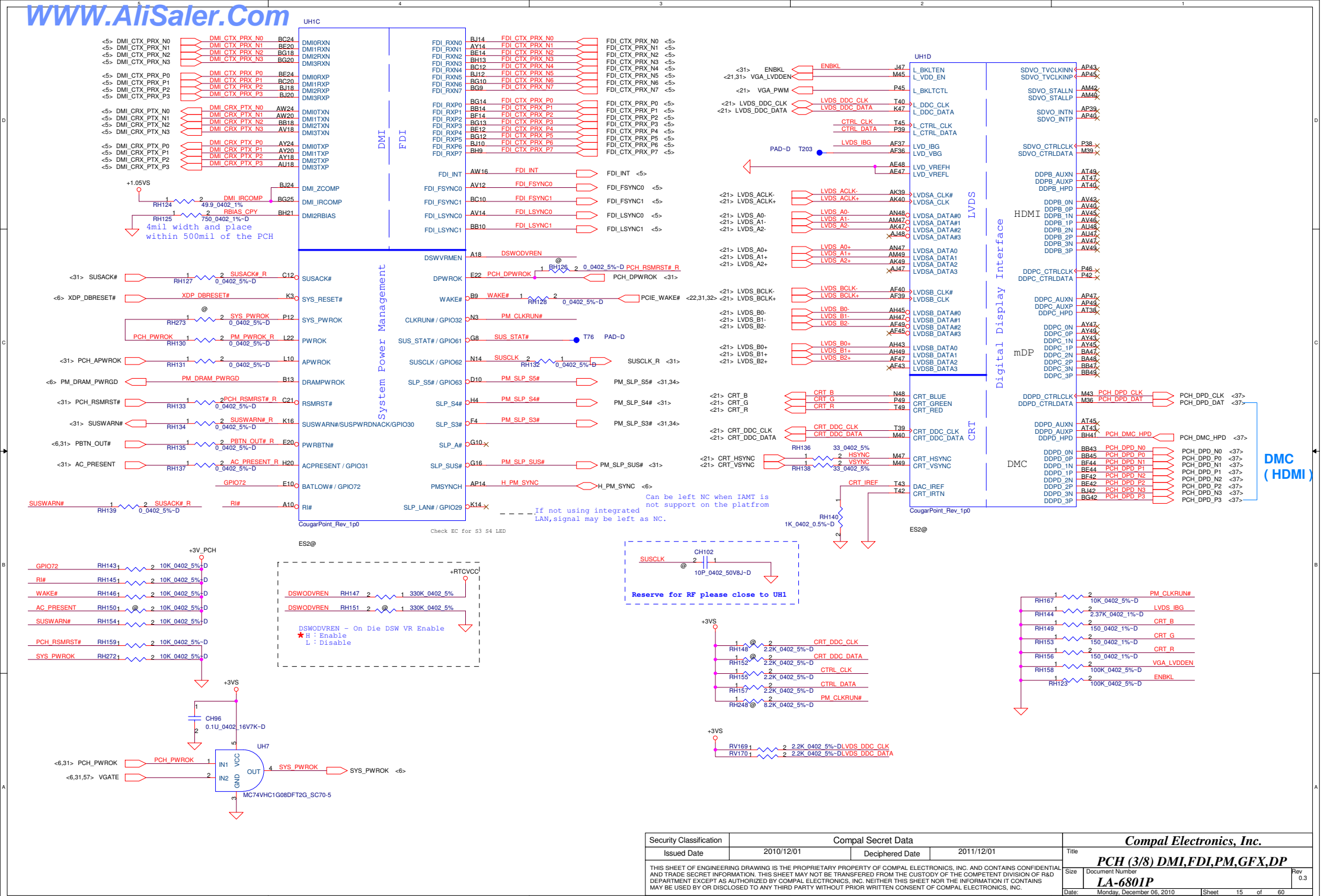


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				LA-6801P	
				Date	
				Monday, December 06, 2010	
				Sheet	
				12 of 60	
				Rev	
				0.3	

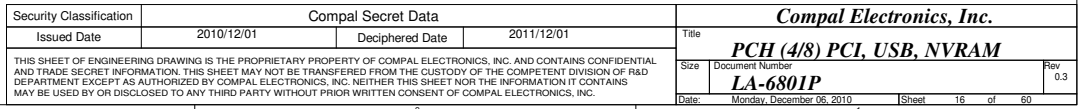


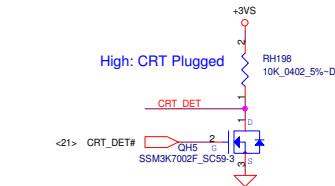
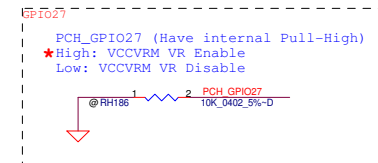
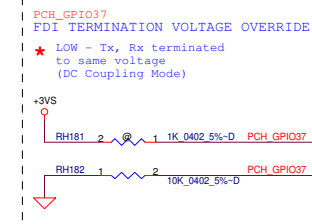
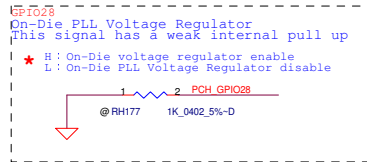
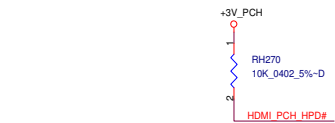






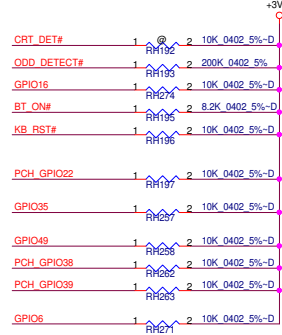
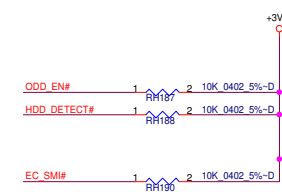
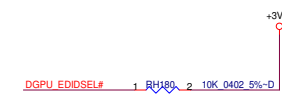
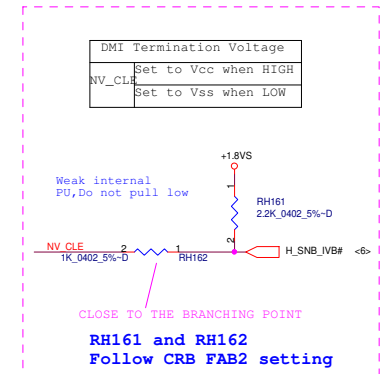
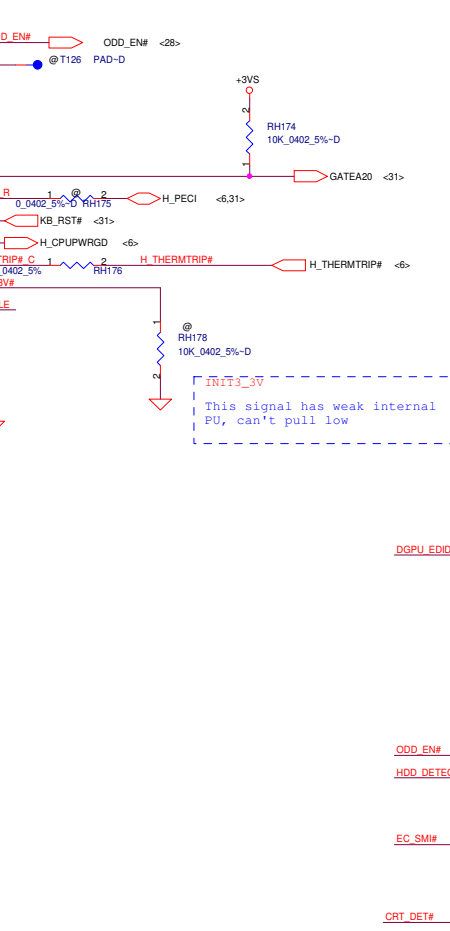
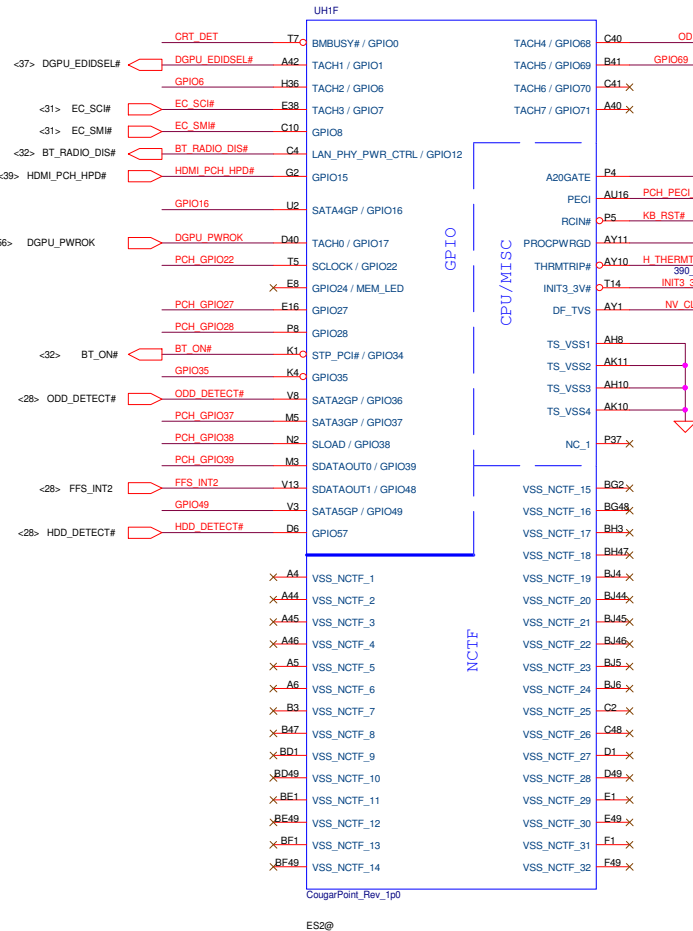




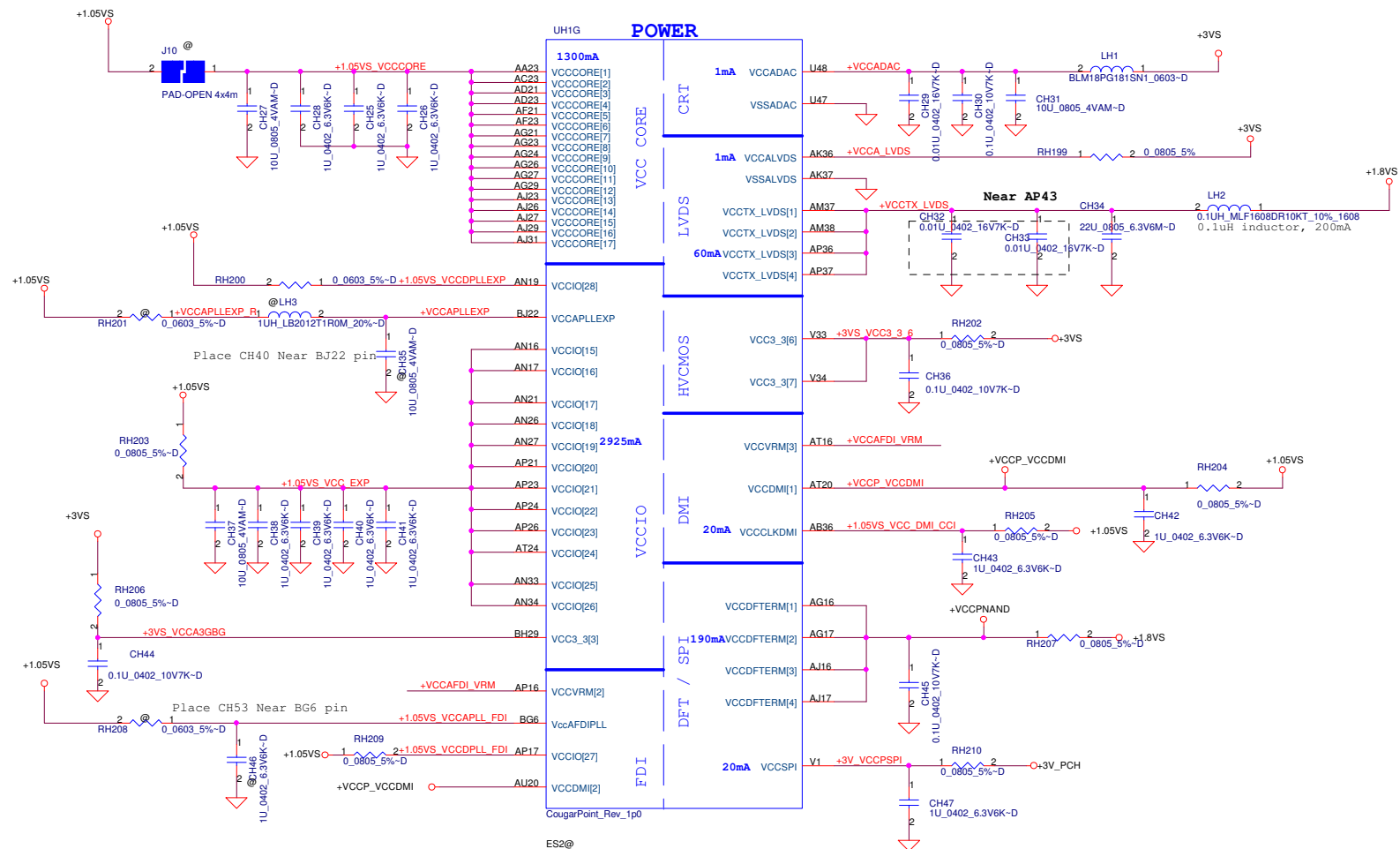


PCH\_GPIO28 needs to be connected to XDP\_FN8  
PCH\_GPIO35 needs to be connected to XDP\_FN9  
PCH\_GPIO15 needs to be connected to XDP\_FN16

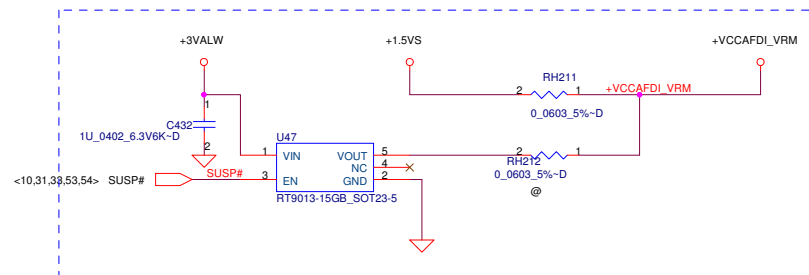
Please refer to Huron River Debug Board DG 0.5



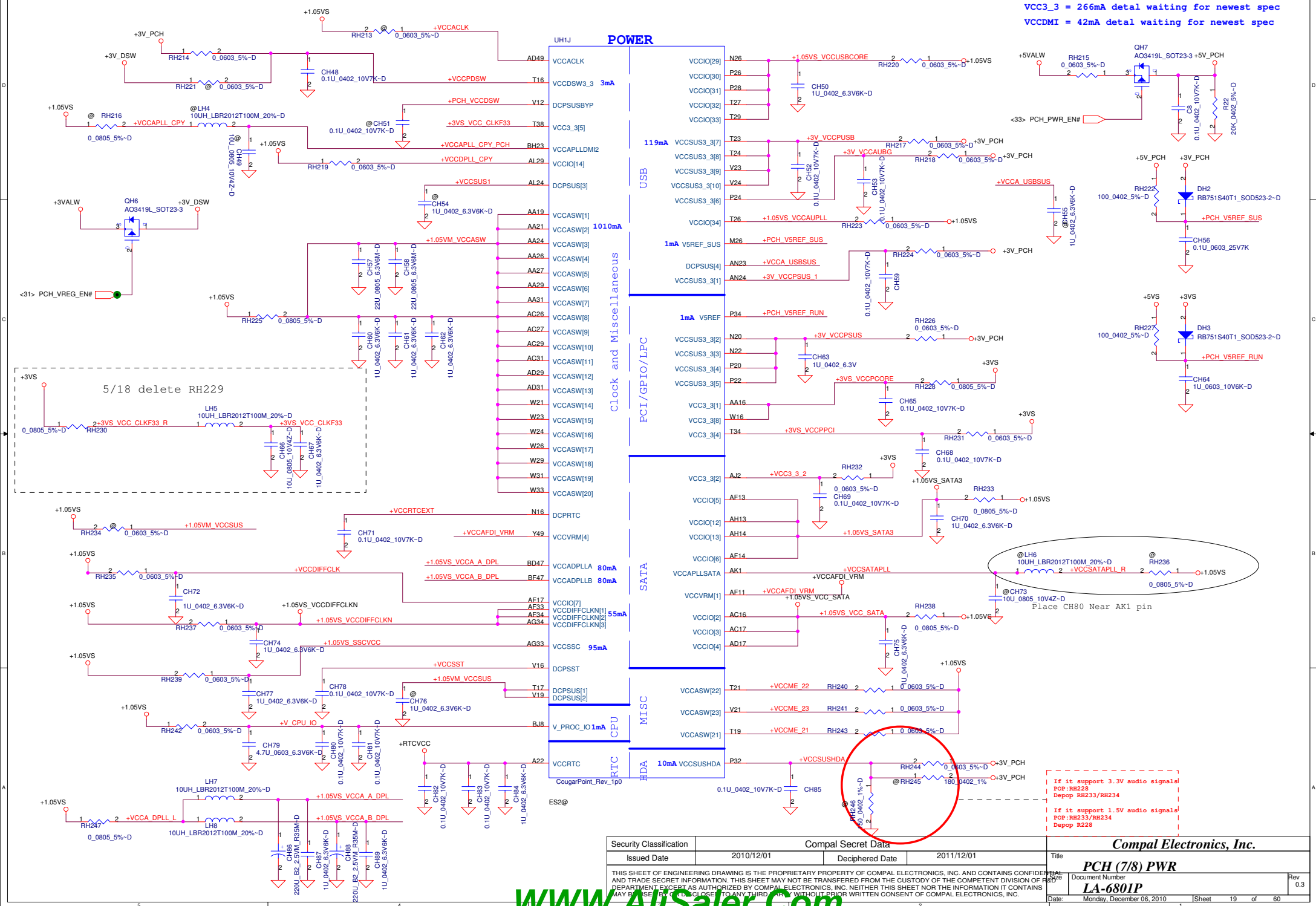
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				LA-6801P	Rev 0.3
				Date	Monday, December 06, 2010
				Sheet	17 of 60

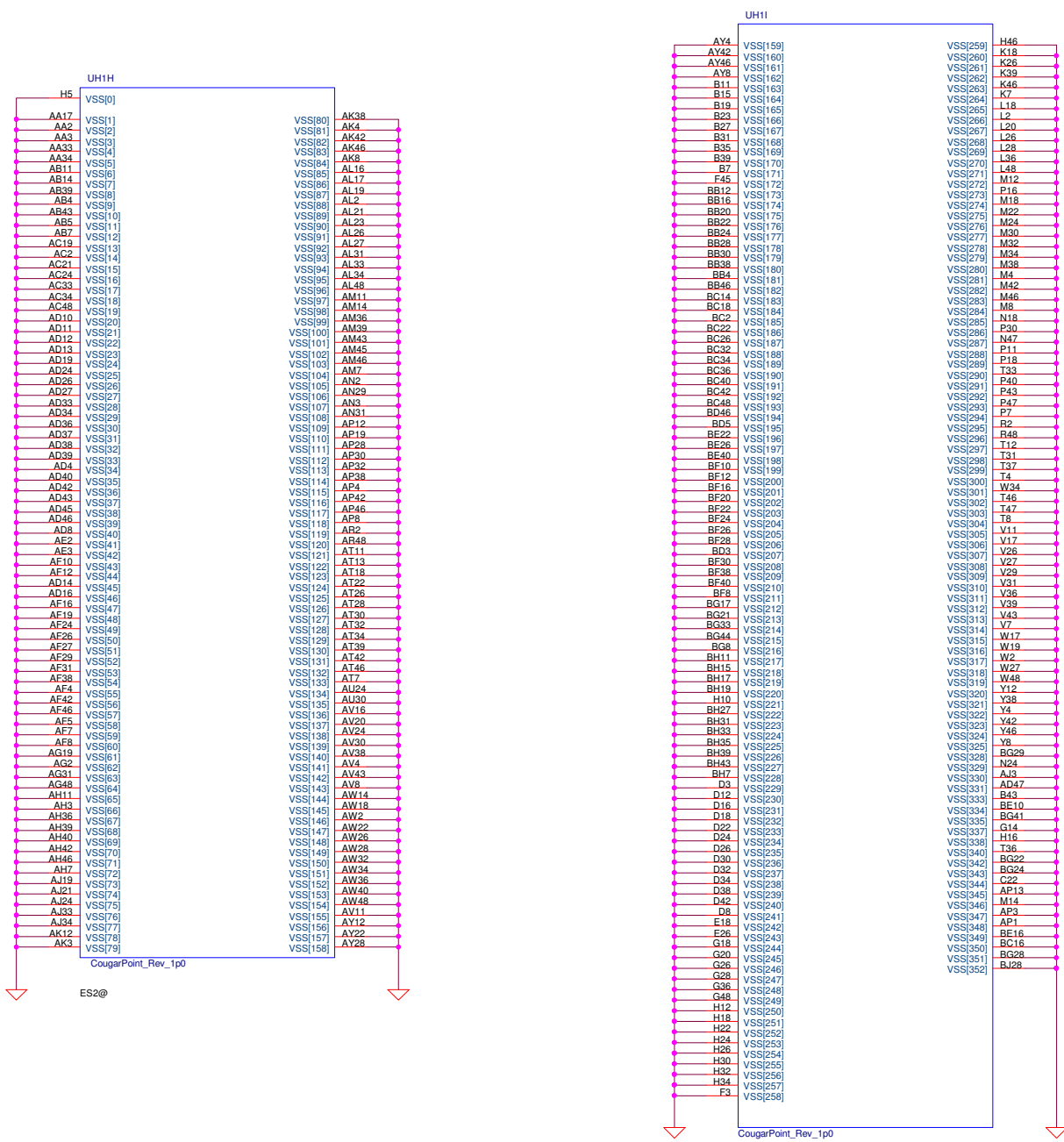


PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLb	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

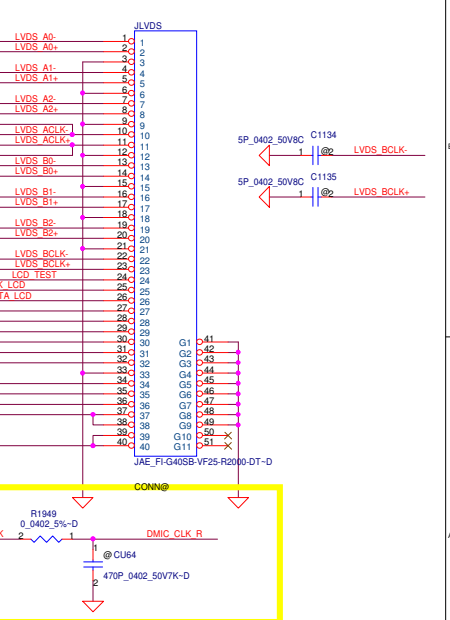
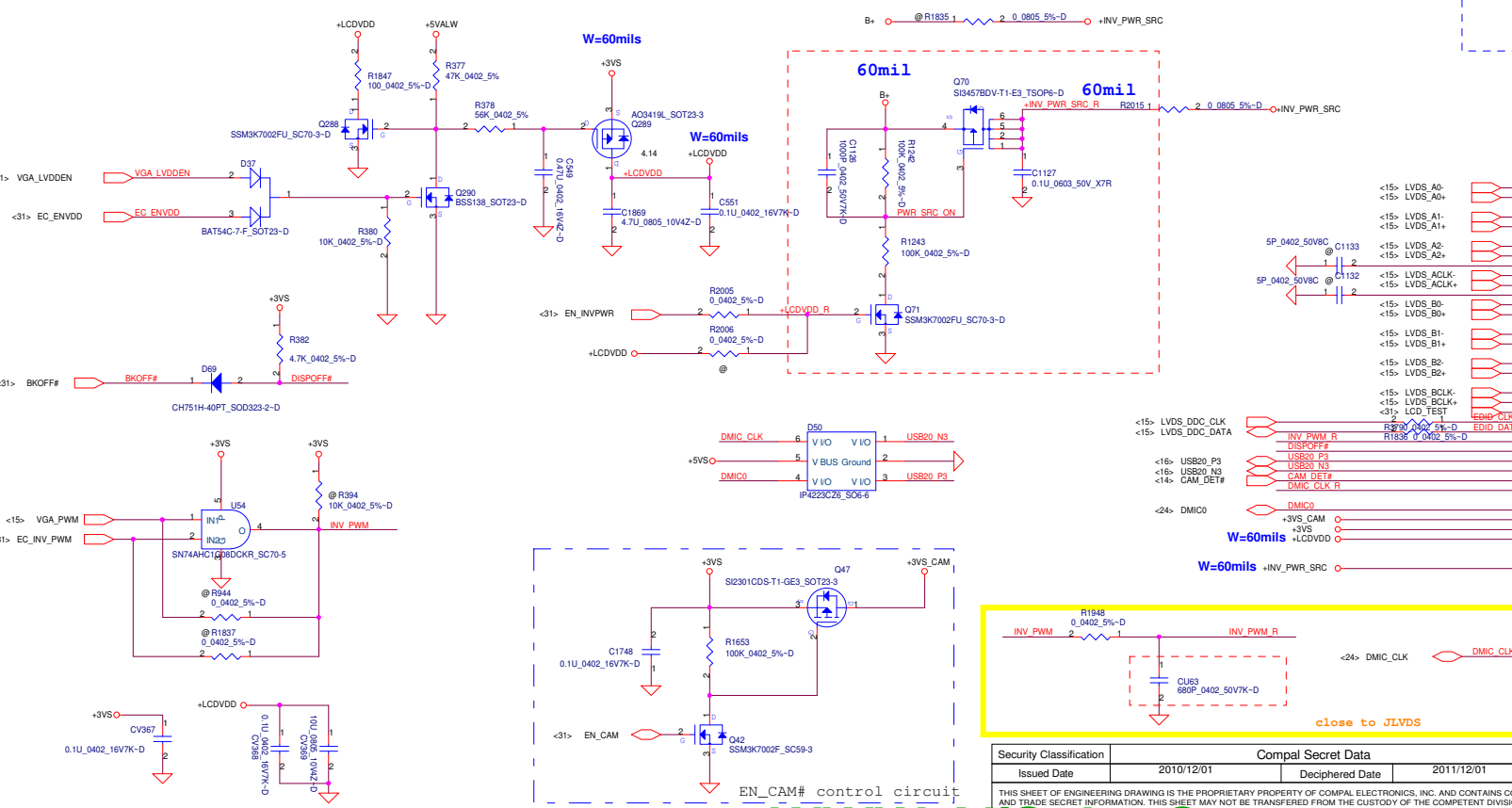
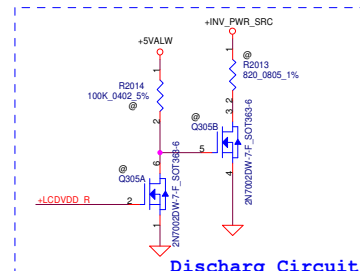
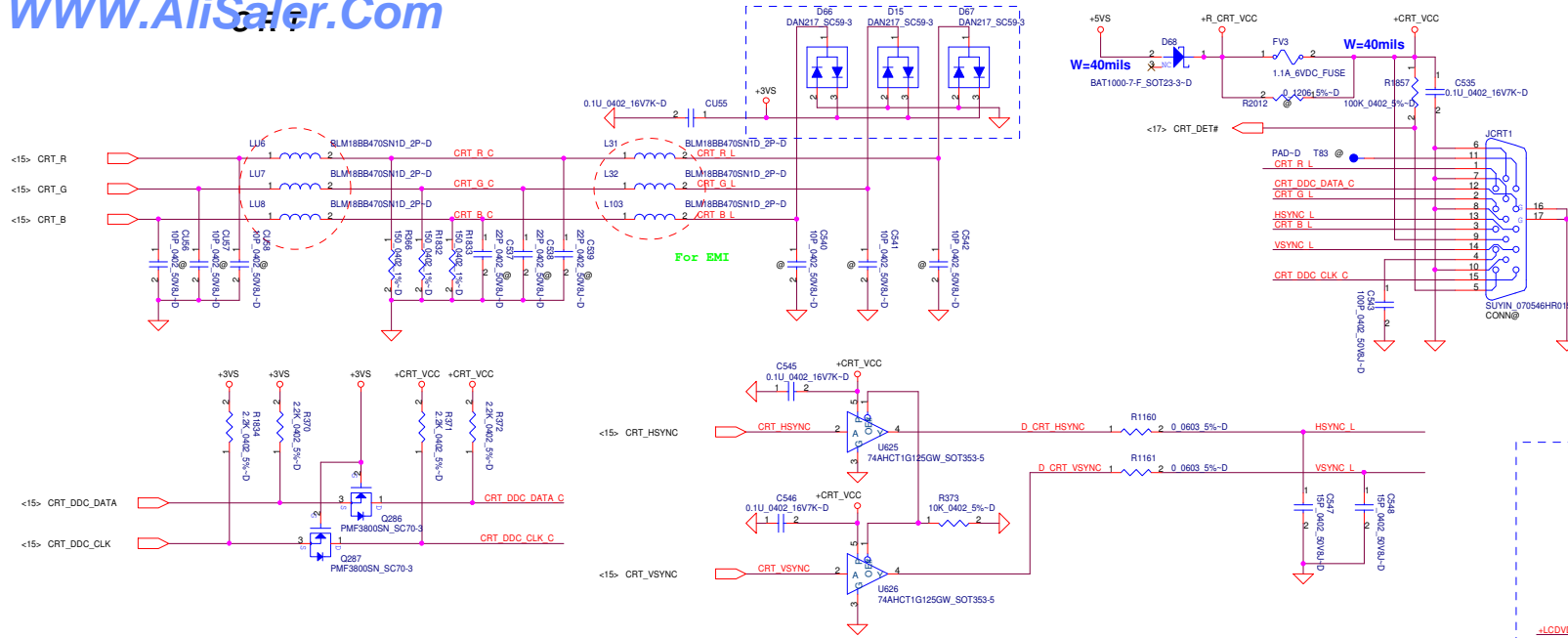


VCCVRM = 160mA detail waiting for newest spec





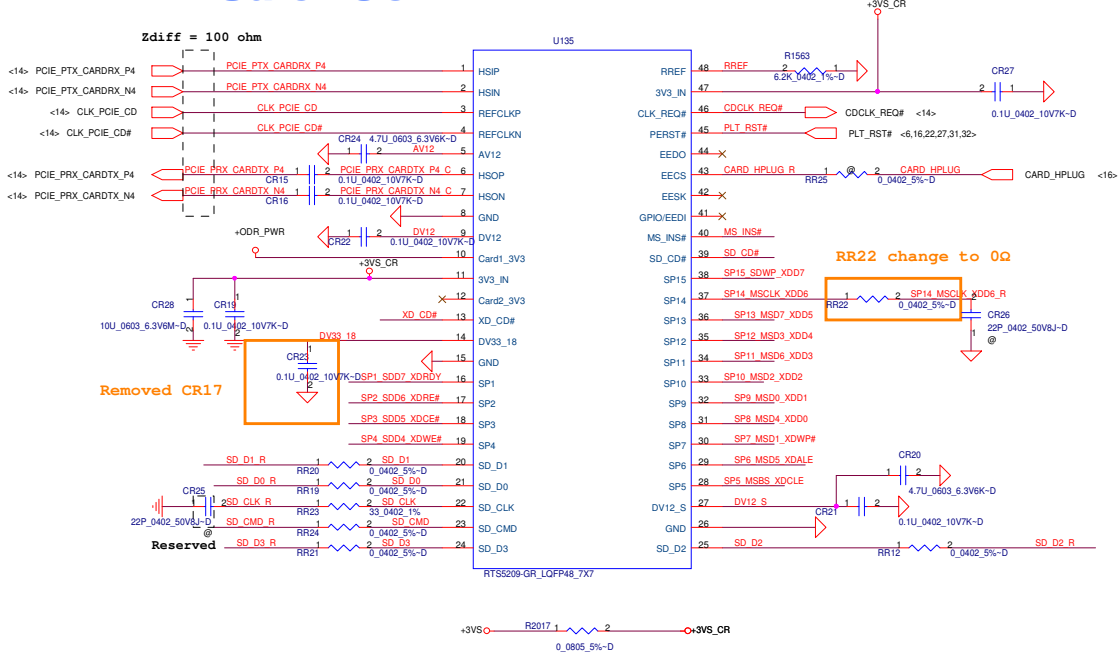
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Date: Monday, December 06, 2010				Sheet	20 of 60

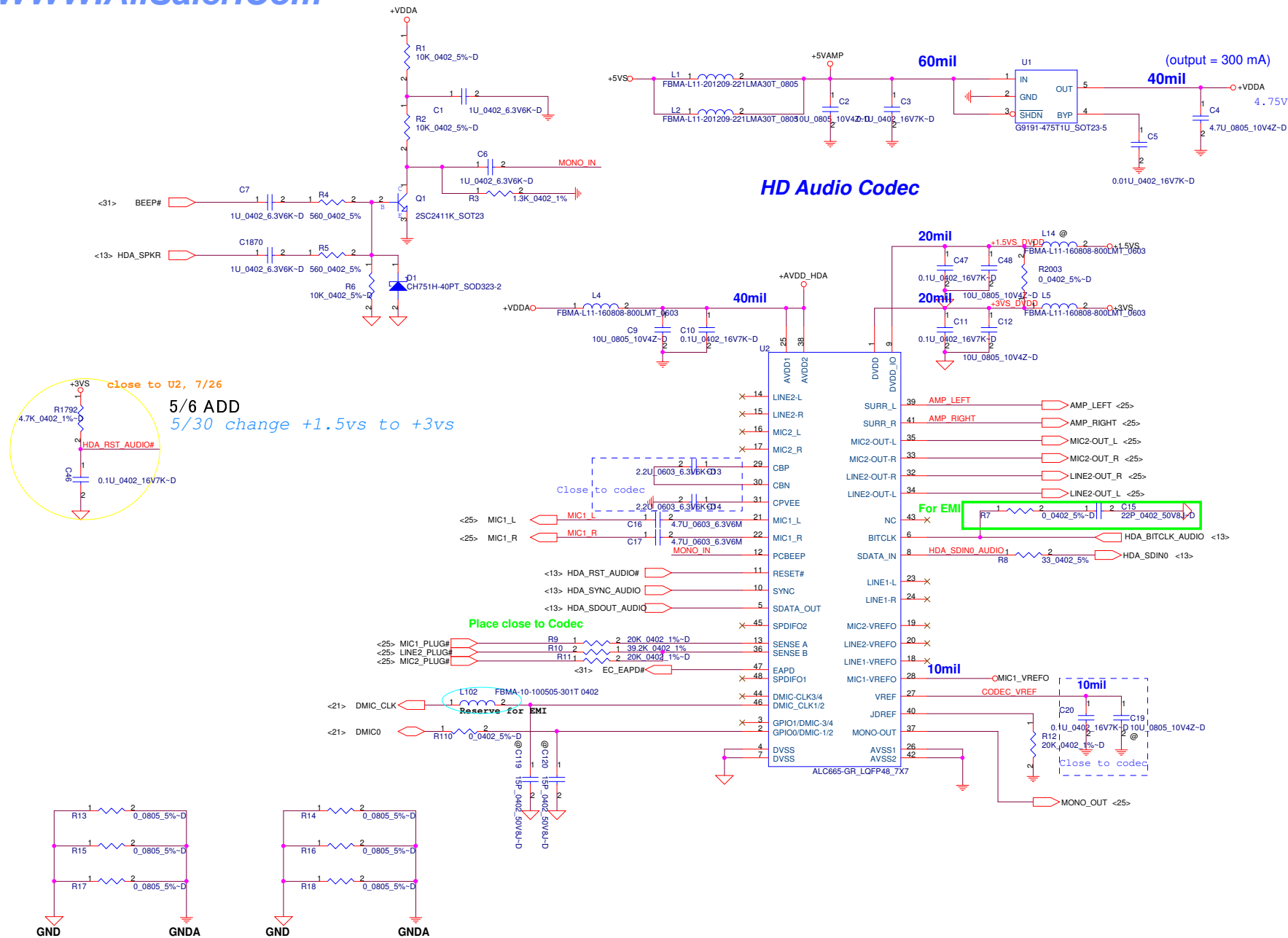


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				Date:	Monday, December 06, 2010
				Sheet	21 of 60









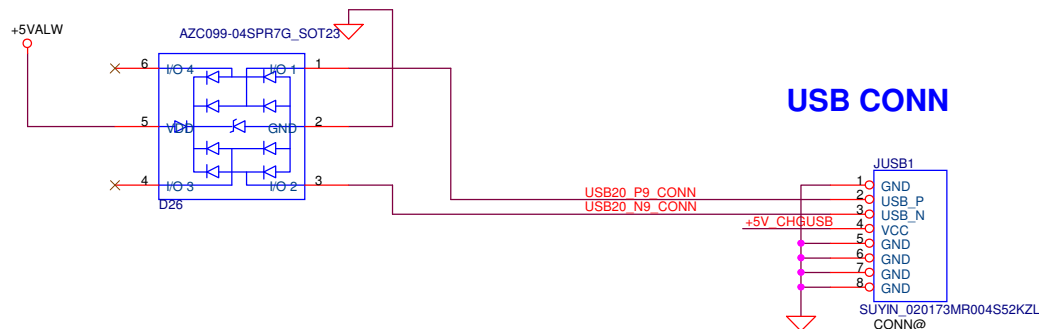
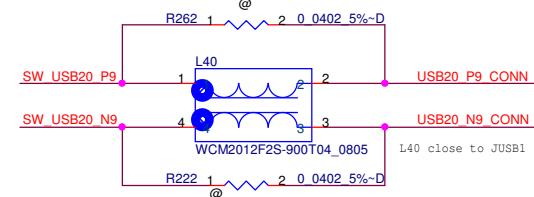
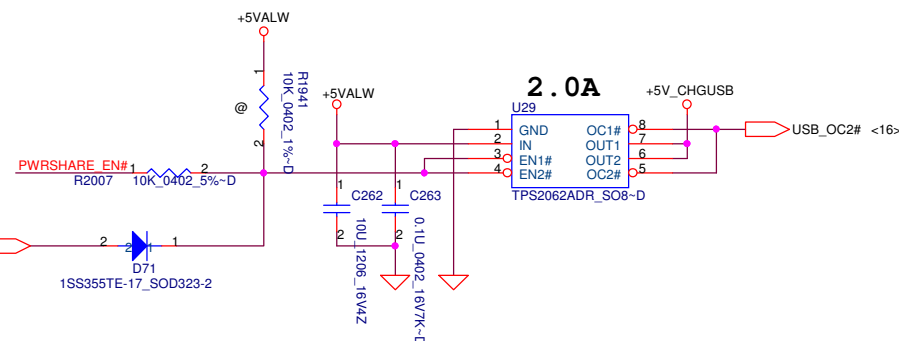
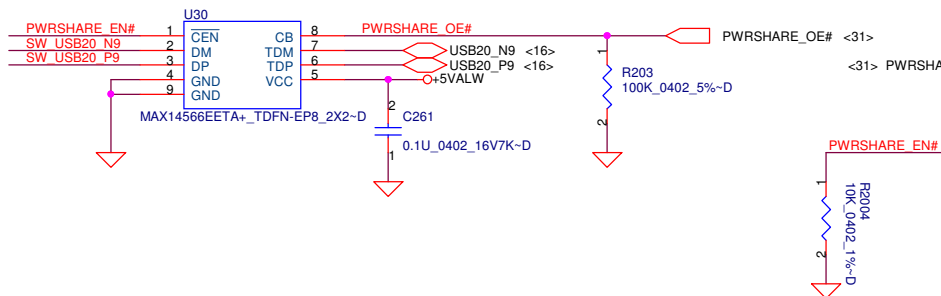
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				Codex ALC665			
				Document Number			
				LA-6801P			
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				Monday, December 06, 2010			
Sheet				24 of 60			
Rev				0.3			

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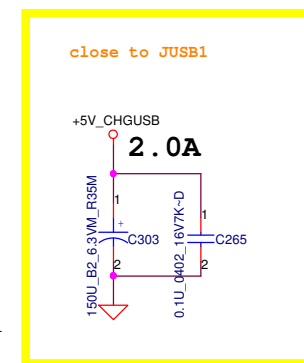
Date:	Monday, December 06, 2010	Sheet	23	of	90
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## Power share

CB	Function
L	auto detection charger identification active
H	DP/DM=TDF/TDM

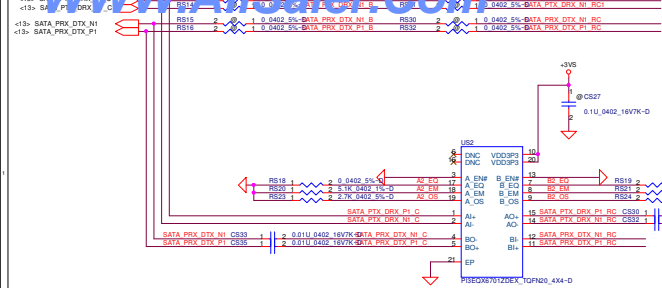


## USB CONN

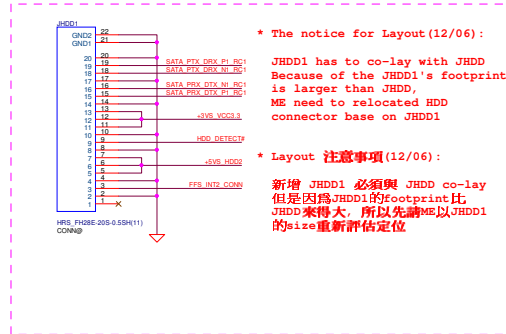
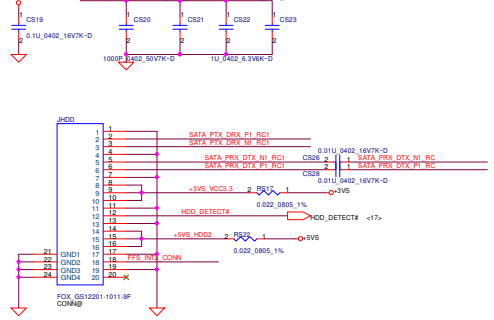
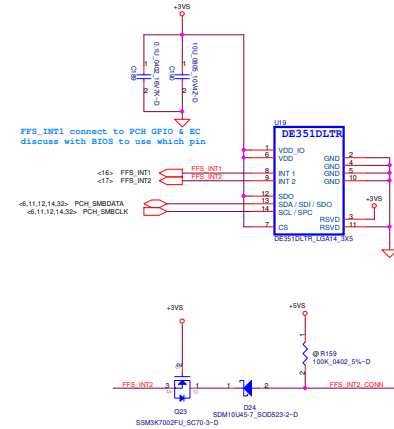


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				Date	Monday, December 06, 2010
				Sheet	26 of 60
				Rev	0.3



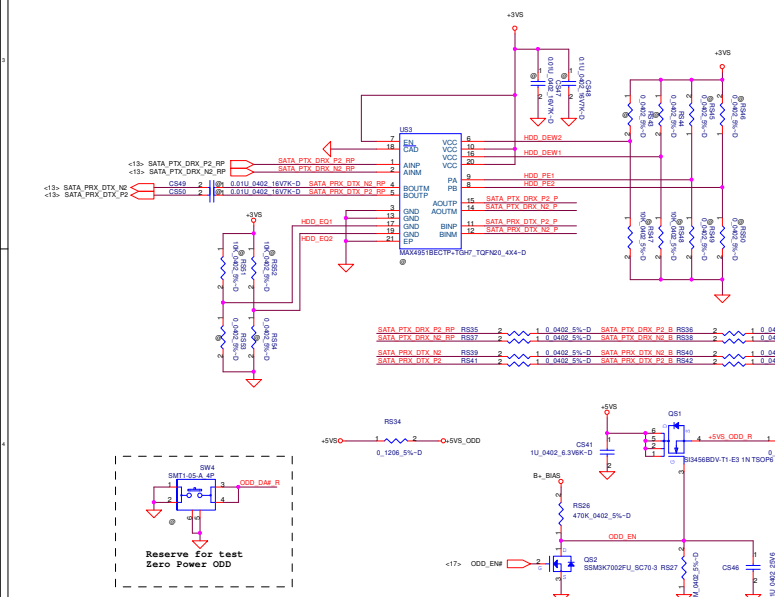


# Free Fall Sensor



\* The notice for Layout (12/06):  
JHDD1 has to co-lay with JHDD  
Because of the JHDD1's footprint  
is larger than JHDD,  
ME need to relocated HDD  
connector base on JHDD1

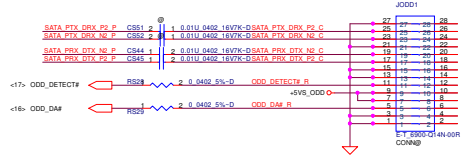
\* Layout 注意事項 (12/06):  
新增 JHDD1 必須與 JHDD co-lay  
但是因為JHDD1的footprint比  
JHDD來得大, 所以先請ME以JHDD1  
的size重新評估定位



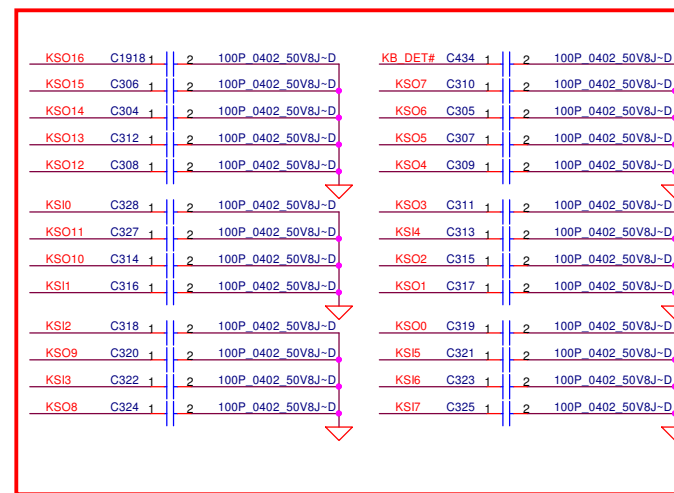
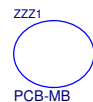
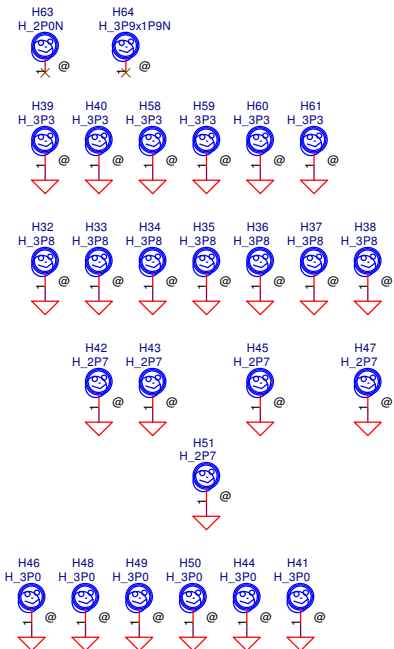
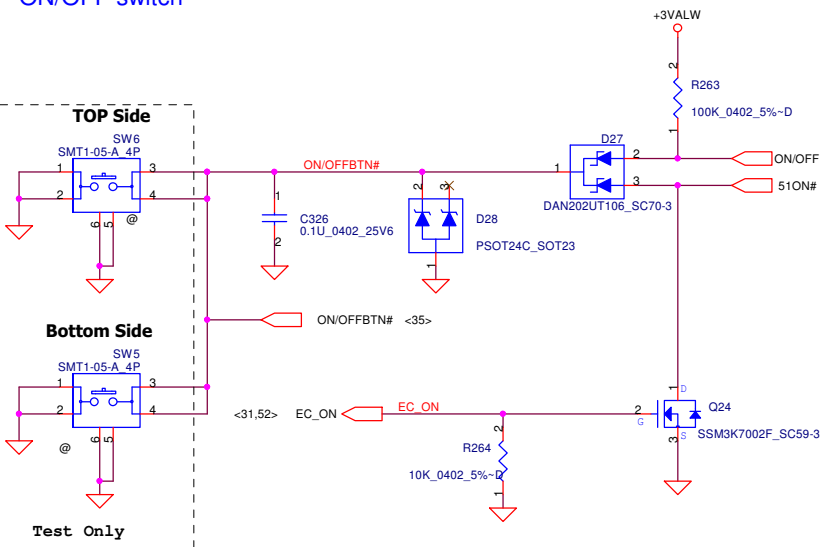
	MAXIM main	TI 2nd
P/N	SA00003LH1L	SA00003ZX0L
RS43 RS44	pop	depop
RS47 RS48	depop	pop
RS53 RS54	pop	depop



# SATA ODD Conn.

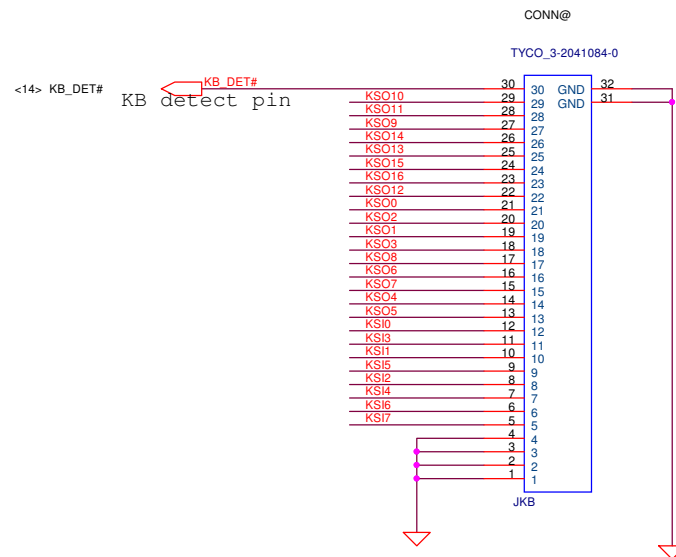


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2011/12/01		Doc. Number
FES/HDD/ ODD Connector		Rev.
LA-6801P		0.3



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KSO[0..16] KSO[0..16] <31>

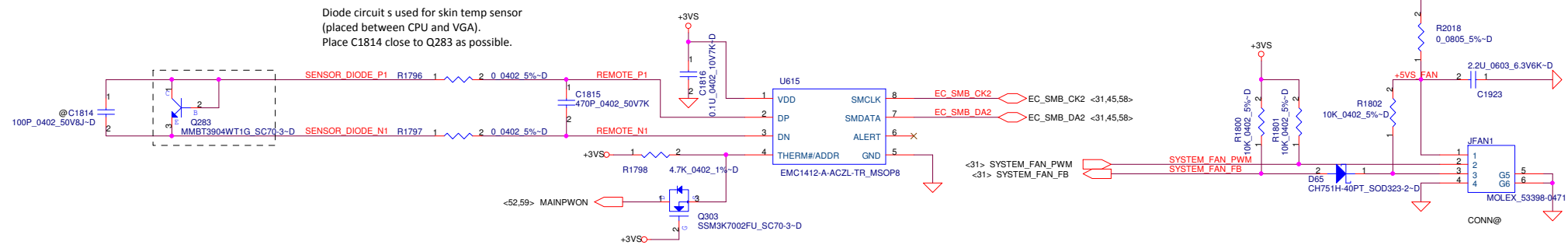
## INT\_KBD Conn.



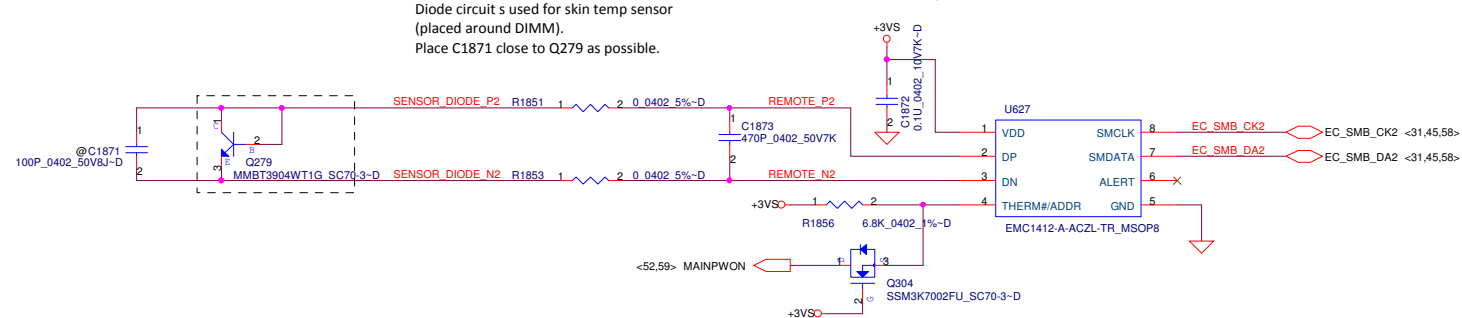
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				Date	Monday, December 06, 2010
				Sheet	29 of 60
				Rev	0.3

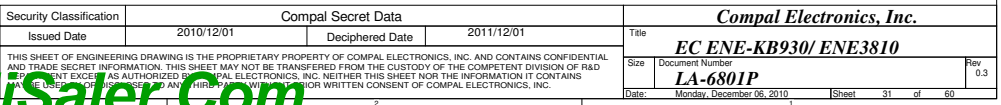


## System Thermal Sensor 1

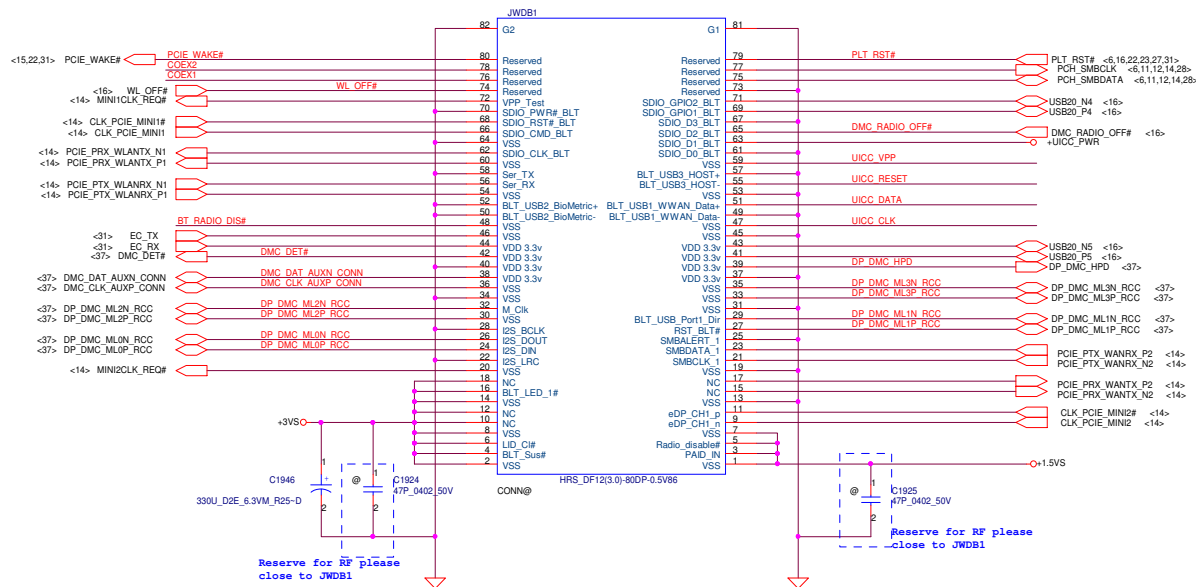


## System Thermal Sensor 2

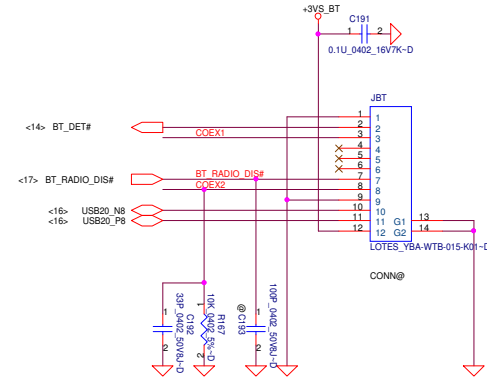
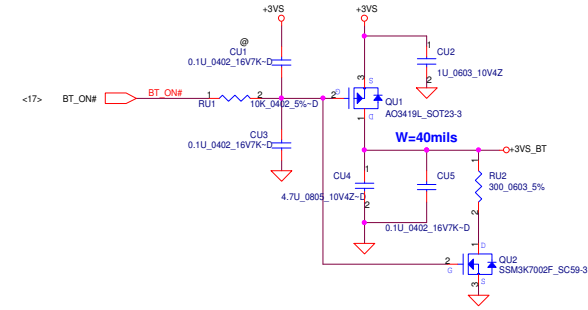




## To DMC PCB connector

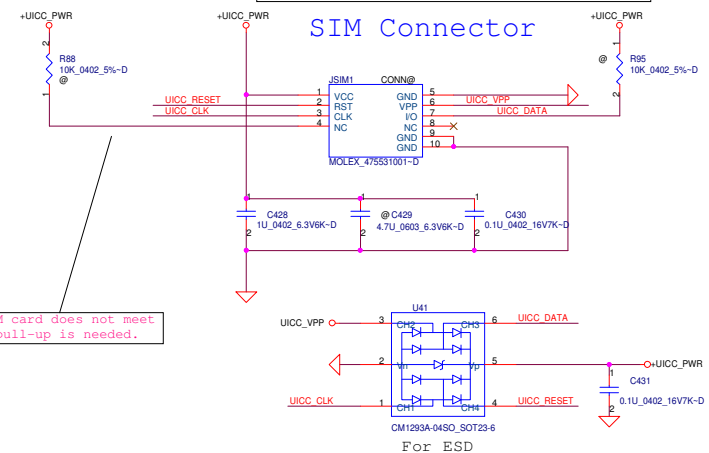


## BlueTooth



SIM card board 4.7uF change to 1uF for Tiger detect issue.

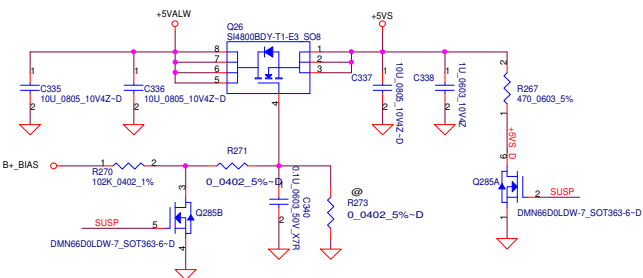
## SIM Connector



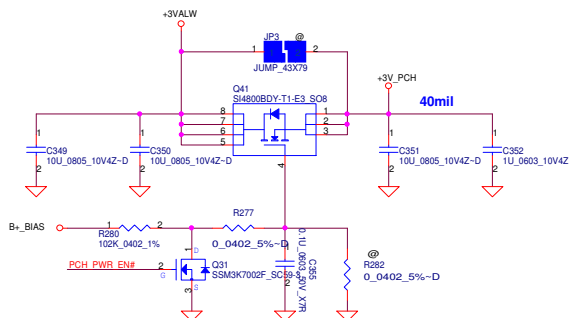
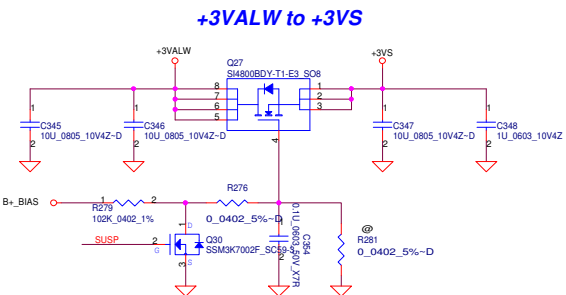
Reserve for SIM card does not meet rise time and pull-up is needed.

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Size	Document Number	Sheet	32	of 60
LA-6801P	Rev	0.3	Date: Monday, December 06, 2010	

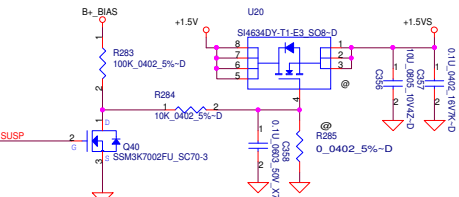
### +5VALW to +5VS



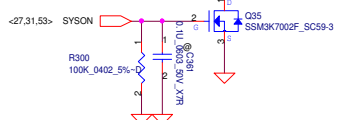
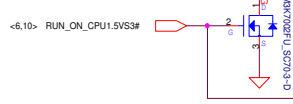
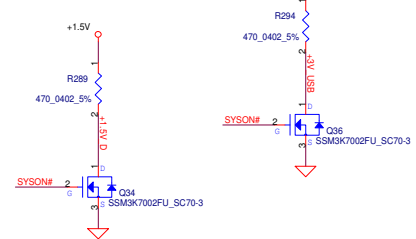
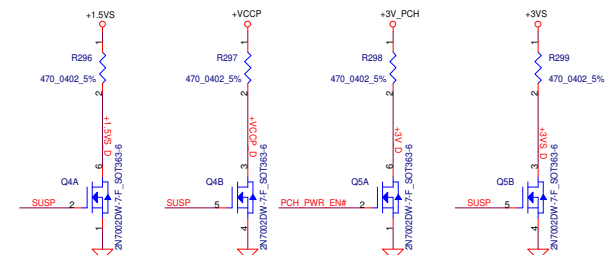
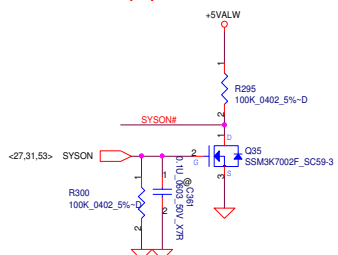
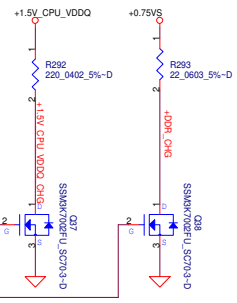
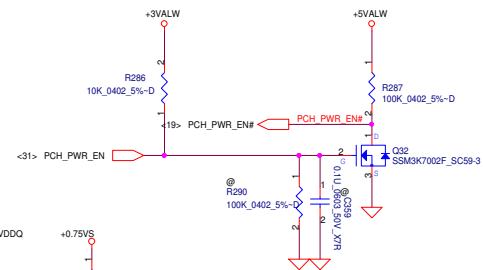
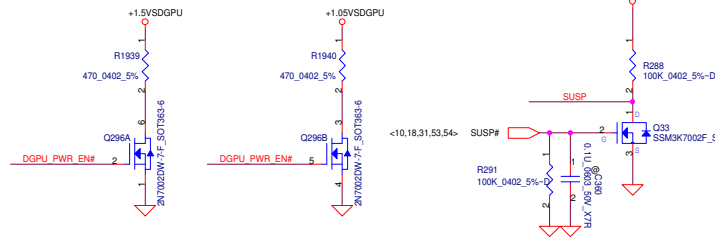
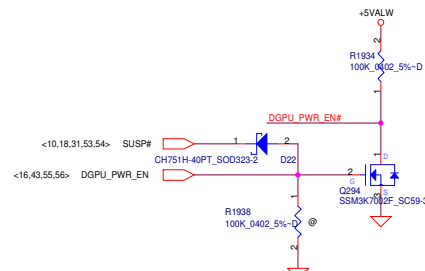
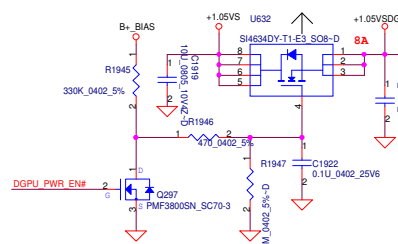
### +3VALW to +3V\_PCH



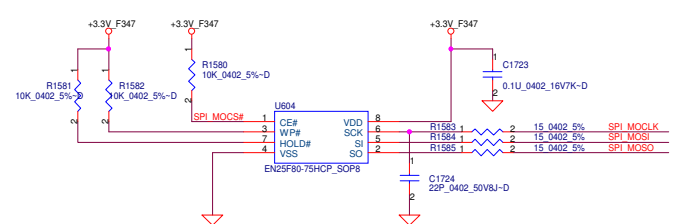
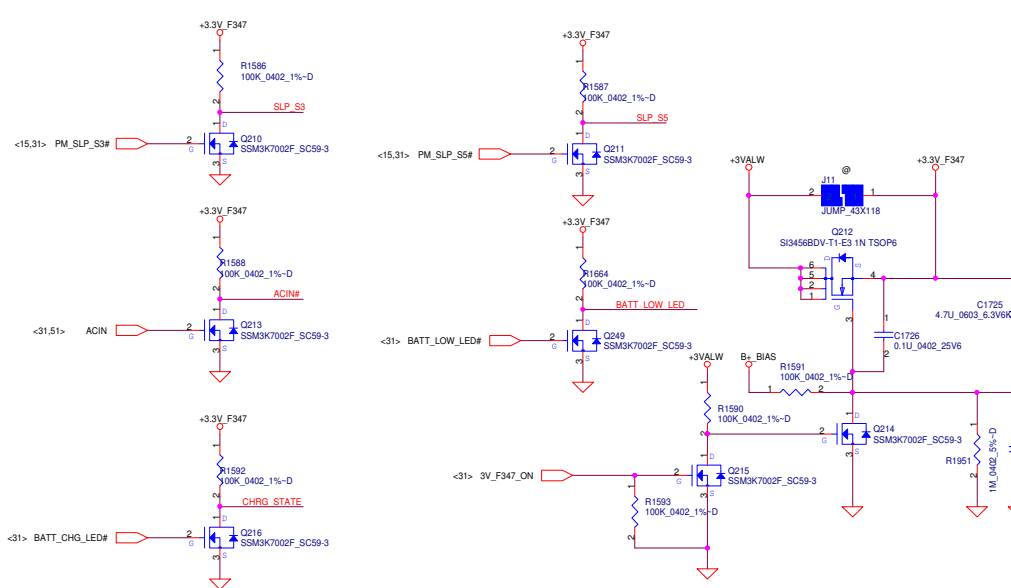
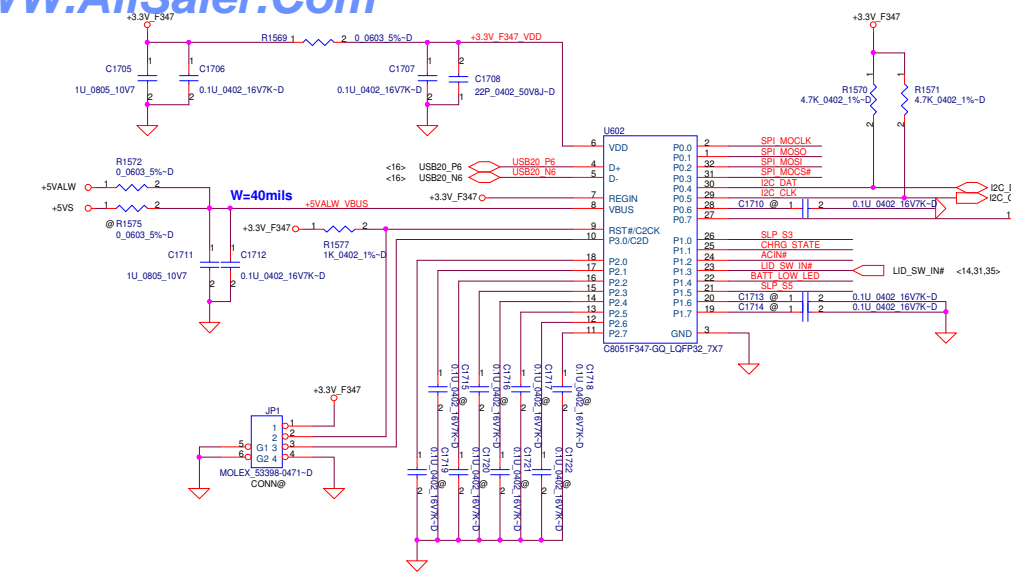
### +1.5V To +1.5VS



### +1.05V to +1.05VSDGPU Transfer



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Size	Document Number	LA-6801P	Rev	0.3
Date	Monday, December 06, 2010	Sheet	33	of 60



+3.3V\_F347 behavior

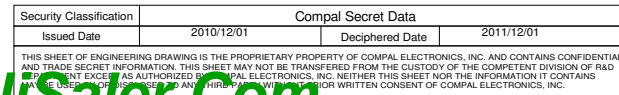
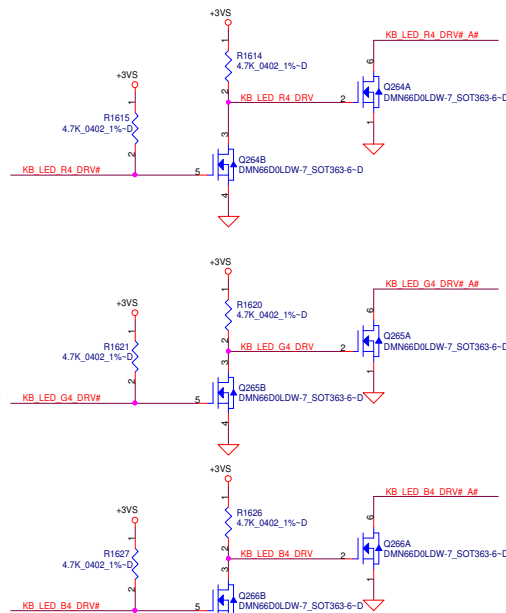
	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

AC mode battery full in S5:turn off ELC controller

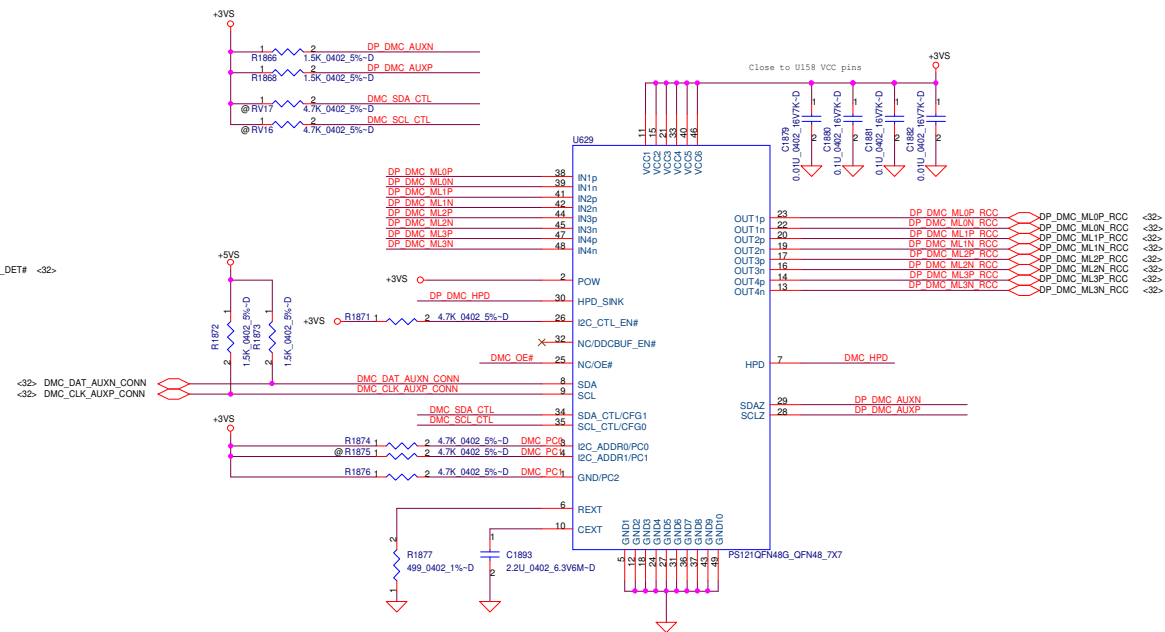
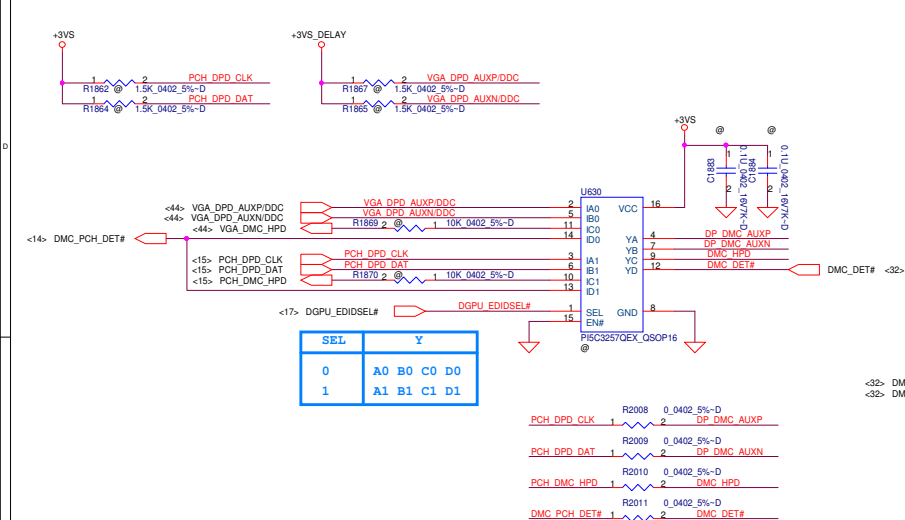


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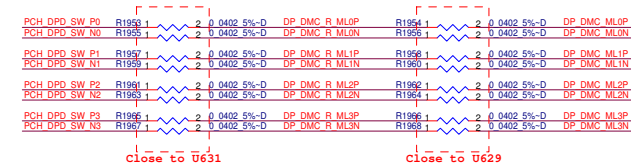
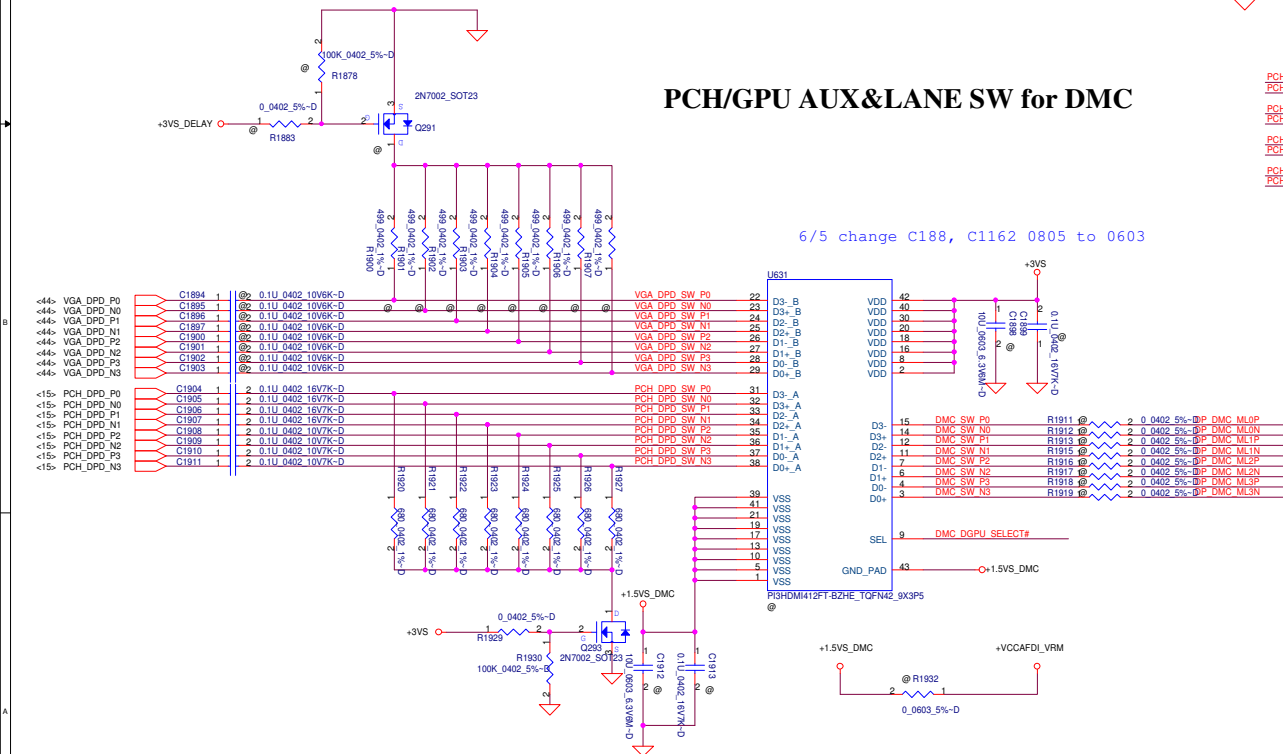




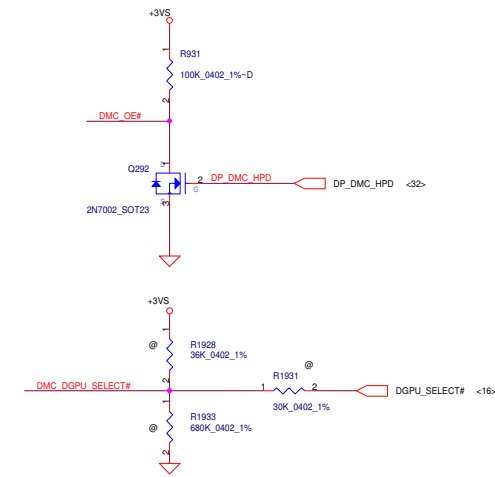
## DMC Redriver



## PCH/GPU AUX&LANE SW for DMC



6/5 change C188, C1162 0805 to 0603

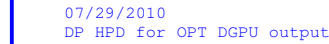


AUX_SEL/SEL1&2	Chanel	Source
0	A	GPU
1	B	PCH

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		LA-6801P				0.3	
Date:		Monday, December 06, 2010			Sheet 37 of 60		



## Normal



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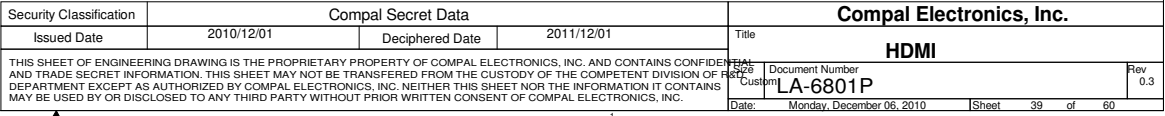
### Mini Display Port

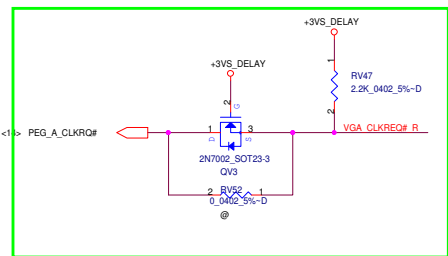
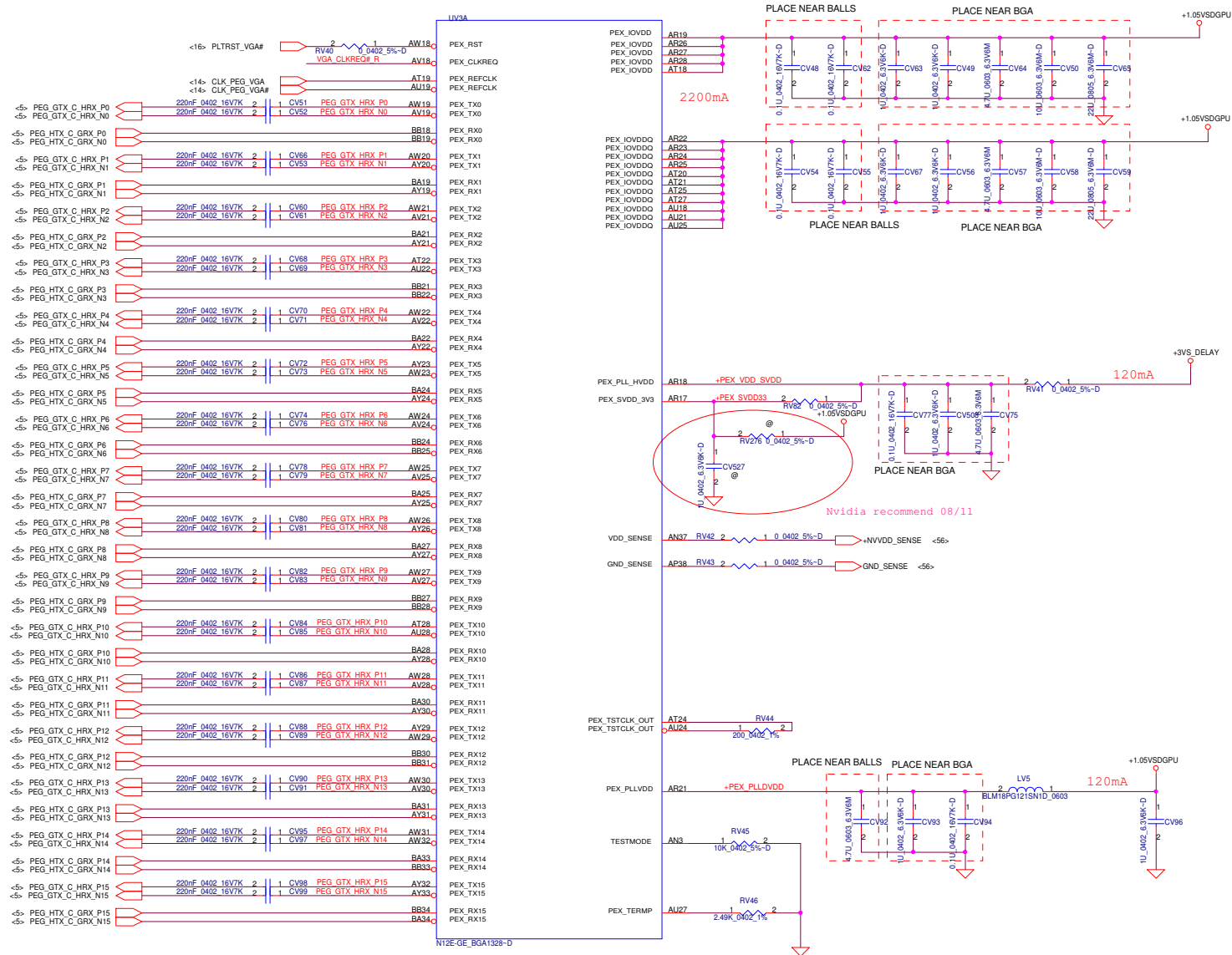
Size	Document Number	Rev
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Custom	A-6801P	0.3
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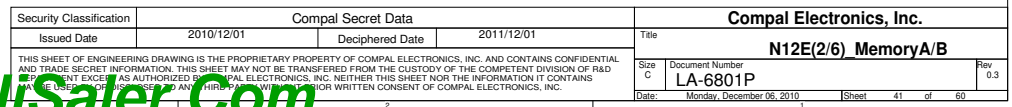
Date:	Monday, December 06, 2010	Sheet	38	of	60
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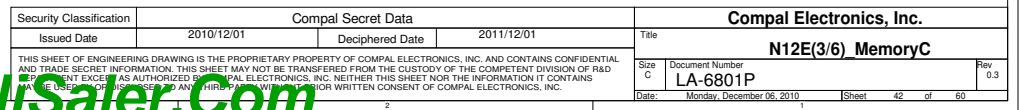
Date:	Monday, December 06, 2016	Sheet	00	01	00
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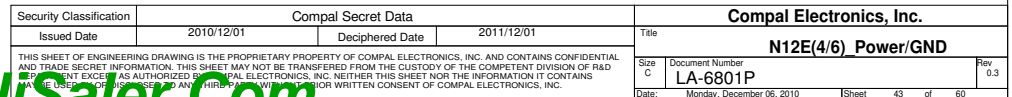


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Deciphered Date		2011/12/01		N12E(1/6)_PCIE	
Size		Document Number		Rev	
C		LA-6801P		0.3	
Date		Monday, December 06, 2010		Sheet 40 of 60	

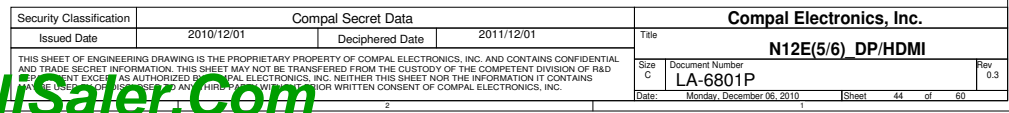






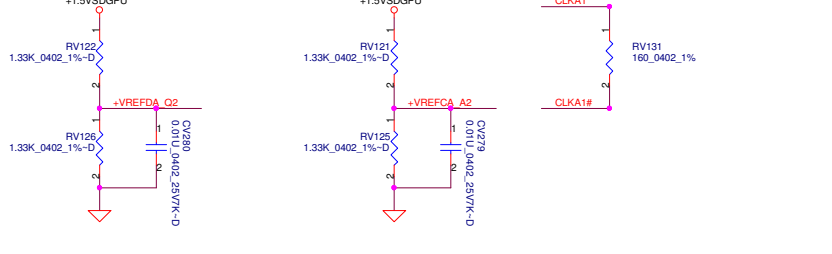
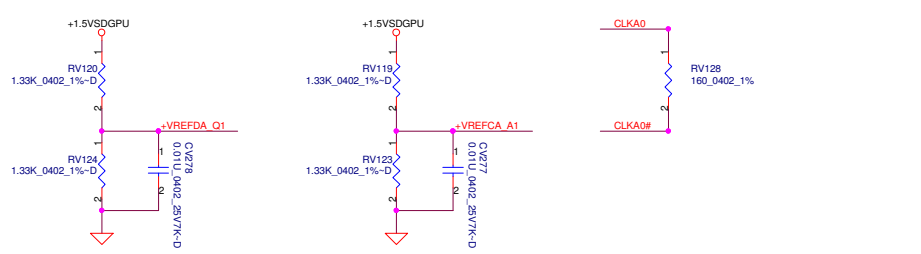
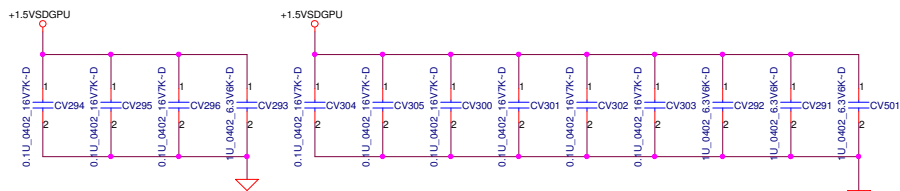
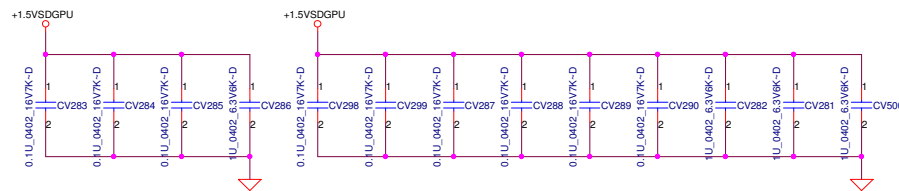
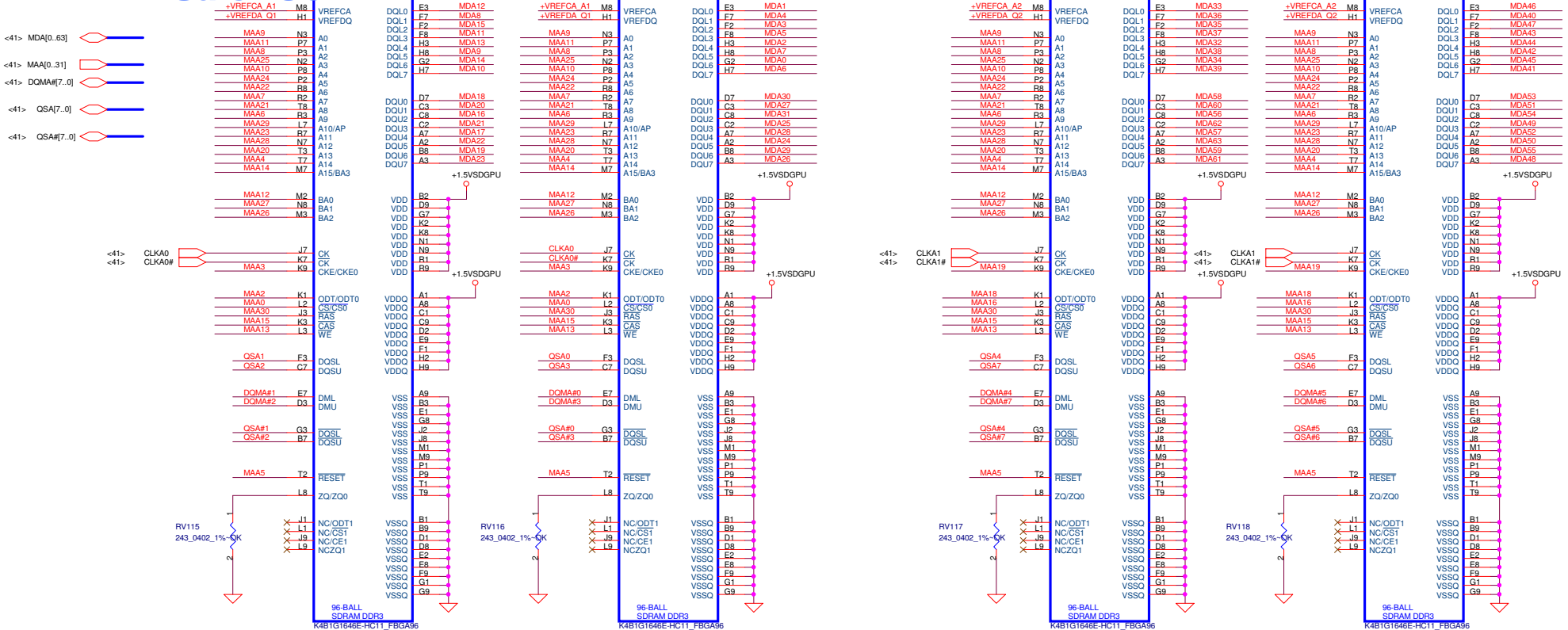






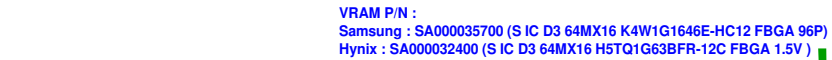


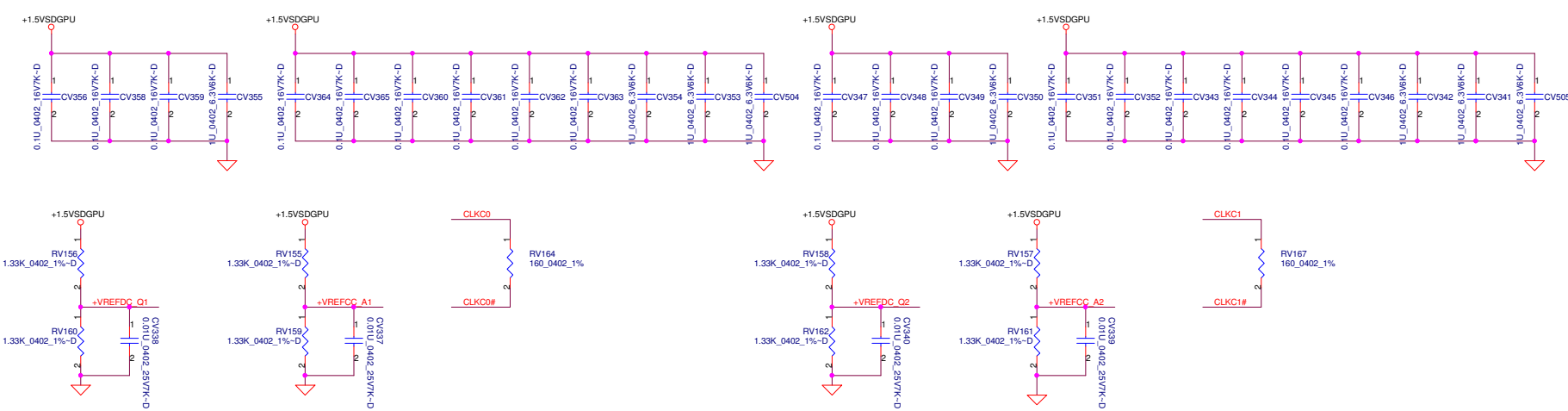
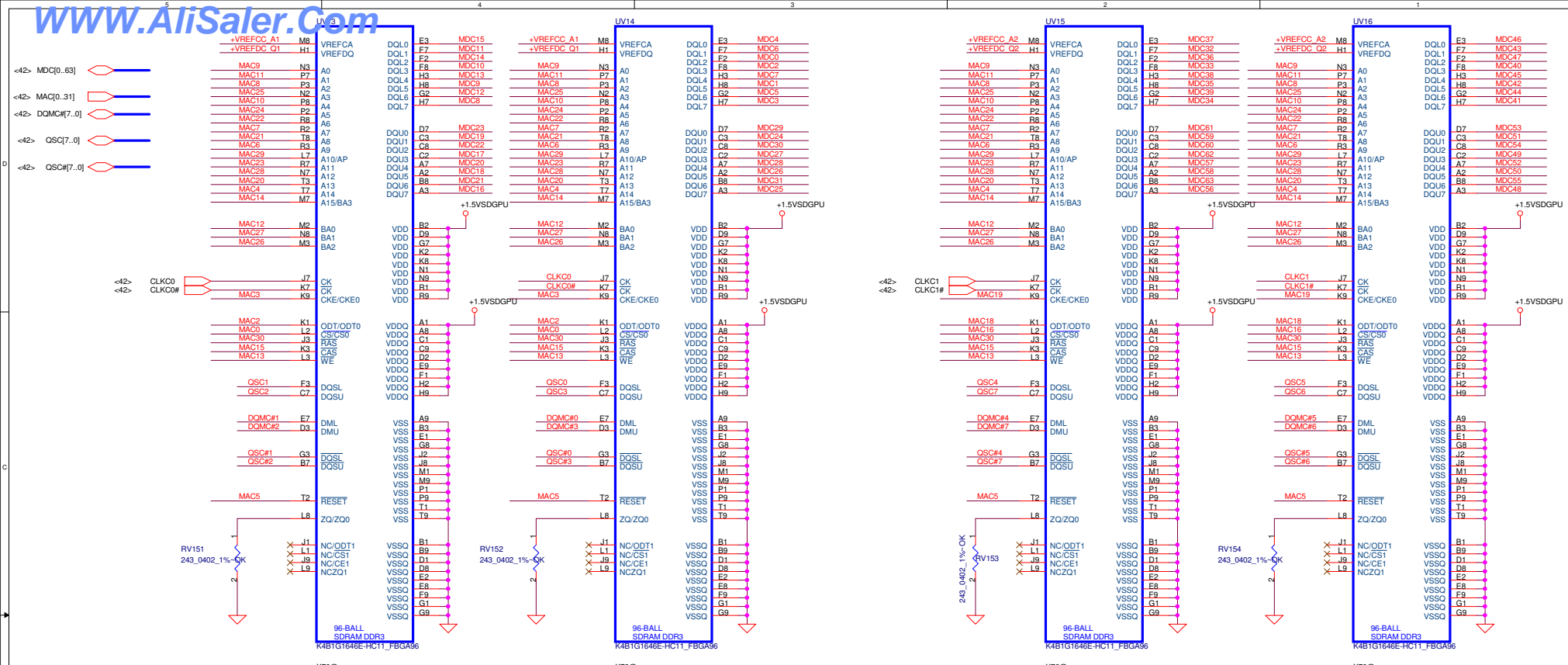
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VRAM P/N :  
Samsung : SA000041T00 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA 96P)  
Hynix : SA000041S20 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA 96P)

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												LA-6801P		0.3	
										Date:		Monday, December 06, 2010		Sheet	

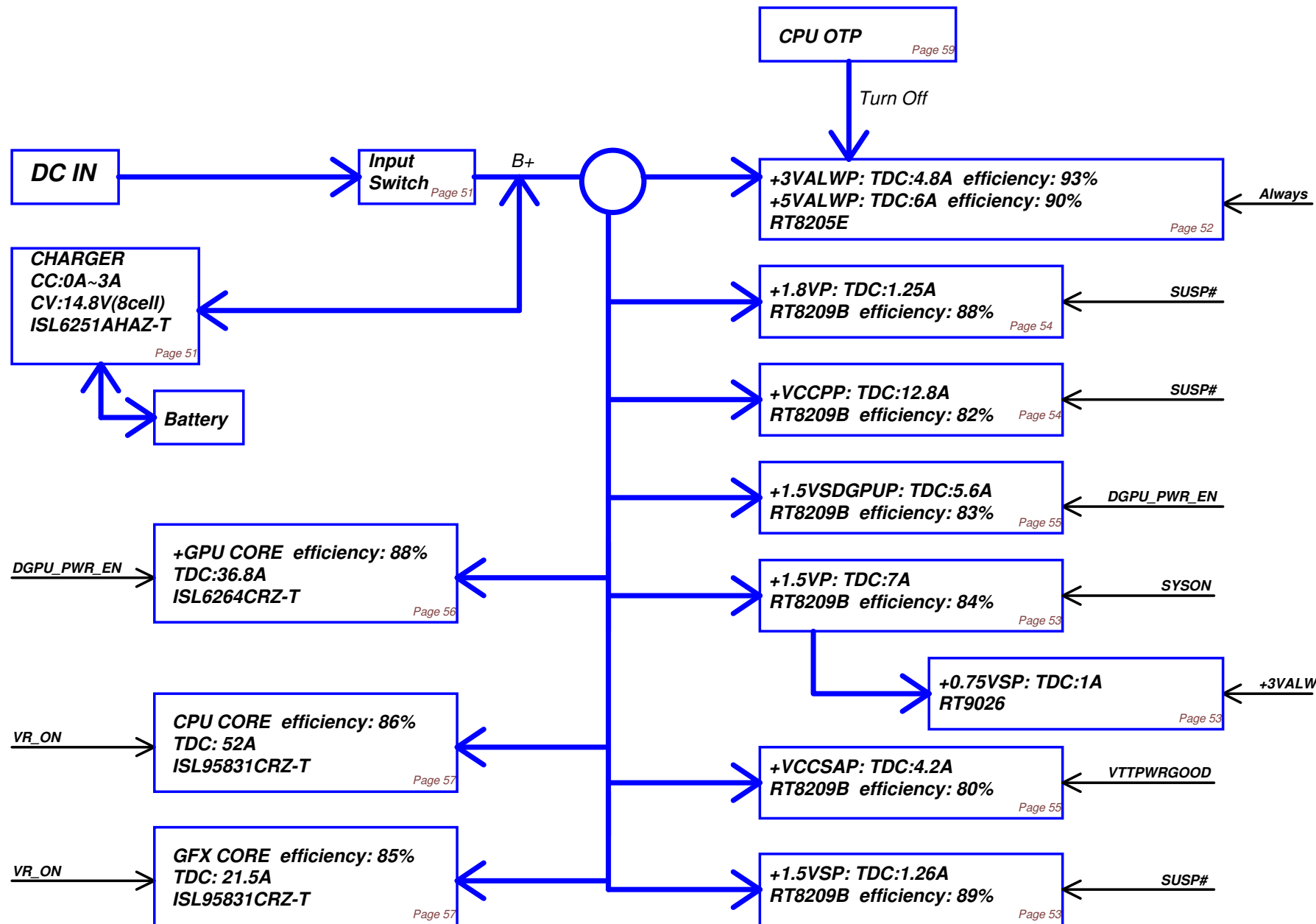




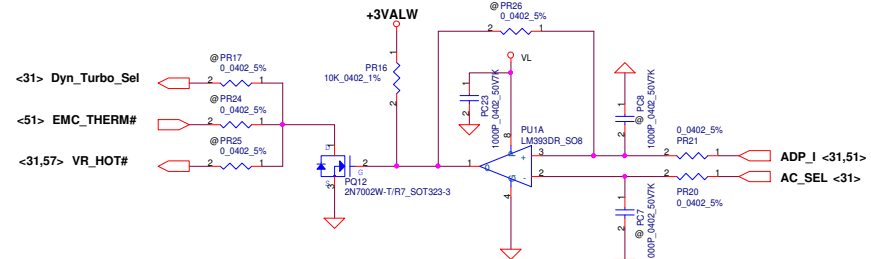
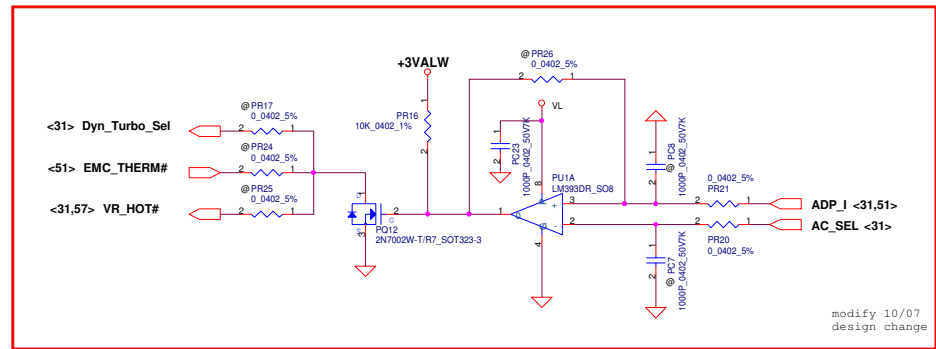
VRAM P/N :  
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)  
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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				LA-6801P				0.3			
Date				Monday, December 06, 2010				Sheet 48 of 60			

# Power block

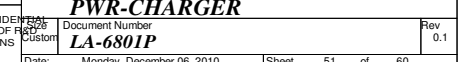


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				Sheet	49 of 60
				Rev	0.1

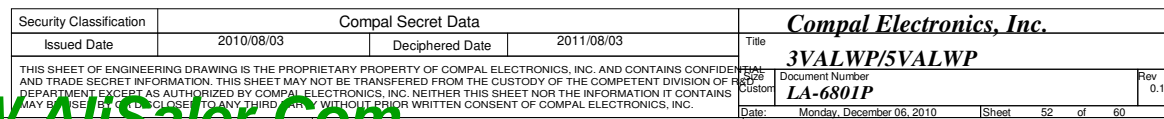


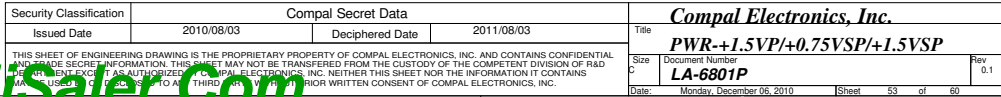
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						Document Number		Rev
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Date: Monday, December 06, 2010						Sheet 50 of 60		





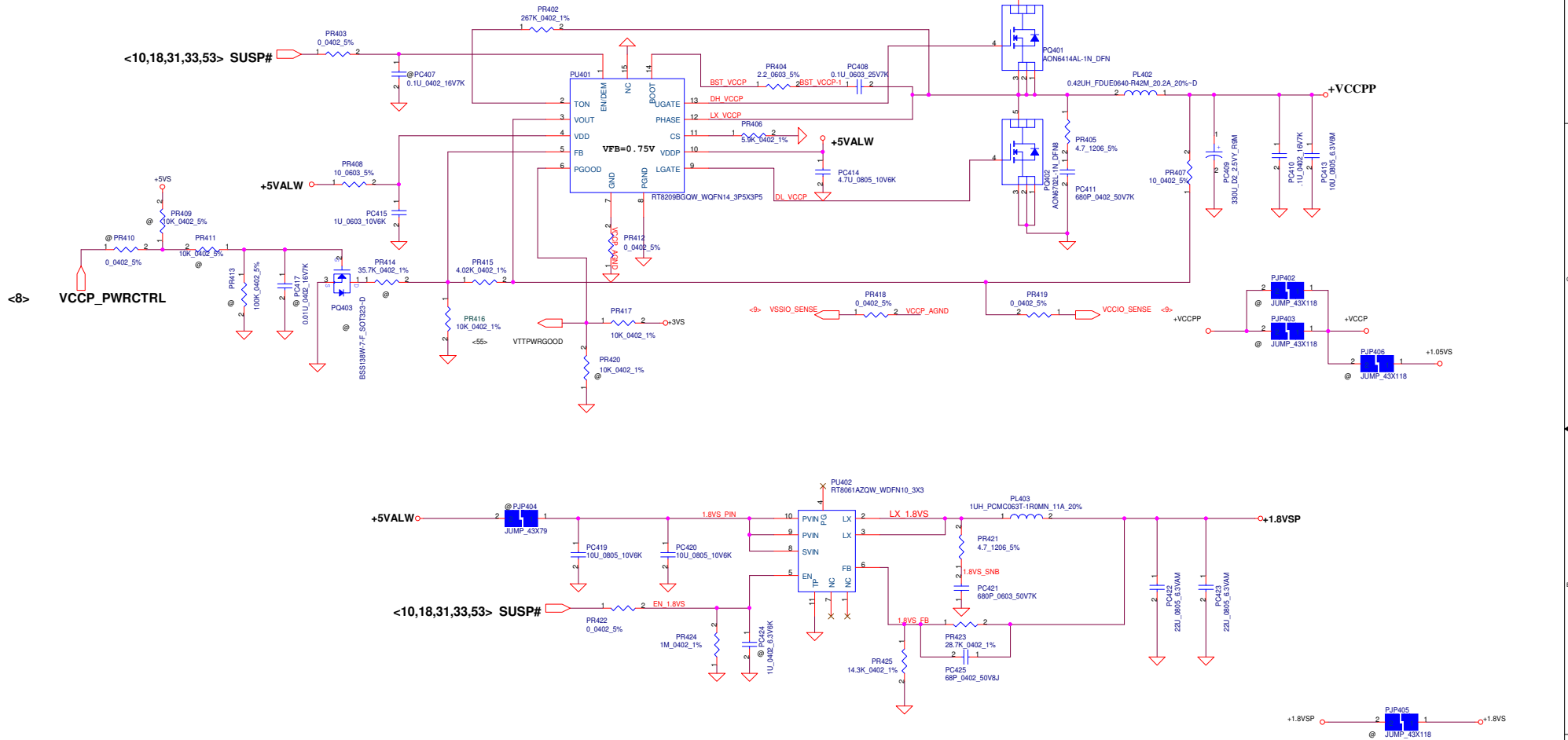
```
5VALWP
TDC 6A
Peak Current 11.24 A
OCP current 13.24 A
```





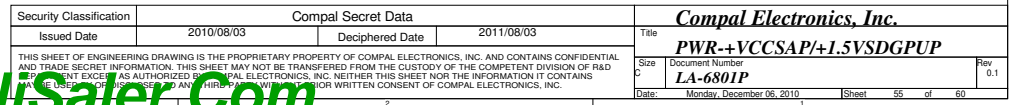
VCCPP  
TDC 12.8 A  
Peak Current 18.3 A  
OCP current 22.4 A

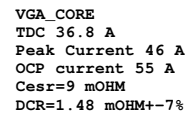
Low Side MOS RDS(on)=2.6m ohm(Typ) , 3.2m ohm(Max)

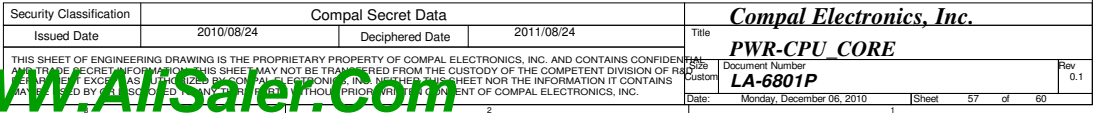


1.8VSP  
TDC 1.25 A  
Peak Current 1.75 A  
OCP current 4 A

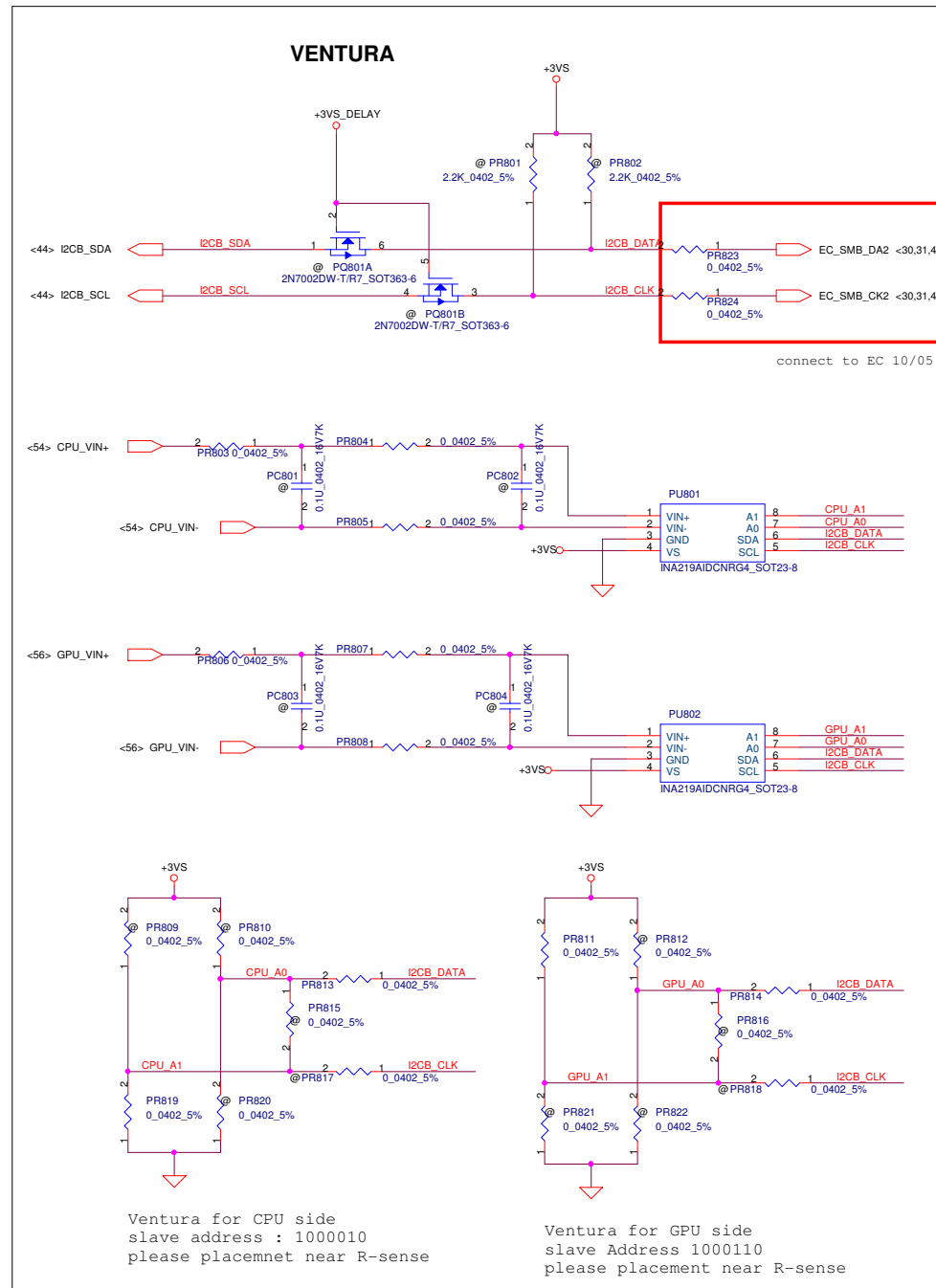
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Date: Monday, December 06, 2010				Rev 0.1
Sheet 54 of 60				











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				Date:	Monday, December 06, 2010
				Sheet	58 of 60
				Rev	0.1

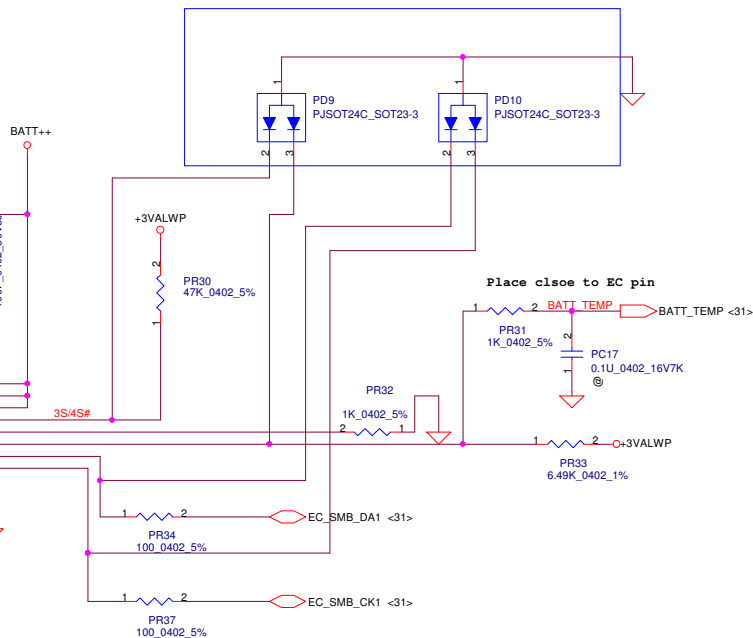
# PJP30 battery connector

## SMART Battery:

11.BAT+  
10.BAT+  
9.BAT+  
8.ID  
7.B/I  
6.TS  
5.SMD  
4.SMC  
3.GND  
2.GND  
1.GND

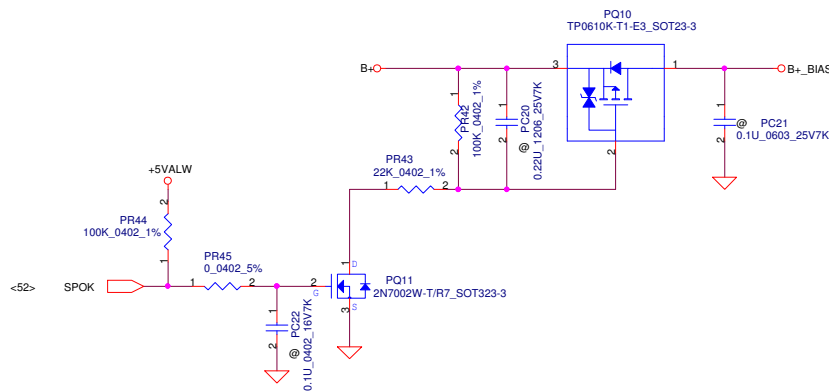
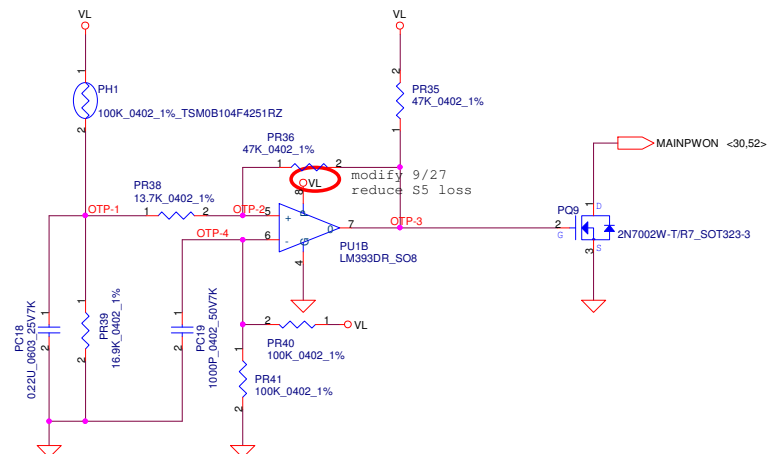
MOLEX 87437-1173 11P-T  
SP020907230

@PJP30



## Battery Connect/OTP

PH1 under CPU bottom side :  
CPU thermal protection at 90 degree C  
Recovery at 50 degree C



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				Date	Monday, December 06, 2010
				Sheet	59 of 60
				Rev	0.1

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