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MODEL NAME: NAP00
PCB NAME: LA-5811P MB
COMPAL P/N: DAA00001P00

Compal confidential

Schematics Document

Intel CULV (SFF)
Penryn + Cantiga + ICH9-M
DISCRETE VGA N11P-GS1 (Switchable Graphics)

2009-12-16

Rev: 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Title: *Cover Sheet*

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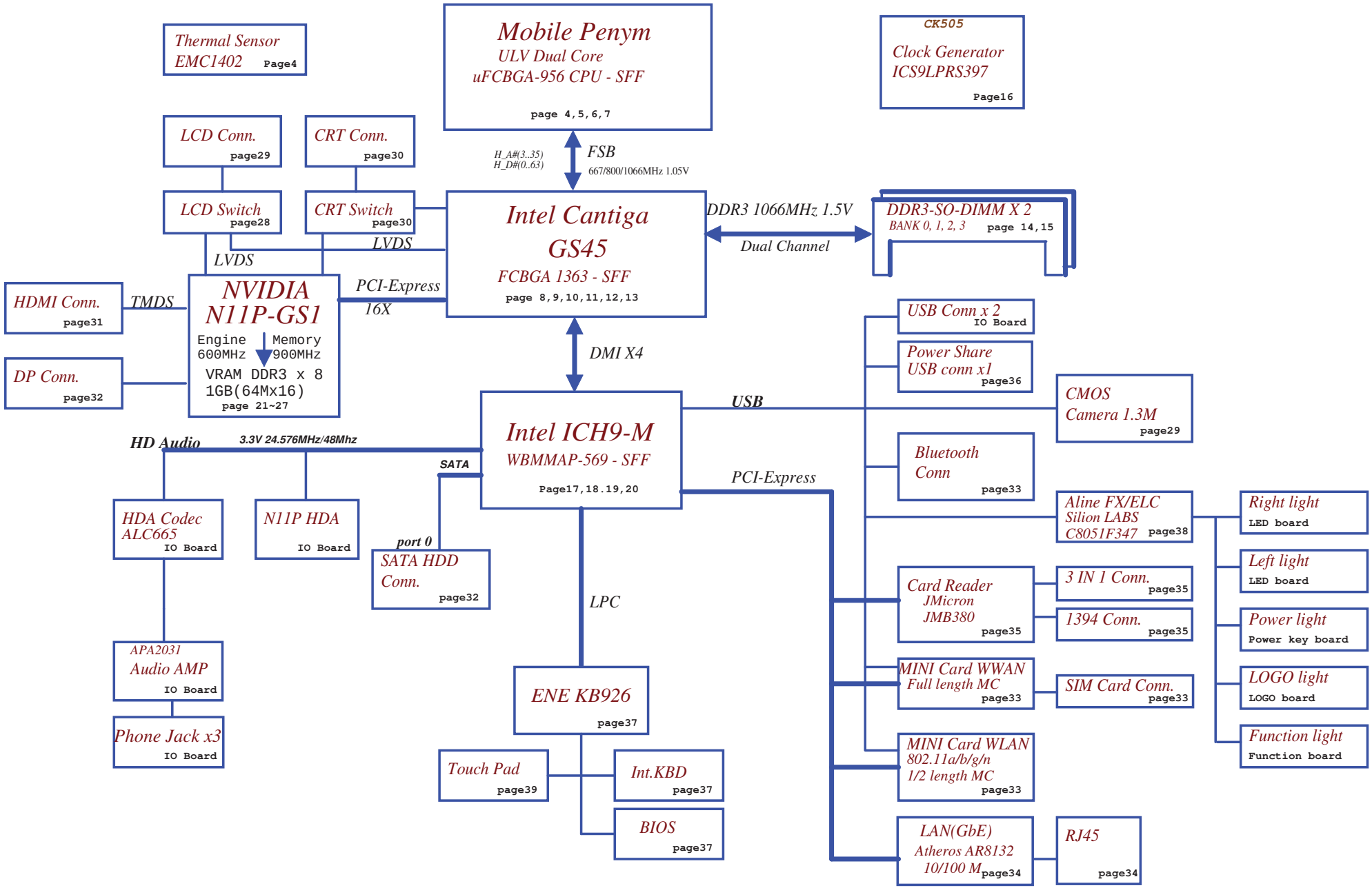
ULV



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Title: **Block Diagram**

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	B+	+5VALW +3VALW VL	+1.8V +1.5V	+5VS +3VS +0.75VS +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

I2C / SMBUS ADDRESSING

	DEVICE	HEX	ADDRESS
EC_SMB_CK1 EC_SMB_DA1	Battery		
EC_SMB_CK2 EC_SMB_DA2	CPU THERMAL SENSOR (EMC1402-1-ACZL)	4C	01001100
	GPU THERMAL SENSOR (ADM1032ARMZ)	4D	01001101
	GPU INTERNAL THERMAL SENSOR	9E	10011110
ICH_SMBCLK ICH_SMBDATA	CLOCK GENERATOR (EXT.)	D2	11010010
	Free Fall Sensor	38	00111000

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

Compal R1 PN
CPU-->SA00003I91L(S IC AV80577UG0132M SLGS4 R0 1.3G FCBGA)----->SU4100
CPU-->SA00003IA1L(S IC AV80577UG0133M SLGS6 R0 1.3G FCBGA)----->SU7300
NB-->SA00002RQ1L(S IC AC82GS45 SLB92 B3 FCBGA 1363)----->45180131L03,45180131L04
SB-->SA00001YC4L(S IC AM82801IUX SLB8N A FCBGA 569P ICH9M)-->45180131L03,45180131L04
VRAM-->SA00003240L(S IC D3 64M16 H5TQ1G63BFR-12C FBGA 96P)-->45180131L03,45180131L04
VRAM-->SA00003570L(S IC D3 64M16 K4W1G1646E-HC12 FBGA 96P)-->45180131L03,45180131L04
Compal R3 PN
CPU-->SA00003I92L(S IC AV80577UG0132M SLGS4 R0 1.3G A31!)----->SU4100
CPU-->SA00003IA2L(S IC AV80577UG0133ML SLGYV R0 1.3G A31!)----->SU7300
NB-->SA00002RQ0L(S IC AC82GS45 SLB92 B3 FCBGA 1363 A31 !)----->45180131L01,45180131L02
SB-->SA00001YC3L(S IC AM82801IUX SLB8N A FCBGA ICH9M A31!)-->45180131L01,45180131L02
VRAM-->SA00003241L(S IC D3 64M16 H5TQ1G63BFR-12C FBGA A31!)-->45180131L01,45180131L02
VRAM-->SA00003571L(S IC D3 64M16 K4W1G1646E-HC12 FBGA A31!)-->45180131L01,45180131L02

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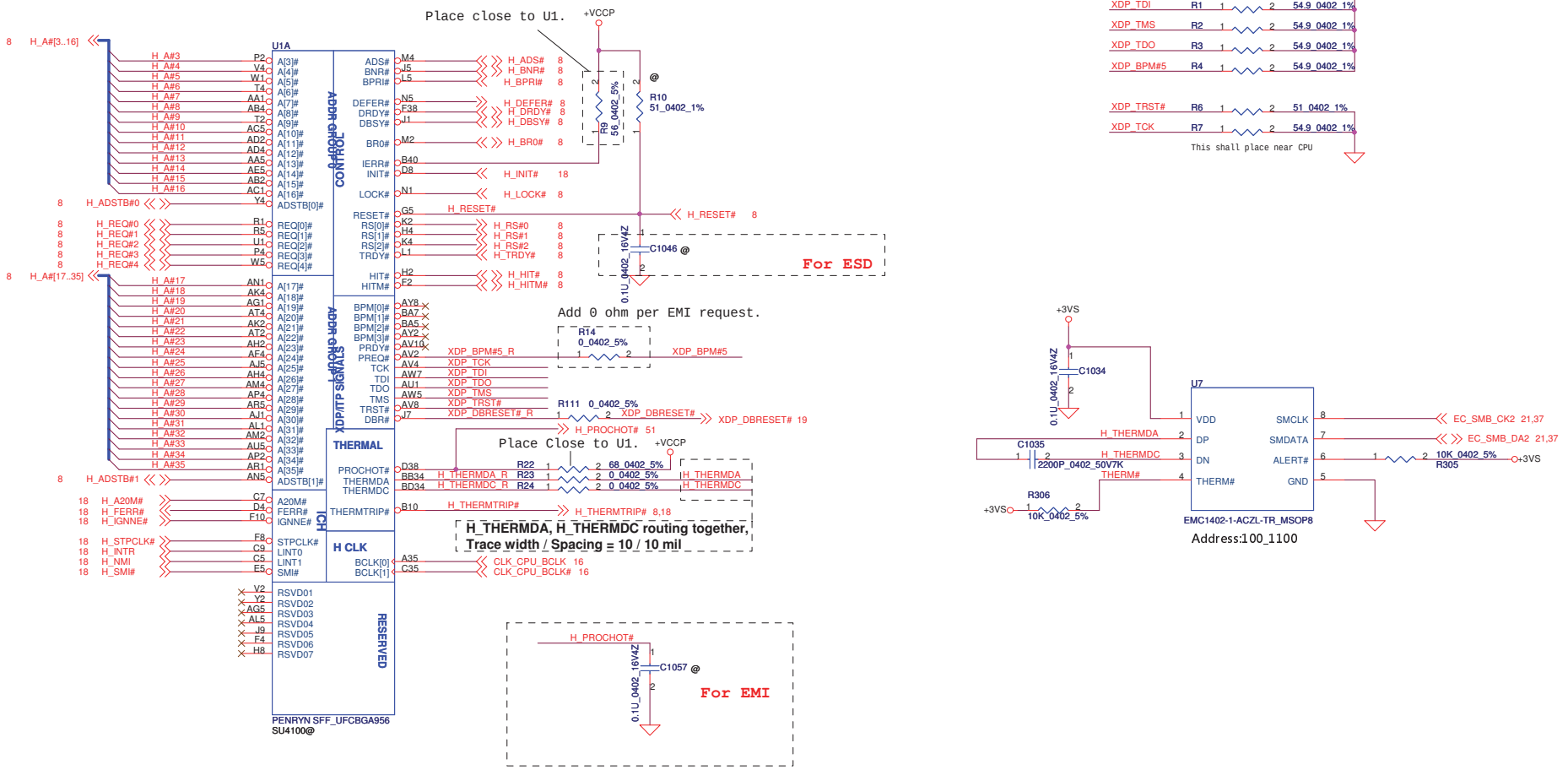

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Title: Penryn(1/4)-AGTL+/ITP-XDP

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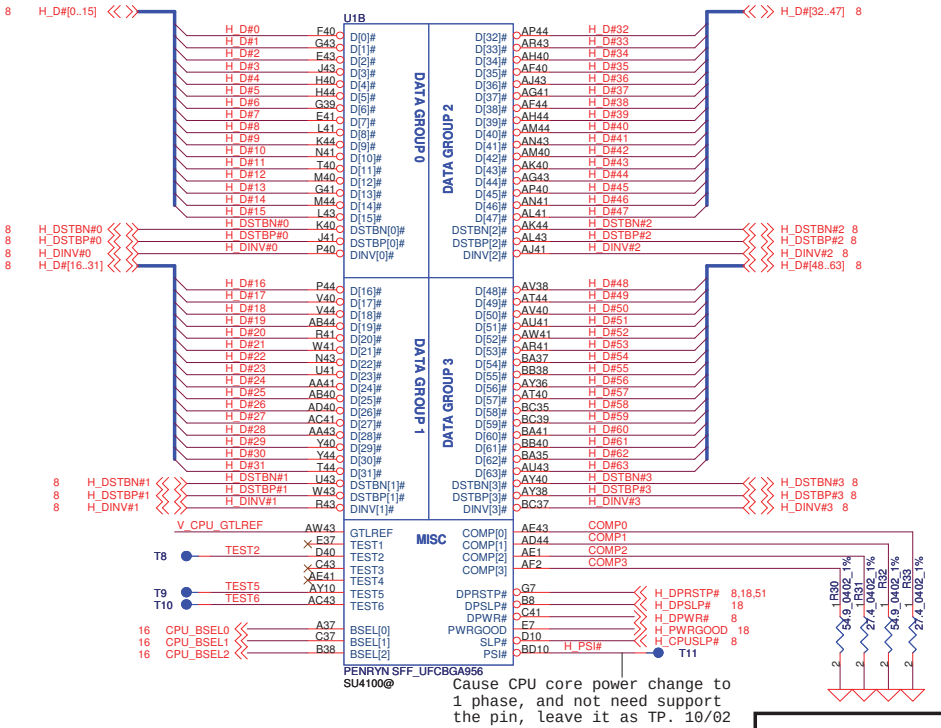
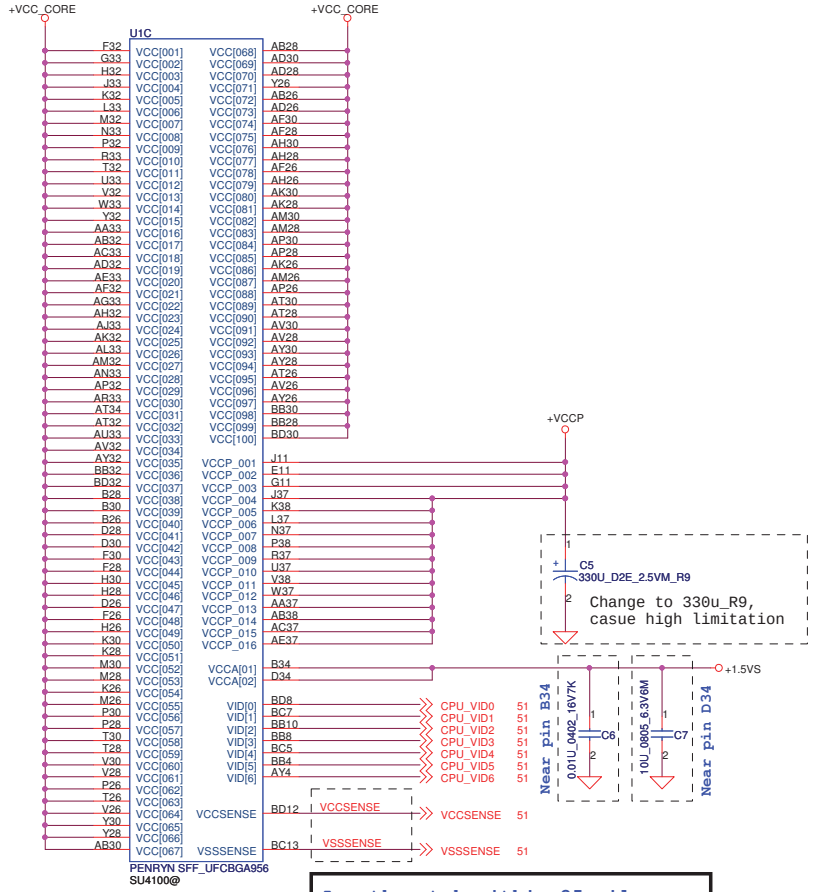


Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

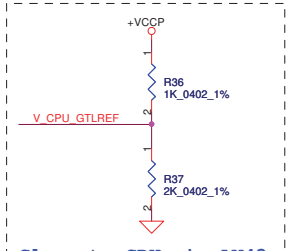
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

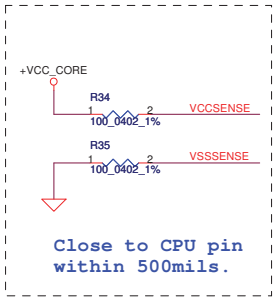
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AW43 within 500mils.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: Penryn(2/4)-AGTL+/ITP-XDP

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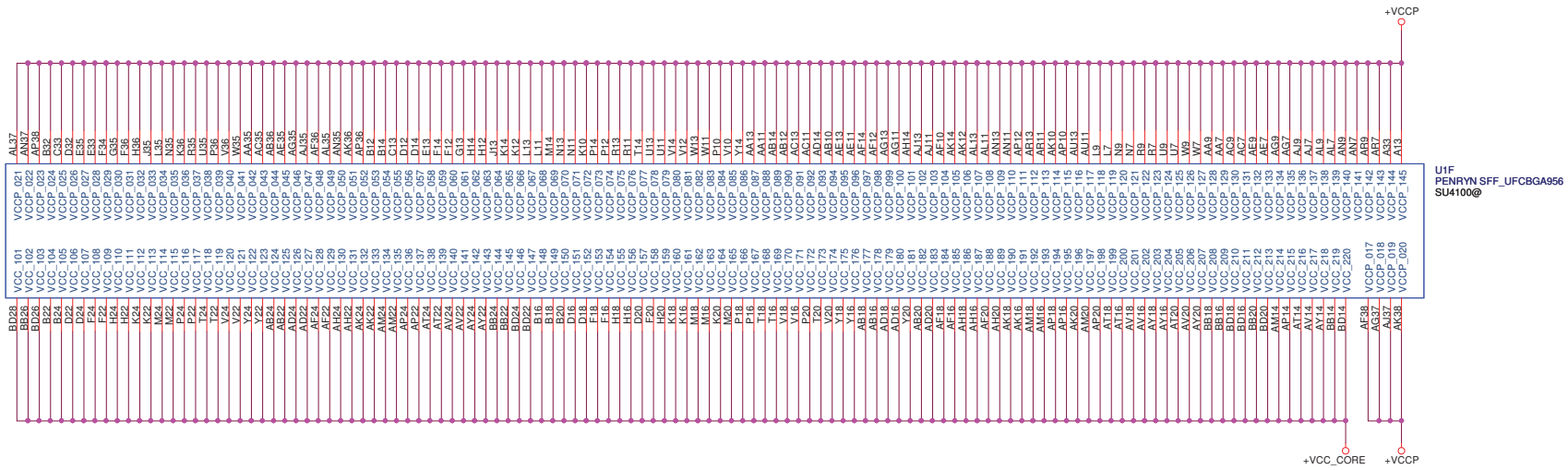

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Compal Electronics, Inc.

Title: **Penryn(3/4)-Power**

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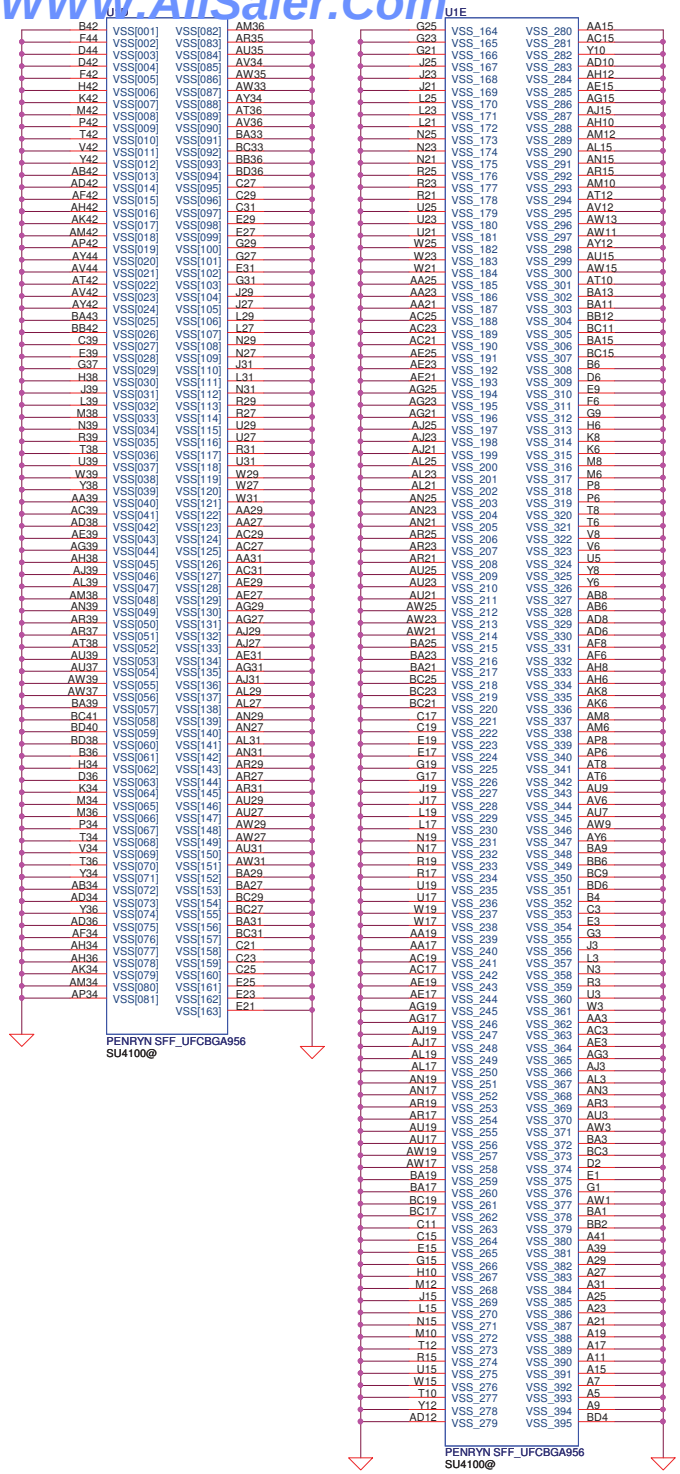

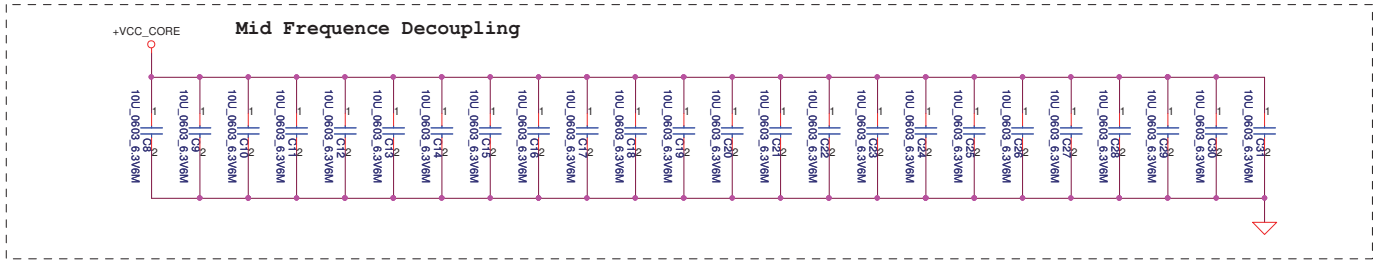

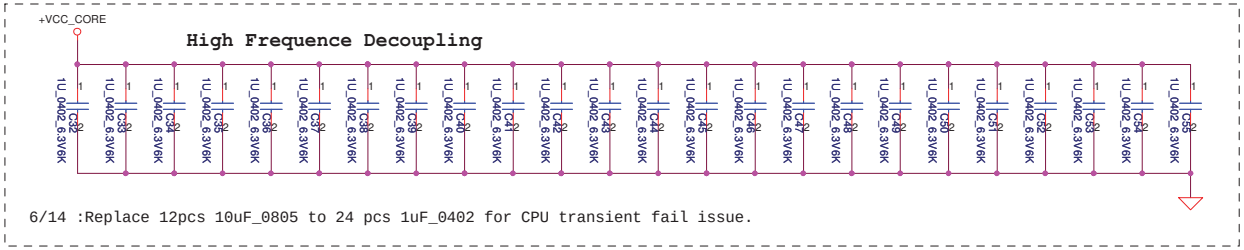

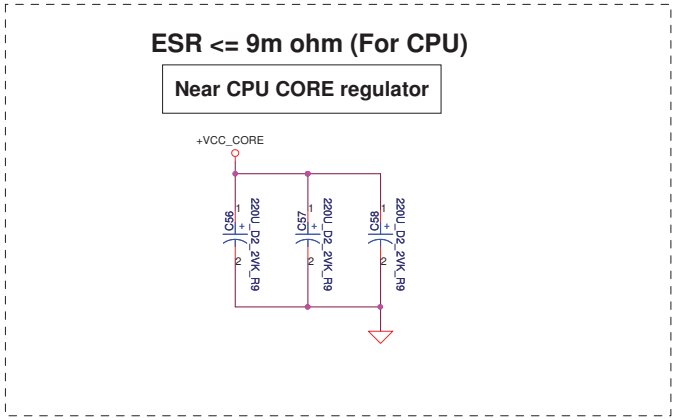

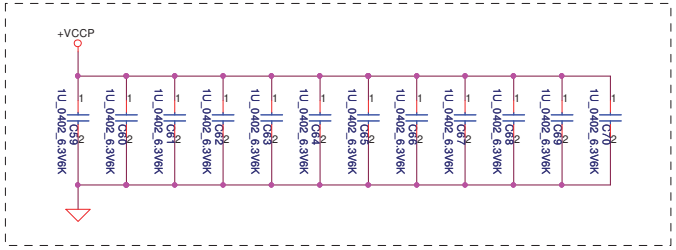

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Title	Compal Electronics, Inc.		
	Penryn(4/4)-GND/Bypass		
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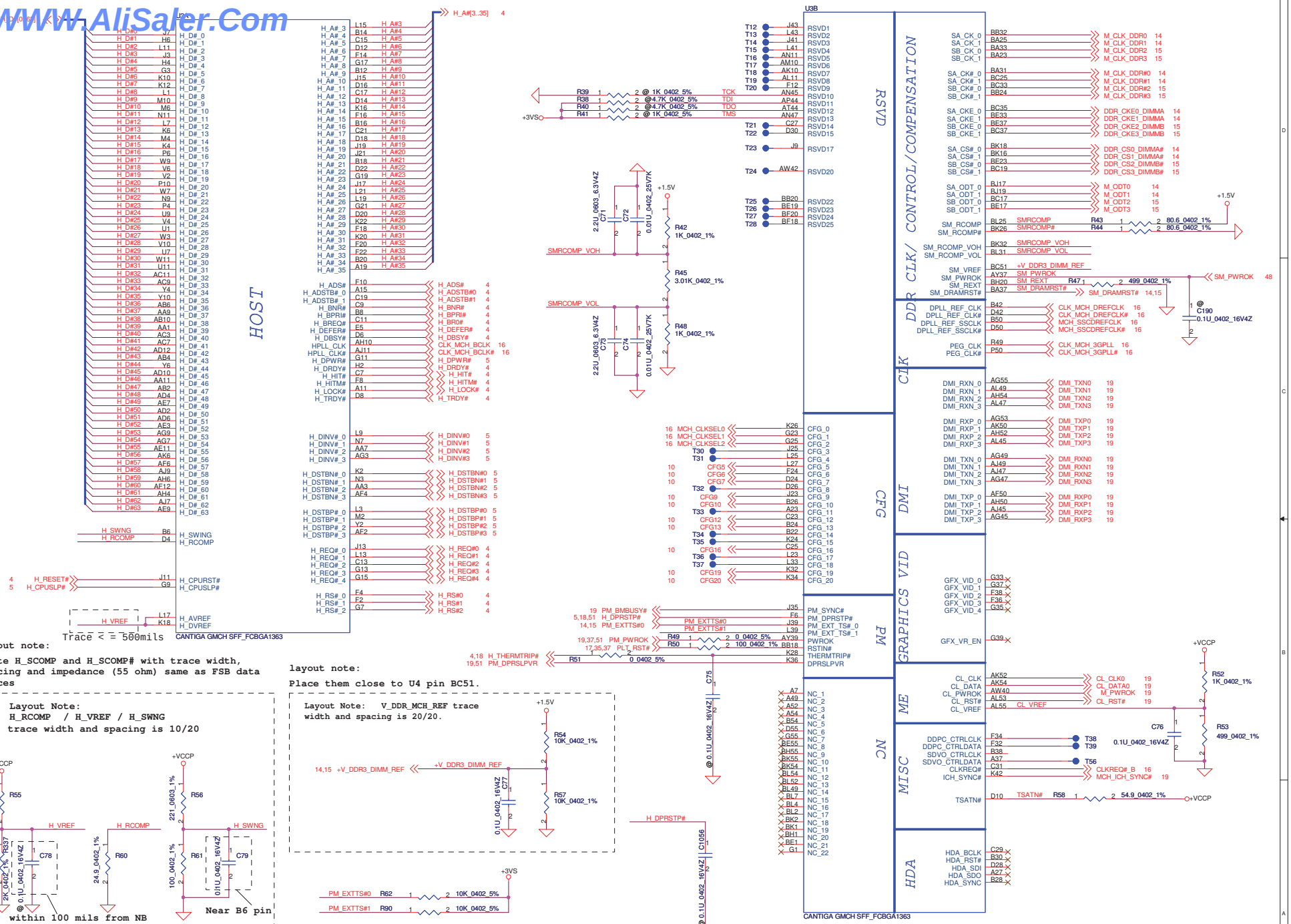

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Title: **Cantiga(1/6)-AGTL/DMI/DDR**

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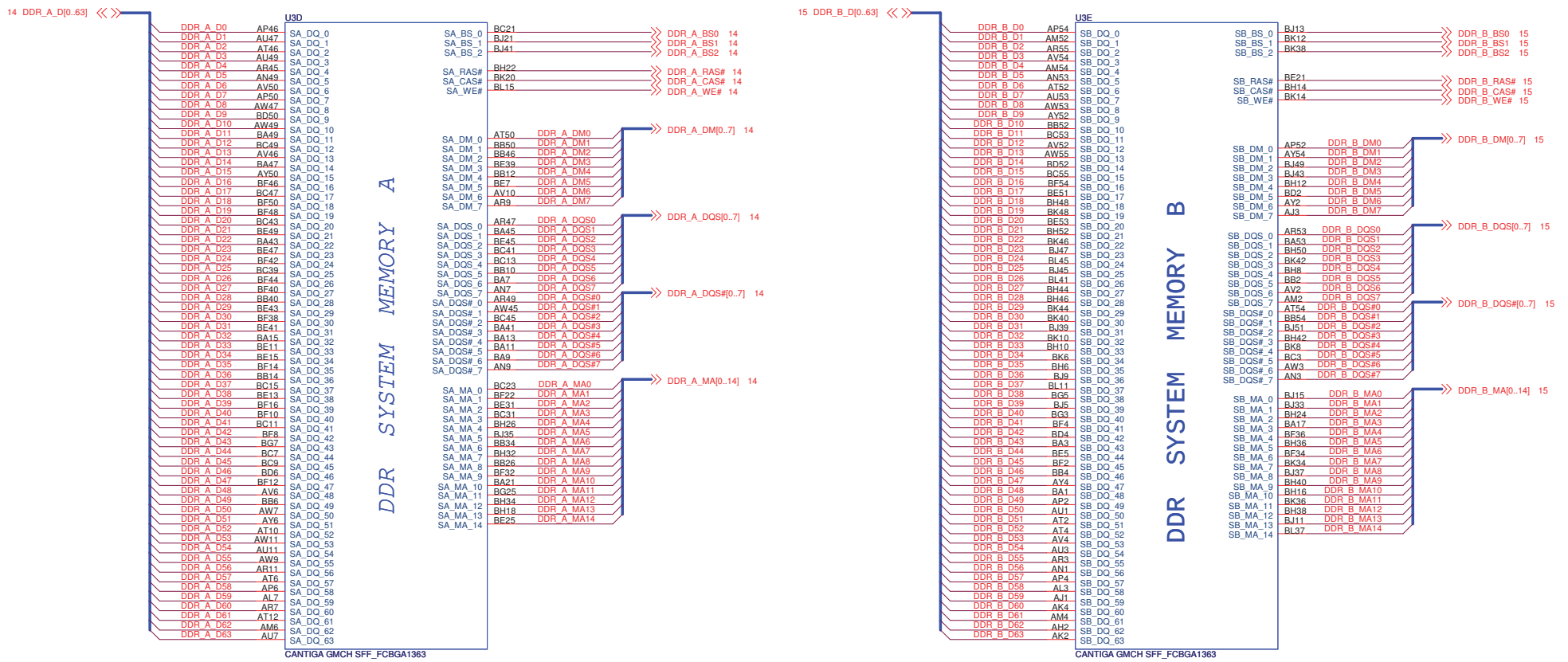

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Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

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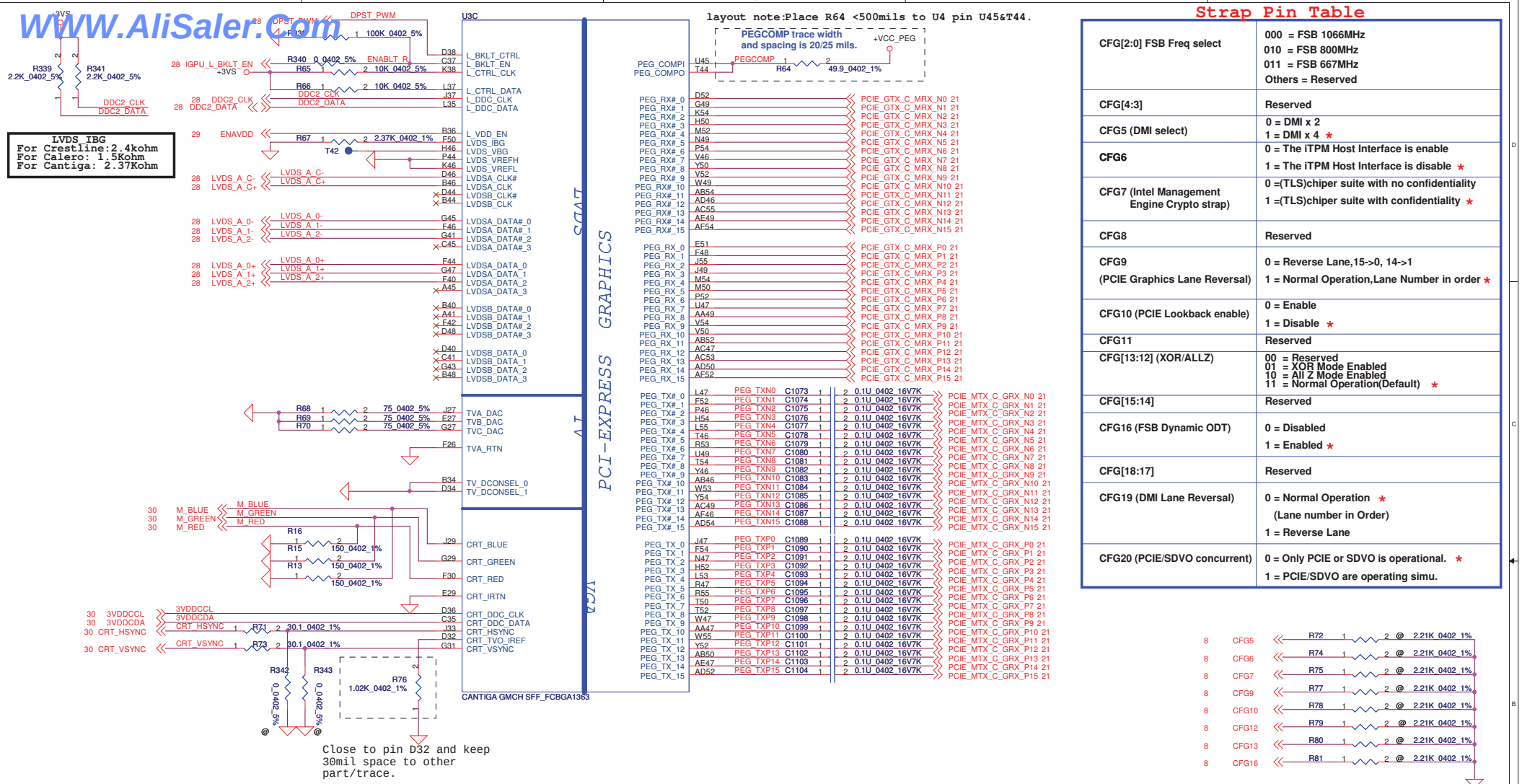

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 ★
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable ★
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality ★
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order ★
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable ★
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) ★
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled ★
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation ★ (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. ★ 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga(3/6)-VGA/LVDS/TV**

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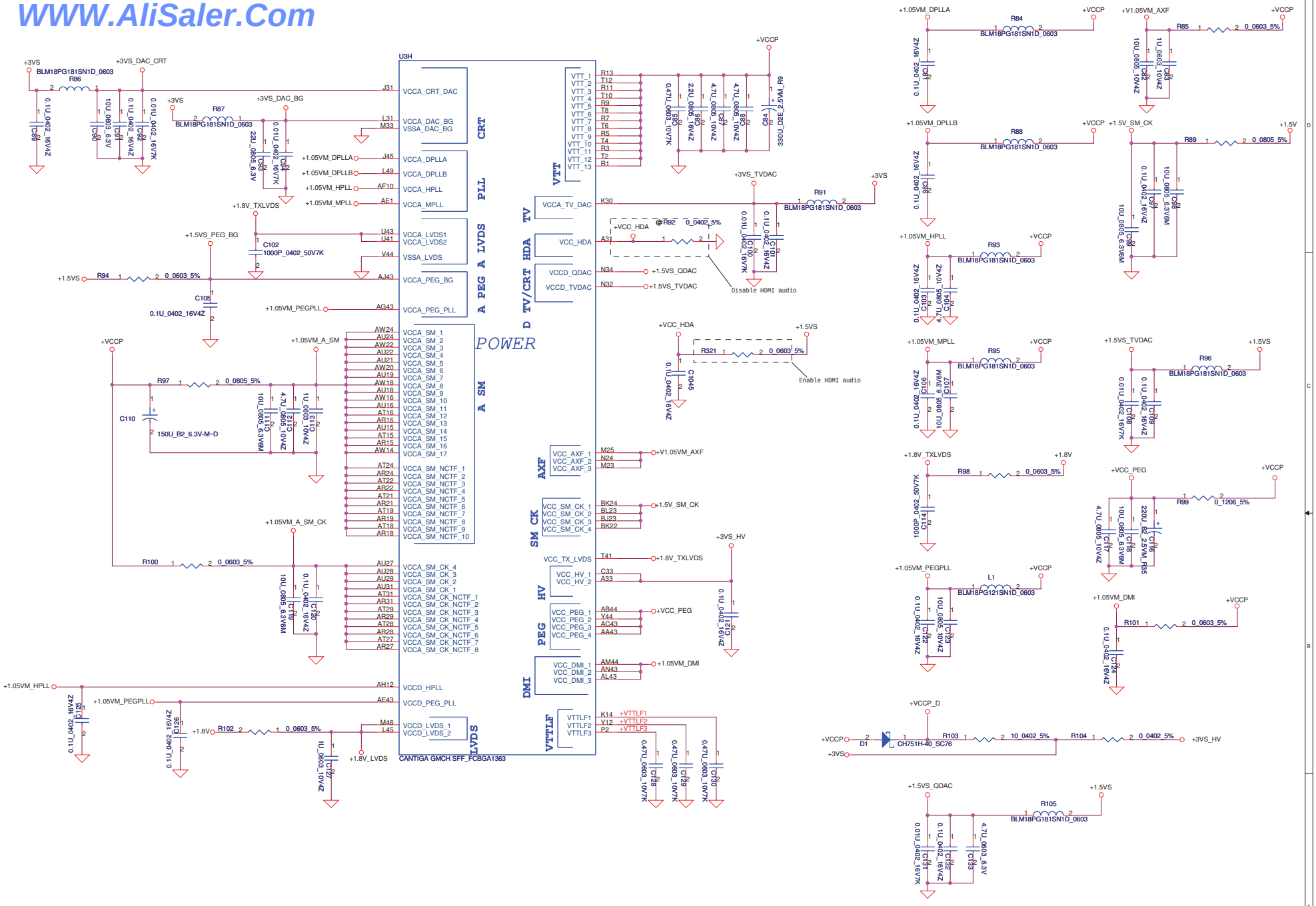

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Title: **Cantiga(4/6)-PWR**

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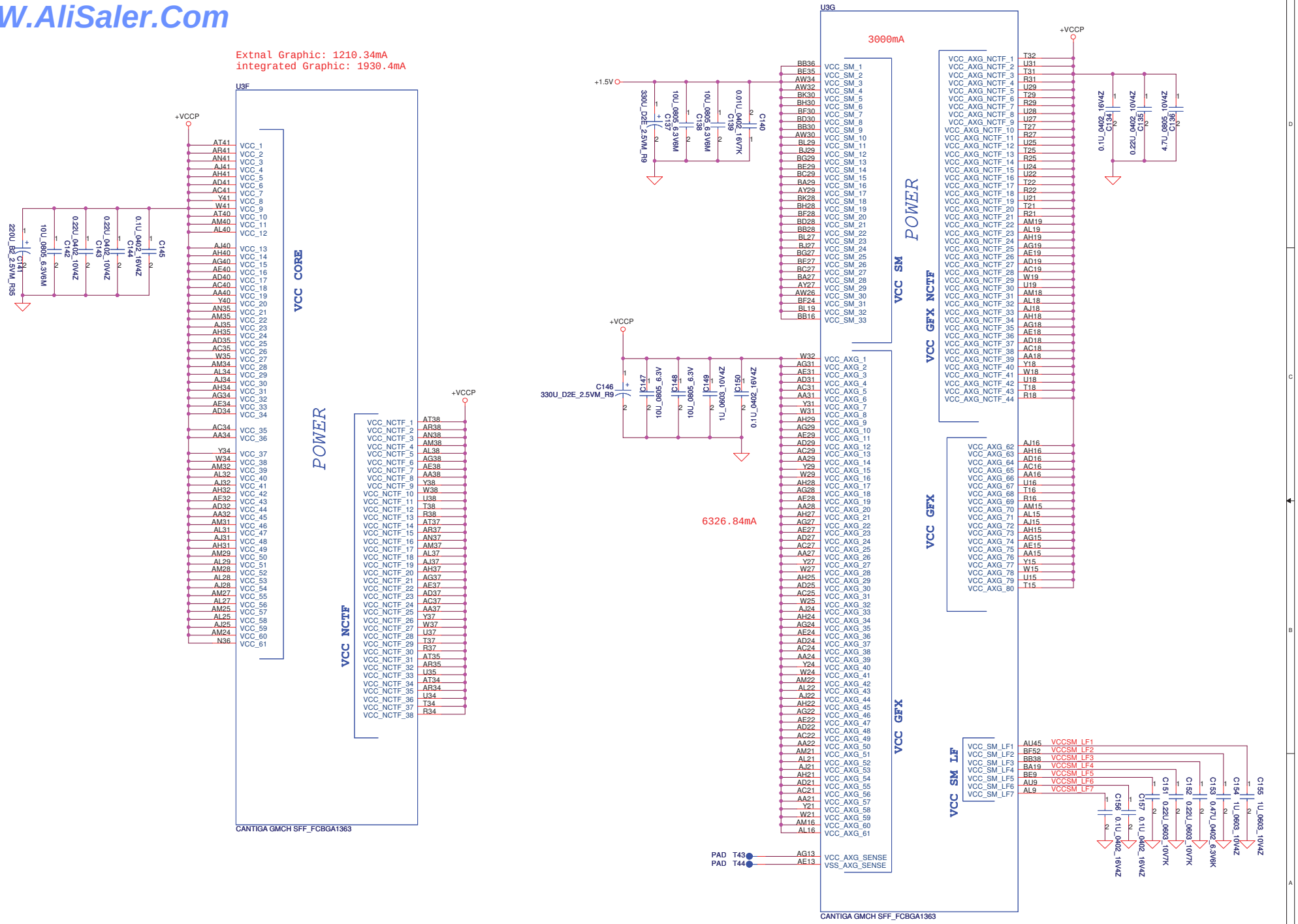

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Title: **Cantiga(5/6)-PWR/GND**

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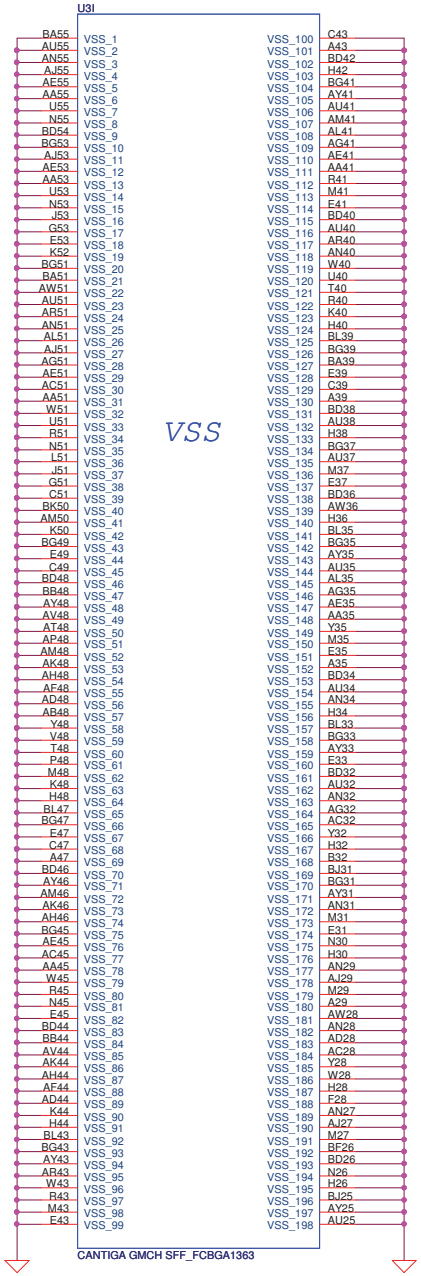

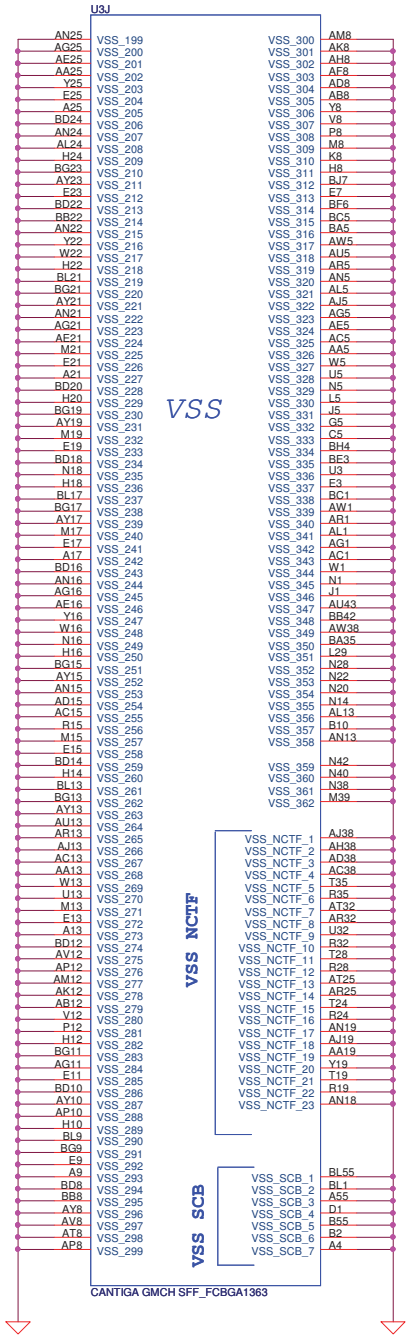

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Title: **Cantiga(6/6)-PWR/GND**

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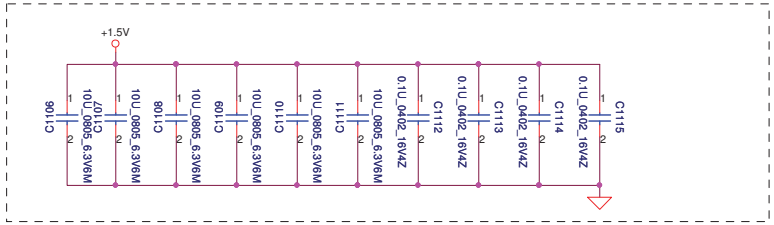
9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]

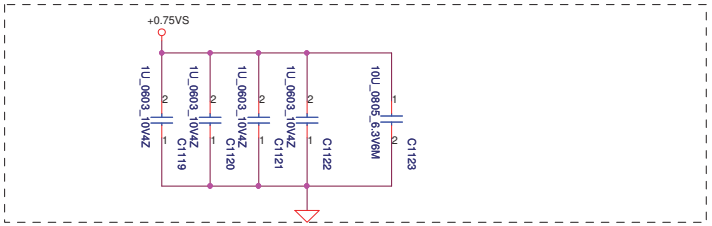
+1.5V
C115
1000P_0402_50V7K
Add C115 for EMI request

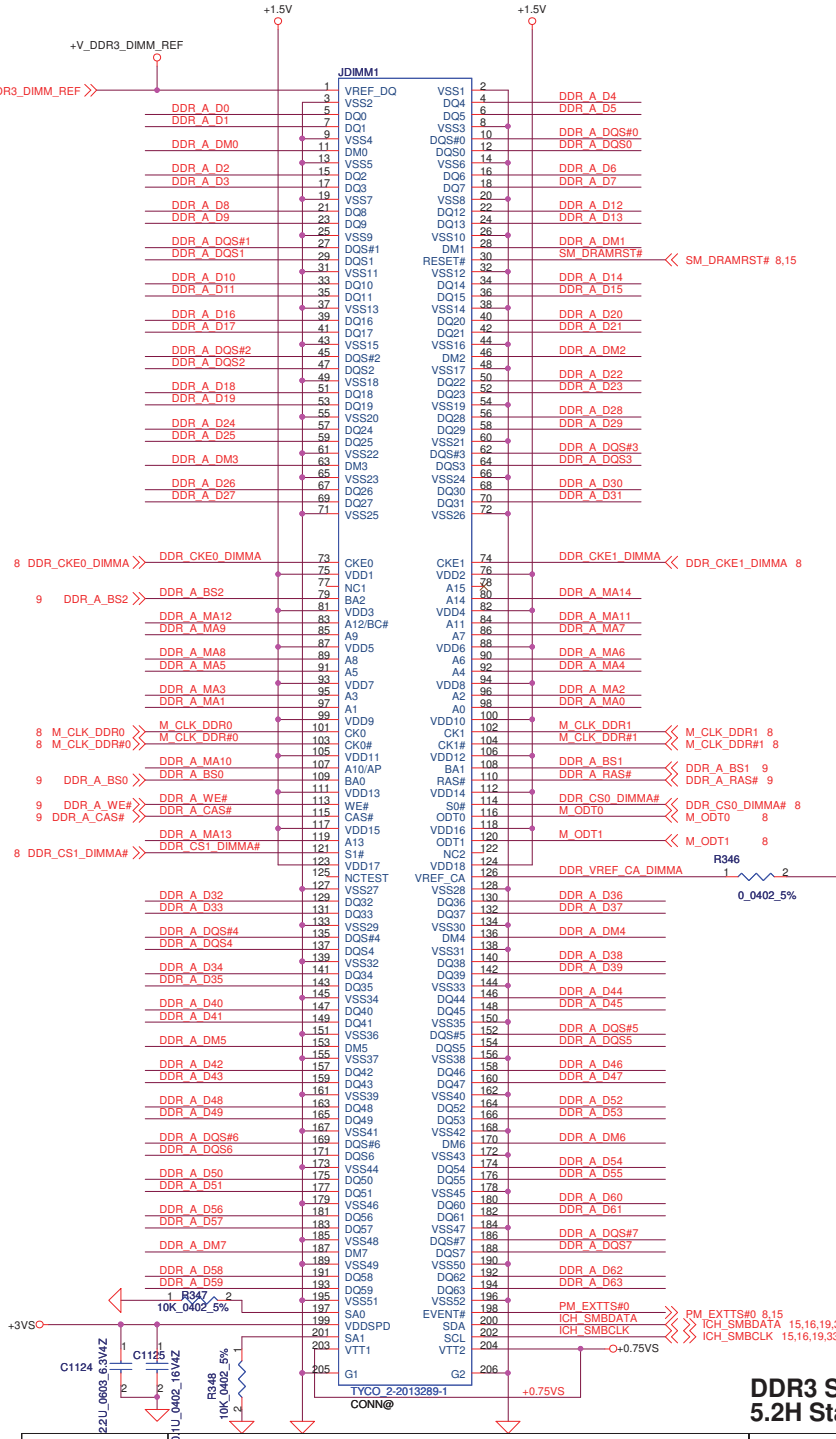
Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDIMM1.203 & JDIMM1.204





DDR3 SO-DIMM A
5.2H Standard

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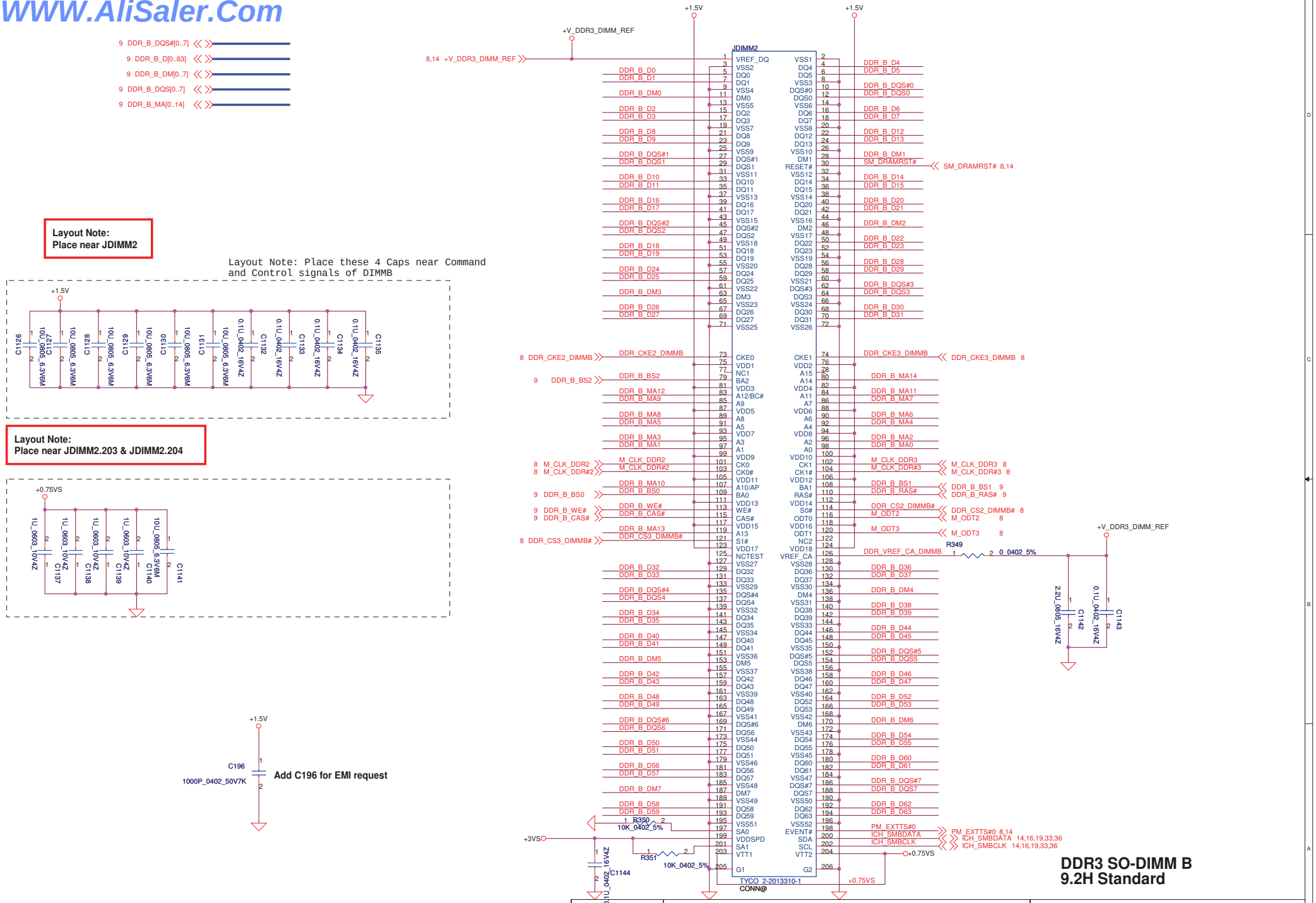

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Compal Electronics, Inc.

Title: DDR3-SODIMM B

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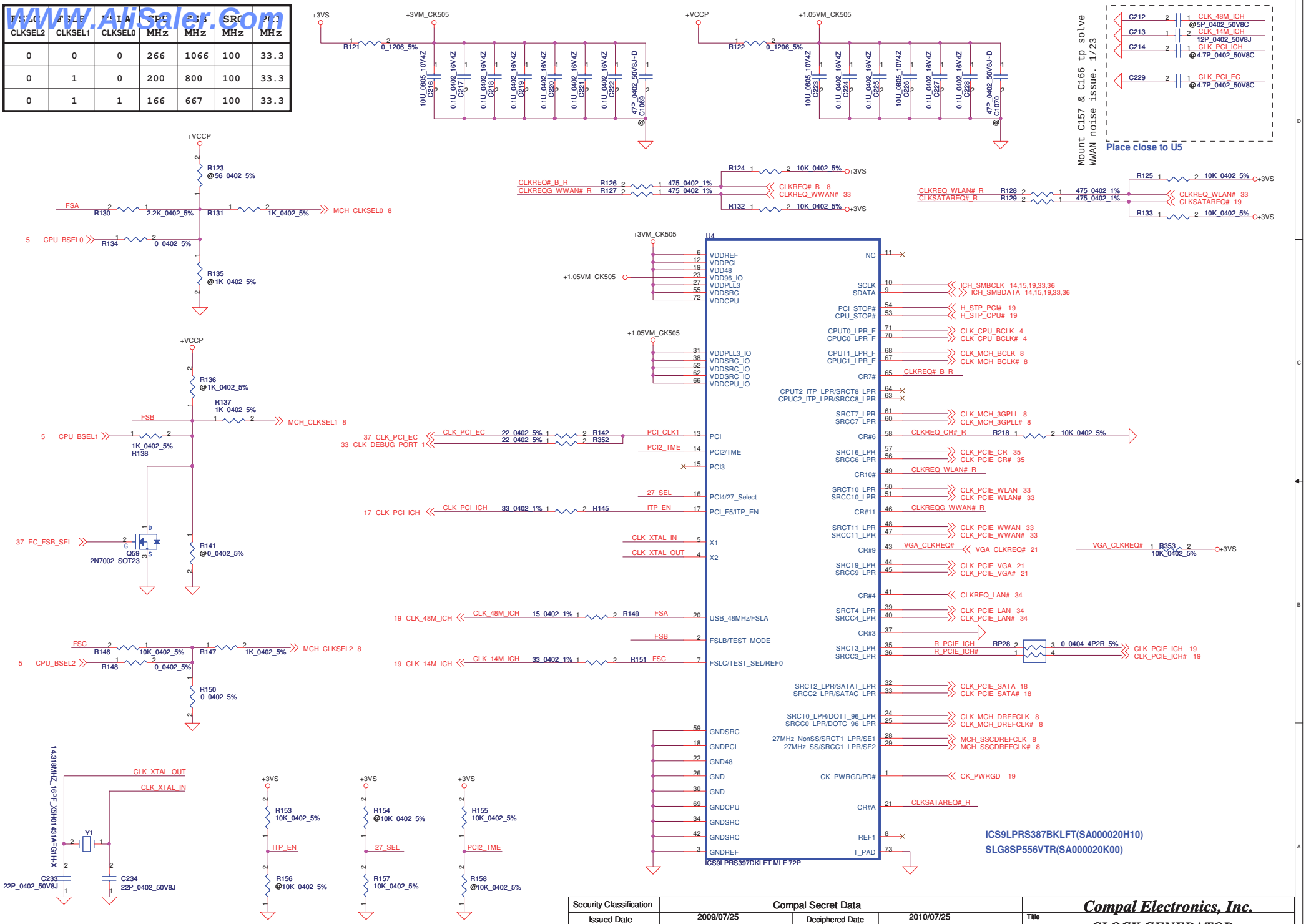
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	3V66 MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



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Compal Electronics, Inc.

Title: CLOCK GENERATOR

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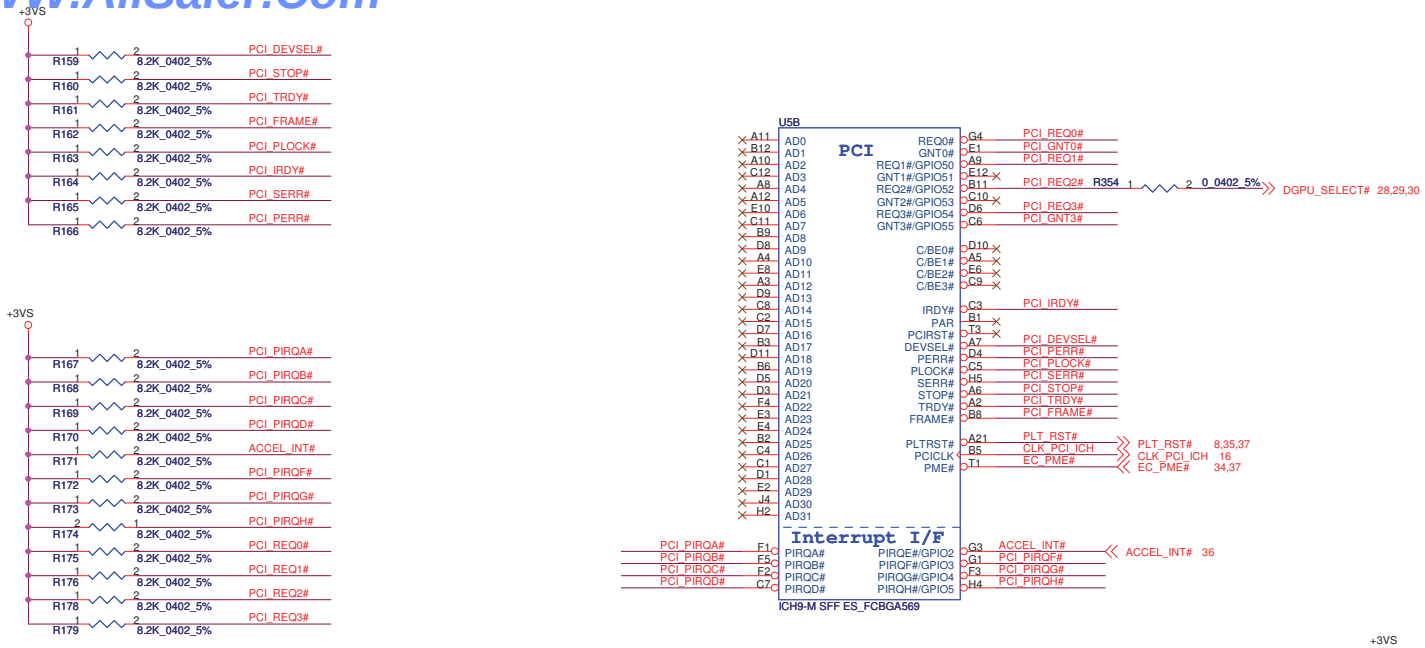
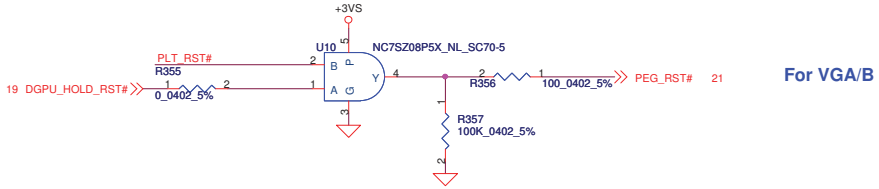
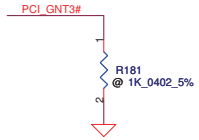


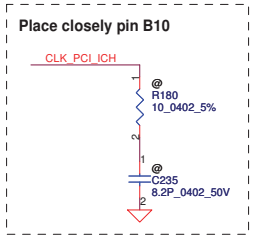


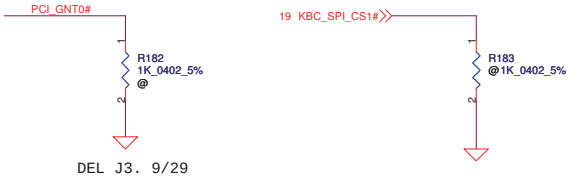
For VGA/B

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





DEL J3. 9/29

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Compal Electronics, Inc.

Title: ICH9(1/4)-PCI/INT

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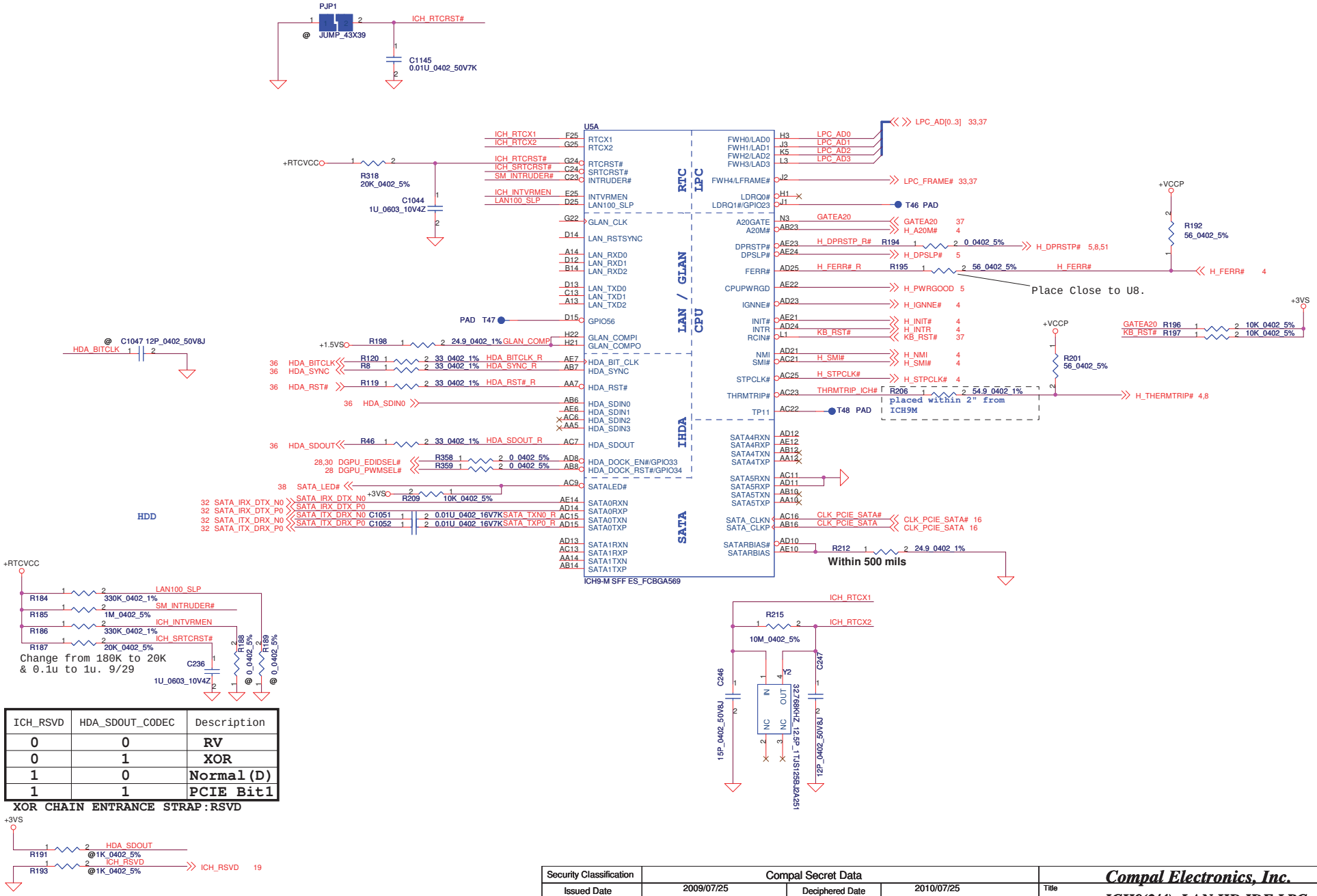
RTC Reset SW



ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal(D)
1	1	PCIE Bit1

XOR CHAIN ENTRANCE STRAP:RSVD

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Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

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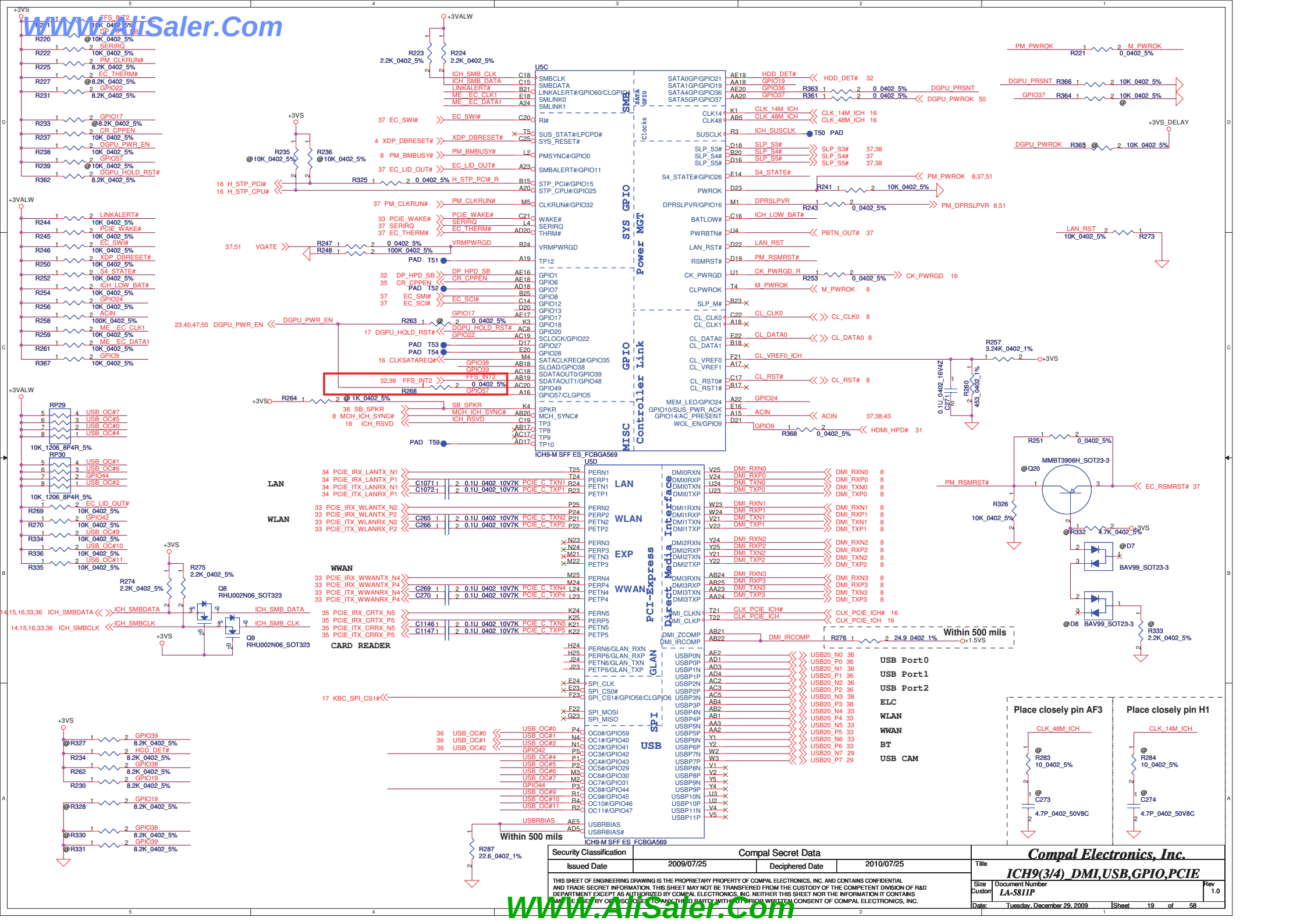

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Compal Electronics, Inc.

Title: ICH9(3/4)_DMI,USB,GPIO,PCIE

Size: Custom | Document Number: LA-5811P | Rev: 1.0

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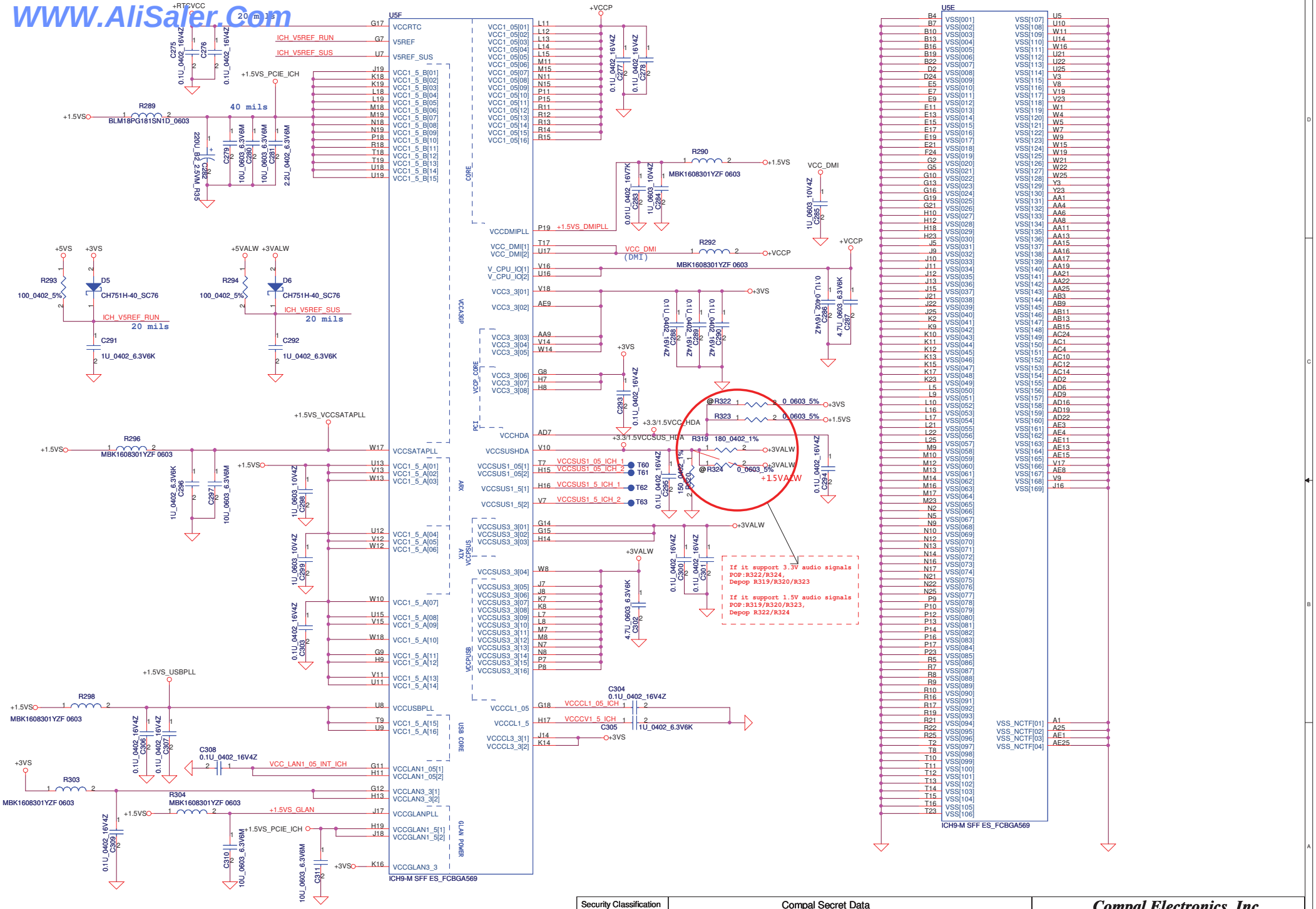

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Compal Electronics, Inc.

Title: ICH9(4/4)_POWER&GND

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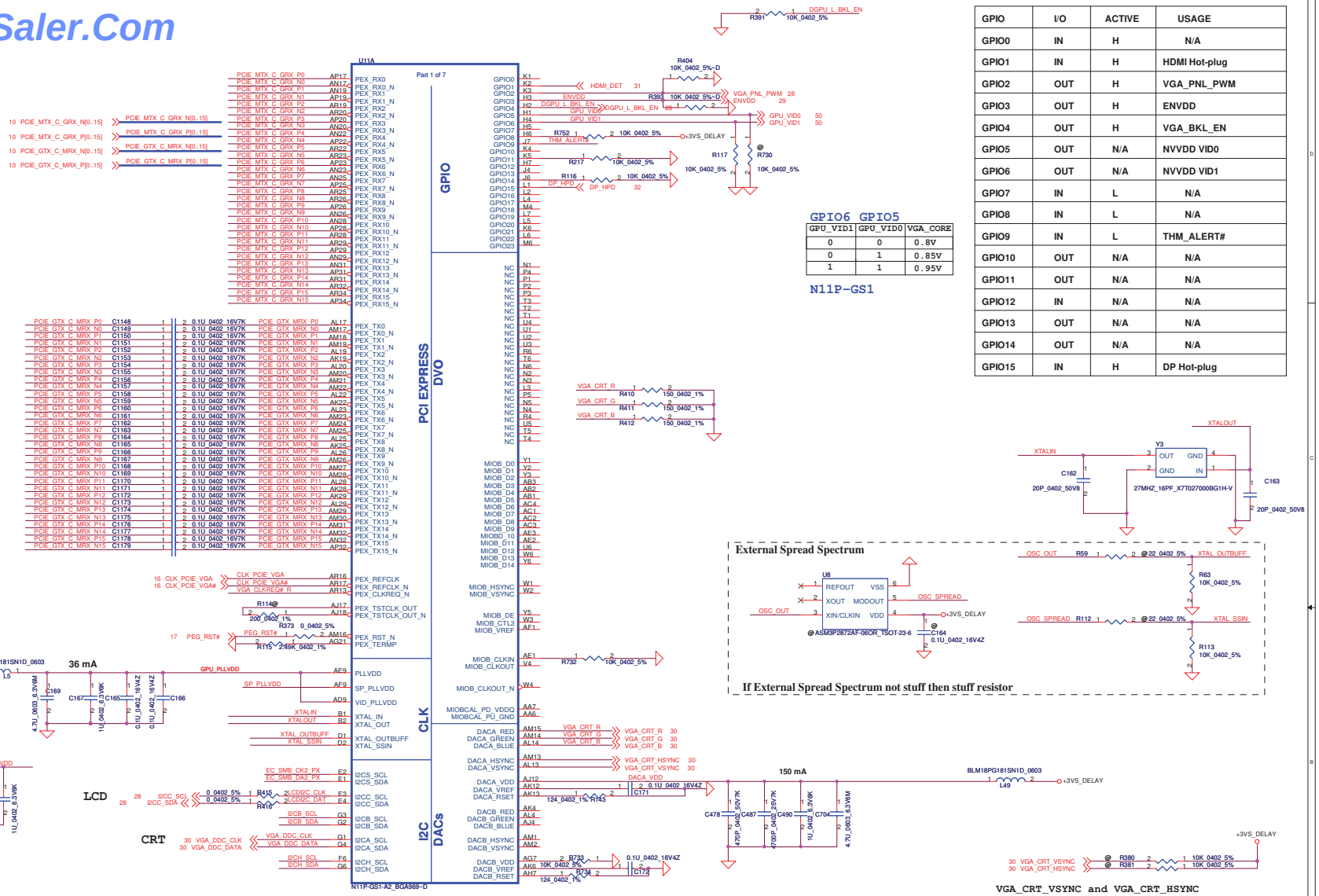

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	H	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	IN	L	N/A
GPIO8	IN	L	N/A
GPIO9	IN	L	THM_ALERT#
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A
GPIO15	IN	H	DP Hot-plug

GPIO6 GPIO5

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.8V
0	1	0.85V
1	1	0.95V

N11P-GS1

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Compal Electronics, Inc.

Title: N11P-GS1(1/5)PCIE/STRAPS/THERM

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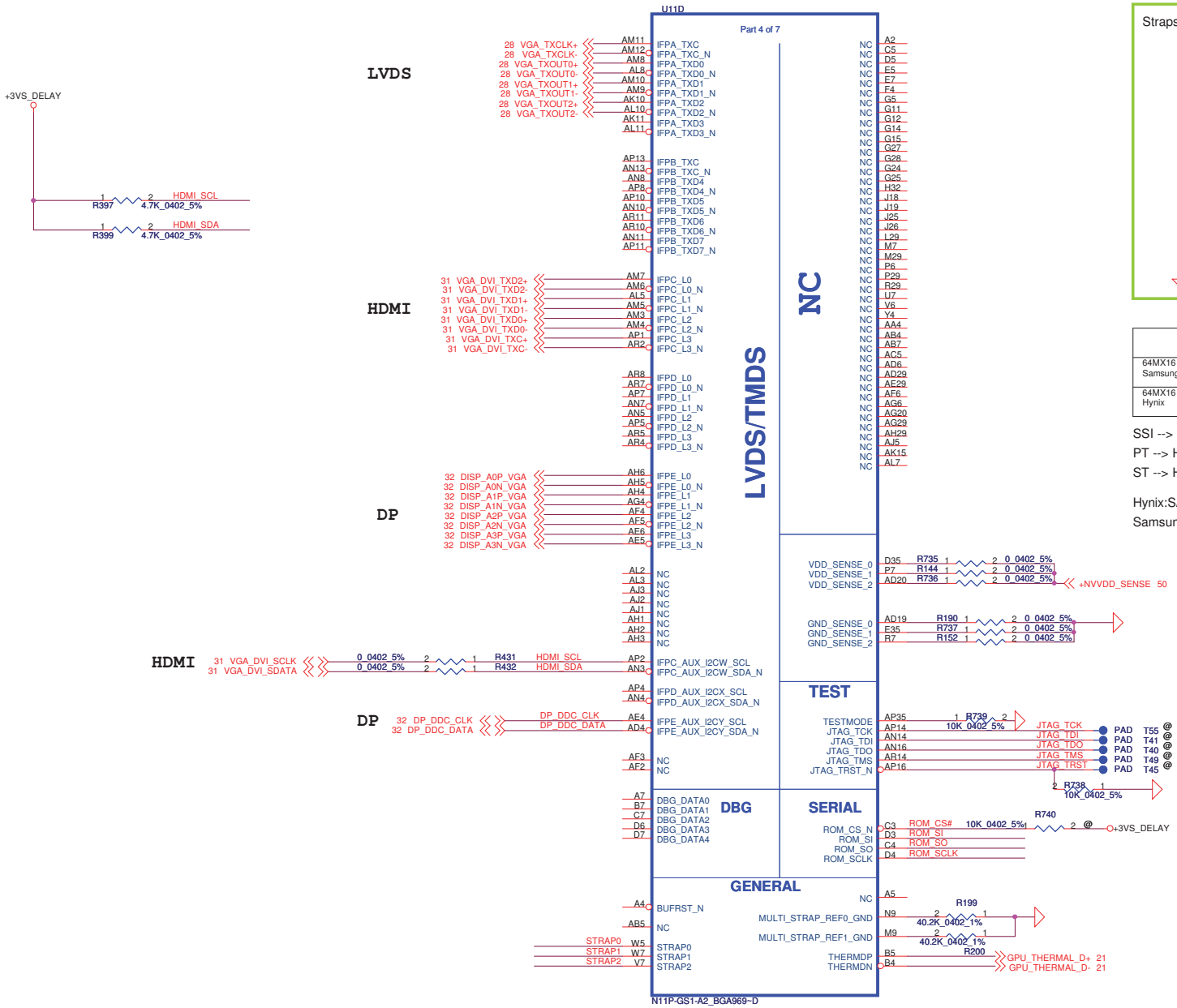

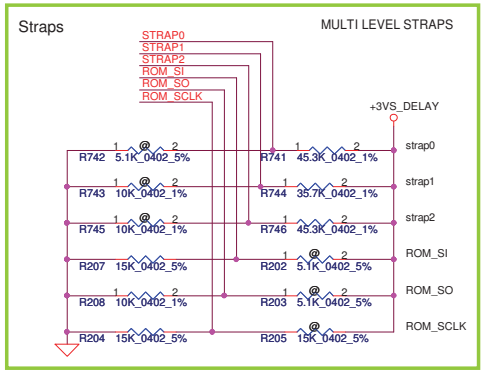

	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K

SSI --> Hynix

PT --> Hynix

ST --> Hynix(main),Samsung(second)

Hynix:SA0000032400

Samsung:SA0000035700

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Compal Electronics, Inc.

Title: N11P-GS1(2/5) IO

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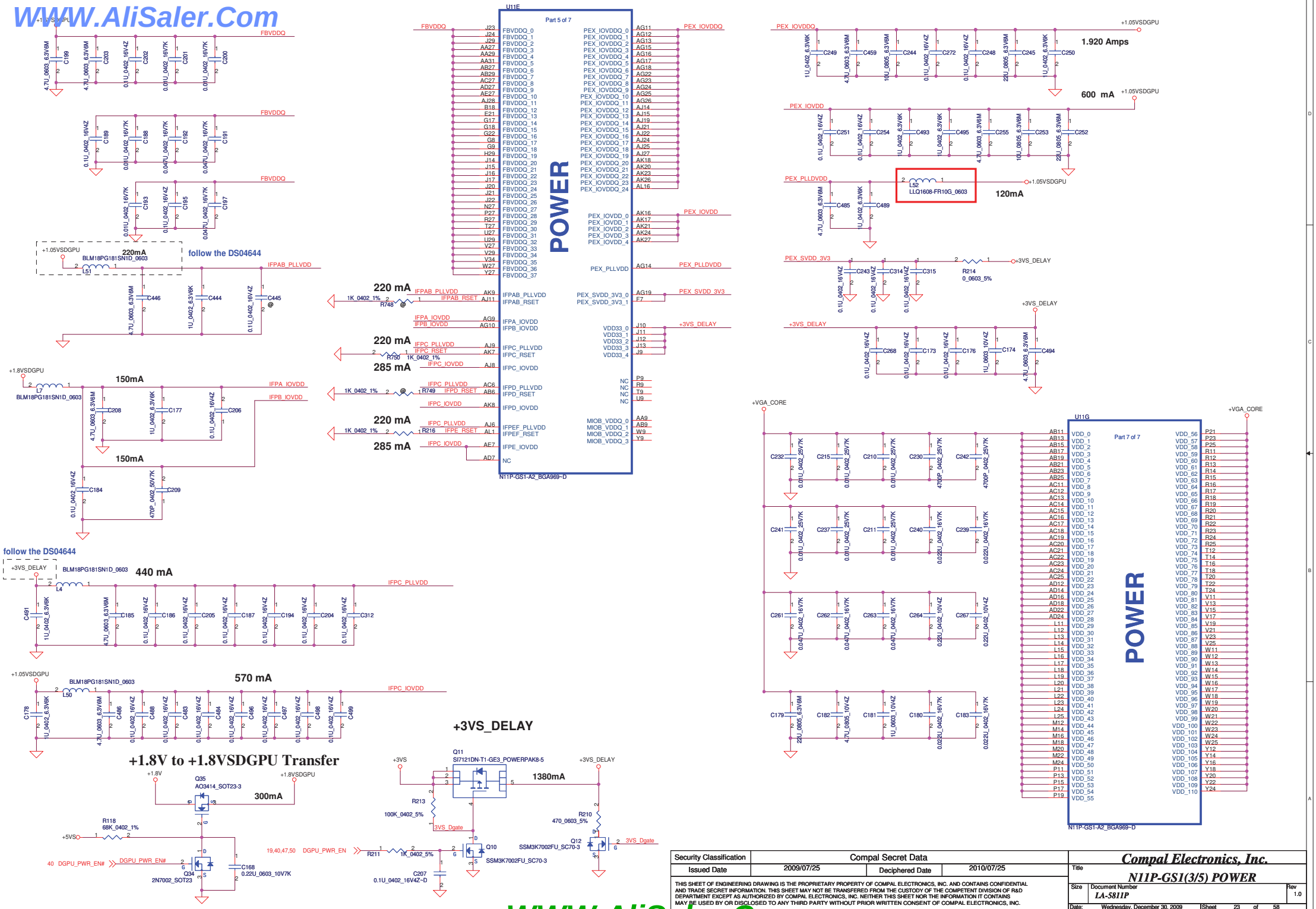

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Compal Electronics, Inc.

Title: N11P-GS1(3/5) POWER

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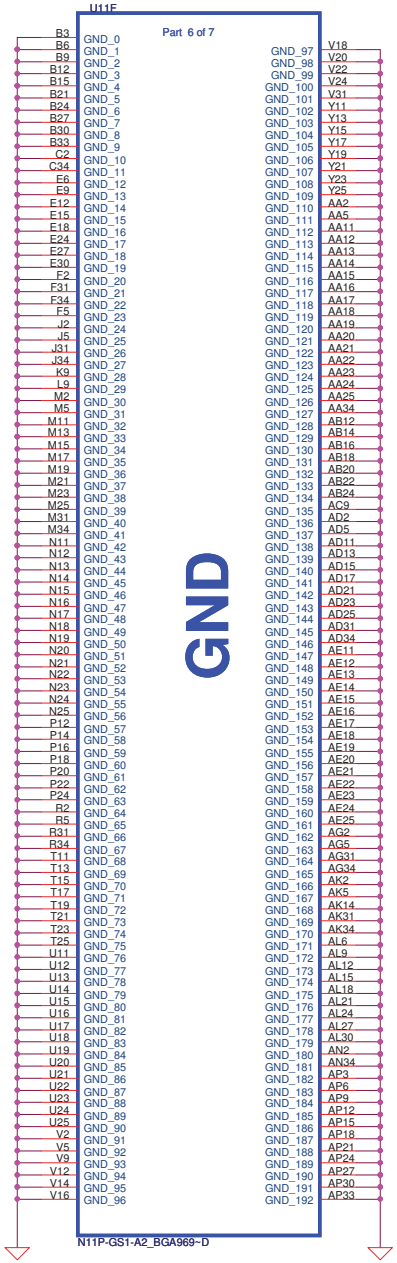

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Compal Electronics, Inc.

Title: **N11P-GS1(4/5) GND**

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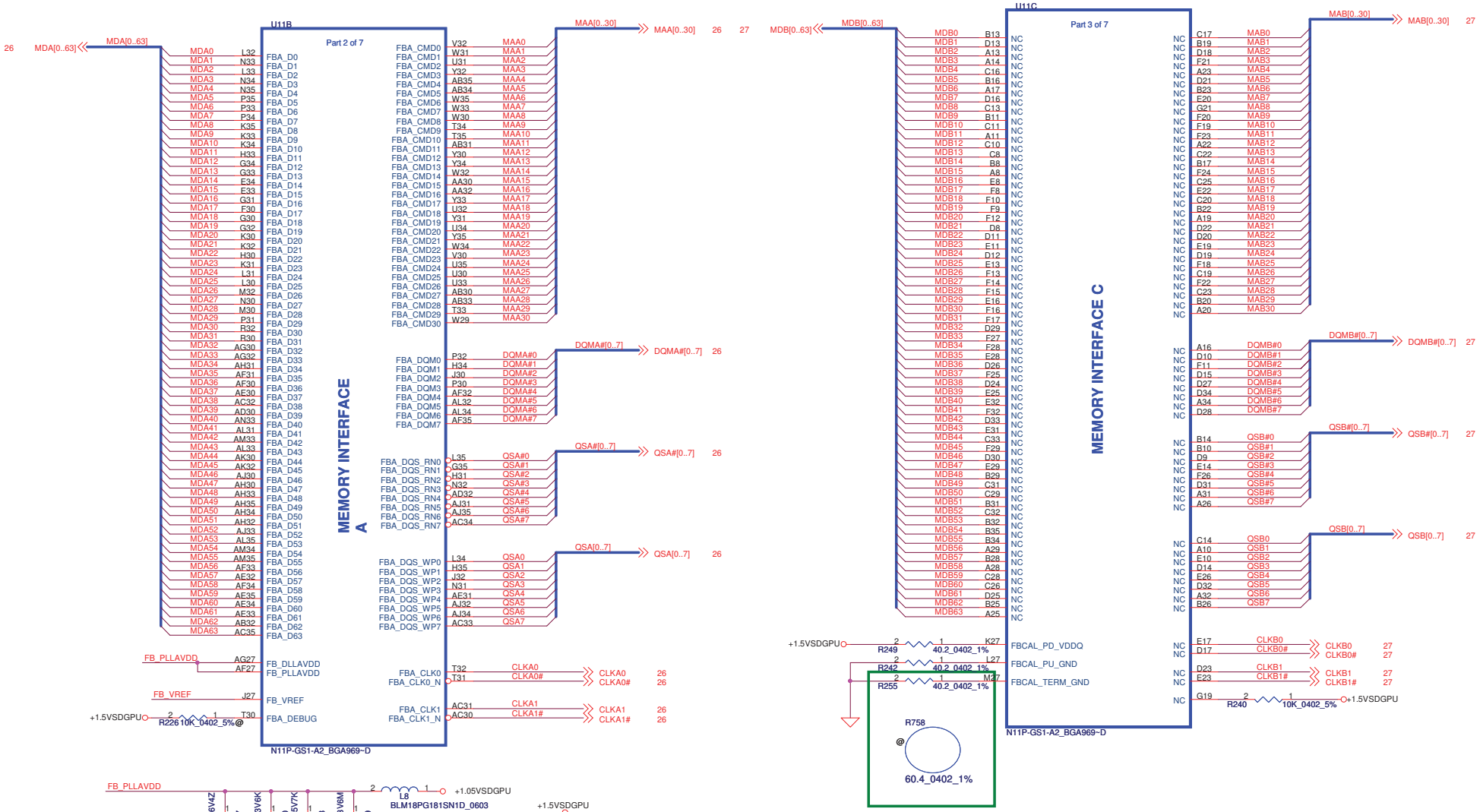

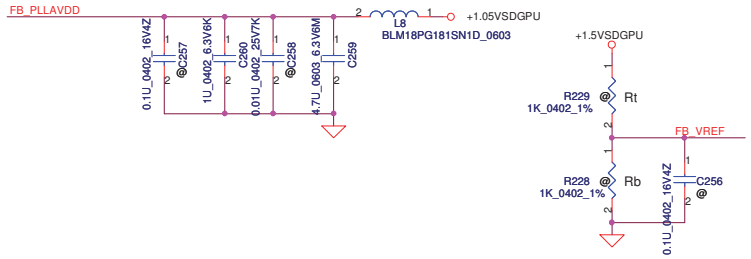

Place Components Close to BGA

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3 (11P)	+1.5VS	40.2 ohm	40.2 ohm	40.2 ohm

Must be used 1% resister for driver calibration

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Compal Electronics, Inc.

Title: N11P-GS1(5/5) MEMORY

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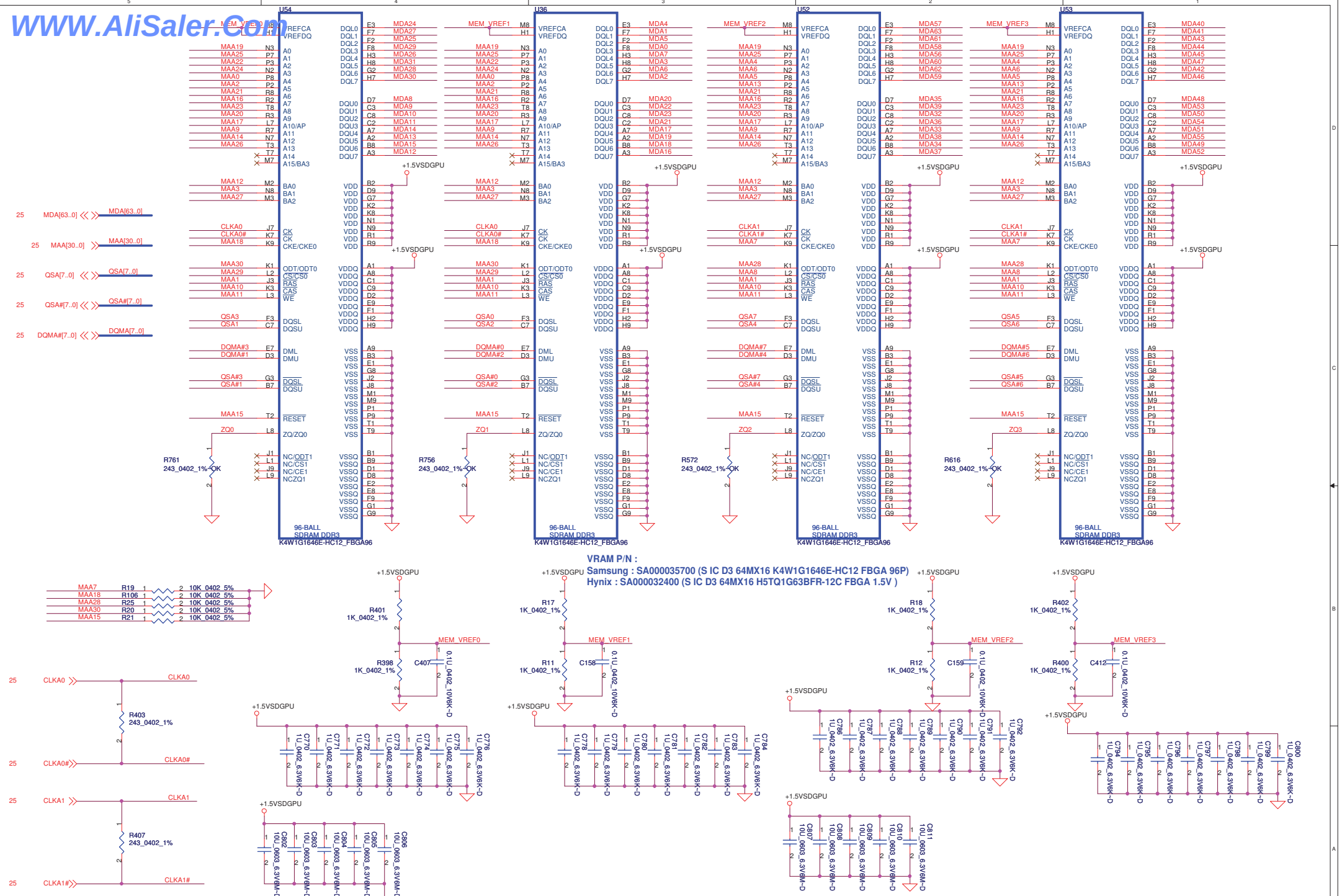

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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Compal Electronics, Inc.

Title: VRAM DDR3 / Channel A

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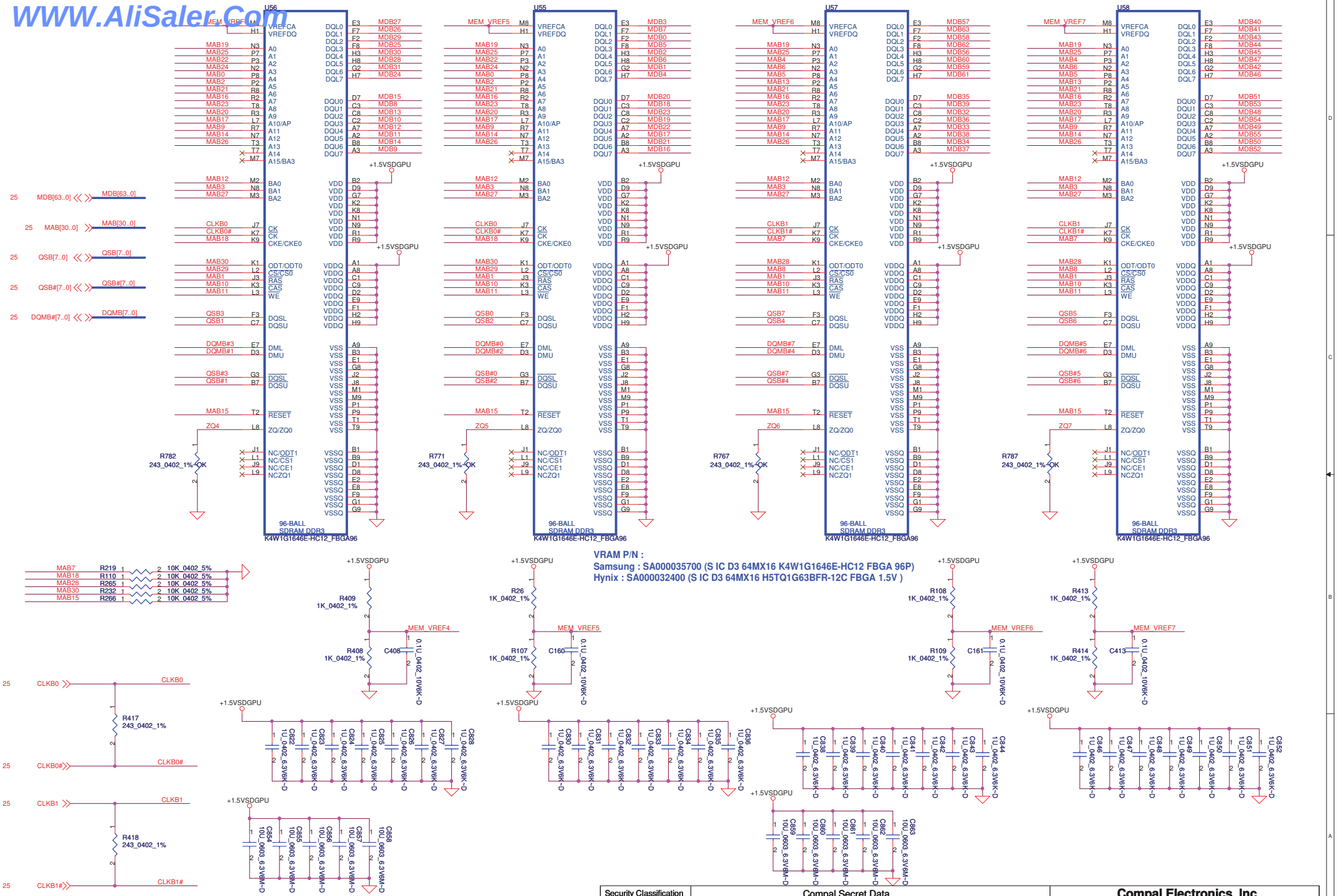

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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Compal Electronics, Inc.

Title: **VRAM DDR3 / Channel B**

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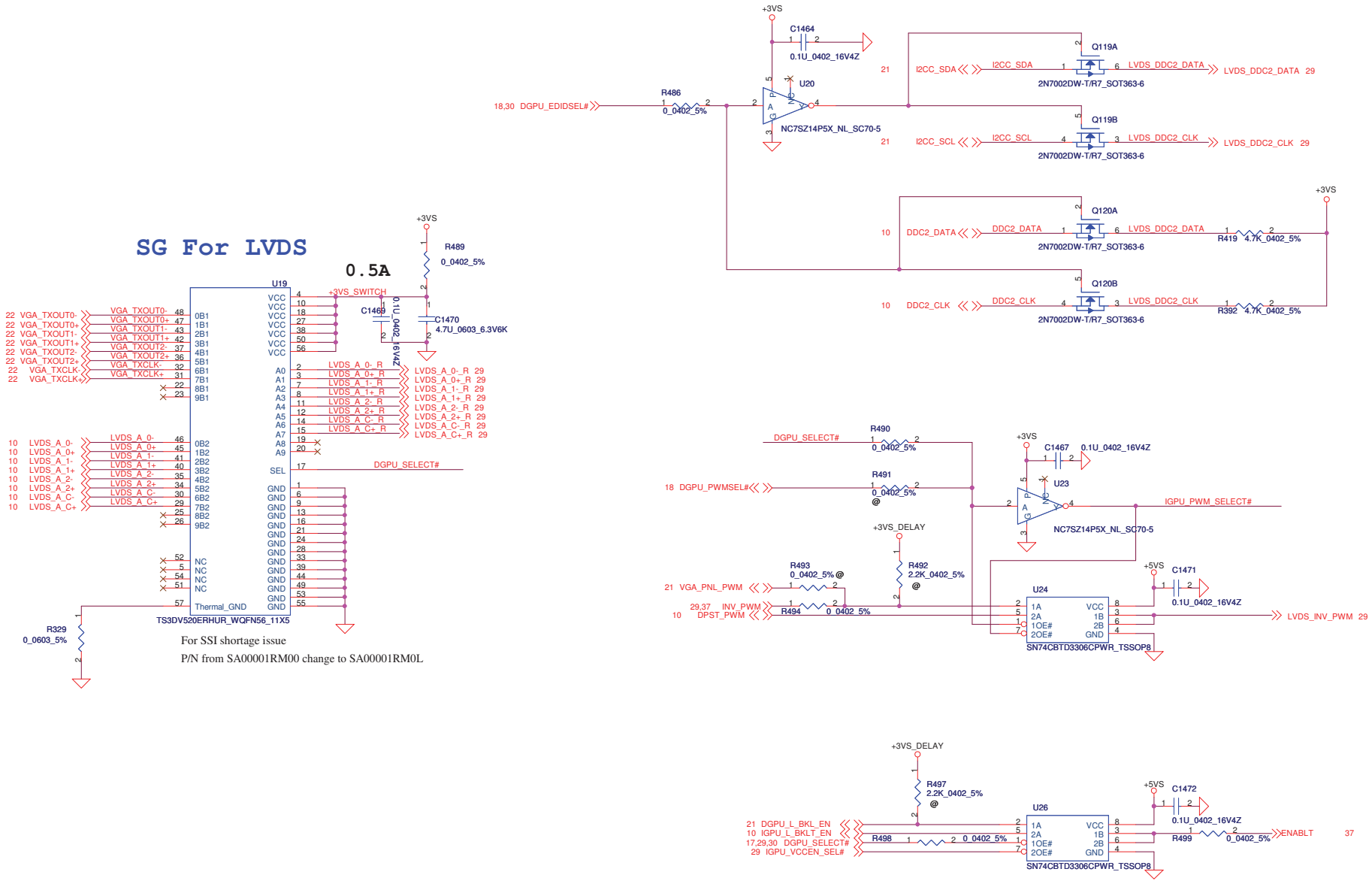

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Compal Electronics, Inc.

Title: LVDS Switch

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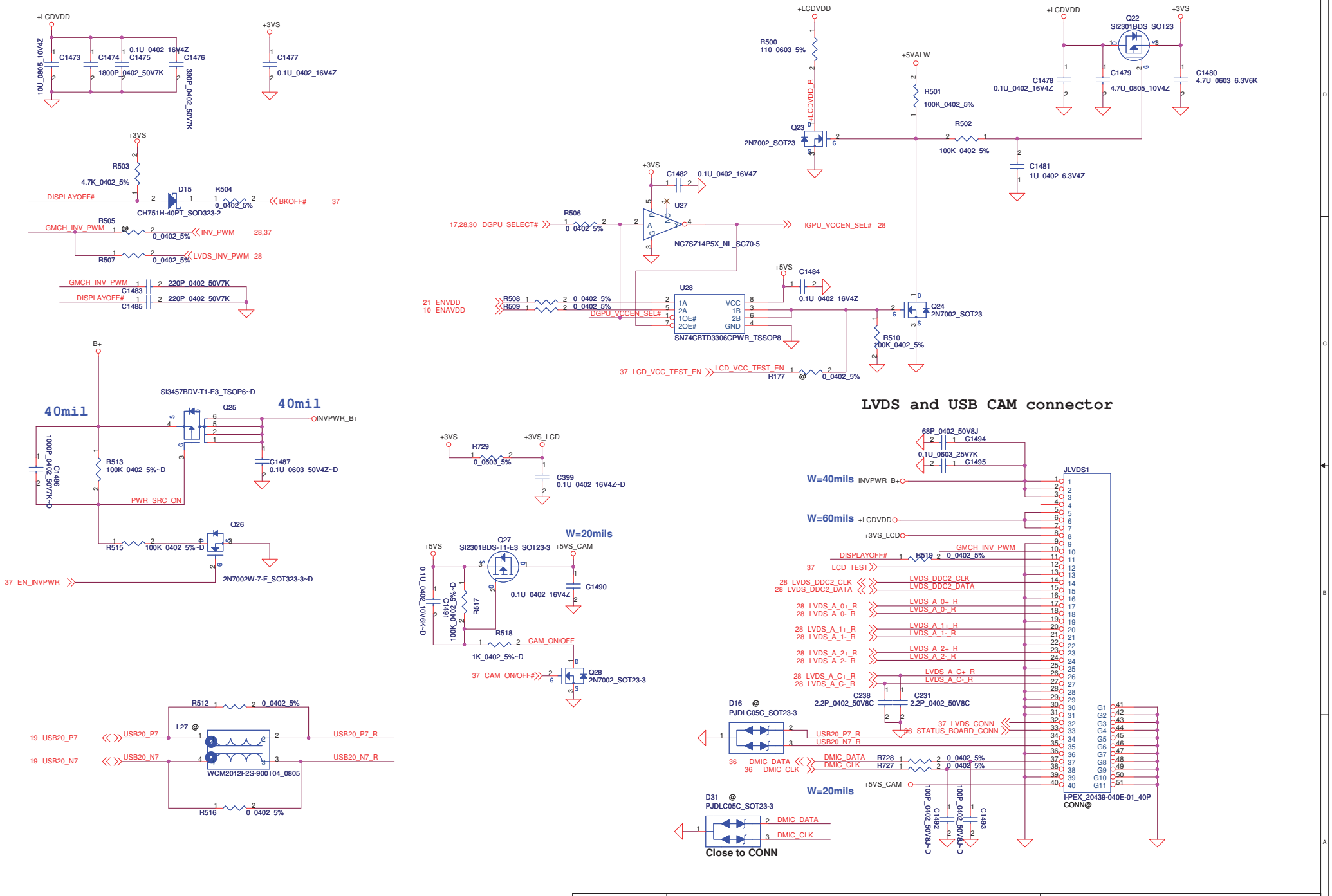

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Compal Electronics, Inc.

Title: LCD CONN

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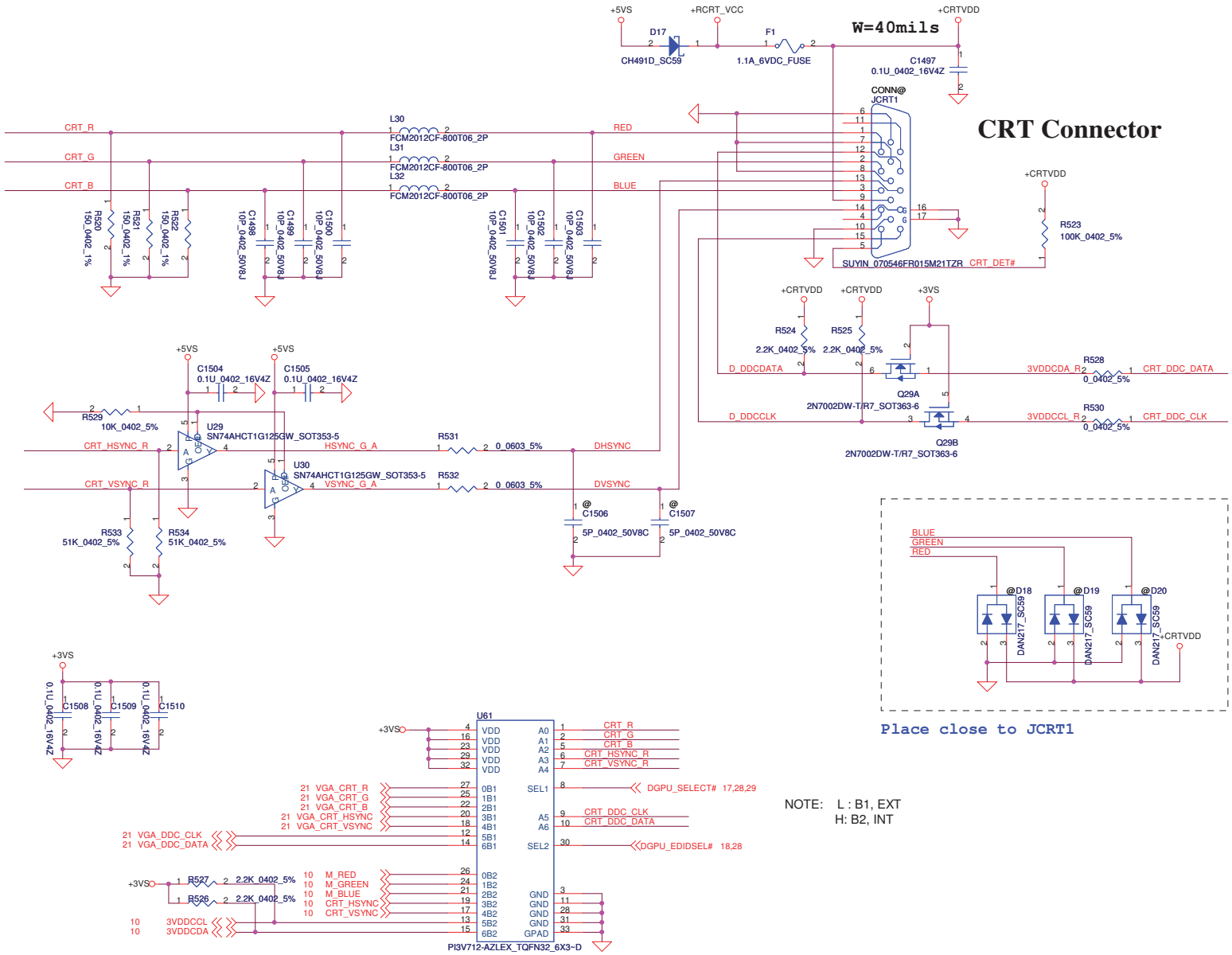

NOTE: L : B1, EXT
H: B2, INT

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Compal Electronics, Inc.

Title: **CRT CONN**

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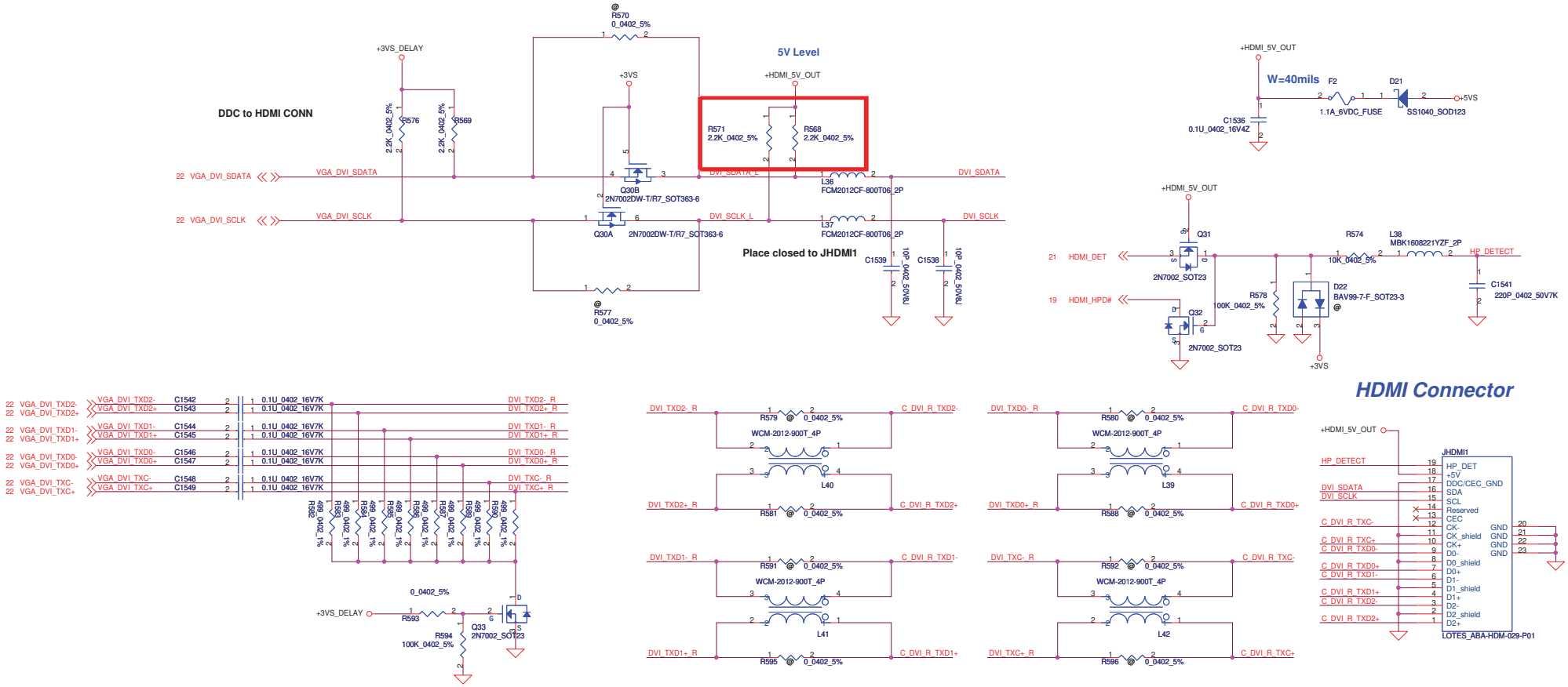

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Compal Electronics, Inc.

Title: **HDMI**

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Custom	LA-5811P	1.0

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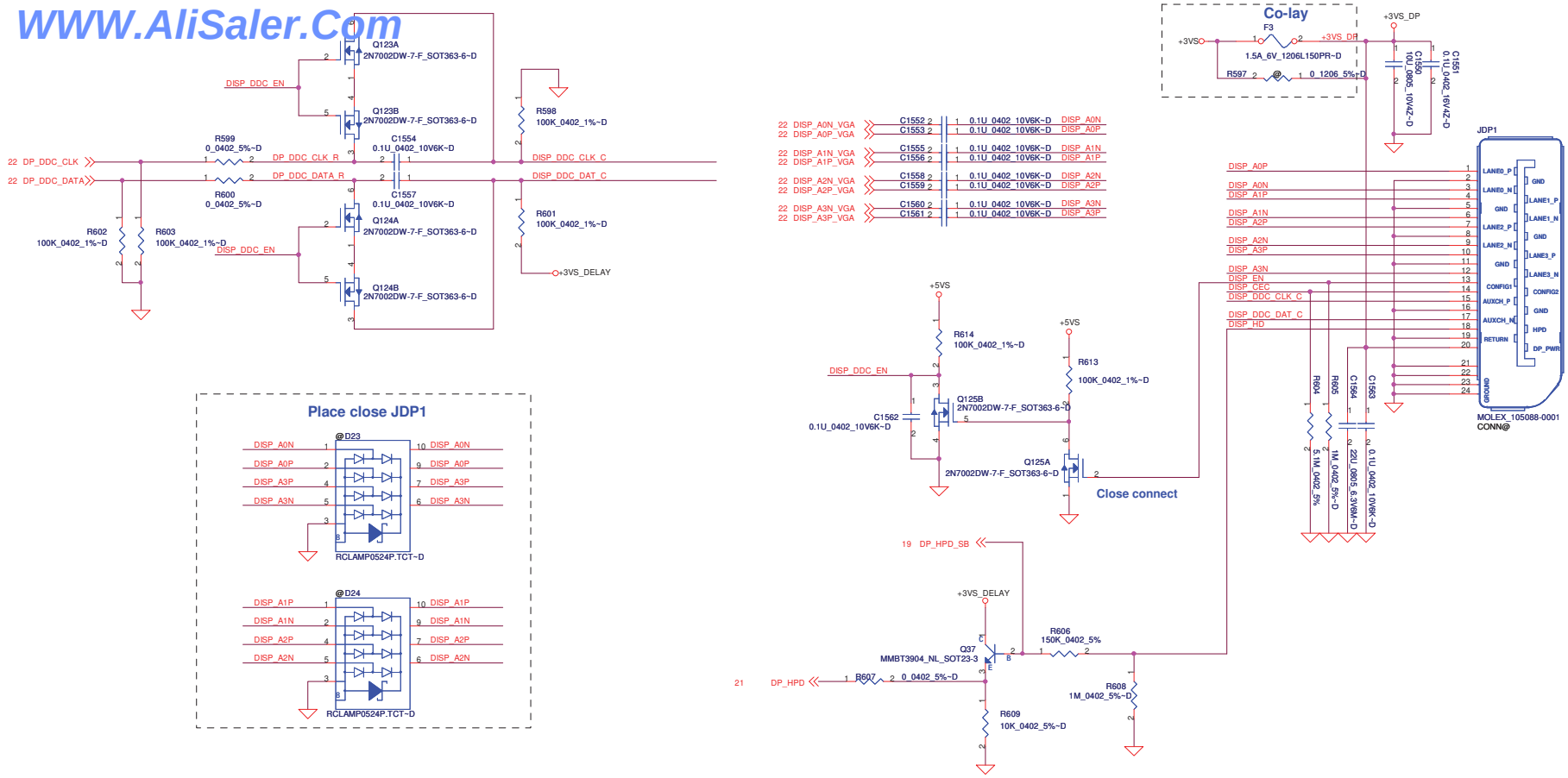

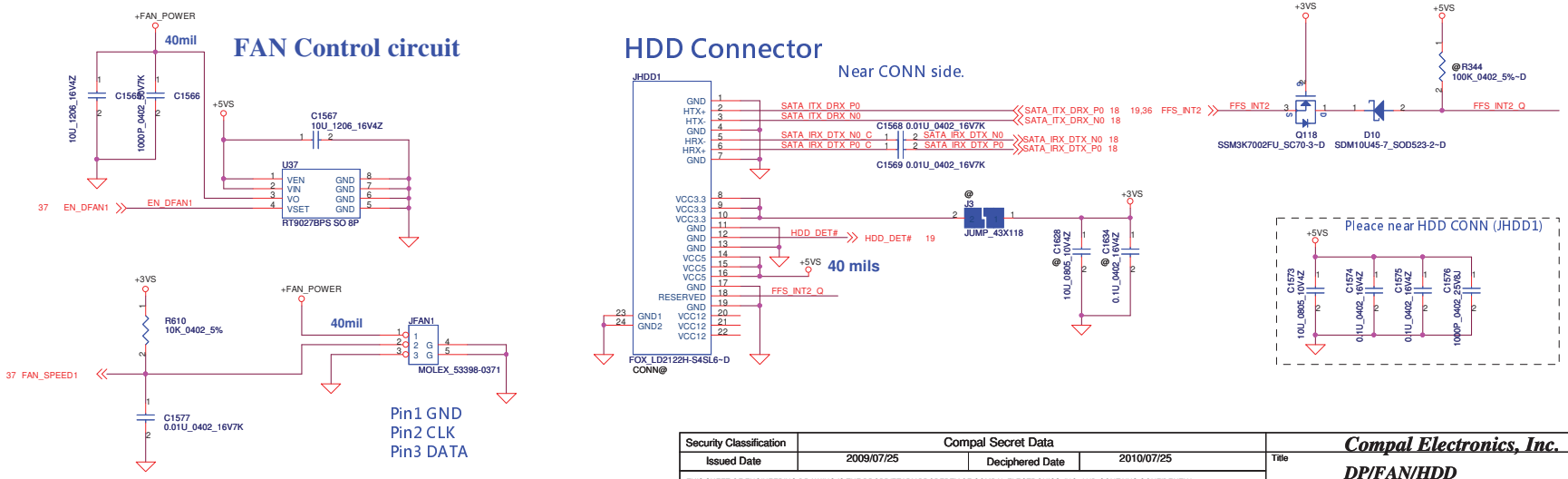

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Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Compal Electronics, Inc.

Title: **DP/FAN/HDD**

Size	Document Number	Rev
Custom	LA-5811P	1.0

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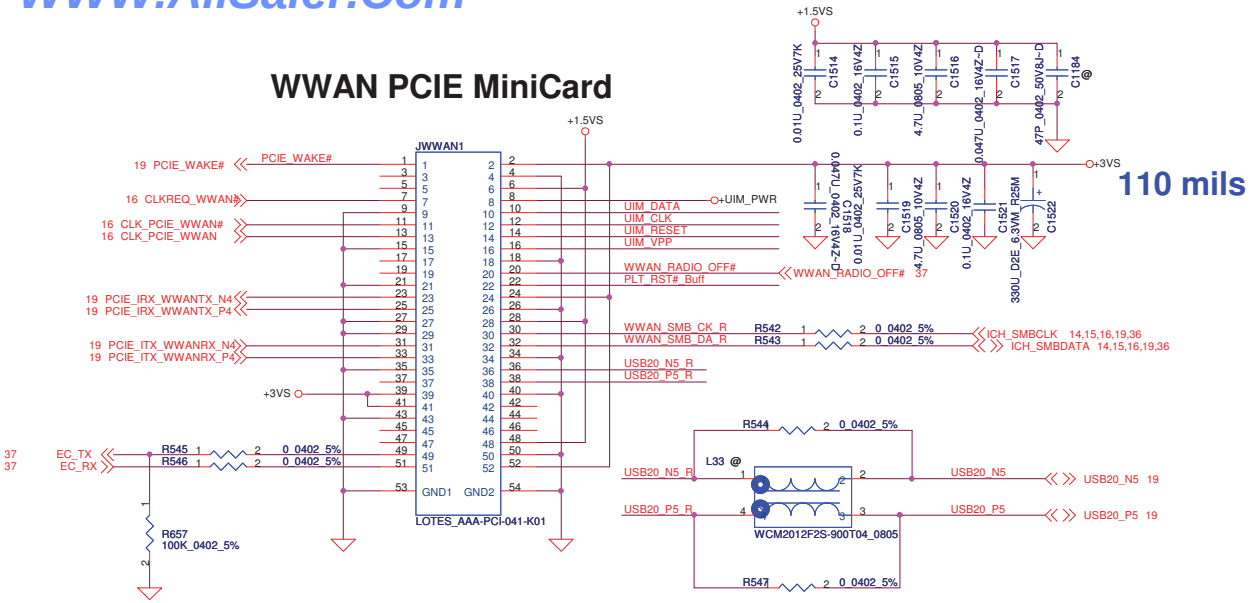
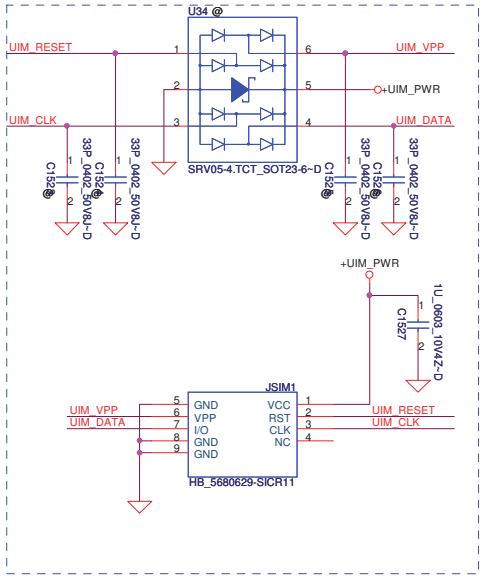
WWAN PCIE MiniCard

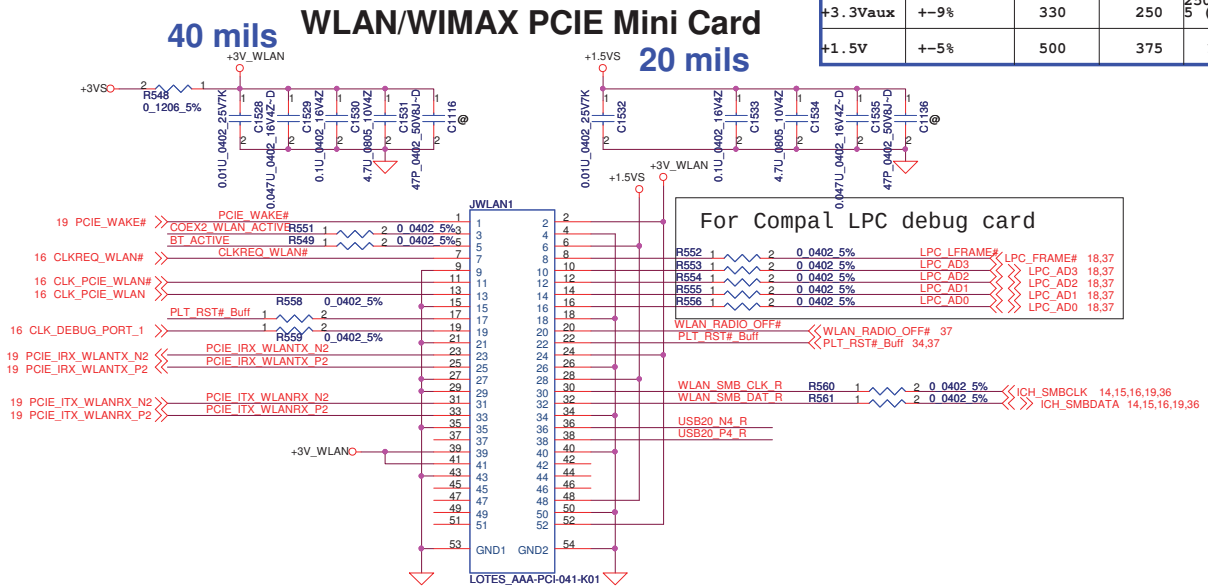


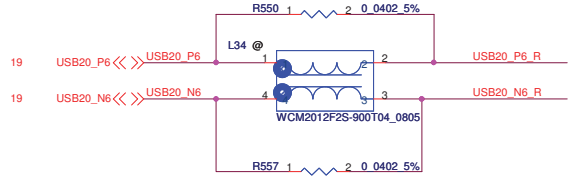
SIM Card



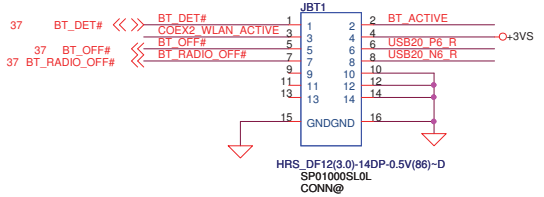
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

WLAN/WIMAX PCIE Mini Card





Bluetooth



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Compal Electronics, Inc.

Title: WLAN/WWAN/SIM/BT

Size: Custom | Document Number: LA-5811P | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 33 of 58

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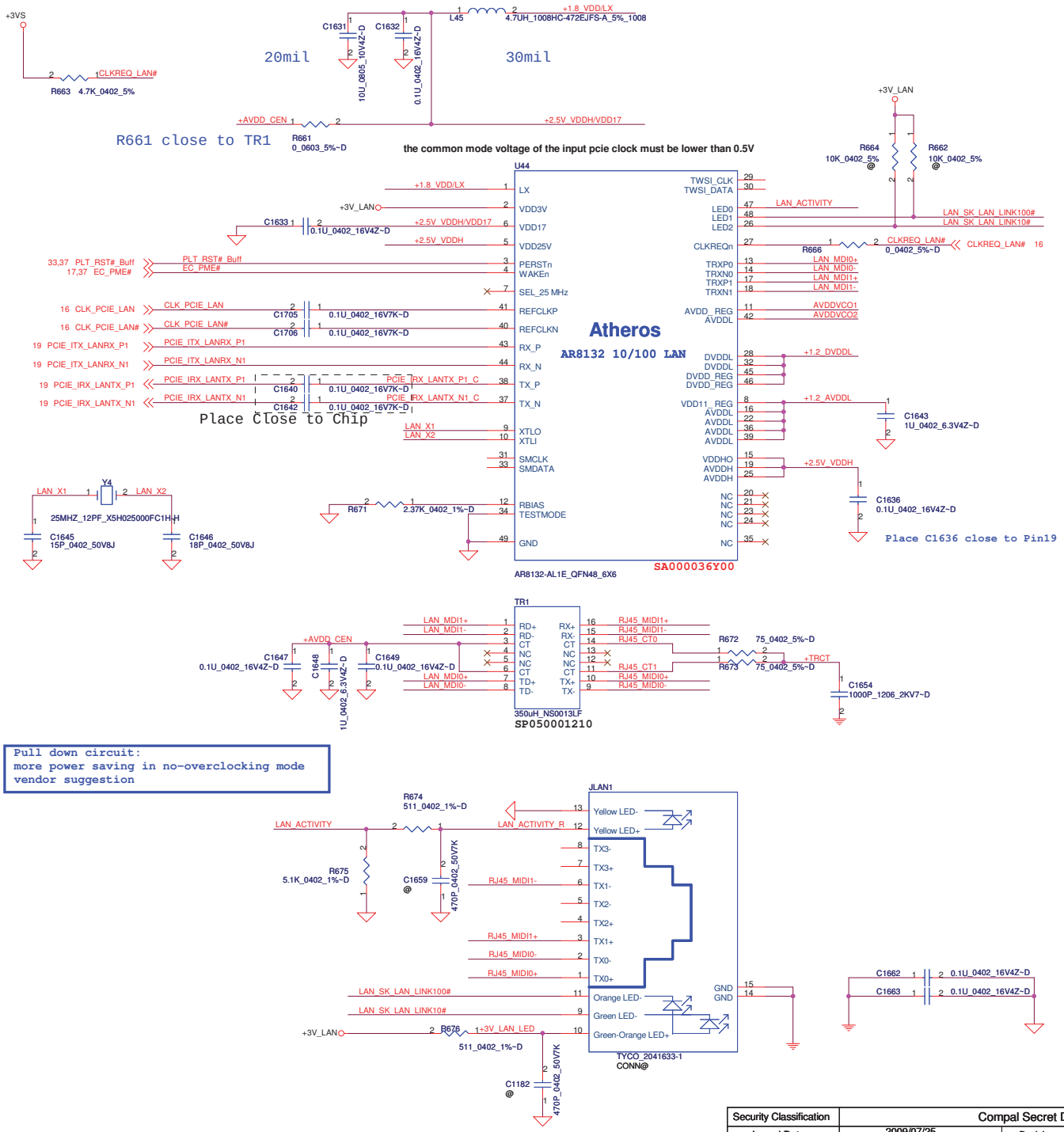
C1631, C1632, L45 Close to pin 1 60mil



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Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Compal Electronics, Inc.

Title: LAN

Size	Document Number	Rev
Custom	LA-5811P	1.0

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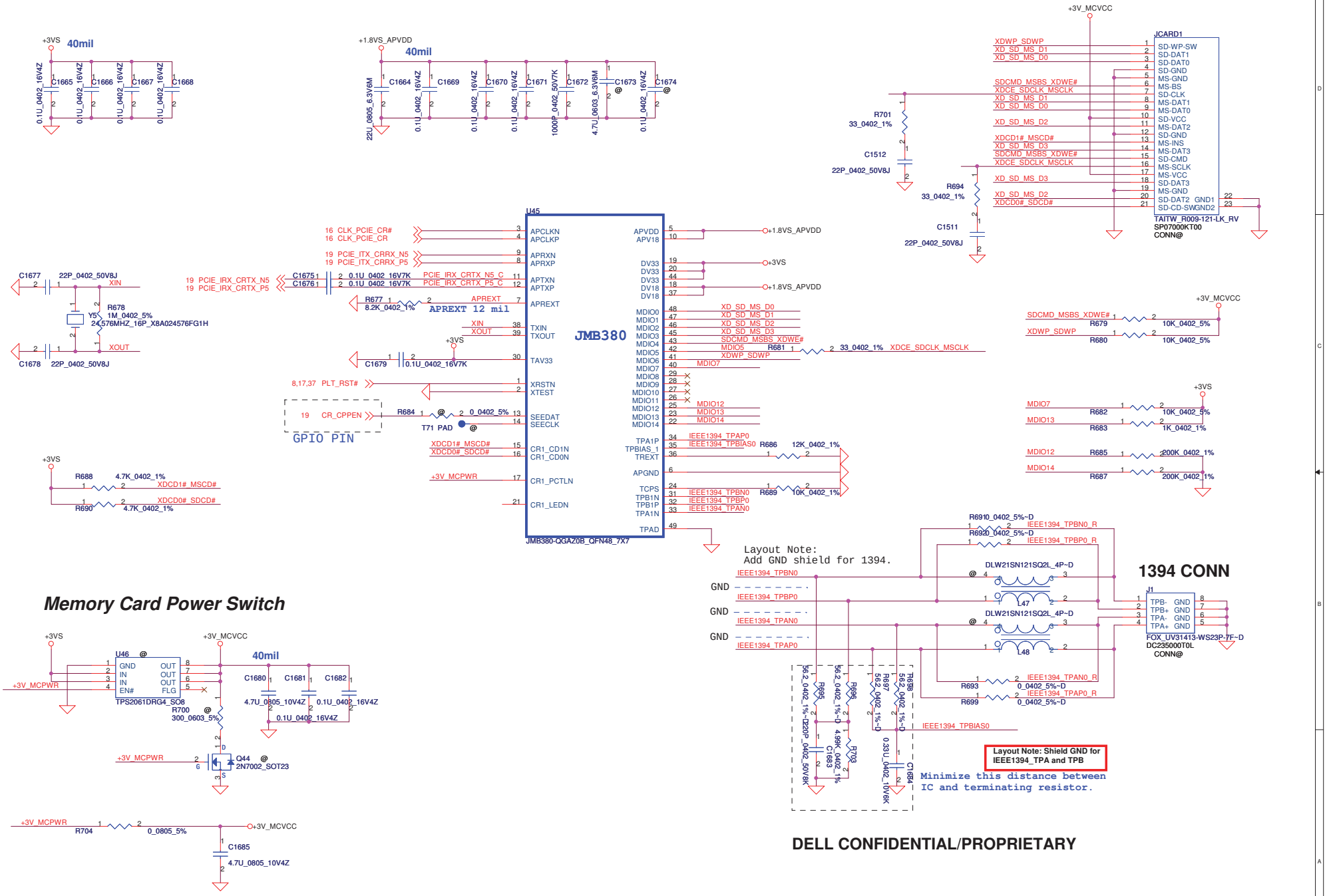
3 in 1 Card Reader CONN



DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Compal Electronics, Inc.

Title: CARD READER/1394

Size: Custom | Document Number: LA-5811P | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 35 of 58

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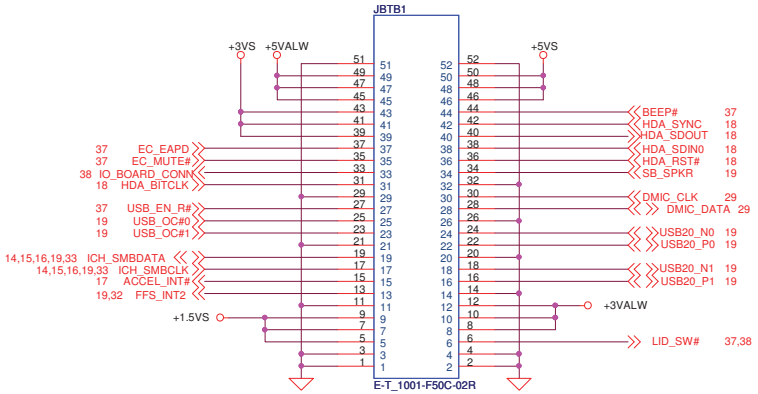
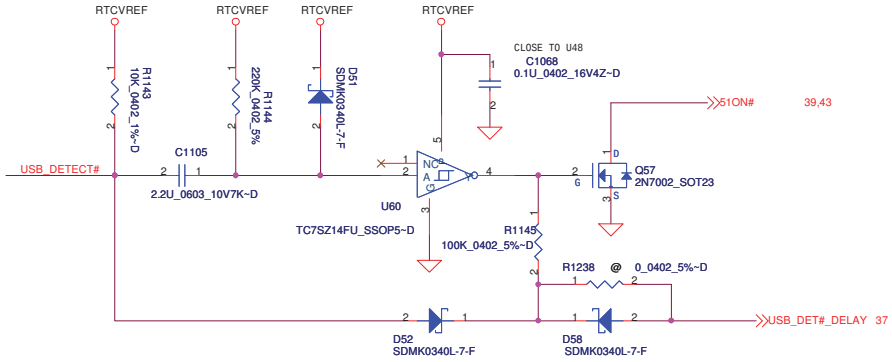
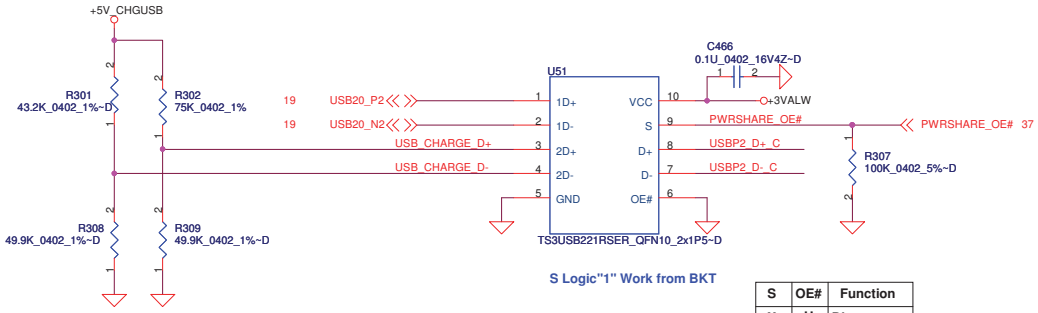
IO Board CONN





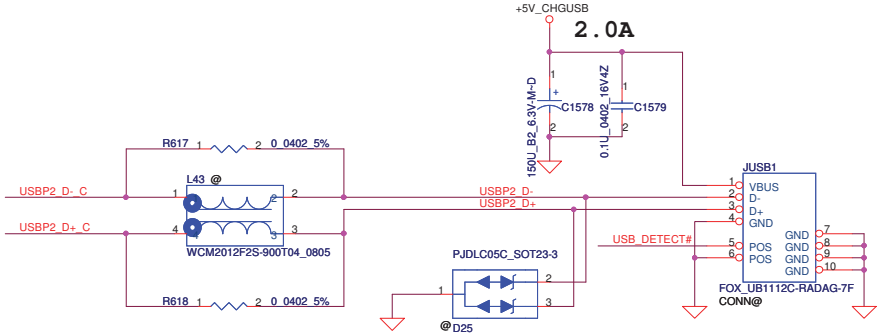
Power share

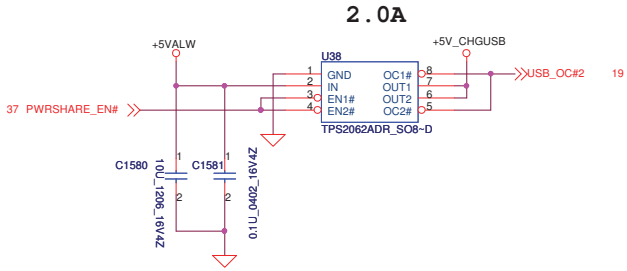
fix +3VALW leakage on Batt mode



S Logic"1" Work from BKT

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D





Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Compal Electronics, Inc.

Title: USB/LID SW/IO CONN

Size: Custom | Document Number: LA-5811P | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 36 of 58

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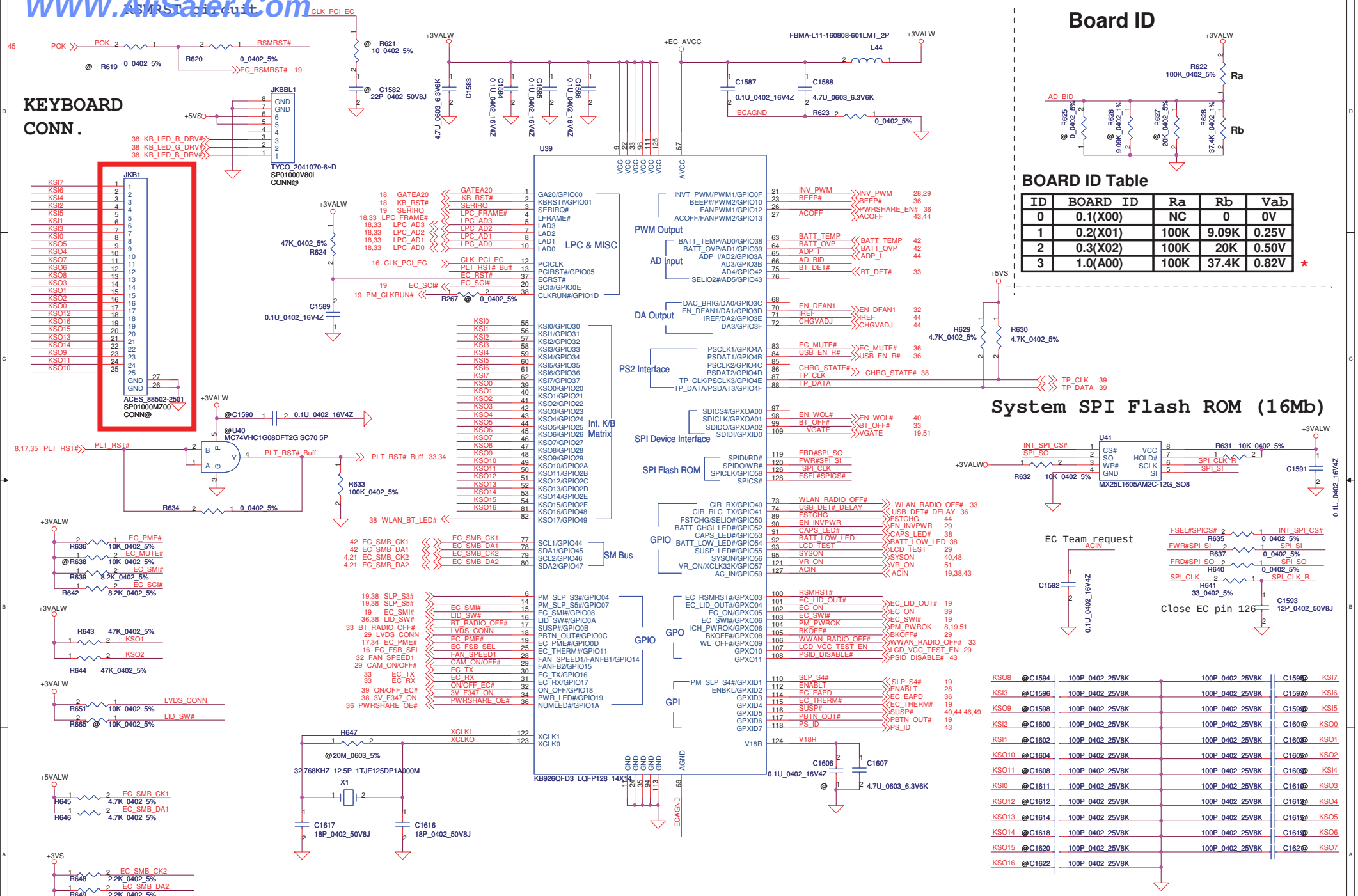
RSMRST Circuit



ID	BOARD ID	Ra	Rb	Vab
0	0.1(X00)	NC	0	0V
1	0.2(X01)	100K	9.09K	0.25V
2	0.3(X02)	100K	20K	0.50V
3	1.0(A00)	100K	37.4K	0.82V *

Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Compal Electronics, Inc.

Title: EC/KB CONN

Size: Custom | Document Number: LA-5811P | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 37 of 58

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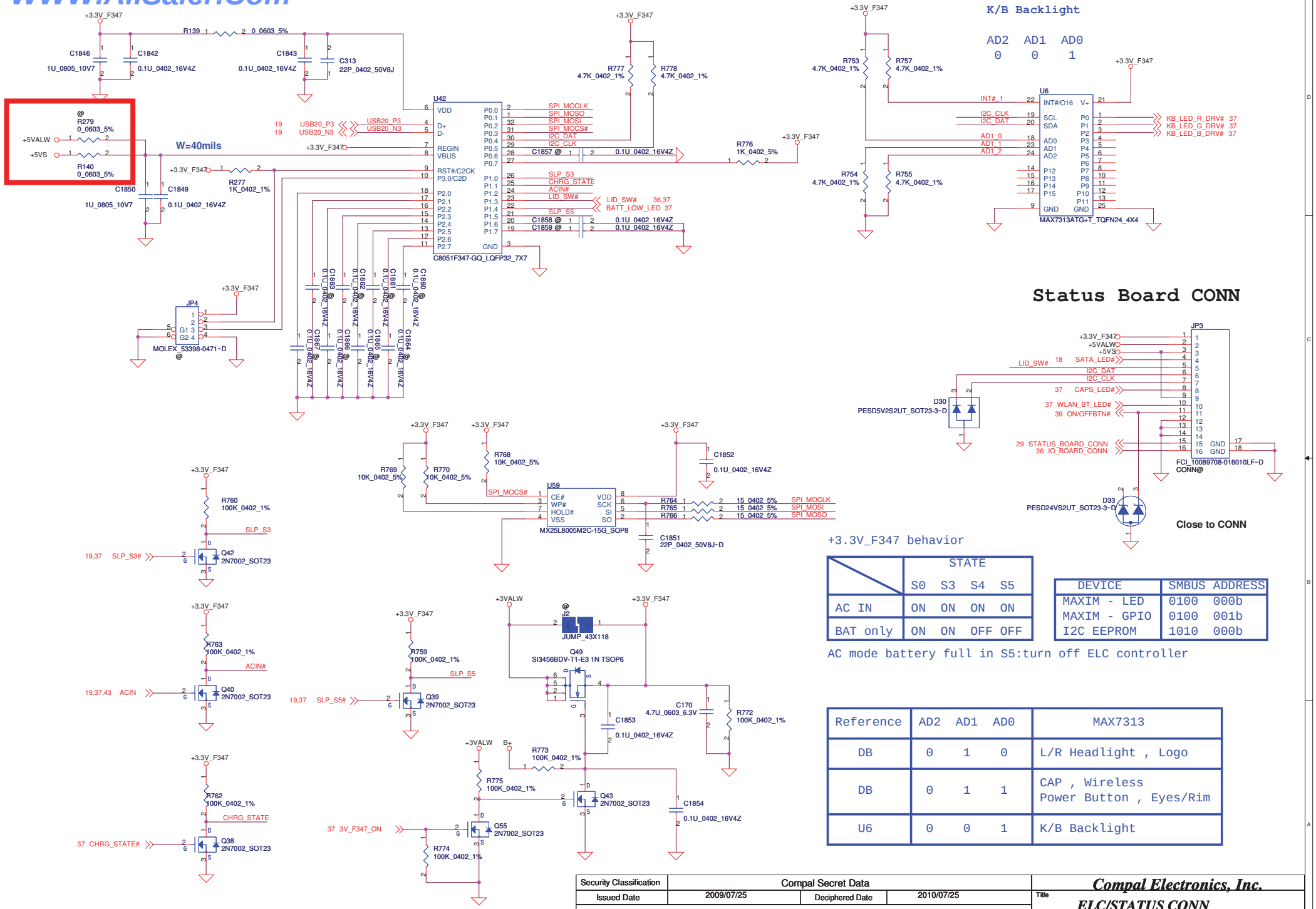

+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

AC mode battery full in S5:turn off ELC controller

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

Reference	AD2	AD1	AD0	MAX7313
DB	0	1	0	L/R Headlight , Logo
DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight

Security Classification	Compal Secret Data		
Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Compal Electronics, Inc.

Title: ELC/STATUS CONN

Size: Custom | Document Number: LA-5811P | Rev: 1.0

Date: Wednesday, December 30, 2009 | Sheet 38 of 58

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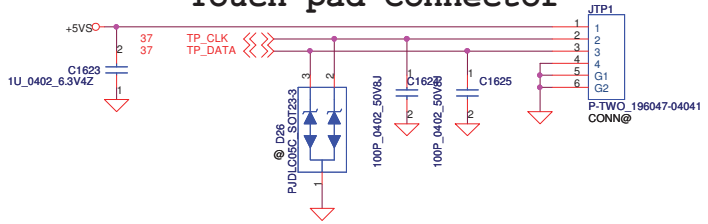
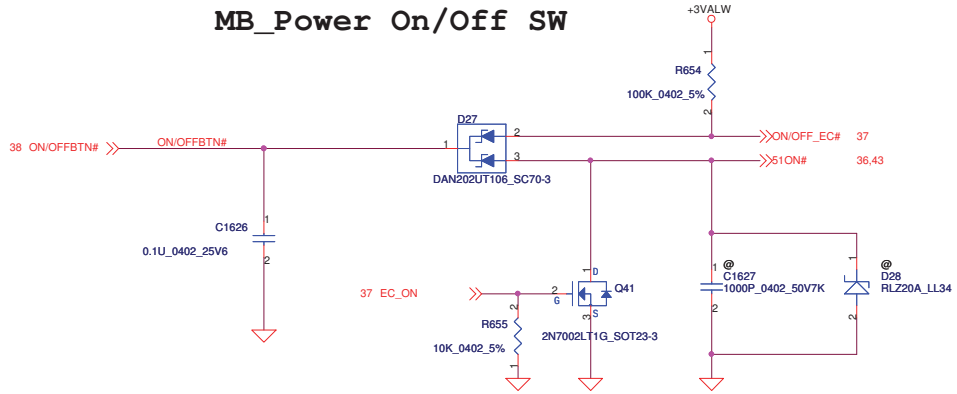
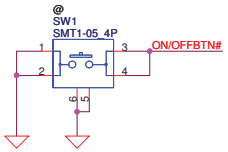
Touch pad Connector

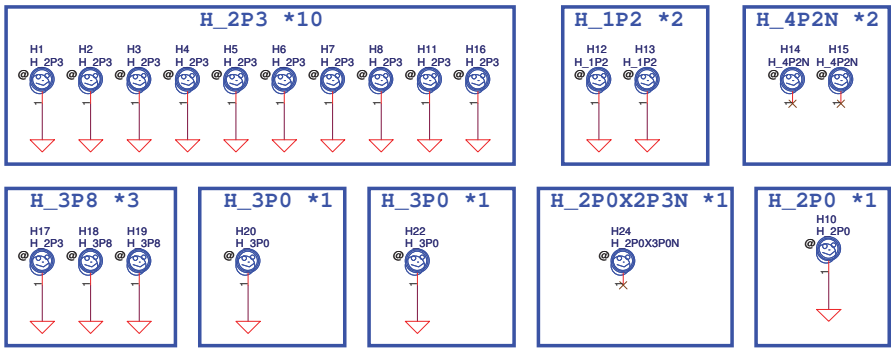


MB_Power On/Off SW



For Debug Only





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Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Compal Electronics, Inc.

Title: SW/TP/SCREW

Size: Custom | Document Number: LA-5811P | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 39 of 58

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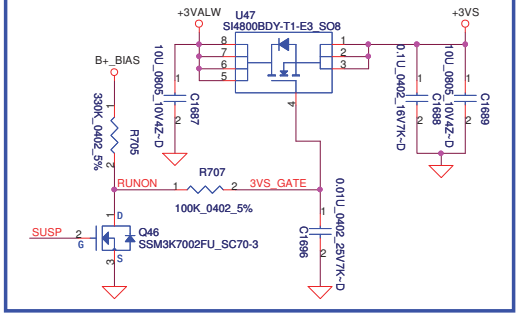
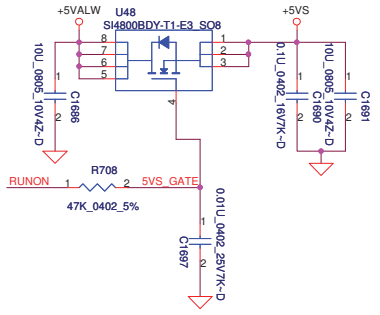
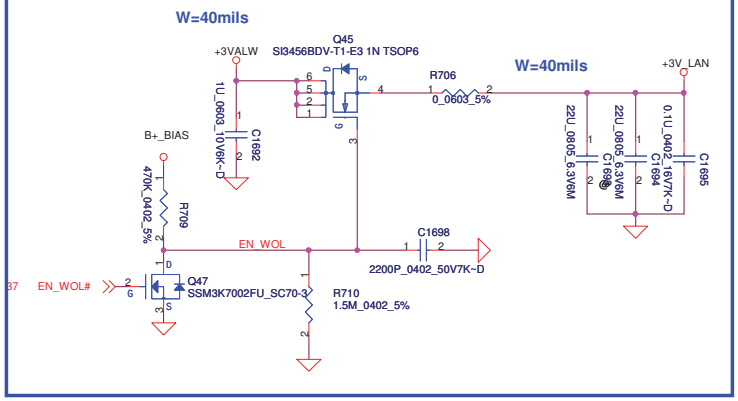
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

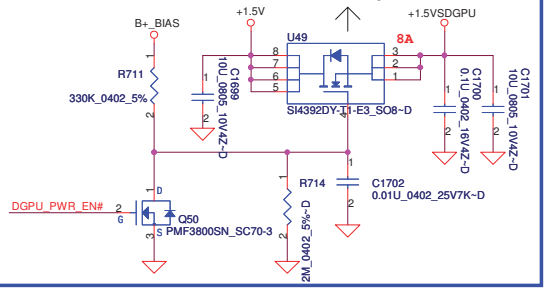


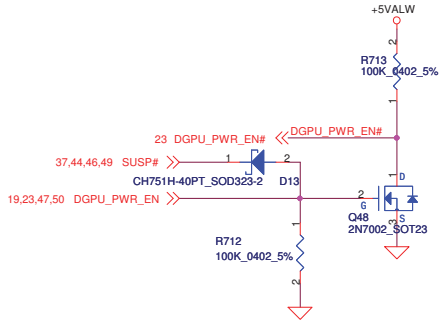
+3VALW to +3LAN Transfer



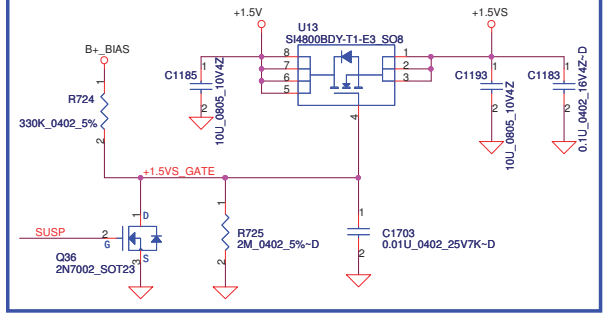
+1.5V to +1.5VSDGPU Transfer

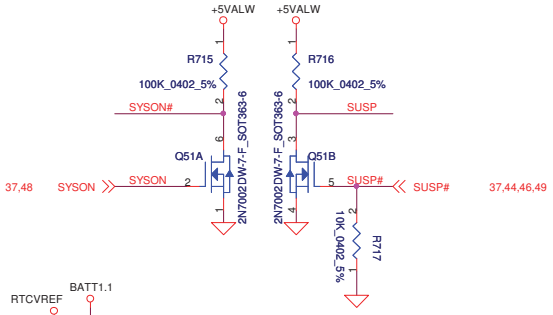
SB54392008L EOL, P/N change to SB54800038L

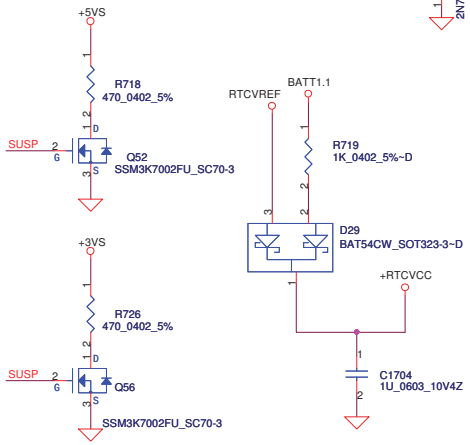


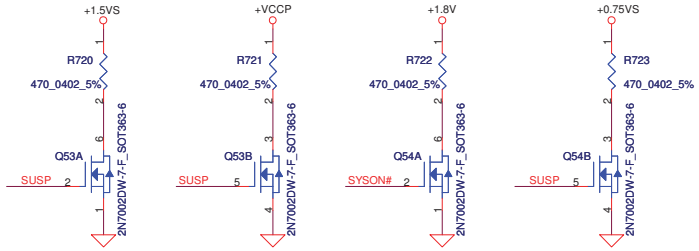


+1.5V to +1.5VS Transfer









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Compal Electronics, Inc.

Title: DC/DC INTERFACE

Size: Custom | Document Number: LA-5811P | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 40 of 58

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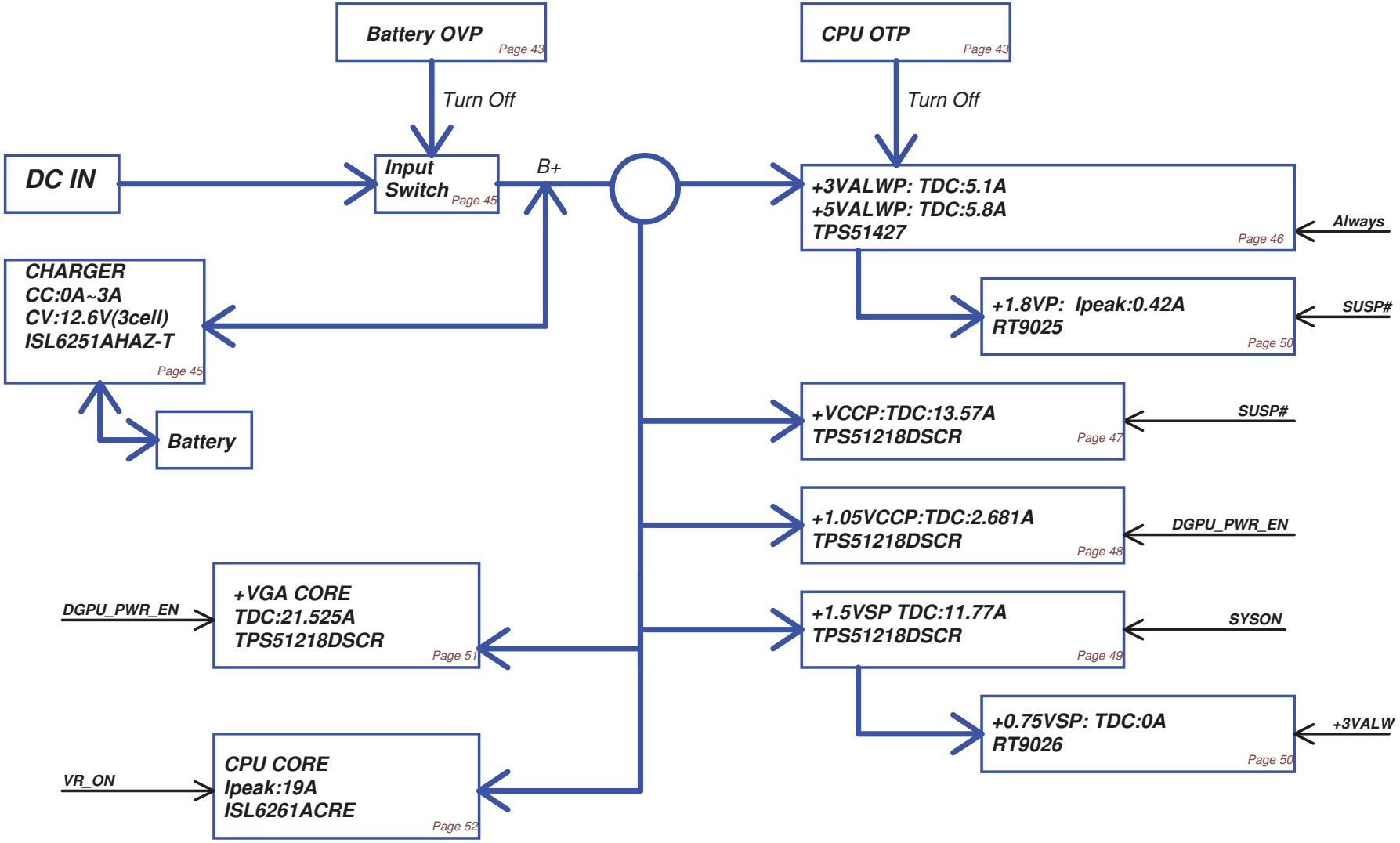
Power block



Title	POWER BLOCK DIAGRAM
Size	Document Number
Rev	
Date: Tuesday, December 29, 2009	Sheet 41 of 58

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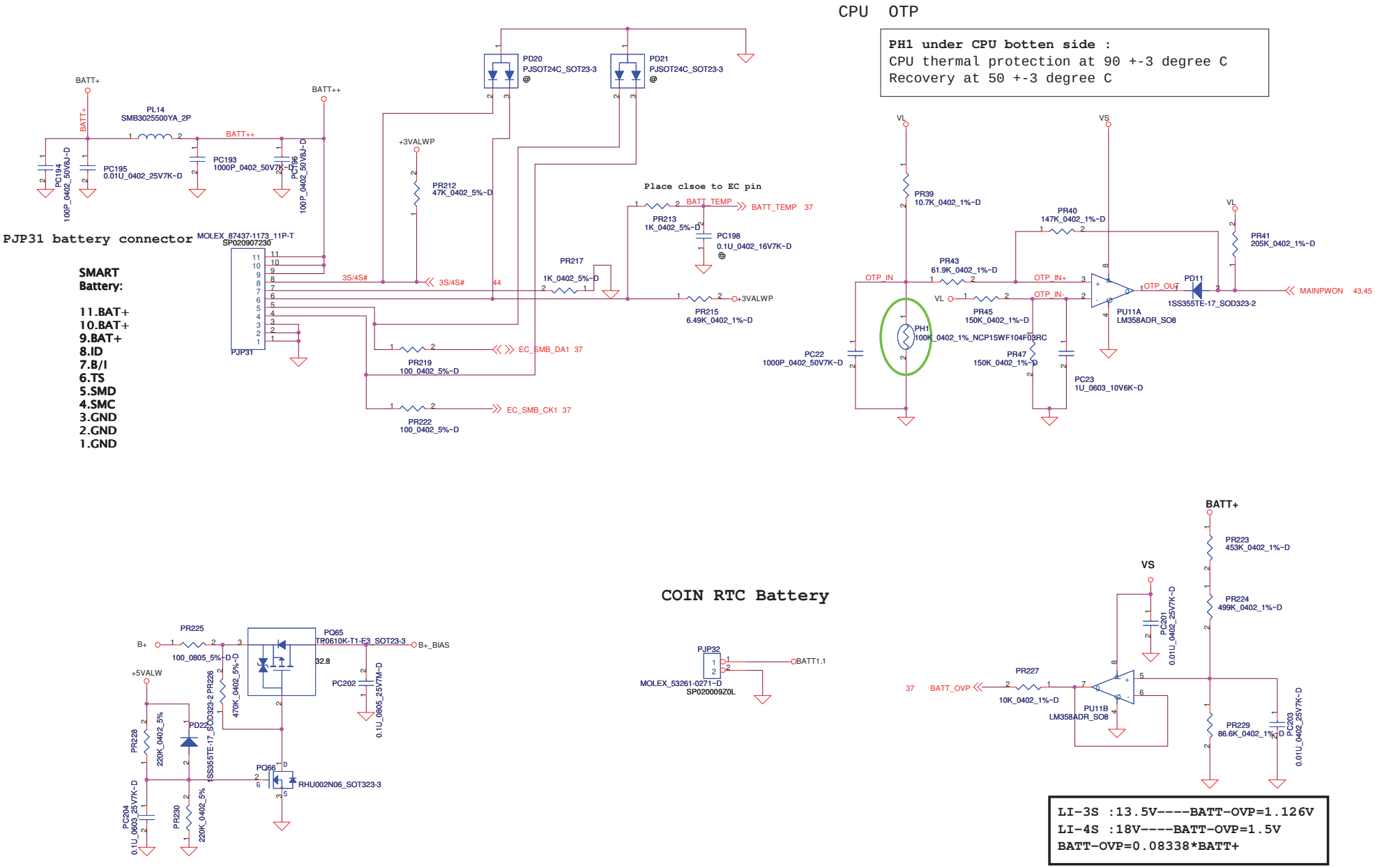

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: BATTERY CONN/OTP
			Size: Custom; Document Number; Rev
			Date: Tuesday, December 29, 2009; Sheet 42 of 58

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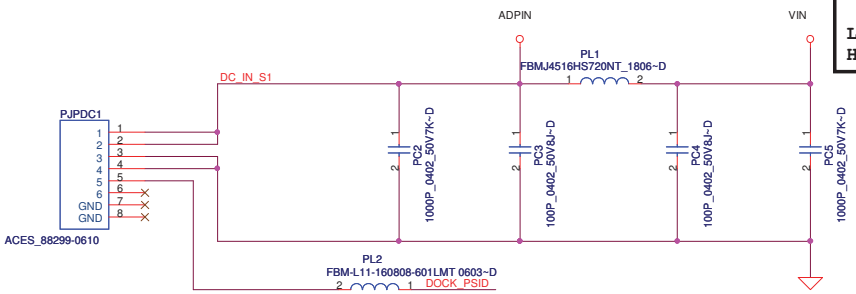
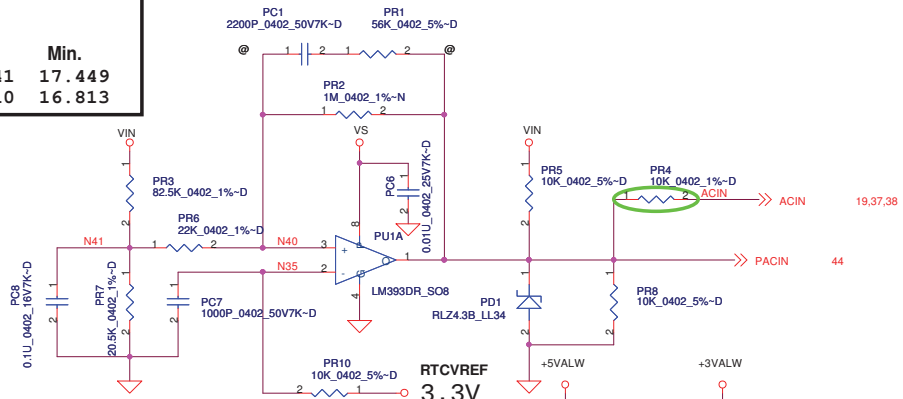
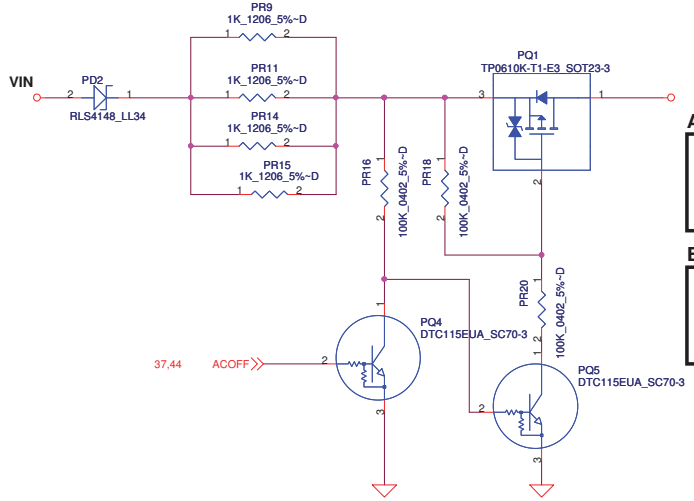
Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813







ACIN

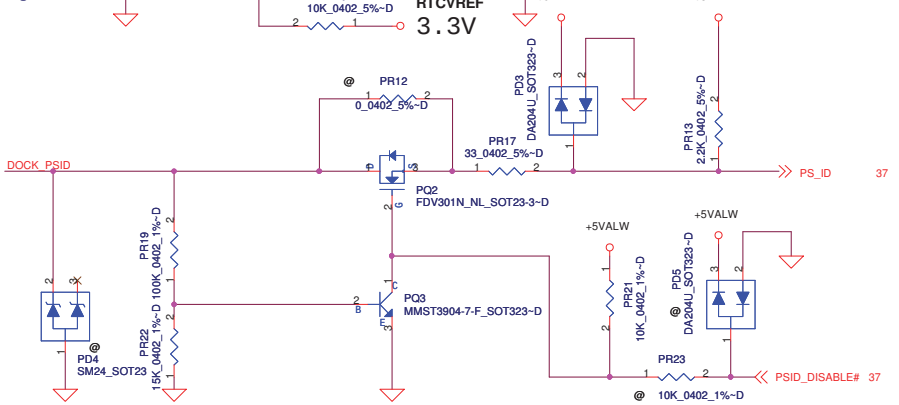
Precharge detector

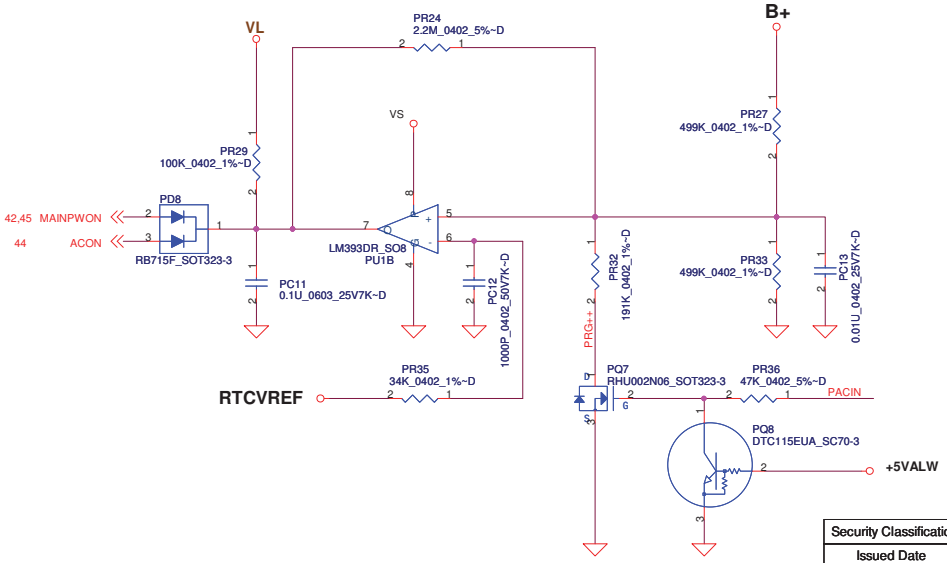
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

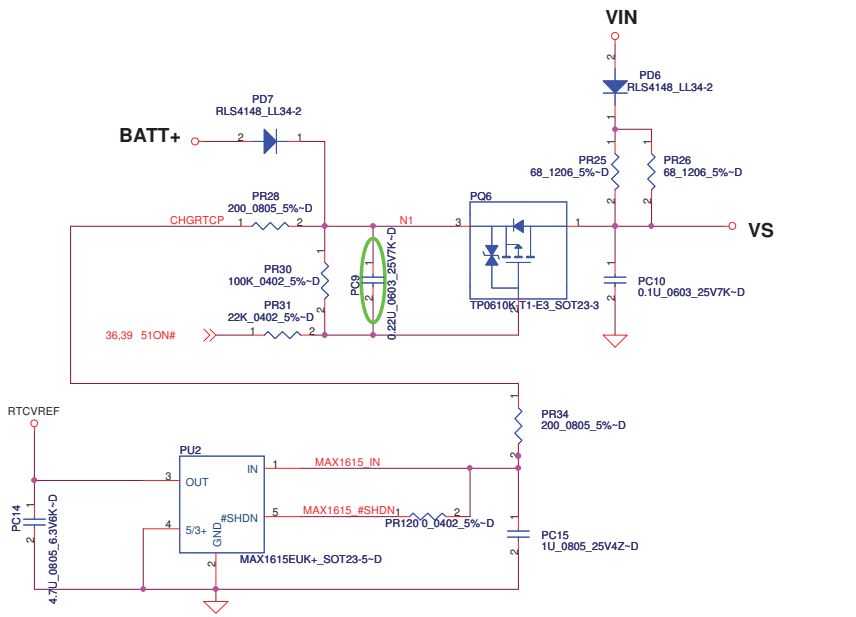
BATT ONLY

Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V







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Issued Date		Deciphered Date	Title: DCIN/DETECTOR

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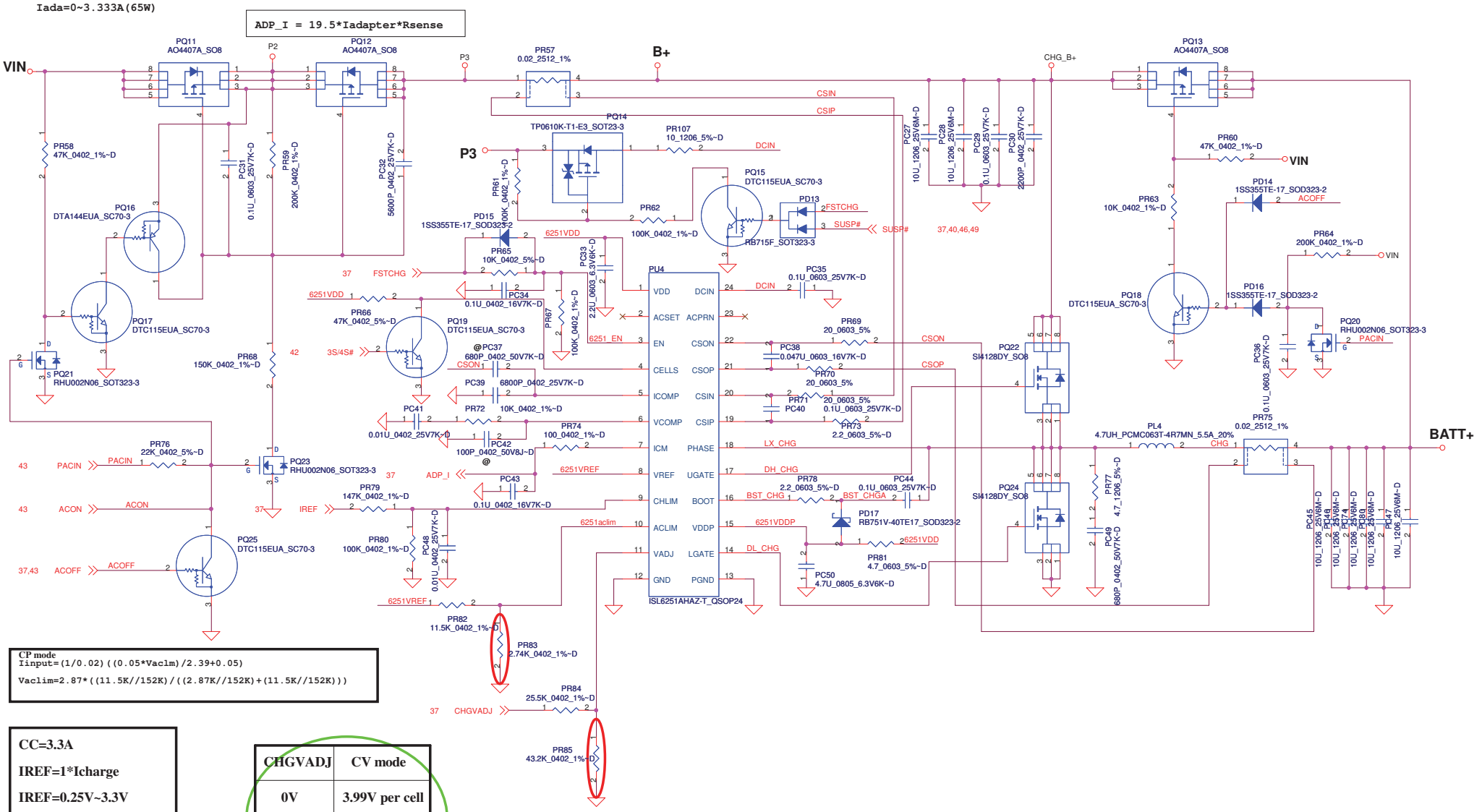

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

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Issued Date		Deciphered Date	Title: CHARGER

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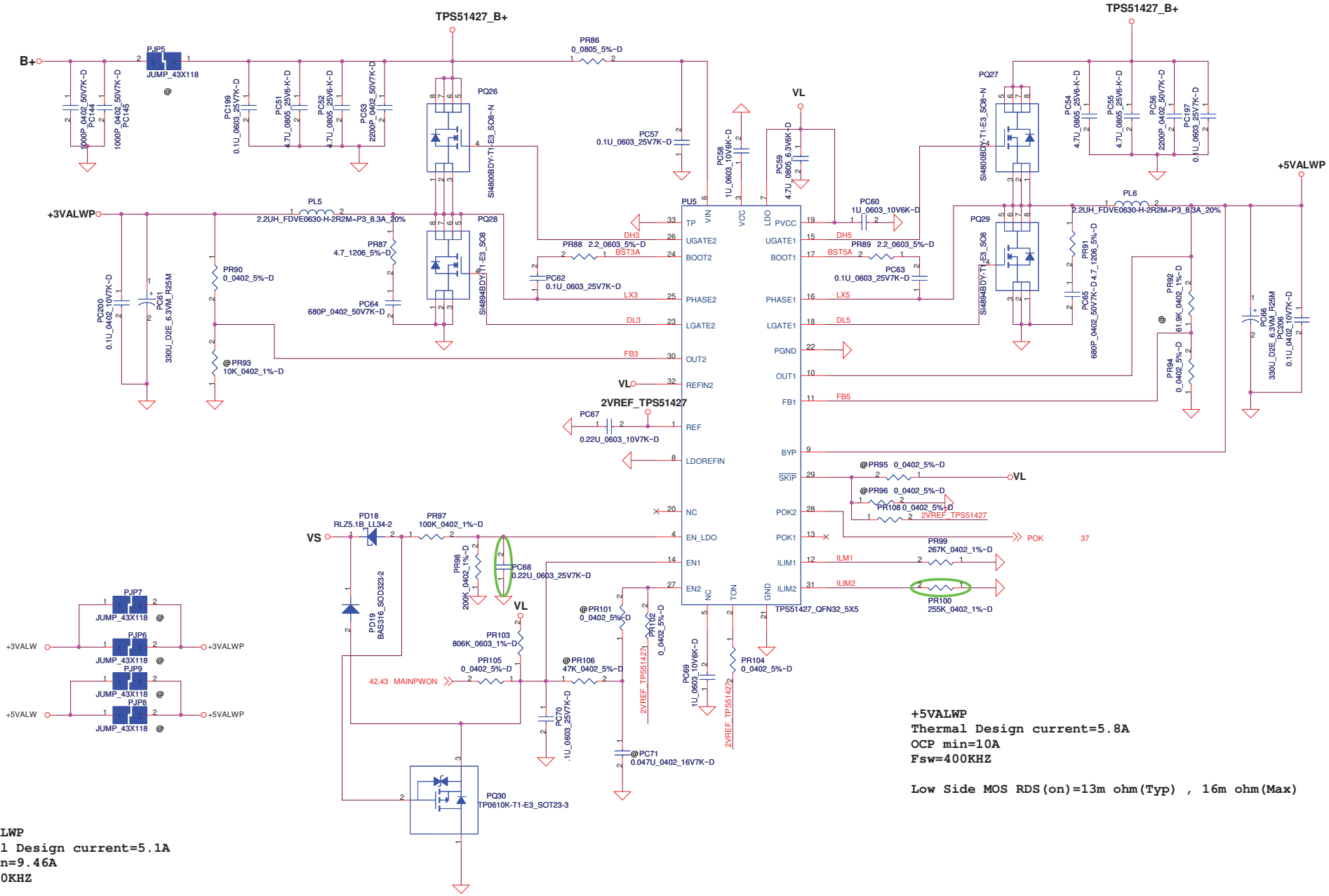

+5VALWP
Thermal Design current=5.8A
OCP min=10A
Fsw=400KHZ

Low Side MOS RDS(on)=13m ohm(Typ) , 16m ohm(Max)

+3.3VALWP
Thermal Design current=5.1A
OCP min=9.46A
Fsw=300KHZ

Low Side MOS RDS(on)=13m ohm(Typ) , 16m ohm(Max)

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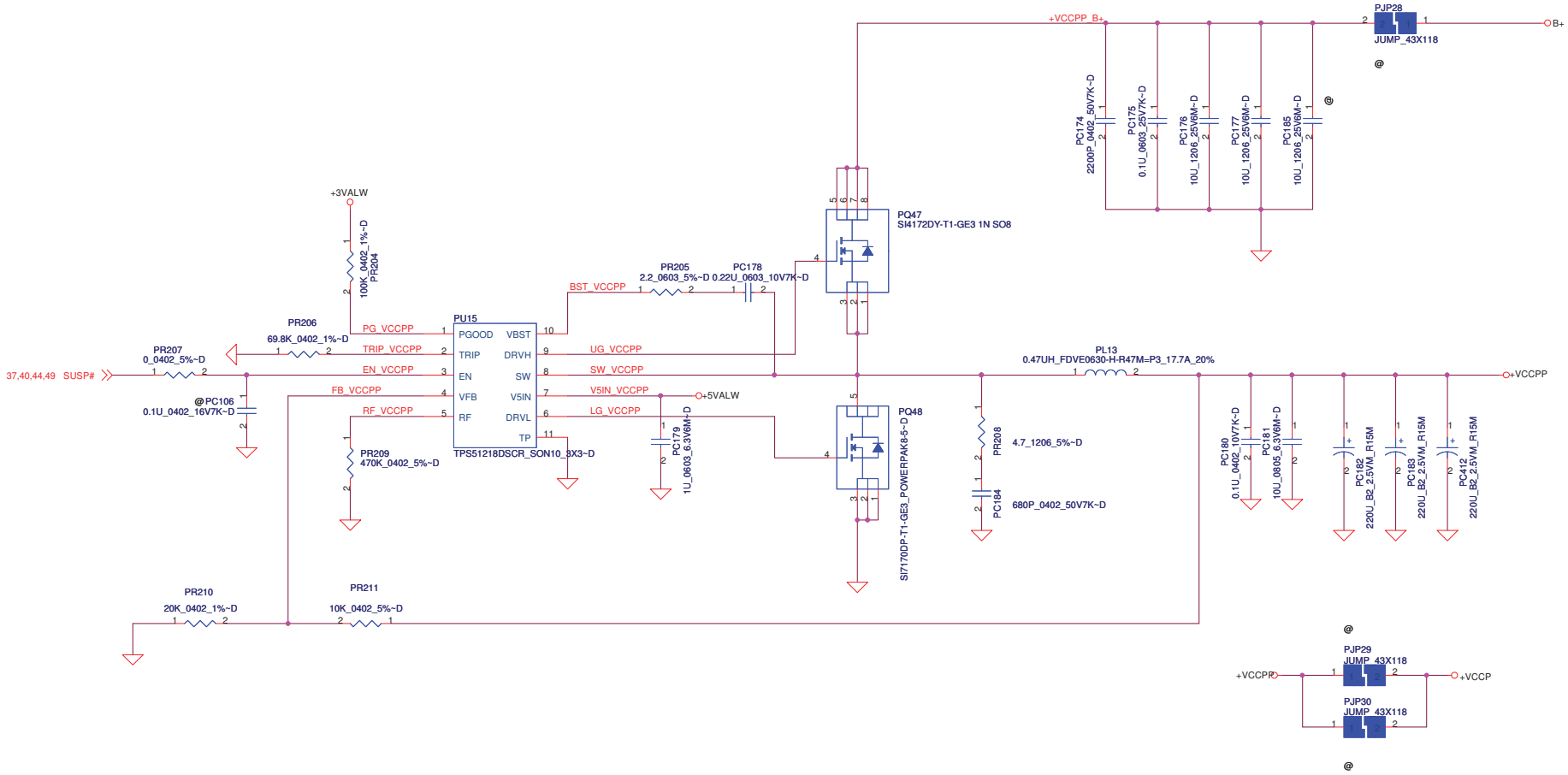

+VCCPP
Thermal Design current=13.57A
OCPmin=25.2A
Fsw=290KHZ

Low Side MOS RDS(on)=3.6m ohm(Typ) , 4.5m ohm(Max)

+VCCPP

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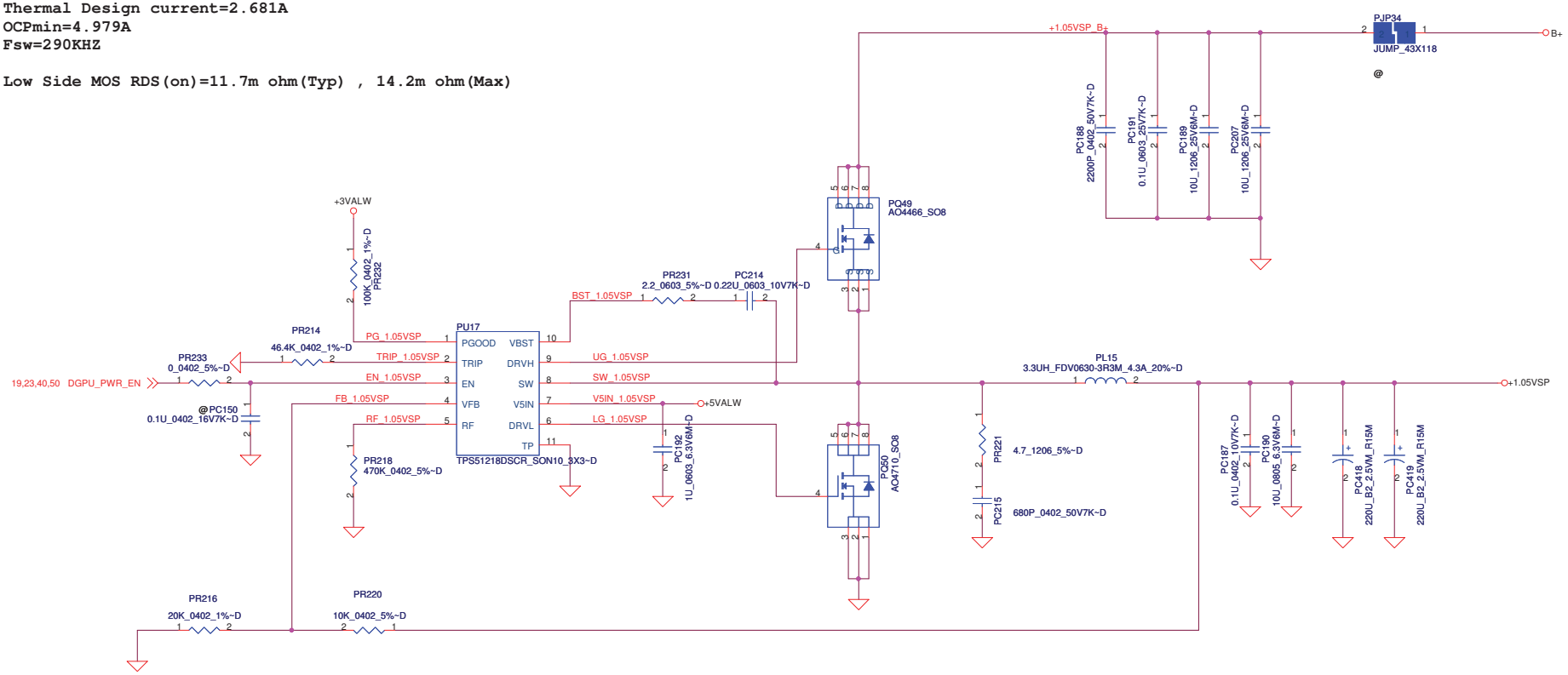
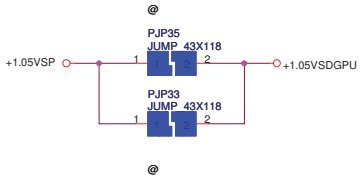
+1.05VSP
Thermal Design current=2.681A
OCPmin=4.979A
Fsw=290KHZ

Low Side MOS RDS(on)=11.7m ohm(Typ) , 14.2m ohm(Max)





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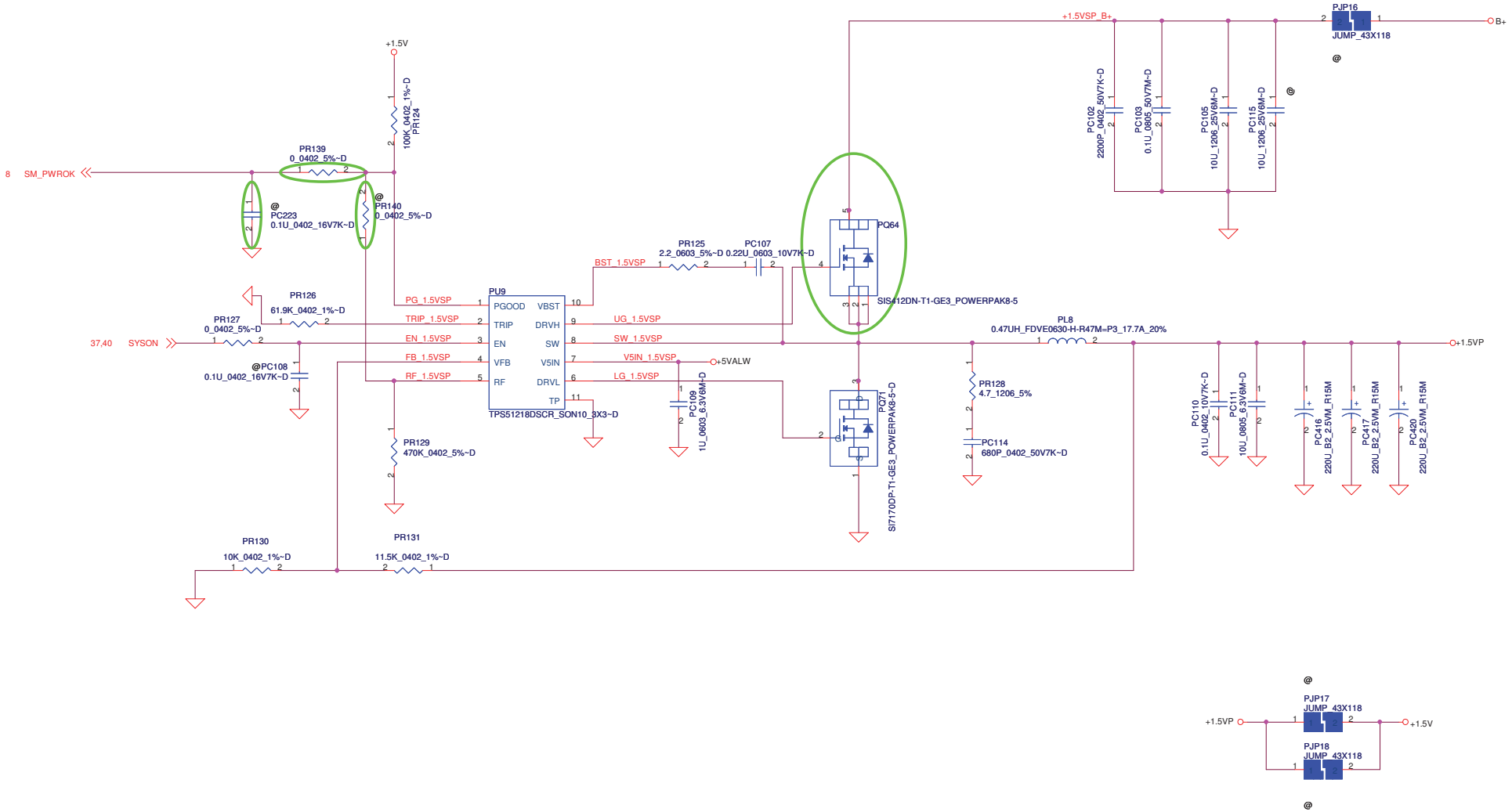
+1.5VSP
Thermal Design current=11.77A
OCPmin=21.85A
Fsw=290KHZ

Low Side MOS RDS(on)=3.6m ohm(Typ) , 4.5m ohm(Max)



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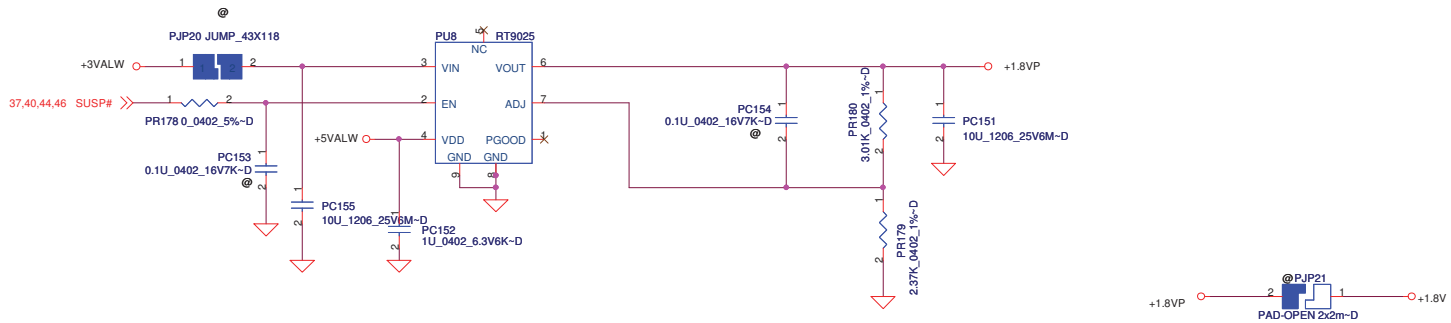
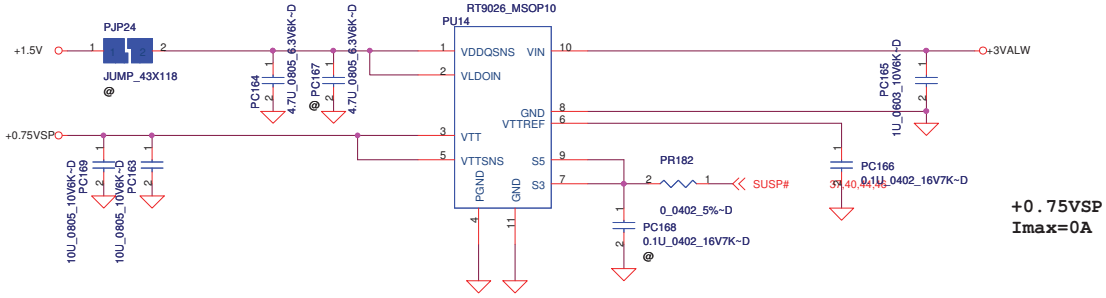


+1.8VSP
Imax=0.42A



+0.75VSP
Imax=0A

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Issued Date	2009/07/25	Deciphered Date	2010/07/25

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Title: +1.8VP / +0.75VSP

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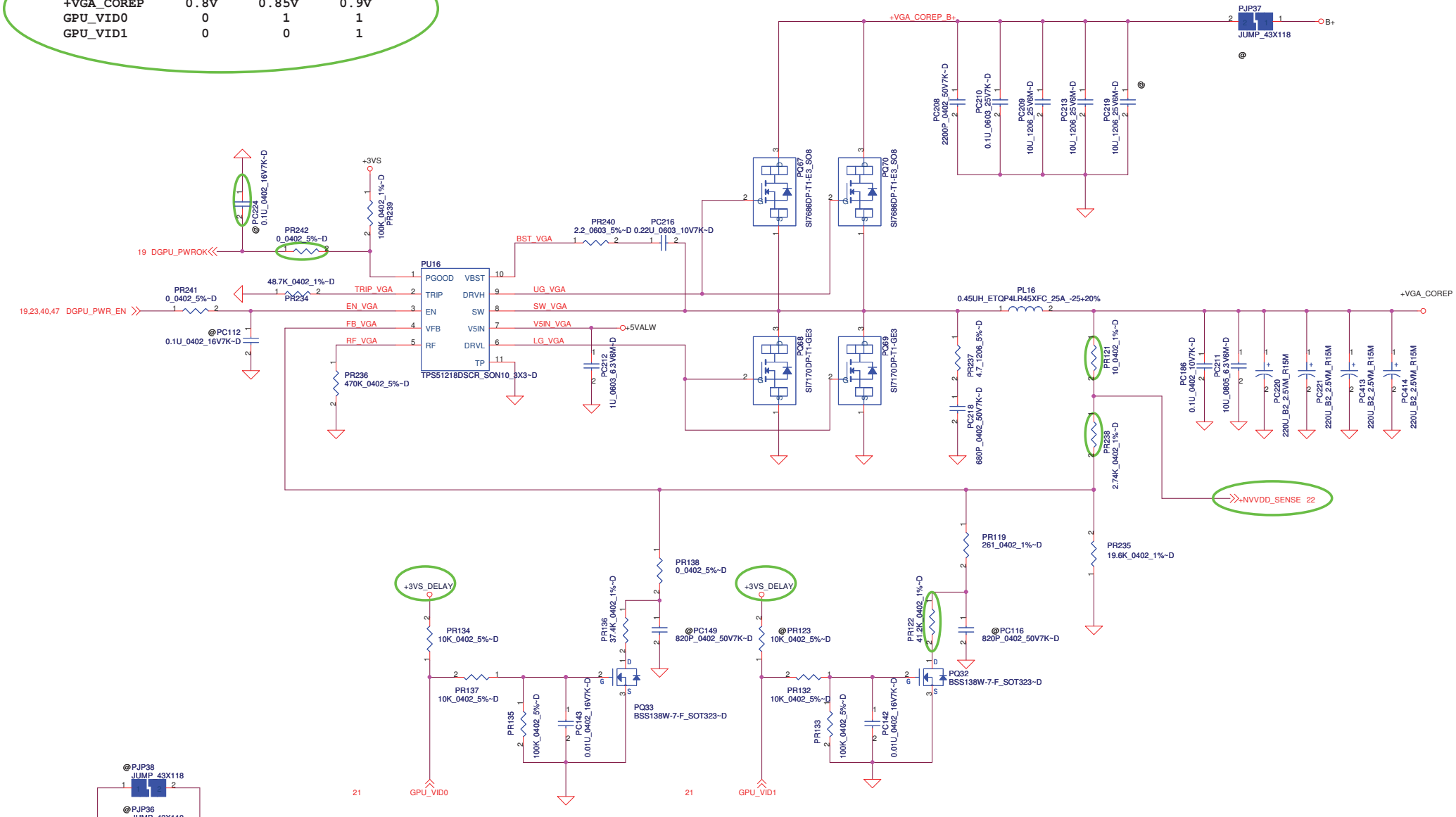
+VGA_COREP
ThermalDesigncurrent=21.525A
OCPmin=36.9A
Fsw=290KHZ
Low Side MOS RDS(on)=1.8m ohm(Typ) , 2.25m ohm(Max)

+VGA_COREP(N10P_GS1) PR122=41.2K ohm

+VGA_COREP	0.8V	0.85V	0.9V
GPU_VID0	0	1	1
GPU_VID1	0	0	1



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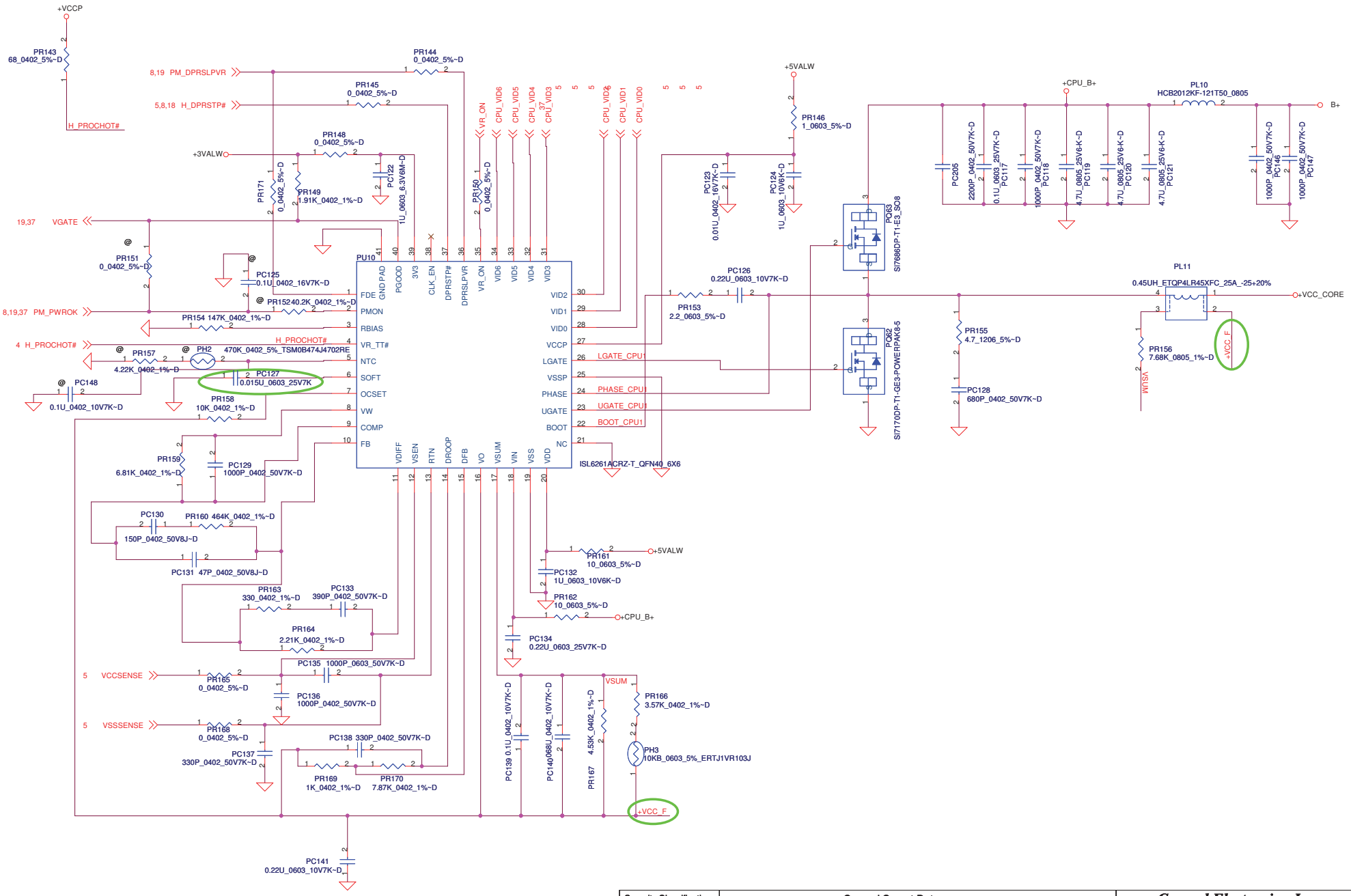

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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR119 from SD02800008L(0 ohm) to SD03426108L(261 ohm)	X00
2	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR122 from SD03424928L(24.9K ohm) to SD03419128L(19.1K ohm)	X00
3	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR136 from SD03437428L(37.4K ohm) to SD03440228L(40.2K ohm)	X00
4	50	VGA_COREP	8/17	Antony	Change output voltage	Change PR238 from SD00000AP8L(2.67K ohm) to SD03427418L(2.74K ohm)	X00
5	50	VGA_COREP	8/17	Antony	Output voltage setting 0.85V (NVIDIA request)	non-populate PR123(reserve space)	X00
6	44	CHARGER	9/10	Antony	CP point 90% setting	Change PR83 from 2.87K ohm to 2.74K ohm	X01
7	44	CHARGER	9/10	Antony	Charger voltage setting	Change PR85 from 200K ohm to 43.2K ohm	X01
8	48	+1.5VSP	9/16	Antony	EE required that SM_PWROK should change to +1.5V	Change net name PR124.1 from +3VALW to +1.5V	X01
9	50	VGA_COREP	9/16	Antony	Change VID time sequence	Change net name PR134.2 and PR123.2 from +3VS to +3VS_DELAY	X01
10	50	VGA_COREP	9/16	Antony	NVIDIA command	interchange with PR121 and PR238	X01
11	50	VGA_COREP	9/16	Antony	NVIDIA command	Delete PR139, +NVVDD_SENCE connect to PR121.2	X01
12	50	VGA_COREP	9/16	Antony	NVIDIA command	Change PR121 from 0 ohm to 10 ohm	X01
13	50	VGA_COREP	9/24	Antony	NVIDIA command	Change PR121 from 19.1K ohm to 41.2K ohm	X01
14	45	3VALWP/5VALWP	9/24	Antony	follow PSL component	Change PD19 from CH355PT to BAS316	X01
15	51	CPU_CORE	9/24	Antony	follow PSL component	Change PC127 to PSL component	X01

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Title: PWR-PIR1

Size | Document Number | Rev 1.0

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	46	+VCCPP	9/24	Antony	Change PN to 0 end	Change PQ48 from SB00000FO0L to SB00000FO00	X01
17	48	+1.5VP	9/24	Antony	Change PN to 0 end	Change PQ48 from SB00000FO0L to SB00000FO00	X01
18	50	VGA_COREP	10/1	Antony	EE required that PU16.1 pull high should change to +3VS	Change net name PR239.1 from +3VALW to +3VS	X01
19	48	+1.5VP	10/5	Antony	EMC request	Reserve PC223 space	X01
20	44	CHARGER	10/5	Antony	Quality enhancement	Reserve PQ22 from AO4466 to SI4128DY	X01
21	44	CHARGER	10/5	Antony	Quality enhancement	Reserve PQ24 from AO4466 to SI4128DY	X01
22	42	BATTERY CONN/OTP	11/13	Antony	OTP meet setting	Change PH1 100K ohm thermestor	X02
23	43	DCIN/DETECTOR	11/13	Antony	Change component size	Change PC9 to size 0603	X03
24	45	+5VALWP/+3VALWP	11/13	Antony	Change component size	Change PC68 to size 0603	X03
25	45	+5VALWP/+3VALWP	11/13	Antony	The quality improvement saggests by PCP	Change PR100 to 255K ohm	X03
26	48	+1.5VSP	11/13	Antony	Reserve 0 ohm space	Add PR139 0 ohm resistor	X03
27	48	+1.5VSP	11/13	Antony	Change component size	Change PQ64 to SIS412DN	X03
28	50	VGA_COREP	11/13	Antony	Reserve RC space	Add PR242 0 ohm resistor and reserve PC223 space	X03
29	45	+5VALWP/+3VALWP	12/21	Antony	Solve S3/S5 acoustic noise issue	PR96 de-populate	X03
30	45	+5VALWP/+3VALWP	12/21	Antony	Solve S3/S5 acoustic noise issue	Add PR108 0 ohm	X03
31	48	+1.5VSP	12/23	Antony	Reserve CCM mode resistor	Reserve PR140 space	X04

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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Rev.	PG#	Modify List
01	2009/09/07	Enable N11P-GS1 +VGA_COREP when boot system	0.2	19	Mount R238 10K ohm pull high
02	2009/09/07	U3 pin SM_PWROK schematics error for DDR3	0.2	08	U3 pin SM_PWROK connect to +1.5V
03	2009/09/07	LVDS EDID can't switch select for panel	0.2	28	Modify U20,Q119,Q120 schematics and +LCDVDD change to +3VS
04	2009/09/07	GMCH L_BKLT_CTRL isn't inverted before MUXed	0.2	28	Remove U25 for net DPST_PWM
05	2009/09/07	Switch IC U4 pin1 can not enable	0.2	28	Remove R491 0 ohm and add mount R490 0 ohm
06	2009/09/07	Change HDMI connector	0.2	31	Change connector JHDMI1
07	2009/09/07	Change Display port connector	0.2	32	Change connector JDP1
08	2009/09/10	Change D-SUB connector	0.2	30	Change connector JCRT1
09	2009/09/10	Change SIM,WWAN,WLAN,FAN connector	0.2	33	Change connector JSIM1,JWWAN1,JWLAN1,JFAN1
10	2009/09/10	Change BTB connector	0.2	36	Change connector JBTB1
11	2009/09/10	Q26 footprint error	0.2	29	Change Q26 footprint
12	2009/09/10	Audio board move IHDA signal 33ohm to MB	0.2	18	Add R8,R46,R119,R120 33ohm
13	2009/09/16	LID switch move to audio board	0.2	36	Delete U2,C2,C3,R5
14	2009/09/16	Audio board ALC665 pin9 need +1.5VS	0.2	36	Change JBTB1 pin5,pin7,pin9 to +1.5VS
15	2009/09/17	Add +3VALW for ELC function LED power	0.2	36	Change JBTB1 pin8,pin10,pin12 to +3VALW
16	2009/09/17	LID SW move from MB to audio board	0.2	36	Change JBTB1 pin6 to LID_SW#
17	2009/09/17	Modify ELC schematics fllow DELL design	0.2	38	Modify ELC schematics
18	2009/09/17	Change D16,D25,D26,D31 to PJDLC05C for EMI	0.2	29	Change BOM D16,D25,D26,D31 to SCA00001100
19	2009/09/17	DGPU +3VS_DELAY 漏電	0.2	21	Modify Q21 schematics
20	2009/09/18	Change R681 to 33ohm for EMI request	0.2	35	Change BOM R681 from 22ohm to 33ohm
21	2009/09/18	BOM mount L39,L40,L41,L42 for EMI request	0.2	31	Change BOM R579,R580,R581,R588,R591,R592,R595,R596 to @
22	2009/09/22	JP3 pin6,pin7(I2C) add PJDLC05C for EMI	0.2	38	Add D30 to JP3 pin6 and pin7
23	2009/09/22	Add 0.1uF to SM_PWROK for EMI request	0.2	08	Add C190 0.1uF
24	2009/09/22	Modify JLAN1 GND for vender request for EMI	0.2	34	Add C1162,C1163 0.1uF
25	2009/09/22	For JMicro vender request	0.2	35	C1685 4.7uF near +3V_MCVCC
26	2009/09/22	DGPU +3VS_DELAY 漏電	0.2	21	Add Q58 and R389 to net VGA_CLKREQ#_R

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Title: HW Changed-List History-1
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Item	Date	Fixed Issue	Rev.	PG#	Modify List
27	2009/09/23	Modify screw H12,H13,H17 for ME request	0.2	39	Modify screw H12,H13,H17
28	2009/09/23	Add +5VS for LED board power budget	0.2	39	Change JP3 pin9 from GND to +5VS
29	2009/09/23	Add 1000pF for EMI request	0.2	14	Add C115 1000pF
30	2009/09/23	Add 1000pF for EMI request	0.2	15	Add C196 1000pF
31	2009/09/24	Add o.1uF on PCIE CLK for vender request	0.2	34	Add C1705,C1706 0.1uF
32	2009/09/24	Add 33ohm and 22pF for EMI request	0.2	35	Add 33ohm and 22pF to JCARD1 pin7,pin16
33	2009/09/24	Change crystal X1 cap. to 27pF	0.2	37	Change BOM C1616,C1617 from 15pF to 27pF(SE071270J8L)
34	2009/09/28	Modify USB powershre schematics	0.2	36	Move L43,R617,R618 near JUSB1
35	2009/09/28	Use the USB detect method for powershare	0.2	36	BOM need mount U60,D52,D58
36	2009/09/28	For CLKRUN# issue	0.2	37	Add U39 pin38 net PM_CLKRUN#
37	2009/09/28	Net SM_PWROK add 0.1uF near PU9 for EMC	0.2	48	Net SM_PWROK add C198 0.1uF
38	2009/09/28	Net SM_PWROK add 0.1uF near U3B for EMC	0.2	08	Net SM_PWROK add C190 0.1uF
39	2009/09/29	For RF request add 47pF for WLAN,WWAN +1.5VS	0.2	33	Add C1136,C1184 47pF to +1.5VS
40	2009/09/29	Intel request delete R27,R28,R29 for layout	0.2	05	Delete R27,R28,R29
41	2009/09/29	Add JLVDS1 connector detect pin	0.2	29	Add JLVDS1 pin32 LVDS_CONN,pin33 STATUS_BOARD_CONN
42	2009/09/30	Add JBTB1 connector detect pin	0.2	36	Add JBTB1 ppin33 IO_BOARD_CONN
43	2009/09/30	Add JP3 connector detect pin	0.2	38	Add JP3 pin15 STATUS_BOARD_CONN,pin16 IO_BOARD_CONN
44	2009/09/30	EC add JLVDS1,JBTB1,JP3 connector detect pin	0.2	37	Add LVDS_CONN to U39 pin18
45	2009/10/01	Add display port AUX schematics	0.2	32	Add Q123,Q124,Q125,R602,R603,R613,R614
46	2009/10/01	Add a FET for CPU overclocking	0.2	06	U39 pin25 add a net EC_FSB_SEL
47	2009/10/05	Add I2CB,I2CH pull high for NVIDIA request	0.2	15	Add R420,R421,R422,R423 pull high to +3VS_DELAY
48	2009/10/06	For Intel request change C1702 BOM	0.2	40	Change C1702 from 0.01uF to 0.1uF
49	2009/10/06	Change BOM error	0.2	23	Change C191,C192,C197,C261,C262,C263 from SE00000JM00 to SE00000MM1M
50	2009/10/08	Change Q35 Id to 300mA	0.2	23	Change Q35 from SB000008J00 to SB000003P10
51	2009/11/05	Change USB D+ and D-	0.3	36	Swap L43 USB signal USBP2_D-_C and USBP2_D+_C
52	2009/11/05	Change location R263 to C271	0.3	19	Change location R263 to C271 for layout.

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Item	Date	Fixed Issue	Rev.	PG#	Modify List
53	2009/11/05	Add 100K pull low for EC debug request	0.3	33	Add JWWAN1 pin49 R657 100K pull low to GND for net EC_TX
54	2009/11/05	Change BIOS ROM part to another PN	0.3	37	Change U41 BOM from SA00001IT0L to SA00002TO0L
55	2009/11/09	Change C189,C195,C202 BOM	0.3	23	Change C189,C195,C202 PN from SE00000IS0A to SE076104K80
56	2009/11/09	Change C1105 BOM	0.3	36	Change C1105 PN from SE000000GK0 to SE00000GC0L
57	2009/11/09	Change C191,C192,C197,C261,C262,C263 BOM	0.3	23	Change C191,C192,C197,C261,C262,C263 PN from SE00000MM1M to SE076473K8L
58	2009/11/10	Add 10K pull high for LAN LED leakage	0.3	34	Add R662,R664 10K pull high to +3V_LAN
59	2009/11/10	Reserved 10K pull high for LID_SW#	0.3	37	Add R665 10K pull high to +3VALW
60	2009/11/10	Modify board ID	0.3	37	Mount R622 100K,R627 20K
61	2009/11/10	Modify U4 pin13,pin14	0.3	16	change R142,R352 to 22ohm,1%
62	2009/11/11	Reserved GPIO49 for DGPU_PWR_EN	0.3	19	Add R263,R268 0 ohm to net DGPU_PWR_EN
63	2009/11/11	For ESD request change D30 PN	0.3	38	Change D30 PN from SCA00001100 to SCA00000200
64	2009/11/12	Change R500 to 110ohm for LCD panel EA	0.3	29	Change R500 from 300ohm to 110ohm
65	2009/11/16	Modify JTP1 footprint for layout	0.3	39	Modify JTP1 footprint
66	2009/11/17	Add a 0603 size 0ohm for LVDS SW thermal	0.3	28	U19 pin 57 add a R329 0ohm to GND
67	2009/11/17	Reserved a jump for HDD 3.3V	0.3	32	Add a J3 to +3VS and C1628,C1634
68	2009/11/17	Change U42 pin8 from +5VS to +5VALW	0.3	38	Change U42 pin8 to +5VALW
69	2009/11/18	Reserved 0.1uF,22P for U42 pin6	0.3	38	Add R139,C1843,C313 to U42 pin6
70	2009/11/20	Net VGA_CLKREQ#_R 重複 pull H to +3VS_DELAY	0.3	21	BOM delete R406 10K ohm
71	2009/11/20	Change Q35 to AO3414 for +1.8VSDGPU 300mA	0.3	23	Change BOM Q35 from SB000003P10 to SB000007600
72	2009/11/20	Change Q11 to SI7121DN for +3VS_DELAY 1380mA	0.3	23	Change Q11 from SB923010020 to SB00000KI00
73	2009/11/20	U42 reserved 0.1uF for RF request.	0.3	38	Add C1857,C1858,C1859,C1860,C1861,C1862,C1863,C1864,C1865,C1866,C1867 0.1uF
74	2009/11/20	Change BOM error.	0.3	40	Change C1702 from 0.1uF to 0.01uF
75	2009/12/16	Modify board ID	1.0	37	Mount R628 37.4K and delete R627 20K
76	2009/12/16	Change DGPU_PWR_EN from GPIO18 to GPIO49	1.0	19	BOM mount R268 0 ohm and delete R263 0 ohm
77	2009/12/16	For DGPU thermal error modify power sequence	1.0	23	BOM mount R210,C207 and change R118 to 68K,C168 to 0.22uF
78	2009/12/16	For nVIDIA request change R571,R568 value	1.0	31	Change BOM R571,R568 from 10K(SD028100280) to 2.2K(SD028220180) or 4.7K

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Item	Date	Fixed Issue	Rev.	PG#	Modify List
103	2009/12/28	Change BOM for DELL 禁用料	1.0	23	Change C1664,C1694,C179,C245,C252,C492,C1564,C1693 from SC1H751H01L to SC1SS355010
104	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change C90 from SE000005T80 to SE000005T8L
105	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change C93 from SE000008L80 to SE000008L0L
106	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change C1117,C1142,C86 from SE049225Z80 to SE049225Z8L
107	2009/12/28	Change BOM for DELL 禁用料	1.0	34	Change C1654 from SE067102K80 to SE067102K8L
108	2009/12/28	Change BOM for DELL 禁用料	1.0	20	Change C286,C288,C289,C290,C293,C304 from SE070104Z80 to SE070104Z8L
109	2009/12/28	Change BOM for DELL 禁用料	1.0	08	Change C1514,C1519,C1528,C1532,C210,C211,C215,C232,C237 ,C241,C72,C74 from SE075103K80 to SE068103K8L
110	2009/12/28	Change BOM for DELL 禁用料	1.0	40	Change C1696,C1697 from SE075103ZN0 to SE068103K8L
111	2009/12/28	Change BOM for DELL 禁用料	1.0	07	Change C56,C57,C58 from SGA20221D40 to SGA20221E8L
112	2009/12/28	Change BOM for RF team request	1.0	29	Change C231,C238 from SE07150AC00 to SE07122AC8L

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Item	Date	Fixed Issue	Rev.	PG#	Modify List
79	2009/12/16	Change L52 part number	1.0	23	Change BOM L52 from SHI00006N0L to SHI00005V0L
80	2009/12/17	Change Q11 Compal PN	1.0	23	Change Q11 from SB00000KI00 to SB00000MK00
81	2009/12/18	Change L39,L40,L41,L42 PN for EMI	1.0	31	Change L39,L40,L41,L42 from SM070000K00 to SM070000I00
82	2009/12/20	Change C1616,C1617 to 18PF	1.0	37	Change C1616,C1617 from SE071270J8L to SE071180J80
83	2009/12/20	Change BOM for cost	1.0	11	Change C5,C84,C146 from SGA19331D10 to SGA00002680
84	2009/12/20	Change BOM for cost	1.0	12	Change C153 from SE124474KT0 to SE124474K80
85	2009/12/20	Change BOM for cost	1.0	12	Change C153 from SE000000GK0 to SE000003H00
86	2009/12/21	Change BOM for DELL 禁用料	1.0	23	Change C179,C245,C252,C492,C1664,C1693,C1694
					from SE000000I10 to SE00000110L
87	2009/12/21	Change BOM for DELL 禁用料	1.0	11	Change C93 from SE000008L80 to SE000008L0L
88	2009/12/22	Change BOM for DELL 禁用料	1.0	23	Change C72,C74,C210,C211,C215,C232,C237,C241,C258,C1514,C1519,C1528,C1532
			1.0		from SE075103K80 to SE068103K8L
89	2009/12/22	Change BOM for DELL 禁用料	1.0	40	Change C1696,C1697 from SE075103ZN0 to SE068103K8L
90	2009/12/22	Change BOM for DELL 禁用料	1.0	07	Change C56,C57,C58 from SGA20221D40 to SGA20221E8L
91	2009/12/22	Change LVDS switch IC	1.0	28	Change U19 from SA00001RM0L to SA00003O900
92	2009/12/22	Modify BOM for cost	1.0	32	BOM @ C1628,C1634
93	2009/12/22	Modify JKB1 footprint for 2nd source DFX	1.0	37	Modify JKB1 LTCX0020V0L footprint to TYCO_2-2041084-5_25P-T
94	2009/12/23	Change BOM for DELL 禁用料	1.0	17	Change U10 from SA007080B9L to SA007080B90
95	2009/12/23	Change BOM for DELL 禁用料	1.0	29	Change Q23,Q34,Q36,Q59 from SB000008J00 to SB570020110
96	2009/12/23	Change BOM for DELL 禁用料	1.0	23	Change Q10,Q12,Q46,Q47,Q52,Q56 from SB000009610 to SB00000960L
97	2009/12/28	Change BOM for DELL 禁用料	1.0	28	Change Q119,Q120,Q21,Q29,Q30 from SB00000AR00 to SB57002528L
98	2009/12/28	Change BOM for DELL 禁用料	1.0	19	Change Q8,Q9 from SB502060000 to SB50206008L
99	2009/12/28	Change BOM for DELL 禁用料	1.0	29	Change Q28,Q58 from SB570020020 to SB57002008L
100	2009/12/28	Change BOM for DELL 禁用料	1.0	29	Change Q26 from SB570020400 to SB57002041L
101	2009/12/28	Change BOM for DELL 禁用料	1.0	40	Change Q51,Q53,Q54 from SB570025280 to SB57002528L
102	2009/12/28	Change BOM for DELL 禁用料	1.0	11	Change D1,D13,D15,D5,D6 from SC1H751H01L to SC1SS355010

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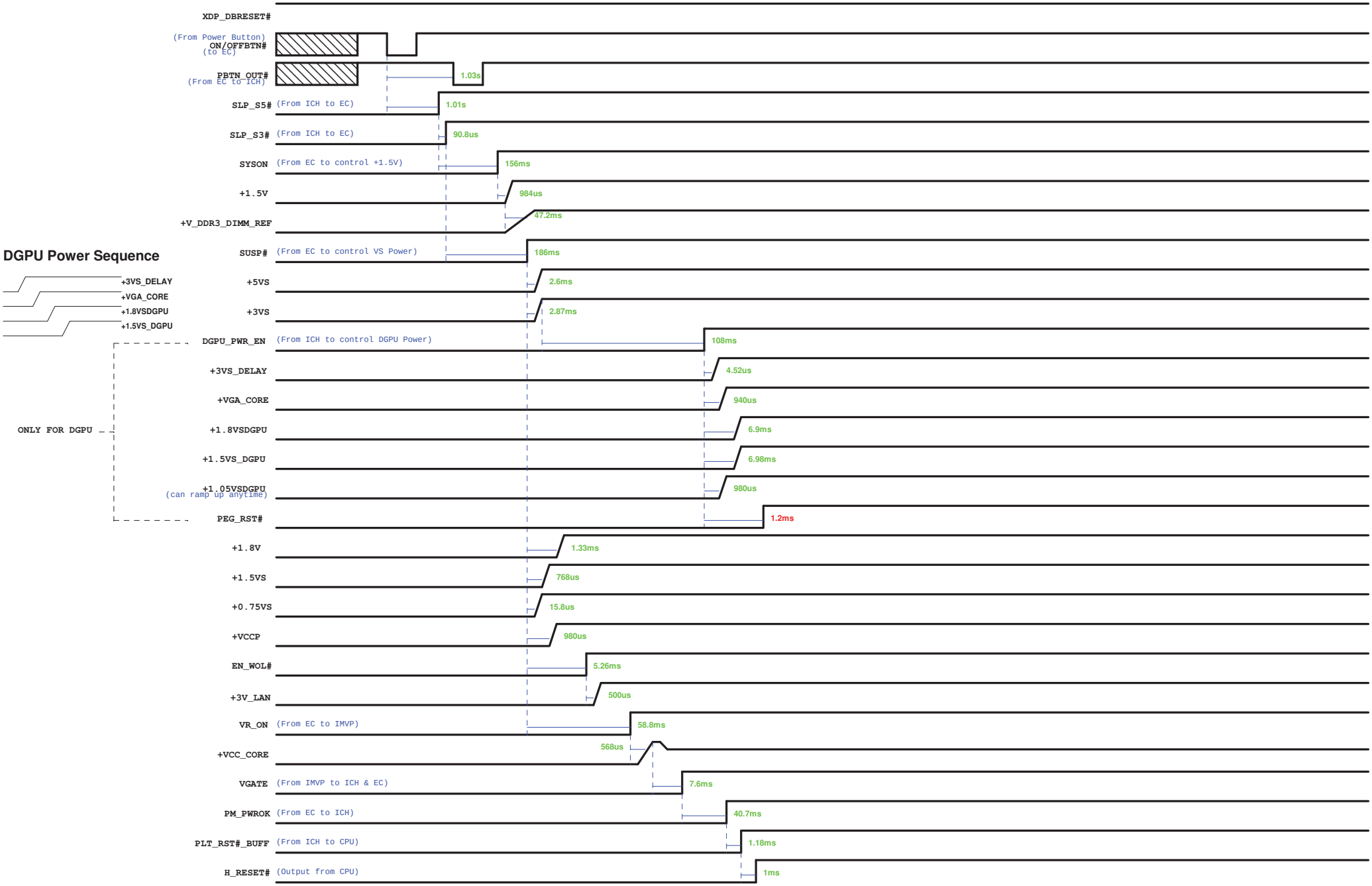
NAP00 Power On Sequence



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