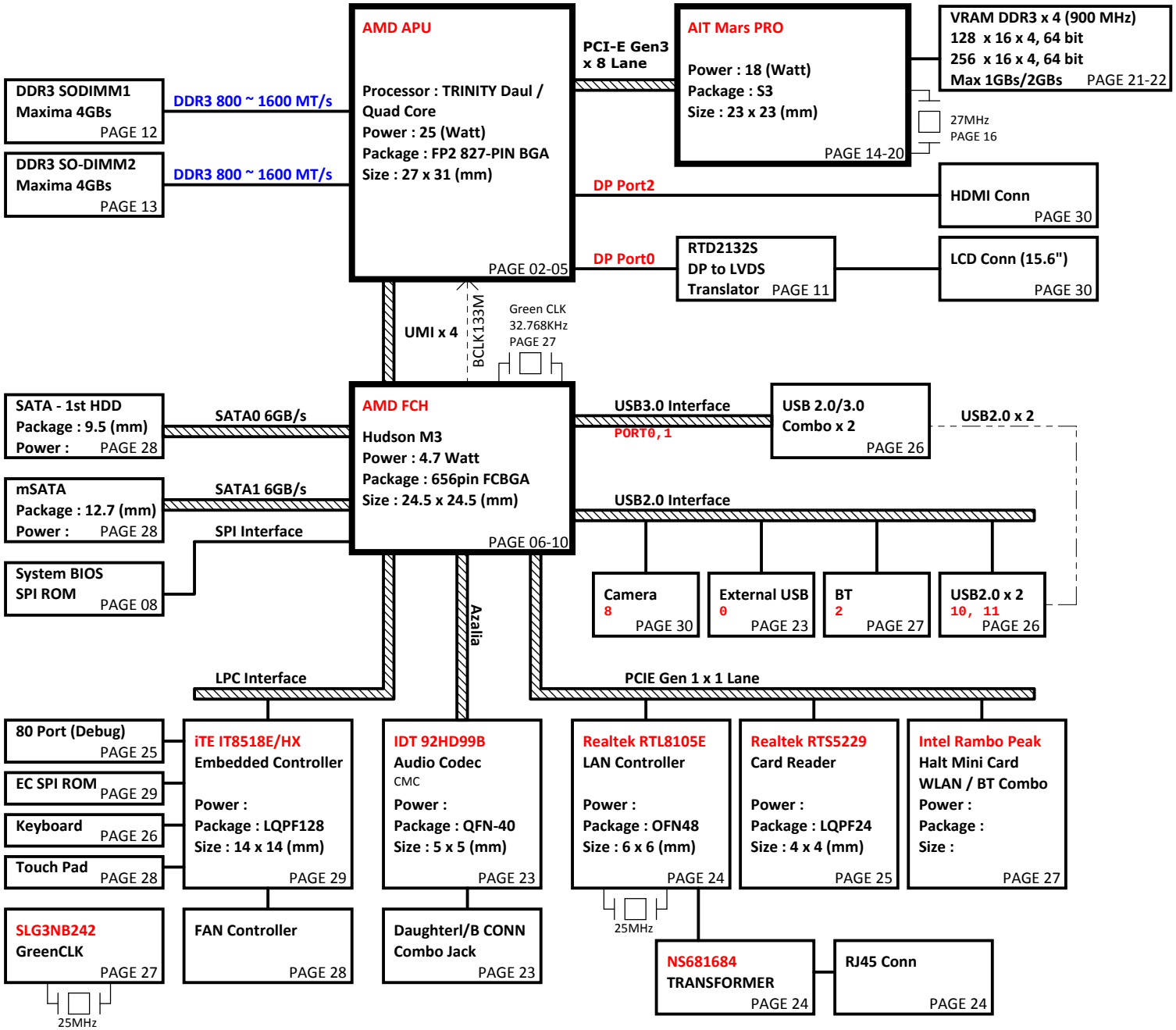
Tiguan1.0_AMD Comal DIS/UMA (15.6") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLANVCC/+1.1V)

Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

ISL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

Richtek RT8228AZ
PCH Power (+1.1VS5)

RT8152E/G5193/G5193R41U/NB650
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)

NB5

PROJECT : U56
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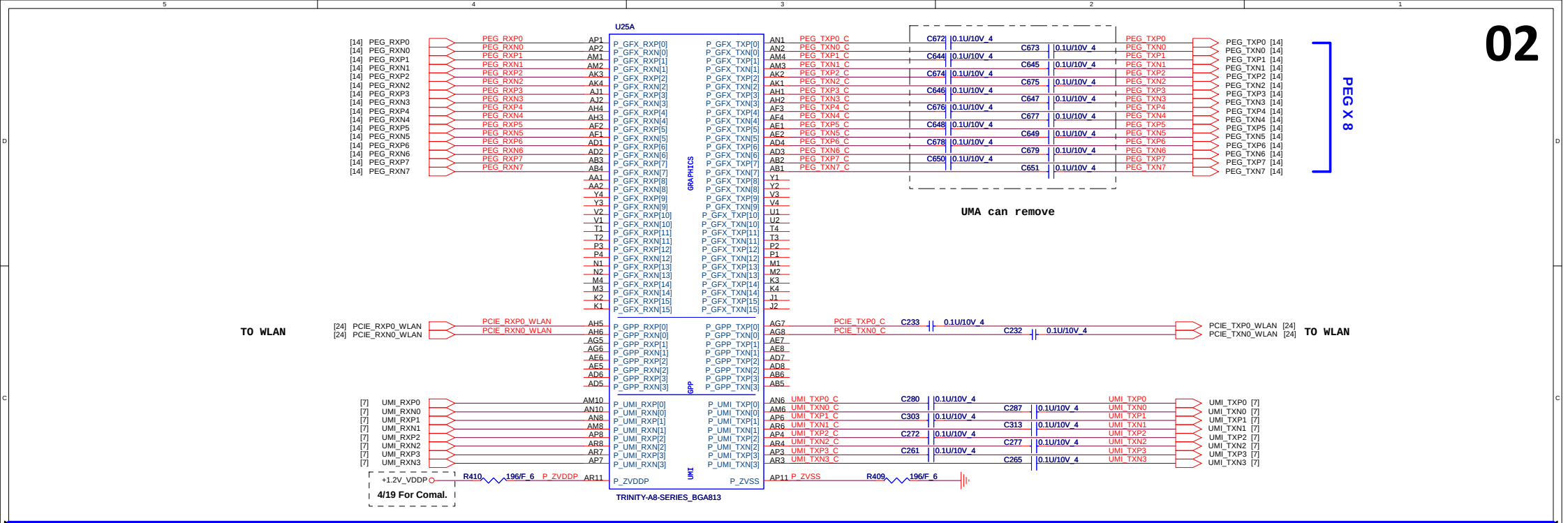
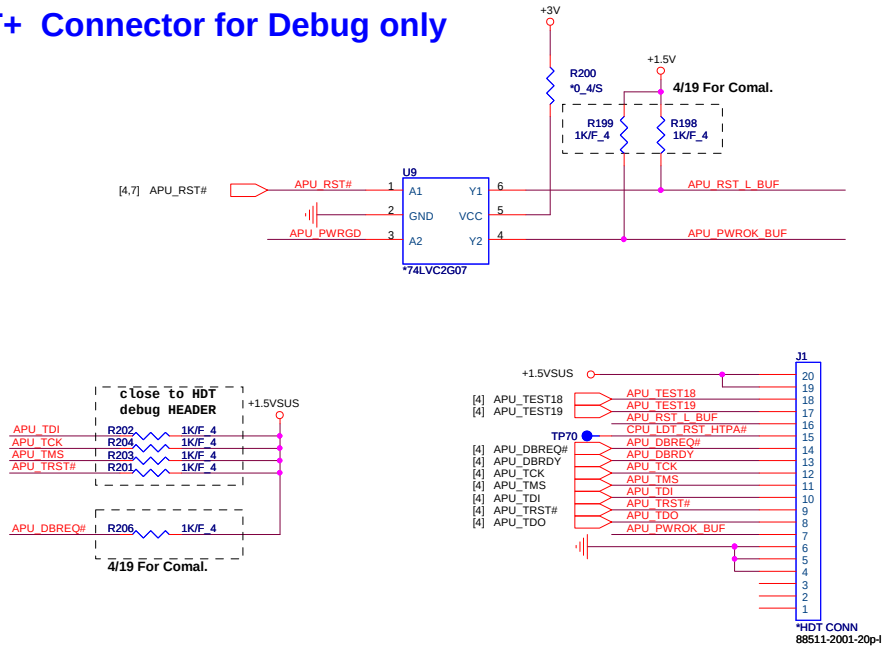
Size	Document Number	Rev
A3	Block Diagram	1A

Date: Thursday, August 09, 2012 | Sheet 1 of 39



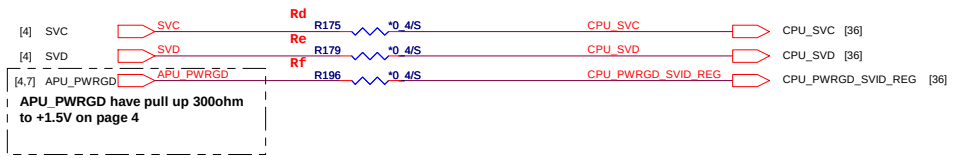
HDT+ Connector for Debug only



VID Override Circuit

Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.

	BOOT VOLTAGE		
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



NB5

PROJECT : U56
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Size	Document Number	Rev
Custom	Llano PCIE/UMI/GPP	1A

Date: Tuesday, August 07, 2012 Sheet 2 of 39

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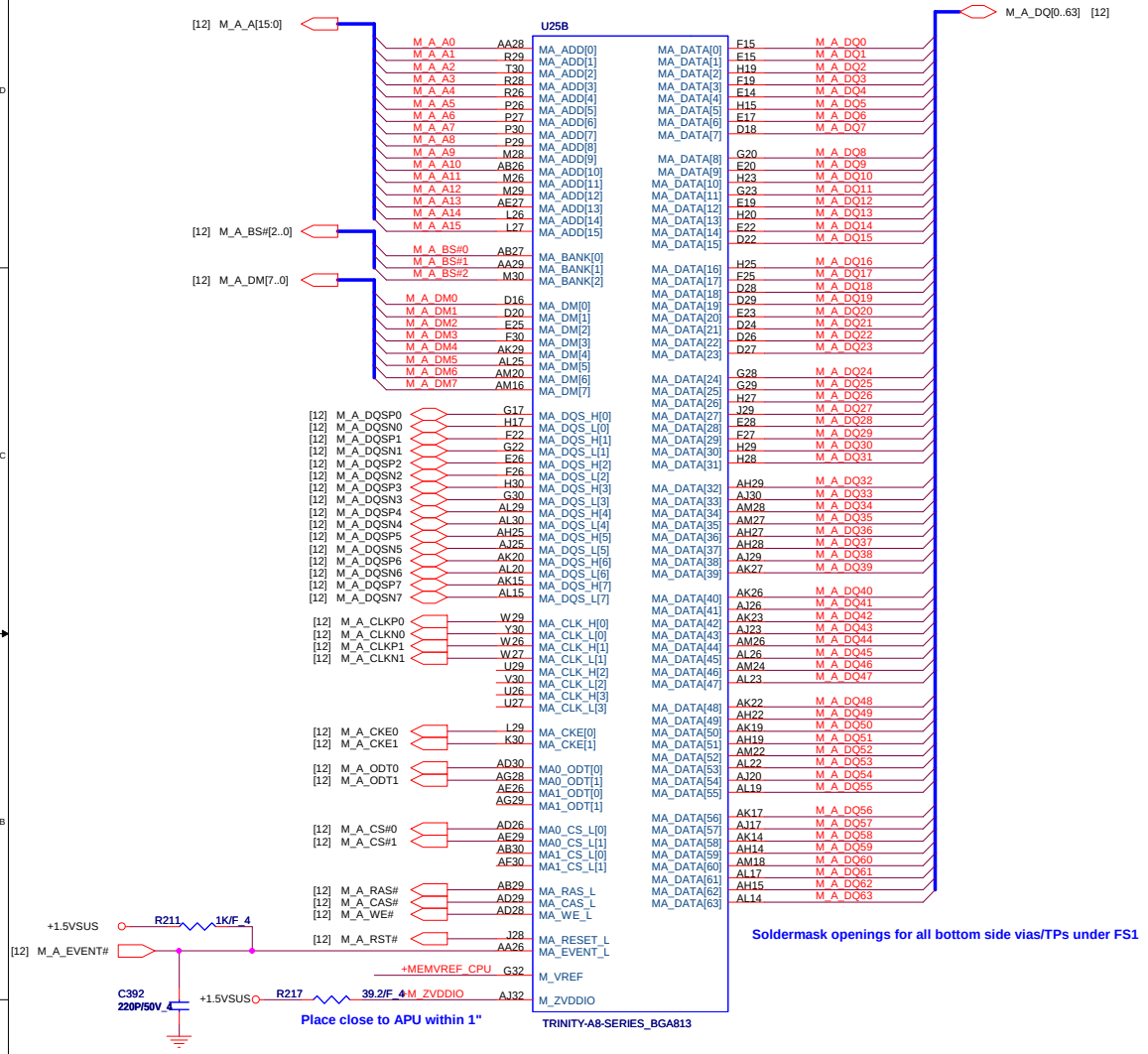
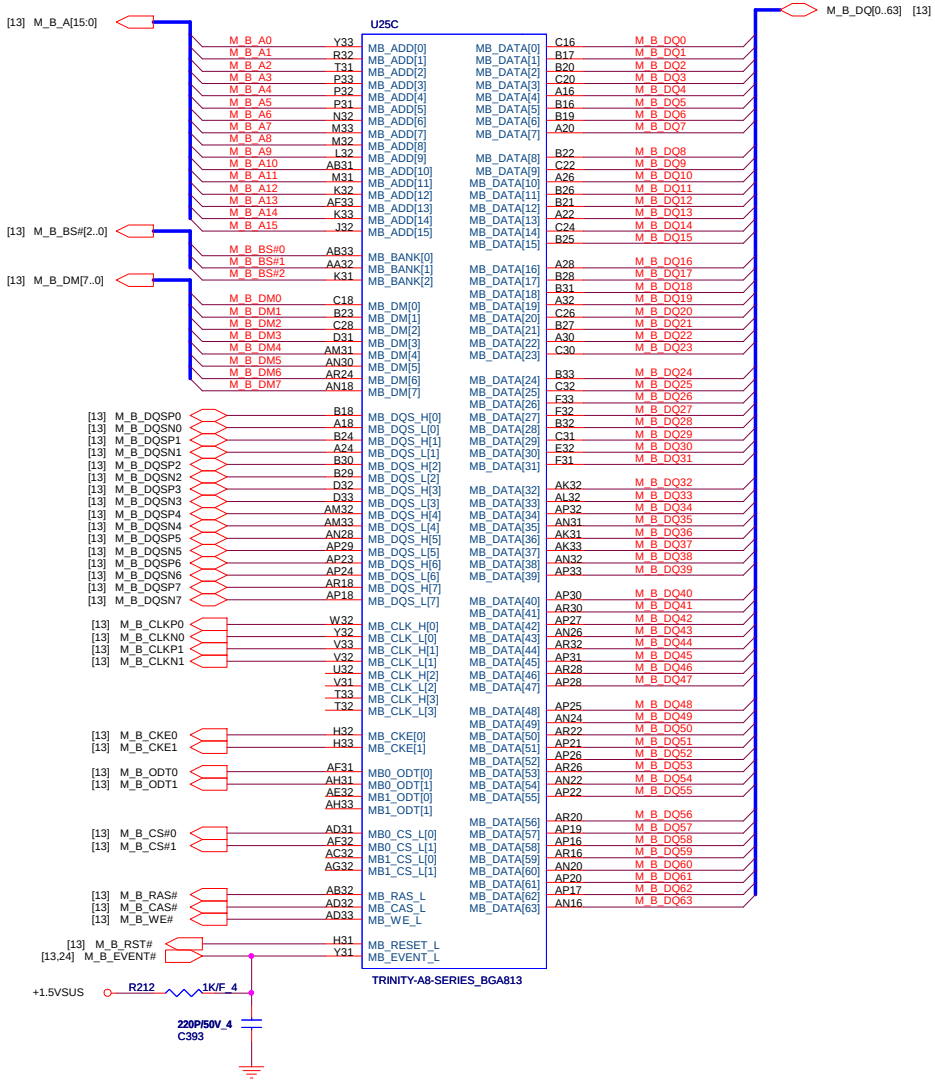
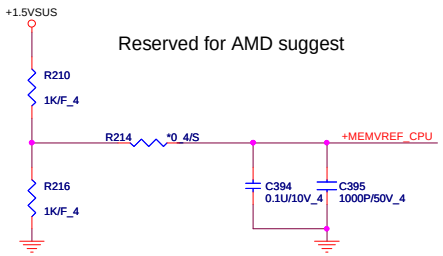


Soldermask openings for all bottom side vias/TPs under FS1





PROJECT : U56
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NB5

Size	Document Number	Rev
Custom	Llano DDR3 MEM I/F	1A

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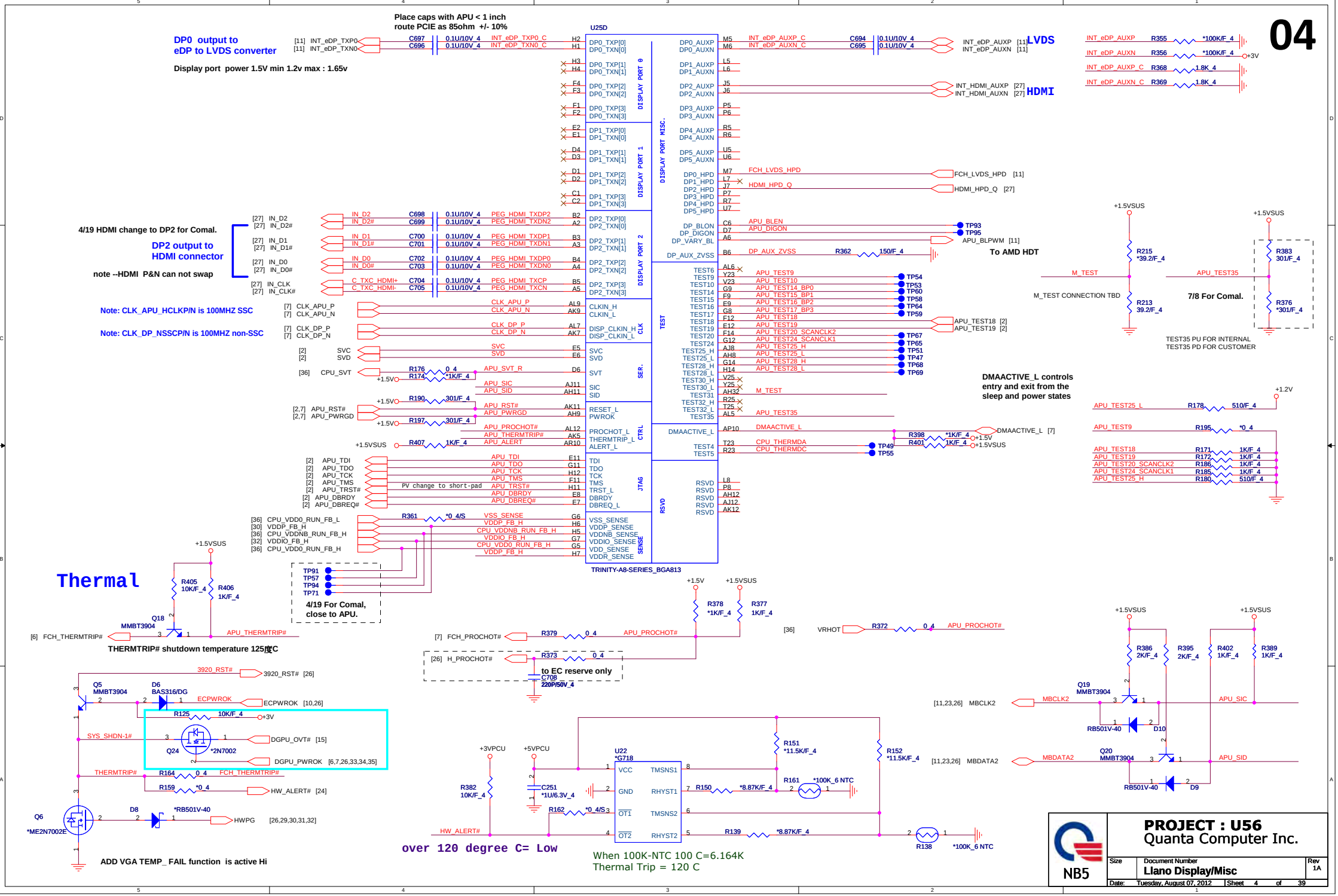

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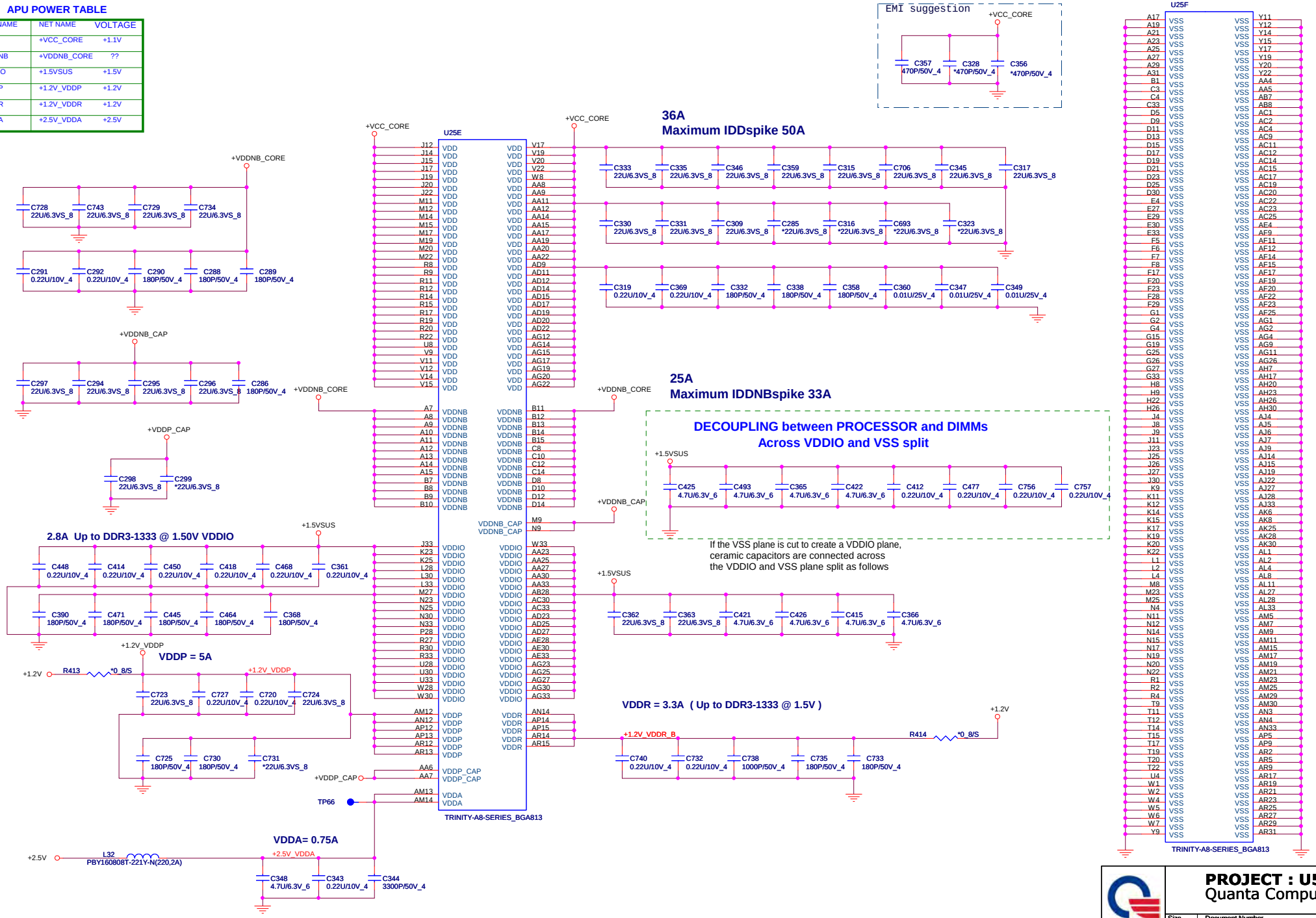
APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



PROJECT : U56
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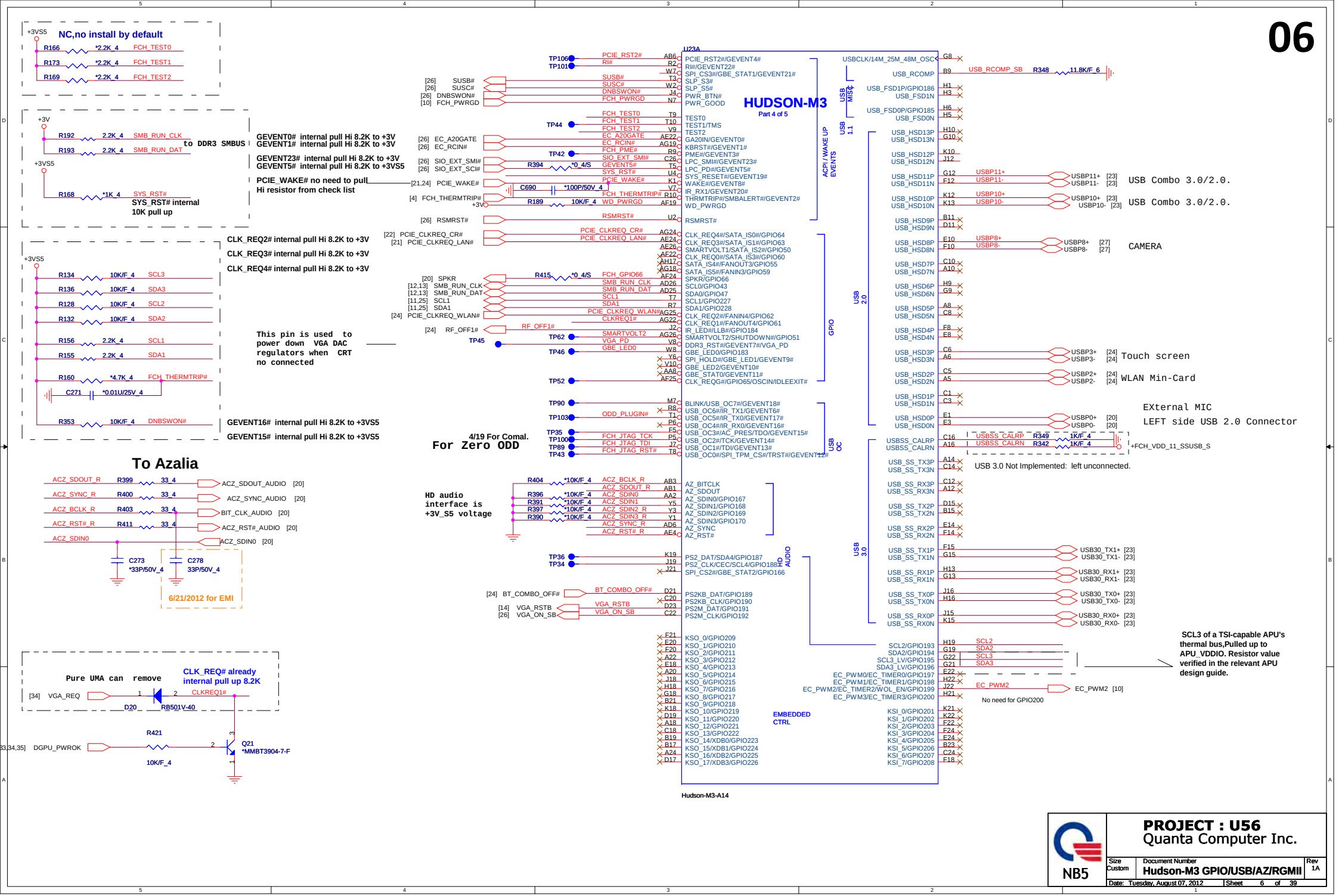
NB5

Size	Document Number	Rev
Custom	Llano POWER/GND	1A

Date: Wednesday, July 11, 2012 Sheet 5 of 39



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NB5

Size	Document Number	Rev
Custom	Hudson-M3 GPIO/USB/AZ/RGMII	1A

Date: Tuesday, August 07, 2012 Sheet 6 of 39

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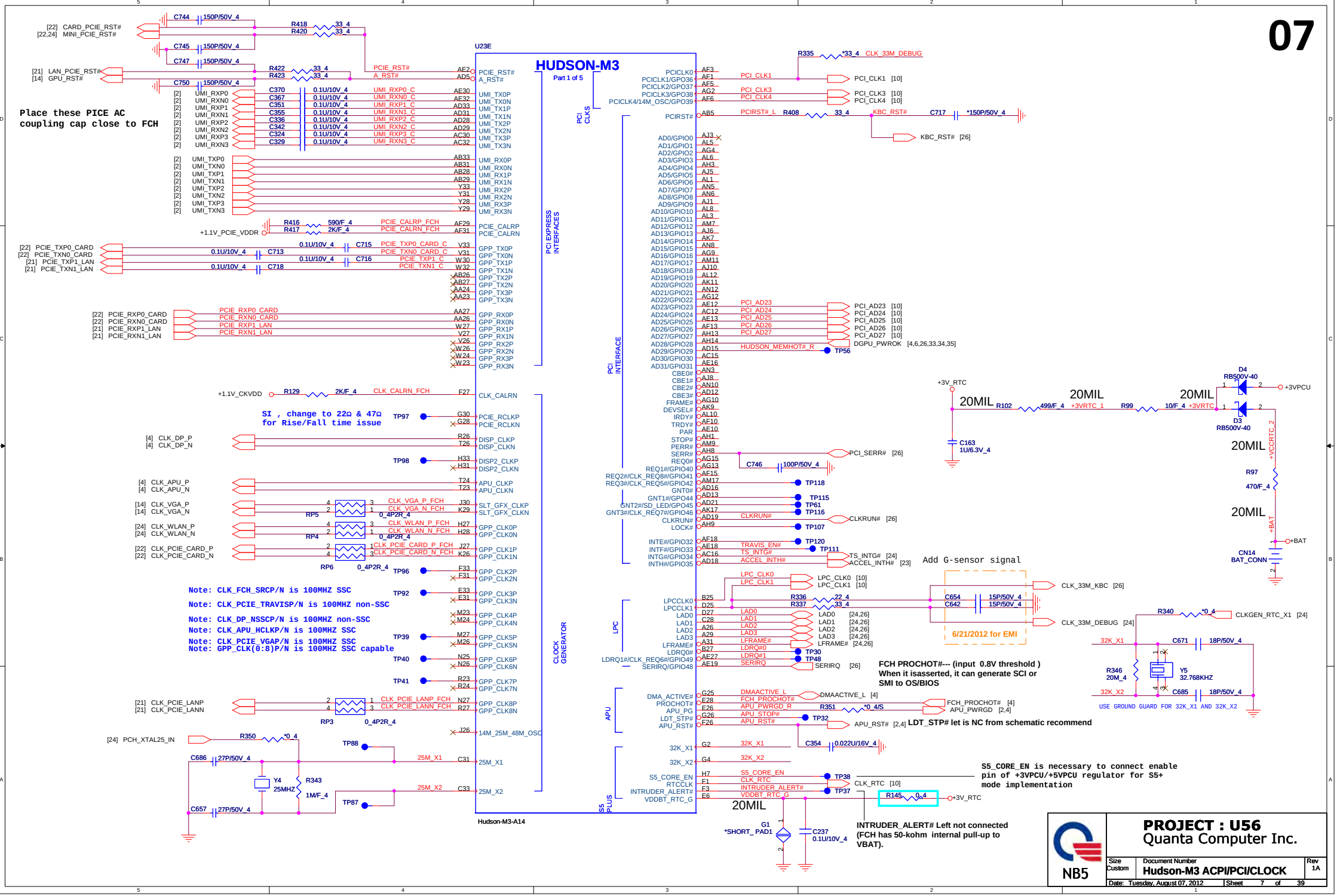

PROJECT : U56
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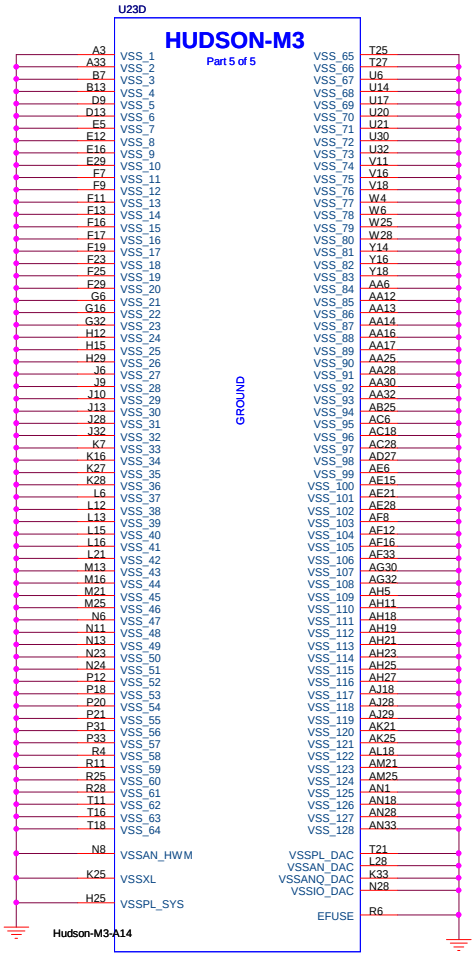
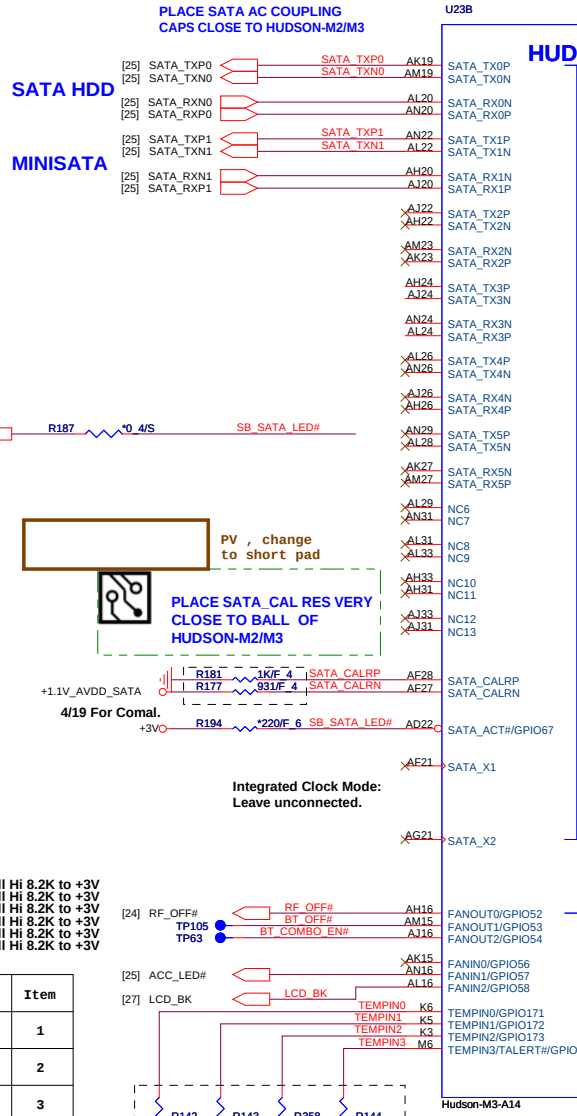
NB5

Size	Document Number	Rev
Custom	Hudson-M3 ACPI/PCI/CLOCK	1A

Date: Tuesday, August 07, 2012 Sheet 7 of 39



PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON-M2/M3



PV , change to short pad

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

4/19 For Comal.

Integrated Clock Mode:
Leave unconnected.

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

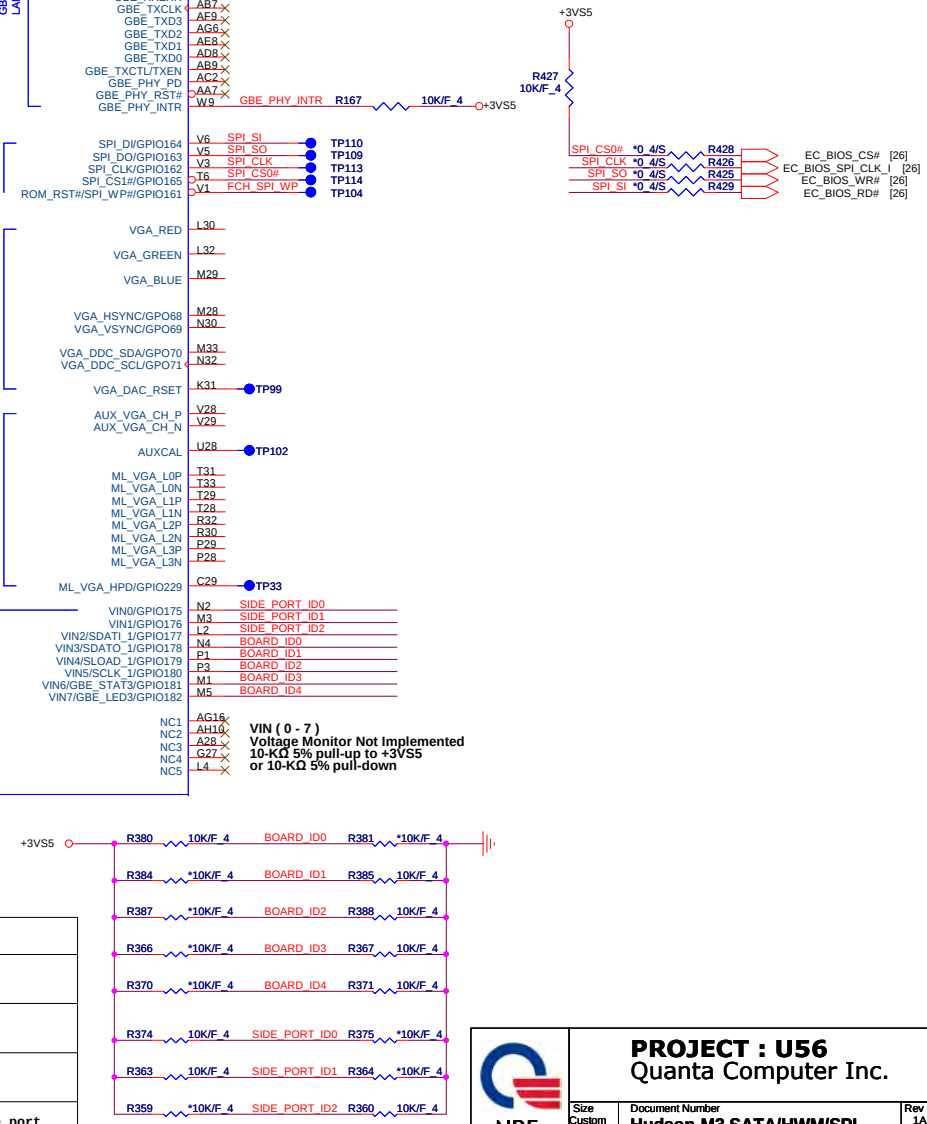
TEMP(0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

VIN (0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port



Size	Document Number	Rev
Custom	Hudson-M3 SATA/HWM/SPI	1A

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NB5

Date: Tuesday, August 07, 2012 Sheet 8 of 39

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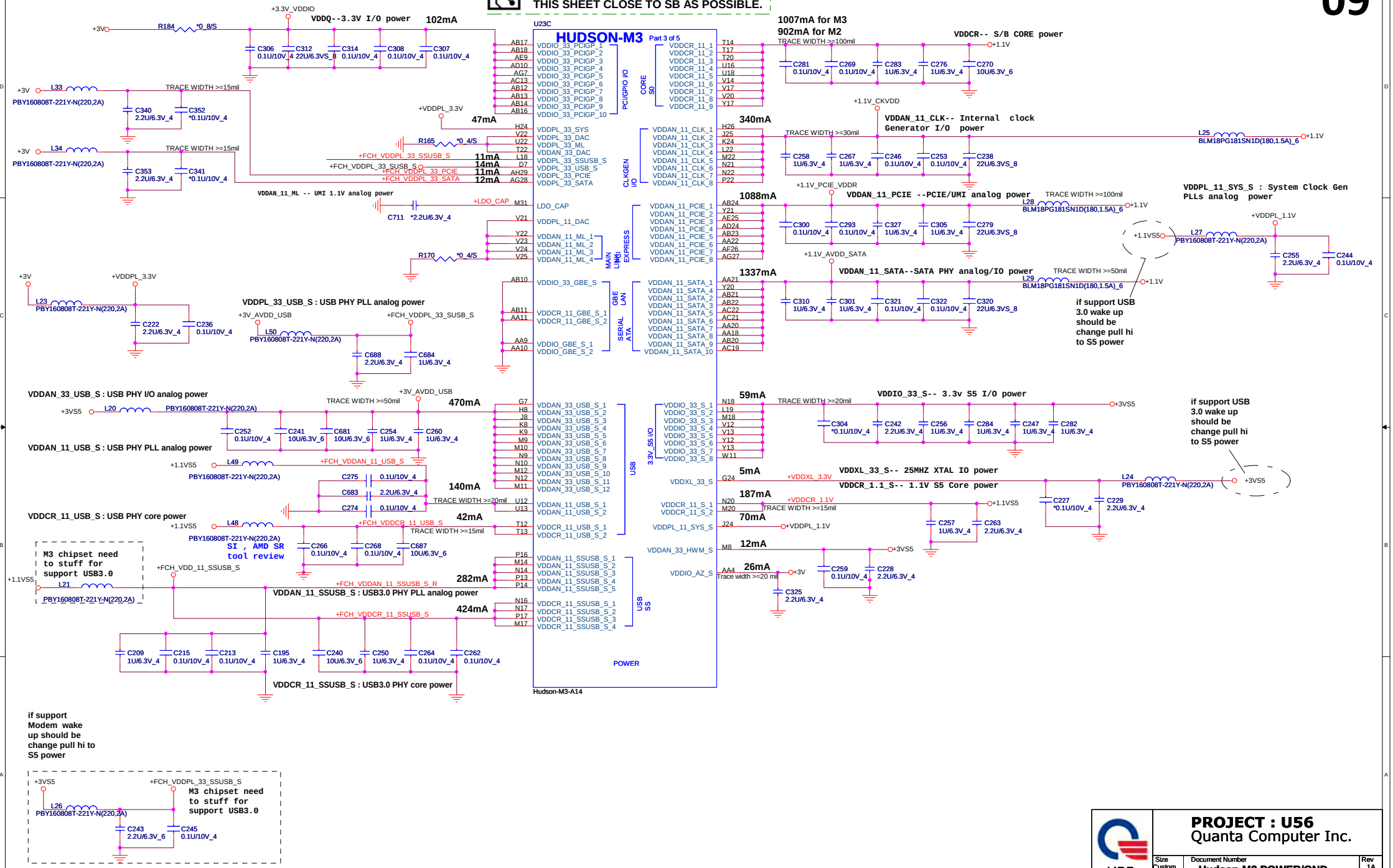
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



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NB5

Size	Document Number	Rev
Custom	Hudson-M3 POWER/GND	1A

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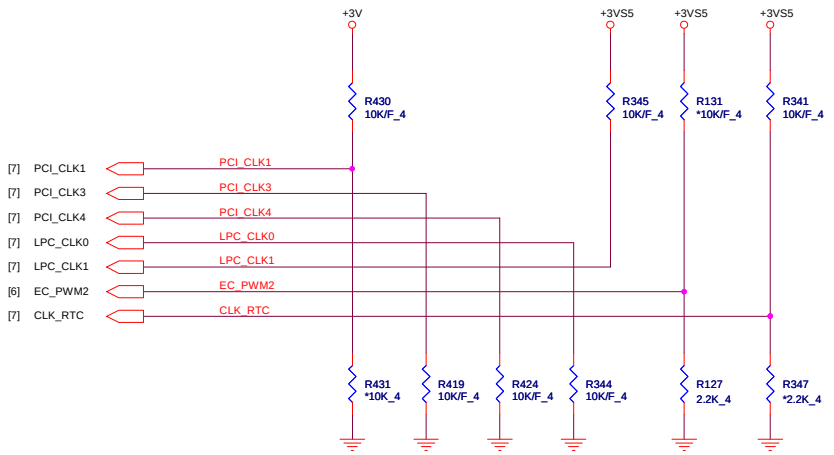
STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

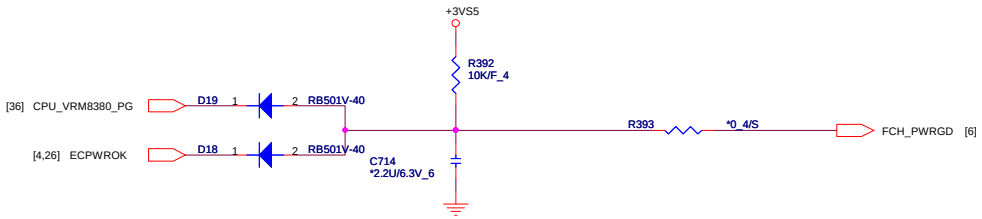
DEBUG STRAPS

10

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD



NB5

PROJECT : U56
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Size	Document Number	Rev
Custom	Hudson-M3 STRAP/PWRGD	1A

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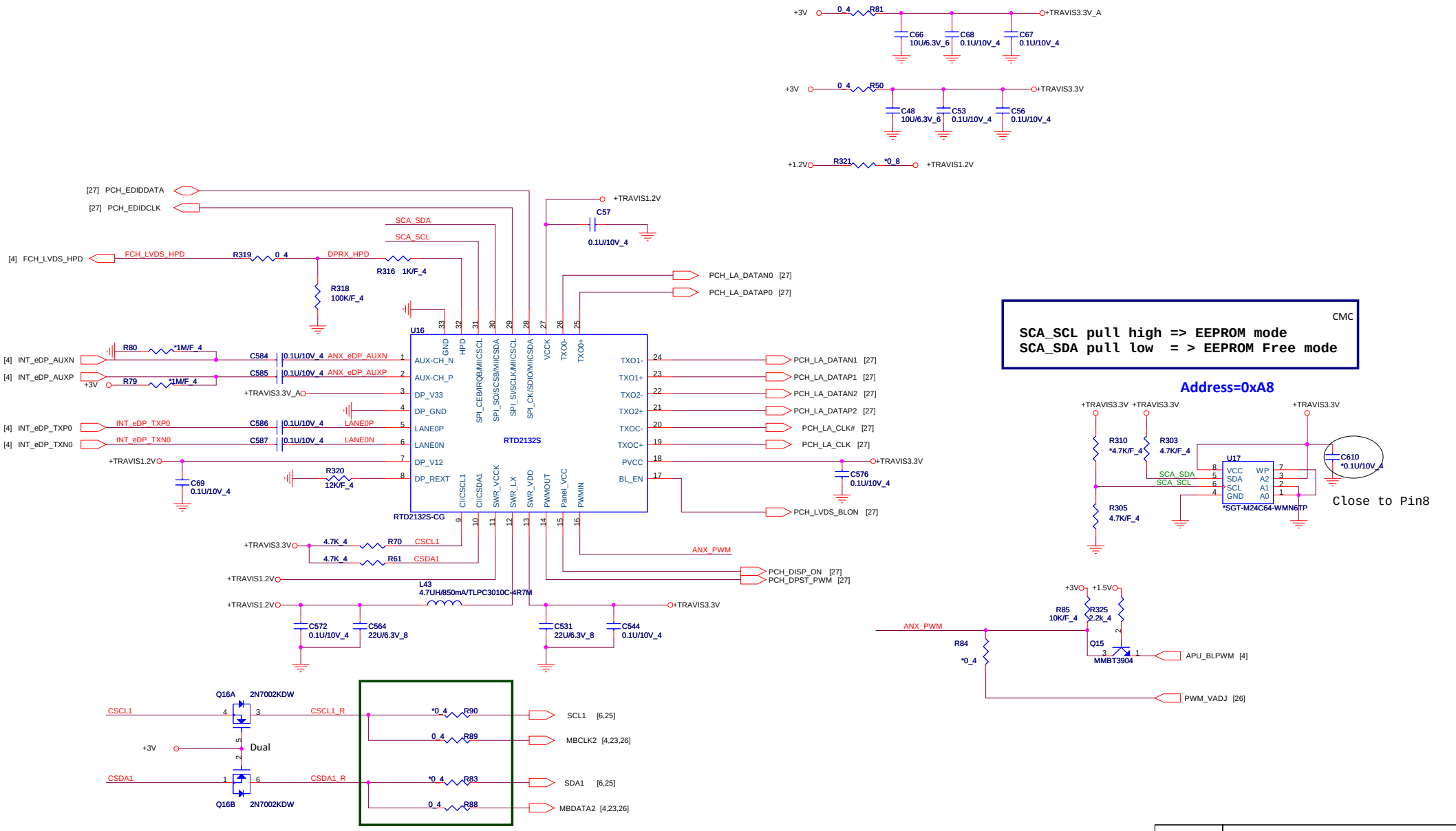

EE PROM R3054,R3056
EC OPTION R3055,R3057

NB5

PROJECT : U56
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Size	Document Number	Rev
Custom	RTD2132S	1A

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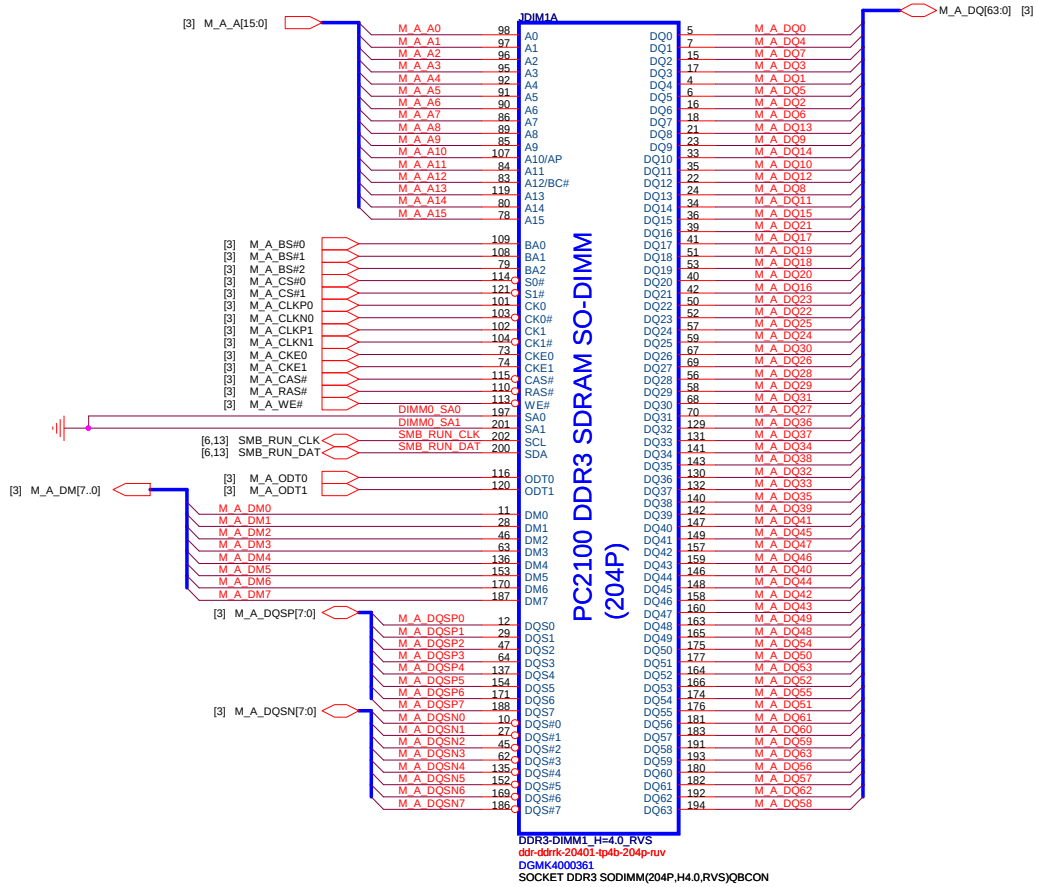
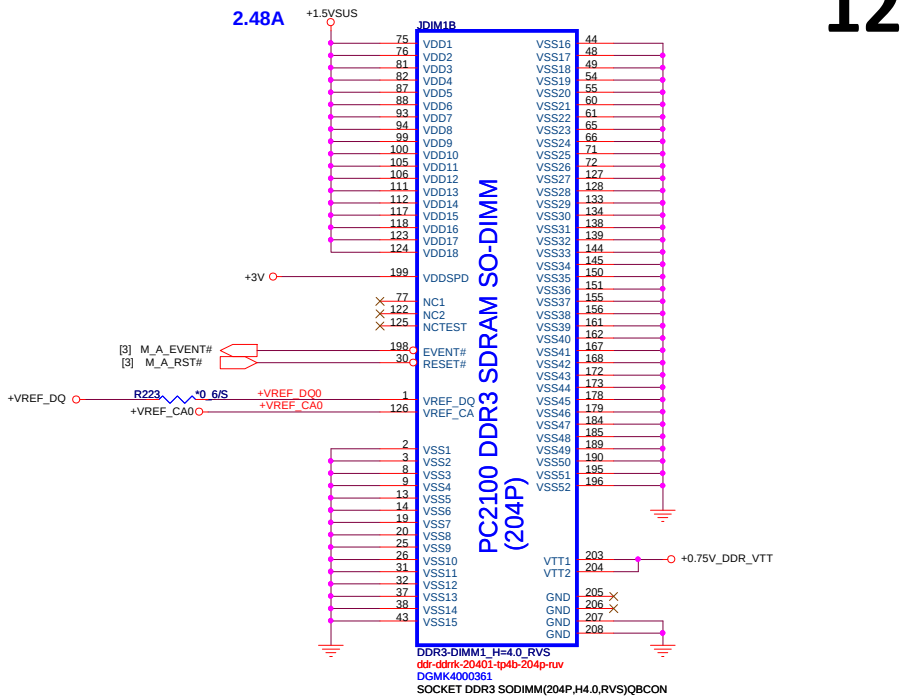
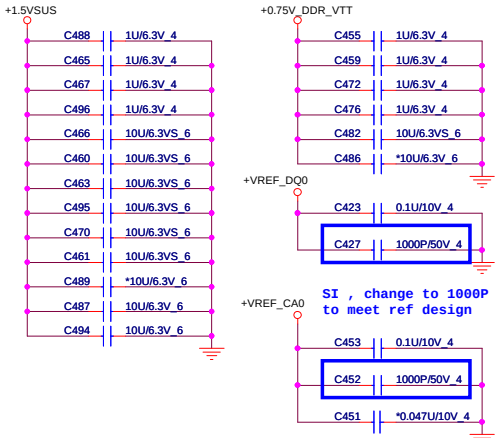


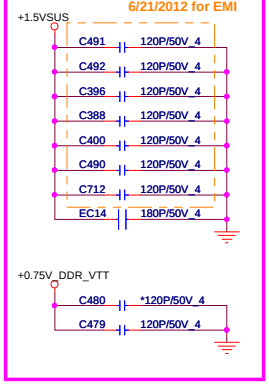


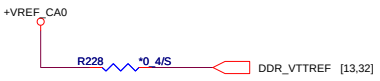
Place these Caps near So-Dimm0.



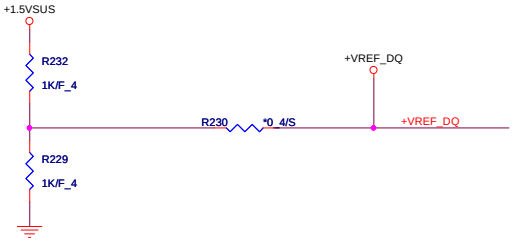
For EMI RESERVE

6/21/2012 for EMI





Reserved for AMD suggest



NB5

PROJECT : U56
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Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	1A

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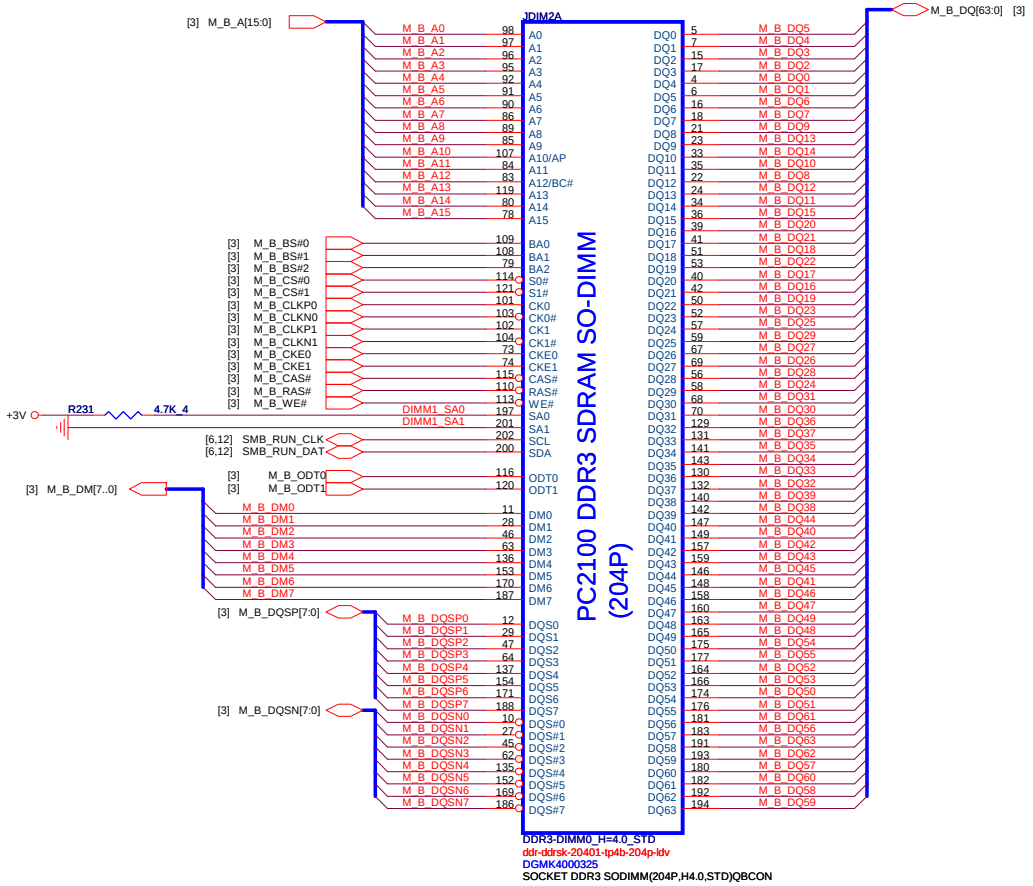
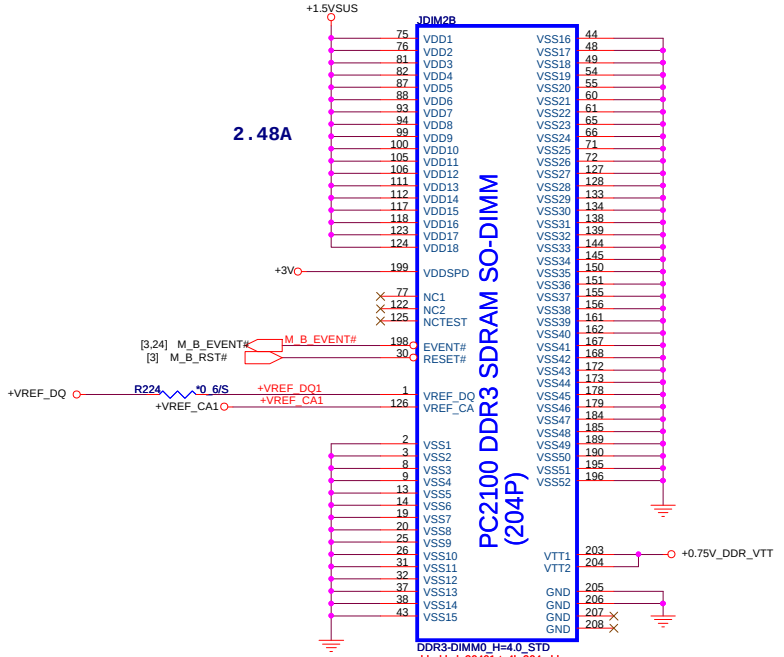
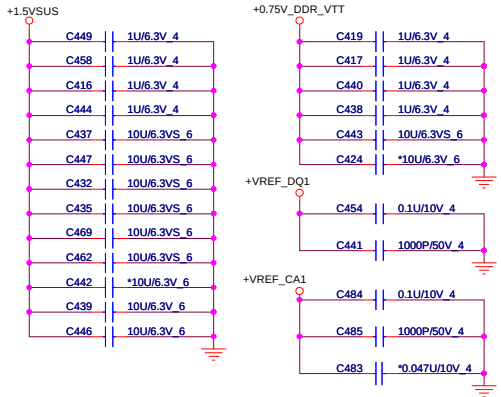
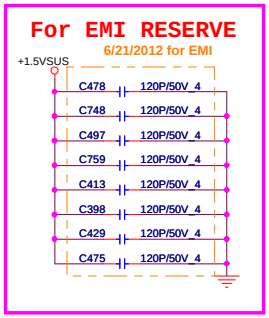


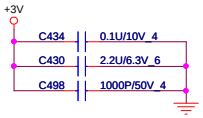


[2,4,6,8,9,10,11,12,14,20,21,22,23,24,25,26,27,33,34,35,38] +3V
[2,3,4,5,12,32,34,38] +1.5VSUS
[12,32] +0.75V_DDR_VTT

Place these Caps near So-Dimm1.







NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A

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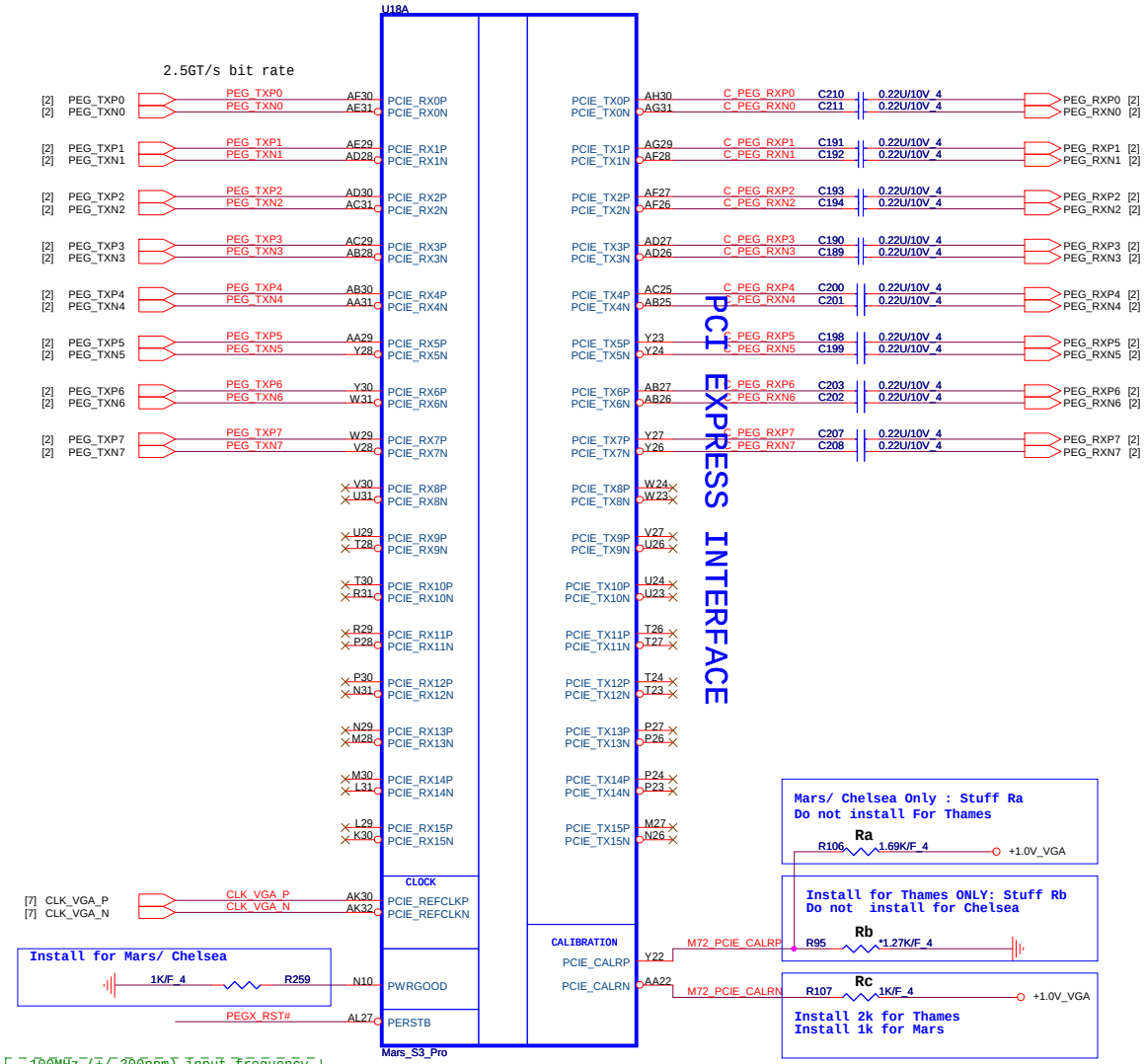
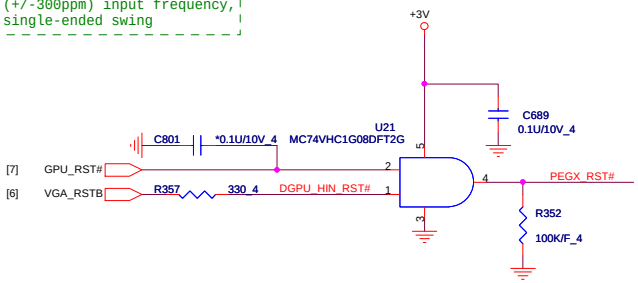
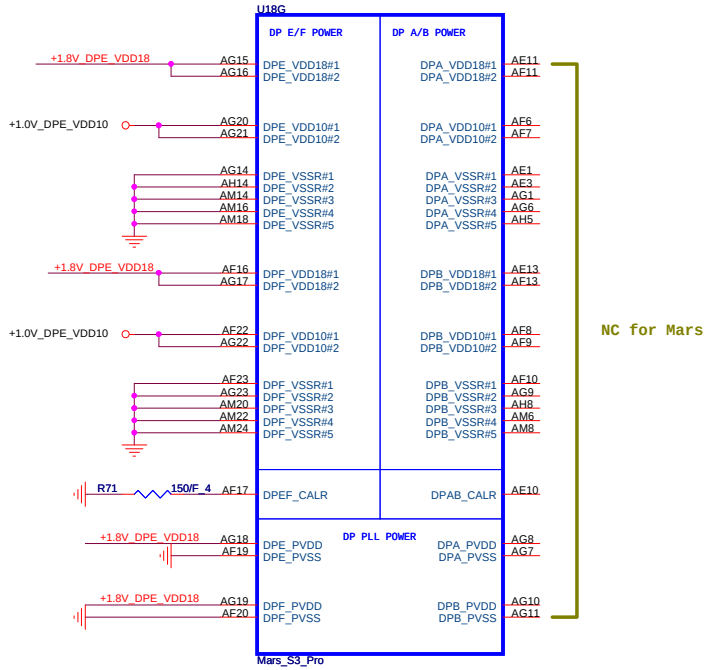
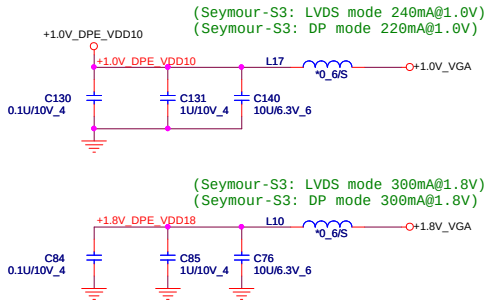


	Chelsea/MARS	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K







+1.0V_VGA [15,17,34]
+1.8V_VGA [15,17,35]

NB5

PROJECT : U56
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Size	Document Number	Rev
Custom	Mars S3 PCIE_Interface	1A

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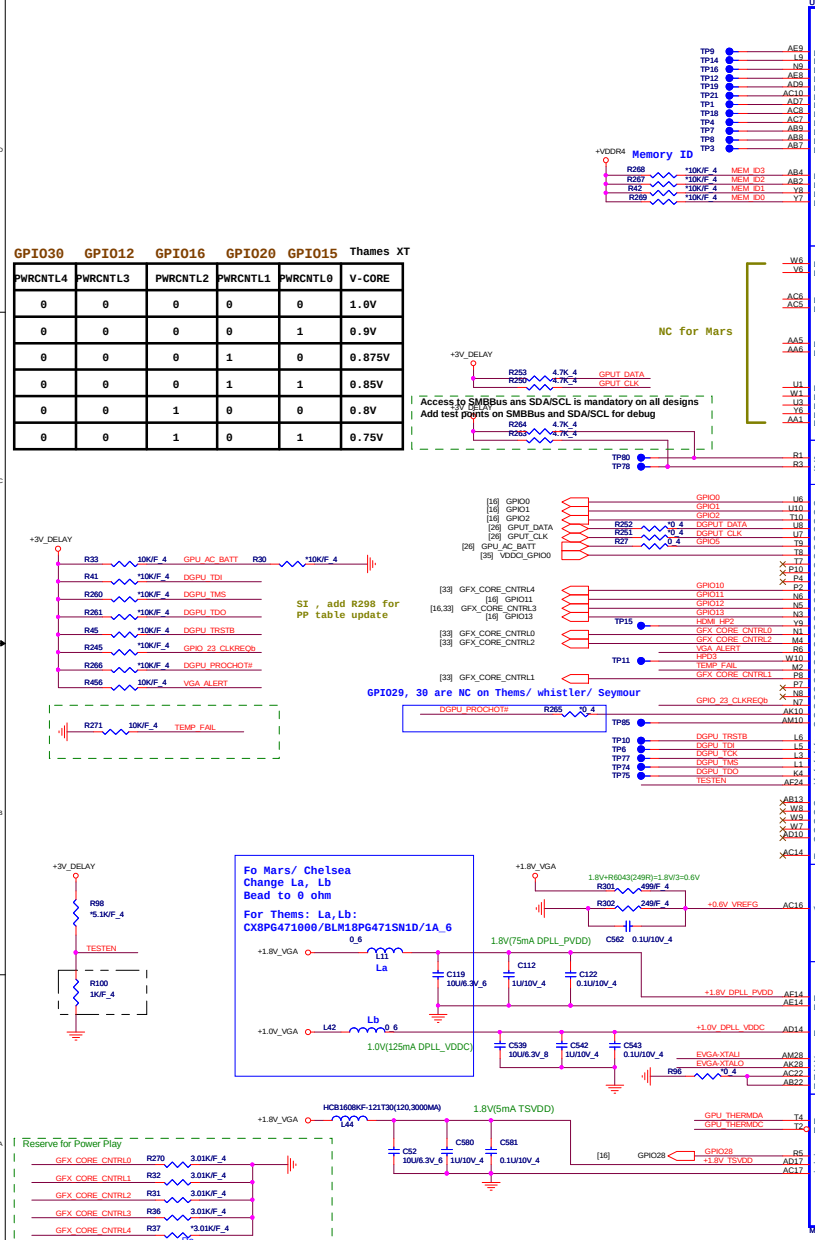
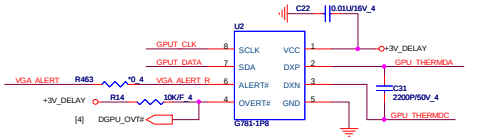
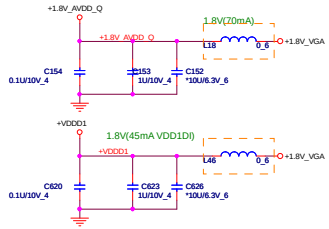
GPIO30	GPIO12	GPIO16	GPIO20	GPIO15	Thames XT
PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
0	0	0	0	0	1.0V
0	0	0	0	1	0.9V
0	0	0	1	0	0.875V
0	0	0	1	1	0.85V
0	0	1	0	0	0.8V
0	0	1	0	1	0.75V



Thermal Solution(Close to GPU)

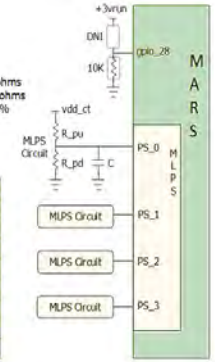


Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

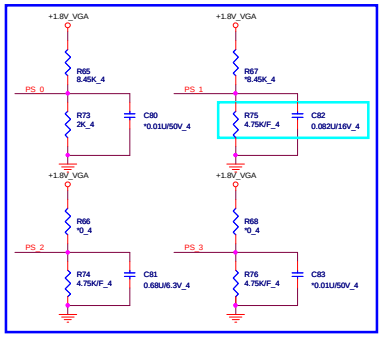
R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

PS_3[3:1]	Vendor	Type	Vendor P/N	R68	R76
000	Hynix- D (VEGA)	128Mx16 *4, 900Mhz	H5TQ1G63DFR-11C	NC	4.75K
001	Micron- G die	128Mx16 *4, 900Mhz	MT41J64M16JT-107G:G	8.45K	2K
010	Samsung- G die	128Mx16 *4, 900Mhz	K4W1G1646G-BC11	4.53K	2K

BIT5 => BIT0

PS0	=>	11001
PS1	=>	01000
PS2	=>	00000
PS3	=>	11000



+1.8V_VGA [14,17,35]
+1.0V_VGA [14,17,34]

PROJECT : U56
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Mars S3 Main	1A

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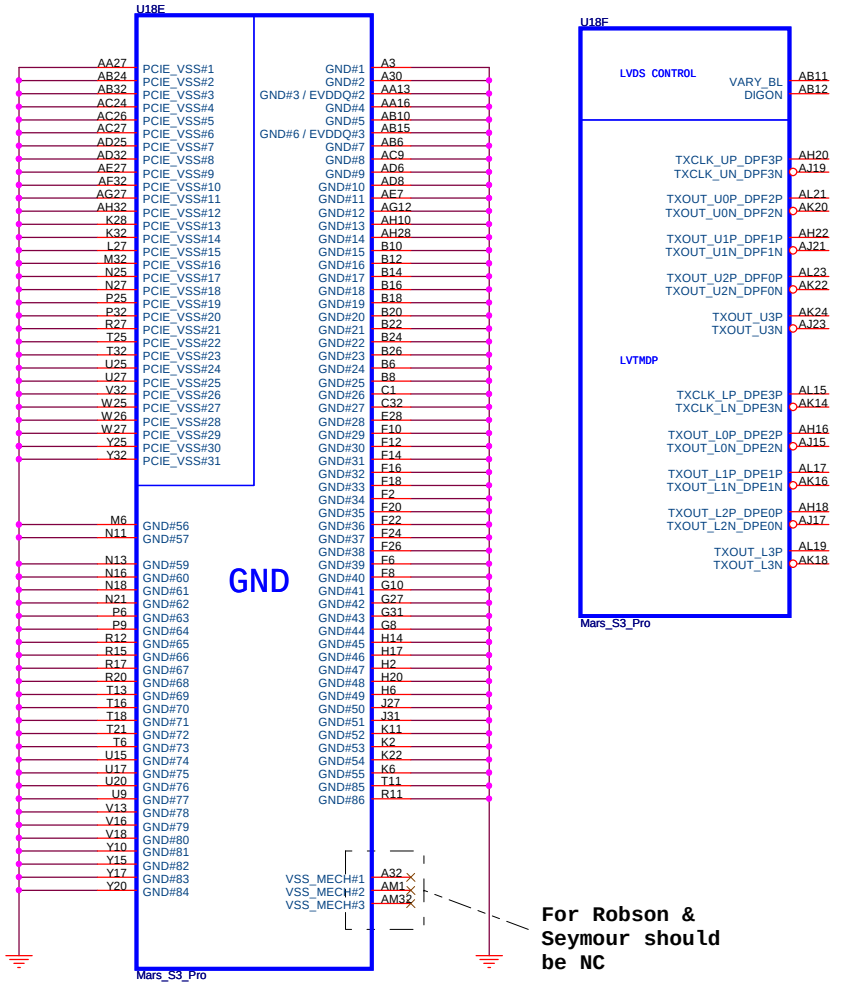


For Robson & Seymour should be NC

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

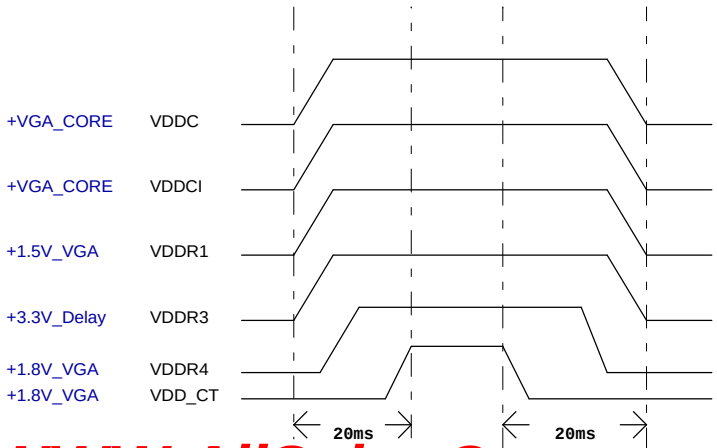
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

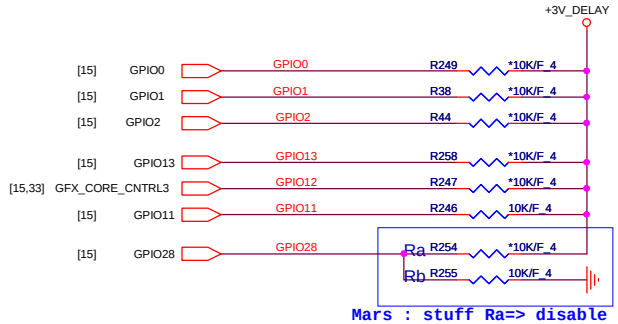
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



Mars : stuff Ra=> disable MLPS
stuff Rb=> enable MLPS

+3V_DELAY [15,17]

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars S3 GND / LVDS/ Straps	1A

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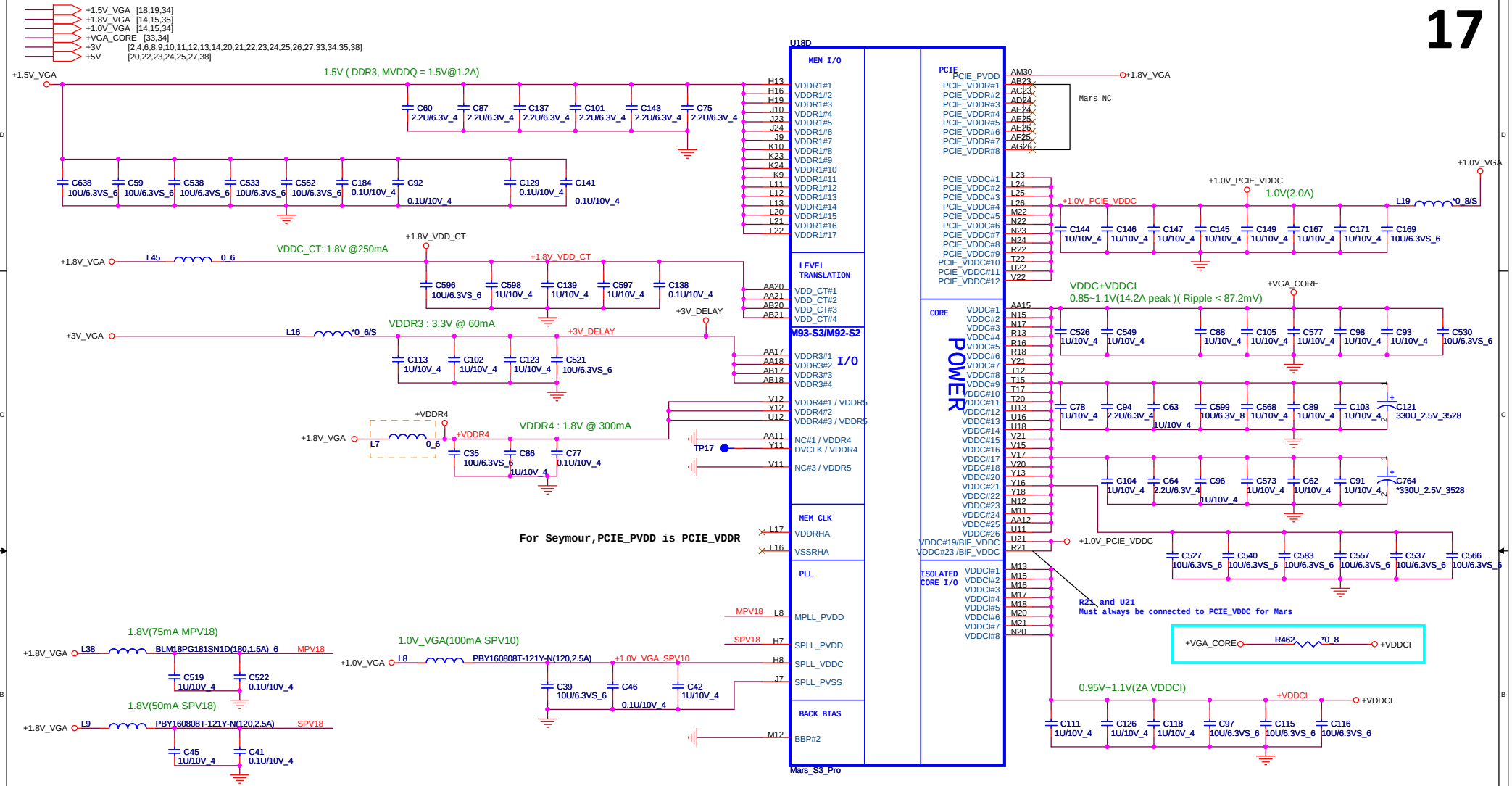

PROJECT : U56
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Mars S3 Power_and_NC	1A

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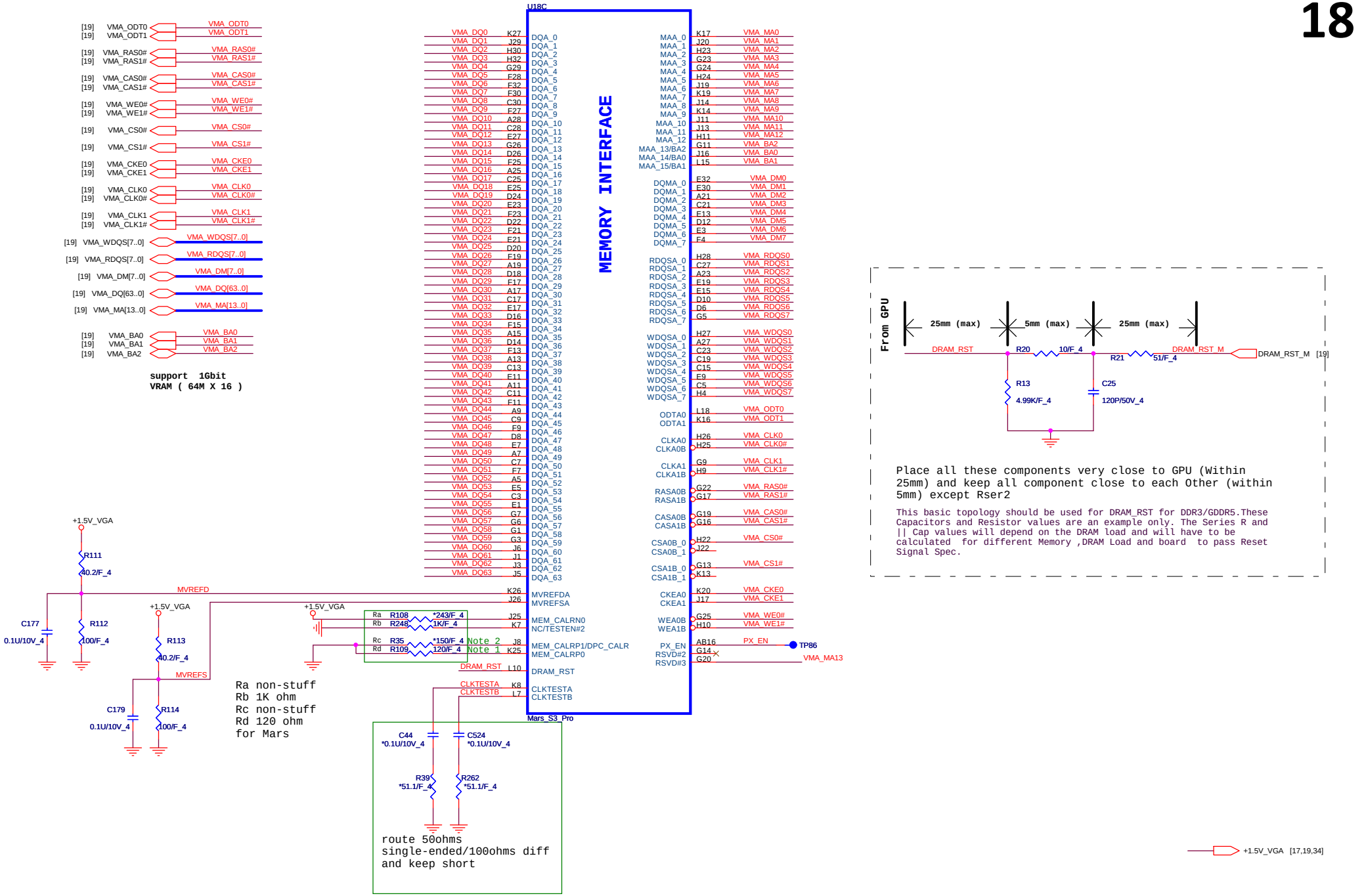

NB5	**PROJECT : U56** Quanta Computer Inc.
Size Custom	Document Number **Mars S3 MEM_Interface**
Rev 1A	
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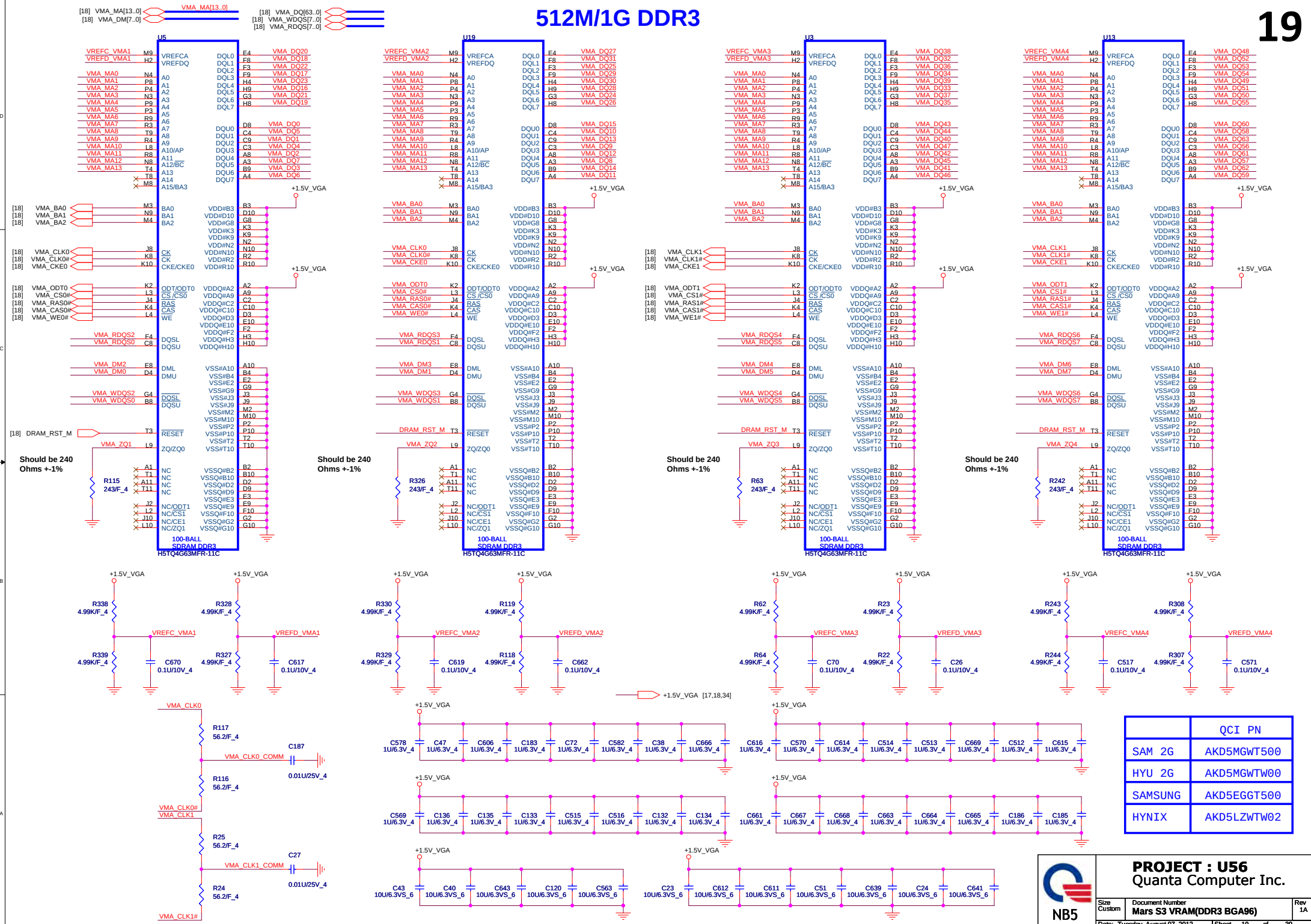
512M/1G DDR3



	QCI PN
SAM 2G	AKD5MGWT500
HYU 2G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZWTW02

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mars S3 VRAM(DDR3 BGA96)	1A

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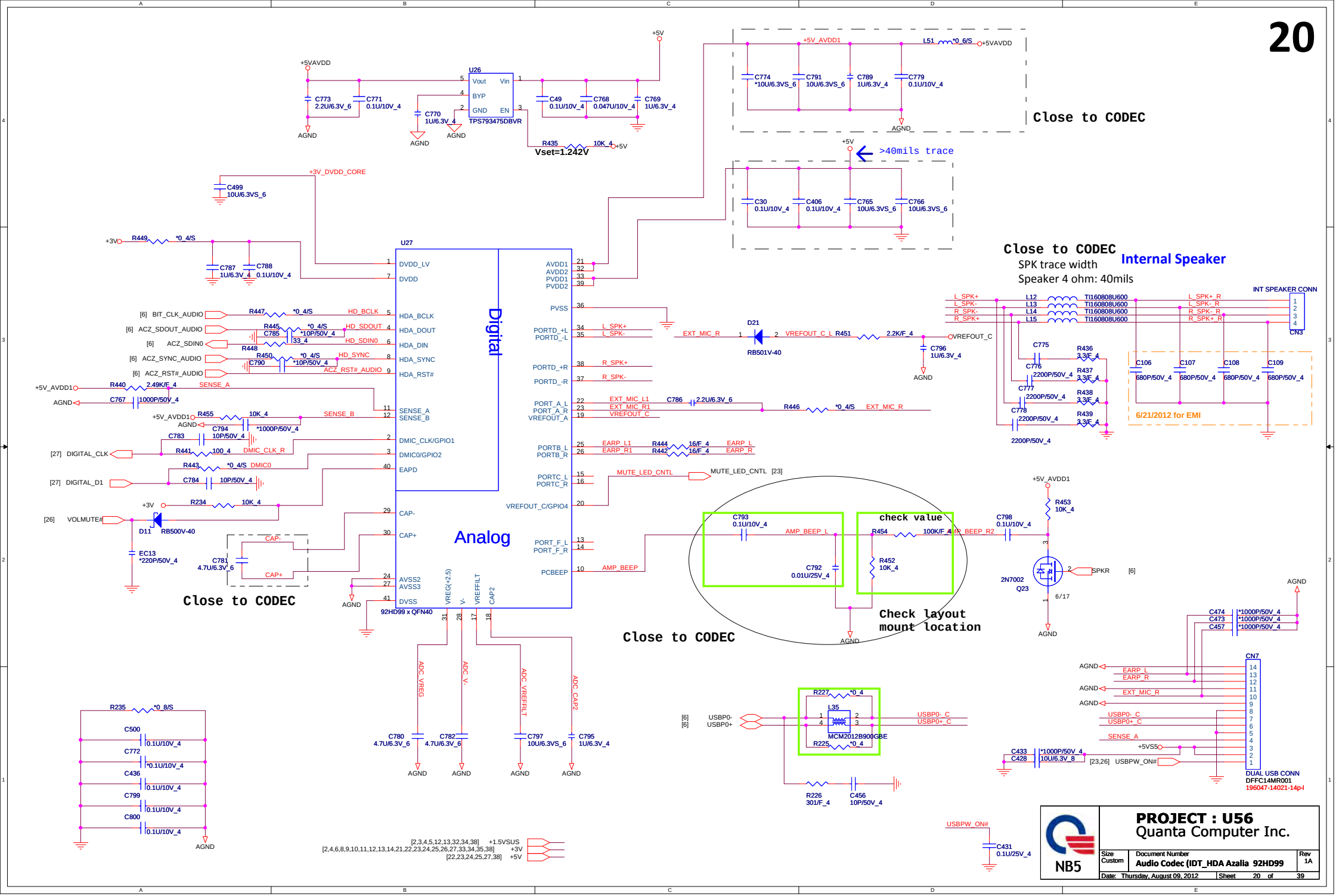

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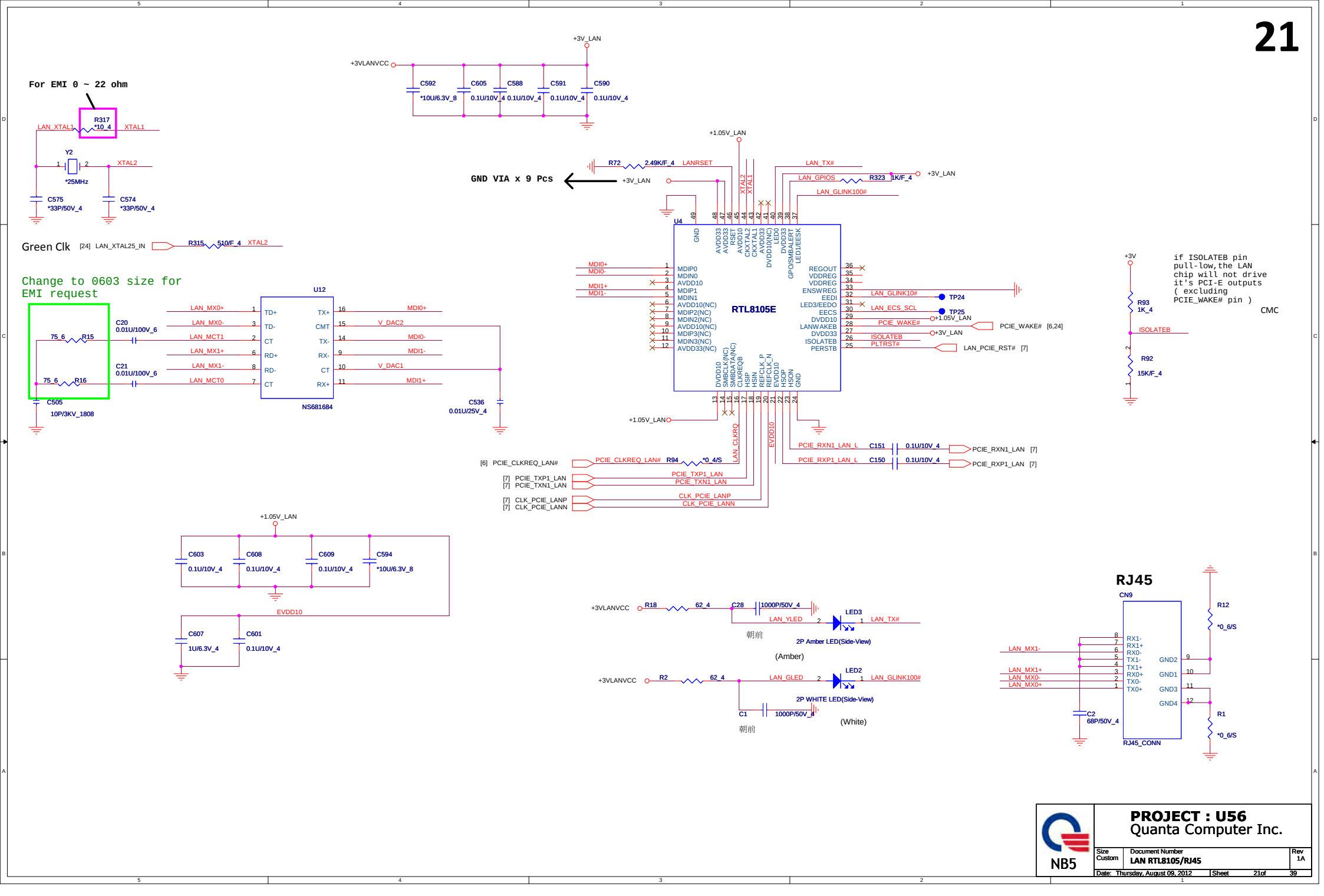
For EMI 0 ~ 22 ohm
R317 *10_4
LAN_XTAL1
XTAL1
Y2
*25MHz
XTAL2
C575 *33P/50V_4
C574 *33P/50V_4
Green Clk
[24] LAN_XTAL25_IN
R315 510/F_4
Change to 0603 size for EMI request
75_6 R15
75_6 R16
C20 0.01U/100V_6
C21 0.01U/100V_6
C505 10P/3KV_1808
U12
NS681684
LAN_MX0+
LAN_MX0-
LAN_MCT1
LAN_MX1+
LAN_MX1-
LAN_MCT0
MDI0+
V_DAC2
MDI0-
MDI1-
V_DAC1
MDI1+
C536 0.01U/25V_4
+3V_LAN
+3VLANVCC
C592 *10U/6.3V_8
C605 0.1U/10V_4
C588 0.1U/10V_4
C591 0.1U/10V_4
C590 0.1U/10V_4
+1.05V_LAN
R72 2.49K/F_4
LANRSET
GND VIA x 9 Pcs
LAN_TX#
LAN_GPIOS
R323 1K/F_4
LAN_GLINK100#
U4
RTL8105E
MDI0+
MDI0-
MDI1+
MDI1-
LAN_GLINK10#
TP24
LAN_ECS_SCL
TP25
PCIE_WAKE#
PCIE_WAKE# [6,24]
ISOLATEB
PLTRST#
LAN_PCIE_RST# [7]
PCIE_RXN1_LAN_L
C151 0.1U/10V_4
PCIE_RXN1_LAN [7]
PCIE_RXP1_LAN_L
C150 0.1U/10V_4
PCIE_RXP1_LAN [7]
[6] PCIE_CLKREQ_LAN#
PCIE_CLKREQ_LAN# R94 *0_4/S
LAN_CLKRQ
EVDD10
[7] PCIE_TXP1_LAN
[7] PCIE_TXN1_LAN
PCIE_TXP1_LAN
PCIE_TXN1_LAN
[7] CLK_PCIE_LANP
[7] CLK_PCIE_LANN
CLK_PCIE_LANP
CLK_PCIE_LANN
+3V
R93 1K_4
ISOLATEB
R92 15K/F_4
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)
CMC
C603 0.1U/10V_4
C608 0.1U/10V_4
C609 0.1U/10V_4
C594 *10U/6.3V_8
EVDD10
C607 1U/6.3V_4
C601 0.1U/10V_4
+3VLANVCC
R18 62_4
C28 1000P/50V_4
LAN_YLED
LED3
LAN_TX#
朝前
2P Amber LED(Side-View)
(Amber)
R2 62_4
LAN_GLED
LED2
LAN_GLINK100#
2P WHITE LED(Side-View)
C1 1000P/50V_4
朝前
(White)
RJ45
CN9
RJ45_CONN
LAN_MX1-
LAN_MX1+
LAN_MX0-
LAN_MX0+
C2 68P/50V_4
R12 *0_6/S
R1 *0_6/S
NB5
PROJECT : U56
Quanta Computer Inc.
Size Custom
Document Number
LAN RTL8105/RJ45
Rev 1A
Date: Thursday, August 09, 2012
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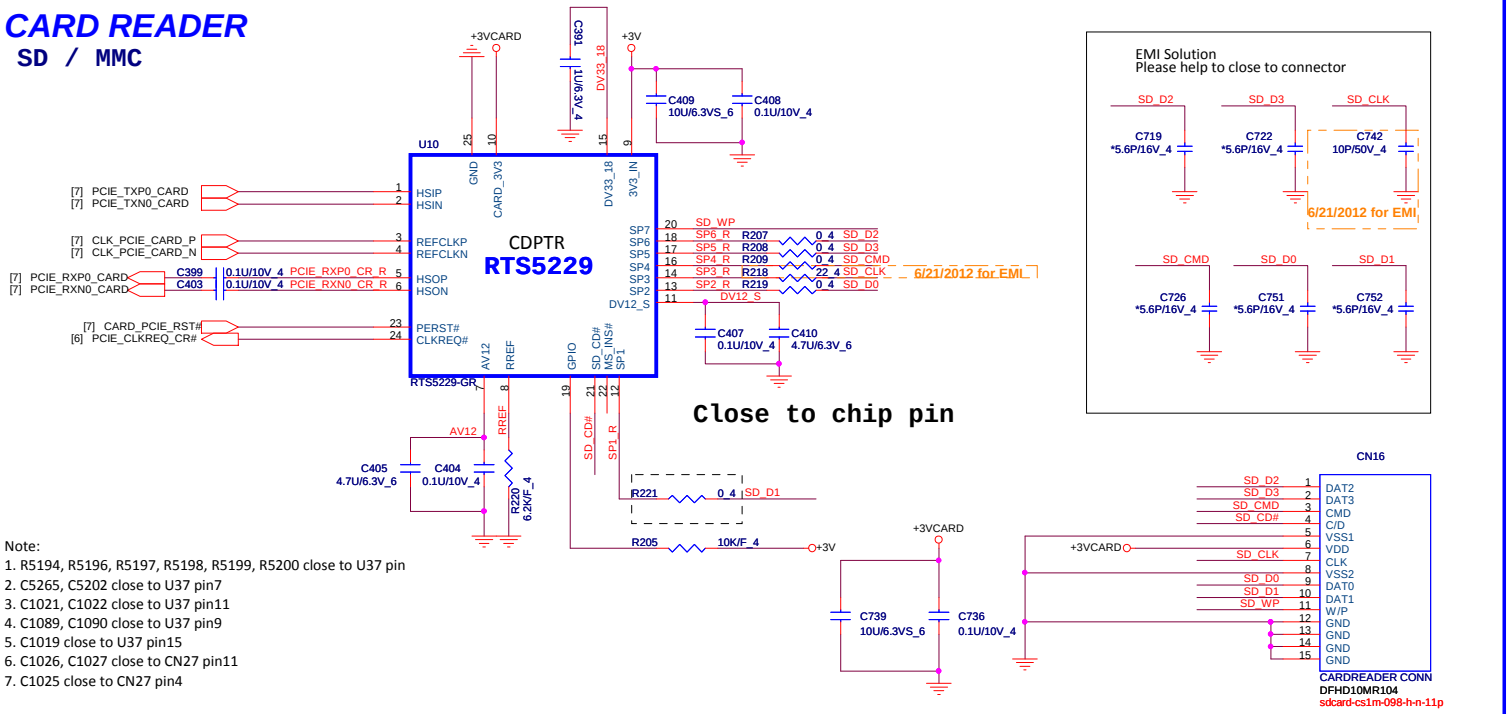
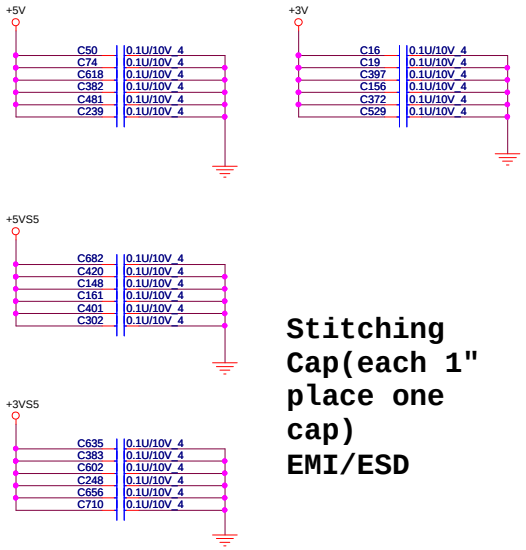
CARD READER
SD / MMC



Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4



Stitching Cap(each 1" place one cap)
EMI/ESD

CPU

H10 *H-TC280BI217D150P2
H11 *H-TC280BI217D150P2
H13 *H-TC280BI217D150P2
H14 *H-TC280BI217D150P2

VGA

H4 *H-TC280BI217D150P2
H8 *H-TC280BI217D150P2
H9 *H-TC280BI217D150P2

FCH

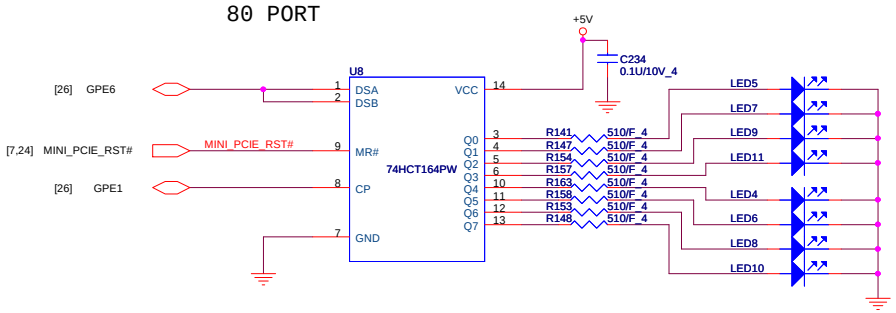
H28 H-TC217BC122D122PT
H26 H-TC217BC122D122PT

mSATA

H25 *h-tc138bc104d104pt
H24 *h-tc138bc104d104pt

H2 *h-tc315bc118d118p2
H5 *H-C315D118P2
H6 *H-TBC315I158D118P2
H1 *H-C315D106P2
H22 *H-C315D110P2
H15 *h-c315ic150d110p2
H23 *H-C315D110P2
H16 *H-C315D110P2
H12 *SPAD-C315NP
H27 *SPAD-C315NP
H3 *h-tc217bc98d98pt
H19 *H-TSBC315D110P2
H17 *h-tsbc315ic190d110p2
H7 *H-TSBC315D106P2
H18 *h-tc315bsic160d110p2
H21 *H-C158D158N
H20 *H-O142X110D142X110N

80 PORT



NB5	**PROJECT : U56** Quanta Computer Inc.	
Size Custom	Document Number **Card Reader control (RTS5229-GR)**	Rev 1A
Date: Tuesday, August 07, 2012	Sheet 22of 39	

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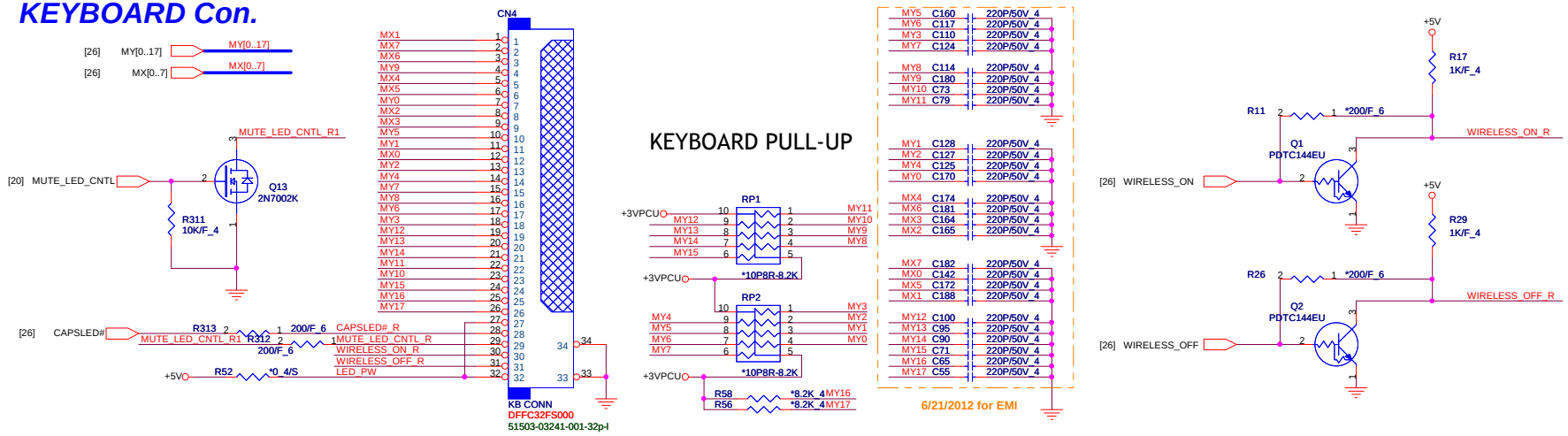
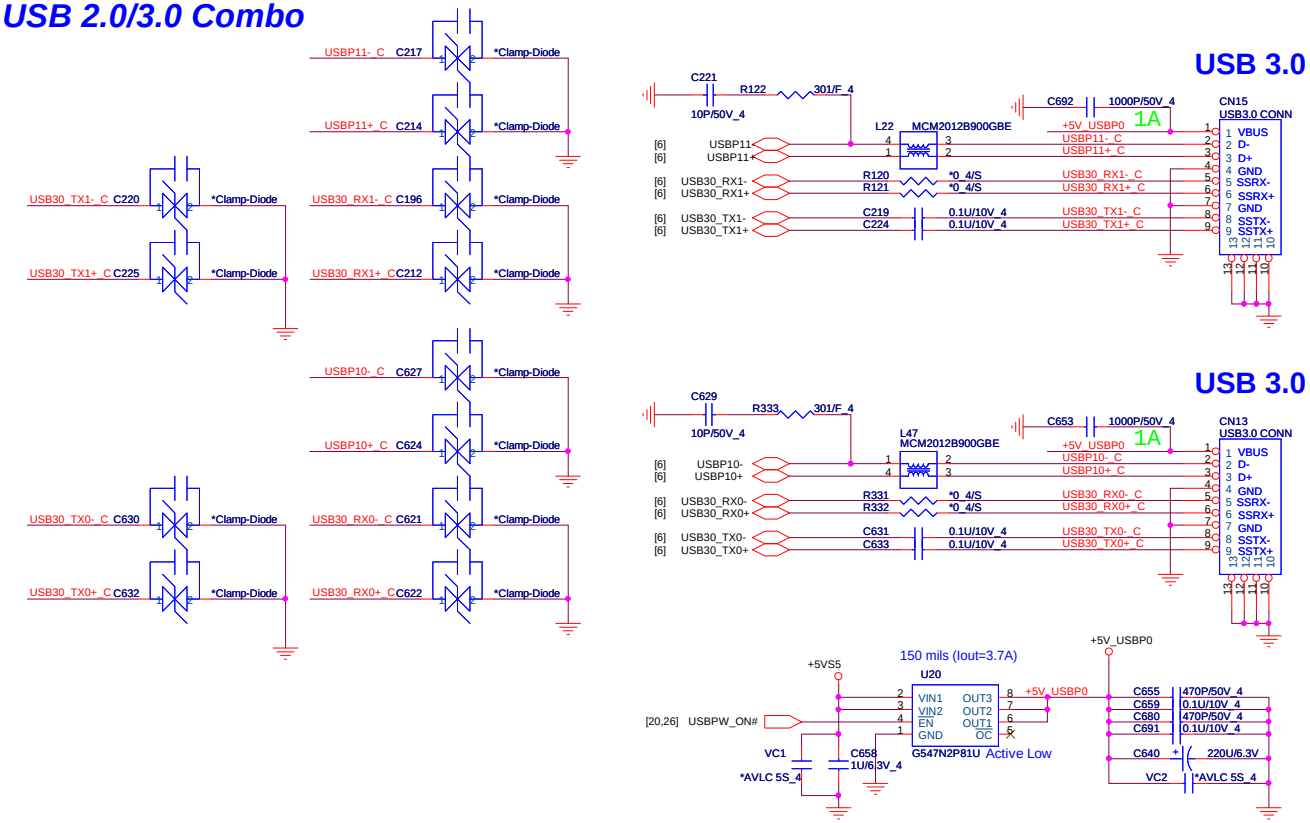
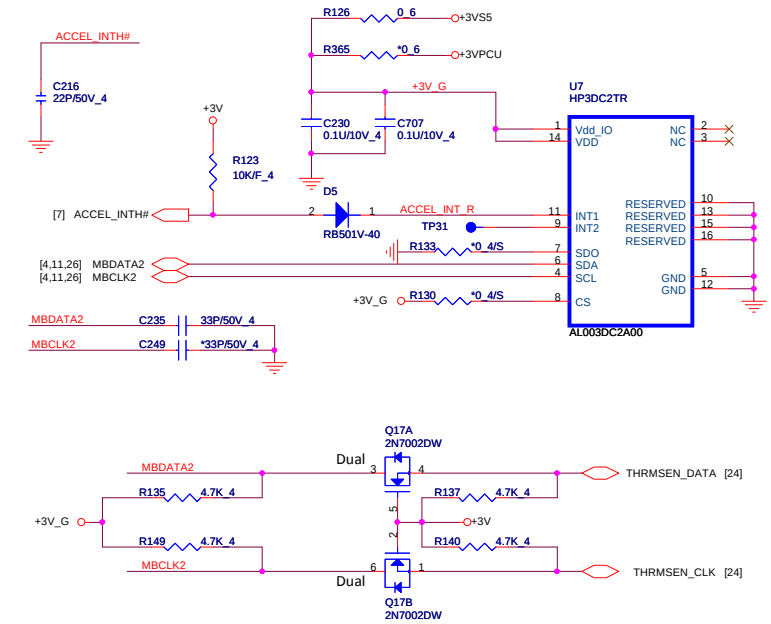
KEYBOARD Con.



USB 2.0/3.0 Combo



Accelerometer Sensor



PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1A

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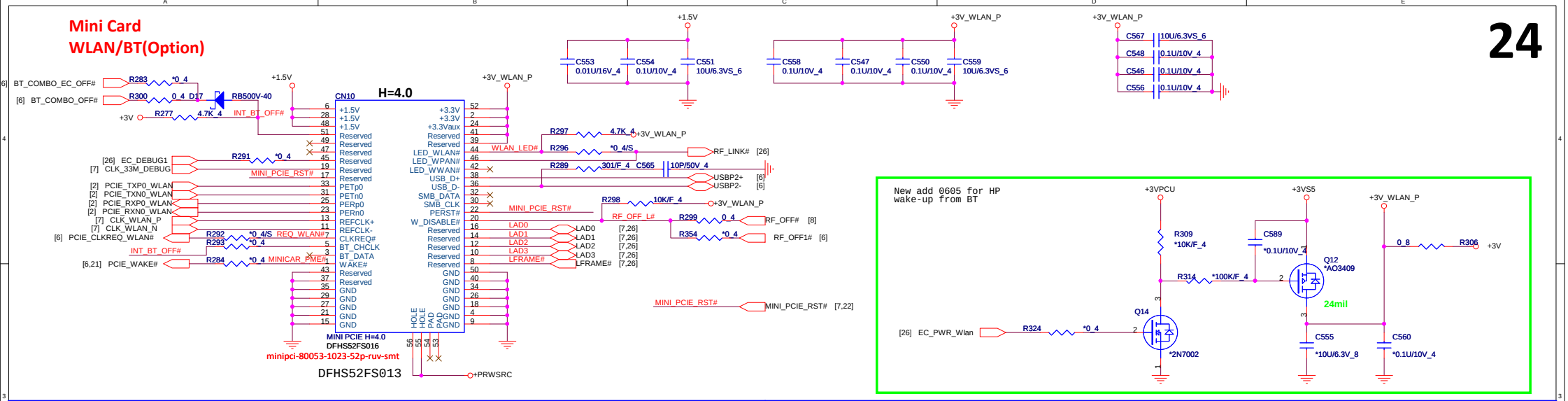
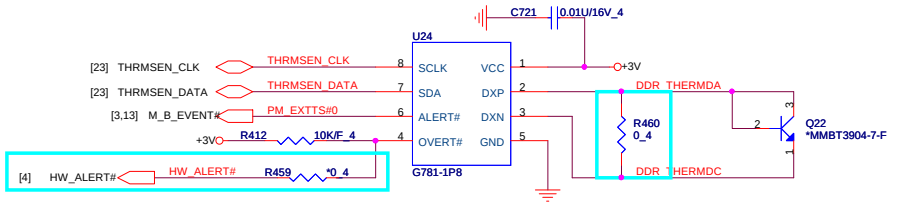
Mini Card WLAN/BT(Option)



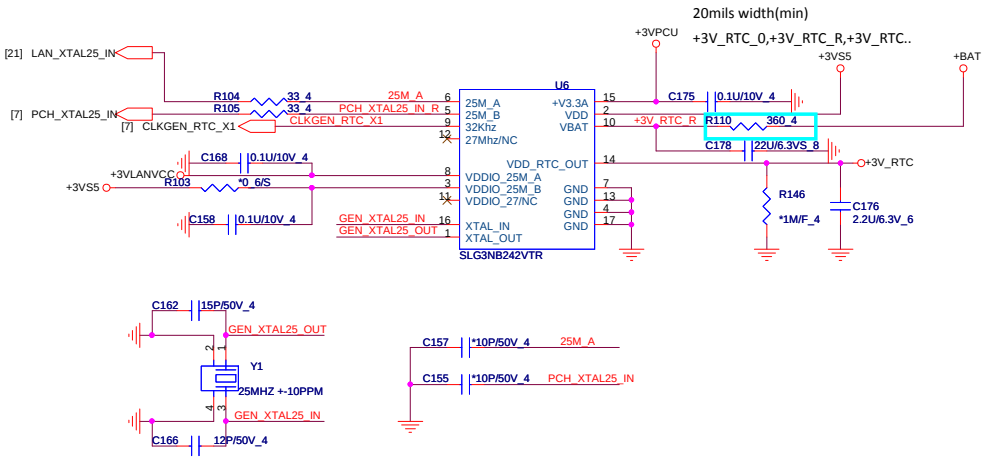
Local Thermal Sensor

DDR3 Thermal Sensor

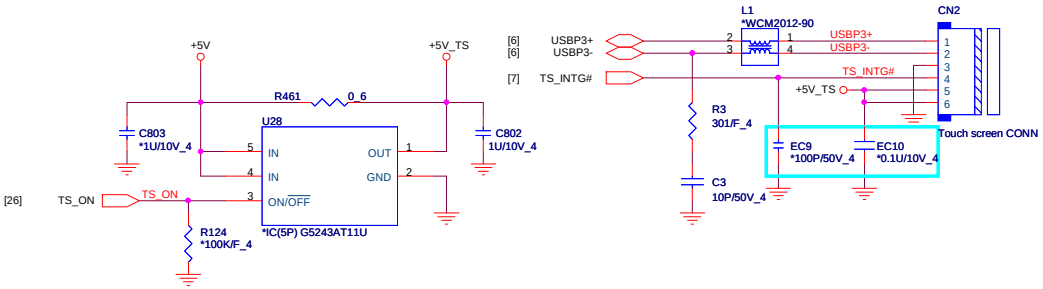


Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

Green CLK Circuitry



Touch screen



[6,8,9,10,22,23,26,29,31,33,34,38] +3VS5
[2,4,6,8,9,10,11,12,13,14,20,21,22,23,25,26,27,33,34,35,38] +3V
[20,22,23,25,27,38] +5V
[4,7,23,25,26,27,28,29] +3VPCU
[2,4,11,25,36,38] +1.5V

NB5	**PROJECT : U56** Quanta Computer Inc.		
Size Custom	Document Number MINI-PCIE/LED		Rev 1A
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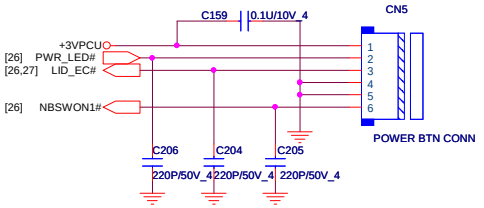
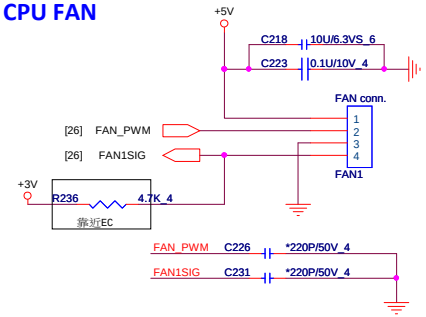
Power Botton Connector

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

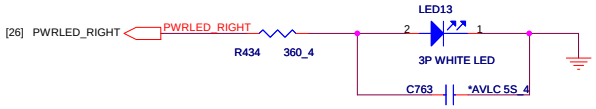


CPU FAN

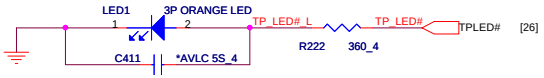


LED Status

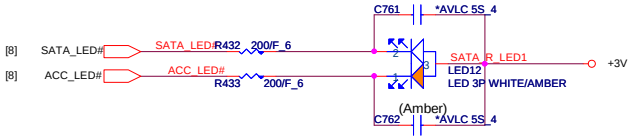
PWR LED



14 "TP LED

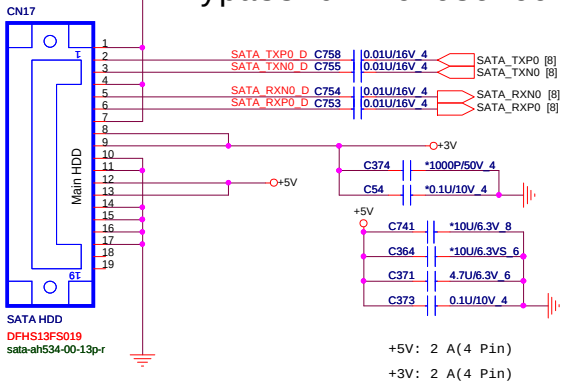


SATA LED

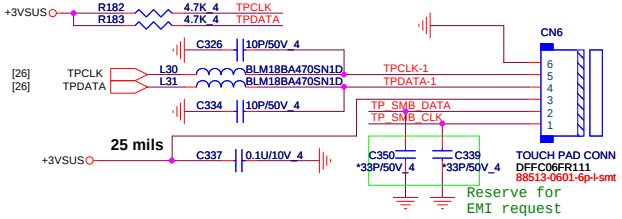


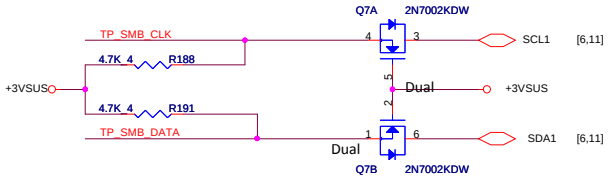
SATA HDD Connector(Cable type)

Bypass CAP close conn

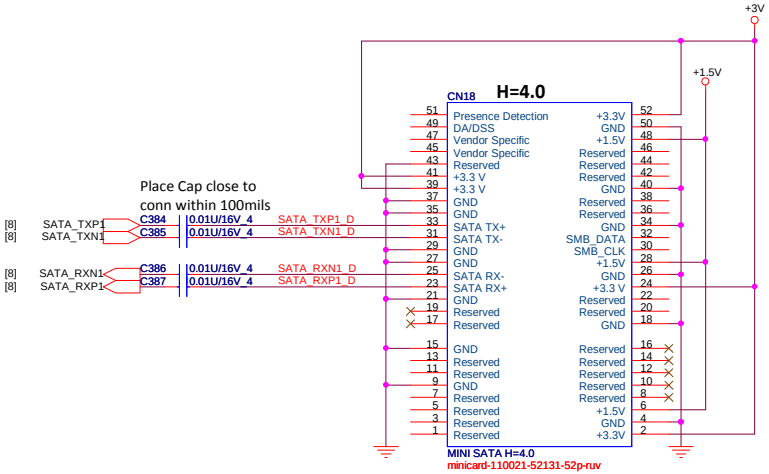


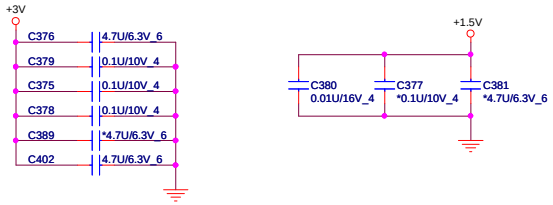
+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)



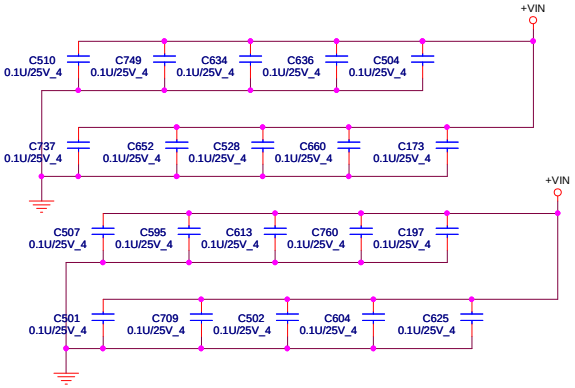


Mini PCI-E Card 2- Full size mSATA





+VIN Cap



[2,4,6,8,9,10,11,12,13,14,20,21,22,23,24,26,27,33,34,35,38] +3V
[20,22,23,24,27,38] +5V
[4,7,23,24,26,27,28,29] +3VPCU
[2,4,11,24,36,38] +1.5V
[28,34,38] +12VALW

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ODD/MSATA CONN	1A

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ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

CAPS LED

CAPSLED# [23]
CAPSLED#_OUT
Q8 2N7002K

+3VPCU_AC L36 FCM1608KF-121T04
+3VPCU_EC L6 FCM1608KF-121T04
500mA

Change to RB500 as Current loss

SCI1# D13 RB501V-40 SIO_EXT_SCI# [6]
DNBSWON1# D12 RB501V-40 DNBSWON# [6]
KBSMI#1 D14 RB501V-40 SIO_EXT_SMI# [6]

HWPG C511 *0.1U/10V_4
FAN1SIG C503 *0.1U/10V_4
DGPU_PR_EN C534 *0.1U/10V_4
For +VIN noise
SERIRQ C804 100P/50V_4

Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

4M SPI EC ROM

U14 A25LQ32AM-F/Q AKE39F-0800 SOIC8-8-1_27

128K byte SPI EC ROM

U15 *W25X40AVSSIG DFHS08FS023 SOIC8-6-1_27

ICT need TP2675 size test point

TP place on top lay for ICT request

PWR_LED

0424 Fix PWR_LED

Q10 MMBT3904

Adapter select

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

IT8518E/HX

AJ085180F04

For GPU thermal
for Battery charge/discharge
for CPU themal
from power button

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A

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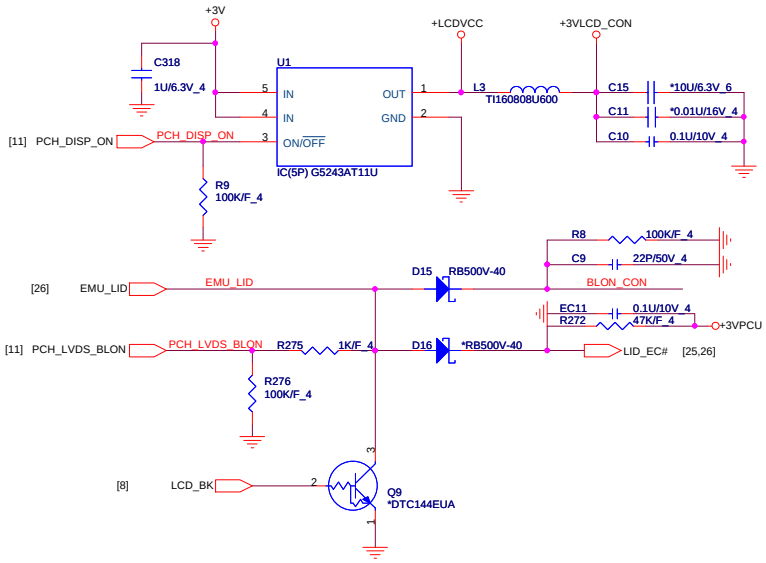
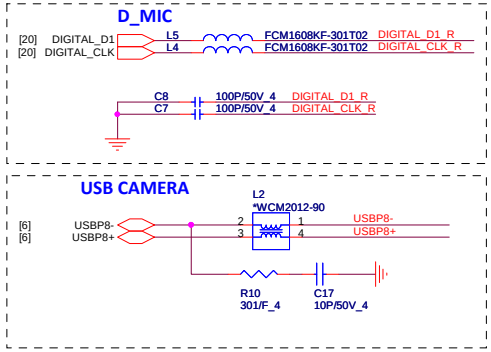
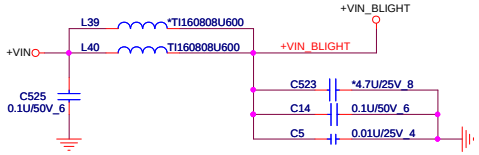
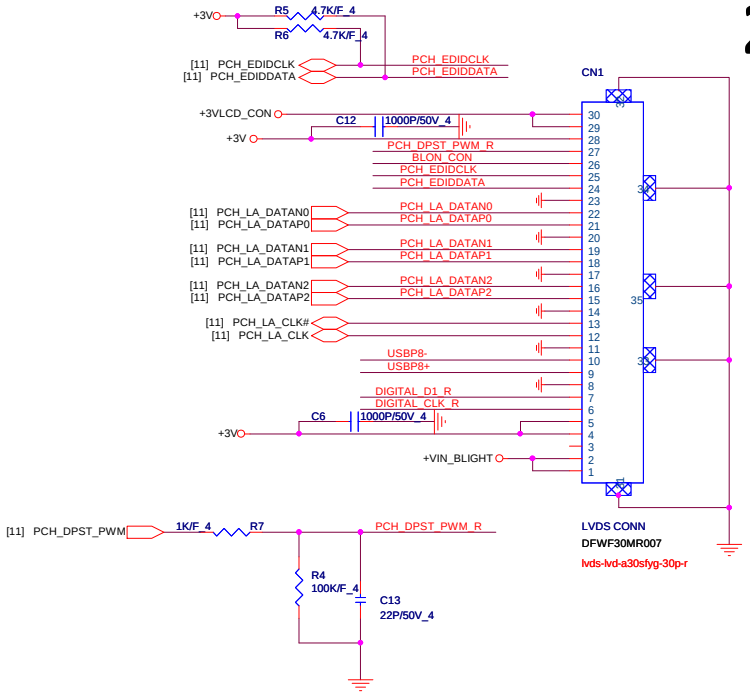
LVDS Conn.

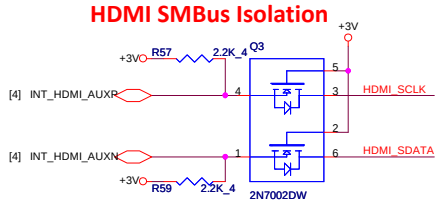


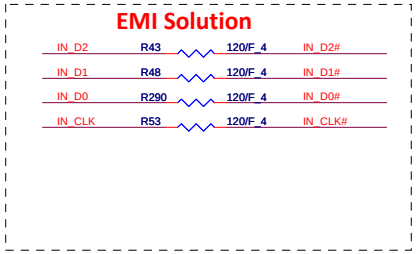


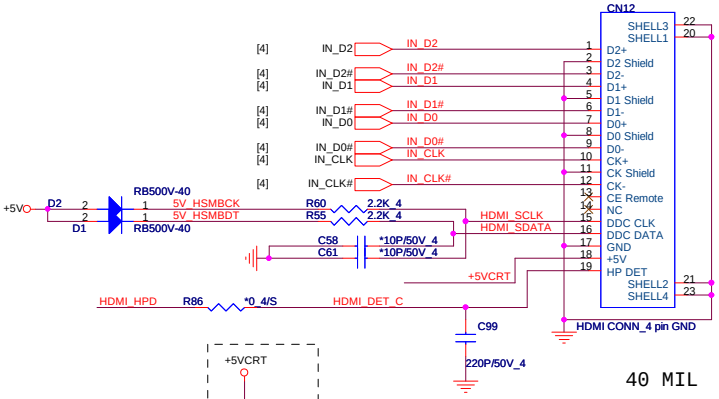


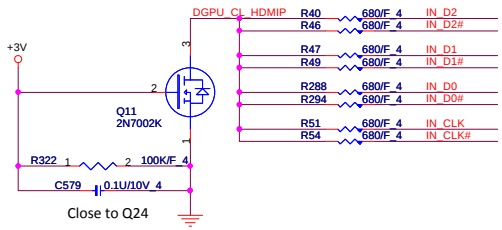


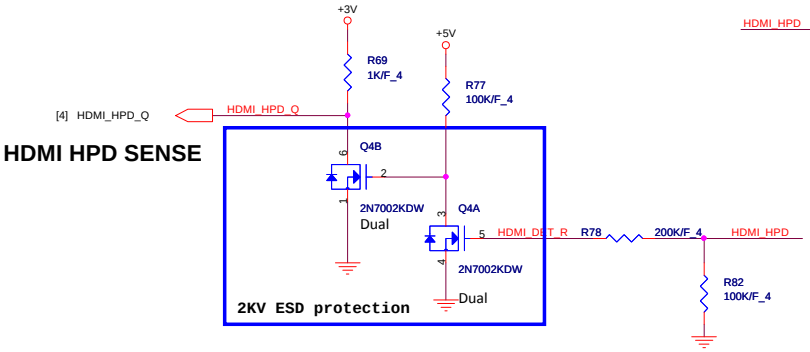
HDMI Conn.



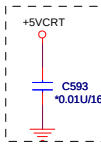




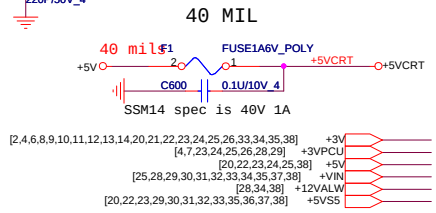




HDMI HPD SENSE



for EMI request



NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A

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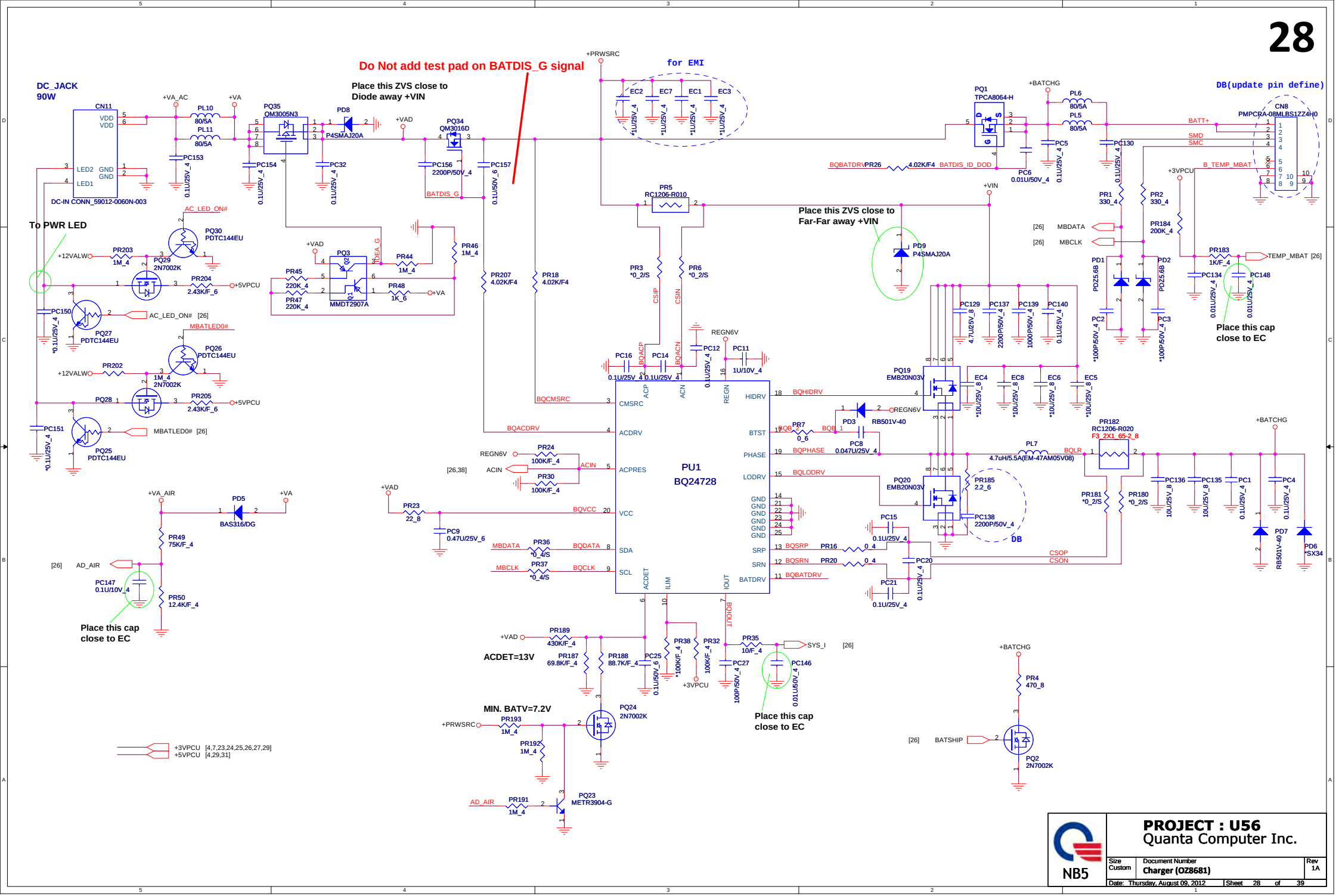

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PROJECT : U56
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Charger (OZ8681)	1A

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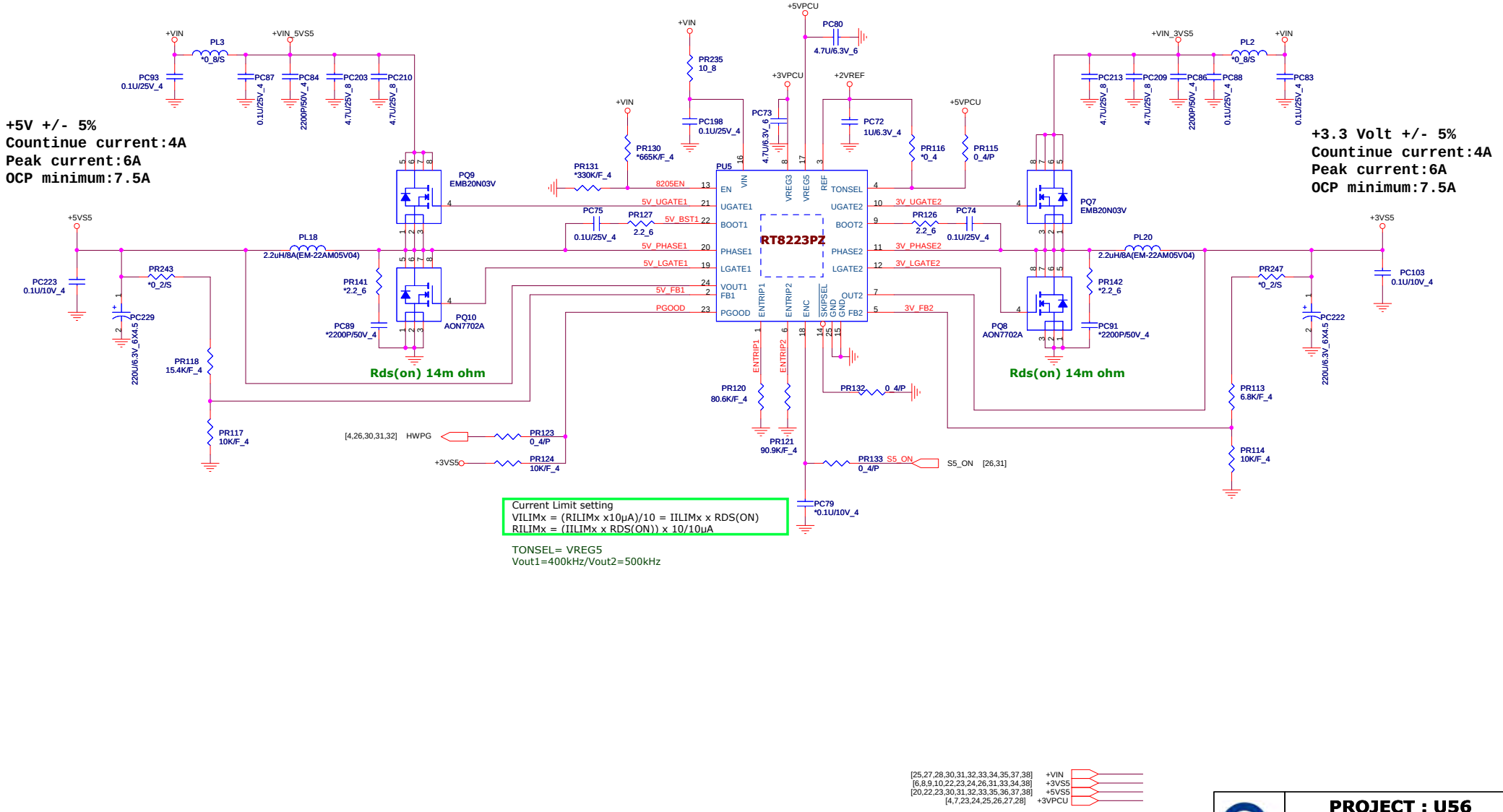
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



[25,27,28,30,31,32,33,34,35,37,38] +VIN
[6,8,9,10,22,23,24,26,31,33,34,38] +3VS5
[20,22,23,30,31,32,33,35,36,37,38] +5VS5
[4,7,23,24,25,26,27,28] +3VPCU

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (RT8223P)	1A

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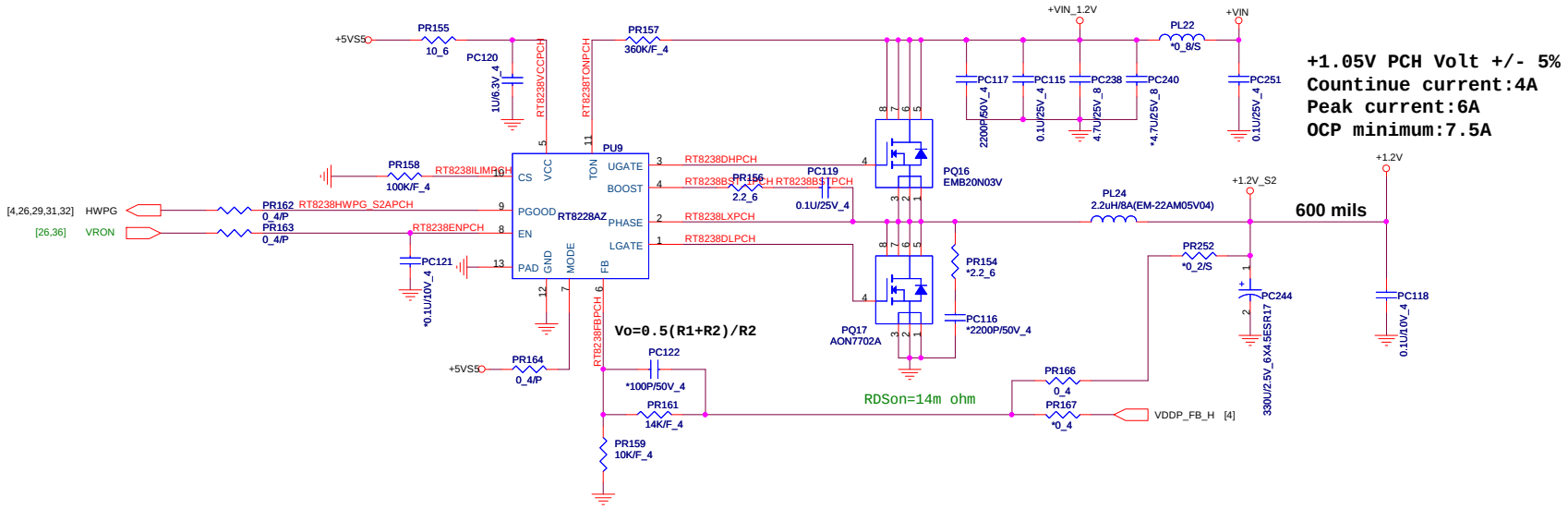

NB5	**PROJECT : U56** Quanta Computer Inc.	
Size Custom	Document Number **+1.2V (RT8228)**	Rev 1A
Date: Tuesday, August 07, 2012	Sheet 30 of 39	

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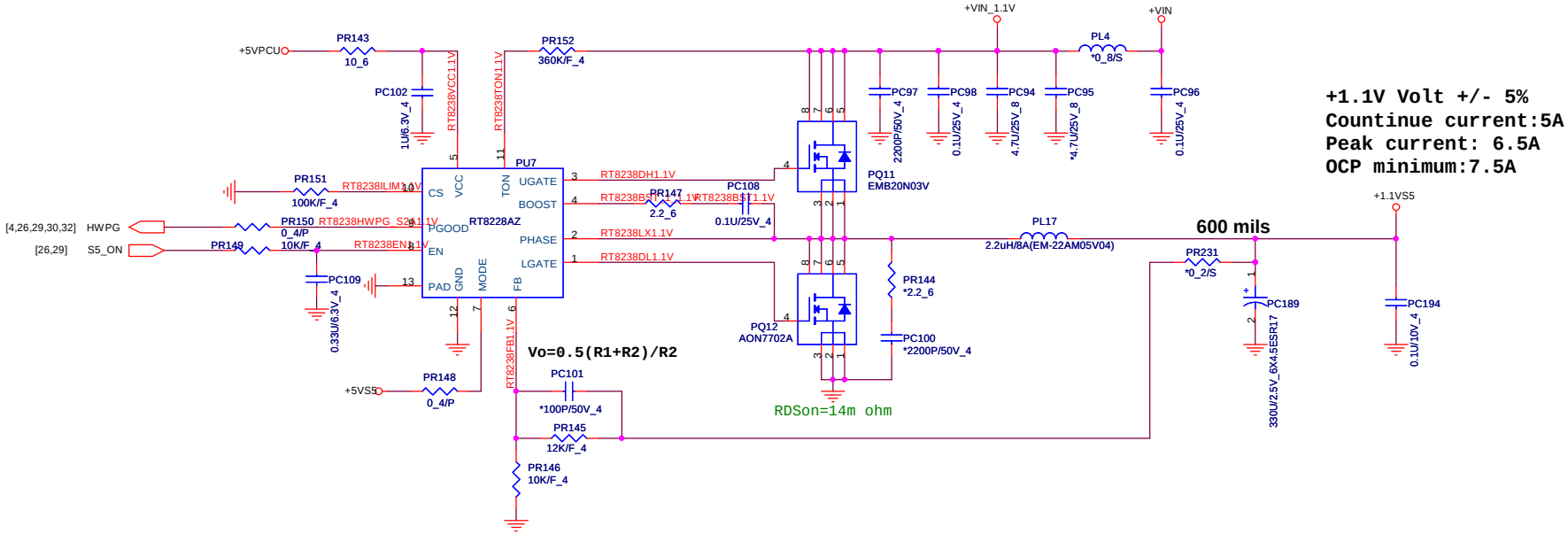

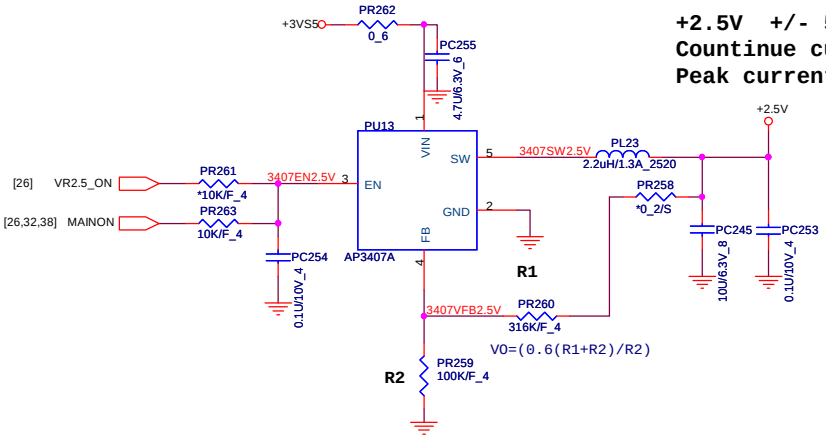

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Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A

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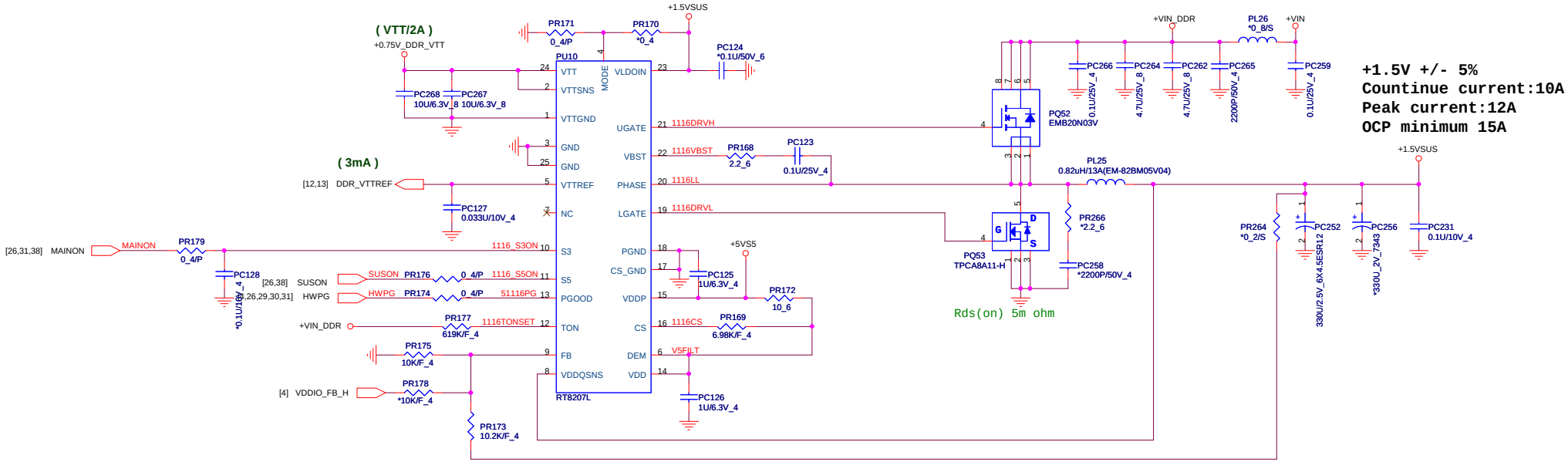

PROJECT : U56
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

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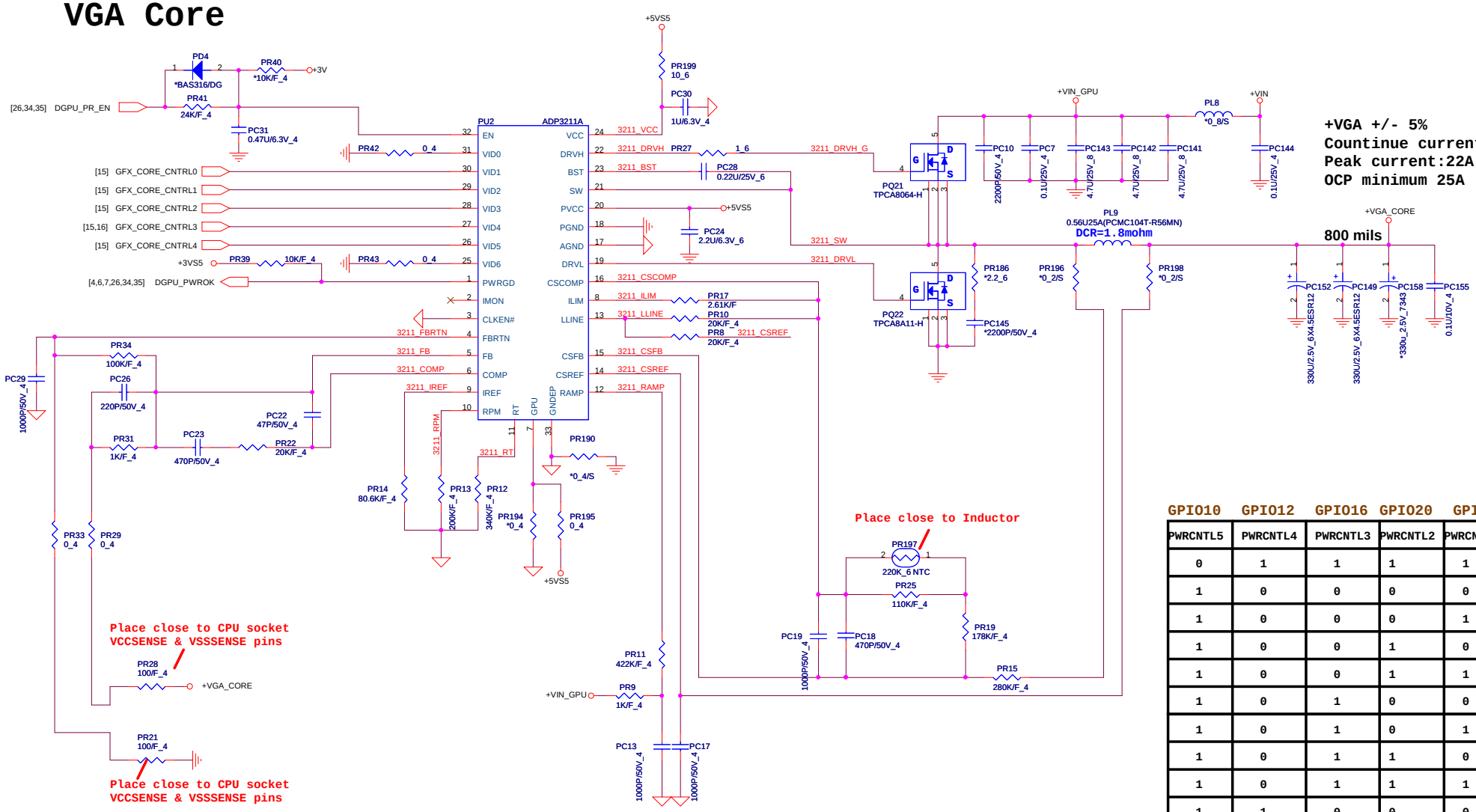
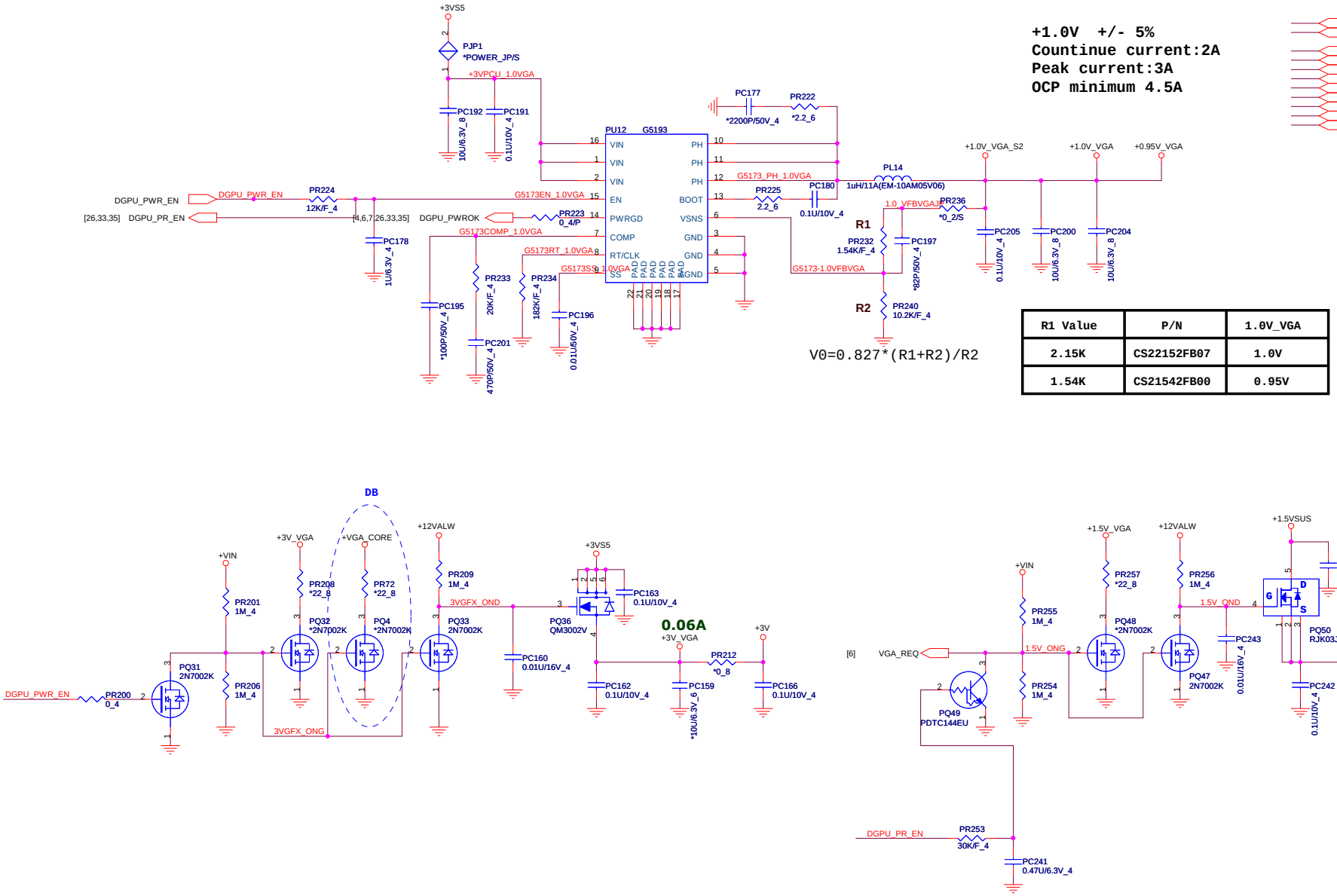
VGA Core



+VGA +/- 5%
Countinue current:18A
Peak current:22A
OCP minimum 25A

GPIO10	GPIO12	GPIO16	GPIO20	GPIO15	Mars XT	
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	Default
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	



R1 Value	P/N	1.0V_VGA
2.15K	CS22152FB07	1.0V
1.54K	CS21542FB00	0.95V

+3V	[2,4,6,8,9,10,11,12,13,14,20,21,22,23,24,25,26,27,33,35,38]
+VIN	[25,27,28,29,30,31,32,33,35,37,38]
+3VS5	[6,8,9,10,22,23,24,26,29,31,33,38]
+5VS5	[20,22,23,29,30,31,32,33,35,36,37,38]
+3V_VGA	[17]
+12VALW	[28,38]
+1.5VSUS	[2,3,4,5,12,13,32,38]
+1.5V_VGA	[17,18,19]
+1.8V_VGA	[14,15,17,35]
+3V_DELAY	[15,16,17]
+VGA_CORE	[17,33]

NB5

PROJECT : U56
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Size	Document Number	Rev
Custom	+VGA POWER	1A

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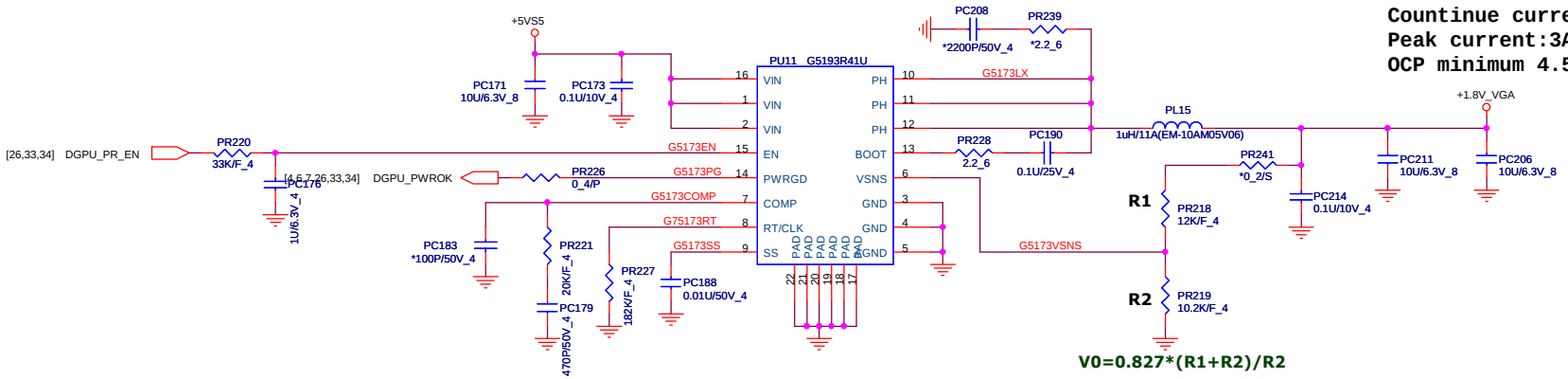
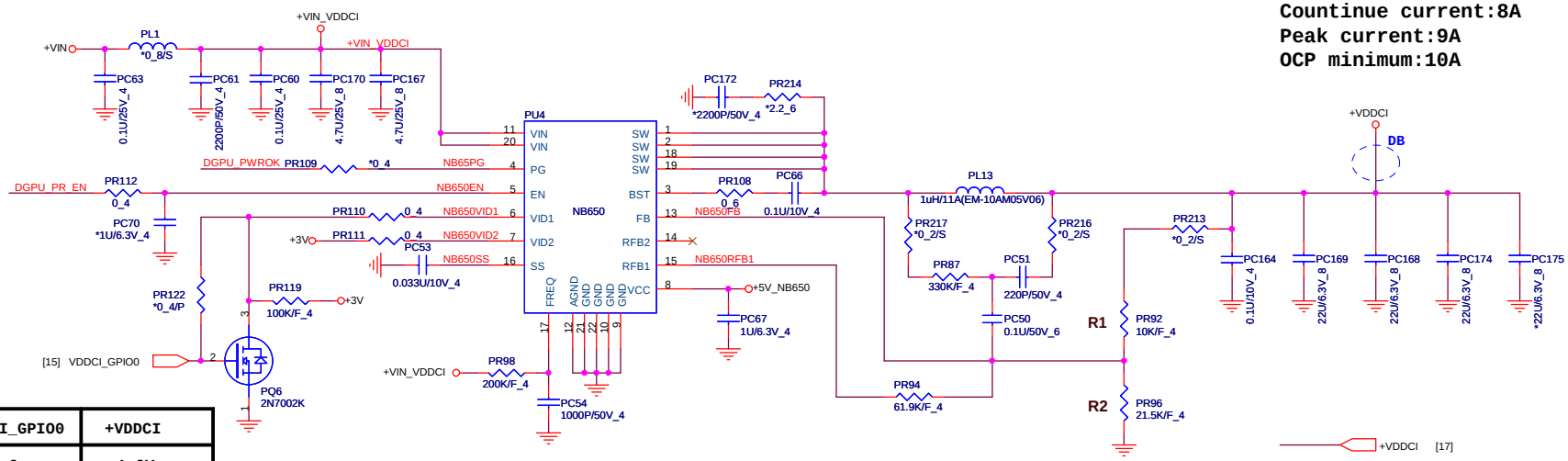
+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A



V0=0.827*(R1+R2)/R2

+VDDCI +/- 5%
Countinue current:8A
Peak current:9A
OCP minimum:10A



VDDCI_GPIO1	VDDCI_GPIO0	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X

NB5

PROJECT : U56
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V_VGA (G5193)	1A

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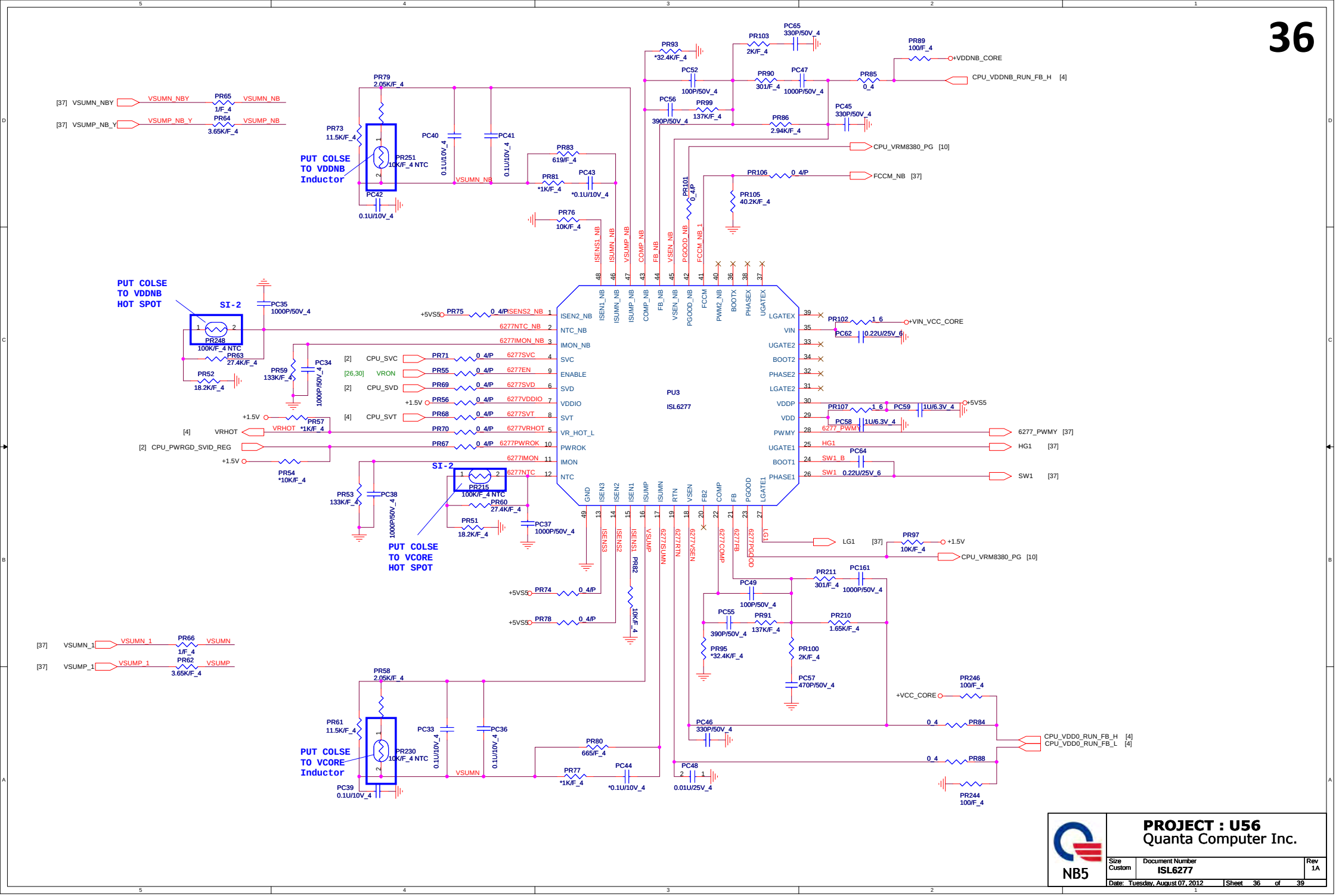

PROJECT : U56
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	ISL6277	1A

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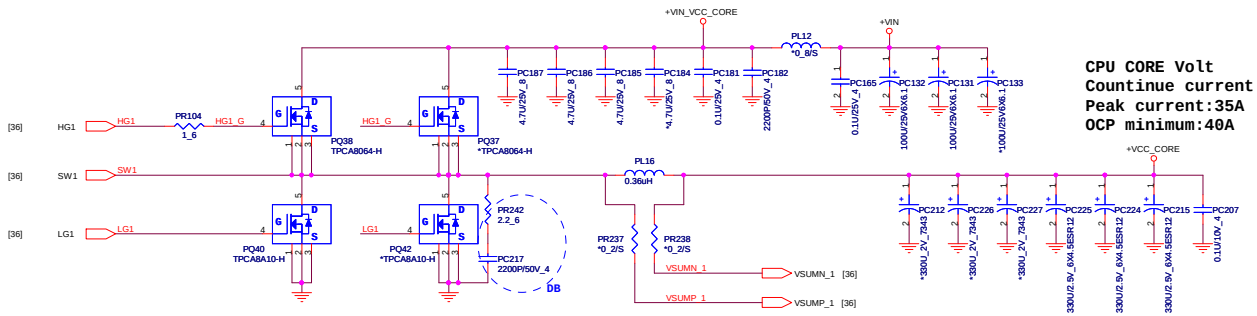
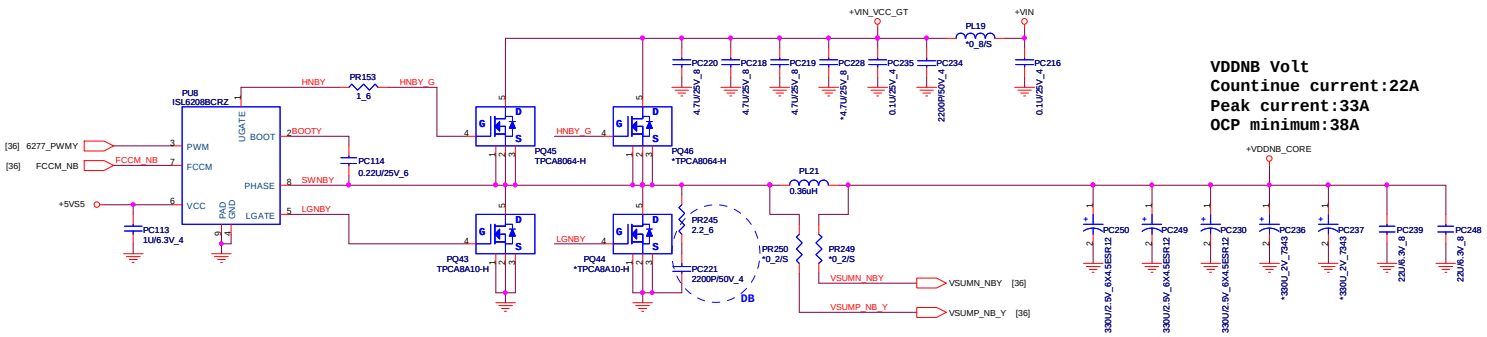


CPU CORE Volt
Countinue current:22A
Peak current:35A
OCP minimum:40A



VDDNB Volt
Countinue current:22A
Peak current:33A
OCP minimum:38A

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Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	ISL6208	1A

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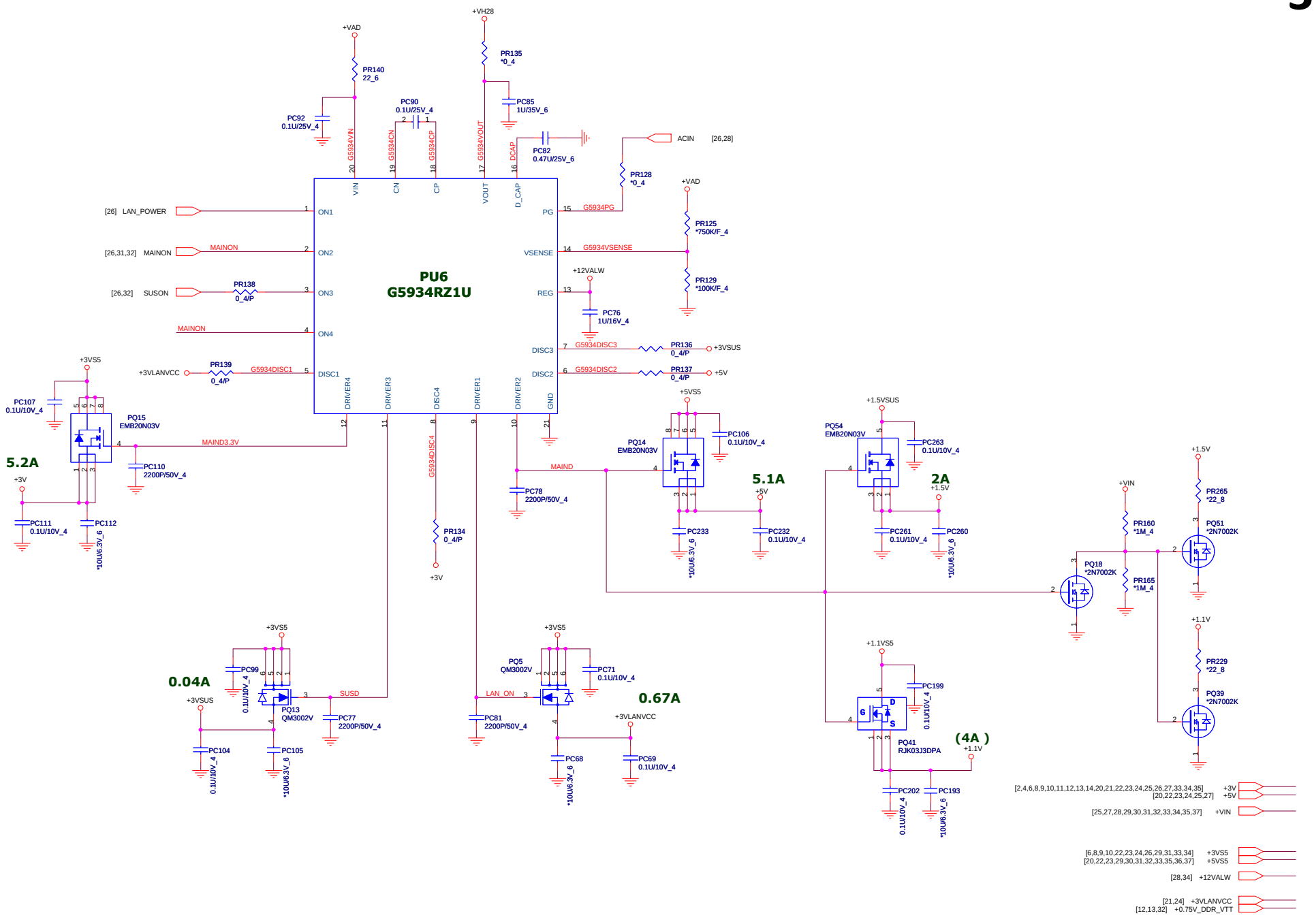

PROJECT : U56
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448V)	1A

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