

COMPAL CONFIDENTIAL

MODEL NAME : **VAZ50**

PCB NO : **LA-9431P (DAA00005Z10)**

BOM P/N : **4319LL31LXX**

GPIO MAP: 3.0C

Goliad 12"

Haswell ULT

2013-05-17

REV : 1.0 (A00)

- @ : Nopop Component
- 1@ : M/B 8M SPI ROM Component
- 2@ : TAA/B 8M SPI ROM
- EMC@ : EMI & ESD & RF Component
- XDP@ : XDP Component
- CONN@ : Connector Component
- 3@ : Delete componet for cost down BOM
- EMC_3@ : Delete EMC component for cost down BOM
- 4@ : M/B 4M SPI ROM Component
- 5@ : TAA/B 4M SPI ROM
- 7@ : M/B for 8M SPI(Reverse)

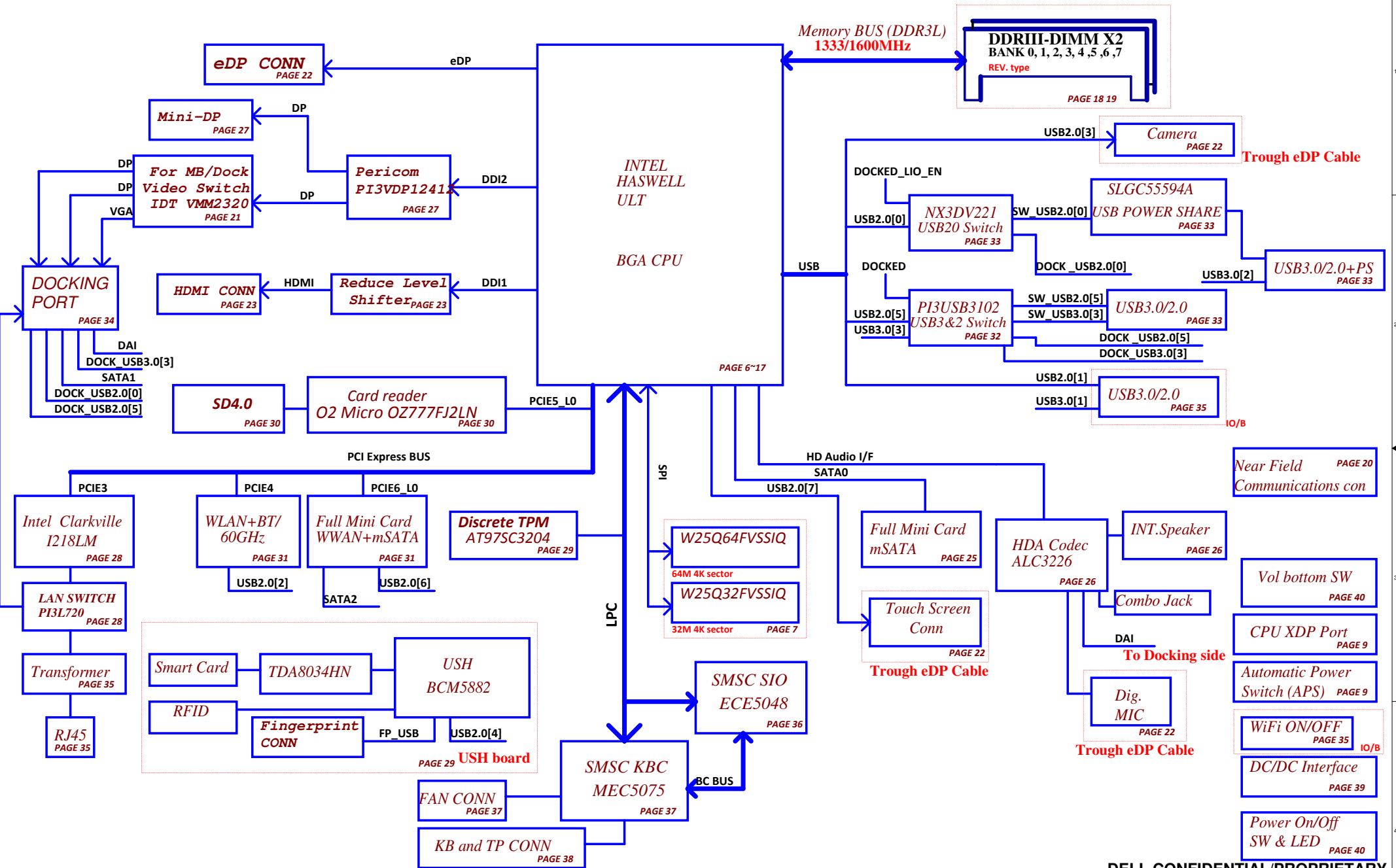
	SPI on MB	TAA
Vpro	1@/4@/EMC@/ 3@/EMC_3@	2@/5@/EMC@ 3@/EMC_3@
non-Vpro	1@/EMC@/ 3@/EMC_3@	2@/5@/EMC@ 3@/EMC_3@
non-Vpro (cost down)	1@/EMC@	2@/5@/EMC@/

MB PCB	
Part Number	Description
DAA00005Z10	PCB QVM LA-9431P REV1 M/B 4

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Block Diagram			
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Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF


need to update Power Status and PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB3-->Right
	USB3.0 2		JUSB1-->Rear left
PCIE 1	USB3.0 3		JUSB2-->Rear Right//DOCK
PCIE 2			
PCIE 3			LOM
PCIE 4			WLAN (WiGi)
PCIE 5			MMI (CARD READER)
PCIE 6		SATA 3	WWAN(PP/mSATA)
		SATA 2	NA
		SATA 1	mSATA
		SATA 0	DOCK

HSW ULT	USB PORT#	DESTINATION
	0	JUSB1 // E-Dock 1
	1	JUSB3
	2	WLAN + BT
	3	CAMERA
	4	USH->SMART CARD
	5	JUSB2 // E-Dock 2
	6	WWAN
	7	TOUCH

USH	0	BIO
	1	NA

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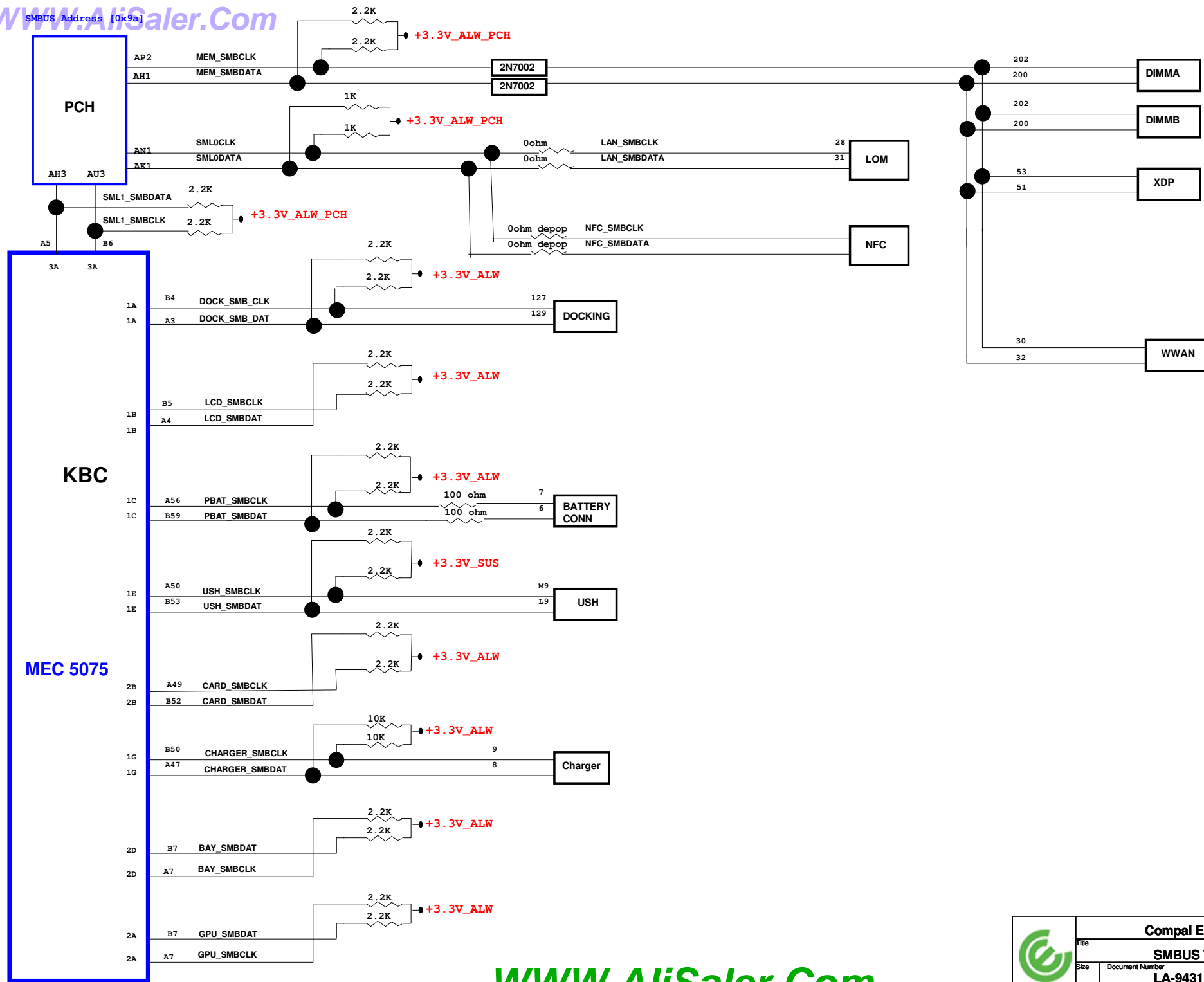
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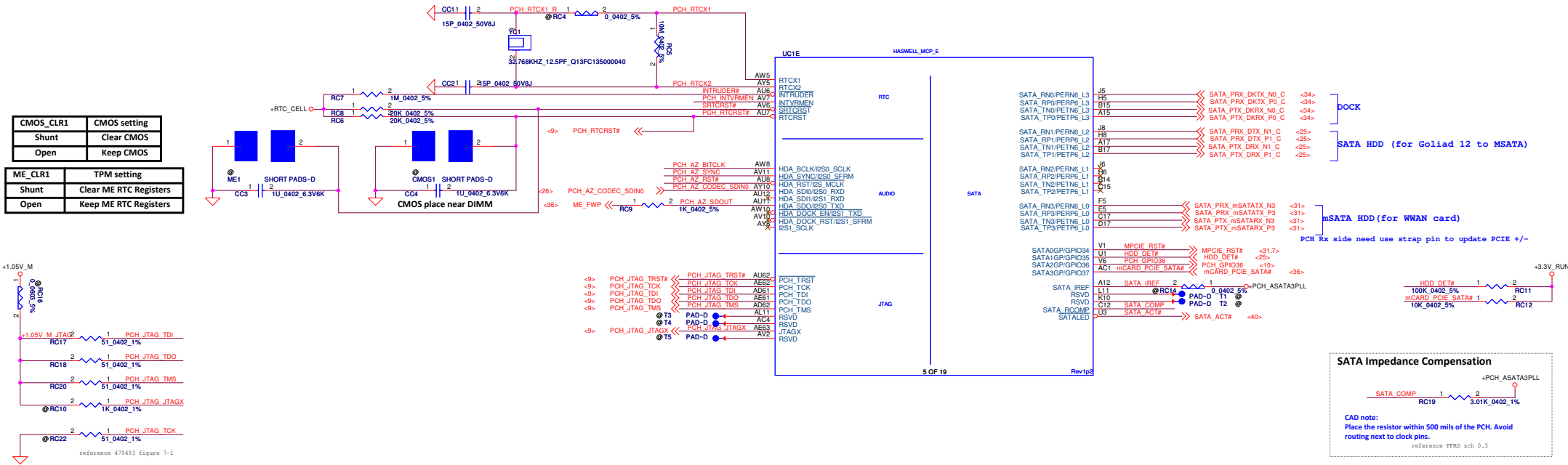


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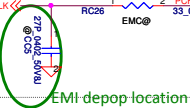
INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT)
HIGH = DISABLE



HDA for Codec

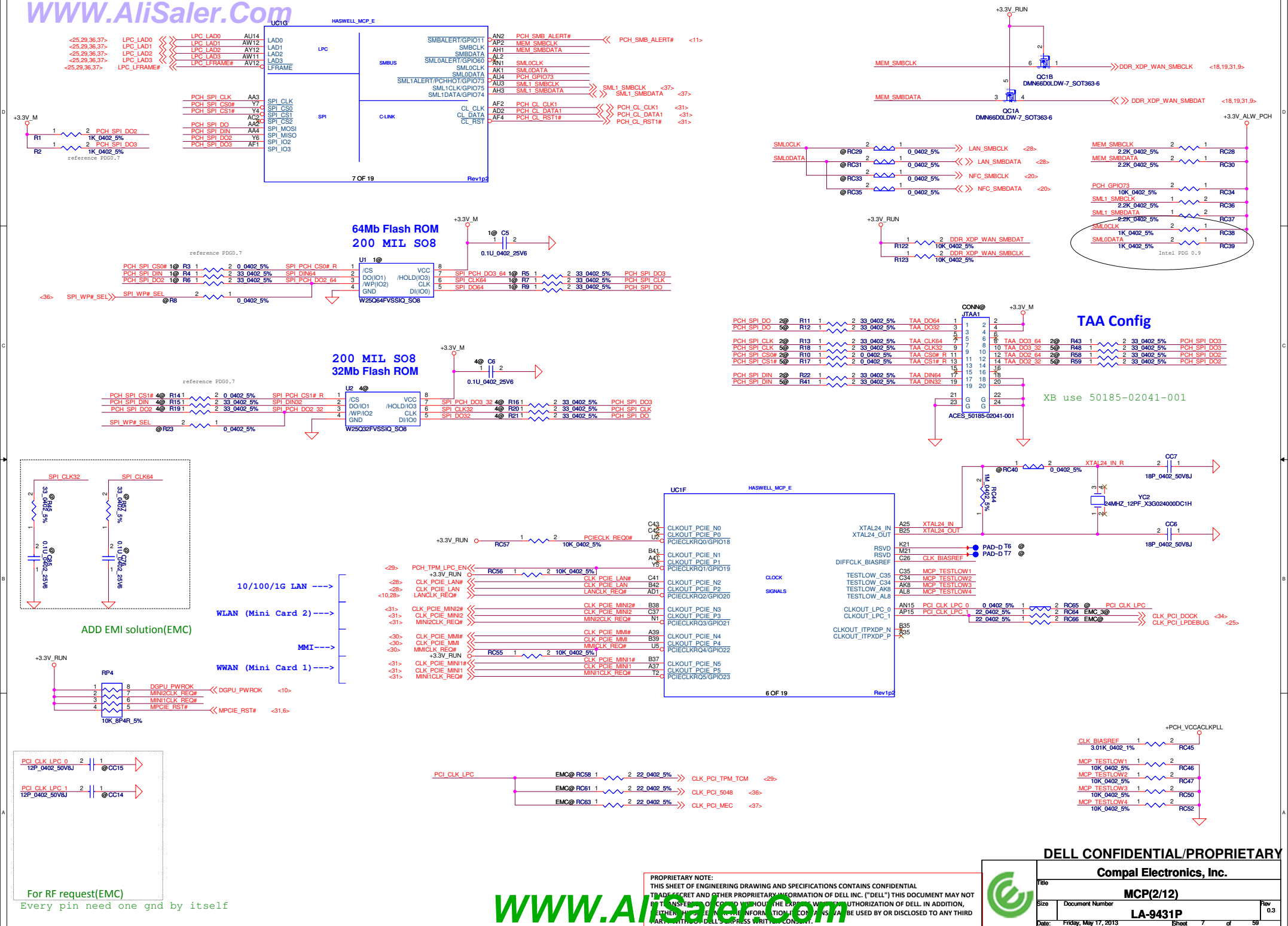
<26> PCH_AZ_CODECD_SDOUT << RC23 1 2 PCH_AZ_SDOUT 33 0402 5%
<26> PCH_AZ_CODECD_SYNC << RC24 1 2 PCH_AZ_SYNC 33 0402 5%
<26> PCH_AZ_CODECD_RST# << RC25 1 2 PCH_AZ_RST# 33 0402 5%
<26> PCH_AZ_CODECD_BITCLK << RC26 1 2 PCH_AZ_BITCLK 33 0402 5%



EMI depop location

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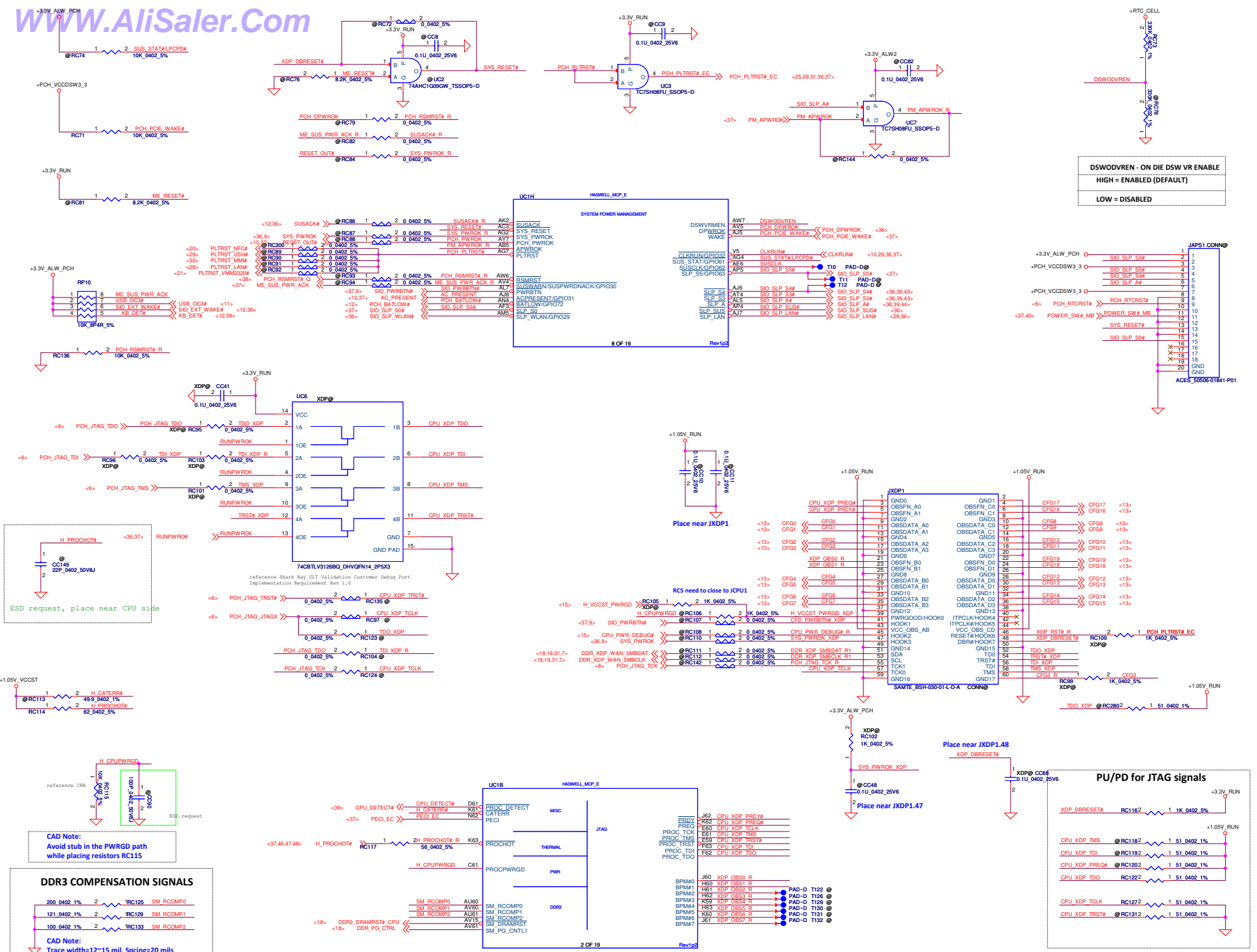
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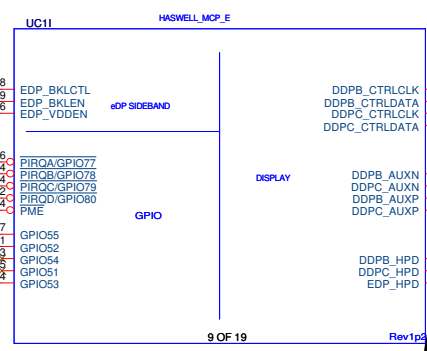
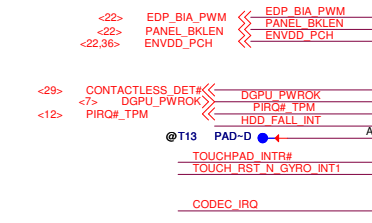
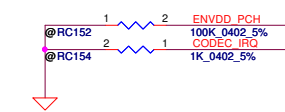
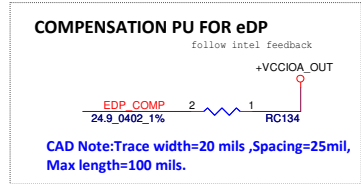
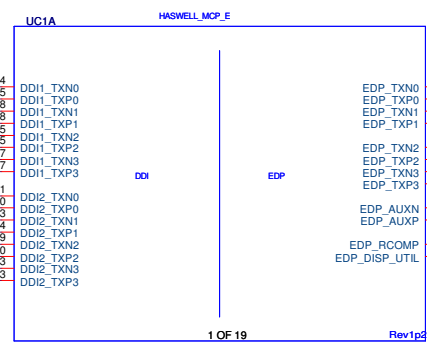
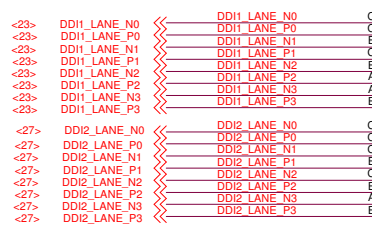
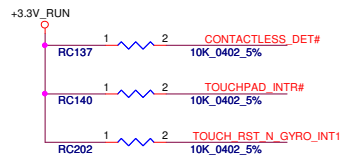
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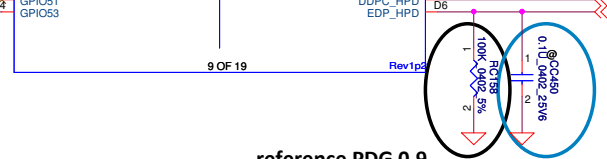
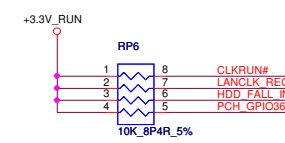
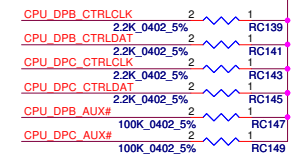
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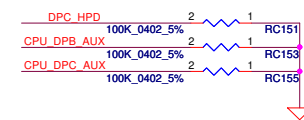
Intel WW18 Strapping option

Intel WW18 Strapping option



reference PDG 0.9

ESD solution for black screen issue



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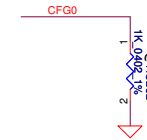
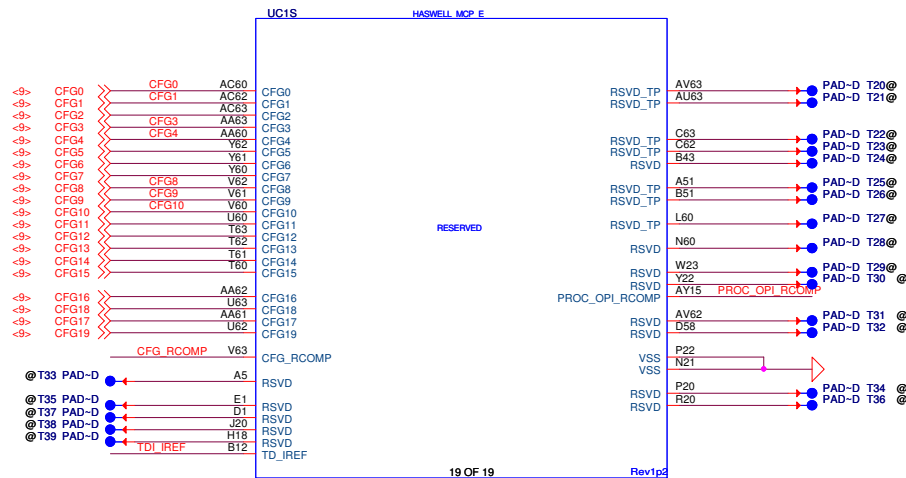
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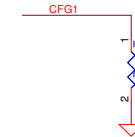
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CFG STRAPS for CPU



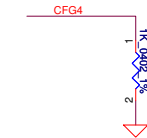
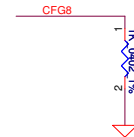
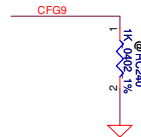
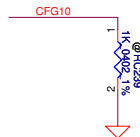
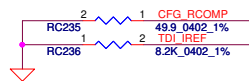
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE

CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed
------	---



PCH/PCH LESS MODE SELECTION

CFG1	1:(Default) Normal Operation 0:Lane Reversed
------	---



SAFE MODE BOOT	
CFG10	<p>1: POWER FEATURES ACTIVATED DURING RESET</p> <p>0: POWER FEATURES (ESPECIALLY CLOCK GATING) ARE NOT ACTIVATED</p>

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	<p>1: VRs support SVID protocol are present</p> <p>0: No VR support SVID is present</p> <p>The chip will not generate (OR Respond to) SVID activity</p>

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	<p>1: Enable(Default): Noa will be disable in locked units and enable in un-locked units</p> <p>0: Enable Noa will be available peggardless of the locking of the unit</p>

Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

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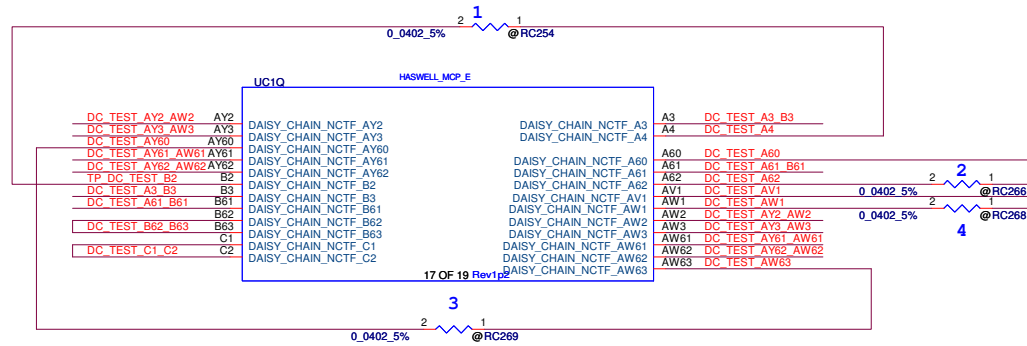
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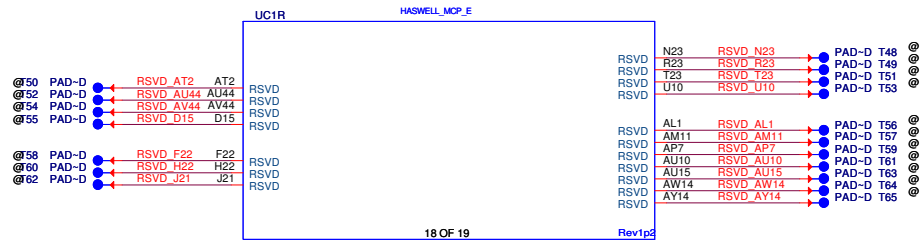
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**Package Daisy Chain:**

1. B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2. A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3. AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4. AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1

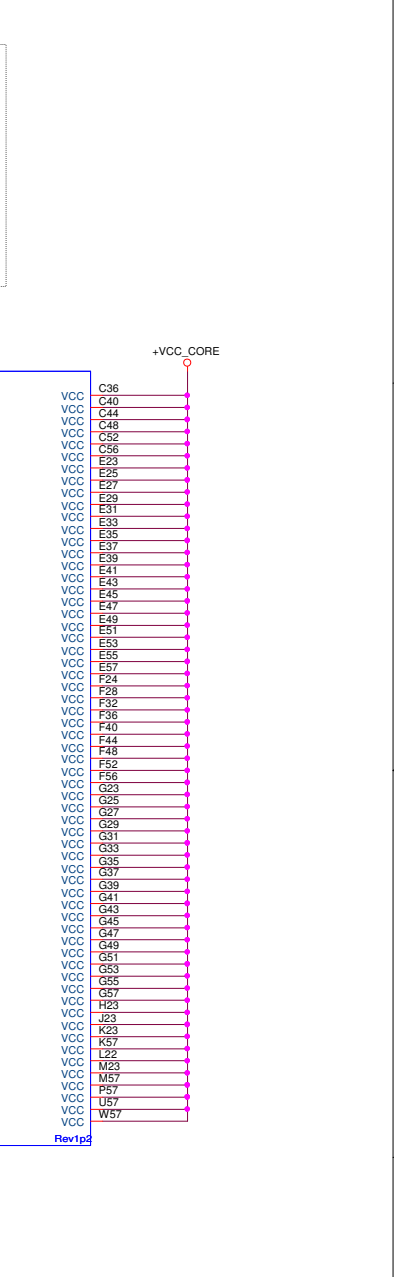
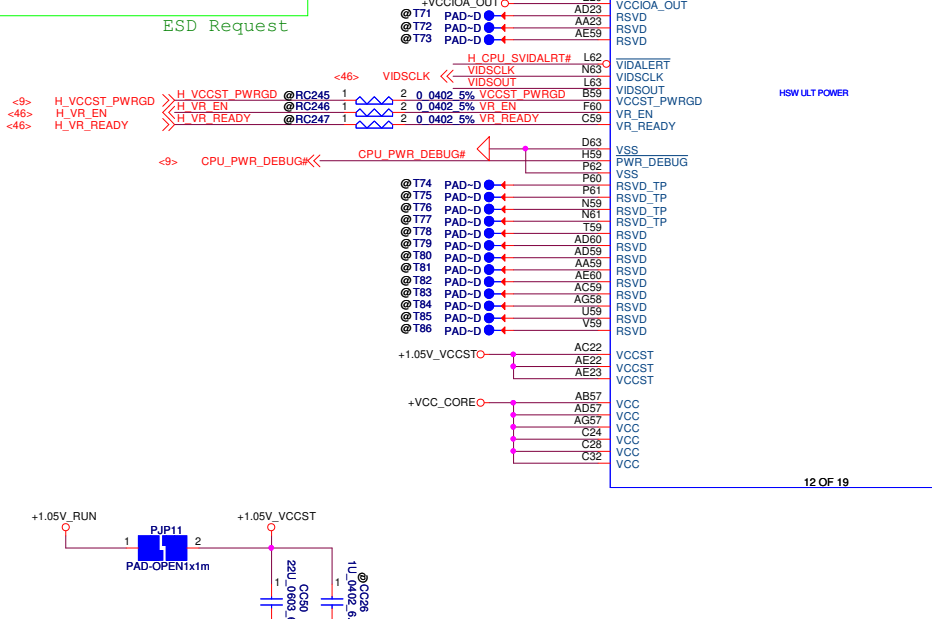
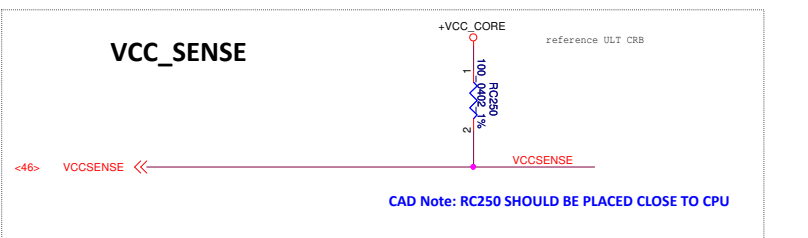
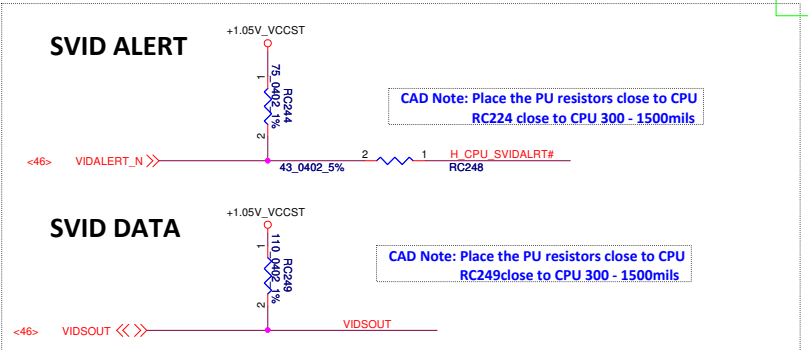
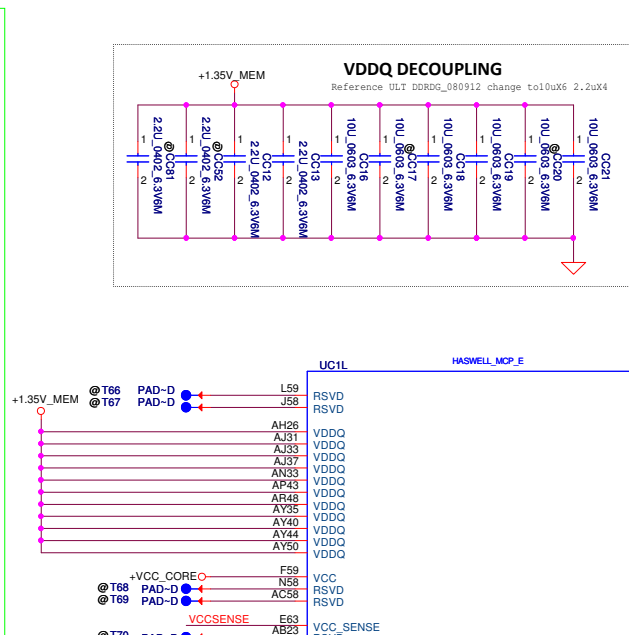
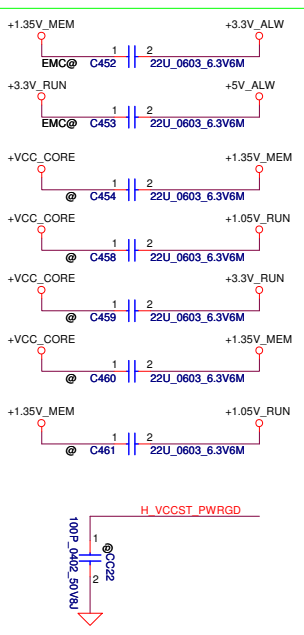
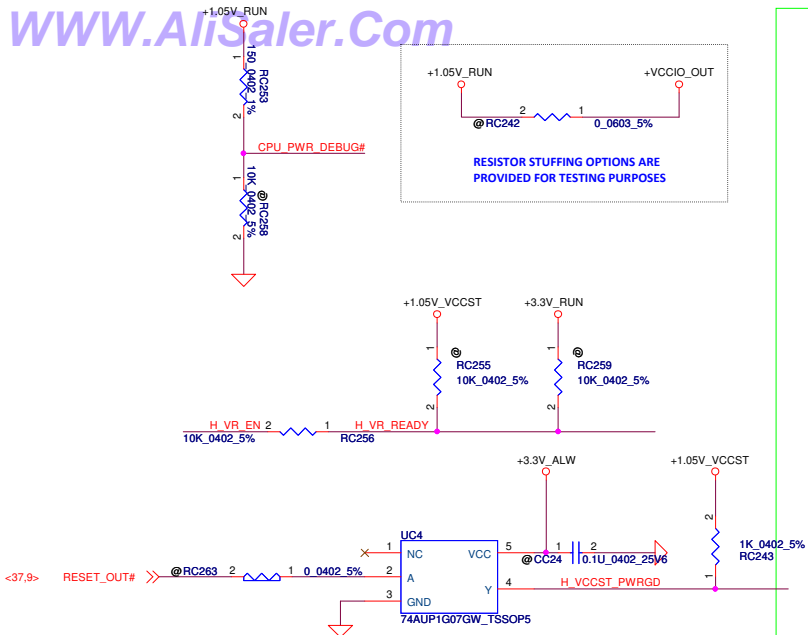


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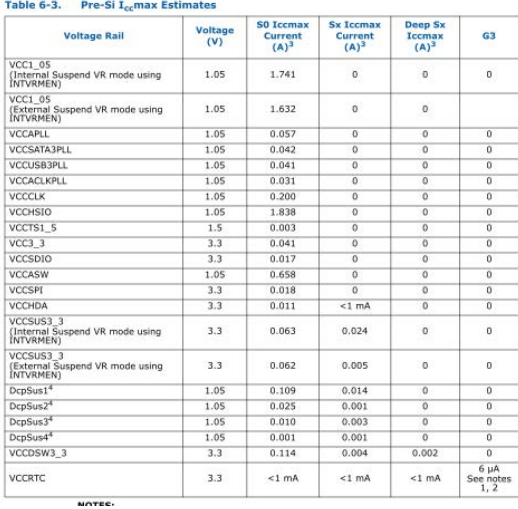
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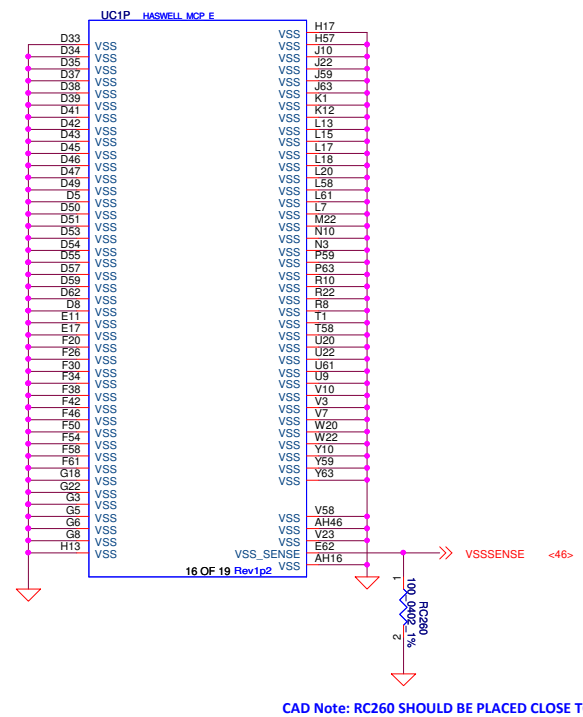
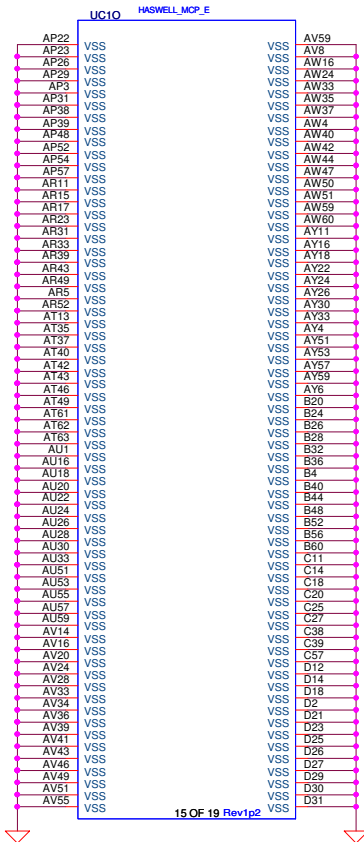
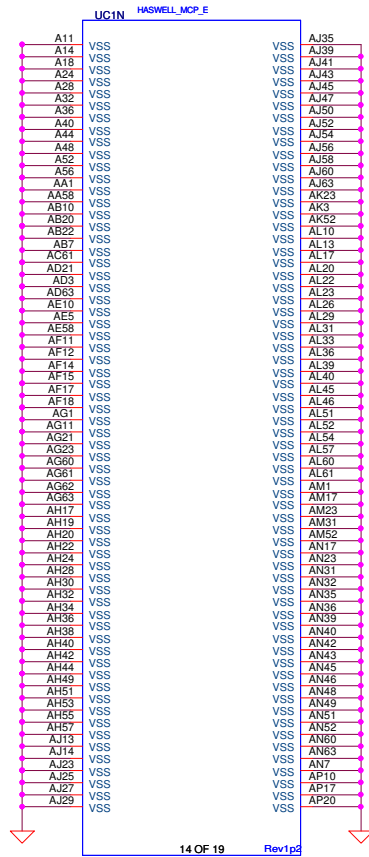




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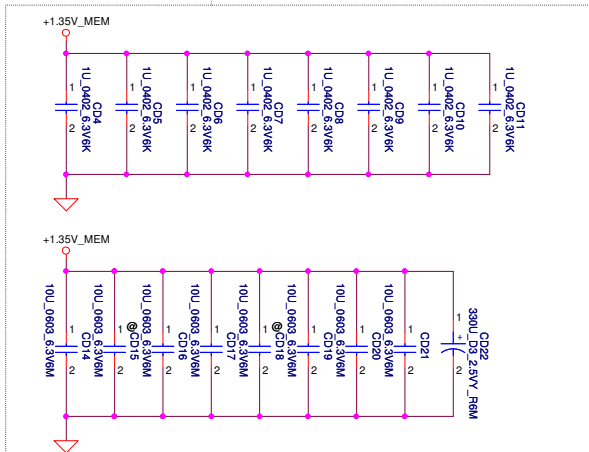
```
Populate RD1, De-Populate RD7 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3
```

All VREF traces should have 10 mil trace width

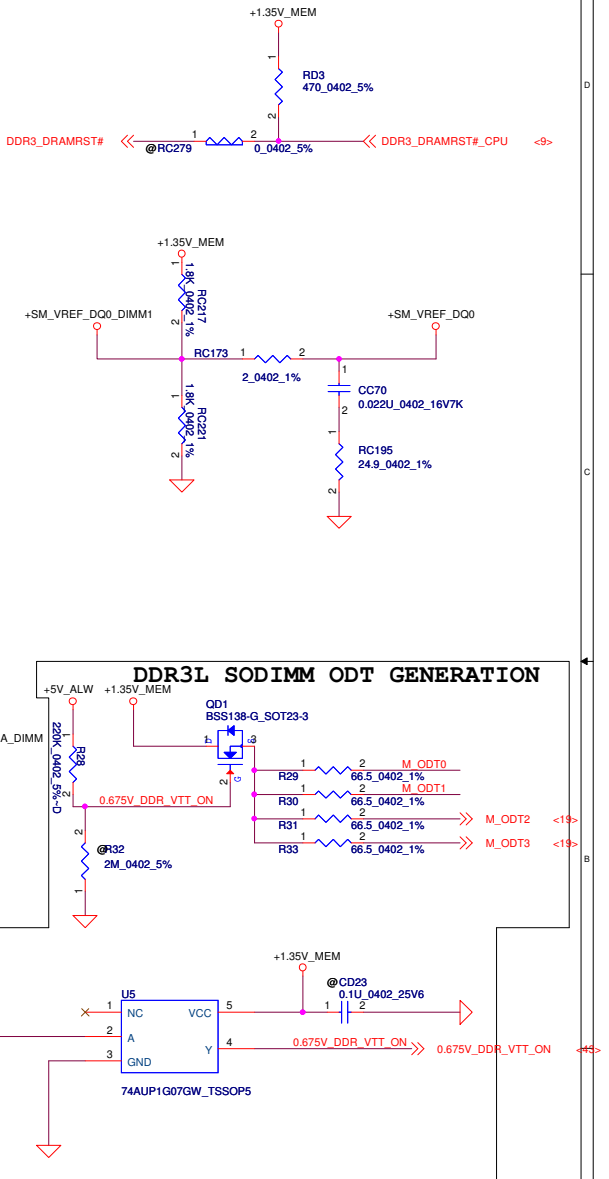
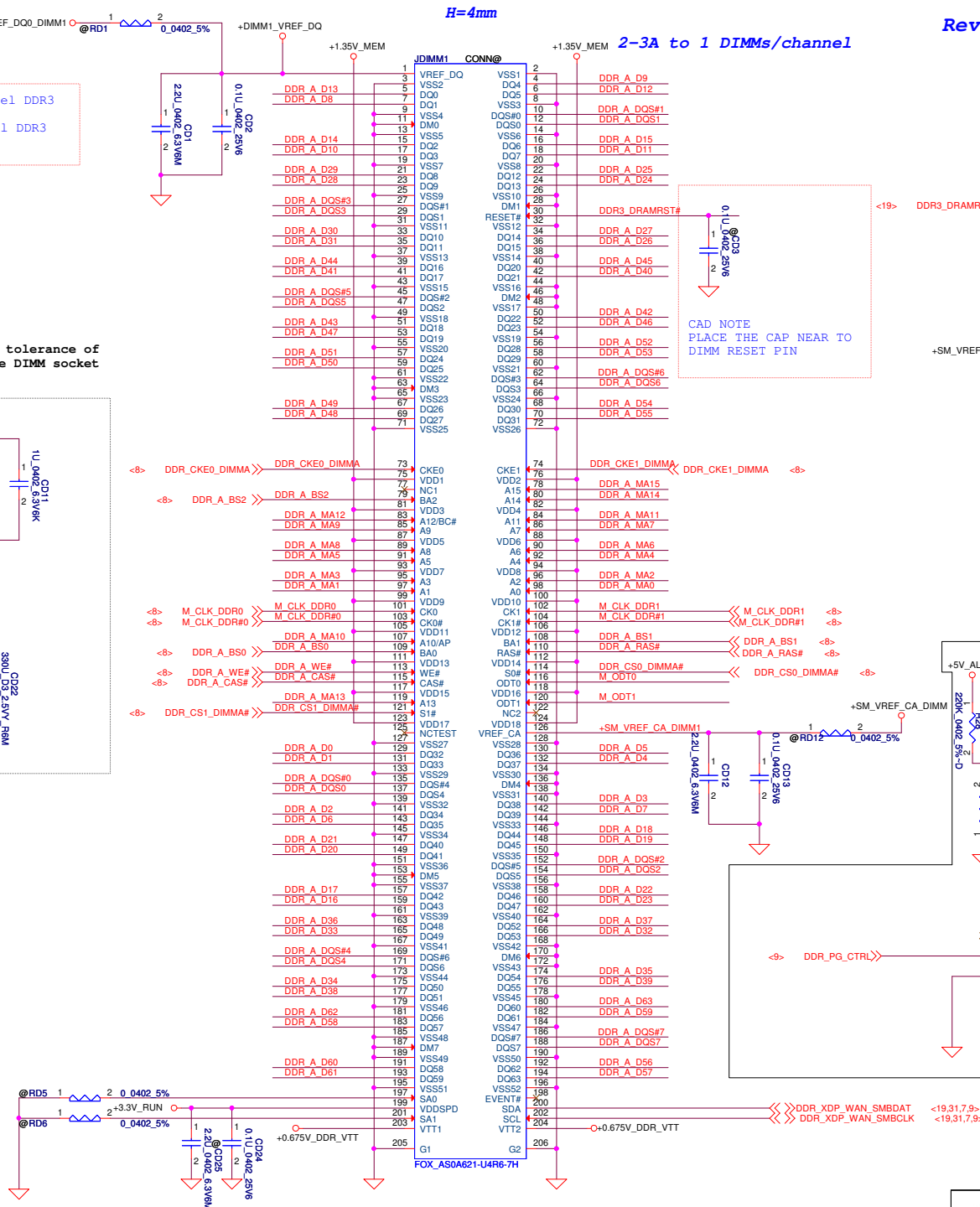
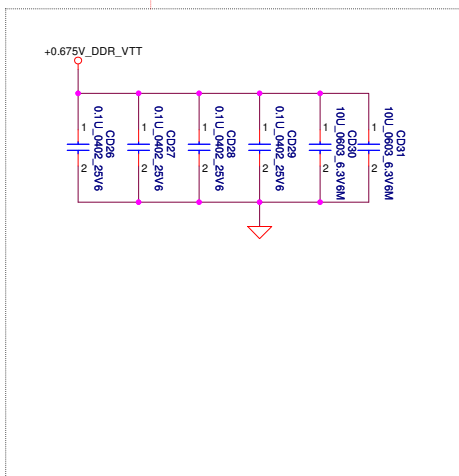
```
<8>   DDR_A_DQS#[0..7] << >>
<8>   DDR_A_D[0..63] << >>
<8>   DDR_A_DQS[0..7] << >>
<8>   DDR_A_MA[0..15] >>
```

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMM1.203,204



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DDRIII-SODIMM SLOT1

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Reverse Type

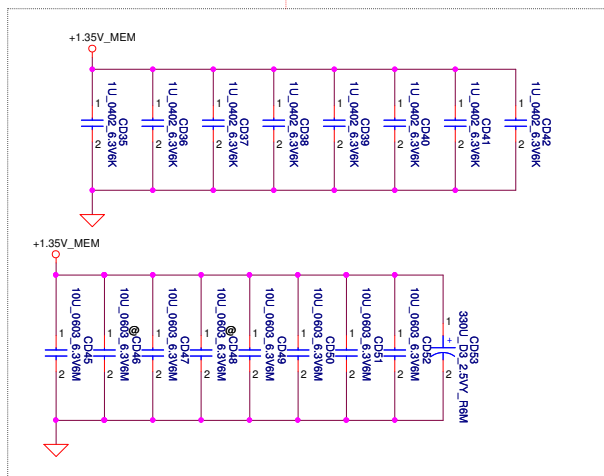
```
Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3
```

```
<8> DDR_B_DQS#[0..7] << >>
<8> DDR_B_D[0..63] << >>
<8> DDR_B_DQS[0..7] << >>
<8> DDR_B_MA[0..15] >>
```

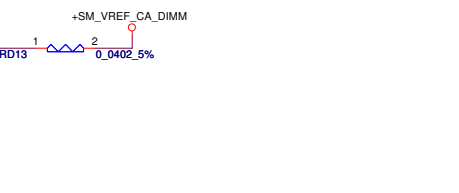
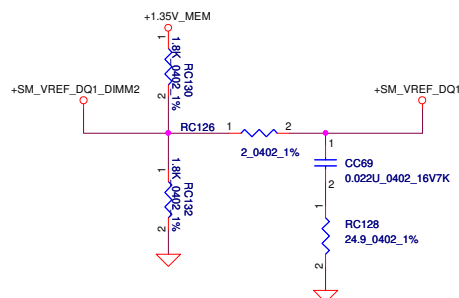
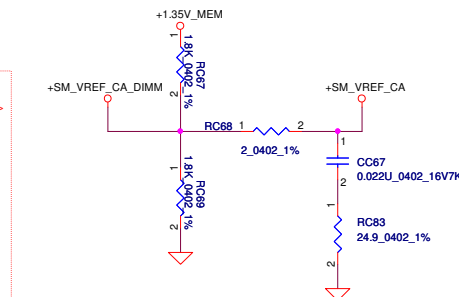
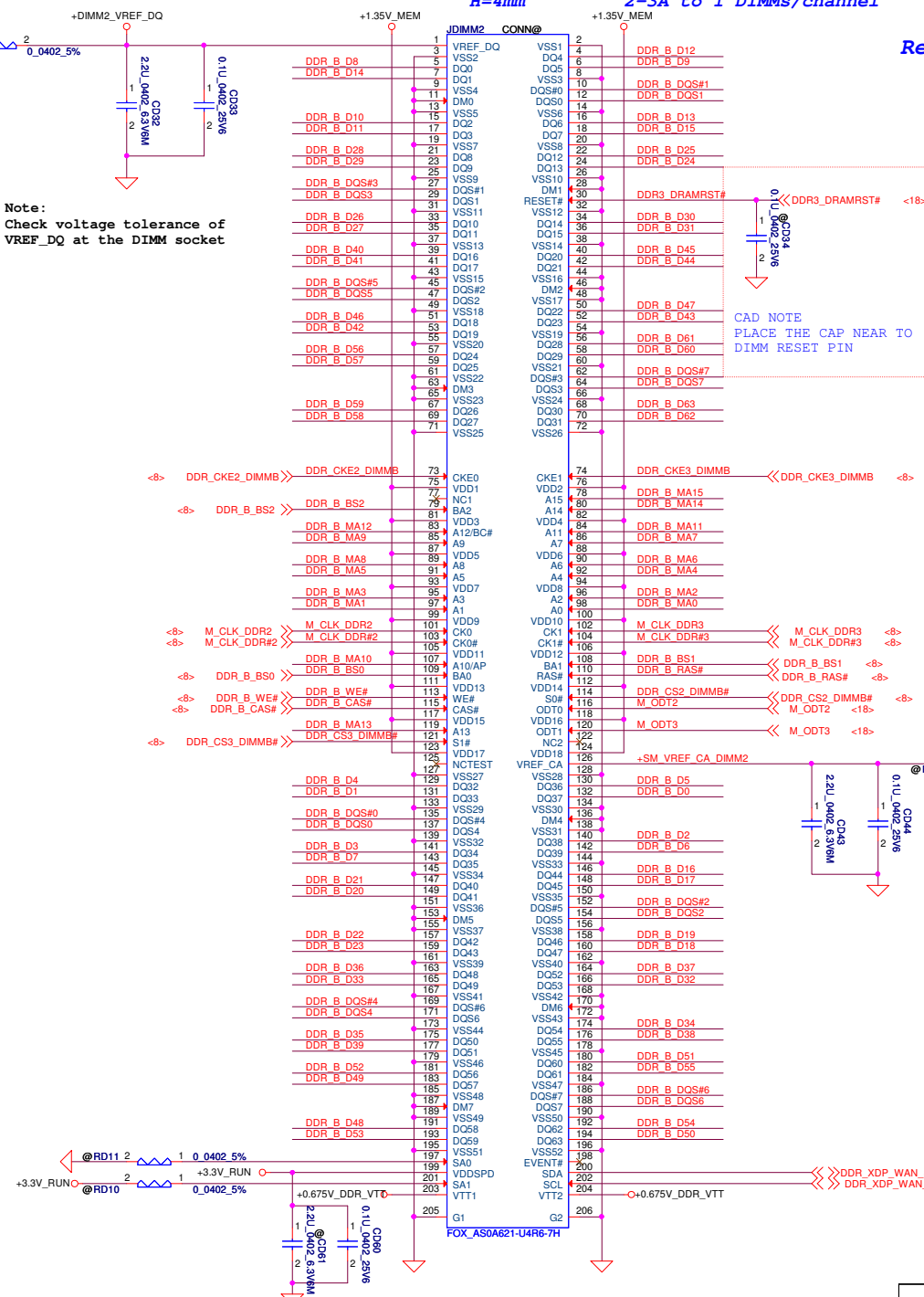
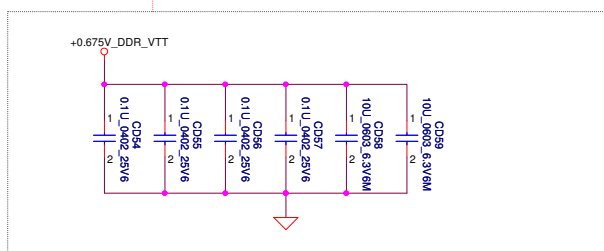
All VREF traces should have 10 mil trace width

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204



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DDRIII-SODIMM SLOT2

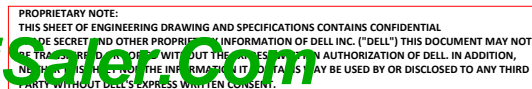
LA-9431P

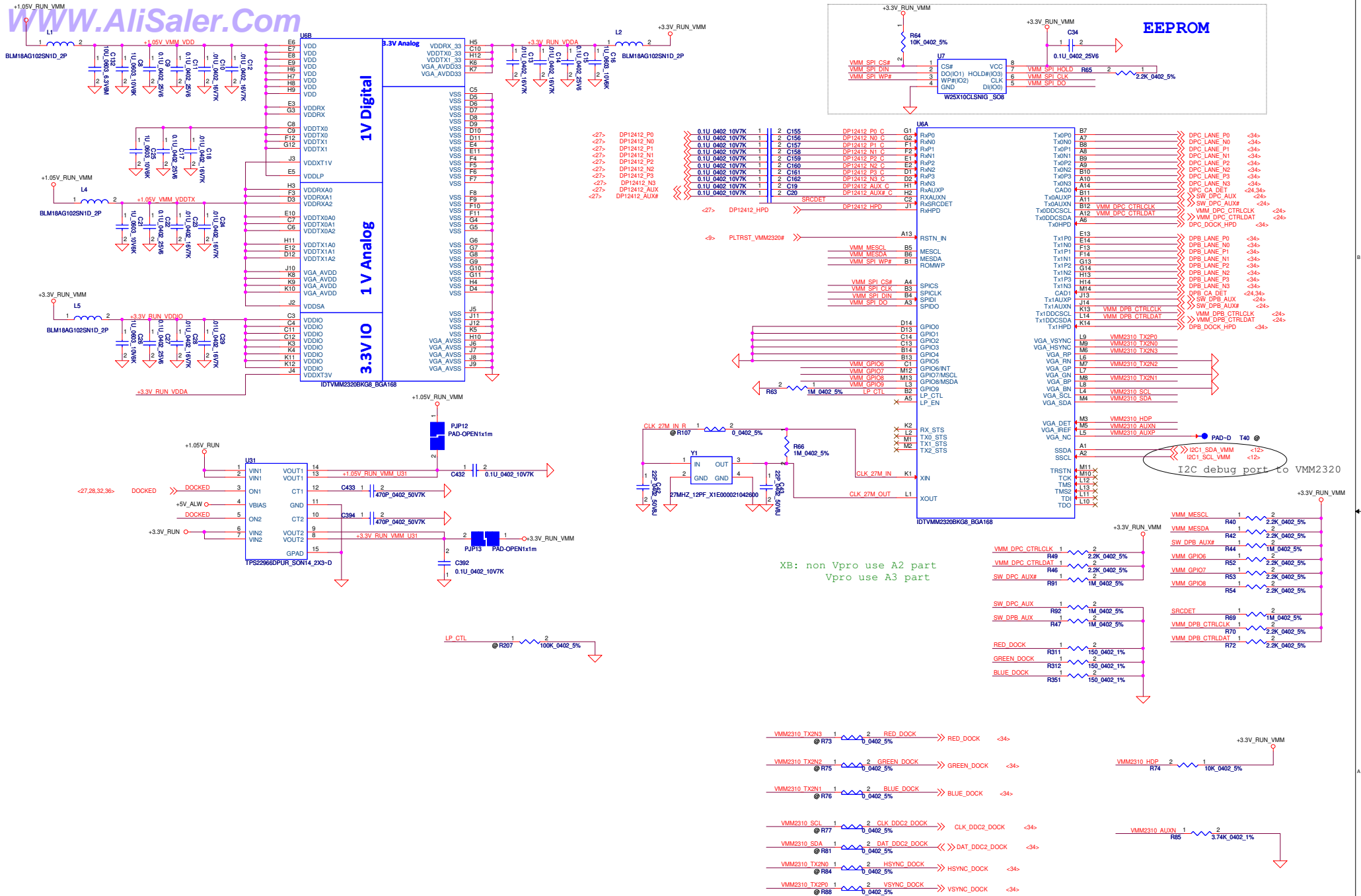
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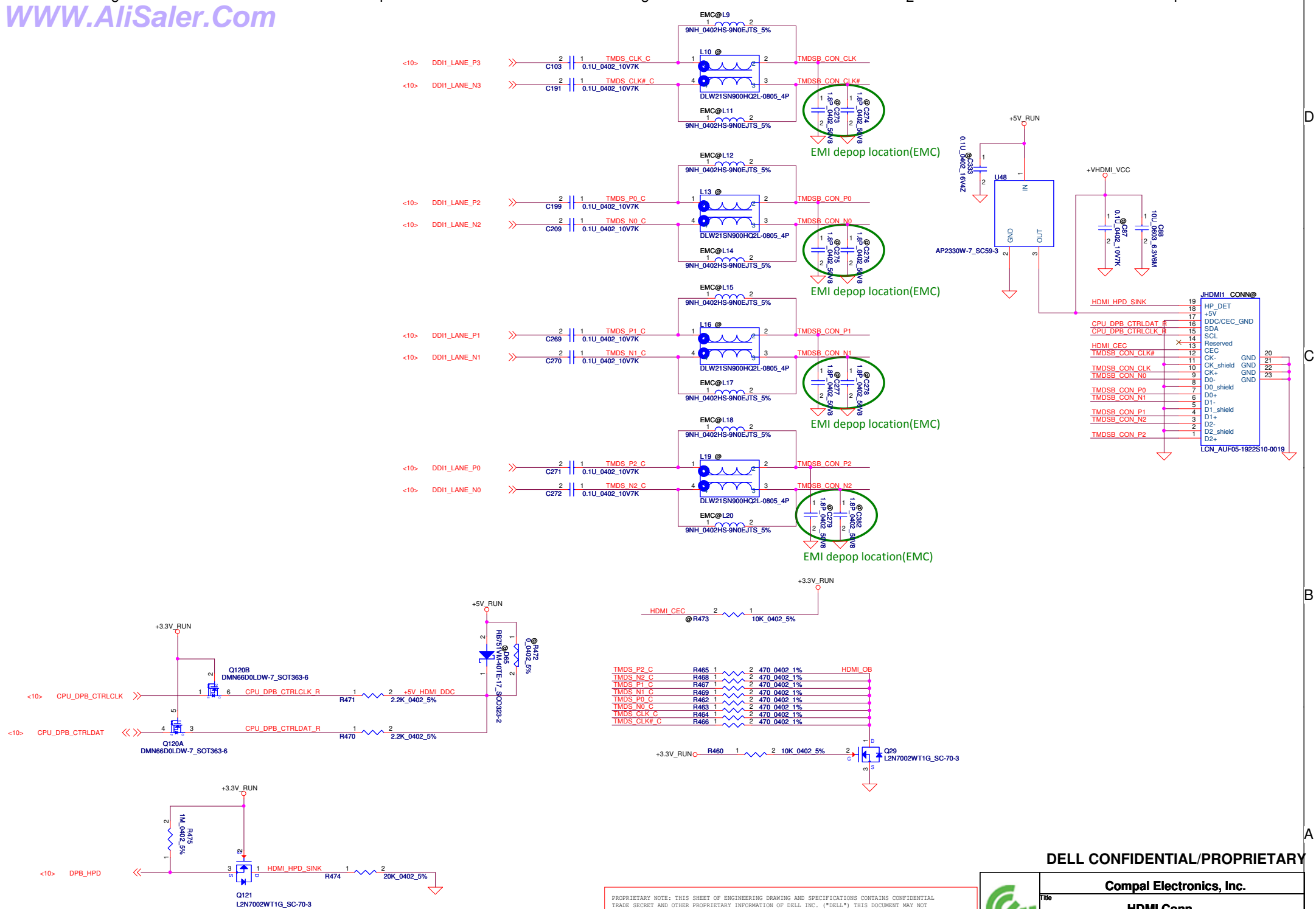
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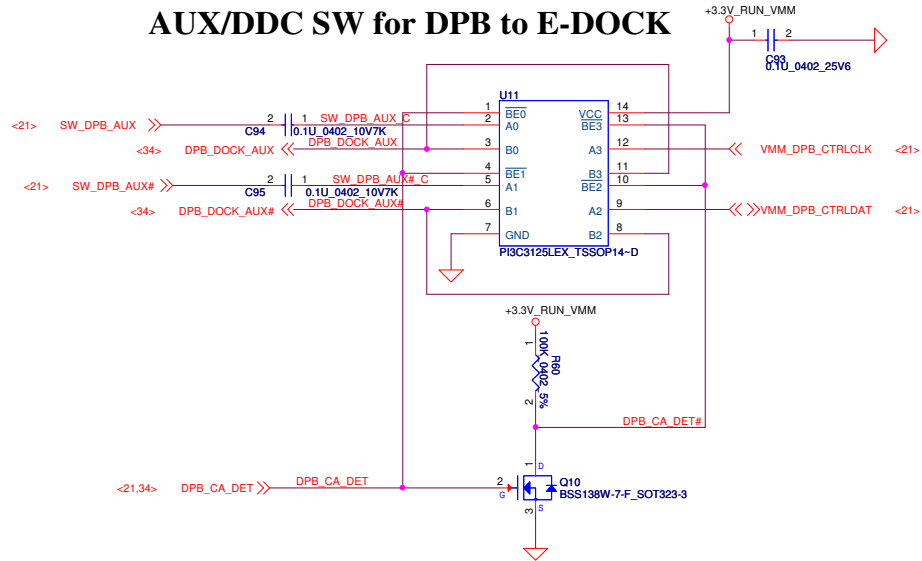
IDT VMM2320 DP and VGA SW

LA-9431P

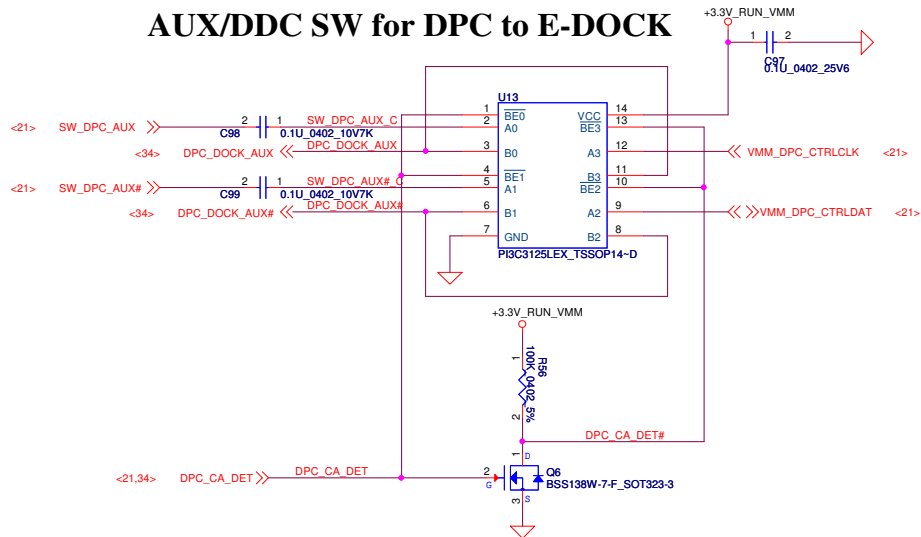
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AUX/DDC SW for DPB to E-DOCK



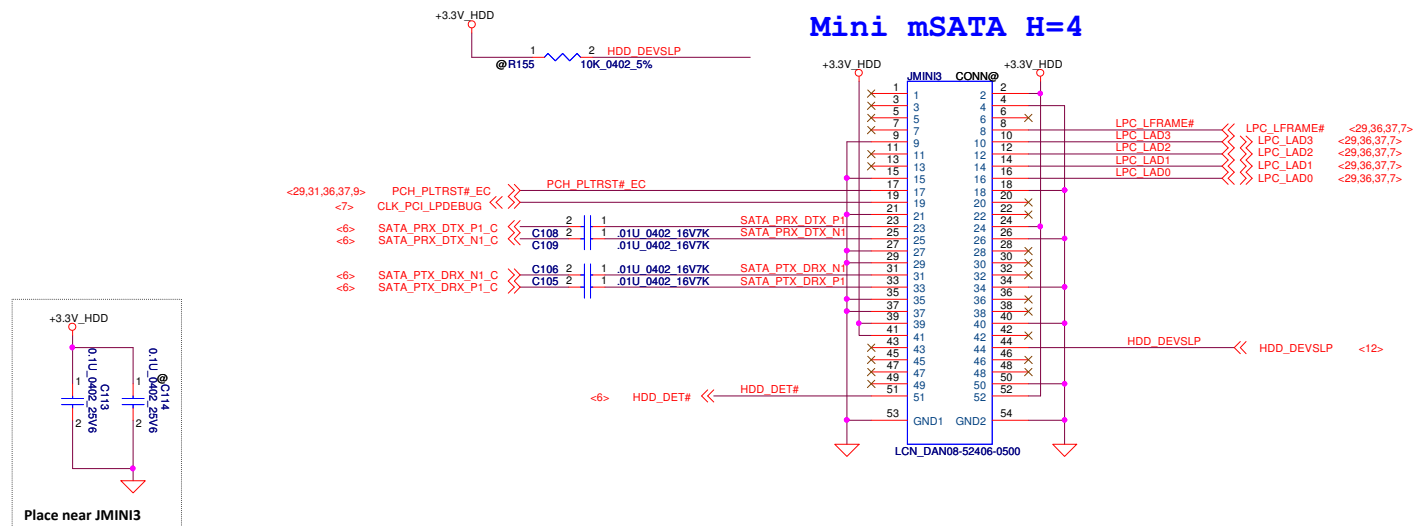
AUX/DDC SW for DPC to E-DOCK



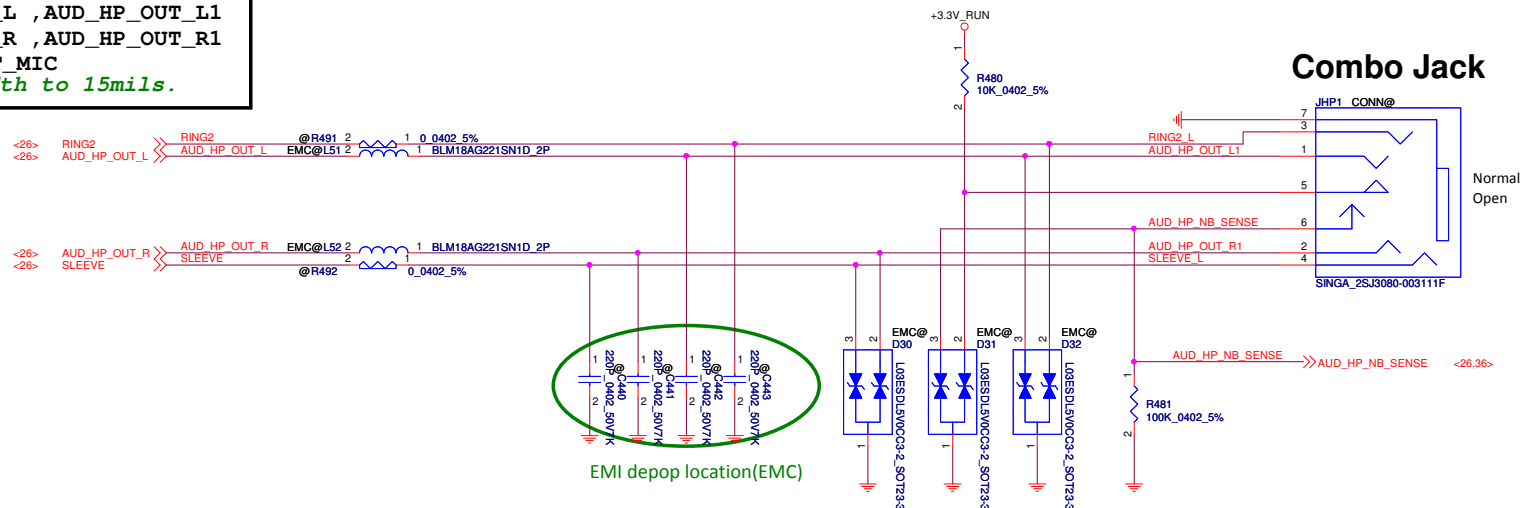
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DP SW DP125			
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RING2 , RING2_L
AUD_HP_OUT_L , AUD_HP_OUT_L1
AUD_HP_OUT_R , AUD_HP_OUT_R1
SLEEVE , EXT_MIC
Trace width to 15mils.



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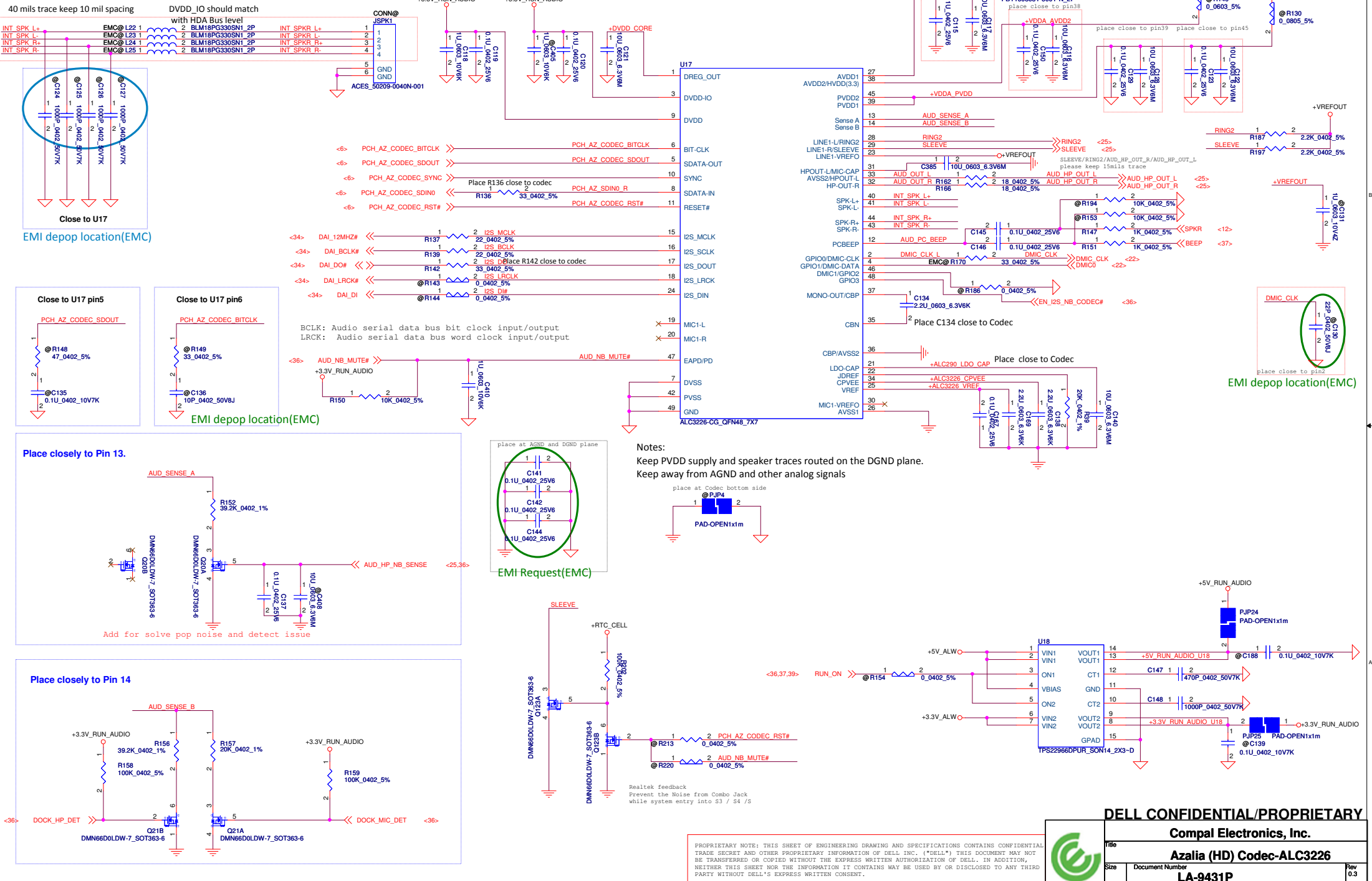
Min Card/mSATA/Combo Jack

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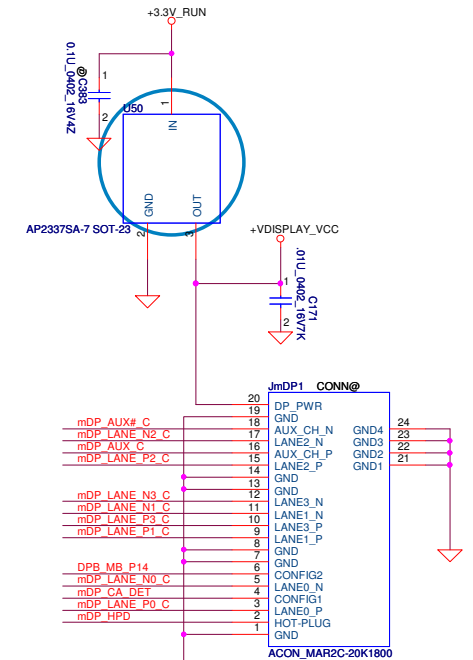
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Title	DB/DB10410
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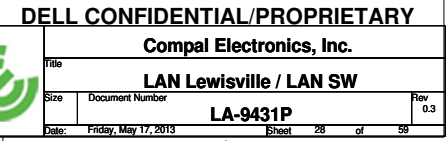


DOCKED	function
1	Dock
0	mini DP

AUX/DDC SW for DPC to Mini DP

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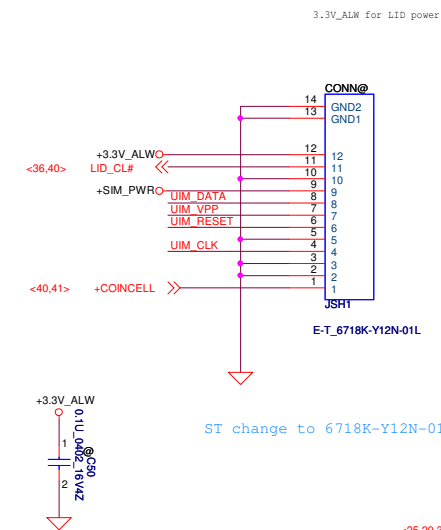
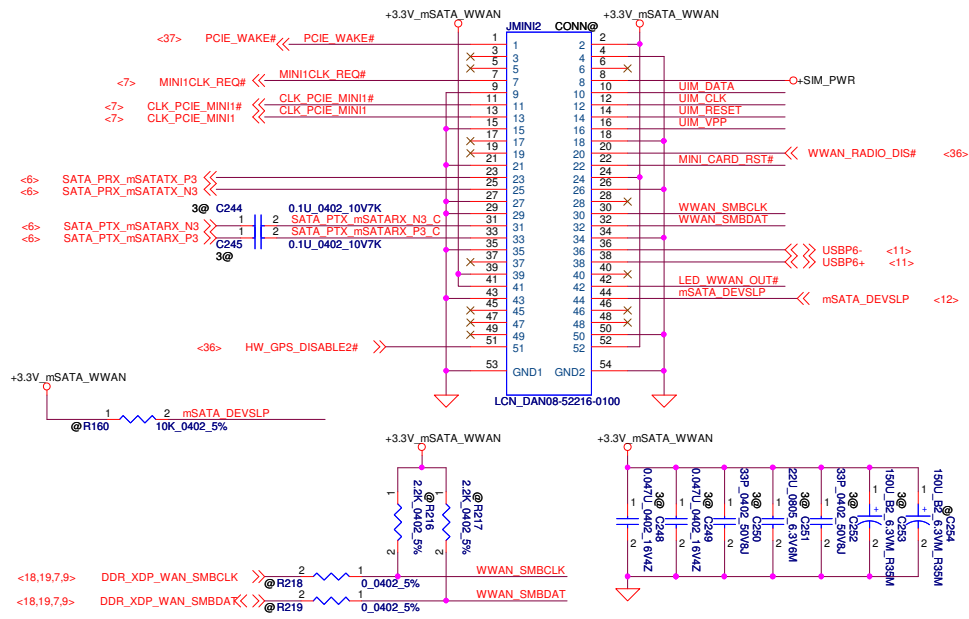




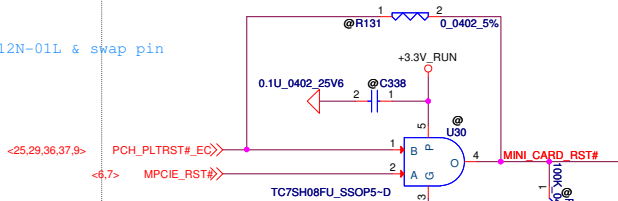


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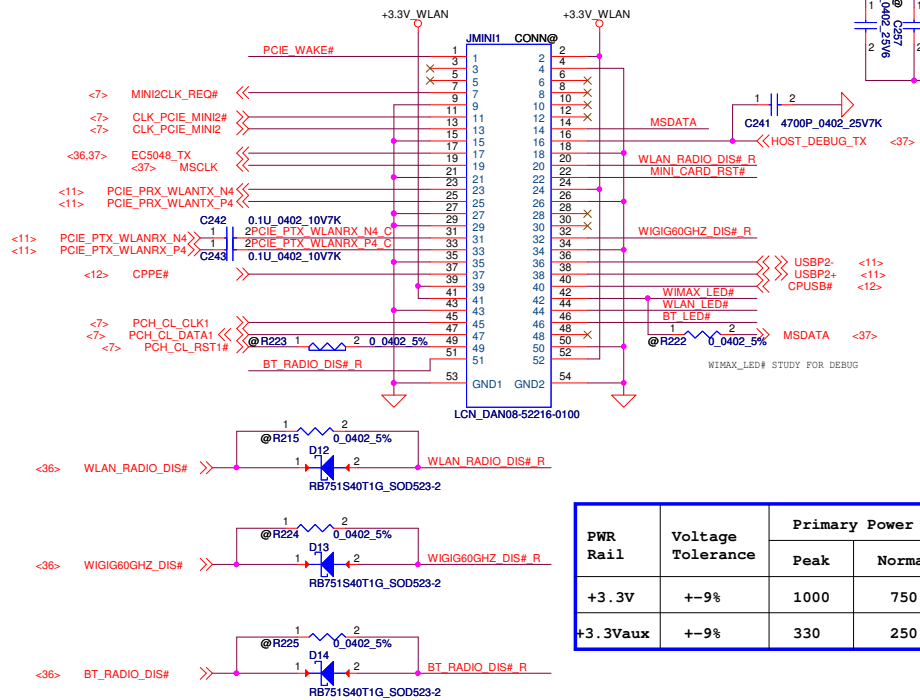
Mini WWAN/GPS/LTE/mSATA H=3.6



ST change to 6718K-Y12N-01L & swap pin

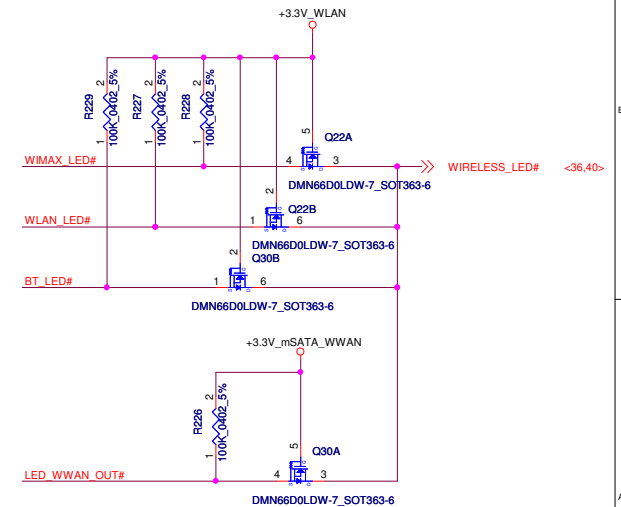


Mini WLAN/WIiGi/BT H=3.6



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+−9%	1000	750	
+3.3Vaux	+−9%	330	250	250 (Wake enable) 5 (Not wake enable)

LED control circuit



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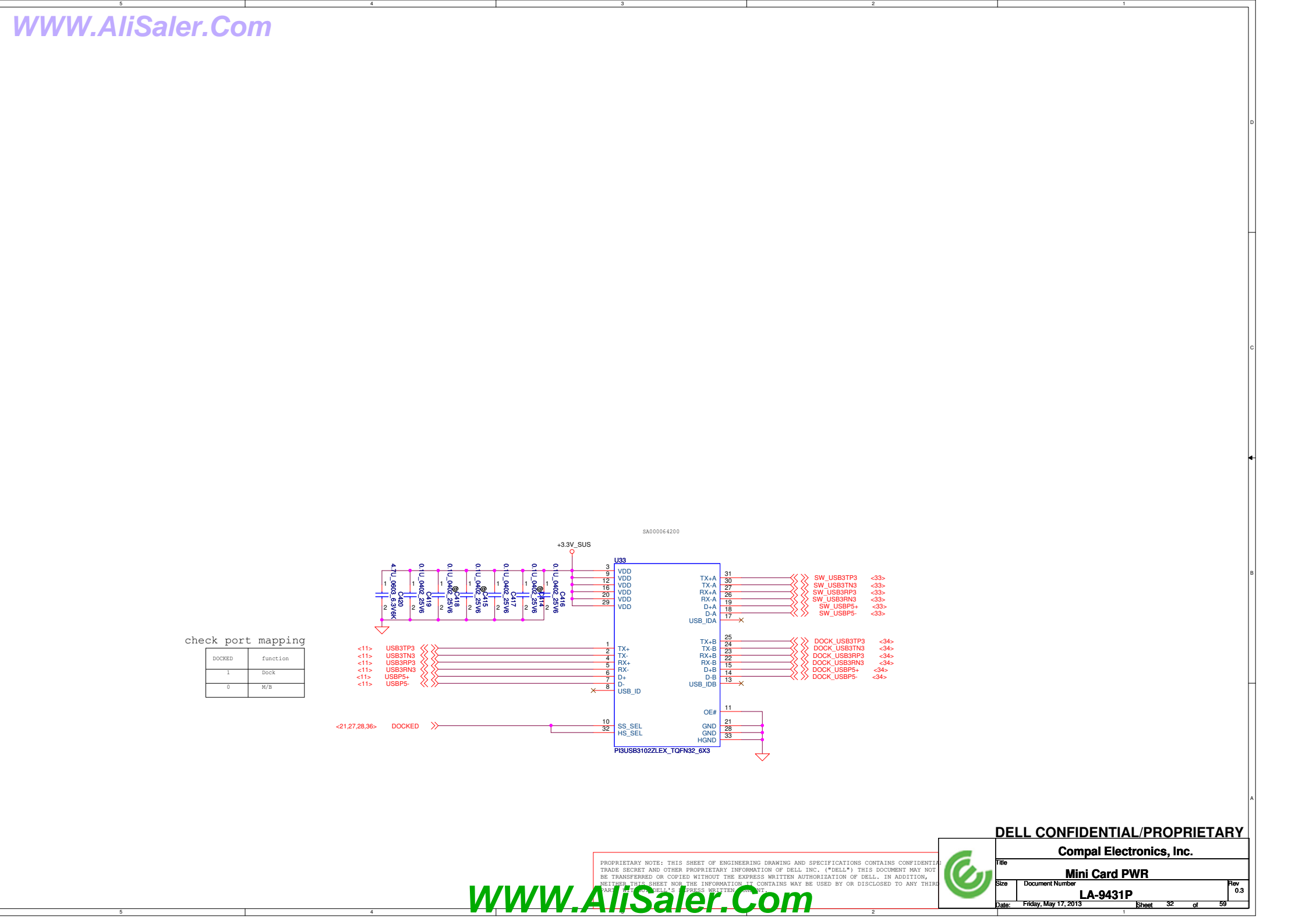
Mini Card/SIM Card

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[illegible]

SA000064200

check port mapping

DOCKED	function
1	Dock
0	N/B

U33

P18USB3102ZLEX_TOFN32_6X3

<11> USB3TP3 >>

<11> USB3TN3 >>

<11> USB3RP3 >>

<11> USB3RN3 >>

<11> USBP5+ >>

<11> USBP5- >>

TX+A 31 >> SW_USB3TP3 <33>

TX-A 30 >> SW_USB3TN3 <33>

RX+A 27 >> SW_USB3RP3 <33>

RX-B 26 >> SW_USB3RN3 <33>

D+A 19 >> SW_USBP5+ <33>

D-B 18 >> SW_USBP5- <33>

USB_IDA 17 X

TX+B 25 >> DOCK_USB3TP3 <34>

TX-B 24 >> DOCK_USB3TN3 <34>

RX+B 23 >> DOCK_USB3RP3 <34>

RX-B 22 >> DOCK_USB3RN3 <34>

D+B 15 >> DOCK_USBP5+ <34>

D-B 14 >> DOCK_USBP5- <34>

USB_IDB 13 X

OE# 11

GND 21

GND 28

HGND 33

<21,27,28,36> DOCKED >>

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SA000064200

check port mapping

DOCKED	function
1	Dock
0	N/B

U33

P18USB3102ZLEX_TOFN32_6X3

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Mini Card PWR

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[illegible]

SA000064200

check port mapping

DOCKED	function
1	Dock
0	N/B

U33

P18USB3102ZLEX_TOFN32_6X3

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Mini Card PWR

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SA000064200

check port mapping

DOCKED	function
1	Dock
0	N/B

<21,27,28,36> DOCKED >>

U33

P18USB3102ZLEX_TOFN32_6X3

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SA000064200

check port mapping

DOCKED	function
1	Dock
0	N/B

U33

P18USB3102ZLEX_TOFN32_6X3

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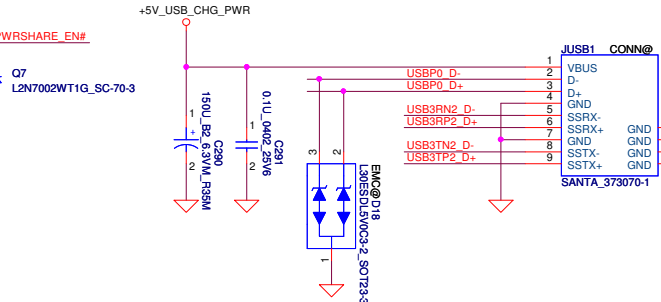
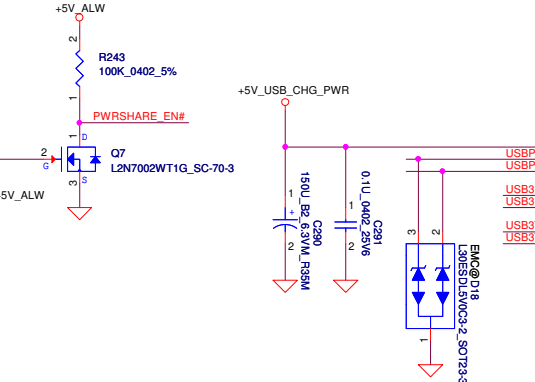
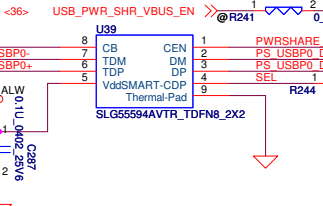
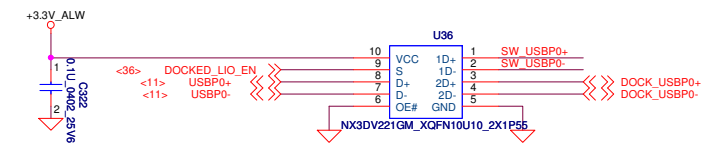
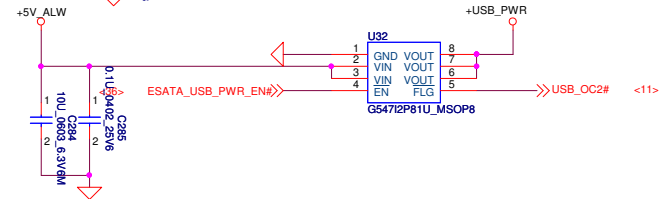
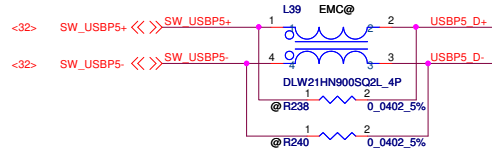
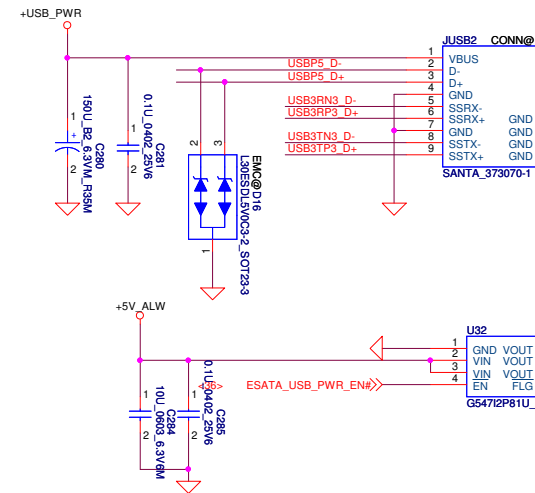
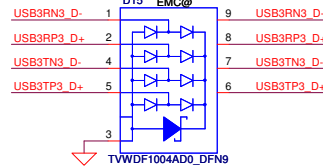
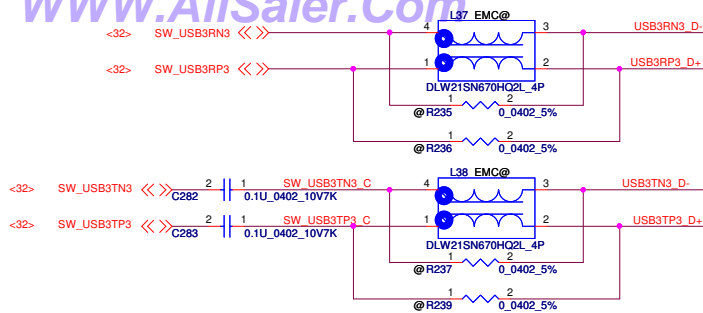
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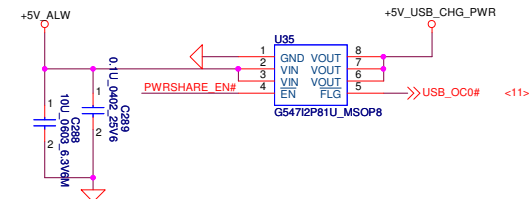
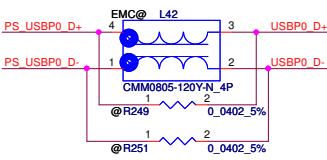
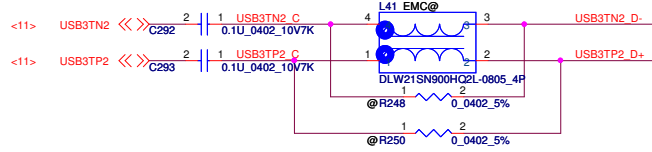
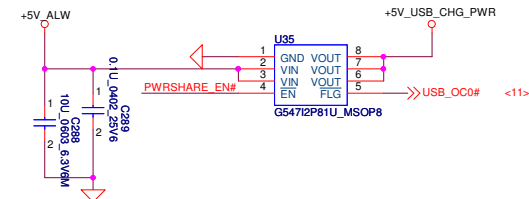
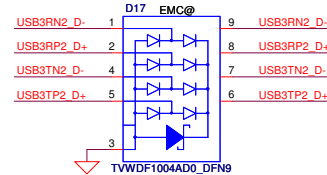
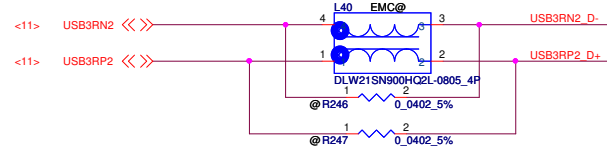
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check port mapping

DOCKED_LIO_EN	function
1	Dock
0	N/A



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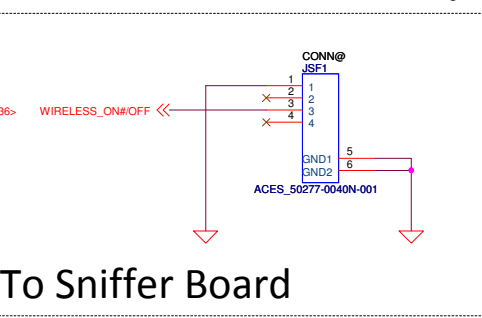
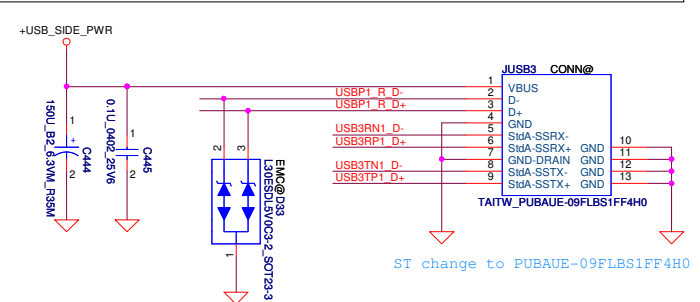
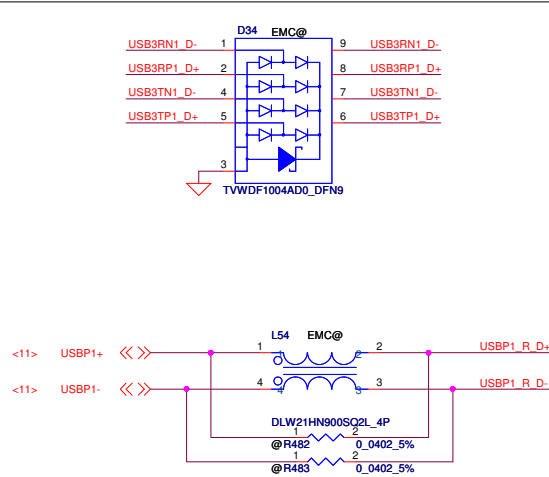
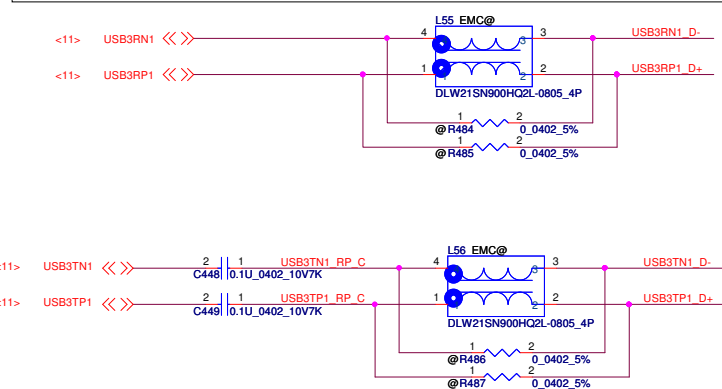
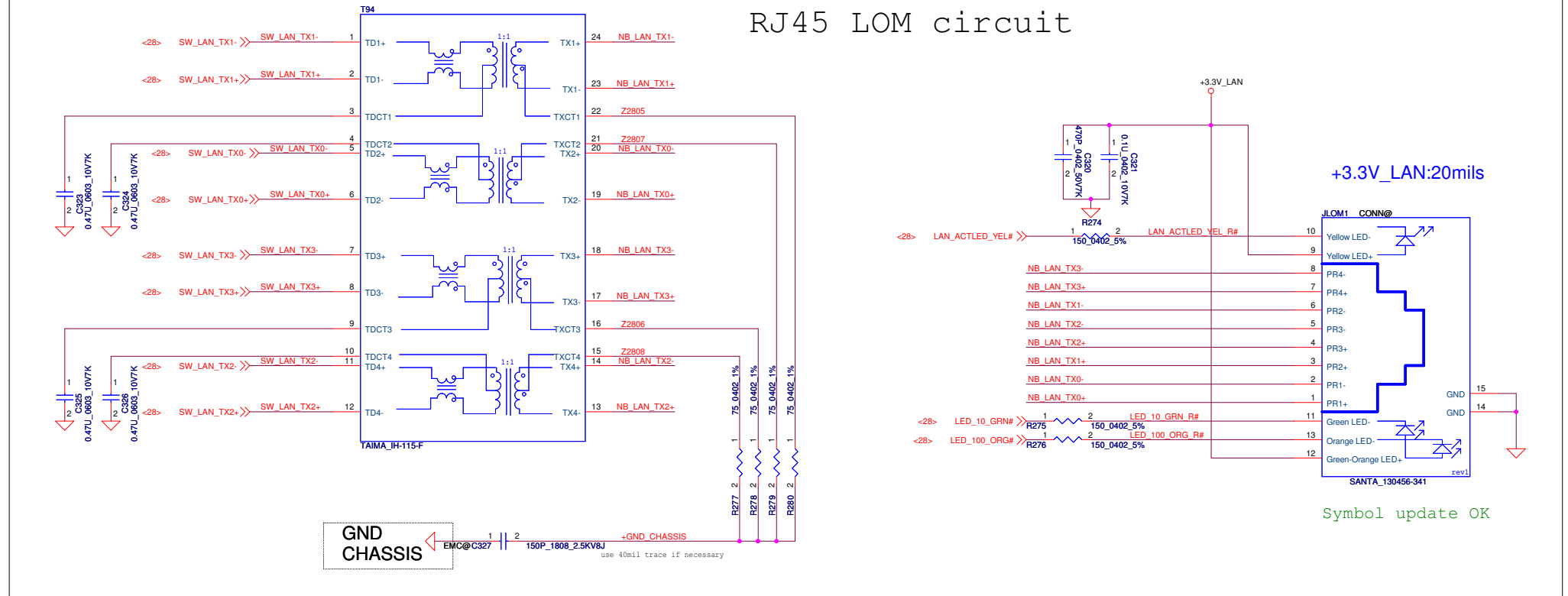


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USB x2			
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RJ45 LOM circuit



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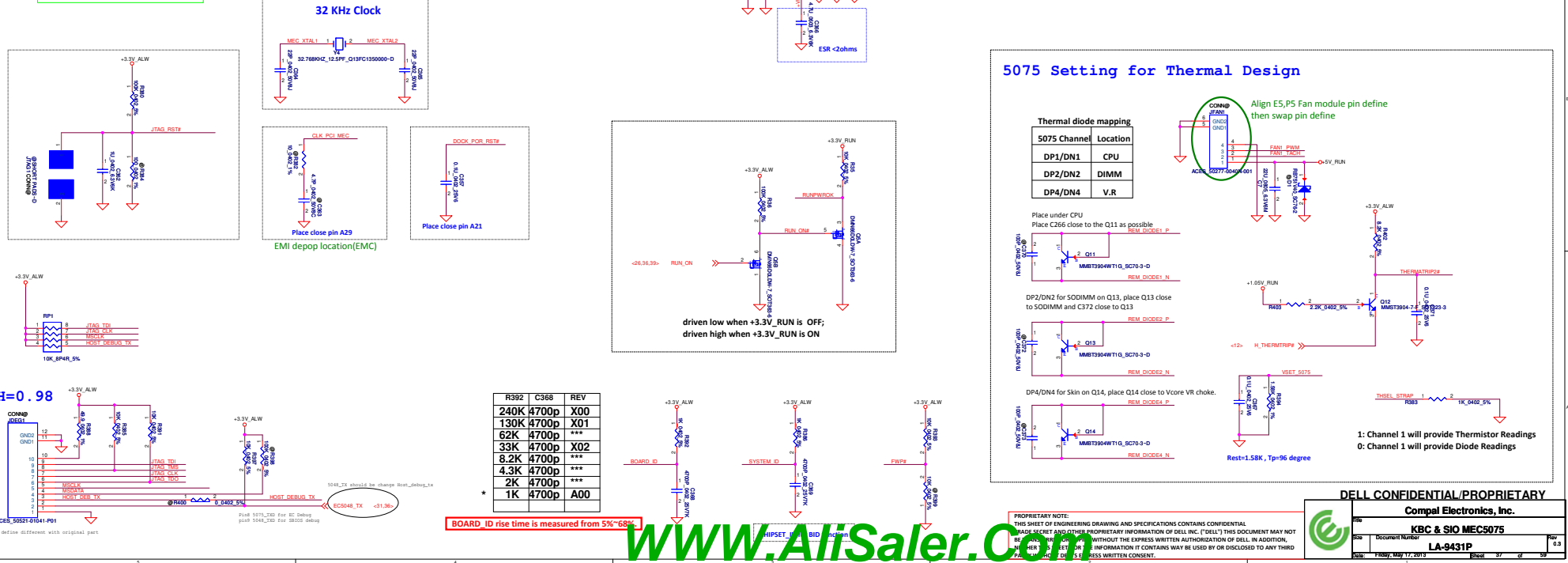
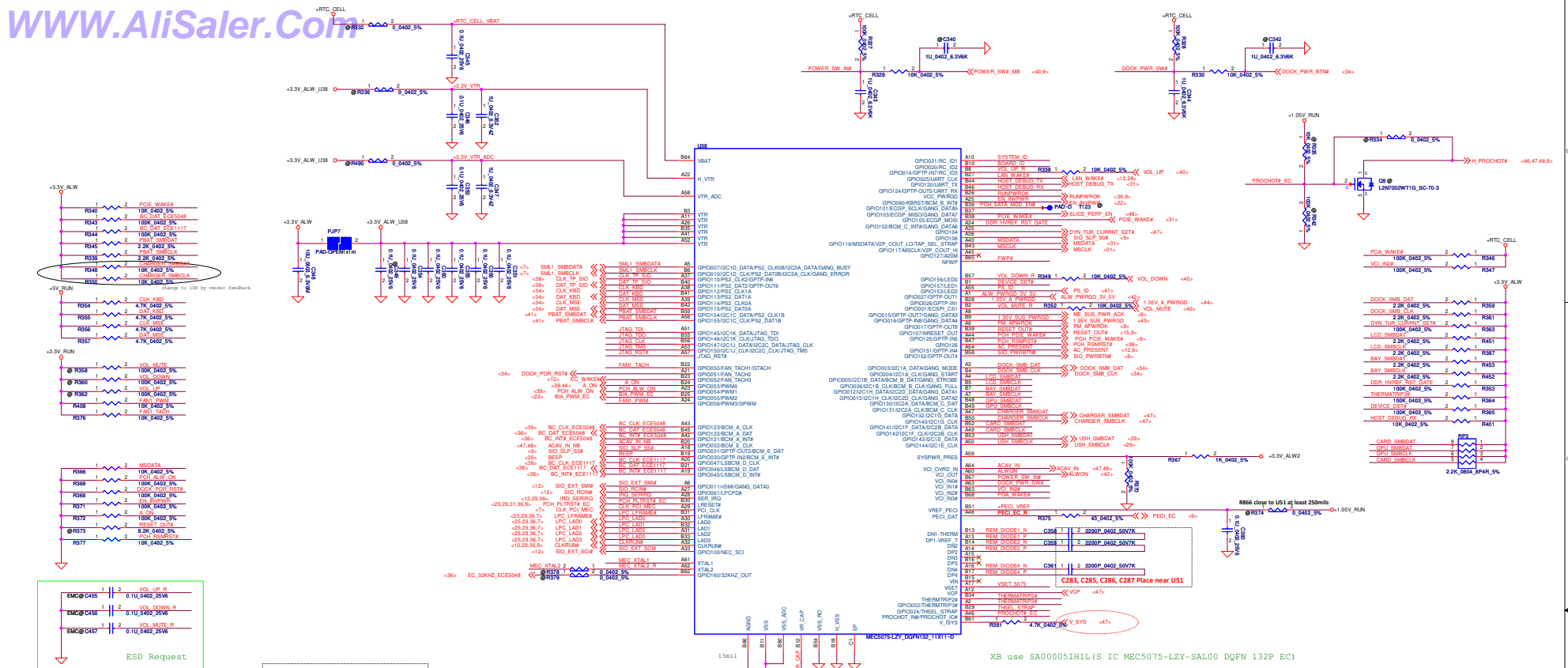
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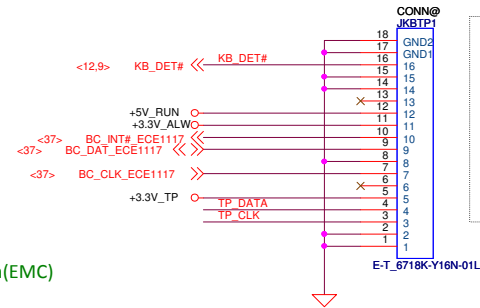
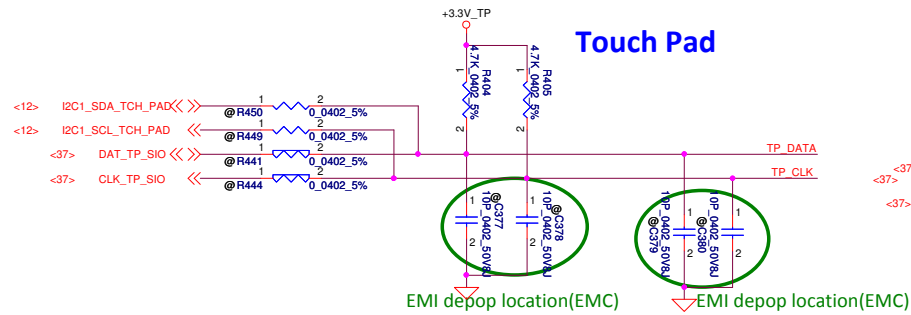
RJ45 and USBx1

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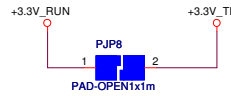
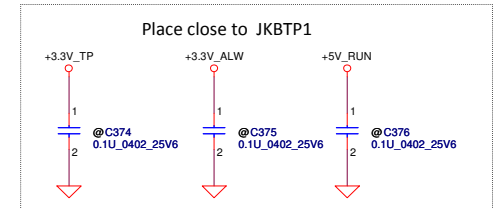
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ST change to 6718K-Y16N-01L



@eDP Cable (30P Normal)

Part Number	Description
DC02001PB00	H-CONN SET 0VM MB-EDP-LED-CAM

@eDP Cable (40P Touch Screen)

Part Number	Description
DC02001PA00	H-CONN SET 0VM MB-EDP-LED-CAM-TS

@Sniffer cable

Part Number	Description
DC02001PS00	H-CONN SET 0VM MB-SNIFFER

@TP_FFC

Part Number	Description
NBX0001CV00	FFC 16P F P0.5 PAD=0.3 104.4MM MB-KBTP

@FP_FFC

Part Number	Description
NBX0001CX00	FFC 6P G P0.5 PAD=0.3 86.4MM USH/B-FP

@USH_FFC

Part Number	Description
NBX0001CT00	FFC 20P G P0.5 PAD=0.3 33.5MM MB-USH/B

@NFC board_FFC

Part Number	Description
NBX0001CU00	FFC 15P F P0.5 PAD=0.3 56.01MM MB-NFC

@Media Board_FFC

Part Number	Description
NBX0001CS00	FFC 8P G P0.5 PAD=0.3 51.8MM MB-MEDIA/B

@SIM Board_FFC + Hall Sensor_FFC

Part Number	Description
NBX0001CR00	FFC 12P G P0.5 PAD=0.3 73.3MM MB-SIM+HALL/B

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

@Speak

Part Number	Description
PK230003Q0L	SPK PACK 2.1X 2.0W 4 OHM FG

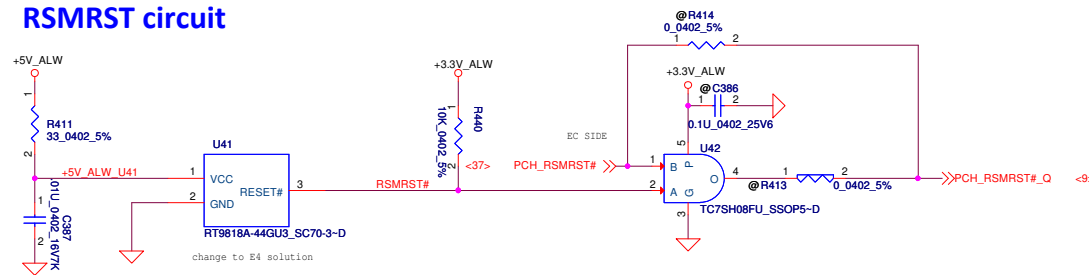
@Battery bridge cable

Part Number	Description
DC020014210	H-CONN SET 0PD H/B-BATTERY 9PIN

@UMA DC_IN wire cable

Part Number	Description
DC30100BN0	CONN SET 0PD DCJACK-MB WMDO-DCE30004-DF

RSMRST circuit



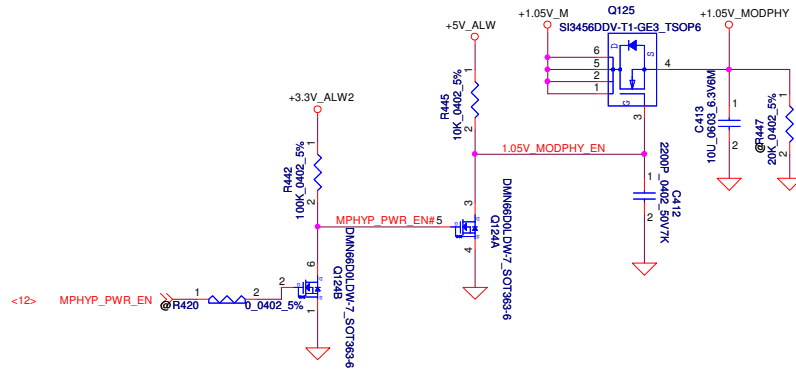
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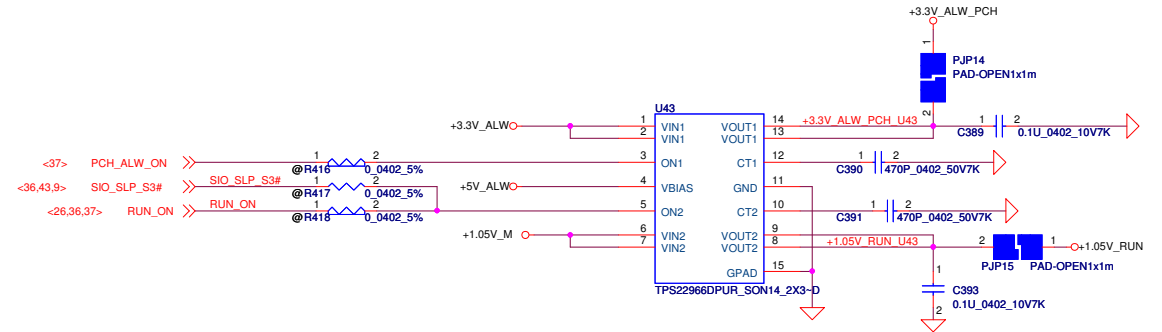
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KB/TP/RSMRST			
LA-9431P			
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+1.05V_MODPHY

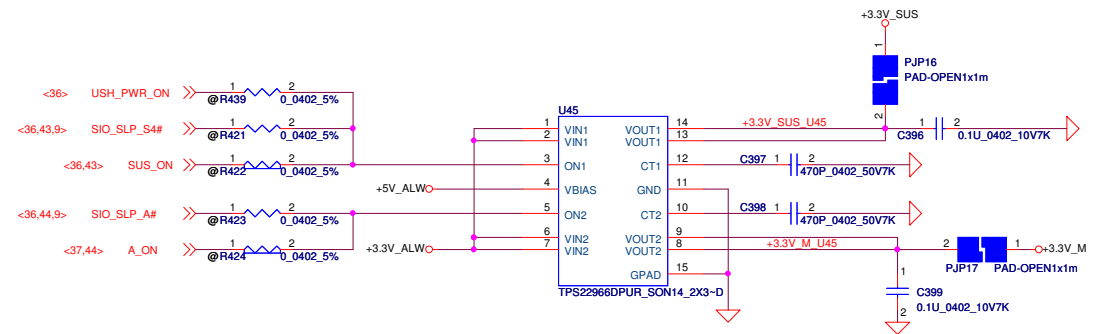


DC/DC Interface

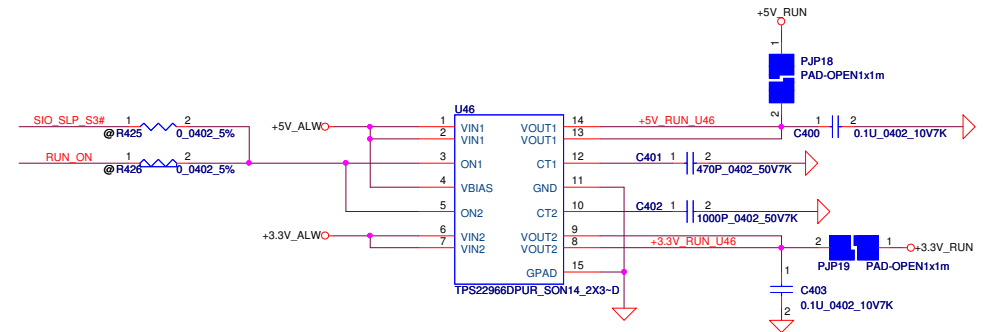
+3.3V_ALW_PCH/+1.05V_RUN source



+3.3V_SUS/+3.3V_M source



+3.3V_RUN/+5V_RUN source



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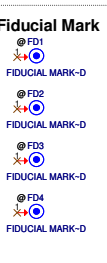
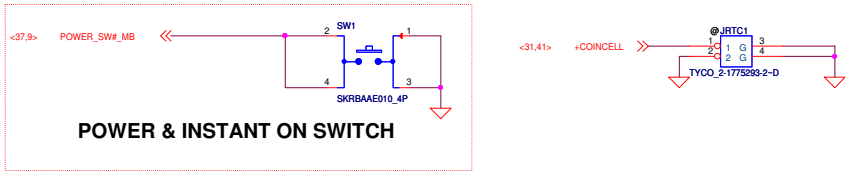
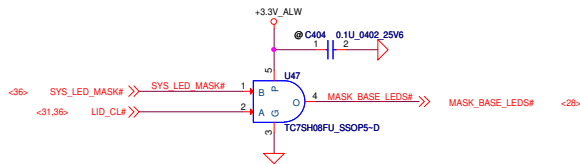
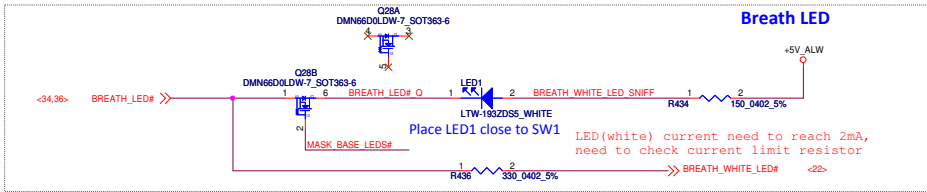
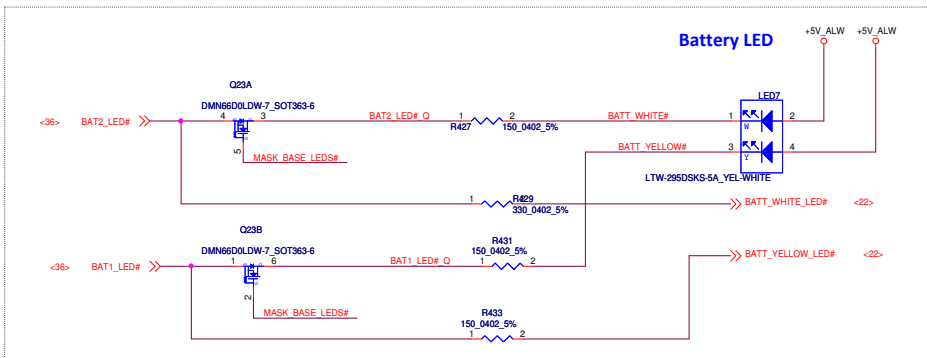
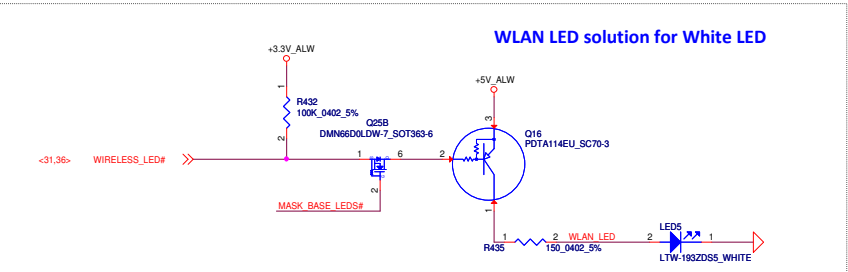
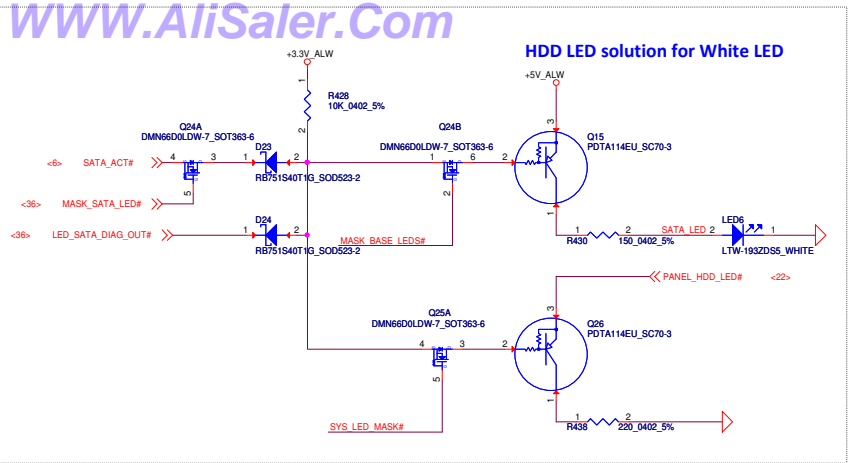
POWER CONTROL

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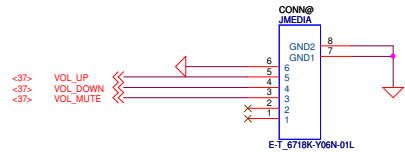
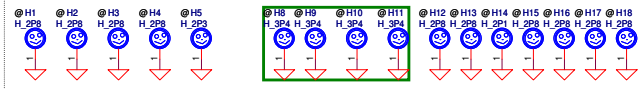
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



ST update symbol to 6718K-Y06N-01L

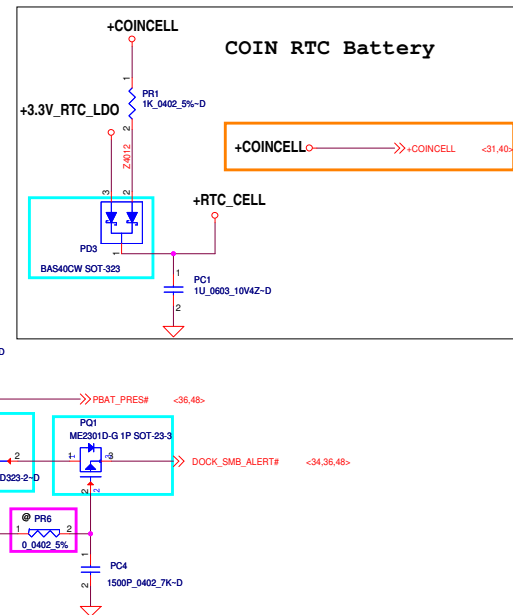
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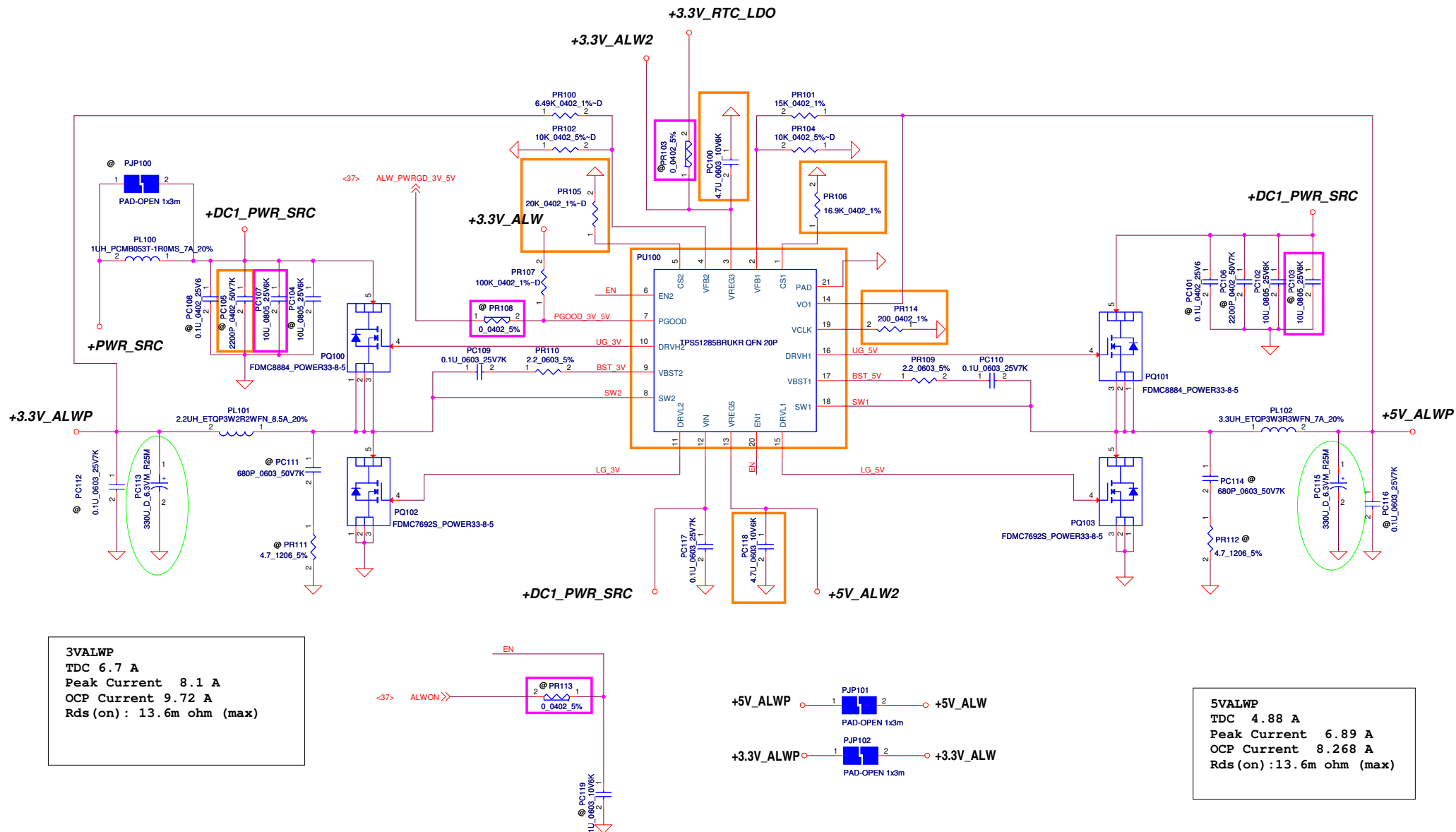
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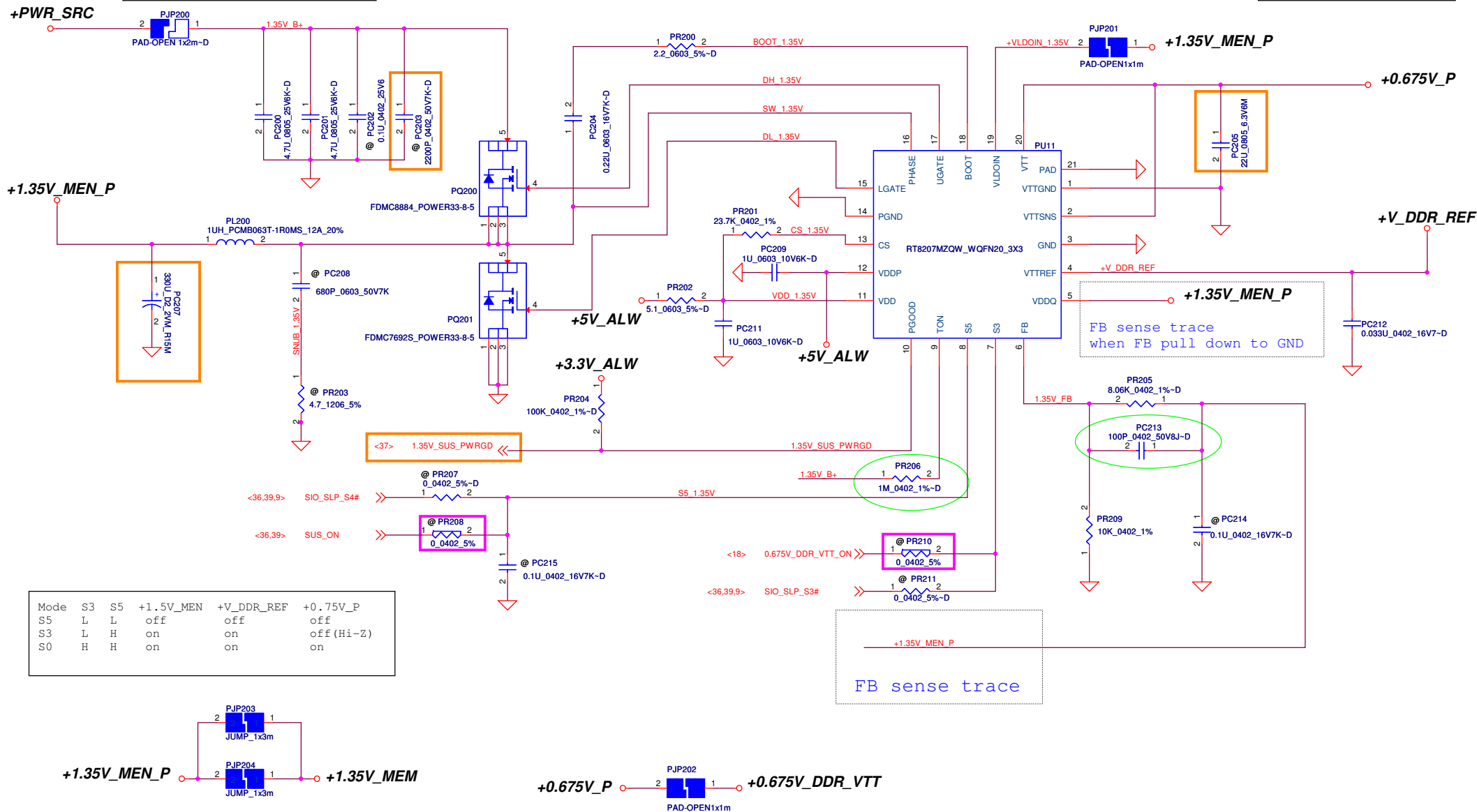


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1.35Volt +/- 5%
TDC: 7.2 A
Peak Current: 10 A
OCP current: 12 A
Rds(on) : 13.6m ohm(max)

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



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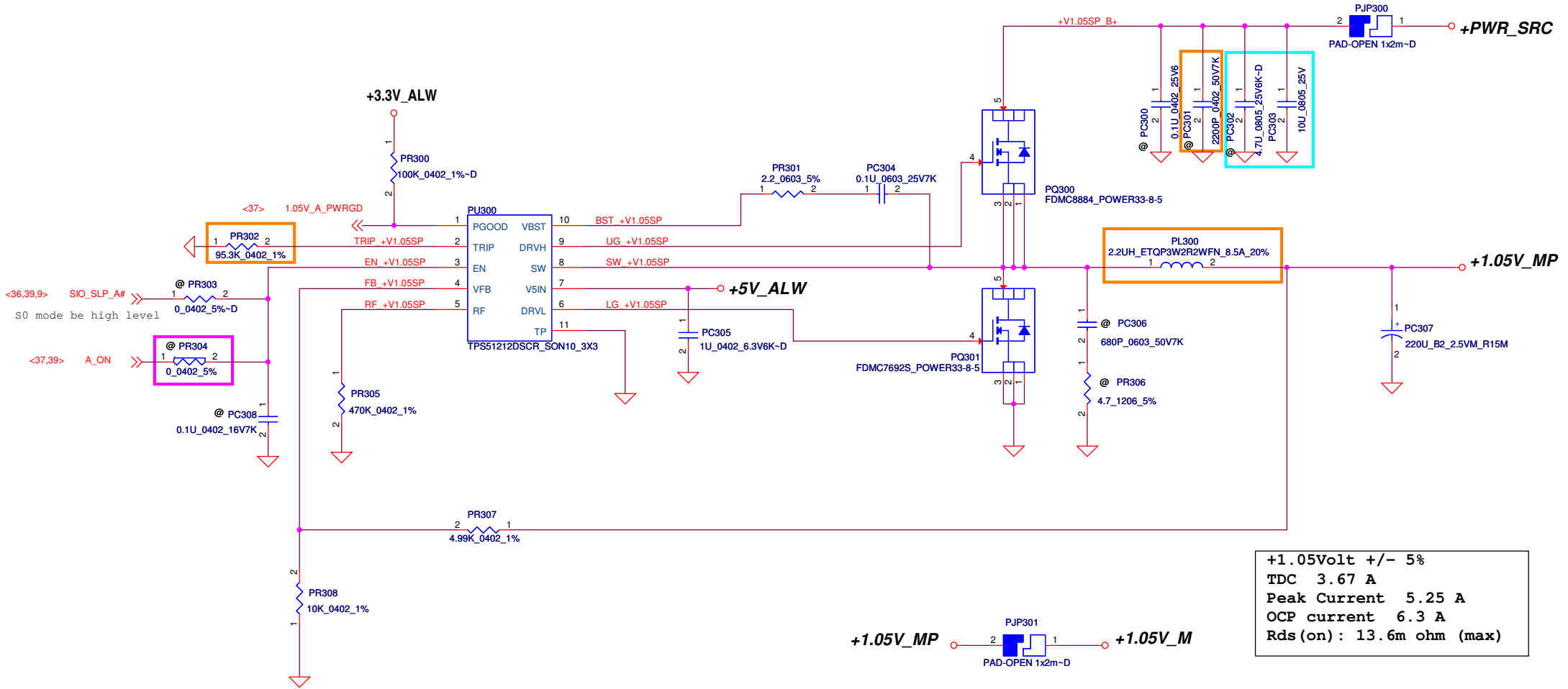
Title
+1.35V MEN/+0.675V DDR VTT

Size Document Number

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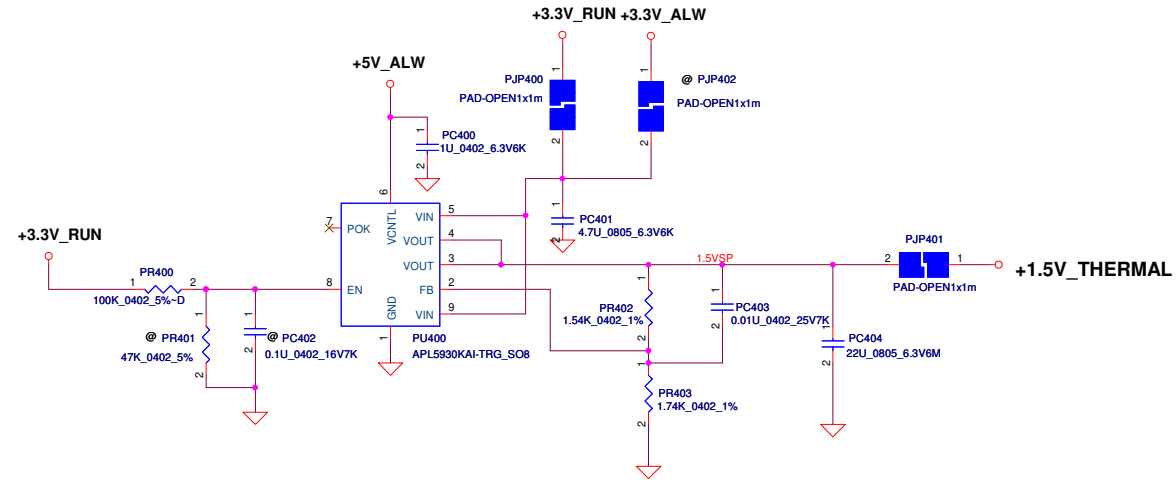
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				Chief River VC	
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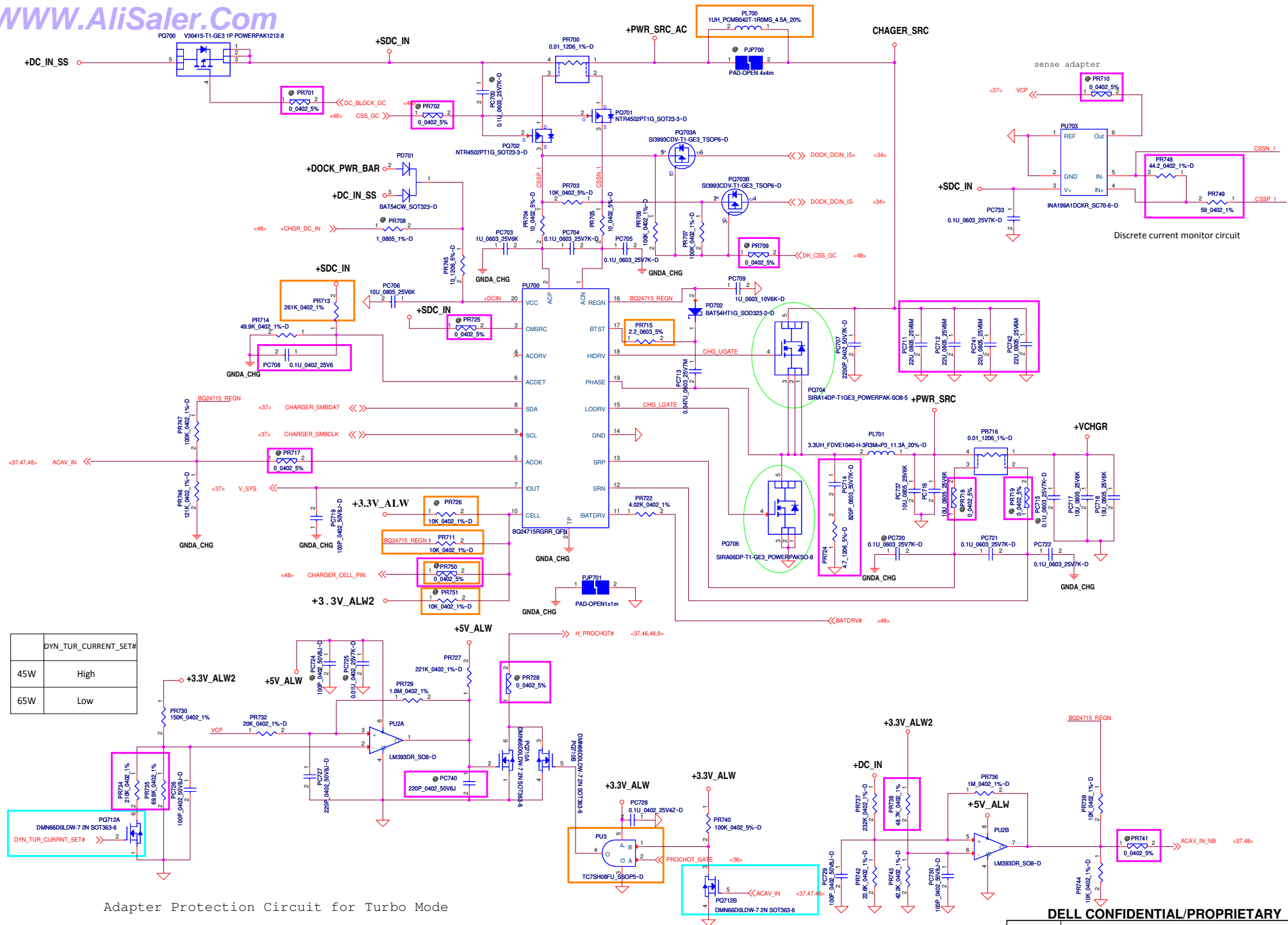
+VCC_CORE

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Adapter Protection Circuit for Turbo Mode

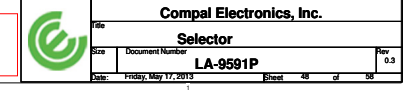
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+GPU CORE

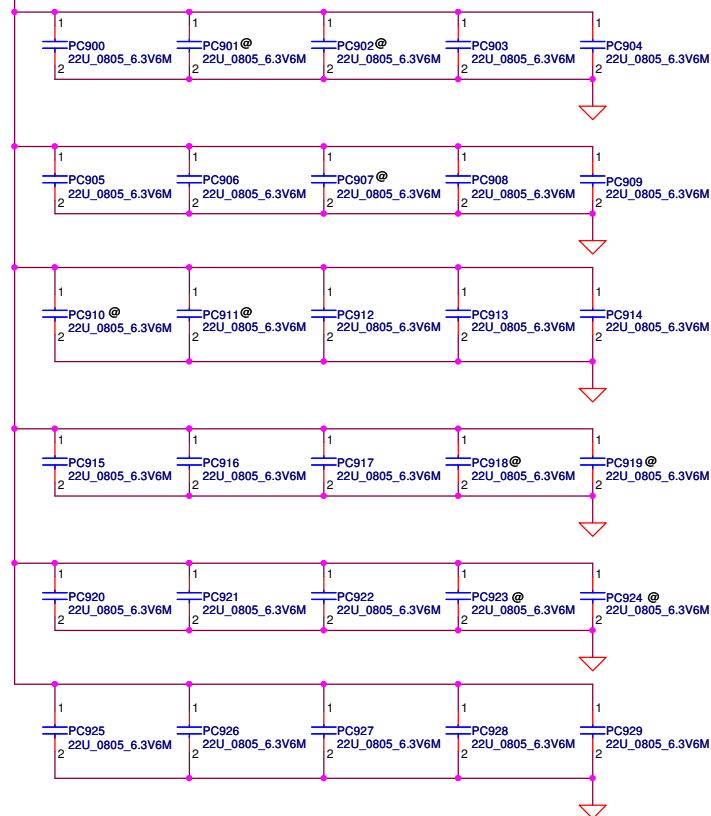
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Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

+VCC_CORE



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1	P45	1.5VSP	8/17	Compal	Base power budget request, add 1.5V powre rail	Add PU400	
2	P42	+5V/+3.3V	8/17	Compal	reserver PR114 for TPS51282 application	ADD @PR114	
3	P47	Charger	8/17	Compal	EC can't detect charger IC cause can't charger	modify SMBus net for correct connect	
4	P46	Vcore	8/17	Compal	schematic control error cause can't set OCP	add Vref net for correct connect	
5	P48	Selector	8/17	Compal	in order to meet latest multi-battery request	change control signal for meet E5 request	
6	P43	1.35V/0.675V	8/17	Compal	chagne OCP setting	change PR201 from 20k to 24.9k.	
7	P42	+5V/+3.3V	10/22	Compal	Reserve 0ohm for 3v5v enable debug	Change PR113 from SD03420018L (S RES 1/16W 2K +-1% 0402) to SD028000080 (S RES 1/16W 0 +-5% 0402)	X01
8	P44	+1.05V_MP	10/22	Compal	+1.05V_MP EA for ripple portion can't meet spec. 31.5mv, after change from 1u to 2.2u test is pass	Change PL300 from SH00000PJ00 (S COIL 1UH +-20% PCMB063T-1R0MS 12A) to SH00000MR00 (S COIL 2.2UH +-20% ETQP3W2R2WFN 8.5A)	X01
9	P42	+5V/+3.3V	10/22	Compal	Original 3v5v IC -TPS51225 can't support 2cell battery follow TI suggestion, When TPS51285A/B is used, please update the below four components. 1)VREG5 cap to 4.7uF 2)VREG3 cap to 4.7uF 3)CS1 resistor to 1/5 of the Tps51275's value 4)CS2 resistor to 1/5 of the Tps51275's value 5)VCLK connection (when not be used): add 200-ohm to GND	Change PU100 from SA00005LS00 (S IC TPS51225CRUKR QFN 20P PWM) to SA000064T00 (S IC TPS51285BRUKR QFN 20P PWM) 1)2)Change PC118(VREG5 Cap) and PC100(VREG3 Cap) from SE080105K80(S CER CAP 1U 10V K X5R 0603) to SE00000MA00(S CER CAP 4.7U 10V K X5R 0603) 3) Change PR106(for CS1) from SD03484528L (S RES 1/16W 84.5K +-1% 0402) to SD034169280 (S RES 1/16W 16.9K +-1% 0402) 4) Change PR105(for CS2) from SD03410038L (S RES 1/16W 100K +-1% 0402) to SD034200280 (S RES 1/16W 20K +-1% 0402) 5) Add PR114 SD034200080(S RES 1/16W 200 +-1% 0402)	X01
10	P47 P48	Charger Selector	10/22	Compal	To avoid HW and Power SMT materials can't entirely replace	Change PU3,PU801,PU804,PU805,PU806,PU807 from SA74108040L(S IC 74AHC1G08GW SOT353 AND) to SA00708012L(S IC TC7SH08FU SSOP 5P AND)	X01
11	P47	Charger	10/22	Compal	follow E5- Salado 14"15" schematic	1) @PQ819, @PQ824 2) EMI request for add PL700 SH00000IW00(S COIL 1UH +-20% PCMB042T-1R0MS 4.5A)	X01
12	P46	Vcore	11/02	Compal	follow TI suggestion modify setting value to meet Intel VR12.6(ULV) validation EA 1) Imon 2) Loadline 3) transient	1) Change PR501 from SD034422380 (S RES 1/16W 422K +-1% 0402) to SD034365380 (S RES 1/16W 365K +-1% 0402) 2) Change PR521 from SD000009M80 (S RES 1/16W 2.61K +-1% 0402) to SD00000WS8L(S RES 1/16W 2.32K +-1% 0402) 3) @PC506 100p_0402 and change PR535 from SD02810028L(S RES 1/16W 10K +-5% 0402) to SD034487100 (S RES 1/16W 4.87K +-1% 0402 (LF))	X01

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13	P47	Charger	11/05	Compal	1) TI suggestion BQ24715 cell pin pull high 3.3V change to V_regn(6v) for sequence issue 2) Reserve 0 ohm for debug	1) Change PR711 from SD02800008L (S RES 1/16W 0 +-5% 0402) to SD034100280 (S RES 1/16W 10K +-1% 0402), add PR750 SD028000080(S RES 1/16W 0 +-5% 0402) 2) Add @PR751	X01
14	P42	+5V/+3.3V	11/05	Compal	follow E5- Salado 14"15" schematic	1) @PR863, @PR870, @PR869, @PR824, @PR875, @PQ823 2) Add @PR848, @PR851 and add PR834, PR852, PR853, all is SD028000080(S RES 1/16W 0 +-5% 0402) 3) Add PR874 SD028100480(S RES 1/16W 1M +-5% 0402) 4) Add PD819 SCS0340L01L(S SCH DIO SDMK0340L-7 F SOD-323)	X01
15	P47	Charger	11/05	Compal	Improve charger efficiency	Change PR715 from SD028200A80 (S RES 1/16W 20 +-5% 0402) to SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	X01
16	P47	Charger	11/05	Compal	follow E5- Salado 14"15" schematic	Delete @PR731, @PR733, @PU702	X01
17	P44	+1.05VTTP	11/05	Compal -QAD team -Huang.Hanks (PCP)	Support QAD WCEPTA analysis, to modify 1.05 OCP Rtrip resistance to 95K, Cpk value will pass specification.	Change PR302 from SD00000H880 (S RES 1/16W 54.9K +-1% 0402) to SD034953280 (S RES 1/16W 95.3K +-1% 0402)	X01
18	P48	+5V/+3.3V 1.35V/0.675V +1.05V_MP	11/05	Compal - EMC team Wen. Andy	EMC team suggestion	@PC105, @PC203, @PC301	X01
19	P48	Selector	11/15	Compal	follow E5- Salado 14"15" schematic for undock shutdown issue	Add PQ827 SB00000U000 (S TR DMN65D8LW-7 1N SOT323-3), @PR856 SD028000080 (S RES 1/16W 0 +-5% 0402), PQ816 SB534020000 (S TR AO3402 1N SOT-23), PQ828 SB00000U000 (S TR DMN65D8LW-7 1N SOT323-3), PR861 SD028000080 (S RES 1/16W 0 +-5% 0402) PR802, PR827, PR840 change from SD028240380 (S RES 1/16W 240K +-5% 0402) to SD028470280 (S RES 1/16W 47K +-5% 0402), PR804, PR826, PR839 change from SD028470280 (S RES 1/16W 47K +-5% 0402), to SD028240380 (S RES 1/16W 240K +-5% 0402)	X01
20	P47 P48	Charger Selector	12/12	Compal		Change PR713 from SD034294380 (S RES 1/16W 294K +-1% 0402) to SD034261380 (S RES 1/16W 261K +-1% 0402) @PR844	X01
21	P41	+DCIN	2013 /01/11	Compal- ESD team	ESD team's PD1 vendor(NXP) proposal PD1 pin 5 connected to the VCC (5V or 3.3V).	PD1 pin5 connect to +3.3V_ALW	X01_2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	P48	Selector	2013/ 01/23	Compal	To avoid +DOCK_PWR_BAR leakage voltage when system only with main battery	1). Add PU808 P/N: SA007080120 (S IC TC7SH08FU SSOP 5P AND) 2). Add PQ830 P/N: SB0000007900 (S TR NTR4502PT1G 1P SOT23-3) 3). Add PQ831 P/N: SB000000U000 (S TR DMN65D8LW-7 1N SOT323-3) 4). Add PD821 P/N: SCS0340L010 (S SCH DIO SDMK0340L-7-F SOD-323) 5). Add PR836, PR837 P/N: SD028100380 (S RES 1/16W 100K +-5% 0402) 6). Add PC814 P/N: SE102104K00 (S CER CAP 0.1U 10V +-10% X7R 0402)	X01_2
23	P41	+DCIN	2013 /02/07	Compal	PPM-Jovins_Chang and Sourcer-Willie_Zeng highlight SB000009N8L will shortage after 2013/05	Change PQ6 From : SB000009N8L (S TR IMD2AT-108 PNP/NPN SC74-62) To : SB000009P80 (TR DCX124EK-7-F PNP/NPN SC74R-6)	X02
24	P48	Selector	2013/ 02/18	Compal	GPIO net - AC_DIS# is high active. Corrent net name. AC_DIS circuit modify to improve output voltage level.	1). Change PQ6A.5 and PR828.1 net name from AC_DIS# to AC_DIS 2). Add PQ829 P/N: SB000000H500 (S TR SI2301CDS-T1-GE3 1P SOT23-3) , PQ832 P/N: SB000000U000 (S TR DMN65D8LW-7 1N SOT323-3) , PD820 P/N: SCS0340L010 (S SCH DIO SDMK0340L-7-F SOD-323) , @PR894 , PR895 P/N: SD028000080 (S RES 1/16W 0 +-5% 0402) 3). modify PR828, PR830 4). Delete PQ820 5). Delete PL5, add PJP1	X02
25	P41	+DCIN	2013/ 02/18	Compal-ME	DFX highlight Battery connetor (locattion:PBATT1) hard to insert.	Battery connetor (locattion:PBATT1) footprint follow ME team Iris requesti to change from SUYIN_200277GR009M262ZR_9P-T to ALLTO_C144LS-109A9-L_9P-T	X02
26	P48	Selector	2013/ 02/18	Compal	layout spec limit	Delete PD817, modify PD815 footprint same as PD701, from SDMK0340L-7-F_SOD323-2 to RB717F_SOT323-3	X02
27	P46 P48	Vcore Selector	2013/ 02/18	Compal- ESD team Hsu. Matt	Add snubber component by ESD team request	Add PC508, PC714 P/N: SE025821K80 (S CER CAP 820P 50V K X7R 0603) PR522, PR724 P/N: SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
28	P48	Selector	2013/ 02/21	Compal	follow E5- Salado 14"15" schematic 1) For Input current sense stablilze 2) To provent charger into sleep mode dual AC transient. 3) Fine tune ACOK response time. 4) Adapter protect rating setting 5) Fine tune H_PROCHOT# response time. 6) Improve ACAV_IN_NB ref voltage accuracy. 7) Improve current sense accuracy.	1). Change PC703 from 0.1U to 1U P/N: SE000006900 (S CER CAP 1UF 25V K X5R 0603) 2). Change PC706 from 1U to 0.1U P/N: SE00000QK00 (S CER CAP 10U 25V K X5R 0805 H1.25) 3). Change PC708 from 0.01U to 10U P/N: SE00000G880 (S CER CAP 0.1U 25V K X5R 0402) 4). Change PR734 from 100K ohm to 210K ohm P/N: SD034210380 (S RES 1/16W 210K +-1% 0402) Change PR735 from 46.4K ohm to 69.8K ohm P/N: SD034698280 (S RES 1/16W 69.8K +-1% 0402) 5). Add @PC740 6). Change PR738.pin1 from BQ24715_REGN connect to +3.3V_ALW2. Change PR738 from 118K ohm to 48.7K ohm P/N: SD034487280 (S RES 1/16W 48.7K +-1% 0402) Change PR744 from 12K ohm to 10K ohm P/N: SD034100280 (S RES 1/16W 10K +-1% 7). Change PR748 from 6.8 ohm to 210K ohm P/N: SD034442A80 (S RES 1/16W 44.2 +-1% 0402) Change PR749 from 10 ohm to 69.8K ohm P/N: SD00000W200 (S RES 1/16W 59 +-1% 0402)	X02
29	P46	Vcore	2013/ 02/26	Compal- ESD team Hsu. Matt	Add 22U_0805 by ESD team request	Change PC732, PC736 from 10U to 22U from P/N: SE00000QK00 (S CER CAP 10U 25V K X5R 0805 H1.25) to P/N: SE00000XH80 (S CER CAP 22U 25V M X5R 0805 H1.25)	X02
30	P48	Selector	2013/ 02/27	Compal	Modify resistor value to meet voltage tolerance	1). Change PR802,PR827,PR840 from 47K ohm to 100K P/N: SD028100380 (S RES 1/16W 100K +-5% 0402) 2). Change PR804,PR826,PR839 from 240K to 100K P/N: SD028100380 (S RES 1/16W 100K +-5% 0402)	X02
31	P47	Charger	2013/ 03/18	Compal	follow E5- Salado 14"15" schematic to add charger input MLCC to 88u	1). Add PC741, PC742 P/N: SE00000XH80 (S CER CAP 22U 25V M X5R 0805 H1.25) 2). Due to space limit, so delete @PC701, @PC702, @PC710	X02_1
32	P42 P43 P44	+5V/+3.3V 1.35V/0.675V +1.05V_MP	2013/ 03/20	Compal	support DFX team change choke layout pad to avoid soldering issue	1). Change PL101, PL102, PL200, PL300 PCB FootPrint change from CYNTE_PCMC063T-2R2MN_2P to CYNTE_PCMB064T-3R3MS_2P	X02_1
33	P46	Vcore	2013/ 03/21	Compal	Support acoustic team to reduce noise	3). Change PC738 from 33U(SGA00005M00) to 100U P/N: SGA00008R00 (S POLY C 100U 20V M D ESR55M (D3L_H=2.8mm)	X02_1
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1	22, 40, 38, 26, 34	ESD	11/05/2012	COMPAL	ESD team request	Remove D3, D27, D22, DE1, DE2 Reserve D20	0.2 (X01)
2	27	Safty	11/05/2012	COMPAL	Safty team request	Pop F2 and reserve R160	0.2 (X01)
3	37	HW	11/05/2012	COMPAL	Based on align E5, P5 Fan module pin define	Swap JFAN1 pin define	0.2 (X01)
4	22, 40, 38, 26	HW	11/06/2012	COMPAL	To avoid PT phase occurs ESD issue and change back ESD request	Reserve D3, D27, D22, DE1, DE2	0.2 (X01)
5	40 36	HW	11/08/2012	DELL	DELL drop Media LED function	Remove backlight LED function and change connector to 6pin	0.2 (X01)
6	26	HW	11/09/2012	COMPAL	Remove EMI solution at Speaker side	Remove R132, R133, R134 and R135	0.2 (X01)
7	12, 22, 37	HW	11/09/2012	DELL	DELL drop ALS function	Remove ALS interface from EC and CPU side than move touch screen signal to eDP side	0.2 (X01)
8	22	HW	11/09/2012	COMPAL	change Webcam power enable from PCH	pop R106 and de-pop R102	0.2 (X01)
9	10	HW	11/09/2012	COMPAL	Schmatic error and remove eDP backlight control pull up resistor	Remove RC150	0.2 (X01)
10	39	HW	11/12/2012	COMPAL	+1.05V_MODPHY can't meet INTEL timing spec	change +1.05V_MODPHY to MOS solution	0.2 (X01)
11	18 19	HW	11/12/2012	COMPAL	Remove DIMM VREF power rail from power side	Remove RD2, RD4, RD8 and RD9	0.2 (X01)
12	27	HW	11/12/2012	COMPAL	change miniDP OCP solution	remove D10 R160 F2 and add U50 de-pop C383	0.2 (X01)
13	26	HW	11/12/2012	COMPAL	refer salado 14" to change PCBEEP circuit	remove C132, C146, R146, R138, C133 and C143 than add C145, C146, R147, R151 and de-pop R194 R153	0.2 (X01)
14	26	HW	11/12/2012	COMPAL	If doesn't has external power, Sleeve will be floating mode and no reference GND.	Add AUD_NB_MUTE# to control Sleeve pin.	0.2 (X01)
15	37	HW	11/12/2012	COMPAL	Change board ID to X01	change R392 form 240K to 130Kohm	0.2 (X01)
16	21	HW	11/12/2012	COMPAL	Vendor update schematic for power saving	change +1.05V_RUN_VMM power enable signal from LP_EN to DOCKED and add +3.3V_RUN_VMM for DP2320 series 3.3V power rail remove L3 and move U6.E5 to +1.05V_VMM_VDD power rail change U6.J4 to +3.3V_RUN_VDDA R85 change to 3.74K_1% remove LP_EN, R232 and U6A.A5 to NC remove R55 and pop-option R207 when use VMM2310	0.2 (X01)
17	21	HW	11/12/2012	COMPAL	change VMM2320 config	remove DP to VGA PTN3392 circuit and add 0ohm pop option for 2320 config	0.2 (X01)
18	22	HW	11/13/2012	COMPAL	Add Mic power and remove DBC function	Add 3.3V_RUN for Mic power and remove DBC function at JeDP.2	0.2 (X01)
19	19	HW	11/13/2012	COMPAL	refer PDG1.0 to change SODIMM control circuit resistor	change RC68, RC126 and RC173 from 2.2 to 2ohm 1% change RC67, RC69, RC130, RC132, RC217 and RC221 from 1.82K to 1.8Kohm 1%	0.2 (X01)
20	37, 36, 12	HW	11/13/2012	COMPAL	GPIO map update to 2.7 version	Move EC_WAKE# from ECE5048[L]5 to MEC5075 GPIO52. Change name: 1.5V_SUS_PWRGD to 1.35V_SUS_PWRGD for DDR3L. Add NFC_DET# ECE5048 GPIOL[5] to NFC moudle & add R38 PU	0.2 (X01)
21	20, 27, 29, 38, 40	ME	11/13/2012	COMPAL	ME change connector	change JmdP1, JNFC1, JMEDIA, JKBTP1, JUSH1	0.2 (X01)
22	24	HW	11/14/2012	COMPAL	Vendor update schematic for power saving	align AUX/DDC SW voltage with DP Hub to +3.3V_RUN_VMM	0.2 (X01)

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23	2, 3, 6, 34	HW	11/15/2012	COMPAL	update SATA topology fro Mainstream CPU	exchange SATA1&SATA2 topology	0.2 (X01)
24	12	HW	11/15/2012	COMPAL	Add LAN_WAKE# T-topology	Pop RC301 to link LAN_WAKE# and EC_WAKE#	0.2 (X01)
25	15	HW	11/15/2012	COMPAL	remove RC252 for cost saving	change RC252 to PJP11(1mm jumper-short)	0.2 (X01)
26	16	HW	11/15/2012	INTEL	MOW_WW46 request change for VCCUSB3PLL and VCCSATA3PLL	change CC42 and CC49 from 1u_0402 to 22u_0603 change CC76 and CC77 from 100u_1206 to 22u_0603	0.2 (X01)
27	20, 28, 30, 31	HW	11/15/2012	COMPAL	change AND gate to same source	Change U20, U26, U29 and U30 from SA74108040L to SA00708012L	0.2 (X01)
28	34	ME	11/15/2012	COMPAL	ME change Docking connector	change JDOCK1 that Pin145 from PWR1 to GND1 & Pin148 from PWR2 to GND2	0.2 (X01)
29	38, 12	HW	11/15/2012	COMPAL	remove +3.3V_TP power load switch solution	remove U40, R458, C424 and C423	0.2 (X01)
30	22	HW	11/15/2012	COMPAL	change LCDVDD power control circuit	change U9 from TPS22966 to APL3512 solution	0.2 (X01)
31	31, 32	HW	11/15/2012	COMPAL	remove TPS22965 solution	remove U51(TPS22965) and U34(TPS22965) than add U3(TPS22966)	0.2 (X01)
32	10, 27	HW	11/15/2012	COMPAL	ESD solution for black screen issue	Add CC450 on EDP_CPU_HPD to GND and C451 on DPC_HPD to GND	0.2 (X01)
33	40	ME	11/16/2012	COMPAL	ME change drawing	Add H18 and H10, H11 change size from 2.3 to 3.4 , H5 change size from 2.8 to 2.3	0.2 (X01)
34	22	HW	11/16/2012	COMPAL	change diode to daul-diode fro cost saving	remove D4, D5, D6, D7 and add D10, D21	0.2 (X01)
35	40	ME	11/16/2012	COMPAL	ME request	change SW1 to SKRBAAE010	0.2 (X01)
36	30	ME	11/16/2012	COMPAL	ME change connector	change SD1	0.2 (X01)
37	21, 26, 28, 31, 39	HW	11/16/2012	COMPAL	For EA rework request	Add PJP12~25 for +1.05V_RUN_VMM, +3.3V_RUN_VMM, +3.3V_ALW_PCH, +1.05V_RUN, +3.3V_SUS, +3.3V_M, +5V_RUN, +3.3V_RUN, +3.3V_LAN, +3.3V_mSATA_WWAN, +3.3V_HDD, +3.3V_WLAN, +5V_RUN_AUDIO, +3.3V_RUN_AUDIO	0.2 (X01)
38	37	HW	11/19/2012	COMPAL	change thermal diode for cost saving	change Q11, Q13 and Q14 form SB000008P0L to SB33904510L	0.2 (X01)
39	38, 26, 30, 22	HW	11/19/2012	COMPAL	change Bead for cost reduce	change L44 and L45 from SM01000558L to SM01000C500 change L35 and L36 from SM01000AM0L to SM01000C500 change LE1 from SM01000DH0L to SM01000BV00 change L21 from SM01001788L to SM010005N00	0.2 (X01)
40	9	HW	11/19/2012	COMPAL	change APS pin 11 net name for DELL APS debug	Change JAPS1.11 net name from SIO_PWRBTN# to POWER_SW#_MB	0.2 (X01)
41	12, 28	HW	11/19/2012	COMPAL	support TLS confidentiality	change net name from HOST_ALERT1_R_N to PCH_GPIO15, and pop RC190 remove R188	0.2 (X01)
42	37	HW	11/19/2012	COMPAL	change thermal OTP to 98 degree	change R394 from 1.24K to 1.82K 1%	0.2 (X01)
43	31	HW	11/20/2012	COMPAL	Intel notice remove HDD_DEVSLP function on WWAN JMINI port	remove HDD_DEVSLP from JMINI2.44 de pop HDD_DEVSLP pull up resistor R155	0.2 (X01)
44	28	HW	11/20/2012	COMPAL	LOM LED issue	reverse Q32, Q33 of C & D gate	0.2 (X01)
45	22	HW	11/20/2012	COMPAL	ME change connector	change JLED1	0.2 (X01)
46	35	HW	11/21/2012	COMPAL	Align EMI part	change L54 pat to DLW21SN900SQ2L that same with L42, L39	0.2 (X01)
47	15	HW	11/22/2012	COMPAL	Per Intel CRB updated	change VCCST_PWRGD pull high value from 10K ohm to 1K ohm	0.2 (X01)
48	26	HW	11/22/2012	COMPAL	Universal Jack no longer supported on X5	Remove D9, D11, R209, R210, C195, C196, R198, R199	0.2 (X01)
49	6, 12, 25, 31	HW	11/26/2012	DELL	For support DEVSLP on WWAN JMINI2 & mSATA JMINI3	SATA HDD change from port0 to port1, and connect HDD_DEVSLP Dock change from port1 to port2, and connect mSATA_DEVSLP	0.2 (X01)

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50	21, 26	HW	11/26/2012	COMPAL	change Bead for cost reduce	L6 and L7 from SM01000GG0L to BLM15PX471SN1D(SM01000M700) L22, L23, L24 and L25 from SM010028800 to BLM15PX121SN1D(SM01000L300)	0.2(X01)
51	31	HW	11/26/2012	COMPAL	change WWAN power control signal	Change U3.5 from 3.3_1.5V_WLAN_E to SIO_SLP_WLAN#	0.2(X01)
52	12, 36	HW	11/27/2012	COMPAL	NFC_DET# change to PCH side GPIO59	UC1.AT5 change from PCH_GPIO59 to NFC_DET# U37.B1 change to NC	0.2(X01)
53	22, 26, 38, 40	HW	11/27/2012	COMPAL	Remove ESD reserve location	Per ESD experiment, D3,D27,D22,DE1,DE2 can be remove	0.2(X01)
54	33	HW	11/27/2012	COMPAL	Per USB2.0 EA result	Change U42 from SM01002080L(DLW21SN900SQ2L) to SM070001600(OCE2012120YZF)	0.2(X01)
55	6, 12, 25, 31	HW	11/27/2012	DELL	Per Dell request, only JMINI3(mSATA) support DEVSLP	SATA HDD use port0 ,Dock use port1	0.2(X01)
56	31	HW	11/28/2012	COMPAL	change +3.3V_WLAN PWR control	change +3.3V_WLAN PWR control from SIO_SLP_WLAN# to AUX_EN_WOWL	0.2(X01)
57	28	HW	11/28/2012	COMPAL	change +3.3V_mSATA_WWAN control	change +3.3V_mSATA_WWAN control from WWAN_mSATA_EN to MCARD_WWAN_PWREN	0.2(X01)
58	34	HW	11/28/2012	COMPAL	For EMI request, change to 33 ohm for docking DVI noise	R252/R253/R254/R255/R256/R257/R258/R259/R260/ R261/R262/R263/R264/R265/R266/R267 change to 33ohm from 0 ohm	0.2(X01)
59	21	HW	11/28/2012	COMPAL	For use IDT2320, need change EEPROM PN	U7 change from SA00003FL10(W25X10BVSNI) to SA00006HH00(W25X10CLSNI)	0.2(X01)
60	22	HW	11/28/2012	COMPAL	change Bead for cost reduce	LE1 change from SM01000DH0L(BLM18BB221SN1D)to SM01000BV00(BLM15BB221SN1D)	0.2(X01)
61	6, 25, 31	HW	11/29/2012	DELL	To support mainstream and Premium CPU, change to SATA port assignment.	SATA HDD change from port0 to port1, and connect HDD_DEVSLP Dock change from port1 to port0, and connect mSATA_DEVSLP	0.2(X01)
62	12, 31, 34	HW	11/29/2012	DELL	To support the SATA DevSLP function for new SATA port assignment.	Change DEVSLP0/GPIO33 to mSATA_DEVSLP and DEVSLP1 to HDD_DEVSLP	0.2(X01)
63	33	HW	01/10/2013	COMPAL	For USB3.0 EA result	L37 & L38 change to SM070000880(S COM FI CHENG HANN WCM2012F2SF-670T04)	0.3(X02)
64	40	HW	01/10/2013	COMPAL	For ME team force test result	SW1 change to SN111005800(S TACK SW BCL31 SKRBAAE010 SPST)	0.3(X02)
65	9	HW	01/17/2013	COMPAL	For U42 2nd source (MC74VHC1G08DFT2G) can't boot issue	PCH_RSMRST#_R add RC136 10K pull down	0.3(X02)
66	28	HW	01/17/2013	COMPAL	For meet INTEL LAN SPEC	Y3 change to SJ10000JC00(S CRYSTAL 25MHZ 18PF +-30PPM 7V25000034)	0.3(X02)
67	22	HW	01/17/2013	COMPAL	For trial run U9 2nd source	U9 pin 4 & pin5 connect to +3.3V_ALW	0.3(X02)
68	40	HW	01/17/2013	COMPAL	For LED light test result	1.change R435 from 1.8k to 150(SD028150080) 2.R430/R438/R436 from 2.2k to 150(SD028150080) 3.R434 change from 220 to 150(SD028150080) 4.R427 change from 1K to 150 ohm(SD028150080) 5.R429 change from 620 to 330 ohm(SD028330080) 6.R431/R433 change from 330 to150 ohm(SD028150080)	0.3(X02)
69	22	HW	01/17/2013	COMPAL	For prevent EDP pin shift then cause broken issue	1. modify JEDP1 pin assignment 2. pin 29 (IO_LOOP) add 1k pull down	0.3(X02)

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70	25, 26	HW	12/05/2012	COMPAL	For Audio Presison result	1.L22/L23/L24/L25 change to SM010019400 from SM01000L300 2.L51/L52 change to SM01000FV00 from SM01000AM0L 3.Delete L50/L53 & add R491/R492 0 ohm-short	0.3 (X02)
71	37	HW	12/07/2012	COMPAL	Change Board ID for ST	R392 change to 33K ohm from 130k ohm	0.3 (X02)
72		HW	02/19/2012	COMPAL	Change connector tyoe	1. JNFC1 change to 6718K-Y15N-01L 2. JKBTP1 change to 6718K-Y16N-01L 3. JUSH1 change to 6718K-Y20N-00L 4. JUSB3 change to PUBAUE-09FLBS1FF4H0 5.JMEDIA change to 6718K-Y06N-01L 6. SH1 change to 6718K-Y12N-01L	0.3 (X02)
73	37	HW	02/21/2012	COMPAL	For OTP issue, & change OTP to 96 degree from 98 degree	1. Q11/Q13/Q14 change to SB000008P00(S TR MMBT3904WT1G NPN SC70-3) from SB33904510L(S TR PMST3904 NPN SOT323-3) 2. R394 chagne to SD00000SJ80(S RES 1/16W 1.58K +-1% 0402) from SD034182180(S RES 1/16W 1.82K +-1% 0402)	0.3 (X02)
74	7	HW	02/21/2012	COMPAL	change JTAA1 connector type	JTAA1 change to PANAS_AKK820145WG from ACES_50185_02041_001	0.3 (X02)
75	38	HW	02/21/2012	COMPAL	Per EMI Test result	Remove L44 & L45	0.3 (X02)
76	38	HW	02/21/2012	COMPAL	Per ESD Test result	Pop C141 & C142 & C143	0.3 (X02)
77	9	HW	02/21/2012	COMPAL	add XDP@ for XDP component	change XDP circuit to XDP@	0.3 (X02)
78	9	HW	02/21/2012	COMPAL	update XDP circuit for INTEL ITE can't boot	remove RC121 and pop RC102	0.3 (X02)
79	9, 11, 35	HW	02/21/2012	COMPAL	Fixed 2 USB Port use the same OC# signal issue	1.change JUSB3 OC# from USB_OC0# to USB_OC1# 2.change USB_OC1#/3# to USB_OC1#, USB_OC3# and add RC166 for OC1# pull up resistor	0.3 (X02)
80	9, 11, 35	HW	02/21/2012	COMPAL	Add jumper for clock buffer co layout	add PJP26, PJP27 and PJP28 beween UC5	0.3 (X02)
81	33	HW	02/21/2013	COMPAL	Per EMI test result	1.L42 change to SM070003N00(CHILISIN CMM0805-20Y-N)from SM070001600 (SUPERWORLD OCE2012120YZF) 2.L37/L38 change to SM070001R00(MURATA DLW21SN670HQ2L) from SM070001E0L(MURATA DLW21SN900HQ2L) 3.L8/L39/L54 change to SM070001N00(MURATA DLW21HN900SQ2L)from SM01002080L(MURATA DLW21SN900SQ2L)	0.3 (X02)
82	33	HW	02/22/2013	COMPAL	Per ESD test result	1. Pop CC71 & CC72 & CC73 2. Add C452 & C453 & C454(@) 22uF 0603 size 3. R338 & R349 & R352 change to 10k ohm from 1k ohm 4. Add C455 & C456 & C457 0.1UF	0.3 (X02)
83	9, 12	HW	02/25/2013	COMPAL	For LID & AOAC S3 wake up issue	Change Net name to SIO_EXT_SMI# from USB_OC3# and change to PCH_GPIO45 from SIO_EXT_SMI#	0.3 (X02)

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84	7	HW	02/25/2013	COMPAL	add RF noise solution at clock buffer	1. add CC86~CC90 between clock signal 2. add RC62 for UC5 power rail 3. change RC100 from 0ohm short to 10ohm 4. change UC5 from IDT_5V60034DCG8 to CYPRESS_CY2304SXI-1T	0.3 (X02)
85	23	HW	02/25/2013	COMPAL	refer INTEL MOW to upfate HDMI cost reduce level shifter main link	change R462~R469 resistor from 680(SD034680080) to 470ohm(SD034470080)	0.3 (X02)
86	33	HW	02/25/2013	COMPAL	change USB charge solution for SAMSUNG phone	change U39 from SA00004VH00 to SA00006L600	0.3 (X02)
87	26	HW	02/27/2013	COMPAL	for Fixed BIOS fliah HOTSOS issue	change R154 from PCH_AUDIO_EN to RUN_ON	0.3 (X02)
88	9	HW	02/28/2013	COMPAL	For ESD request	Add CC149(0) on H_PROCHOT# near CPU side	0.3 (X02)
89	9	HW	02/28/2013	COMPAL	Follow INTEL CRB XDP schematic	CC68 change to 0.1uF from 0.01uF	0.3 (X02)
90	7	HW	02/28/2013	COMPAL	For RF 24MHz issue	1. remove UC5 CC25, CC57, CC80, CC86~CC90, CC22, RC62, RC100, CC23 2. Change RC65 to 0 ohm-short	0.3 (X02)
91	9	HW	02/28/2013	COMPAL	For Touch panel issue	1. TOUCH_PANEL_INTR# add RC181(0) PU & RC180 PD	0.3 (X02)
92	7, 29	HW	03/01/2013	COMPAL	refer GPIO3.0 to add PCH_TPM_LPC_EN	1. add RC56 for pull up enable signal and add R198 for pop option 2. change R193 form 0hm to 10ohm	0.3 (X02)
93	7	HW	03/12/2013	COMPAL	Base on INTEL EDS SPEC Update Rev 1.5.1	1. LANCLK_REQ# change to UC1.AD1 from UC1.Y5 2. MINI1CLK_REQ# change to UC1.T2 from UC1.U2 3. MINI2CLK_REQ# change to UC1.N1 from UC1.T2 4. MMICLK_REQ# change to UC1.U5 from UC1.AD1 5. PCH_TPM_LPC_EN change to UC1.Y5 from UC1.U5	0.4 (X02)
94	7	HW	03/14/2013	COMPAL	For PCIE CLK & PCIE CLK REQ signal mapping	1. CLK_PCIE_LAN change CLKOUT_PCIE port2 2. CLK_PCIE_MINI2 change CLKOUT_PCIE port3 3. CLK_PCIE_MMI change CLKOUT_PCIE port4 4. CLK_PCIE_MINI1 change CLKOUT_PCIE port5	0.4 (X02)
95	30	HW	03/14/2013	COMPAL	For O2 enters into test mode unexpectedly with SD card inserted incompletely issue.	1. SD/MMCCD# add C256(0.1uF) & R493(1M) pull-down to GND 2. C222 change to 1uF(SE000000K80) from 0.1u(SE000000G880)	0.4 (X02)
96	21	HW	03/15/2013	COMPAL	For Synaptics vender request	1. Delete VMM2310 co-lay related schematic	0.4 (X02)
97	21	HW	03/15/2013	COMPAL	For ESD request	1. Add C458(0) & C459(0) & C460(0) & C461(0) 22uF 0603 size	0.4 (X02)
98	7	HW	03/18/2013	COMPAL	For INTEL request	PCIECLK_REQ0# add RC57(10k) pull-high to +3.3V_RUN	0.4 (X02)
99	21	HW	03/20/2013	COMPAL	For Synaptics vender request	1. Delete R78/R80/R82 2. add C132	0.4 (X02)
100	21	HW	03/20/2013	COMPAL	For ME request	ST2 change to H_2P8 from CLIP_C5P1	0.4 (X02)
101	9, 12, 15	HW	03/22/2013	COMPAL	For ESD request	1. H_CPUPWRGD add CC90 100pF(0) to GND 2. H_THERMTRIP# add CC91 100pF(0) to GND 3. H_VCCST_PWRGD add CC22 100pF(0) to GND	0.4 (X02)

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102	9	HW	03/27/2013	COMPAL	For Touch panel issue	pop RC181 and depop RC180 (@)	0.4 (X02)
103	9	HW	03/27/2013	COMPAL	For XDP SPEC	pop RC97 & RC135	0.4 (X02)
104	32	HW	04/24/2013	COMPAL	For USB S3 wake up issue	U33 power rail change from +3.3V_RUN to +3.3V_SUS	1.0 (A00)
105	9	HW	04/24/2013	COMPAL	For XDP signal should be contact to PCH	change RC97 and RC135 to 0ohm short	1.0 (A00)
106	37	HW	04/25/2013	COMPAL	Change Board ID for A00	R392 change from33K ohm to 1K ohm	1.0 (A00)
107	40	HW	04/25/2013	COMPAL	For LED EA	R436 change from150 ohm to 330 ohm;R438 change from 150 ohm to 220 ohm	1.0 (A00)
108	28	HW	04/25/2013	COMPAL	for support Vpro reset pin	depop U20 and add R145	1.0 (A00)
109	12	HW	04/25/2013	COMPAL	reserve for support non vpro pop option pin	reserve RC292 100 ohm pull down	1.0 (A00)
110	6	HW	05/13/2013	COMPAL	For Crystal EA result & RTC time fail issue	1. CC1 & CC2 change from 18pF to 15pF	1.0 (A00)
111	16	HW	05/17/2013	COMPAL	For ESD request	Depop CC71/CC72/CC73	1.0 (A00)

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