

***Strongbow_KL
Schematics Document***

***DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed***

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipet Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

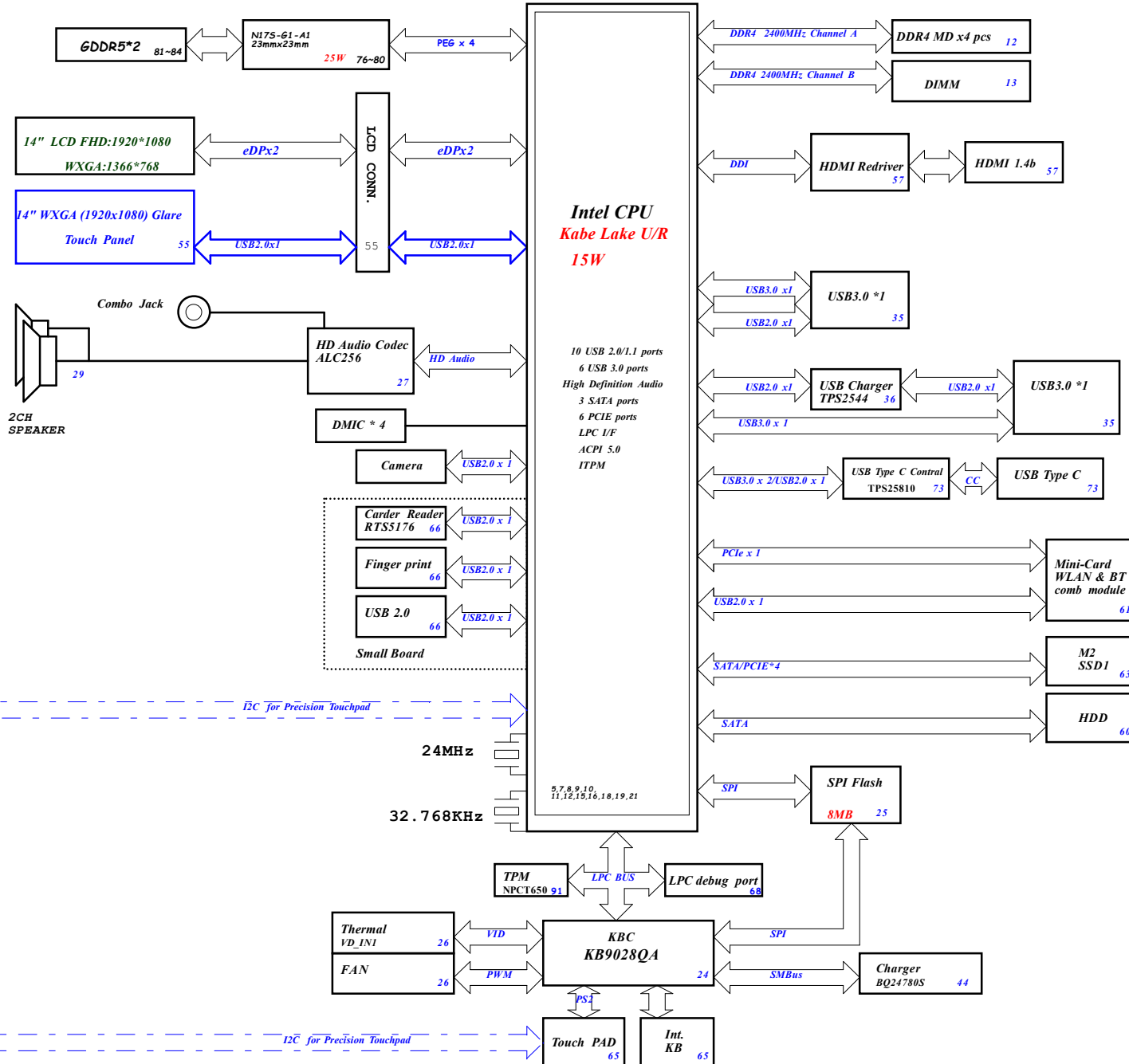
Document Number

Rev
1

Date: Thursday, January 11, 2018

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Strongbow_KBL Block Diagram



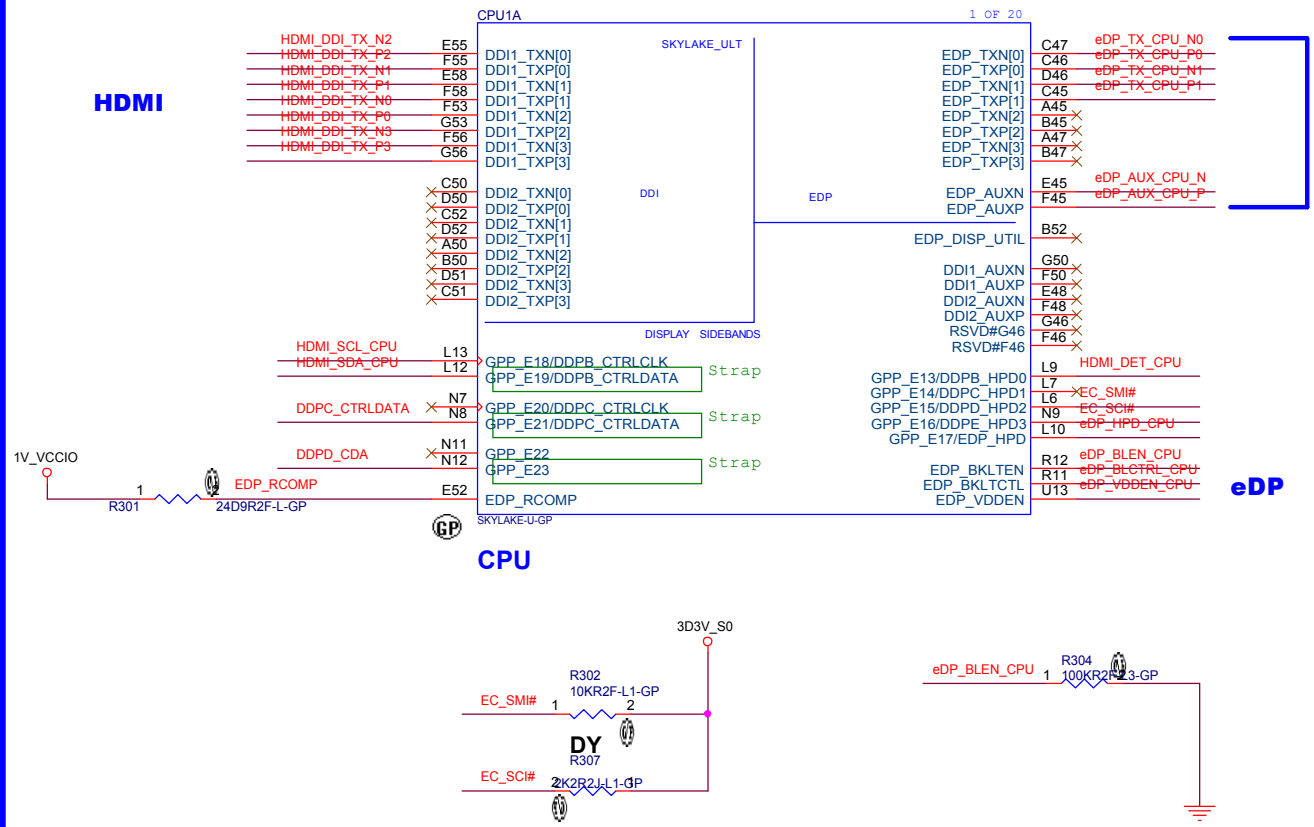
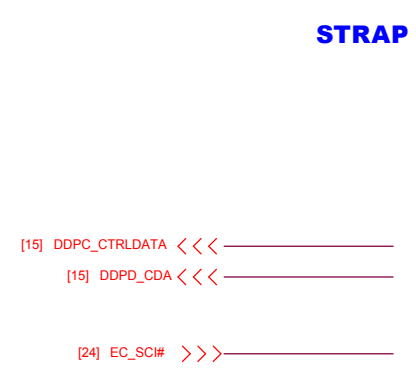
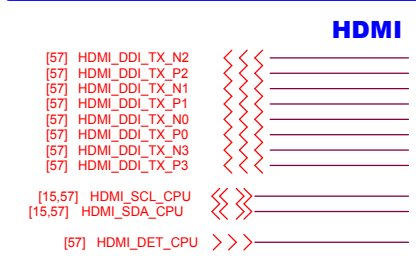
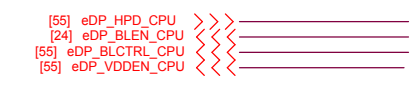
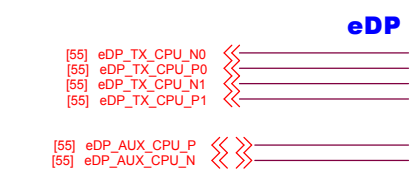
GPU DC/DC RT8813D6QW-GP 85		CHARGER BQ24780S 44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S0	1V_V6ACORE_S0	AD* BT*	19V_DCBATOUT
GPU DC/DC RT8816A6QW-GP 86		SYSTEM DC/DC RT6258C6QUF-GP 45	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	1D35V_V6A_S0	19V_DCBATOUT	3D3V_AUX_S5 5V_S5
GPU DC/DC SY8003ADFC-GP 86		SYSTEM DC/DC RT6256B6QUF-GP 45	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_AON_S0	19V_DCBATOUT	3D3V_S5
GPU DC/DC APE8939GN3-GP 86		CPU DC/DC RT3602 46-47	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D8V_AON_S0	1D8V_V6A_S0	19V_DCBATOUT	1V_CPU_CORE
GPU DC/DC APE8939GN3-GP 86		CPU DC/DC AOZ5049 48	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D0V_S5	1V_1D05V_V6A_S0	19V_DCBATOUT	1V_VCCGT
		CPU DC/DC RT9610B 50	
		INPUTS	OUTPUTS
		5V_S5	1V_VCCSA
		CPU DC/DC G5388K11U-GP 51	
		INPUTS	OUTPUTS
		5V_S5	PWR_VDDQ
		CPU DC/DC APL5930KAI 51	
		INPUTS	OUTPUTS
		5V_S5	2D5V_S3
		SYSTEM DC/DC G5388K11U-GP 52	
		INPUTS	OUTPUTS
		5V_S5	1D0V_S5
		SYSTEM DC/DC G9661-25ADJ 53	
		INPUTS	OUTPUTS
		3D3V_S5	1D8V_S5
		SYSTEM Load switch TPS22976 40	
		INPUTS	OUTPUTS
		3D3V_S5	1D5V_S0
		5V_S5	5V_S0
		1D0V_S5	1V_VCCST
		1D8V_S5	1D8V_S0
		SYSTEM Load switch APE8939 40	
		INPUTS	OUTPUTS
		1D0V_S5	1V_VCCIO

<Core Design>

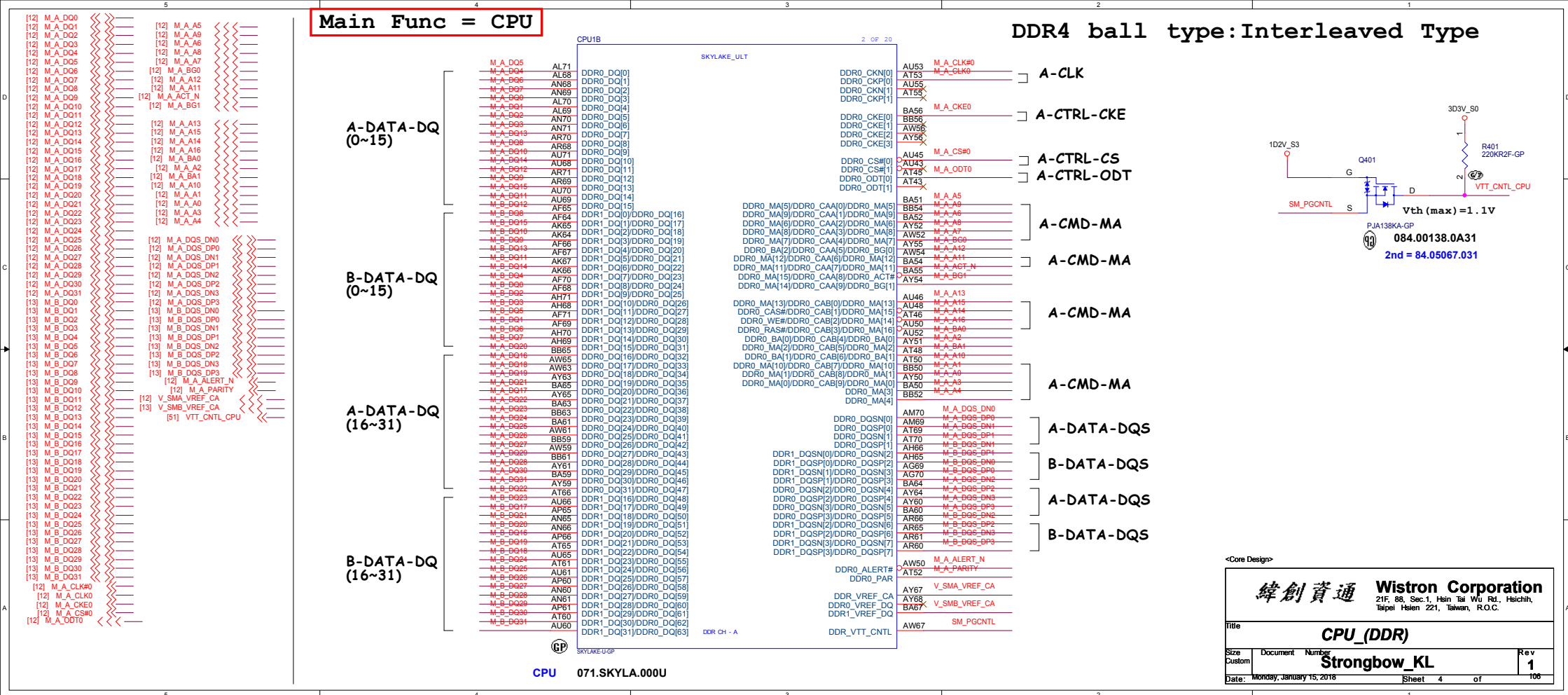
緯創資通 Wistron Corporation
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Block Diagram			
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Main Func = CPU



DDR4 ball type:Interleaved Type



<Core Design>

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Title				CPU_(DDR)			
Size	Document	Number					Rev
Custom	Strongbow_KL						1
Date:	Monday, January 15, 2018		Sheet	4	of	106	

Main Func = CPU

DDR4 ball type:Interleaved Type

[13] M_B_DQ32	[13] M_B_A5	
[13] M_B_DQ33	[13] M_B_A9	
[13] M_B_DQ34	[13] M_B_A6	
[13] M_B_DQ35	[13] M_B_A8	
[13] M_B_DQ36	[13] M_B_A7	
[13] M_B_DQ37	[13] M_B_BG0	
[13] M_B_DQ38	[13] M_B_A12	
[13] M_B_DQ39	[13] M_B_A11	
[13] M_B_DQ40	[13] M_B_ACT_N	
[13] M_B_DQ41	[13] M_B_BG1	
[13] M_B_DQ42	[13] M_B_A13	
[13] M_B_DQ43	[13] M_B_A15	
[13] M_B_DQ44	[13] M_B_A14	
[13] M_B_DQ45	[13] M_B_A16	
[13] M_B_DQ46	[13] M_B_BA0	
[13] M_B_DQ47	[13] M_B_A2	
[13] M_B_DQ48	[13] M_B_BA1	
[13] M_B_DQ49	[13] M_B_A10	
[13] M_B_DQ50	[13] M_B_A1	
[13] M_B_DQ51	[13] M_B_A0	
[13] M_B_DQ52	[13] M_B_A3	
[13] M_B_DQ53	[13] M_B_A4	
[13] M_B_DQ54	[13] M_B_CLK#0	
[13] M_B_DQ55	[13] M_B_CLK0	
[13] M_B_DQ56	[13] M_B_CKE0	
[13] M_B_DQ57	[13] M_B_CS#0	
[13] M_B_DQ58	[13] M_B_ODT0	
[13] M_B_DQ59	[13] M_B_DQS_DN4	
[13] M_B_DQ60	[13] M_B_DQS_DN5	
[13] M_B_DQ61	[13] M_B_DQS_DN6	
[13] M_B_DQ62	[13] M_B_DQS_DN7	
[13] M_B_DQ63	[13] M_B_DQS_DN8	
[12] M_A_DQ32	[12] M_A_DQS_DP6	
[12] M_A_DQ33	[12] M_A_DQS_DP7	
[12] M_A_DQ34	[12] M_A_DQS_DP4	
[12] M_A_DQ35	[12] M_B_DQS_DP5	
[12] M_A_DQ36	[13] M_B_DQS_DP4	
[12] M_A_DQ37	[13] M_B_DQS_DN5	
[12] M_A_DQ38	[13] M_B_DQS_DP6	
[12] M_A_DQ39	[13] M_B_DQS_DN6	
[12] M_A_DQ40	[13] M_B_DQS_DP6	
[12] M_A_DQ41	[13] M_B_DQS_DN7	
[12] M_A_DQ42	[13] M_B_DQS_DP7	
[12] M_A_DQ43		
[12] M_A_DQ44	[13] M_B_ALERT_N	
[12] M_A_DQ45	[13] M_B_PARITY	
[12] M_A_DQ46	[12,13] SM_DRAMRST#	
[12] M_A_DQ47	[13] M_B_ODT1	
[12] M_A_DQ48	[13] M_B_CS#1	
[12] M_A_DQ49		
[12] M_A_DQ50	[13] M_B_CLK#1	M_B_CLK1
[12] M_A_DQ51		
[12] M_A_DQ52	[13] M_B_CLK1	
[12] M_A_DQ53		
[12] M_A_DQ54		
[12] M_A_DQ55	[13] M_B_CKE1	M_B_CKE1
[12] M_A_DQ56		
[12] M_A_DQ57		
[12] M_A_DQ58		
[12] M_A_DQ59		
[12] M_A_DQ60		
[12] M_A_DQ61		
[12] M_A_DQ62		
[12] M_A_DQ63		

A-DATA-DQ (32~47)

B-DATA-DQ (32~47)

A-DATA-DQ (48~63)

B-DATA-DQ (48~63)

M_A_DQ32	AY39	DDR0_DQ32/DDR1_DQ[0]
M_A_DQ36	AW39	DDR0_DQ36/DDR1_DQ[4]
M_A_DQ34	AY37	DDR0_DQ34/DDR1_DQ[2]
M_A_DQ38	AW37	DDR0_DQ38/DDR1_DQ[6]
M_A_DQ35	BB39	DDR0_DQ35/DDR1_DQ[3]
M_A_DQ37	BA39	DDR0_DQ37/DDR1_DQ[5]
M_A_DQ36	BA37	DDR0_DQ36/DDR1_DQ[4]
M_A_DQ39	BB37	DDR0_DQ39/DDR1_DQ[7]
M_A_DQ45	BB37	DDR0_DQ45/DDR1_DQ[13]
M_A_DQ41	AW35	DDR0_DQ41/DDR1_DQ[9]
M_A_DQ43	AW35	DDR0_DQ43/DDR1_DQ[11]
M_A_DQ44	AY33	DDR0_DQ44/DDR1_DQ[12]
M_A_DQ45	BB35	DDR0_DQ45/DDR1_DQ[13]
M_A_DQ46	BA35	DDR0_DQ46/DDR1_DQ[14]
M_A_DQ43	BA33	DDR0_DQ43/DDR1_DQ[10]
M_B_DQ36	ALU0	DDR0_DQ36/DDR1_DQ[4]
M_B_DQ38	AT40	DDR0_DQ38/DDR1_DQ[6]
M_B_DQ36	AT37	DDR0_DQ36/DDR1_DQ[4]
M_B_DQ38	AR40	DDR0_DQ38/DDR1_DQ[6]
M_B_DQ39	AP37	DDR0_DQ39/DDR1_DQ[7]
M_B_DQ40	AT33	DDR0_DQ40/DDR1_DQ[8]
M_B_DQ41	AT33	DDR0_DQ41/DDR1_DQ[9]
M_B_DQ42	AT33	DDR0_DQ42/DDR1_DQ[10]
M_B_DQ43	AT33	DDR0_DQ43/DDR1_DQ[11]
M_B_DQ44	AT33	DDR0_DQ44/DDR1_DQ[12]
M_B_DQ45	AT33	DDR0_DQ45/DDR1_DQ[13]
M_B_DQ46	AT33	DDR0_DQ46/DDR1_DQ[14]
M_B_DQ47	AT33	DDR0_DQ47/DDR1_DQ[15]
M_B_DQ48	AT33	DDR0_DQ48/DDR1_DQ[16]
M_B_DQ49	AT33	DDR0_DQ49/DDR1_DQ[17]
M_B_DQ50	AT33	DDR0_DQ50/DDR1_DQ[18]
M_B_DQ51	AT33	DDR0_DQ51/DDR1_DQ[19]
M_B_DQ52	AT33	DDR0_DQ52/DDR1_DQ[20]
M_B_DQ53	AT33	DDR0_DQ53/DDR1_DQ[21]
M_B_DQ54	AT33	DDR0_DQ54/DDR1_DQ[22]
M_B_DQ55	AT33	DDR0_DQ55/DDR1_DQ[23]
M_B_DQ56	AT33	DDR0_DQ56/DDR1_DQ[24]
M_B_DQ57	AT33	DDR0_DQ57/DDR1_DQ[25]
M_B_DQ58	AT33	DDR0_DQ58/DDR1_DQ[26]
M_B_DQ59	AT33	DDR0_DQ59/DDR1_DQ[27]
M_B_DQ60	AT33	DDR0_DQ60/DDR1_DQ[28]
M_B_DQ61	AT33	DDR0_DQ61/DDR1_DQ[29]
M_B_DQ62	AT33	DDR0_DQ62/DDR1_DQ[30]
M_B_DQ63	AT33	DDR0_DQ63/DDR1_DQ[31]
M_B_DQ64	AT33	DDR0_DQ64/DDR1_DQ[32]
M_B_DQ65	AT33	DDR0_DQ65/DDR1_DQ[33]
M_B_DQ66	AT33	DDR0_DQ66/DDR1_DQ[34]
M_B_DQ67	AT33	DDR0_DQ67/DDR1_DQ[35]
M_B_DQ68	AT33	DDR0_DQ68/DDR1_DQ[36]
M_B_DQ69	AT33	DDR0_DQ69/DDR1_DQ[37]
M_B_DQ70	AT33	DDR0_DQ70/DDR1_DQ[38]
M_B_DQ71	AT33	DDR0_DQ71/DDR1_DQ[39]
M_B_DQ72	AT33	DDR0_DQ72/DDR1_DQ[40]
M_B_DQ73	AT33	DDR0_DQ73/DDR1_DQ[41]
M_B_DQ74	AT33	DDR0_DQ74/DDR1_DQ[42]
M_B_DQ75	AT33	DDR0_DQ75/DDR1_DQ[43]
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M_B_DQ77	AT33	DDR0_DQ77/DDR1_DQ[45]
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M_B_DQ79	AT33	DDR0_DQ79/DDR1_DQ[47]
M_B_DQ80	AT33	DDR0_DQ80/DDR1_DQ[48]
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M_B_DQ87	AT33	DDR0_DQ87/DDR1_DQ[55]
M_B_DQ88	AT33	DDR0_DQ88/DDR1_DQ[56]
M_B_DQ89	AT33	DDR0_DQ89/DDR1_DQ[57]
M_B_DQ90	AT33	DDR0_DQ90/DDR1_DQ[58]
M_B_DQ91	AT33	DDR0_DQ91/DDR1_DQ[59]
M_B_DQ92	AT33	DDR0_DQ92/DDR1_DQ[60]
M_B_DQ93	AT33	DDR0_DQ93/DDR1_DQ[61]
M_B_DQ94	AT33	DDR0_DQ94/DDR1_DQ[62]
M_B_DQ95	AT33	DDR0_DQ95/DDR1_DQ[63]

SKYLAKE_U LT	DDR1_CKN[0]	AN45	M_B_CLK#0
	DDR1_CKN[1]	AN45	M_B_CLK#1
	DDR1_CKN[2]	AP45	M_B_CLK#0
	DDR1_CKN[3]	AP45	M_B_CLK#1
	DDR1_CKE[0]	AN56	M_B_CKE0
	DDR1_CKE[1]	AN56	M_B_CKE1
	DDR1_CKE[2]	AP53	X
	DDR1_CKE[3]	AP53	X
	DDR1_CS#0	BB42	M_B_CS#0
	DDR1_CS#1	BB42	M_B_CS#1
	DDR1_ODT[0]	AW42	M_B_ODT0
	DDR1_ODT[1]	AW42	M_B_ODT1
	DDR1_ODT[2]	AW42	M_B_ODT2
	DDR1_ODT[3]	AW42	M_B_ODT3
	DDR1_ODT[4]	AW42	M_B_ODT4
	DDR1_ODT[5]	AW42	M_B_ODT5
	DDR1_ODT[6]	AW42	M_B_ODT6
	DDR1_ODT[7]	AW42	M_B_ODT7
	DDR1_ODT[8]	AW42	M_B_ODT8
	DDR1_ODT[9]	AW42	M_B_ODT9
	DDR1_ODT[10]	AW42	M_B_ODT10
	DDR1_ODT[11]	AW42	M_B_ODT11
	DDR1_ODT[12]	AW42	M_B_ODT12
	DDR1_ODT[13]	AW42	M_B_ODT13
	DDR1_ODT[14]	AW42	M_B_ODT14
	DDR1_ODT[15]	AW42	M_B_ODT15
	DDR1_ODT[16]	AW42	M_B_ODT16
	DDR1_ODT[17]	AW42	M_B_ODT17
	DDR1_ODT[18]	AW42	M_B_ODT18
	DDR1_ODT[19]	AW42	M_B_ODT19
	DDR1_ODT[20]	AW42	M_B_ODT20
	DDR1_ODT[21]	AW42	M_B_ODT21
	DDR1_ODT[22]	AW42	M_B_ODT22
	DDR1_ODT[23]	AW42	M_B_ODT23
	DDR1_ODT[24]	AW42	M_B_ODT24
	DDR1_ODT[25]	AW42	M_B_ODT25
	DDR1_ODT[26]	AW42	M_B_ODT26
	DDR1_ODT[27]	AW42	M_B_ODT27
	DDR1_ODT[28]	AW42	M_B_ODT28
	DDR1_ODT[29]	AW42	M_B_ODT29
	DDR1_ODT[30]	AW42	M_B_ODT30
	DDR1_ODT[31]	AW42	M_B_ODT31
	DDR1_ODT[32]	AW42	M_B_ODT32
	DDR1_ODT[33]	AW42	M_B_ODT33
	DDR1_ODT[34]	AW42	M_B_ODT34
	DDR1_ODT[35]	AW42	M_B_ODT35
	DDR1_ODT[36]	AW42	M_B_ODT36
	DDR1_ODT[37]	AW42	M_B_ODT37
	DDR1_ODT[38]	AW42	M_B_ODT38
	DDR1_ODT[39]	AW42	M_B_ODT39
	DDR1_ODT[40]	AW42	M_B_ODT40
	DDR1_ODT[41]	AW42	M_B_ODT41
	DDR1_ODT[42]	AW42	M_B_ODT42
	DDR1_ODT[43]	AW42	M_B_ODT43
	DDR1_ODT[44]	AW42	M_B_ODT44
	DDR1_ODT[45]	AW42	M_B_ODT45
	DDR1_ODT[46]	AW42	M_B_ODT46
	DDR1_ODT[47]	AW42	M_B_ODT47
	DDR1_ODT[48]	AW42	M_B_ODT48
	DDR1_ODT[49]	AW42	M_B_ODT49
	DDR1_ODT[50]	AW42	M_B_ODT50
	DDR1_ODT[51]	AW42	M_B_ODT51
	DDR1_ODT[52]	AW42	M_B_ODT52
	DDR1_ODT[53]	AW42	M_B_ODT53
	DDR1_ODT[54]	AW42	M_B_ODT54
	DDR1_ODT[55]	AW42	M_B_ODT55
	DDR1_ODT[56]	AW42	M_B_ODT56
	DDR1_ODT[57]	AW42	M_B_ODT57
	DDR1_ODT[58]	AW42	M_B_ODT58
	DDR1_ODT[59]	AW42	M_B_ODT59
	DDR1_ODT[60]	AW42	M_B_ODT60
	DDR1_ODT[61]	AW42	M_B_ODT61
	DDR1_ODT[62]	AW42	M_B_ODT62
	DDR1_ODT[63]	AW42	M_B_ODT63

071.SKYLA.000U #543016

CPU

Design Guideline: SM_RCOMP keep routing length less than 500 mils.

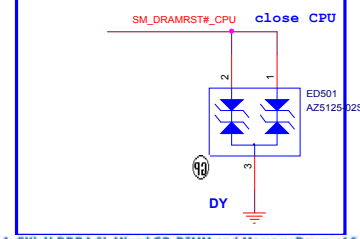
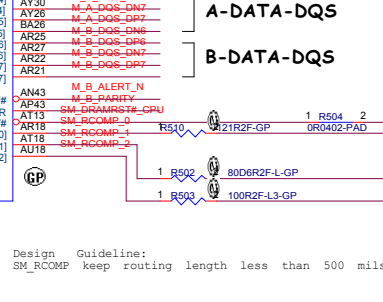
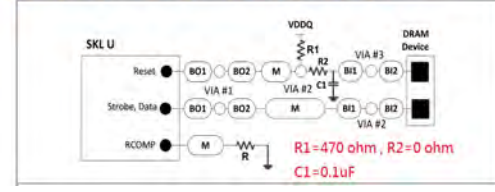
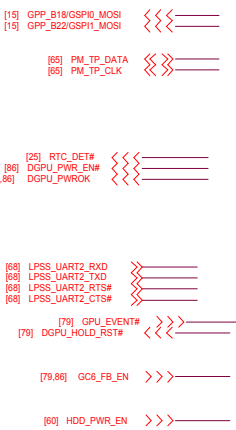


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology Memory Down Strobe/Data/Reset/RCOMP Signal Topologies

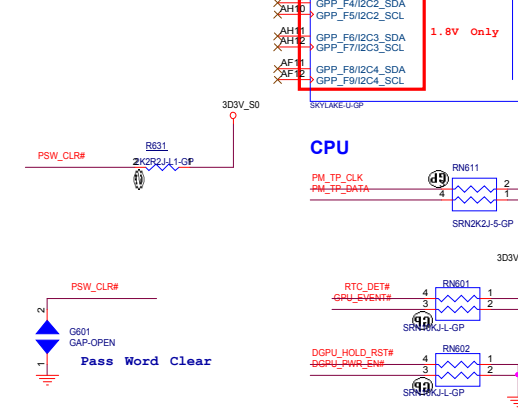


File		CPU_(DDR)	
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Main Func = PCH



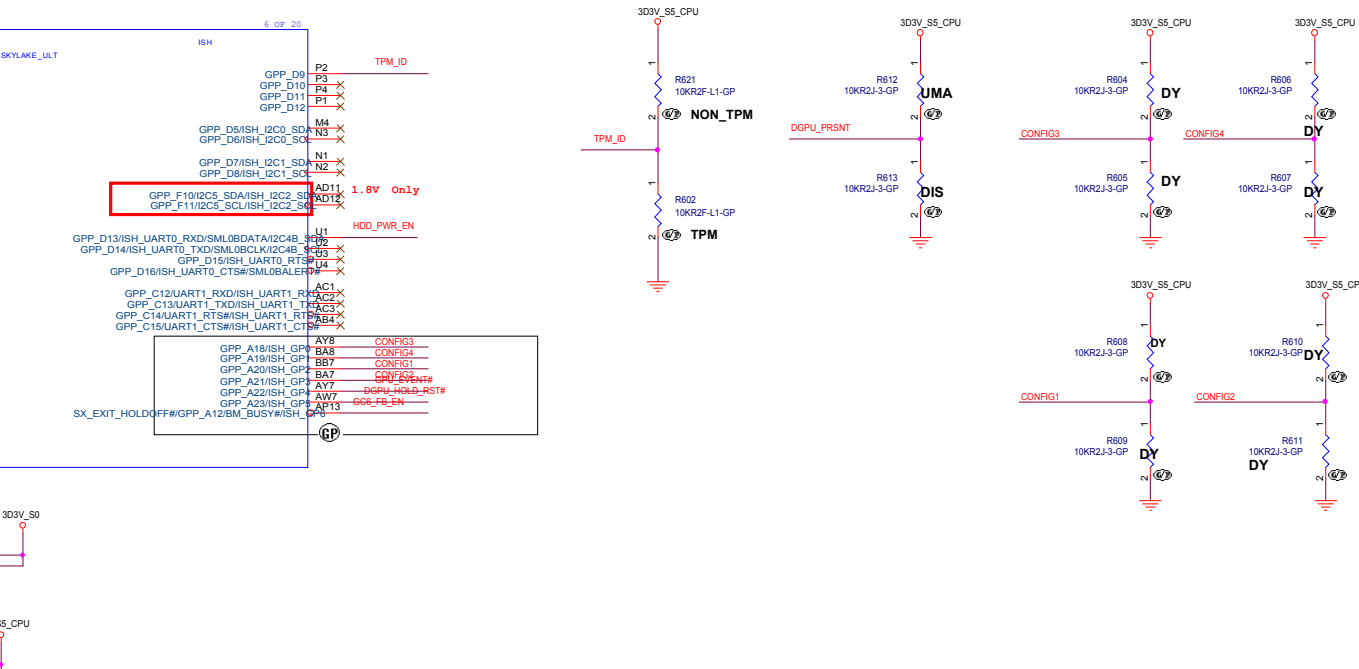
Touch Pad



GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

Vendor	NFIG4 (GPP_A1)	NFIG3 (GPP_A1)	NFIG2 (GPP_A2)	NFIG1 (GPP_A)	Mfr. PN	DDP/SDP	Wistron . P/N	Capacity	Stage
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	SDP	KN.8GB0G.049	8Gb	
Micron	0	0	0	1	MT40A512M16LY-075	SDP	KN.8GB04.027	8Gb	LAB
Micron	0	0	1	0	MT40A1G16KNR-075	DDP	KN.01604.003	16Gb	LAB
HYNIX	0	0	1	1	H5ANAG6NAMR-UHC	DDP	KN.0160G.010	16Gb	



<Core Design>

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Title: CPU (LPSS/ISH)
Strongbow_KL

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Main Func = CPU

SVID

[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU

[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE
[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU
[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE

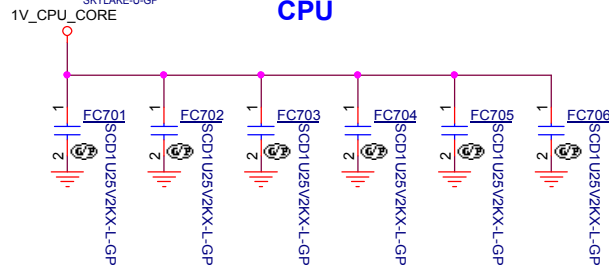
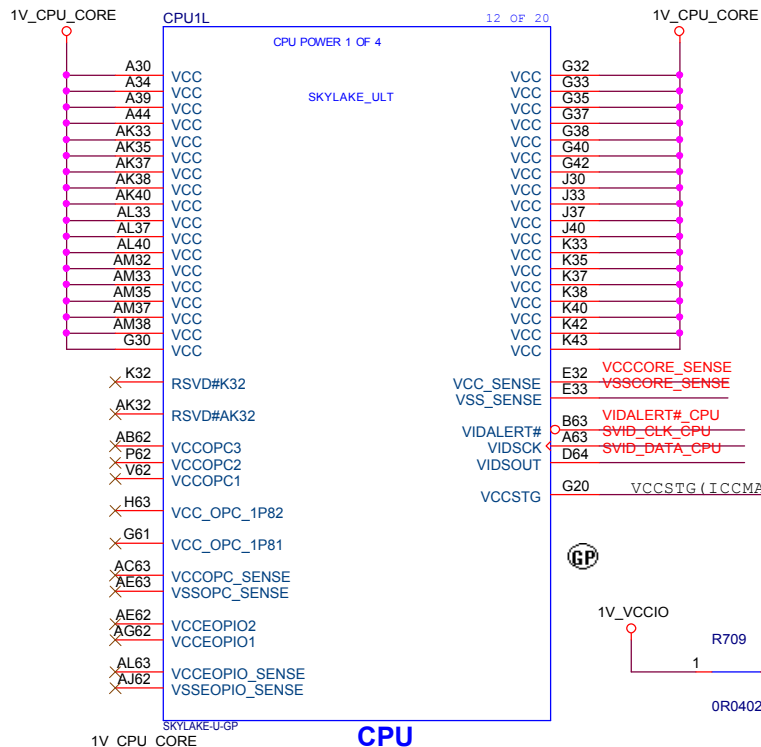
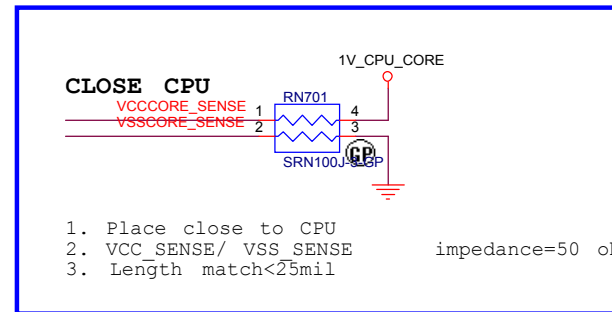
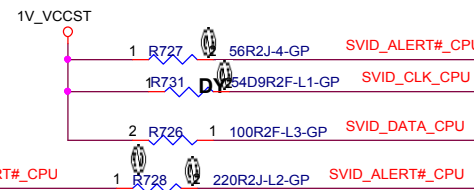


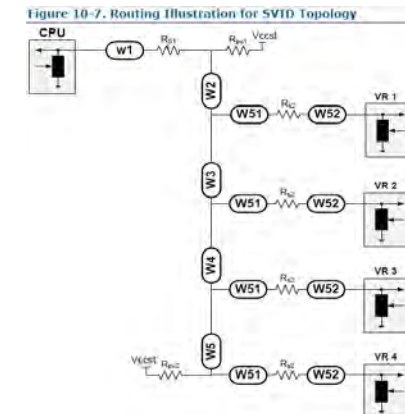
Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{EU1} [Ω]	R _{EU2} [Ω]	R _{S1} [Ω]	R _{S2} [Ω]	V _{CCST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil



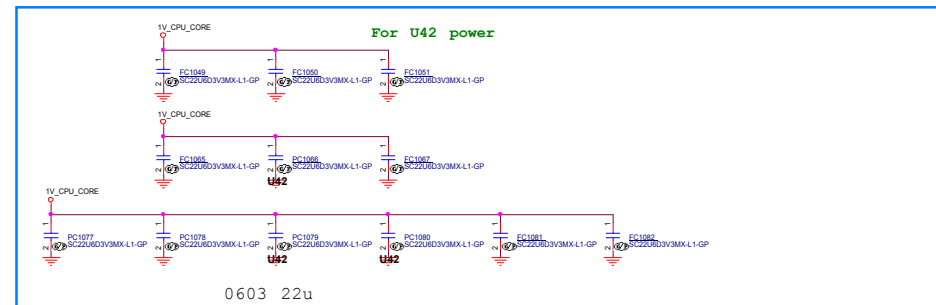
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Title			
CPU_POWER1			
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Blanking

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0402 Assignment:
Inside box use 1uF 0402
Outside box use 10uF 0402

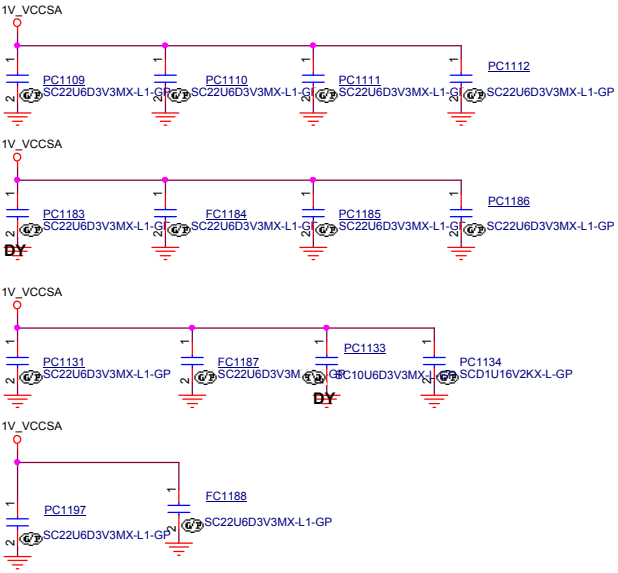
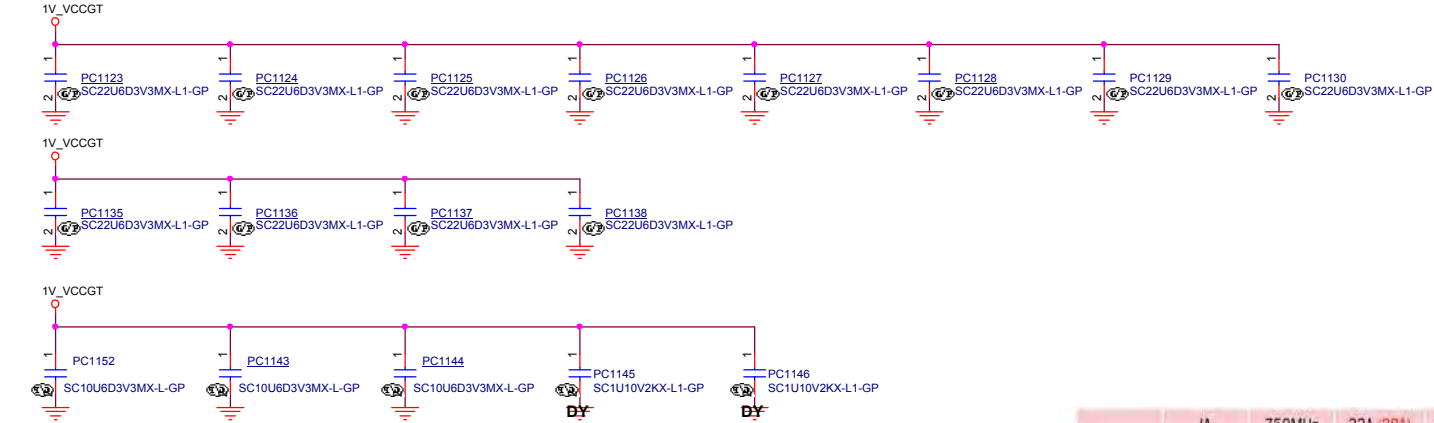
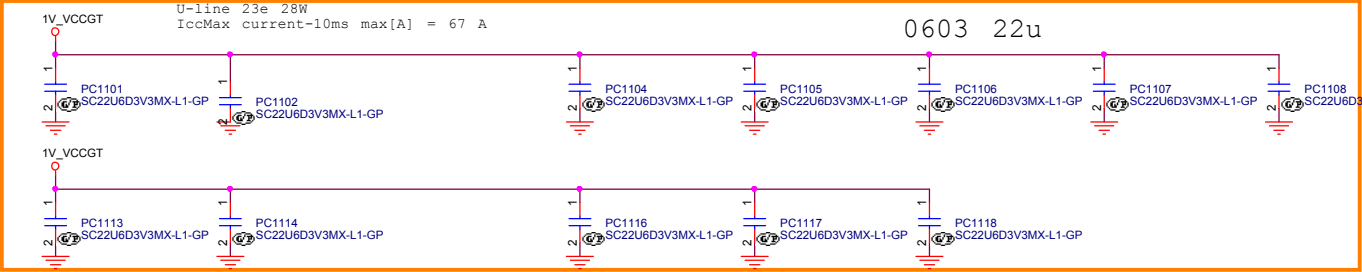
Domain	Backside cap	Primary side cap	Placement guideline
V _{CC}	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V) ¹	
		8x 10 uF 0402	
V _{CC} /V _{CCGT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
V _{CCGT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V) ¹	

Notes:

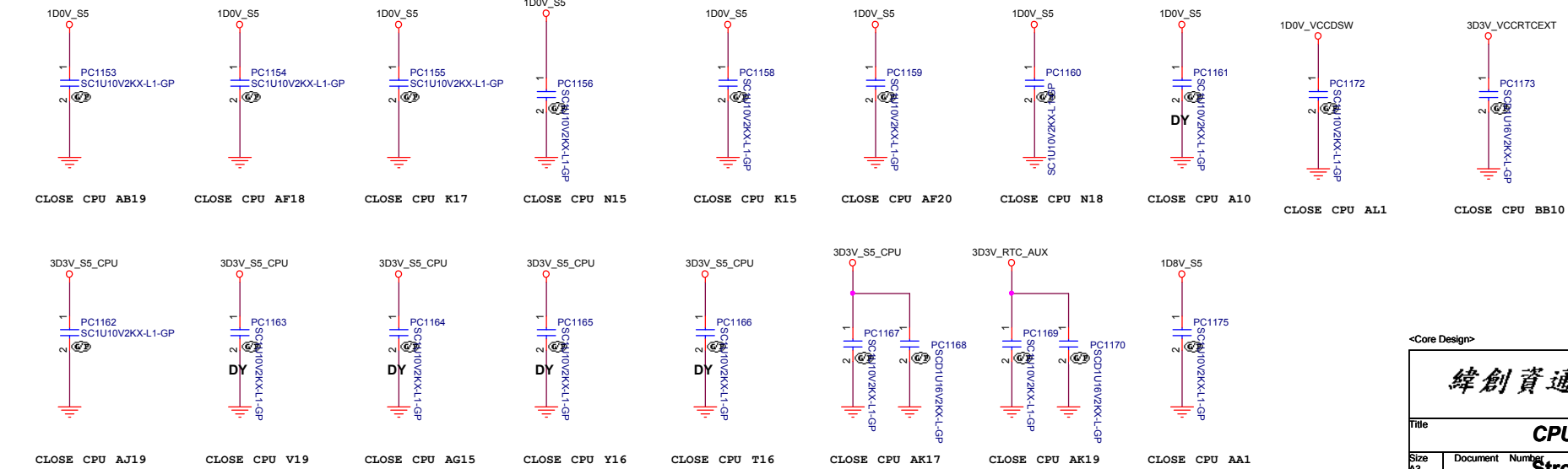
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Main Func = CPU

SLICED GT



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
	GT	750KHz	40A (31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF
								Or	1x330uF/9mW	36x22uF



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Title CPU_(Power CAP2)

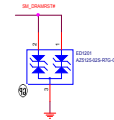
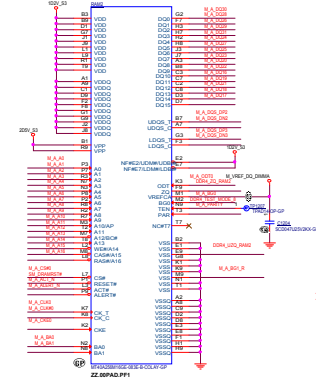
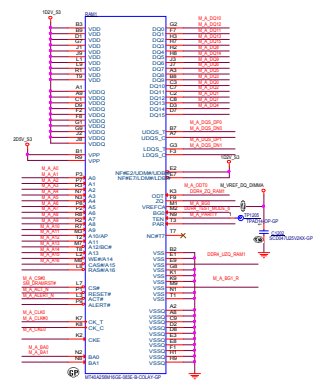
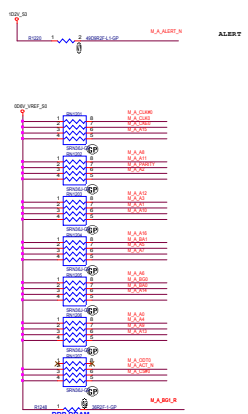
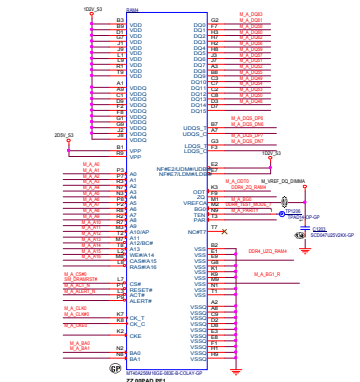
Size A3 Document Number Strongbow_KL Rev 1

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[illegible]

The schematic diagram illustrates the pin connections for the Z80000-0100 CPU. The CPU package is shown with pins 1 through 100. The connections are as follows:

- Power Supply:** VDD (pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100) and VSS (pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100).
- Address Bus:** A[23:0] (pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100).
- Data Bus:** D[31:0] (pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100).
- Control Signals:** RST (pin 1), NMI (pin 2), INT (pin 3), etc.
- Peripheral Devices:** Z80000-0100 and Z80000-0101.



Memory Configuration	Power Domain	Decoupling Location	Qty x μP (size)	Note
DDR4 Memory Dwell x16 - 4 Devices per Channel	VDDQ/VDD (shunt)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VFP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTI	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

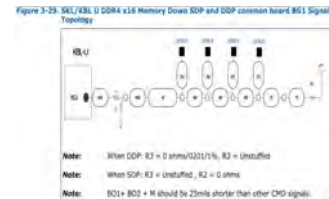
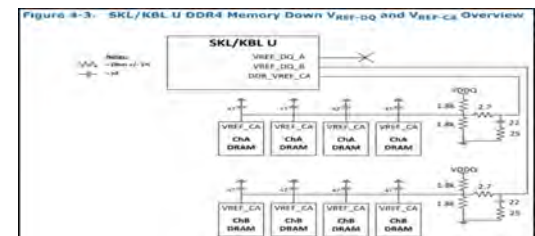
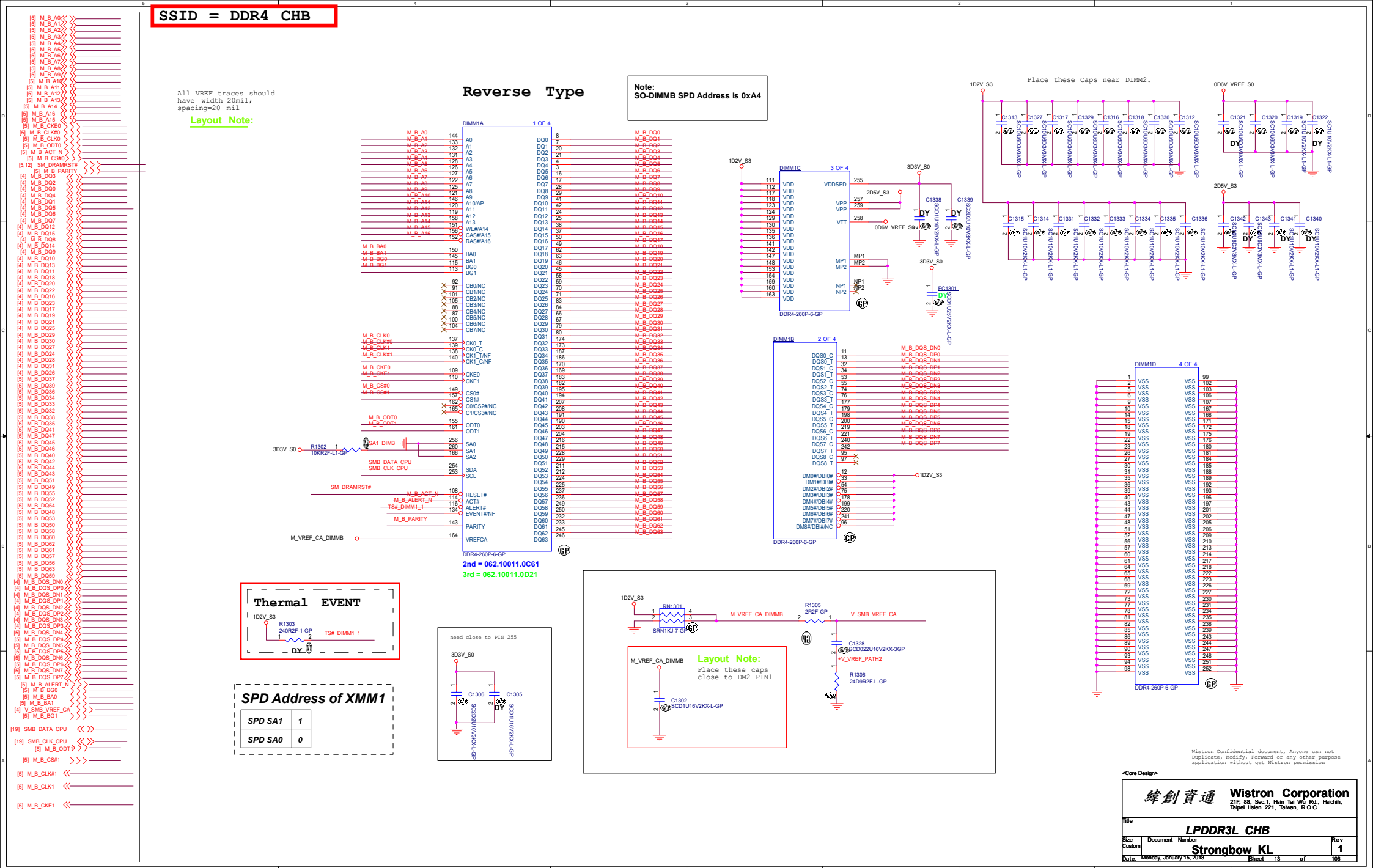


Figure 1: Schematic diagram of the DDP circuit. The diagram shows a central DDP circuit with two input channels, each consisting of a resistor (R1, R2) and a capacitor (C1, C2) in series, connected to a common node. The output is connected to a DDP DRAM. The circuit is powered by a 1.8V supply. The schematic is labeled with component values: R1=1k, R2=1k, C1=100pF, C2=100pF, and DDP DRAM. The output is labeled DDP DRAM.

[illegible]

Title			
LPDDR3L CHB			
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Custom	Strongbow KL		1
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	5	4	3	2	1
D					
C					
B					
A					<div> <div><Core Design></div> <div> <div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div> <div> <div>Title</div> <div>CPU_POWER3</div> </div> <div> <div>Size Custom</div> <div>Document Number</div> <div>Strongbow_KL</div> <div>Rev 1</div> </div> <div> <div>Date: Thursday, January 11, 2018</div> <div>Sheet 14 of 106</div> </div> </div> </div>
	5	4	3	2	1

SSID = STRAP

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confidentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC SHOULD BE PLACED OUTSIDE KIC AREA

Name	Internal Pull-up/ Pull Down (Note 1)	De-assert (Note 2)	Multiplexed With	Default	NMI or SMI Capable	Note
GPP_B22	20K PD (see note)	No	SPI0_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts.
GPP_B23	20K PD (see note)	Yes	SPI0_MOSI / PCMD0#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts.

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HDA_AUDIO_INTERFACE					
HDA_BSP#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO#	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_SDO	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO(1:0)	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

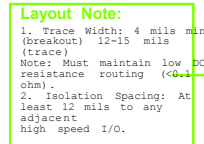
Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	OFF
SPI0_MOSI	Primary	Internal Pull-up/ Pull-down (See Note 3, 6-2)	Driven Low	Driven Low	OFF
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	OFF
SPI0_CS0#	Primary	Driven High	Driven High	Driven High	OFF
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	OFF
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	OFF
SPI0_IO[2:1]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	OFF
SPI1_CLK	Primary	Undriven	Undriven	Undriven	OFF
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	OFF
SPI1_MISO	Primary	Undriven	Undriven	Undriven	OFF
SPI1_CS#	Primary	Undriven	Undriven	Undriven	OFF
SPI1_IO[2:1]	Primary	Undriven	Undriven	Undriven	OFF

Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPT0_MOST / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO-REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GPPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory (readable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 4)). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Boot BIOS Destination 0 = SPI 1 = LPC Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash to be directly to the PCIE's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI access initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
signal	Usage	When Sampled	Comments
DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot block. PCr will invert A16 (default) for cycles going to the upper two cache banks in the PCH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FIC). Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Boot, Device31, Function0, Offset 0ch:Bit4). 4. This signal is in the primary well.
SMALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AHT with TLS and Intel SBA (Small Business Advantage) with TLS. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SMIOALERT# / GPP_C3	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Core Design

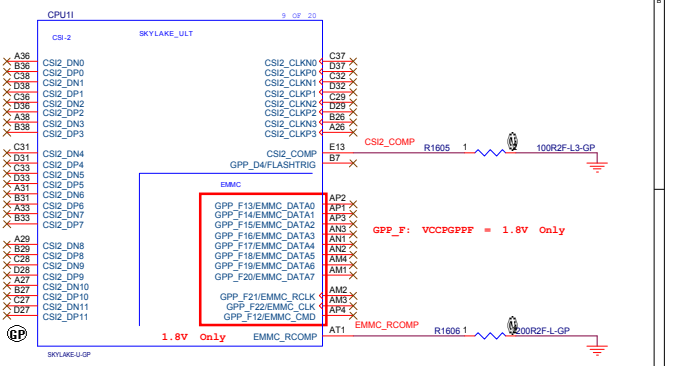
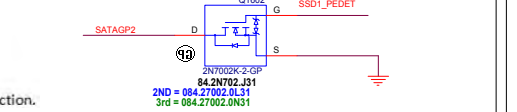
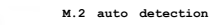
GPU



State #	Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration ²
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	N/C	GND	GND	SSD - PCIe	N/A

	KBL Premium U	Acer 2015	2017 R15(Premium)	2017 R15(base)
Lane1	USB3 Port1	USB 3 (iO)	USB 3 (iO)	USB 3 (iO)
Lane2	USB3 Port2	USB 3 (iO)	USB 3 (iO)	USB 3 (iO)
Lane3	USB3 Port3	USB 3 (iO)	USB 3 Type-C (iO)	USB 3 Type-C (iO)
Lane4	USB3 Port4			
Lane5	USB3 Port5 (Premium)	PCIe Port1		
Lane6	USB3 Port6 (Premium)	PCIe Port2		
Lane7		dGPU	gGPU	gGPU
Lane8		PCIe Port3		
Lane9		PCIe Port4		
Lane10		PCIe Port5	LAN	
Lane11	PCIe Port6	WiFi	WiFi	WiFi
Lane11	SATA0 (Base/Premium)	PCIe Port7 (Premium)	HDD	HDD
Lane12	SATA1 (Base/Premium)	PCIe Port8 (Premium)	ODD	
Lane13		PCIe Port9		
Lane14		PCIe Port10	RA	
Lane15	SATA1 (Premium)	PCIe Port11		
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x1)	
	USB2 Port1	USB 3 (iO)	USB 3 (iO) / (USB20)	USB 3 (iO) / (USB20)
	USB2 Port2	USB 3 (iO)	USB 3 (iO) / (USB20)	USB 3 (iO) / (USB20)
	USB2 Port3	USB 3 (iO)	USB 2 Type-C (iO)	USB 2 Type-C (iO)
	USB2 Port4	USB 2 (iO) / Sensor/Hub	USB 2 (iO)	USB 2 (iO)
	USB2 Port5	BT	BT	BT
	USB2 Port6	FS	FS	FS
	USB2 Port7	GD	GD	GD
	USB2 Port8	CR (USB) / FP	CR	CR
	USB2 Port9	IG	FP	FP
	Port10			

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA



<Core Design>

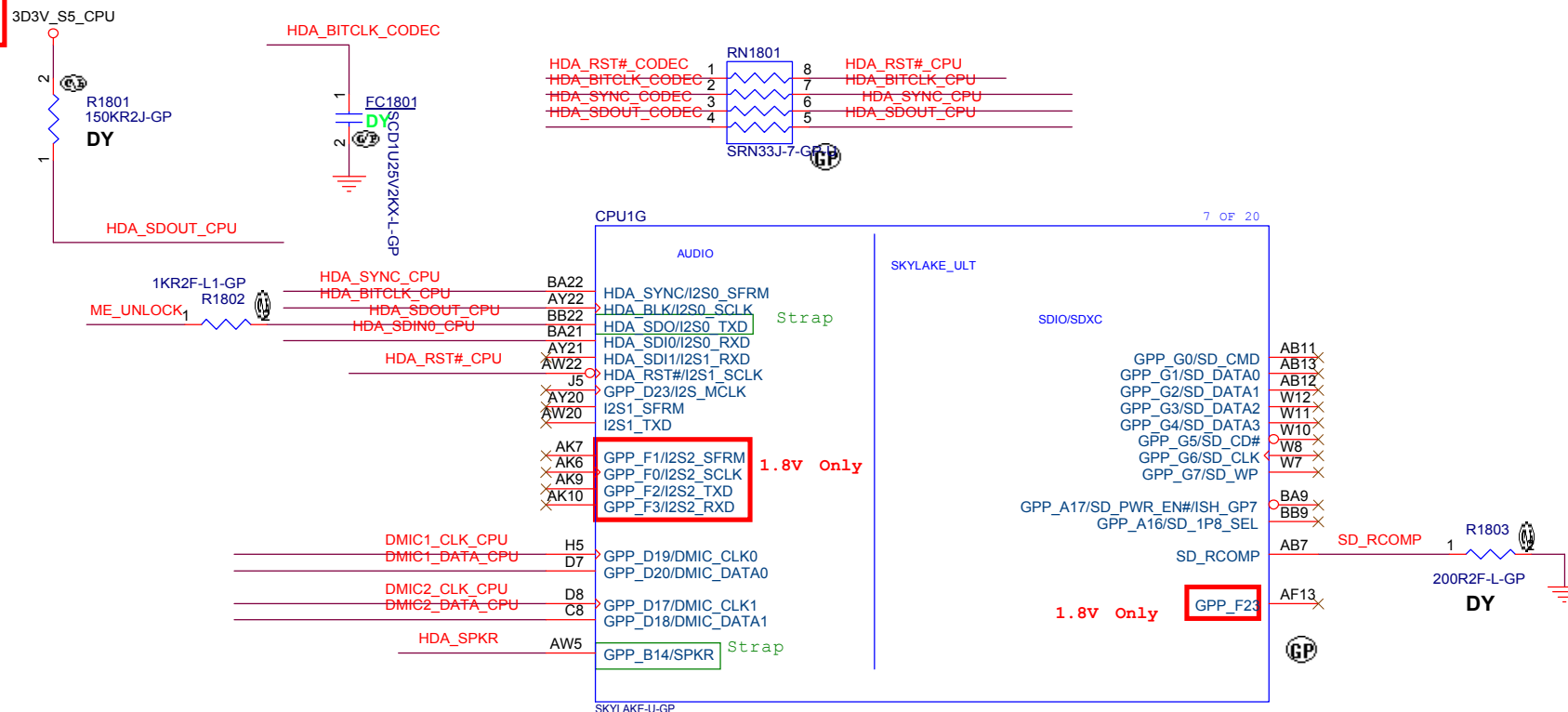
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Title			
CPU_(PCIE/SATA/USB)			
Size	Document Number	Rev	
Custom	Strongbow_KL	1	
Date: 20080815 2008.08.15		Sheet	46 of 106

Audio Code

[24] ME_UNLOCK <<< _____

[55] DMIC2 DATA CPU <<—————

```
[55] DMIC1_DATA_CPU <--
[55] DMIC1_CLK_CPU   <--
[55] DMIC2_CLK_CPU    <--
```



SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

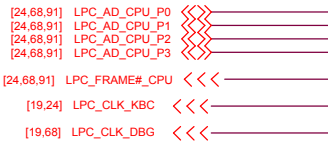
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Size	Document Number	Rev
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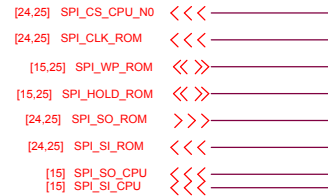
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Main Func = PCH

LPC

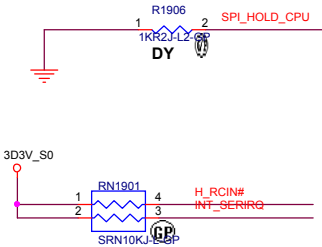
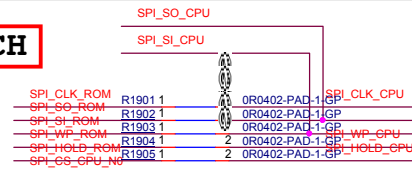
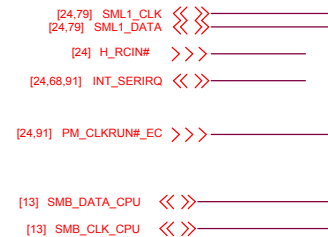


SPI

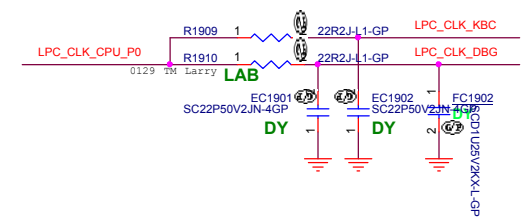
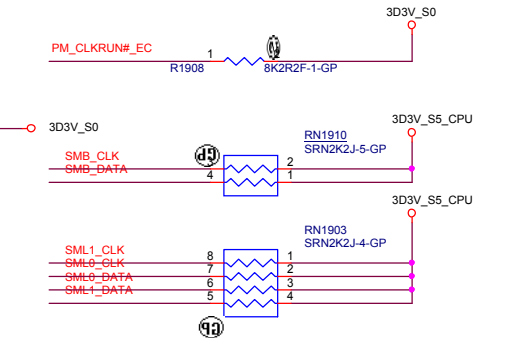
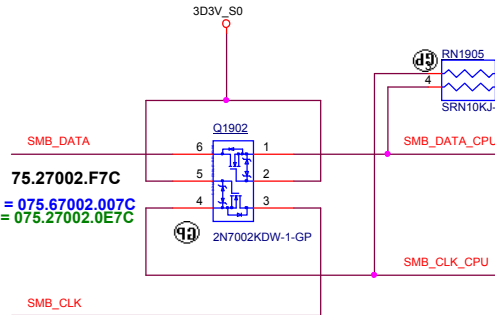
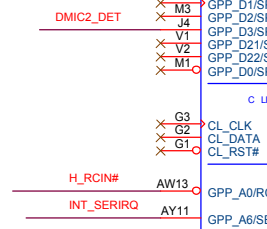


DM1&2 TPAD and XDP

KBC



CPU



20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S - Sample Phase**, Signal driven low
- **R - Recovery Phase**, Signal driven high
- **T - Turn-around Phase**, Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0-1, 3-15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20-23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

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```

[24] SYS_PWRK >>>
[4] PCH_PWRK >>>
[16.63.80] PCI_RMR2 >>>
[24.40] ALL_SYS_PWRD >>>
[24.61.63.79.80.91] PLT_RSTA <<<
[24] RSMSTR_KBC >>>
[45.52] 3V_5V_POK >>>
[24.40.58] PM_SLP_S3R <<<
[24.40.51] PM_SLP_S4R <<<
[24] PM_PWRSTRT >>>
[4] AC_PRESENT >>>
[24.40.60.91] PM_SLP_S0R >>>

```

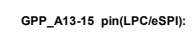
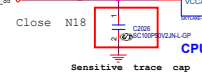
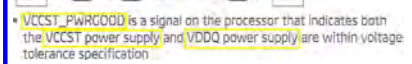


Figure 10: SCIV_SS_CPU pin connections. The diagram shows the following connections:

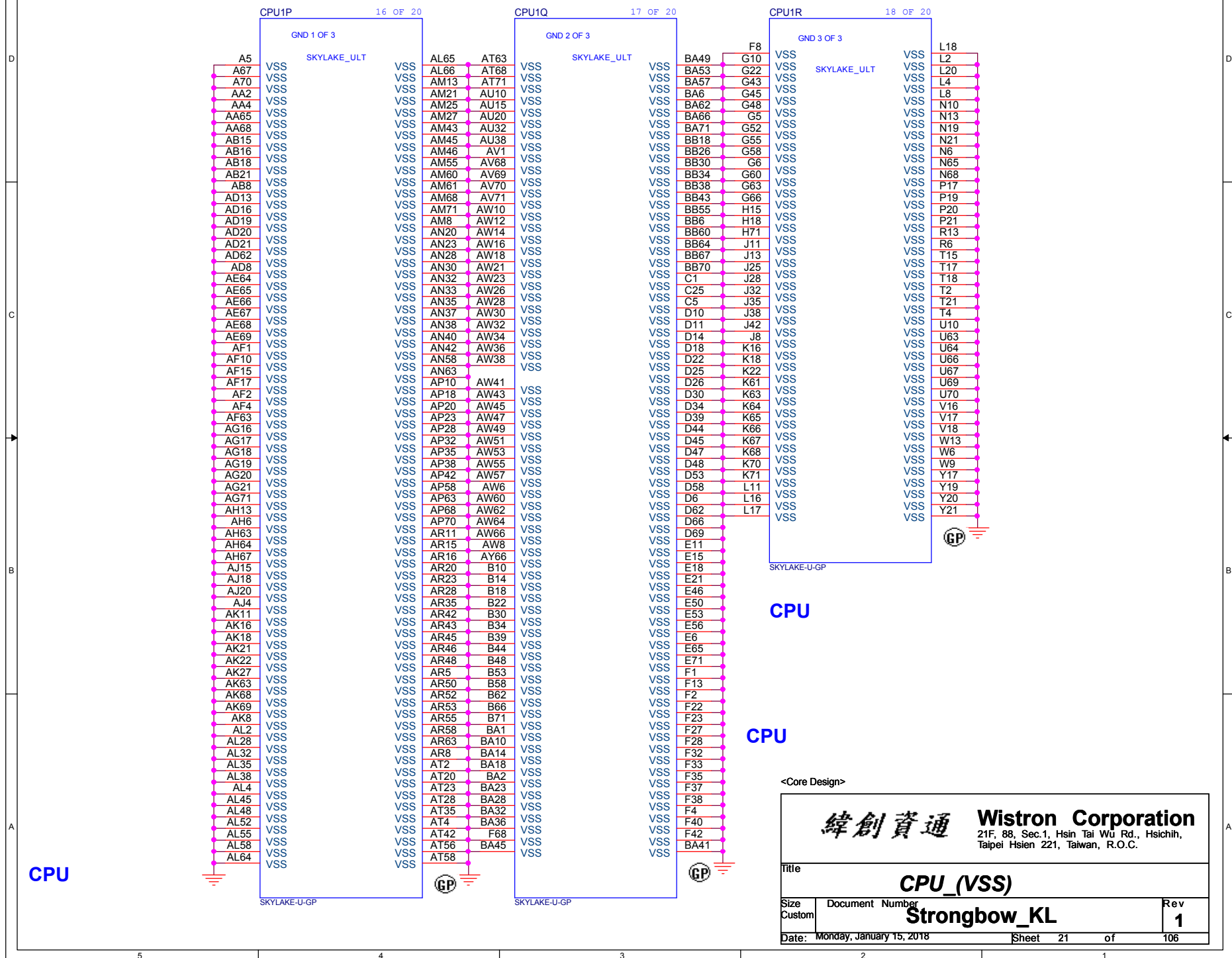
- CPUCLK_IN** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- CPUCLK_OUT** (pin 2) connects to **R2009** (2) and **SCIV_SS_CPU** (2).
- PCIE_WAKEN** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- PCIE_RESETN** (pin 2) connects to **R2009** (2) and **SCIV_SS_CPU** (2).
- PMU_PWDEN** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- EXT_PWR_DATA** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- SM_INTERRUPT#** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- PMU_RESET#** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- XCP_DRESET#** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- SCIV_SS_CPU** (pin 1) connects to **R2009** (1) and **SCIV_SS_CPU** (1).
- SCIV_SS_CPU** (pin 2) connects to **R2009** (2) and **SCIV_SS_CPU** (2).
- SCIV_SS_CPU** (pin 3) connects to **R2009** (3) and **SCIV_SS_CPU** (3).
- SCIV_SS_CPU** (pin 4) connects to **R2009** (4) and **SCIV_SS_CPU** (4).
- SCIV_SS_CPU** (pin 5) connects to **R2009** (5) and **SCIV_SS_CPU** (5).
- SCIV_SS_CPU** (pin 6) connects to **R2009** (6) and **SCIV_SS_CPU** (6).
- SCIV_SS_CPU** (pin 7) connects to **R2009** (7) and **SCIV_SS_CPU** (7).
- SCIV_SS_CPU** (pin 8) connects to **R2009** (8) and **SCIV_SS_CPU** (8).
- SCIV_SS_CPU** (pin 9) connects to **R2009** (9) and **SCIV_SS_CPU** (9).
- SCIV_SS_CPU** (pin 10) connects to **R2009** (10) and **SCIV_SS_CPU** (10).
- SCIV_SS_CPU** (pin 11) connects to **R2009** (11) and **SCIV_SS_CPU** (11).
- SCIV_SS_CPU** (pin 12) connects to **R2009** (12) and **SCIV_SS_CPU** (12).
- SCIV_SS_CPU** (pin 13) connects to **R2009** (13) and **SCIV_SS_CPU** (13).
- SCIV_SS_CPU** (pin 14) connects to **R2009** (14) and **SCIV_SS_CPU** (14).
- SCIV_SS_CPU** (pin 15) connects to **R2009** (15) and **SCIV_SS_CPU** (15).
- SCIV_SS_CPU** (pin 16) connects to **R2009** (16) and **SCIV_SS_CPU** (16).
- SCIV_SS_CPU** (pin 17) connects to **R2009** (17) and **SCIV_SS_CPU** (17).
- SCIV_SS_CPU** (pin 18) connects to **R2009** (18) and **SCIV_SS_CPU** (18).
- SCIV_SS_CPU** (pin 19) connects to **R2009** (19) and **SCIV_SS_CPU** (19).
- SCIV_SS_CPU** (pin 20) connects to **R2009** (20) and **SCIV_SS_CPU** (20).
- SCIV_SS_CPU** (pin 21) connects to **R2009** (21) and **SCIV_SS_CPU** (21).
- SCIV_SS_CPU** (pin 22) connects to **R2009** (22) and **SCIV_SS_CPU** (22).
- SCIV_SS_CPU** (pin 23) connects to **R2009** (23) and **SCIV_SS_CPU** (23).
- SCIV_SS_CPU** (pin 24) connects to **R2009** (24) and **SCIV_SS_CPU** (24).
- SCIV_SS_CPU** (pin 25) connects to **R2009** (25) and **SCIV_SS_CPU** (25).
- SCIV_SS_CPU** (pin 26) connects to **R2009** (26) and **SCIV_SS_CPU** (26).
- SCIV_SS_CPU** (pin 27) connects to **R2009** (27) and **SCIV_SS_CPU** (27).
- SCIV_SS_CPU** (pin 28) connects to **R2009** (28) and **SCIV_SS_CPU** (28).
- SCIV_SS_CPU** (pin 29) connects to **R2009** (29) and **SCIV_SS_CPU** (29).
- SCIV_SS_CPU** (pin 30) connects to **R2009** (30) and **SCIV_SS_CPU** (30).
- SCIV_SS_CPU** (pin 31) connects to **R2009** (31) and **SCIV_SS_CPU** (31).
- SCIV_SS_CPU** (pin 32) connects to **R2009** (32) and **SCIV_SS_CPU** (32).
- SCIV_SS_CPU** (pin 33) connects to **R2009** (33) and **SCIV_SS_CPU** (33).
- SCIV_SS_CPU** (pin 34) connects to **R2009** (34) and **SCIV_SS_CPU** (34).
- SCIV_SS_CPU** (pin 35) connects to **R2009** (35) and **SCIV_SS_CPU** (35).
- SCIV_SS_CPU** (pin 36) connects to **R2009** (36) and **SCIV_SS_CPU** (36).
- SCIV_SS_CPU** (pin 37) connects to **R2009** (37) and **SCIV_SS_CPU** (37).
- SCIV_SS_CPU** (pin 38) connects to **R2009** (38) and **SCIV_SS_CPU** (38).
- SCIV_SS_CPU** (pin 39) connects to **R2009** (39) and **SCIV_SS_CPU** (39).
- SCIV_SS_CPU** (pin 40) connects to **R2009** (40) and **SCIV_SS_CPU** (40).
- SCIV_SS_CPU** (pin 41) connects to **R2009** (41) and **SCIV_SS_CPU** (41).
- SCIV_SS_CPU** (pin 42) connects to **R2009** (42) and **SCIV_SS_CPU** (42).
- SCIV_SS_CPU** (pin 43) connects to **R2009** (43) and **SCIV_SS_CPU** (43).
- SCIV_SS_CPU** (pin 44) connects to **R2009** (44) and **SCIV_SS_CPU** (44).
- SCIV_SS_CPU** (pin 45) connects to **R2009** (45) and **SCIV_SS_CPU** (45).
- SCIV_SS_CPU** (pin 46) connects to **R2009** (46) and **SCIV_SS_CPU** (46).
- SCIV_SS_CPU** (pin 47) connects to **R2009** (47) and **SCIV_SS_CPU** (47).
- SCIV_SS_CPU** (pin 48) connects to **R2009** (48) and **SCIV_SS_CPU** (48).
- SCIV_SS_CPU** (pin 49) connects to **R2009** (49) and **SCIV_SS_CPU** (49).
- SCIV_SS_CPU** (pin 50) connects to **R2009** (50) and **SCIV_SS_CPU** (50).
- SCIV_SS_CPU** (pin 51) connects to **R2009** (51) and **SCIV_SS_CPU** (51).
- SCIV_SS_CPU** (pin 52) connects to **R2009** (52) and **SCIV_SS_CPU** (52).
- SCIV_SS_CPU** (pin 53) connects to **R2009** (53) and **SCIV_SS_CPU** (53).
- SCIV_SS_CPU** (pin 54) connects to **R2009** (54) and **SCIV_SS_CPU** (54).
- SCIV_SS_CPU** (pin 55) connects to **R2009** (55) and **SCIV_SS_CPU** (55).
- SCIV_SS_CPU** (pin 56) connects to **R2009** (56) and **SCIV_SS_CPU** (56).
- SCIV_SS_CPU** (pin 57) connects to **R2009** (57) and **SCIV_SS_CPU** (57).
- SCIV_SS_CPU** (pin 58) connects to **R2009** (58) and **SCIV_SS_CPU** (58).
- SCIV_SS_CPU** (pin 59) connects to **R2009** (59) and **SCIV_SS_CPU** (59).
- SCIV_SS_CPU** (pin 60) connects to **R2009** (60) and **SCIV_SS_CPU** (60).
- SCIV_SS_CPU** (pin 61) connects to **R2009** (61) and **SCIV_SS_CPU** (61).
- SCIV_SS_CPU** (pin 62) connects to **R2009** (62) and **SCIV_SS_CPU** (62).
- SCIV_SS_CPU** (pin 63) connects to **R2009** (63) and **SCIV_SS_CPU** (63).
- SCIV_SS_CPU** (pin 64) connects to **R2009** (64) and **SCIV_SS_CPU** (64).
- SCIV_SS_CPU** (pin 65) connects to **R2009** (65) and **SCIV_SS_CPU** (65).
- SCIV_SS_CPU** (pin 66) connects to **R2009** (66) and **SCIV_SS_CPU** (66).
- SCIV_SS_CPU** (pin 67) connects to **R2009**



SWL_PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPB_A_0	in	BCINB	<GPIO>	
GPB_A_1	inout	LAD_0	ESPI_IO_0	LPC Cmd/Addr/Data or eSPI Data [0]
GPB_A_2	inout	LAD_1	ESPI_IO_1	LPC Cmd/Addr/Data or eSPI Data [1]
GPB_A_3	inout	LAD_2	ESPI_IO_2	LPC Cmd/Addr/Data or eSPI Data [2]
GPB_A_4	inout	LAD_3	ESPI_IO_3	LPC Cmd/Addr/Data or eSPI Data [3]
GPB_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPB_A_6	inout	SERIRQ	<GPIO>	
GPB_A_7	inout	REQQAB	<GPIO>	
GPB_A_9	out	LPC_CLKOUT_0	ESPI_CLK	
GPB_A_14	out	SUS_STATB	ESPI_RESETB	
GPB_C_5, SM L0ALR2B	input	ESPI_EN_Pln Strap		eSPI Enable Pin strap; latched at RMRST# deassertion 0: LPC; 1: eSPI
VCCIOGPA	-	3.3V	1.8V	Voltage for all GPIOs in GPB_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

Main Func = PCH



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CPU_(VSS)

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Document Number

Strongbow_KL

Rev

1

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Sheet 21

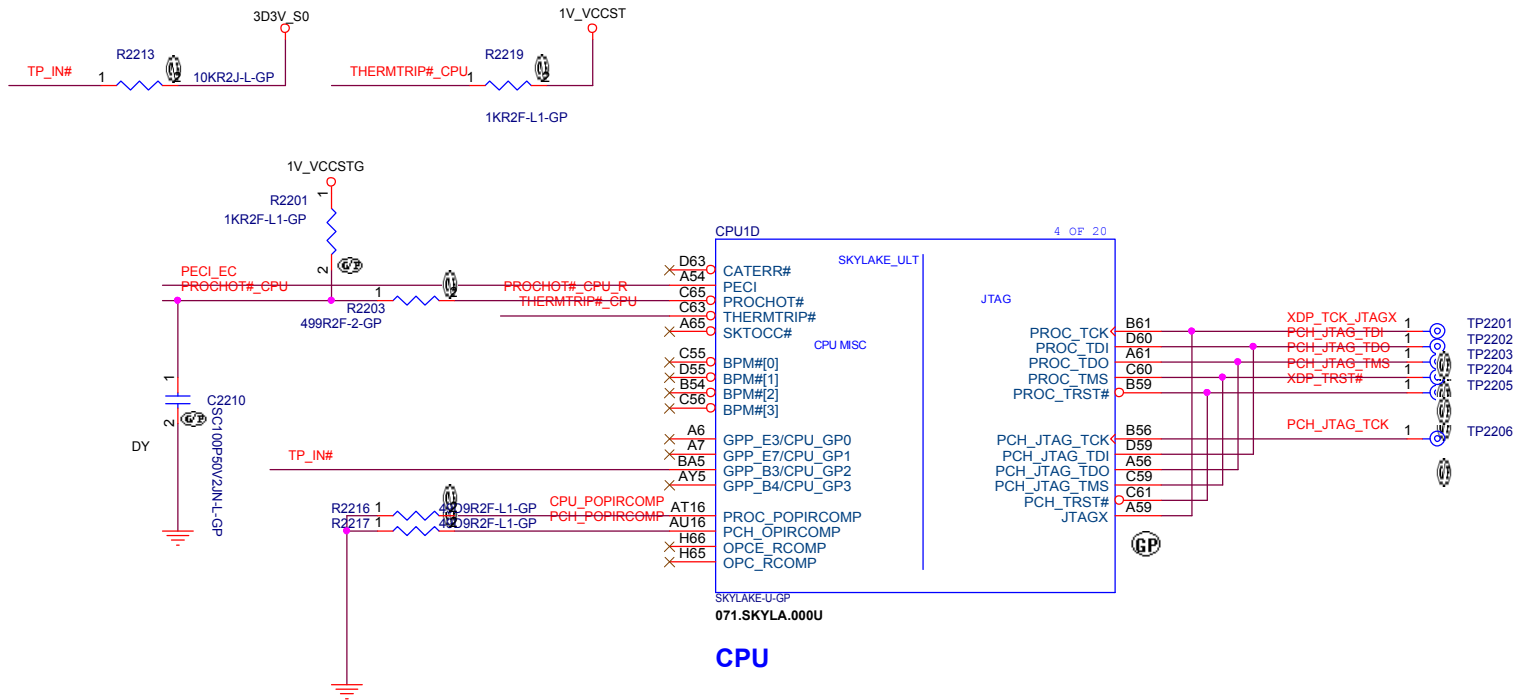
of

106

Main Func = CPU

[24] PECI_EC << >>—
[24,44,46] PROCHOT#_CPU << >>—

[65] TP_IN# >>> —

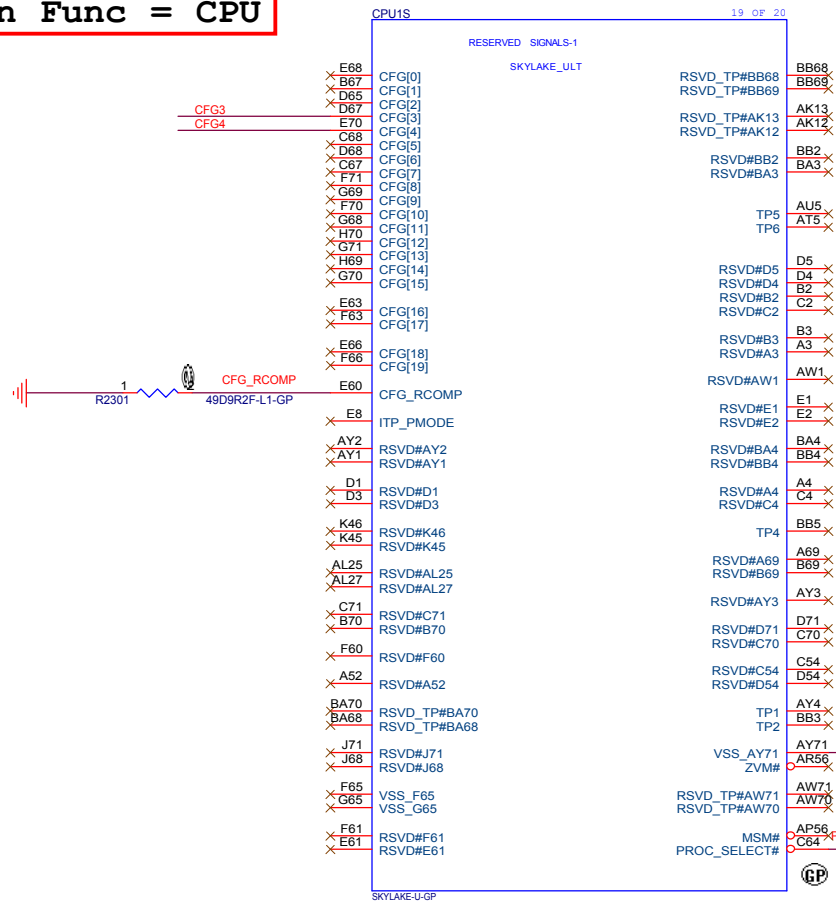


PROCHOT#	Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD 0	SE	All processor lines
THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	0	OD	SE	All processor lines

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Size Custom	Document Number Strongbow KL Rev 1
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Main Func = CPU

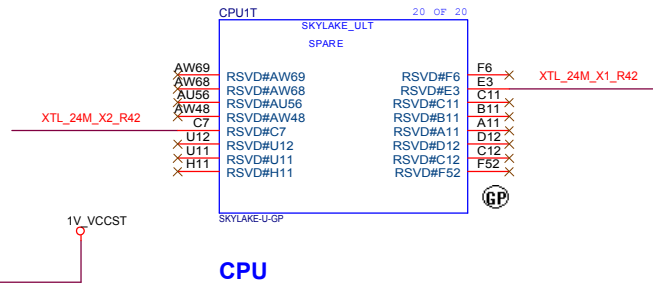


Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

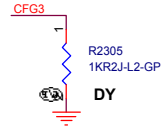
Intel recommends placing test points on the board for CFG pins.

- CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
 - 1 = (Default) Normal Operation;
 - 0 = Stall.
- CFG[1]:** Reserved configuration lane.
- CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
 - 1 = Normal operation
 - 0 = Lane numbers reversed.
- CFG[3]:** Reserved configuration lane.
- CFG[4]:** eDP enable:
 - 1 = Disabled.
 - 0 = Enabled.
- CFG[6:5]:** PCI Express* Bifurcation
 - 00 = 1 x8, 2 x4 PCI Express*
 - 01 = reserved
 - 10 = 2 x8 PCI Express*
 - 11 = 1 x16 PCI Express*
- CFG[7]:** PEG Training:
 - 1 = (default) PEG Train immediately following RESET# de assertion.
 - 0 = PEG Wait for BIOS for training.
- CFG[19:8]:** Reserved configuration lanes.

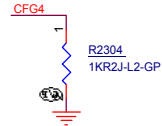
I/O GTL SE



PCH strap pin:



PCH strap pin:

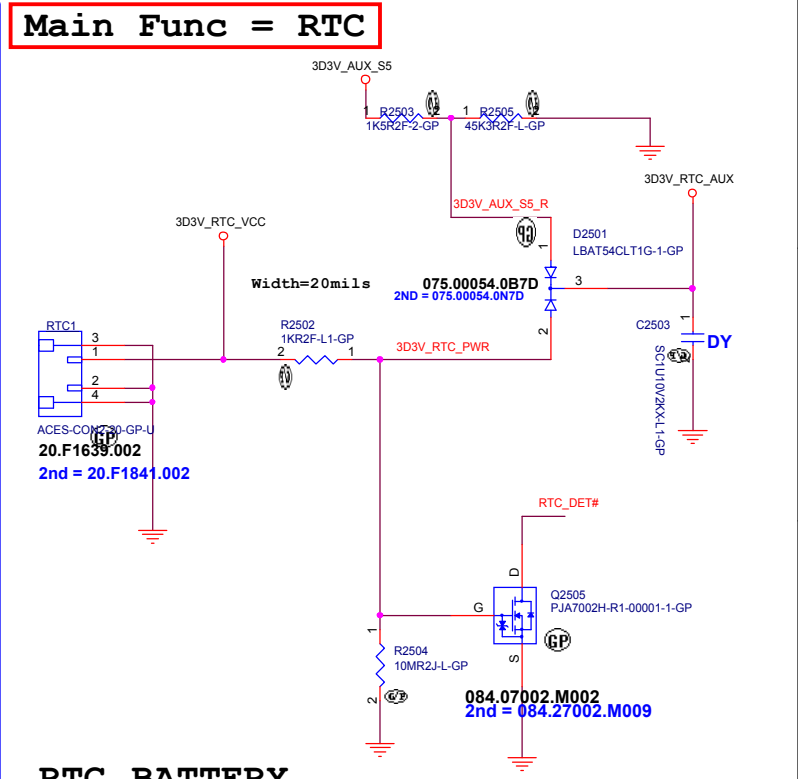
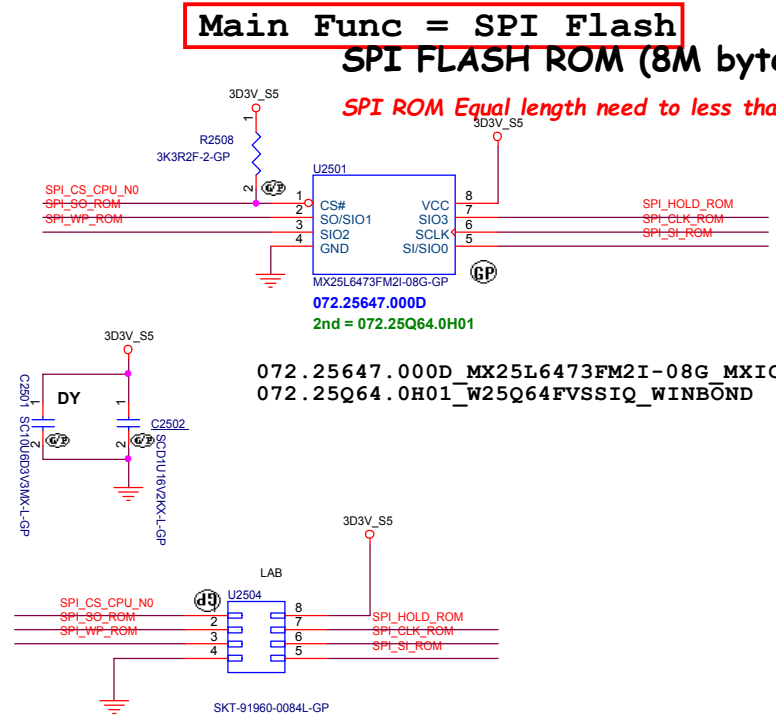
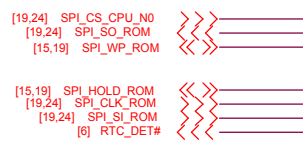


DISPLAY PORT PRESENCE STRAP
CFG[4]
0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

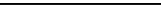
PROC_SELECT#	Processor Select: This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines
--------------	---	--	--	-----	---------------------

<Core Design>

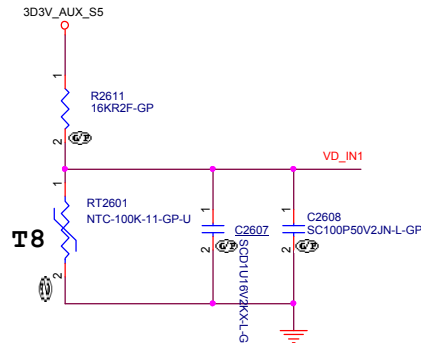
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CPU_RESERVED_CFG	
Title Size Custom Date: Monday, January 15, 2018	Document Number Strongbow_KL Sheet 23 of 106
Rev 1	



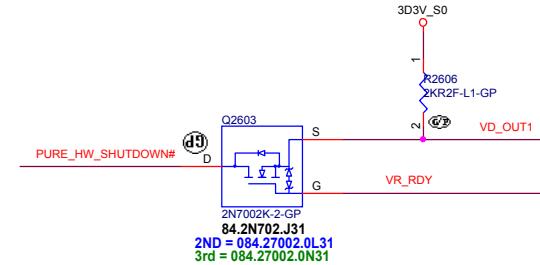
RTC BATTERY
1st= TBD
2nd= TBD

<Core Design>			
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Title			
Flash(KBC+PCH)/RTC			
Size Custom	Document Number	Strongbow KL	Rev 1
Date: Monday, January 15, 2015		Sheet 25 of	106

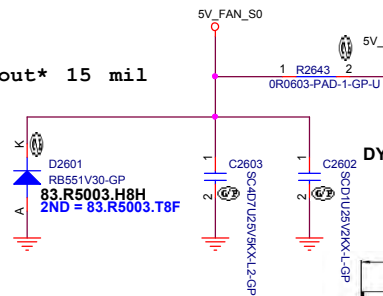
SSID = Thermal



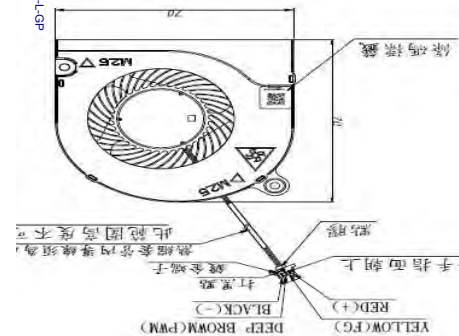
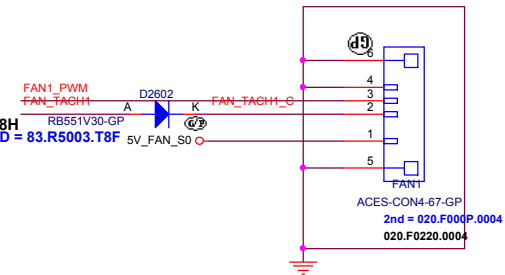
RT2601 close CPU and Vcore chock
VD_IN1 trace 10 mli



Layout 15 mil



83.R5003.H8H
2ND = 83.R5003.T8F



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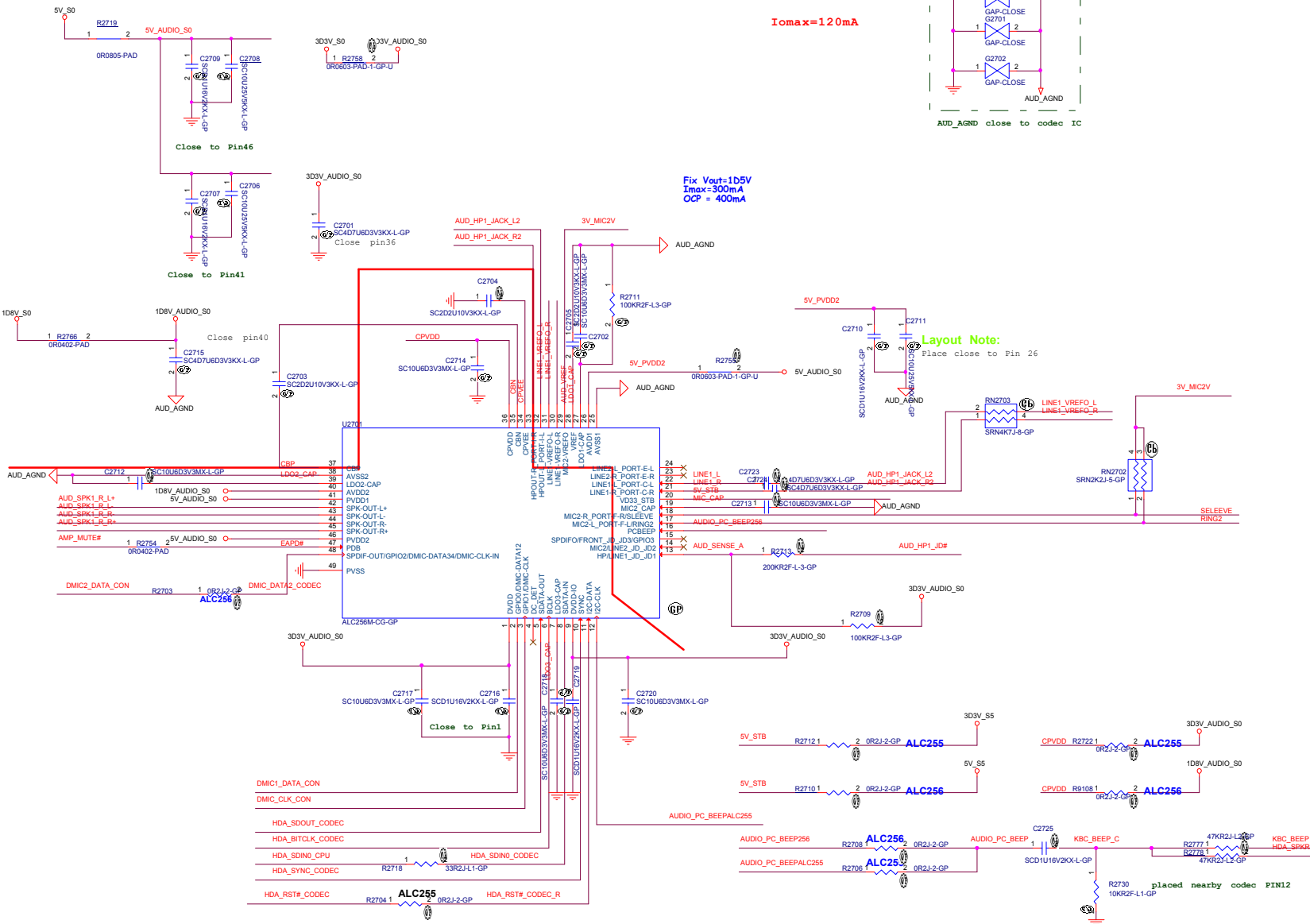
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Thermal 7718/Fan Controllor P2793			
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Custom	Strongbow KL		1
Date:	Monday, January 15, 2018		Sheet 26 of 106


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[18] HDA_BITCLK_CODEC _____
[18] HDA_SYNC_CODEC _____
[18] HDA_SSDIN_CPU _____
[18] HDA_SSDOUT_CODEC _____
[18] HDA_RST#_CODEC <<<-

[24] AMP_MUTE# _____
[55] DMIC2_DATA_CON _____
[55] DMIC2_CLK_CON _____
[55] DMIC1_DATA_CON _____
[29] AUD_HP1_JACK_L2 _____
[29] AUD_HP1_JACK_R2 _____
[29] AUD_HP1_JOM _____
[29] RING2 _____
[29] SELEEVE _____
[24] KBBC_RESET _____
[15,19] HDA_SPKR _____
(29,8) AUD_SPK1_R_L+ _____
(29,8) AUD_SPK1_R_L- _____
(29,8) AUD_SPK1_R_R+ _____
(29,8) AUD_SPK1_R_R- _____

```



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Audio Codec ALC256			
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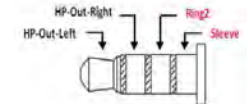
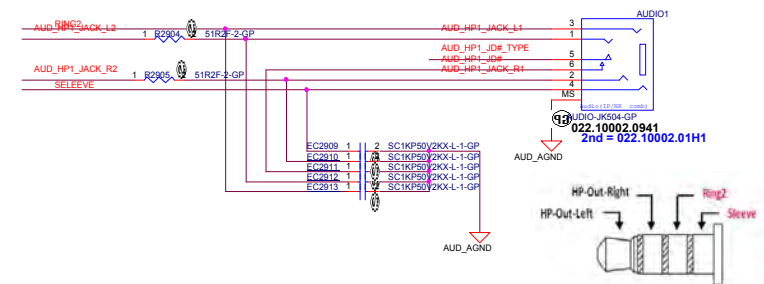
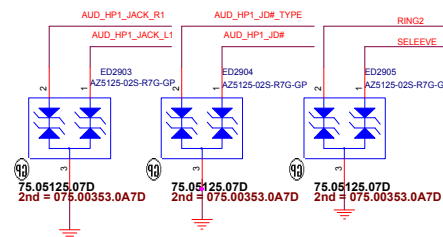
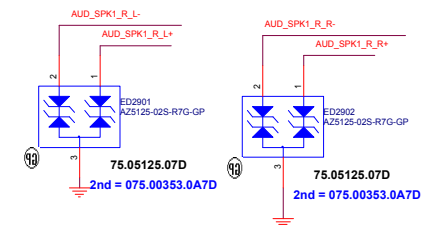
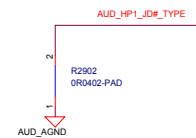
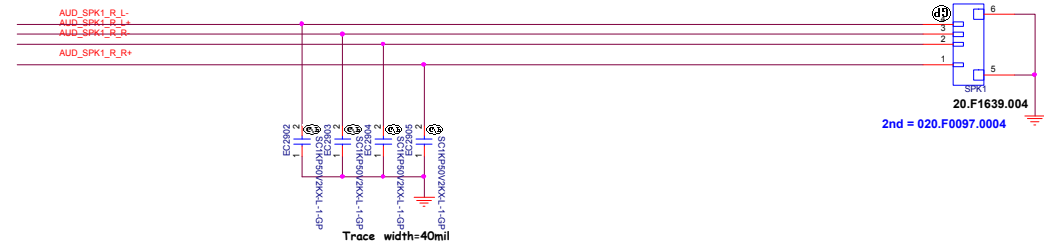
Strongbow KL

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1

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Speaker



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Title			
Speaker/HPMIC			
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Title

(LAN+VGA) CONNECTOR

Size
A4

Document Number

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Title			
RTS5170(CARD READER)			
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SSID = SDIO

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[16] USB1_USB20_N << >> _____
[16] USB1_USB20_P << >> _____
[24,66] USB_PWR_EN << >> _____

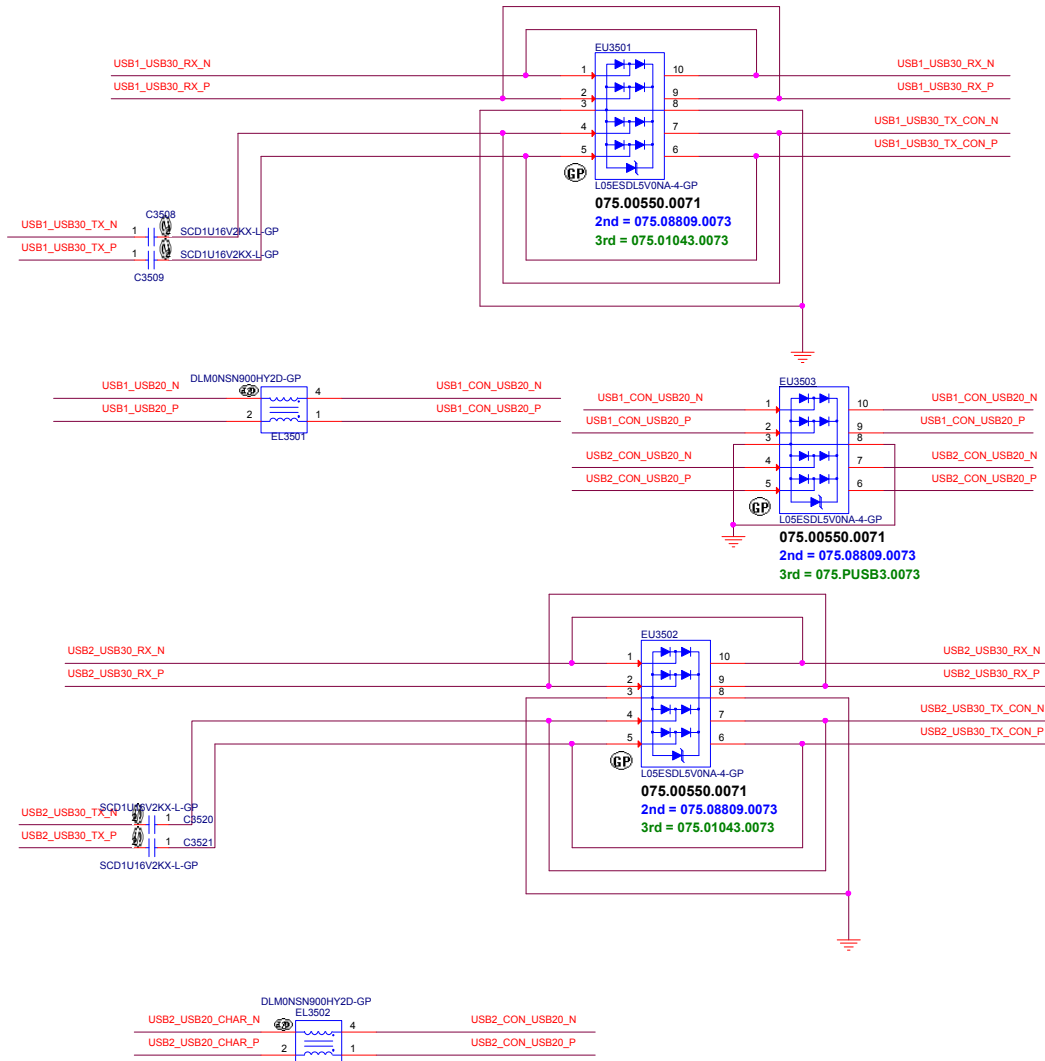
[16] USB1_USB30_RX_N << >> _____
[16] USB1_USB30_RX_P << >> _____
[16] USB1_USB30_TX_N << >> _____
[16] USB1_USB30_TX_P << >> _____

[89] USB1_CON_USB20_N << >> _____
[89] USB1_CON_USB20_P << >> _____

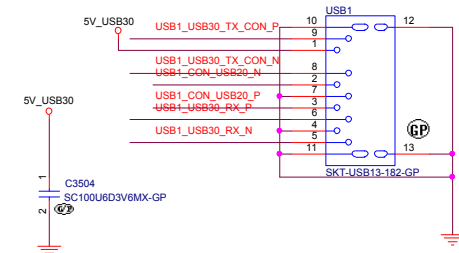
[36] USB2_USB20_CHAR_N << >> _____
[36] USB2_USB20_CHAR_P << >> _____

[16] USB2_USB30_RX_N << >> _____
[16] USB2_USB30_RX_P << >> _____
[16] USB2_USB30_TX_N << >> _____
[16] USB2_USB30_TX_P << >> _____

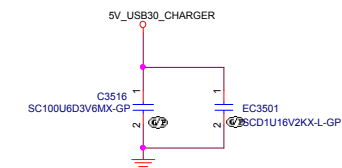
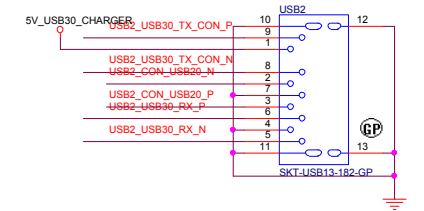
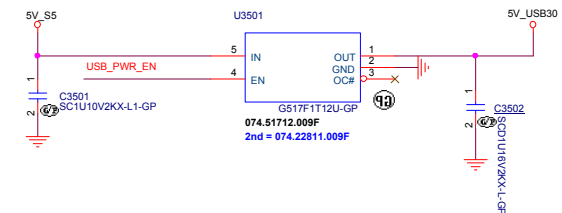
[89] USB2_CON_USB20_N << >> _____
[89] USB2_CON_USB20_P << >> _____



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



High Active 2A

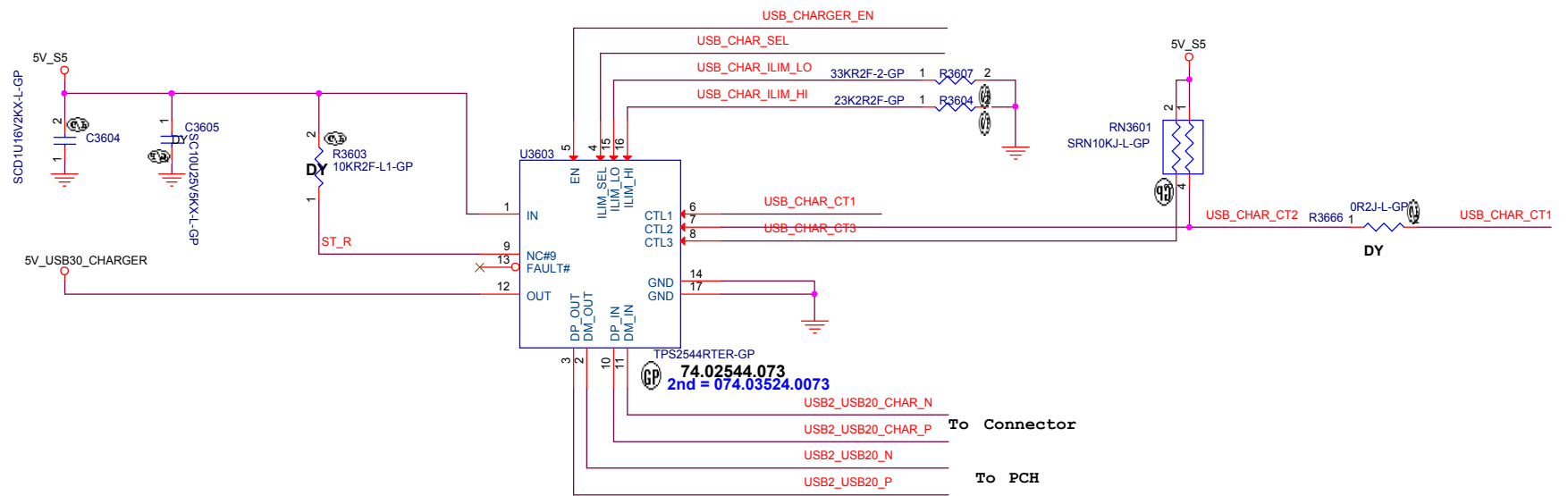


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Title		USB 3.0	
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[16] USB2_USB20_N << >> _____

[16] USB2_USB20_P << >> _____



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP Auto	ILIM_HI	Data Lines
0	1	1	X			Disconnected
0	1	0	0	SDP1	ILIM_LO	Data Lines
0	1	0	1		ILIM_HI	connected
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 ⁽¹⁾	ILIM_LO	Connected
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	Data Lines Connected

S0 state

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Size <div>A4</div>	Document Number <div>Strongbow KL</div>	Rev <div>1</div>
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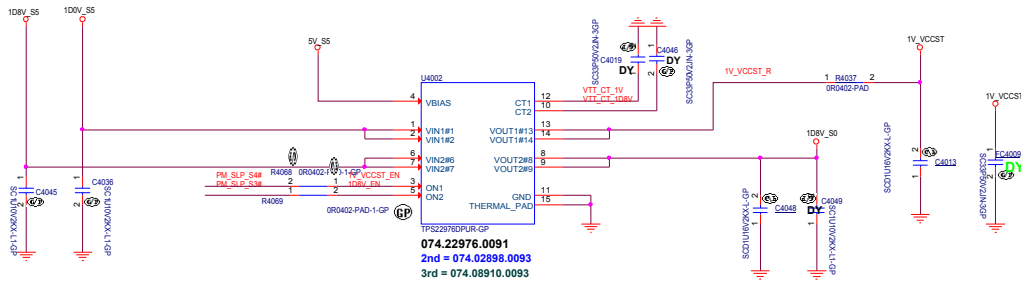
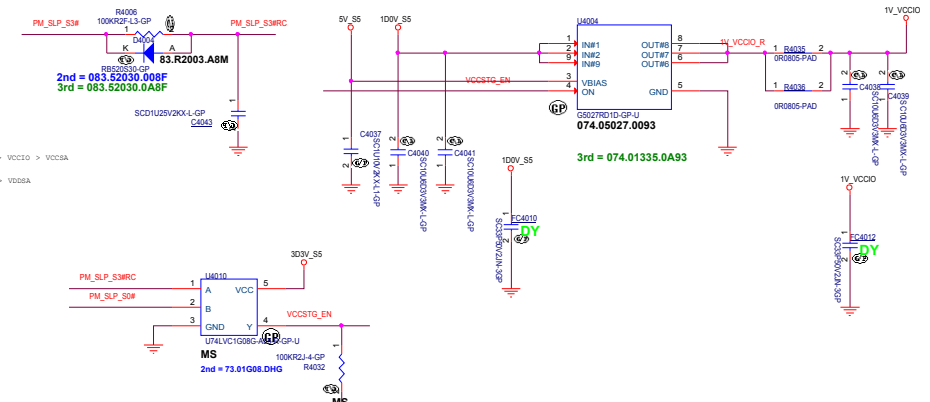
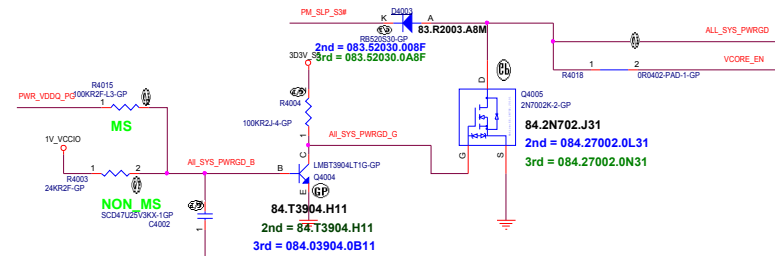

```

[20,46] VR_RDY >>> _____
[20,24,58] PM_SLP_S3# <<< >>> _____
[20] PCH_PWROK <<< _____
[24] 3V_S5_EN >>> _____
[45] 3V_EN <<< _____

[24,26] PURE_HW_SHUTDOWN# >>> _____
[20,24] ALL_SYS_PWRGD <<< _____
[46] VCORE_EN <<< _____
[20,24,51] PM_SLP_S4# >>> _____
[20,24,60,91] PM_SLP_S0# >>> _____

[51] PWR_VDDQ_PG >>> _____

```



```

1126 Simon
Turning RC for DRAM
VCCIO = SLP_S3
2.5v = SLP_S4
VCCIO = SLP_VCCA

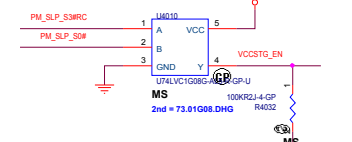
Sequence should
SLP_S4 > 2.5V > VDDQ > VCCIO > VCCA

DOR3 =
SLP_S4 > VDDQ > VDDIO > VDDSA

DOR4
R4006 = 100K
C4043 = 0.22u
DS702 = stuff

DOR3
R4006 = 33K
C4043 = 0.1u
DS702 = stuff

```



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Title	Power Plane Enable & SEQUENCE
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Title

DCIN JACK

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A4

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Adaptor in to generate DCBATOUT



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Title

BATT CONN

Size

Document	Number
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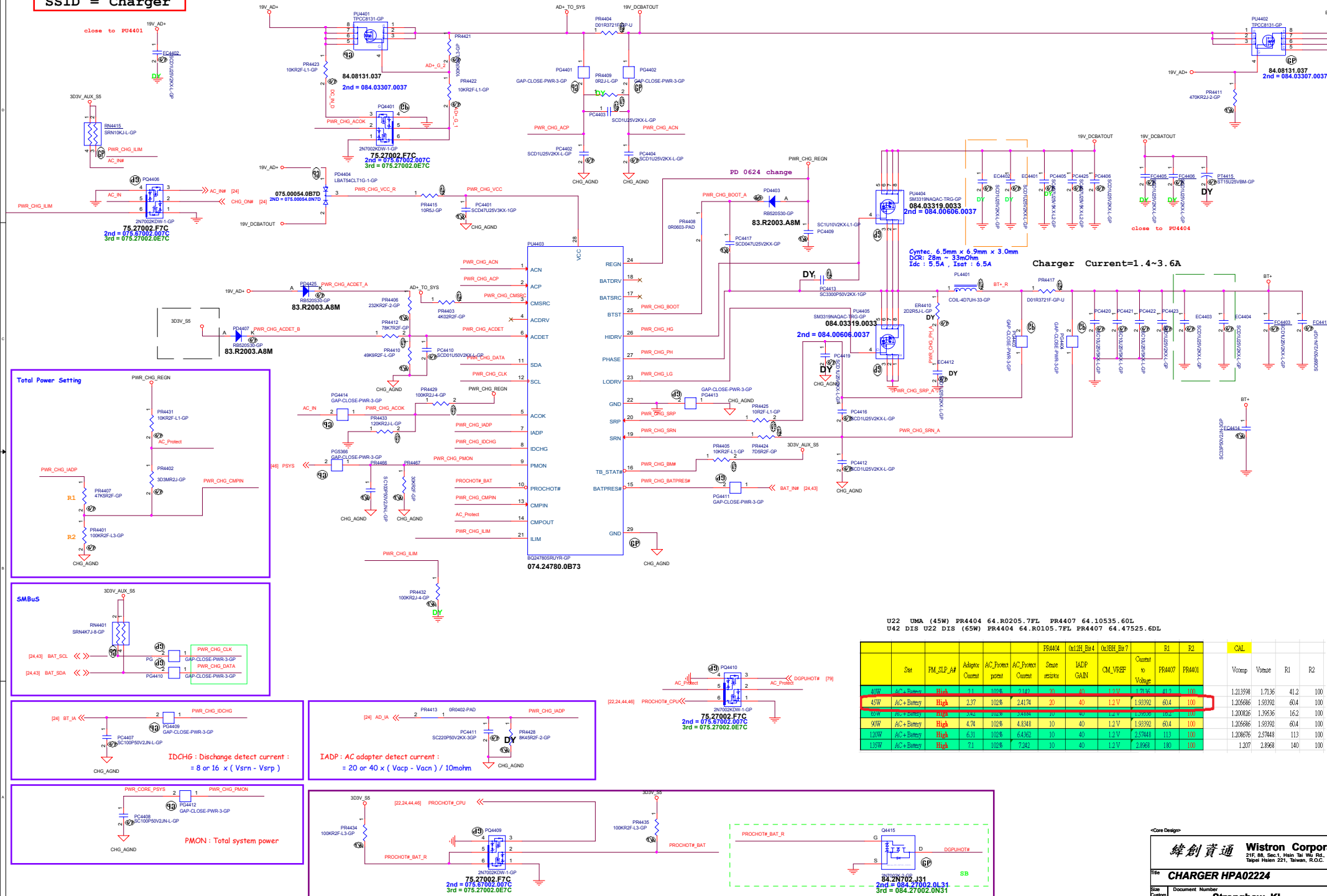
Strongbow KL

Date: Monday, January 15, 2018

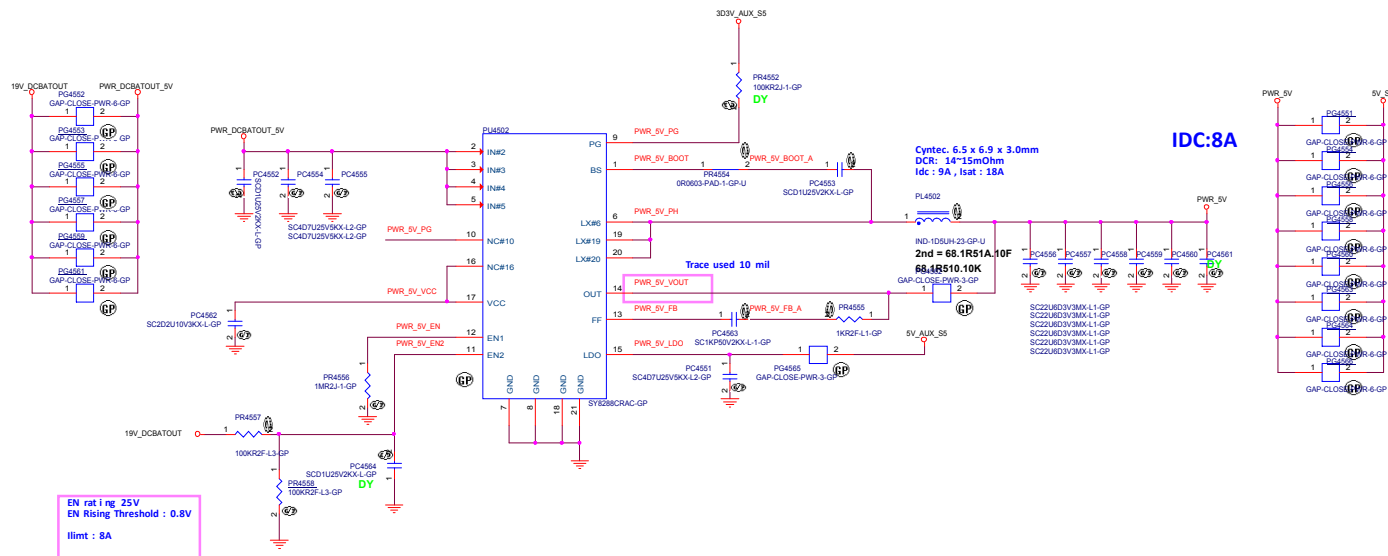
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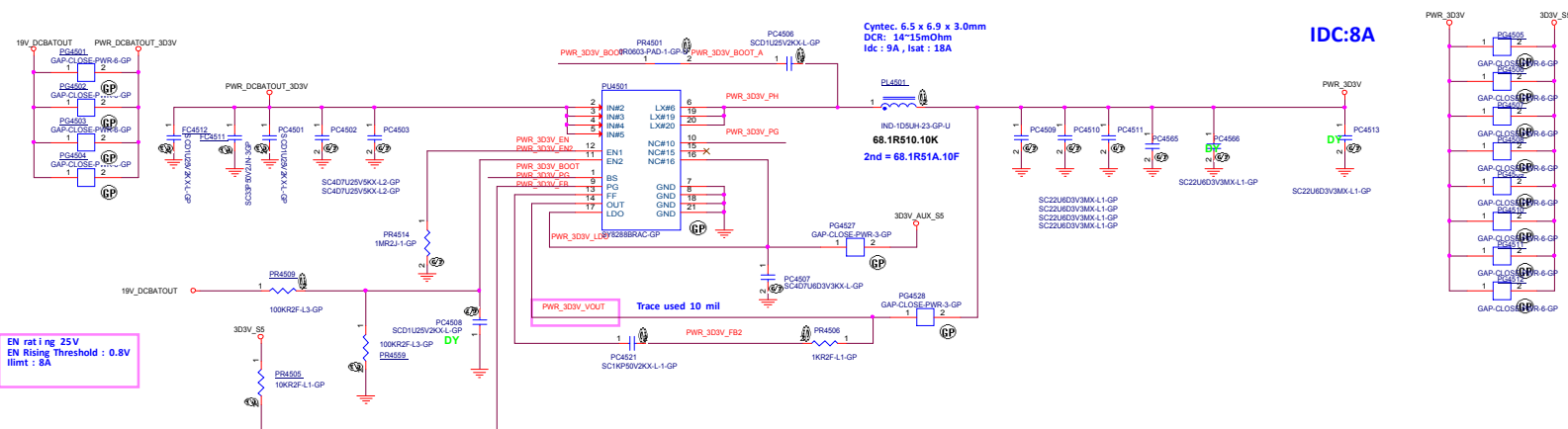
SSID = Charger



[24] 5V EN >>> 2 PR4517 1 PWR_5V_EN



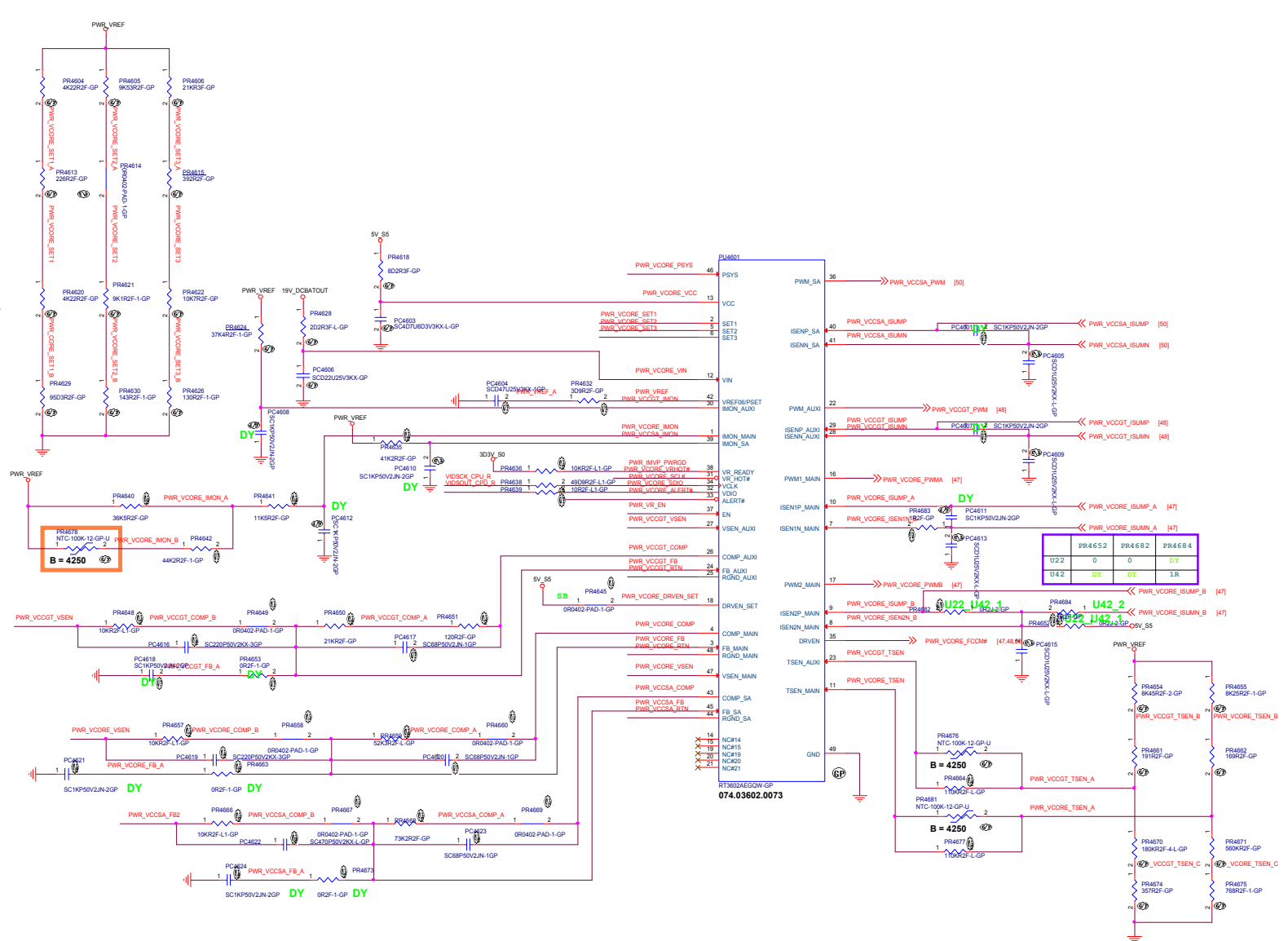
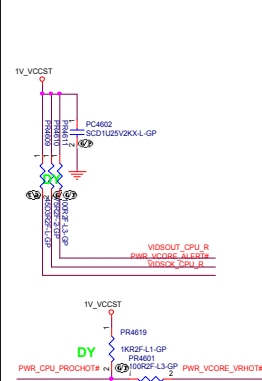
40] 3V EN >>> 2 PR4515 1 PWR_3D3V_EN



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RT6575D 5V3D3V			
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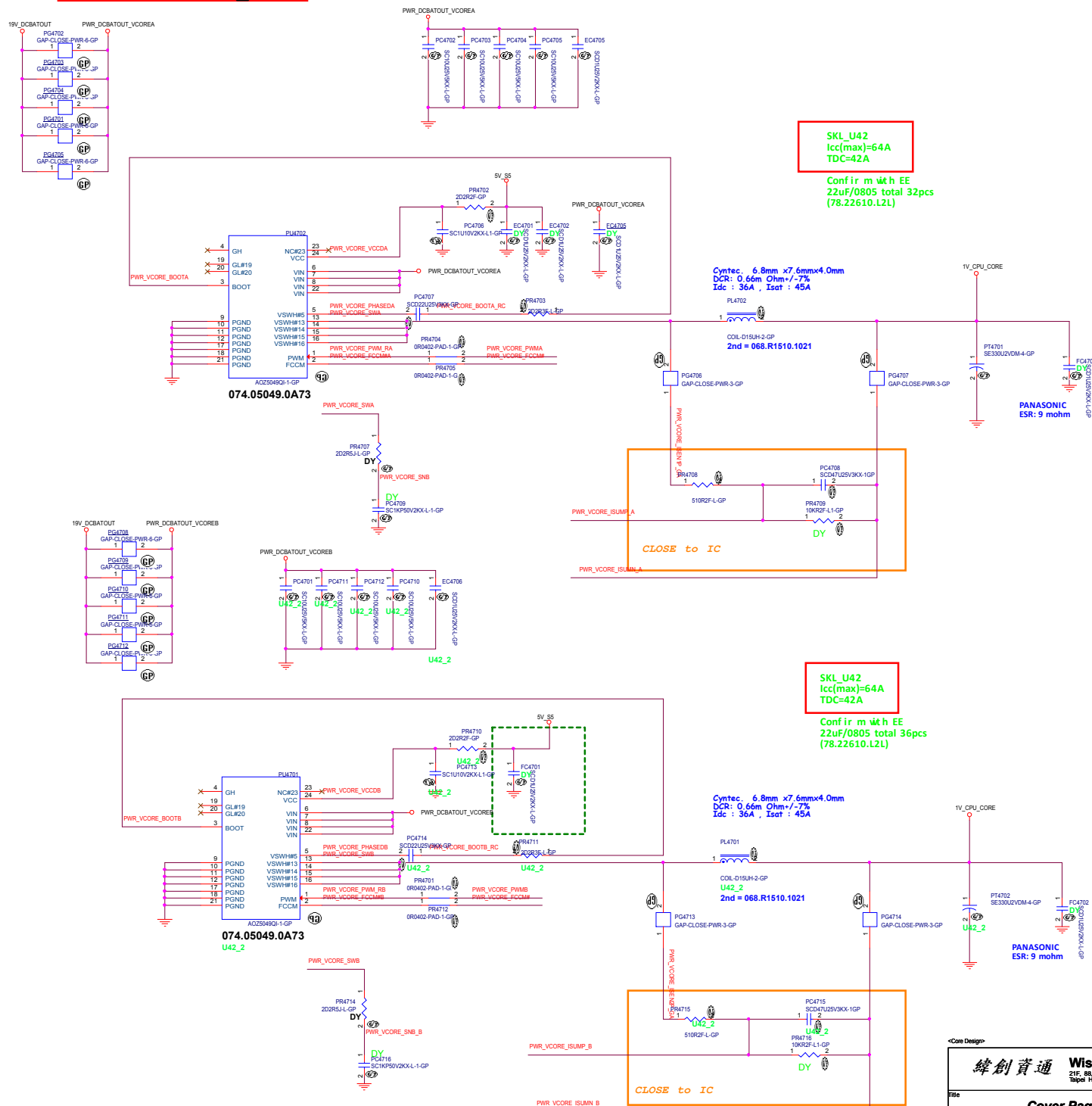

```
Main Func = CPU_CORE
```



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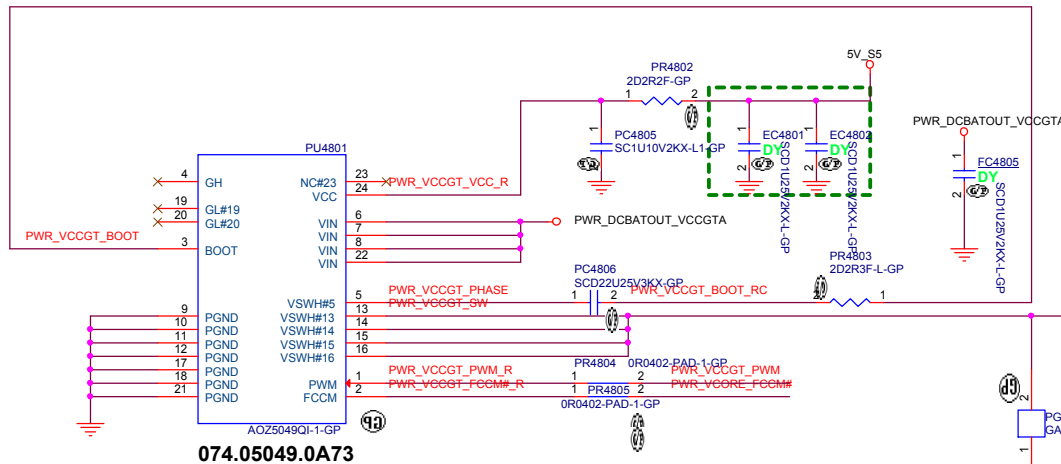
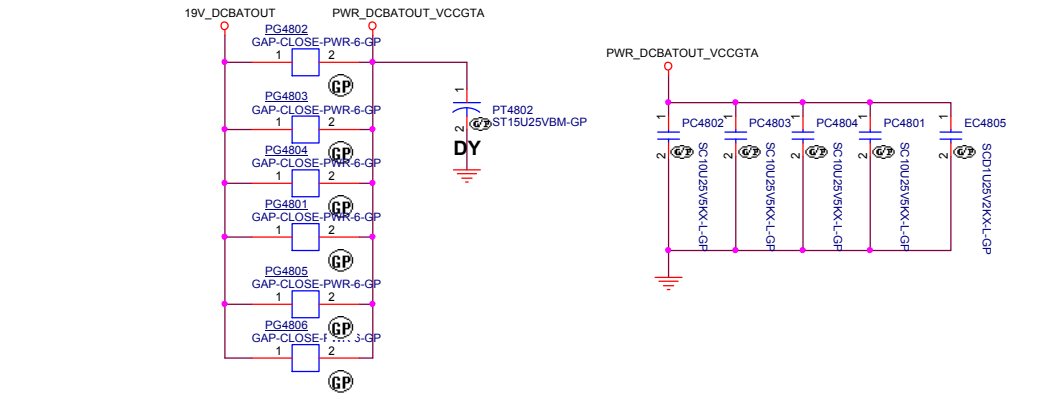
Main Func = CPU_CORE

[46] PWR_VCORE_PVMA
 [46,48,50] PWR_VCORE_FCCM
 [46] PWR_VCORE_ISUMP_A
 [46] PWR_VCORE_ISUMP_B
 [46] PWR_VCORE_ISUMN_A
 [46] PWR_VCORE_ISUMN_B

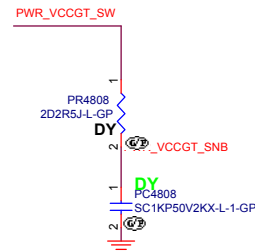


Main Func = CPU_CORE

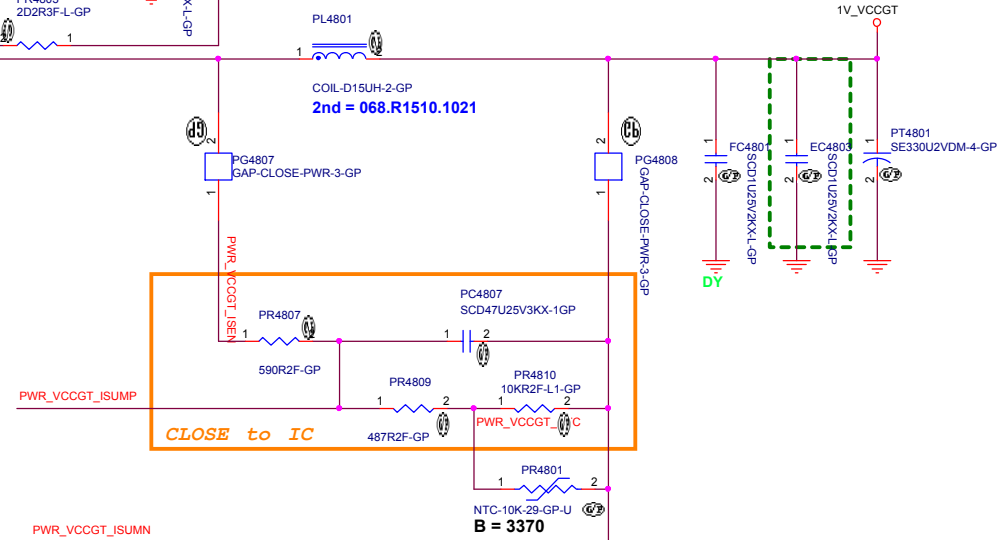
[46] PWR_VCCGT_PWM
[46.47.50] PWR_VCORE_FCCM#
[46] PWR_VCCGT_ISUMP
[46] PWR_VCCGT_ISUMN



074.05049.0A73



Cynotec 6.8mm x7.6mmx4.0mm
DCR: 0.66m Ohm+/-7%
Idc : 36A , Isat : 45A



SKL_U42
Icc(max)=28A
TDC=12A

Confir m with EE
22uF/0805 total 26pcs
(78.22610.L2L)

<Core Design>

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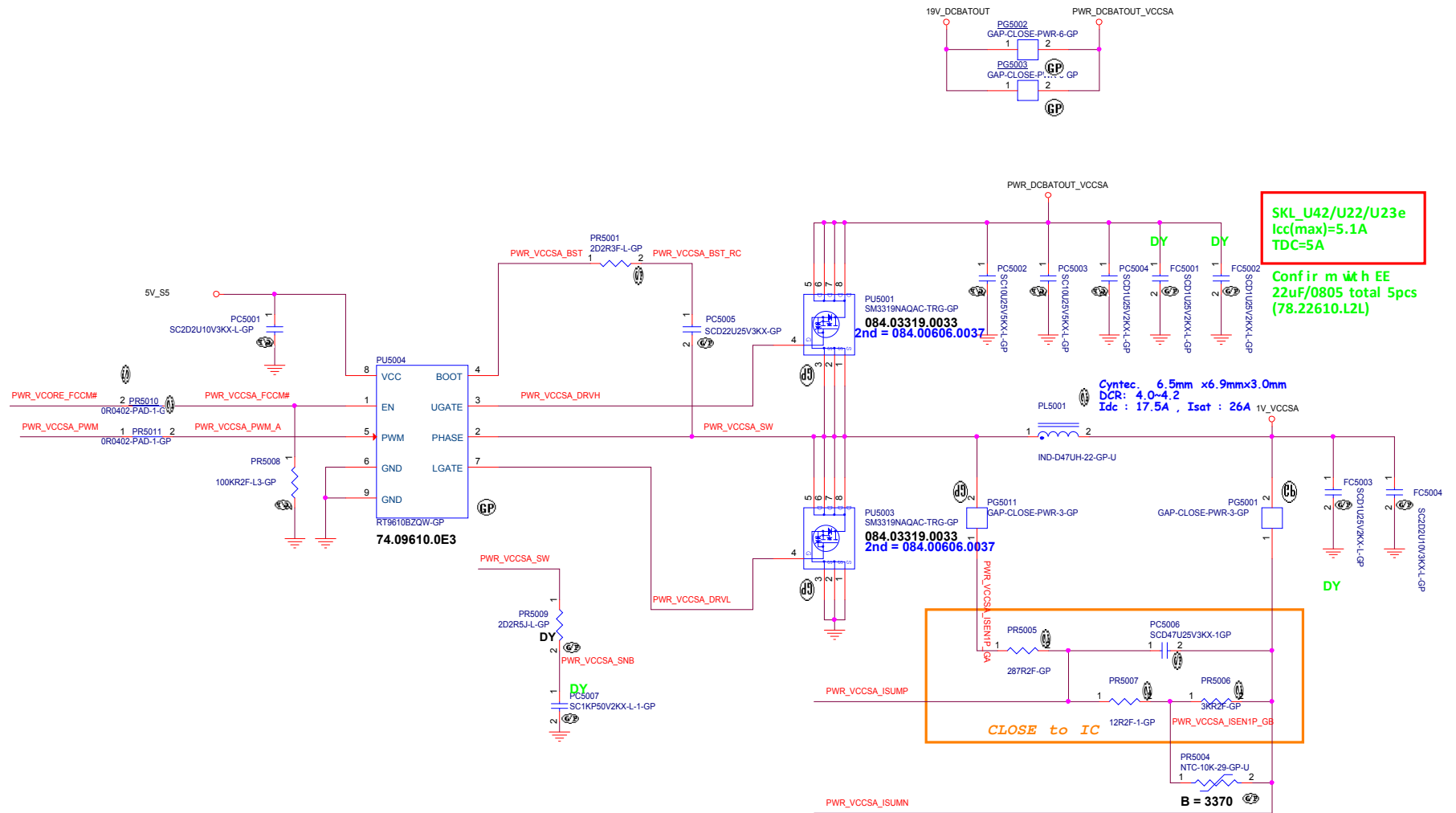
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Main Func = CPU_CORE

[46,47,48] PWR_VCORE_FCCM# >>>
[46] PWR_VCCSA_PWM >>>
[46] PWR_VCCSA_ISUMP <<<
[46] PWR_VCCSA_ISUMN <<<



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[53] 1D8V_S5_PWRGD >>_____



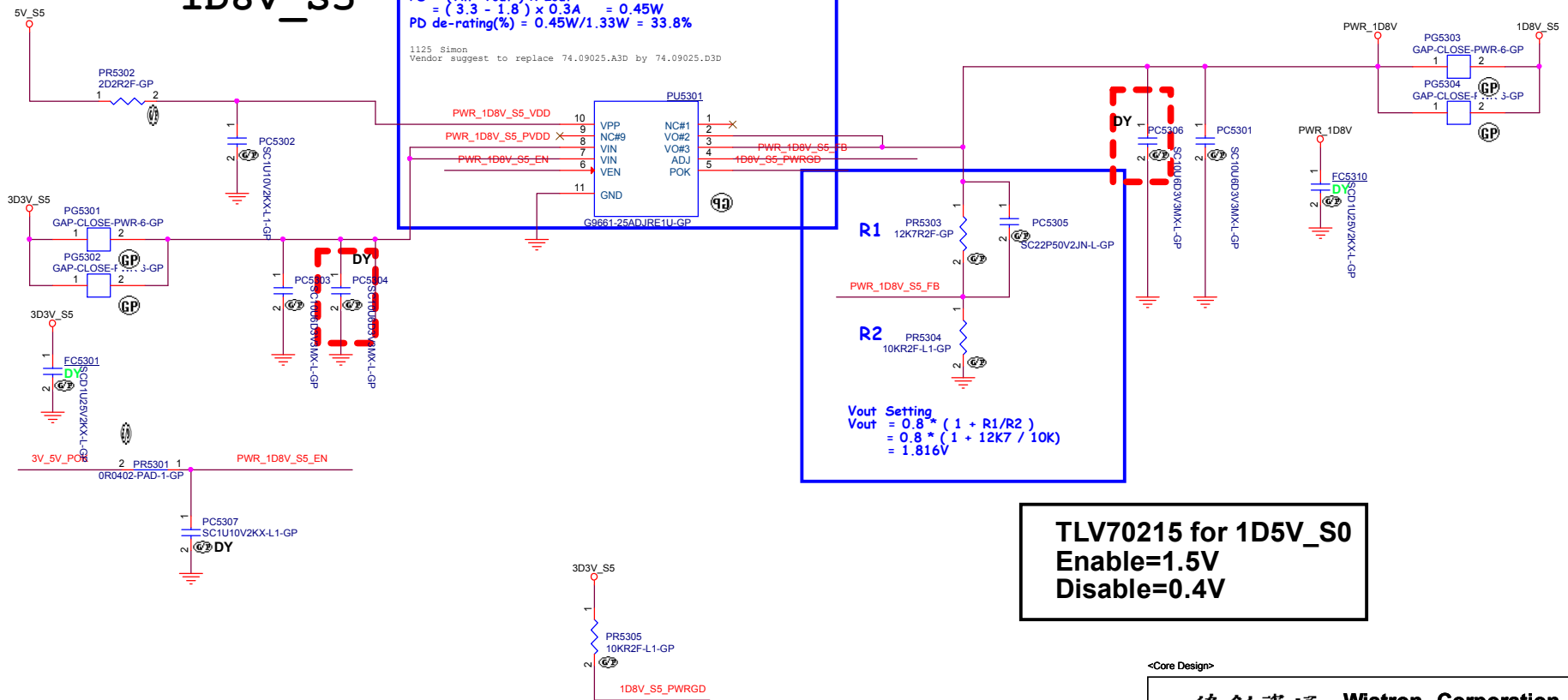
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Title			
RT8237 1D0V S5			
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1D8V S5

$$\begin{aligned} PD &= (V_{in} - V_{out}) \times I_{out} \\ &= (3.3 - 1.8) \times 0.3A = 0.45W \\ PD \text{ de-rating}(\%) &= 0.45W / 1.33W = 33.8\% \end{aligned}$$

```
1125 Simon
Vendor suggest to replace 74.09025.A3D by 74.09025.D3D
```



TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

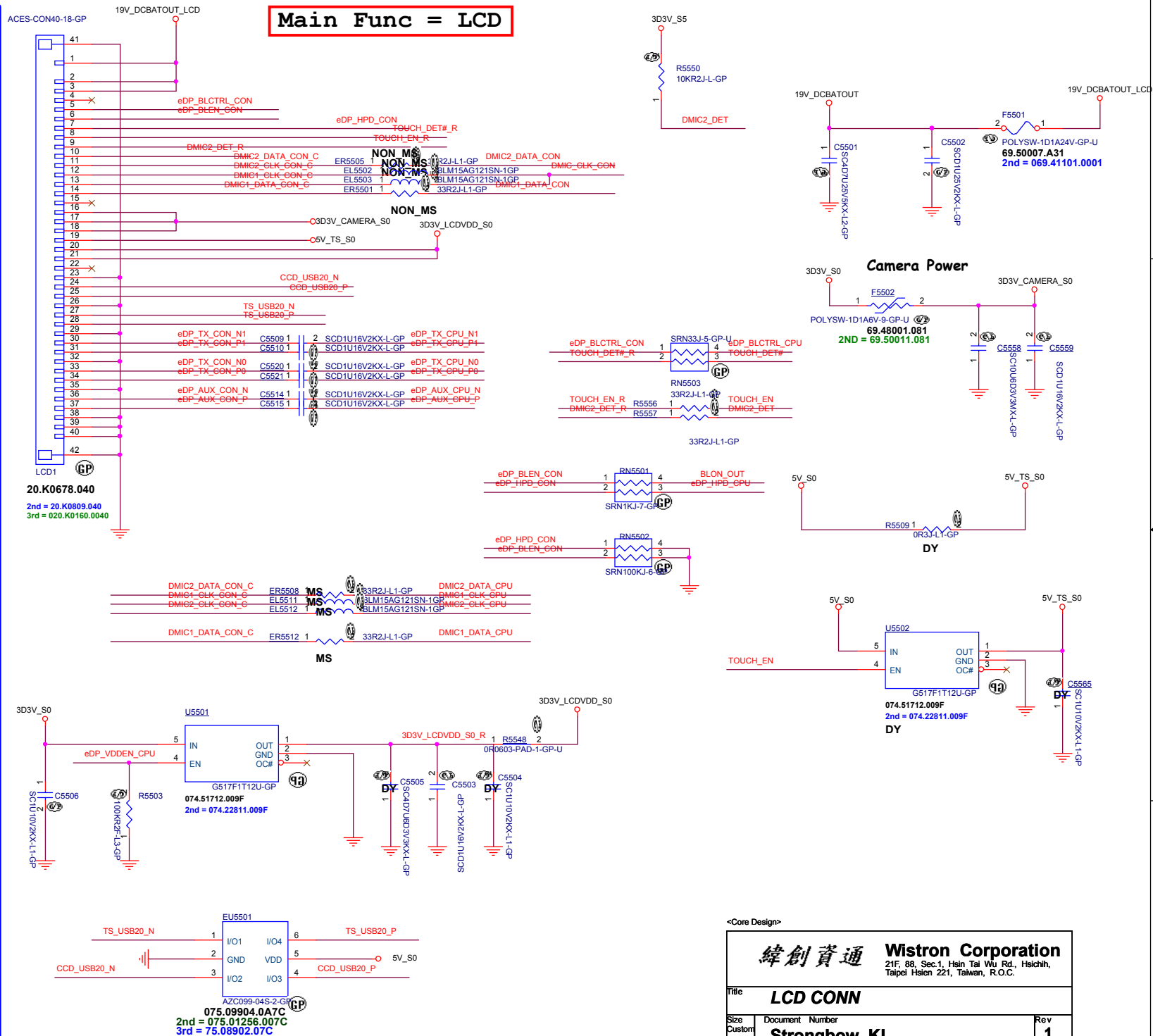
Title	RT5797_1D8V
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Title			
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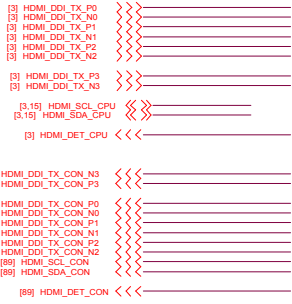


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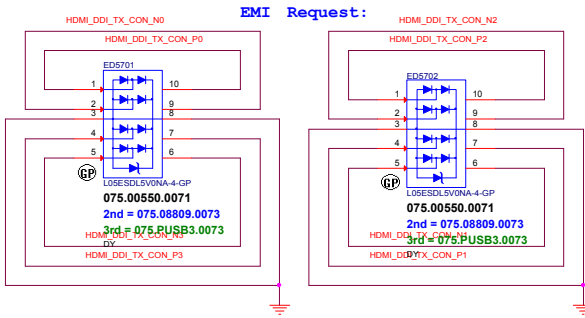
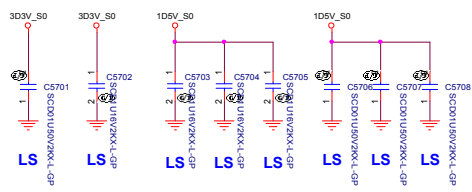
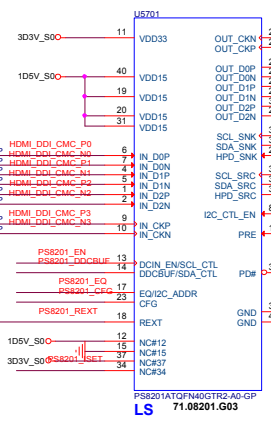
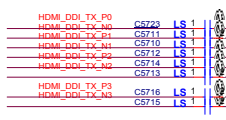
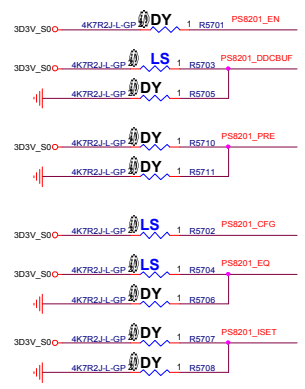
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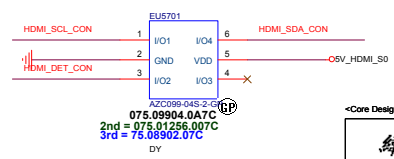
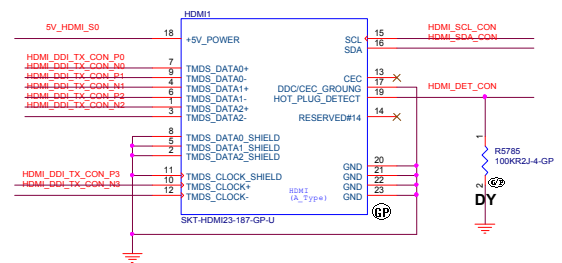
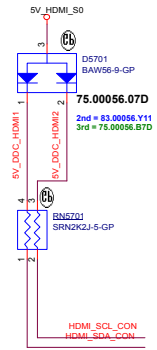
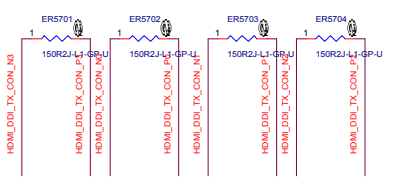


SSID = VIDEO

HDMI 1.4 & CONNECTOR



HDMI CONN



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HDMI Level Shifter/Connector

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SSID = SATA



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HDD

2

Strongbow_KL

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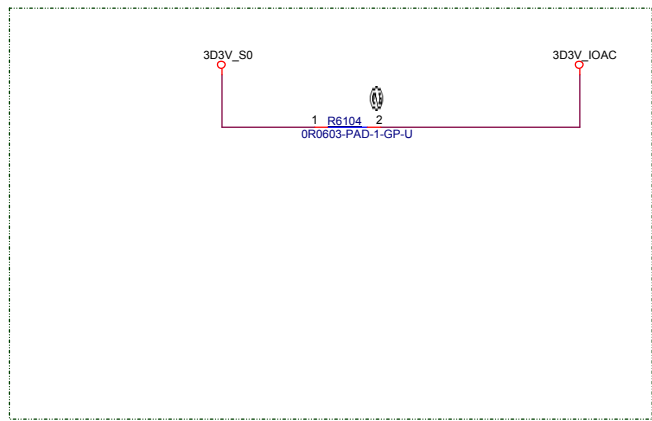
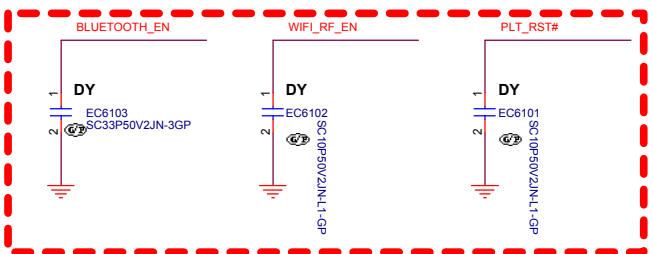
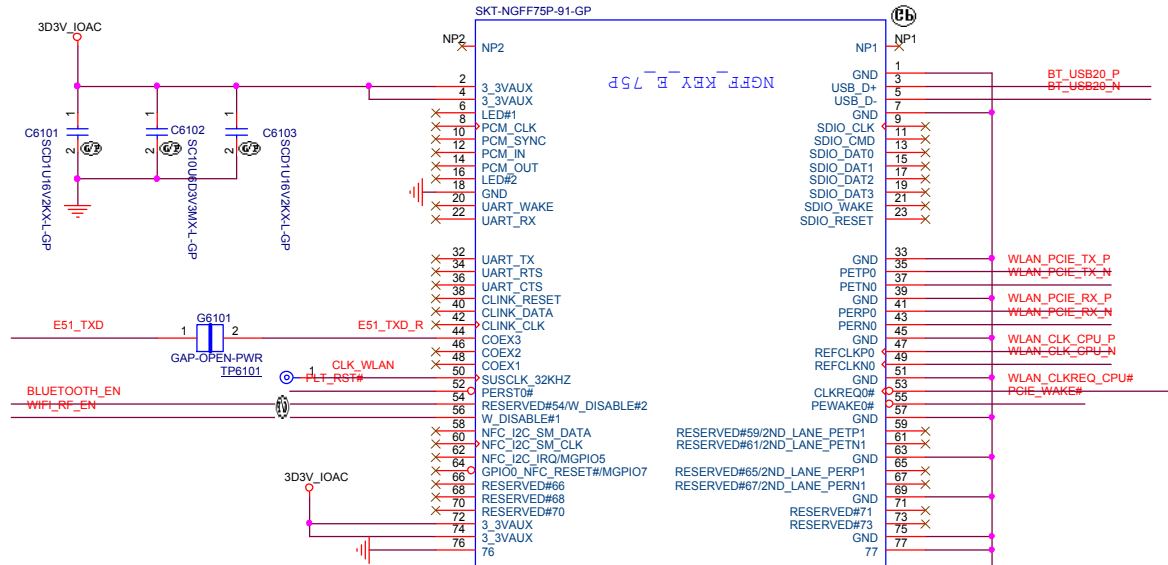
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

[24,61,68] E51_TXD >>> _____
[16,89] BT_USB20_P <<< _____
[16,89] BT_USB20_N <<< _____
[24,61,68] E51_TXD >>> _____
[24,89] BLUETOOTH_EN >>> _____
[24,89] WIFI_RF_EN <<< _____
[20,24,63,68,79,89,91] PLT_RST# >>> _____

[16,89] WLAN_PCIE_TX_P >>> _____
[16,89] WLAN_PCIE_TX_N >>> _____
[16,89] WLAN_PCIE_RX_P <<< _____
[16,89] WLAN_PCIE_RX_N <<< _____
[17,89] WLAN_CLK_CPU_P >>> _____
[17,89] WLAN_CLK_CPU_N >>> _____

[20,63,89] PCIE_WAKE# <<< _____
[17,89] WLAN_CLKREQ_CPU# <<< _____



WLAN1
062.10003.0611
2nd = 062.10003.0C11
3rd = 062.10003.0E31
4th = 062.10003.0C61

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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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SSID = mSATA

Mini Card Connector(mSATA)

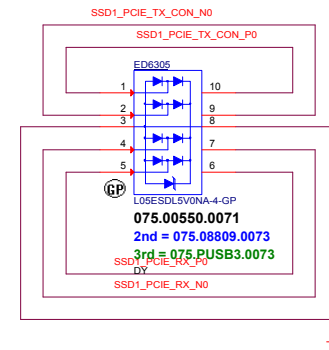
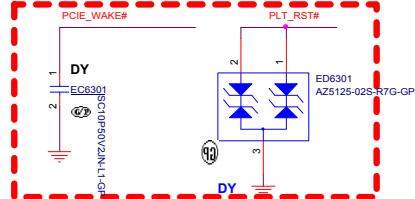
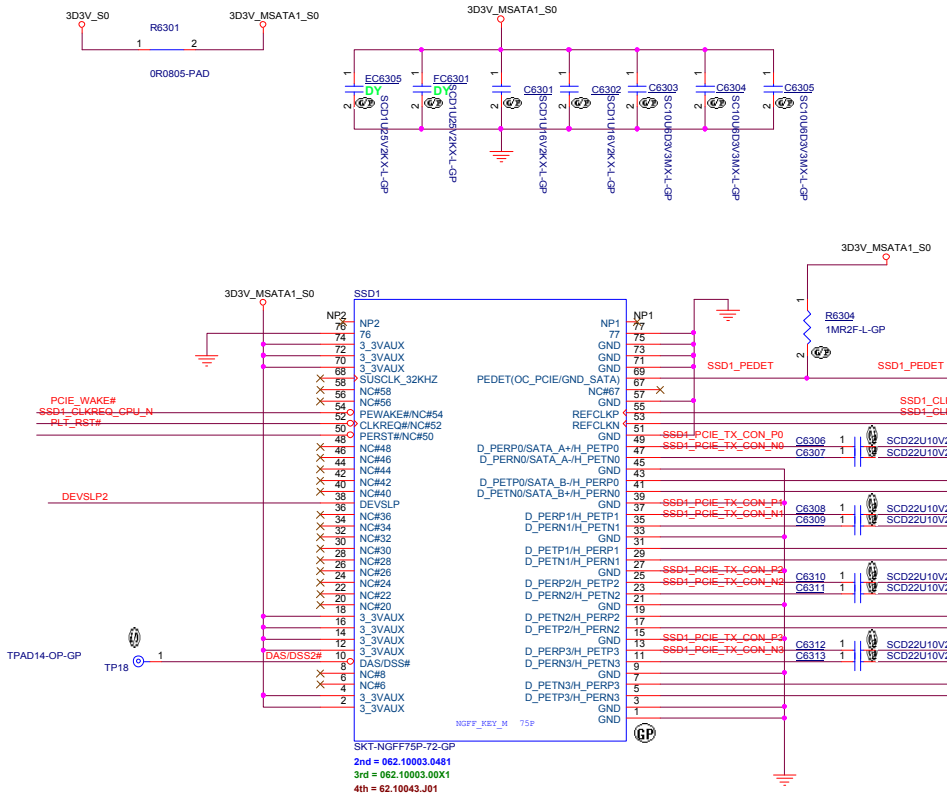
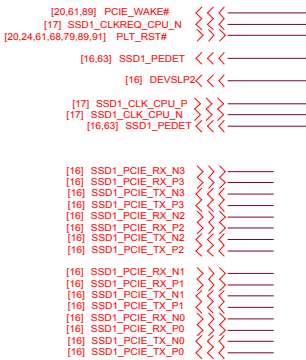


Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter

PCIe Link Details		PCIe® Controller #1				PCIe® Controller #2				PCIe® Controller #3			
Flex I/O Lane #	PCIe Lane #	5	6	7	8	9	10	11	12	13	14	15	16
Base-U		RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12
Premium-U		RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12
Premium-T		RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 3 / SATA	PCI Express® Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe® Gen 2 / SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe® Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: Refer to Chapter 3, "General Differential Signals Design Guidelines," along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe® lane that needs to support either **PCIe® Gen 2 devices** or **PCIe® Gen 3 devices**, follow the PCIe® Gen 3 / SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes			Module Type and Main Host Interface ¹	Port Configuration ²
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 68)	CONFIG_2 (Pin 75)		
0	GND	GND	GND	SSD - SATA	N/A
1	GND	NC	GND	SSD - PCIe	N/A

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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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<div> <div>Title</div> <div>LED Bard/Power Button</div> </div>	
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<div> <div>Date:</div> <div>Thursday, January 11, 2018</div> </div>	
<div> <div>Sheet</div> <div>64</div> <div>of</div> <div>106</div> </div>	


```
[24.89] KSI[0..7] >>> _____
[24.89] KSOQ[0..17] <<< _____

[24] EC_TPCLK <<< _____
[24] EC_TPDATA <<< _____

[24.89] FUN_OFF# >>> _____

[89] EC_TP_CLK_C <<< _____
[89] EC_TP_DATA_C <<< _____
[89] I2C1_DATA_TP <<< _____
[89] I2C1_CLK_TP <<< _____

4] PTP_PWR_EN >>> _____
[22] TP_IN# <<< _____

[24.89] EC_TP_IN# <<< _____
[24.89] EC_TP_IN_R# <<< _____

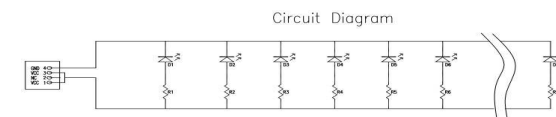
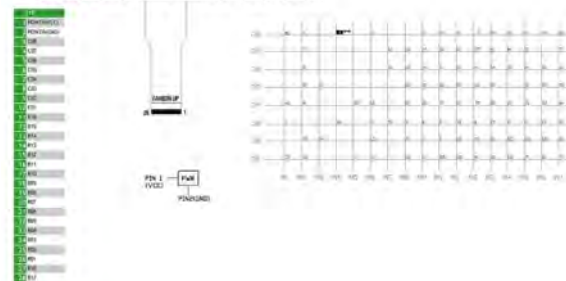
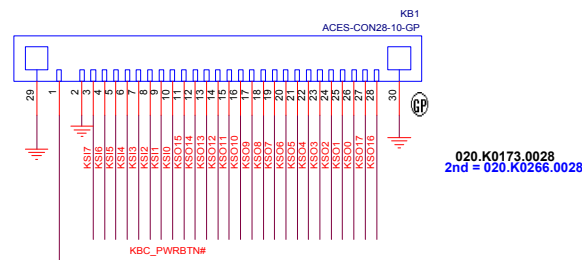
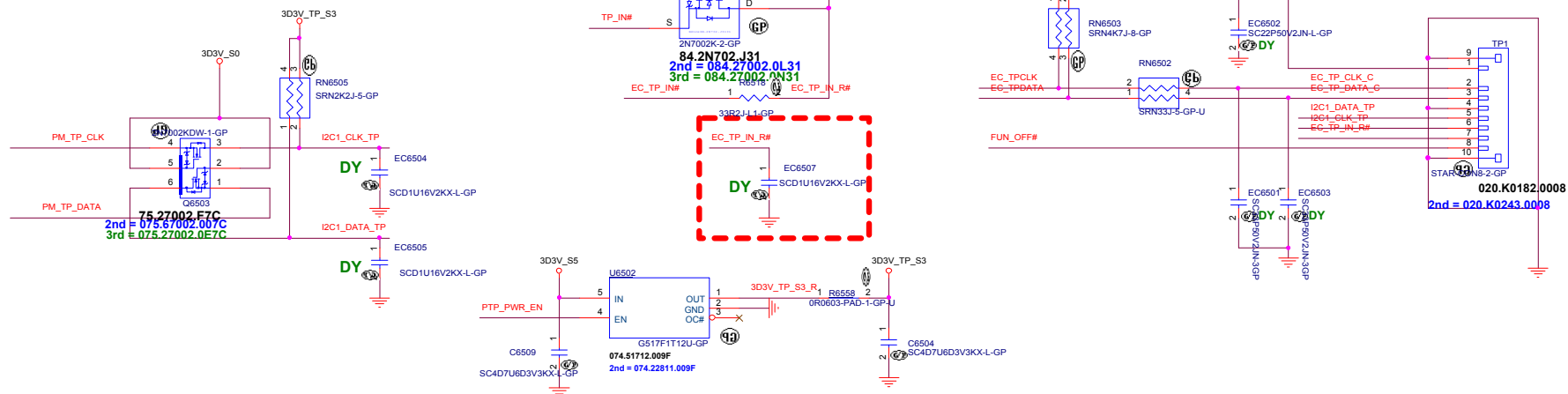
[6] PM_TP_CLK <<< _____
[6] PM_TP_DATA <<< _____

[24] KB_BL_PWM >>> _____

[24] KB_BL_DET <<< _____

[89] KB_BL_DET_R# <<< _____
[89] KB_LED_PWM# <<< _____

4,64.89] KBC_PWRBTN# <<< _____
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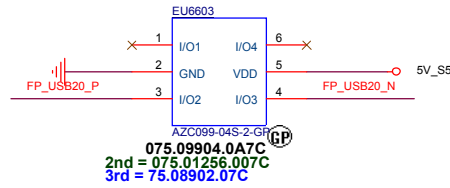
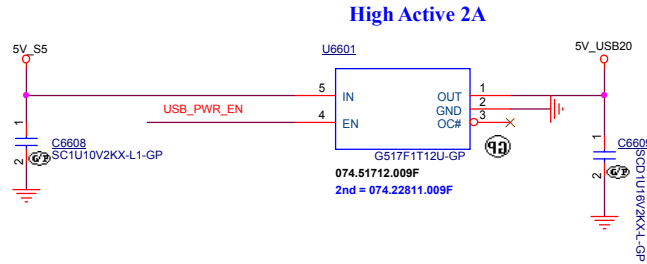
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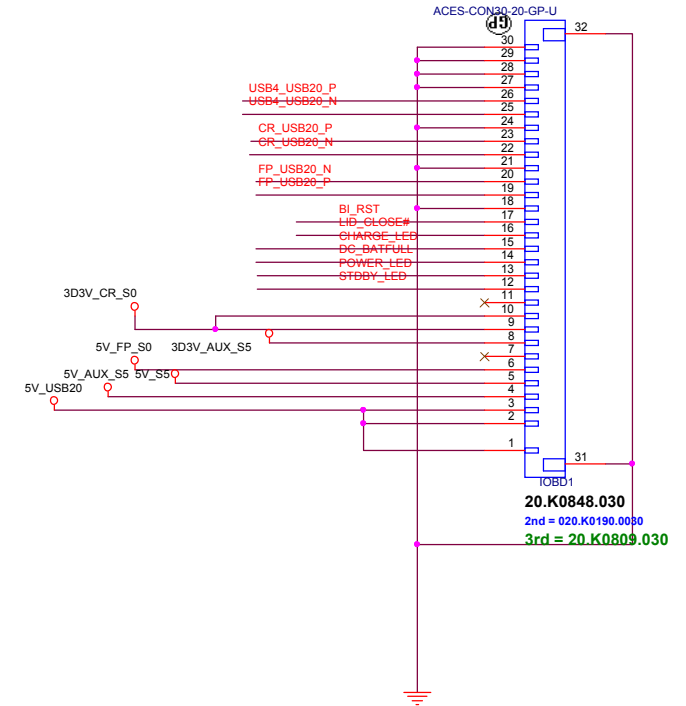
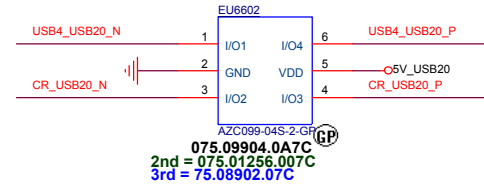
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SSID = User.Interface



Close connector



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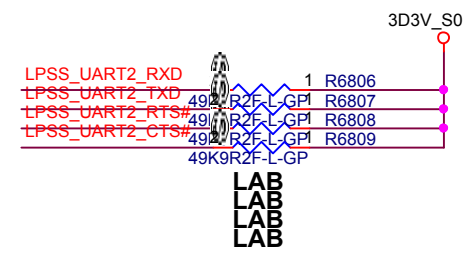
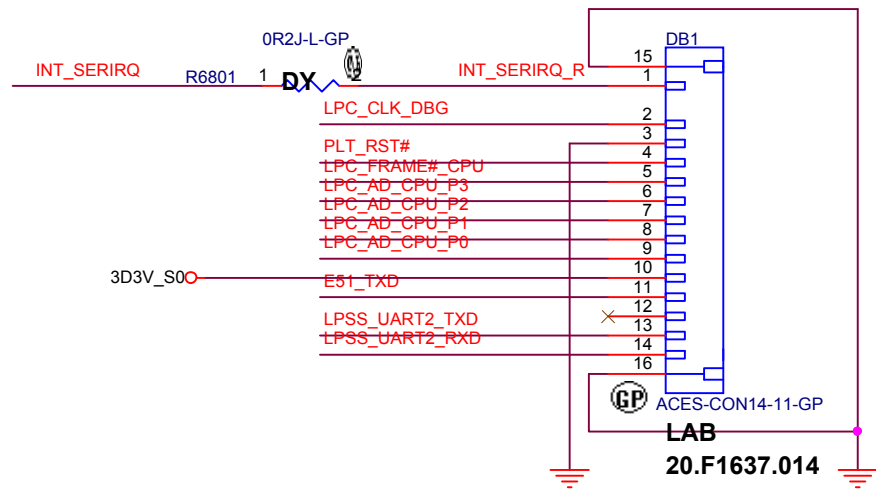
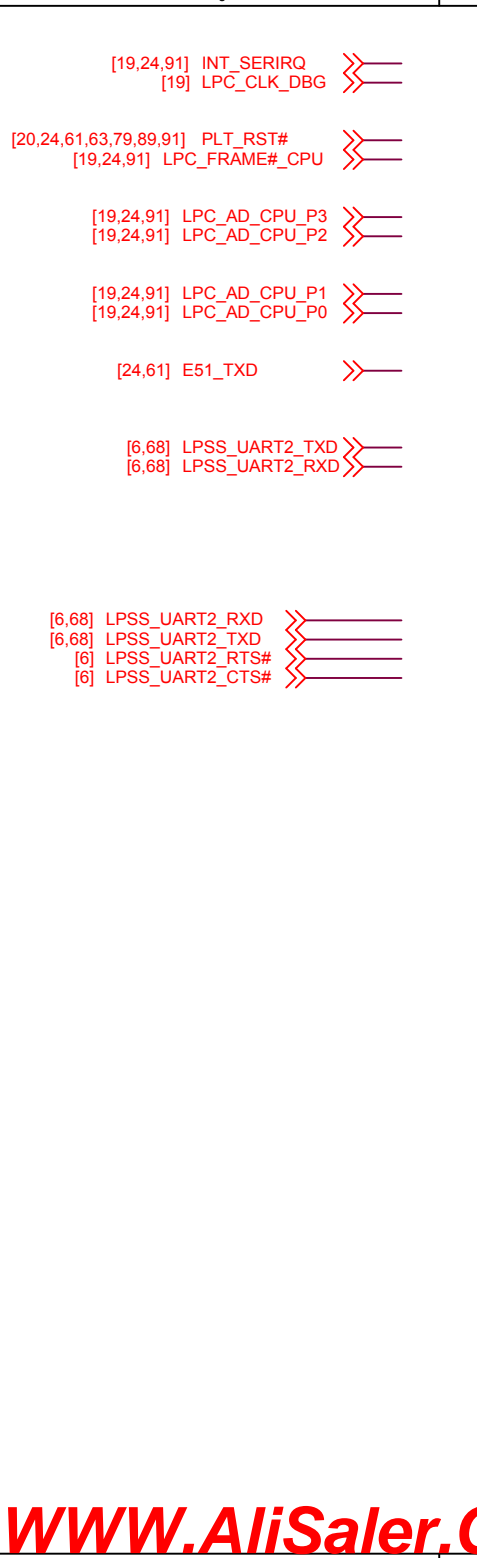
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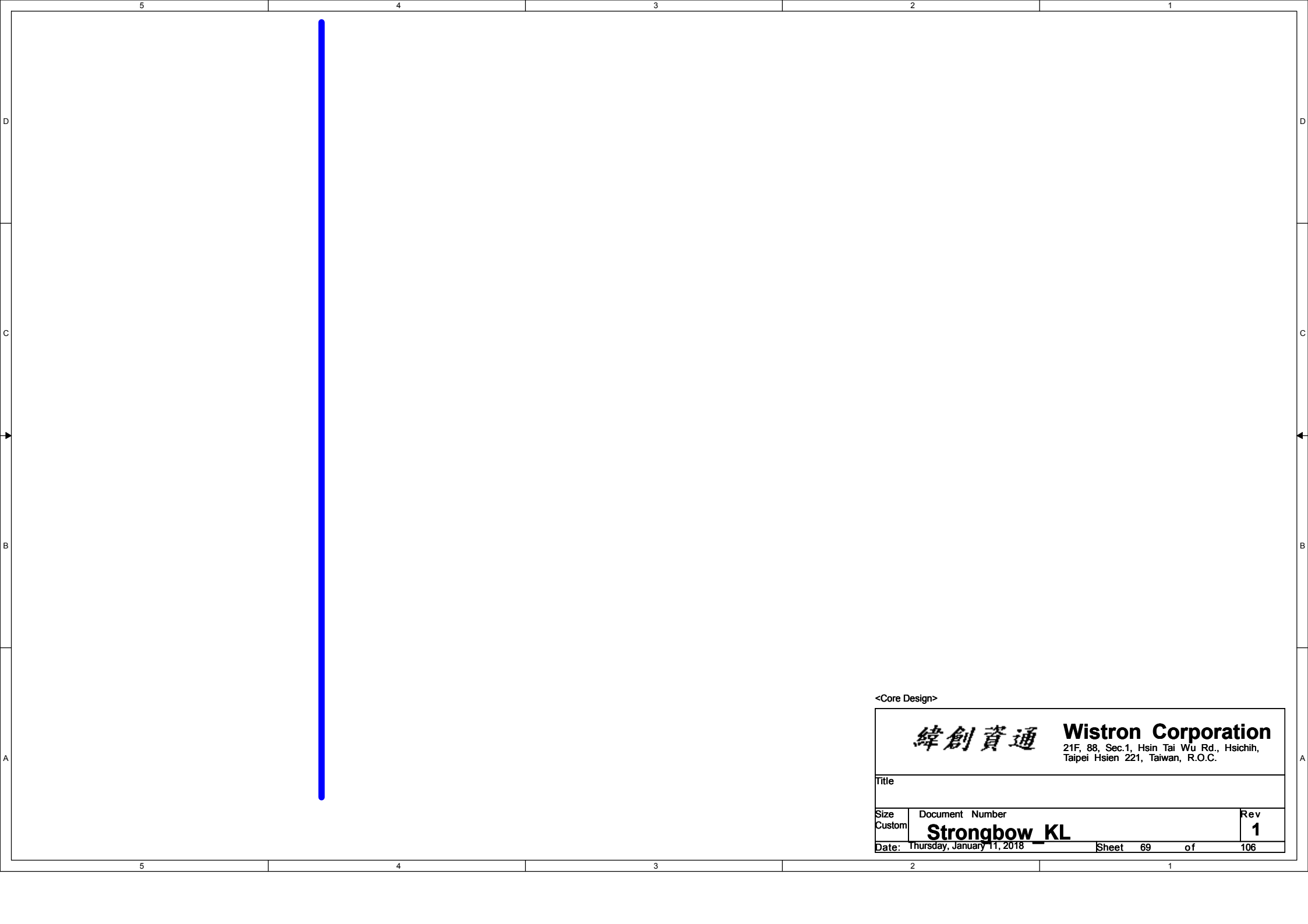
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SSID = User.Interface

G Sensor

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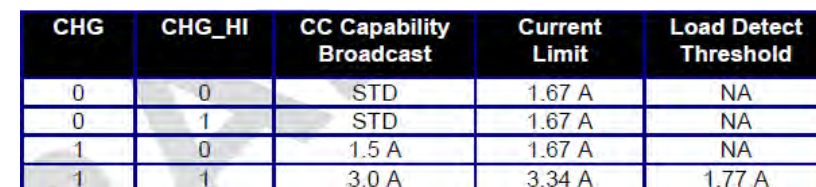
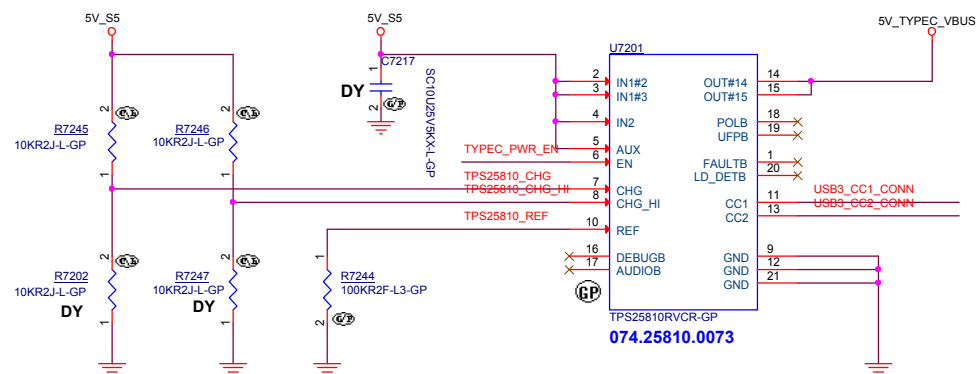
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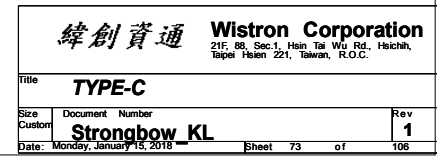
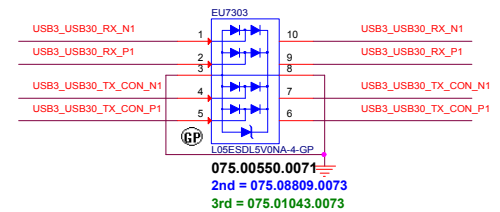
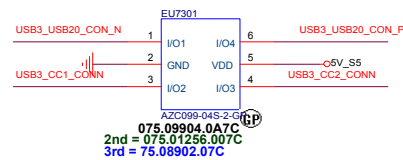
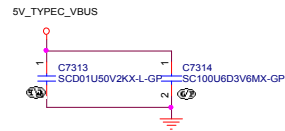
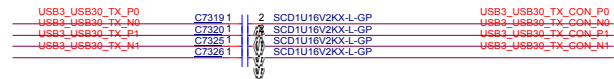
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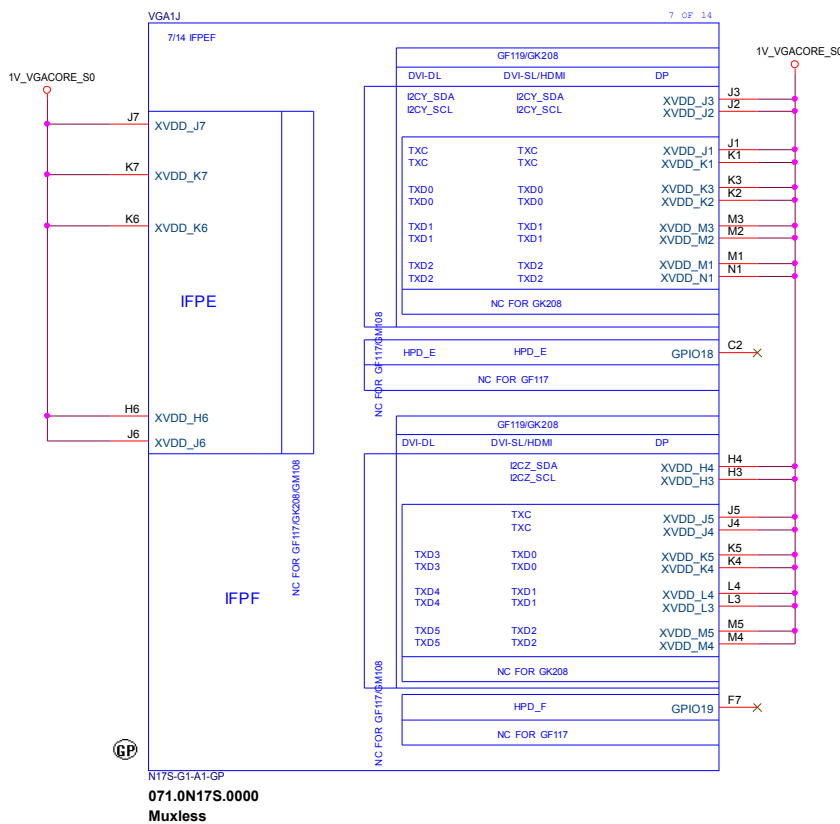
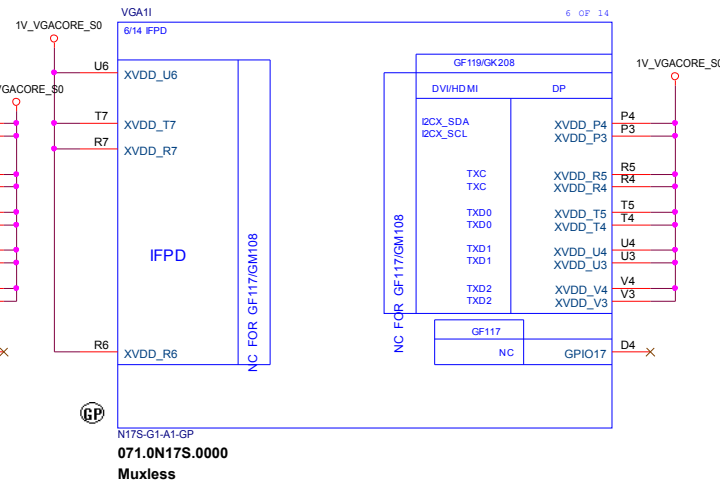
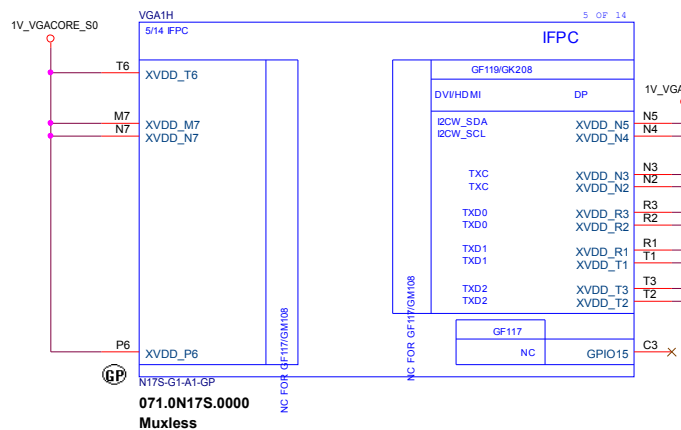
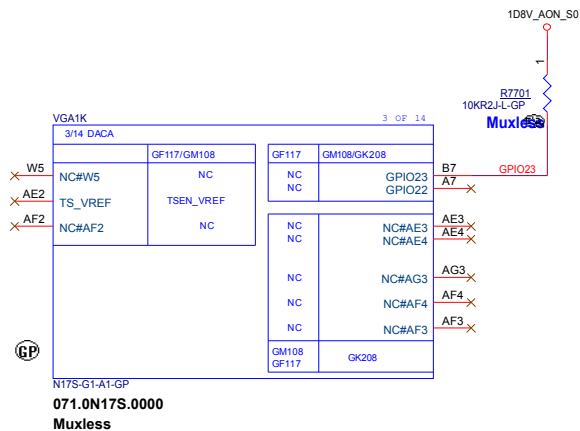
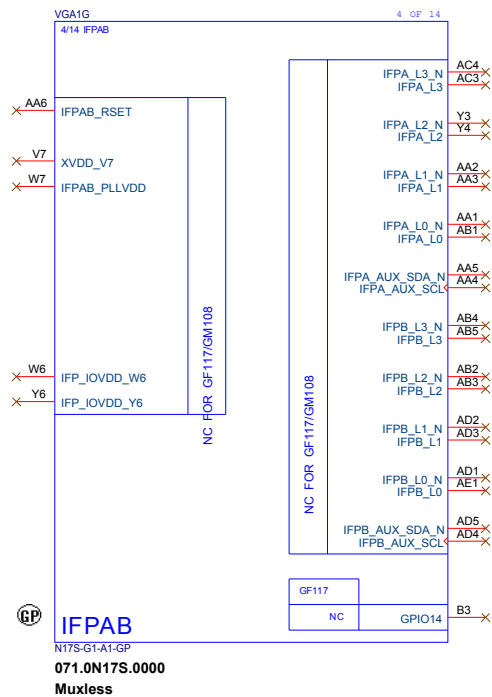
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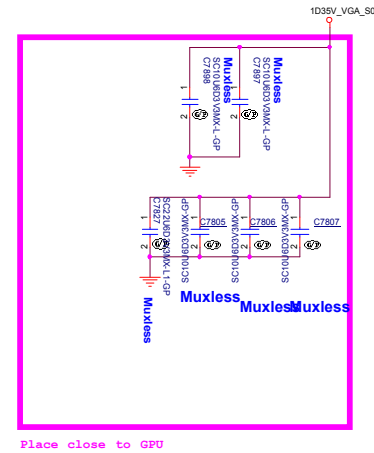
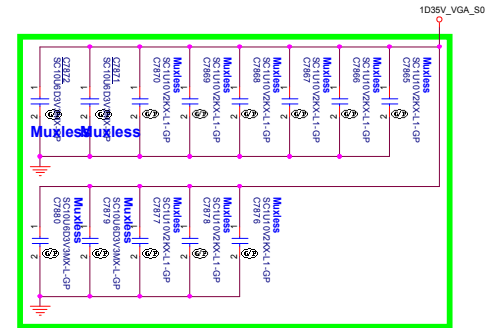
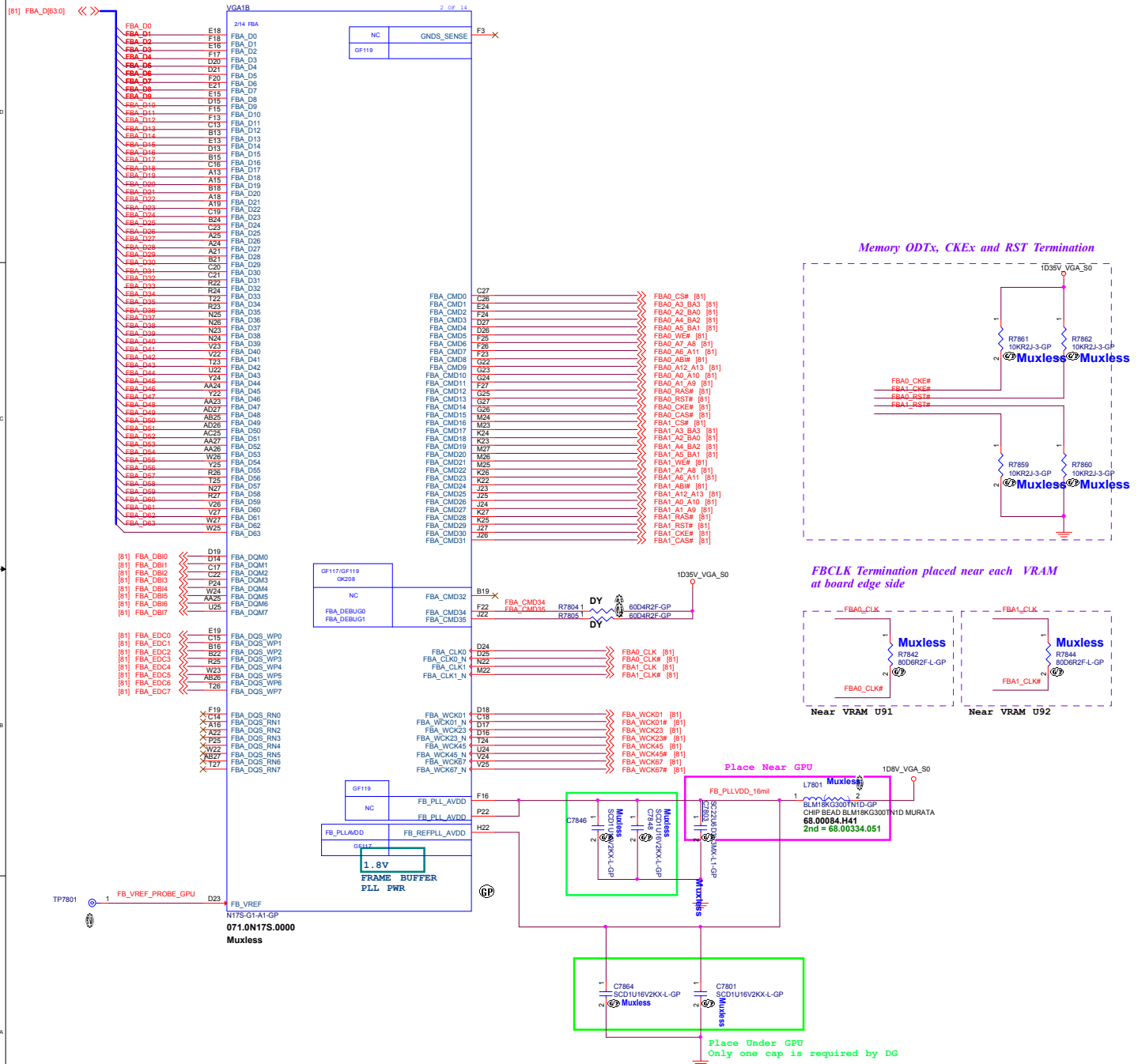


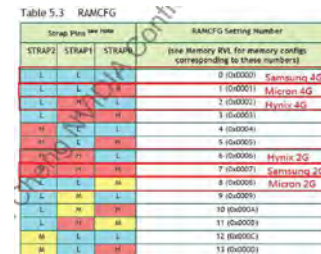
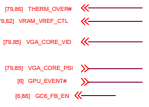
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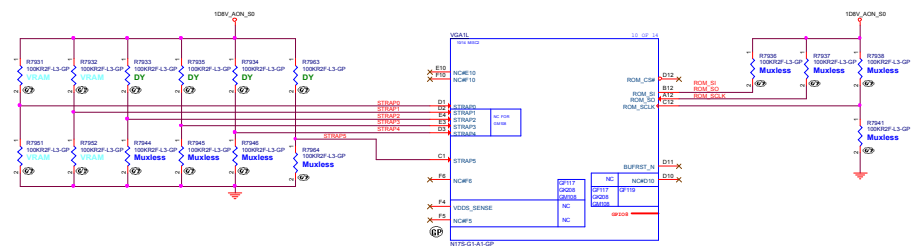
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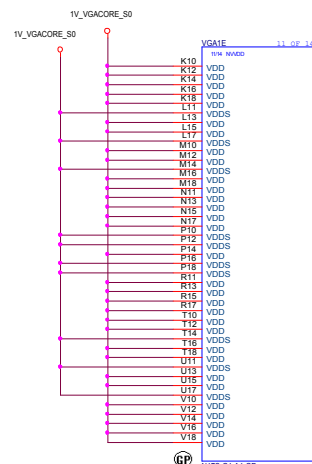
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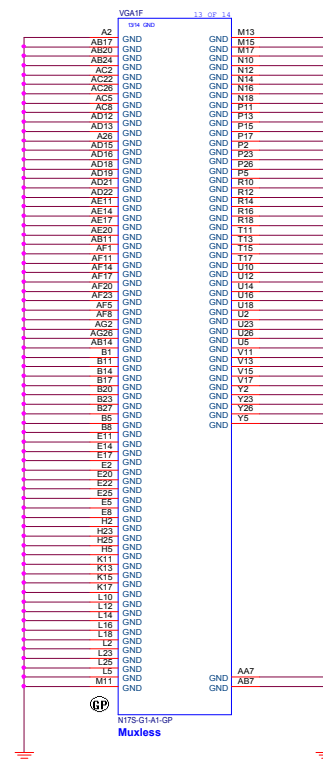
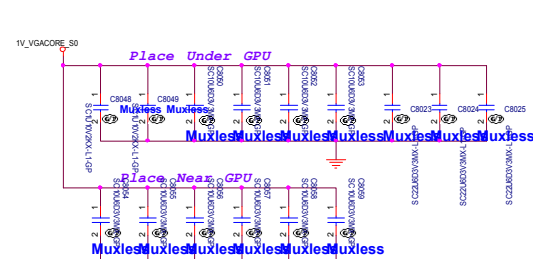


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			SamSung	K4G00325FB-HC18	B-die	Da0	8 Gbps	N/A	N/A	Substitution allowed with warning
			Almicon	MT71256B12DF-70-A	A-die	Da1	7 Gbps	N/A	Full	Production ready
Memory Density	Allowed Memory Configuration	FBDWG	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
4 Gb	128Mb;12 256Mb;16	1.35V	Almicon	MT71256B12DF-80-A	A-die	Da1	8 Gbps	N/A	N/A	Substitution allowed with warning
			Hynix	H5GCG4Q4UR-R0C	M-die	Da2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GCG4Q4UR-R4C	M-die	Da2	8 Gbps	N/A	N/A	Substitution allowed with warning
			Hynix	H5GCG4Q4UR-R0C	A-die	Da6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GCG4Q4UR-R4C	A-die	Da6	8 Gbps	N/A	N/A	Substitution allowed with warning
			SamSung	K4G41325FE-AC18	E-die	Da7	7 Gbps	N/A	Full	Production ready
			SamSung	K4G41325FE-HC25	E-die	Da7	8 Gbps	N/A	N/A	Substitution allowed with warning
			Almicon	EDW40128AG-70-F	A-die	Da8	7 Gbps	N/A	Full	Post production ready

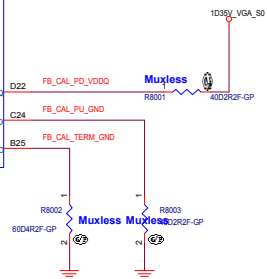
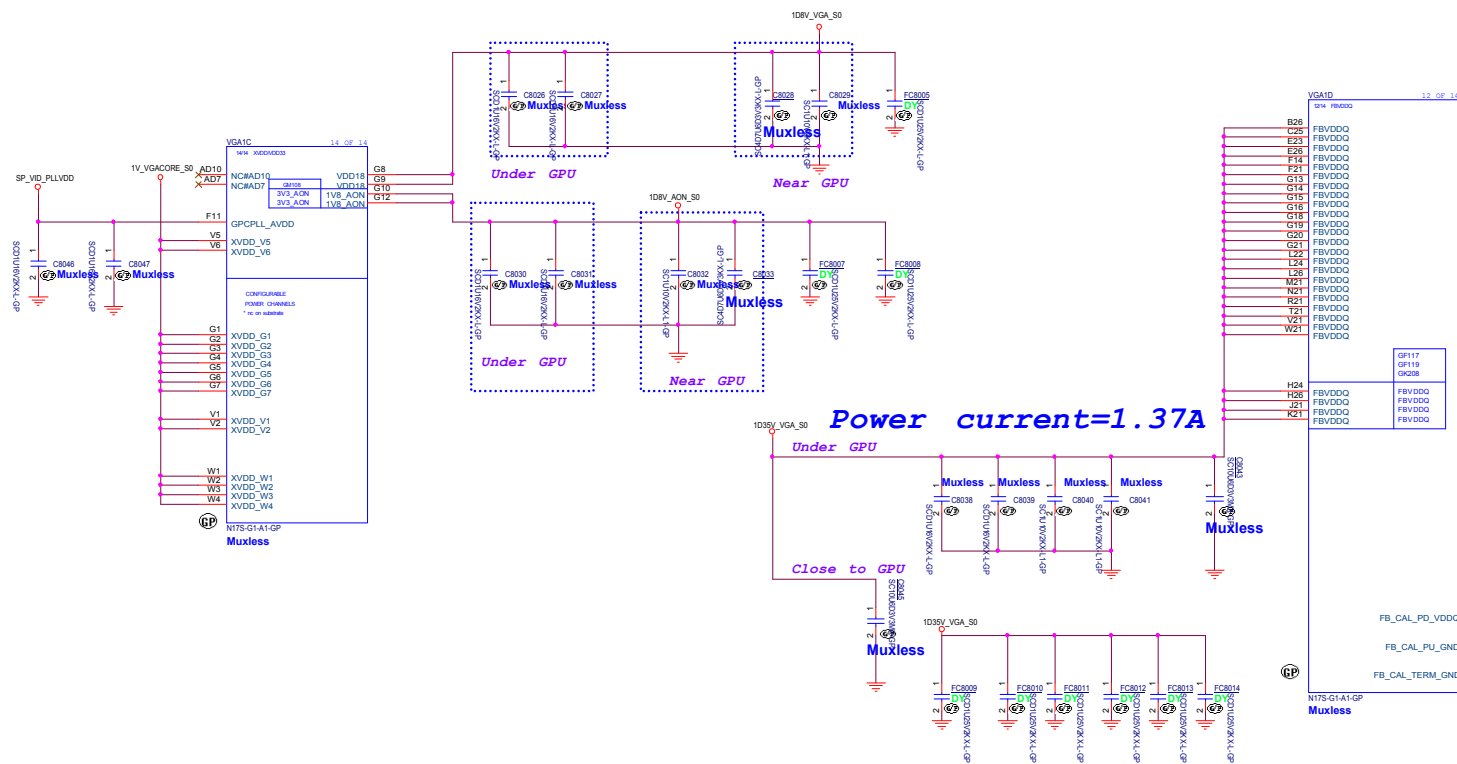




Power ^{Muxless} *current=26A*



Power current=60mA



[78] FBA_D[63:0] << >>

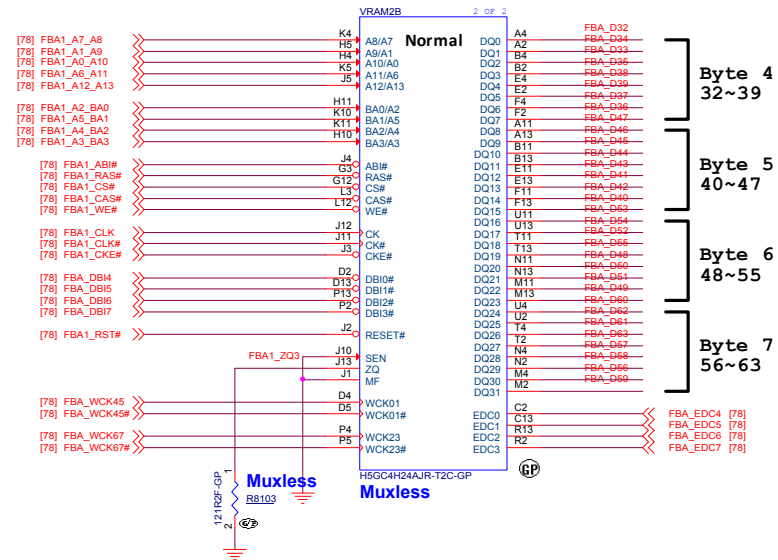
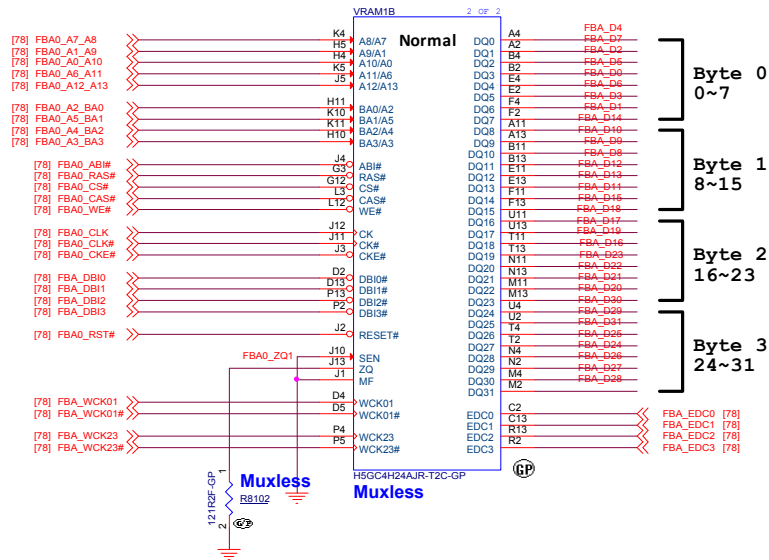
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072.04032.000N

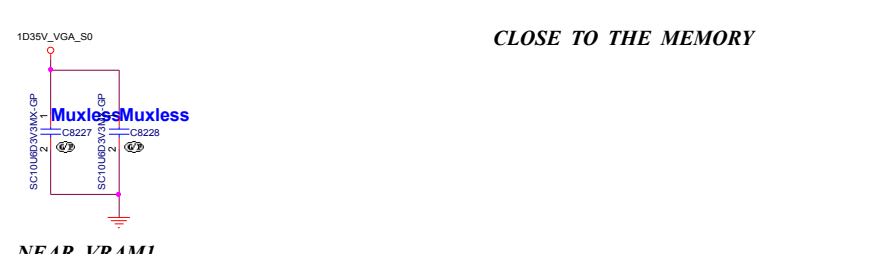
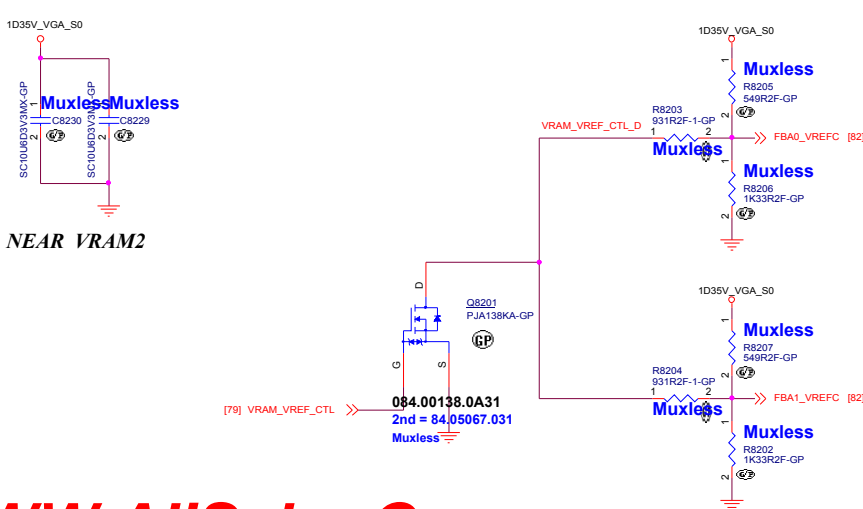
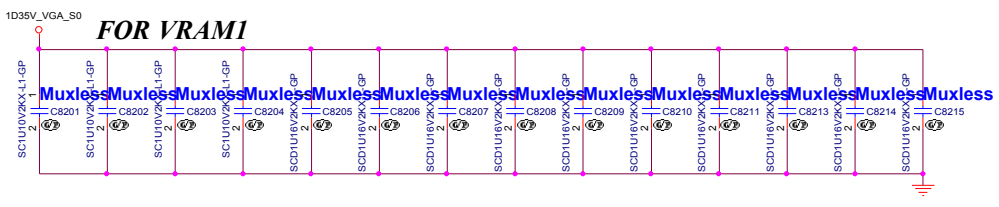
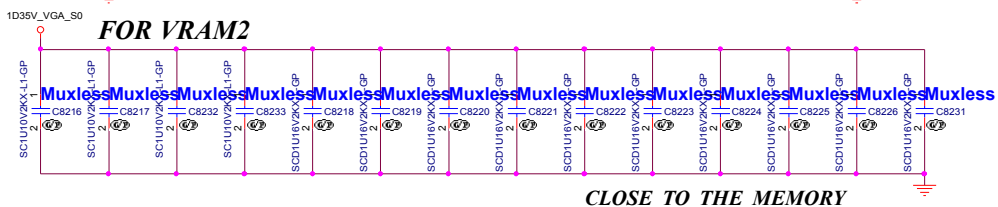
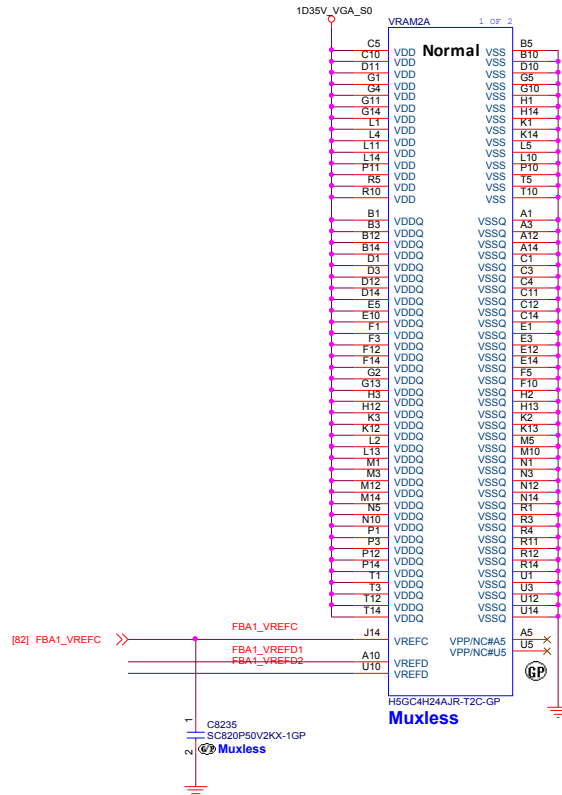
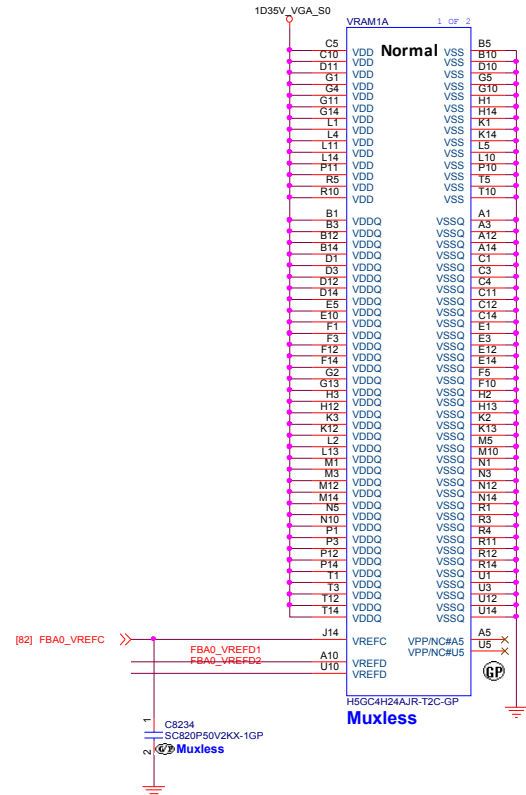
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VRAM CHANNEL-A			
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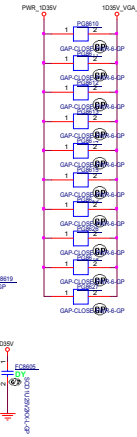
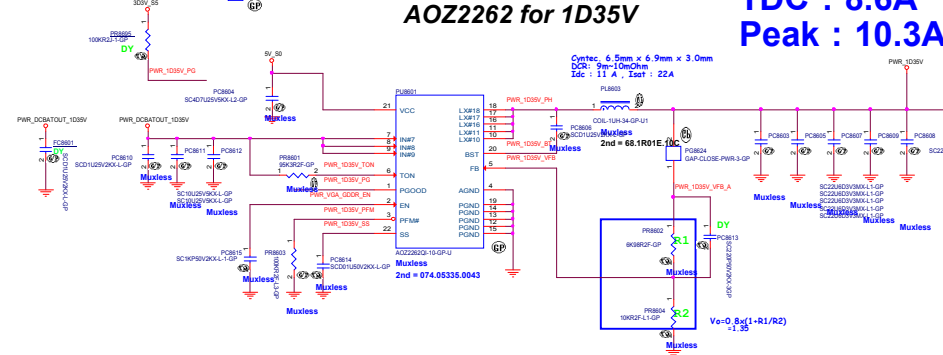
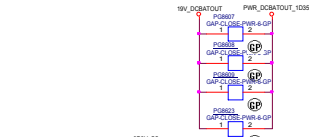
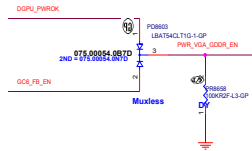
SSID = PWR.Plane.Regulator_1p0v

SSID = PWR.Plane.Regulator_1p35v

IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
COM	074.02262.0043	074.02261.0A73	074.02260.0043
Check	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 for 1D35V

TDC : 8.6A
Peak : 10.3A



SYW232 for 1D8V_AON

VGA_CORE1D05V_VGA_S0 Discharge Circuit
3D3V_S5 to 1D8V_AON_S0



20150821 R8615 change to PAD

N17 EE Change

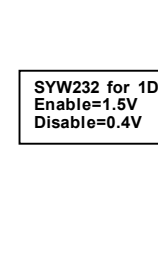
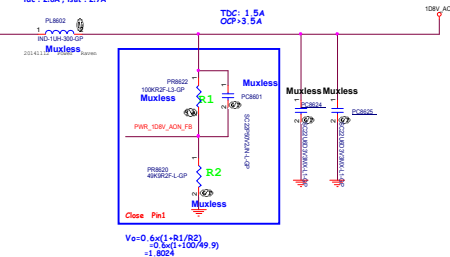
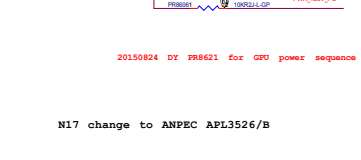
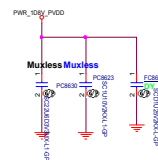
20150824 DY R8621 for GPU power sequence

N17 change to ANPEC APL3526/B

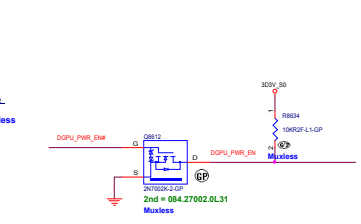
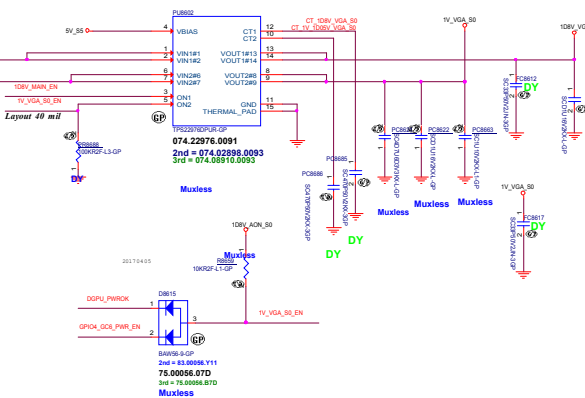
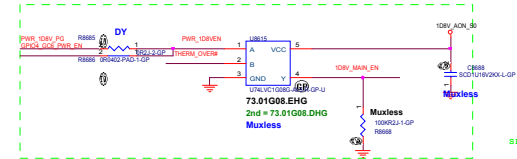
Cyntec 2.5 x 2.0 x 1.2mm
DCR: 37.43 mOhm
IDC : 2.6A , Isst : 2.7A

TDC : 1.5A
OCP: 3.5A

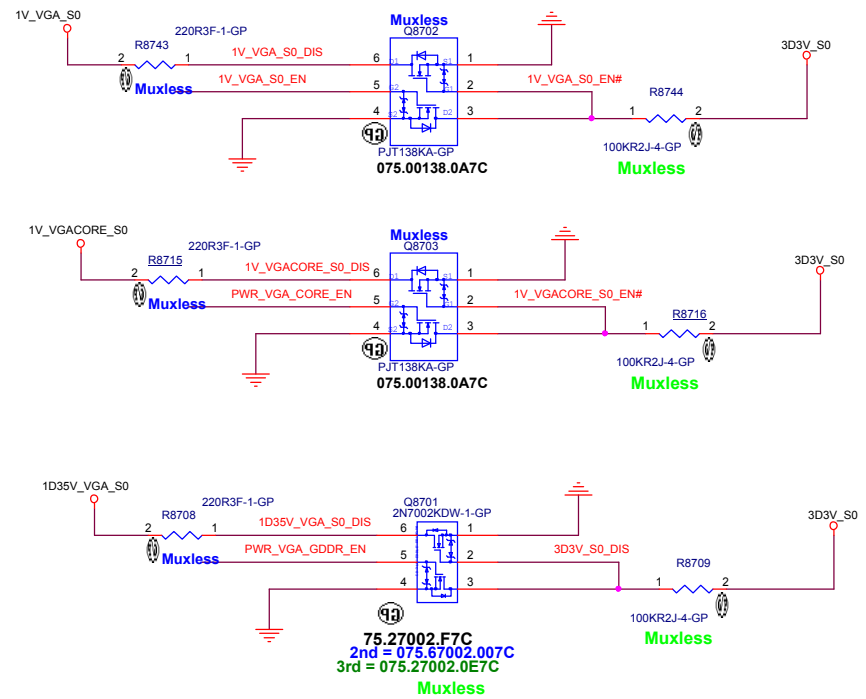
SYW232 for 1D05V
Enable=1.5V
Disable=0.4V



SYW232 for 1D8V_MAIN

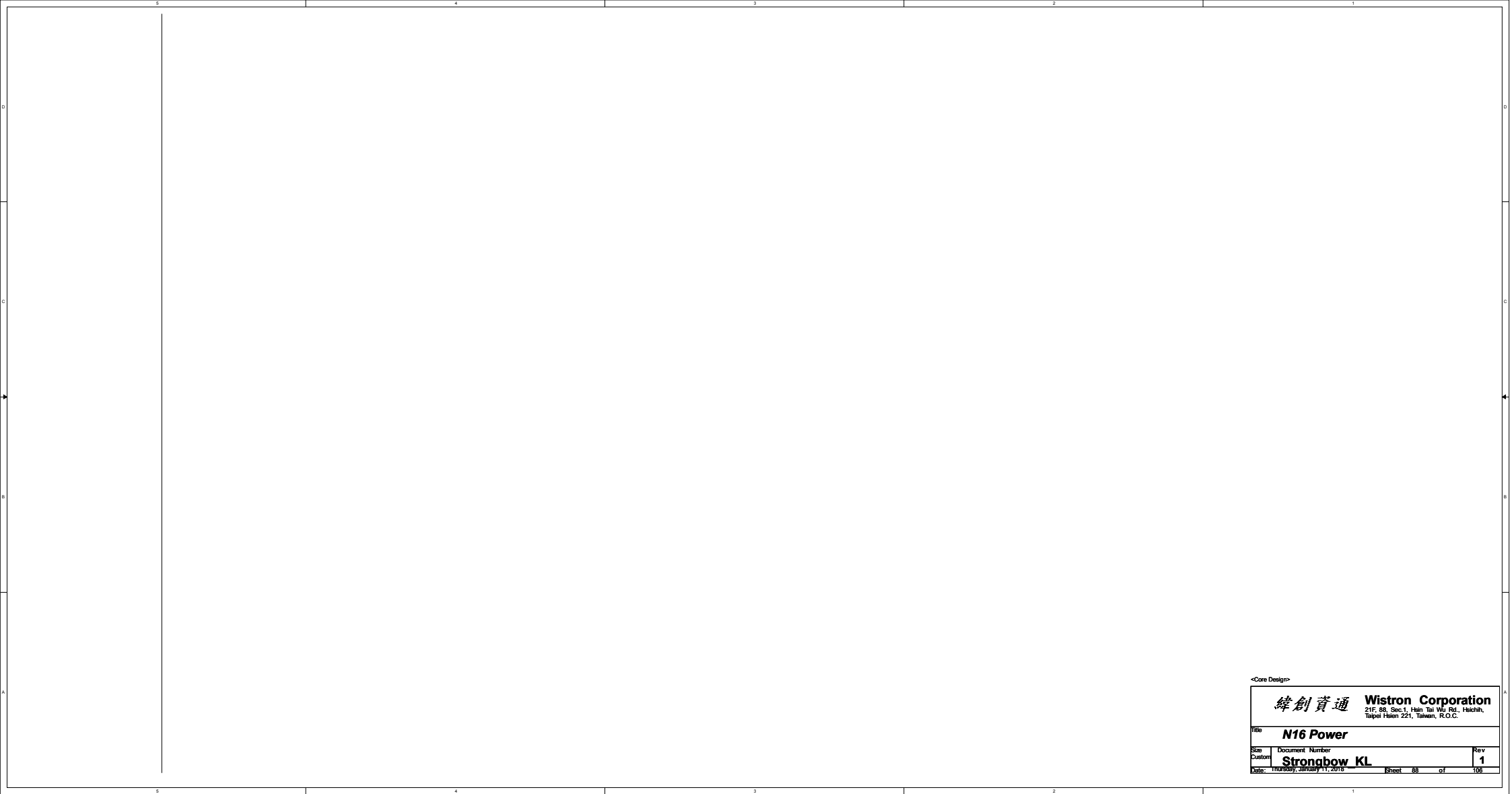


[86] 1V_VGA_S0_EN <<< _____
[85] PWR_VGA_CORE_EN >>> _____
[86] PWR_VGA_GDDR_EN >>> _____



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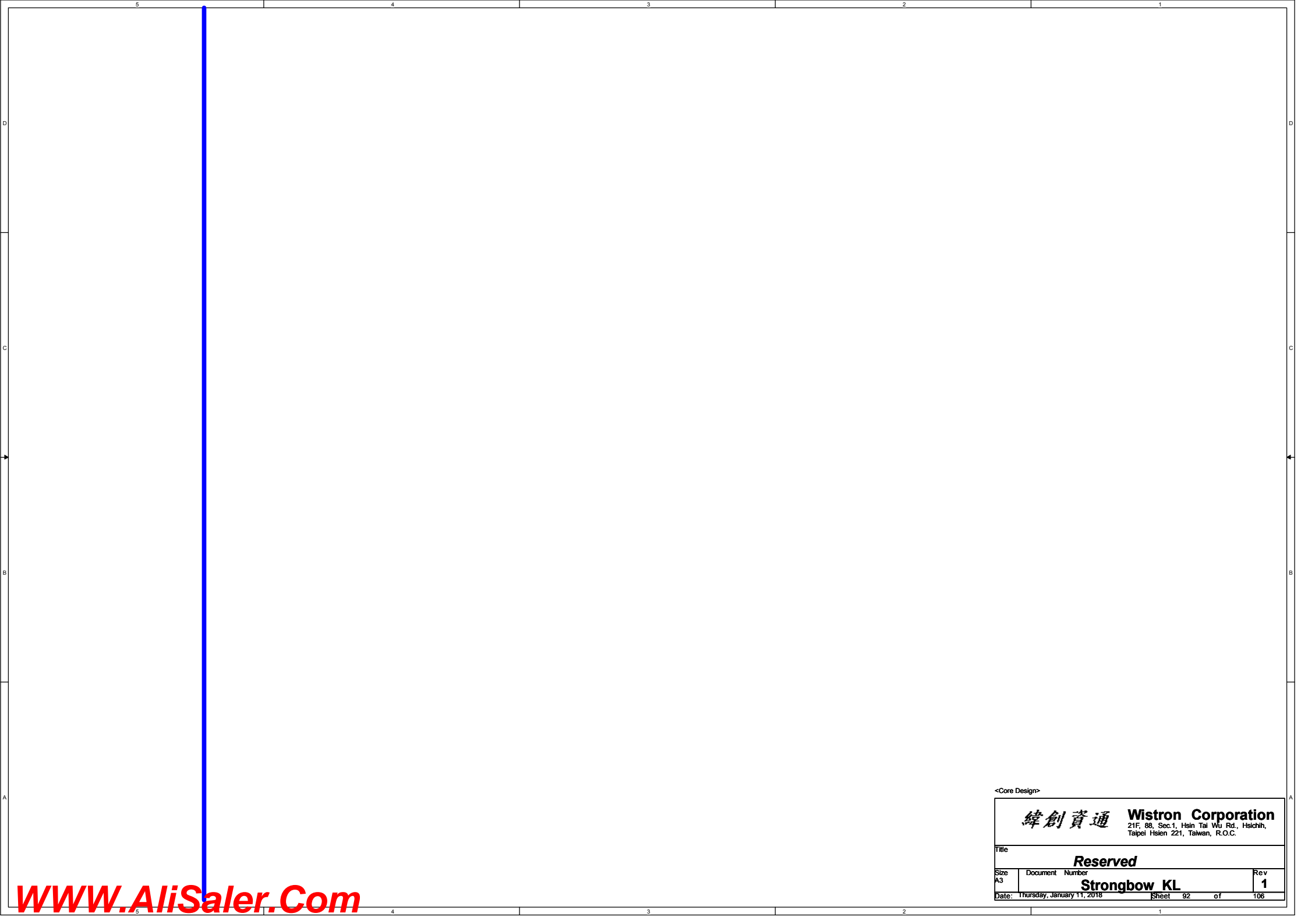


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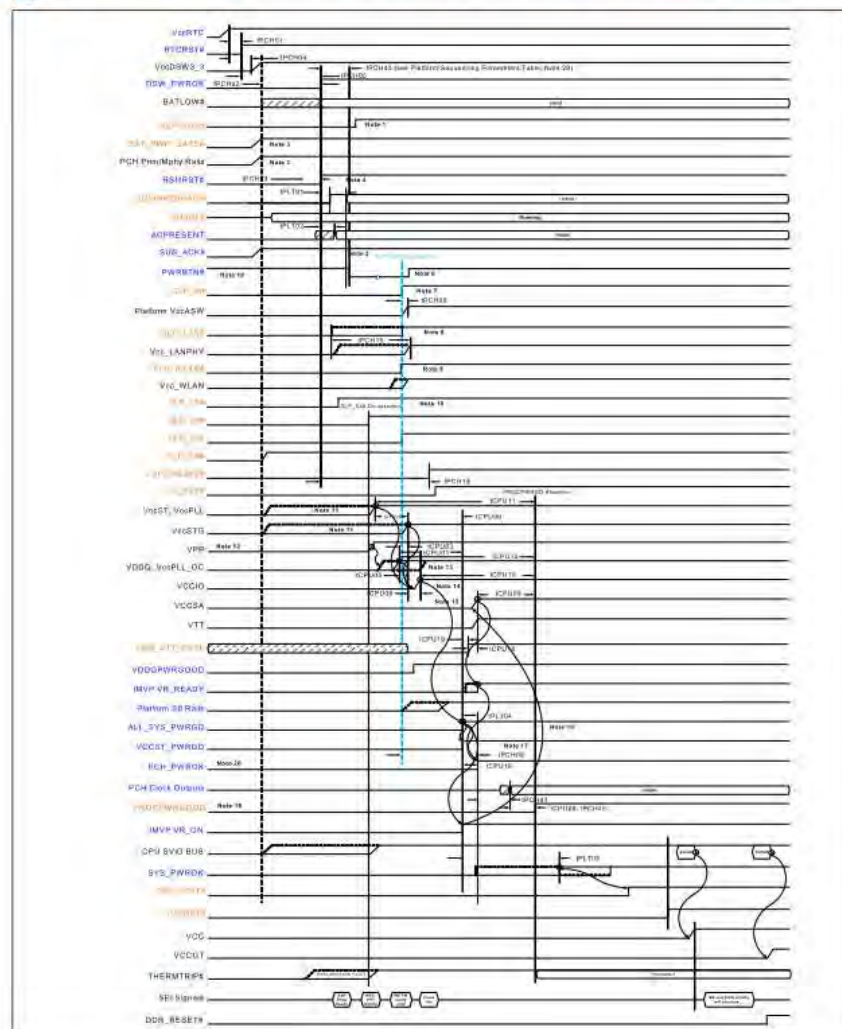
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Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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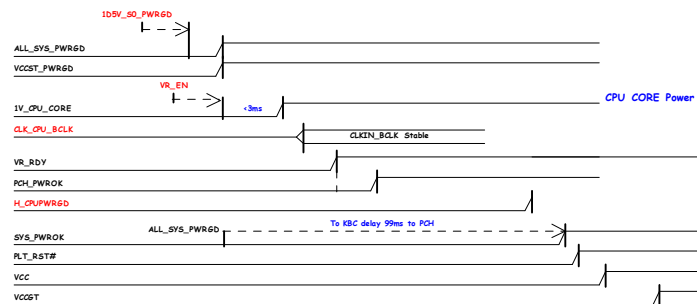
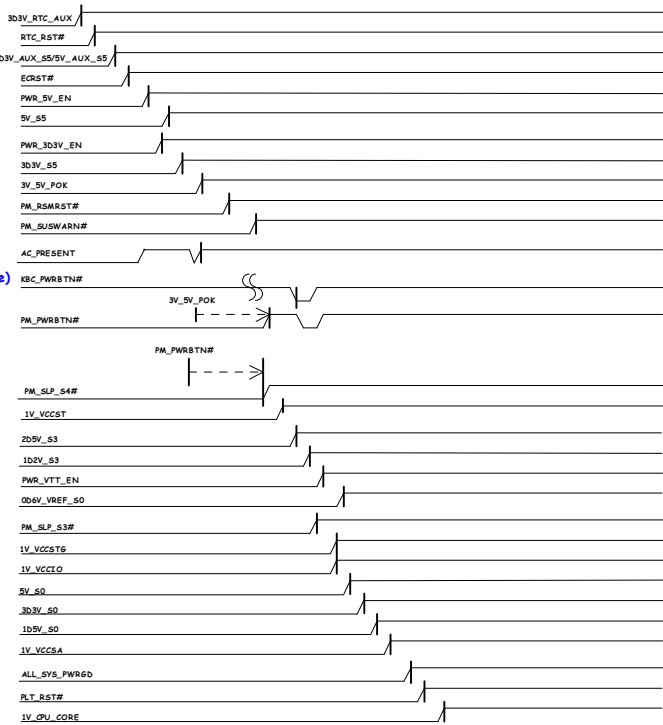
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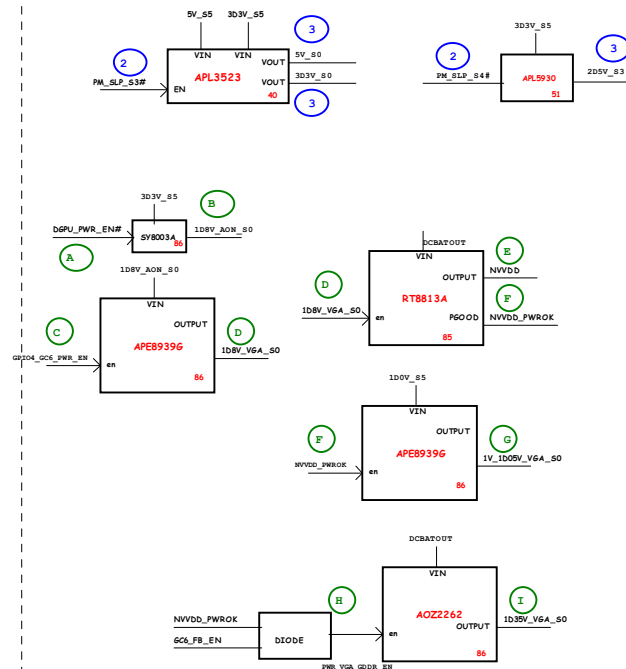
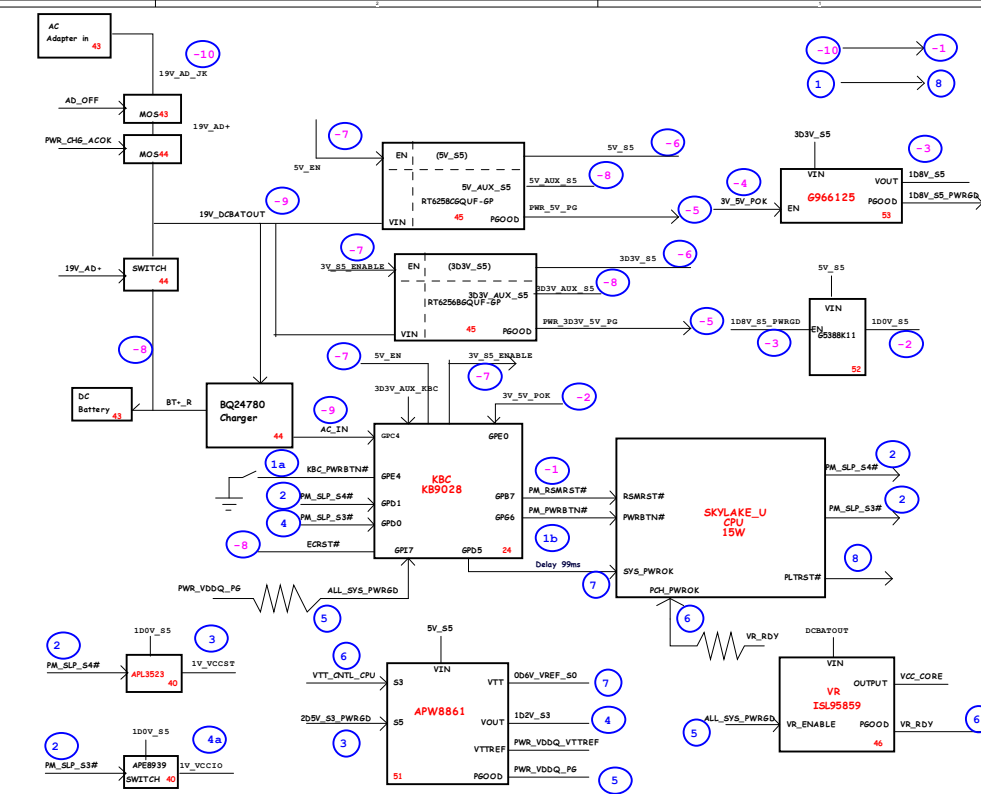
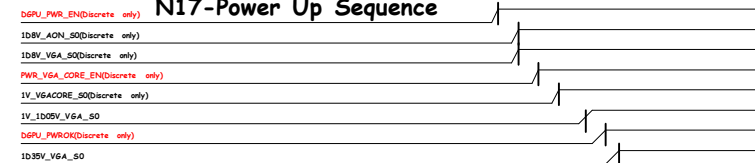
Intel-Power Up Sequence

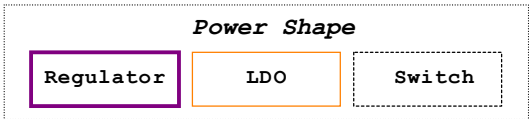
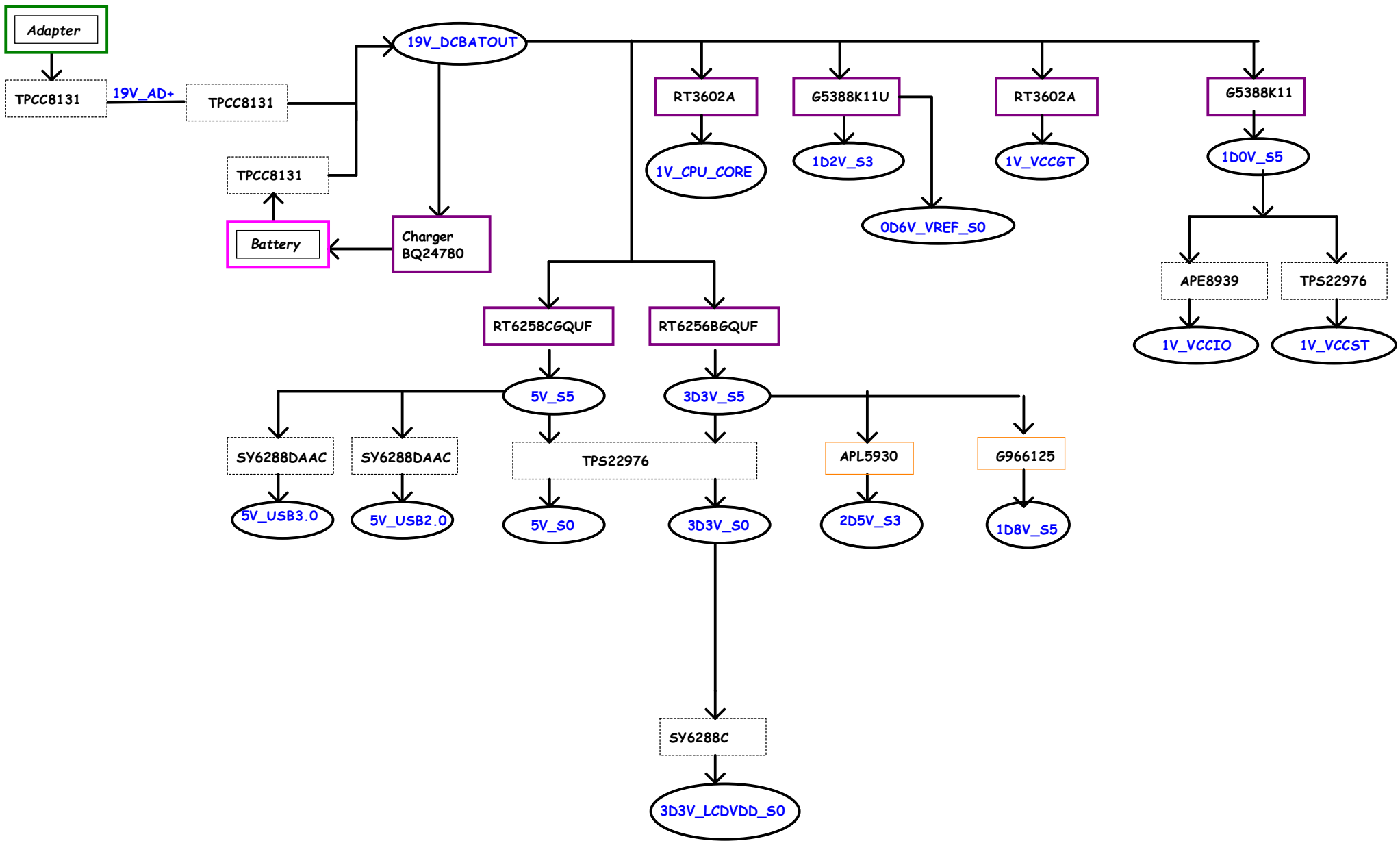
(AC mode)

mode) (DC mode)

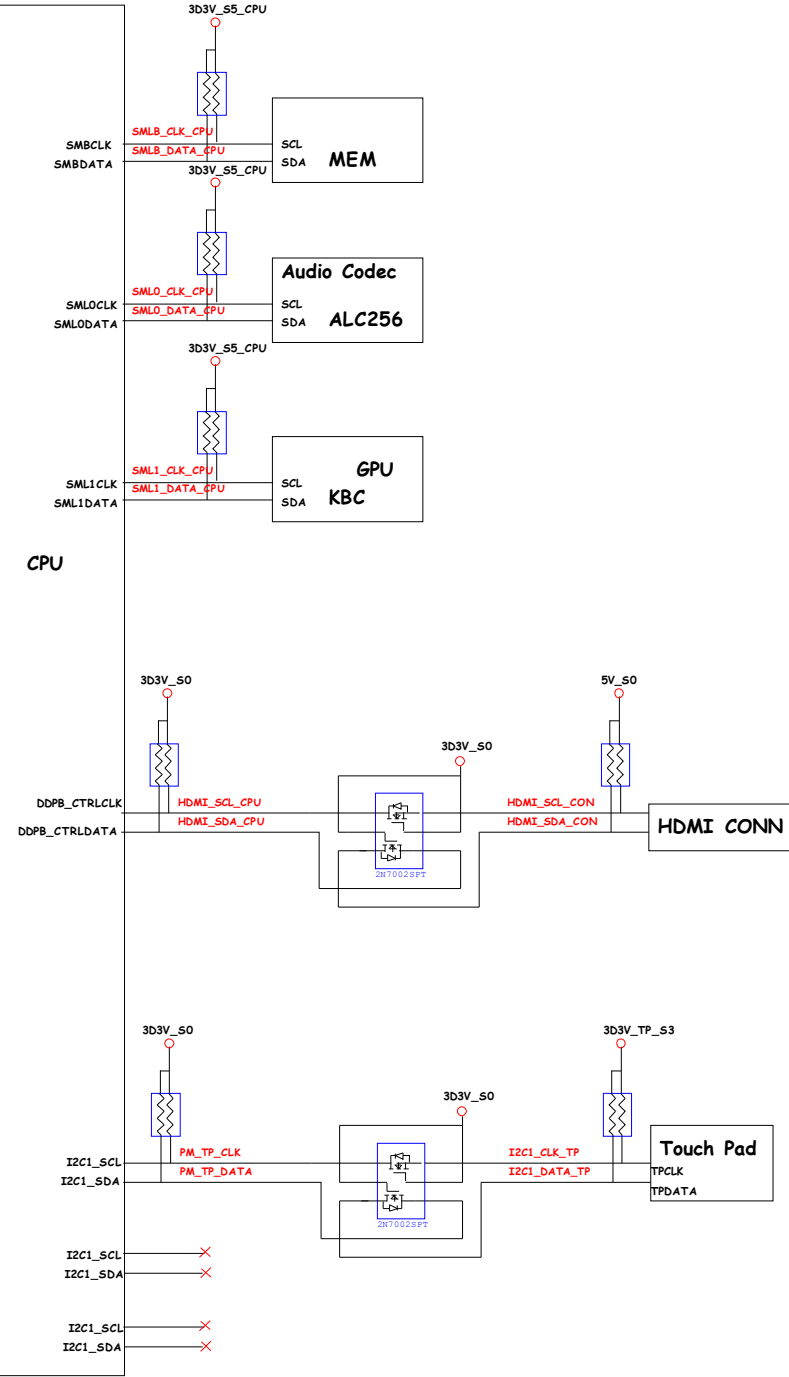


N17-Power Up Sequence

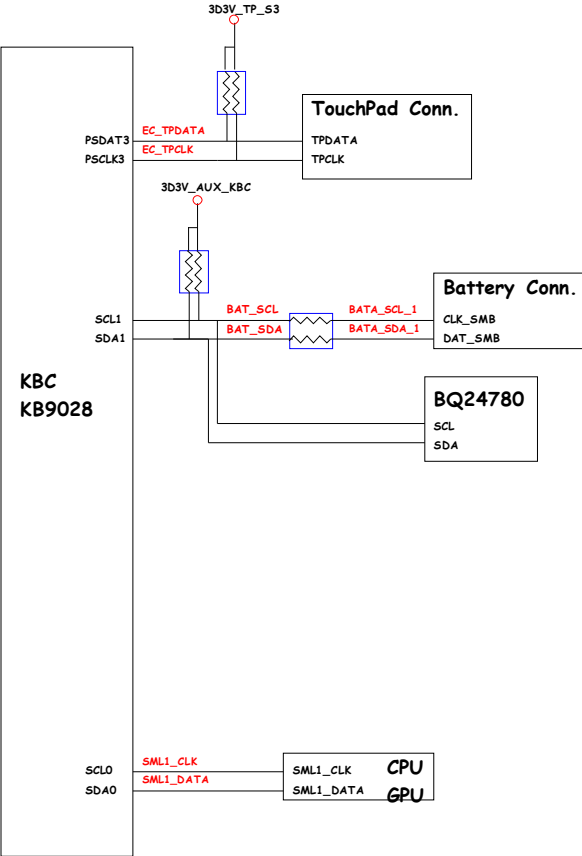




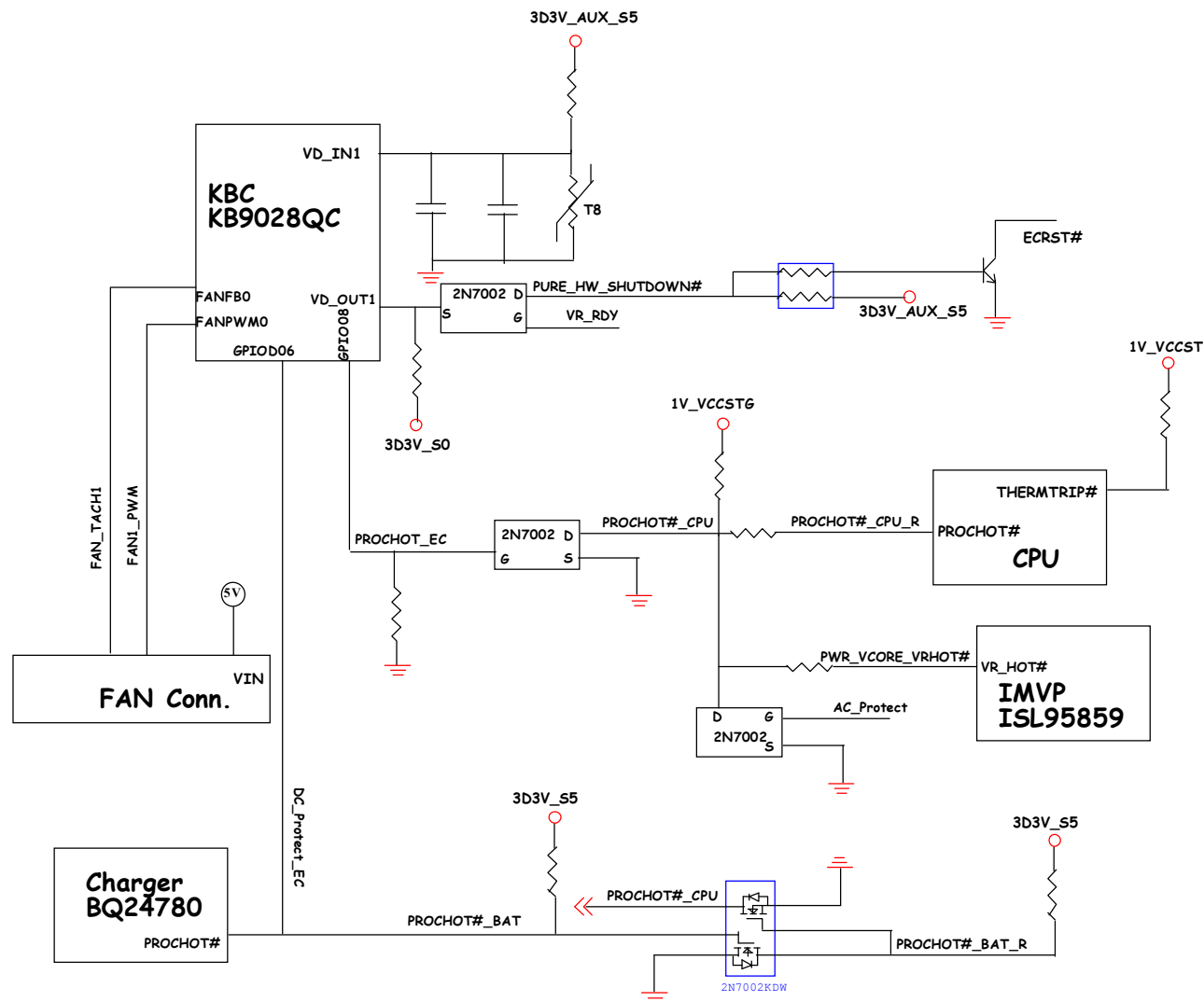
PCH SMBus/I2C Block Diagram



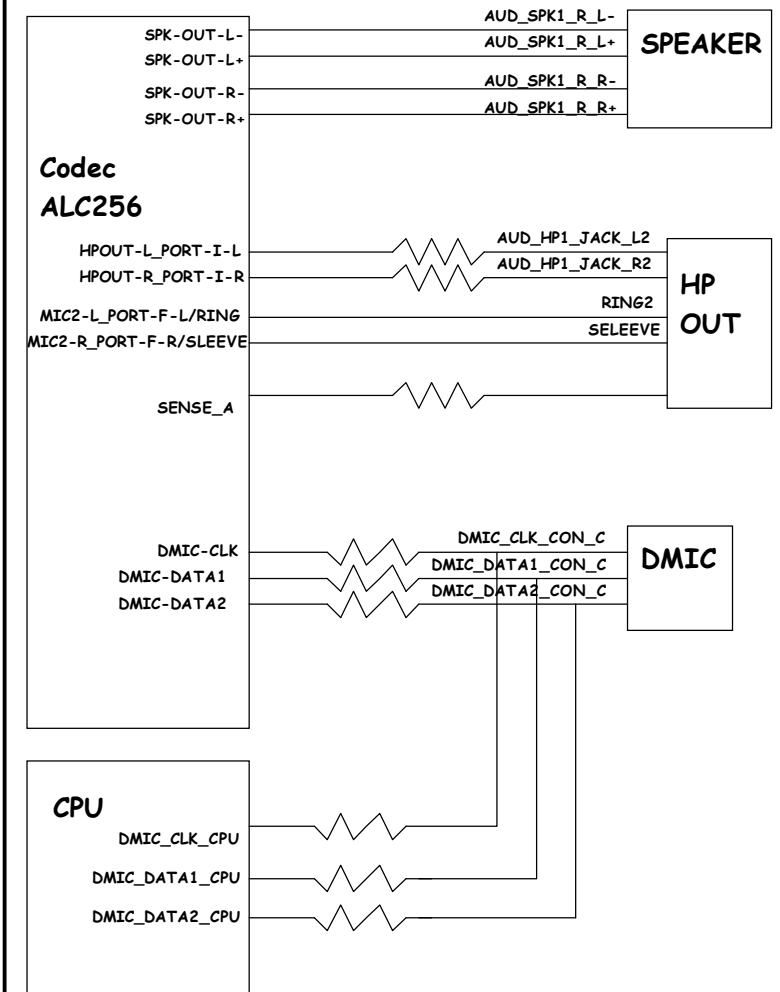
KBC SMBus/I2C Block Diagram



Thermal Block Diagram



Audio Block Diagram



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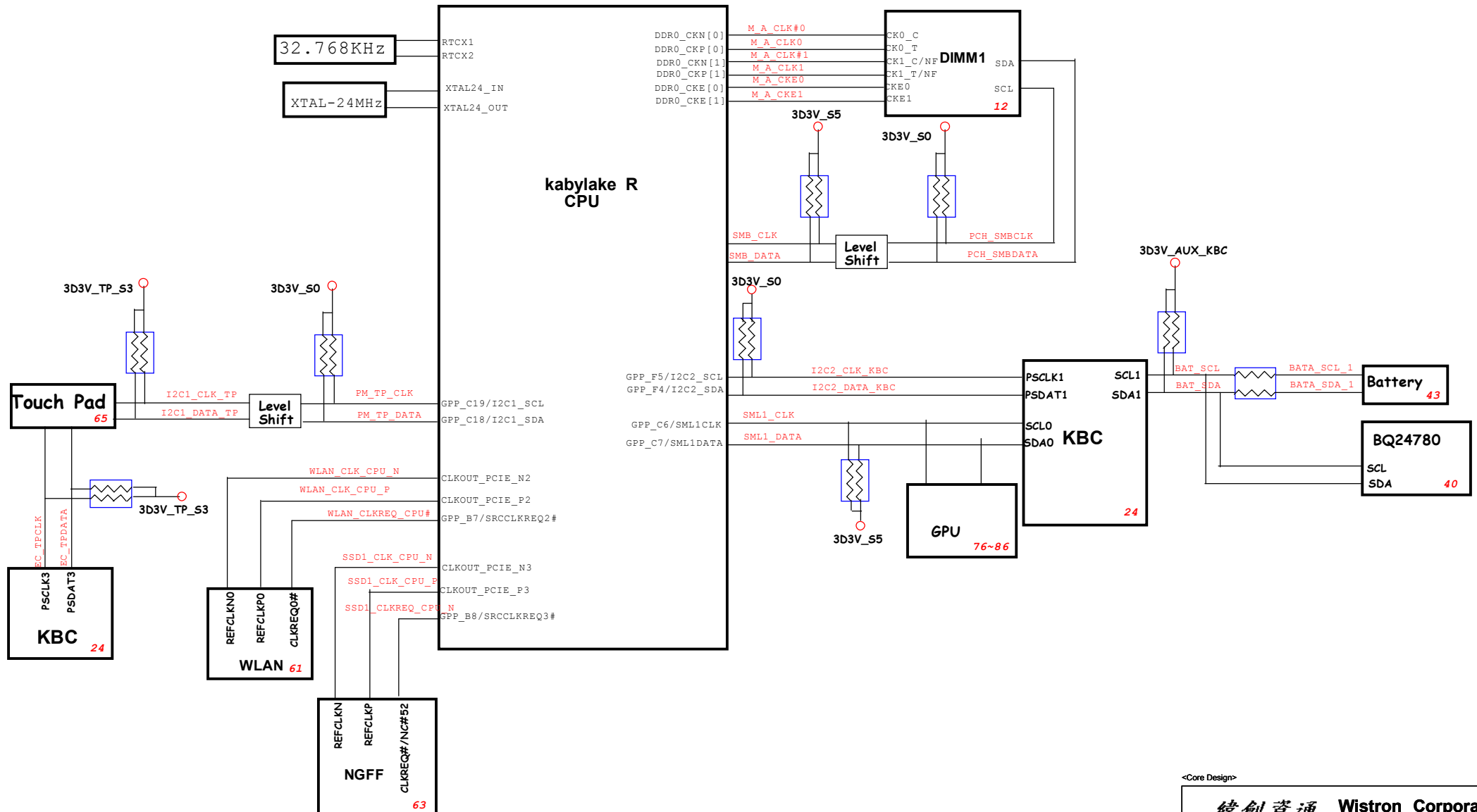
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CLOCK BLOCK DIAGRAM



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