

Compal Confidential

FH50P MB Schematics Document

AMD Picasso Platform

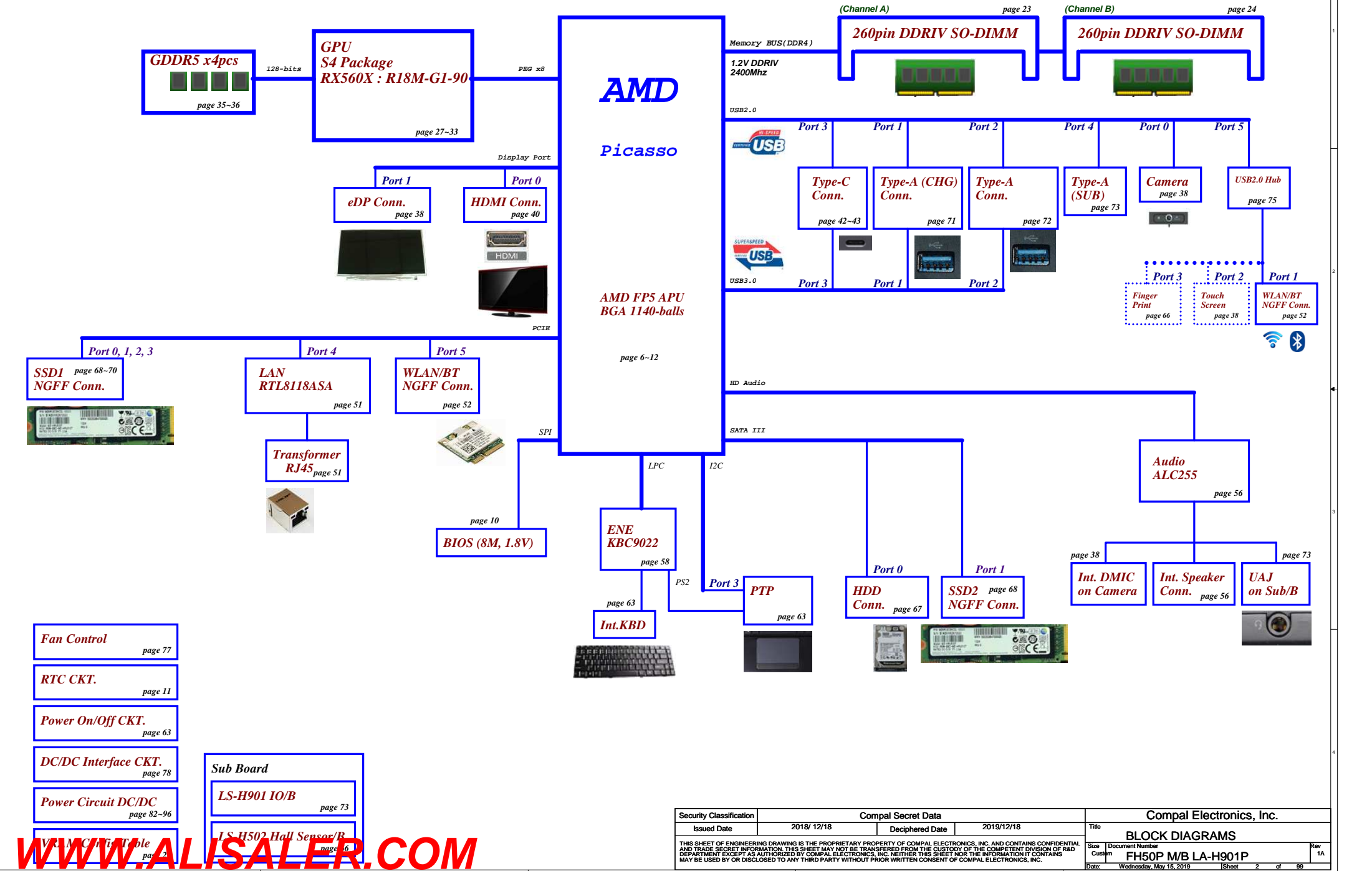
AMD R18M-G1-90

LA-H901P REV:1A

2019-05-13

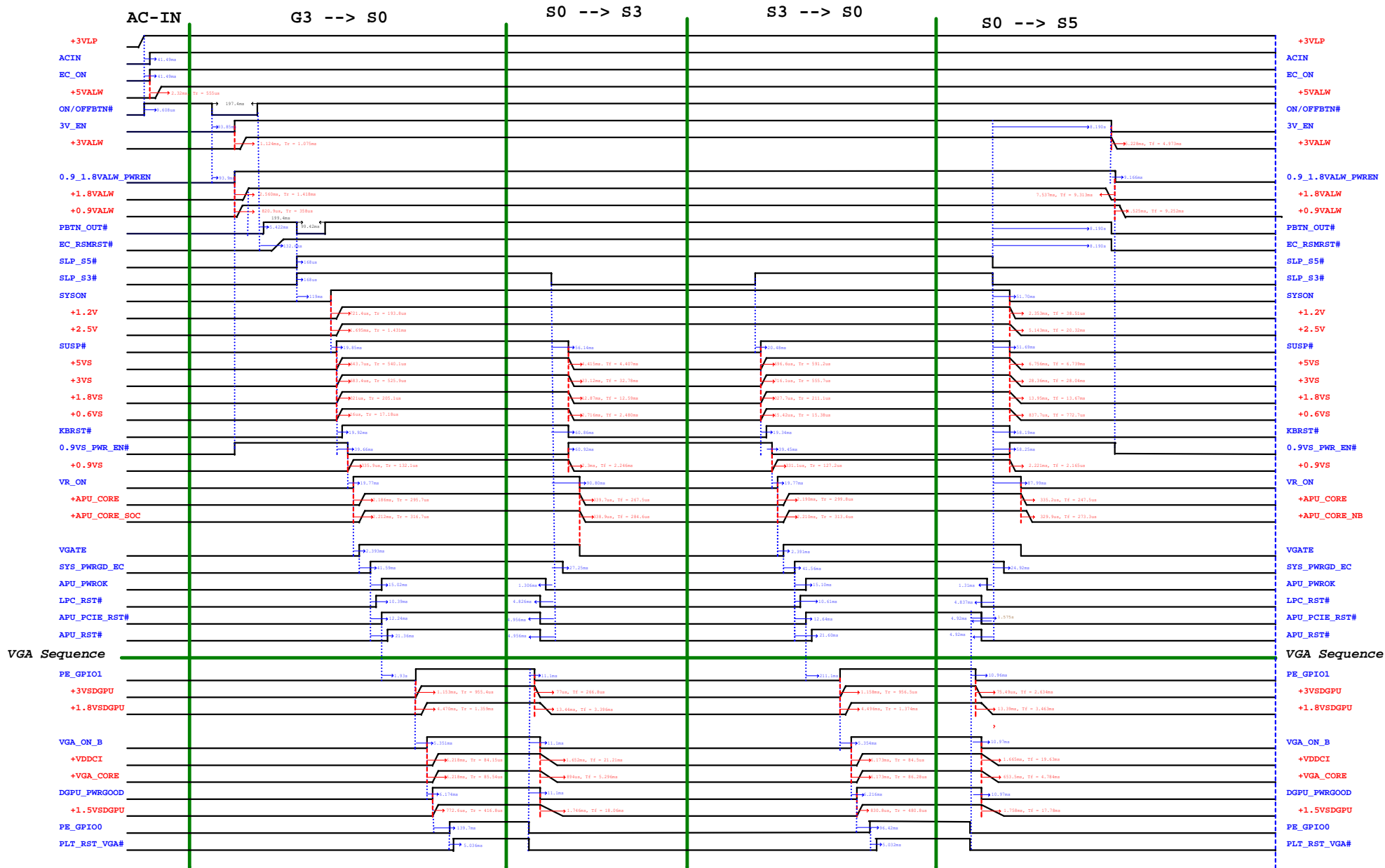
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				Sheet	1 of 99
				Rev	1A

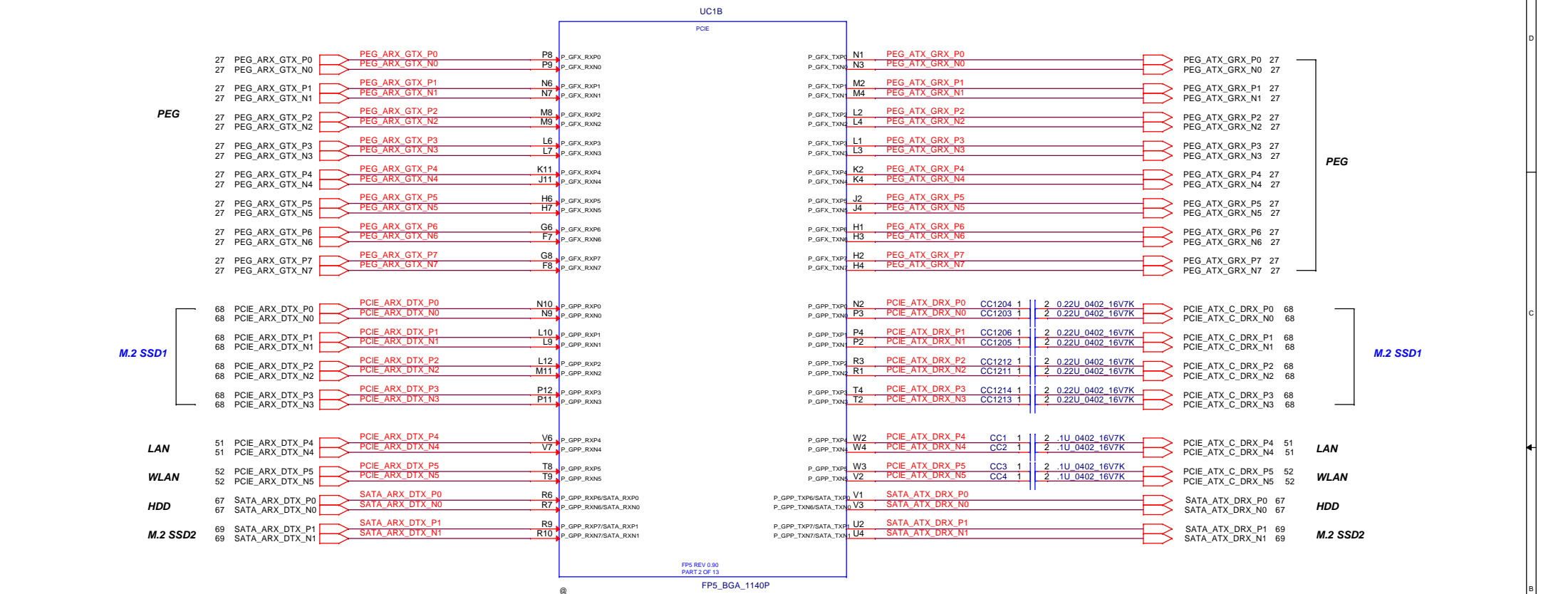


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				Custom	FH50P M/B LA-H901P
				Date	Wednesday, May 15, 2019
				Sheet	2 of 99
				Rev	1A



Main Func = CPU



APU PN Table

APU Platform	Customer PN	Customer PN	Customer PN	Customer PN	Compal PN	Compal PN
Picasso	UC1 R5APUQC@	UC1 R7APUQC@	UC1 R5APU@	UC1 R7APU@		
	S IC RYZEN5 YM3500C4T4MFG 2.1G BGA APU	S IC RYZEN7 YM3700C4T4MFG 2.3G BGA APU	S IC RYZEN5 YM3500C4T4MFG 2.1G APU ABO!	S IC RYZEN7 YM3700C4T4MFG 2.3G APU ABO!		
	SA0000CCR20	SA0000C7640	SA0000CCR60	SA0000C7680		

PCB Number

- ZZZ EVT@
PCB 2QE LA-H901P REV0 MB 2
DA8001JM000
- ZZZ PVT@
PCB FH50P LA-H901P LS-H901P/H502P
DAZZQE00100
PCB: DAZ2QE00100, DA8001JM010 REV: 1.0/1.0/1.0
- ZZZ MP@
PCB FH50P LA-H901P LS-H901P/H502P
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PCB: DAZ2QE00100, DA8001JM010 REV: 1.0/1.0/1.0

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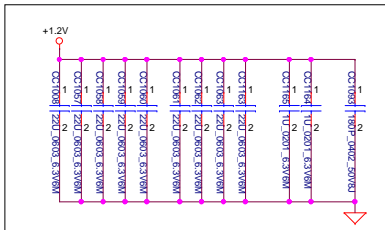
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Size	Document Number	Rev		FH50P M/B LA-H901P	
Custom				1A	
Date:	Wednesday, May 15, 2019	Sheet	6	of	99



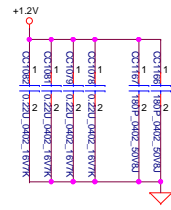
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						FP5 (2/7) DDR4			
						Size	Document Number	Rev	
						Customer	FH50P M/B LA-H901P		1A
Date: Wednesday, May 15, 2019				Sheet		7 of 99			

Main Func = CPU

```
+APU_CORE_SOC Cap
place at Power Side
```

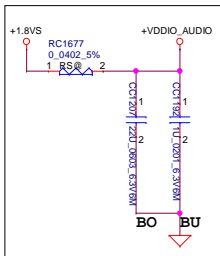


All BU (on bottom side under SOC)

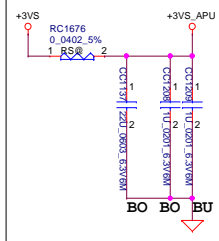


SCL/MBDG:
9*22uF (BU)
2*1uF (BU)
4*0.22uF
1*180pF (BU)
2*180pF

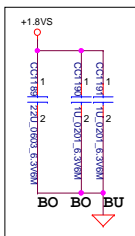
ACROSS VDDIO AND VSS SPLIT



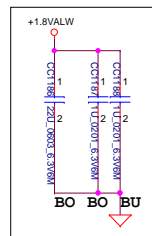
SCL/MBDG:
1 *22uF (B)
1*1uF (BU)



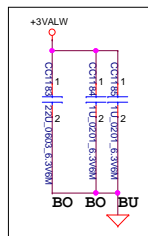
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



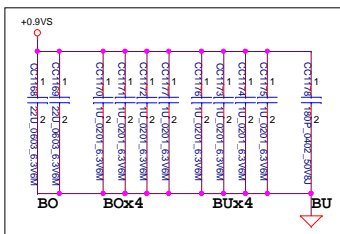
+1.8VALW



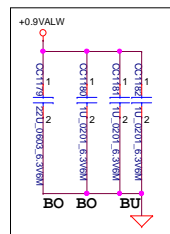
+3VALW



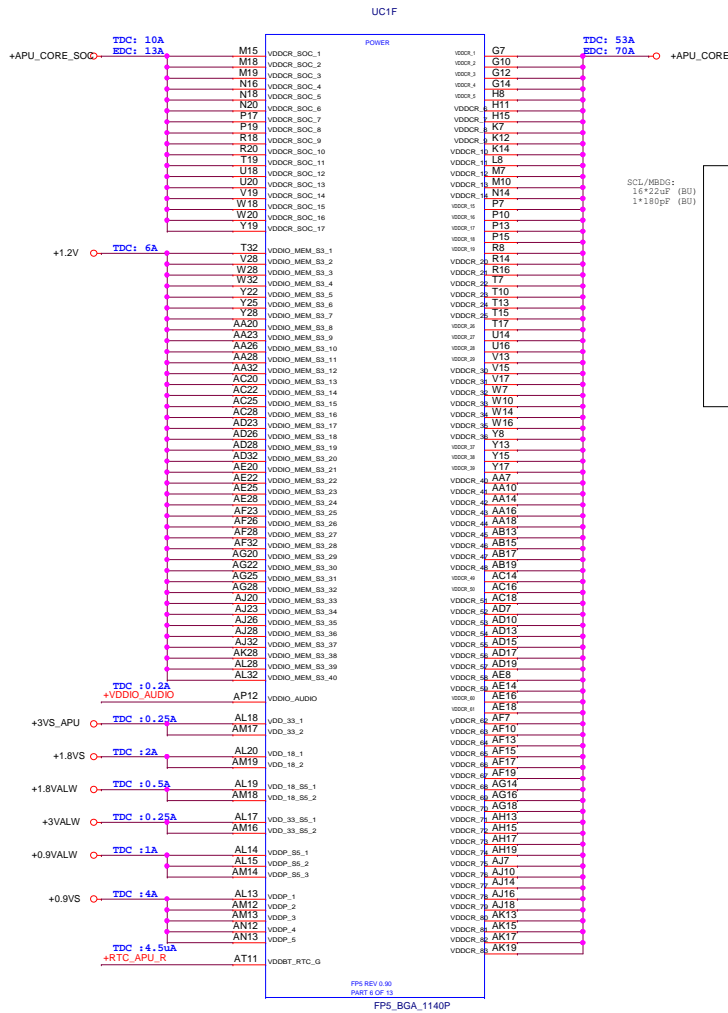
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



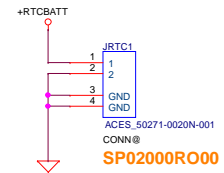
SCL/MBDG:
2 *22uF (BO)
8*1uF (BOx4+BUx4)
1*180pF (BU)



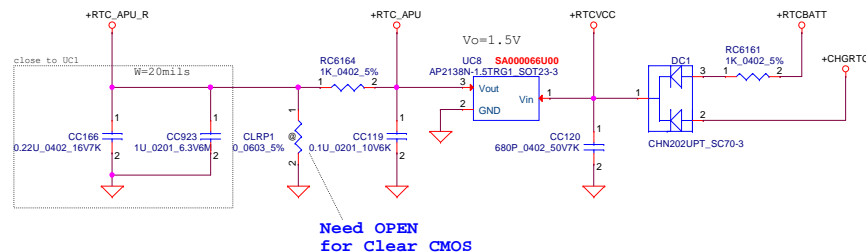
SCL/MBDG:
1 *22uF (B0)
3*1uF (B0x1+BUx2)



```
+APU_CORE Cap place at Power Side
```



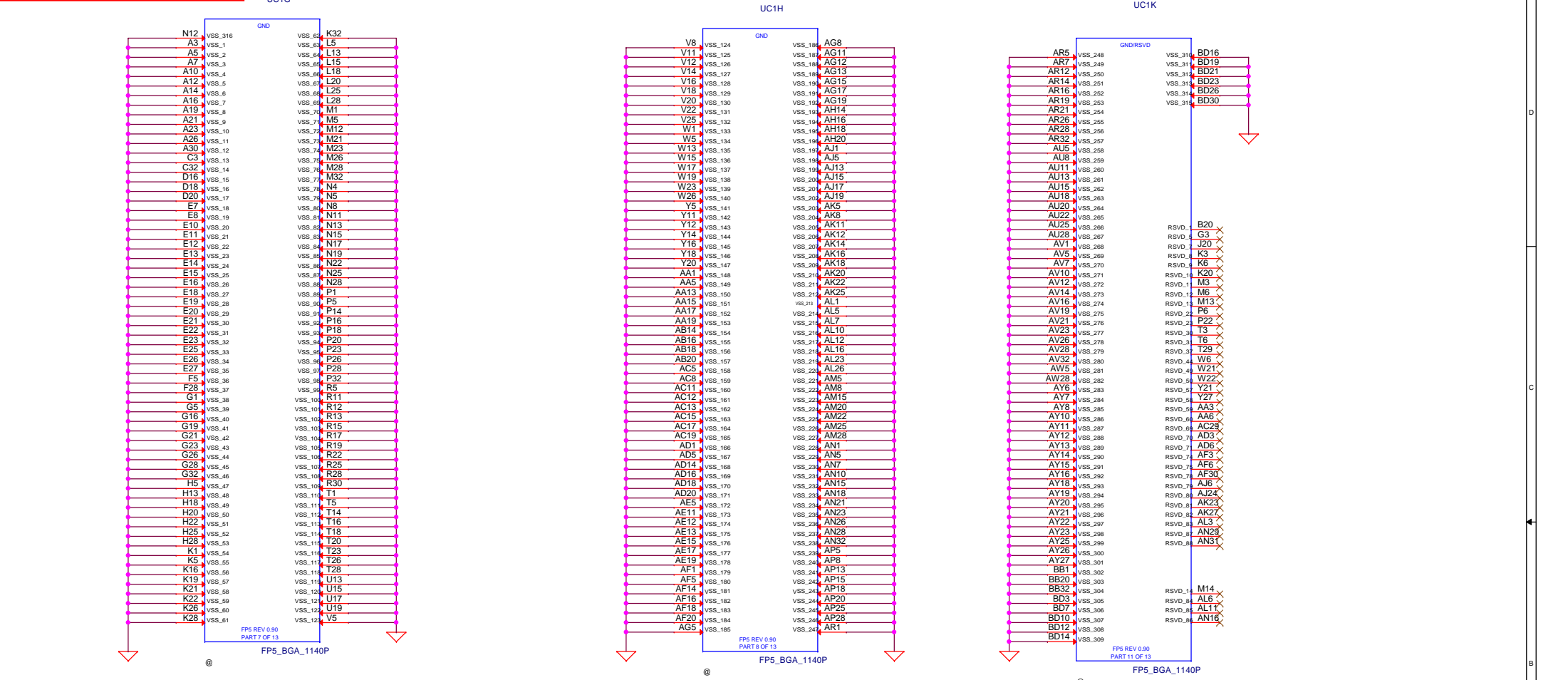
RTC OF APU



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				Custom	FH50P M/B LA-H901P	1A
				Date:	Wednesday, May 15, 2019	Sheet 11 of 99

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Main Func = CPU



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				Size	Document Number	Rev
				Custom	FH50P M/B LA-H901P	1A
				Date:	Wednesday, May 15, 2019	Sheet 12 of 99

Reserve Page

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				Date:	Wednesday, May 15, 2019
				Sheet	13 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	14 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	15 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date:	Wednesday, May 15, 2019
				Sheet	16 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	17 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

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				Date:	Wednesday, May 15, 2019
				Sheet	18 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date:	Wednesday, May 15, 2019
				Sheet	19 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	20 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Sheet	21 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date:	Wednesday, May 15, 2019
				Sheet	22 of 99
				Rev	1A
				FH50P M/B LA-H901P	

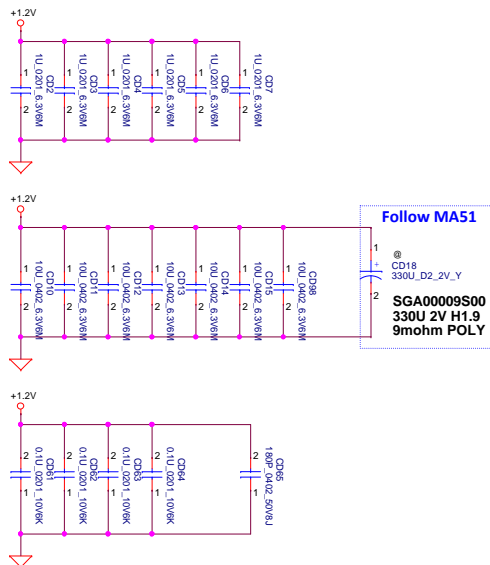
2-3A to 1 DIMMs/channel

Diagram illustrating a 3-phase 4-wire system configuration. The system consists of three parallel RYB phases (R, Y, B) and a common neutral line. Each phase is connected to a 3VS source. The impedances for each phase are labeled as 0.0402 5%. The neutral line is connected to a common point. Labels on the right indicate the connection points for DDR_A_SAT, DDR_A_SA2, and DDR_A_SA0.

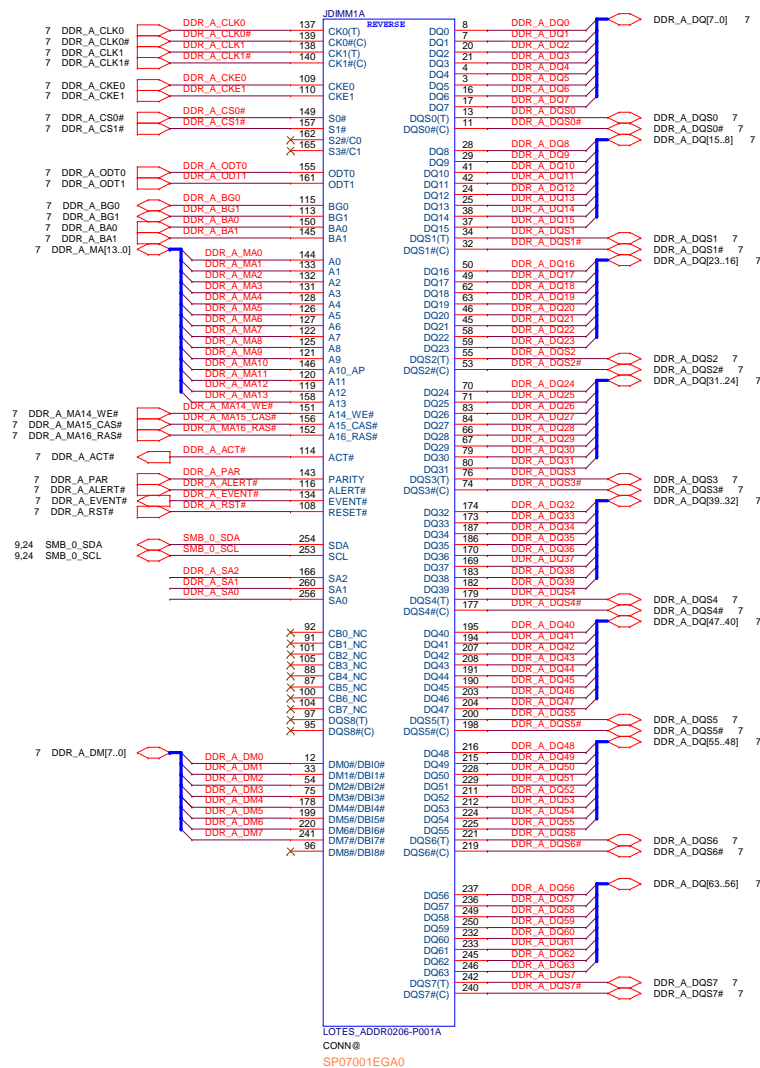
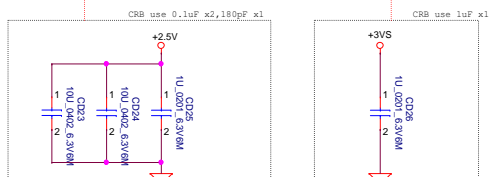
Note:
Check voltage tolerance of
VREF DQ at the DIMM socket

DDR4 support Even Parity check in DRAMs.

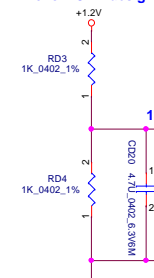
CRB use 0.1uF x12 (6 pop, 6 unpop), 180pF x1, 100uF x2



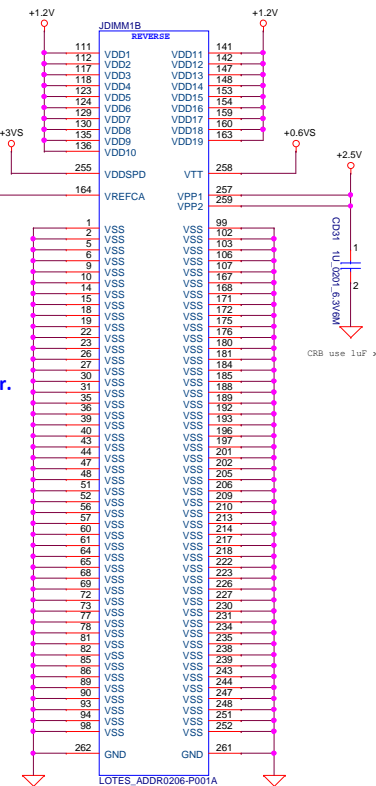
Layout Note:
Place near JDIMM1.255



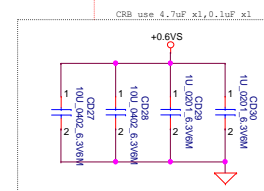
Follow CRB design



Place near to SO-DIMM connector.



Layout Note:
Place near JDIMM1.258



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				Custm	FH50P M/B LA-H901P
				Date:	Wednesday, May 15, 2019
				Sheet	23 of 99

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2-3A to 1 DIMMs/channel

3V3

R0244
10K 0.0402 5%

R0246
0.0402 5%

R0247
0.0402 5%

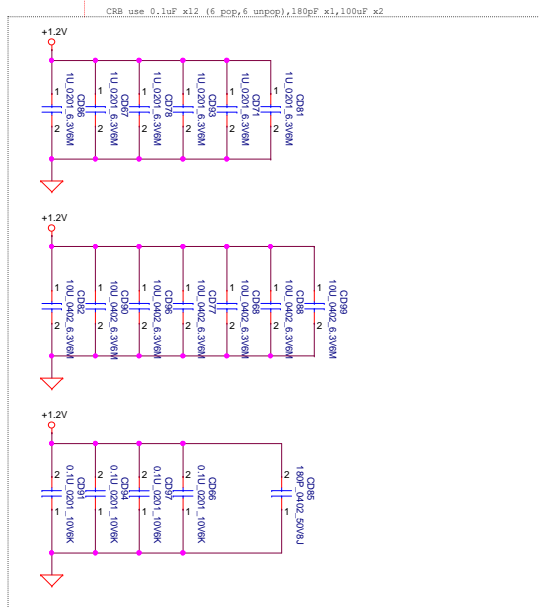
R0248
0.0402 5%

DDR_B_SA2

DDR_B_SA1

DDR_B_SA0

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



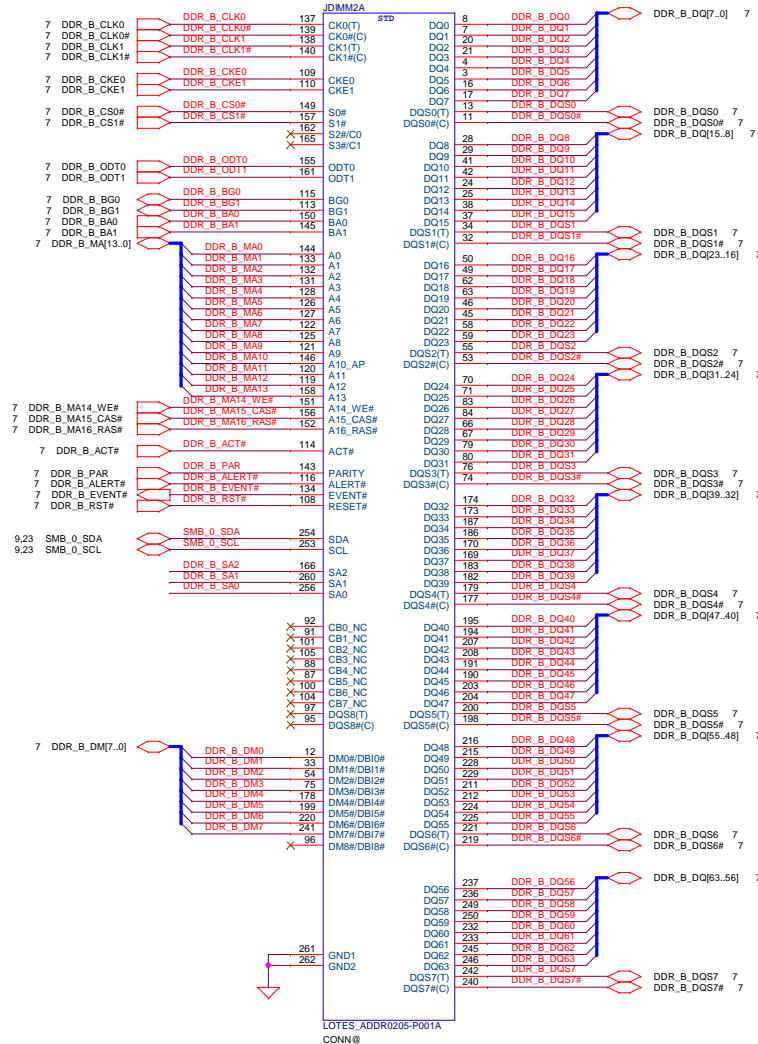
CRB use 0.1uF x2, 180pF x1

CRB3
1 0.001 6.3V6M

CRB5
1 0.002 6.3V6M

CRB1
1 0.002 6.3V6M

A circuit diagram showing a 3V battery connected to a 1000µF capacitor. The capacitor is labeled "1000µF" and "3V". A red box is drawn around the top of the circuit, and a red line connects it to the text "CRB use 1uF x1".

[illegible][illegible]

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				Document Number	
				Customer	FH50P M/B LA-H901P
Date:	Wednesday, May 15, 2019	Sheet	24	of	99

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Reserve Page

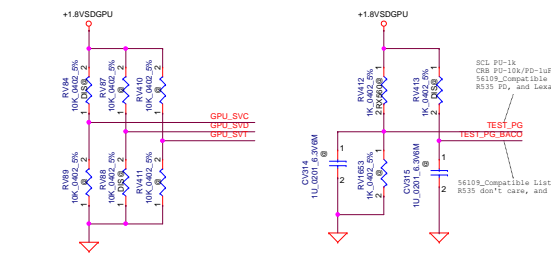
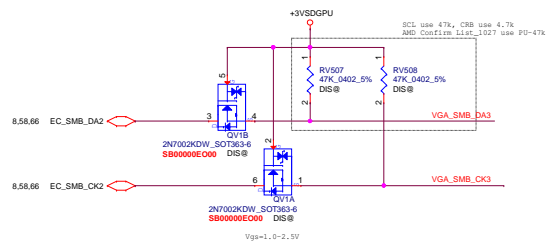
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				Sheet	25 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date:	Wednesday, May 15, 2019
				Sheet	26 of 99
				Rev	1A
				FH50P M/B LA-H901P	



Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

RX560 Strap

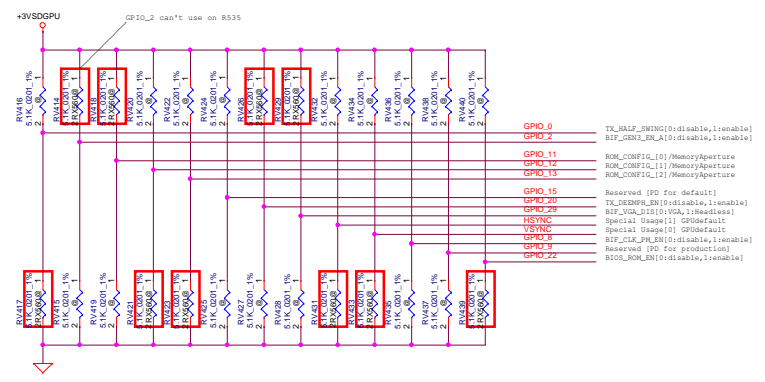
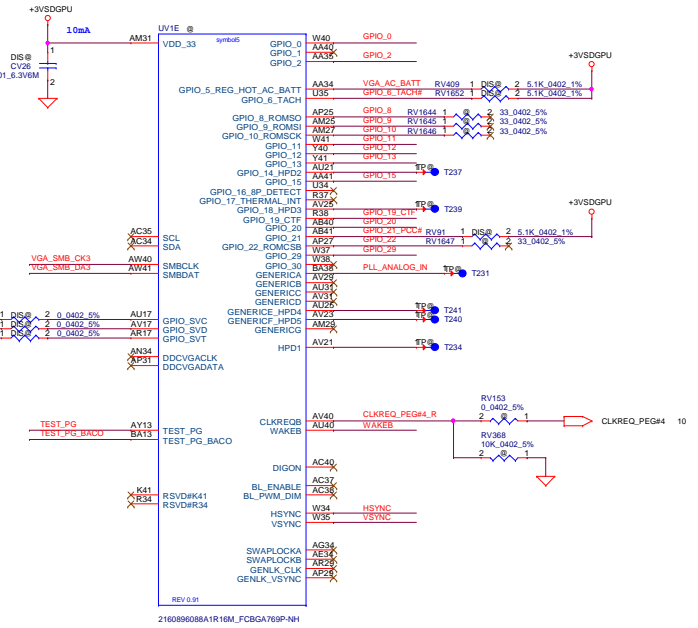


Table 3-27 Primary Memory Aperture Sizes Requested at PCI Configuration

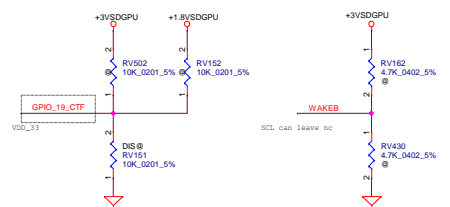
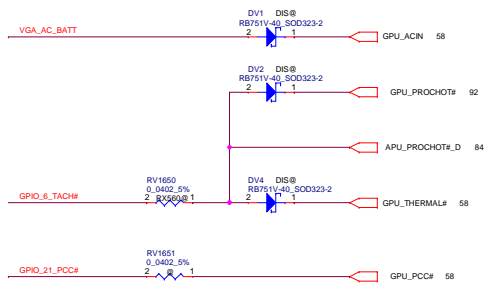
Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110

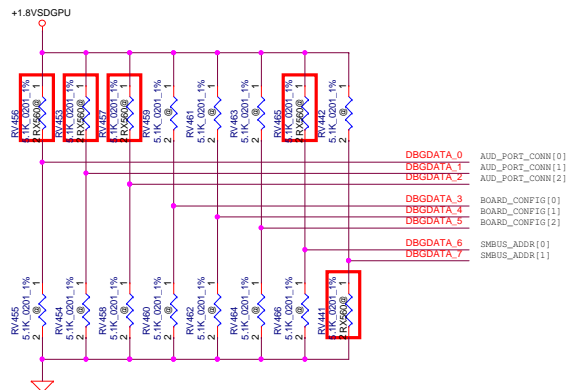
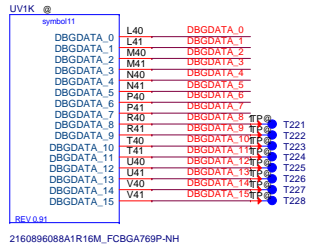
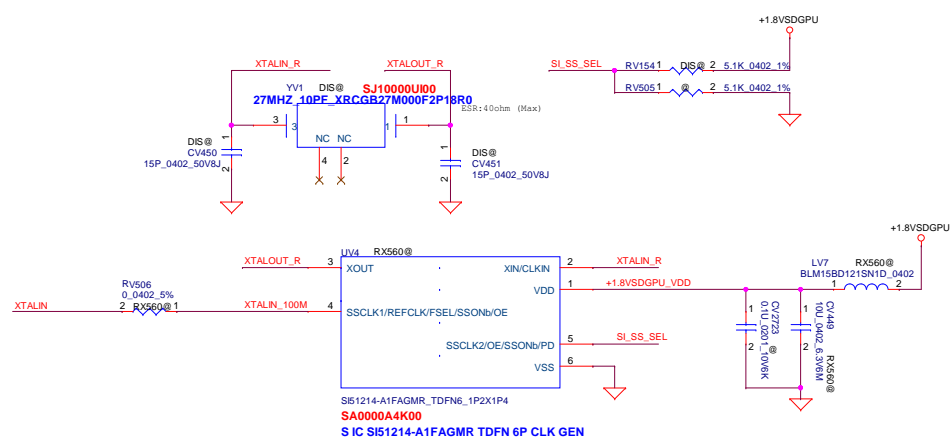
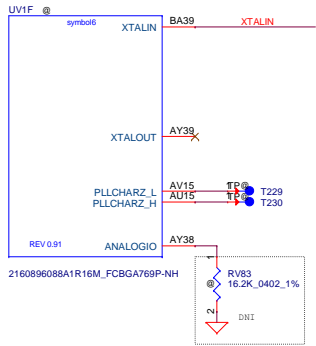
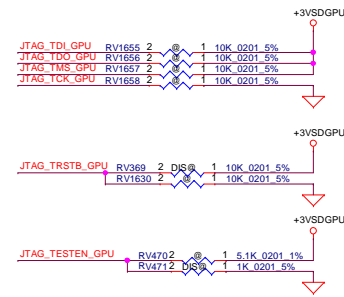
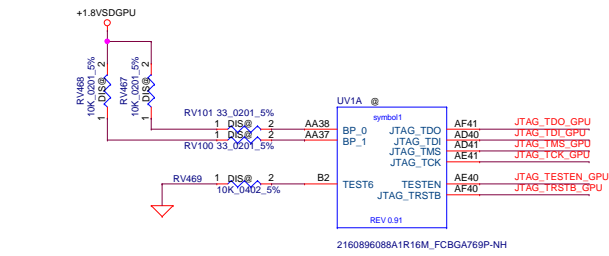
3.22.2 ROM Configurations

- For designs that have a dedicated ROM device for the GPU video BIOS:
- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
 - Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).



Function Support	Pin	R18M-G1-90	R17M-G1-90/75
AC/DC Mode	GP105	Yes	Yes
Thermal VR_HOT# (Fan tachometer)	GP106	No	Yes
Peak Current Control	GP1021	No	Yes

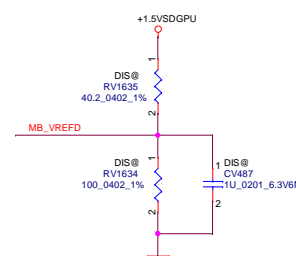
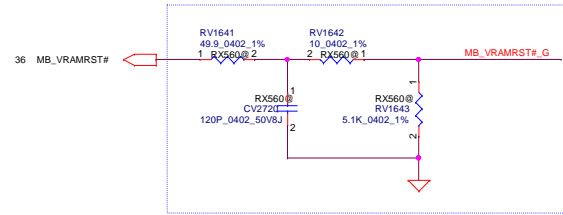
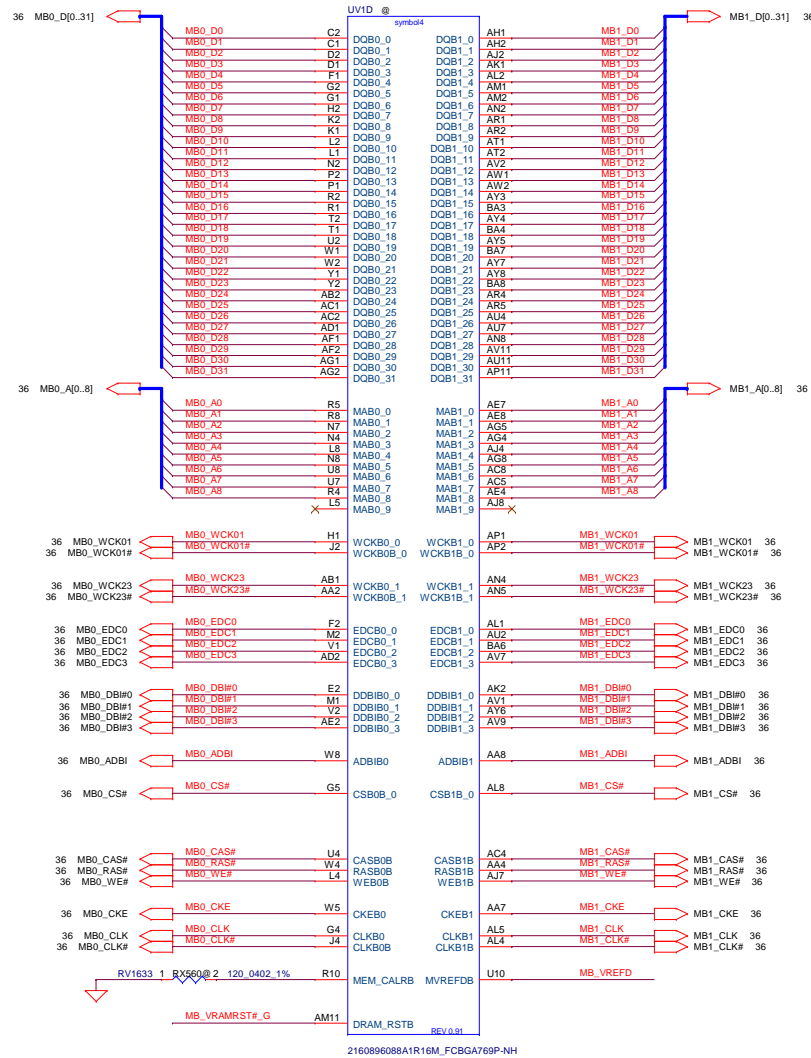
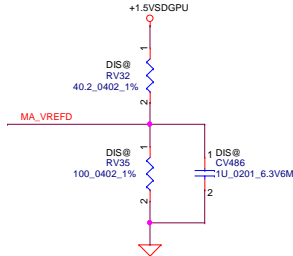
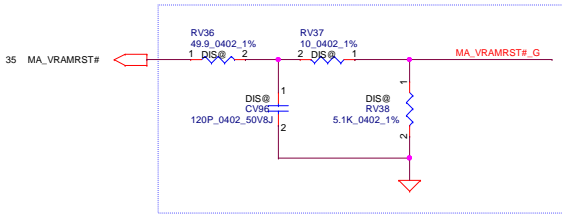
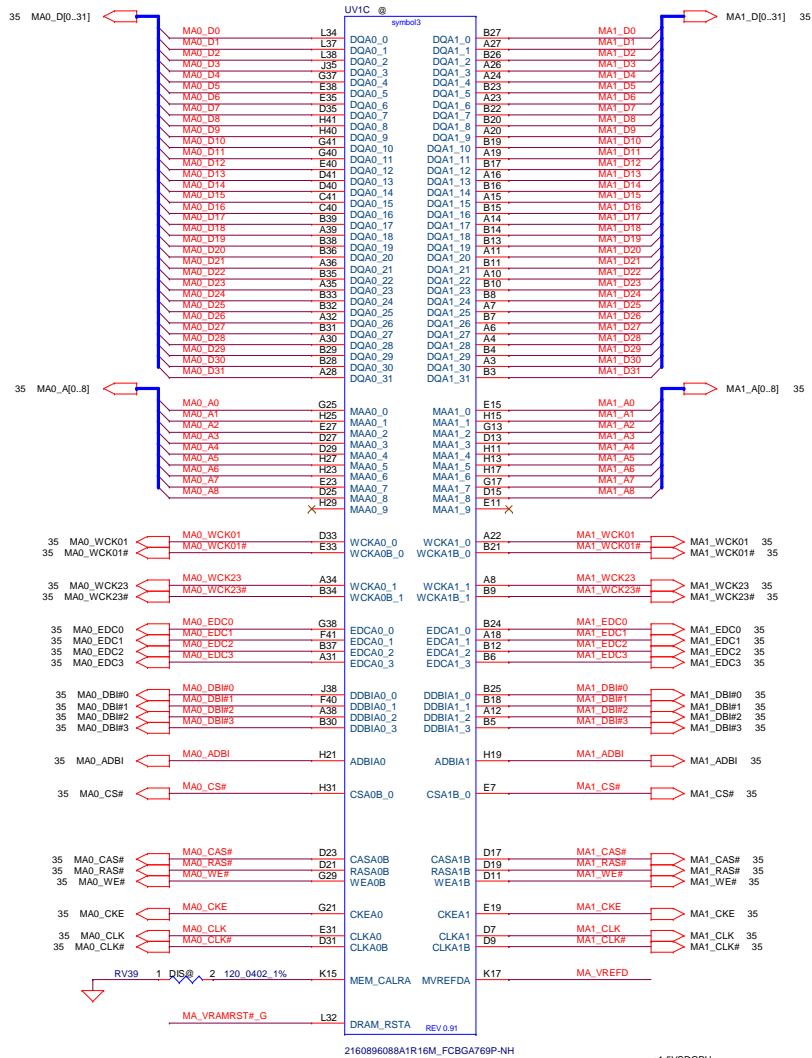


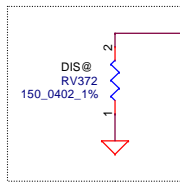
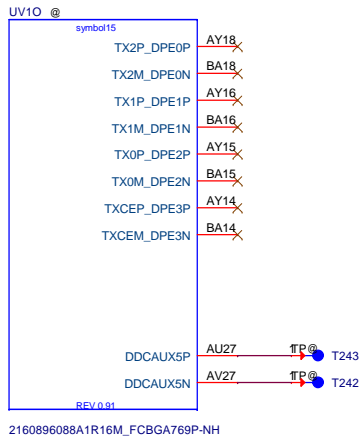


AUD_PORT_CONN [2:6]
* 111: No usable endpoints
110: One usable endpoint
101: Two usable endpoints
100: Three usable endpoints
011: Four usable endpoints
010: Five usable endpoints
001: Six usable endpoints
000: All endpoints are usable

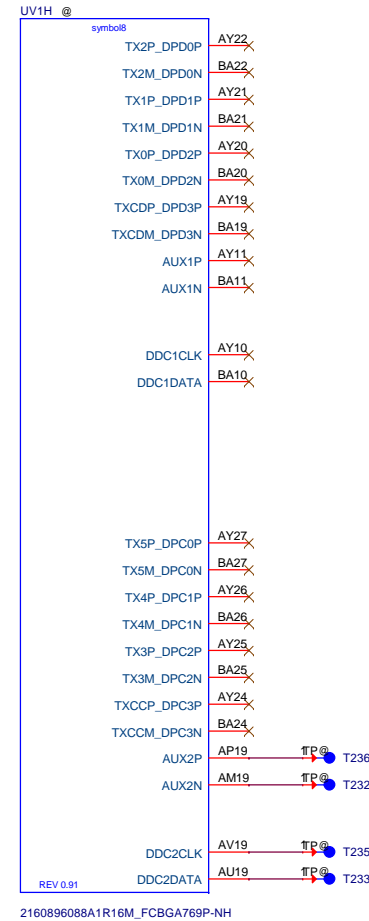
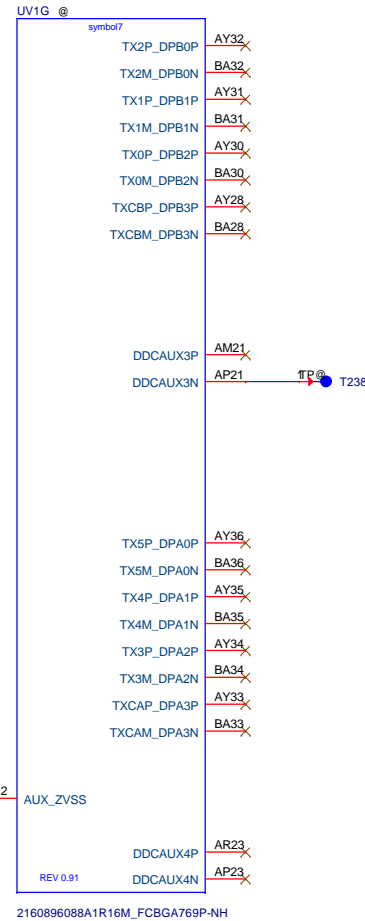
BOARD_CONFIG [2:6]
000: SMT 256Mx32 (8Gb)
001: Hynix 256Mx32 (8Gb)
010:
011:
100:
101:
110:
111:
(BOM at Page33)

DBGDATA [7:6]
* 00: 0x40
01: 0x41
10: 0x42
11: 0x43

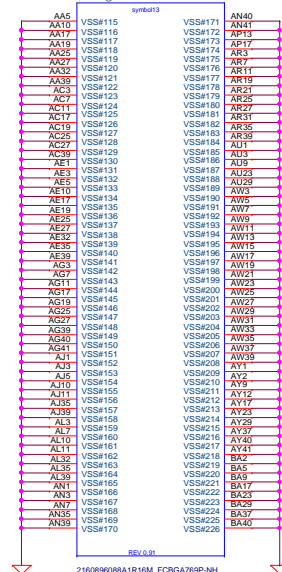
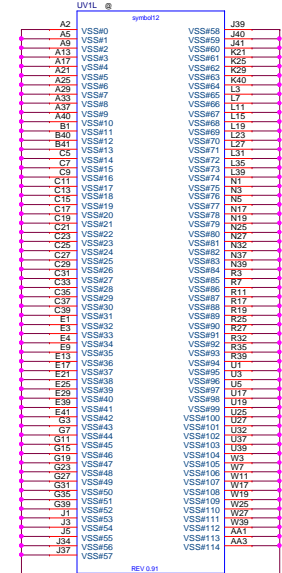
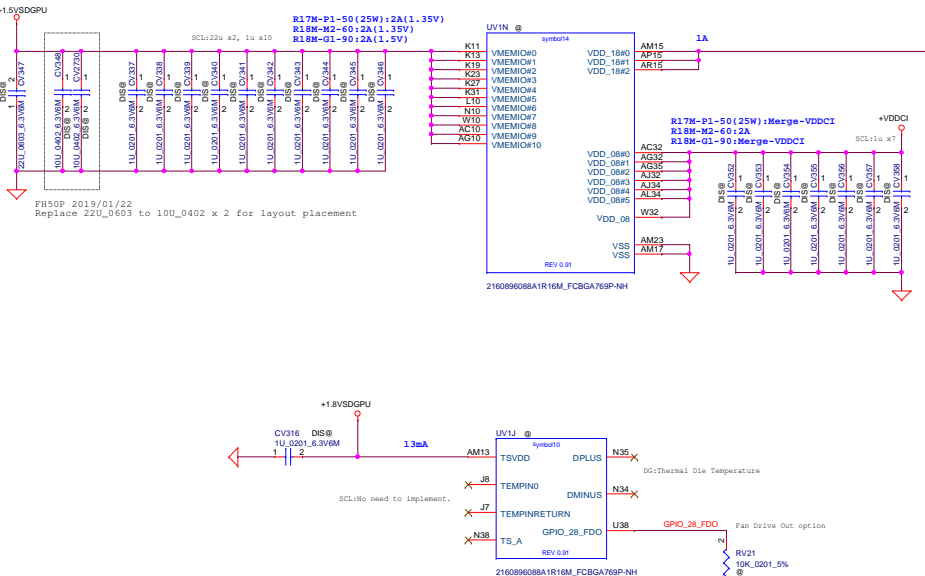
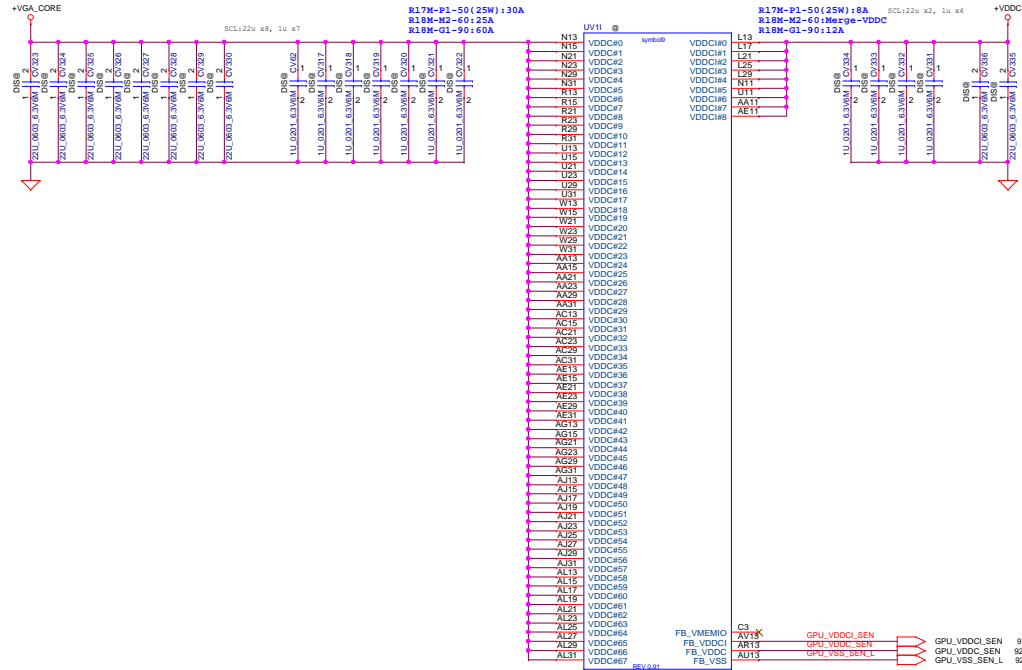




Data Book: need
config even if not
use display function



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				Date: Wednesday, May 15, 2019	Sheet 31 of 99
				Rev 1A	

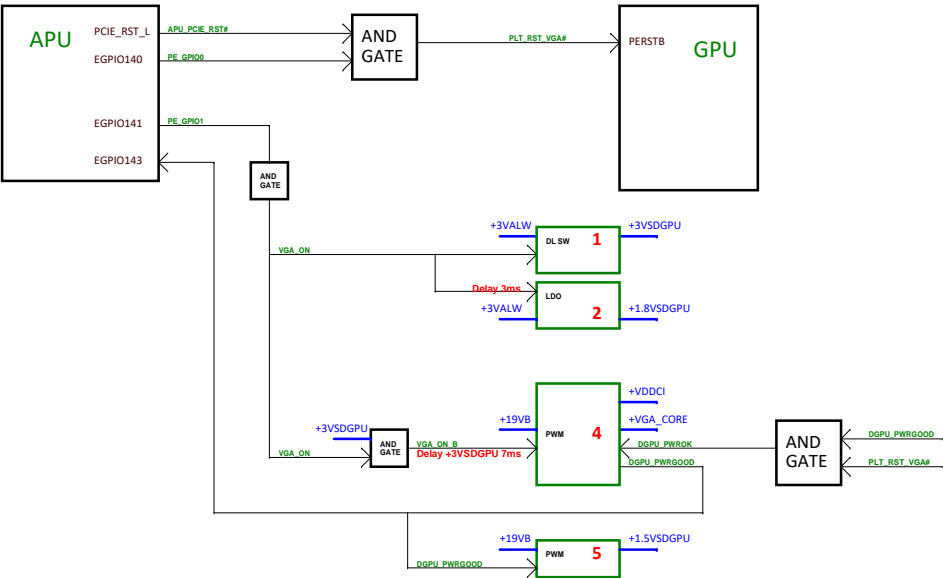
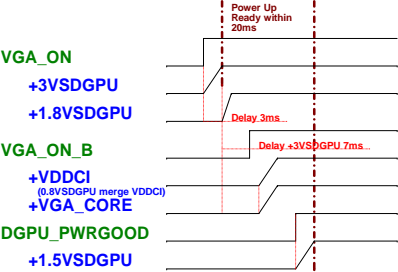


5.3 Power-up/down Sequence

"R17M-G1-50 / R17M-G1-70 / R18M-G1-90" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/μs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

R18M-G1-90



For AMD R18M-G1-90 VRAM Device ID: 67EF/C0

Memory ID/Vendor/Size	Memory PN R3(ABOI)	BOARD_CONFIG[2:0]	DBGDATA_3 (H: RV463, L: RV464) DBGDATA_2 (H: RV464, L: RV462) DBGDATA_1 (H: RV459, L: RV460)
000 (8Gb) SAMSUNG 256M x32	UV1001 X78_S4G@ UV1002 X78_S4G@ UV1003 X78_S4G@ UV1004 X78_S4G@ S IC D5 256M32 K4G80325FB-HC25 FBGA ABOI SA00009TA10	RV464 X78_S4G@ RV462 X78_S4G@ RV460 X78_S4G@ S RES 1/20W 5.1K +/-1% 0201 SD000008900	
001 (8Gb) HYNIX 256M x32	UV1001 X78_H4G@ UV1002 X78_H4G@ UV1003 X78_H4G@ UV1004 X78_H4G@ S IC D5 256M32 H5GC8H24AJR-R2C BGA ABOI SA0000C1700	RV464 X78_H4G@ RV462 X78_H4G@ RV460 X78_H4G@ S RES 1/20W 5.1K +/-1% 0201 SD000008900	
010 SAMSUNG 128M x32			
011 HYNIX 128M x32			
100 MICRON 256M x32			

AMD GPU PN

R18M-G1-90 PN R1(ROH)
UV1 RX560@
S IC 215-0908004 A1 R18M-G1-90 ABOI SA0000BFF10

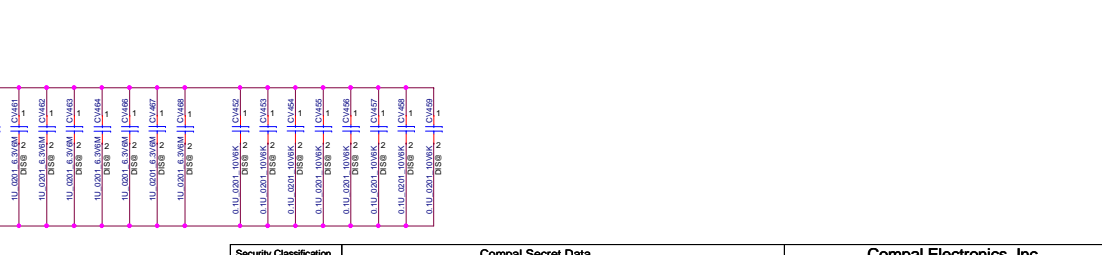
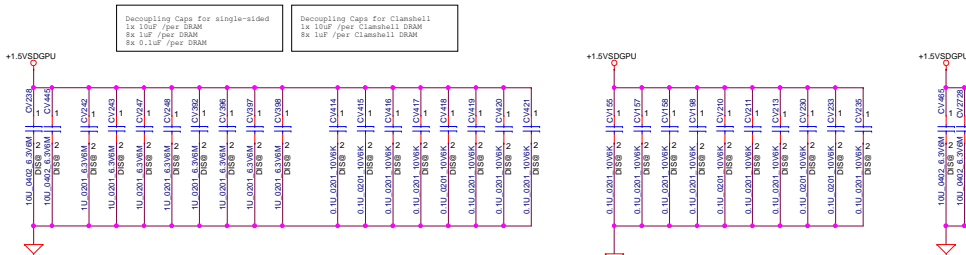
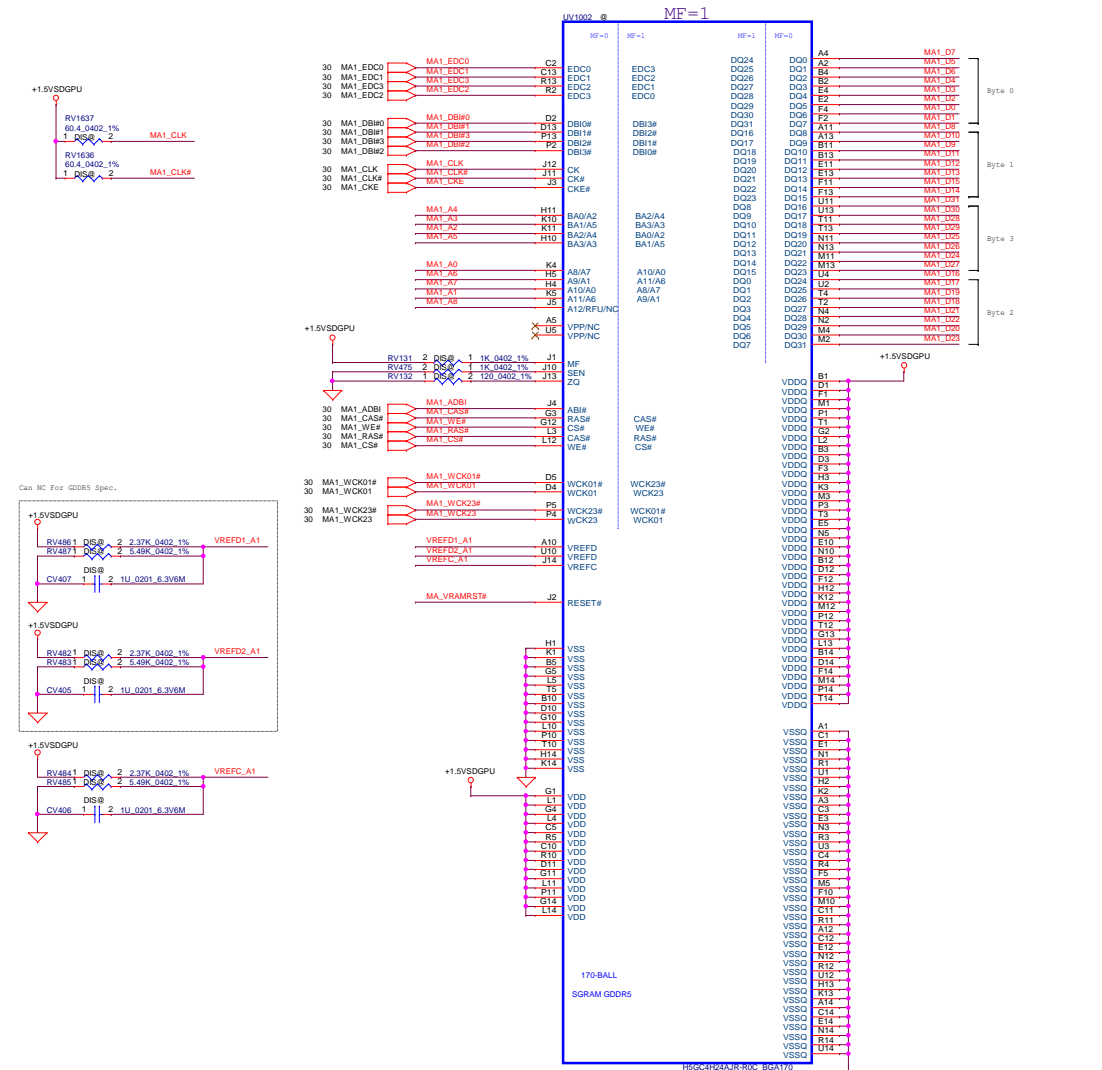
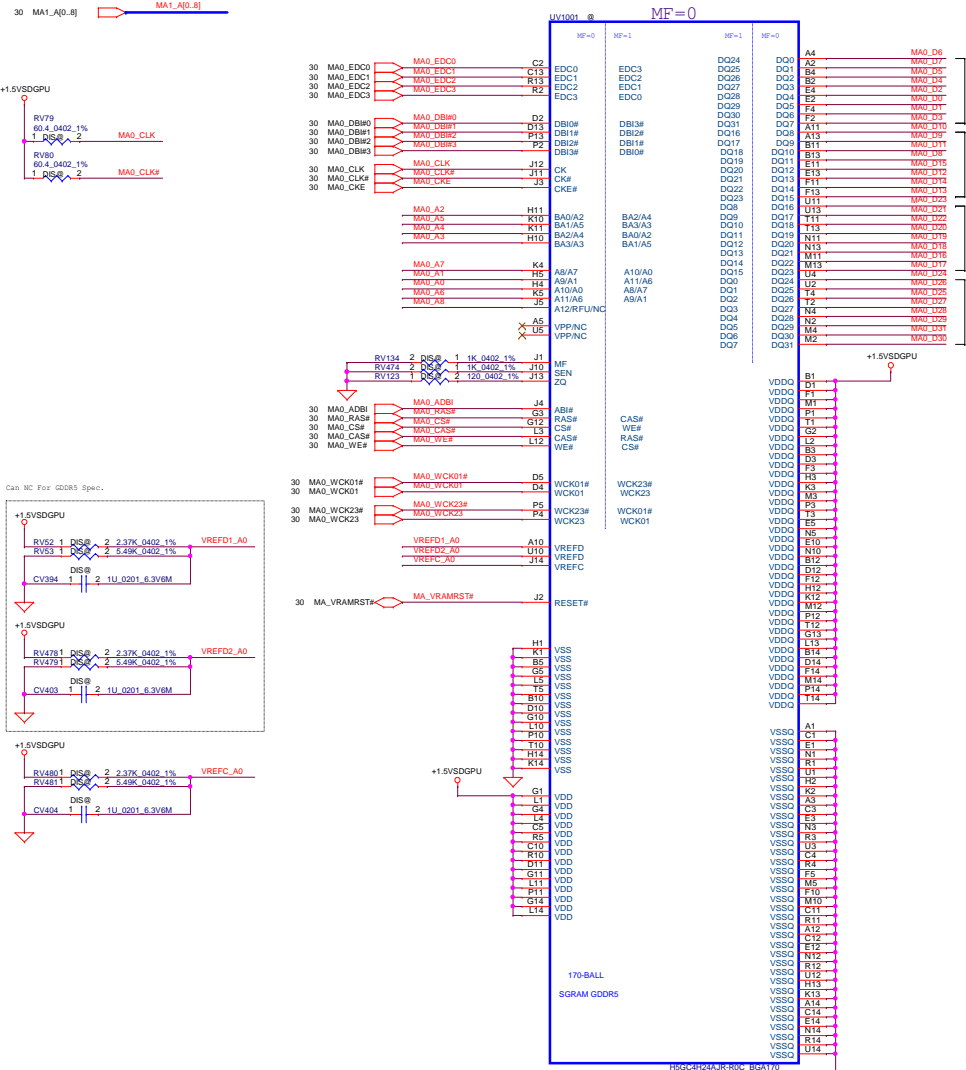
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				Date	Wednesday, May 15, 2019
				Sheet	34 of 99
				Rev	1A
				FH50P M/B LA-H901P	

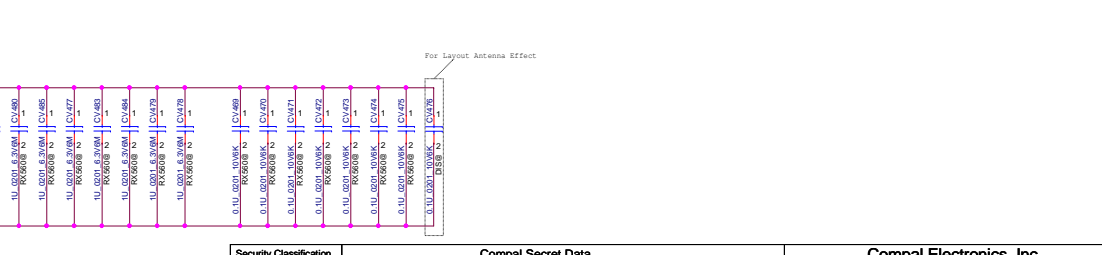
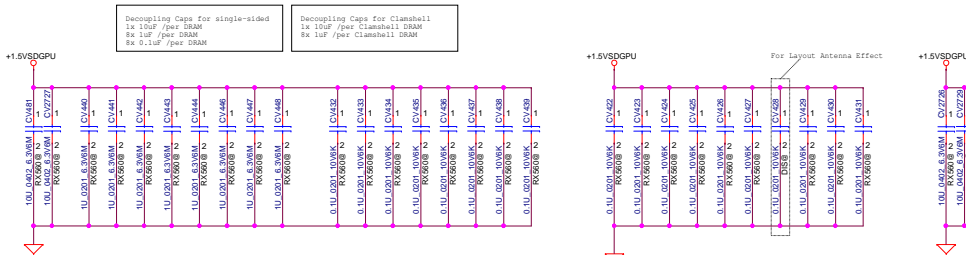
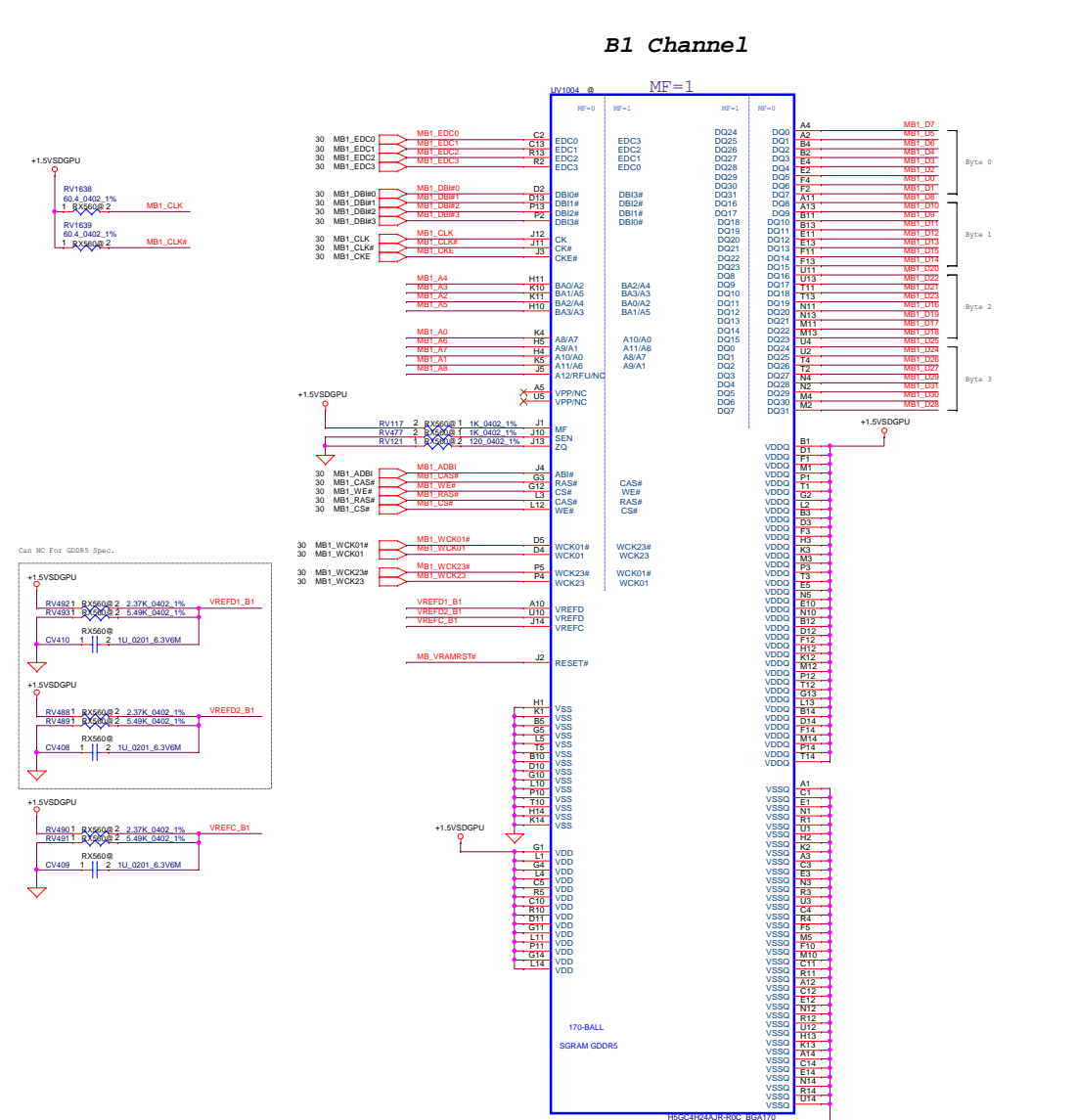
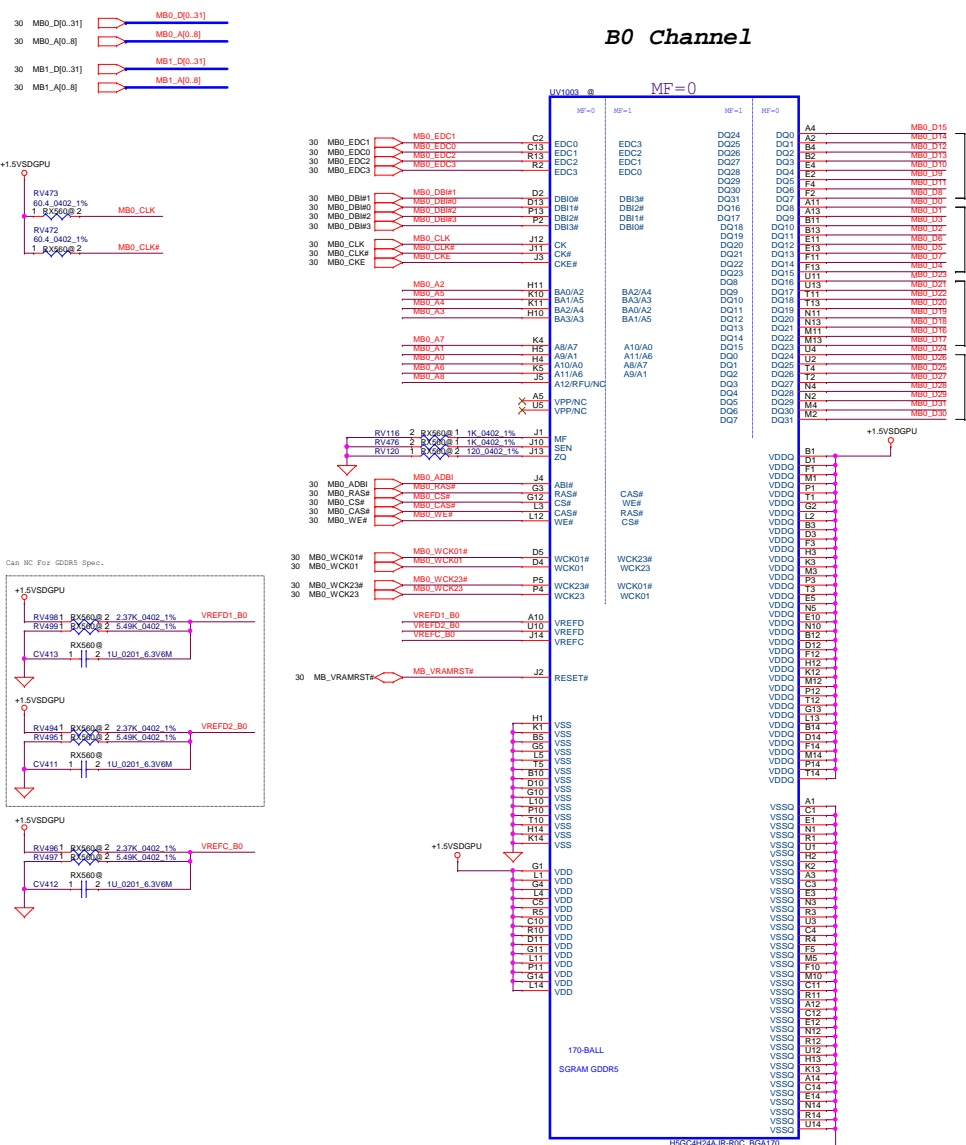
A0 Channel

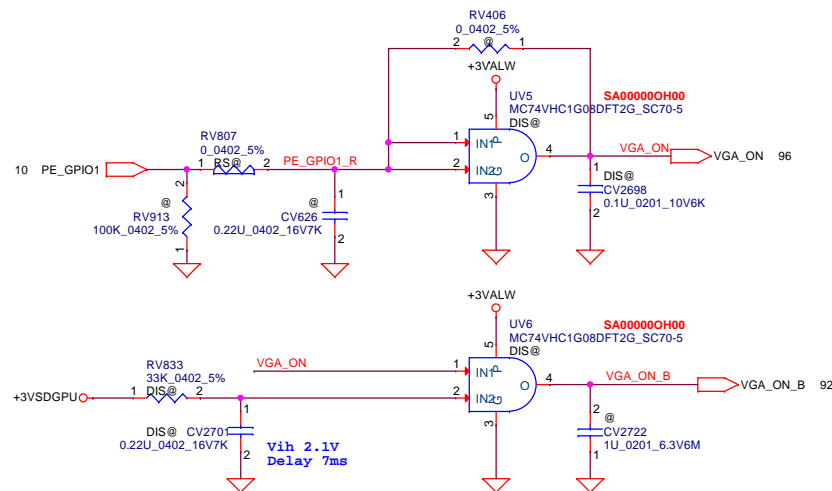
A1 Channel



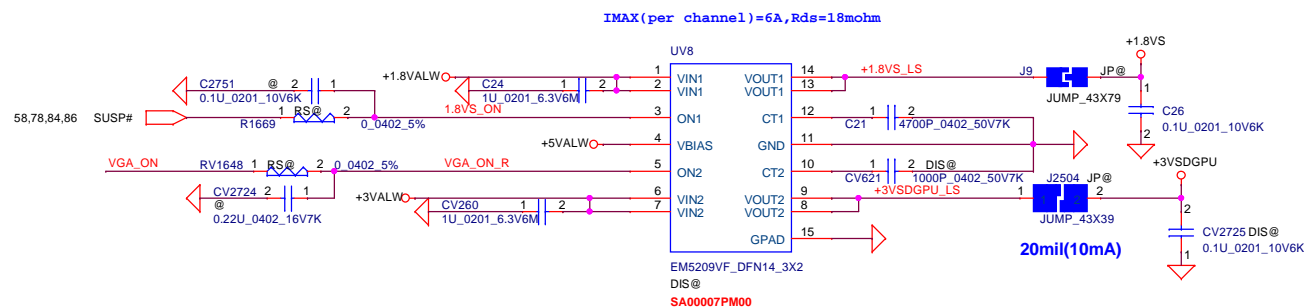
B0 Channel1

B1 Channel1





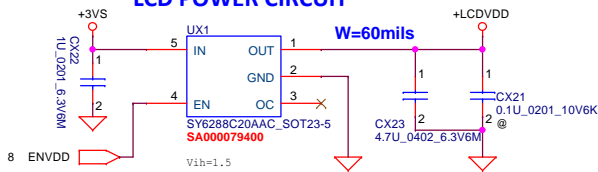
+3VALW TO +3VSDGPU



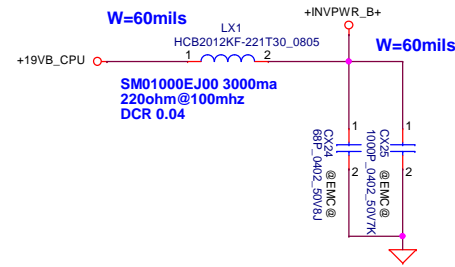
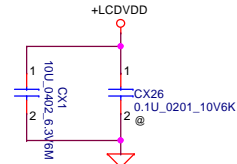
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				Date	Wednesday, May 15, 2019
				Sheet	37 of 99
				Rev	1A
				FH50P M/B LA-H901P	

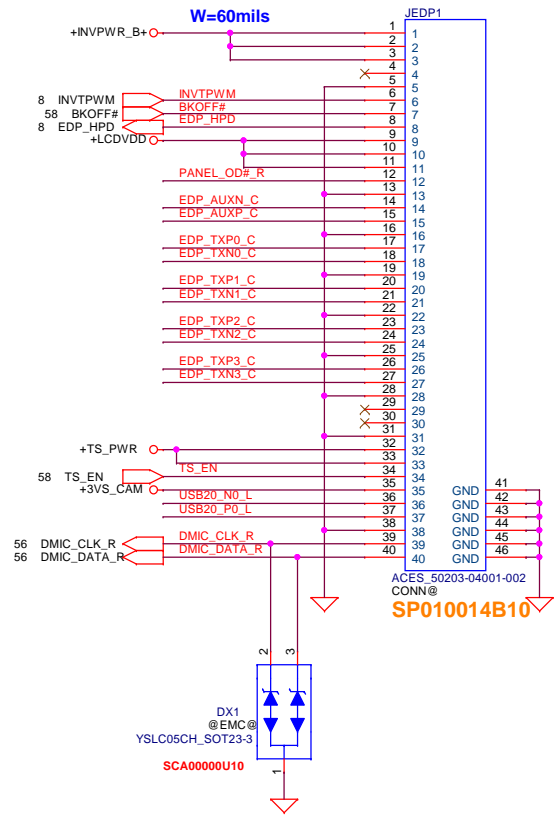
LCD POWER CIRCUIT



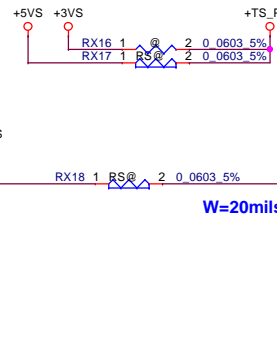
Place closed to JEDP1



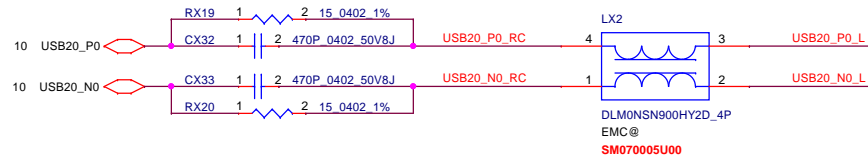
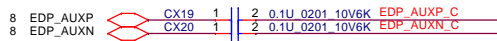
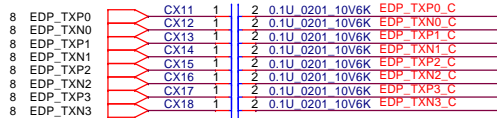
LED PANEL Conn.



Touch Screen



Place closed to JEDP1



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Size	Custom	Document Number	FH50P M/B LA-H901P	Rev	1A
Date:	Wednesday, May 15, 2019	Sheet	38	of	99

Reserve Page

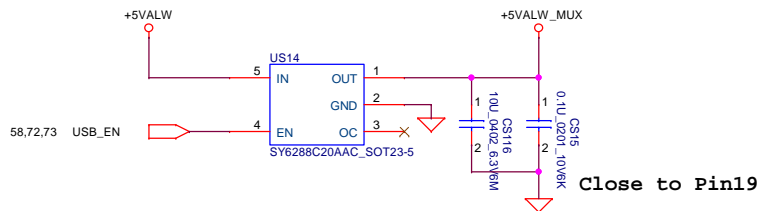
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				Date:	Wednesday, May 15, 2019
				Sheet	39 of 99
				Rev	1A
				FH50P M/B LA-H901P	

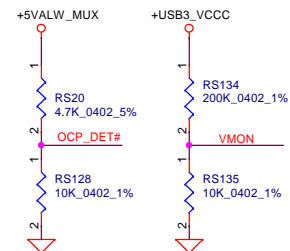
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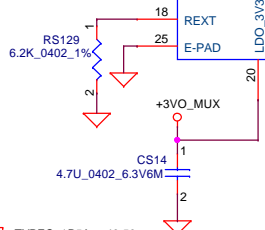
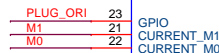
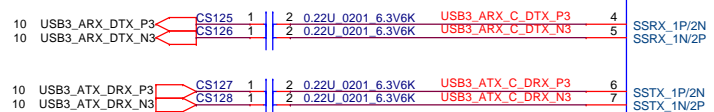
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				Sheet	41 of 99
				Rev	1A
				FH50P M/B LA-H901P	



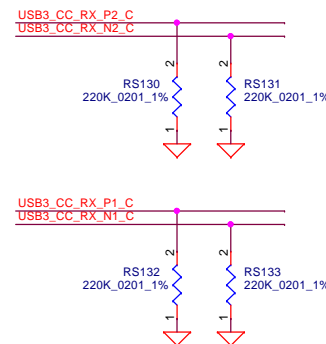
Close to Pin19



USB3.0 (Port 3)



Close to Pin13



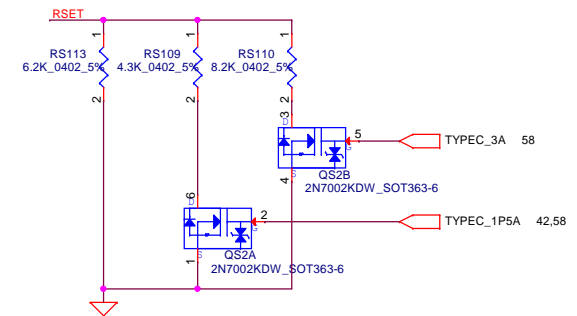
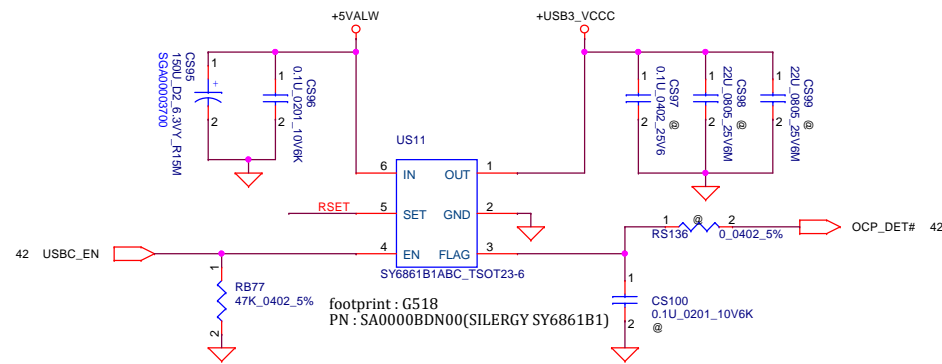
5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

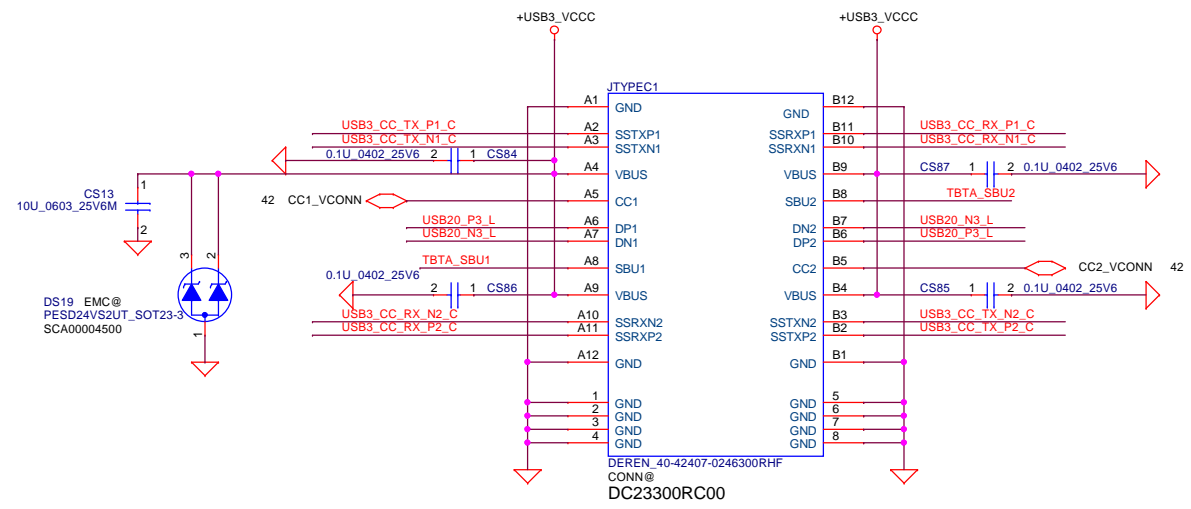
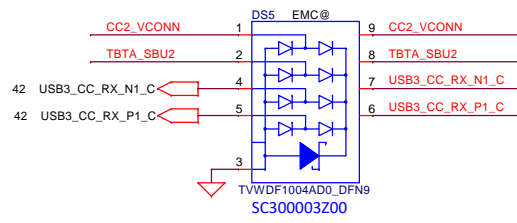
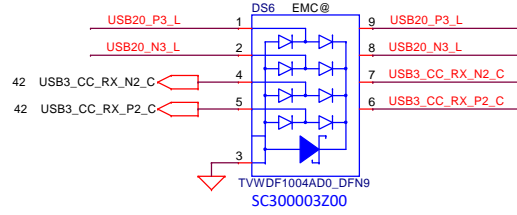
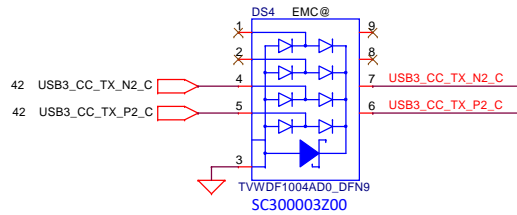
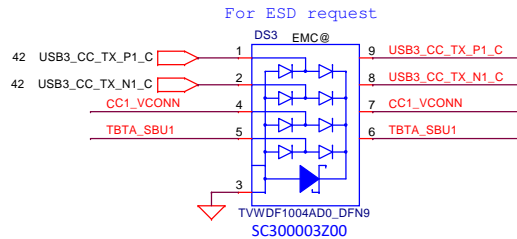
confirm realtek hand-shake

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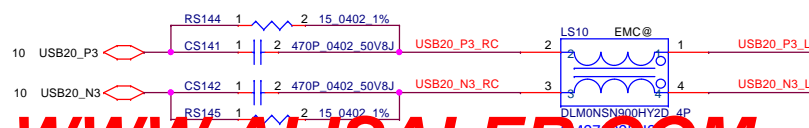
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				Document Number	FH50P M/B LA-H901P
				Date	Wednesday, May 15, 2019
				Sheet	42 of 99
				Rev	1A



SILERGY SY6861B1 MOS Current Limit				
TYPEC_1P5A	TYPEC_3A	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



CC1_VCONN & CC2_VCONN need 20mil trace width.



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				Custom				FH50P M/B LA-H901P			
				Date				Wednesday, May 15, 2019			
				Sheet				43 of 99			

Reserve Page

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				Date	Wednesday, May 15, 2019
				Sheet	44 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	45 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	46 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	47 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	48 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

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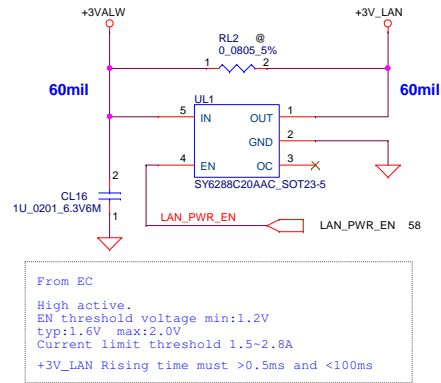
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				Date	Wednesday, May 15, 2019
				Sheet	49 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

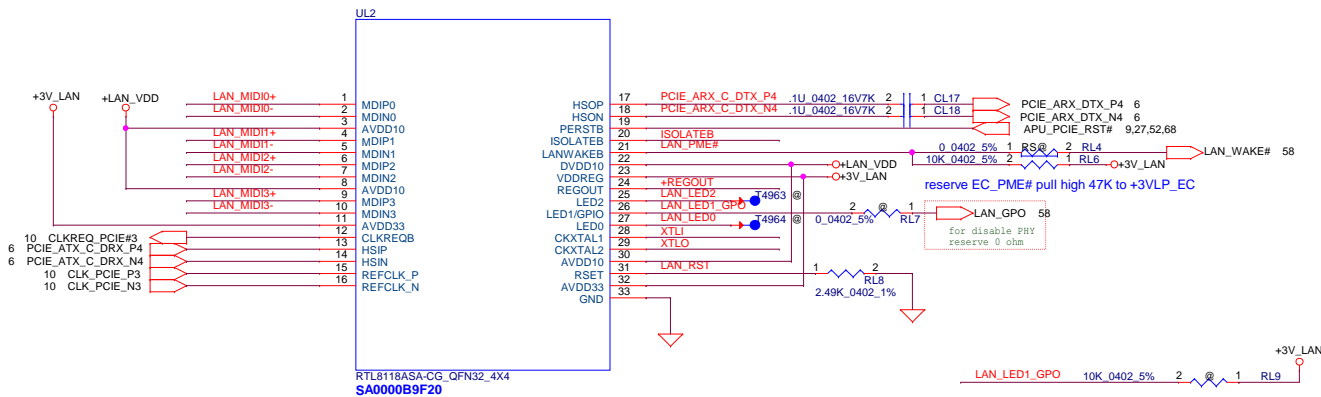
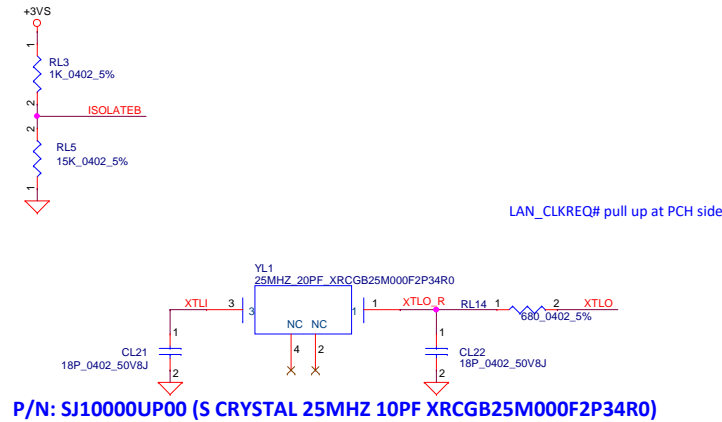
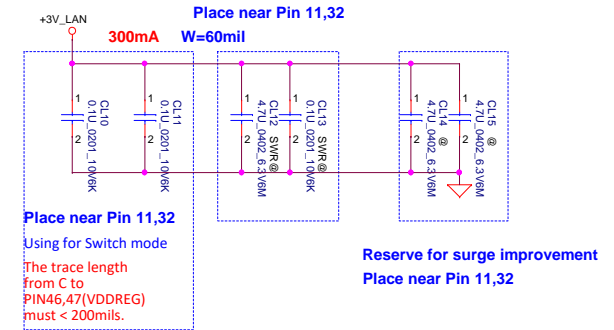
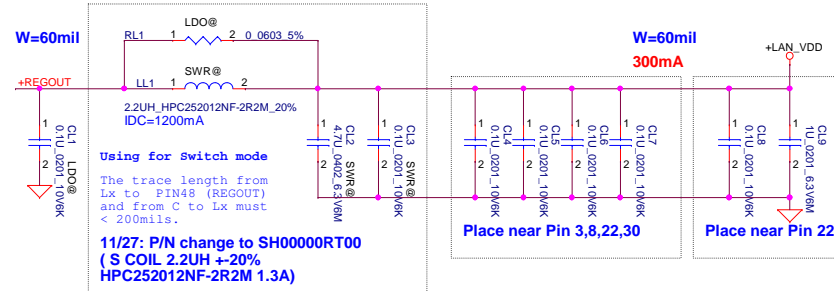
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				Date	Wednesday, May 15, 2019
				Sheet	50 of 99
				Rev	1A
				FH50P M/B LA-H901P	

+3V_LAN Rising time (10%-90%) must >0.5mS and <100mS

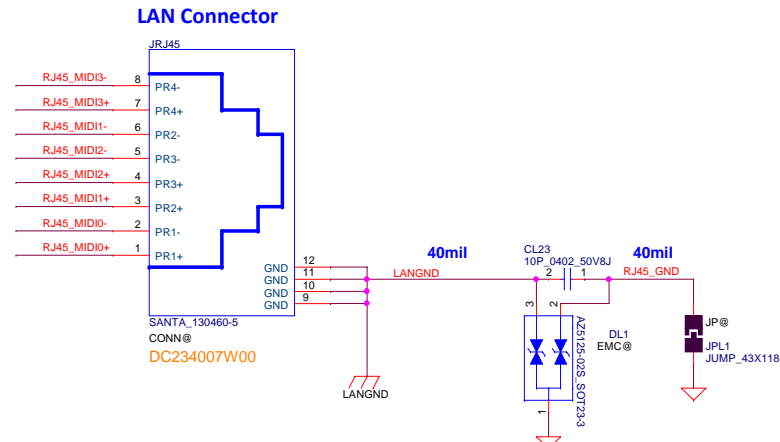
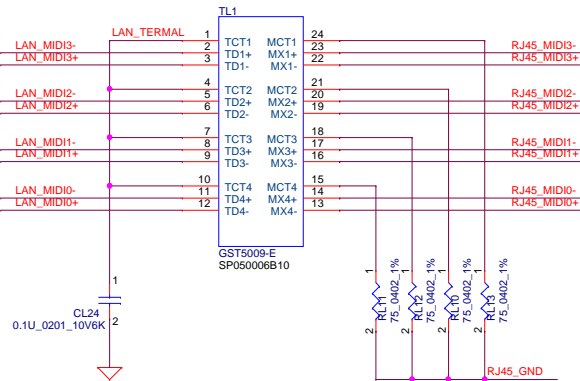


RTL8111H LDO mode
RTL8118ASA SWR mode



P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)

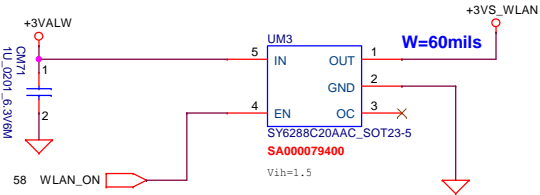
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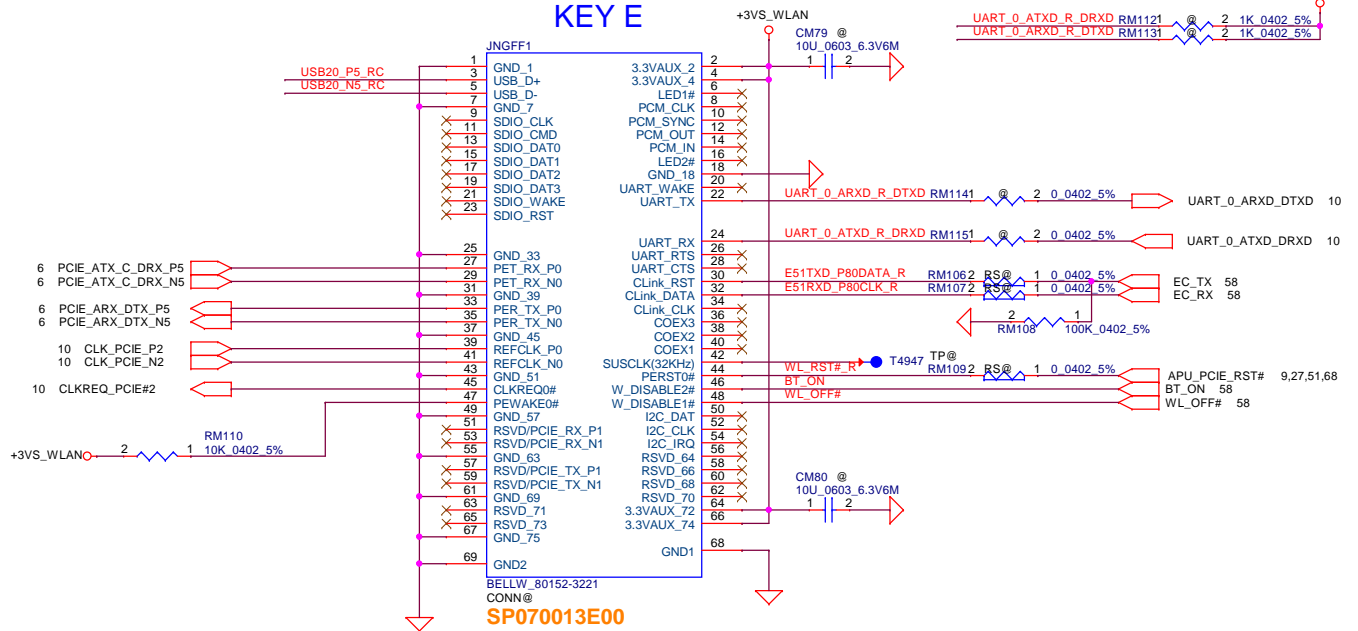
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				Date:	Wednesday, May 15, 2019
				Sheet	51 of 99

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74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKIN1	73
70	UM_Power_BPC/GPIO/PWAKE#	RESERVED/REFCLKIN1	71
68	UM_Power_SINK/CLKREQ1#	GND	69
66	UM_SWP/PERST#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERTW (IO/Q3.3)	GND	63
60	QCC CLK (IO/Q3.3)	Reserved/PTn1	61
58	QCC DATA (IO/Q3.3)	Reserved/PTP1	59
56	W_DISABLEn (OIO/Q3.3V)	GND	57
54	Reserved_W_DISABLE2 (OIO/Q3.3V)	PWAKEOr (OIO/Q3.3V)	55
52	PERSTW (OIO/Q3.3V)	CLKREQOr (OIO/Q3.3V)	53
50	SUSCLK(32MHz) (OIO/Q3.3V)	GND	51
48	CODEK1 (IO/Q3.1.8V)	REFCLKIN0	49
46	CODEK2 (IO/Q3.1.8V)	REFCLKP0	47
44	CODEK3 (OIO/Q3.1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	PTn0	39
36	UART RTS (IO/Q3.1.8V)	PTP0	37
34	UART CTS (IO/Q3.1.8V)	GND	35
32	UART Tx (IO/Q3.1.8V)	GND	33
22	UART Rx (IO/Q3.1.8V)	SDIO Reset (OIO/Q3.1.8V)	23
20	UART Wake# (IO/Q3.3V)	SDIO Wake# (IO/Q3.1.8V)	21
18	GND	SDIO DATA3 (IO/Q3.1.8V)	19
16	LED2# (IO/GND)	SDIO DATA2 (IO/Q3.1.8V)	17
14	PCM_OUT/IS_SD_OUT (OIO/Q3.1.8V)	SDIO DATA1 (IO/Q3.1.8V)	15
12	PCM_IN/IS_SD_IN (IO/Q3.1.8V)	SDIO DATA0 (IO/Q3.1.8V)	13
10	PCM_SYNC/IS WS (OIO/Q3.1.8V)	SDIO CMD0 (IO/Q3.1.8V)	11
8	PCM_CLK/IS SCK (IO/Q3.1.8V)	SDIO CLK0 (OIO/Q3.1.8V)	9
6	LED1# (IO/GND)	GND	7
4	3.3V	USB_D-#	5
2	3.3V	USB_D+ #	3
		GND	1



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Date:		Wednesday, May 15, 2019		Sheet	52	of	99

Reserve Page

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				Date	Wednesday, May 15, 2019
				Sheet	53 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	54 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date	Wednesday, May 15, 2019
				Sheet	55 of 99
				Rev	1A
				FH50P M/B LA-H901P	

2000mA 600ohm@100MHz
DCR 0.1



40r

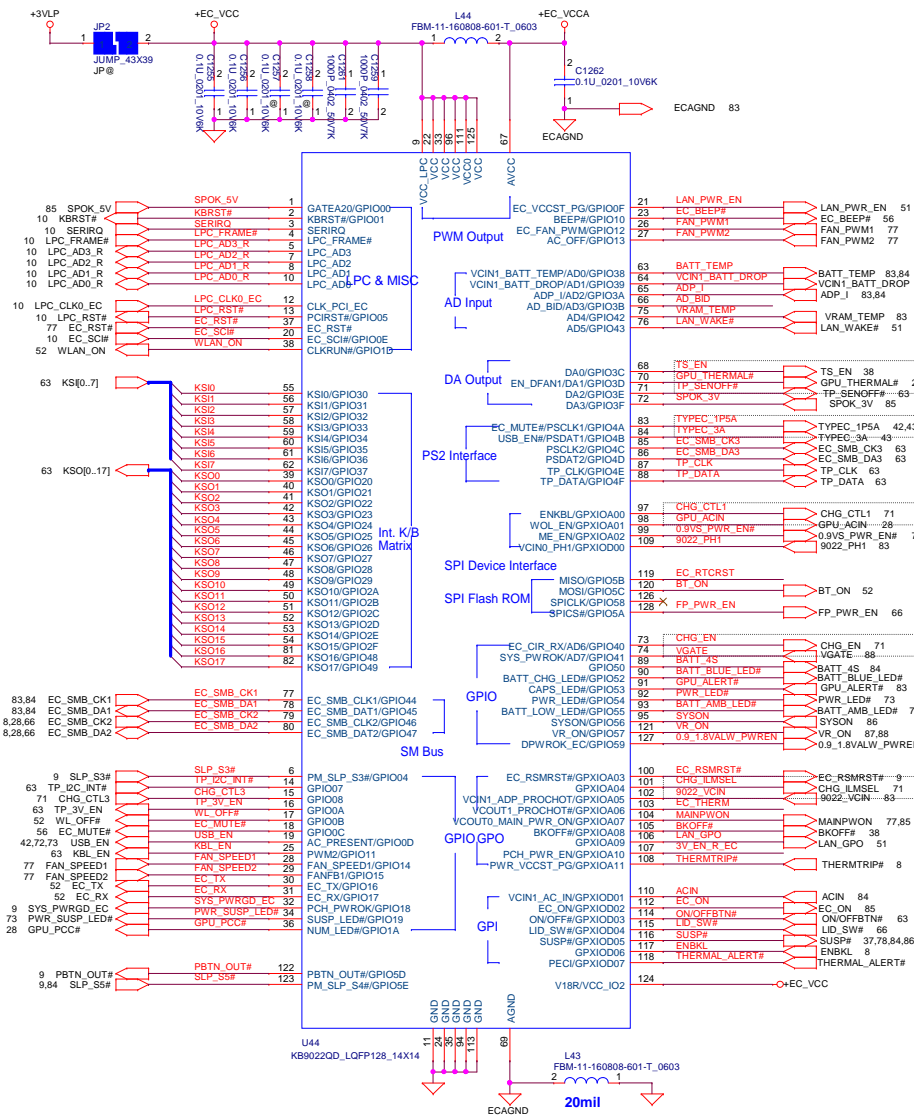
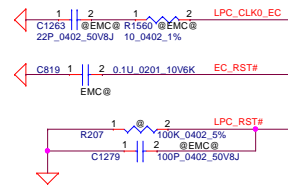


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						Customer	FH50P M/B LA-H901P		1A
						Date:	Wednesday, May 15, 2019	Sheet	56

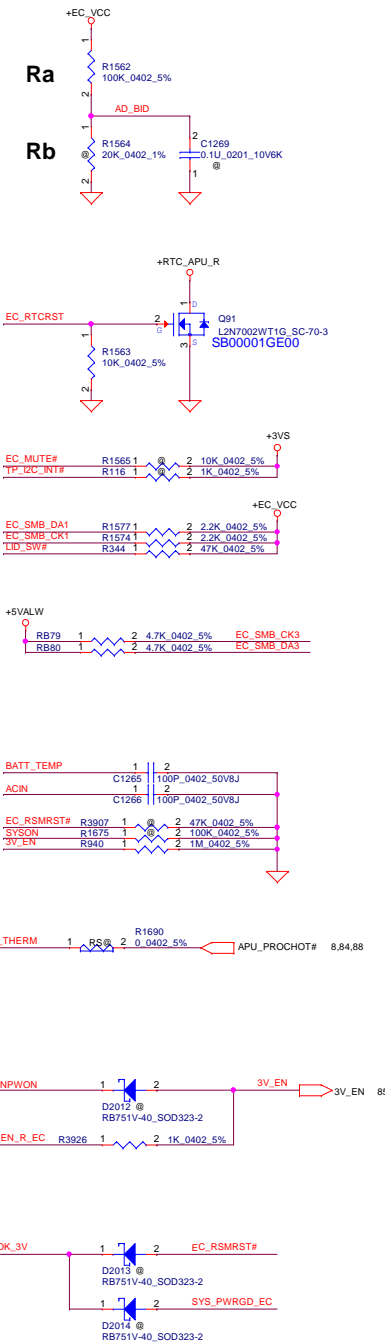
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				Date	Wednesday, May 15, 2019
				Sheet	57 of 99
				Rev	1A
				FH50P M/B LA-H901P	



Board ID / Rb		
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PVT	1	R1564 PVT@ 12K 0402 1% SD034120280
MP	2	R1564 MP@ 15K 0402 1% SD034150280



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				Custm	FH50P M/B LA-H901P	

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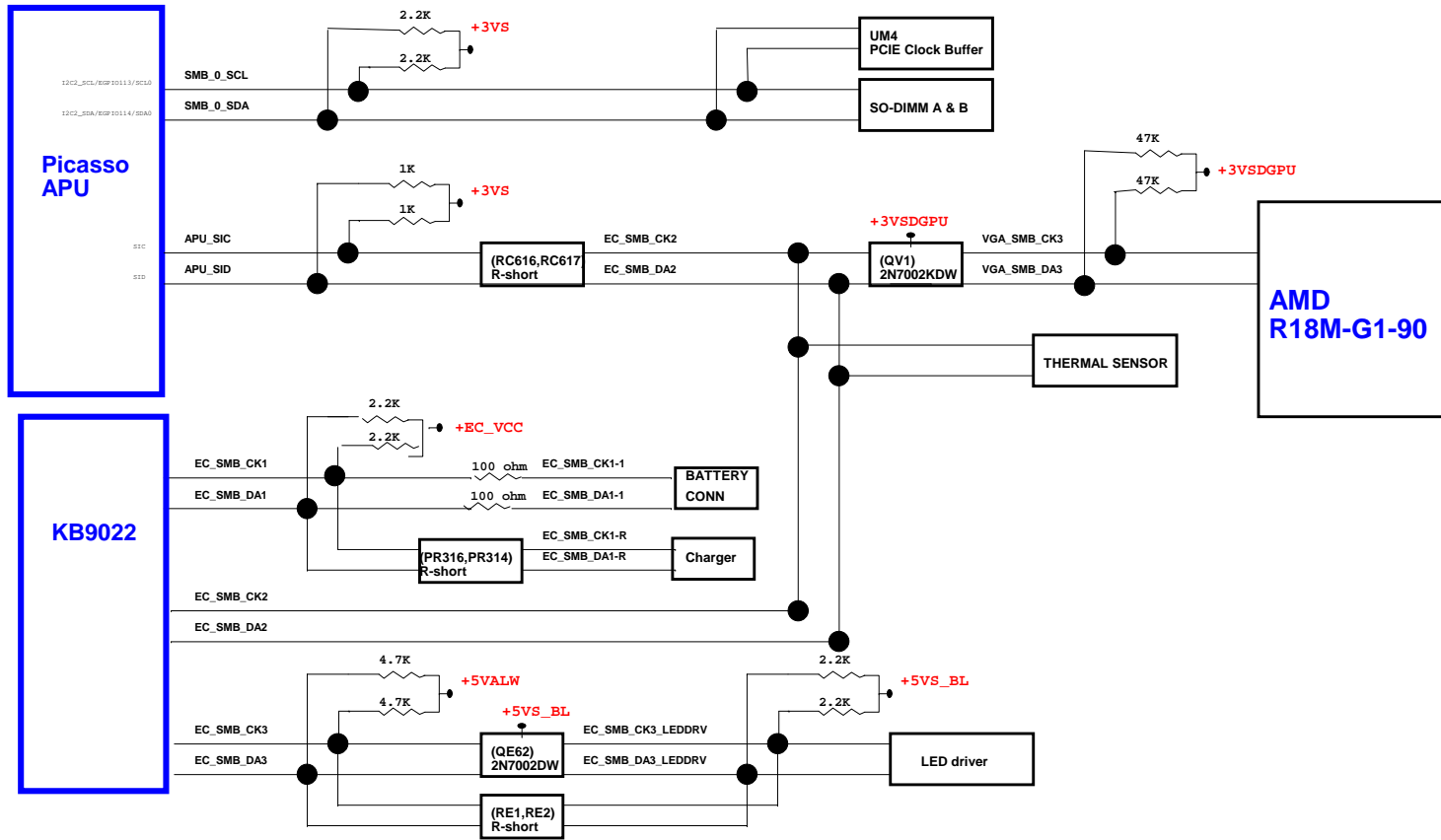
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				Date:	Wednesday, May 15, 2019
				Sheet	59 of 99
				Rev	1A
				FH50P M/B LA-H901P	

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				Date:	Wednesday, May 15, 2019
				Sheet	60 of 99
				Rev	1A
				FH50P M/B LA-H901P	

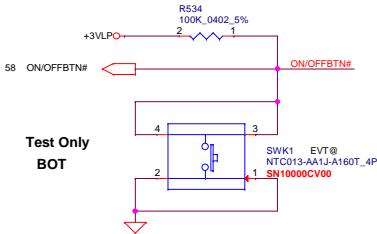


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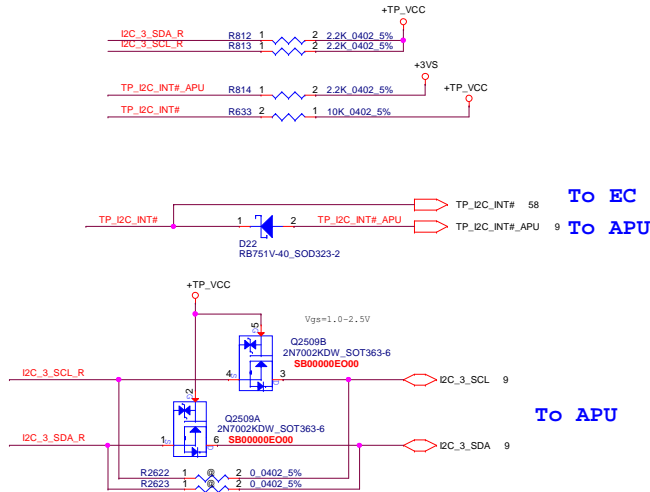
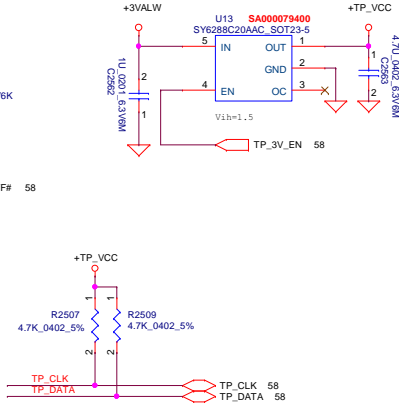
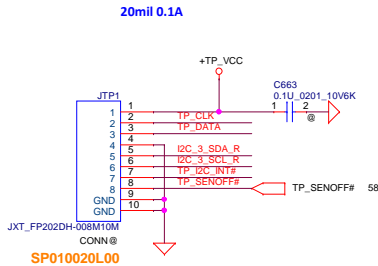
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				Date:	Wednesday, May 15, 2019
				Sheet	62 of 99
				Rev	1A
				FH50P M/B LA-H901P	

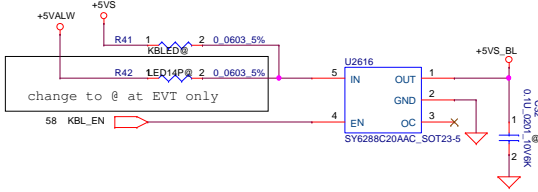
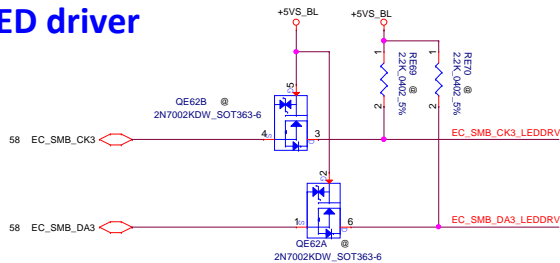
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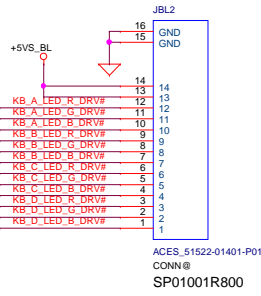
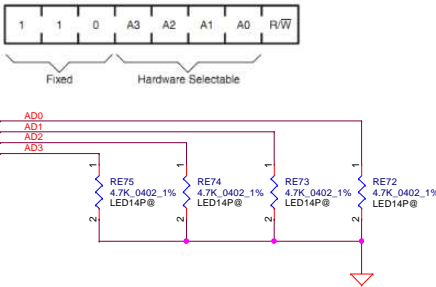
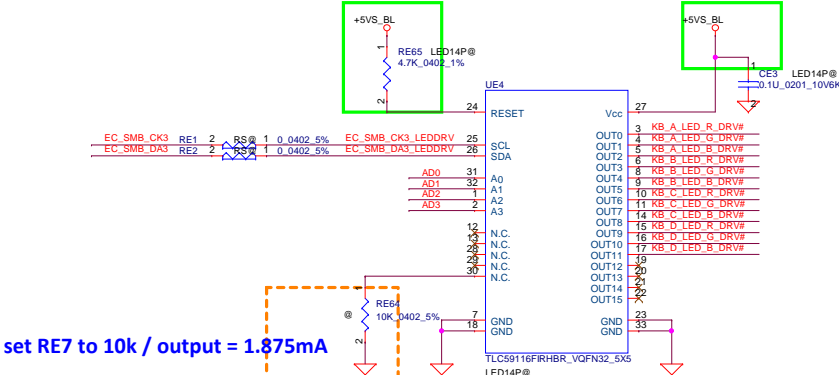
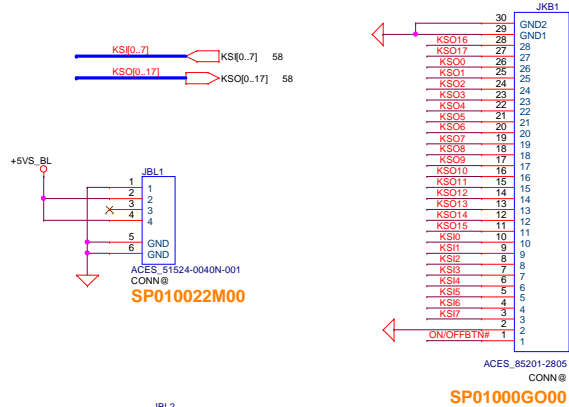
TP/B Conn.



LED driver



KB Conn. / Backlight



KB Conn.
KB BackLight

set RE7 to 10k / output = 1.875mA

Raptor: NC for 59116F

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				Customer	FH50P M/B LA-H901P
				Date	Wednesday, May 15, 2019
				Sheet	63 of 99

Reserve Page

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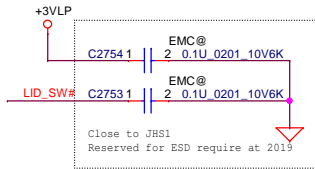
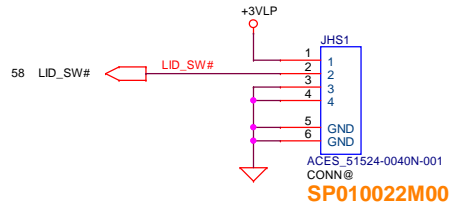
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				Date	Wednesday, May 15, 2019
				Sheet	64 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

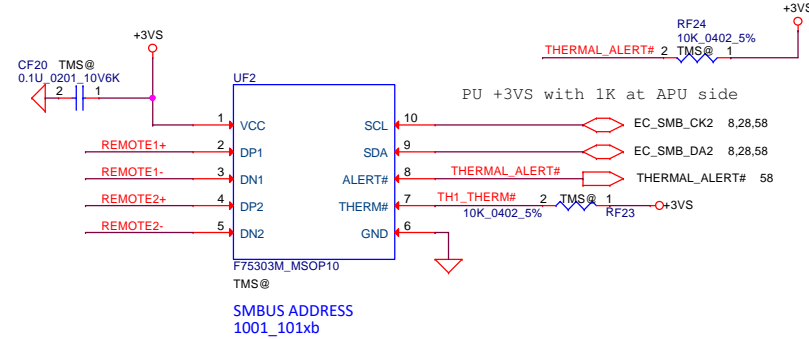
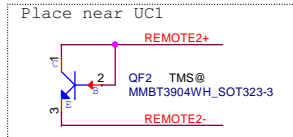
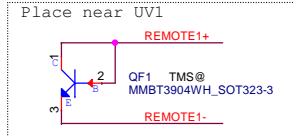
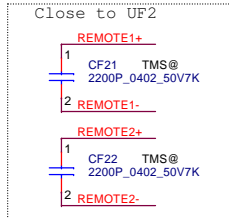
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				Date:	Wednesday, May 15, 2019
				Sheet	65 of 99
				Rev	1A
				FH50P M/B LA-H901P	

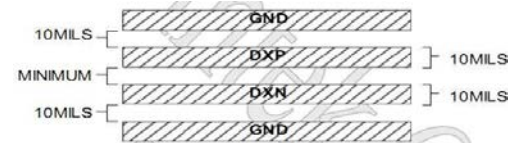
To Hall sensor/B



THERMAL SENSOR

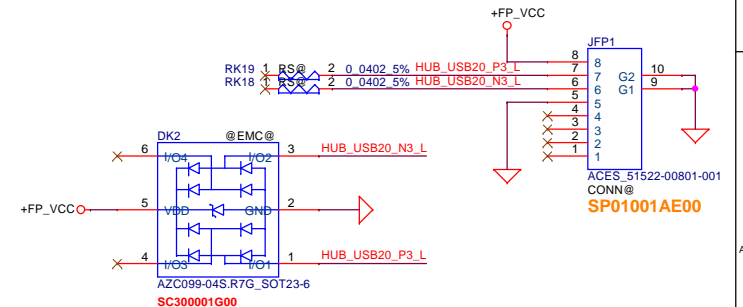
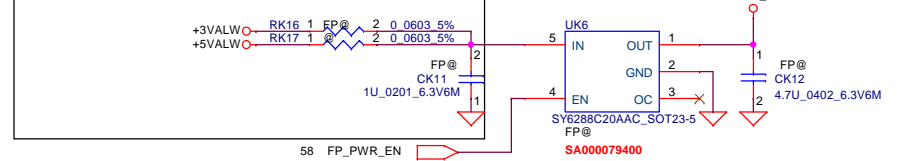


REMOTE1, 2 (+/-) :
Trace length: <8"



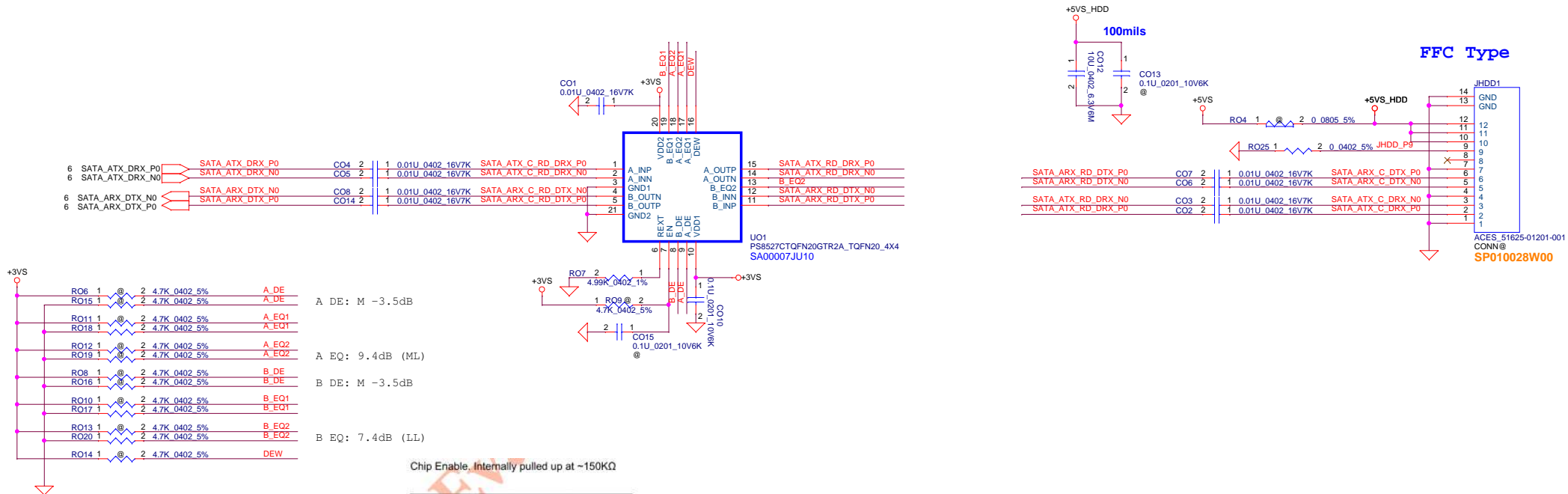
Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

SATA Re-Driver and cable HDD Conn.



Chip Enable, Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

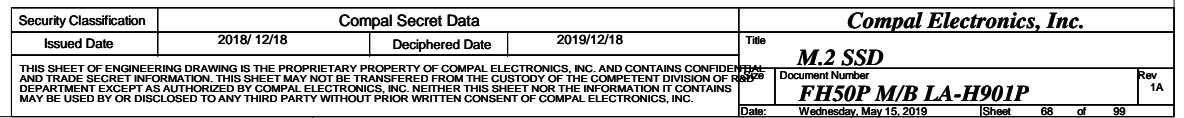
Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

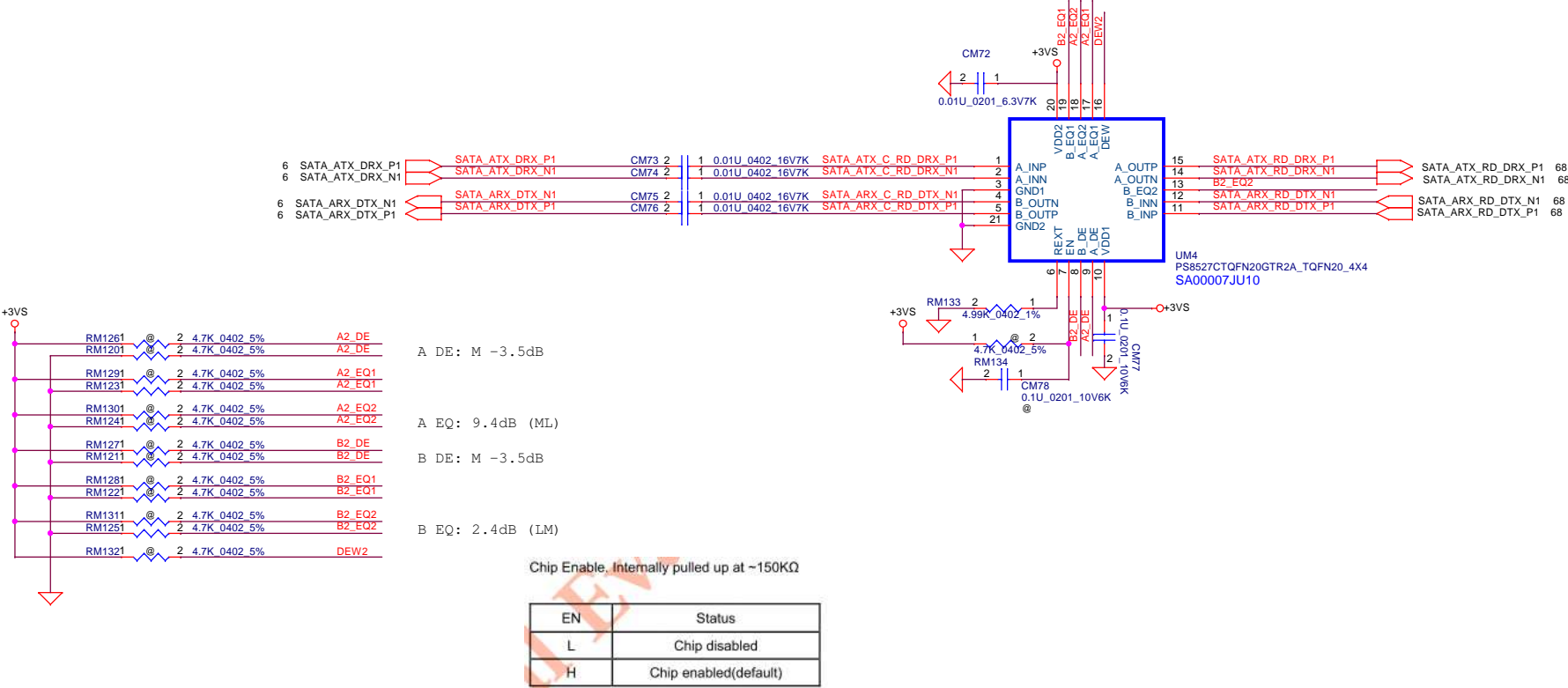
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Date	Wednesday, May 15, 2019	Sheet 67 of 99

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SATA Re-Driver for M.2 Connector



Programmable output de-emphasis level setting for channel A. Internally tied to VDD/2(M status).		Programmable output de-emphasis level setting for channel B. Internally tied to VDD/2(M status).	
A_DE	De_Emphasis	B_DE	De_Emphasis
M	-3.5dB(Default)	M	-3.5dB(Default)
L	0dB	L	0dB
H	-6dB	H	-6dB

Equalizer control and program for channel A. Internally tied to VDD/2 (M status).			Equalizer control and program for channel B. Internally tied to VDD/2(M status).		
A_EQ2	A_EQ1	EQ for channel loss	B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB	L	M	2.4dB
L	L	7.4dB	L	L	7.4dB
L	H	14.4dB	L	H	14.4dB
M	M	12.2dB(default)	M	M	12.2dB(default)
M	L	9.4dB	M	L	9.4dB
M	H	13.3dB	M	H	13.3dB
H	M	6.2dB	H	M	6.2dB
H	L	11.2dB	H	L	11.2dB
H	H	5dB	H	H	5dB

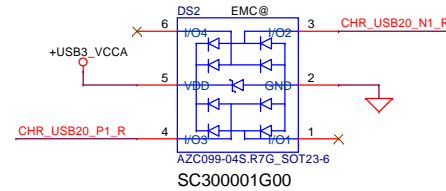
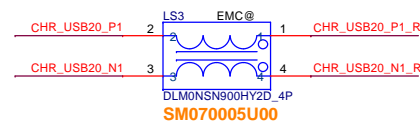
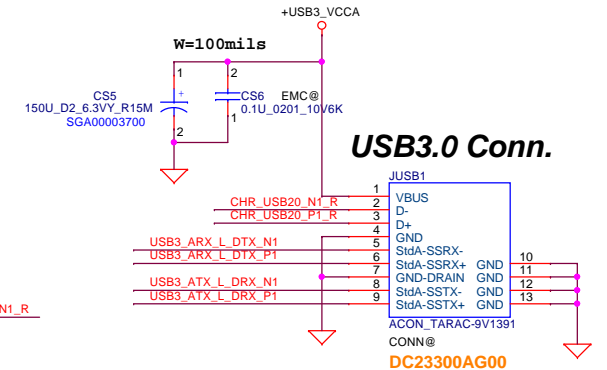
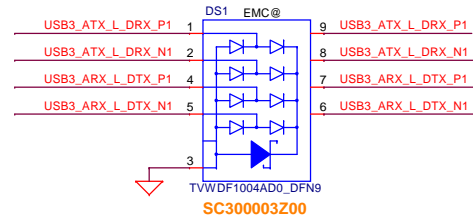
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				Date	Wednesday, May 15, 2019
				Sheet	69 of 99
				Rev	1A

Reserve Page

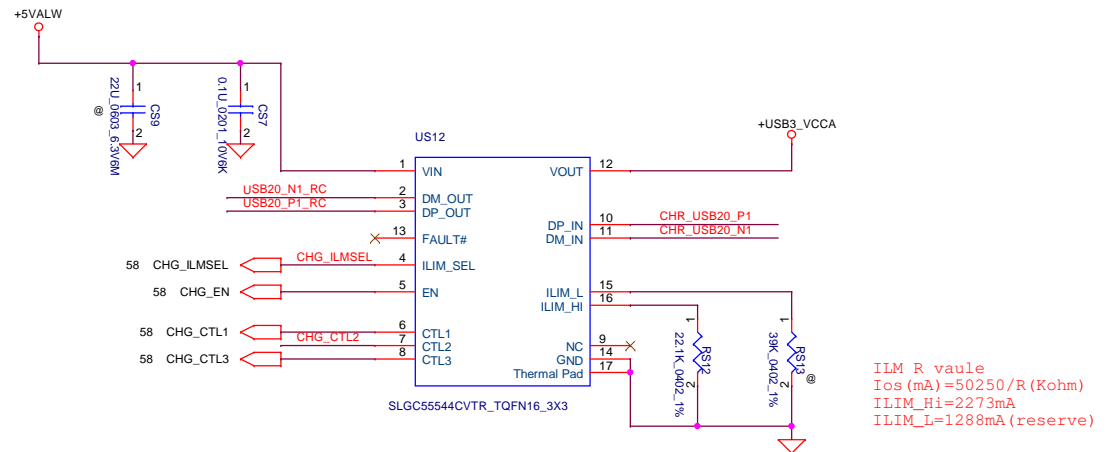
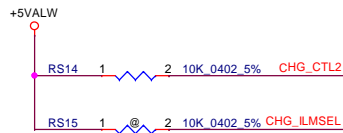
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				Date:	Wednesday, May 15, 2019
				Sheet	70 of 99
				Rev	1A
				FH50P M/B LA-H901P	

USB3.0



USB Host Charger



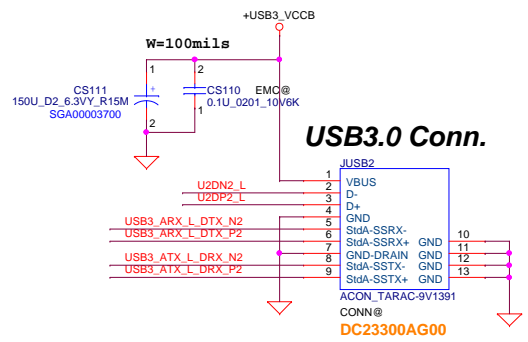
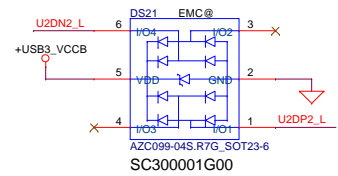
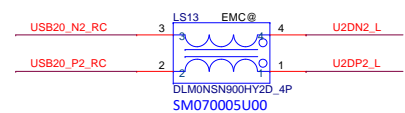
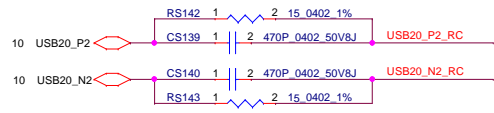
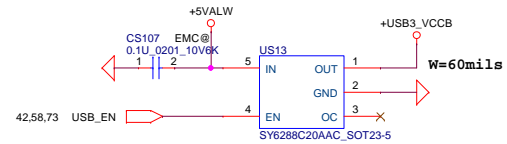
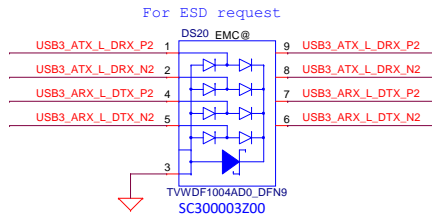
USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

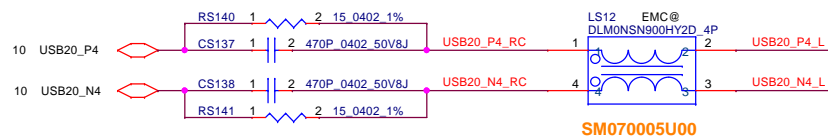
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						Size	Document Number			Rev	
						Custom	FH50P M/B LA-H901P			1A	
Date:		Wednesday, May 15, 2019		Sheet		71		of 99			

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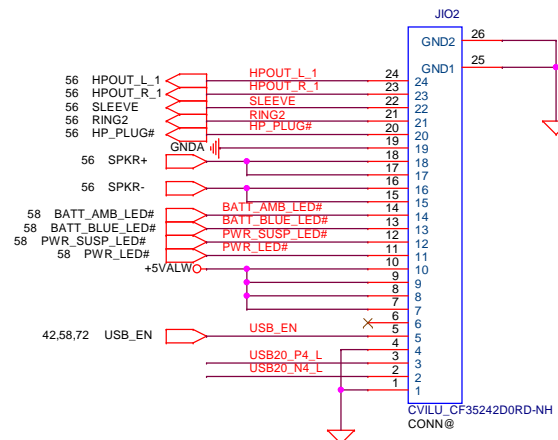
USB3.0



IO/B CONN



SM070005U00



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				Date	Wednesday, May 15, 2019
				Sheet	73 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

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				Date	Wednesday, May 15, 2019
				Sheet	74 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

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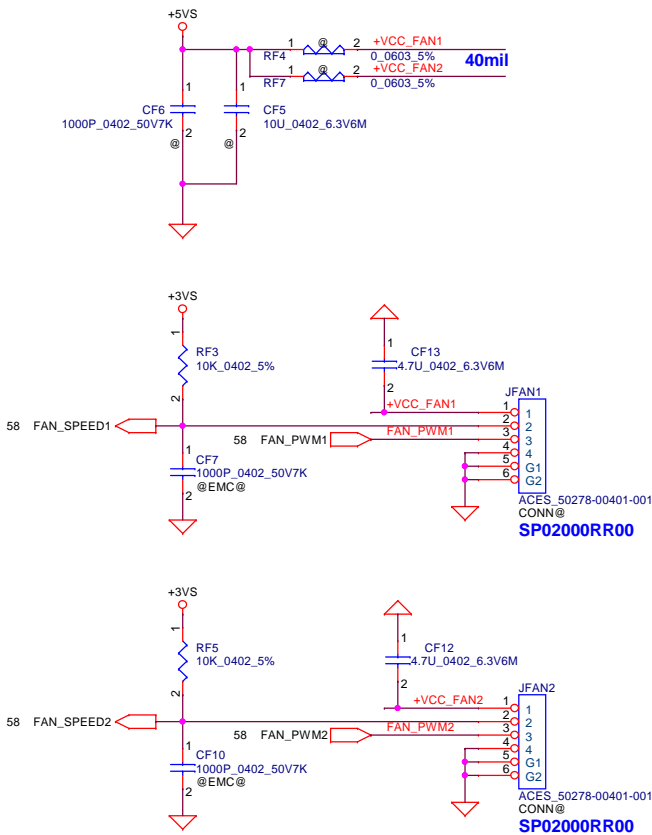
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				Date	Wednesday, May 15, 2019
				Sheet	75 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

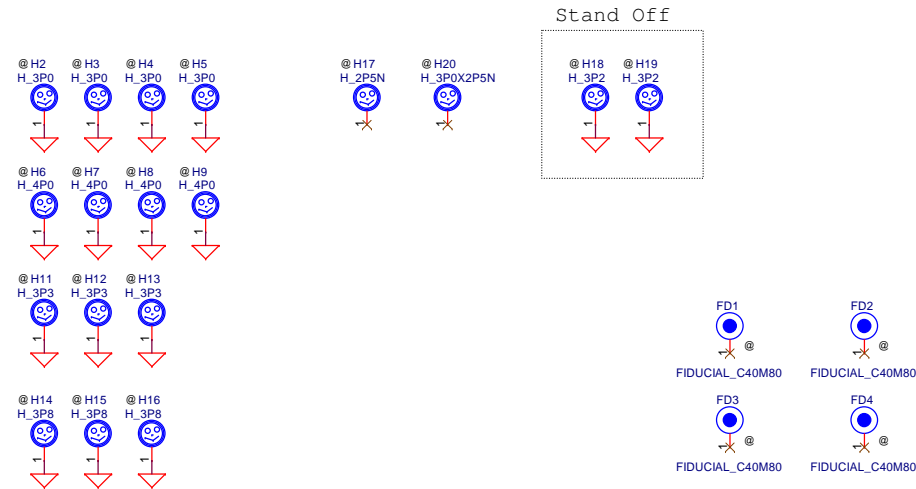
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				Date	Wednesday, May 15, 2019
				Sheet	76 of 99
				Rev	1A
				FH50P M/B LA-H901P	

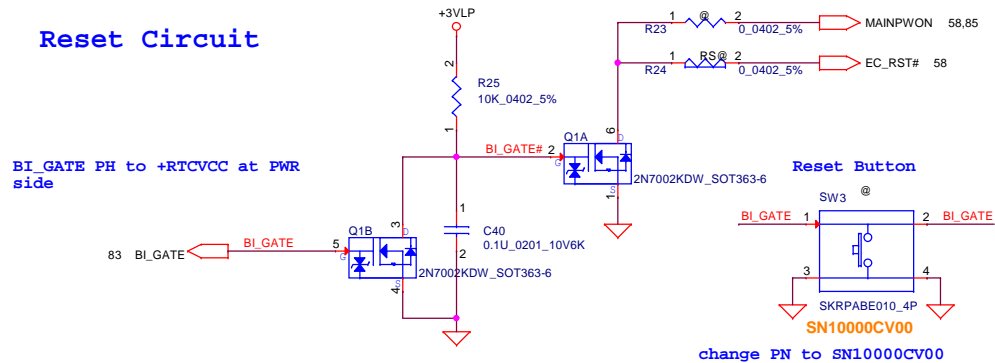
FAN Conn



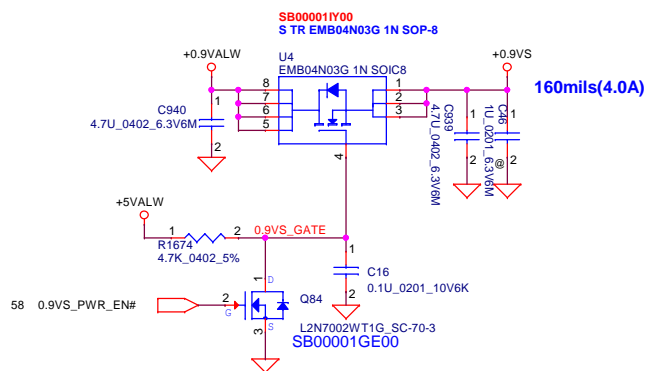
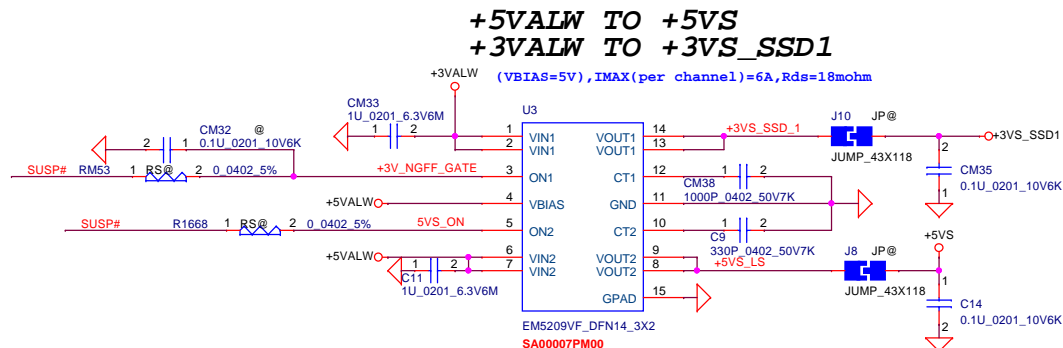
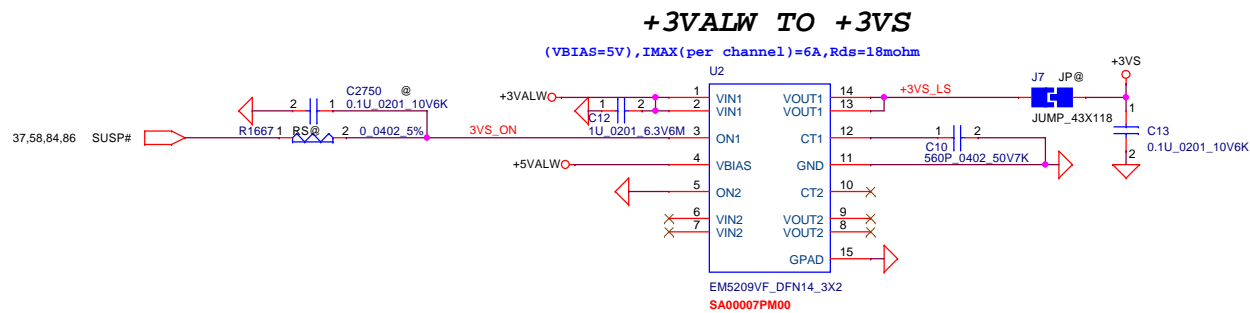
Screw Hole



Reset Circuit



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				Size Document Number
				Custom FH50P M/B LA-H901P
				Rev 1A
				Date: Wednesday, May 15, 2019
				Sheet 77 of 99



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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title	
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Size	Document Number	Rev		1A	
Custom	FH50P M/B LA-H901P				
Date:	Wednesday, May 15, 2019	Sheet	78	of	99

Reserve Page

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Issued Date	2018/ 12/18	Deciphered Date	2019/12/18	Title	Reserve Page
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				Date	Wednesday, May 15, 2019
				Sheet	79 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Reserve Page

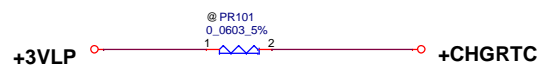
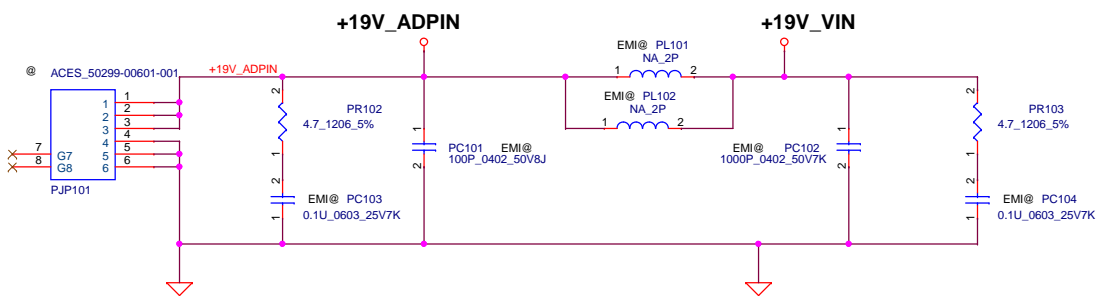
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				Date	Wednesday, May 15, 2019
				Sheet	80 of 99
				Rev	1A
				FH50P M/B LA-H901P	

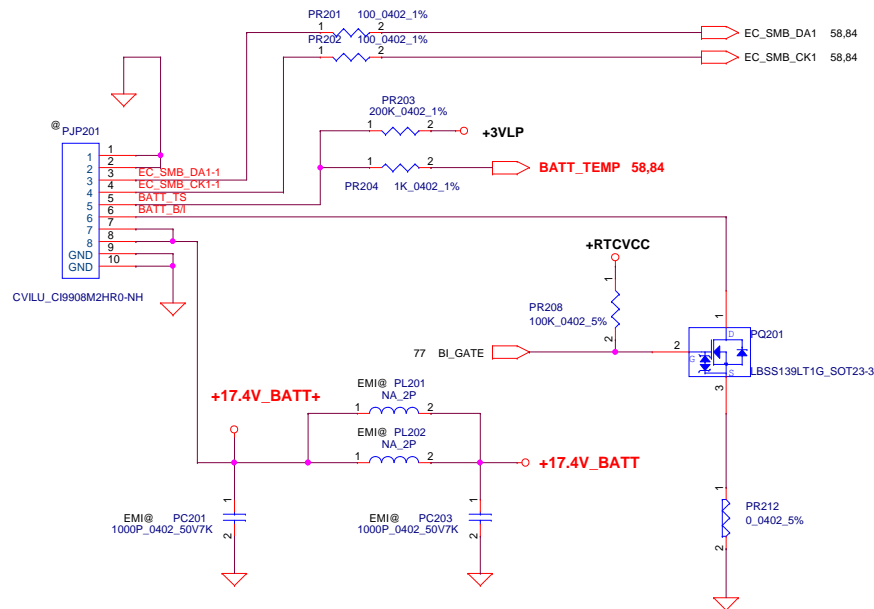
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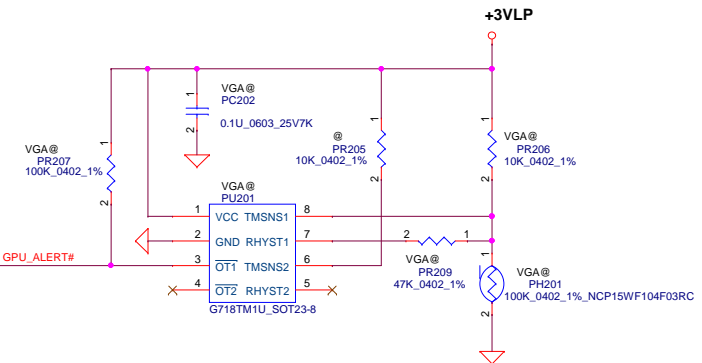
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				Date:	Wednesday, May 15, 2019
				Sheet	81 of 99
				Rev	1A
				FH50P M/B LA-H901P	



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Date: Wednesday, May 15, 2019		Sheet 82 of 99		



58 GPU_ALERT#

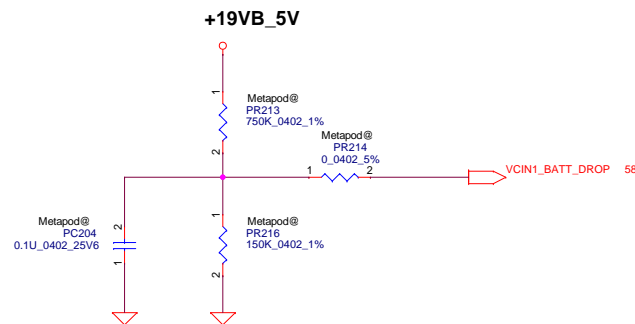


For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3092K	26.11K

For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

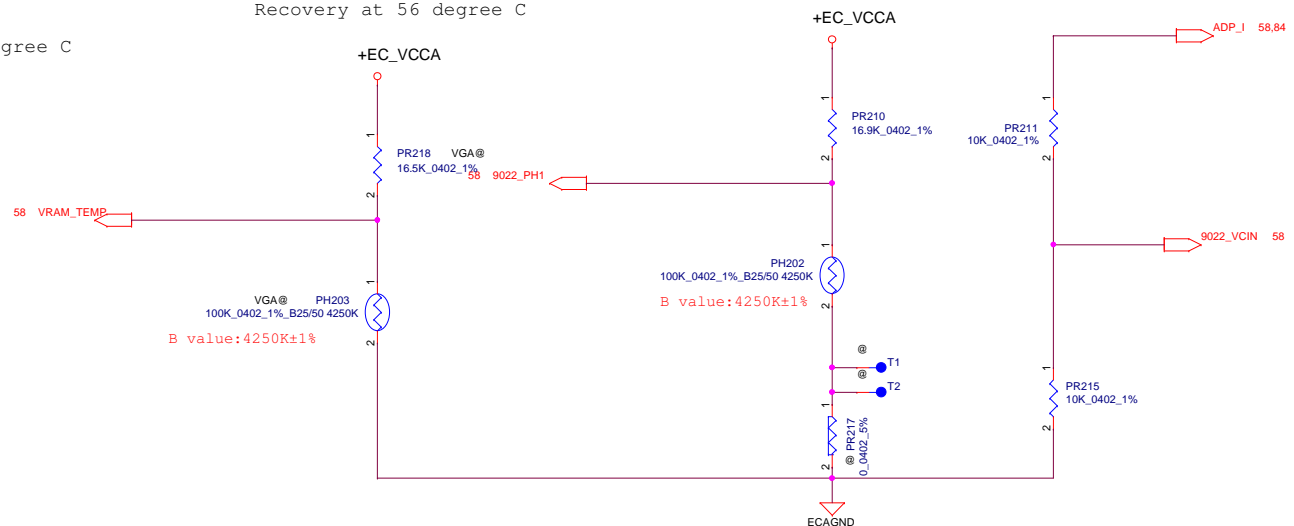
2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

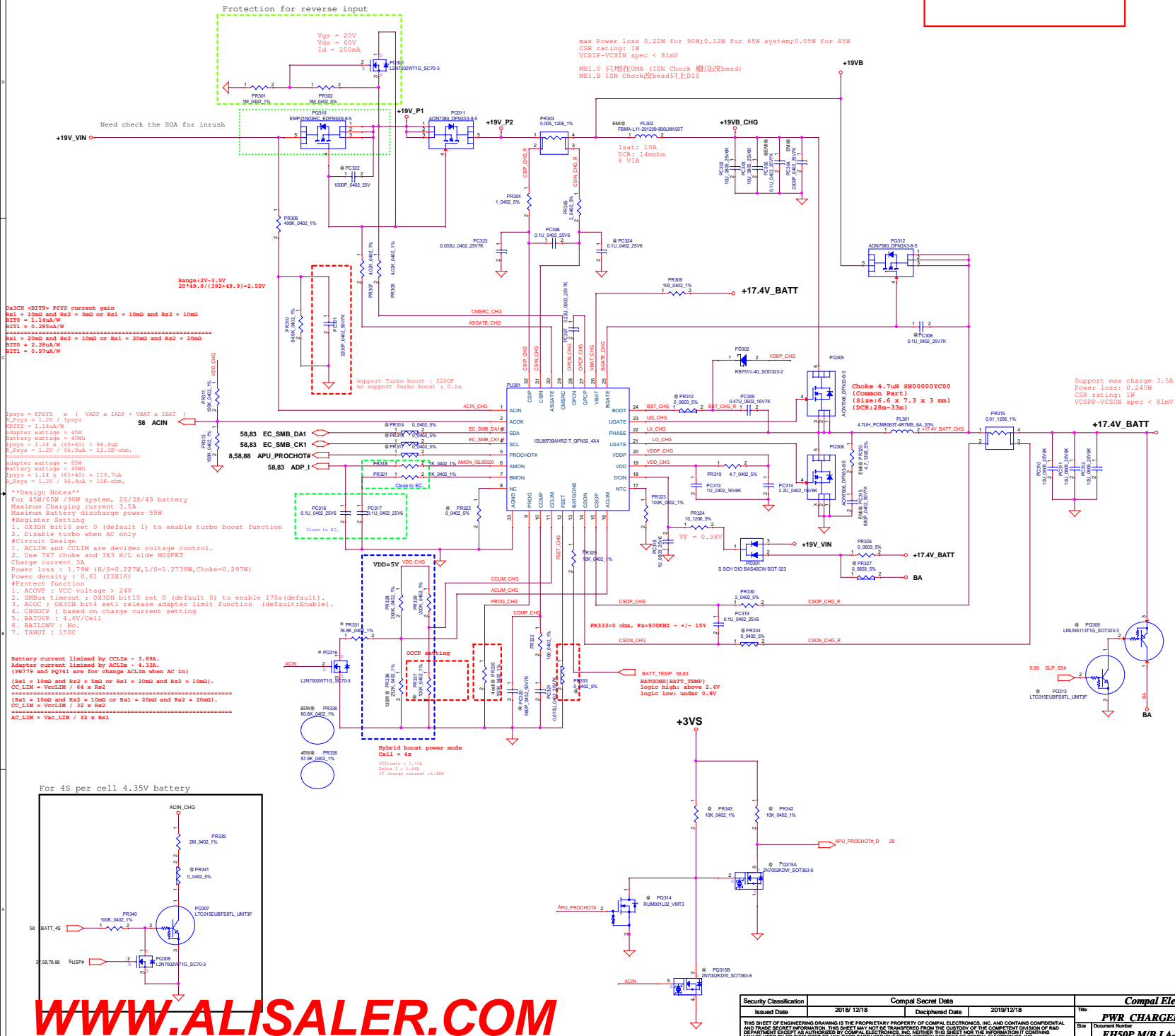
Reserve for 2-cell design



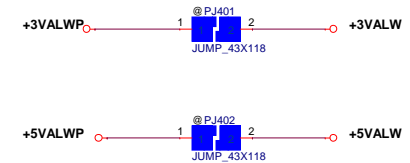
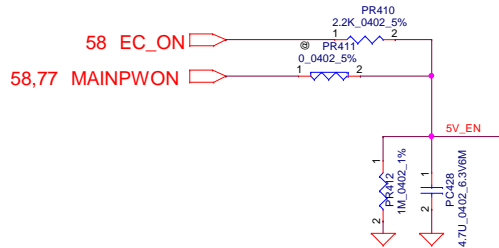
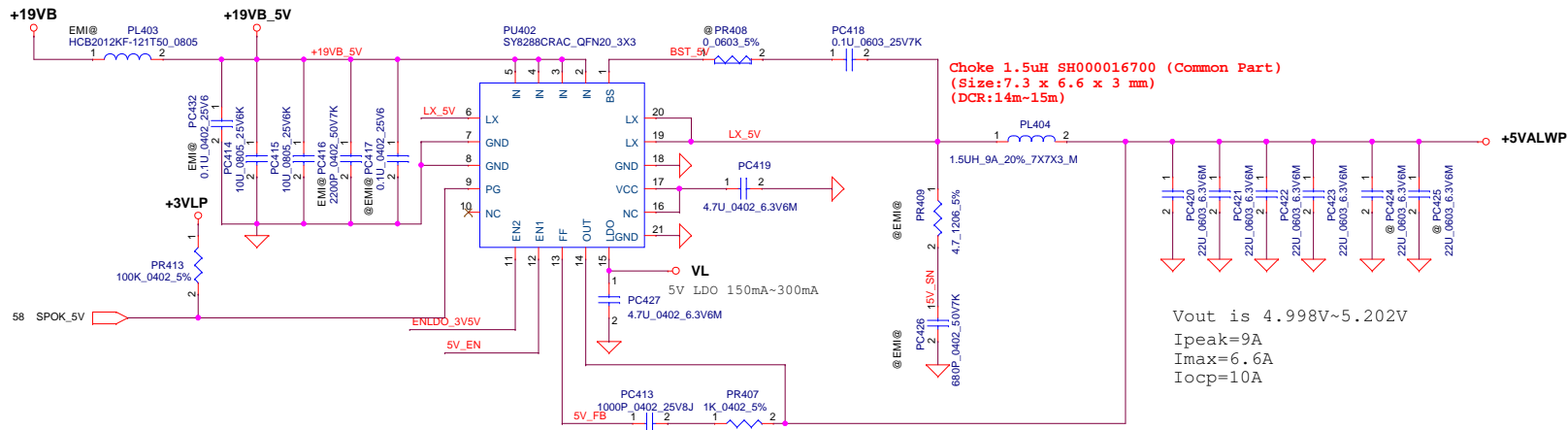
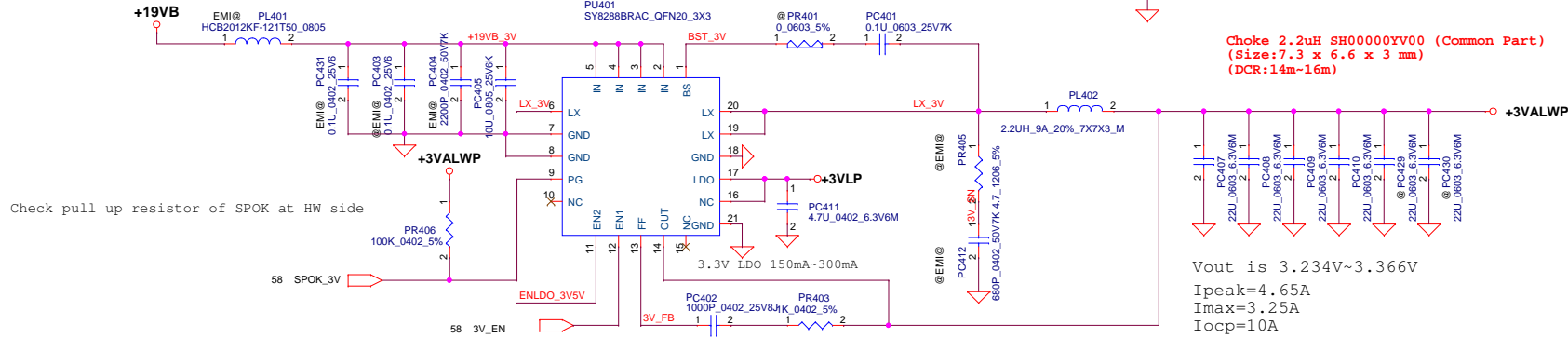
Recovery at 56 degree C

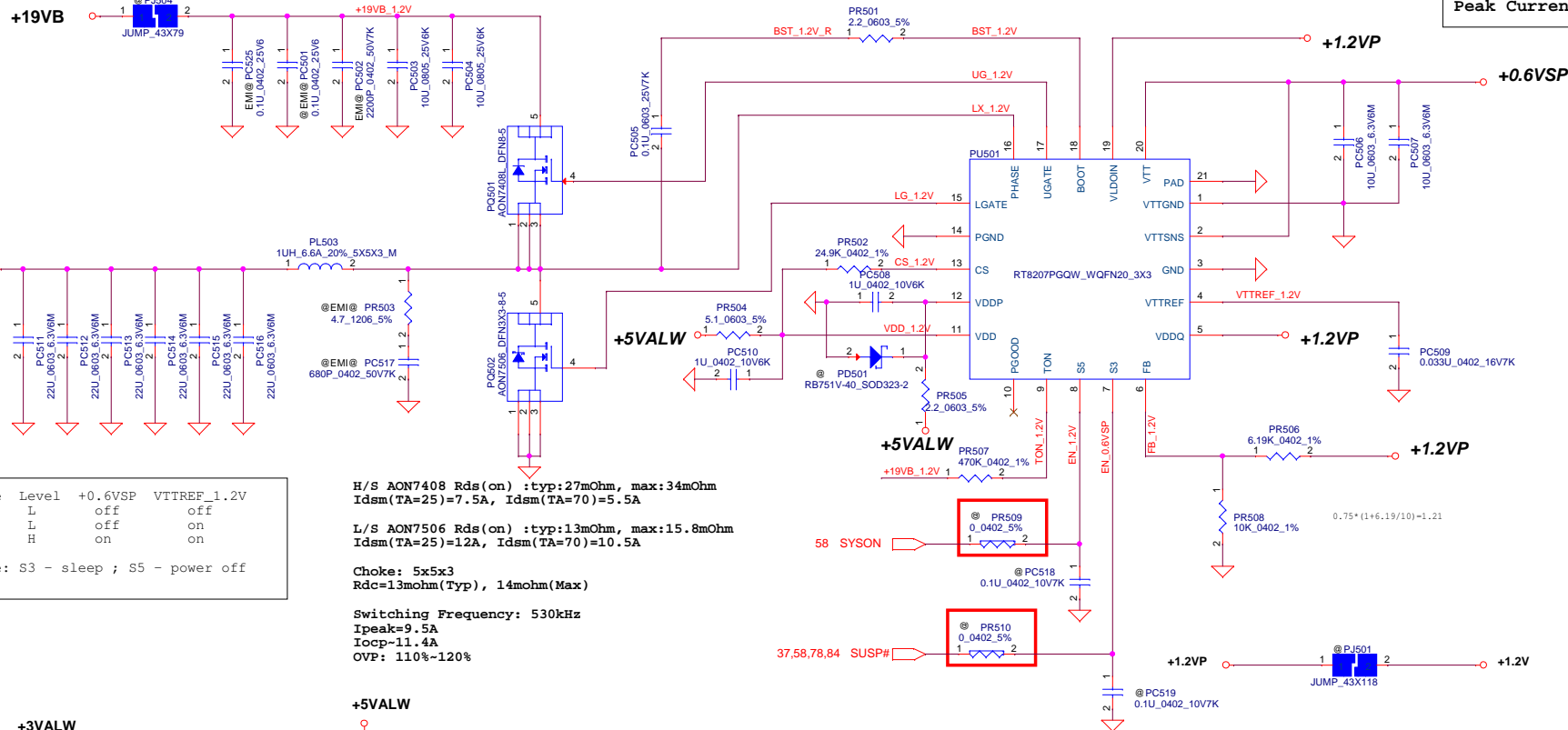
PH202 under CPU bottom side :
CPU thermal protection at 96 degree C (shutdown)
Recovery at 56 degree C





EN1 and EN2 don't floating



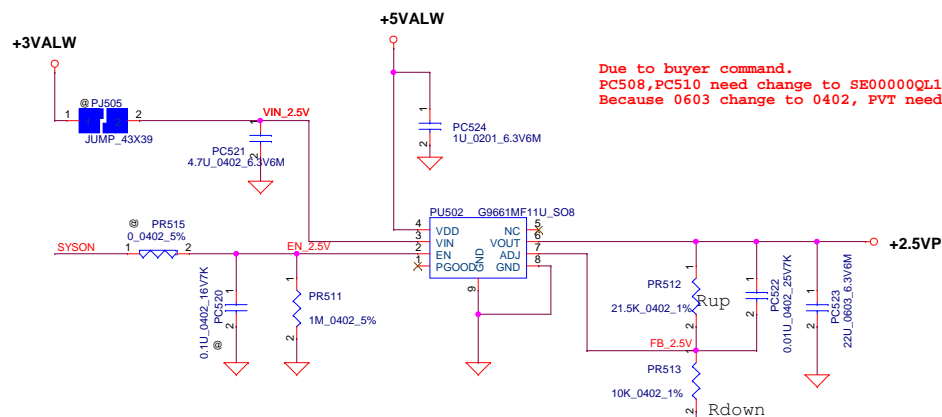


0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

Mode Level +0.6VSP VITREF_1.2V
S5 L off off
S3 L off on
S0 H on on
Note: S3 - sleep ; S5 - power off

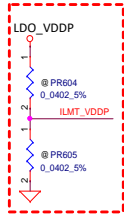
H/S AON7408 $R_{ds(on)}$: typ:27mOhm, max:34mOhm
 $I_{dsm}(TA=25)=7.5A$, $I_{dsm}(TA=70)=5.5A$
L/S AON7506 $R_{ds(on)}$: typ:13mOhm, max:15.8mOhm
 $I_{dsm}(TA=25)=12A$, $I_{dsm}(TA=70)=10.5A$
Choke: 5x5x3
 $R_{dc}=13mohm(Typ)$, 14mohm(Max)
Switching Frequency: 530kHz
 $I_{peak}=9.5A$
 $I_{ocp}=11.4A$
OVP: 110%-120%

Due to buyer command.
PC508, PC510 need change to SE00000QL10.
Because 0603 change to 0402, PVT need change footprint.

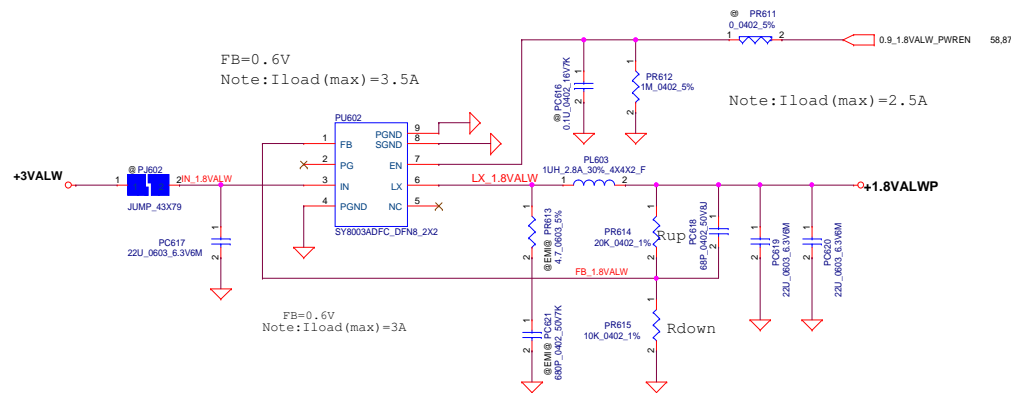
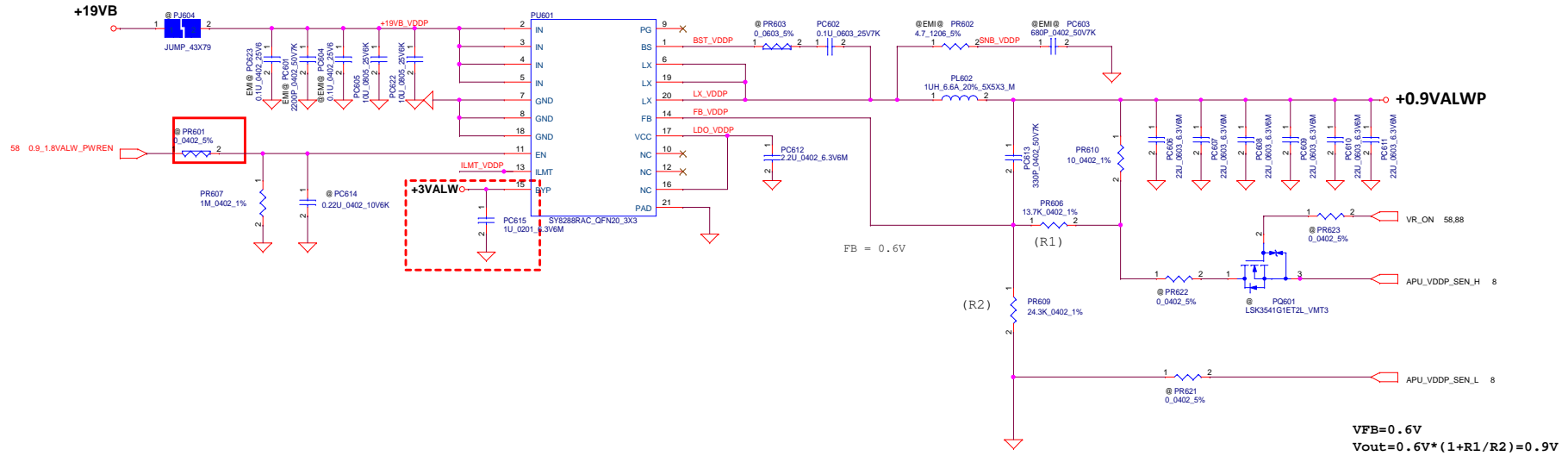
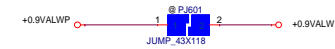


$$V_{out}=0.8V* (1+(21.5/10)) = 2.52V \quad 0.8\%$$

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				Date	Wednesday, May 15, 2019
				Sheet	86 of 99



EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

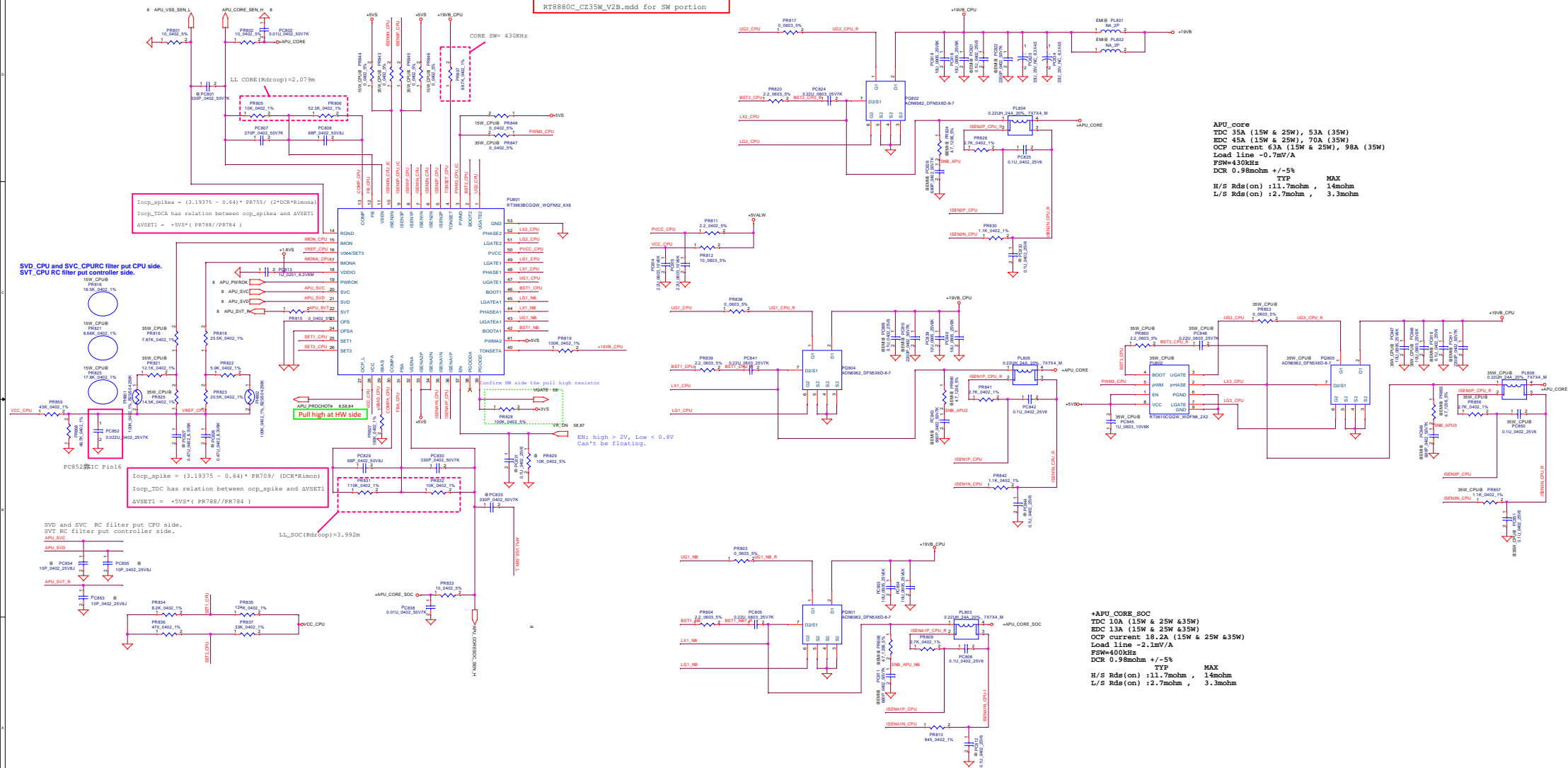


Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Module model information

RT8880C_CZ35W_V2A.mdd for IC portion

RT8880C_CZ35W_V2B.mdd for SW portion



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			S/N	
			FHSOP ML LA-H90IP	
			Date	March 15/2018
			Printed	58 of 29

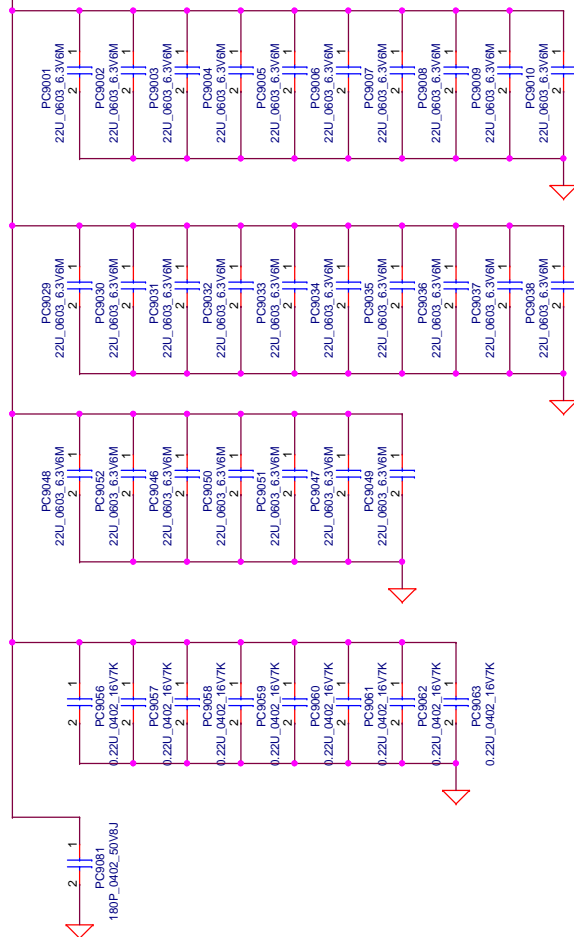
Reserve Page

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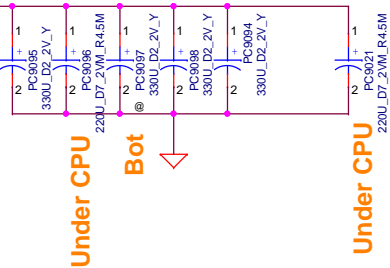
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				Date	Wednesday, May 15, 2019
				Sheet	89 of 99
				Rev	1A
				FH50P M/B LA-H901P	

+APU_CORE

+APU_CORE



+APU_CORE



Under CPU

Bot

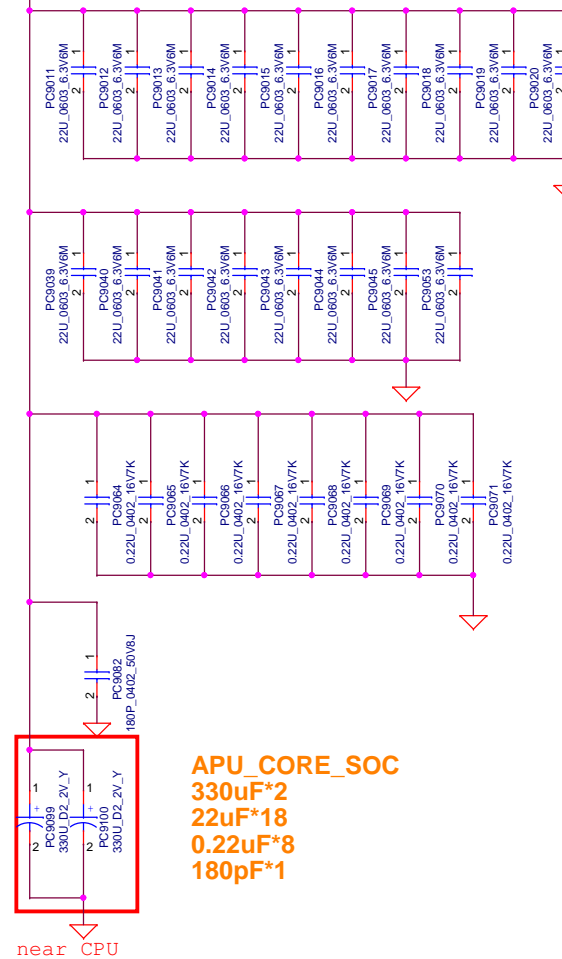
Under CPU

330u is common part SGA00009S00

APU_CORE
330uF*5
22uF*27
0.22uF*8
180pF*1

+APU_CORE_SOC

+APU_CORE_SOC



near CPU

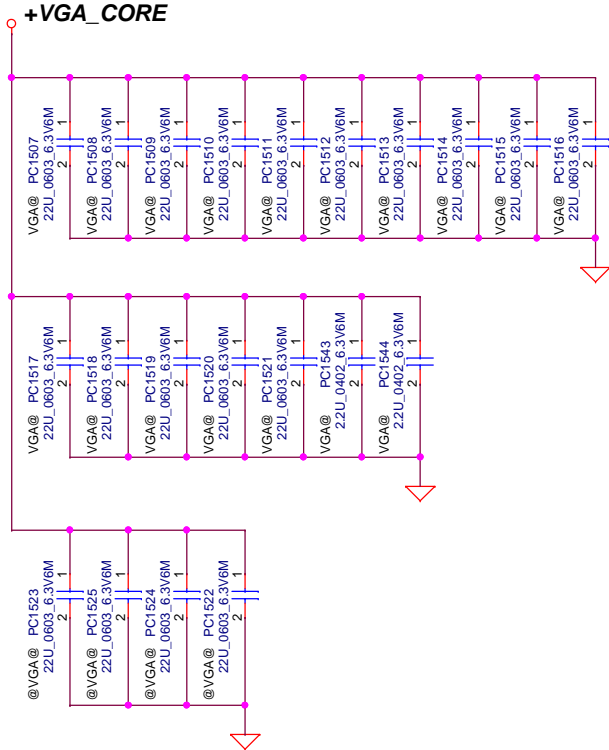
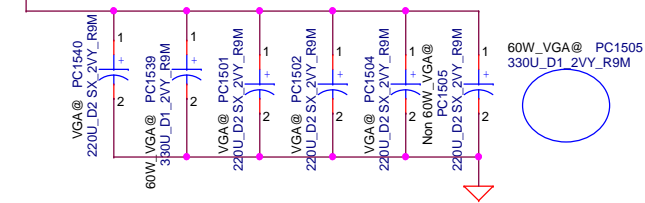
330u is common part SGA00009S00

APU_CORE_SOC
330uF*2
22uF*18
0.22uF*8
180pF*1

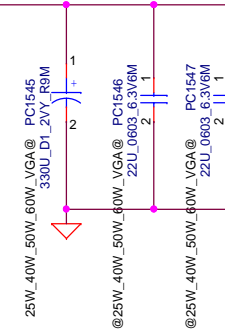
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				Date:	Wednesday, May 15, 2019
				Sheet	91 of 99
				Rev	1A
				FH50P M/B LA-H901P	

+VGA_CORE

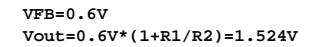


+VDDCI



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				Document Number	1A
				FH50P M/B LA-H901P	
				Date: Wednesday, May 15, 2019	Sheet 93 of 99

Module model information
SY8208D_V1.mdd



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				Date	Wednesday, May 15, 2019
				Sheet	95 of 99
				Rev	1A
				FH50P M/B LA-H901P	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	POWER Module design Change	0.1		PQ310: EMB04N03H_SB00001C500 -> _EMP21N03HC_SB00001LC00 PC313: 1U_0402_10V6K_SE00000QL10 -> _1U_16V_K_X5R_0402_SE00000OU00 PC314: 1U_0402_10V6K_SE00000QL10 -> _2.2U_16V_K_X5R_0402_SE000013780	2019/03/22	A
02	Design Update	CPU_CORE transient and load line test	0.1		PC830: 270P_0402_50V7K_SE074271K80 -> _330P_0402_50V7K_SE074331K80 PR831: 97.6K_0402_1%_SD034976280 -> _110K_0402_1%_SD034110380 Pr806: 34.8K_0402_1%_SD034348280 -> _52.3K_0402_1%_SD034523280 PC9097: 330U_D2_2V_Y_SGA00009S00 -> _Unpop	2019/03/22	A
04	Design Update	reduce part count	0.1		PR212: 0_0402_5%_SD028000080 -> _R-SHORT PR333: 0_0402_5%_SD028000080 -> _R-SHORT PR314: 0_0402_5%_SD028000080 -> _R-SHORT PR316: 0_0402_5%_SD028000080 -> _R-SHORT PR317: 0_0402_5%_SD028000080 -> _R-SHORT	2019/03/22	A
05	Design Update	reduce part count	0.1		Del colay PJ1401 PJ1402 PJ1403	2019/03/22	A
06	Design Update	prochot 調整	0.3		PR304: change R-SHORT SD028000080 0_0402_5% -> SD028100B80 1_0402_5% PC323: add NA -> SE000006O00 0.033U_0402_25V7K PC324: add NA -> @ SE00000G880 0.1U_0402_25V6 PR211: change SD034200280 20K_0402_1% -> SD034100280 10K_0402_1% PR310: change SD034665280 66.5K_0402_1% -> SD034649280 64.9K_0402_1%	2019/04/26	C
07	Design Update	EMI 需求	0.3		PR1437,PR1419,PR1402,PR1463: unpop ->SD001470B804.7_1206_5% PC1442,PC1426,PC1408,PC1467: unpop ->SE074681K80680P_0402_50V7K	2019/05/07	C
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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01
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Size	Customer	Document Number	Date	Scale	Rev
1/8"	FH50P M/B LA-H901P	1A	Wednesday, May 16, 2018	1/8"	1A

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1			03/28	Change 0 ohm to R-Short	R1667, R1669, RM53, RX21 change to R-Short	PVT	1.0
2	10	CPU	03/28	ESPI_ALERT_L PU to VDD	Add RC6168 and PU to +3VS	PVT	1.0
3	29	CLK GEN	03/28	27MHz Crystal Correlation Update	CV450,CV451 change to 15P_0402	PVT	1.0
4	38	Panel	03/28	144Hz Panel OD Function Circuit Update	Rename PANEL_OD_EN to PANEL_OD# UN-POP RX11	PVT	1.0
5	40	HDMI	03/28	Mask un-use co-lay component	L2512, L2513, L2514, L2515 footprint change to INPAQ_HCM1012GH900BP_4P-NPM	PVT	1.0
6	43	TypeC	03/28	TypeC current limiting adjust	RS109 change to 4.3K_0402 RS110 change to 8.2K_0402	PVT	1.0
7	51	LAN	03/28	Correct YL1 Value	YL1 update vale to XRCGB25M000F2P34R0	PVT	1.0
				Change DL1 Material	DL1 change from SCA00002M00 to SCA00001A00		
8	68	M.2 SSD1	03/28	Reserved Circuit for PCIE compatibility	Change RM28 to 0_0402 Add RM135, UM5	PVT	1.0
		M.2 SSD2	03/28	BOM change M.2 SSD2 power need a break point	Pop RM21, un-pop RM20, CM58 Add RO26, JSSD2 power change to +3VS_SSD2		
9	75	HUB	03/28	BOM change	Change RS154, RS152 with HUB@	PVT	1.0
10	77	Others	03/28	Screw hole change	H11, H12, H13 change from H_3P8 to H_3P3	PVT	1.0
11	78	DC-DC	03/28	Material Change	U4 change to SB00001IY00	PVT	1.0
12	06	CPU	03/29	Add R5/ R7 CPU PN	Add SA0000CCR60/ SA0000C7680	PVT	1.0
13	06	CPU	04/01	Material Change	YC2 Change from SJ10000AF00 to SJ10000JP00	PVT	1.0
14	09	CPU	04/02	BOM change	Un-Pop RC693	PVT	1.0
15	10	CPU	04/02	BOM change	YC3 change to SJ10000PW00 CC686 change to 12P_0402 CC682 change to 10P_0402	PVT	1.0
16	28,38, 58,63		04/02	Material Change	DV1,DV2,DV4, DX2, D2012,D2013,D2014,D22 change to SCS00009P00	PVT	1.0
17	58	EC	04/26	Add Board ID for MP	Add R1564 15K_0402_1% for MP	MP	1A
18	75 52 38 66 58	HUB	04/30	Remove Hub and other component/net	Delete RS148 ~ RS158, CS145 ~ CS153, YS1, US15 Move RS146, RS147, CS143, CS144 to page52 and POP Delete net HUB_USB20_P2/HUB_USB20_N2 (JEDP1 pin 29,30) Delete net HUB_USB20_P3/HUB_USB20_N3 (RK19, RK18 pin 1) Delete net USB_HUB_RESET# (U44 pin 126)	MP	1A
19	52	M.2 SSD1	04/30	Reserved 10U_0603 on WLAN Power	Reserved CM79, CM80	MP	1A
20	52	M.2 SSD2	05/14	WLAN power path change	Un-Pop RM101 POP UM3, CM71	MP	1A
21	37	DC-DC	05/14	Adjust C21 for +1.8VS Sequence	Change C21 to 4700pF	MP	1A