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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

VELLFIRE

2020.06.05

[illegible]

DESIGN / DRAWER				XXX		DATE		21-OCT-2002		TITLE				MODEL,PROJECT,FUNCTION				
CHECK										MAIN BOARD								
APPROVAL										SIZE	A3	CODE	CS	DOC NUMBER	1310XXXX-0-0		REV	X01
FILE NAME																		
PCB P/N				60XXXXXXXXXX		PCB VER		XXX		SHEET 1 of 130								

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55.AUDIO LINE
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58.M.2 FOR SSD1
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60.TYPE-C CNTR
61.USB_CHARGER
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63.TPM
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66.SEQUENCING
67.SEQUENCING

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SMALL BOARD1&2

120.TUBRO_BOARD/HALL_SENSOR_BOARD

SMALL BOARD3

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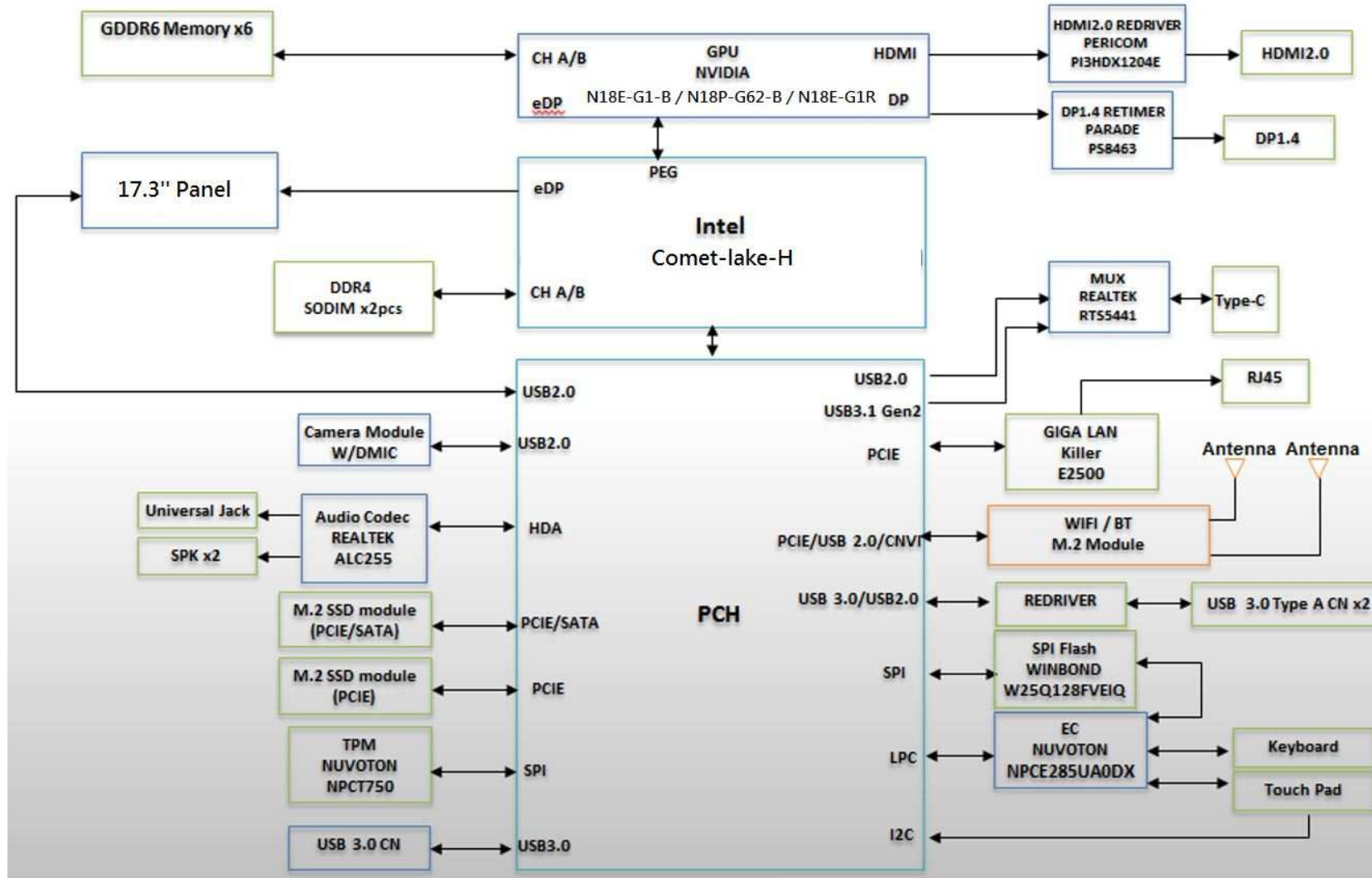
FOR 17 SMALL BOARD1&2

129.KB_BL
130.KB

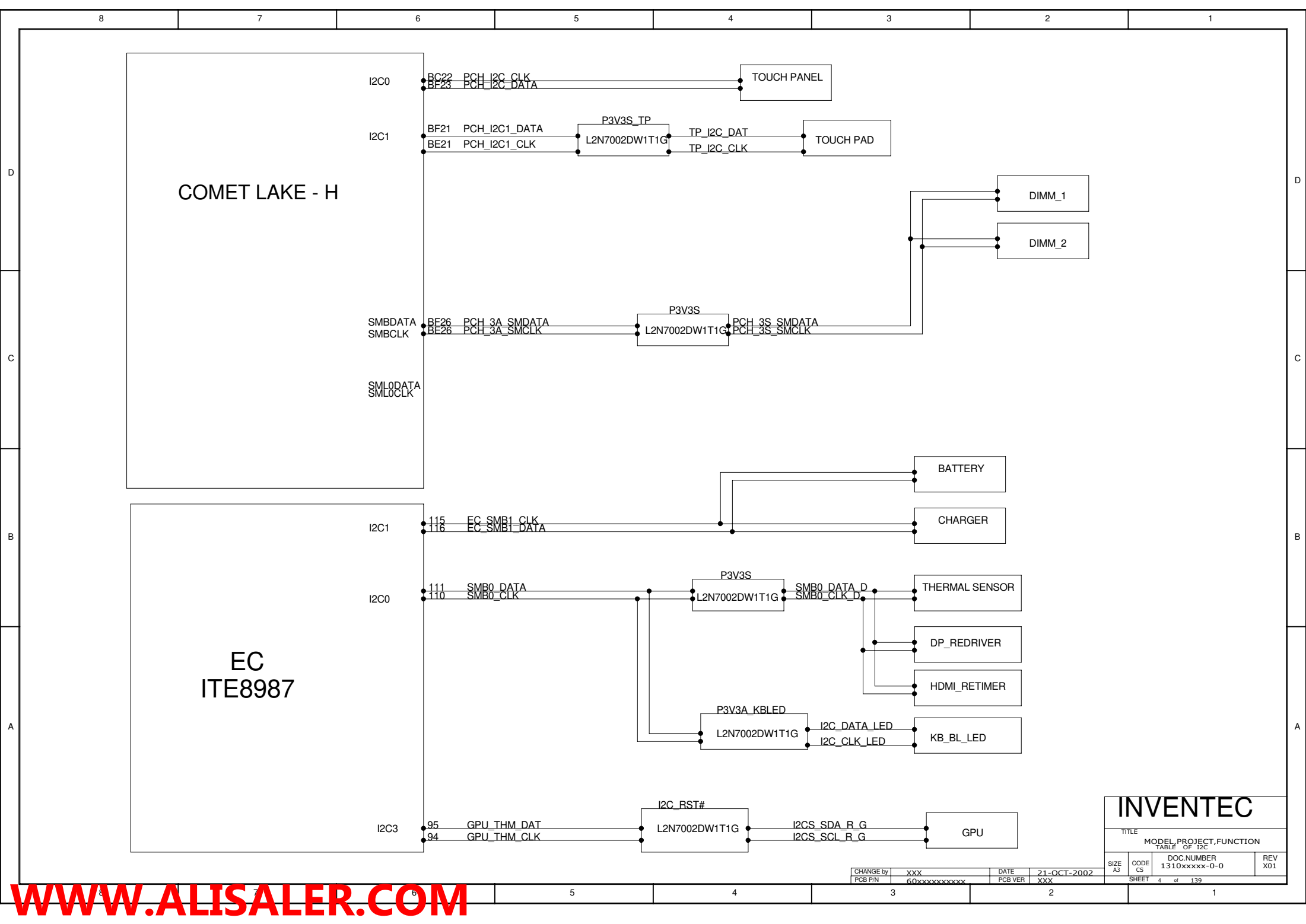
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INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
TABLE OF THE CONTENT			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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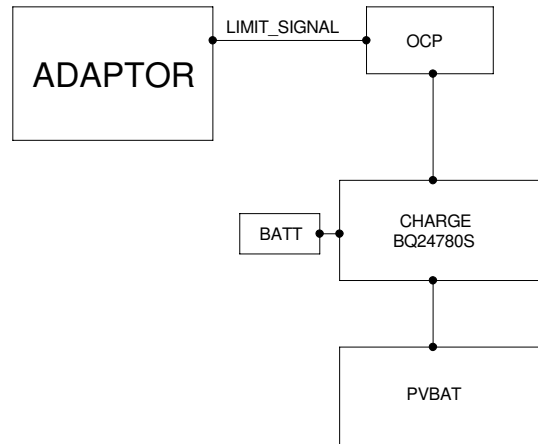
CHANGE by	XXX	DATE	21-OCT-2002
PCB PIN	60xxxxxxxxxxx	PCB VER	XXX



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
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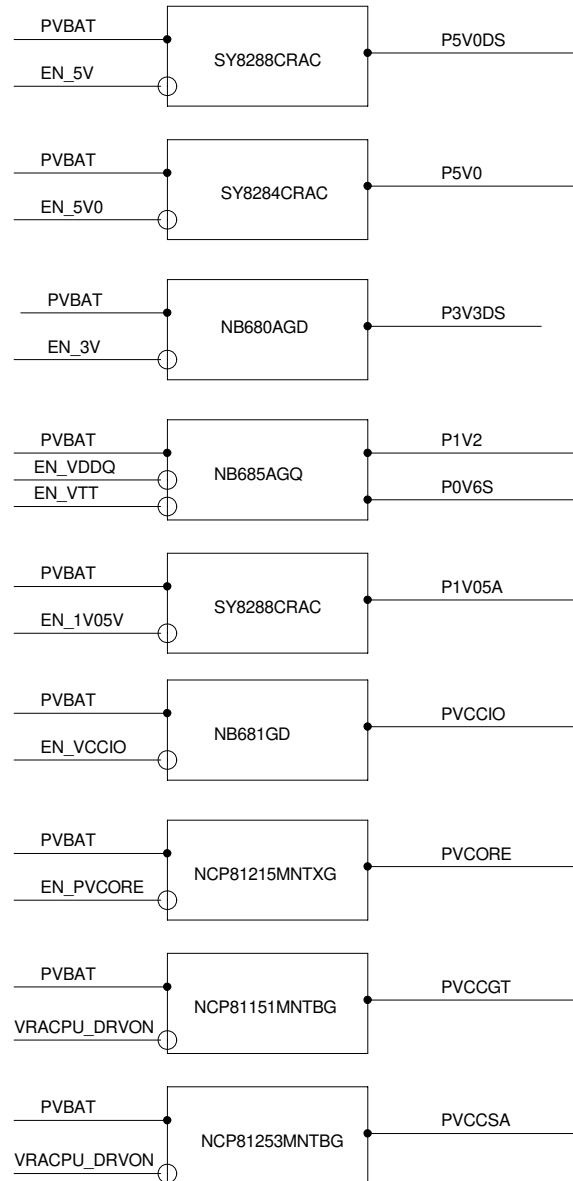


POWER BLOCK



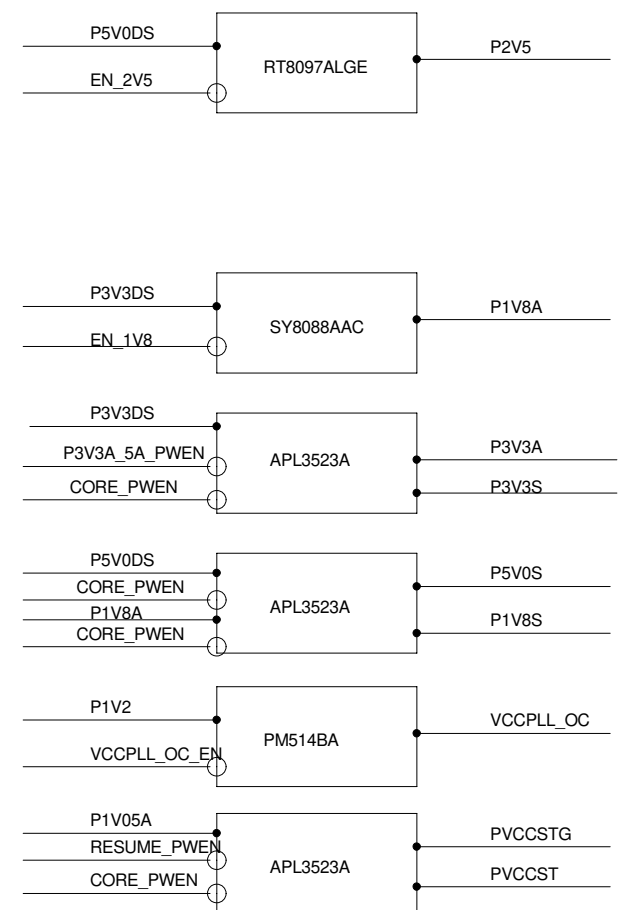
IN/EN

OUT



IN/EN

OUT



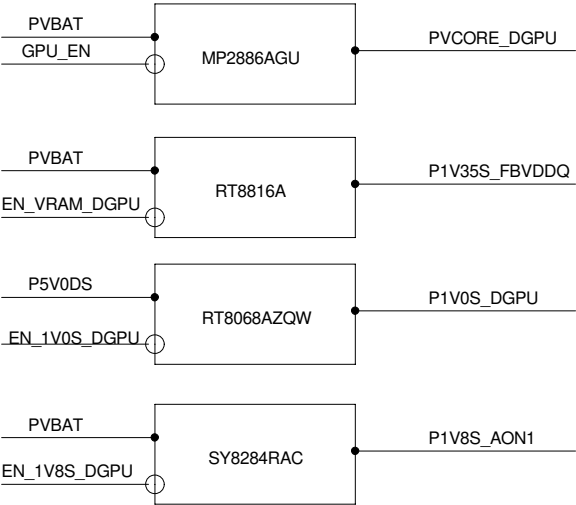
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TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

GPU POWER BLOCK

IN/EN OUT



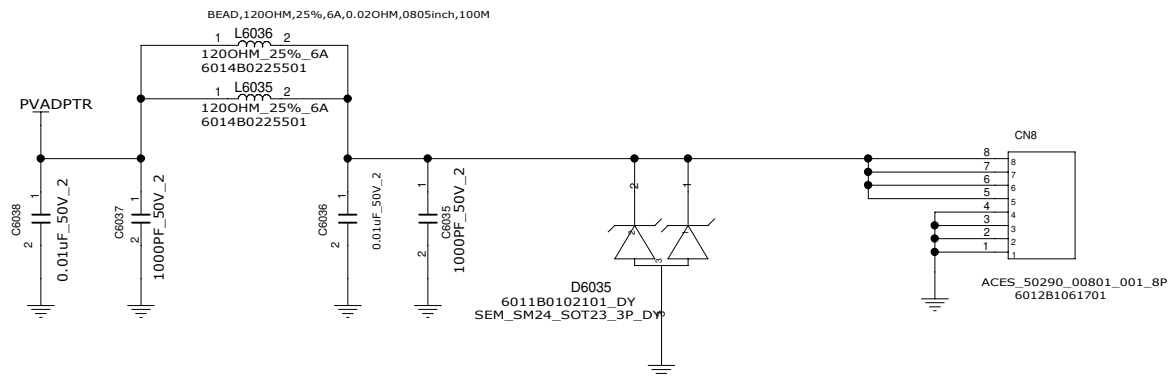
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TITLE
MODEL PROJECT, FUNCTION
TABLE OF 12C

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

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INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

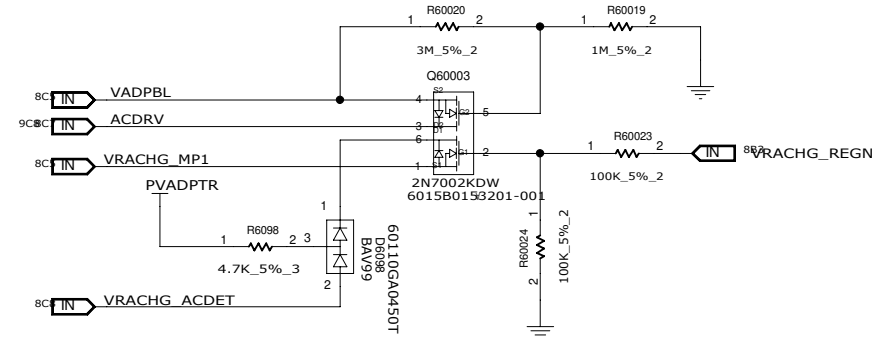
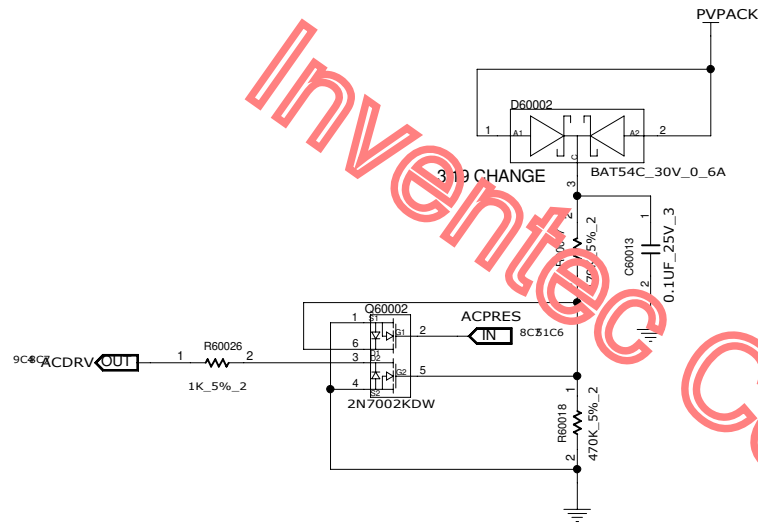
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PCB P/N 60xxxxxxxxxxx PCB VER XXX

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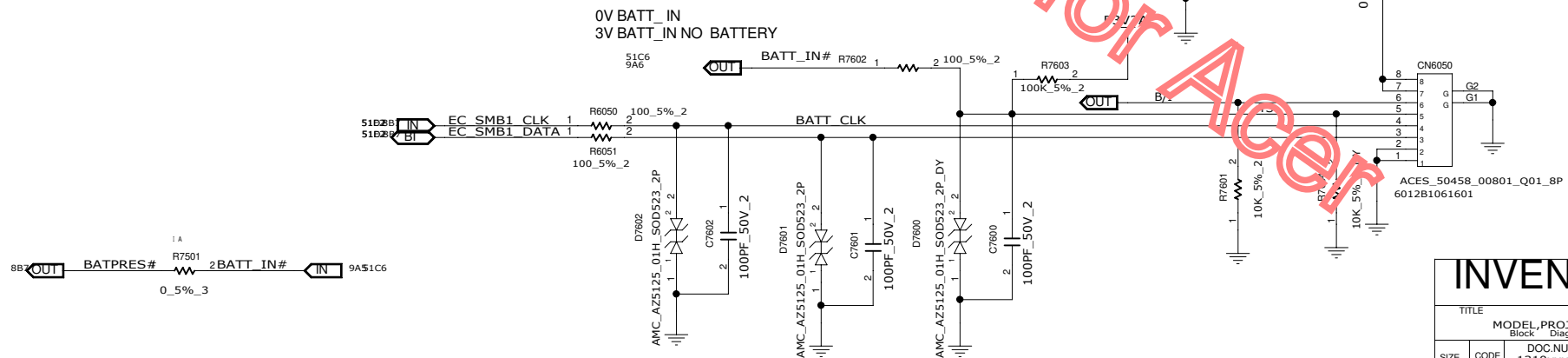
FOR CHARGER

SCP

ARP



BATT



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE CODE
A3 CS 1310xxxx-0-0 REV X01

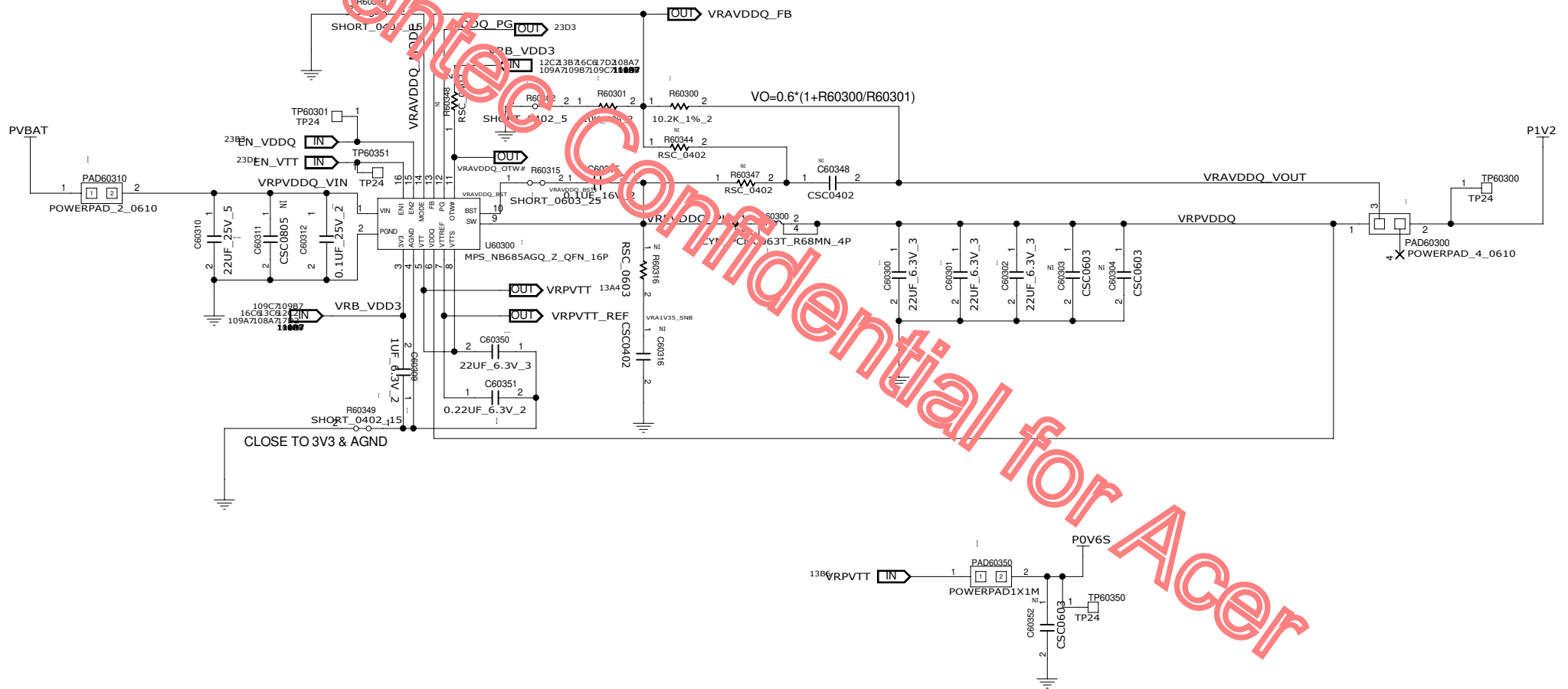
CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

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Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

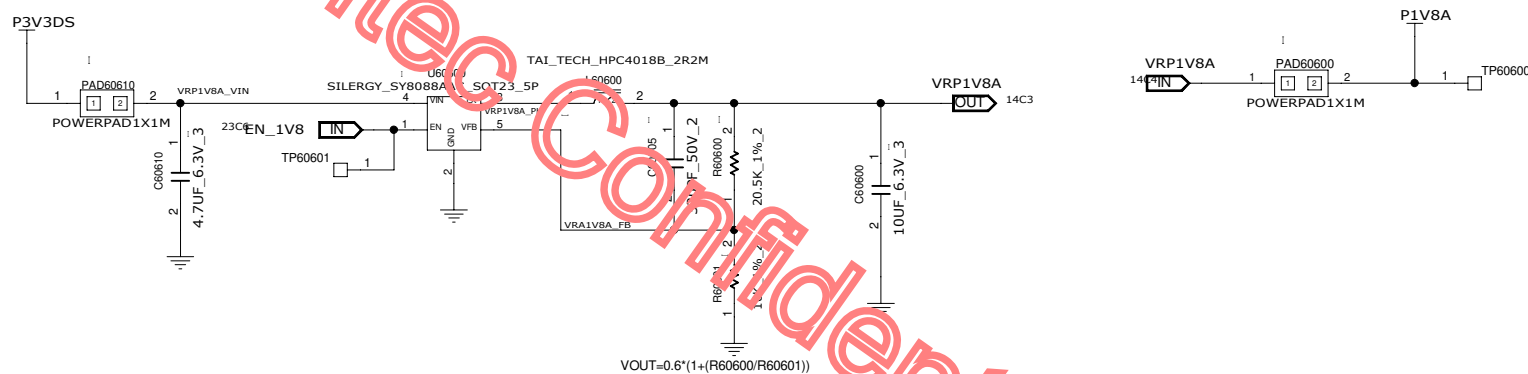


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
VDDO	

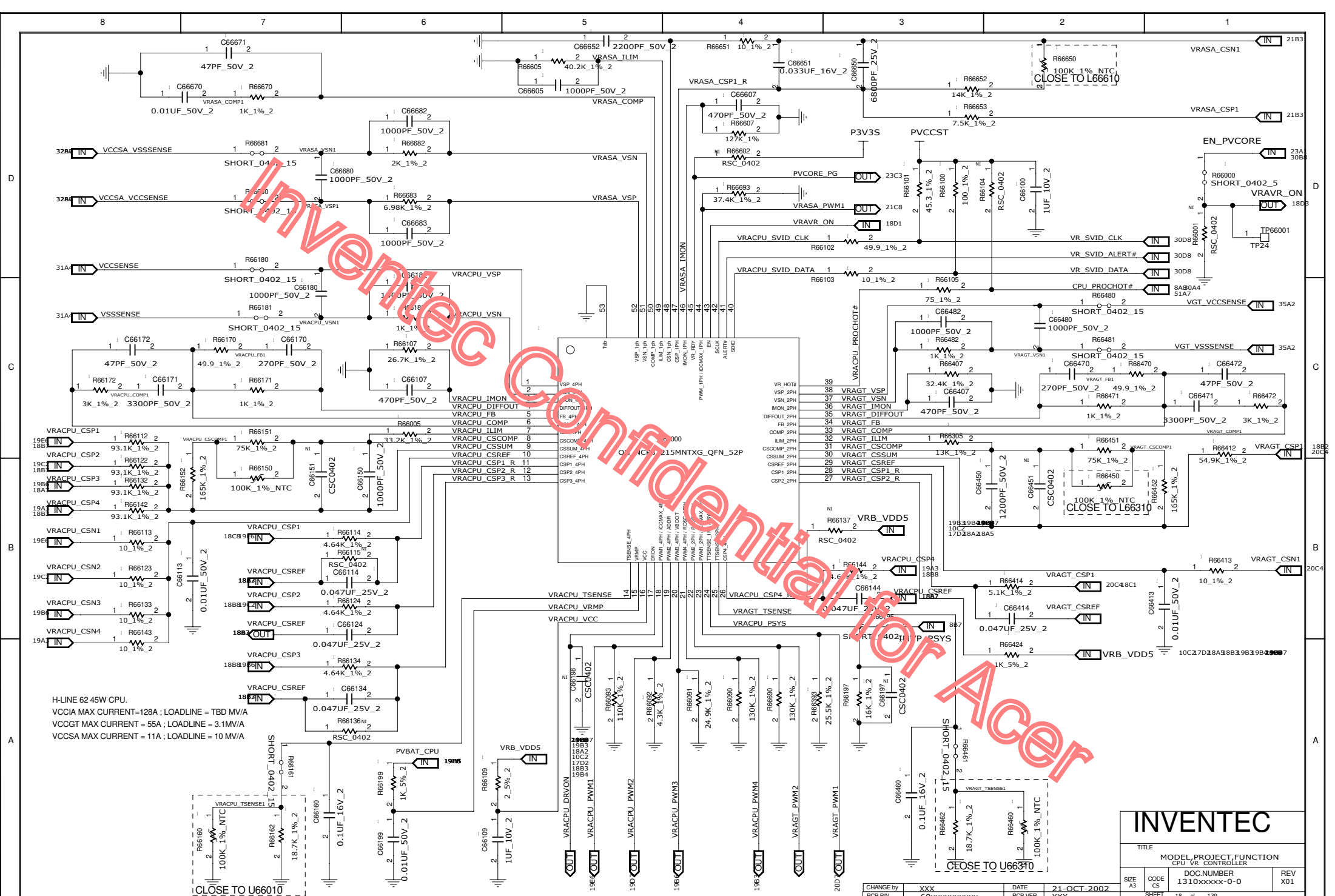
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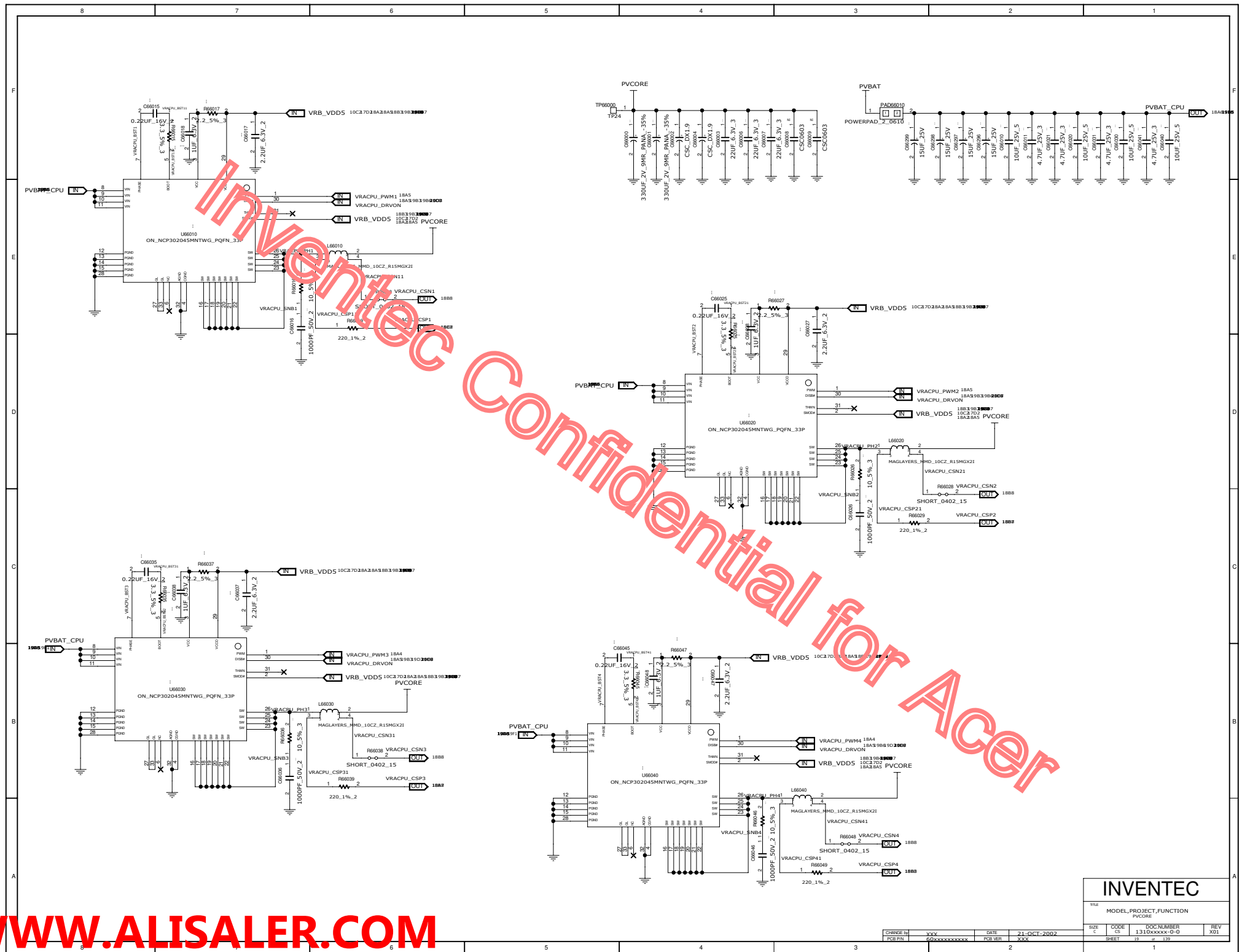
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX



$$VOUT=0.6*(1+(R60600/R60601))$$

INVENTEC				
TITLE MODEL PROJECT,FUNCTION P1V8DS				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 14 of 139

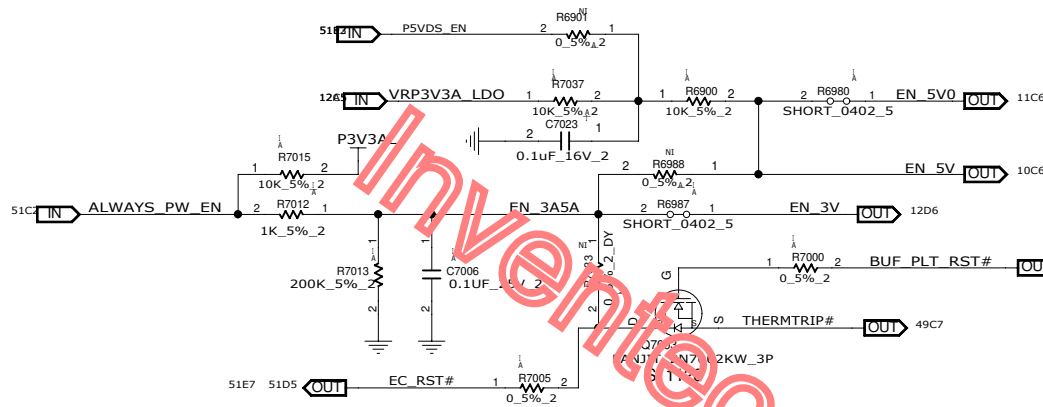




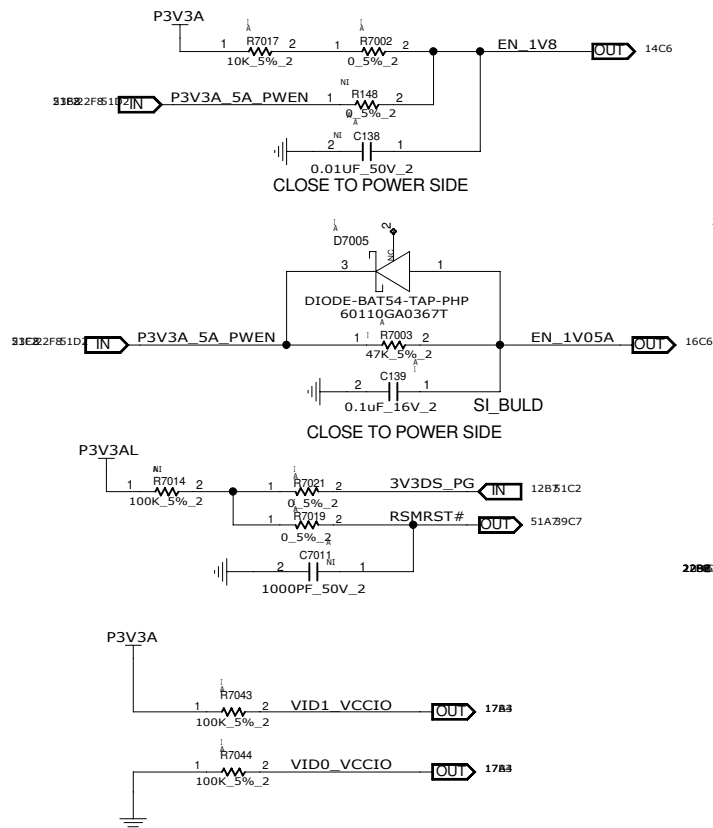
INVENTEC			
MODEL, PROJECT, FUNCTION			
SIZE	CODE	DOC NUMBER	REV
C	C5	1310xxxxx-0-0	X01
SHEET	19	139	

CHANGE D	XXXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

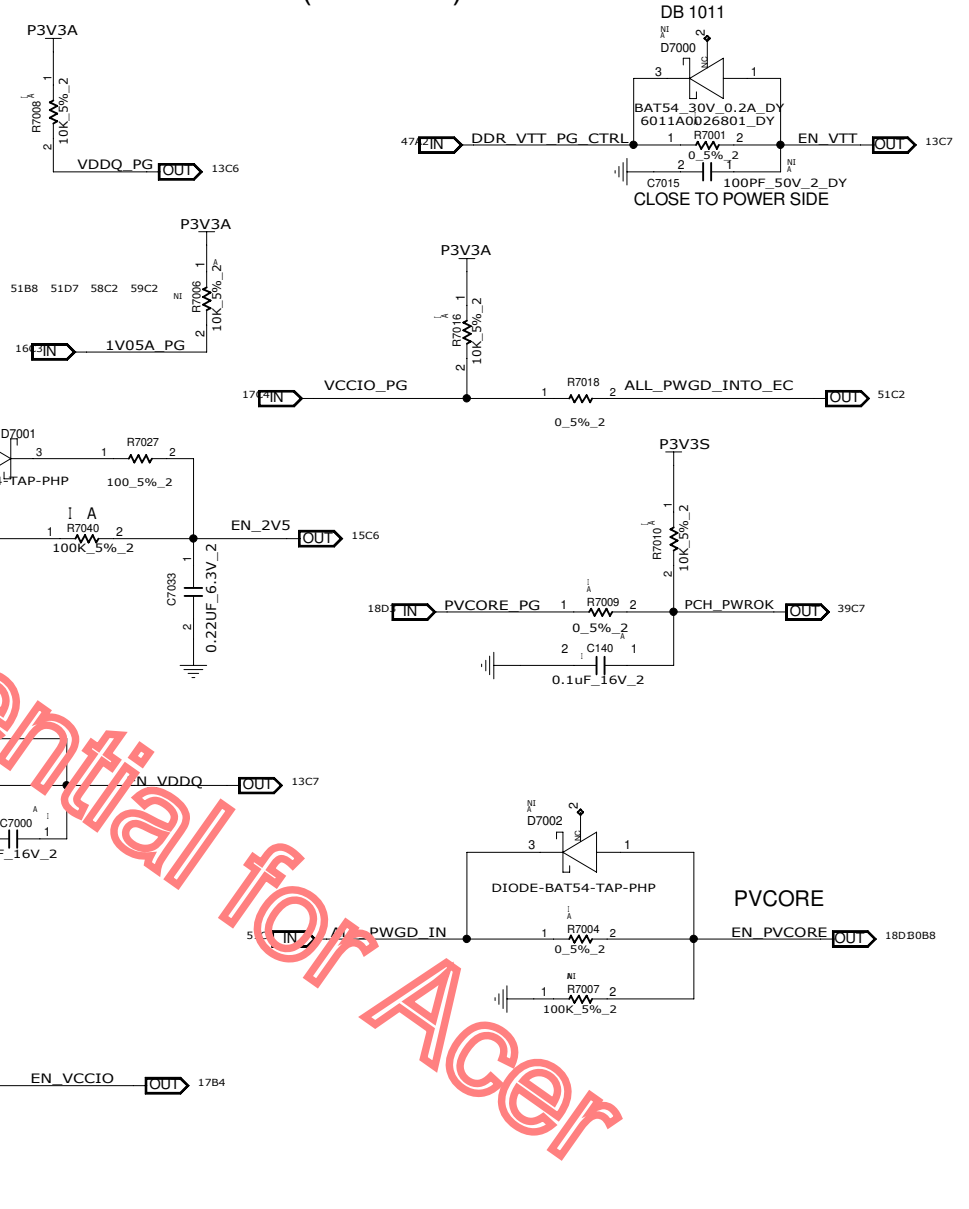
1. P3V3DS / P5V0DS



2. P1V0A / P1V8A / P3V3A



3. P1V2 / P1V8 / VCCSFR(PVCCST)

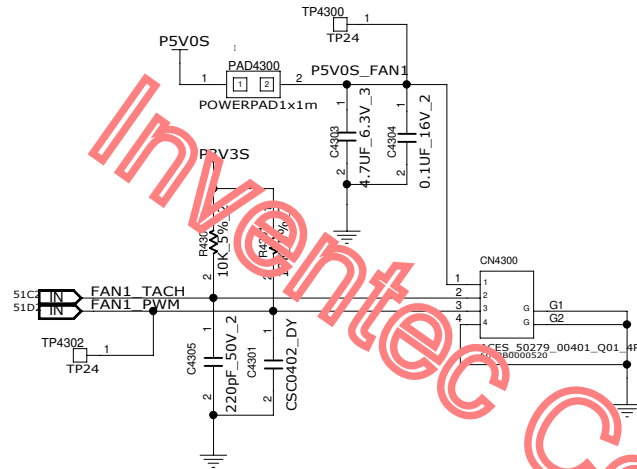


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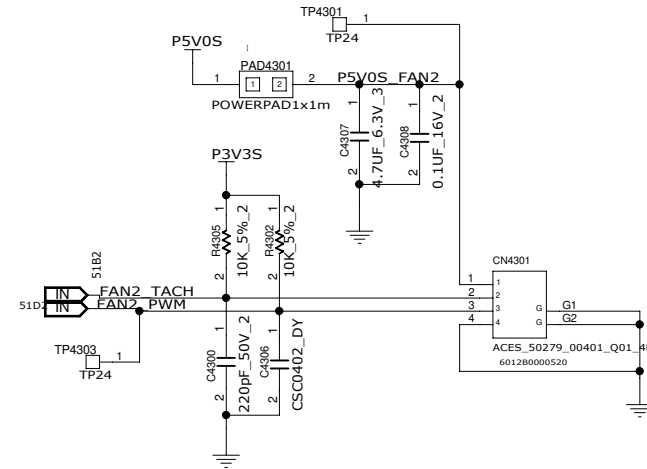
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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CHANGE by	XXX	DATE	XX/XX/2002
PCB P/N	6066xxxxxxx	PCB VER	XX/XX/2002

REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU

INVENTEC

TITLE			
MODEL,PROJECT FUNCTION FAN & THERMAL			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

REFERENCE 0~49(PCB SCREW)

1 FIX1
FIX_MASK
1 FIX2
FIX_MASK
1 FIX3
FIX_MASK
1 FIX4
FIX_MASK

1 FIX5
FIX_MASK
1 FIX6
FIX_MASK
1 FIX7
FIX_MASK
1 FIX8
FIX_MASK

1 S35
SCREW280_900_700_1P
1 S18
SCREW280_700_1P
1 S19
SCREW280_700_1P
1 S20
SCREW280_700_1P
1 S21
SCREW280_700_1P
1 S22
SCREW280_700_1P
1 S23
SCREW280_700_1P
1 S24
SCREW280_700_1P

1 S27
SCREW390_850_700_1P
1 S25
SCREW390_850_700_1P
1 S26
SCREW390_1160_850_1P
1 S11
SCREW280_900_550_NP_1P
1 S10
SCREW280_850_700_1P
1 S16
SCREW280_850_700_1P
1 S17
SCREW280_700_1P

PCB

1 S2
SCREW420_700_1P
1 S3
SCREW420_700_1P
1 S4
SCREW420_700_1P
1 S5
SCREW420_700_1P
1 S6
SCREW420_700_1P
1 S7
SCREW420_700_1P
1 S8
SCREW420_700_1P

INVENTEC

TITLE
MODEL PROJECT FUNCTION
XDP & ME CONN.

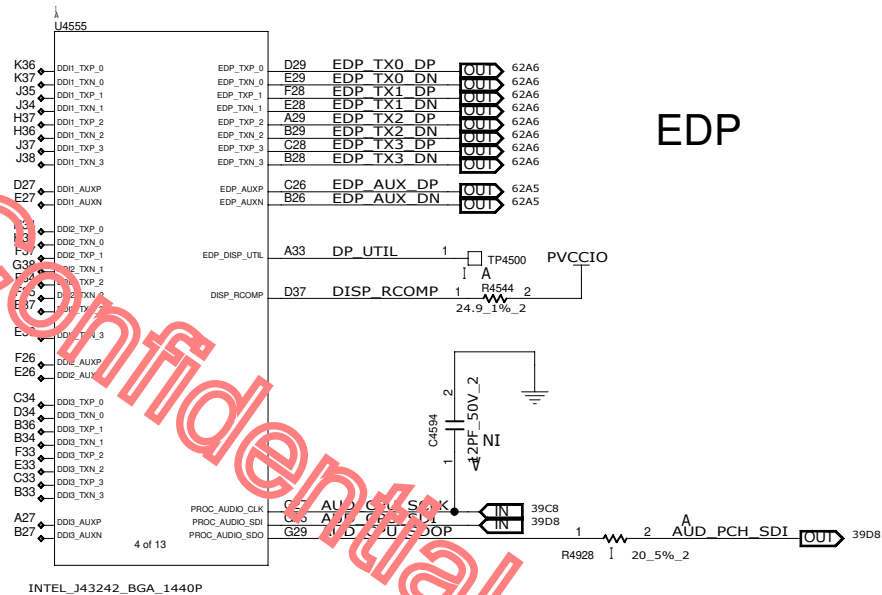
SIZE CODE
A3 CS 1310xxxxx-0-0 REV
X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

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8	7	6	5	4	3	2	1
D							
C							
B							
A							
<div>Inventory Control for Acer</div>							
<div>INVENTEC</div> <div>TITLE MODEL PROJECT FUNCTION SKYLAKE_L_H-PEG_HDMI</div> <div>SIZE CODE DOC NUMBER REV A3 CS 1310xxxxx-0-0 X01</div> <div>CHANGE by DATE 21-OCT-2002 PCB P/N 60xxxxxxxxxxx PCB VER XXX</div> <div>SHEET 26 of 139</div>							

Inventec Confidential for Acer



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION SKYLAKE2_H-DD1,EDP			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

Inv

470	BI	M A DO<3>	BR3	DDR0_DQ_3,DDR0_DQ_3	AK1	M CLK DDR1 DN	BI	47C7
471	BI	M A DO<4>	BN5	DDR0_DQ_4,DDR0_DQ_4	AL3			
472	BI	M A DO<5>	BP6	DDR0_5,DDR0_DQ_5	AK3			
473	BI	M A DO<6>	BP2	DDR0_6,DDR0_DQ_6	AL2			
474	BI	M A DO<7>	BN3	DDR0_7,DDR0_DQ_7	AL1			
475	BI	M A DO<8>	BL4	DDR0_8,DDR0_DQ_8				
476	BI	M A DO<9>	BL5	DDR0_9,DDR0_DQ_9	AT1	M CKE0	BI	47C7
477	BI	M A DO<10>	BL2	DDR0_10,DDR0_DQ_10	AT2	M CKE1	BI	47C7
478	BI	M A DO<11>	BM1	DDR0_11,DDR0_DQ_11	AT3			
479	BI	M A DO<12>	BK4	DDR0_12,DDR0_DQ_12	AT5			
480	BI	M A DO<13>	BK5	DDR0_13,DDR0_DQ_13				
481	BI	M A DO<14>	BK1	DDR0_14,DDR0_DQ_14	AD5	M CS#0	BI	47C7
482	BI	M A DO<15>	BK2	DDR0_15,DDR0_DQ_15	AE2	M CS#1	BI	47C7
483	BI	M A DO<16>	BG4	DDR0_16,DDR0_DQ_32	AD2			
484	BI	M A DO<17>	BG5	DDR0_17,DDR0_DQ_33	AE5			
485	BI	M A DO<18>	BF4	DDR0_18,DDR0_DQ_34				
486	BI	M A DO<19>	BF5	DDR0_19,DDR0_DQ_35	AD3	M ODT0	BI	47C7
487	BI	M A DO<20>	BG2	DDR0_20,DDR0_DQ_36	AE4	M ODT1	BI	47C7
488	BI	M A DO<21>	BG1	DDR0_21,DDR0_DQ_37	AE1			
489	BI	M A DO<22>	BF1	DDR0_22,DDR0_DQ_38	AD4			
490	BI	M A DO<23>	BF2	DDR0_23,DDR0_DQ_39				
491	BI	M A DO<24>	BC1	DDR0_24,DDR0_DQ_40	AH5	M A BS0	BI	47D7
492	BI	M A DO<25>	BC2	DDR0_25,DDR0_DQ_41	AH1	M A BS1	BI	47D7
493	BI	M A DO<26>	BC5	DDR0_26,DDR0_DQ_42	AU1	M A BG0	BI	47D7
494	BI	M A DO<27>	BC3	DDR0_27,DDR0_DQ_43				
495	BI	M A DO<28>	BD4	DDR0_28,DDR0_DQ_44	AH4	M A RAS#	BI	47D7
496	BI	M A DO<29>	BD4	DDR0_29,DDR0_DQ_45	AG4	M A WE#	BI	47D7
497	BI	M A DO<30>	BC1	DDR0_30,DDR0_DQ_46	AD1	M A CS#	BI	47D7
498	BI	M A DO<31>	BC2	DDR0_31,DDR0_DQ_47				
499	BI	M A DO<32>	AB1	DDR0_32,DDR0_DQ_48	AH3	M A A 0	BI	47D7
500	BI	M A DO<33>	AB2	DDR0_33,DDR0_DQ_49	AP4	M A A 1	BI	47D7
501	BI	M A DO<34>	AA4	DDR0_34,DDR0_DQ_50	AN4	M A A 2	BI	47D7
502	BI	M A DO<35>	AA5	DDR0_35,DDR0_DQ_51	AP5	M A A 3	BI	47D7
503	BI	M A DO<36>	AB5	DDR0_36,DDR0_DQ_52	AP2	M A A 4	BI	47D7
504	BI	M A DO<37>	AB4	DDR0_37,DDR0_DQ_53	AP1	M A A 5	BI	47D7
505	BI	M A DO<38>	AA2	DDR0_38,DDR0_DQ_54	AP3	M A A 6	BI	47D7
506	BI	M A DO<39>	AA1	DDR0_39,DDR0_DQ_55	AN1	M A A 7	BI	47D7
507	BI	M A DO<40>	V5	DDR0_40,DDR0_DQ_8	AN3	M A A 8	BI	47D7
508	BI	M A DO<41>	V2	DDR0_41,DDR0_DQ_9	AT4	M A A 9	BI	47D7
509	BI	M A DO<42>	U1	DDR0_42,DDR0_DQ_10	AH2	M A A 10	BI	47D7
510	BI	M A DO<43>	U2	DDR0_43,DDR0_DQ_11	AN2	M A A 11	BI	47D7
511	BI	M A DO<44>	V1	DDR0_44,DDR0_DQ_12	AU4	M A A 12	BI	47D7
512	BI	M A DO<45>	V4	DDR0_45,DDR0_DQ_13	AL3	M A A 13	BI	47D7
513	BI	M A DO<46>	U5	DDR0_46,DDR0_DQ_14	AL2	M A BG1	BI	47D7
514	BI	M A DO<47>	U4	DDR0_47,DDR0_DQ_15	AL3	M A ACT#	BI	47C3
515	BI	M A DO<48>	R2	DDR0_48,DDR0_DQ_32				
516	BI	M A DO<49>	P5	DDR0_49,DDR0_DQ_33				
517	BI	M A DO<50>	R4	DDR0_50,DDR0_DQ_34				
518	BI	M A DO<51>	P4	DDR0_51,DDR0_DQ_35				
519	BI	M A DO<52>	R5	DDR0_52,DDR0_DQ_36				
520	BI	M A DO<53>	P2	DDR0_53,DDR0_DQ_37	BR5	M A DOS0 DN	BI	47B7
521	BI	M A DO<54>	R1	DDR0_54,DDR0_DQ_38	BL3	M A DOS1 DN	BI	47B7
522	BI	M A DO<55>	P1	DDR0_55,DDR0_DQ_39	BG3	M A DOS2 DN	BI	47B7
523	BI	M A DO<56>	M4	DDR0_56,DDR0_DQ_40	BG3	M A DOS3 DN	BI	47B7
524	BI	M A DO<57>	M1	DDR0_57,DDR0_DQ_41	AA3	M A DOS4 DN	BI	47B7
525	BI	M A DO<58>	L4	DDR0_58,DDR0_DQ_42	U3	M A DOS5 DN	BI	47B7
526	BI	M A DO<59>	L2	DDR0_59,DDR0_DQ_43	P3	M A DOS6 DN	BI	47B7
527	BI	M A DO<60>	M5	DDR0_60,DDR0_DQ_44	L3	M A DOS7 DN	BI	47B7
528	BI	M A DO<61>	M2	DDR0_61,DDR0_DQ_45				
529	BI	M A DO<62>	L5	DDR0_62,DDR0_DQ_46				
530	BI	M A DO<63>	L1	DDR0_63,DDR0_DQ_47				
531	BI	M A DO<64>	BA2	NCDDR0_ECC_0				
532	BI	M A DO<65>	BA1	NCDDR0_ECC_1				
533	BI	M A DO<66>	AY4	NCDDR0_ECC_2				
534	BI	M A DO<67>	AY5	NCDDR0_ECC_3				
535	BI	M A DO<68>	BA5	NCDDR0_ECC_4				
536	BI	M A DO<69>	BA4	NCDDR0_ECC_5				
537	BI	M A DO<70>	AY1	NCDDR0_ECC_6				
538	BI	M A DO<71>	AY2	NCDDR0_ECC_7				

1 OF 13
DDR CHANNEL A

DDR0_DQ_3,DDR0_DQ_3

DDR0_DQ_4,DDR0_DQ_4

DDR0_5,DDR0_DQ_5

DDR0_6,DDR0_DQ_6

DDR0_7,DDR0_DQ_7

DDR0_8,DDR0_DQ_8

DDR0_9,DDR0_DQ_9

DDR0_10,DDR0_DQ_10

DDR0_11,DDR0_DQ_11

DDR0_12,DDR0_DQ_12

DDR0_13,DDR0_DQ_13

DDR0_14,DDR0_DQ_14

DDR0_15,DDR0_DQ_15

DDR0_16,DDR0_DQ_32

DDR0_17,DDR0_DQ_33

DDR0_18,DDR0_DQ_34

DDR0_19,DDR0_DQ_35

DDR0_20,DDR0_DQ_36

DDR0_21,DDR0_DQ_37

DDR0_22,DDR0_DQ_38

DDR0_23,DDR0_DQ_39

DDR0_24,DDR0_DQ_40

DDR0_25,DDR0_DQ_41

DDR0_26,DDR0_DQ_42

DDR0_27,DDR0_DQ_43

DDR0_28,DDR0_DQ_44

DDR0_29,DDR0_DQ_45

DDR0_30,DDR0_DQ_46

DDR0_31,DDR0_DQ_47

DDR0_32,DDR0_DQ_48

DDR0_33,DDR0_DQ_49

DDR0_34,DDR0_DQ_50

DDR0_35,DDR0_DQ_51

DDR0_36,DDR0_DQ_52

DDR0_37,DDR0_DQ_53

DDR0_38,DDR0_DQ_54

DDR0_39,DDR0_DQ_55

DDR0_40,DDR0_DQ_8

DDR0_41,DDR0_DQ_9

DDR0_42,DDR0_DQ_10

DDR0_43,DDR0_DQ_11

DDR0_44,DDR0_DQ_12

DDR0_45,DDR0_DQ_13

DDR0_46,DDR0_DQ_14

DDR0_47,DDR0_DQ_15

DDR0_48,DDR0_DQ_32

DDR0_49,DDR0_DQ_33

DDR0_50,DDR0_DQ_34

DDR0_51,DDR0_DQ_35

DDR0_52,DDR0_DQ_36

DDR0_53,DDR0_DQ_37

DDR0_54,DDR0_DQ_38

DDR0_55,DDR0_DQ_39

DDR0_56,DDR0_DQ_40

DDR0_57,DDR0_DQ_41

DDR0_58,DDR0_DQ_42

DDR0_59,DDR0_DQ_43

DDR0_60,DDR0_DQ_44

DDR0_61,DDR0_DQ_45

DDR0_62,DDR0_DQ_46

DDR0_63,DDR0_DQ_47

NCDDR0_ECC_0

NCDDR0_ECC_1

NCDDR0_ECC_2

NCDDR0_ECC_3

NCDDR0_ECC_4

NCDDR0_ECC_5

NCDDR0_ECC_6

NCDDR0_ECC_7

DDR0_CKE_0,DDR0_CKE_0

DDR0_CKE_1,DDR0_CKE_1

DDR0_CKE_2,DDR0_CKE_2

DDR0_CKE_3,DDR0_CKE_3

DDR0_CSK_0,DDR0_CSK_0

DDR0_CSK_1,DDR0_CSK_1

NCDDR0_CSK_2

NCDDR0_CSK_3

DDR0_ODT_0,DDR0_ODT_0

NCDDR0_ODT_1

NCDDR0_ODT_2

NCDDR0_ODT_3

DDR0_CAB_4,DDR0_BA_0

DDR0_CAB_6,DDR0_BA_1

DDR0_CAA_5,DDR0_BG_0

DDR0_CAB_3,DDR0_MA_16

DDR0_CAB_2,DDR0_MA_14

DDR0_CAB_1,DDR0_MA_15

DDR0_CAB_9,DDR0_MA_0

DDR0_CAB_8,DDR0_MA_1

DDR0_CAB_5,DDR0_MA_2

NCDDR0_MA_3

NCDDR0_MA_4

DDR0_CAA_0,DDR0_MA_5

DDR0_CAA_7,DDR0_MA_6

DDR0_CAA_4,DDR0_MA_7

DDR0_CAA_3,DDR0_MA_8

DDR0_CAA_0,DDR0_MA_9

DDR0_CAA_7,DDR0_MA_10

DDR0_CAA_7,DDR0_MA_11

DDR0_CAA_6,DDR0_MA_12

DDR0_CAA_5,DDR0_MA_13

DDR0_CAA_5,DDR0_MA_14

DDR0_CAA_5,DDR0_MA_15

NCDDR0_ALERT#

DDR0_DQSN_0,DDR0_DQSN_0

DDR0_DQSN_1,DDR0_DQSN_1

DDR0_DQSN_2,DDR0_DQSN_4

DDR0_DQSN_3,DDR0_DQSN_5

DDR0_DQSN_4,DDR0_DQSN_0

DDR0_DQSN_5,DDR0_DQSN_1

DDR0_DQSN_6,DDR0_DQSN_4

DDR0_DQSN_7,DDR0_DQSN_5

DDR0_DQSP_0,DDR0_DQSP_0

DDR0_DQSP_1,DDR0_DQSP_1

DDR0_DQSP_2,DDR0_DQSP_4

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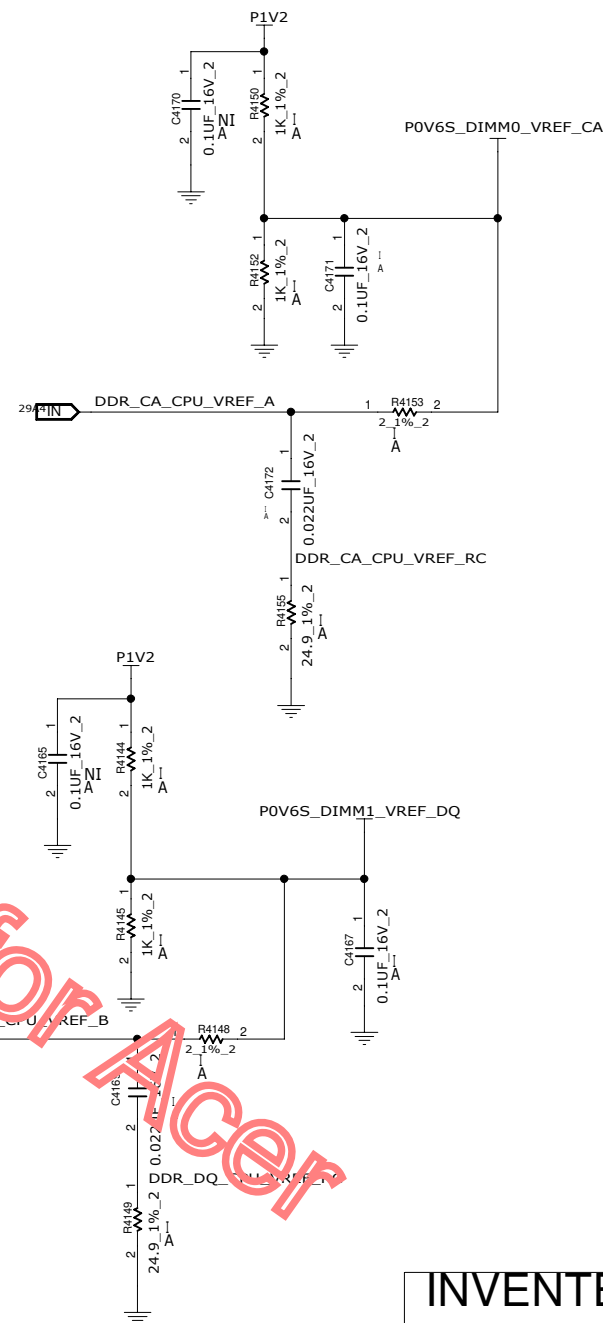
DDR0_DQSP_6,DDR0_DQSP_5

DDR0_DQSP_7,DDR0_DQSP_5

DDR0_DQSP_8,DDR0_DQSP_8

DDR0_DQSN_8,DDR0_DQSN_8

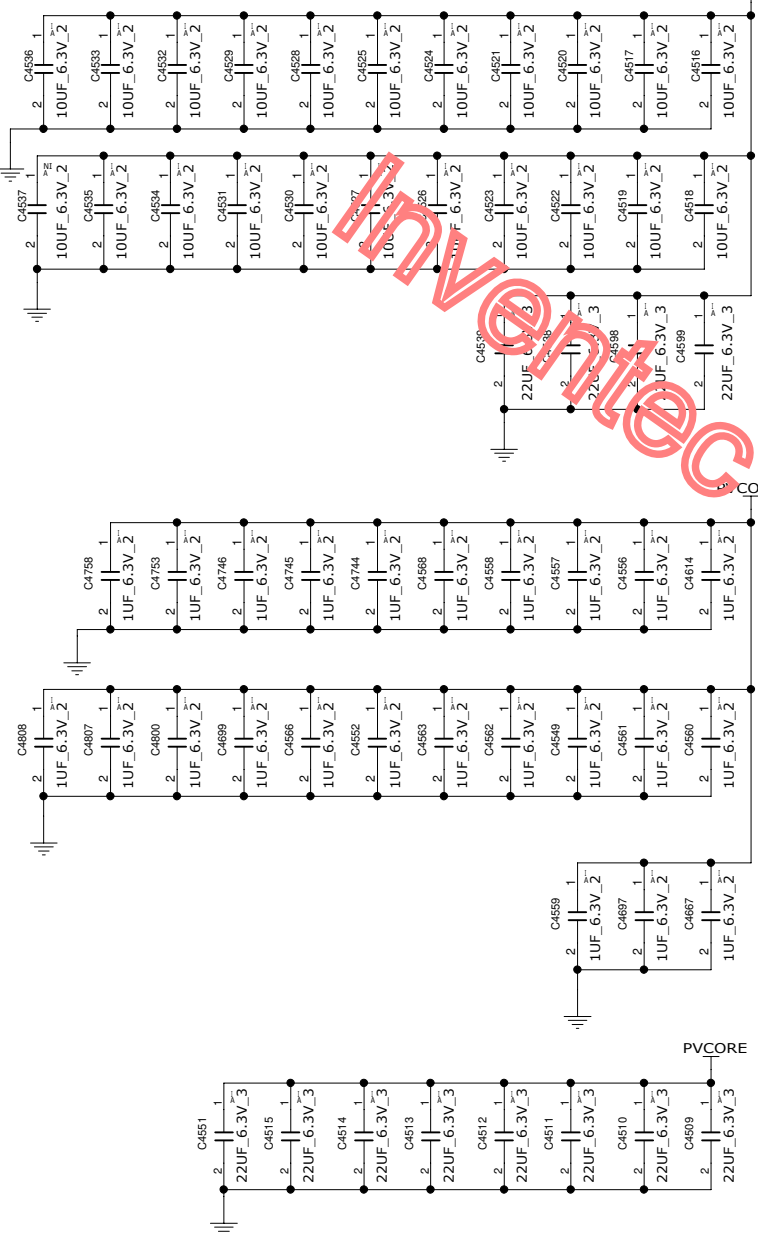
for Acer



CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 29 of 139			

PLACE IN BACK SIDE

PVCORE



EDS VER0.7

PVCORE
47UF X 5 22UF X 12
10UF X 21 1UF X 24

PVCORE

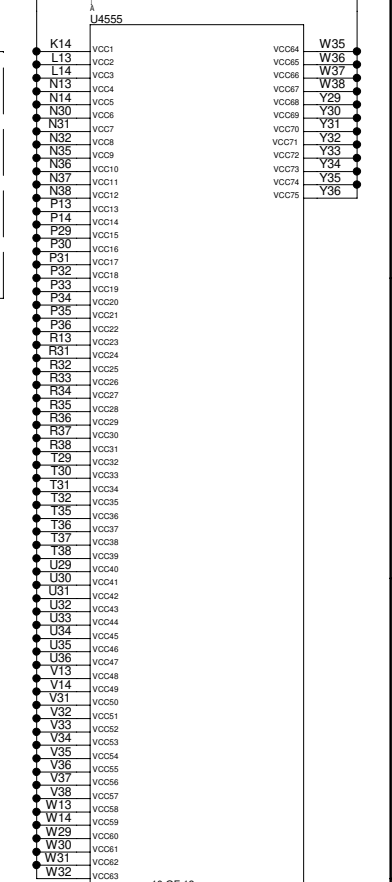
PVCORE

PVCORE

PLACE IN BOTTOM SIDE

PVCORE

PVCORE

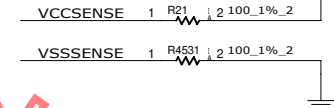


INTEL_J43242_BGA_1440P

9 OF 13

VCC_SENSE
VSS_SENSE

AG37 VCCSENSE
AG38 VSSSENSE



INTEL_J43242_BGA_1440P

10 OF 13

INVENTEC

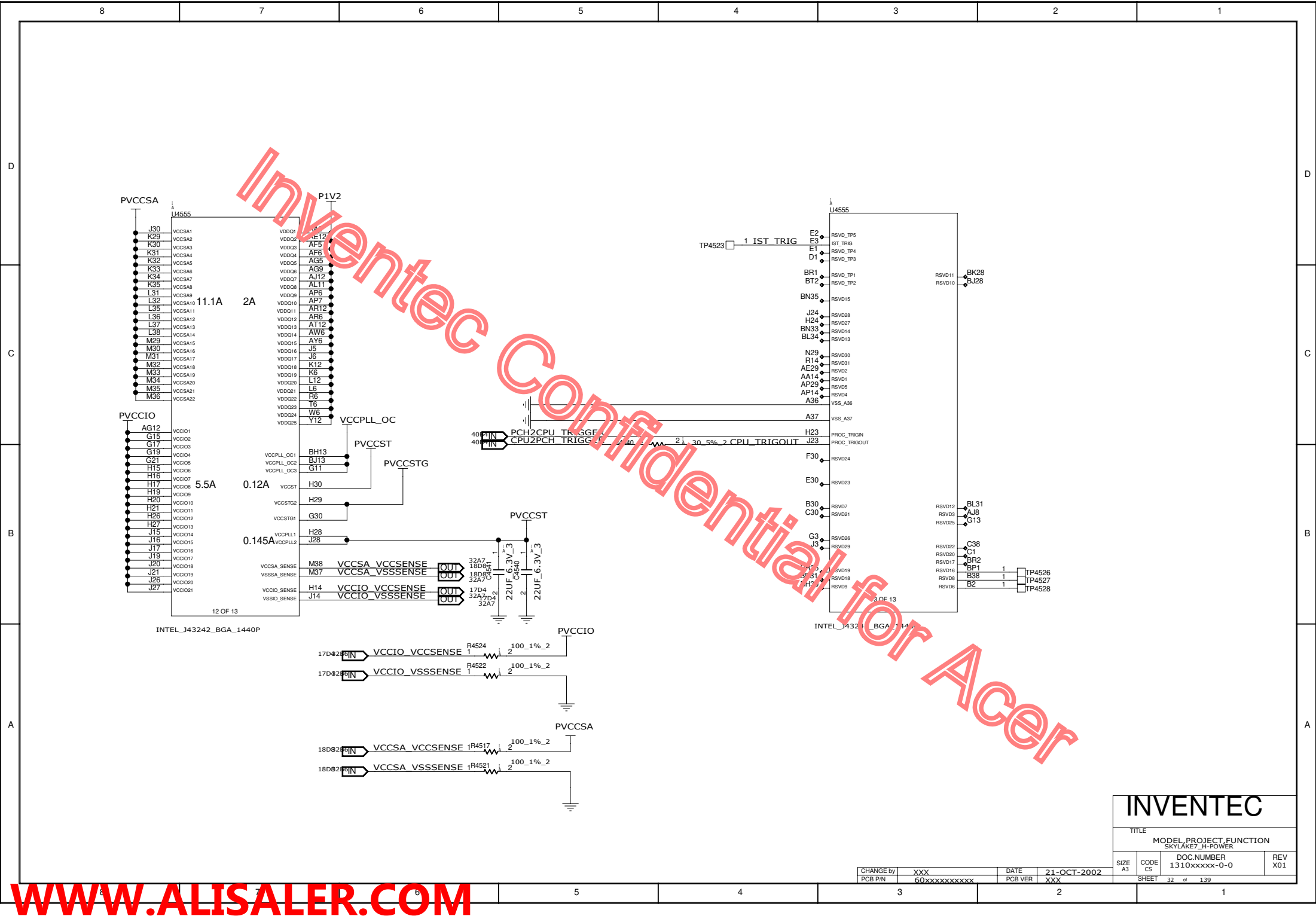
TITLE
MODEL PROJECT FUNCTION
SKYLAKES_HI-POWER

SIZE A3 CODE CS
DOC NUMBER 1310xxxxx-0-0
REV X01

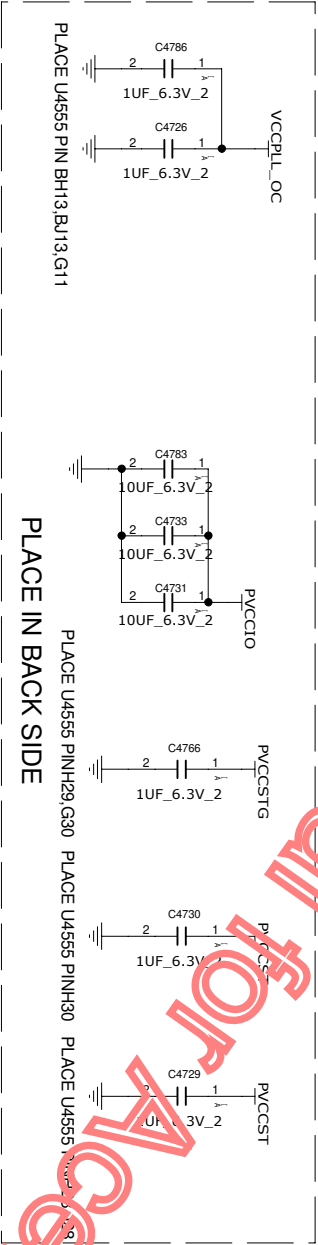
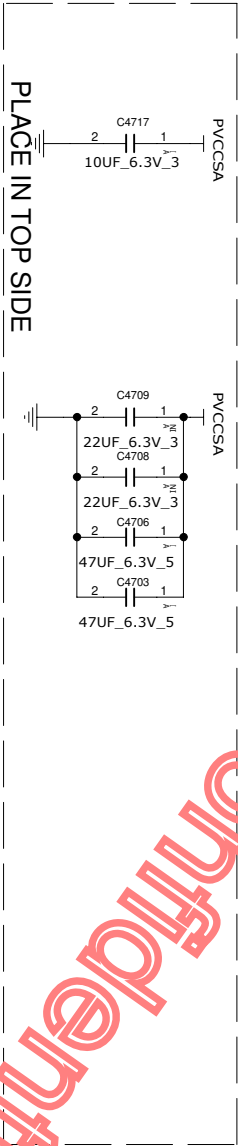
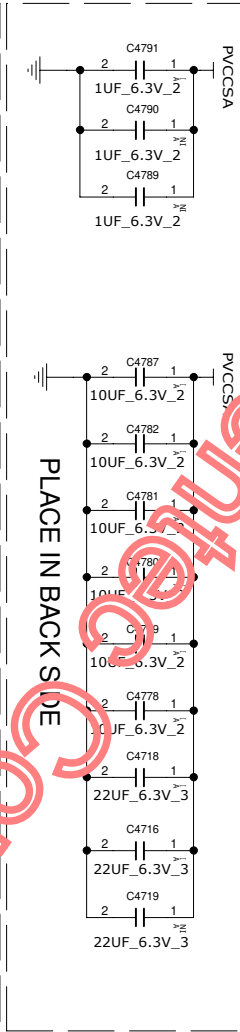
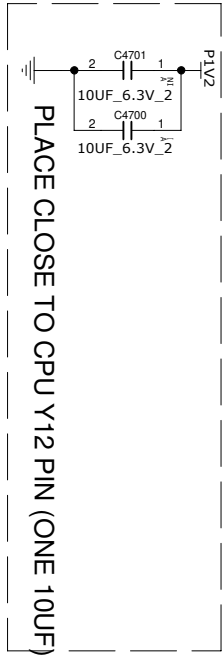
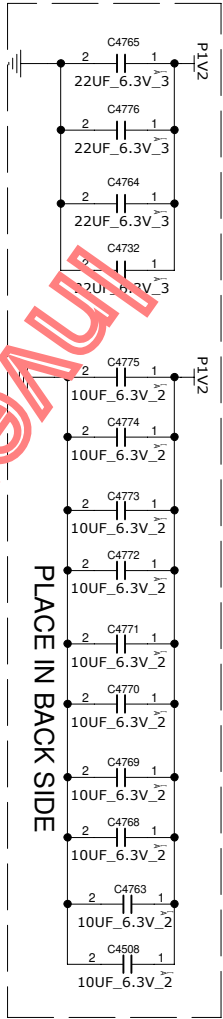
CHANGE by XXX
PCB P/N 60xxxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

SHEET 31 of 139



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
SKYLAKE7_H-POWER			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
SHEET		32 of 139	1

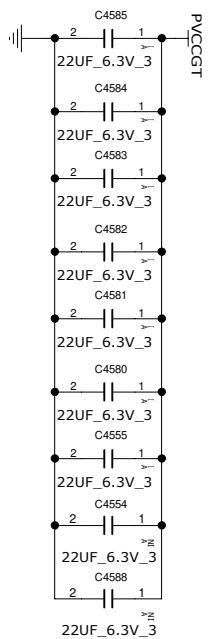
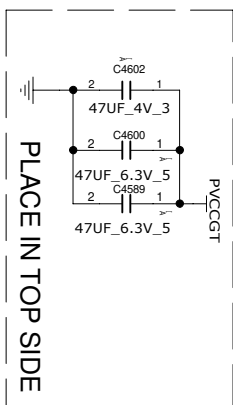


EDS VER0.7
P1V2
10UF X 11 22UF X 4
PVCCSA
47UF X 2 22UF X 2
10UF X 7 1UF X 1

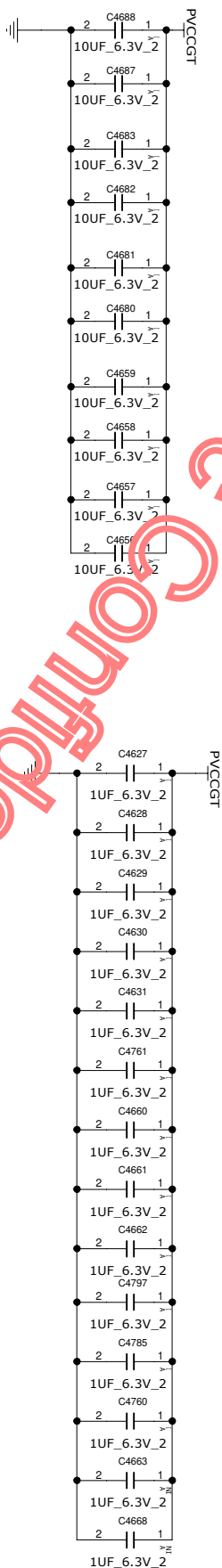
INVENTEC

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX

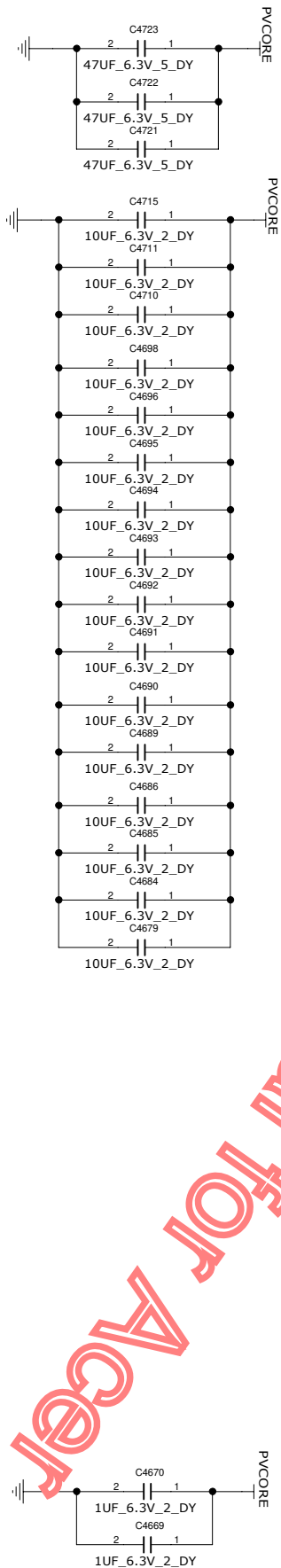
TITLE	MODEL/PROJECT/FUNCTION
SIZE	CS
CODE	1310XXXX-0-0
SHEET	33 of 139



PLACE IN BACK SIDE

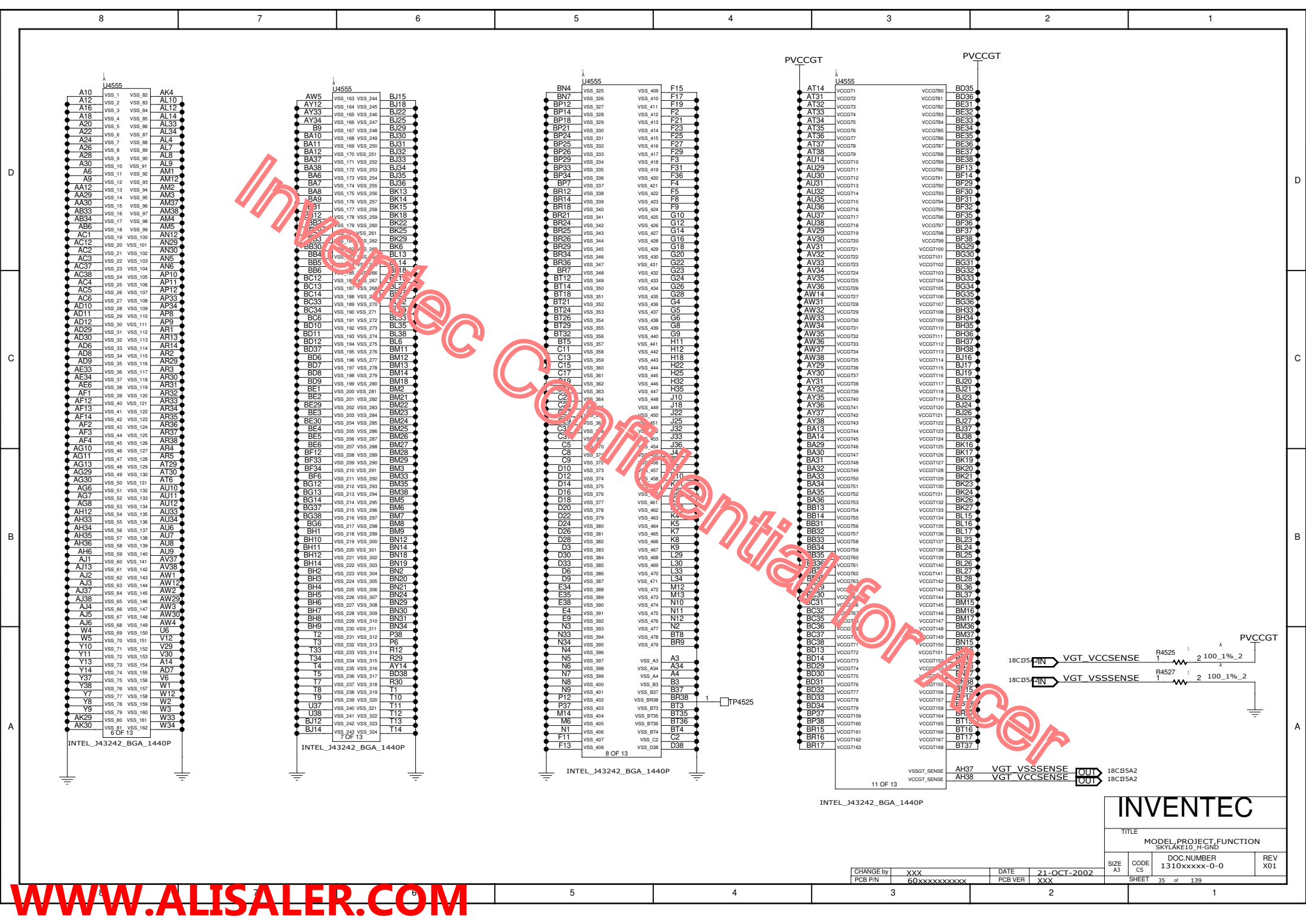


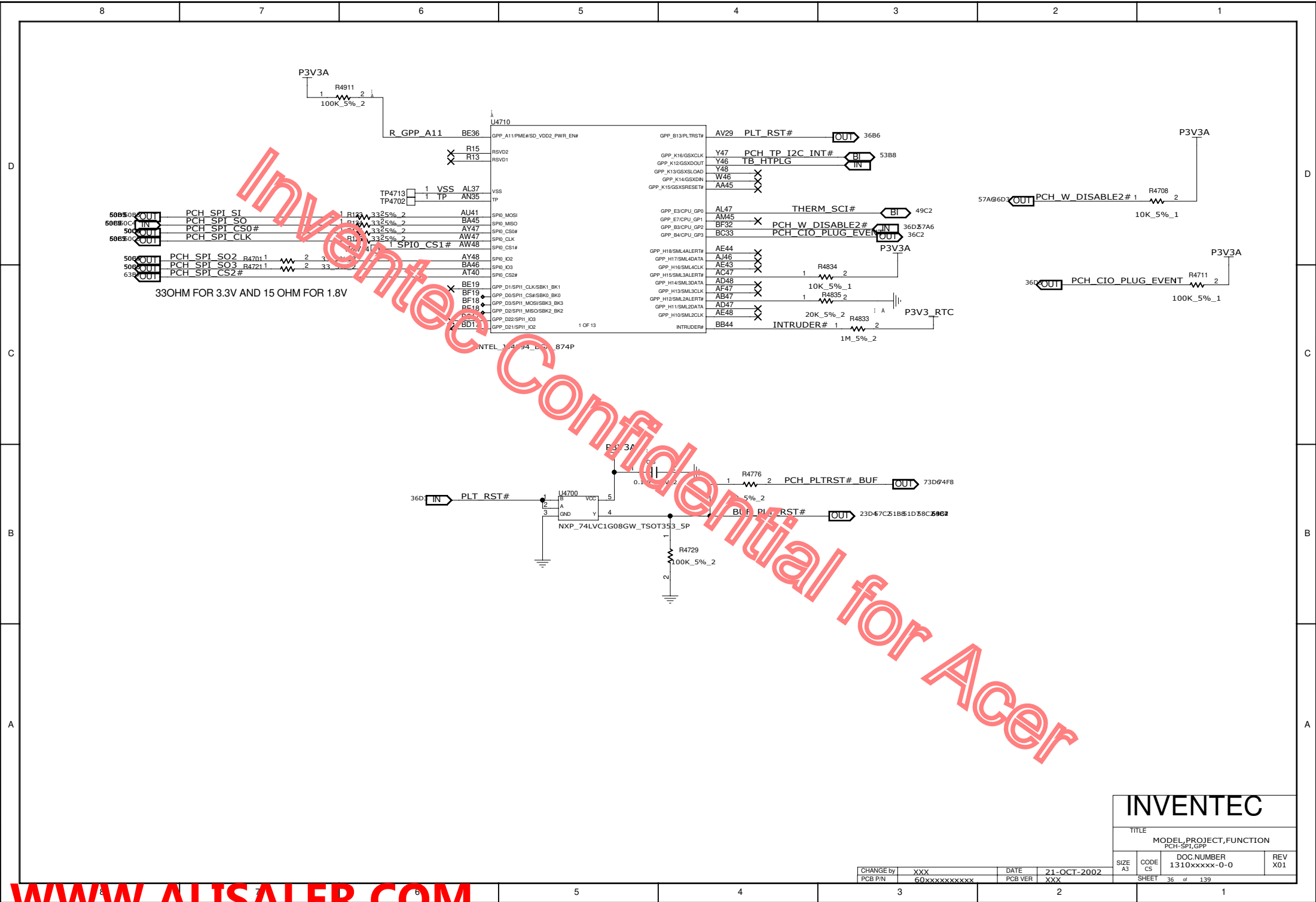
H82 CPU



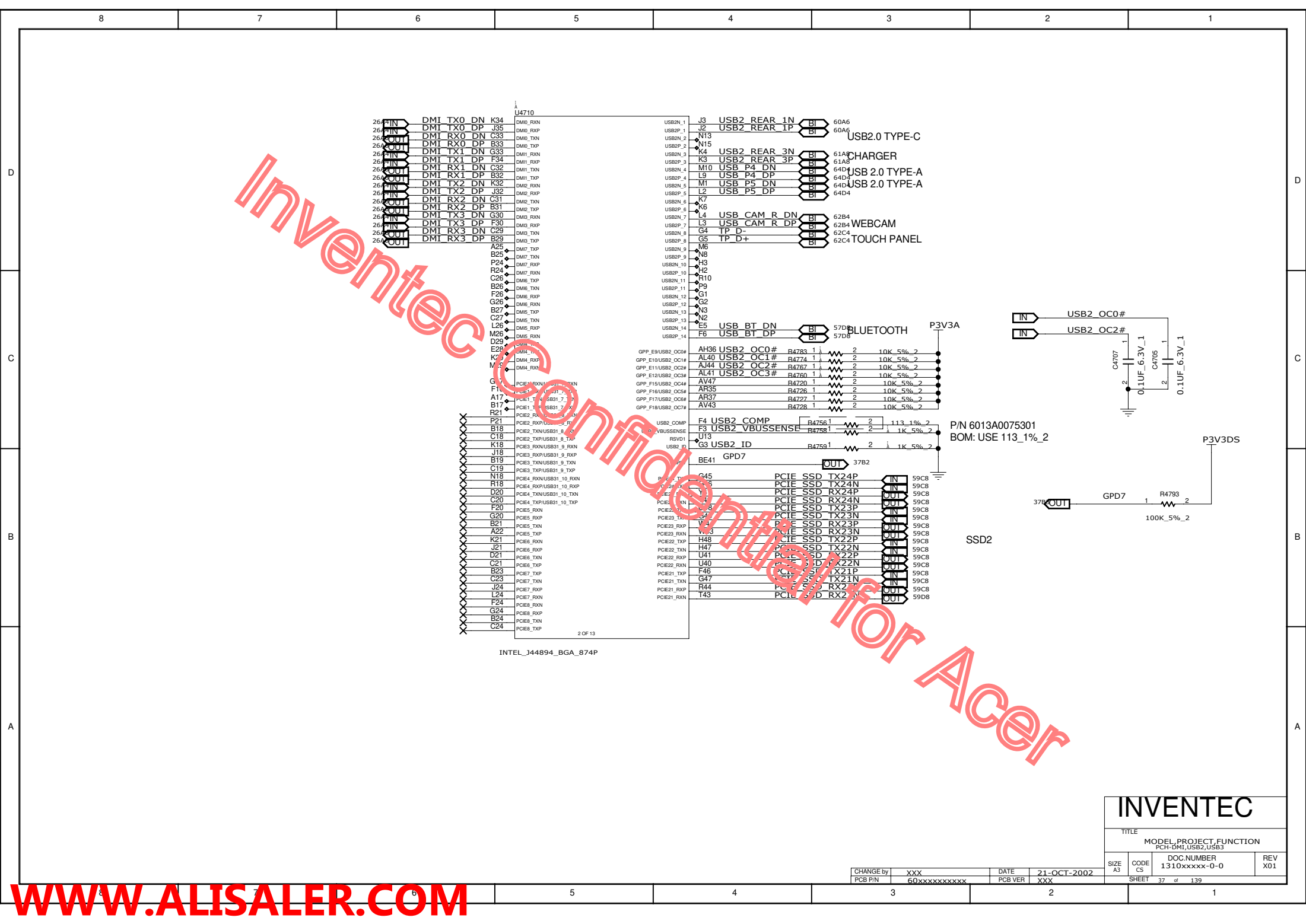
INVENTEC

MODEL PROJECT FUNCTION SKYLAKE9 H-GT DECOUPLING		CODE CS	DOC NUMBER 1310XXXXXX-0-0	SIZE A3	DATE 21-OCT-2002	CHANGE BY XXX	PGM VER XXX	REVISION 60XXXXXXXXXX
		SHEET 34 of 139						

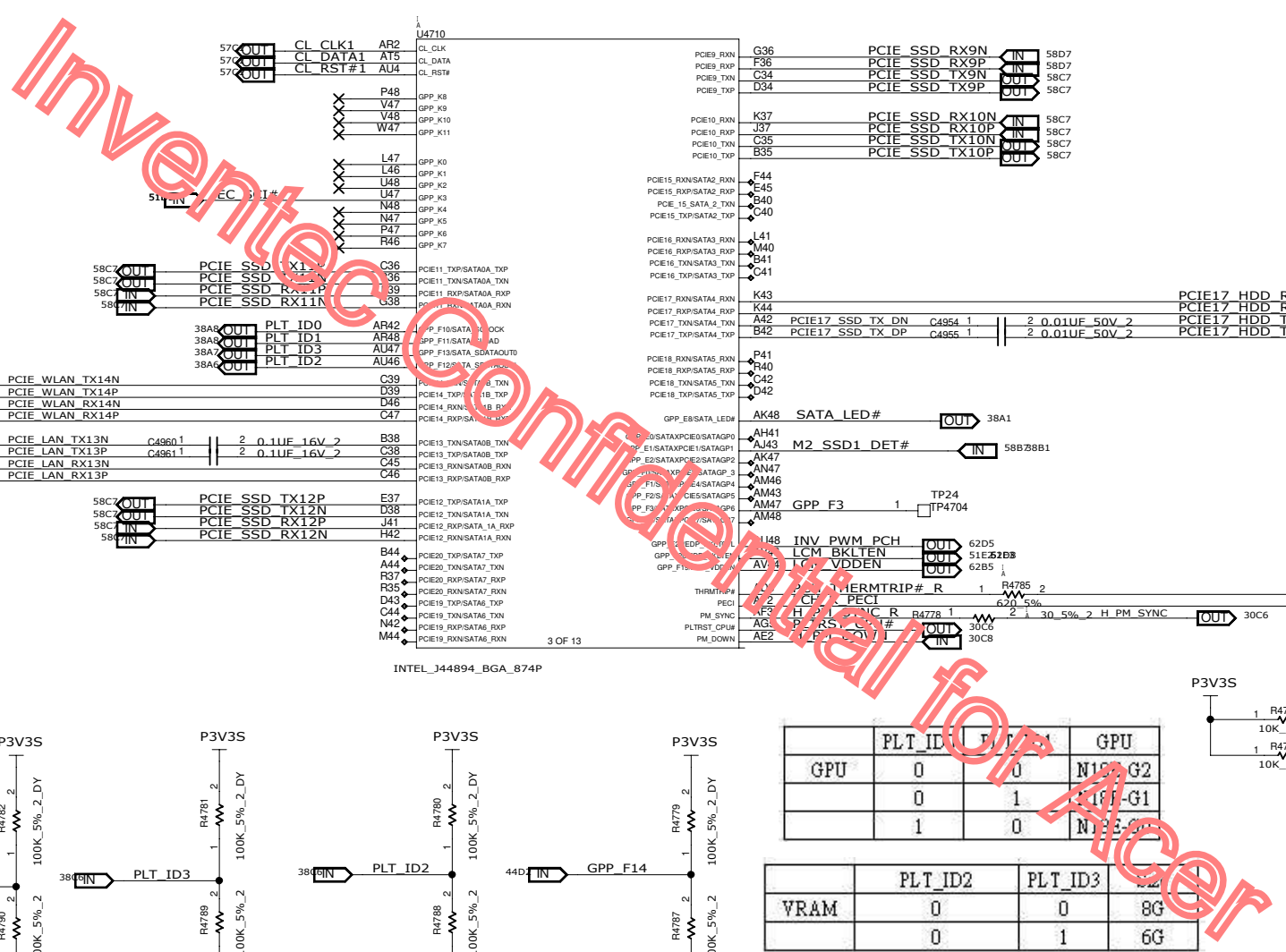




INVENTEC				
TITLE				
MODEL PROJECT,FUNCTION				
PCH-SPI-GPP				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
SHEET		36 of 139		



INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION PCH-DMI,USB2,USB3				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		REV X01
SHEET 37 of 139				



	PLT_ID1	PLT_ID2	GPU
GPU	0	0	N19 G2
	0	1	N19 G1
	1	0	N19 G0

	PLT_ID2	PLT_ID3	VRAM
VRAM	0	0	8G
	0	1	6G

	GPP_F14	Panel
GPU	0	15"
	1	17"

INVENTEC

TITLE

MODEL PROJECT FUNCTION

PCH-CLK/FAN/PCIE/SATA/HOST

SIZE A3

CODE CS

DOC NUMBER 1310xxxxx-0-0

REV X01

CHANGE by XXX

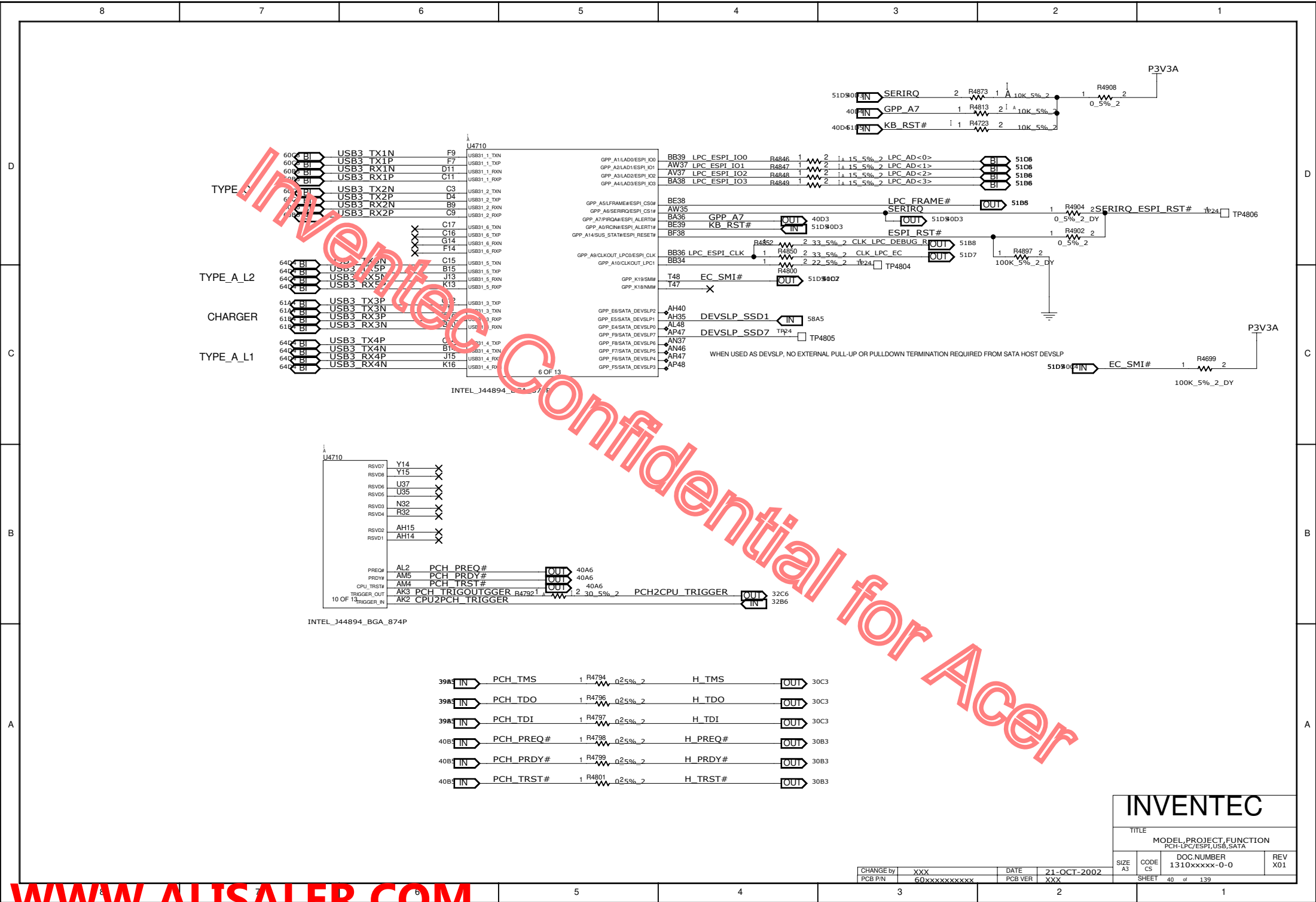
DATE 21-OCT-2002

PCB P/N 60xxxxxxxxxx

PCB VER XXX

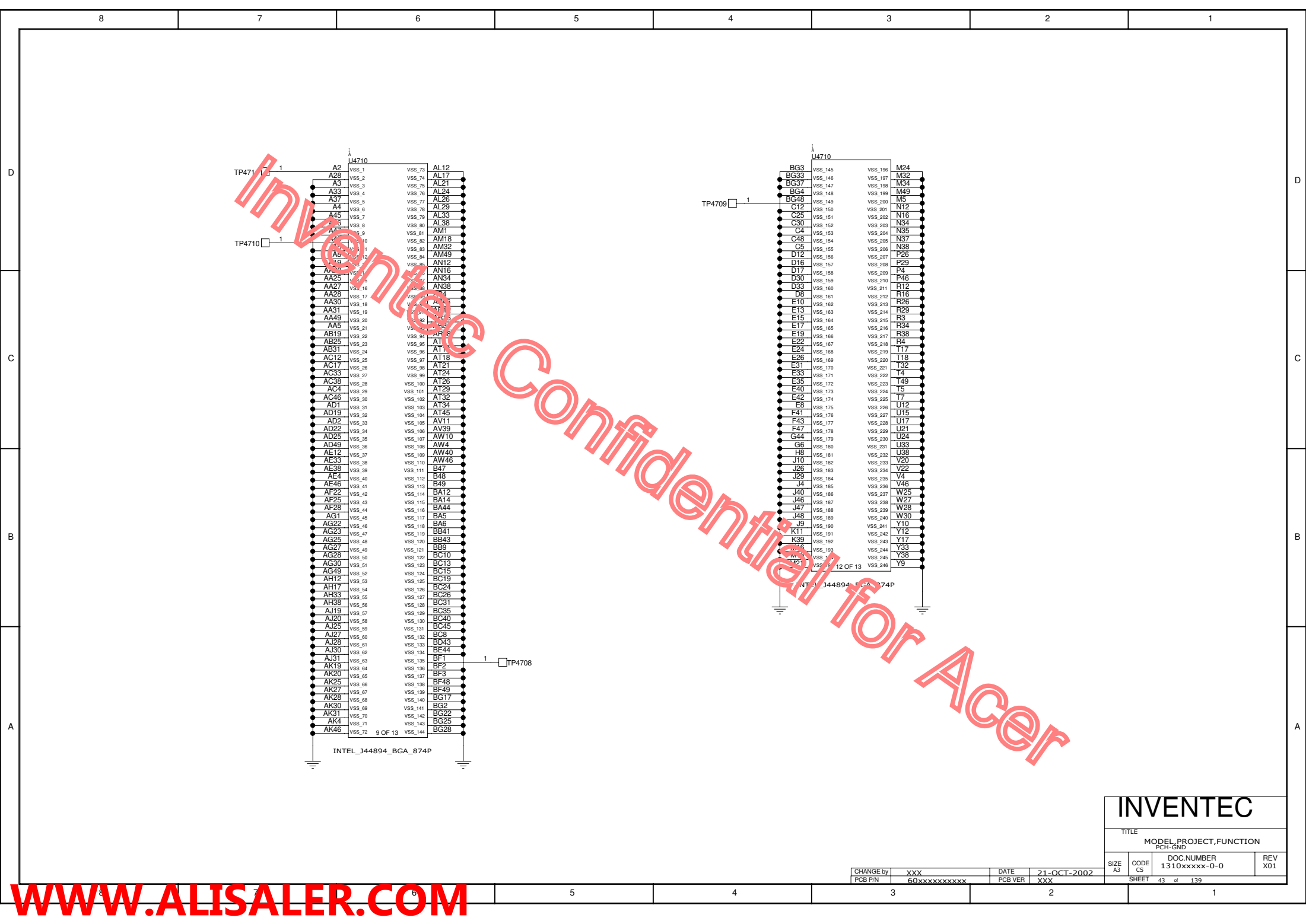
SHEET 38 of 139





INVENTEC				
TITLE				
MODEL PROJECT FUNCTION				
PCH-LPC/ESPI, USB, SATA				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
CHANGE by	DATE	21-OCT-2002		
PCB P/N	PCB VER	XXX		
SHEET		40 of 139		





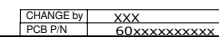
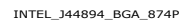
INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION PCB-GND				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01	
SHEET 43 of 139				

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



A

- A



D

C

B

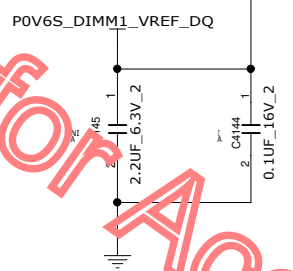
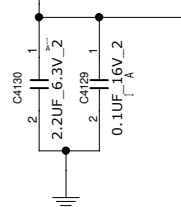
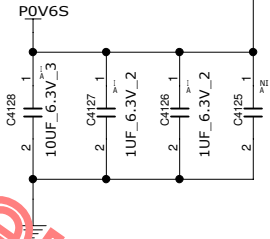
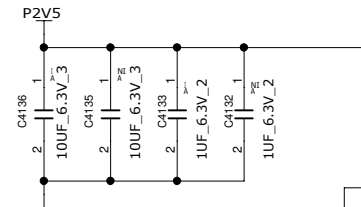
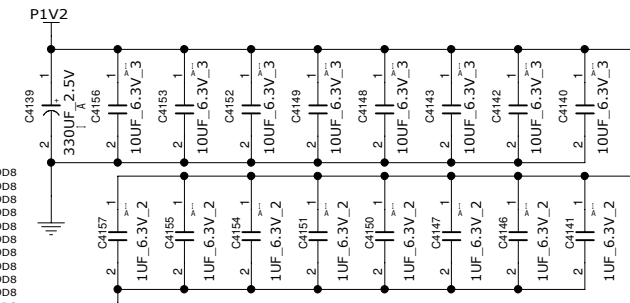
A

D

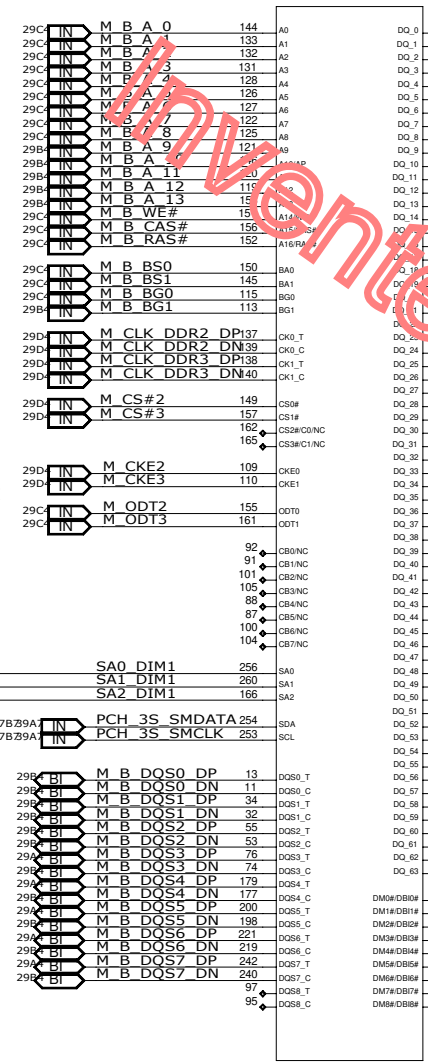
C

B

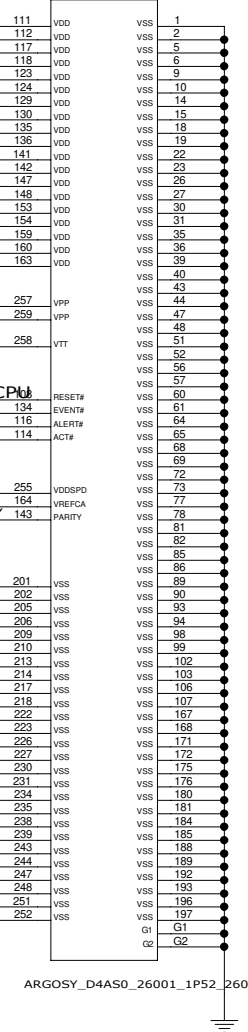
A



CN4125
6026B0363901-001



CN4125
6026B0363901-001



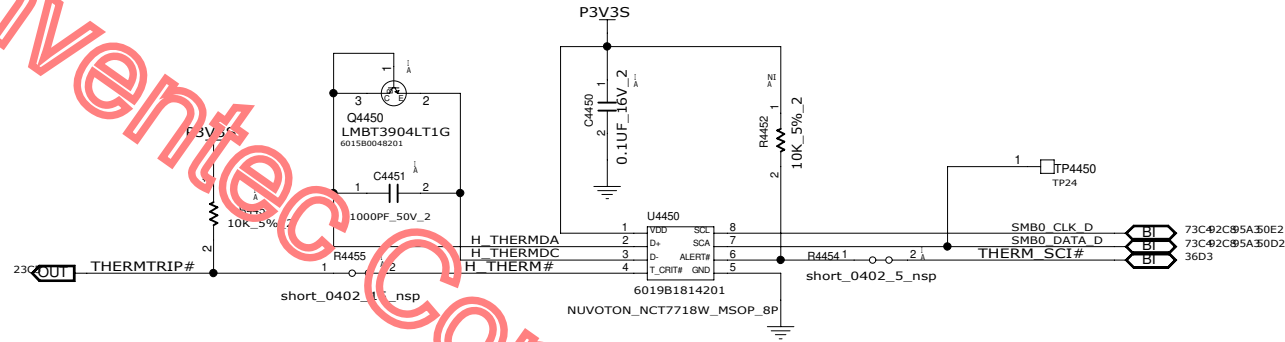
ARGOSY_D4A50_26001_1P52_260P

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
DDR4 SO DIMM1			
SIZE A3		DOC NUMBER	REV
CODE CS		1310xxxxx-0-0	X01
SHEET		48 of 139	

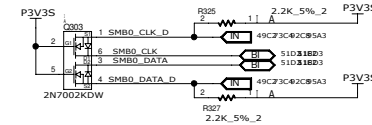
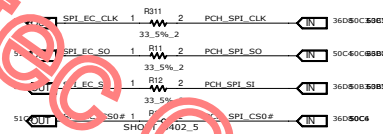
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

THERM SENSOR

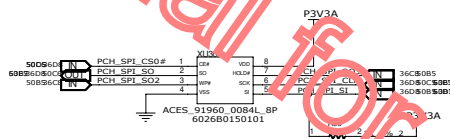
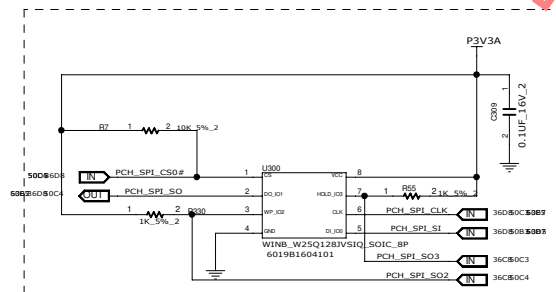


AS	CS		
SHEET		49	of 139

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THERMAL SENSOR
HDMI
DP



INVENTEC			
MODEL PROJECT FUNCTION Block Diagram			
CHANGE D	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX
SIZE A3	CODE CS	DOC NUMBER	1310xxxxx-0-0
SHEET		SD	139
		REV	X01

Location 300 ~ 389
2013EE1B
Ver.05 20120824



Block Diagram

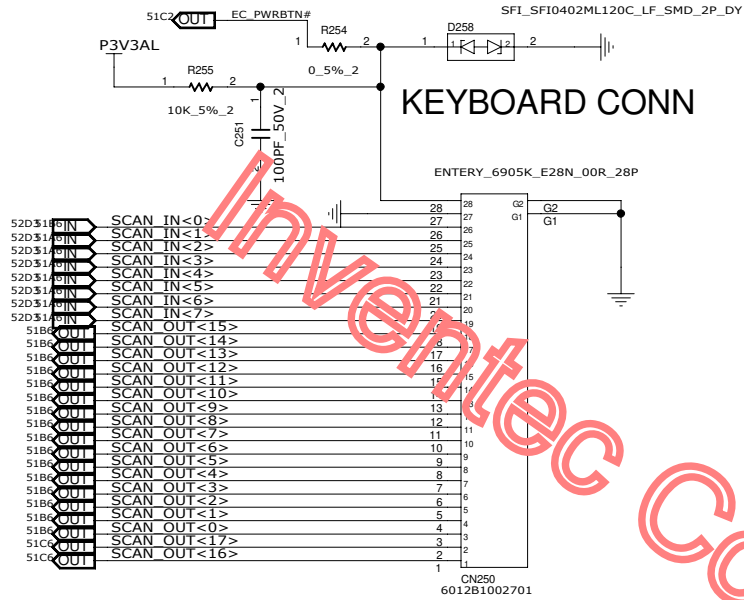
SIZE	CODE	DOC. NUMBER
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A3	CS	1310xxxxx-0-0
SHEET		51 of 139

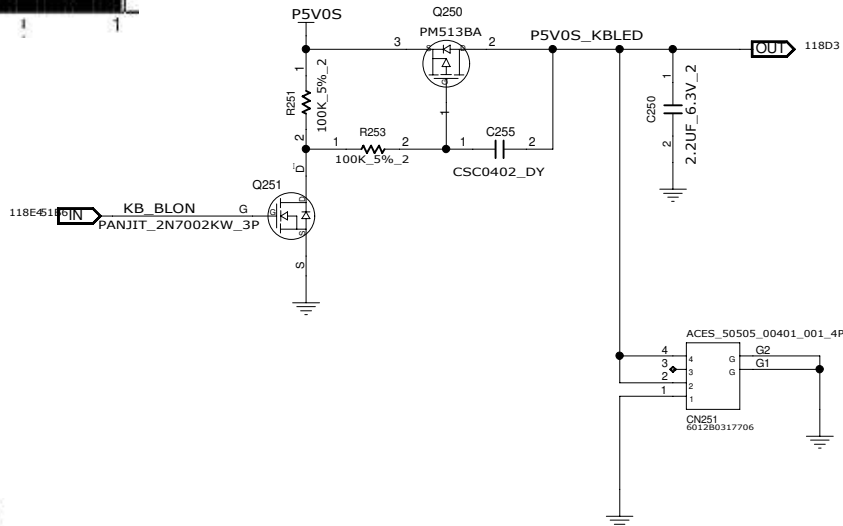
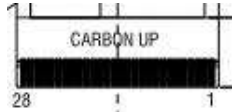
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WWW.ALISALER.COM

REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



NEE TO CHANGE 6012B1002701
5/2 REVERSE

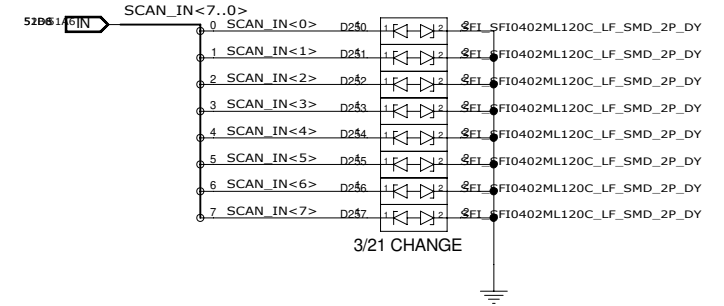


KEYBOARD LED CONN

VCC : 45V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

	14*
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



INVENTEC

TITLE MODEL,PROJECT,FUNCTION
Block Diagram

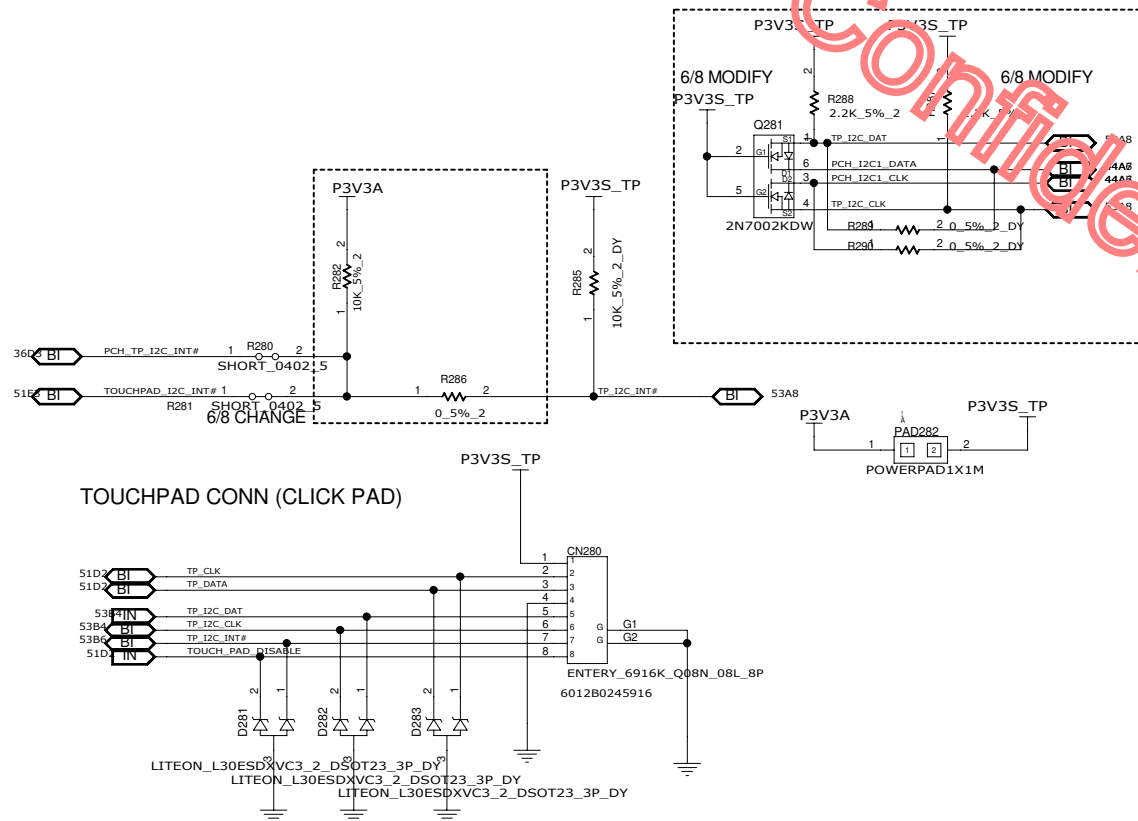
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CHANGE by XXX
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

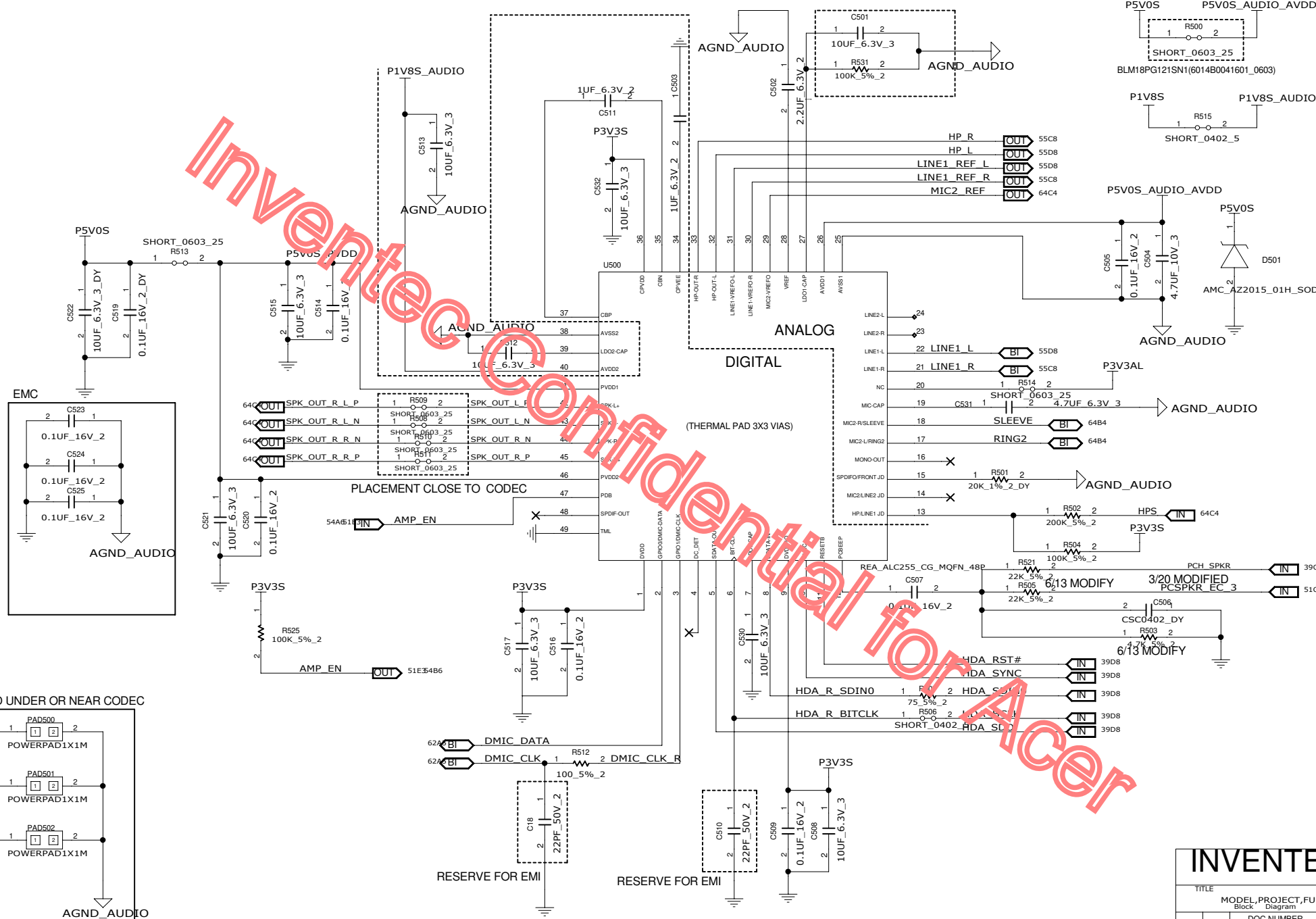
SHEET 52 of 139

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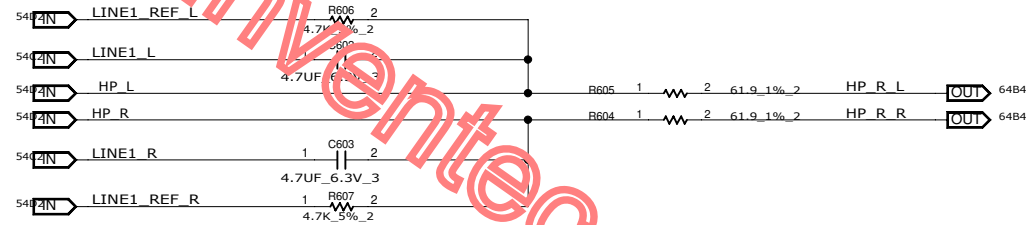
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TITLE				
MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxxx-0-0	X01	
SHEET 53 of 139				

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



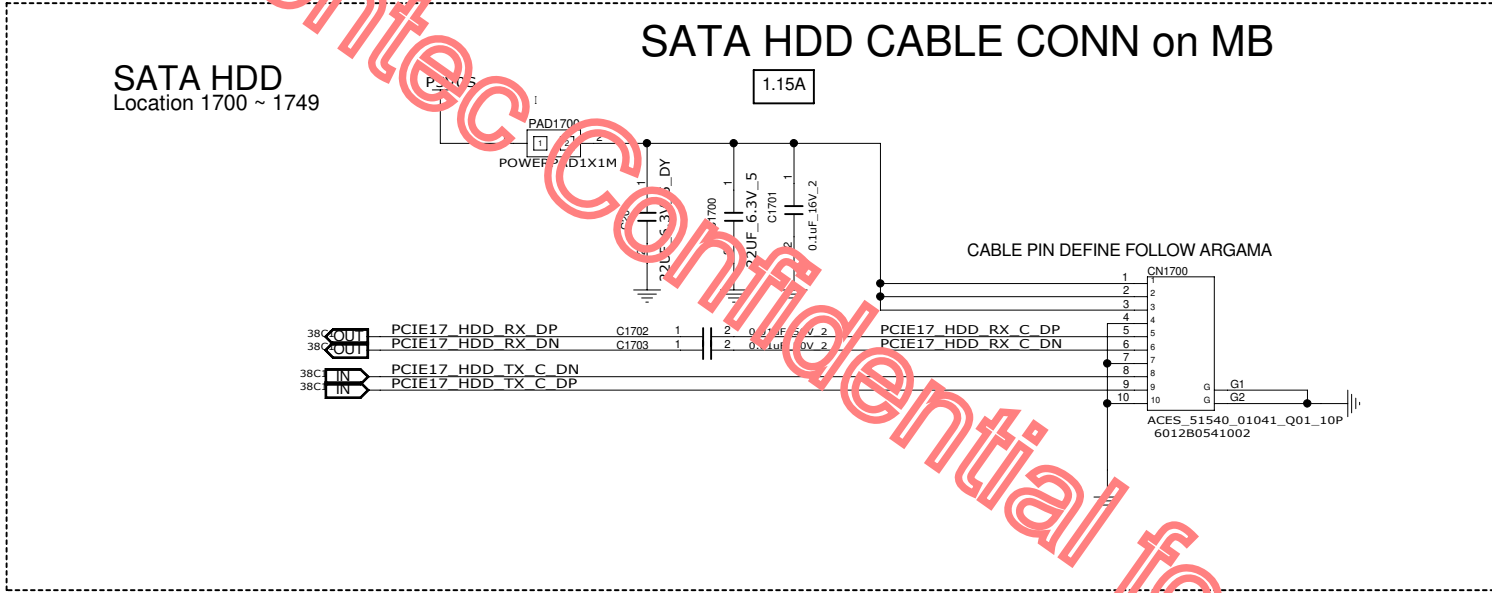
INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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SHEET 55 of 139

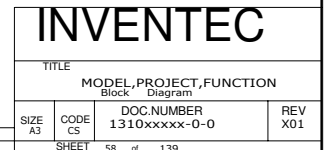


INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
SHEET		56 of 139	1

D
C
B
A



D
C
B
A



The schematic diagram illustrates the electrical connections for the SSD2 SATA LED# and SSD2 WAKE# signals. The central component is the CN1900 (6026B0436901-001) connector, which is connected to the SSD2 SATA LED# signal. The SSD2 SATA LED# signal is connected to the ITP1902 component. The SSD2 WAKE# signal is connected to the ITP1903 component. The diagram also shows the connection of the SSD2 WAKE# signal to the ITP1903 component. The diagram includes a large red watermark 'Inventec Confidential for Acer'.

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION SATA HDD CONN.			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		50 of 130	

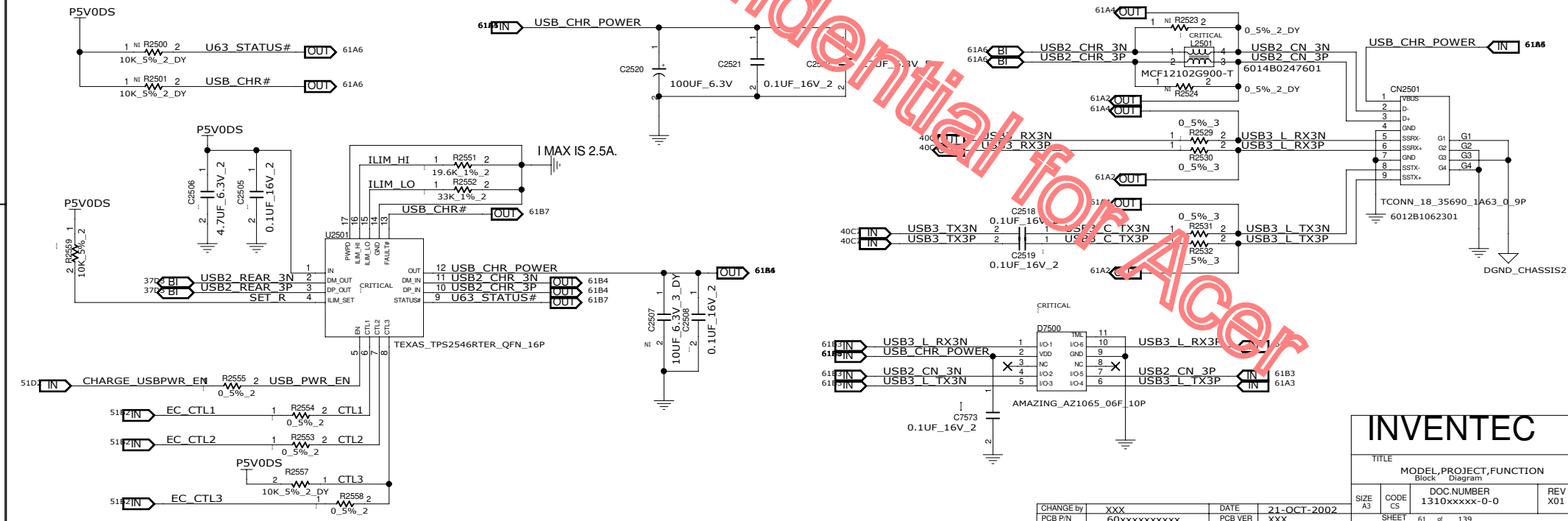
CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCR P/N	60xxxxxxxxxx	PCR V/R	YYY			SHEET		50 of 130	



CHANGE by	XXX
PCB P/N	60xxxxxxxxxxxx

USB CHARGER

USB Faster Charger in S4/S5	USB Charger controller: TI2546	Ctrl.Pin (CTL1/CTL2/CTL3/ILIM_SEL)	Mode	ILIM	Note
Enable	S0	1/1/1/1	CDP	ILIM=2510mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
Disable	S0	1/1/1/1	CDP	ILIM=1525mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/0/0	Turn off switch	ILIM=1525mA	No support charger



INVENTEC

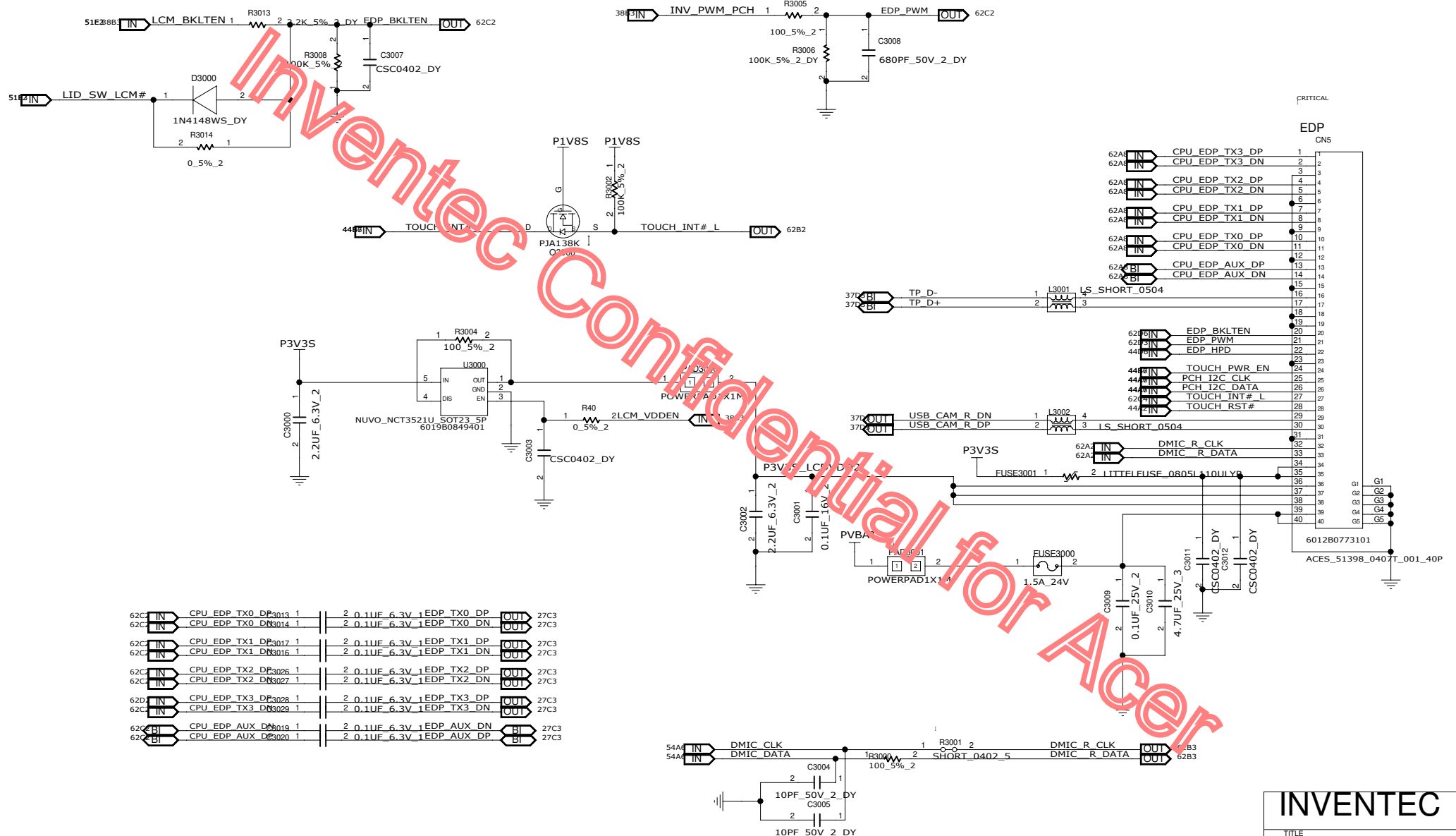
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		61 of 139	

CHANGE by: XXX
PCB P/N: 60xxxxxxxxxx

DATE: 21-OCT-2002
PCB VER: XXX

REFERENCE 3000~3049(LCM)

EDP CONN



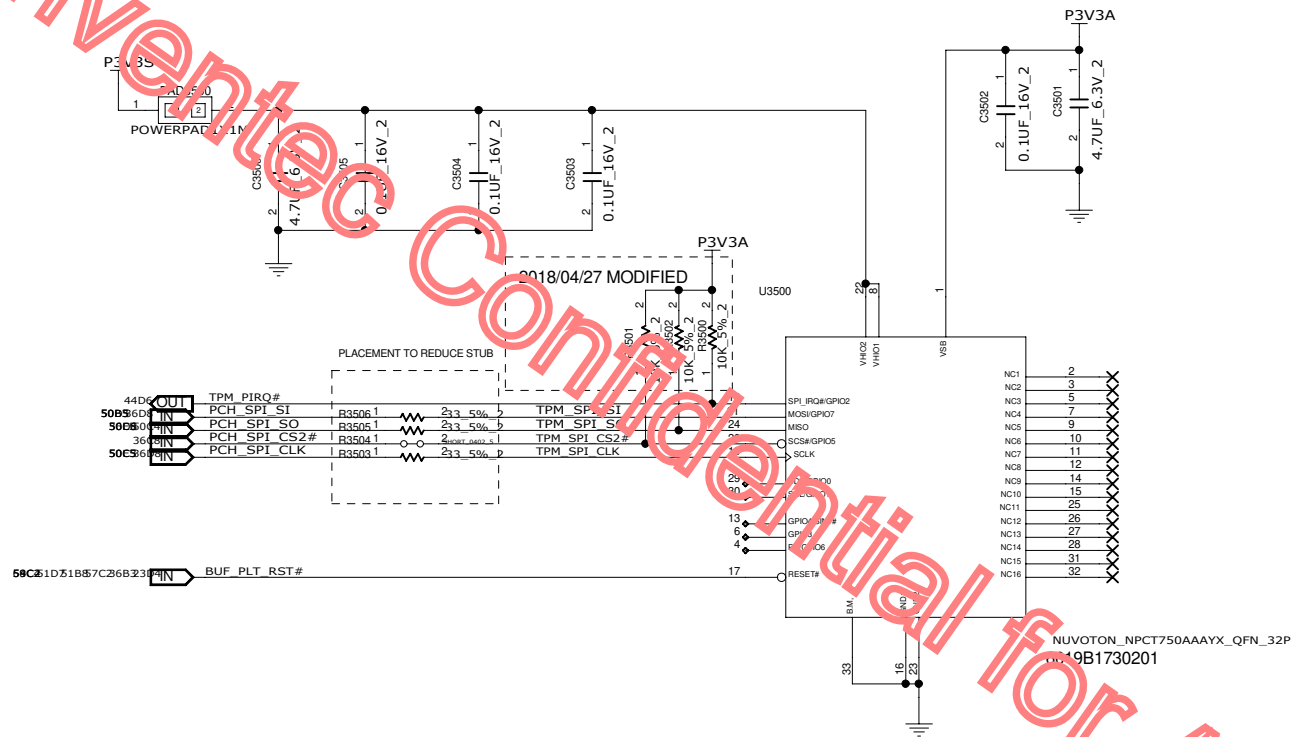
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

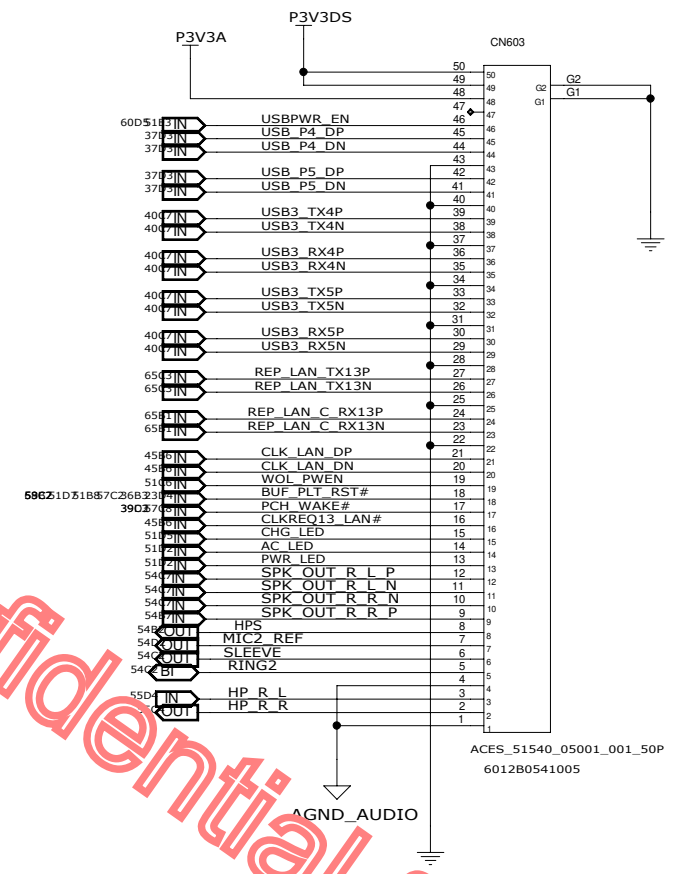
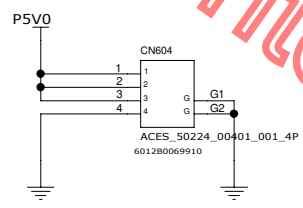
SHEET 62 of 139

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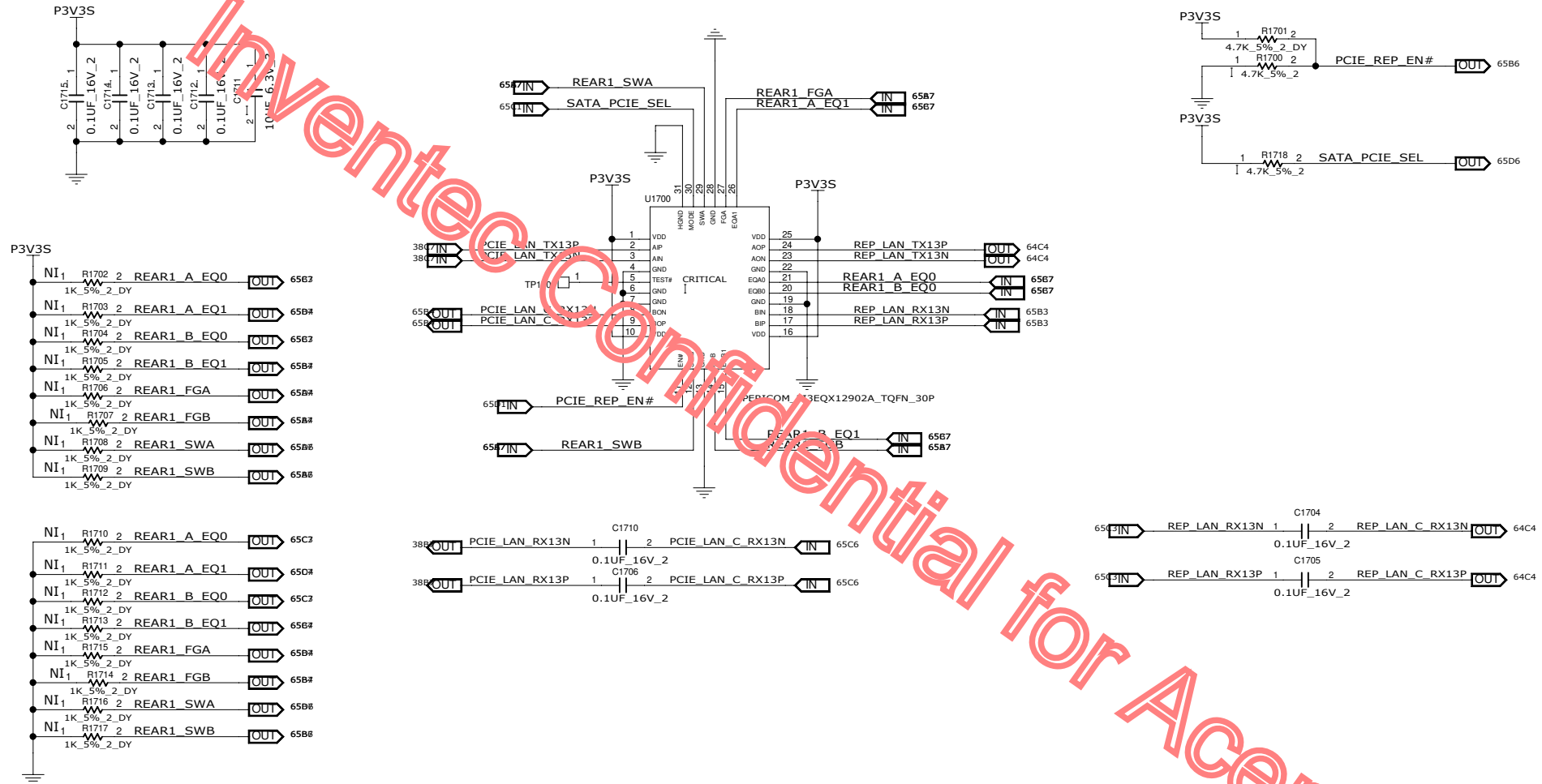
INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	
CHANGE by		DATE	21-OCT-2002	
PCB P/N		PCB VER	XXX	
SHEET		63 of 139	1	

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INVENTEC				
TITLE MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 64 of 139

PCIE REPEATER



INVENTEC

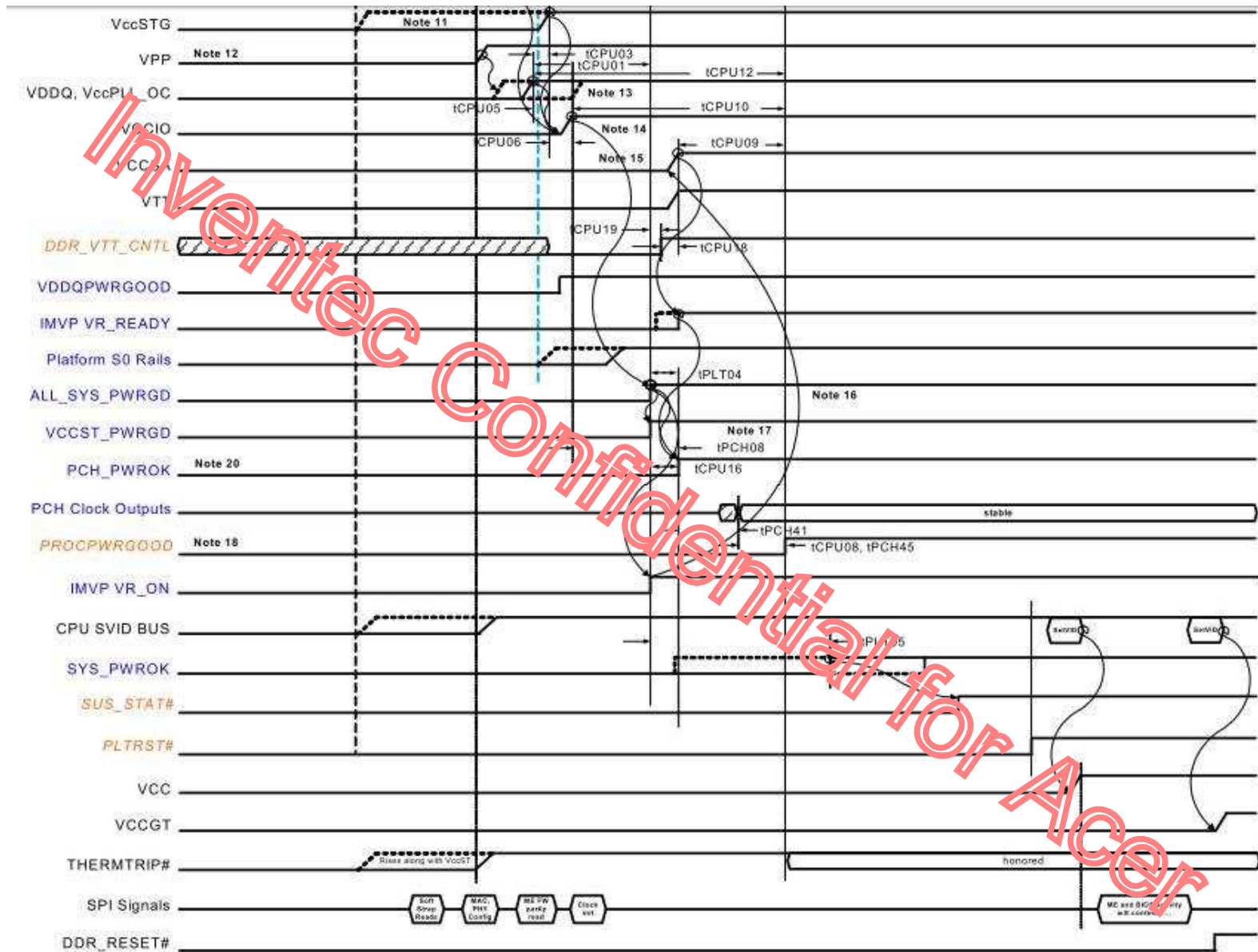
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxxx

DATE 21-OCT-2002
PCB VER XXX

SHEET 65 of 139



D

C

B

A

D

C

B

A

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		67 of 139	1

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8		7		6		5		4		3		2		1	
D															
C															
B															
A															

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INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 68 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8		7		6		5		4		3		2		1	
D															
C															
B															
A															

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INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 69 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8		7		6		5		4		3		2		1	
D															
C															
B															
A															

8	7	6	5	4	3	2	1
D							
C							
B							
A							

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N18E-G0
N18E-G1
N18E-G2 MAX-Q
8GB DDR5 256M X 16 X 2 X6

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 71 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

PCA CODE NAME : N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001

G1 : 6019B1849201

G2 MAXQ:6019B1849301

PCB VERSION : X01

BOARD SIZE:

SCH P/N:

PCB P/N:

PCA P/N:

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL

NI: NON-INSTALL

DY: NON-INSTALL

MP: PRODUCTION

PROTO: PRE-PRODUCTION

CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14
6019B1847701

MICRON MT61K256M32JE-14:A
6019B1847701

SHEET	CONTENT	SHEET	CONTENT
71	TITLE	101	GPU 1V8_AON DECOUPLING
72	INDEX	102	GPU NVDD DECOUPLING
73	VGA CONNECTION WITH MONITOR BOARD	103	GPU FBVDD DECOUPLING
74	GPU PCI-E GEN3 X 16	104	GPU GND
75	GPU MEMORY PARTITION A	105	GPU POWER SEQUENCE
76	GPU MEMORY PARTITION B	106	GPU POWER DISCHARGE
77	GPU MEMORY PARTITION C	107	GPU 1V8_MAIN
78	GPU MEMORY PARTITION D	108	GPU NVVDD/NVVDDS (MP2886A)
79	GPU MEMORY FBA PARTITION 31-0	109	PVCORE_DGPU (MP86941_1-2P)
80	GPU MEMORY FBA PARTITION 63-32	110	PVCORE_DGPU (MP86941_3-4P)
81	GPU MEMORY FBB PARTITION 31-0	111	PVCORE_DGPU (MP86941_5-6P)
82	GPU MEMORY FBB PARTITION 63-32	112	P1V35S_DGPU (MP86941_2P)
83	GPU MEMORY FBC PARTITION 31-0	113	P1V0S_DGPU (MP86941)
84	GPU MEMORY FBC PARTITION 63-32	114	P1V8S_DGPU (R18158A)
85	GPU MEMORY FBD PARTITION 31-0	115	NOTES
86	GPU MEMORY FBD PARTITION 63-32	116	HISTORY
87	GPU 27 MHZ XTAL	117	
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90	GPU IFP_AB	120	
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92	GPU DP REDRIVER PI3DPX1203ZHEX	122	
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100	GPU FBVDD	130	

INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET	72	of	139				

CONNECTION TO MAINBOARD

74D75C	IN	CLK_PCIE_DGPU_100MHZ_P	OUT
74D75C	IN	CLK_PCIE_DGPU_100MHZ_N	OUT
26B74D	OUT	PCIE_DGPU_RX15P	OUT
26B74D	OUT	PCIE_DGPU_RX15N	OUT
74D26B	IN	PCIE_DGPU_TX15P	OUT
74D26B	IN	PCIE_DGPU_TX15N	OUT
26B74D	OUT	PCIE_DGPU_RX14P	OUT
26B74D	OUT	PCIE_DGPU_RX14N	OUT
74D26B	IN	PCIE_DGPU_TX14P	OUT
74D26B	IN	PCIE_DGPU_TX14N	OUT
26B74D	OUT	PCIE_DGPU_RX13P	OUT
26B74D	OUT	PCIE_DGPU_RX13N	OUT
74D26B	IN	PCIE_DGPU_TX13P	OUT
74D26B	IN	PCIE_DGPU_TX13N	OUT
26B74D	OUT	PCIE_DGPU_RX12P	OUT
26B74D	OUT	PCIE_DGPU_RX12N	OUT
74D26B	IN	PCIE_DGPU_TX12P	OUT
74C26B	IN	PCIE_DGPU_TX12N	OUT
26B74C	OUT	PCIE_DGPU_RX11P	OUT
26B74C	OUT	PCIE_DGPU_RX11N	OUT
74C26B	IN	PCIE_DGPU_TX11P	OUT
74C26B	IN	PCIE_DGPU_TX11N	OUT
26B74C	OUT	PCIE_DGPU_RX10P	OUT
26B74C	OUT	PCIE_DGPU_RX10N	OUT
74C26B	IN	PCIE_DGPU_TX10P	OUT
74C26B	IN	PCIE_DGPU_TX10N	OUT
26C74C	OUT	PCIE_DGPU_RX9P	OUT
26C74C	OUT	PCIE_DGPU_RX9N	OUT
74C26B	IN	PCIE_DGPU_TX9P	OUT
74C26B	IN	PCIE_DGPU_TX9N	OUT
26C74C	OUT	PCIE_DGPU_RX8P	OUT
26C74C	OUT	PCIE_DGPU_RX8N	OUT
74C26B	IN	PCIE_DGPU_TX8P	OUT
74C26B	IN	PCIE_DGPU_TX8N	OUT
26C74C	OUT	PCIE_DGPU_RX7P	OUT
26C74C	OUT	PCIE_DGPU_RX7N	OUT
74B26B	IN	PCIE_DGPU_TX7P	OUT
74B26B	IN	PCIE_DGPU_TX7N	OUT
26C74B	OUT	PCIE_DGPU_RX6P	OUT
26C74B	OUT	PCIE_DGPU_RX6N	OUT
74B26B	IN	PCIE_DGPU_TX6P	OUT
74B26B	IN	PCIE_DGPU_TX6N	OUT
26C74B	OUT	PCIE_DGPU_RX5P	OUT
26C74B	OUT	PCIE_DGPU_RX5N	OUT
74B26B	IN	PCIE_DGPU_TX5P	OUT
74B26B	IN	PCIE_DGPU_TX5N	OUT
26C74B	OUT	PCIE_DGPU_RX4P	OUT
26C74B	OUT	PCIE_DGPU_RX4N	OUT
74B26B	IN	PCIE_DGPU_TX4P	OUT
74B26B	IN	PCIE_DGPU_TX4N	OUT
26C74B	OUT	PCIE_DGPU_RX3P	OUT
26C74B	OUT	PCIE_DGPU_RX3N	OUT
74B26B	IN	PCIE_DGPU_TX3P	OUT
74B26B	IN	PCIE_DGPU_TX3N	OUT
26C74A	OUT	PCIE_DGPU_RX2P	OUT
26C74A	OUT	PCIE_DGPU_RX2N	OUT
74A26B	IN	PCIE_DGPU_TX2P	OUT
74A26B	IN	PCIE_DGPU_TX2N	OUT
26D74A	OUT	PCIE_DGPU_RX1P	OUT
26D74A	OUT	PCIE_DGPU_RX1N	OUT
74A26B	IN	PCIE_DGPU_TX1P	OUT
74A26B	IN	PCIE_DGPU_TX1N	OUT
26D74A	OUT	PCIE_DGPU_RX0P	OUT
26D74A	OUT	PCIE_DGPU_RX0N	OUT
74A26B	IN	PCIE_DGPU_TX0P	OUT
74A26B	IN	PCIE_DGPU_TX0N	OUT

105B403D41D84D IN DGPU_PWR_EN OUT

GPU PWR ENABLE COME FROM PCH/EC
MAKE SURE 10K P3V3S PULL UP

74F86B IN PCH_PLTRST#_BUF OUT

PCH PLATFORM RESET#
MAKE SURE 100K PULL TO GND

74F814A IN IRMT_HOLD_RST# OUT

PCH HOLD RESET#
MAKE SURE 100K PULL TO GND

TO PCH

GPU_EVENT_PCH# OUT

GPU EVENT FOR GPU WILL EXIT GC6 MODS

89E51C IN DGPU_PWRLE_1L OUT

15.3.2 PWR_LEVEL* (GPIO12)

The **PWR_LEVEL** input signal triggers an immediate low-to-high or slow-to-high transition followed by the driver capping the GPU power state to the appropriate limit. There are a few events that can trigger this signal assertion: AC to battery power transition, total system power overdraw event.

45C74E8 OUT PEX_CLKREQ# IN

PCIE CLK REQUESTD#

51D8 105A OUT ALL_POWER_GOOD IN

GPU ALL S RAIL GOOD
MAKE SURE 10K P3V3S PULL UP

93A54A OUT DP_MA_HPD# IN

DP HPD TO MAINBOARD

MAKE SURE 10K P3V3S PULL UP

50D295A32C873C49C SMB0_DATA_D BI

50E295A32C873C49C SMB0_CLK_D BI

DP REDRIVER I2C CONNECT TO MOBARD
MAINBOARD NEED TO PULL UP

95A54A OUT HDMI_MB_HPD# IN

HDMI HPD TO MB

98B8 50E295A32C873C49C SMB0_DATA_D BI

50E295A32C873C49C SMB0_CLK_D BI

HDMI RETIMER I2C TO MB
MAINBOARD NEED TO PULL UP

GPU_OVERT_EC# IN

GPU OVERT TEMPERATURE TO PCH OR EC

105B414C89B8 OUT GC6_EN_PCH IN

3.3V LEVEL
GC6 ENABLE SIGNAL TO PCH OR EC

EC

89E51C BI EC_SMBDATA0 BI

89E51C BI EC_SMBCLK0 BI

GPU I2C, COMMUNICATED WITH EC
THIS SIGNAL REQUIRE AN EXTERNAL PULL UP

INVENTEC

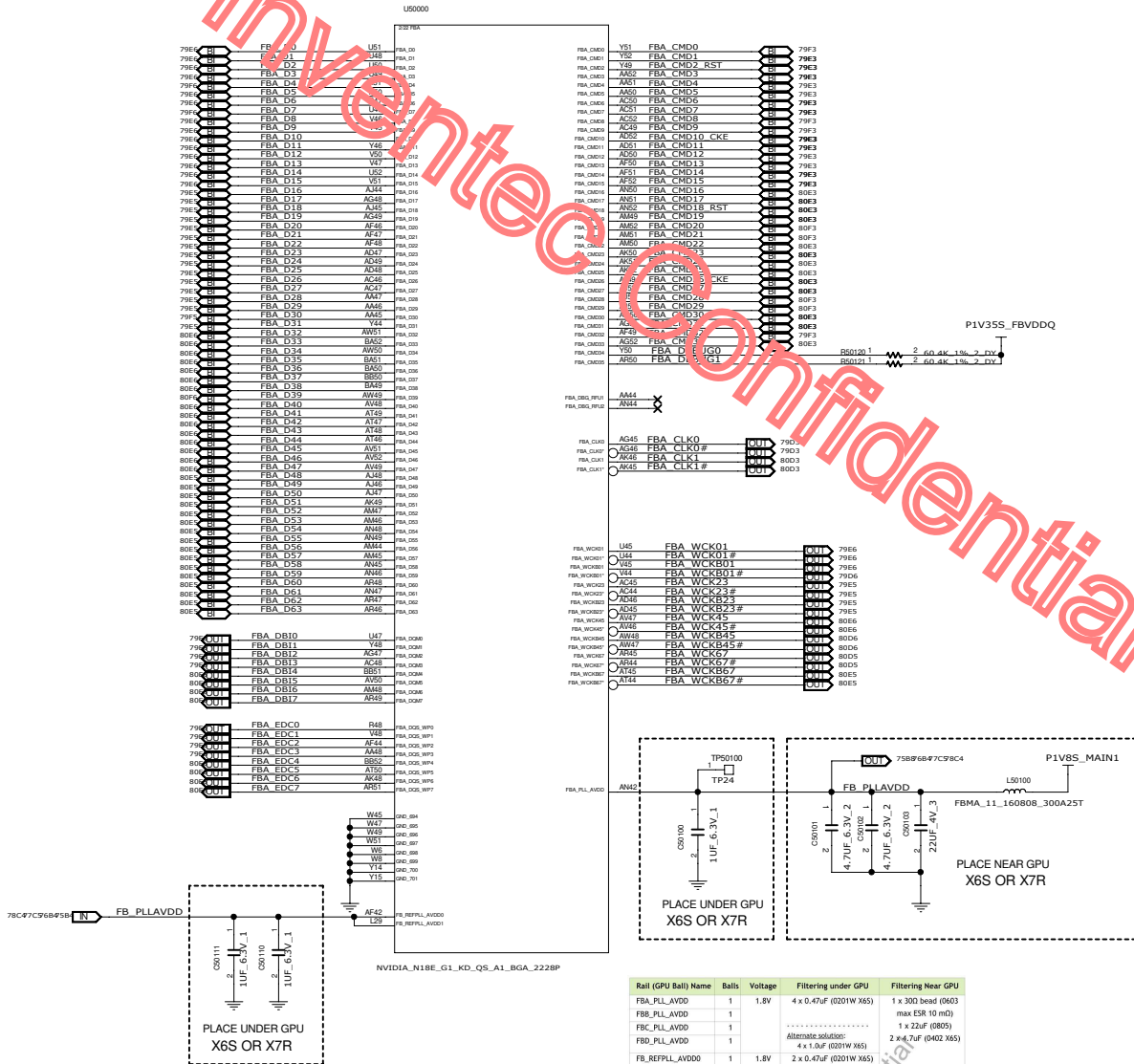
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 73 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1			2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 x 22uF (0805)
FBC_PLL_AVDD	1		Alternate solution: 4 x 1.0uF (0201W X6S)	2 x 4.7uF (0402 X6S)
FBD_PLL_AVDD	1			
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1		Alternate solution: 2 x 1.0uF (0201W X6S)	

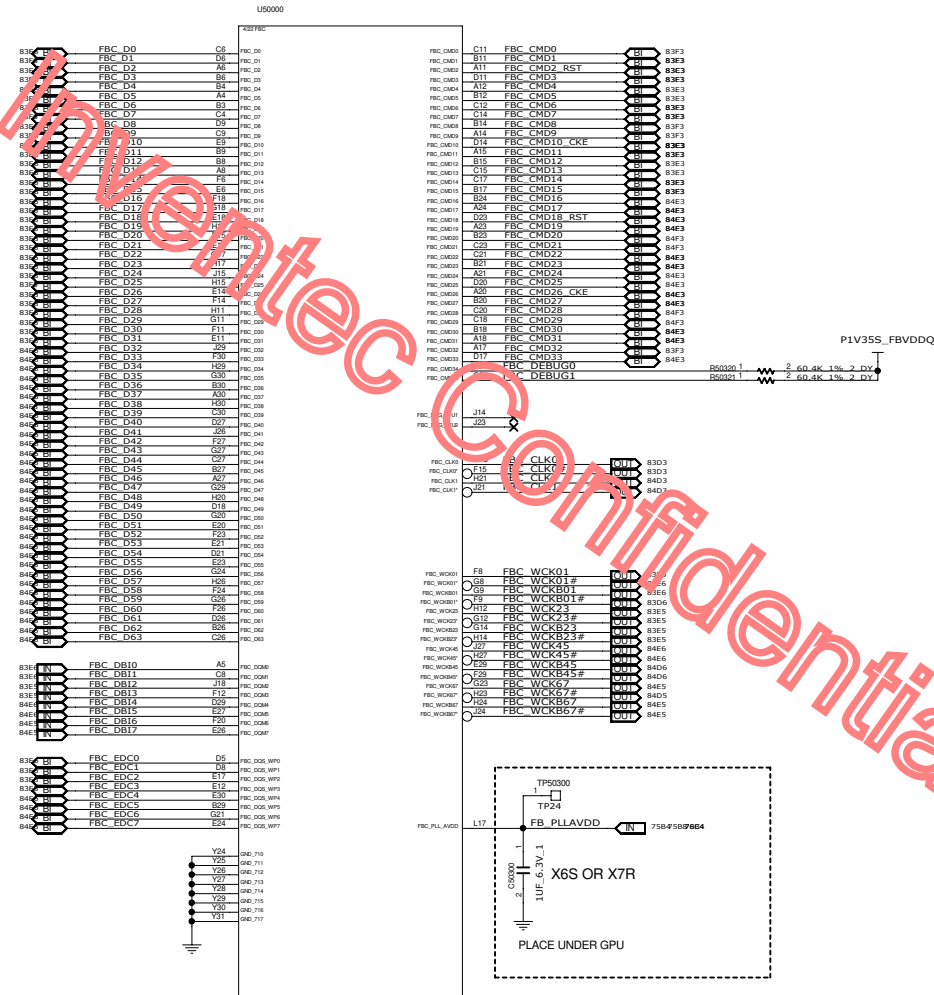
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MODEL, PROJECT, FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	C5	1310xxxxx-0-0	X01
CHANGE D1		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
SHEET		75	139
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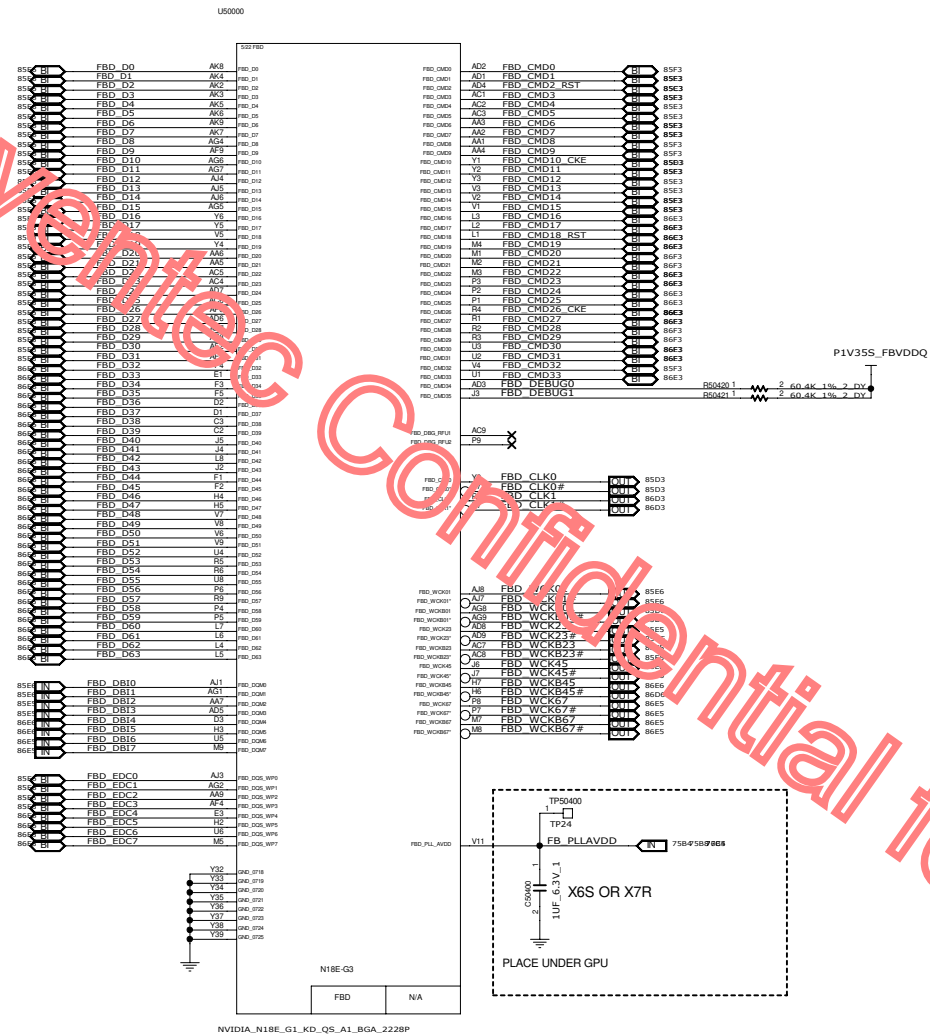
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TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxxx-0-0	REV X01
SHEET		76 of 179	

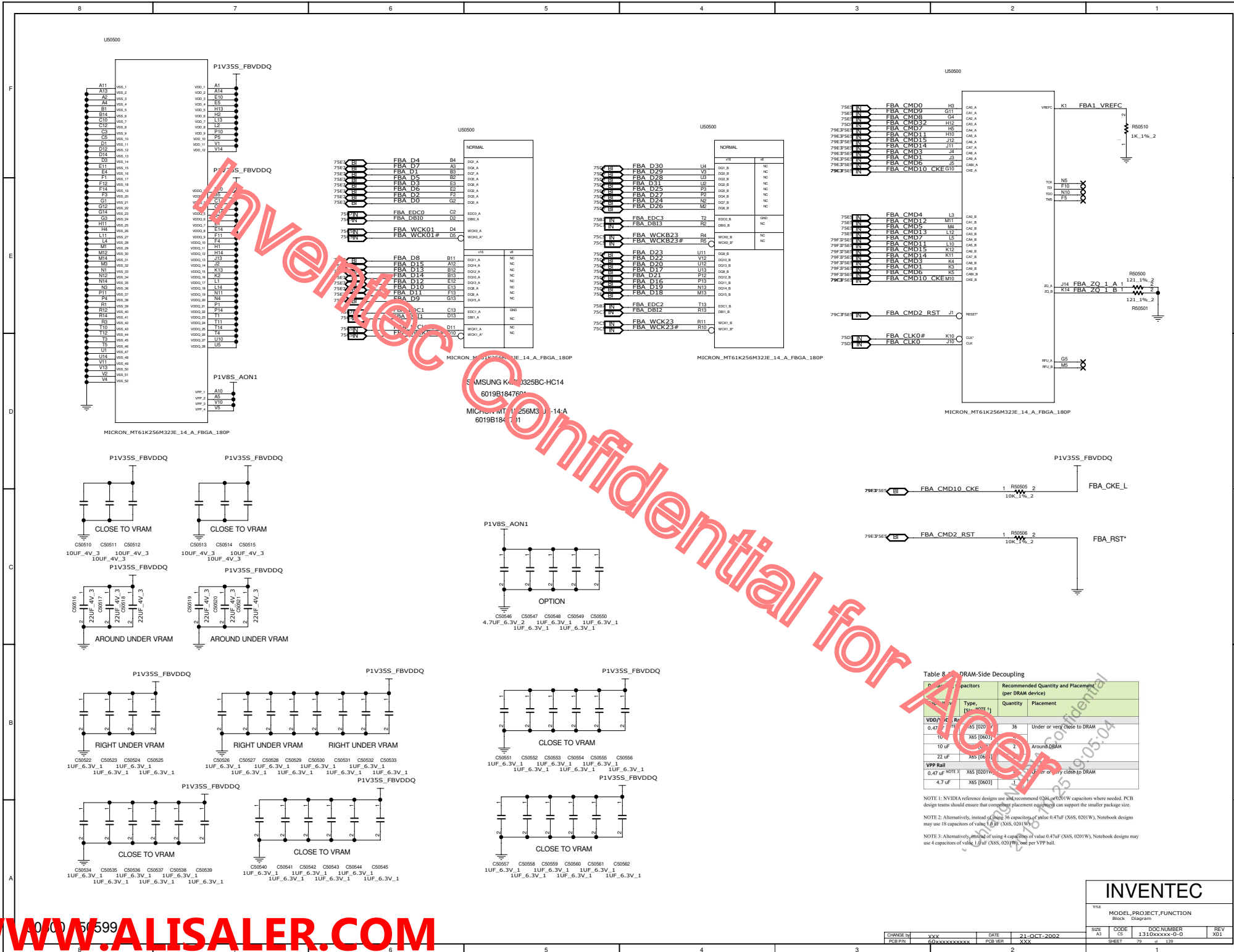
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 76 of 139			
2				1			

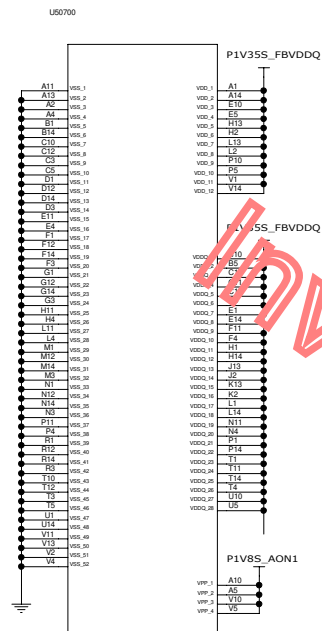
GPU FRAME BUFFER C



GPU FRAME BUFFER D

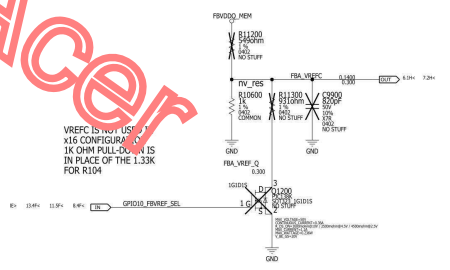
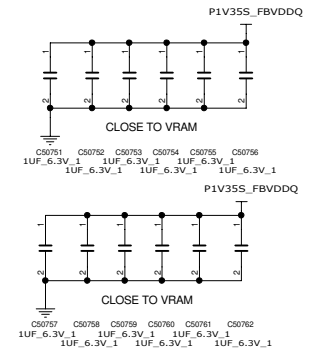
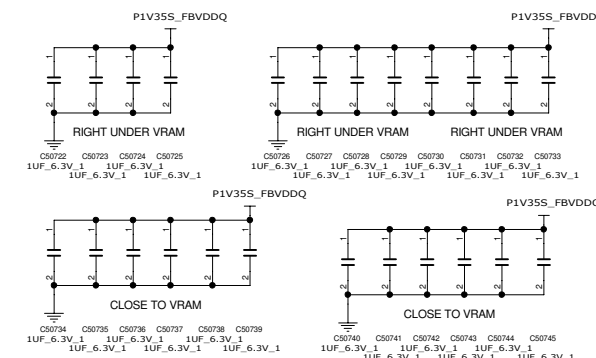
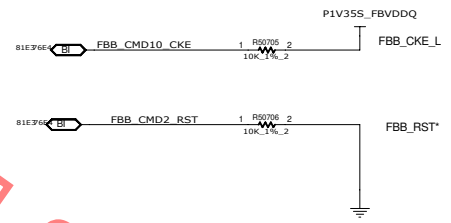
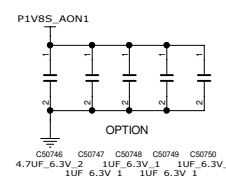
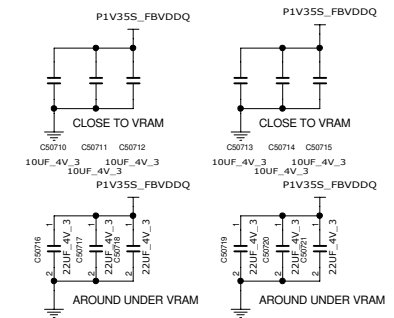
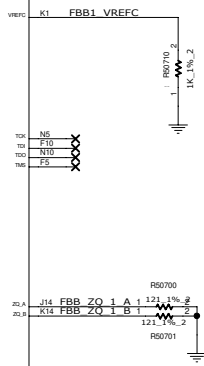
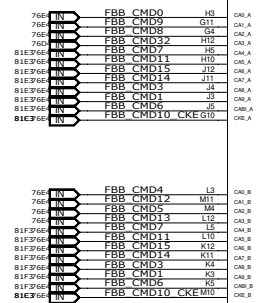
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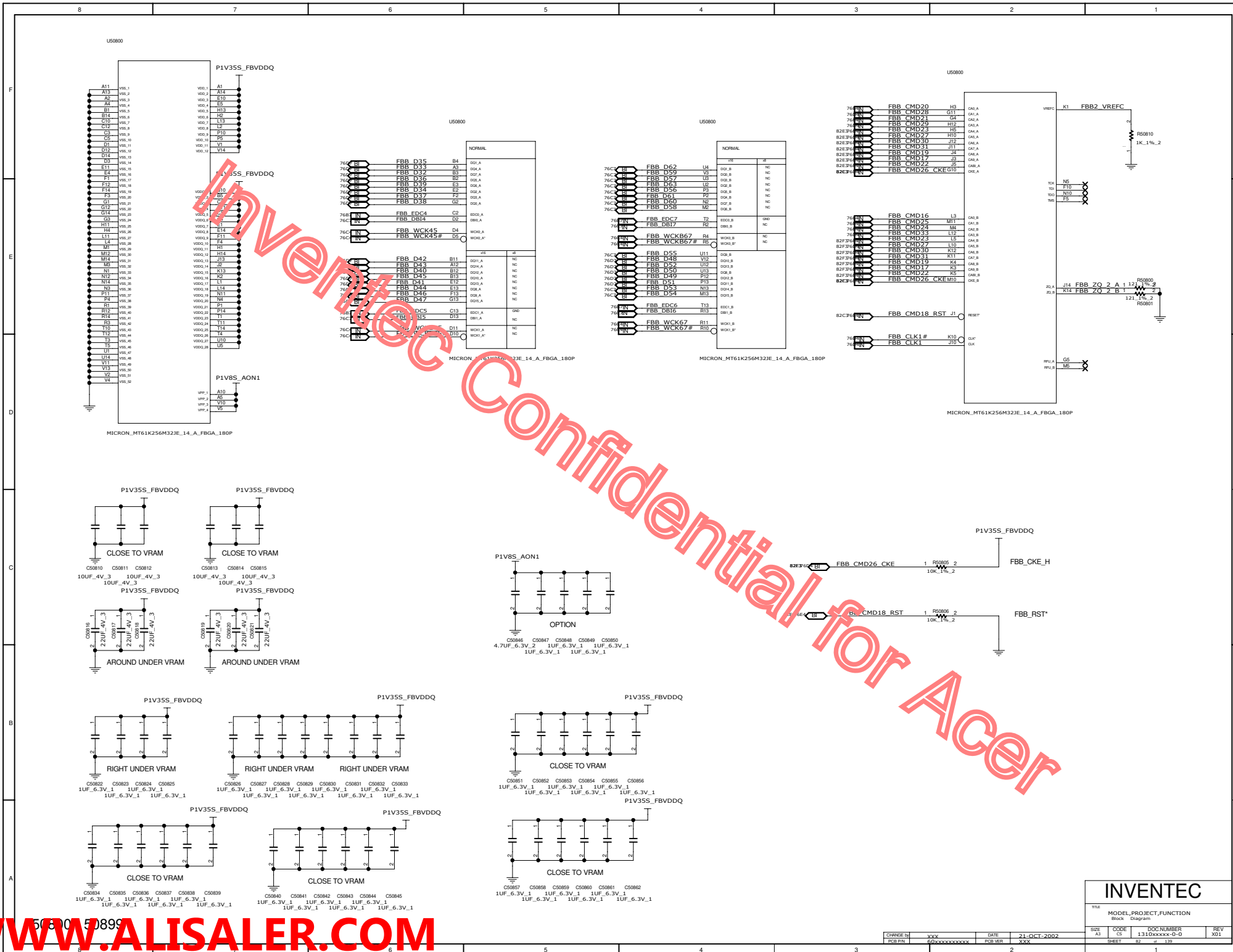




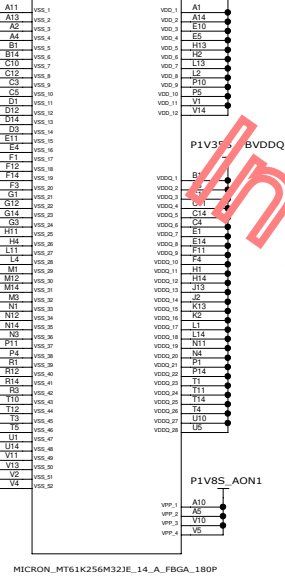
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766	IN	FBB D4	B1
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766	IN	FBB D97	B0
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766	IN	FBB D100	A0

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766	IN	FBB D29	U2
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766	IN	FBB D60	U2
766	IN	FBB D61	U2
766	IN	FBB D62	U2
766	IN	FBB D63	U2
766	IN	FBB D64	U2
766	IN	FBB D65	U2
766	IN	FBB D66	U2
766	IN	FBB D67	U2
766	IN	FBB D68	U2
766	IN	FBB D69	U2
766	IN	FBB D70	U2
766	IN	FBB D71	U2
766	IN	FBB D72	U2
766	IN	FBB D73	U2
766	IN	FBB D74	U2
766	IN	FBB D75	U2
766	IN	FBB D76	U2
766	IN	FBB D77	U2
766	IN	FBB D78	U2
766	IN	FBB D79	U2
766	IN	FBB D80	U2
766	IN	FBB D81	U2
766	IN	FBB D82	U2
766	IN	FBB D83	U2
766	IN	FBB D84	U2
766	IN	FBB D85	U2
766	IN	FBB D86	U2
766	IN	FBB D87	U2
766	IN	FBB D88	U2
766	IN	FBB D89	U2
766	IN	FBB D90	U2
766	IN	FBB D91	U2
766	IN	FBB D92	U2
766	IN	FBB D93	U2
766	IN	FBB D94	U2
766	IN	FBB D95	U2
766	IN	FBB D96	U2
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766	IN	FBB D98	U2
766	IN	FBB D99	U2
766	IN	FBB D100	U2

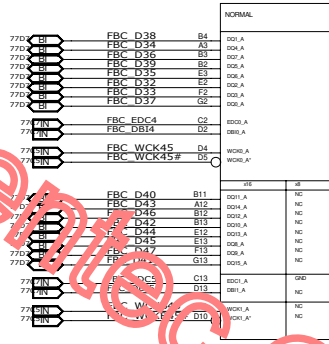




U51000

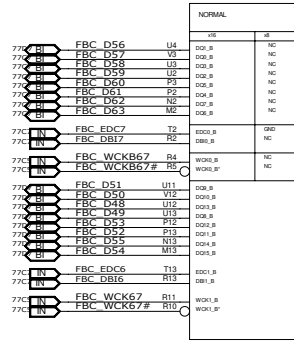


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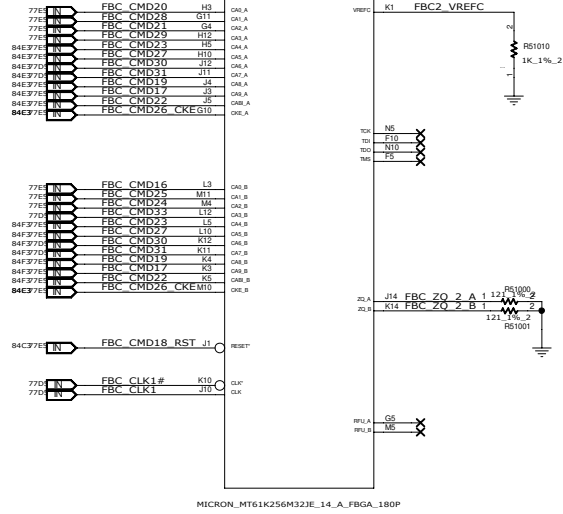
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U51000



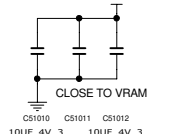
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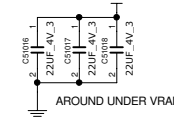


MICRON_MT61K256M32JE_14_A_FBGA_180P

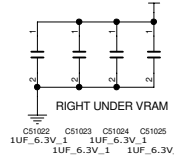
P1V35S_FBVDQ



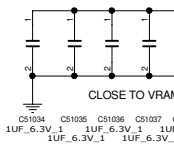
P1V35S_FBVDQ



P1V35S_FBVDQ



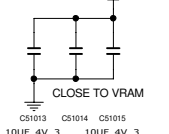
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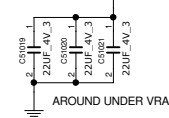
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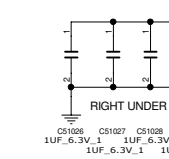
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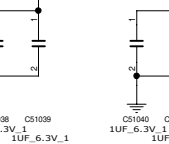
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P1V35S_FBVDQ



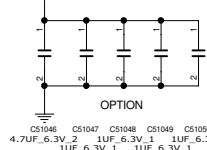
P1V35S_FBVDQ



P1V35S_FBVDQ



P1V8S_AON1



OPTION

4.7uF 6.3V2 1uF 6.3V1 1uF 6.3V1 1uF 6.3V1 1uF 6.3V1

P1V35S_FBVDQ



FBC_CKE_H

10K 1% 2

10K 1% 2

10K 1% 2

10K 1% 2

10K 1% 2

10K 1% 2

10K 1% 2

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10K 1% 2

INVENTEC

MODEL PROJECT,FUNCTION

Block Diagram

SIZE A3 CODE C5 DOC NUMBER 1310xxxxx-0-0 REV X01

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1

CHANGE D1 XXXX

PCB P/N XXXXXXXXXXXXX

DATE 21-OCT-2002

PCB VER XXX

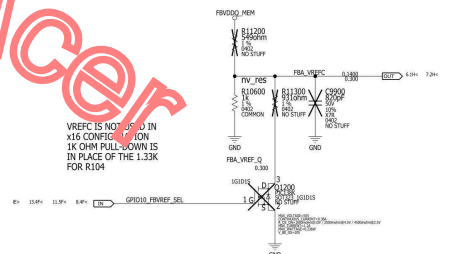
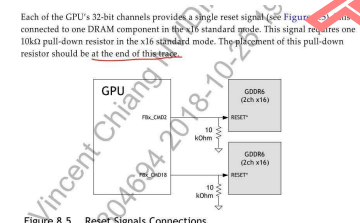
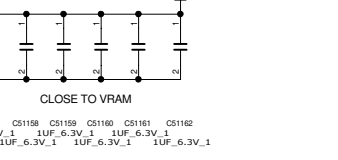
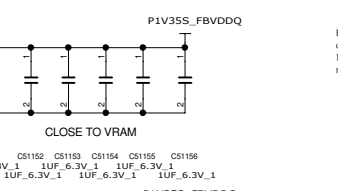
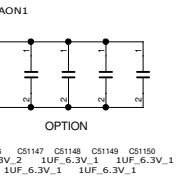
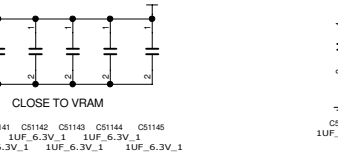
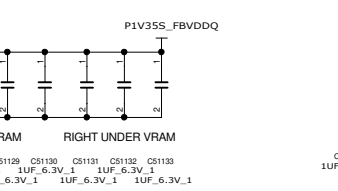
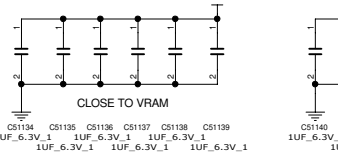
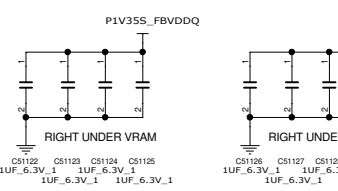
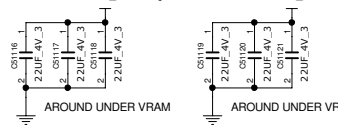
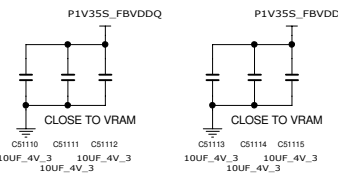
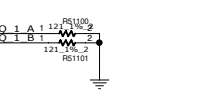
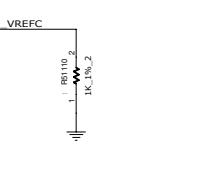
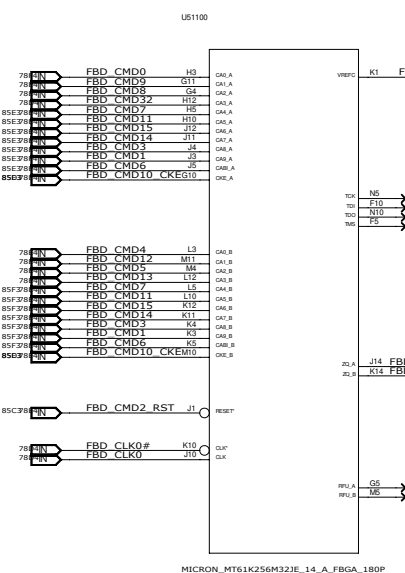
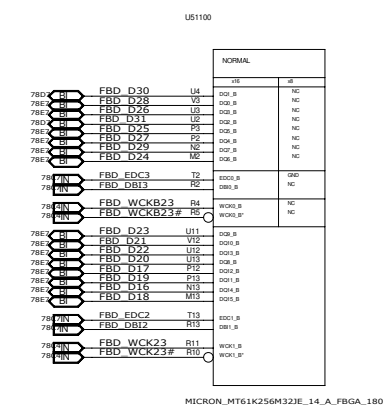
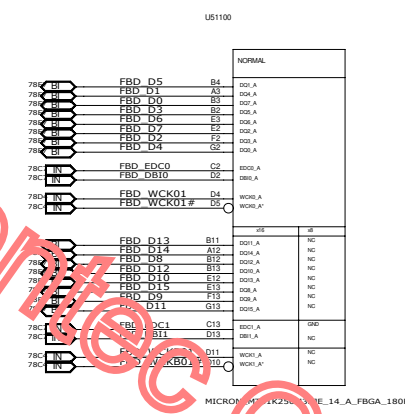
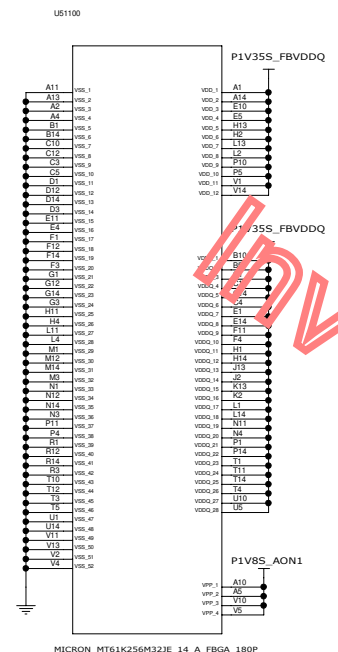


Figure 8.5 Reset Signals Connections

27 MHZ XTAL

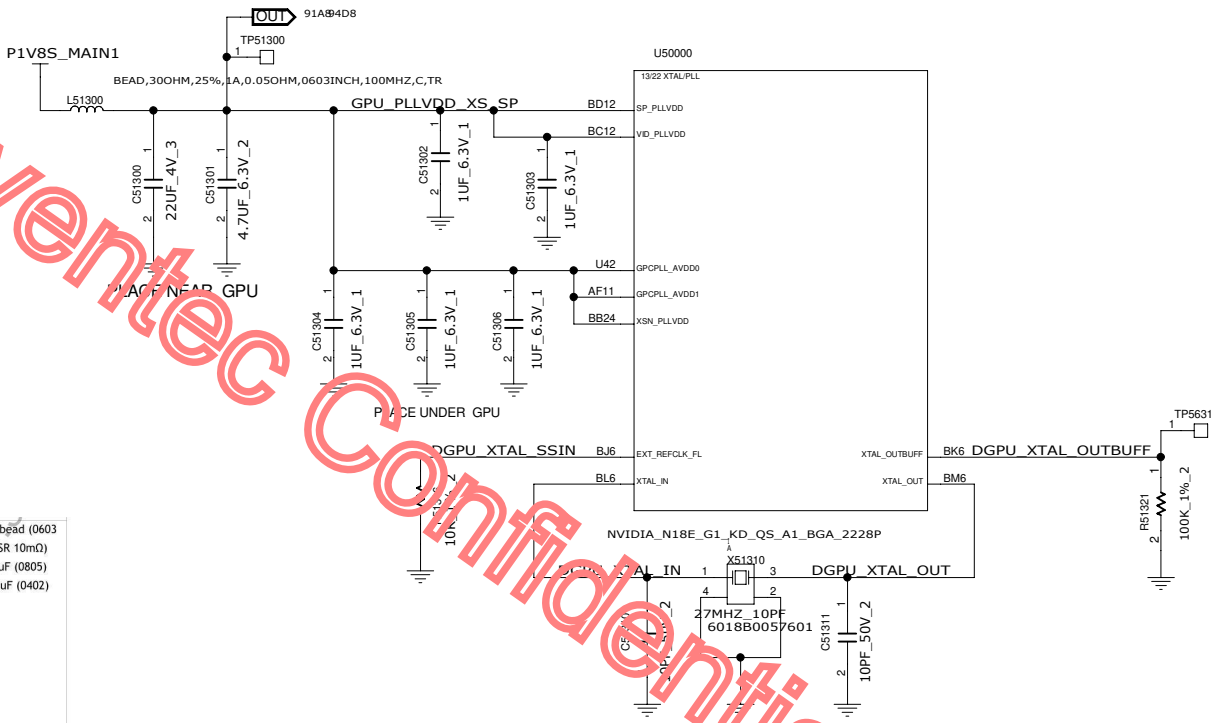
CL=2*10-(5+3)=12

CL_trim = 2 * CLoad - (Cstray + C1)

- Where:
- ▶ C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
 - ▶ C_{stray} is 3pF (Stray capacitance of XTAL pads and any significant trace routing)
 - ▶ C₁ is pin capacitance (5 pF)

Typical CL_{trim} = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF.

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X65)	1 x 30Ω bead (0603 max ESR 10mΩ)
IFPCD_PLLVDD	1			
IFPEF_PLLVDD	1			
			Alternate solution:	
			3 x 1.0uF (0201W X65)	1 x 22uF (0805)
GPCPLL_AVDDx	3		3 x 0.47uF (0201W X65)	1 x 4.7uF (0402)
XSN_PLLVDD				
			Alternate solution:	
			3 x 1.0uF (0201W X65)	
SP_PLLVDD	1		1 x 0.47uF (0201W X65)	
			Alternate solution:	
			1 x 1.0uF (0201W X65)	
VID_PLLVDD	1		1 x 0.47uF (0201W X65)	
			Alternate solution:	
			1 x 1.0uF (0201W X65)	



51300 - 51399

GPU VBIOS, EXTERNAL STRAPS

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins see Note	Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL
L	L	L	0	0
L	L	H	0	0
L	H	L	0	0
L	H	H	0	0
H	L	L	0	1
H	L	H	0	1
H	H	L	0	1
H	H	H	0	1
L	L	L	1	0
L	L	H	1	0
L	H	L	1	0
L	H	H	1	0
H	L	L	1	0
H	L	H	1	0
H	H	L	1	0
H	H	H	1	0

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins see Note	Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL
L	L	L	0	0
L	L	H	0	0
L	H	L	0	0
L	H	H	0	0
H	L	L	0	1
H	L	H	0	1
H	H	L	0	1
H	H	H	0	1
L	L	L	1	0
L	L	H	1	0
L	H	L	1	0
L	H	H	1	0
H	L	L	1	0
H	L	H	1	0
H	H	L	1	0
H	H	H	1	0

DEFAULT IS SAMSUNG

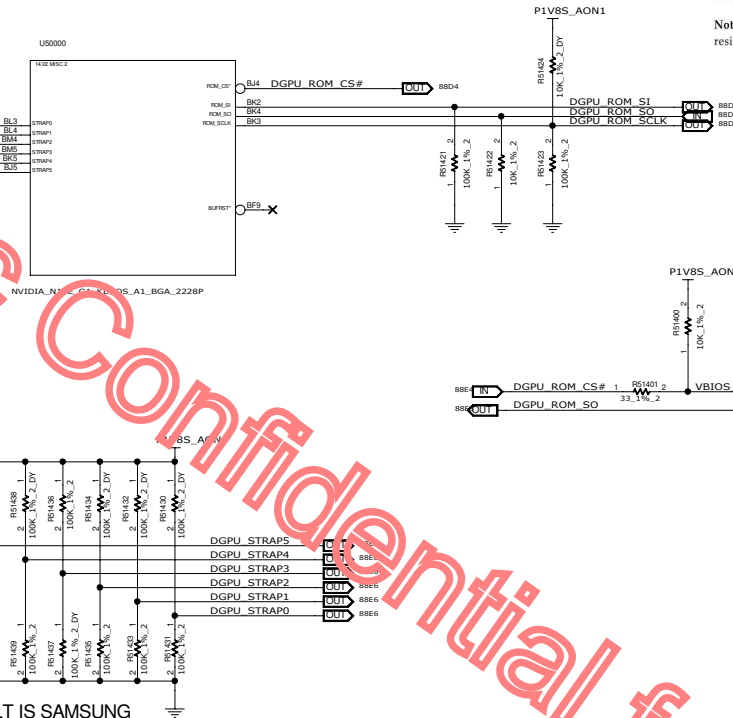
SAMSUNG K4Z80325BC-HC14
6019B1847601
STRAP 0X0=000
SAMSUNG-R51431 STUFF
R51430 NOT STUFF

MICRON MT61K256M32JE-14-A
6019B1847701
STRAP 0X1=001
MICRON-R51430 STUFF
R51431 NOT STUFF

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBW/DQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Qual Plan	Status
8 Gb	2Chx256Mb16 and 1.35V	1.23V	Micron	MT61K256M32JE-14-A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD



GPU GPIO

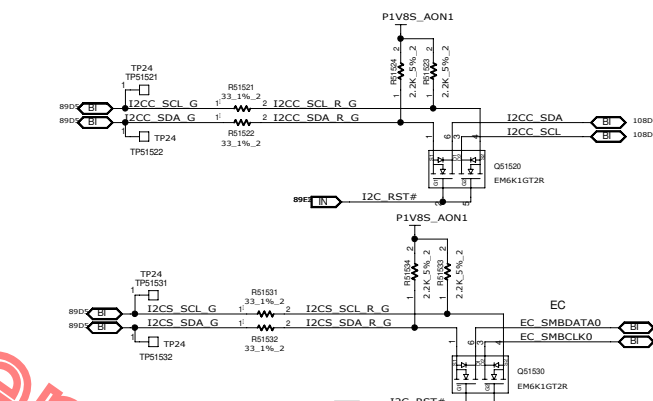
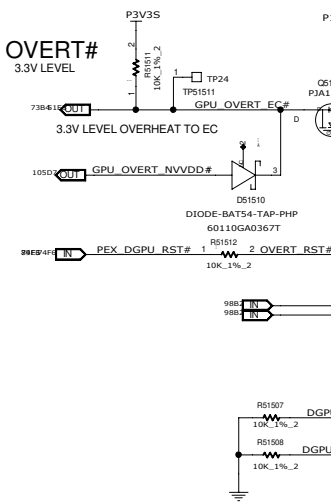
Table 7 Thermal Specifications

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
Thermal Resistance (Junction to Case, R _{JA})	0.014	0.017	0.017	TBD	C/W
Thermal Resistance (Junction to PCB Board, R _{JB})	0.44	0.56	0.56	TBD	C/W
GPU Shutdown Temperature (T _{SDT})	99	99	99	TBD	°C
GPU Shutdown Temperature (T _{HEM_ALERT})	94	94	94	TBD	°C

Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
GPU Maximum Operating Temperature ¹	89	89	89	TBD	°C
GPU Target Temperature (T _{90min})	87 (Default) 75 (min)	87 (Default) 75 (min)	87 (Default) 75 (min)	TBD	°C

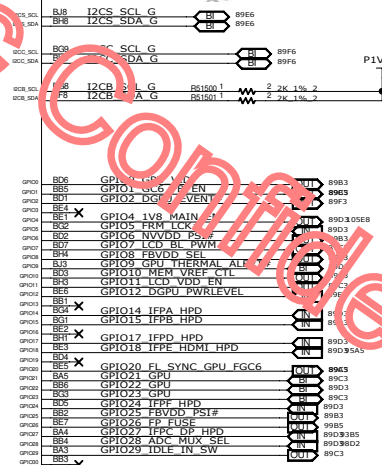
Notes:
1. OVERT results in an 87.5% (18) hardware clock slowdown.
2. THERM_ALERT results in a 50% (12) hardware clock slowdown.
3. The GPU maximum operating temperature is the maximum GPU temperature at which the GPU is guaranteed to operate at the target performance (base clock) under the 100% power mode.

OVERT# 3.3V LEVEL



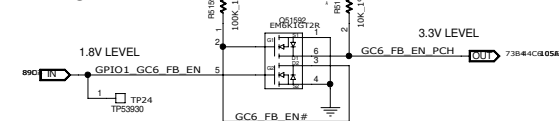
13.3.2.1 I2CS Slave Address

The default I2CS address is 0x9E

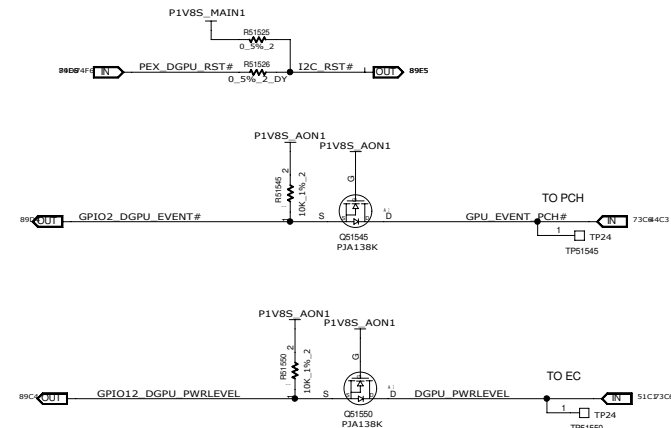
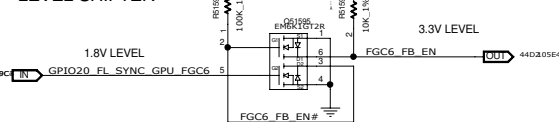


NVIDIA_N18E_G1_KD_QS_A1_BGA_222BP

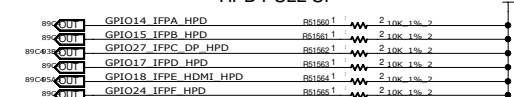
GC6_FB_EN LEVEL SHIFTER



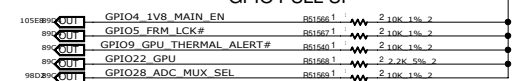
GC6_FB_EN LEVEL SHIFTER



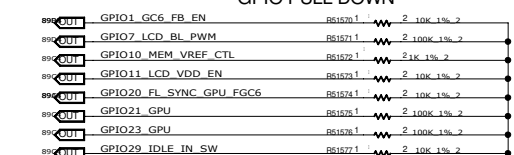
HPD PULL UP



GPIO PULL UP



GPIO PULL DOWN



53900 - 54199

51500 - 51599

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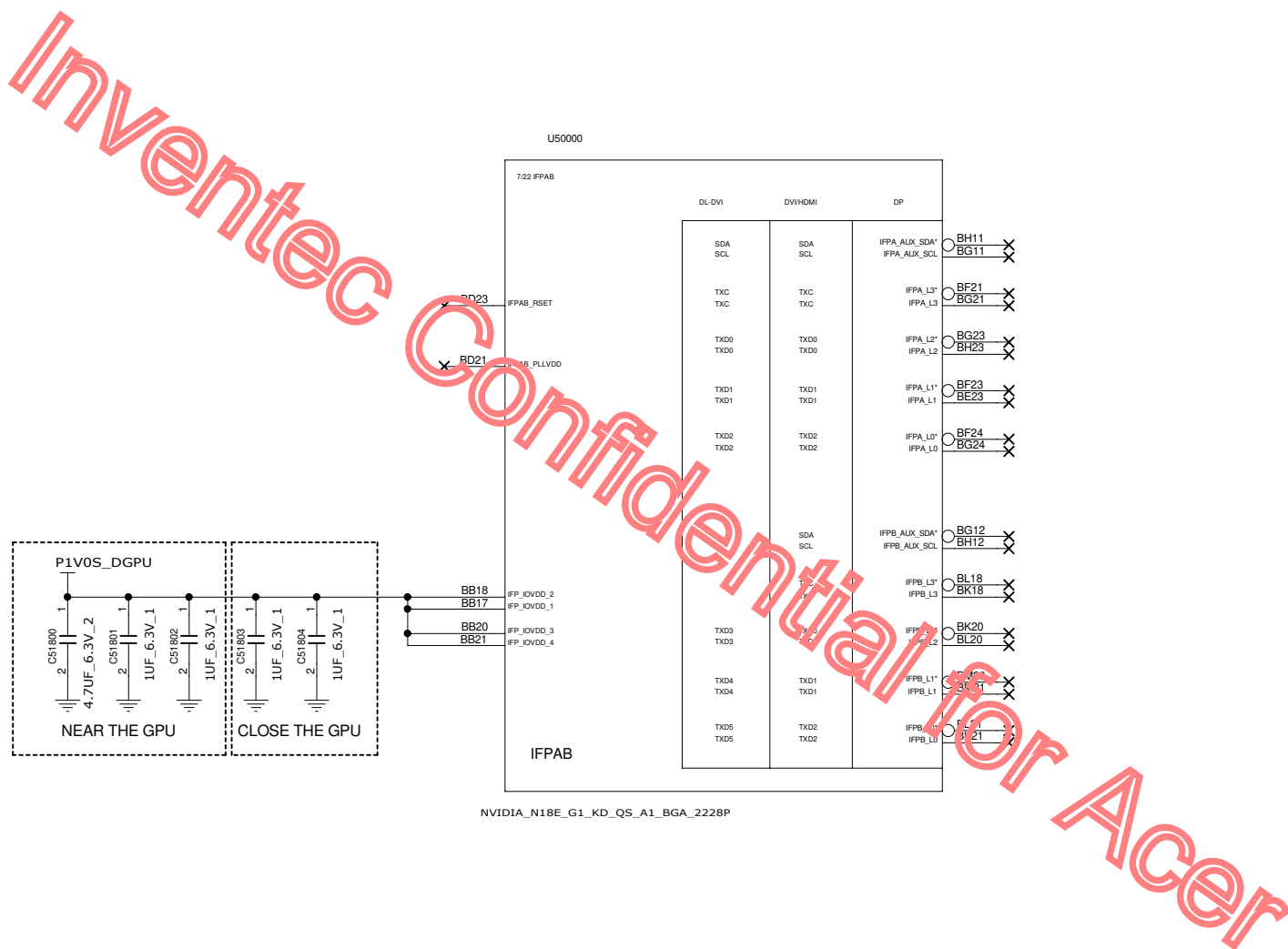
INVENTEC

MODEL	PROJECT	FUNCTION
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SHEET	89	139
REV	X01	

CHANGE D1 XXXX

DATE 21-OCT-2002

PCB VER XXX

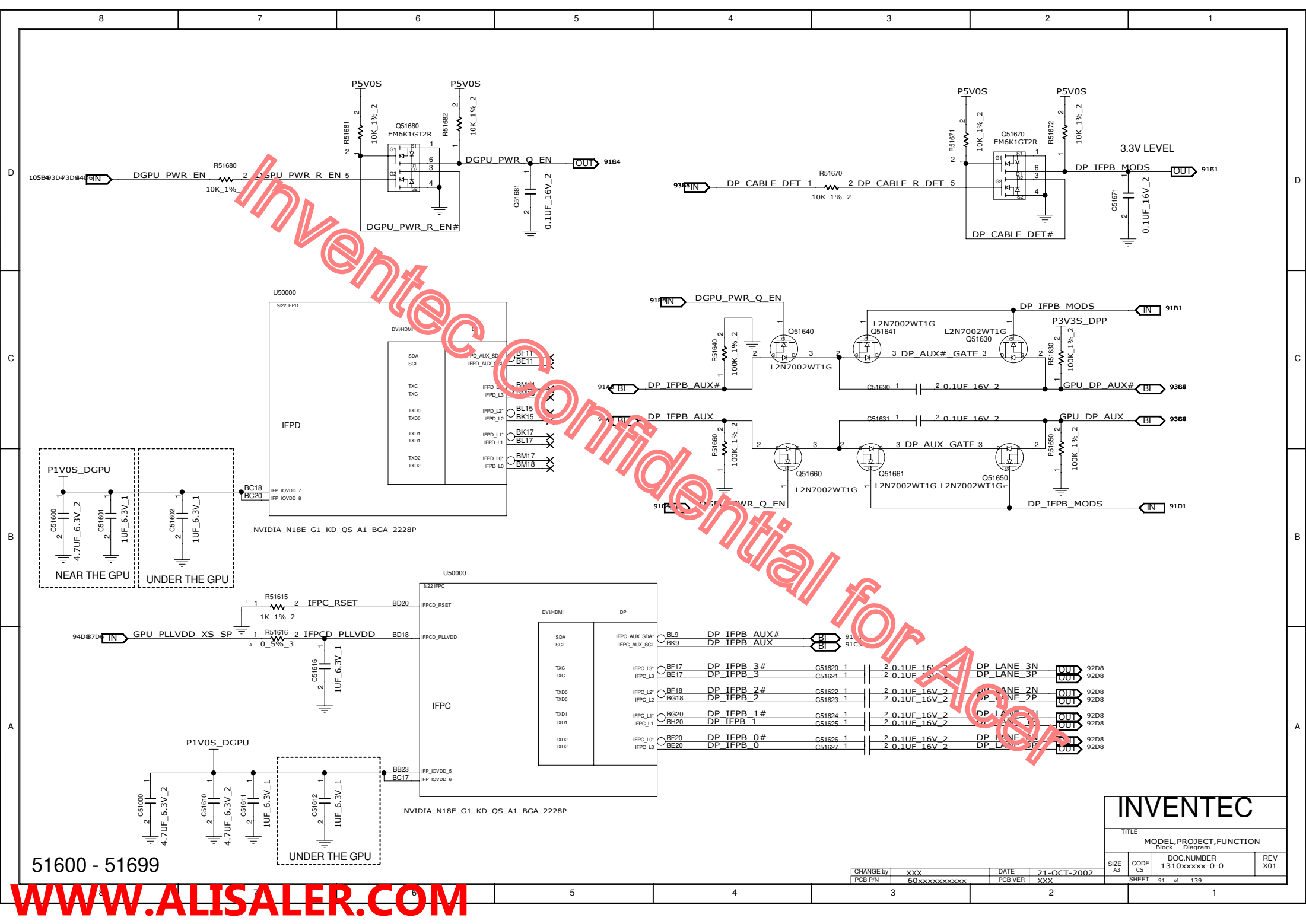


51800 - 51899

WWW.ALISALER.COM

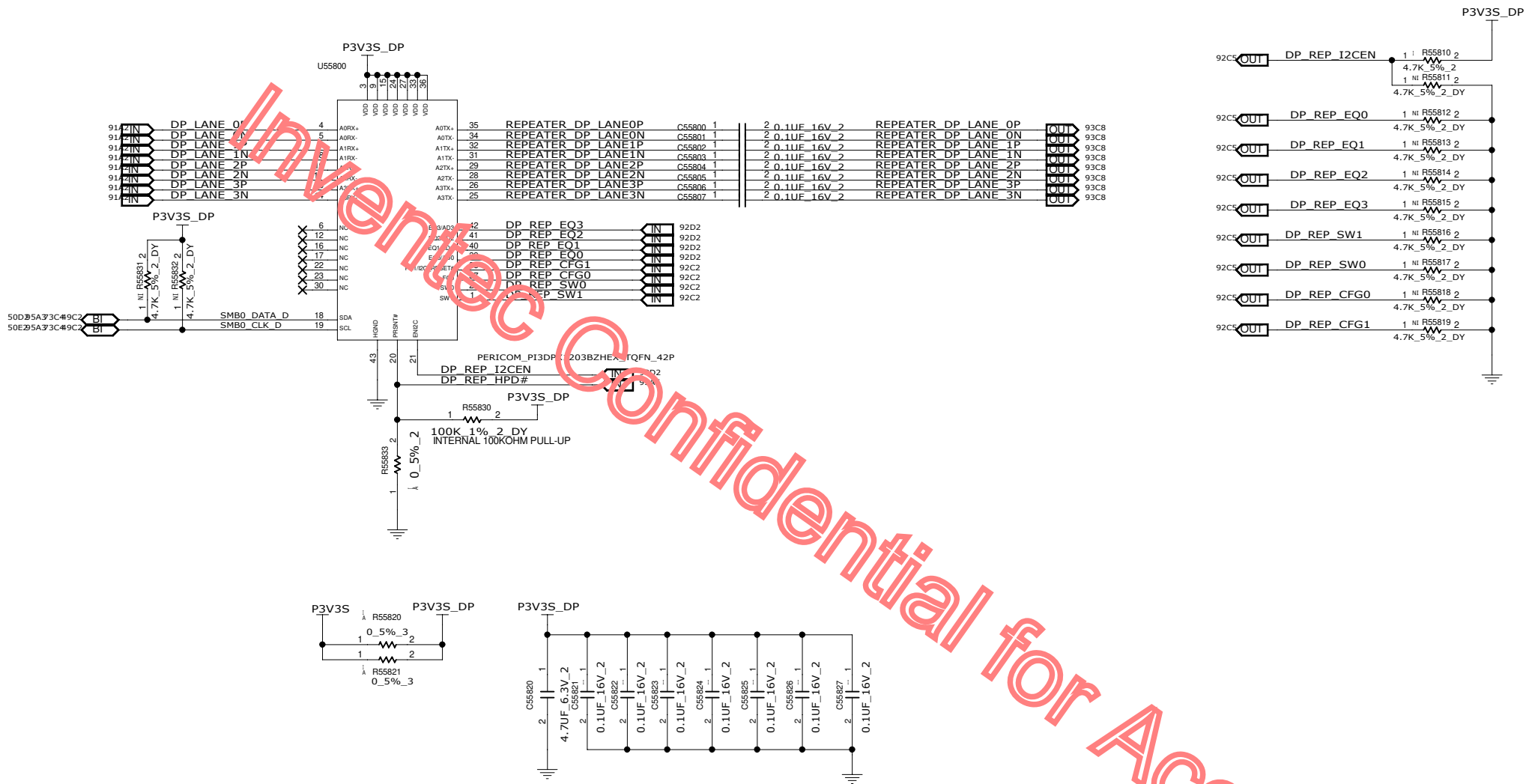
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 90 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



8	7	6	5	4	3	2	1
<div>INVENTEC</div> <div>CONFIDENTIAL for A</div>							
<div>51600 - 51699</div> <div>WWW.ALISALER.COM</div>							
<div>CHANGE by XXX</div> <div>DATE 21-OCT-2002</div> <div>PCB P/N 60xxxxxxxxxx</div> <div>PCB VER XXX</div> <div>SHEET 91 of 139</div>							

DP REDRIVER



55800 - 55999 56000 - 56199

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CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET	92	of	139				

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

D

C

B

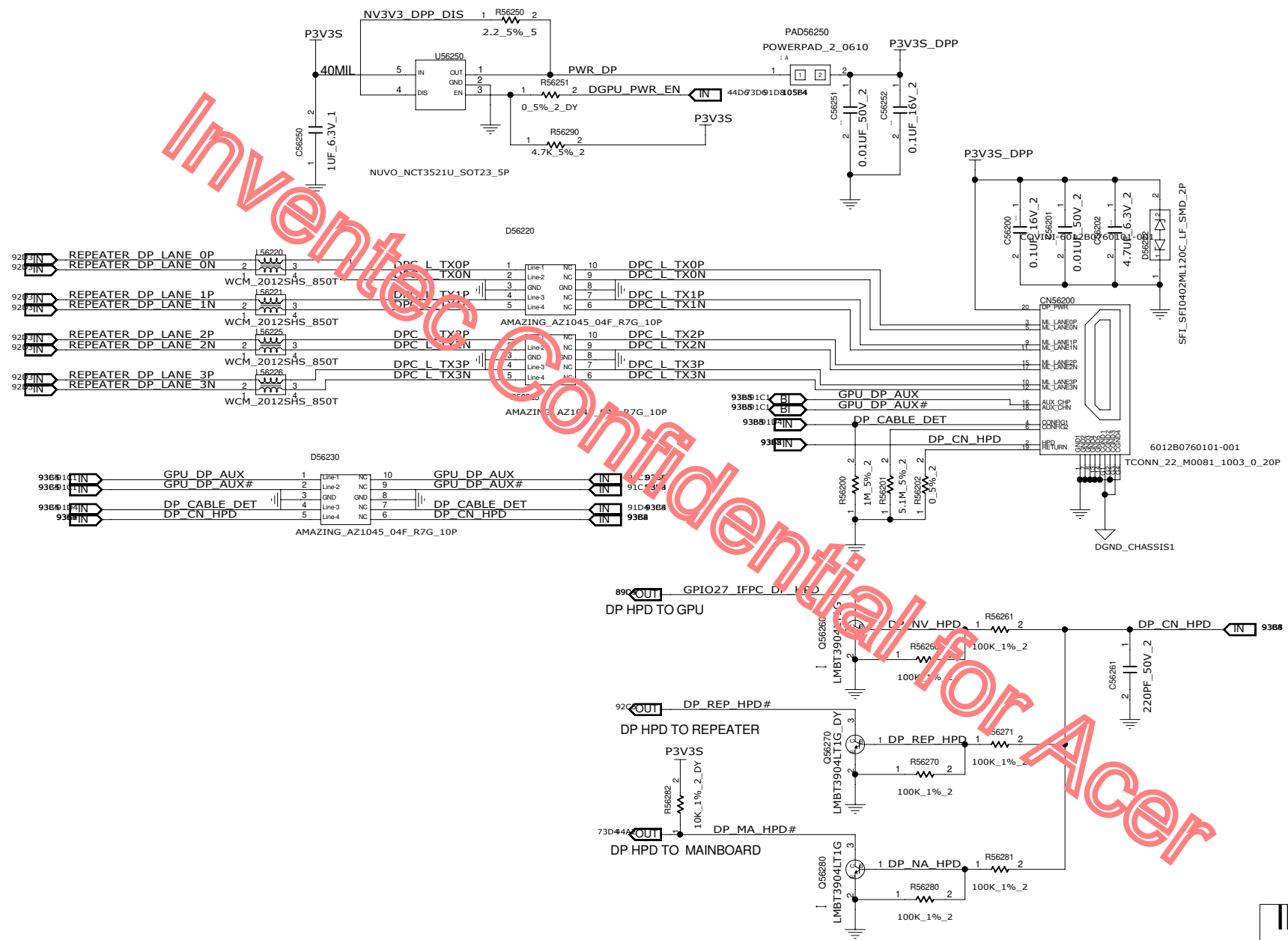
A

D

C

B

A



56200 - 56399

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	93	of	139				

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
DOC NUMBER			
1310xxxxx-0-0			
REV			
X01			

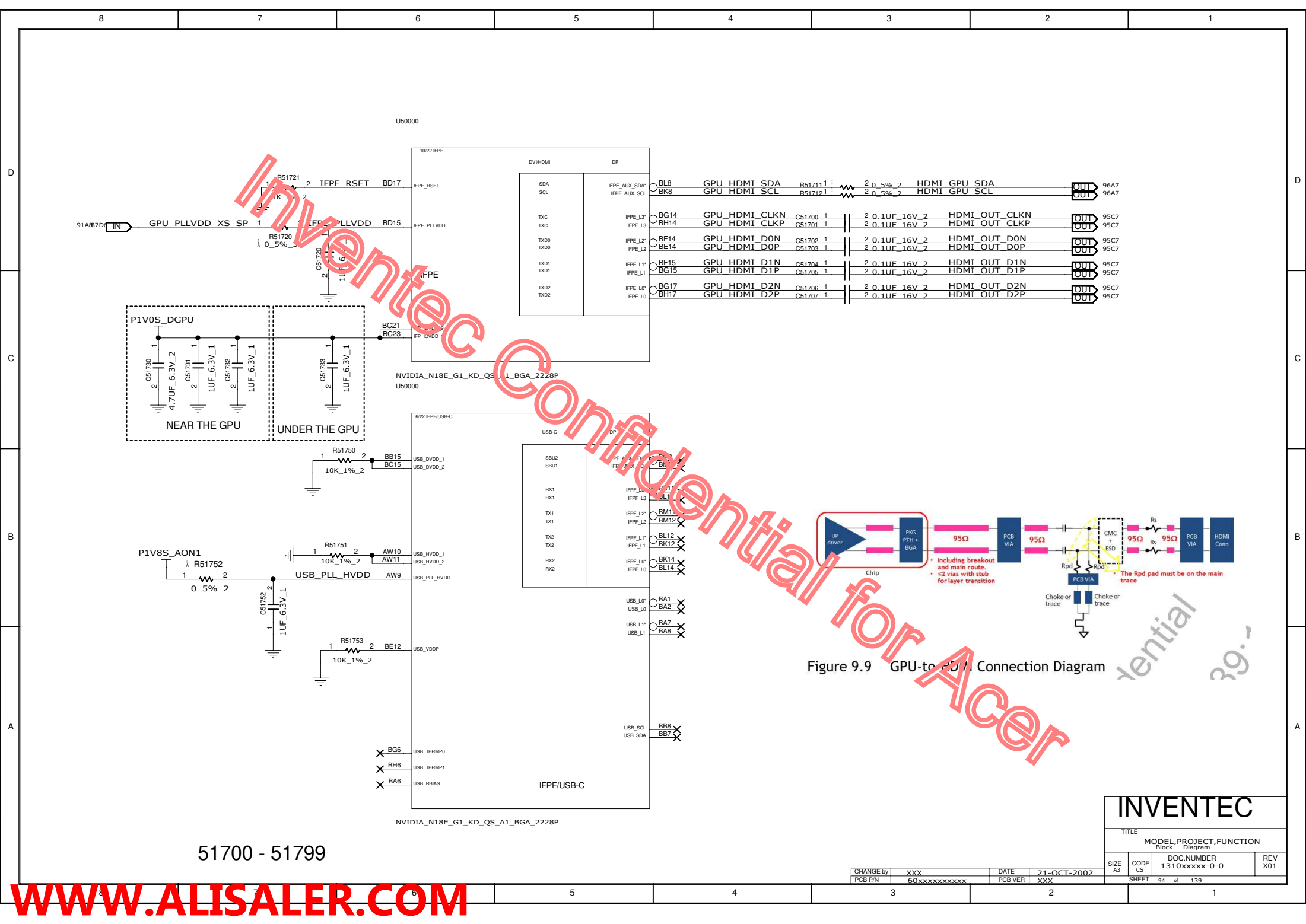
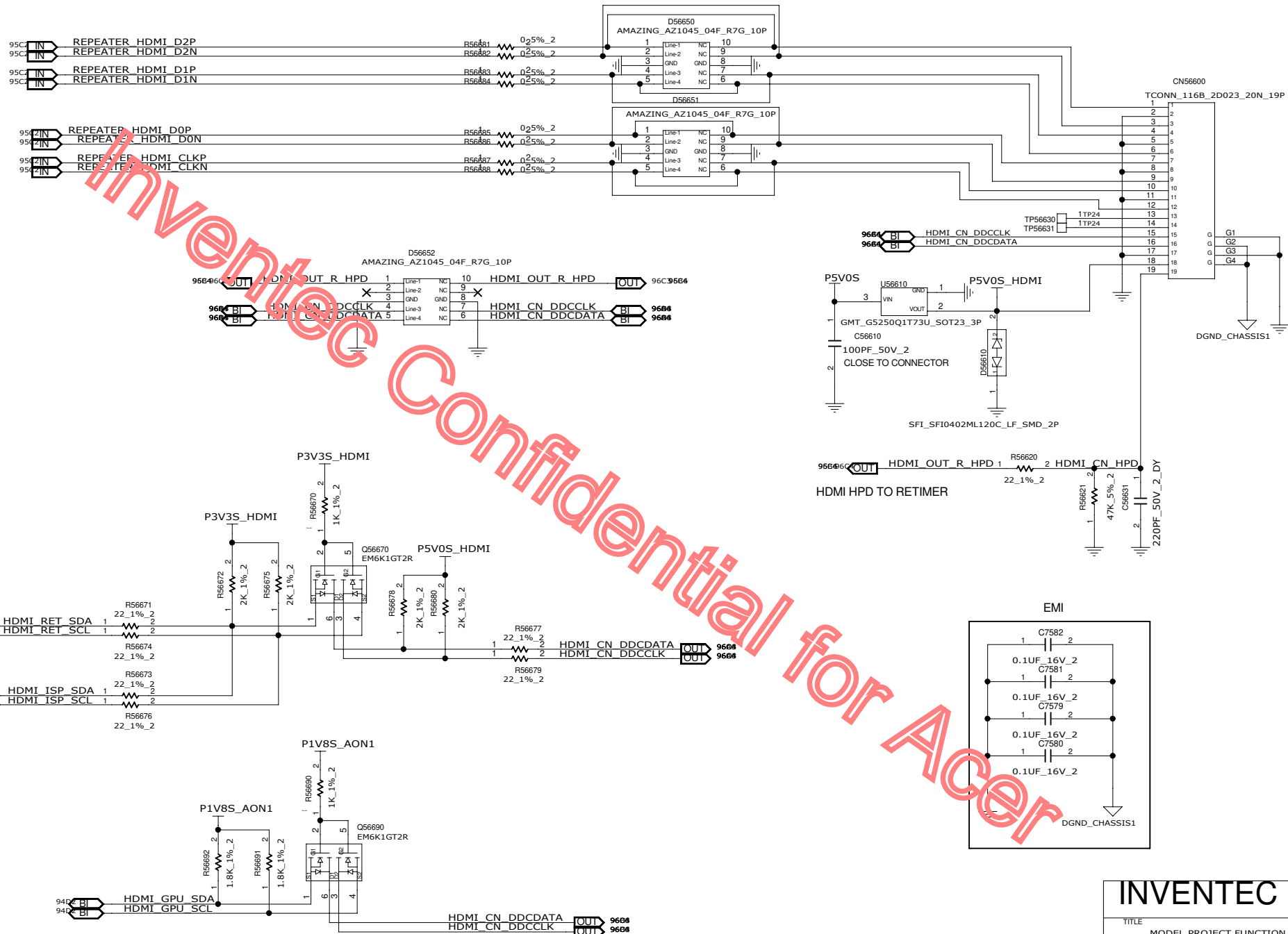
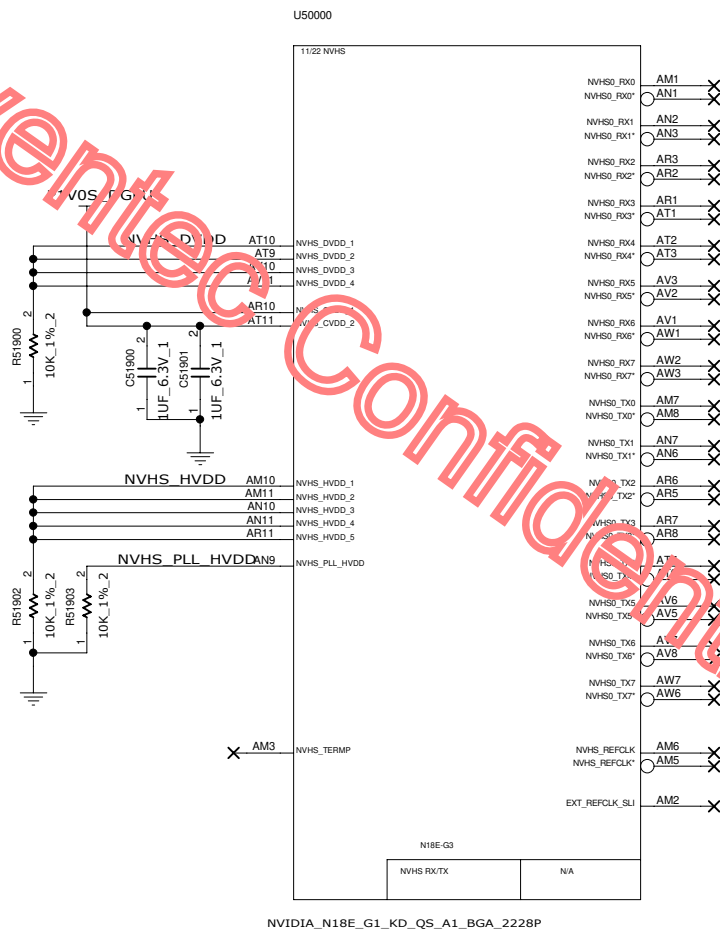


Figure 9.9 GPU-to-PD/A Connection Diagram



56600 - 56799



NVIDIA_N18E_G1_KD_QS_A1_BGA_2228P

51900 - 51999

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INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
Block	Diagram

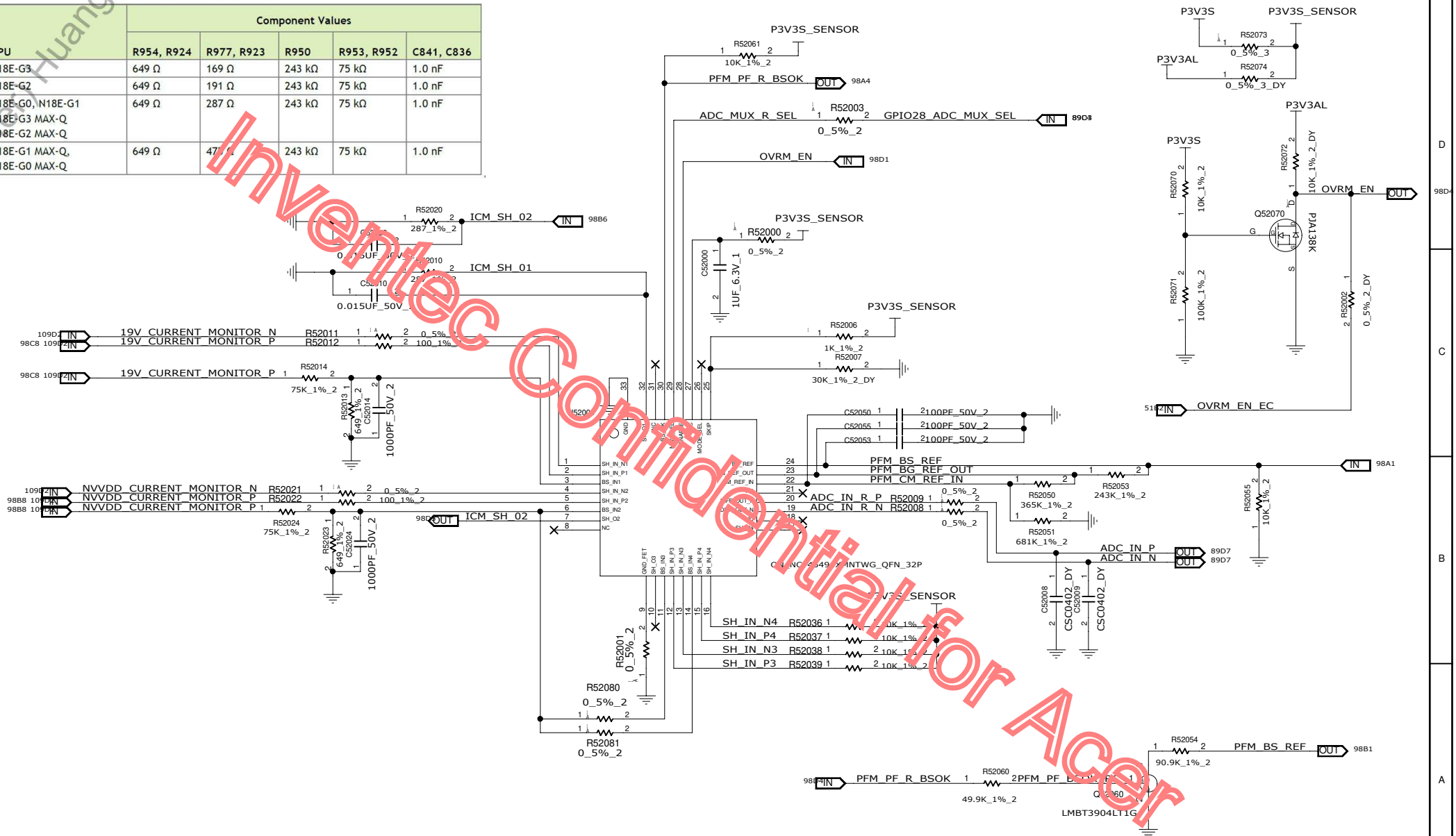
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SHEET 97 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX

SHEET 97 of 139

Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G2	649 Ω	191 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G0, N18E-G1	649 Ω	287 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G3 MAX-Q					
N18E-G2 MAX-Q					
N18E-G1 MAX-Q	649 Ω	471 Ω	243 k Ω	75 k Ω	1.0 nF
N18E-G0 MAX-Q					



52000 - 52099

INVENTEC

TITLE MODEL, PROJECT, FUNCTION
Block DiagramSIZE CODE DOC. NUMBER REV
A3 C5 1310xxxxx-0-0 X01CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxx PCB VER: XXX

SHEET 98 of 139

D

C

B

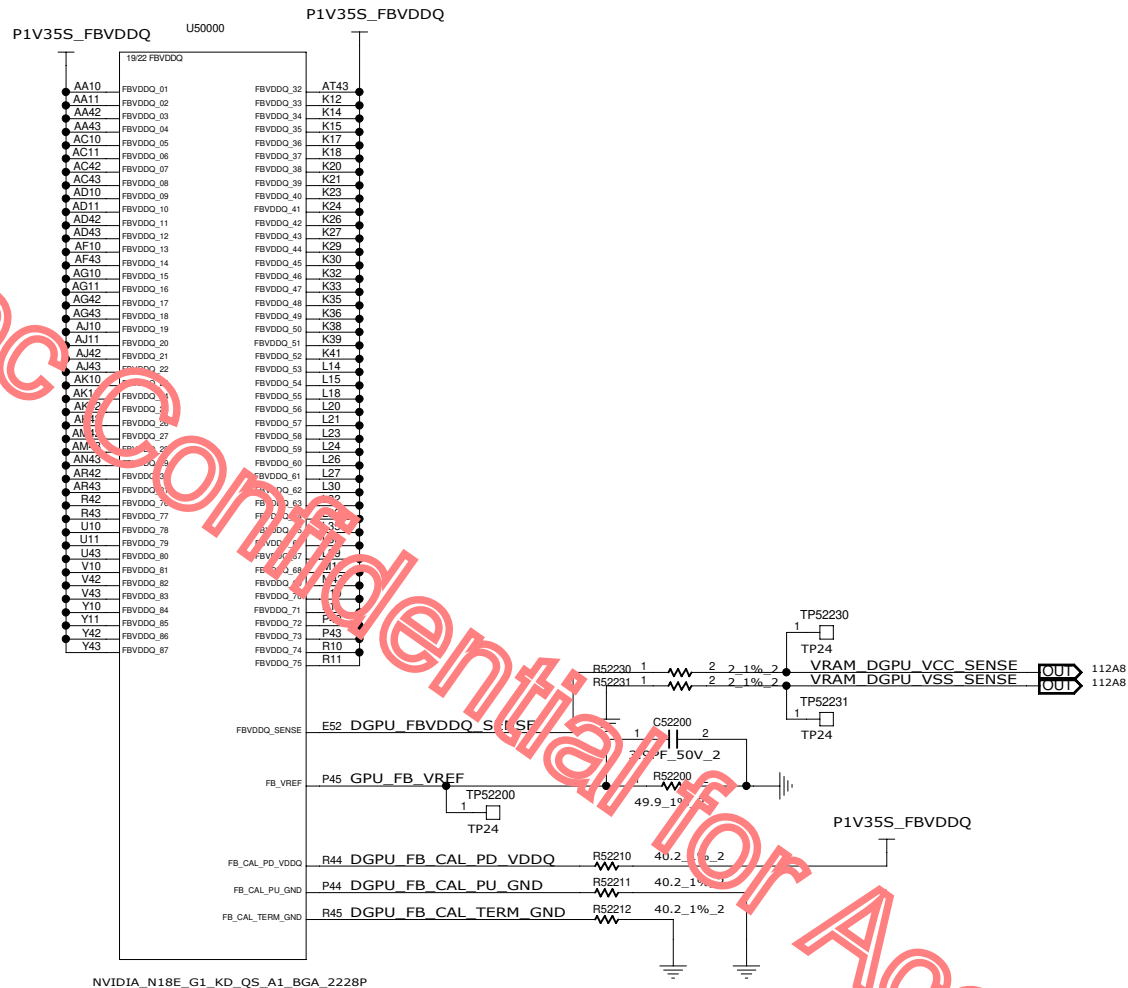
A

D

C

B

A

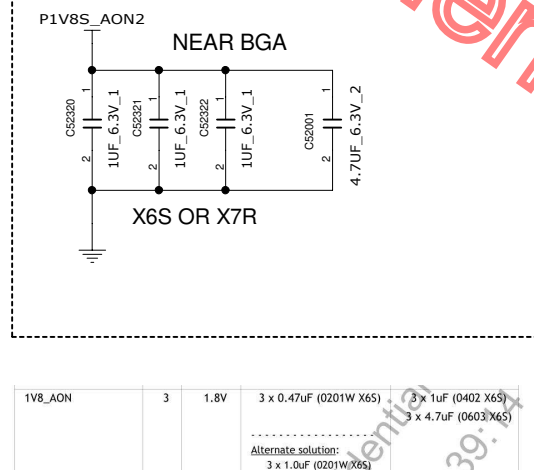
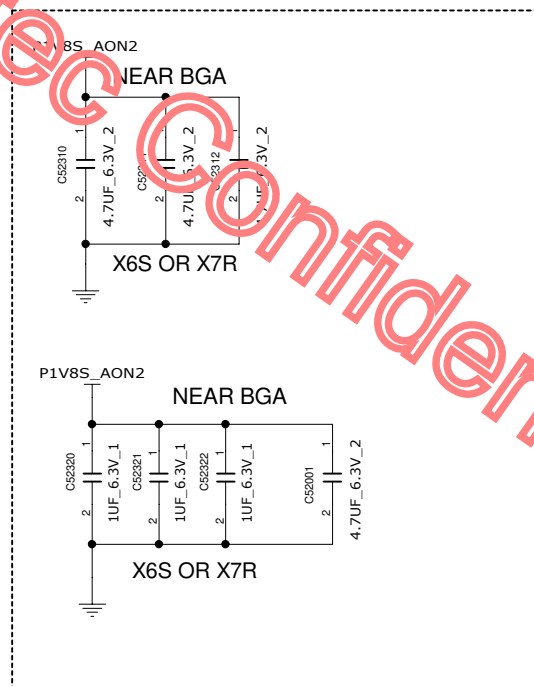
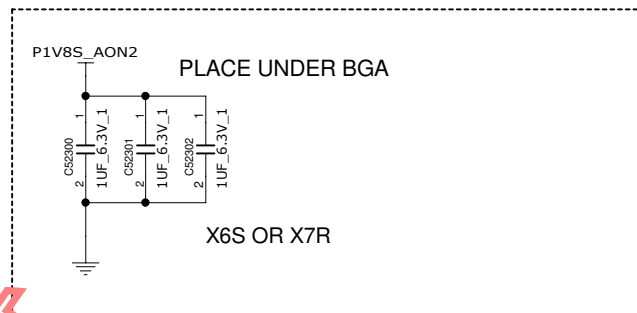


55600 - 55699
52200 - 52299

INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		REV X01
SHEET		100 of 139		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

GPU 1V8_AON DECOUPLING



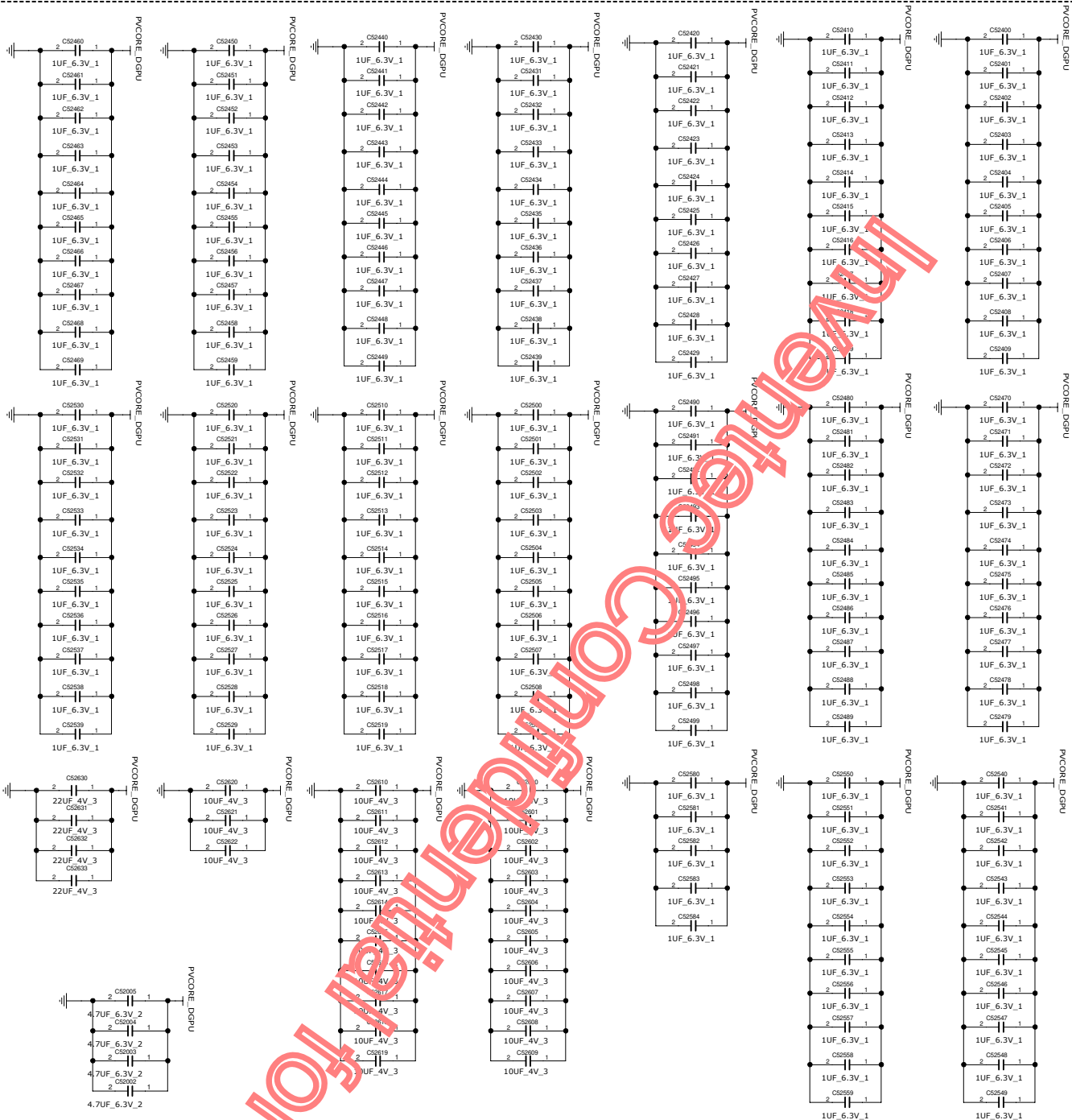
1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S)	3 x 1uF (0402 X6S)
			Alternate solution: 3 x 1.0uF (0201W X6S)	3 x 4.7uF (0603 X6S)

52300 - 52399

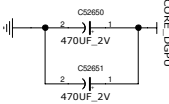
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TITLE MODEL, PROJECT, FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SHEET 101 of 139

52400 - 52999

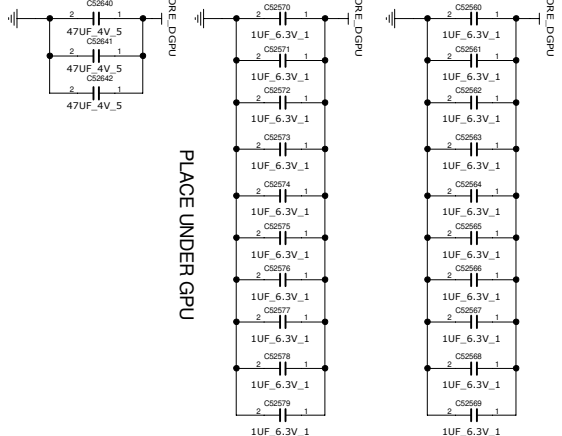
PLACE UNDER GPU



PLACE NEAR GPU



PLACE UNDER GPU



INVENTEC

MODEL PROJECT FUNCTION

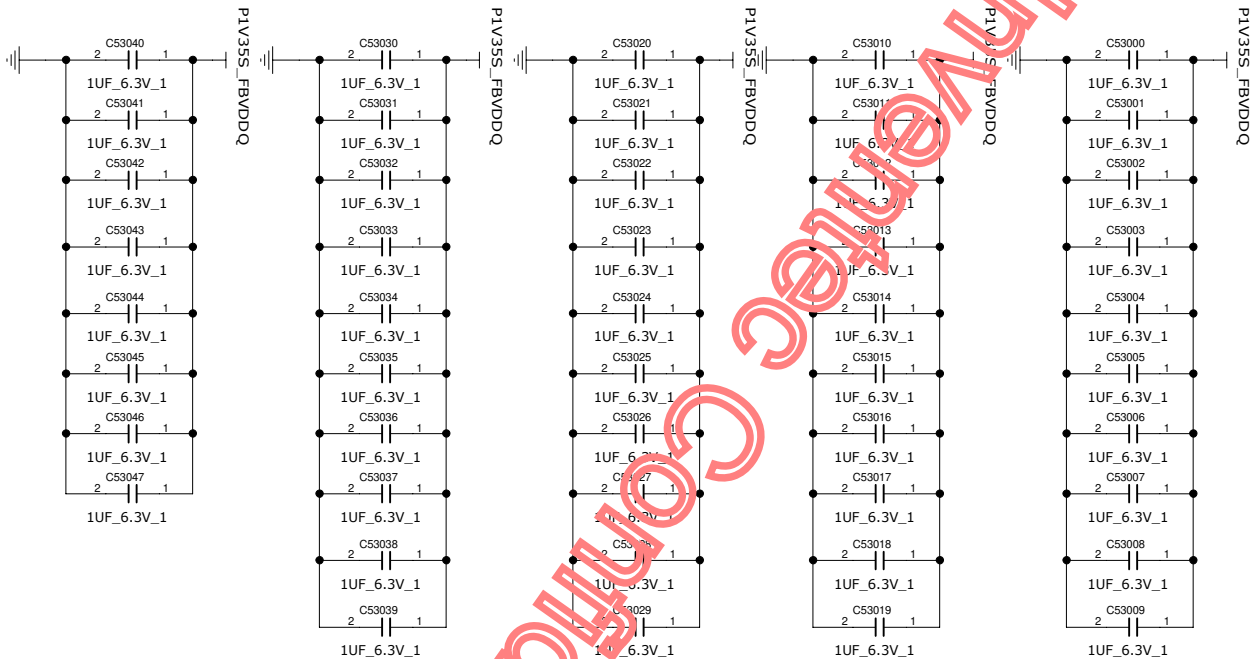
DATE 21-01-2002

PAGE 2

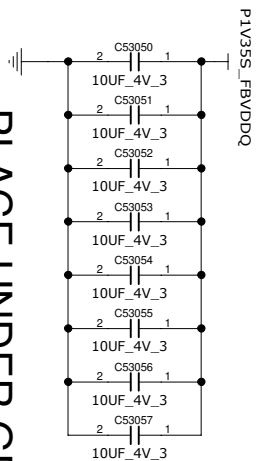
REV 1.0

53000 - 53299

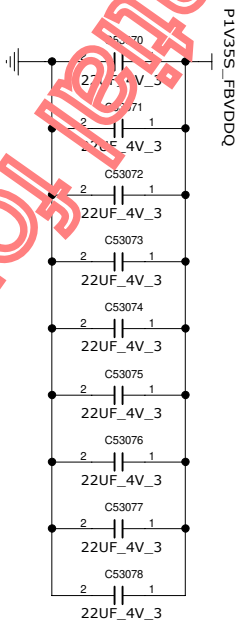
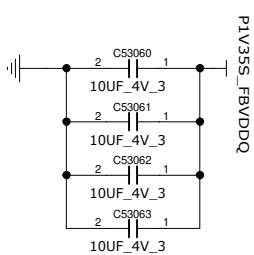
PLACE UNDER GPU



PLACE UNDER GPU



PLACE NEAR GPU



FBVDQ (GPU side)		4 x 10uF (0603 X65)	
25V		9 x 22uF (0603 X65)	
8 x 10uF (0603 X65)			
Generate solution:			
24 x 1.0uF (0201W X65) 2			
8 x 10uF (0603 X65)			

INVENTEC

CHANGE BY: XXX		DATE: 21-OCT-2002		SIZE: A3		SHEET: 10 of 139	
PCB P/N: 60XXXXXXXXXX		PCB VER: XXX		CODE: 1310XXXX-0-0		REVISION: X	
MODEL: PROJECT FUNCTION		DOC NUMBER					

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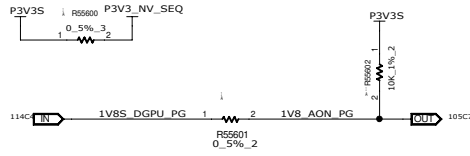
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U50000

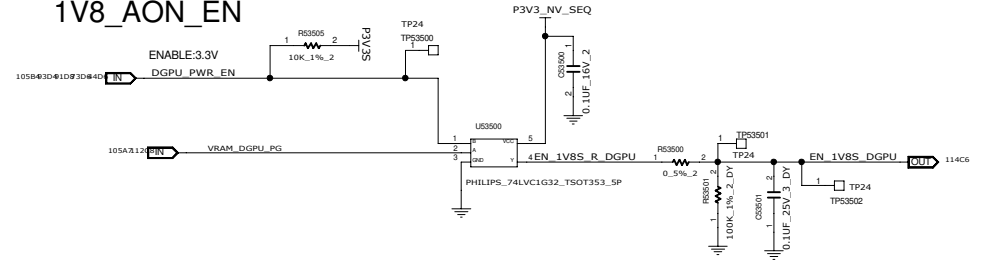
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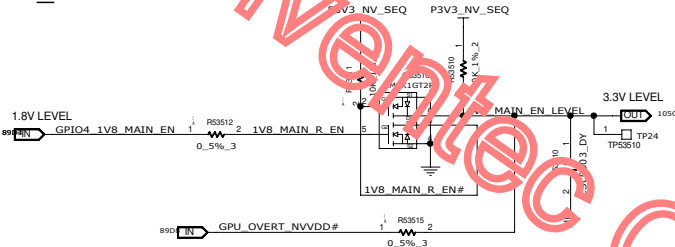
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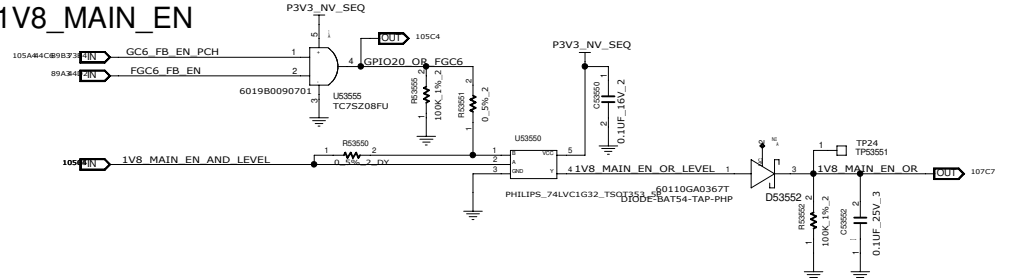
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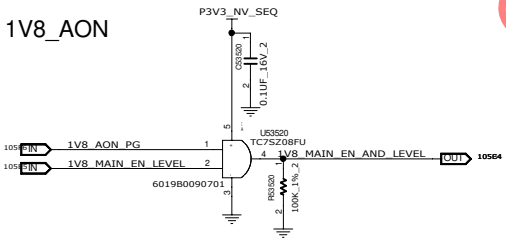
1V8_MAIN_EN LEVEL SHIFT



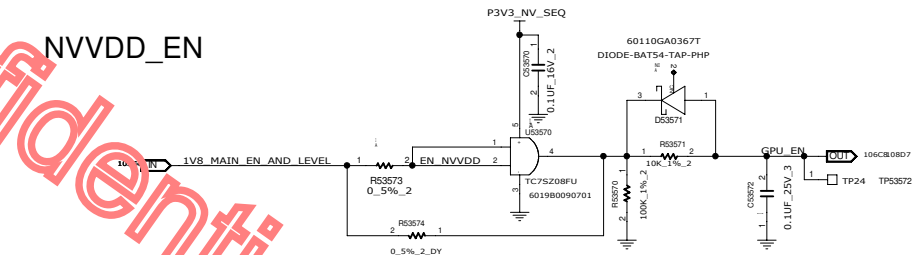
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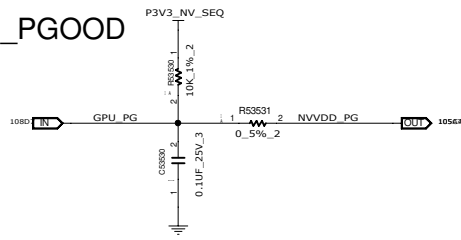
1V8_MAIN_EN AND WITH 1V8_AON



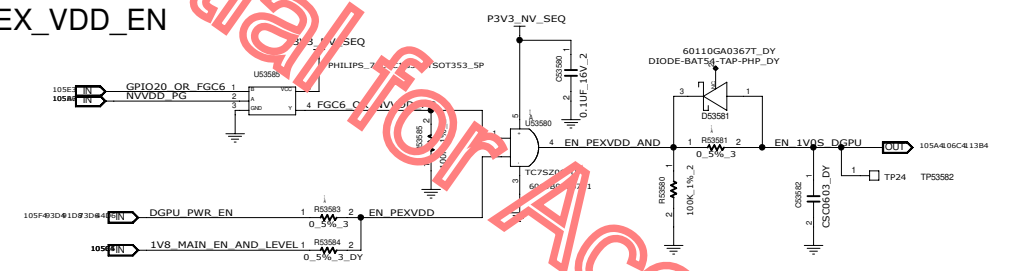
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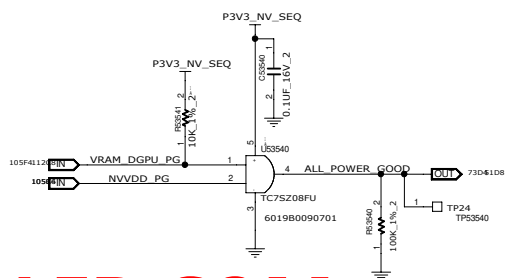
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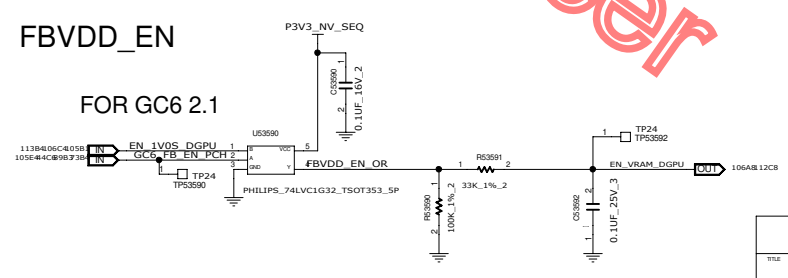


ALL POWER GOOD



FBVDD_EN

FOR GC6 2.1



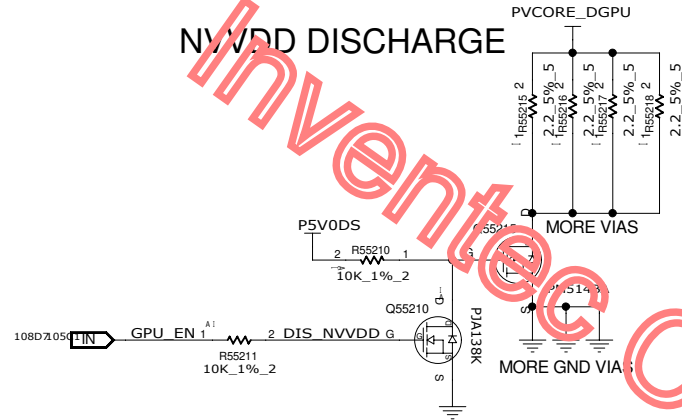
INVENTEC

MODEL PROJECT FUNCTION			
SIZE	A3	CODE	C5
DOC NUMBER	1310xxxxx-0-0		
REV	X01		

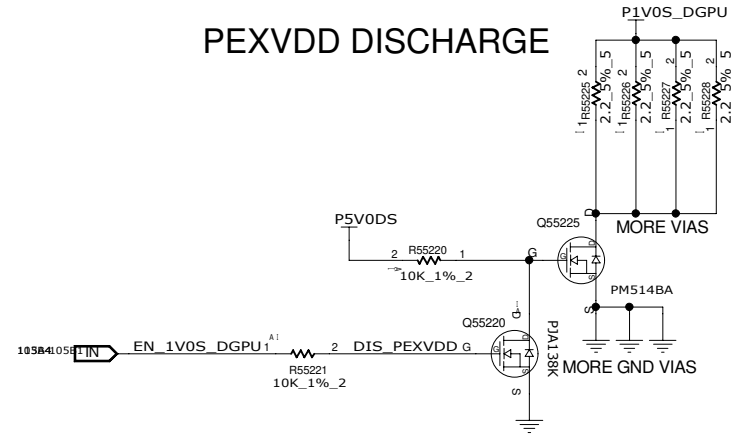
CHANGE D	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

DISCHARGE CIRCUIT

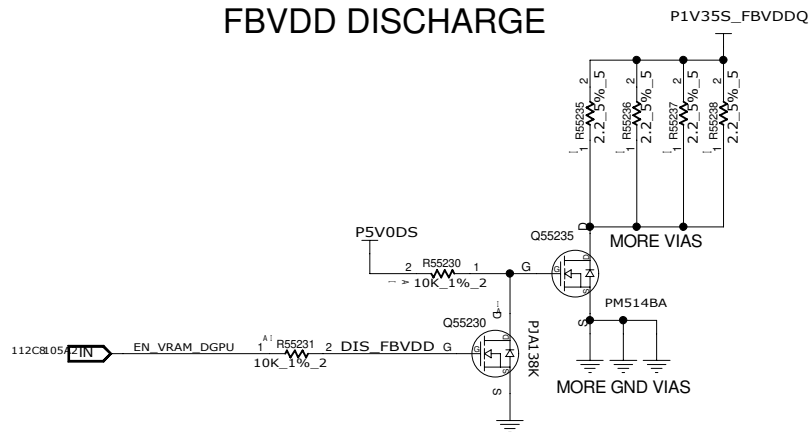
NVVDD DISCHARGE



PEXVDD DISCHARGE

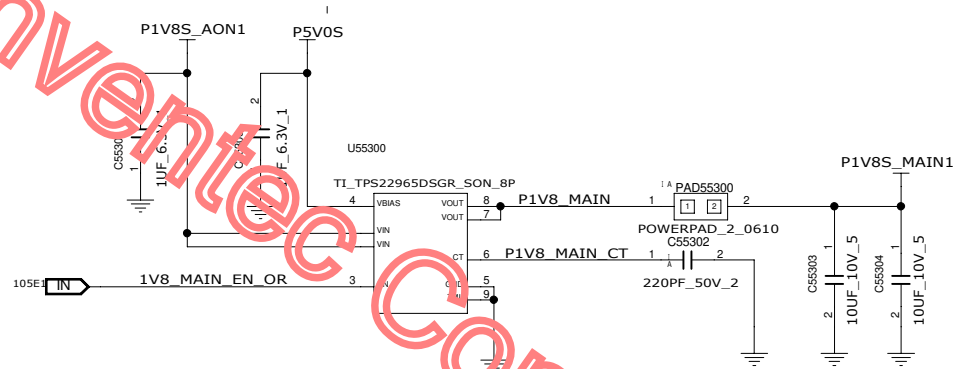


FBVDD DISCHARGE



55200 - 55299

1V8_MAIN



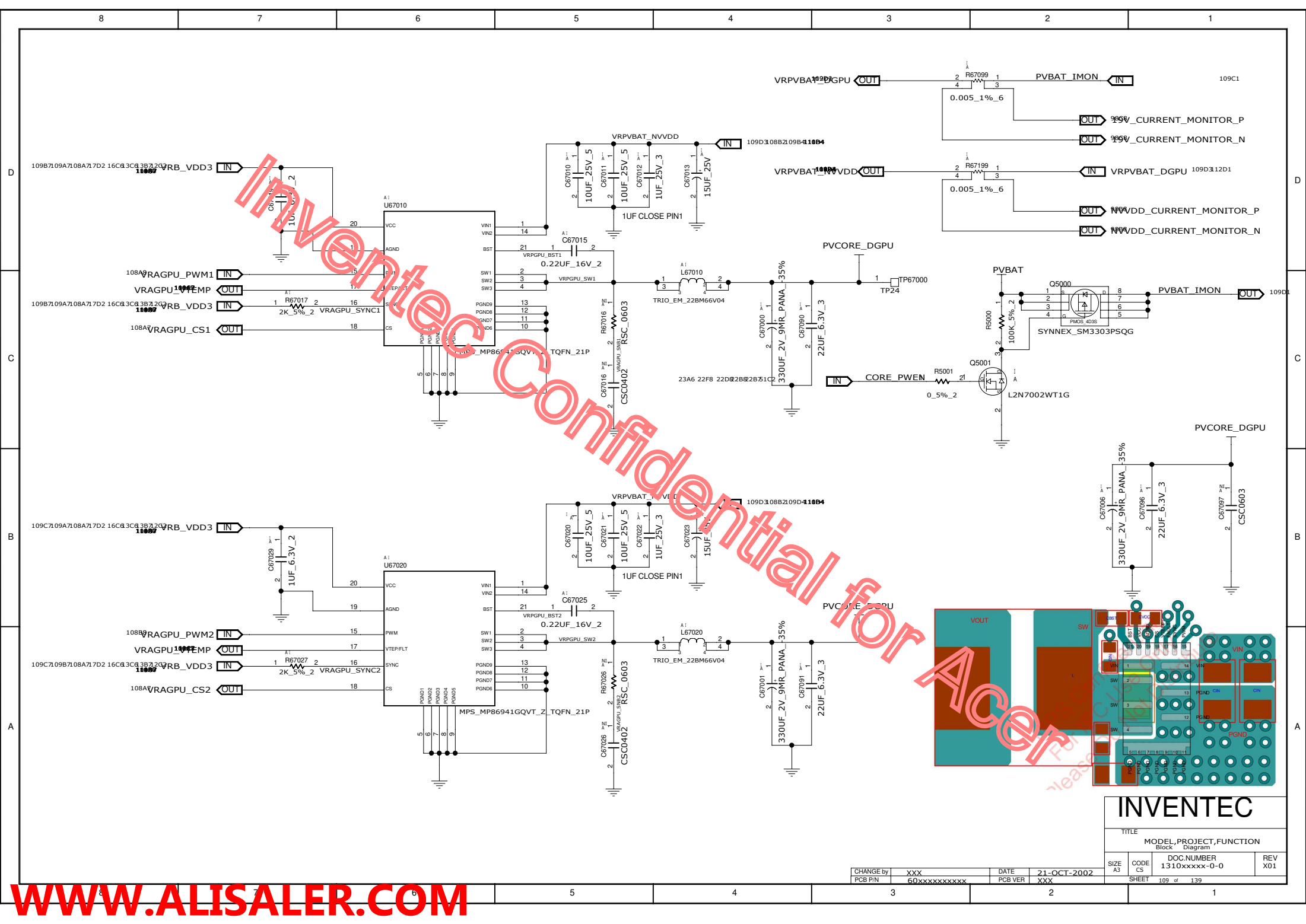
55300 - 55399

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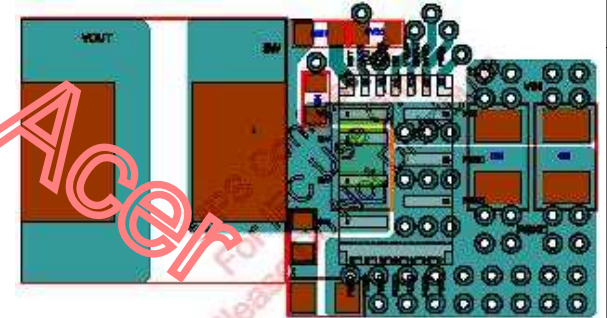
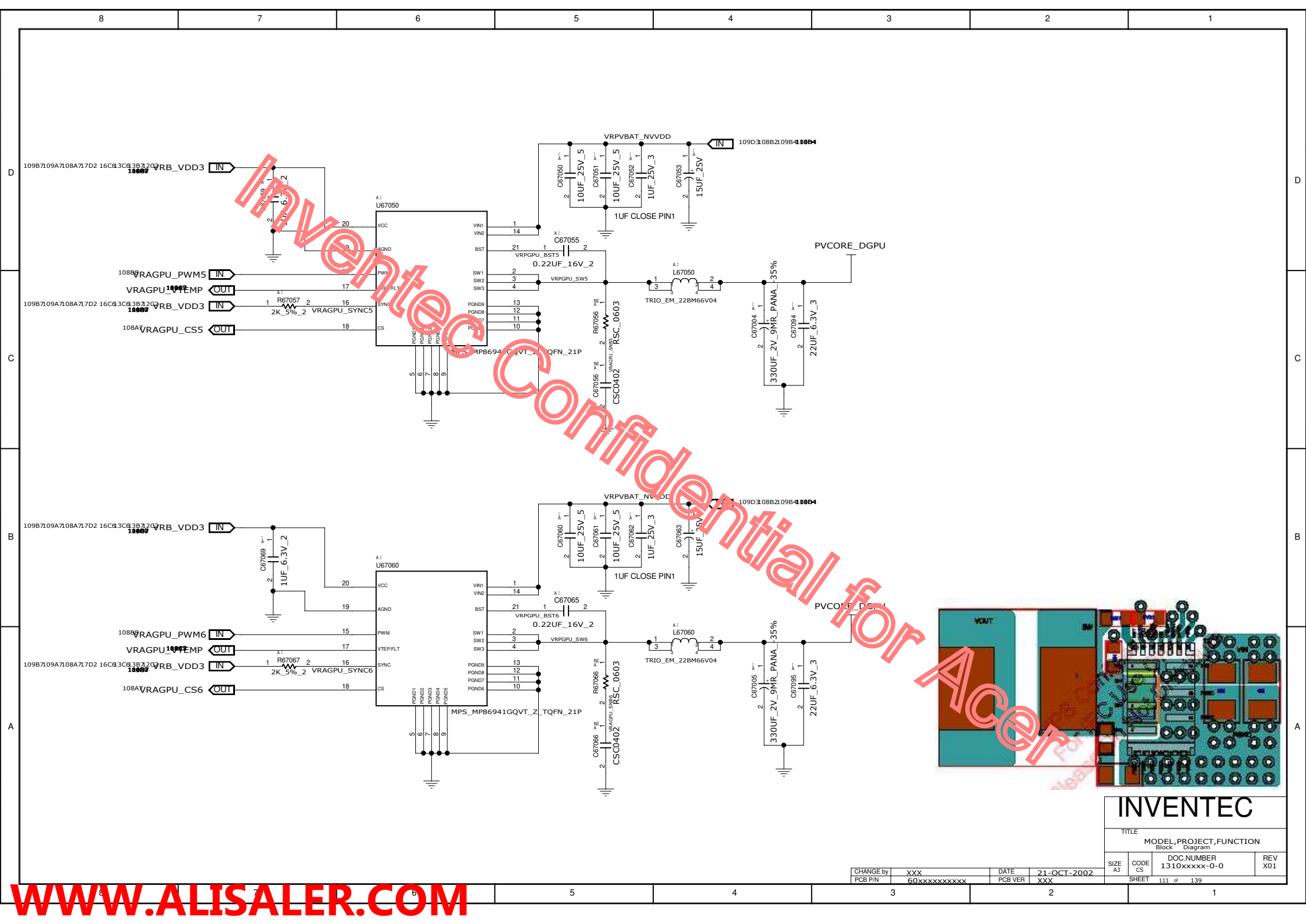
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 107 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



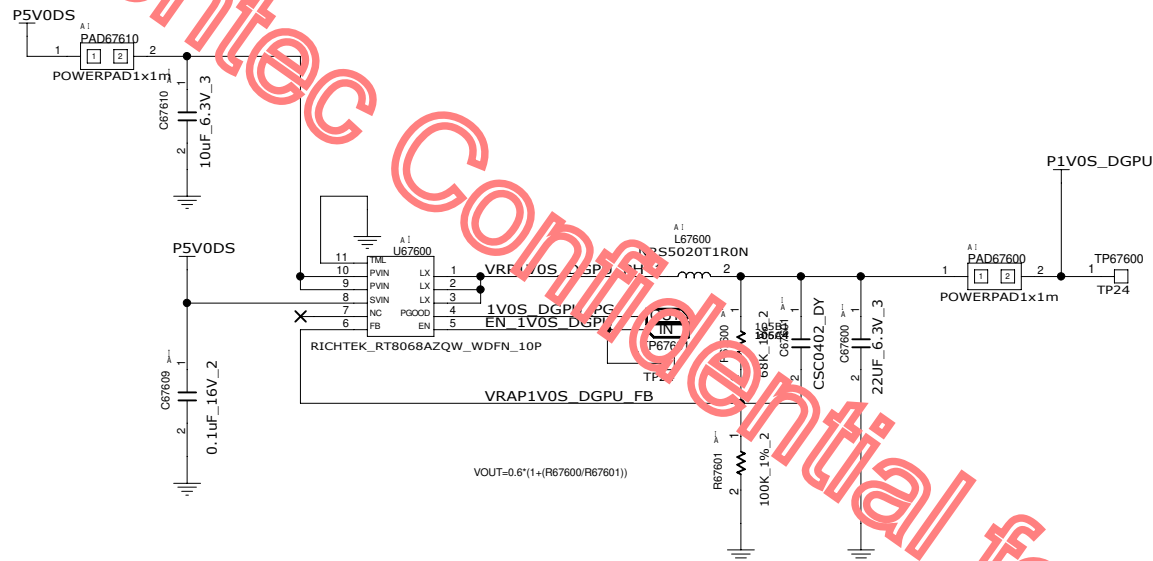
CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	109	of	139				



INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	111 of 139		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

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INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

SHEET 113 of 139

Table 12. Output EDP-Continuous

Product	NVVDD		FB TOTAL ⁵	1.0V Total ¹	1.8V Total ²
	(W)	(A)	(A)	(A)	(A)
N18E-G3	150	142	46	1.6	2.3
	160	150			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Table 14. Output EDP-Peak

Product	NVVDD		FB TOTAL ⁴	1.0V Total ¹	1.8V Total ²
	(W)	(A)	(A)	(A)	(A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms) ² (A)	Input EDPp (5ms) ² (A)	Input EDPc (1sec) ¹ (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$\text{Input EDPc Current (A)} = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$\text{Input EDPp (A) at } V_{\text{new}} = \text{Input EDPp (A) at } 19V \times \frac{19V}{V_{\text{new}}(V)}$$

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TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

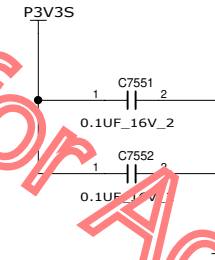
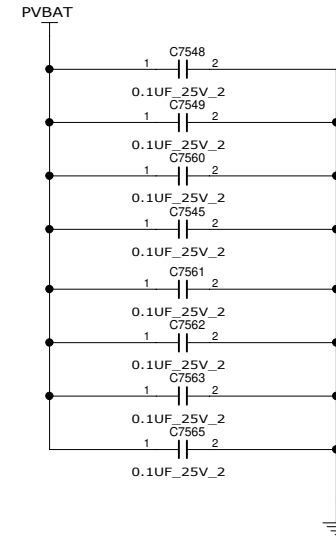
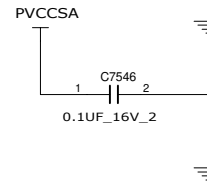
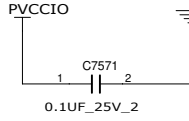
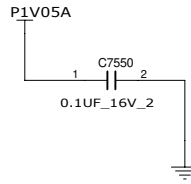
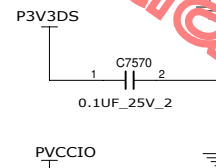
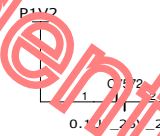
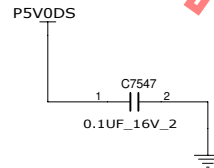
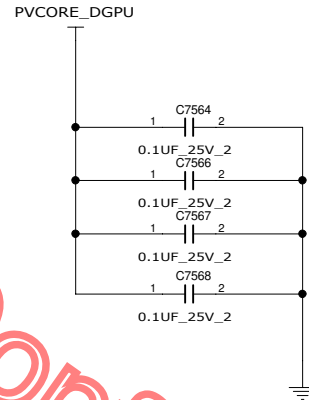
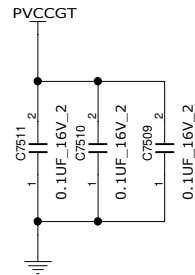
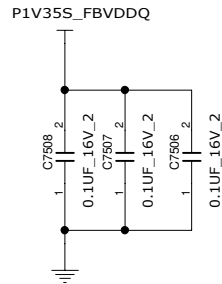
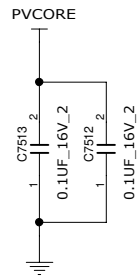
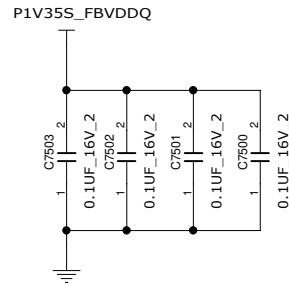
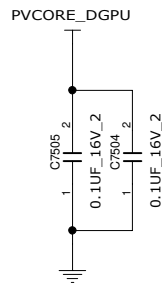
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CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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					TITLE		
					MODEL, PROJECT, FUNCTION		
					Block Diagram		
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EMI



INVENTEC

TITLE MODEL, PROJECT, FUNCTION
NFC_CNNL

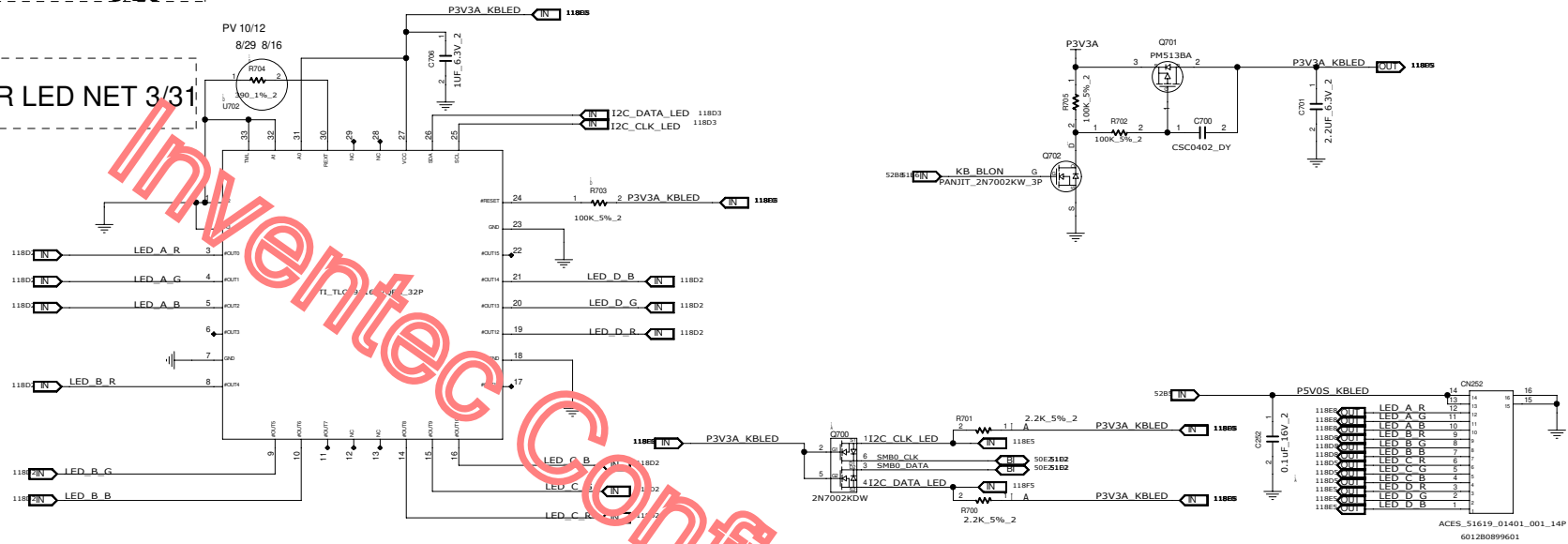
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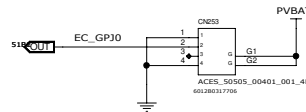
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ADJUST LED RES 8/16
8/29

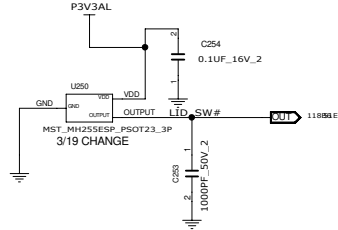
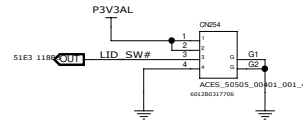
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TURBO#



HALL_SENSOR



REFERENCE NUMBER:700~800

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INVENTEC			
MODEL,PROJECT,FUNCTION			
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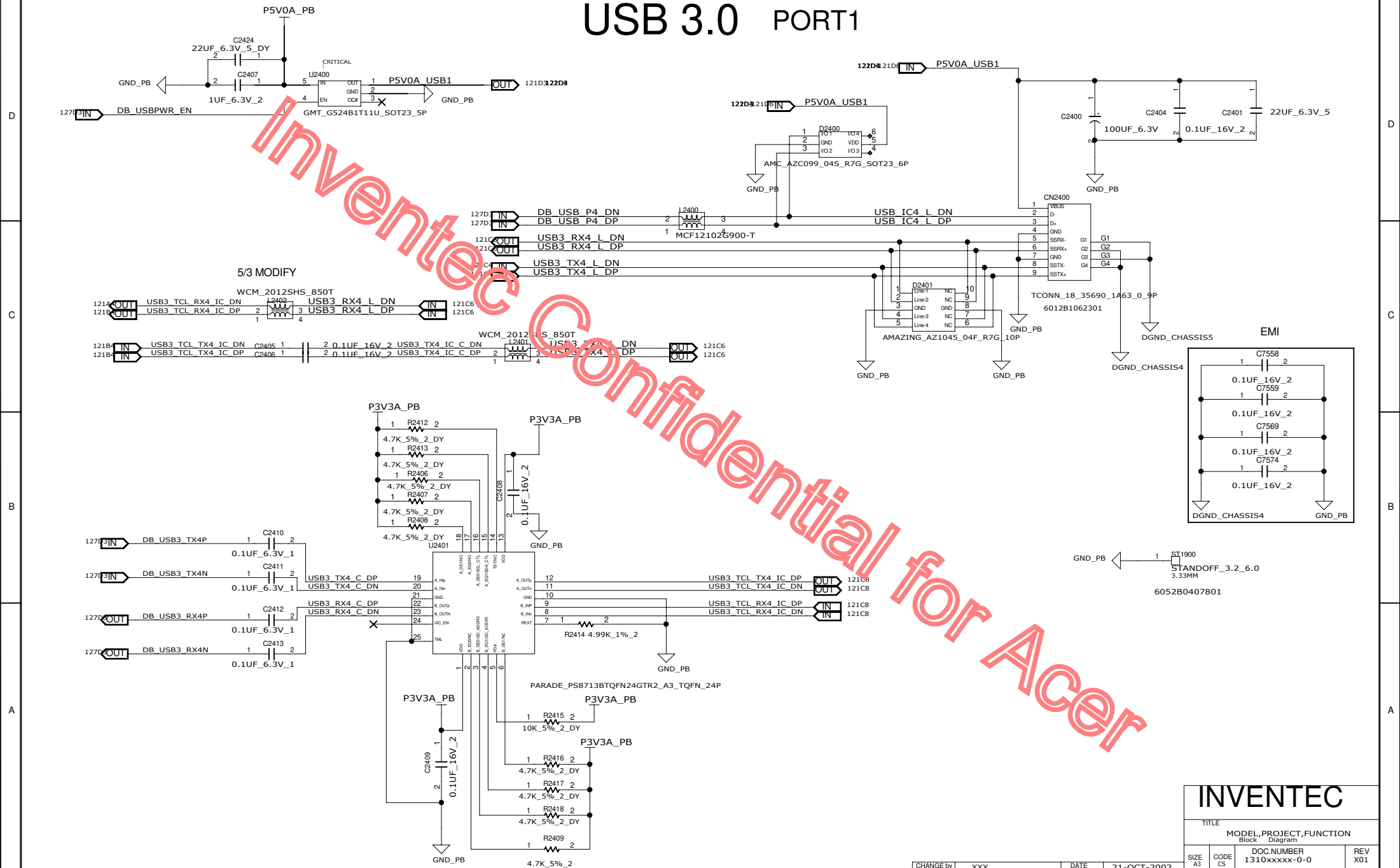
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TURBO# BOARD

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MODEL, PROJECT, FUNCTION Block Diagram			
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XXX 60xxxxxxxxxx		21-OCT-2002 XXX	119 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



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TITLE

MODEL, PROJECT, FUNCTION

Block Diagram

DOC NUMBER

1310xxxx-0-0

REV

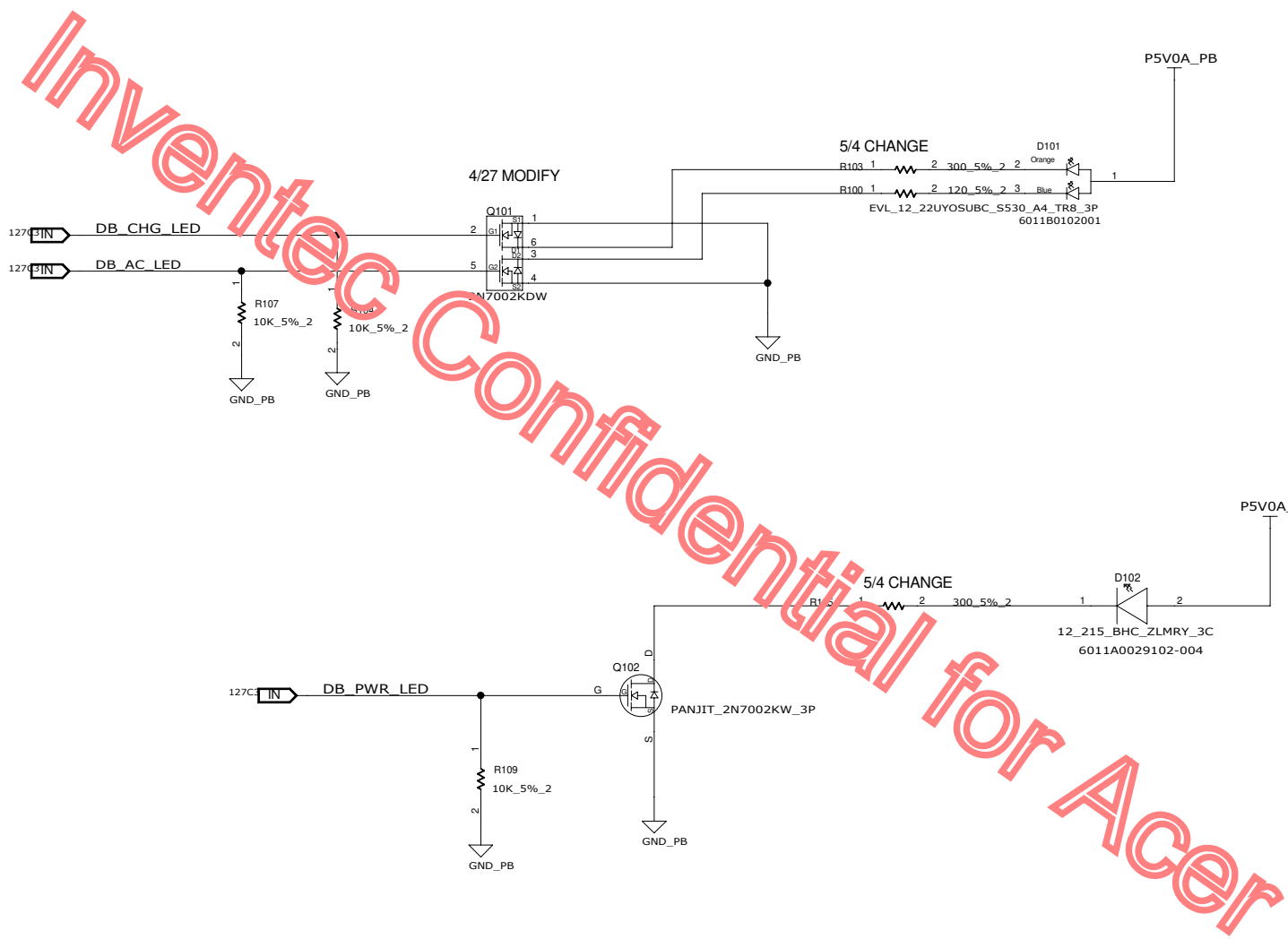
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PCB P/N 60xxxxxxxxxx

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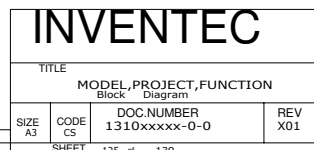
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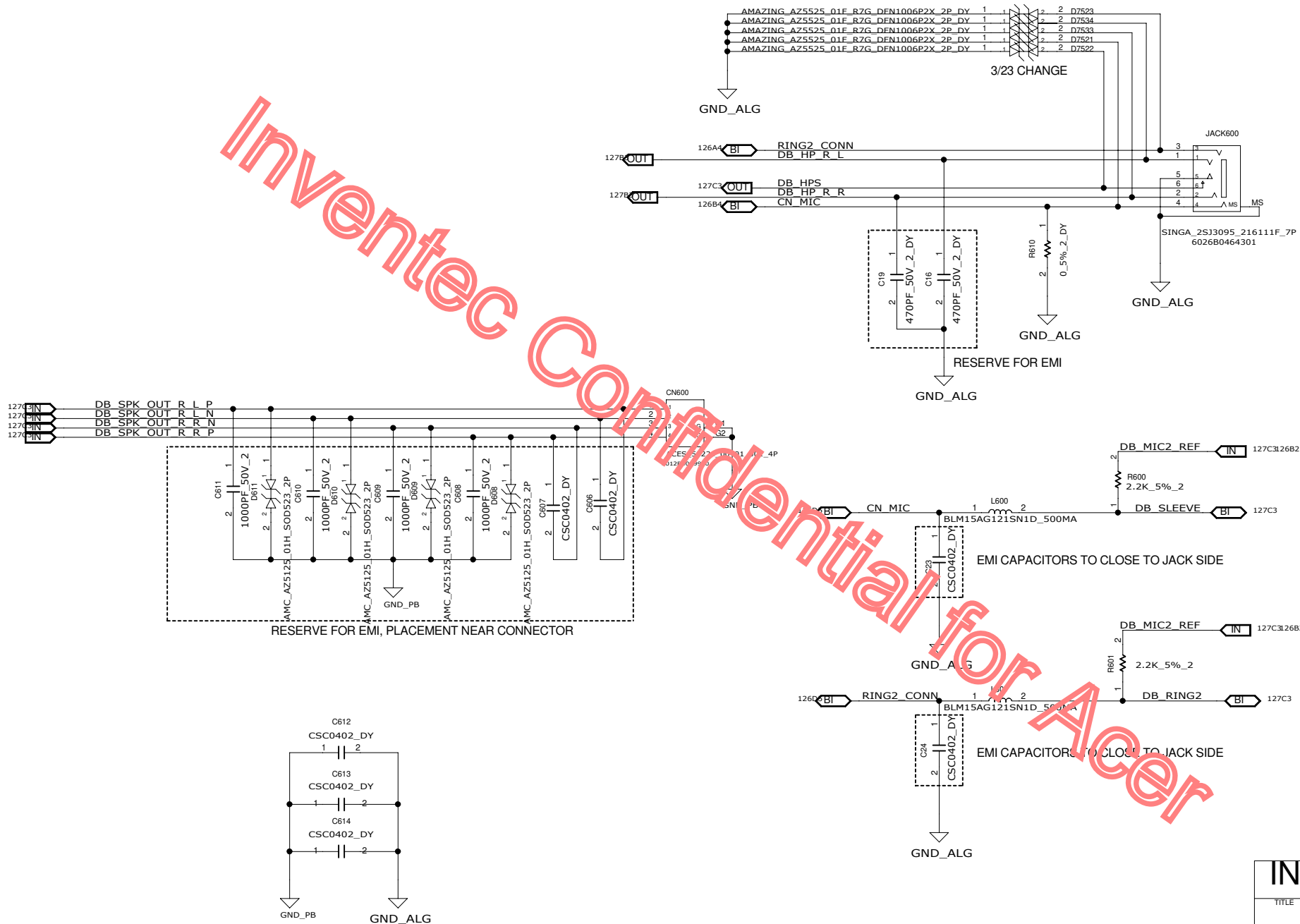
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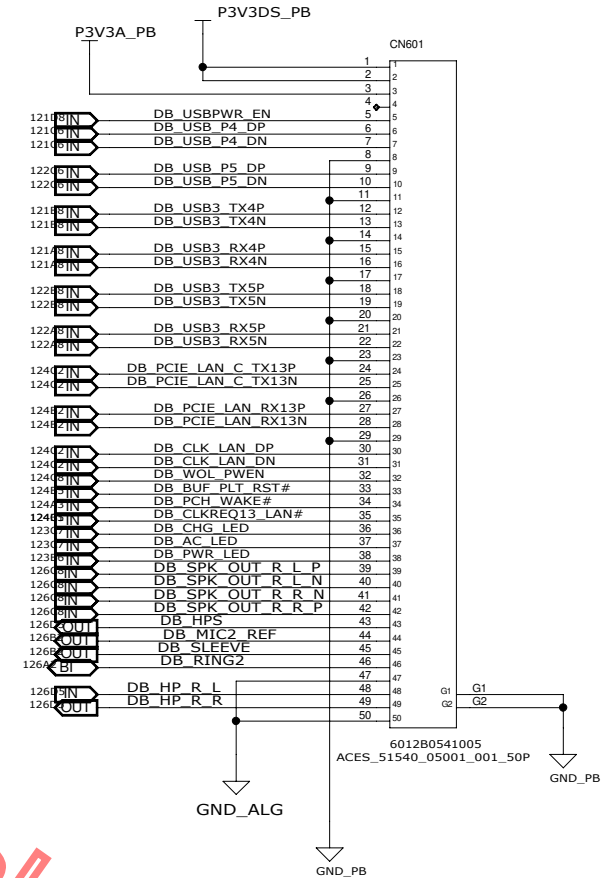
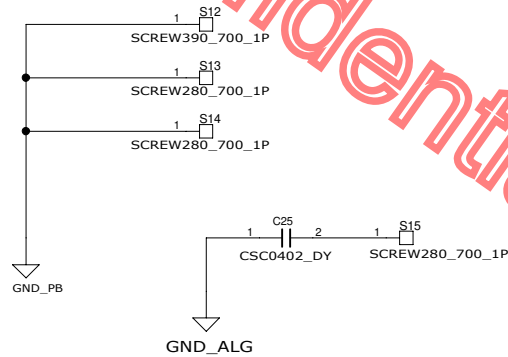
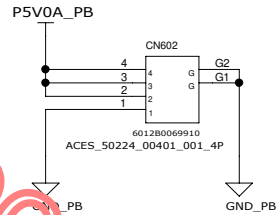
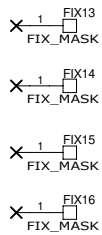
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Block Diagram				
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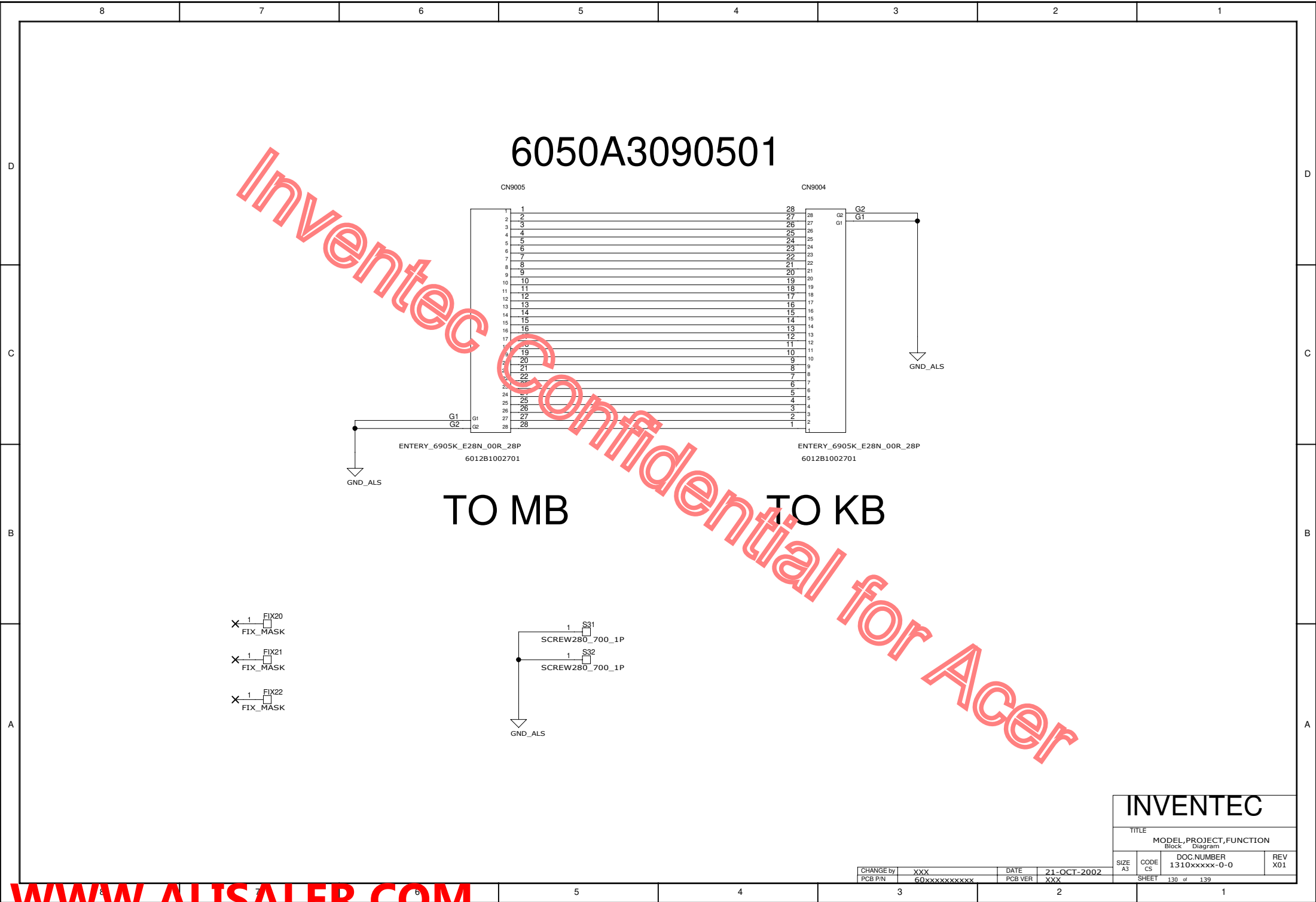
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TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

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BLOCK DIAGRAM															
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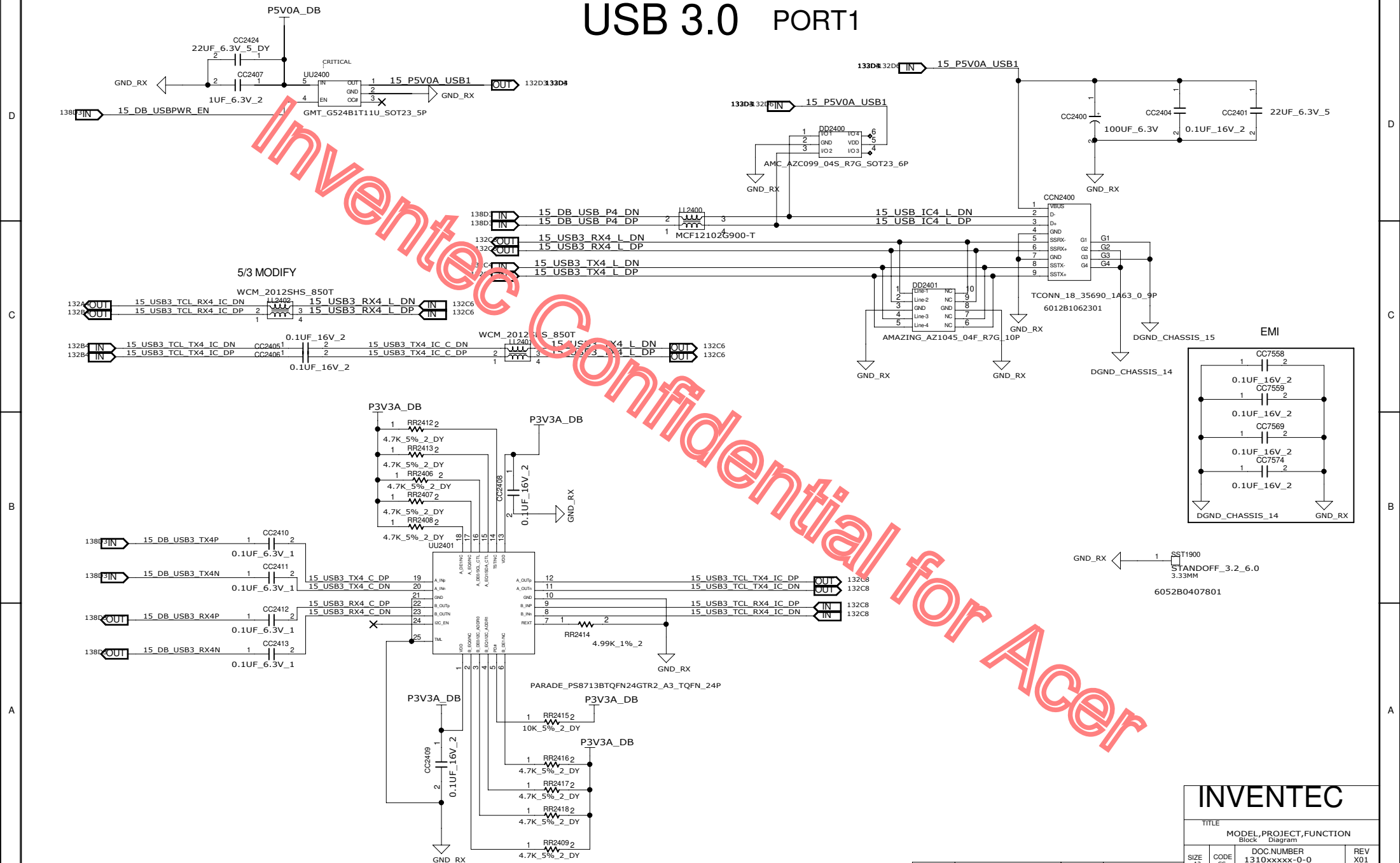
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MODEL, PROJECT, FUNCTION			
Block Diagram			
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CHANGE by	XXX	DATE	21-OCT-2002
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REFERENCE 2400~2450(USB3.0)

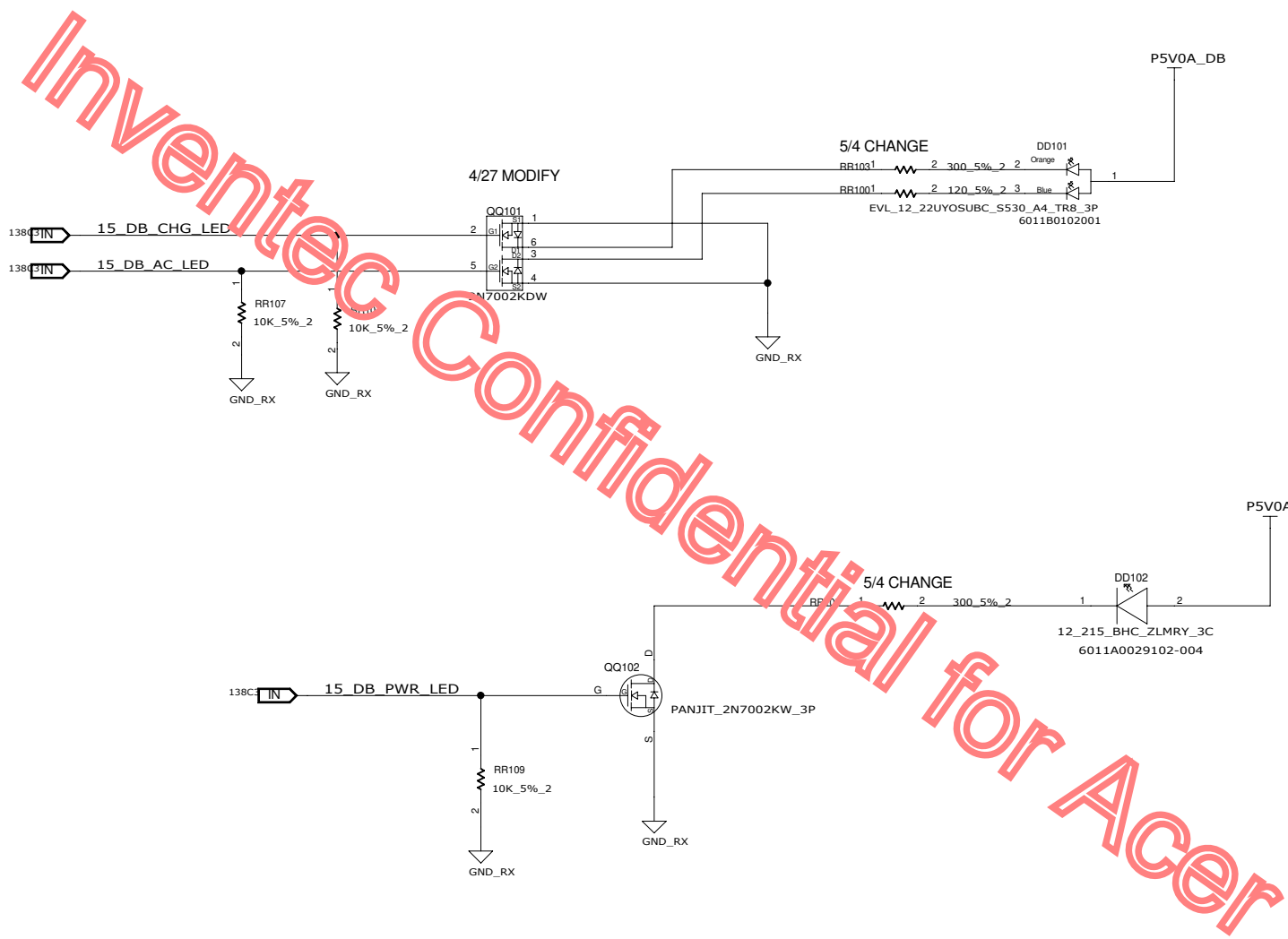
USB 3.0 PORT1



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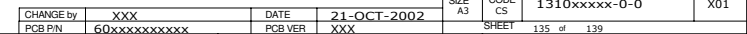
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Block Diagram			
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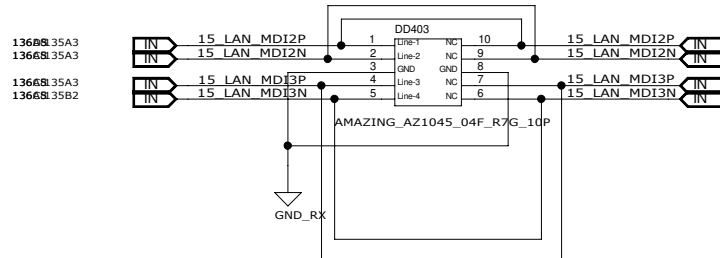
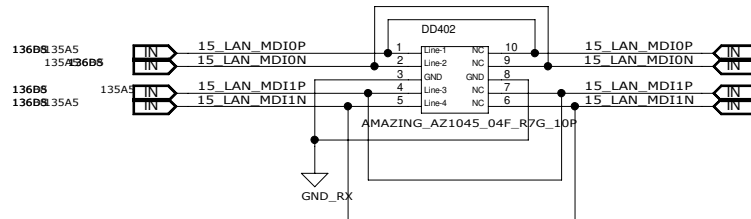
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TITLE MODEL, PROJECT, FUNCTION Block Diagram				
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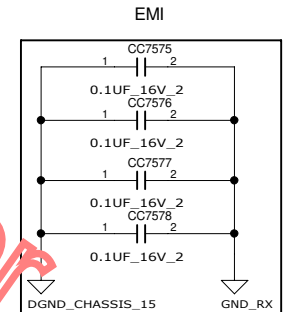
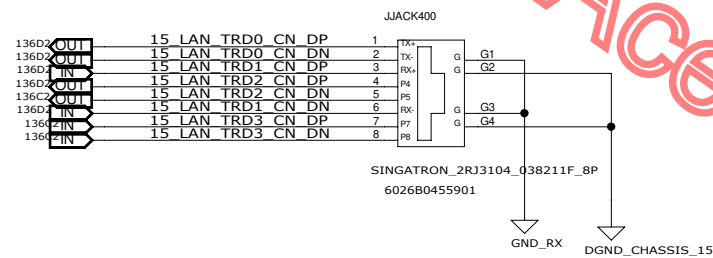
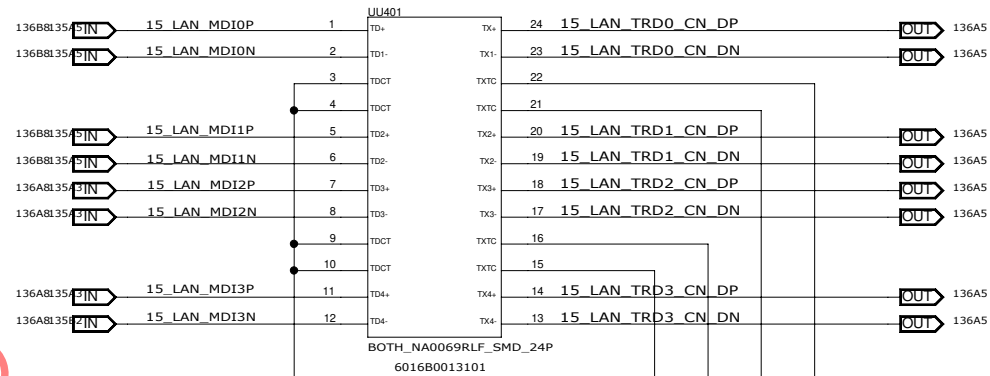


TRANSFORMER

ESD



RJ-45



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TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

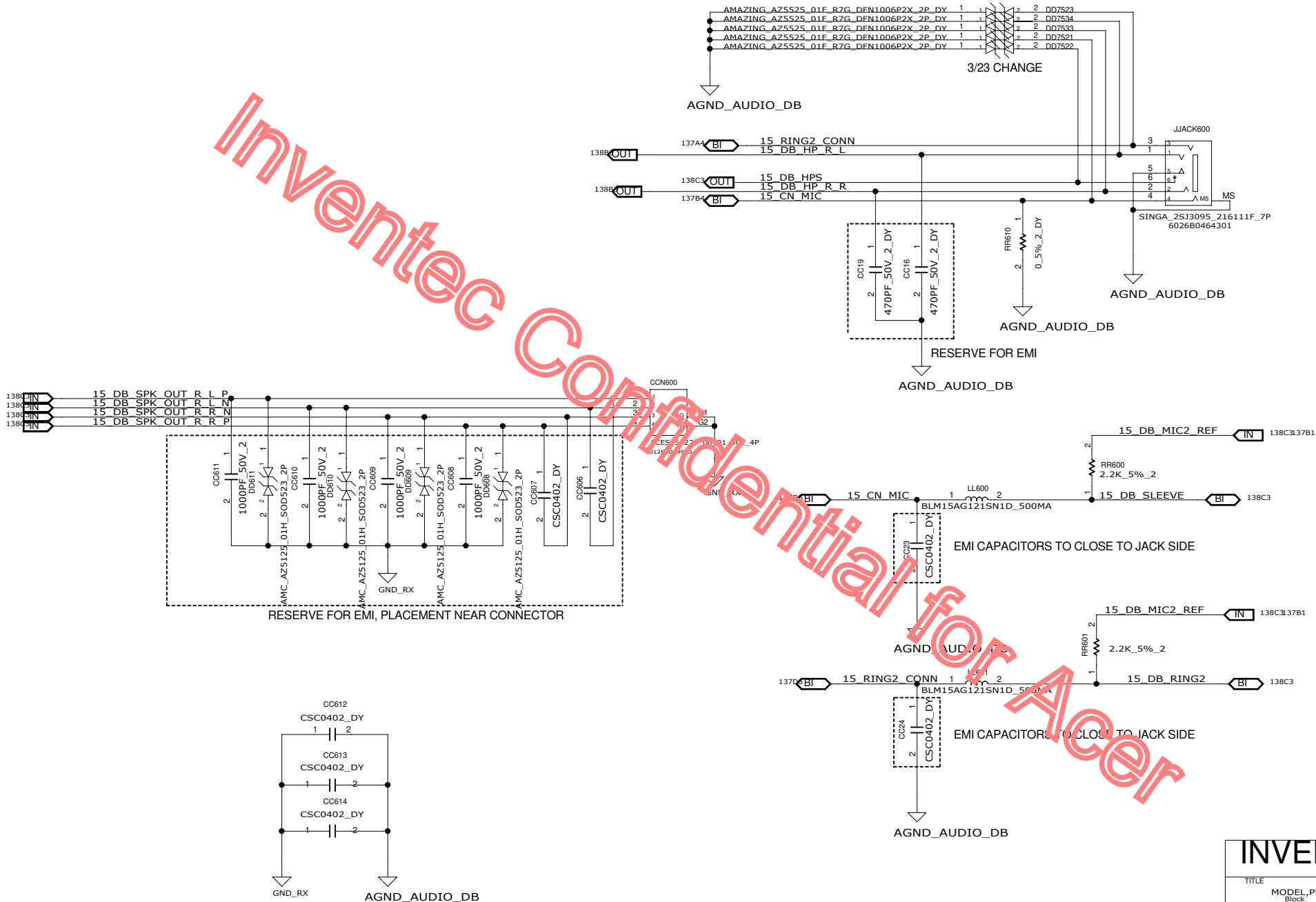
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INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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