


Compal Confidential

Model Name : Ezel_CX

Board NO: LA-A001P

PCB
ZZZ

LA-A001P REV0 M/B 5 S
DA8000WC210

DA8000WC200 PCB 0YO LA-A001P REV0 M/B 5 S
DA8000WC210 PCB 0YO LA-A001P REV1 M/B 5 S

updated for new panelization

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V5MM1 M/B Schematics Document

Intel Chief River (Ivy Bridge 2C BGA+ Pather Point)

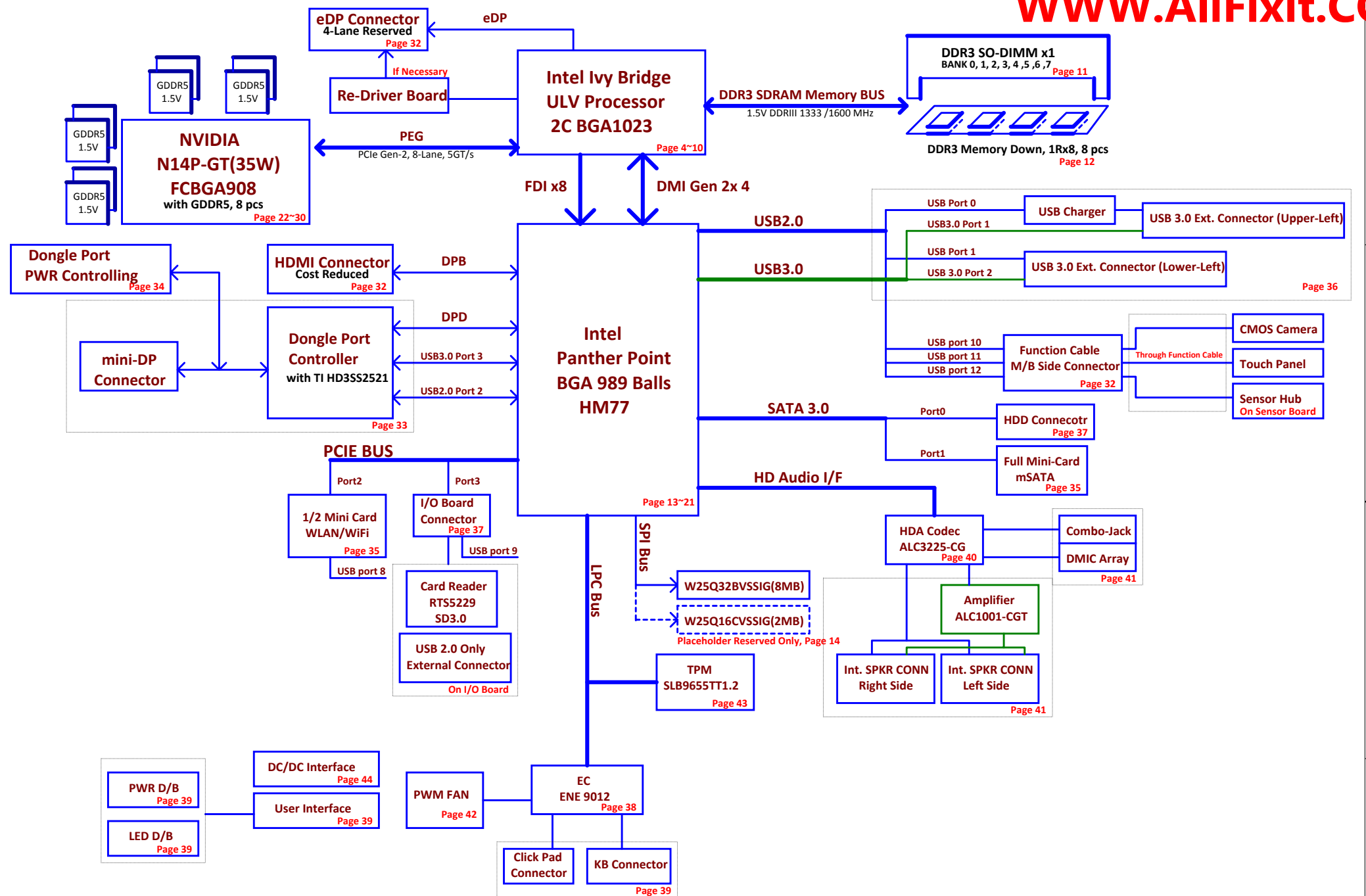
with On Board DRAM, 1Rx8, 8 pcs

Nvidia N14P-GT with GDDR5*8

2012-03-12

REV: 1.0

Panelization Information	
Main Board	LA-A001P
I/O Board	LS-A001P
Sensor Board	LS-A002P
Re-driver Board	LS-A003P
LAN Board	LS-A004P
LED Board	LS-A005P
PWR Board	LS-A006P
E-Compass Board	LS-A007P



System Power Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC power	ON	ON	ON	ON
VIN	Adapter power supply (19V)	N/A	ON	ON	ON
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+VSB	+VSB for power rails to control sequence	ON	ON	ON	ON
+CPU_CORE	Power Supply for CPU Core Power Well	ON	OFF	OFF	OFF
+VGFX_CORE	Power Supply for incorporated GPU	ON	OFF	OFF	OFF
+5VALW	5V Power Source from 3V/5V IC	ON	ON	ON	ON
+5VALW_PCH	5V Power Supply for PCH VccSus Power Well	ON	ON	ON*	ON*
+5VS	from 5VALW, power supply for 5V device	ON	OFF	OFF	OFF
+3VALW	3V Power Source from 3V/5V IC	ON	ON	ON	ON
+3VALW_PCH	3V Power Supply for PCH VccSus Powr Well	ON	ON	ON*	ON*
+3VS	from 3VALW, power supply for 3V device	ON	OFF	OFF	OFF
+VCCSA	power supply for CPU System Agent Voltage	ON	OFF	OFF	OFF
+1.8VS	use 3VALW source, for CPU VDDPLL and PCH LVDS power	ON	OFF	OFF	OFF
+1.5V	use 5VALW source, for DDR3 and for 1.5VS Gate	ON	ON	OFF	OFF
+1.5VS	from 1.5V, power supply for CPU memory controller and PCH	ON	OFF	OFF	OFF
+1.05VS_VTT	source from 5VALW, for CPU VCCIO and PCH Core Power Well	ON	OFF	OFF	OFF
+0.75VS	source from internal LDO of PU501, for DDR3 terminator	ON	OFF	OFF	OFF
+3V_LAN	3V power supply for RTL8111GS-CG LAN IC(on D/B)	ON	ON	OFF*	OFF*
+3VS_WLAN	3V power supply for WLAN	ON	OFF*	OFF*	OFF*
+3VS_DGPU	3V powr source for dGPU	ON	OFF	OFF	OFF
VGA_CORE	Core power for dGPU	ON	OFF	OFF	OFF
+1.5VSDGPU	1.5V for VRAM and memory controller of dGPU	ON*	OFF	OFF	OFF
+1.05VSDGPU	1.05V power source for dGPU	ON	OFF	OFF	OFF

ON*: if no need to disable for Erp Lot 6
OFF*: always connected is not supported by default
ON*: 1.5VSDGPU will be switched off by GC6 toggleed

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x b
Charger IC	0001 0010 b

EC SM Bus2 address

Device	Address
On Board Thermal Sensor	1001_101xb

PCH SM Bus address

Device	Address
ChannelA DIMM0 A0	1010 000X JDIMM1 (SPD)

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 port with charging (upper)
		1	USB3.0 port (lower)
	UHCI1	2	Lightning-Bolt with TI solution
		3	
	UHCI2	4	
		5	
	UHCI3	6	
EHCI2	UHCI4	7	
		8	Mini-Card for WiFi
	UHCI5	9	External port- USB 2.0 only
		10	CMOS Camera
	UHCI6	11	Touch Panel
		12	Sensor Hub

USB 3.0	Port	
XHCI	1	USB external port (upper)
	2	USB external port (lower)
	3	Lightning-Bolt with TI solution
	4	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	SLP_S6#	SLP_S7#	SLP_S8#
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

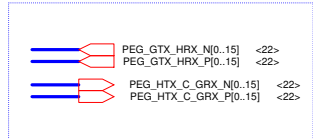
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
with dGPU	dGPU@
UMA Only	UMAO@
with GC6	GC6@
w/o GC6	NGC6@
daul-mode supported	DM@
EMI solution	EMI@
ESD solution	ESD@
RF solution	RF@
reserved for EMC	XEMC@
daul-mode not supported	NDM@
IOAC supported	IOAC@
no stuff	@
Connector	CONN@
i3-3227U	3227@
i5-3337U	3337@
i7-3537U	3537@
PCH HM77	HM77@
ELPIDA DRAM Chip	ELPIDA@
VRAM Hynix-MFR	HYNMFR@
VRAM Hynix-AFR	HYNAFR@

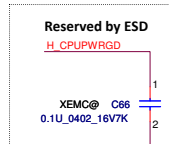
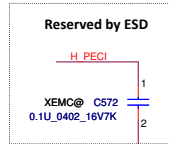
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/12/13	Deciphered Date	Date of EOP	Notes List	
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				Date: Wednesday, March 13, 2013	Sheet 3 of 64



Trace Width to R3= 12-mil
Trace Spacing to Other Signals= 15-mil
Routing Length= 500-mil

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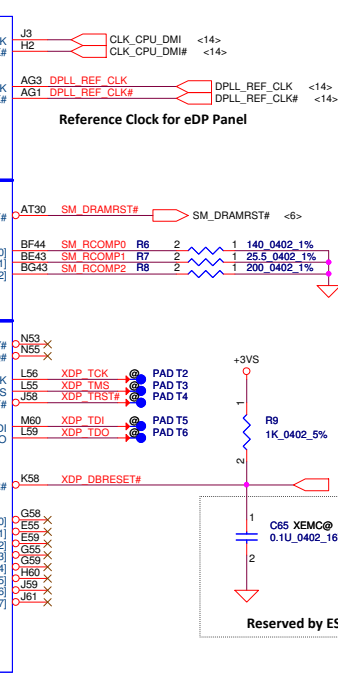
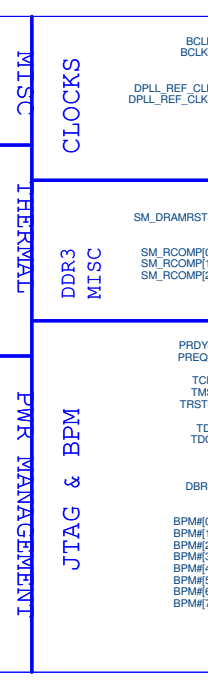
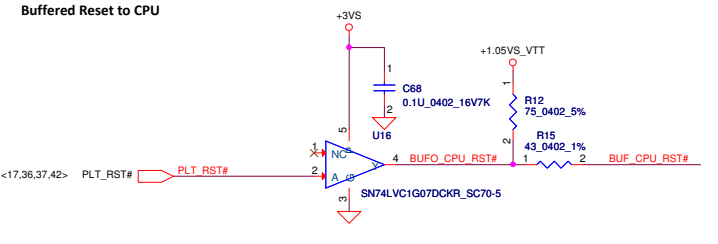
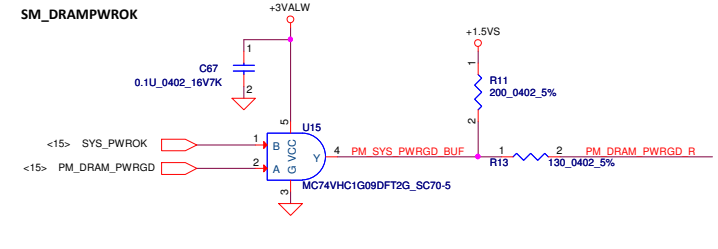
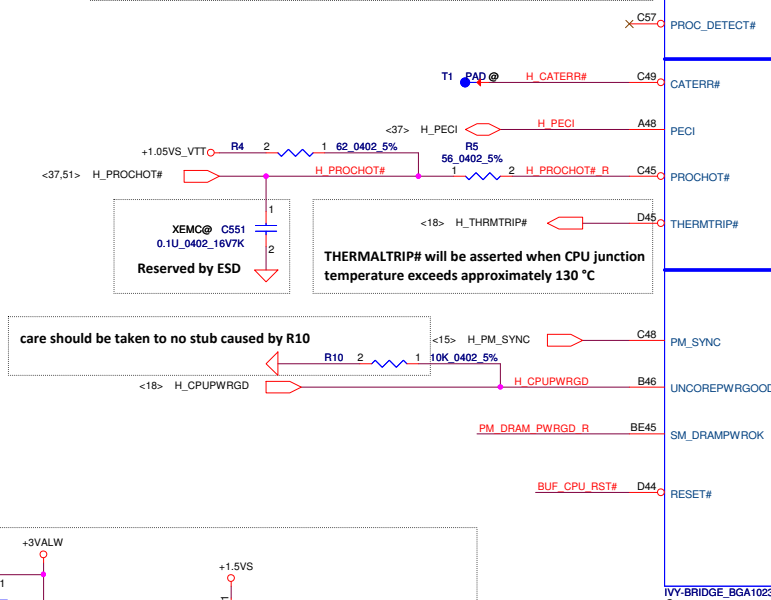
C572 should be as close as possible to CPU



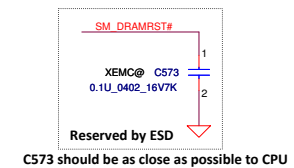
C66 should be as close as possible to CPU

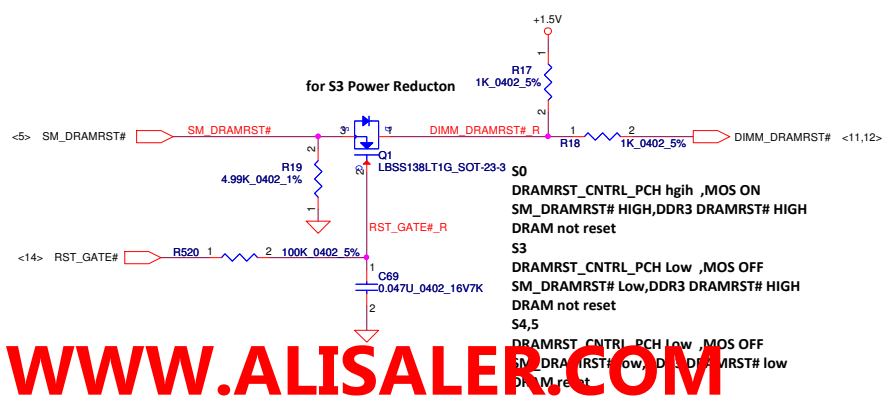
For 2nd Generation Intel® Core processor family mobile, the output will be high.
For Mobile 3rd Generation Intel® Core processor family, the output will be low.

<17> H_SNB_IVB#



	Width	Spacing	Length
SM_RCOMP0	20-mil	20-mil	< 500-mil
SM_RCOMP1	20-mil	20-mil	< 500-mil
SM_RCOMP2	15-mil	20-mil	< 500-mil



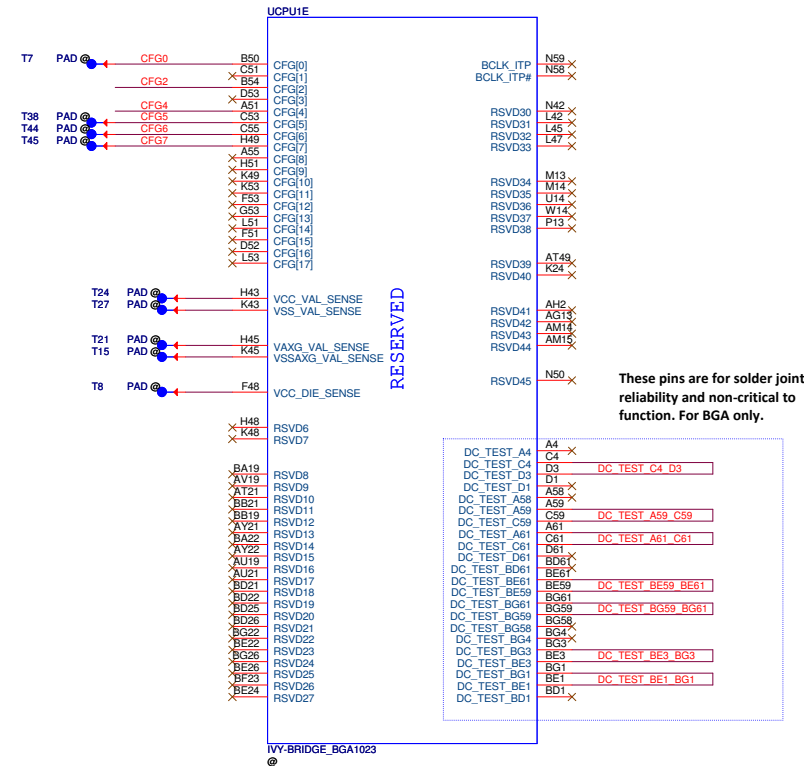


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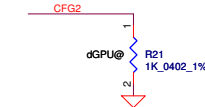
Docuement Number
Ezel_CX MB_LA-A001P

Rev
1.

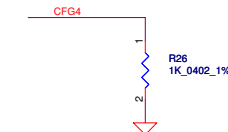
PEG DEFER TRAINING	
CFG7	<p>* 1: (Default) PEG Trains immediately and follows xxRESETB de-assertion</p> <p>0: PEG Wait for BIOS for training</p>



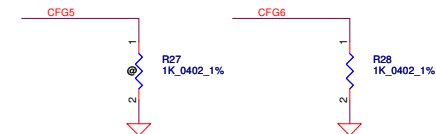
CFG Straps for Processor



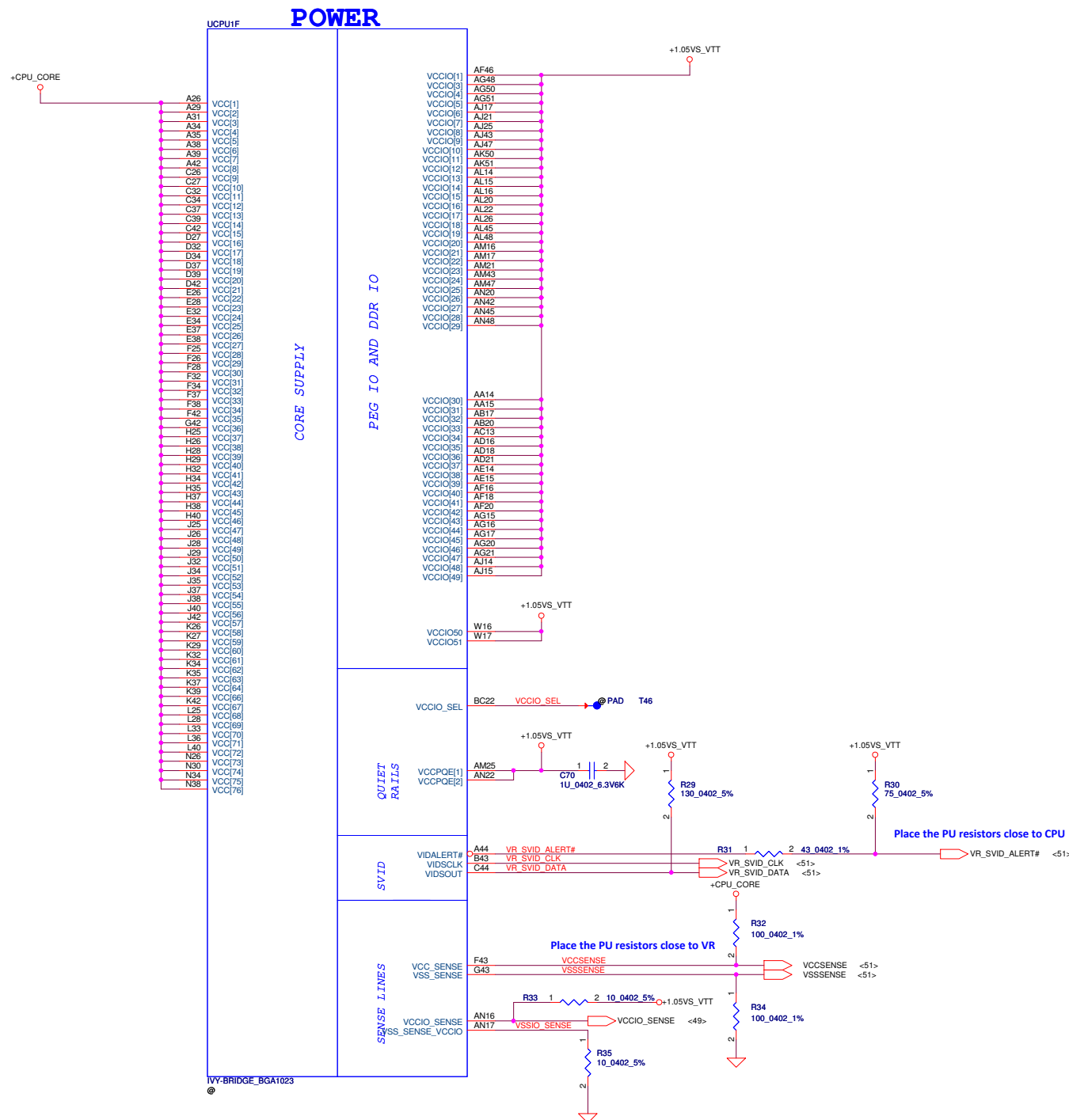
PCIe Static x16 Lane Numbering Reversal	
CFG2	<p>1: (Default) Normal Operation Lane # definition matches socket pin map definition</p> <p>* 0: Lane Reversed</p>



eDP Enable Strap	
CFG4	<p>1: (Default) Disable</p> <p>* 0: Enable</p>



PCIe Port Bifurcation Straps	
CFG[6:5]	<p>11: (Default) 1x16 PCI Express</p> <p>* 10: 2x8 PCI Express</p> <p>01: Reserved</p> <p>00: 1x8, 2x4 PCI Express</p>



CPU Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
VCC	0.65~1.2	33	Processor Core Voltage
VCCIO	1.05	8.5	Processor Uncore Voltage
VDDQ	1.5	5	Memory Controller Voltage
VCCSA	0.675~0.9	4	System Agent Voltage
VCCPLL	1.8	1.2	Processor PLL Voltage
VAXG	0.65~1.25	29	Processor Graphics Voltage

Refer to Mobile 3rd Generation Intel® Core Processor Family External Design Specification (EDS) Volume 1 of 2 Revision 2.2

POWER

UCPU1G

+VGFX_CORE
DC 29A

AA46 VAXG[1]
AB47 VAXG[2]
AB50 VAXG[3]
AB51 VAXG[4]
AB53 VAXG[5]
AB55 VAXG[6]
AB56 VAXG[7]
AB58 VAXG[8]
AB59 VAXG[9]
AC61 VAXG[10]
AD47 VAXG[11]
AD48 VAXG[12]
AD50 VAXG[13]
AD52 VAXG[14]
AD53 VAXG[15]
AD55 VAXG[16]
AD56 VAXG[17]
AD58 VAXG[18]
AD59 VAXG[19]
AE46 VAXG[20]
AE47 VAXG[21]
AE48 VAXG[22]
AE49 VAXG[23]
F47 VAXG[24]
P48 VAXG[25]
P50 VAXG[26]
P51 VAXG[27]
P52 VAXG[28]
P53 VAXG[29]
P55 VAXG[30]
P56 VAXG[31]
T48 VAXG[32]
T58 VAXG[33]
T59 VAXG[34]
T61 VAXG[35]
U46 VAXG[36]
V47 VAXG[37]
V48 VAXG[38]
V50 VAXG[39]
V51 VAXG[40]
V52 VAXG[41]
V53 VAXG[42]
V55 VAXG[43]
V56 VAXG[44]
V58 VAXG[45]
V59 VAXG[46]
W50 VAXG[47]
W51 VAXG[48]
W52 VAXG[49]
W53 VAXG[50]
W55 VAXG[51]
W56 VAXG[52]
W61 VAXG[53]
Y48 VAXG[54]
Y61 VAXG[55]
Y61 VAXG[56]

GRAPHICS

DDR3 - 1.5V RAILS

QUIET RAILS

SENSE LINES

1.8V RAIL

SA RAIL

SENSE LINES

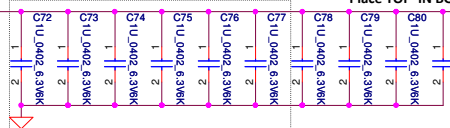
VCCSA VID Lines

SM_VREF
SA_DIMM_VREFDO
SB_DIMM_VREFDO

5A

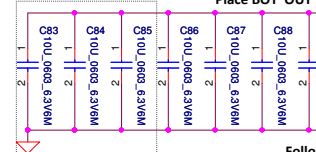
VDDQ[1] AJ28
VDDQ[2] AJ33
VDDQ[3] AJ36
VDDQ[4] AL30
VDDQ[5] AL34
VDDQ[6] AL38
VDDQ[7] AL42
VDDQ[8] AM33
VDDQ[9] AM36
VDDQ[10] AM40
VDDQ[11] AN30
VDDQ[12] AN34
VDDQ[13] AN38
VDDQ[14] AR26
VDDQ[15] AR28
VDDQ[16] AR30
VDDQ[17] AR32
VDDQ[18] AR34
VDDQ[19] AR36
VDDQ[20] AR40
VDDQ[21] AV41
VDDQ[22] AW26
VDDQ[23] BA40
VDDQ[24] BB28
VDDQ[25] BC33
VDDQ[26]

stuff for first version then check the feasibility to remove them



Place TOP IN BGA

Place BOT OUT BGA

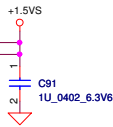


Follow VDDQ 1.5V-Rail Decoupling Recommendation from Intel PDDG Rev 1.0,

1. 1x 330uF
2. 8x 10uF (0603)
3. 10x 1uF (0402)

stuff for first version then check the feasibility to remove them

VCCDQ[1] AM28
VCCDQ[2] AN26



*For ULV Only

VID[0] ball D48	VID[1] ball D49	VCCSA Output
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VDDQ_SENSE
VSS_SENSE_VDDQ

BC43
BA43

VCCSA_SENSE

U10

D48 H_VCCSA_VID0

D49 H_VCCSA_VID1

H_VCCSA_VID0

H_VCCSA_VID1

<50>

<50>

VAXG_SENSE
VSSAXG_SENSE

BB3
BC1
BC4

VCCPLL[1]
VCCPLL[2]
VCCPLL[3]

BB3
BC1
BC4

VCCSA[1]
VCCSA[2]
VCCSA[3]
VCCSA[4]
VCCSA[5]
VCCSA[6]
VCCSA[7]
VCCSA[8]
VCCSA[9]
VCCSA[10]
VCCSA[11]
VCCSA[12]
VCCSA[13]
VCCSA[14]
VCCSA[15]
VCCSA[16]

L17
N16
N20
N22
P17
P20
R16
R18
R21
U15
V18
V17
V18
V18
V21
V20

IVYBRIDGE_BGA1023

6A

C92
C94
C95

10uF 0402 6.3V6K

10uF 0402 6.3V6K

10uF 0402 6.3V6K

10uF 0402 6.3V6K

10uF 0402 6.3V6K

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10uF 0402 6.3V6K

10uF 0402 6.3V6K

10uF 0402 6.3V6K

Follow VCCSA Plane Decoupling Recommendations from Intel PDDG Rev 1.0,

1. 1x 330uF
2. 5x 10uF (0603)
3. 5x 1uF (0402)

stuff for first version then check the feasibility to remove them

stuff for first version then check the feasibility to remove them

stuff for first version then check the feasibility to remove them

Follow VCCSA Plane Decoupling Recommendations from Intel PDDG Rev 1.0,

1. 1x 330uF
2. 5x 10uF (0603)
3. 5x 1uF (0402)

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Follow VCCSA Plane Decoupling Recommendations from Intel PDDG Rev 1.0,

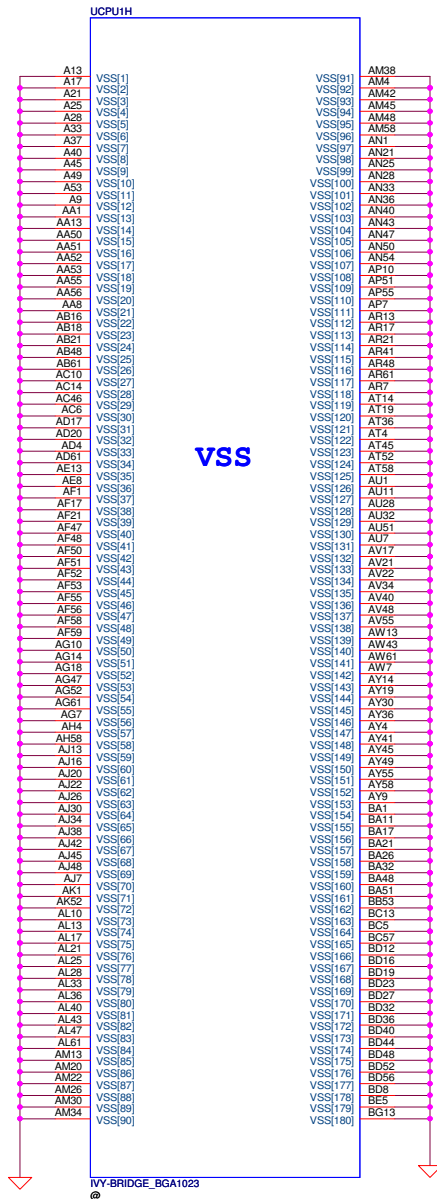
1. 1x 330uF
2. 5x 10uF (0603)
3. 5x 1uF (0402)

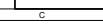
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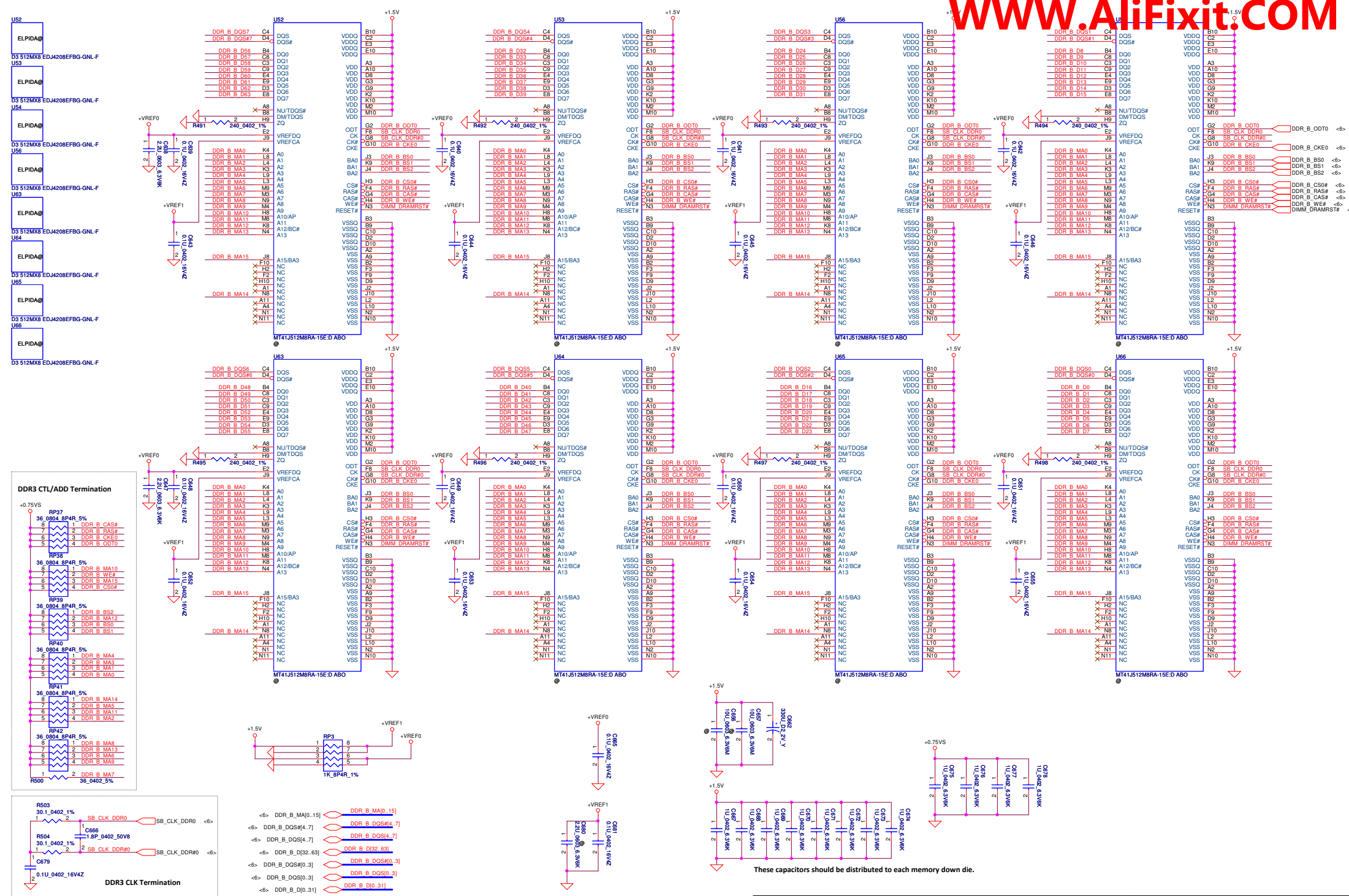
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Issued Date	2012/07/29	Deciphered Date	Date of EOP	PROCESSOR(6/7) PWR
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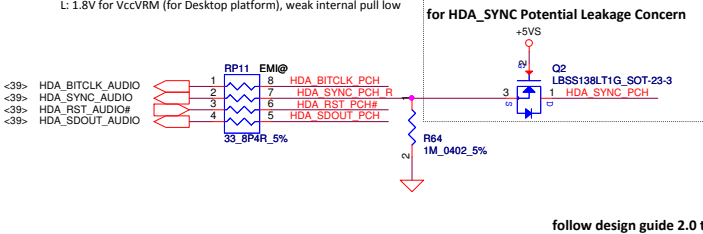
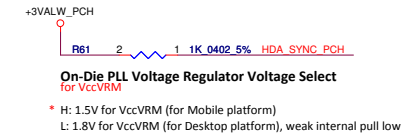
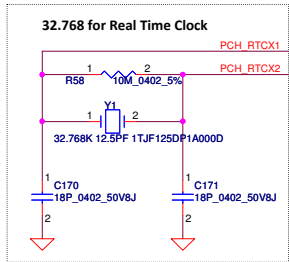
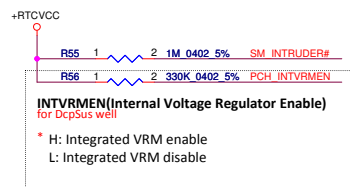
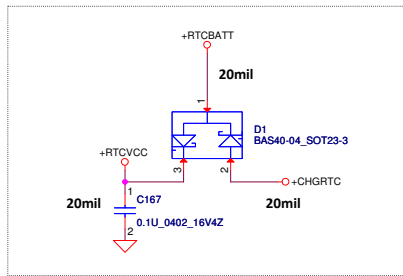




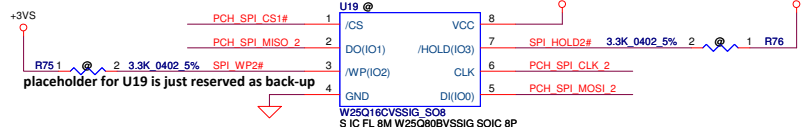
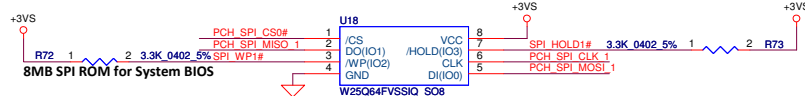
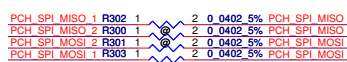
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				Date: Wednesday, March 13, 2013	Rev 1.0
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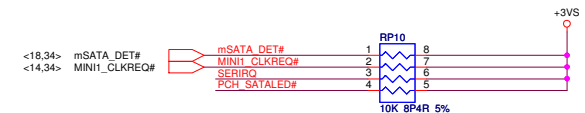
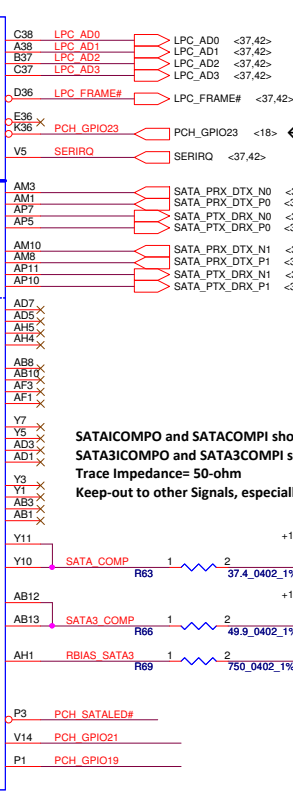
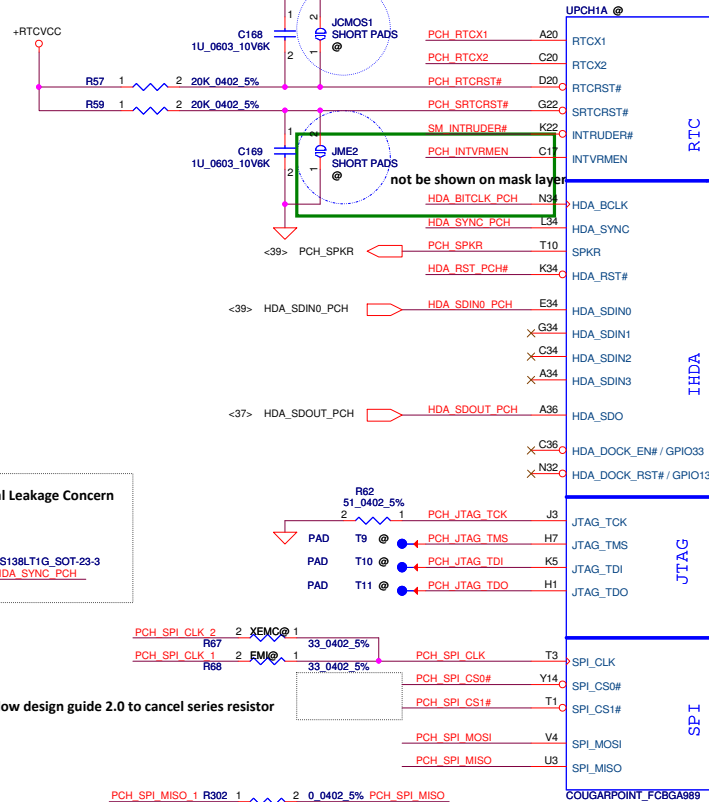
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							DDRIII DIMMB
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Date:	Wednesday, March 13, 2013	Sheet		12		of 64	



follow design guide 2.0 to cancel series resistor



Both JCMOS1 and JME2 should be placed close to JDIMM1

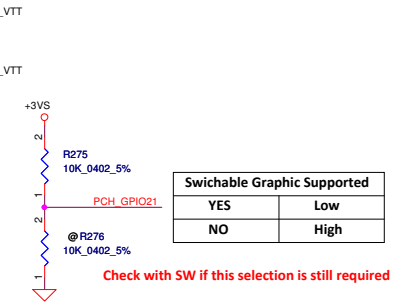


← On Board DRAM Flag

SATA Port 0 is for HDD Connector

SATA Port 0 is for SSD

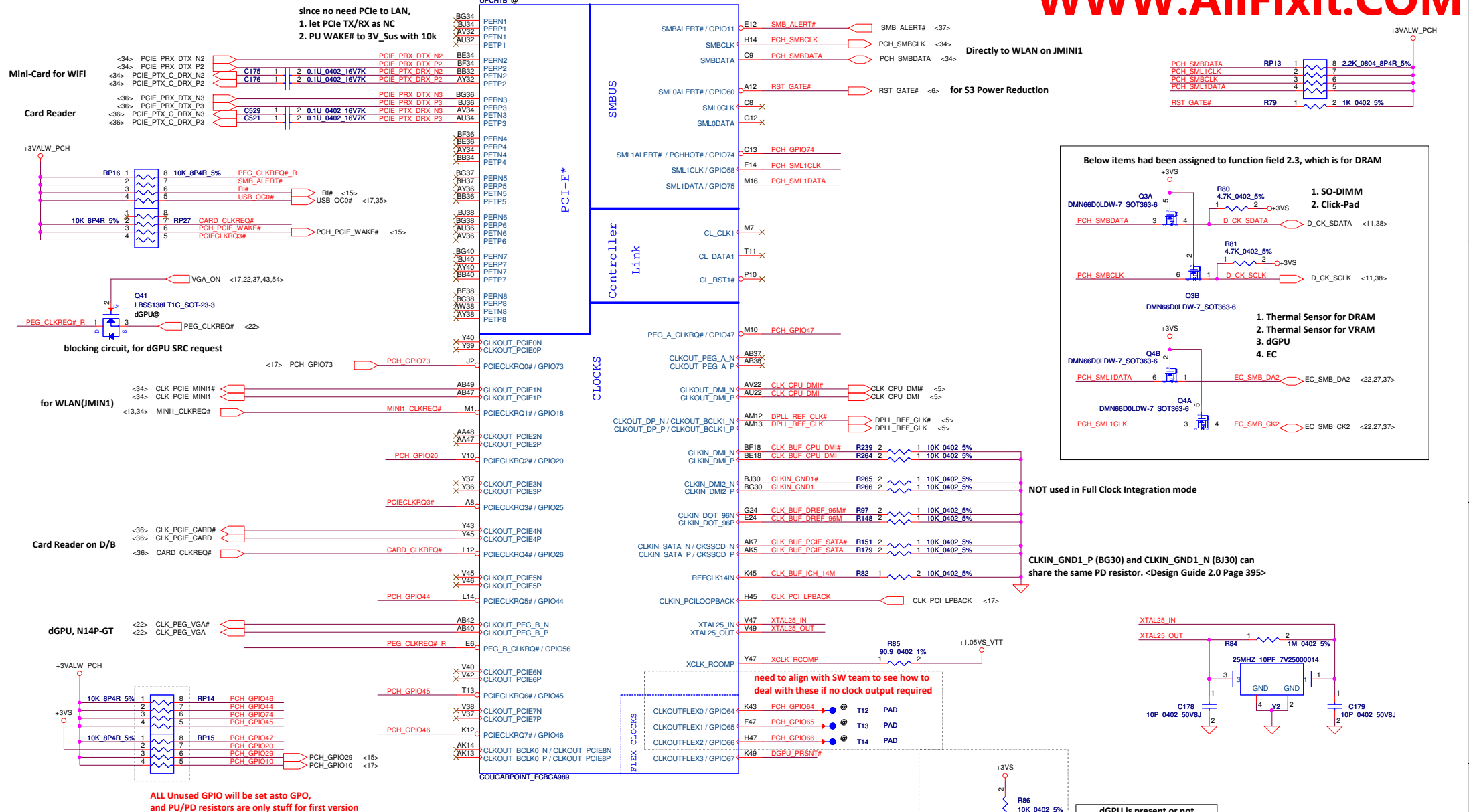
SATAICOMPO and SATACOMPI should be connected together then to R63.
SATA3ICOMPO and SATA3COMPI should be connected together then to R66.
Trace Impedance= 50-ohm
Keep-out to other Signals, especially to CLK= 15-mil

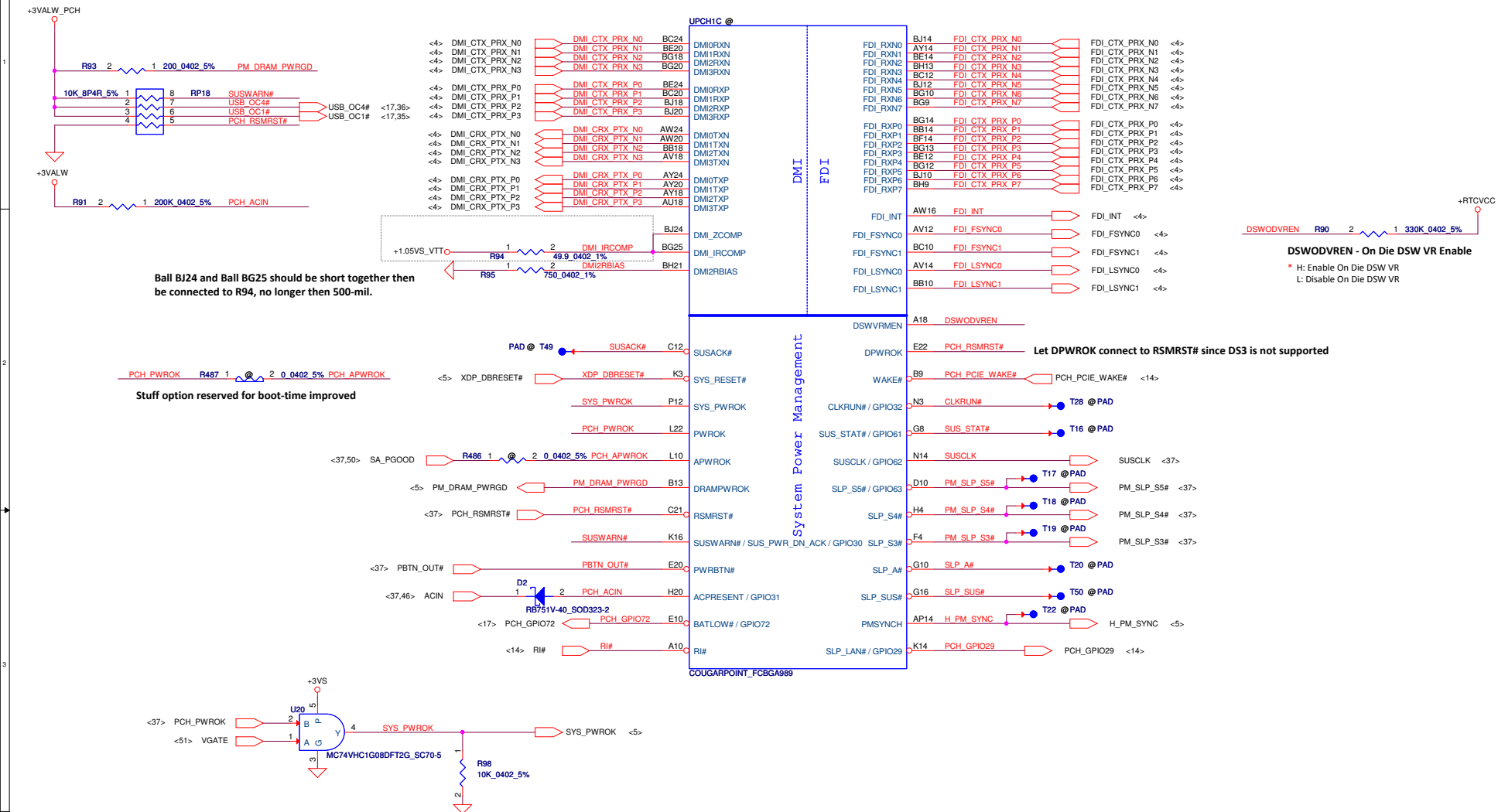


In accordance with design guide 2.0 page 274, if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary.

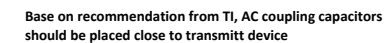
Boot BIOS Destination Selection		
Routing	GTN1# / GPIO51 (BBS1)	SATA1GP / GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1

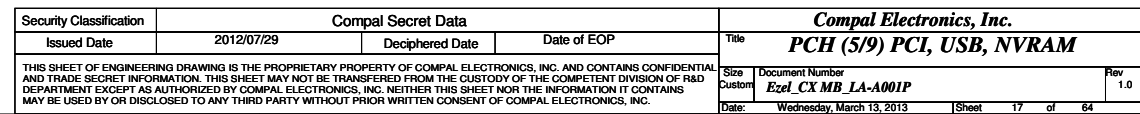
keep R still be stuff for safety SMT, then check if it is okay to remove or not

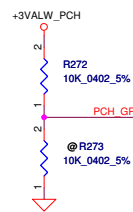
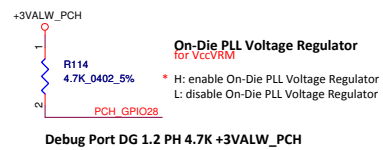




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				Date: Wednesday, March 13, 2013	Sheet 15 of 64

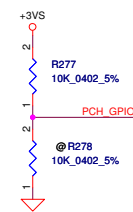






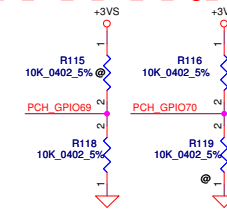
Check with SW if this selection is still required

DDR3/DDR3L	
DDR3	High
DDR3L	Low



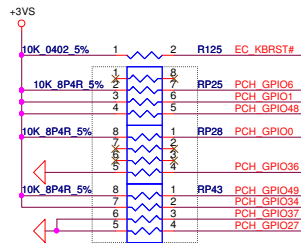
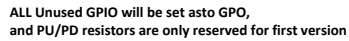
Check with SW if this selection is still required

GDDR3/GDDR5	
GDDR3	Low
GDDR5	High



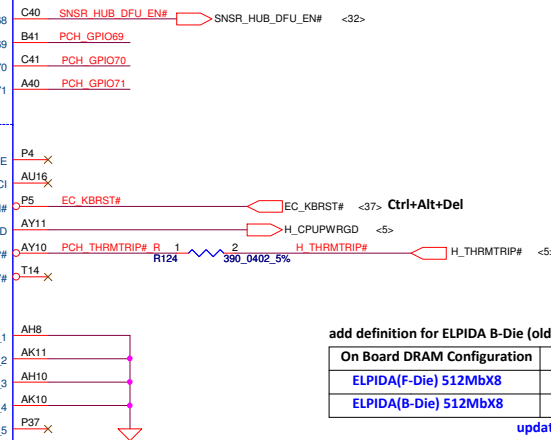
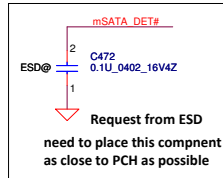
Project Code	GPIO69	GPIO70
	0	0
w/TPM	0	1
	1	0
	1	1

Currently, to be the same configuration as Sage, use GPIO69 and GPIO70 to define SKUs has TPM solution or not. **updated on 2013/01/15**



GPI071 is for GDDR3/GDDR5 selection.
PU for GDDR5 only.

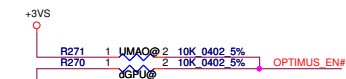
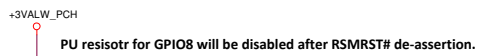
**ALL Unused GPIO will be set as GPO,
and PU/PD resistors are only stuff for first version**



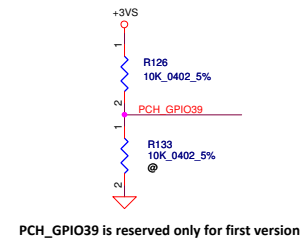
add definition for ELPIDA B-Die (old die)

On Board DRAM Configuration	GPIO23	GPIO22
ELPIDA(F-Die) 512MbX8	0	0
ELPIDA(B-Die) 512MbX8	0	1

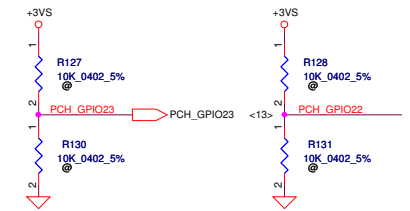
updated on 2013/01/15



NV Optimus Enable	
W/Optimus	Low
W/O Optimus	High



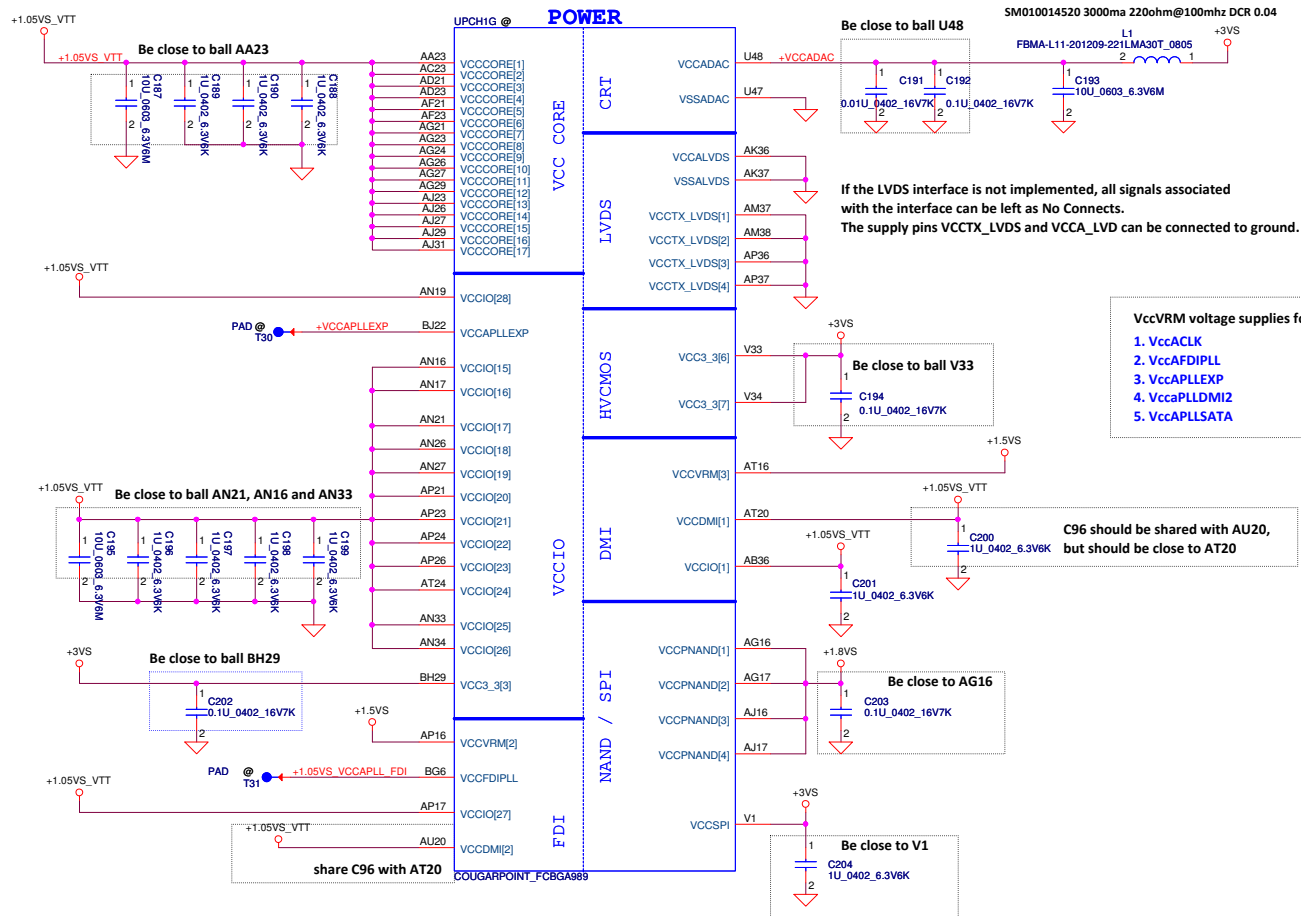
PCH_GPIO39 is reserved only for first version



Being configured by ALT Group

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Date:				Wednesday, March 13, 2013	Sheet	18 of 64

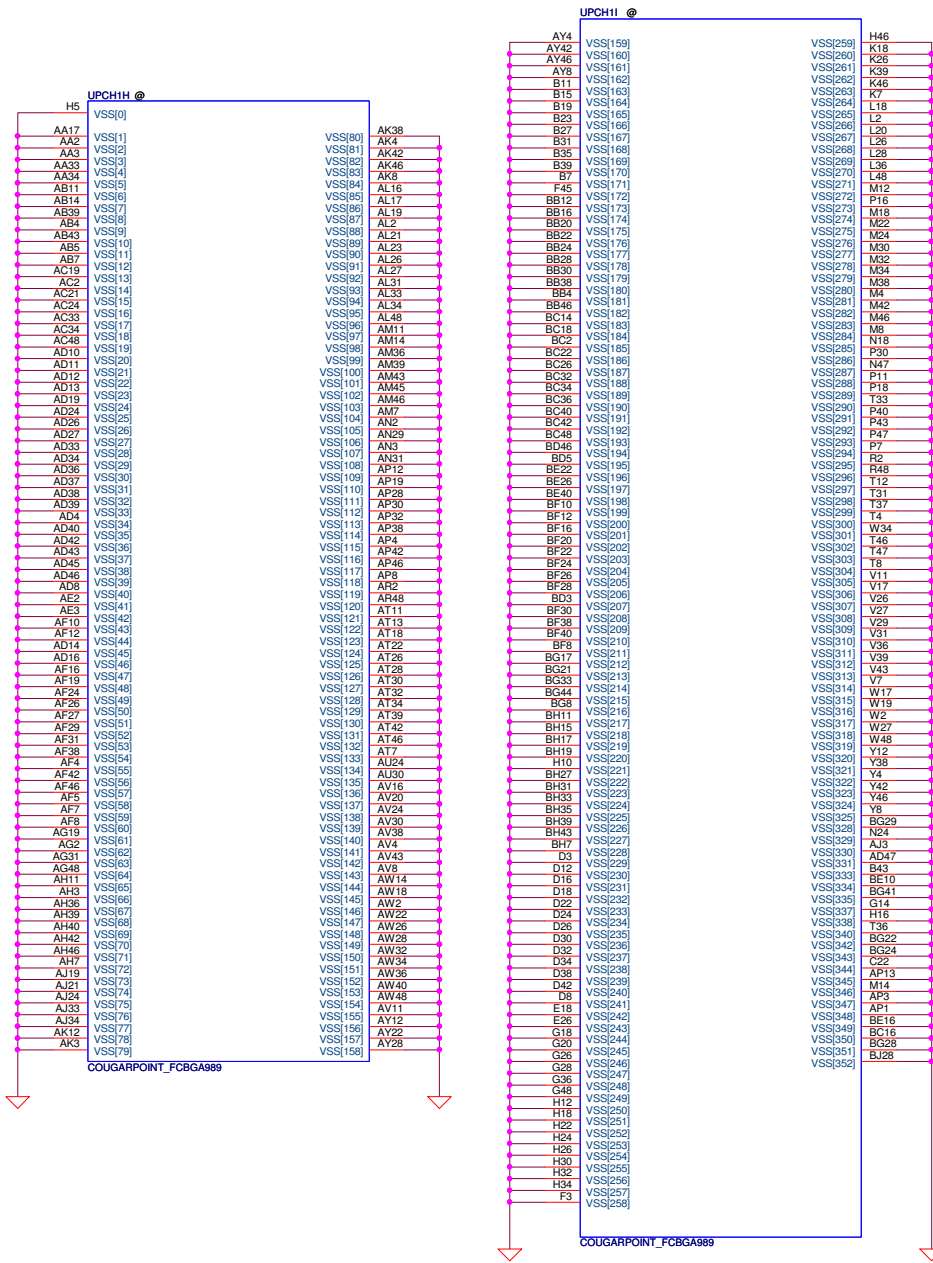
Refer to Intel® 7 Series / C216 Chipset Family Platform Controller Hub (PCH) External Design Specification (EDS) Revision 2.1

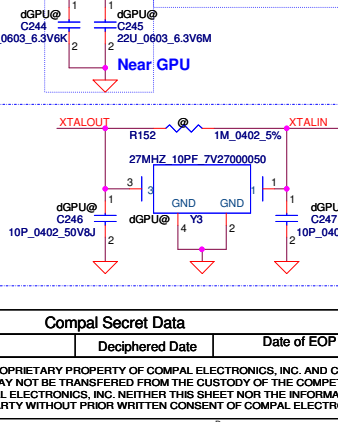
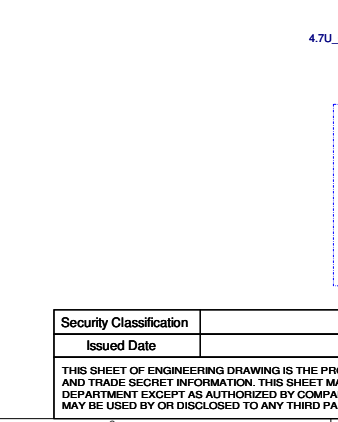
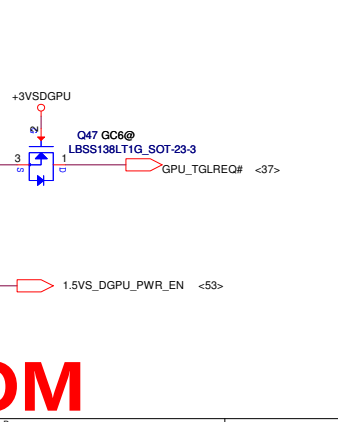
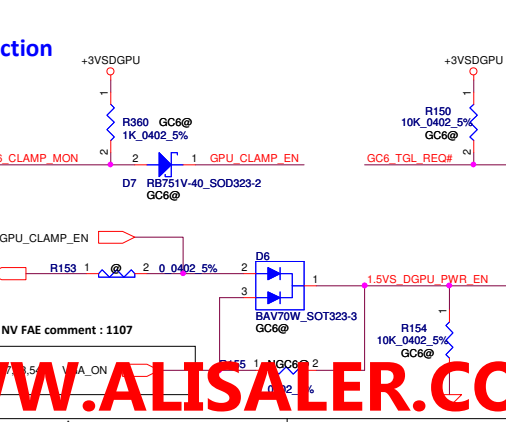
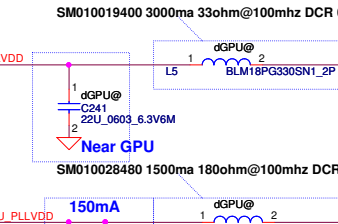
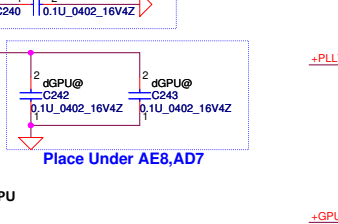
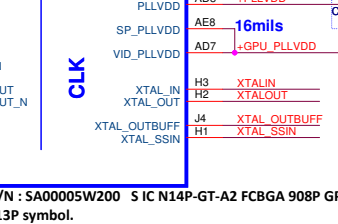
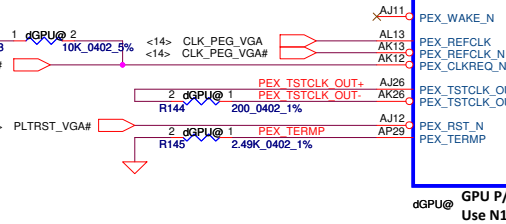
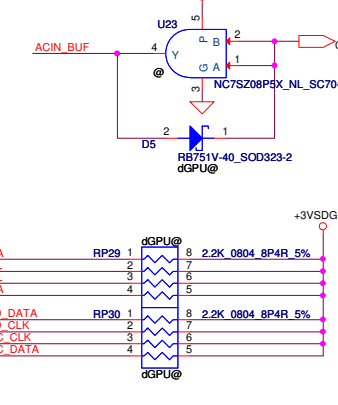
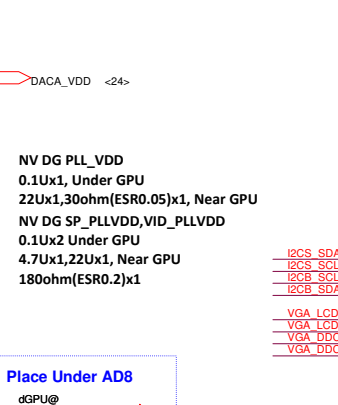
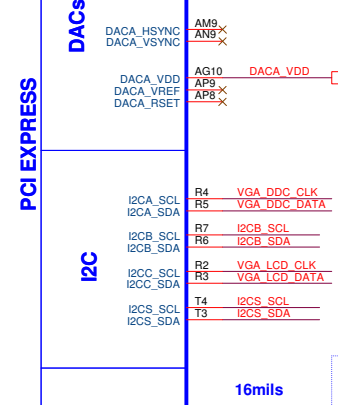
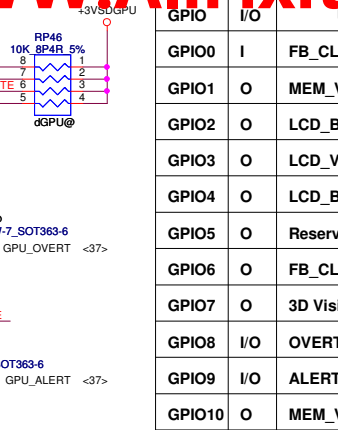
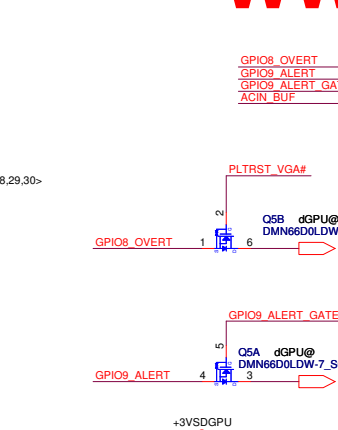
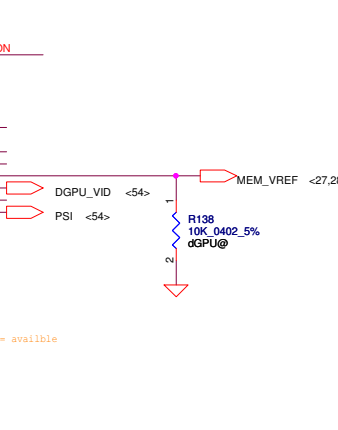
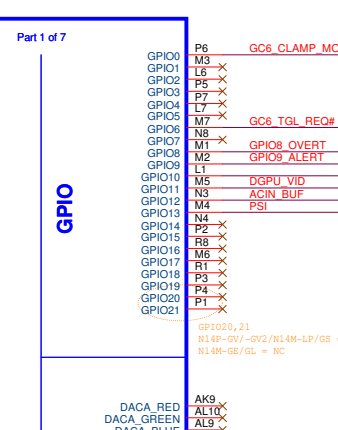
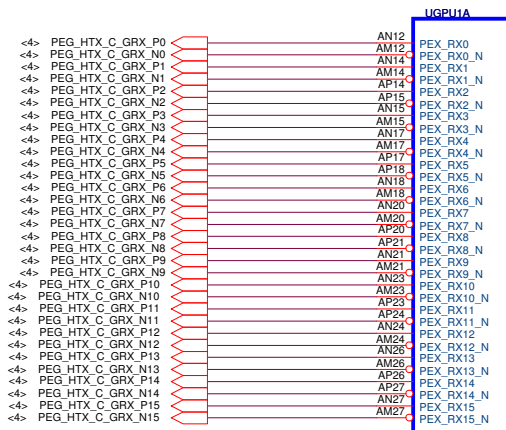


PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/O
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltage
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLL	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW3_3	3.3	0.001	3.3v supply for Deep Sx well
VccDFTERN (VccPNAND)	1.8	0.002	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	RTC Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.5	0.147	1.5 V Internal PLL and VRMs
VccCLKDMI	1.05	0.075	DMI differential Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.05	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.04	I/O power supply for LVDS (Mobile Only)



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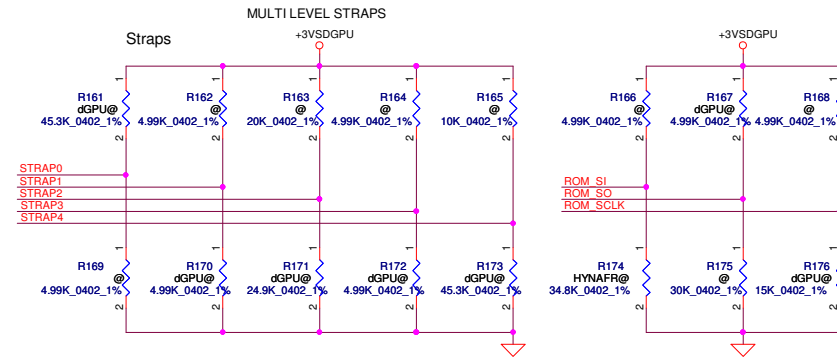
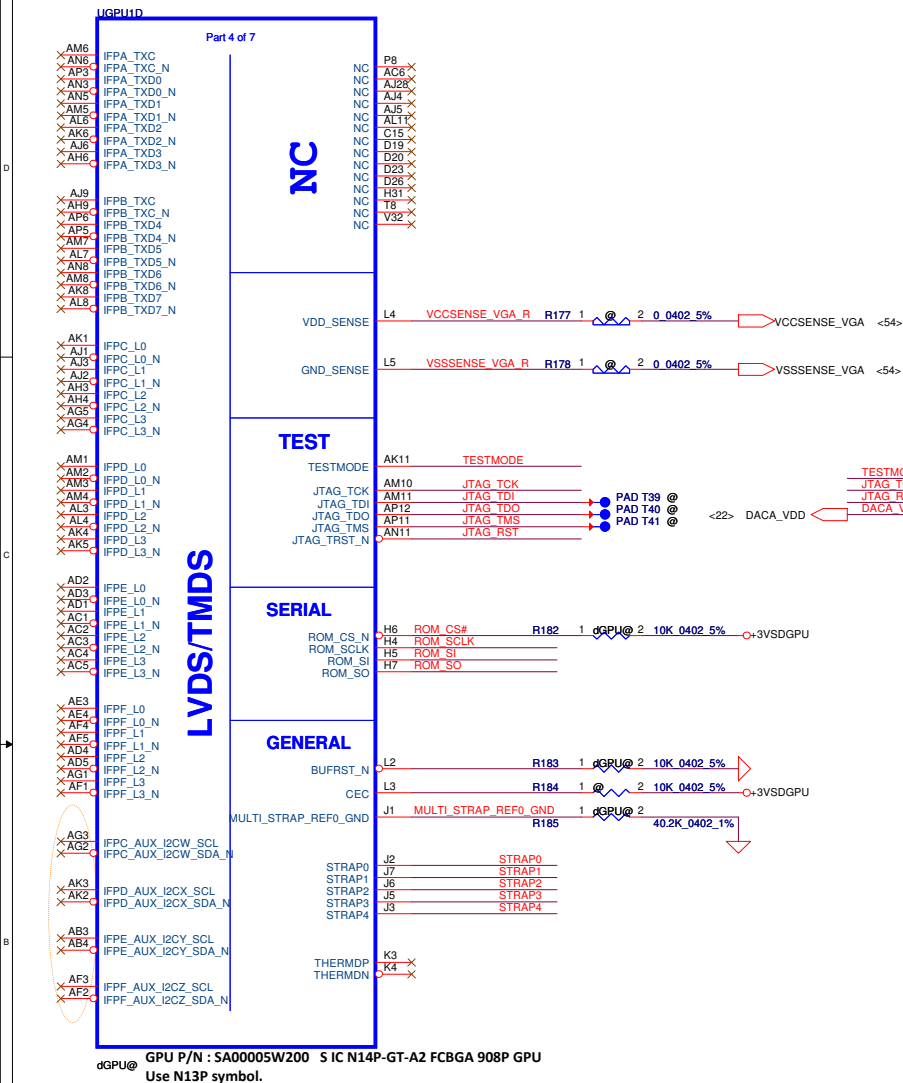


GPIO	I/O	USAGE
GPIO0	I	FB_CLAMP_MON
GPIO1	O	MEM_VD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	Reserved
GPIO6	O	FB_CLAMP_TGL_REQ
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	O	FRM_CLK
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21		Reserved

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VRAM BOM Config

VRAM P/N

128Mx16x8 HYN 64*32 SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABOI)

For N14P-GT-A2(QS) strap table

Device ID : 0xFE4

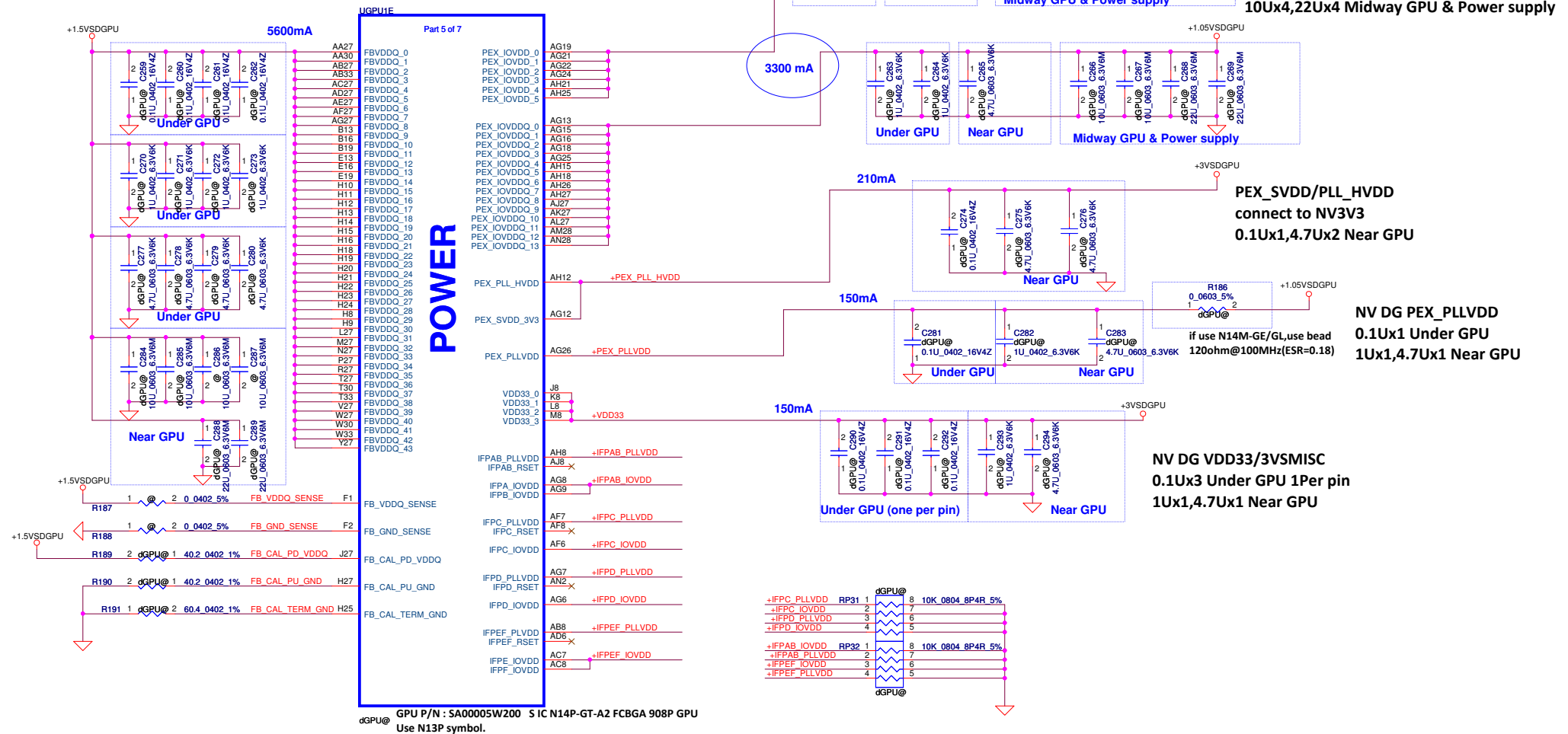
GDDR5	Vendor	Strap	ROM_SI
128M x 16	Hynix	0x4	24.9K

GPU	WCK Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GT	2.5GHZ	128M*16	Hynix	R PU 45K	R PD 5K	R PD 25K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PD 15K

Resistor Values	Pull-up	Pull-down
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]
STRAP3	SOR[3:0]
STRAP4	PEG_SPEED_CHANGE_GEN3, PEX_MAX_SPEED, DP_PLLVDD33V
ROM_SCLK	PCI_DEV[4], SUB_VENDOR, PCI_DEV[5], PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3:0]
ROM_SO	FB_BAR_SIZE[1:0], SMB_ ALT_ADDR, VGA_DEVICE

NV 14x DG FBVDDQ(GDDR5) GB4-128
0.1Ux4,1Ux4 Under GPU
4.7Ux4,10Ux2,22Ux2 Near GPU



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				Date	Wednesday, March 13, 2013	Sheet

UGPU1F

Part 6 of 7

A2	GND_0	D2
AA17	GND_1	D31
AA18	GND_2	D33
AA20	GND_3	E10
AA22	GND_4	E22
AB12	GND_5	E25
AB14	GND_6	E5
AB16	GND_7	E7
AB19	GND_8	E28
AB2	GND_9	F7
AB21	GND_10	G10
A33	GND_11	G13
AB23	GND_12	G16
AB28	GND_13	G19
AB30	GND_14	G2
AB32	GND_15	G25
AB5	GND_16	G28
AB7	GND_17	G3
AC13	GND_18	G30
AC15	GND_19	G32
AC17	GND_20	G33
AC18	GND_21	G5
AA13	GND_22	G7
AC20	GND_23	K2
AC22	GND_24	K28
AE2	GND_25	K30
AE28	GND_26	K32
AE30	GND_27	K33
AE32	GND_28	K5
AE33	GND_29	K7
AE5	GND_30	M13
AE7	GND_31	M15
AH10	GND_32	M17
AA15	GND_33	M18
AH13	GND_34	M20
AH16	GND_35	M22
AH19	GND_36	N12
AH2	GND_37	N14
AH22	GND_38	N16
AH24	GND_39	N19
AH28	GND_40	N2
AH29	GND_41	N21
AH30	GND_42	N23
AH32	GND_43	N28
AH33	GND_44	N30
AH5	GND_45	N32
AH7	GND_46	N33
AJ7	GND_47	N5
AK10	GND_48	N7
AK7	GND_49	P13
AL12	GND_50	P15
AL14	GND_51	P17
AL15	GND_52	P18
AL17	GND_53	P20
AL18	GND_54	P22
AL2	GND_55	R12
AL20	GND_56	R14
AL21	GND_57	R16
AL23	GND_58	R19
AL24	GND_59	R23
AL26	GND_60	R23
AL28	GND_61	T13
AL30	GND_62	T15
AL32	GND_63	T17
AL33	GND_64	T18
AL5	GND_65	T2
AM13	GND_66	T20
AM16	GND_67	T22
AM19	GND_68	AG11
AM22	GND_69	T28
AM25	GND_70	T32
AN1	GND_71	T5
AN10	GND_72	T7
AN13	GND_73	U12
AN16	GND_74	U14
AN19	GND_75	U16
AN22	GND_76	U19
AN25	GND_77	U21
AN30	GND_78	U23
AN34	GND_79	V12
AN4	GND_80	V14
AN7	GND_81	V16
AP2	GND_82	V19
AP33	GND_83	V21
B1	GND_84	V23
B10	GND_85	W13
B22	GND_86	W15
B25	GND_87	W17
B28	GND_88	W18
B31	GND_89	W20
B34	GND_90	W22
B4	GND_91	W28
B7	GND_92	Y12
C10	GND_93	Y14
C13	GND_94	Y16
C19	GND_95	Y19
C22	GND_96	Y21
C25	GND_97	Y23
C28	GND_98	AH11
C7	GND_99	C16
		W32
		GND_OPT
		GND_OPT

GND

+VGA_CORE

UGPU1G

Part 7 of 7

AA12	VDD_0	V17
AA14	VDD_1	V18
AA16	VDD_2	V20
AA19	VDD_3	V22
AA21	VDD_4	W12
AA23	VDD_5	W16
AB13	VDD_6	W19
AB15	VDD_7	W21
AB17	VDD_8	W23
AB18	VDD_9	Y13
AB20	VDD_10	Y15
AB22	VDD_11	Y17
AC12	VDD_12	Y18
AC14	VDD_13	Y20
AC16	VDD_14	Y22
AC19	VDD_15	
AC21	VDD_16	
AC23	VDD_17	U1
M12	VDD_18	U2
M14	VDD_19	U3
M16	VDD_20	U4
M19	VDD_21	U5
M21	VDD_22	U6
M23	VDD_23	U7
N13	VDD_24	U8
N15	VDD_25	
N17	VDD_26	V1
N18	VDD_27	V2
N20	VDD_28	V3
N22	VDD_29	V4
P12	VDD_30	V5
P14	VDD_31	V6
P16	VDD_32	V7
P19	VDD_33	V8
P21	VDD_34	
P23	VDD_35	
R13	VDD_36	W2
R15	VDD_37	W3
R17	VDD_38	W4
R18	VDD_39	W5
R20	VDD_40	W7
R22	VDD_41	W8
T12	VDD_42	
T14	VDD_43	
T16	VDD_44	
T19	VDD_45	Y1
T21	VDD_46	Y2
T23	VDD_47	Y3
U13	VDD_48	Y4
U15	VDD_49	Y5
U17	VDD_50	Y6
U18	VDD_51	Y7
U20	VDD_52	Y8
U22	VDD_53	
V13	VDD_54	
V15	VDD_55	AA1
		AA2
		AA3
		AA4
		AA5
		AA6
		AA7
		AA8

POWER

N14P-GT EDP 45A

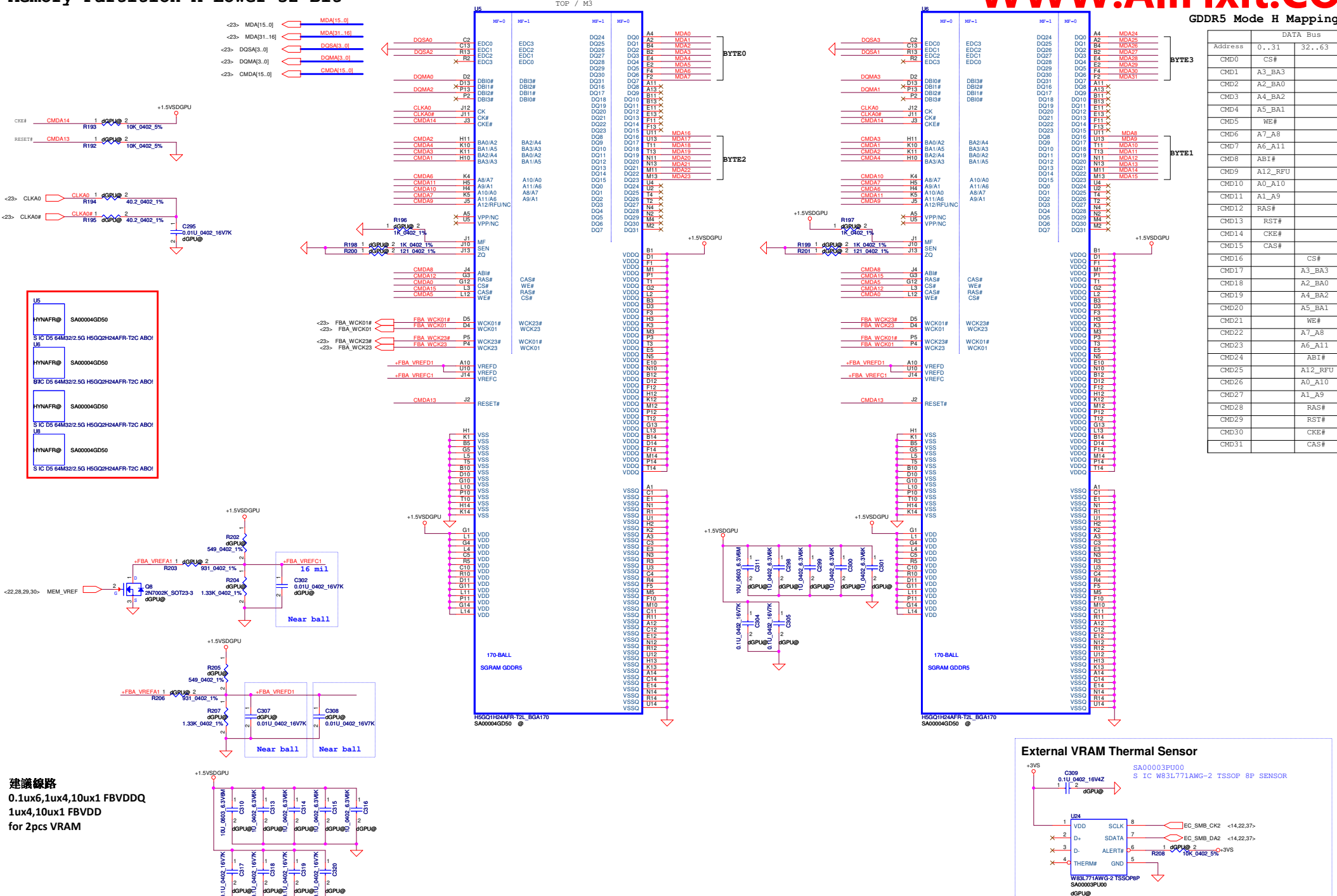
dGPU@ GPU P/N : SA00005W200 S IC N14P-GT-A2 FCBGA 908P GPU
Use N13P symbol.

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				Date: Wednesday, March 13, 2013	Sheet 26 of 64

N14P POWER & GND 5/9

Ezel CX MB LA-A001P

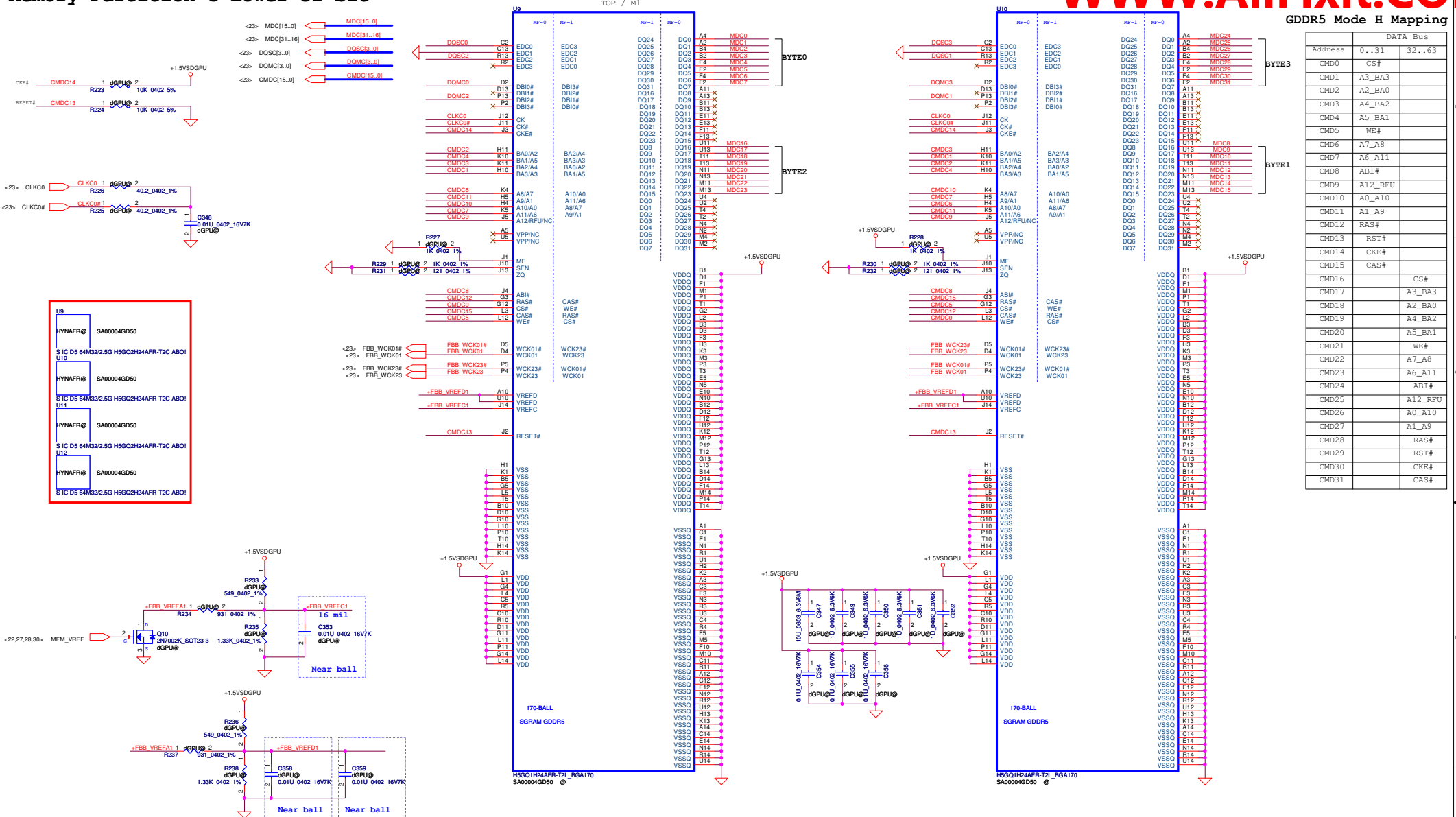
WWW.AliFixit.COM



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Memory Partition C Lower 32 bit



建議線路

0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

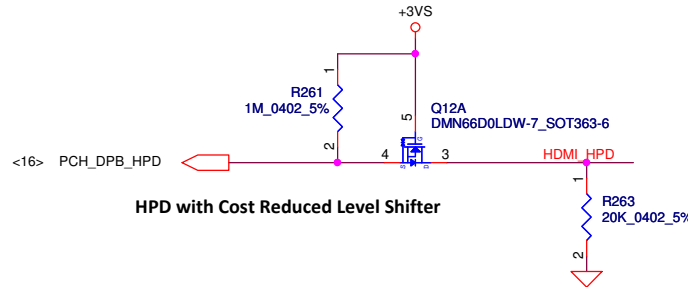
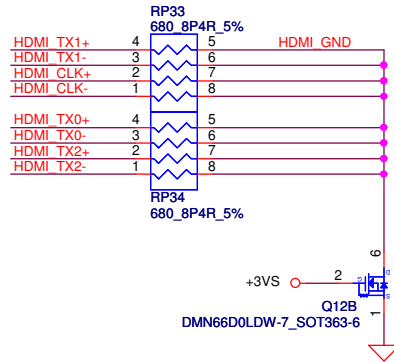


Cost Reduced Level Shifter Topology

<16> PCH_DPB_N0	C397	2	1	0.1U	0402	16V7K	HDMI TX2-
<16> PCH_DPB_P0	C398	2	1	0.1U	0402	16V7K	HDMI TX2+
<16> PCH_DPB_N1	C399	2	1	0.1U	0402	16V7K	HDMI TX1-
<16> PCH_DPB_P1	C400	2	1	0.1U	0402	16V7K	HDMI TX1+
<16> PCH_DPB_N2	C401	2	1	0.1U	0402	16V7K	HDMI TX0-
<16> PCH_DPB_P2	C402	2	1	0.1U	0402	16V7K	HDMI TX0+
<16> PCH_DPB_N3	C403	2	1	0.1U	0402	16V7K	HDMI CLK-
<16> PCH_DPB_P3	C404	2	1	0.1U	0402	16V7K	HDMI CLK+

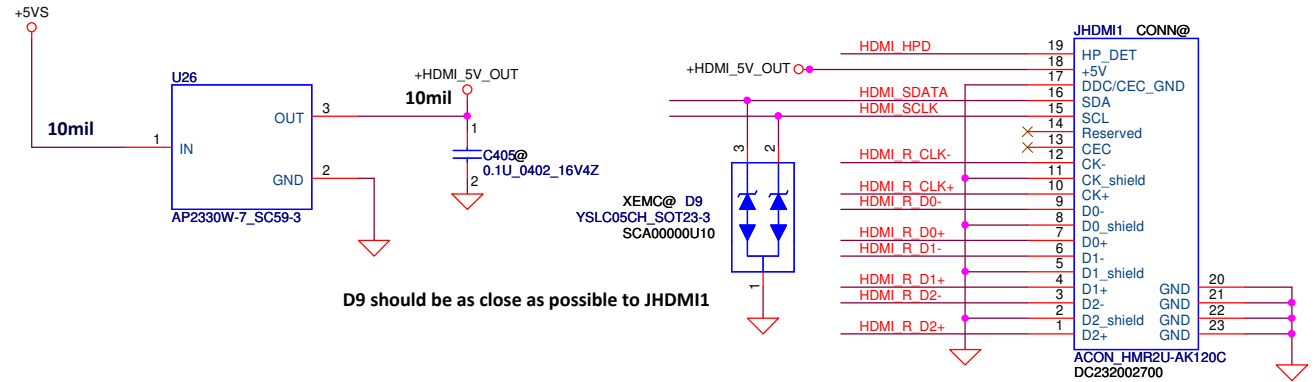
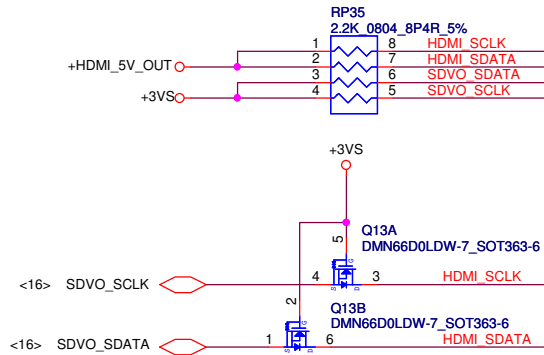
Pin Mapping for HDMI by Port B

PCH Pin Name	HDMI O/P
DDPB_[0]P	TMDSB_DATA2
DDPB_[0]N	TMDSB_DATA2#
DDPB_[1]P	TMDSB_DATA1
DDPB_[1]N	TMDSB_DATA1#
DDPB_[2]P	TMDSB_DATA0
DDPB_[2]N	TMDSB_DATA0#
DDPB_[3]P	TMDSB_CLK
DDPB_[3]N	TMDSB_CLK#
DDPB_AUXP	NA
DDPB_AUXN	NA
DDPB_HPD	HDMIB_HPD
SDVO_CTRLCLK	HDMIB_CTRLCLK
SDVO_CTRLDATA	HDMIB_CTRLDATA



HDMI CLK-	R254	1	2	0	0402	5%	HDMI R CLK-
HDMI CLK+	R255	1	2	0	0402	5%	HDMI R CLK+
HDMI TX0-	R256	1	2	0	0402	5%	HDMI R D0-
HDMI TX0+	R257	1	2	0	0402	5%	HDMI R D0+
HDMI TX1-	R258	1	2	0	0402	5%	HDMI R D1-
HDMI TX1+	R259	1	2	0	0402	5%	HDMI R D1+
HDMI TX2-	R260	1	2	0	0402	5%	HDMI R D2-
HDMI TX2+	R262	1	2	0	0402	5%	HDMI R D2+

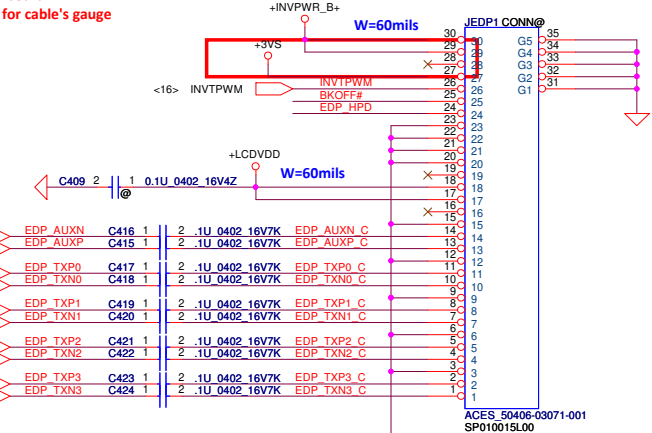
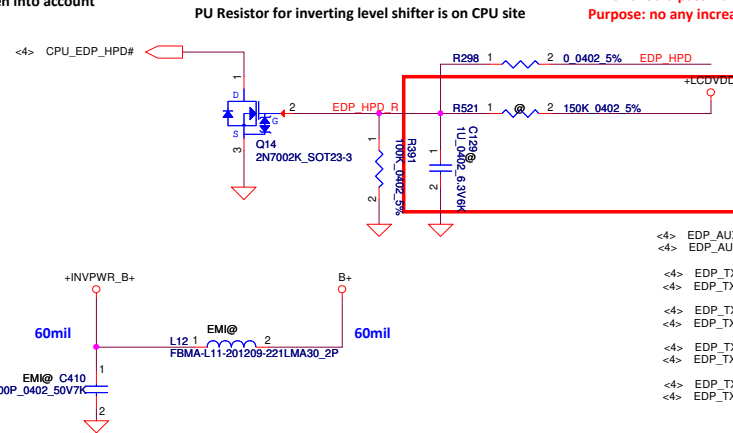
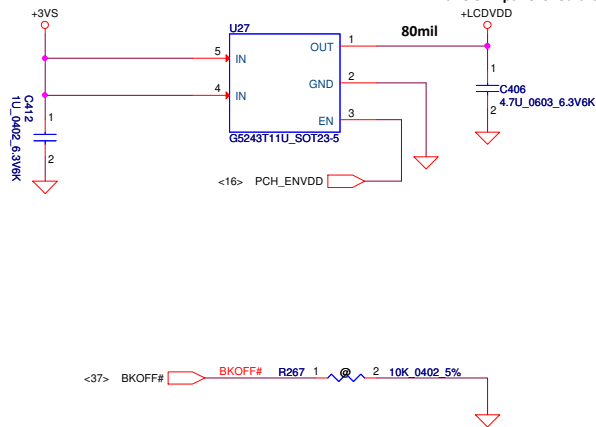
Change to short pad for experiment for the first PCB version , request by EMI



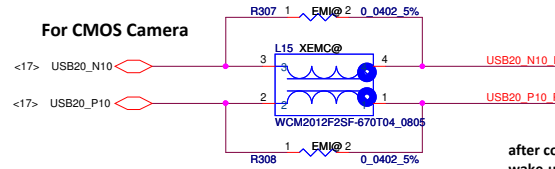
D9 should be as close as possible to JHDMI1

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				Custom		
				Date:	Wednesday, March 13, 2013	Sheet 31 of 64

eDP Panel Power Circuit

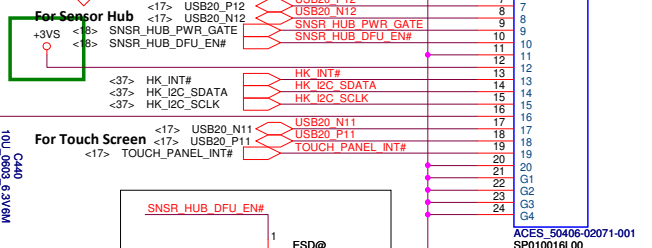


For CMOS Camera

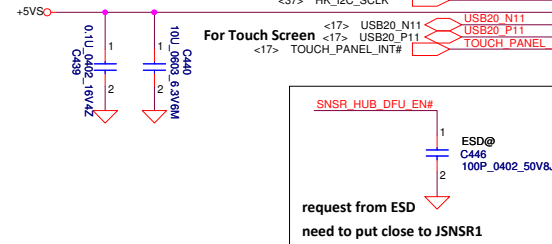


after confirming, home key will not support wake-up function by Ezel_CX

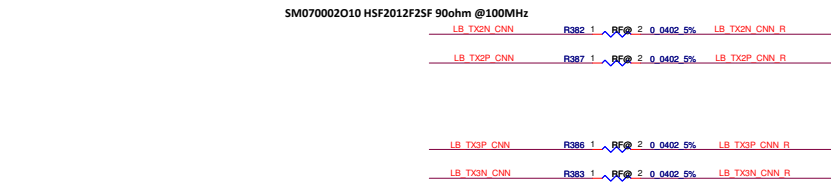
For Sensor Hub



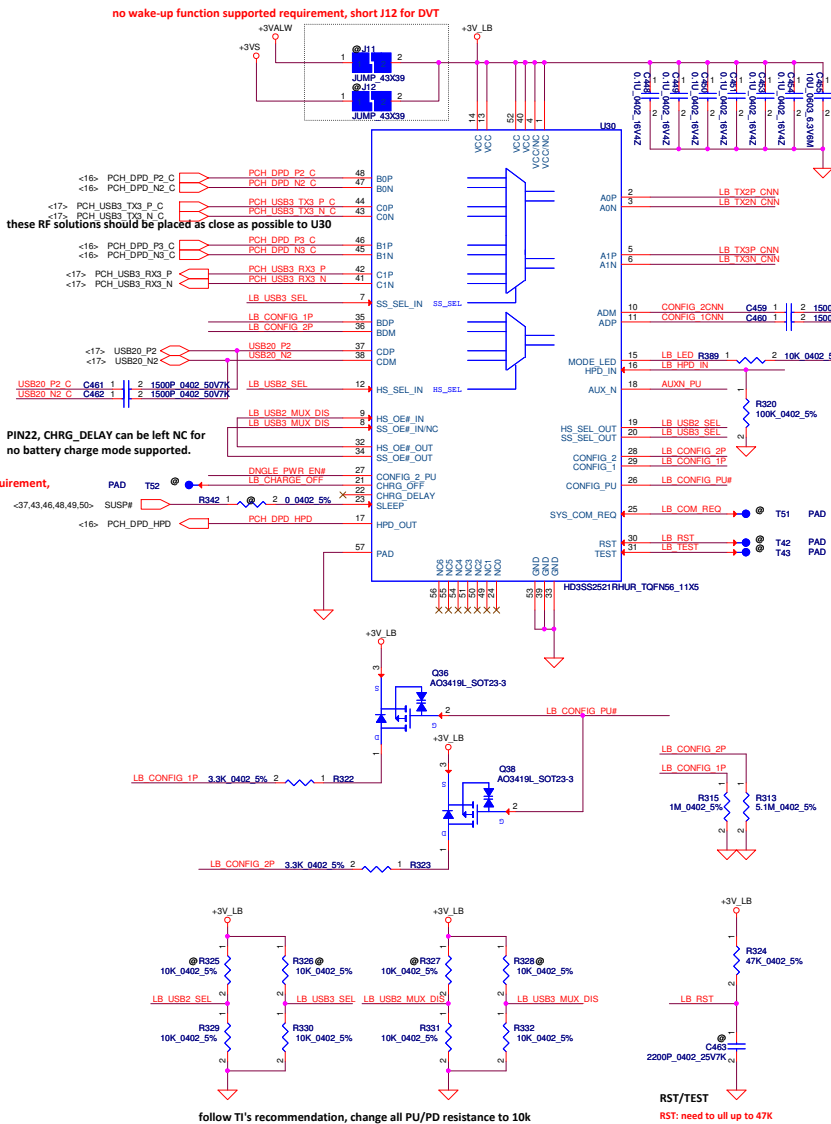
For Touch Screen



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								Custom		Ezel_CX MB_LA-A001P		1.0	
								Date:		Wednesday, March 13, 2013		Sheet 32 of 64	

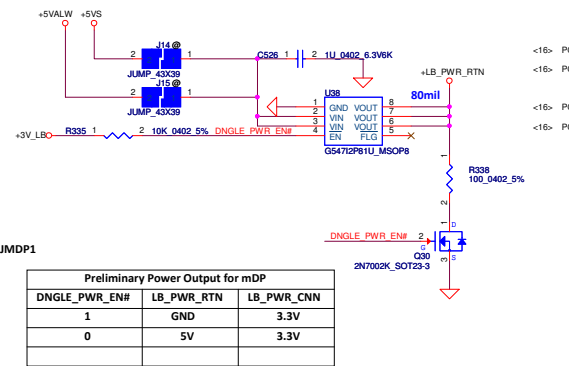


these RF solutions should be placed as close as possible JMDP?



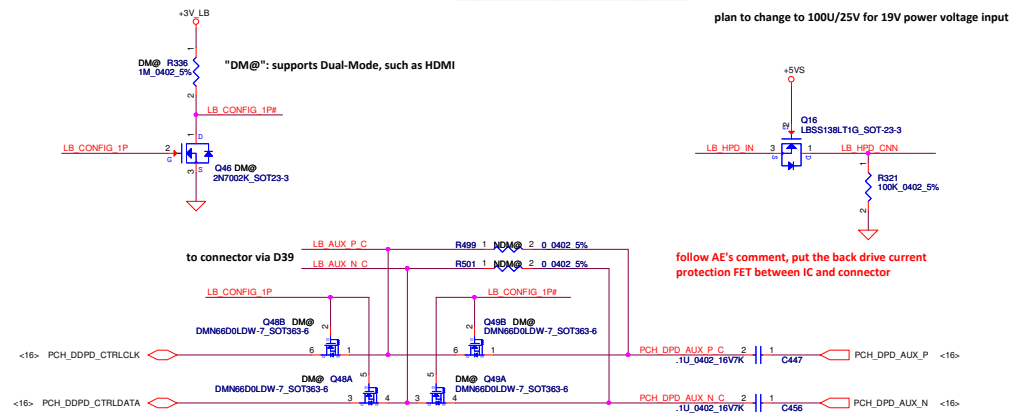
follow TI's recommendation, change all PU/PD resistance to 10k

RST: need to ull up to 47K
TEST: reserve test point for FW update



Preliminary Power Output for mDP		
DNGLE_PWR_EN#	LB_PWR_RTN	LB_PWR_CNN
1	GND	3.3V
0	5V	3.3V

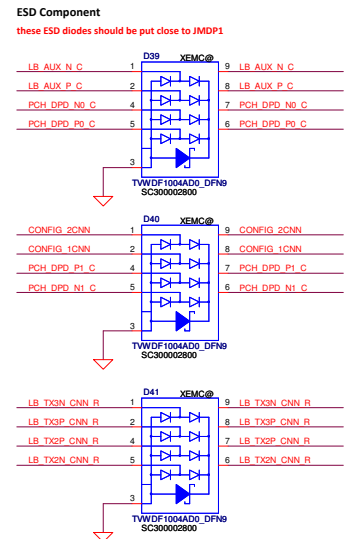
"DM@": supports Dual-Mode, such as HDMI



follow AE's comment, put the back drive current protection FET between IC and connector

Control Signals and Miscellaneous

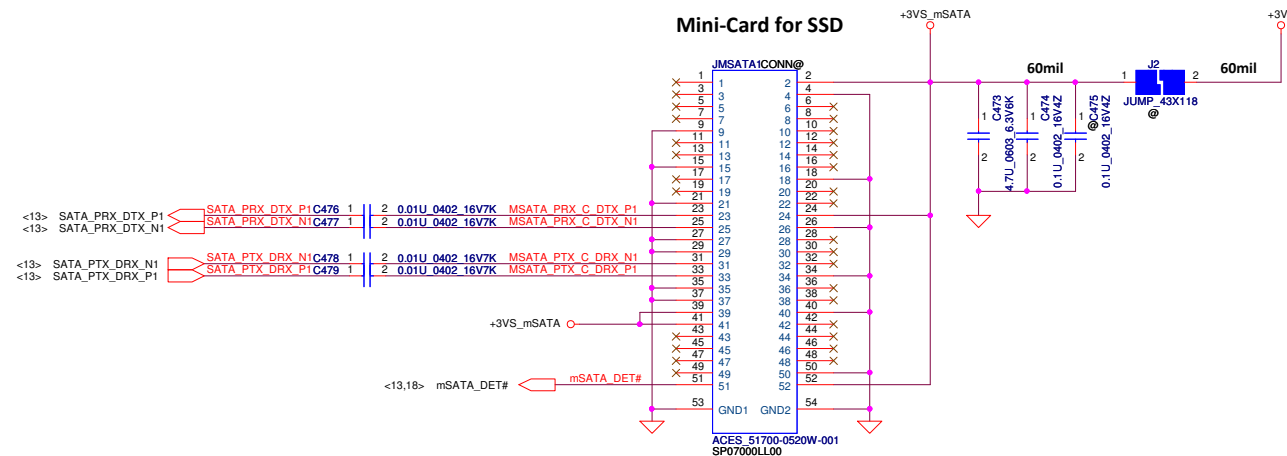
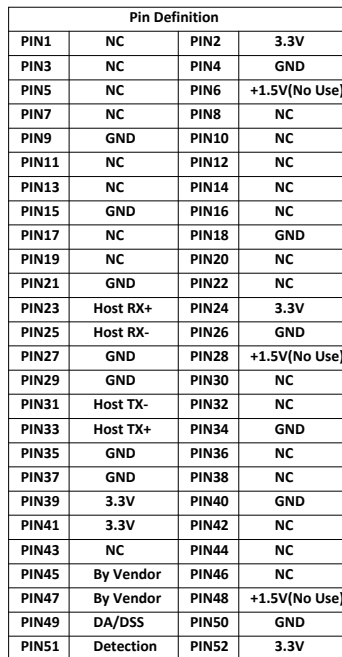
		Docking Port Mode		Acer
Pin Number	DP Mode	USB3.0 (2-Lane Mode)	Full DP Mode (4-Lane Mode)	mDP DNGLE Mode
PIN1	GND	GND	GND	GND
PIN2	HPD	HPD	HPD	HPD
PIN3	DP_ML_0P	DP_ML_0P	DP_ML_0P	DP_ML_0P
PIN4	CONFIG1	<u>USB20_P</u>	CONFIG1	<u>USB20_P</u>
PIN5	DP_ML_0N	DP_ML_0N	DP_ML_0N	DP_ML_0N
PIN6	CONFIG2	<u>USB20_N</u>	CONFIG2	<u>USB20_N</u>
PIN7	GND	GND	GND	GND
PIN8	GND	GND	GND	GND
PIN9	DP_ML_1P	DP_ML_1P	DP_ML_1P	DP_ML_1P
PIN10	DP_ML_3P	<u>USB30_TXP</u>	DP_ML_3P	<u>USB30_TXP</u>
PIN11	DP_ML_1N	DP_ML_1N	DP_ML_1N	DP_ML_1N
PIN12	DP_ML_3N	<u>USB30_TXN</u>	DP_ML_3N	<u>USB30_TXN</u>
PIN13	GND	GND	GND	GND
PIN14	GND	GND	GND	GND
PIN15	DP_ML_2P	<u>USB30_RXP</u>	DP_ML_2P	<u>USB30_RXP</u>
PIN16	AUX_P	AUX_P	AUX_P	AUX_P
PIN17	DP_ML_2N	<u>USB30_RXN</u>	DP_ML_2N	<u>USB30_RXN</u>
PIN18	AUX_N	AUX_N	AUX_N	<u>PWR 5V 1.5A</u>
PIN19	DP_PWR_RTN	DP_PWR_RTN	DP_PWR_RTN	<u>PWR 5V 1.5A</u>
PIN20	<u>PWR 3V 500mA</u>			<u>PWR 3V 500mA</u>



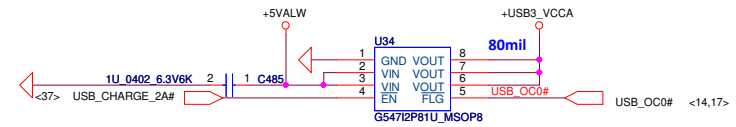
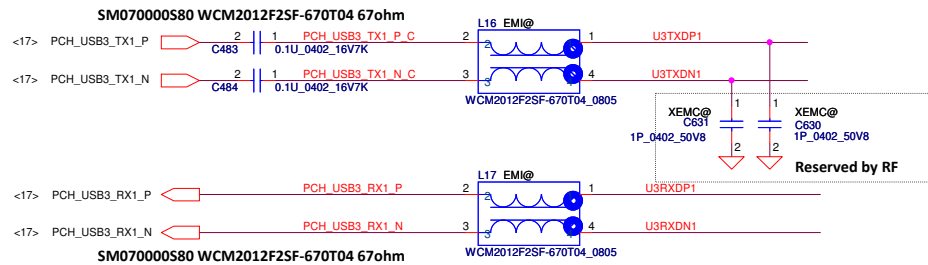
ESD Component

these ESD diodes should be put close to JMDP1

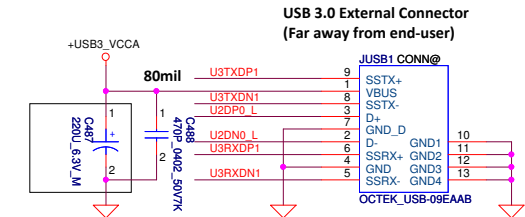
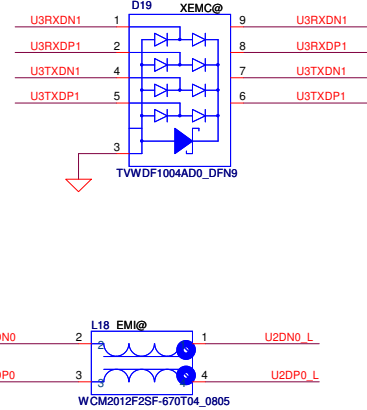
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					Ezel CX MB LA-A00P			1.0	
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D19 should be put as close as possible to JUSB1



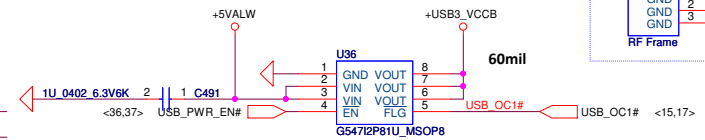
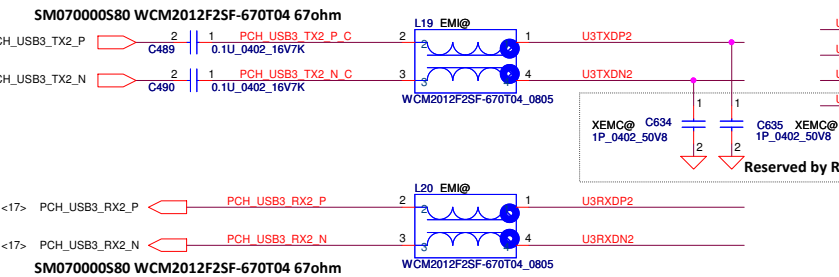
Part Number	Description	ESR
SF000002Y00	S_A-P_CAP 220U 6.3V M 6.3X4.2 R17M VLPs	17mΩ

Truth Table for Inserted Device

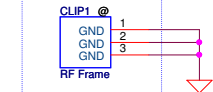
CB	SELCDP	
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only, to distinguish if Fast Charging should be supported or not

Exteranal USB-IF Device Type	
DCP	Dedicated Charging Port
SDP	Standard Downstream Port
CDP	Charging Downstream Port

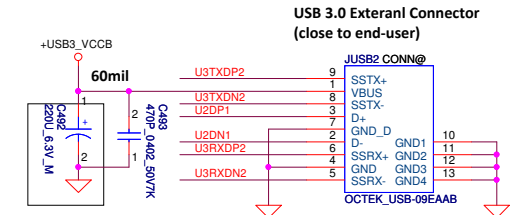
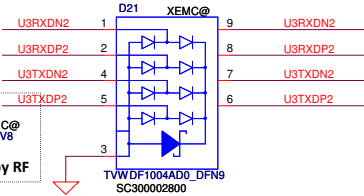
SM070000S80 WCM2012F2SF-670T04 67ohm



add Frame for RF

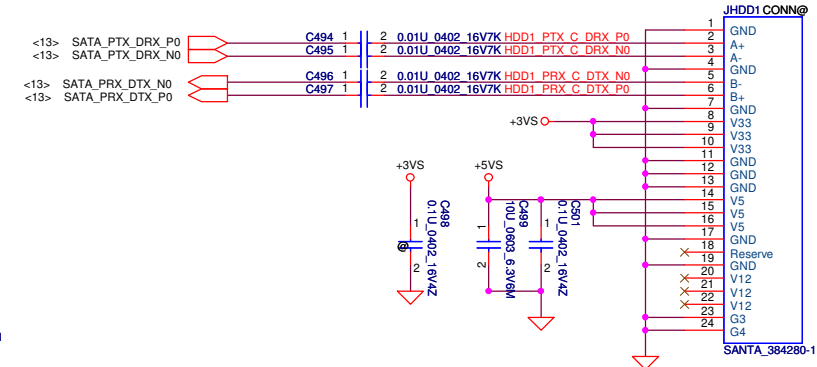
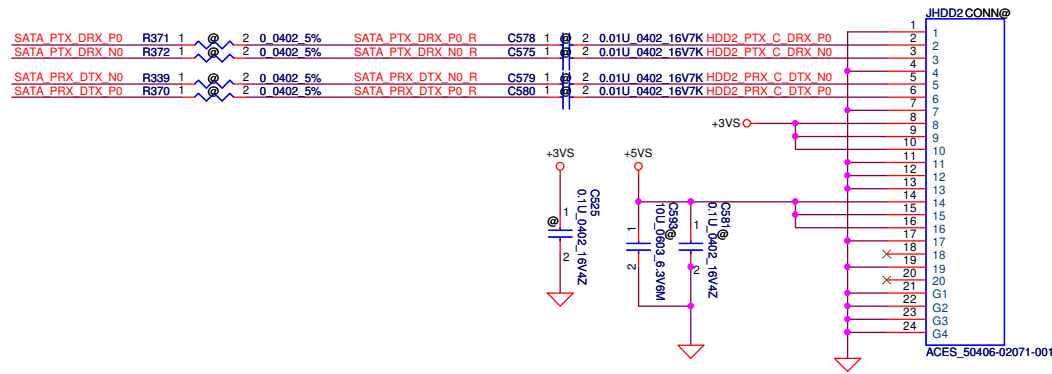


D21 should be put as close as possible to JUSB1



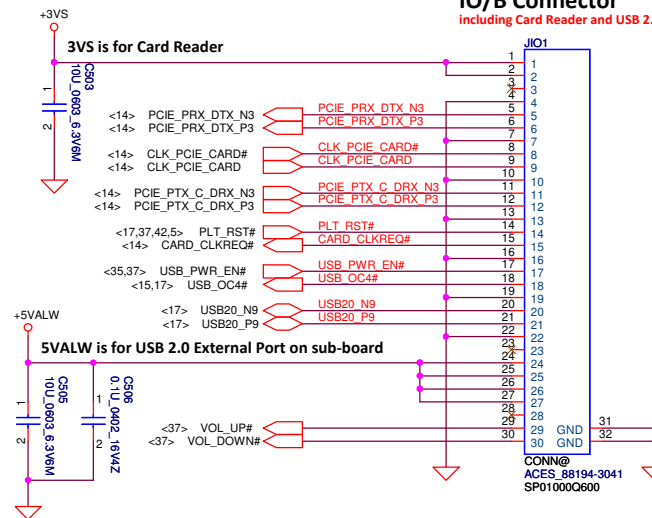
Part Number	Description	ESR
SF000002Y00	S_A-P_CAP 220U 6.3V M 6.3X4.2 R17M VLPs	17mΩ

SATA HDD Connector(DIP Type)



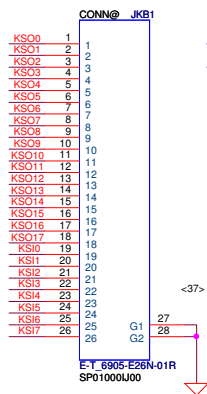
IO/B Connector

including Card Reader and USB 2.0 external port



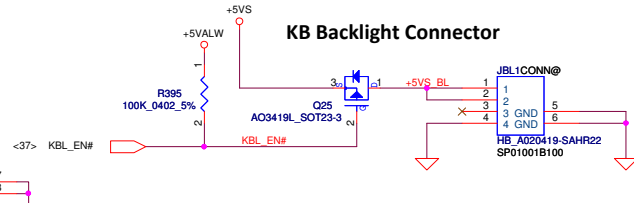
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KB Connector

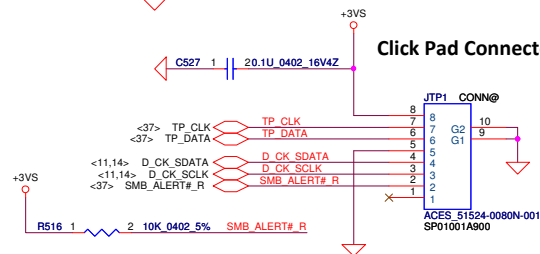


KSII[0..7] <37>
KSOI[0..17] <37>

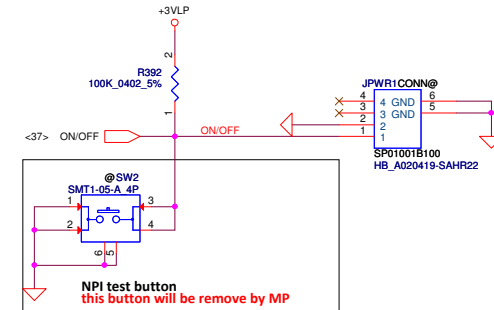
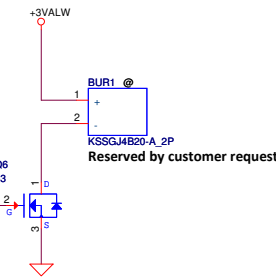
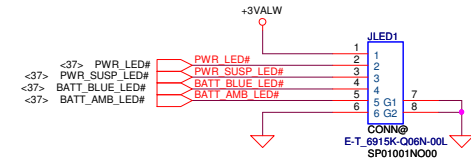
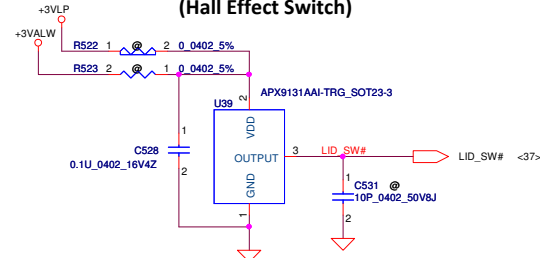
KB Backlight Connector



Click Pad Connector

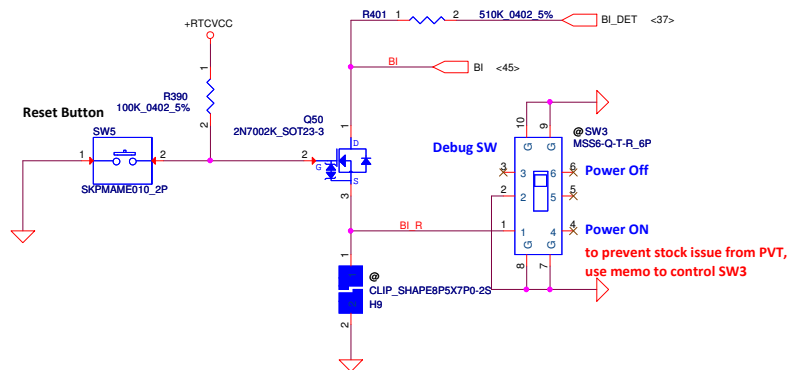


Lid Switch (Hall Effect Switch)



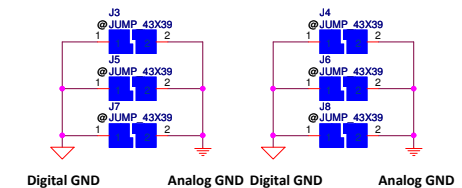
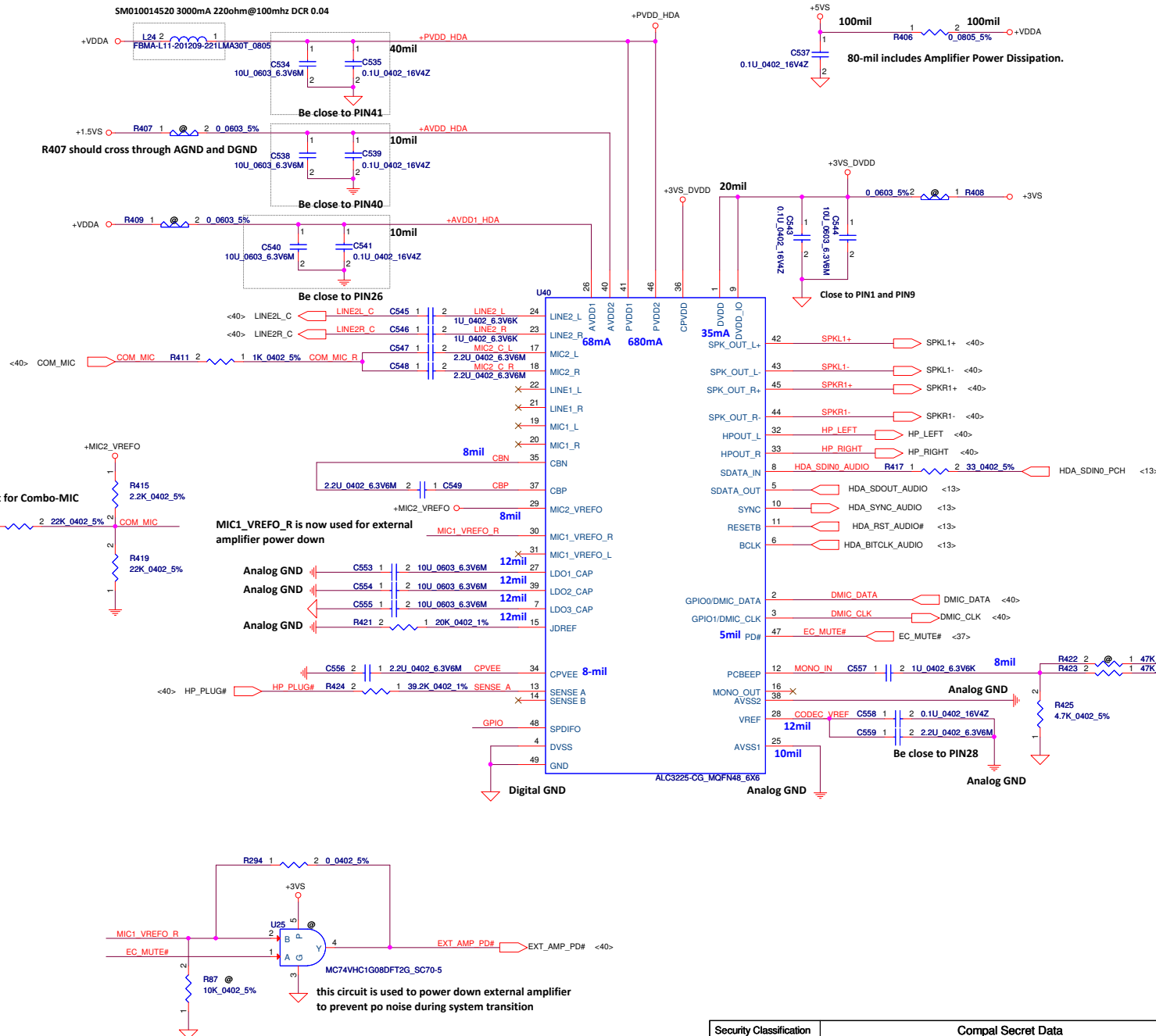
Embedded Battery Reset Button

Debug switch will be removed after MP.

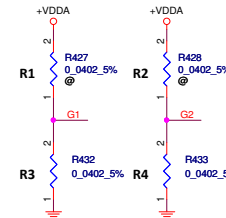
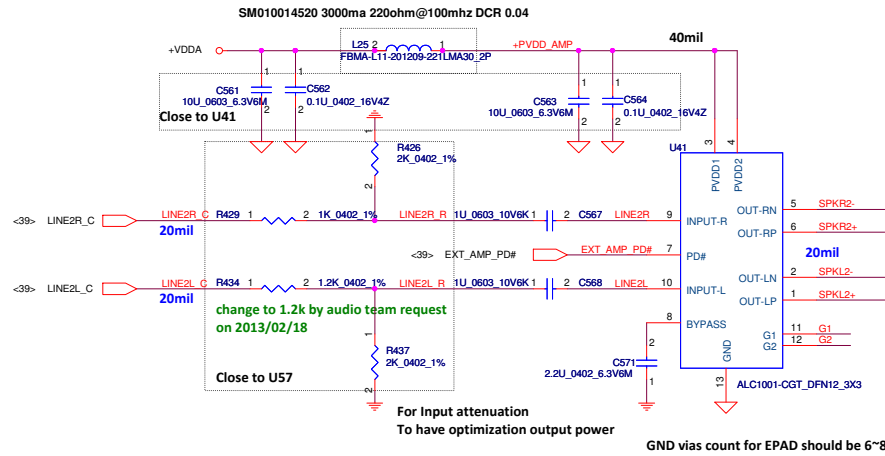


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HD Audio Codec- ALC3225 with Embedded Speaker Amplifier



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								HD Audio Codec ALC3225X + ALC1001							
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								Customer		Ezel CX MB LA-A001P				1.0	
								Date:		Wednesday, March 13, 2013				Sheet 39 of 64	

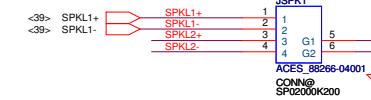


R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

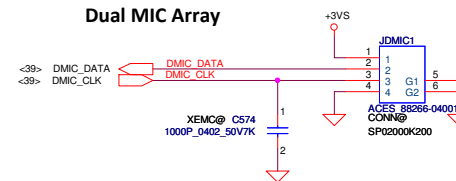
Speaker Connector (Right)



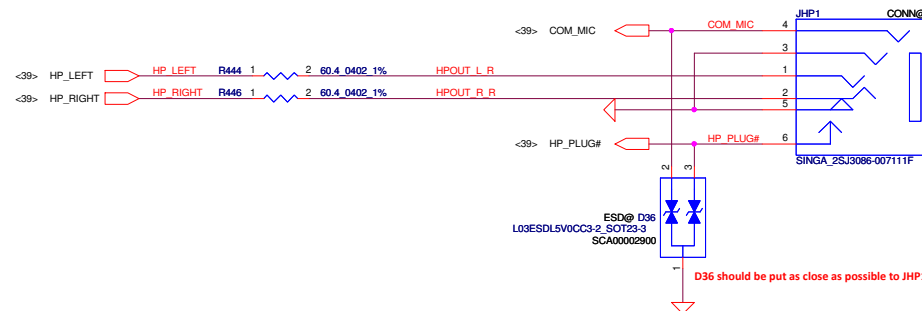
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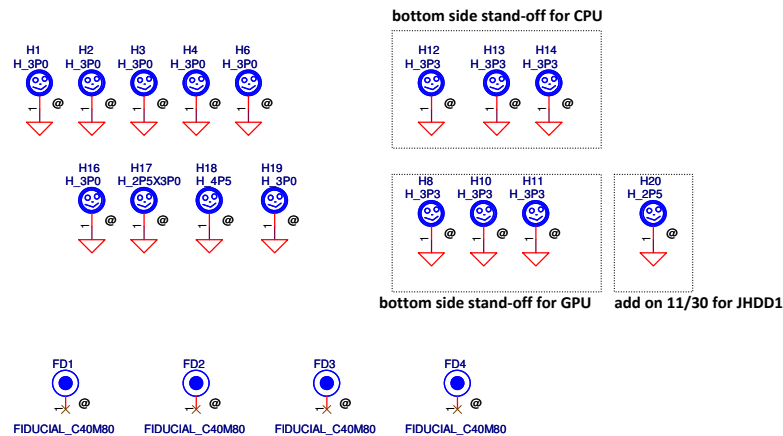
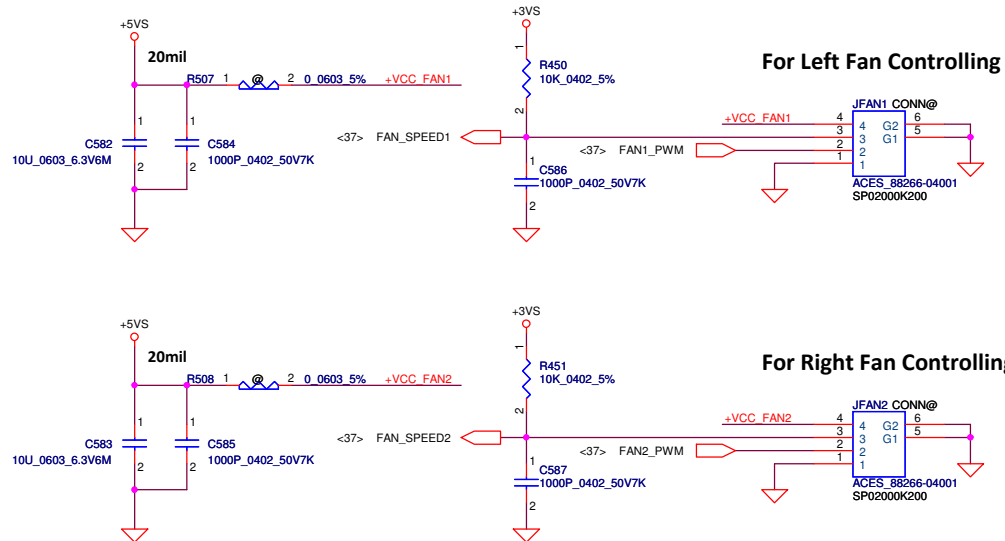


Dual MIC Array



Headphone Out/Mic Combo (Noraml-Open Type)

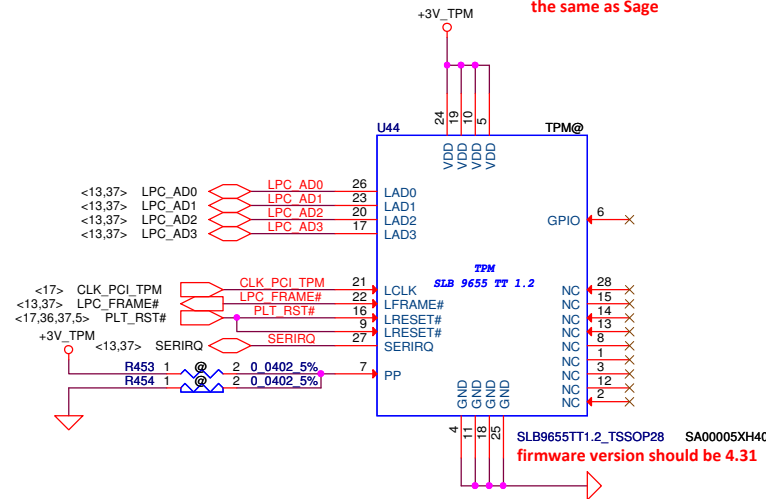
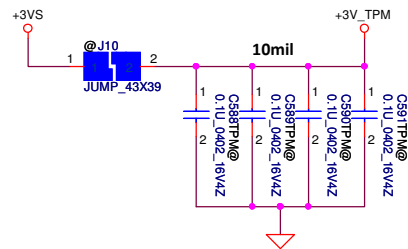




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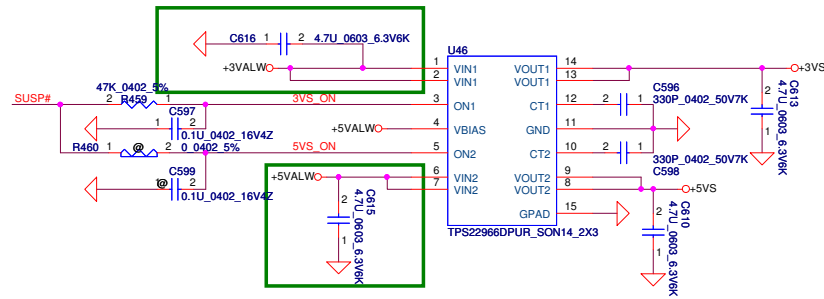
TPM on board solution (INFINEON)

the same as Sage



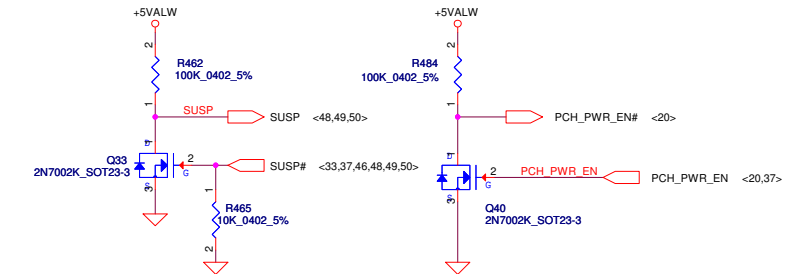
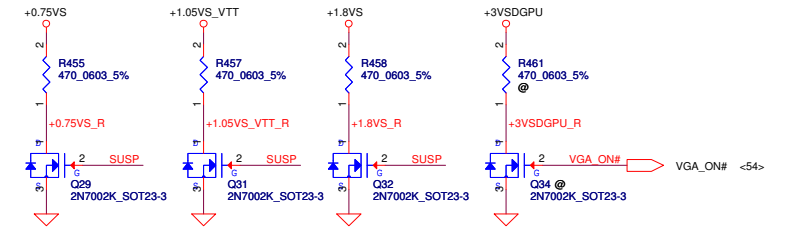
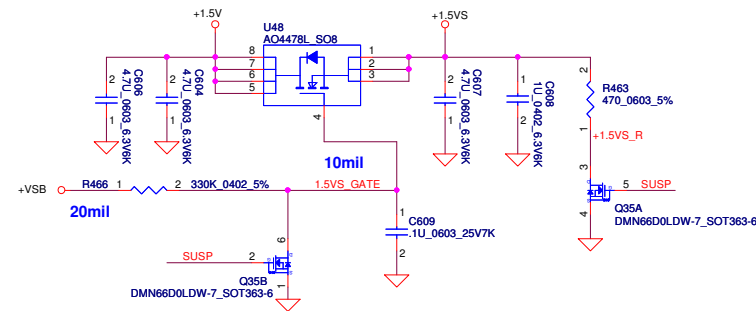
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				Custom	1.0
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Use Dual Load Switch for 3VS/5VS Power Supply

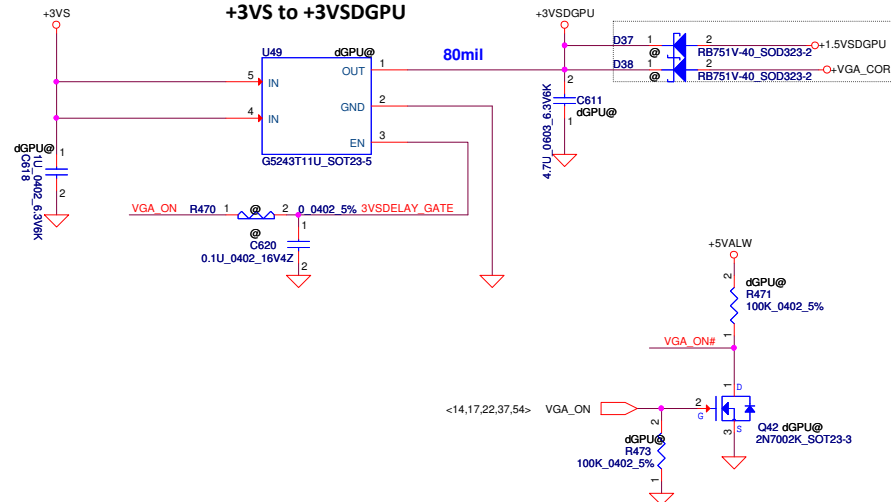


C615 and C616 are $\leq 4.7\mu\text{F}$ hence it is okay for APE8990GN3B

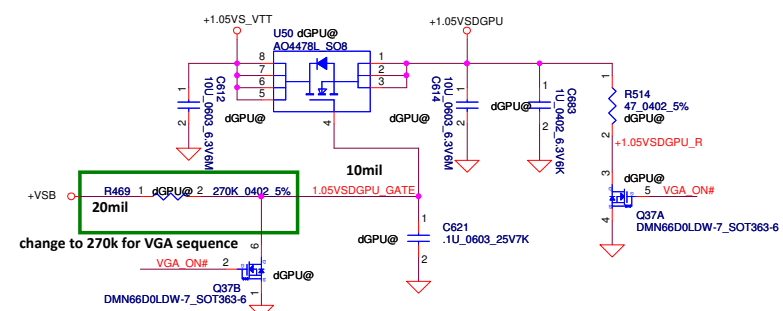
+1.5V to +1.5VS



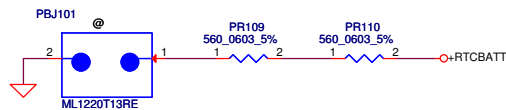
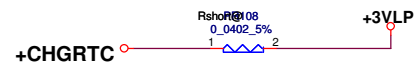
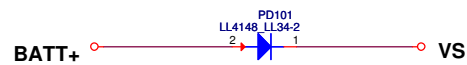
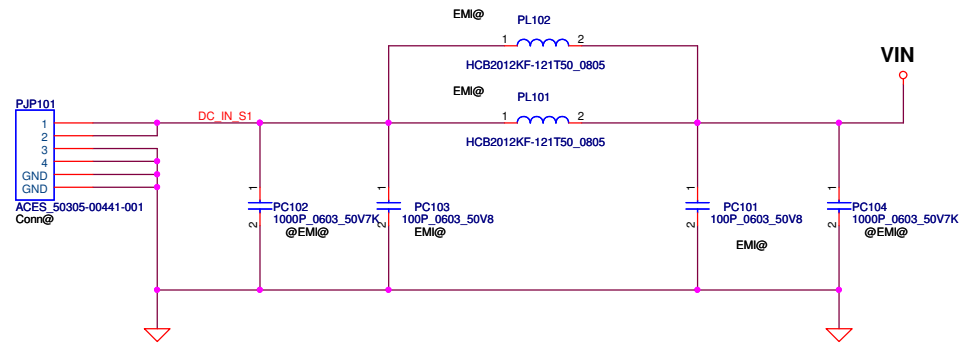
+3VS to +3VSDGPU



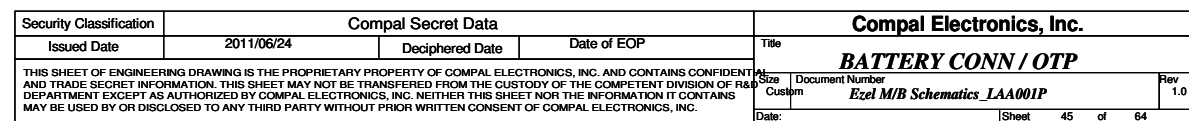
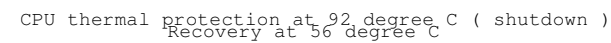
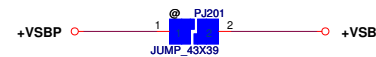
+1.05VS_VTT TO +1.05VSDGPU

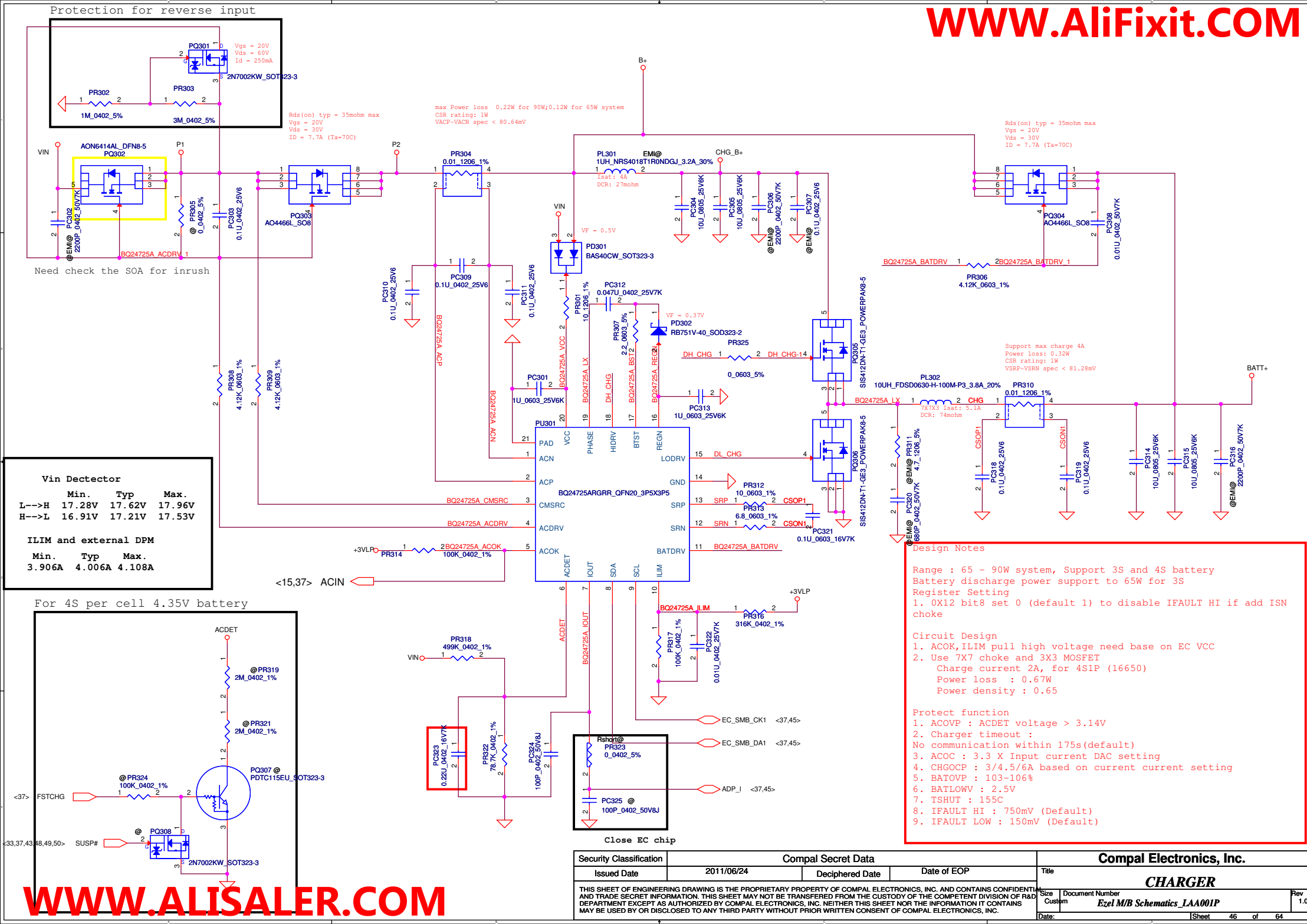


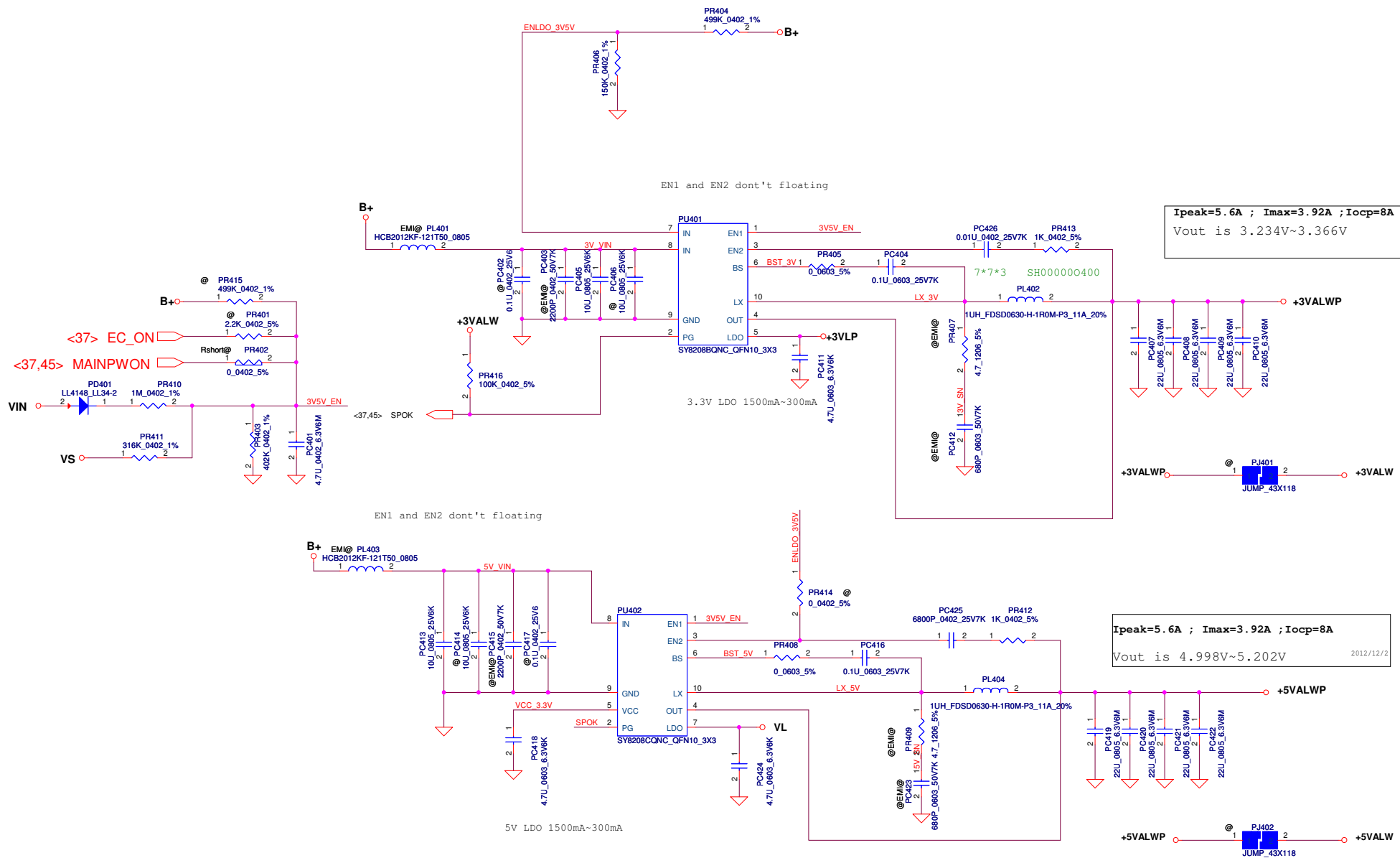
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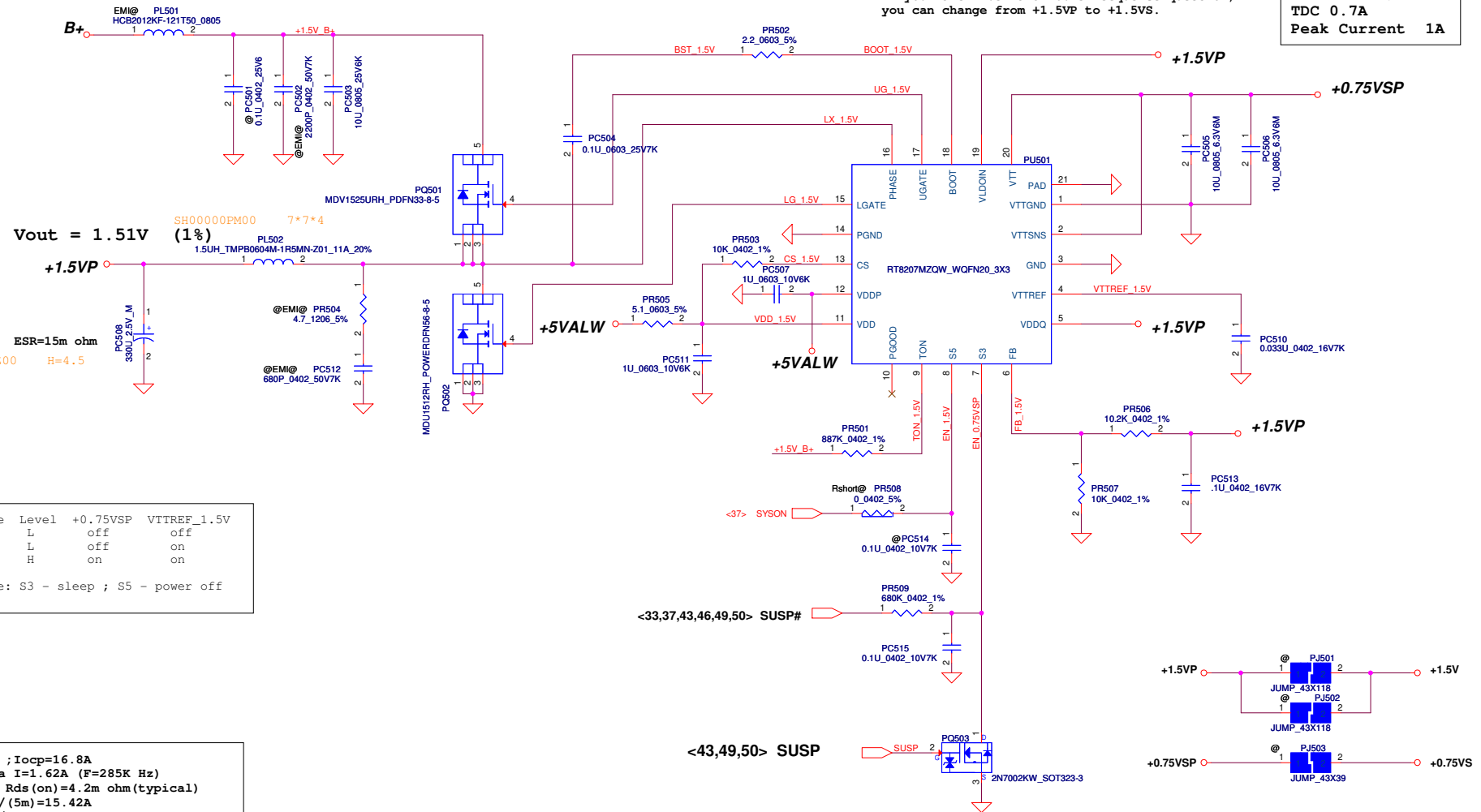


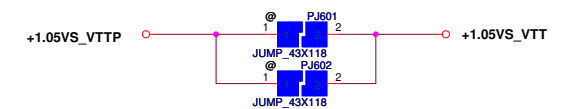
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				Date:	Sheet	44 of 64





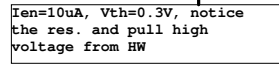
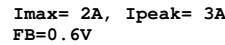






```
+1.05VS
Ipeak=15.37A ;Iocp=18.44A ;Imax=10.76A
1/2Delta I=1.71A (F=290K Hz)
choose PR603=75Kohm
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Iocp=Ilimit+1/2Delta I=18.88~26.4A
```

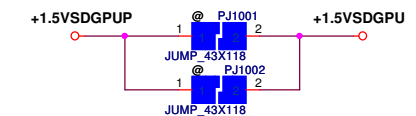
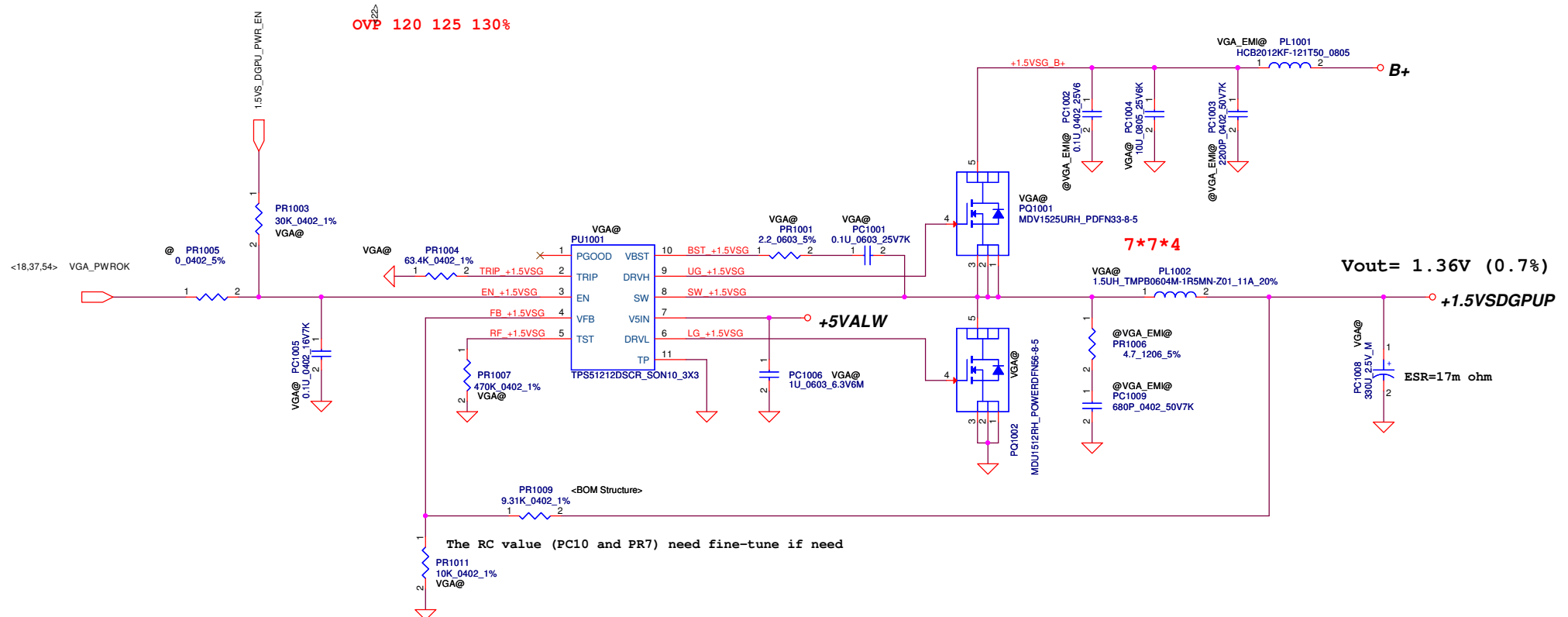
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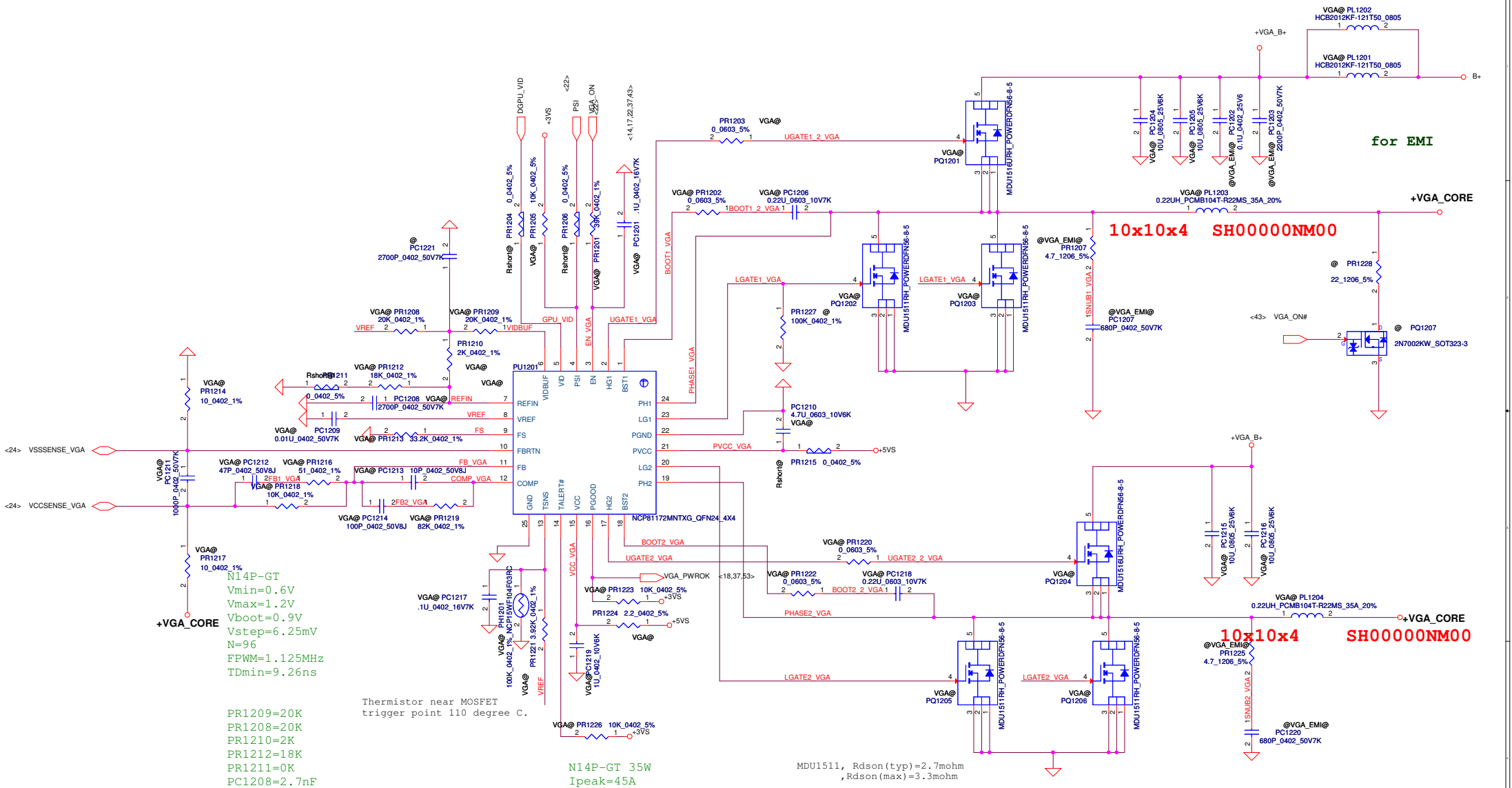
WWW.ALISALER.COM


```
+1.5VSDGPU
Ipeak=12.5A ; 1.2Ipeak=15A ; Imax=8.75A
1/2Delta I=1.08A (F=290K Hz)
FR1004=63.4Kohm
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Iocp=Ilimit+1/2Delta I=15.16~21.5A
Iocp(min)>1.2Ipeak
```

2013/03/13

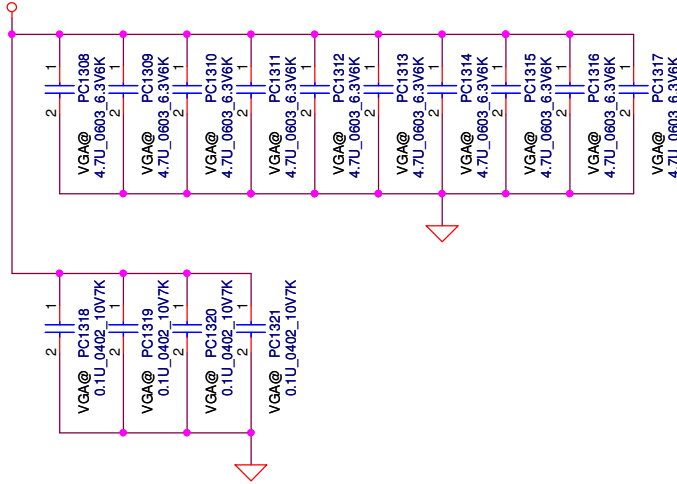


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				+1.5VSDGPUP		
				Size	Document Number	Rev
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+VGA_CORE Under VGA Core



GB4-128

Under

4.7uF_0603_10pcs

0.1uF_0402_4pcs

Near

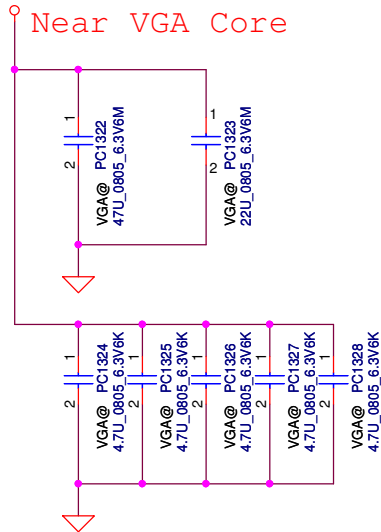
47uF_0805_1pcs

22uF_0805_1pcs

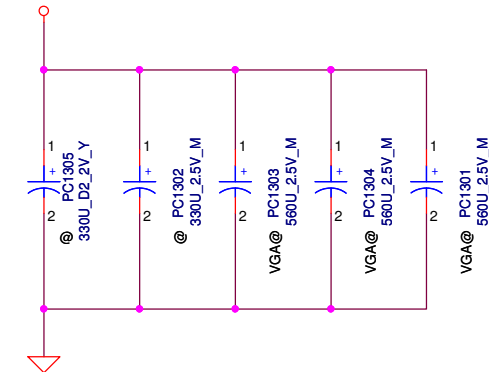
4.7uF_0805_5pcs

+VGA_CORE

Near VGA Core



+VGA_CORE



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Acoustic noise	3V 5V light load efficiency improvement		3V/5V	1.Add 2pcs 1K_0402_5% (PR412 PR413) 1pcs 4700P_0402_25V7K (PC425) 1pcs 0.047U_0402_25V7K (PC426) 2.Add 4.7u_0402_6.3V6M (PC401)	01/03	EVT
2	Silergy update revision	3V 5V enable control for Rev0.7. But un-pop.		3V/5V	Add un-pop 2pcs 0402 resistors (PR415 PR414)	01/03	EVT
3		UMA SKU VGA_CORE IC un-pop		VGA	PU1201 change to VGA@	01/03	EVT
4		Reduce part count		VGA	Change to R-short (PR1211 PR1204 PR1206 PR1215)	01/03	EVT
5		DFB: PC1305 PC1304 PC1303 PC1301 too close.		VGA	330U_2.5V_M_SF000002Z00 change to 330U_D2_2V_Y_SGA20331E10 (PC1305)	01/03	EVT
6		EMI risk fot CPU/GFX H-Side		CPU	Change 2pcs 0_0603_5% (PR809 PR827)	01/03	EVT
7		The modify values for CPU transition test		CPU	1. 422_0402_1% change to 604_0402_1% (PR807) 2. 0.22uH_SH000000200 change to 0.36uH_SH000000J00 (PL803)	01/03	EVT
8		modify charger current to meet battery charge time.		Charger	0.02_1206_1%_SD00000S110 charger to 0.01_1206_1%_SD00000K820	01/10	EVT
9		AC Mode no rest function		3V/5V	Del PQ401 2N7002KW_SOT323-3	02/18	DVT
10		VRAM efficiency improvement		1.5VDGPU	1.PQ1002 AON7702A_SB00000T600 change to MDU1512RH_POWERDFN56-8-5_SB00000SY00 2.PQ1001 AON7408L 1N DFN_SB00000H800 change to MDV1525URH 1N PDFN33-8_SB00000S600	02/18	DVT
11		When pwm IC shutdown on S0, EC could detect SLP_S5#, but cannot detect PCH was no power.		3V/5V	PR416 add 100K_0402_5%_SD028100380	02/18	DVT
12		The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail.		VGA	PR1228 add un-pop 22_1206_5%_SD001220A80 PQ1207 add un-pop 2N7002KW_SOT323-3_SB000009Q80	02/18	DVT
13		The 5VALW will fast than 3VALW and the rising time will under 2mS.		3V/5V	PC426 4700P_0402_25V7K_SE075472K80 change to 0.01U_0402_25V7K_SE075103K80 PC425 0.047U_0402_25V7K_SE00000MJ00 change to 6800P_0402_25V7K_SE075682K80	02/18	DVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
14		VCIN1_function		OTP	1.90W@ PR225 3.3K_0402_1%_SD00000GW80 change to 6.19K_0402_1%_SD034619180 2.65W@ PR225 1.02K_0402_1%_SD034102180 change to 1.91K_0402_1%_SD000009080 3.PR207 10K_0402_1%_SD034100280 change to 60.4K_0402_1%_SD034604280	02/18	DVT
15		VGA enable sequence for NV suggest.		VGA	PR1003 22K_0402_1%_SD034220280 change to 30K_0402_1%_SD034300280 PR1201 22K_0402_1%_SD034220280 change to 39K_0402_1%_SD034390280	02/18	DVT
16		VRAM voltage change to 1.35V.		1.5VDGPU	PR100911.5K_0402_1%_SD034115280 change to 9.31K_0402_1%_SD034931180 PR1004 137K_0402_1%_SD034137380 change to 63.4K_0402_1%_SD03463K280 PR318 499K_0402_0.1%_SD00000U380 change to 499K_0402_1%_SD034499380	03/13	PVT

Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
1	33	HW	12/27/2012	Customer	To reserve DP++ circuitry to support dual-mode	reserve placeholder of Q46, Q48, Q49, R499, R501	Rev02
2	33	HW	12/27/2012	Compal	output from mDP connector cannot be normally transition	change R389 from 100k to 10k	Rev02
3	33	HW	12/27/2012	Compal	for safety concern	a. change U29 from AP2330W-7 to RB491D-YS b. also reserve one jump, J11, then track DVT result	Rev02
4	39	HW	12/27/2012	Compal	change PU domain for LID_SW#	change PU domain of R361 from +3VALW to +3VALW_EC	Rev02
5	39	HW	12/27/2012	Customer	remove LAN board	remove JLAN1, add JPWR1 (A020419-SAHR22, the same as JBL1)	Rev02
6	39	HW	12/27/2012	Compal	add NPI test on/off button on M/B	add SW6	Rev02
7	39	HW	12/27/2012	Compal	update driving circuit for buzzer	add R519 and Q6	Rev02
8	33	HW	12/28/2012	Compal	recommandation from vendor	follow AE's comment, put the back drive current protection FET, Q16, between IC and connector	Rev02
9	34	HW	12/28/2012	Compal	recommandation from vendor	follow AE's comment, change R338 from 100k to 0ohm, and base on DVT's test result to see if okay to remove it or not	Rev02
10	9	HW	12/28/2012	Compal	ME height limit, caused by click-pad structure	remove C82, then reserve placeholder for C689 and C690	Rev02
11	38	HW	12/28/2012	Compal	to prevent back drive from WLAN module, change the PU power domain from 3VALW to 3V_WLAN	connect 3V_WLAN to R379 then move this component to the page related WLAN	Rev02
12	38	HW	12/28/2012	Compal	to avoid 0.02V leakage voltage on 3VS	change the connection direction of Q24A	Rev02
13	38	HW	12/28/2012	Compal	update board ID for DVT build	stuff R384(100k) and change R388 to 8.2k	Rev02
14	14, 38	HW	12/28/2012	Customer	LAN/B request had been cancelled by customer	1. delete the connection of LAN_PWR_EN and EC_PME# 2. remove C628, C530, C682, C629 and JLAN1 3. remove C173 and C174	Rev02
15	38	HW	12/28/2012	Compal	no PU for Home-Key related signals	add RP45 for I2C and INT# signals to PU to 3VALW_EC	Rev02
16	38	HW	12/28/2012	Compal	wrong control signal for buzzer	swap pin connection for BT_ON# and BUZZ#	Rev02

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Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
17	38	HW	12/28/2012	Compal	no PU for volume tuning button	PU VOL_UP# and VOL_DOWN# to 3VS by RP45 and RP44 respectively	Rev02
18	32	HW	12/28/2012	Compal	1. abnormal display via redriver board 2. to solve the probelm without any gauge increased	add R521 and C129, then connects PIN27 fo JEDP1 to 3VS, this solution is only for cable which need to pass via re-drvier board	Rev02
19	38	HW	12/28/2012	Compal	for keyboard back light auto-negotiation	swap the pin connected for EC_SPOK and KB_BKL	Rev02
20	17	HW	12/28/2012	Compal	to reduce 0-ohm usage	1. remove R488 and R485 becuase GC6 is ready 2. remove R489 and R490 because GC6 is ready	Rev02
21	13	HW	12/30/2012	Compal	for long-term solution, use 64Mb to replace 32Mb+16Mb	change U18 as 8MB ROM part, and only reserve placeholder for U19	Rev02
22	14	HW	12/30/2012	Compal	to pervent potential back drive from PCH	correct PU domain for OC6# from 3VS to 3VALW_PCH	Rev02
23	20	HW	12/30/2012	Compal	to reduce 0-ohm usage	change R480 to J16 and change R78 to J17	Rev02
24	39	HW	12/30/2012	Compal	to reserve power source from 3VLP for LID	add R522 and R523	Rev02
25	39	HW	12/30/2012	Compal	short-term solution for battery no output with PMOS	add R376 and R299	Rev02
26	13	HW	01/03/2013	Compal	to trial-run single 8MB SPI ROM	add R300, R301, R302 and R303 and only stuff R302 and R303	Rev02
27	35	HW	01/03/2013	Compal	add PU resistor for A4 EC's GPIO5B's pin type	Add R393 as PU resistor, PU to 3VS_WLAN	Rev02
28	42	HW	01/03/2013	Compal	hole with diameter 6mm do not need screw hole footprint	remove H5	Rev02
29	33	HW	01/07/2013	Compal	change the CFG pin of Lightning-Bolt from 2 PMOS to 1 2 in 1 NMOS and one single channel NMOS	delete Q17 and Q18, then add Q50 and Q47	Rev02

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30	33	HW	01/07/2013	Compal	to reduce the usage of 0-ohm	replace R309 and R310 by jumps (J11 and J12)	Rev02
31	38	HW	01/07/2013	Compal	change the power domain of EC	connects EC power from +3VALW to +3VLP, stuff R513 and also change the power domain of lid switch as EC--> stuff R522	Rev02
32	6	HW	01/07/2013	Compal	for known issue from DM meeting about RST_GATE#	change R520 from 0-ohm to 100k	Rev02
33	32	HW	01/07/2013	Compal	to reduce EDP cable's gauge	add R521 and C129 to replace HPD signal by +LCDVDD, but still reserve R298 and R391 as back-up	Rev02
34	20	HW	01/07/2013	Compal	default as no Erp Lot 6 concern for PCH power	remove R479	Rev02
35	13	HW	01/07/2013	Compal	SPI uses single device topology	remove R67 and RP12	Rev02
36	39	HW	01/07/2013	Compal	no need to PU twice for LID_SW#	remove R400	Rev02
37	33	HW	01/07/2013	Compal	PU LB_RST when not in debug mode	add R324 with 47k	Rev02
38	18	HW	01/15/2013	Compal	to identify SKUs have TPM solution or not	after aligning with SW team, add R116 and R118 for DVT	Rev02
39	39	HW	01/15/2013	Compal	let lid swich has the same power domain as EC	stuff R522, and de-pop R523	Rev02
40	33	HW	01/17/2013	Compal	update the config1 and config2 control circuit	remove Q50, Q47 and R390 and replaced by Q36 and Q38	Rev03
41	33	HW	01/29/2013	Compal	to reduce 0-ohm usage	remove R316 and R317	Rev03
42	33	HW	01/29/2013	Compal	to remove placeholder for depop. components	remove SW1	Rev03
42	33	HW	01/29/2013	Compal	to remove placeholder for depop. components	remove LED3 and R318	Rev03

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43	33	HW	01/29/2013	Compal	to remove placeholder for depop. components	remove R375--> back-dirve just depends on the configuration of external device. for this unexpected situation, we need to keep protect FET present	Rev03
44	33	HW	01/29/2013	Compal	to reduce components which might interfered by RF frame	remove R400, R517 and change R522 and R523 to 0402 size	Rev03
45	32	HW	01/30/2013	Compal	ESD test fail	add C446 (22p capacitor) close to sensor connector for ESD	Rev03
46	13	HW	01/30/2013	Compal	8MB SPI ROM ready	change BOM structure of R75 and R76 to "@"	Rev03
47	38	HW	01/30/2013	Compal	normally update board ID for PVT PCB	change R338 from 8.2k to 18k	Rev03
48	40	HW	01/31/2013	Compal	no need to connect BEEP# from EC	depop R422 first then track PVT result	Rev03
49	41	HW	02/01/2013	Compal	no too many problems from EC, change EC power domain to +3VLP	change R513 to short pad	Rev03
50	44	HW	02/03/2013	Compal	for VGA sequence	R469 change from 47k to 270k	Rev03
51	18	HW	02/03/2013	Compal	ESD test fail	add C472, 0.1uF, on mSATA_DET# and close to PCH	Rev03
52	33.34	HW	02/05/2013	Compal	for cost saving and USB safety concern	add U38 (USB power switch) and C526 change R338 from 0-ohm to 100-ohm for discharge circuit replace C457 by C691 and C692 then stuff one of them remove Q19, Q20, R333, R447, Q45, U31, R337, R334, R476 change connection of LB_CHARGE_OFF to test point only	Rev03
53	42	HW	02/05/2013	Compal	request from ME	change H18 from 3P0 to 4P5	Rev03
54	32, 38	HW	02/05/2013	Compal	no need to support wake-up function by home-key	change power to home key from +3VALW to +3VS, change PU domain for home key related signals to +3VS	Rev03
55	39	HW	02/05/2013	Compal	to prevent worse contact for safety screw hole	change H9 footprint to CLIP_SHAPE8P5X7P0-S	Rev03

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56	9	HW	02/05/2013	Compal	to reduce depop. components	remove C93, C689, C128, C109, C110, C123, C125, C407, C467, C470, C471, R92, C502, C500, R365, C524, C536, C592, C542, C560, C658, C659, C660, C661, C664, R70, R71, R111, R117 change to stuff C111, C112, C126	Rev03
57	34	HW	02/05/2013	Compal	for part count reduction, idea from EC	depop R393, R344 and Q23 first then track PVT result	Rev03
58	36	HW	02/06/2013	Compal	to avoid assembly interfere	remove C504	Rev03
59	36	HW	02/06/2013	Compal	to reduce 0-ohm usage	change R407, R408 and R409 from 0-ohm to R-Shotr	Rev03
60	35	HW	02/06/2013	Compal	add Frame for RF, for USB 3.0 signal noise	add CLIP1	Rev03
61	20	HW	02/18/2013	Compal	to reduce system power under S4/S5	stuff Q39 and U28 for 3V/5V PCH power	Rev03
62	38	HW	02/18/2013	Compal	reset battery is defined and toggled only by battery only & and change the design circuit to prevent battery no output caused by PMOS	del Q28, R403 and D29 add R390, 100k and PU to +RTCVCC remove C533	Rev03
63	43	HW	02/18/2013	Compal	after checking VGA sequence, discharge circuit is not needed for 3VSDGPU	no stuff R461 and Q34	Rev03
64	14	HW	02/18/2013	Compal	for part count reduction	remove R515 and let SMB_ALERT# connect to RP16	Rev03
65	36	HW	02/18/2013	Compal	to avoid components' interfere	no stuff C593, C581, C575, C578, C579, C580	Rev03
66	38	HW	02/18/2013	Compal	to correct switch button type	remove SW6	Rev03
67	40	HW	02/18/2013	Compal	to solve the not balance volume output from R/L speaker	change R434 from 1k to 1.2k	Rev03

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68	38	HW	02/18/2013	Compal	not request from EMC and no reason to keep	no stuff C531	Rev03
69	32	HW	02/18/2013	Compal	to avoid unstable configuration for HPD cause anything wrong	stuff R298 and R391, then depop. R521 and C129	Rev03
70	40	HW	02/23/2013	Customer	to avoid too large deviation cause problems for speaker volume	keep resistance of R434,R437,R426,R429 as before but change the tolerance from 5% to 1%	Rev03
71	4, 6	HW	03/10/2013	Customer	to improve thermal problem and base upon request from our end-customer, change PEG CFG to 8X	depop C1,C2,C3,C4,C5,C6,C7,C8,C17,C18,C19,C20,C21,C22,C23,C24,C33,C34,C35,C36,C37,C38,C39,C40,C49,C50,C51,C52,C53,C54,C55,C56 add R27 and R28 for PEG CFG to strap to 8-Lane	Rev10
72	34	HW	03/10/2013	Customer	cancel the request to for IOAC supported	add J18 then depop. C468 and U33	Rev10
73	33	HW	03/10/2013	Comapl	to prevent HD3SS2521 only works on DP mode after system cold-boot	swap pin-3 and pin-4 of Q48A	Rev10
74	39	HW	03/11/2013	Comapl	to prevent pop noise	add U25, R294 and R87	Rev10
75	33	HW	03/12/2013	Comapl	follow TI AE's recommendation	chagne R320 to 100k and remove R319 then connected the signal directly	Rev10
75	32	EMI	03/12/2013	Comapl	to fix EMI solution and remove unnecessary items	del R293, R297 and L13 then pass the signal directly del R304, R305 and L14 then pass the signal directly del R410, R412, R413, R414 then pass the signals directly del R430, R431, R435, R436 then pass the signals directly del R440, R445, R447 then pass the signals directly	Rev10
76	32	ESD	03/12/2013	Comapl	request from ESD	change R446 from 22p to 100p	Rev10
77	32	ESD	03/12/2013	Comapl	to fix ESD solution and remove unnecessary items	remove D30, D31, D32, D33	Rev10

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