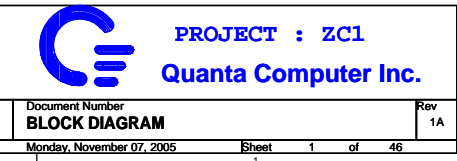
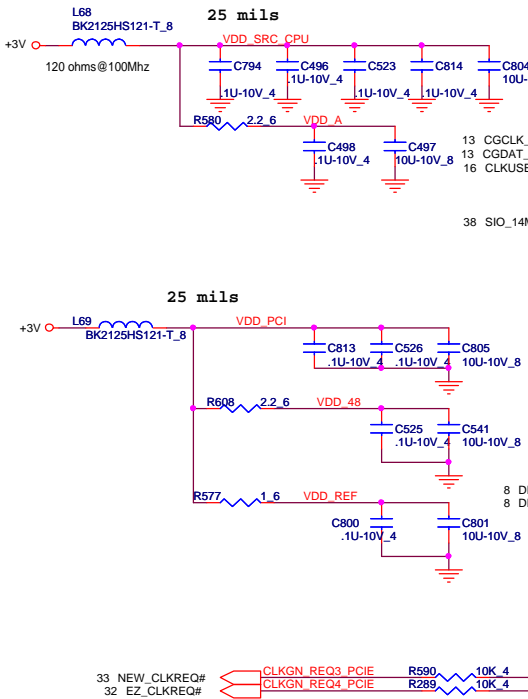


```
EV@: Stuff when external VGA used
SH@: Stuff when SATA HDD used
PH@: Stuff when PATA HDD used
```



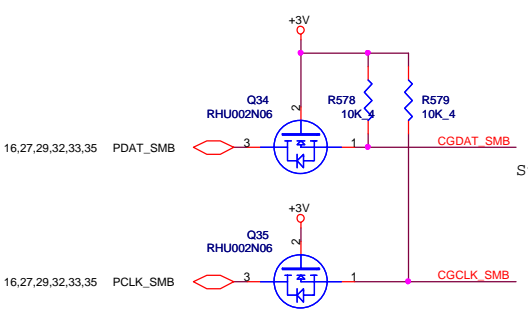
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

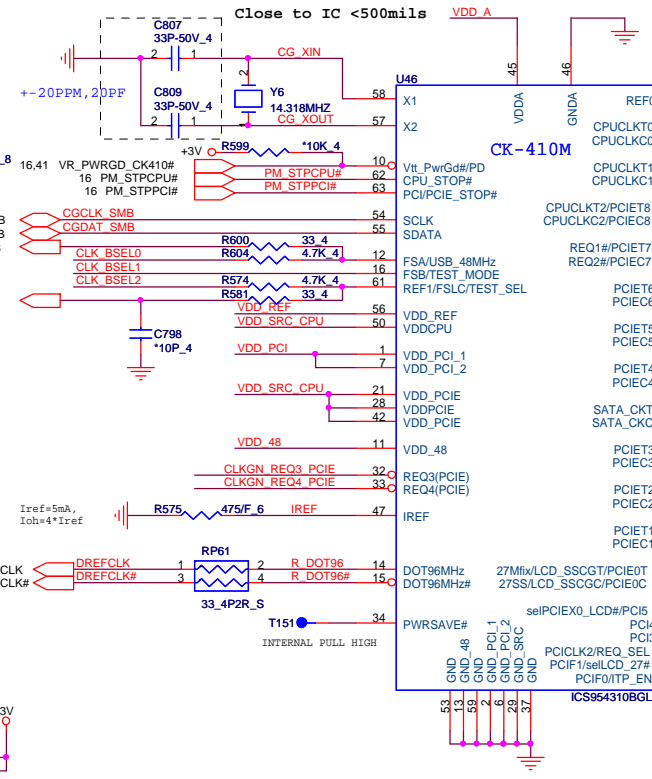


PREQ3(PCIE) Latched Select
"0" : CLK Enable
"1" : CLK Disable Control : PCIE 2,4,6,8

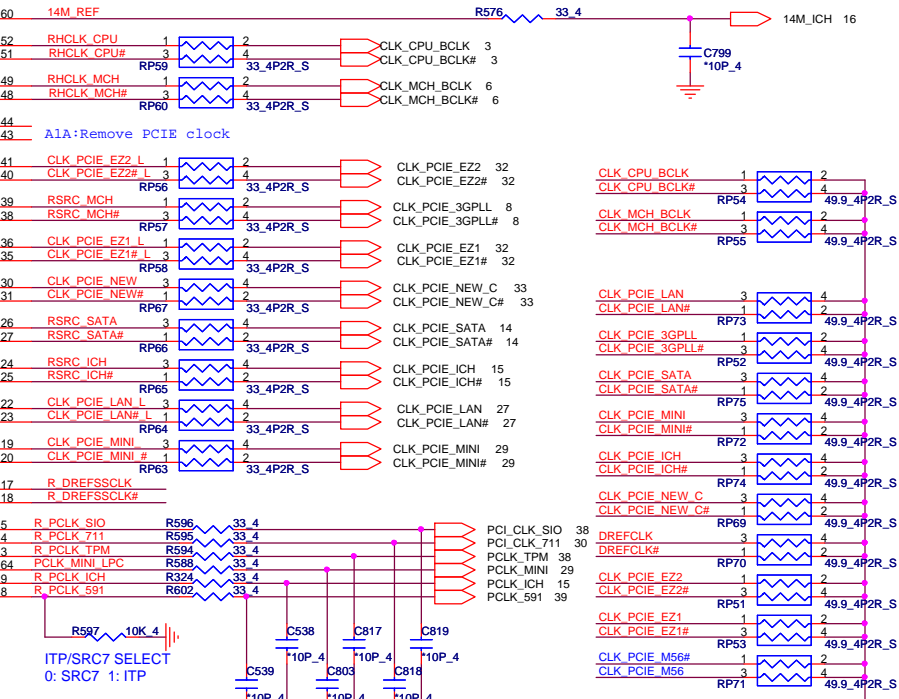
PREQ4(PCIE) Latched Select
"0" : CLK Enable
"1" : CLK Disable Control : PCIE 1,3,5,7



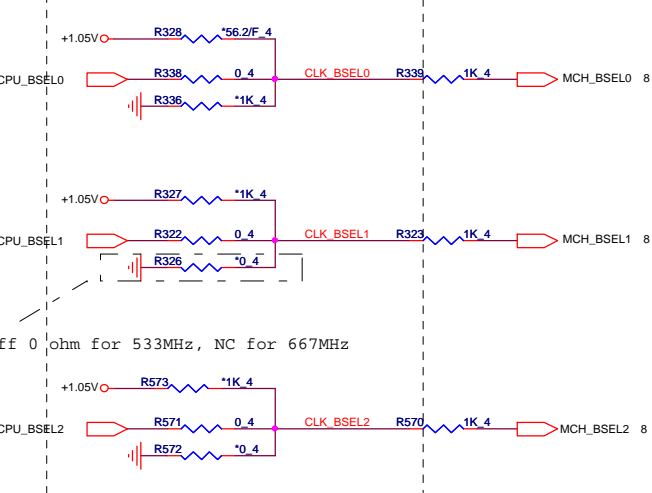
AlA-change X1,X2 capacitor from 27pf to 33pf(CL=20pf)



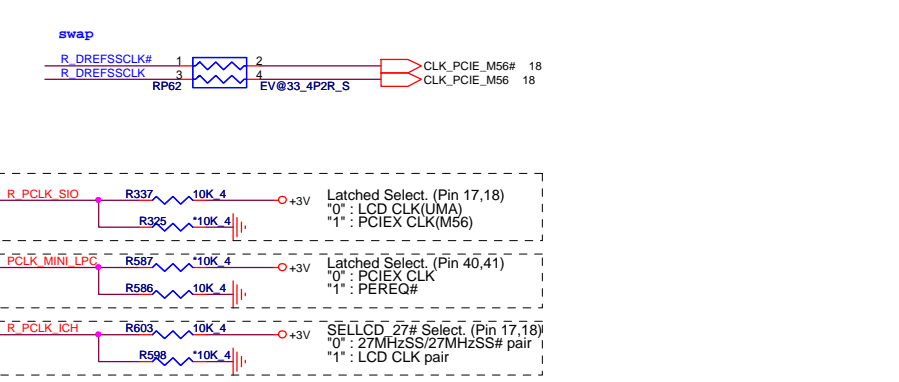
Place these termination to close CK410M.




AlA-FSB Frequency Select:by CPU driven



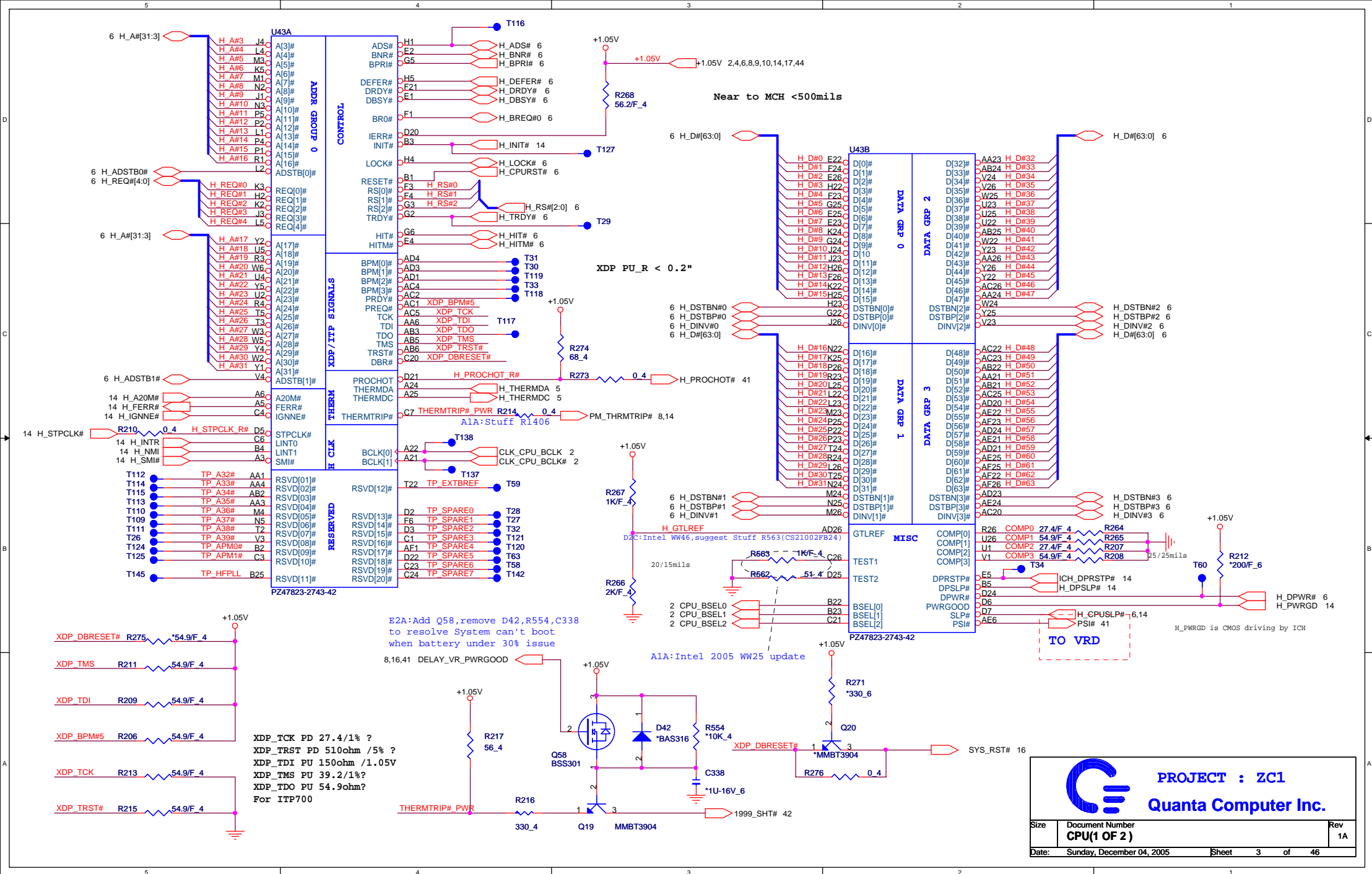
AlA:Change pin 3 PCLK_LAN to PCLK_TPM





PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date:	Friday, December 09, 2005	Sheet 2 of 46

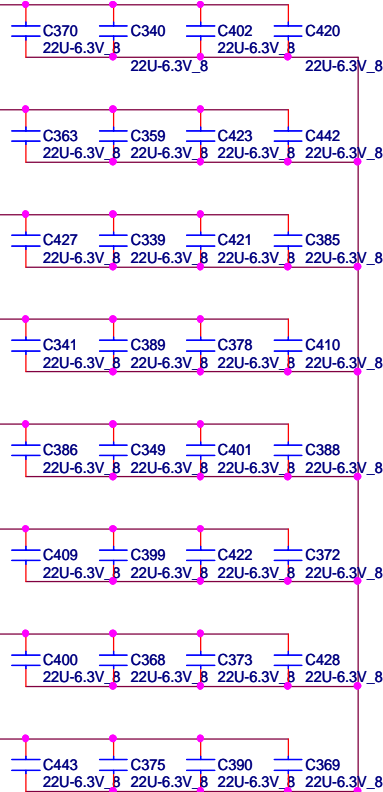


U43D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
A26	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]

PZ47823-2743-42

P6		
P21		
P24		
R2		
R5		
R22		
R25		
T1		
T4		
T23		
T26		
U3		
U6		
U21		
U24		
V2		
V5		
V22		
V25		
W1		
W4		
W23		
W26		
Y3		
Y6		
Y21		
Y24		
AA2		
AA5		
AA8		
AA11		
AA14		
AA16		
AA19		
AA22		
AA25		
AB1		
AB4		
AB8		
AB11		
AB13		
AB16		
AB19		
AB23		
AB26		
AC3		
AC6		
AC8		
AC11		
AC14		
AC16		
AC19		
AC21		
AC24		
AD2		
AD5		
AD8		
AD11		
AD13		
AD16		
AD19		
AD22		
AD25		
AE1		
AE4		
AE8		
AE11		
AE14		
AE16		
AE19		
AE23		
AE26		
AF3		
AF6		
AF8		
AF11		
AF13		
AF16		
AF19		
AF21		
AF24		

VCC_CORE



change to 0805

VCC_CORE

U43C

A7	VCC[001]	VCC[68]
A9	VCC[002]	VCC[69]
A10	VCC[003]	VCC[70]
A12	VCC[004]	VCC[71]
A13	VCC[005]	VCC[72]
A15	VCC[006]	VCC[73]
A17	VCC[007]	VCC[74]
A18	VCC[008]	VCC[75]
A20	VCC[009]	VCC[76]
B7	VCC[010]	VCC[77]
B9	VCC[011]	VCC[78]
B10	VCC[012]	VCC[79]
B12	VCC[013]	VCC[80]
B14	VCC[014]	VCC[81]
B15	VCC[015]	VCC[82]
B17	VCC[016]	VCC[83]
B18	VCC[017]	VCC[84]
B20	VCC[018]	VCC[85]
C9	VCC[019]	VCC[86]
C10	VCC[020]	VCC[87]
C12	VCC[021]	VCC[88]
C13	VCC[022]	VCC[89]
C15	VCC[023]	VCC[90]
C17	VCC[024]	VCC[91]
C18	VCC[025]	VCC[92]
D9	VCC[026]	VCC[93]
D10	VCC[027]	VCC[94]
D12	VCC[028]	VCC[95]
D14	VCC[029]	VCC[96]
D15	VCC[030]	VCC[97]
D17	VCC[031]	VCC[98]
D18	VCC[032]	VCC[99]
E7	VCC[033]	VCC[100]
E9	VCC[034]	
E10	VCC[035]	VCCP[01]
E12	VCC[036]	VCCP[02]
E13	VCC[037]	VCCP[03]
E15	VCC[038]	VCCP[04]
E17	VCC[039]	VCCP[05]
E18	VCC[040]	VCCP[06]
E20	VCC[041]	VCCP[07]
F7	VCC[042]	VCCP[08]
F9	VCC[043]	VCCP[09]
F10	VCC[044]	VCCP[10]
F12	VCC[045]	VCCP[11]
F14	VCC[046]	VCCP[12]
F15	VCC[047]	VCCP[13]
F17	VCC[048]	VCCP[14]
F18	VCC[049]	VCCP[15]
F20	VCC[050]	
AA7	VCC[051]	
AA9	VCC[052]	
AA10	VCC[053]	
AA12	VCC[054]	
AA13	VCC[055]	
AA15	VCC[056]	
AA17	VCC[057]	
AA18	VCC[058]	
AA20	VCC[059]	
AB9	VCC[060]	
AC10	VCC[061]	
AB10	VCC[062]	
AB12	VCC[063]	
AB14	VCC[064]	
AB15	VCC[065]	VCCSENSE
AB17	VCC[066]	
AB18	VCC[067]	VSSSENSE

PZ47823-2743-42

VCC_CORE

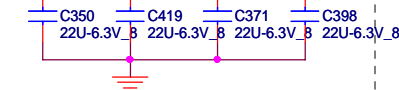
+1.05V

VCC CORE

+1.5V

+1.05V 2,3,6,8,9,10,14,17,44
VCC_CORE 41
+1.5V 8,10,15,17,29,33,42,43

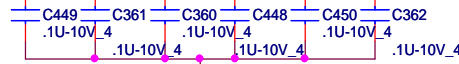
VCC_CORE



+1.05V

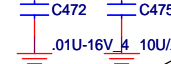
+1.05V

330U-2.5V-7343



near CPU B26

+1.5V



.01U-16V_4 10U/X5R-6.3V_8

+1.5V

B26 VCCA (1.5v) is a power source required by the PLL clock

VCCA

VID[0]

VID[1]

VID[2]

VID[3]

VID[4]

VID[5]

VID[6]

AD6	H_VID0	41
AE5	H_VID1	41
AE5	H_VID2	41
AE4	H_VID3	41
AE3	H_VID4	41
AE2	H_VID5	41
AE2	H_VID6	41

VCC_CORE

R221

*100/F_4

VCCSENSE

41

VSSSENSE

41

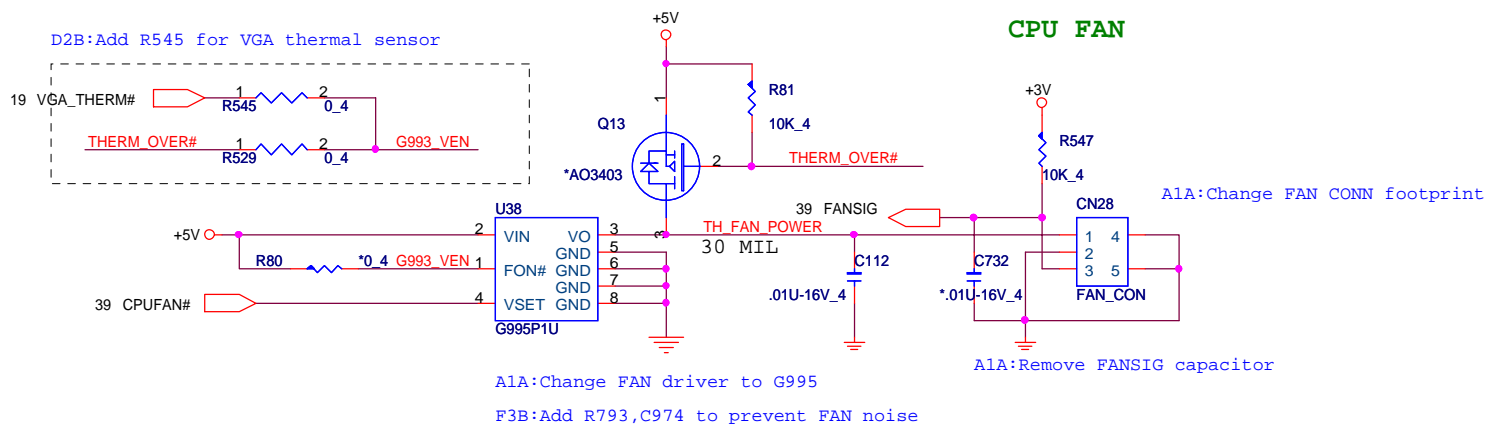
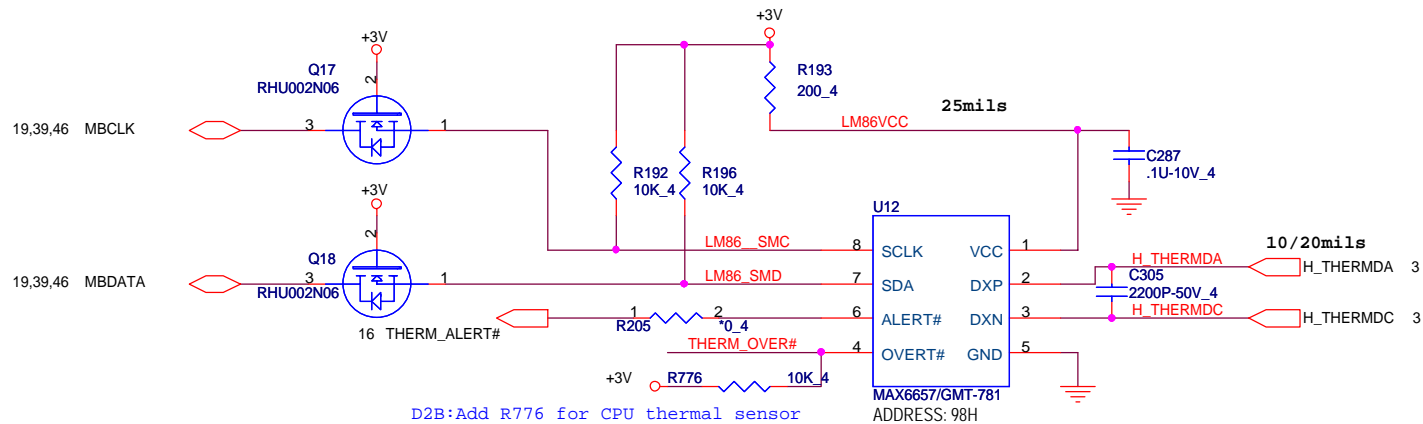
A1A:Reversed VCCSENSE/VSSSENSE on Vcore side

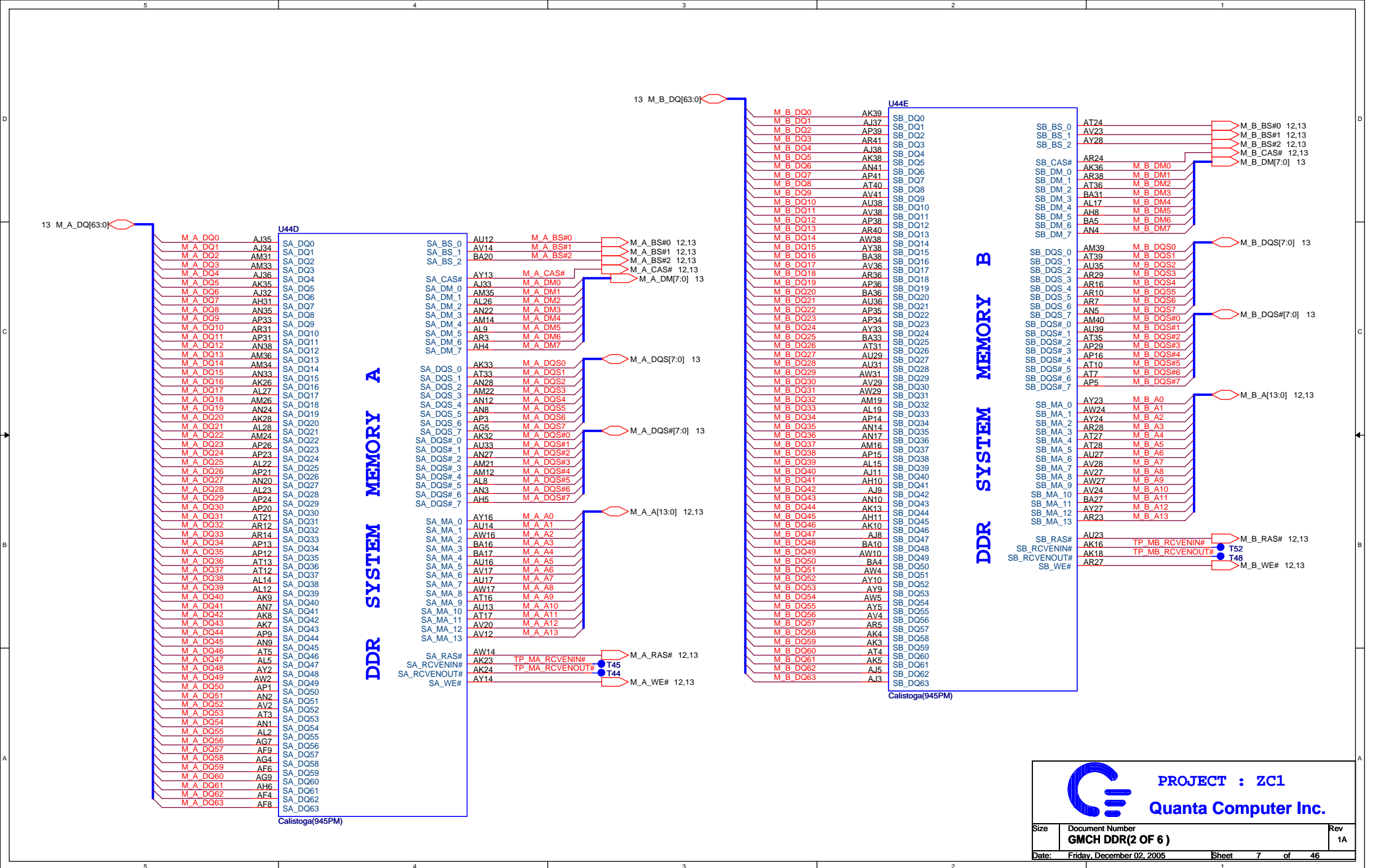



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(2 OF 2)	1A
Date:	Monday, November 28, 2005	Sheet 4 of 46

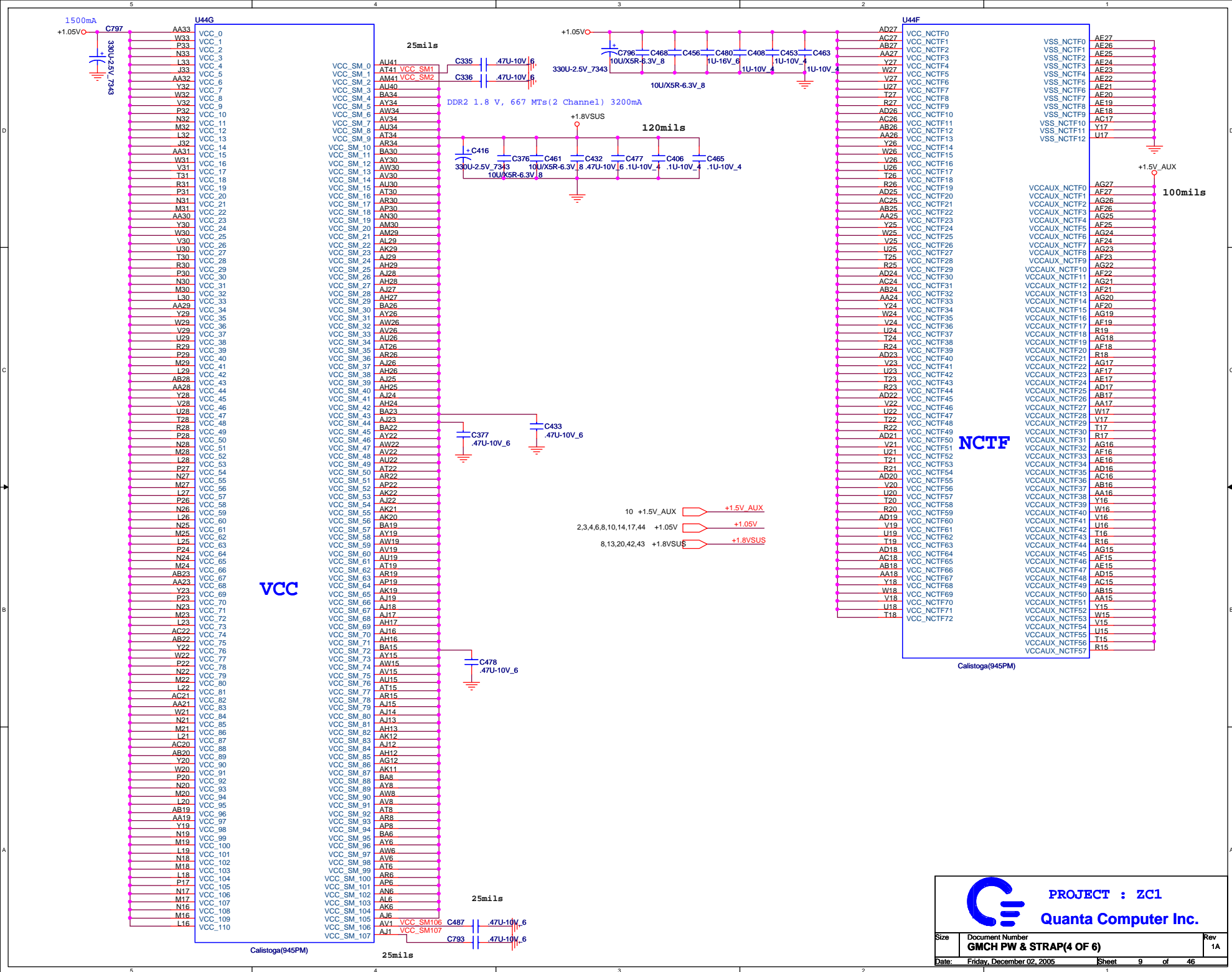


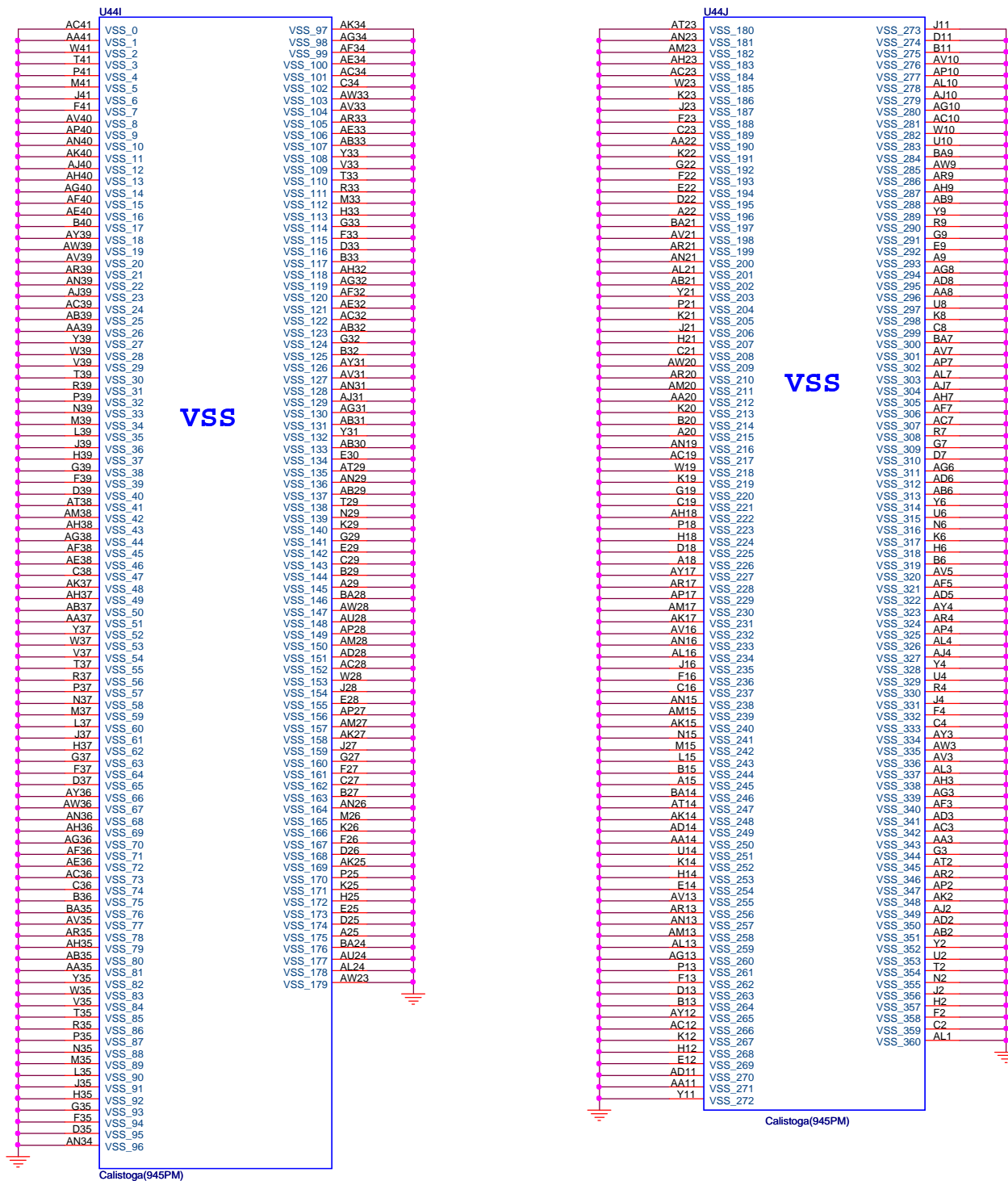




PROJECT : ZC1
Quanta Computer Inc.

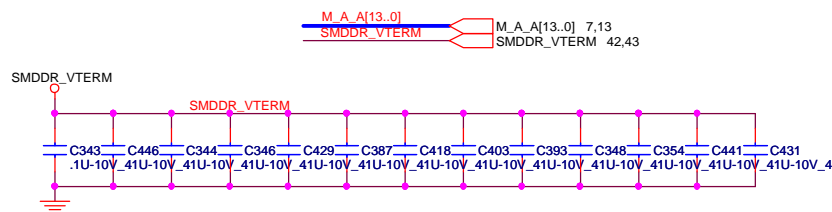
Size	Document Number GMCH DDR(2 OF 6)	Rev 1A
Date:	Friday, December 02, 2005	Sheet 7 of 46



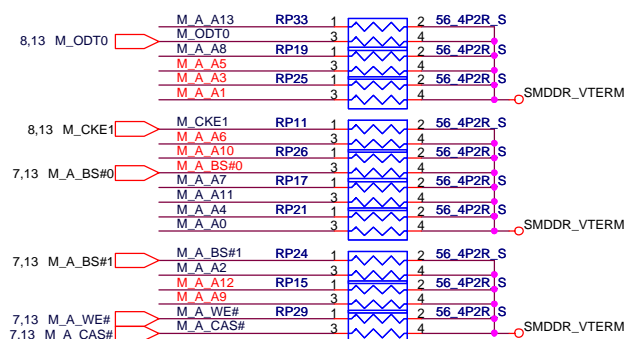


DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

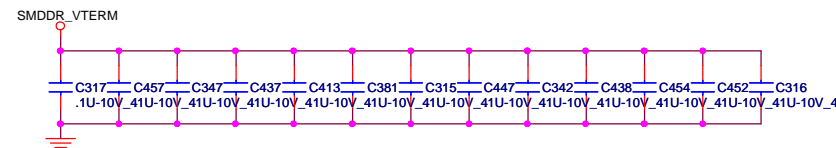


A1A:Swap net



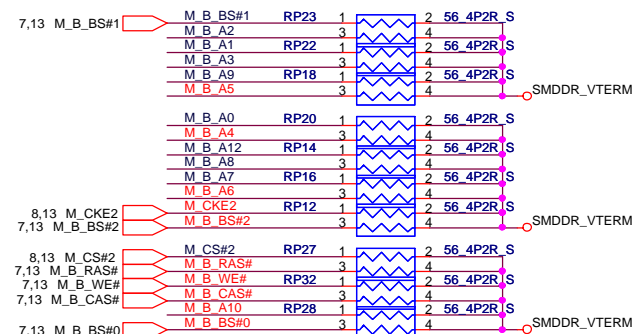
Legend:
 M_B_A[13..0] → M_B_A[13..0] 7,13
 +1.8VSUS → +1.8VSUS 8,9,13,20,42,43
 +3V → +3V 2,5,8,10,13,14,15,16,17,18,19,20,24,25,26,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44

DDRII B CHANNEL

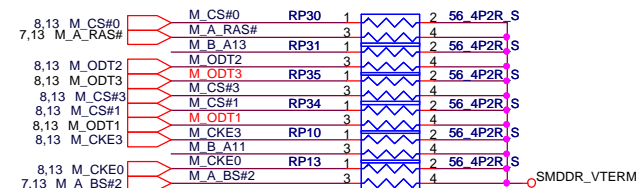


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

A1A:Swap net

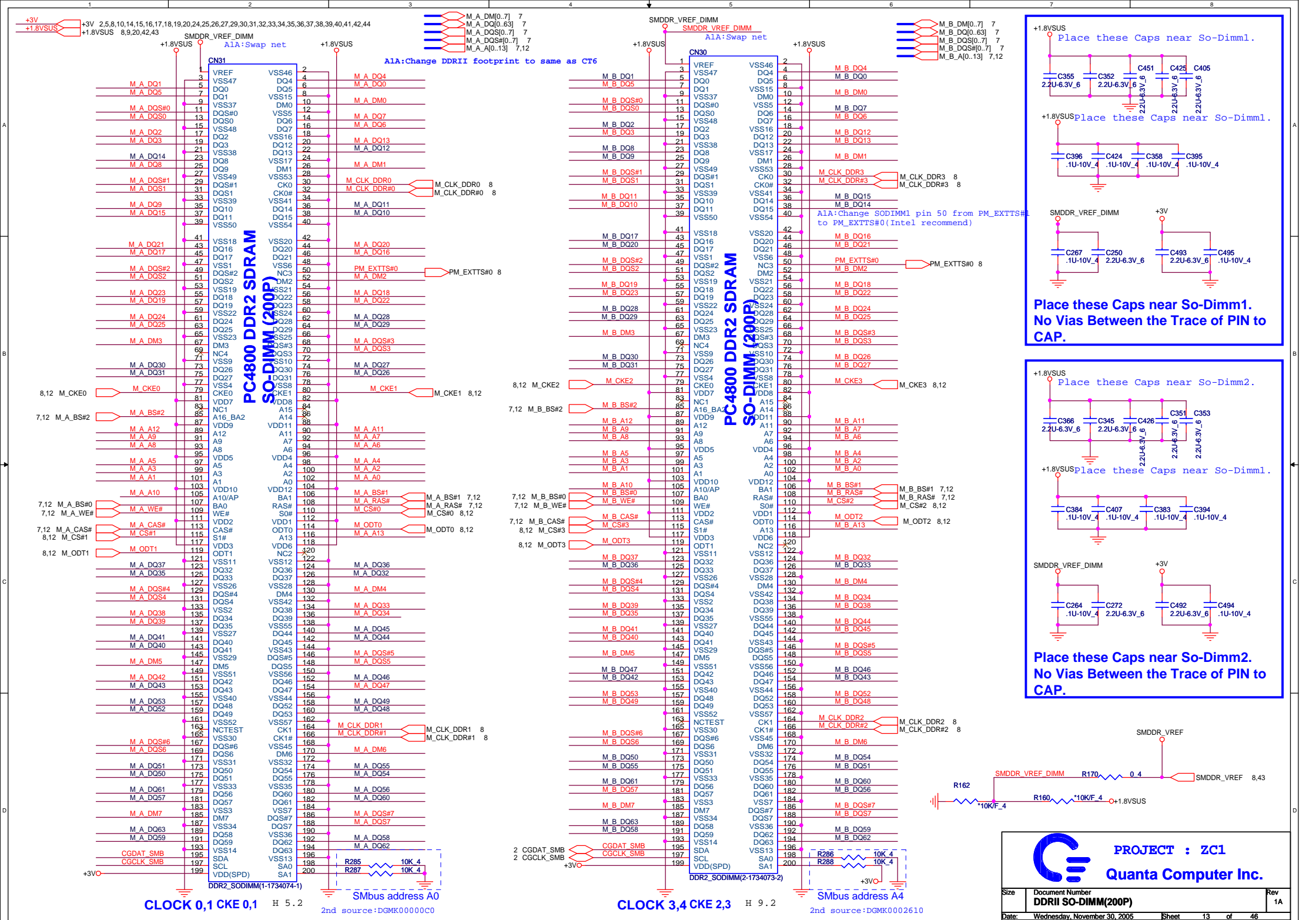


A1A:Swap net

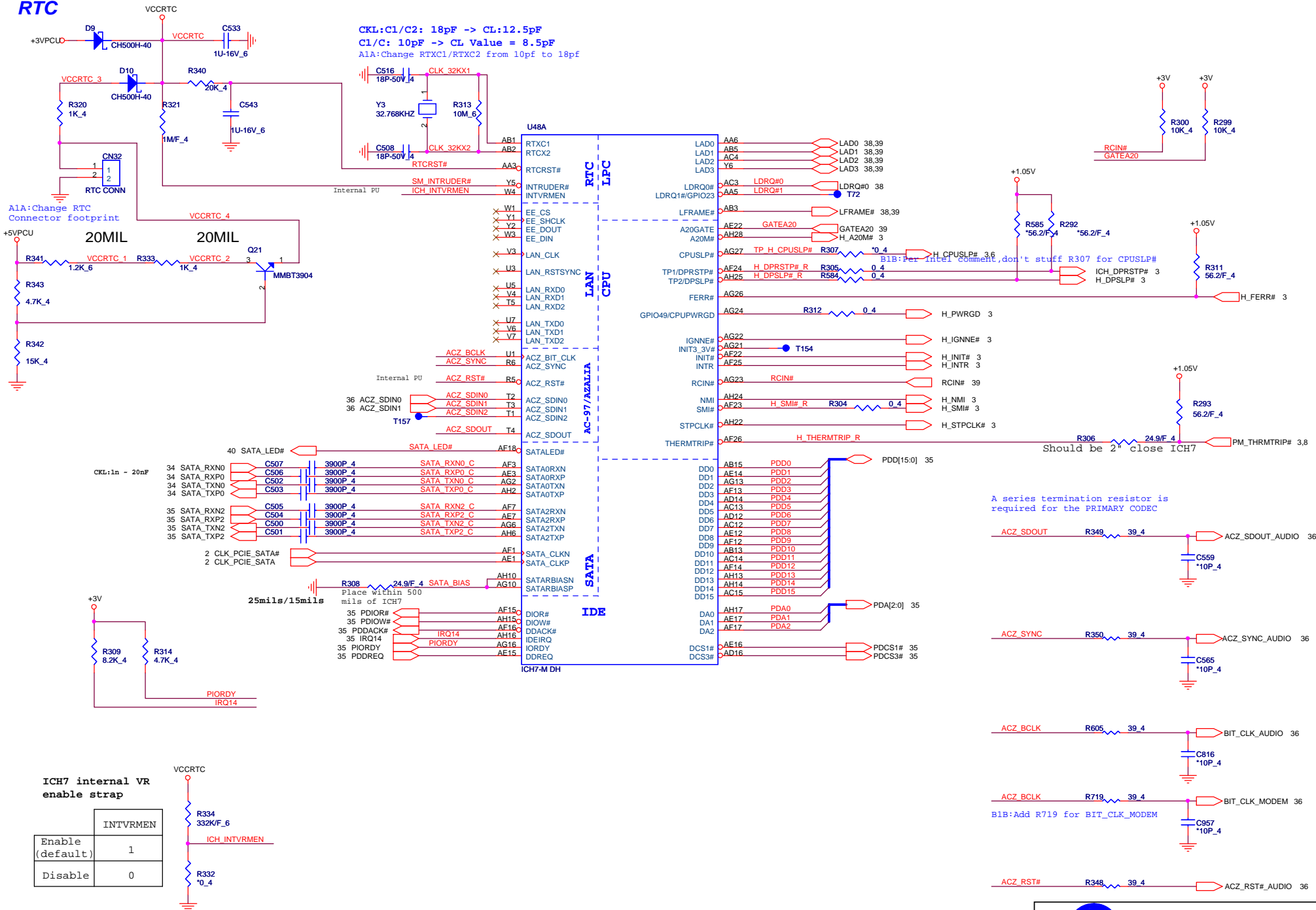


PROJECT : ZC1
 Quanta Computer Inc.

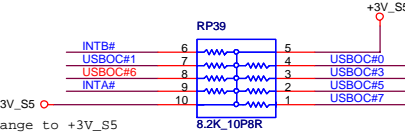
Size	Document Number	Rev
	DDR RES. ARRAY	1A
Date:	Monday, November 28, 2005	Sheet 12 of 46



RTC



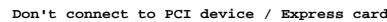
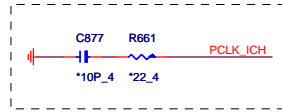
EZ4_2



D2B:Change to +3V_S5

CKL use 10Kohm

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

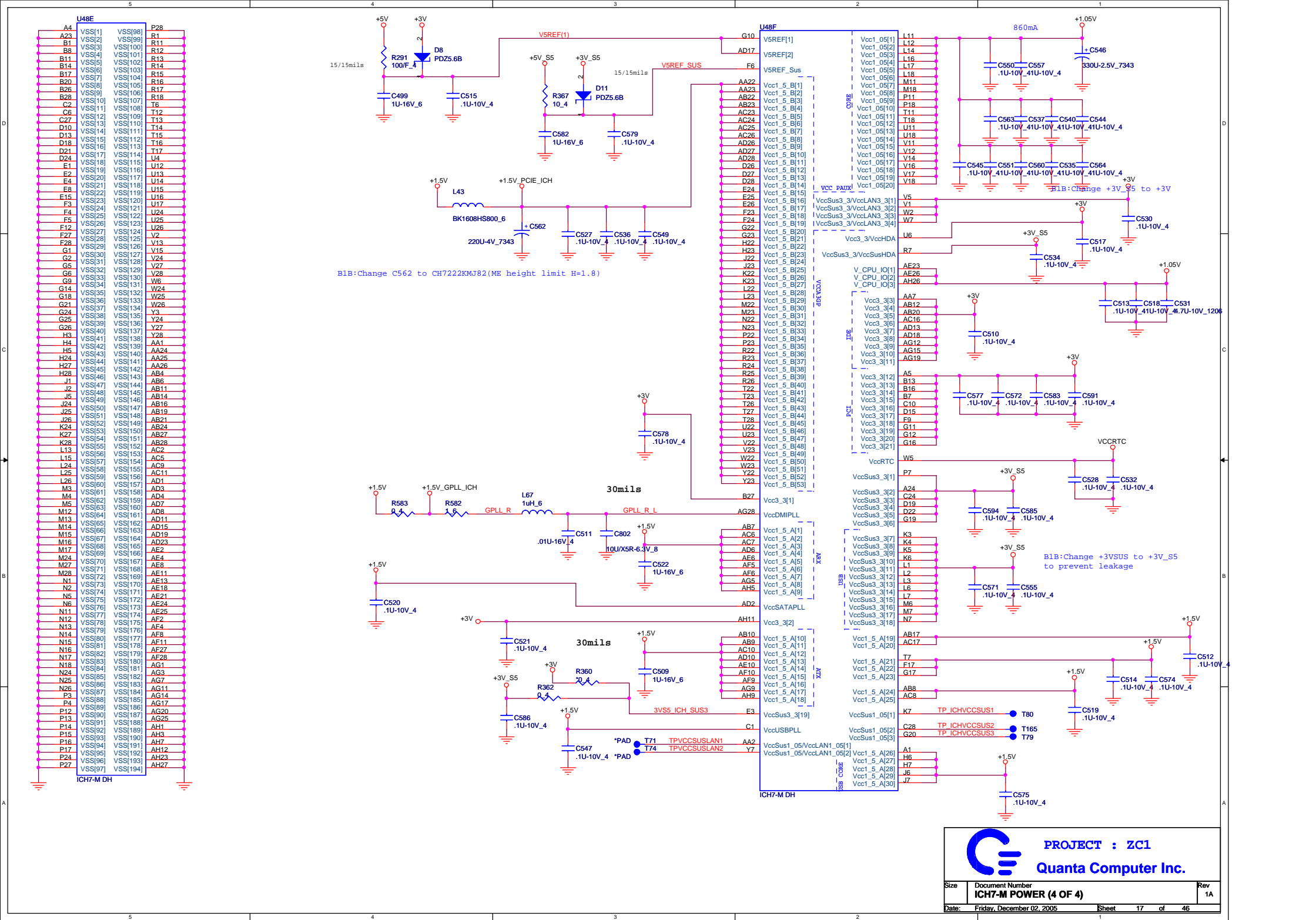


PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
OZ711MP1	AD25	REQ0# / GNT0#	INTE#



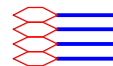
PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number ICH7-M PCI E (2 OF 4)	Rev 1A
Date:	Friday, December 09, 2005	Sheet 15 of 46

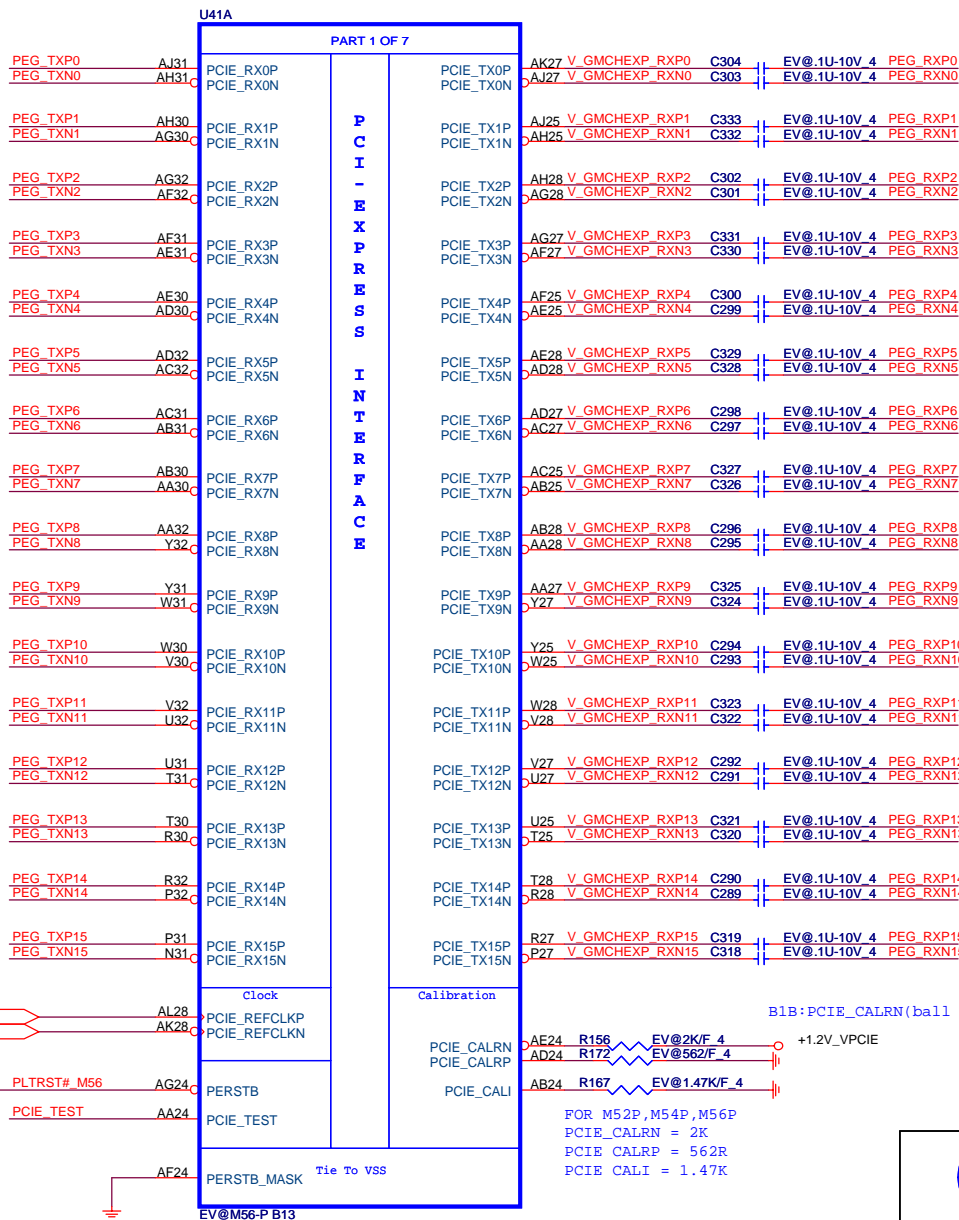
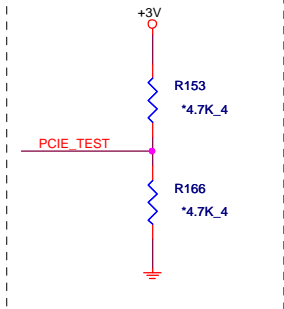


PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

8 PEG_RXP[15:0]
8 PEG_RXN[15:0]
8 PEG_TXP[15:0]
8 PEG_TXN[15:0]



ATI FEATURE NOT ENABLED (M52P,M54P,M56P)
B1B:Don't stuff R153,R166 for PCIE_TEST



B1B:PCIE_CALRN(ball AE24) need change to +1.2V_VPCIE

FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE_CALRP = 562R
PCIE_CALI = 1.47K



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Quanta Computer Inc.

Size	Document Number M56P 1 OF 7	Rev 1A
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MEMORY CLOCK SPREAD SPECTRUM

ANY UNUSED GPIO CAN OPTIONALLY
BE MEMORY TYPE CONFIG STRAPS

C1C:Change GPIO27 instead of GPIO25 for MEMTYPE_1
E3A:Add R792 for MEMTYPE_1

24 MEMTYP_1
24 MEMTYP_0

B1B:Change R177,R181 to 0 ohm for VGA 27MHz

EV@CY25819
MK1726-8

27M_IN EV@0.4
27M_O "0.4

VGA27M
R550

R551

EV@0.4
R181

MK PD

EV@71.5F.4

C739

EV@10P.50V.4

R171

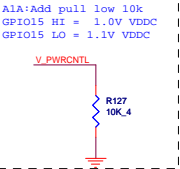
EV@10K.4

B1B:Don't stuff C739

Voltage divider resistor values R181
and R551 to ensure XTALIN/XTALOUT
voltage level matches vddc

AlA:Reversed LVDSCLK, LVDSDATA
pull high to LVDS side

AlA:change LVDS_DAT/LVDS_CLK
to DVPDATA18/DVPDATA19

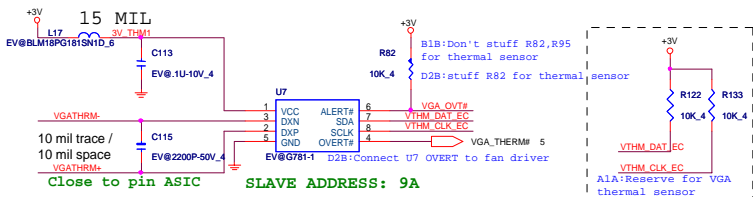


V_PWRCTRL DRIVEN HI SELECT 1.0V VDDC
V_PWRCTRL DRIVEN LO SELECT 1.1V VDDC

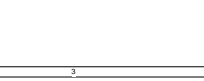
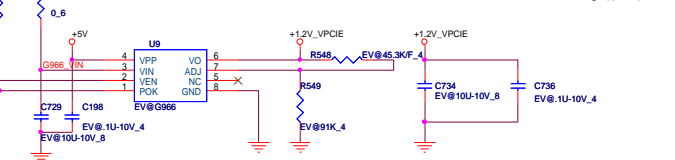
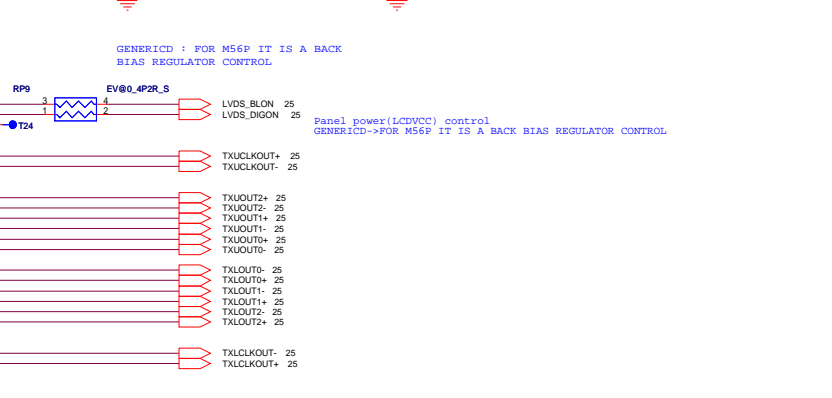
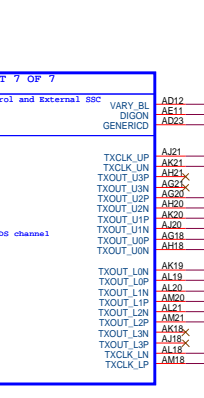
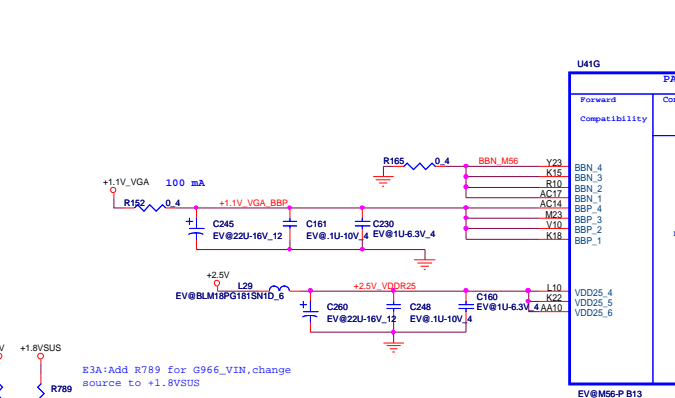
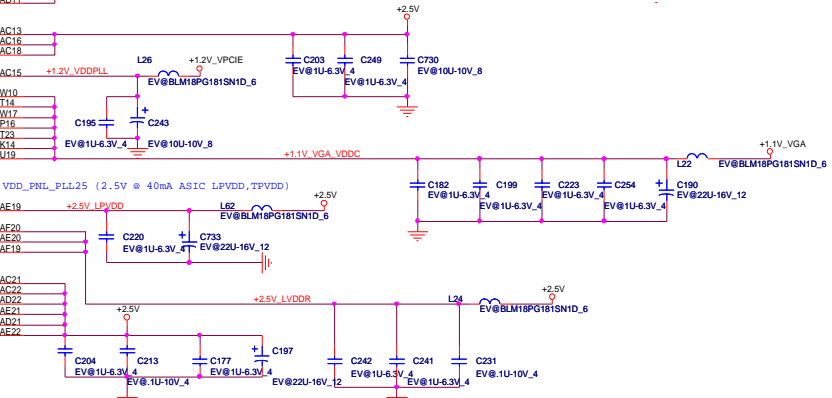
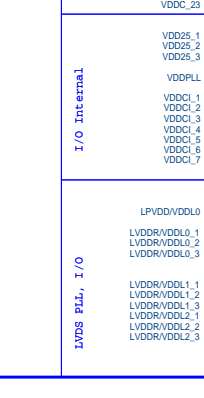
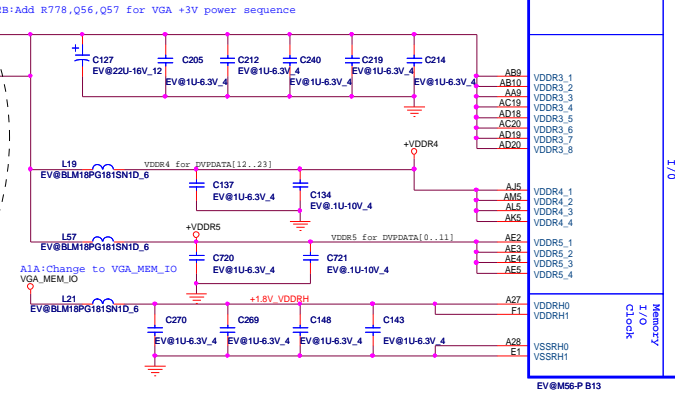
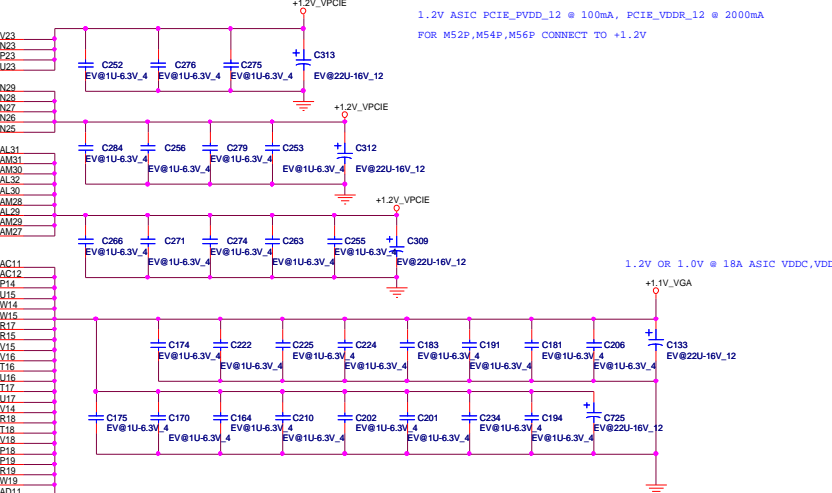
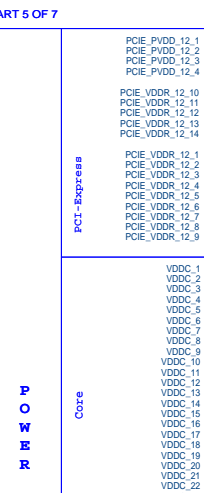
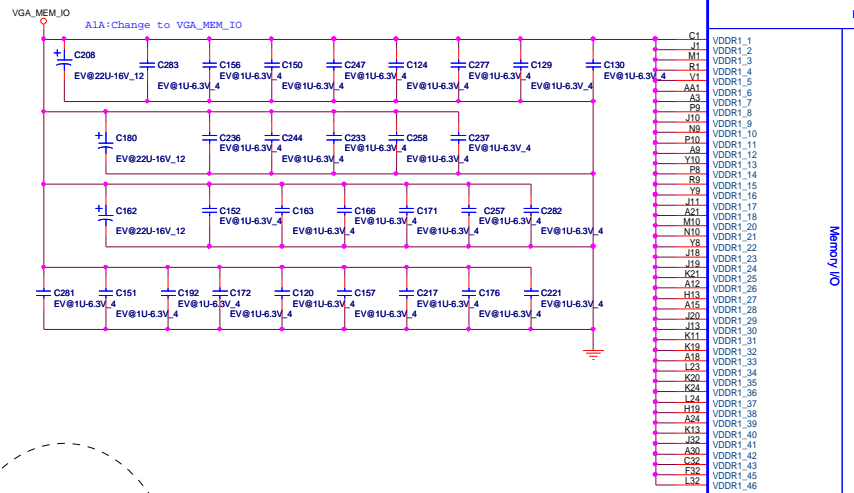
For m26x,m52p,m54p,m56p thermal interrupt
is low edge and connects to gpio17

FOR M52P,M54P,M56P CONNECT TO +2.5V

1.2V OR 1.0V @ 20mA ASIC MPVDD
CONNECT TO VDDC



IF memory interface has to be up to 600MHz or above, the GPU core voltage and memory I/O voltage may need to be increased to 1.2-1.3V and 2.0V



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	M56P POWER	1A
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Channel B



DOMB[0..7] 22
RDQSB[0..7] 22
WQDSB[0..7] 22
MDB[0..63] 22




```
GPIO_[13:0] have internal PD
AlA:Change GPIO0 to high
```

```
GPIO_[13:0] have internal PD
AlA:Change GPIO0 to high
```

Ground  High logic voltage

BOM

```
GPIO[13:12] = 00:128M memory aperture  
GPIO[13:12] = 01:256M memory aperture  
GPIO[13:12] = 10:64M memory aperture  
GPIO[13:12] = 11:Reversed
```

BOM Memory ID

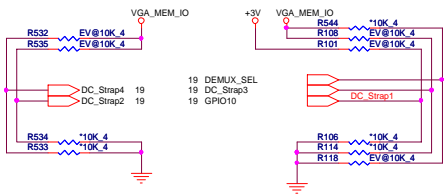
STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26X, M50P - INSTALL WITH ATI R8480, R8400, RX480, RC410, R8482 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE(M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM. AP. SIZE=0(128MB) 001x - No ROM, MEM. AP. SIZE=0(128MB) 010x - No Rom, MEM. AP. SIZE=1(256MB) 011x - No ROM, MEM. AP. SIZE=1(Reserved) 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1100 - Serial NX25F011B ROM (SSI), chip IDs from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC, GENERIC	ATI FEATURE NOT ENABLED (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	H2SYNC	RSVD	
	PCIE_TEST	RSVD	

AlA:change ROMIDCFG(3:0) to 0010

REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	MEMORY TYPE AND SPEED SELECT Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory(256Mb) 136 Ball BGA package 01 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Infineon GDDR 3 memory(256Mb) 136 Ball BGA package 11 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package	00
DC_Strap1	GPIO(10)	Internal TMD5 Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Not detected	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)	1

MEMORY TYPE AND SPEED SELECT



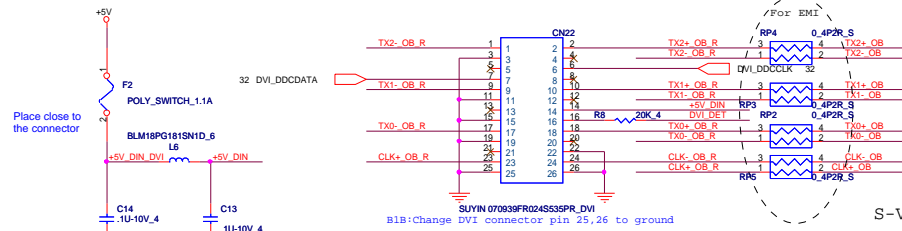
```
AlA:change video capture
enable setting
```



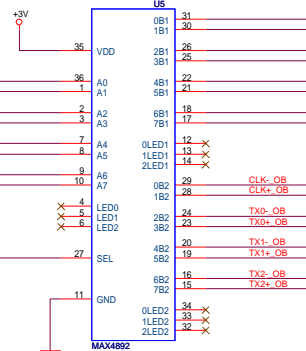
PROJECT : ZC1
Quanta Computer Inc.

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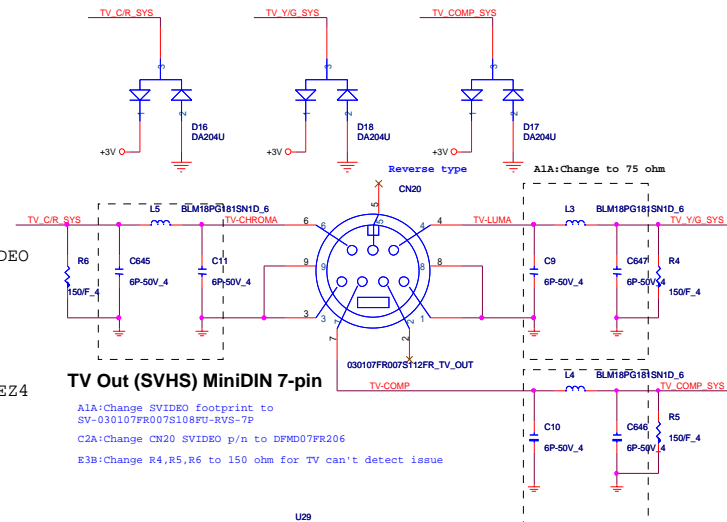
DVI-I CONNECTOR (DVI-D)

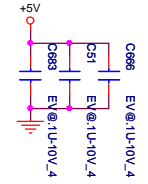
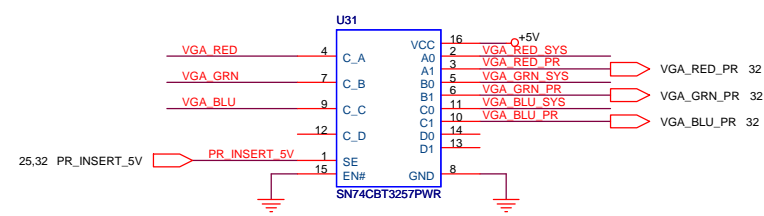
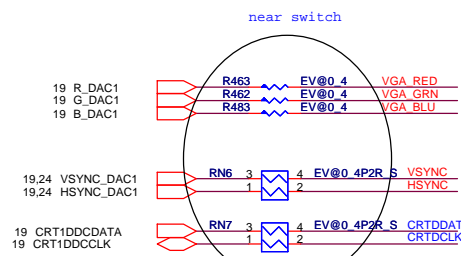


DVI PORT

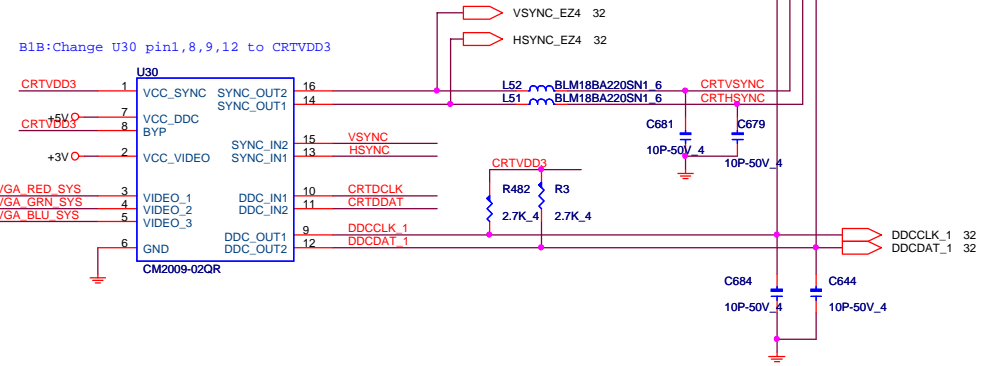
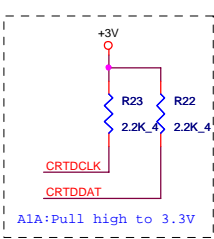
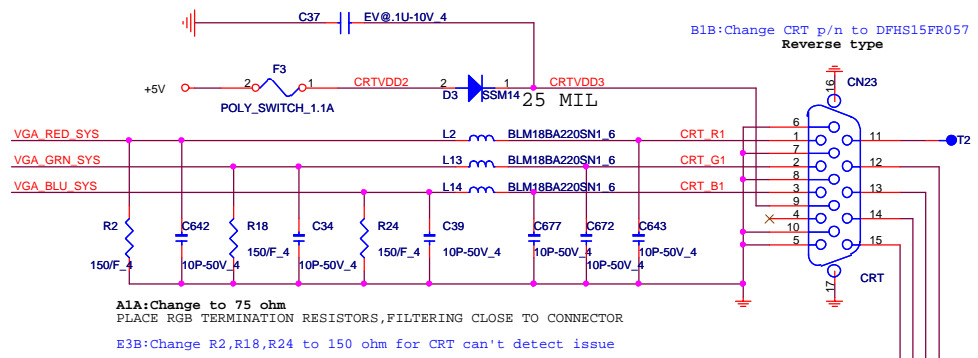


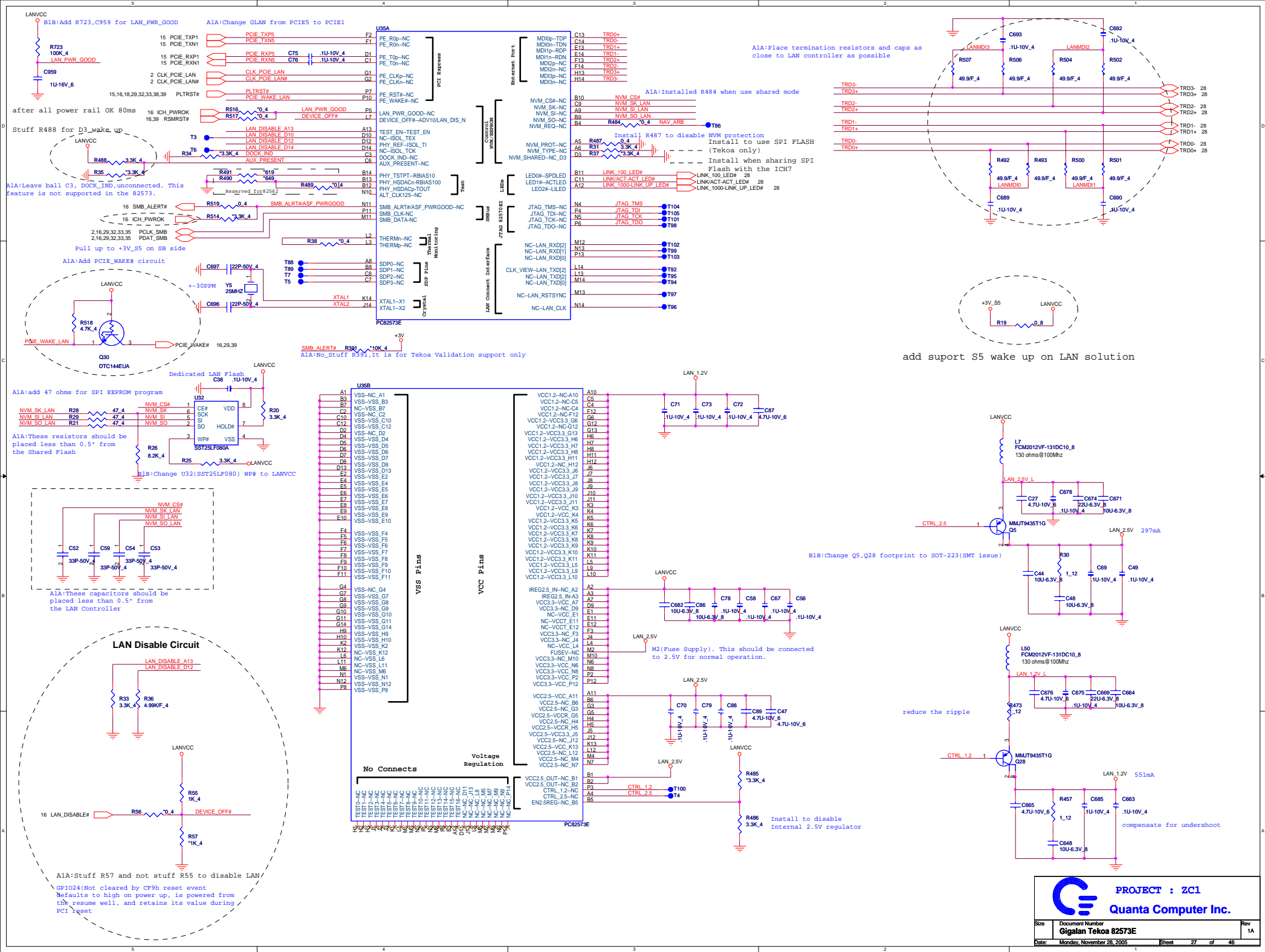
SEL	FUN
H	B2
L	B1

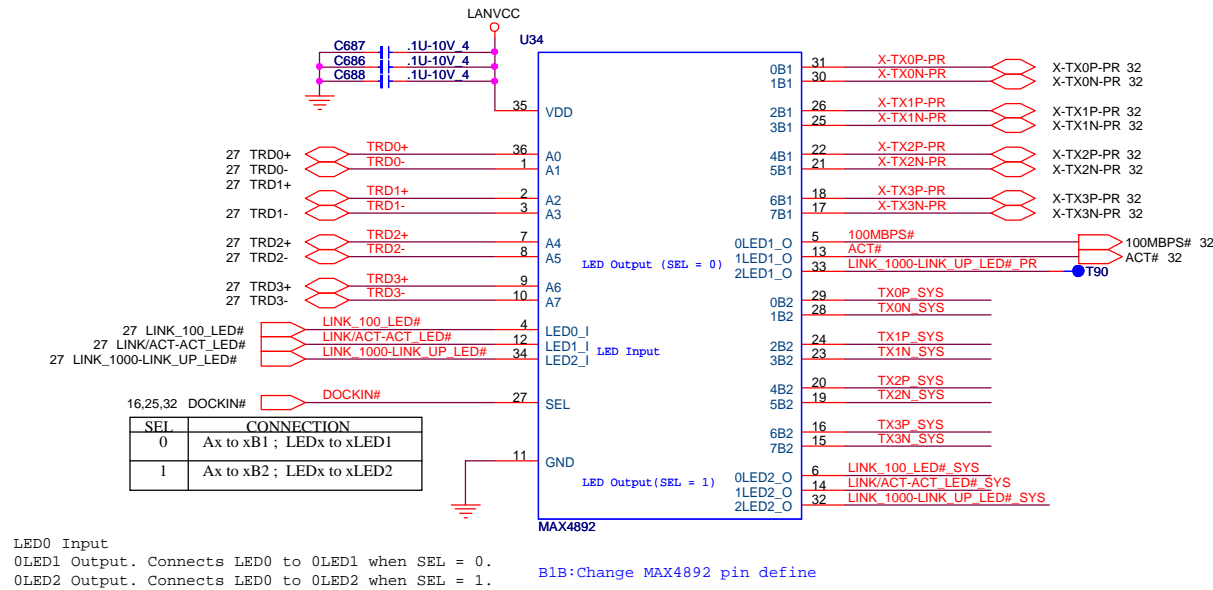




B1B:Remove UMA CRT support

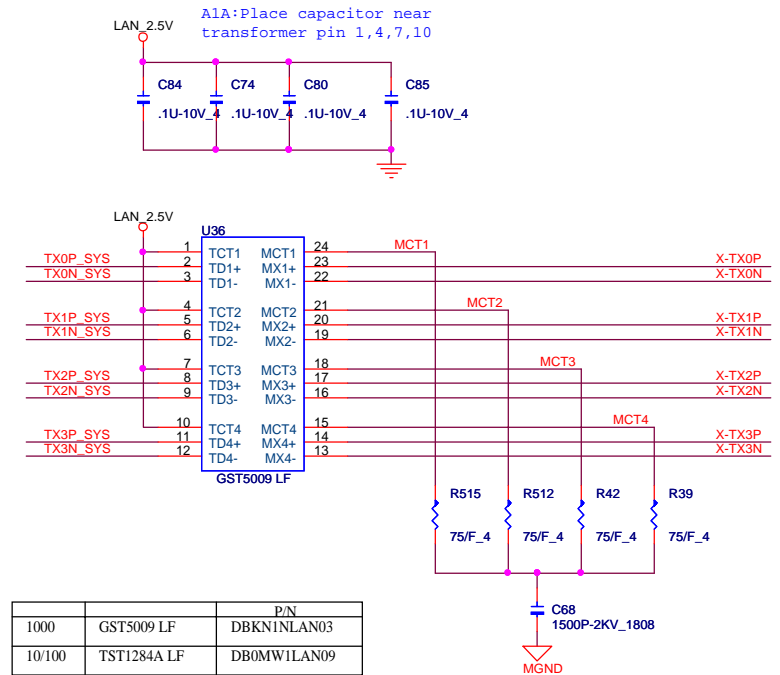
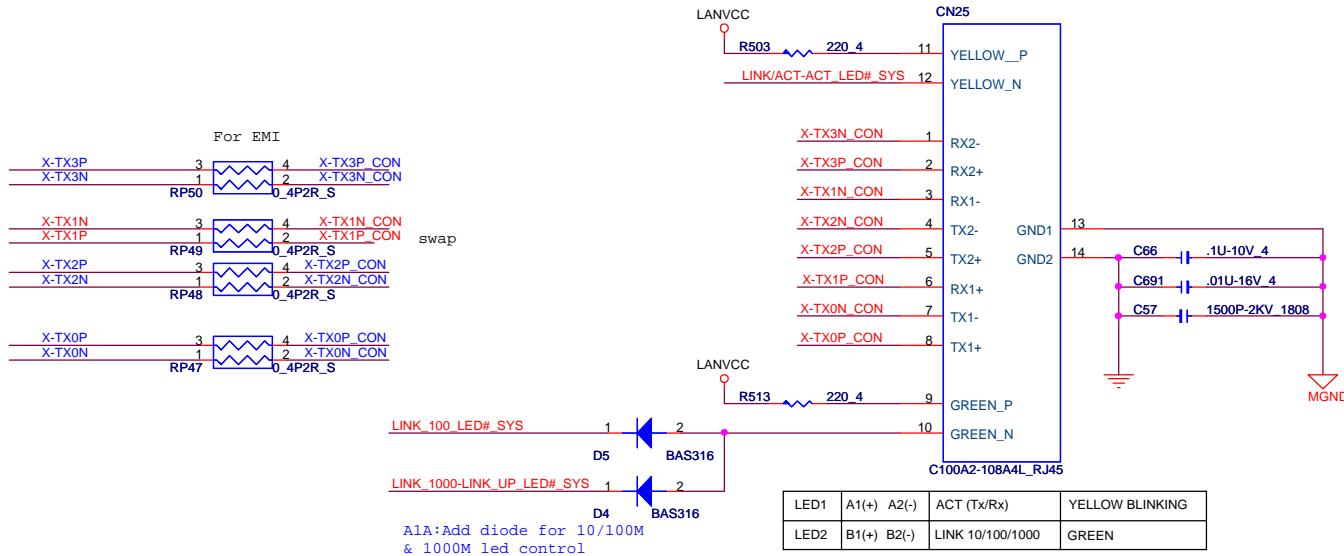






B1B:Change MAX4892 pin define

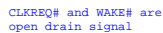
A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define



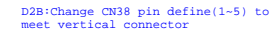
PROJECT : ZC1
Quanta Computer Inc.

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TRANSFORMER/RJ45 Rev A
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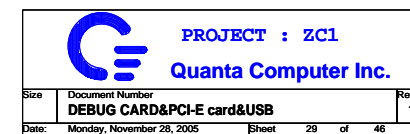
BOT contact



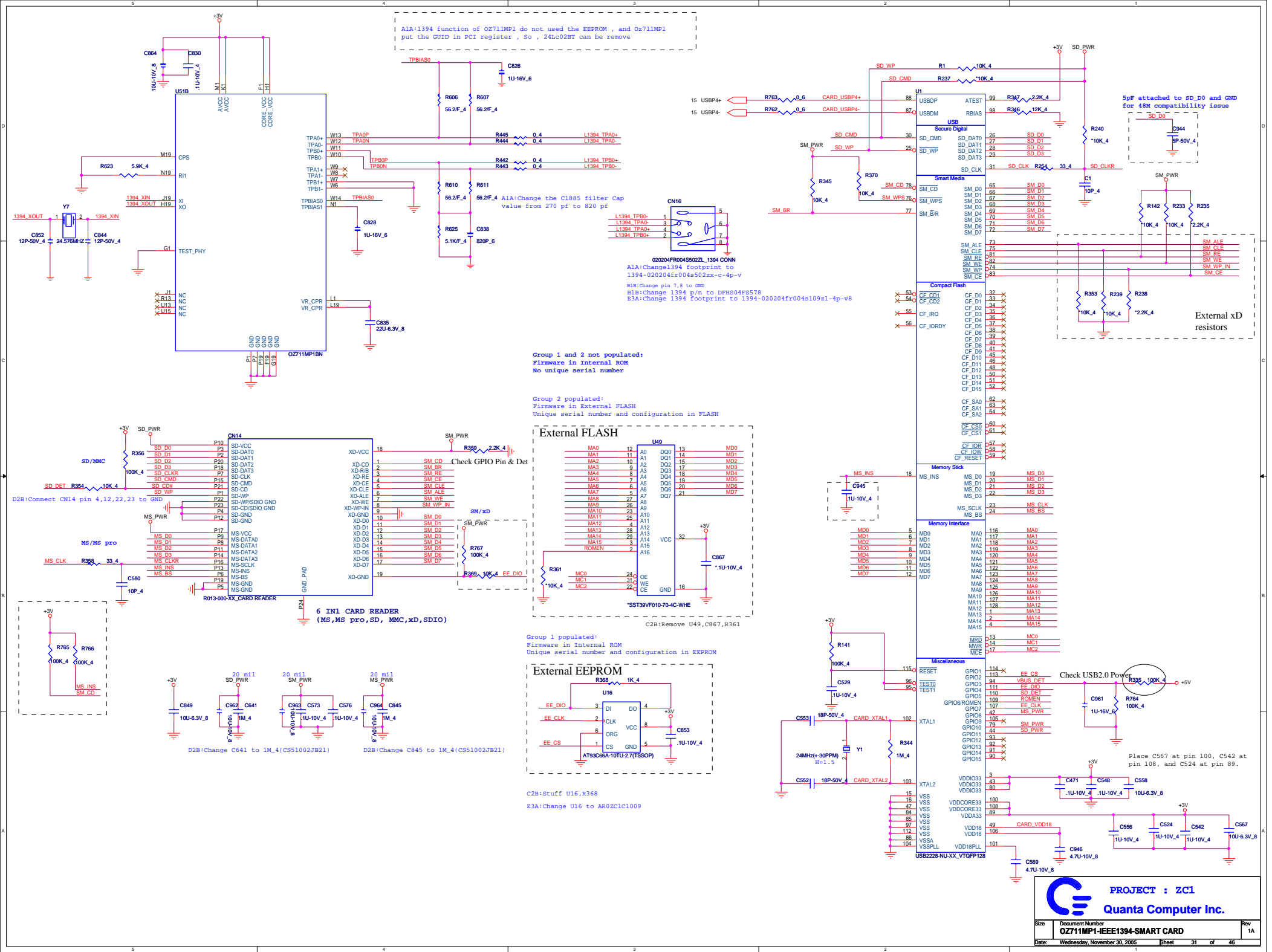
Q43 A1A:Change BT CONN to 5 pin

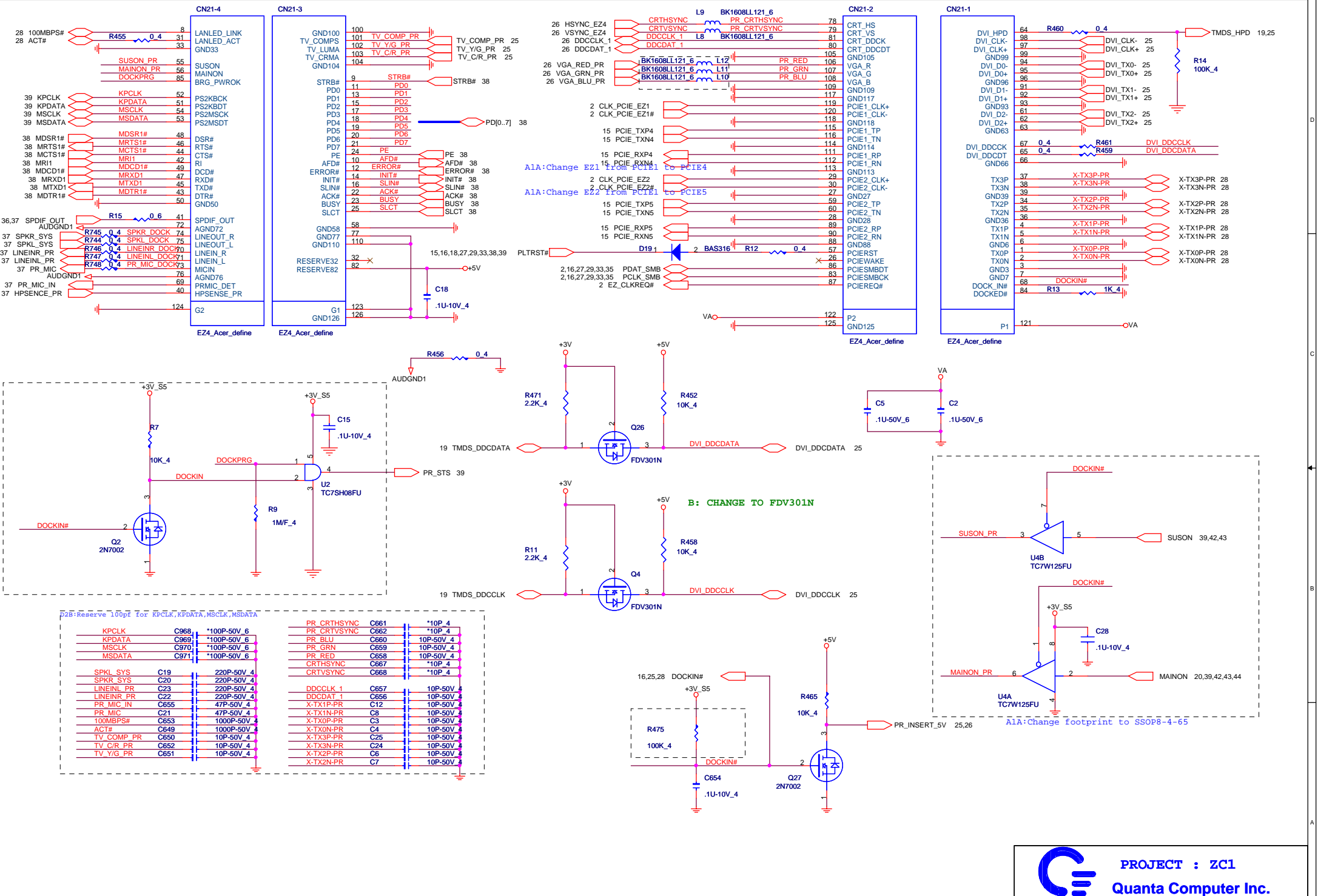


80mil



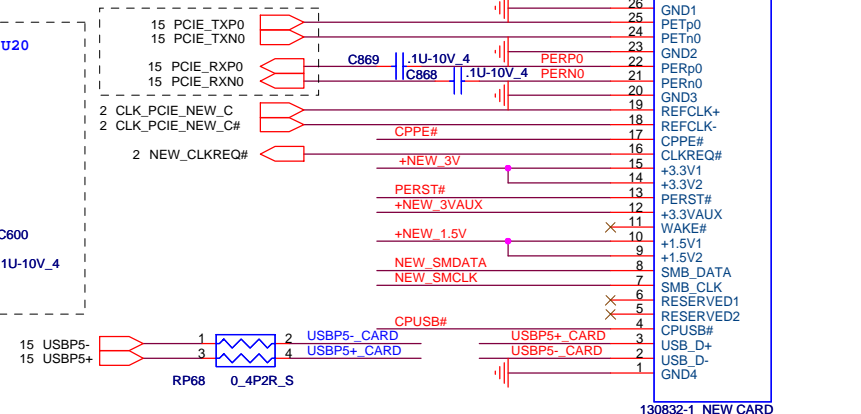
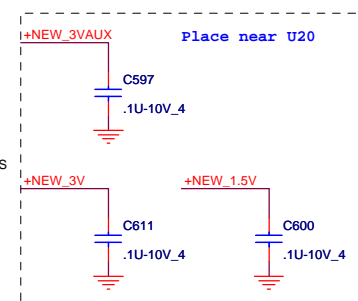






AlA:Change New card to small type(130832-1)
Reverse

CN35



130832-1_NEW CARD

Place near CN35

+NEW_3VAUX

C837
.1U-10V_4

+NEW_3V

C857
4.7U-10V_8


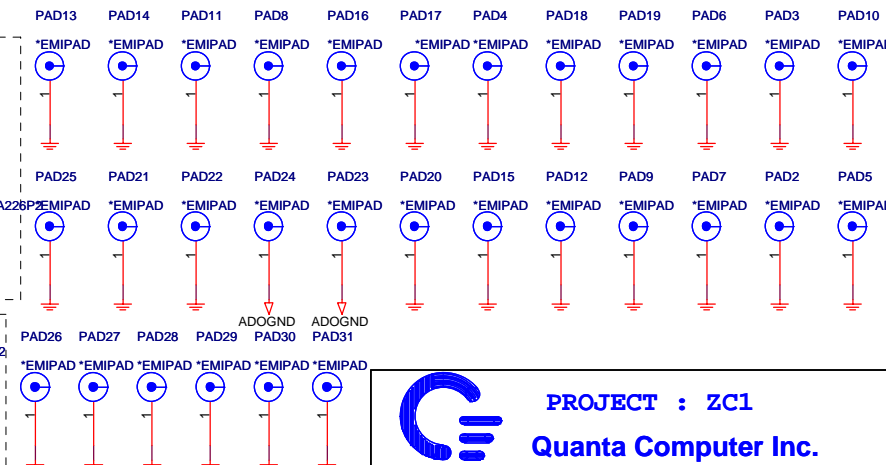
C843
.1U-10V_4

C847
.1U-10V_4

+NEW_1.5V

C829
4.7U-10V_8

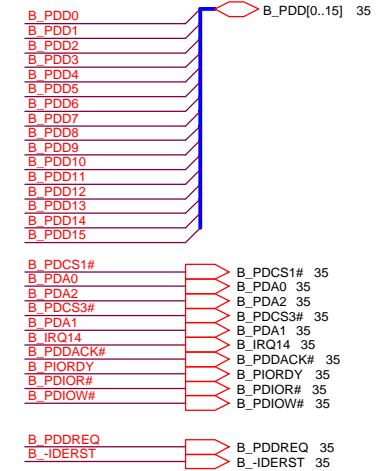
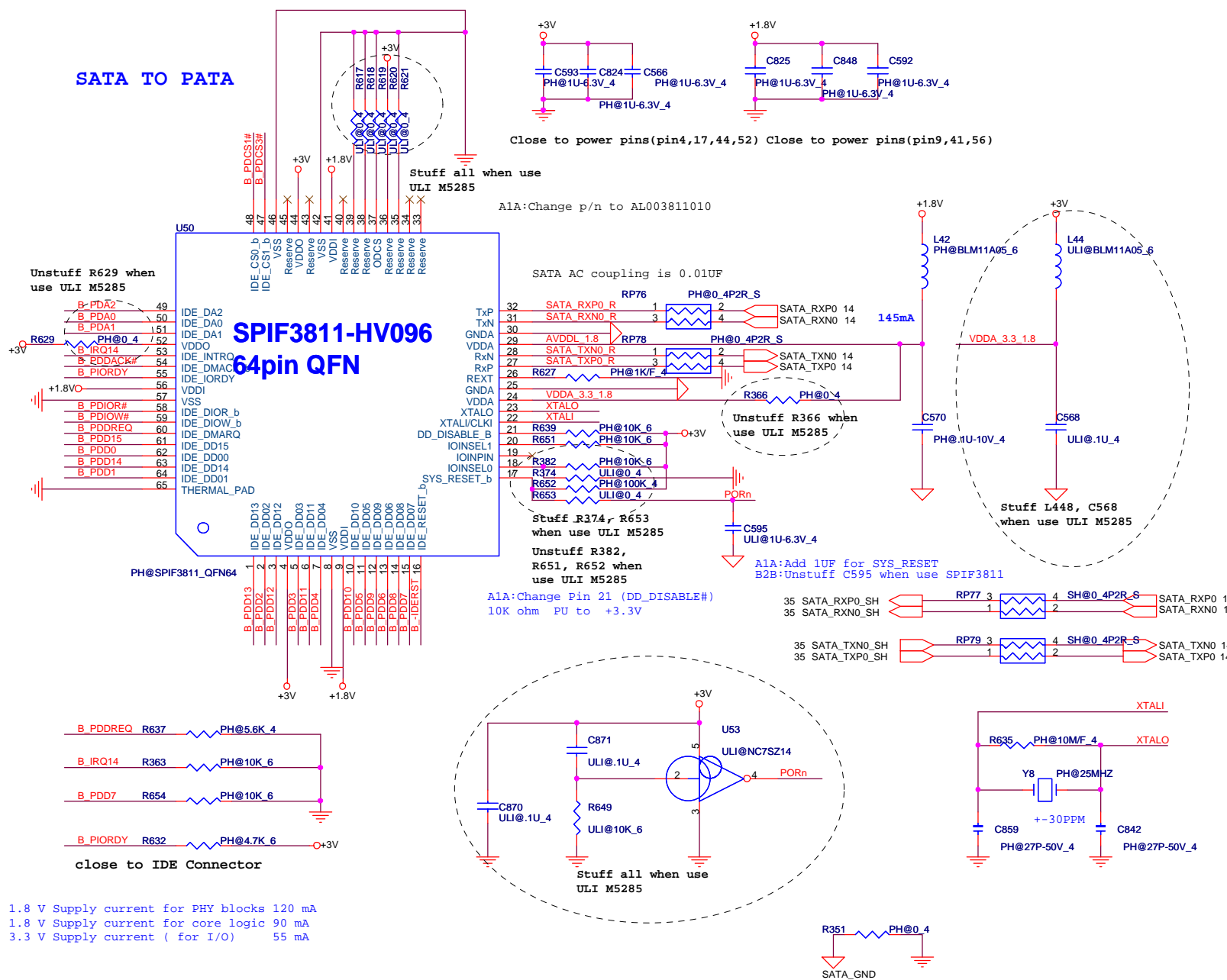
C834
.1U-10V_4



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SATA TO PATA



Reference clock select

ATAIOEN	Note
0	disable PATA output
1	enable PATA output

Operation Mode

MODE[2..0]	
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	Device mode 150MB/S
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVED

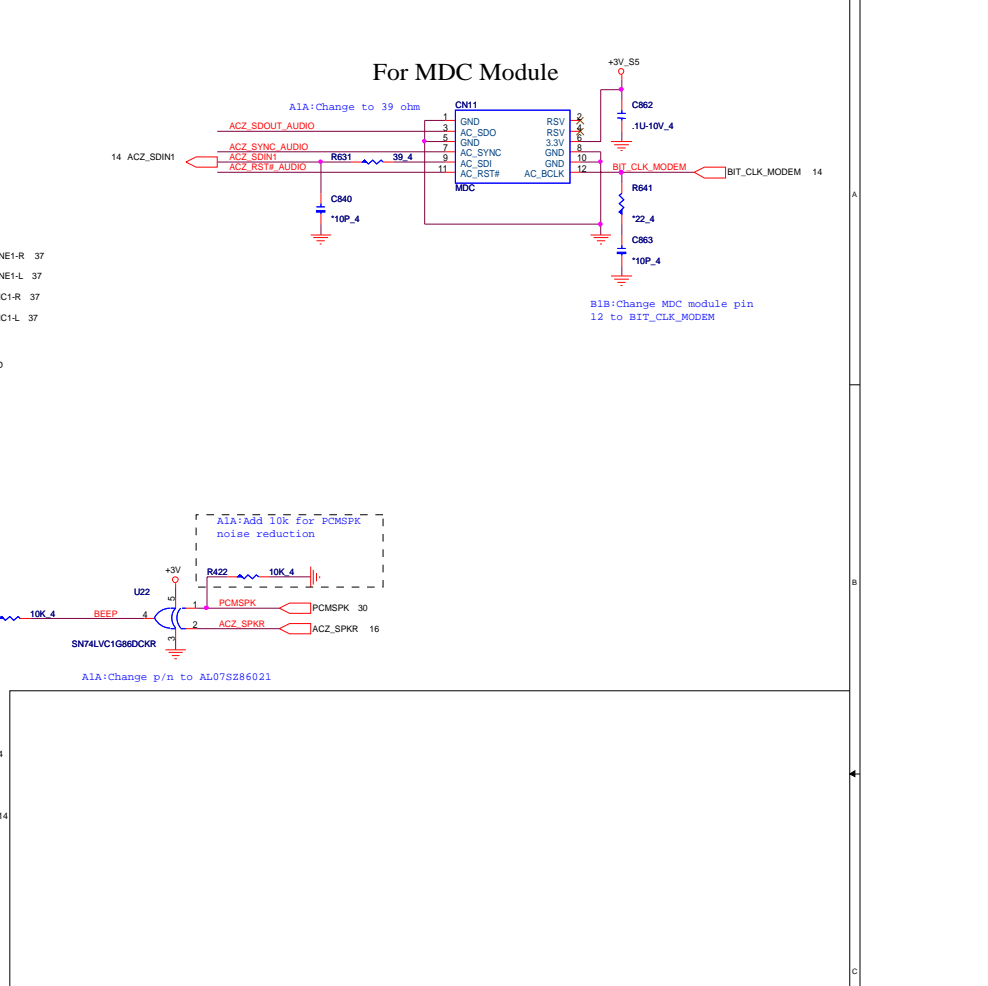
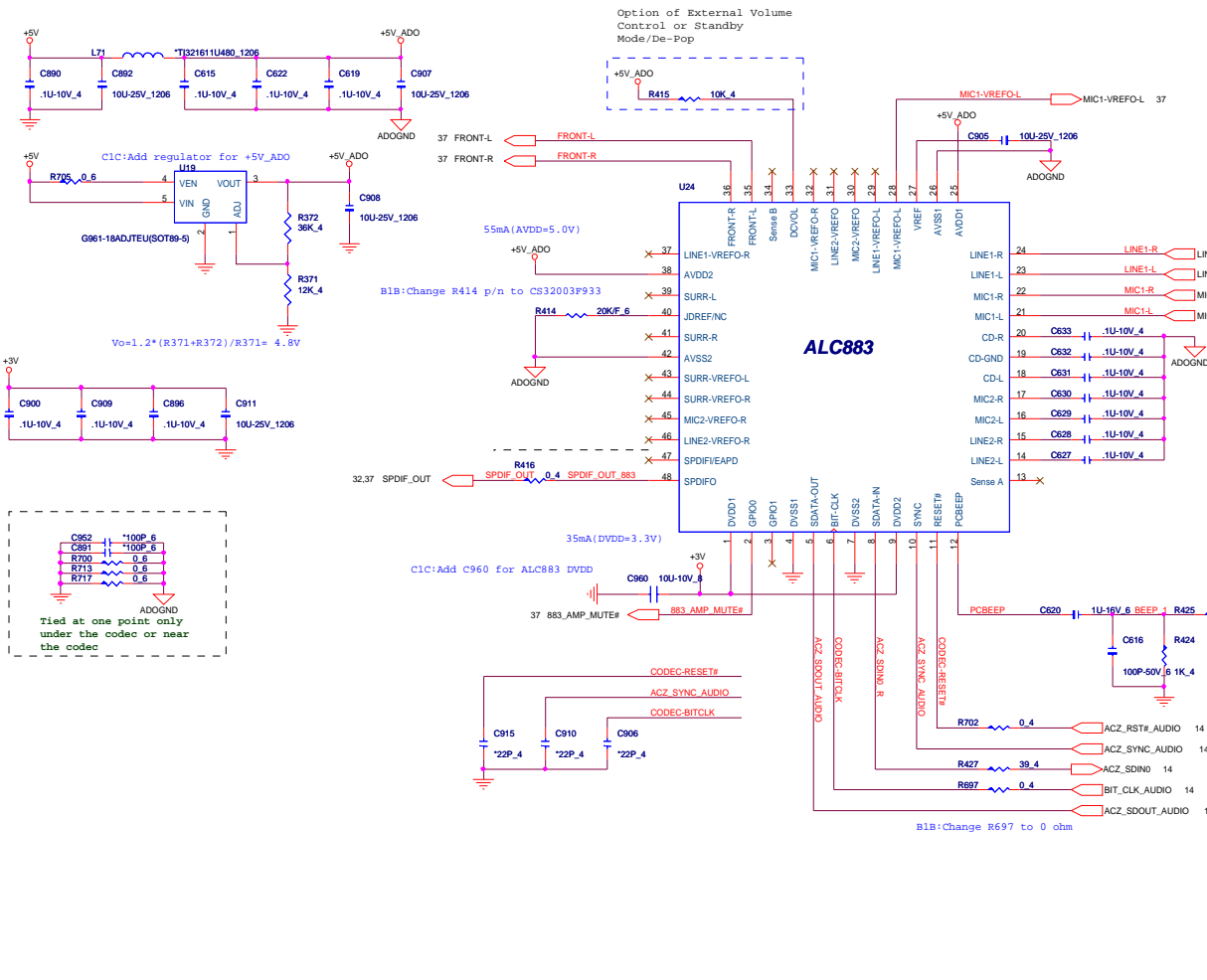
Reference clock select

CLKSEL[1..0]	External clock
0 0	20 MHZ
0 1	25 MHZ

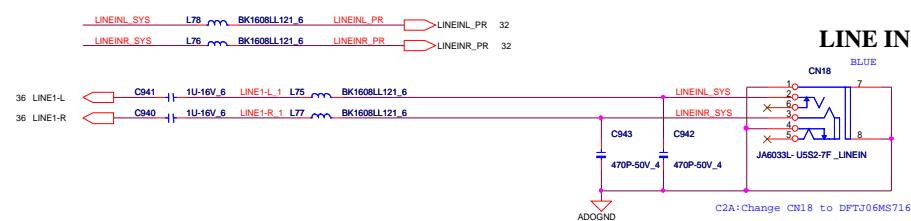
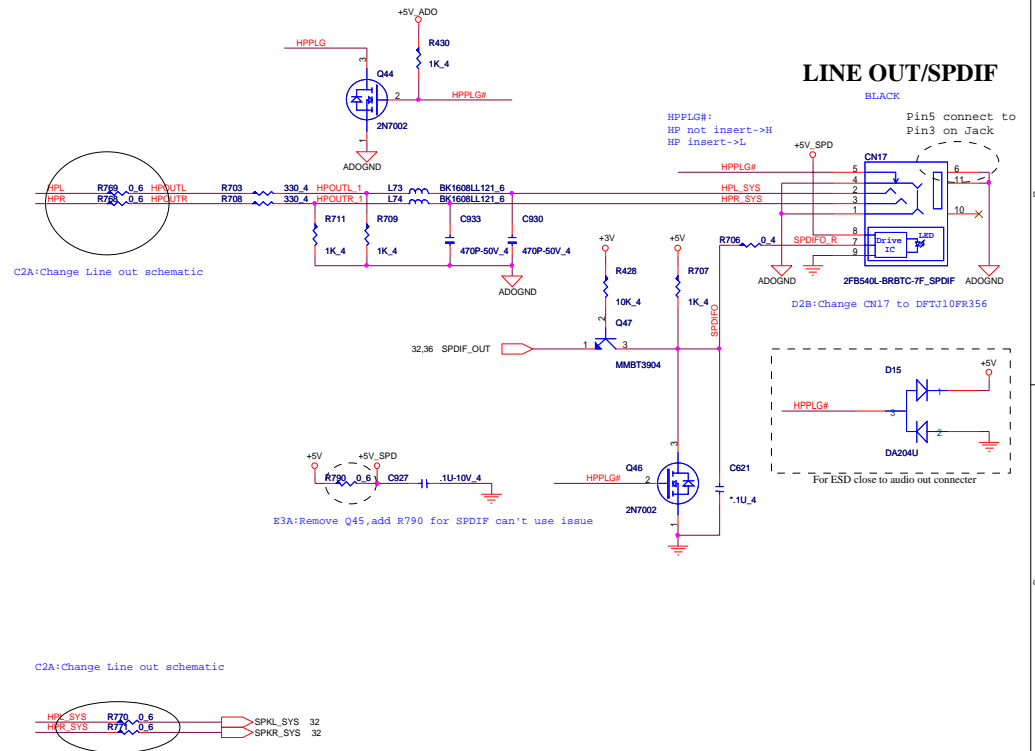
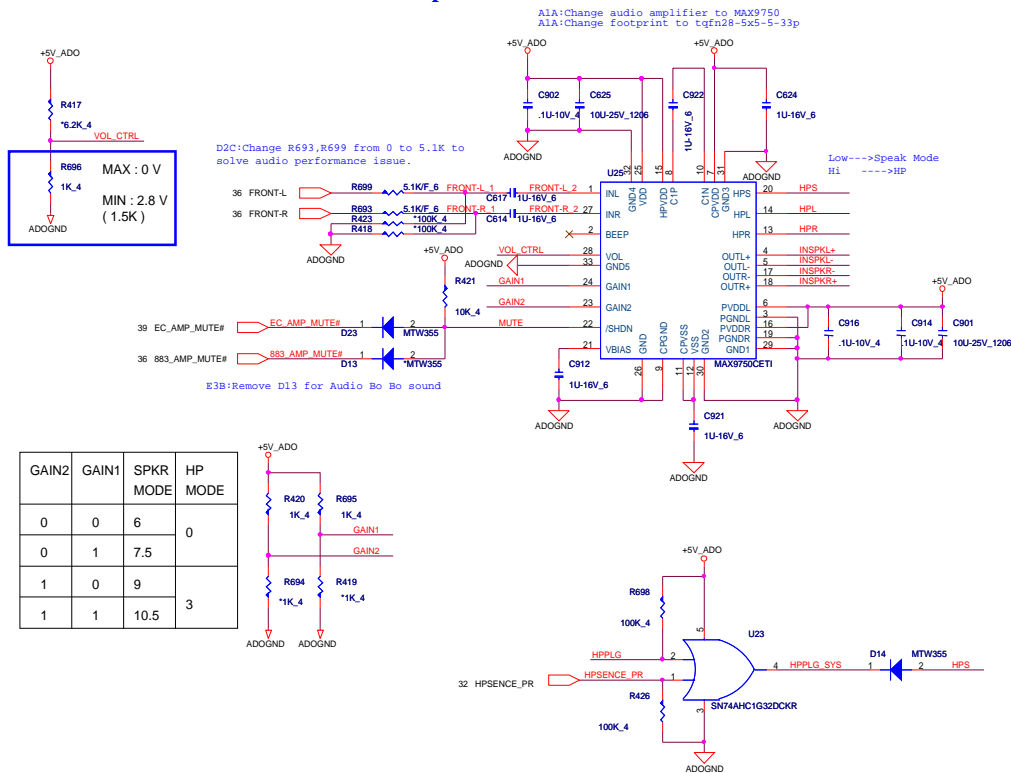


PROJECT : ZC1
Quanta Computer Inc.

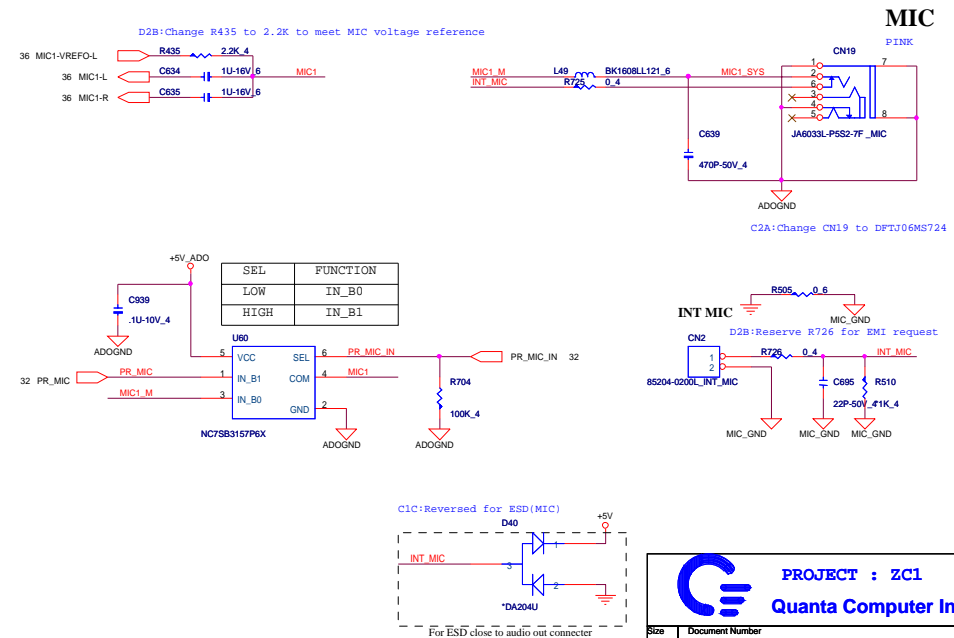
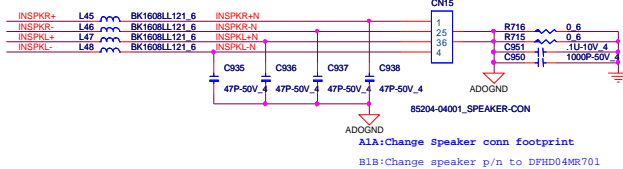
Size	Document Number	Rev
	SATA/PATA	A
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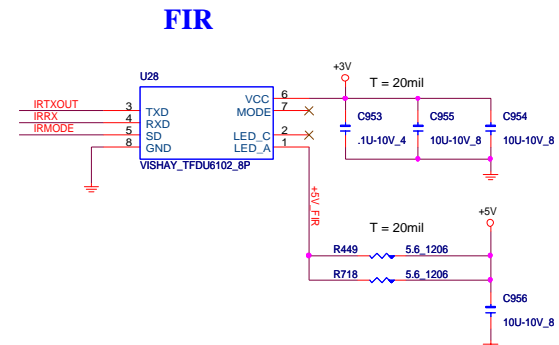
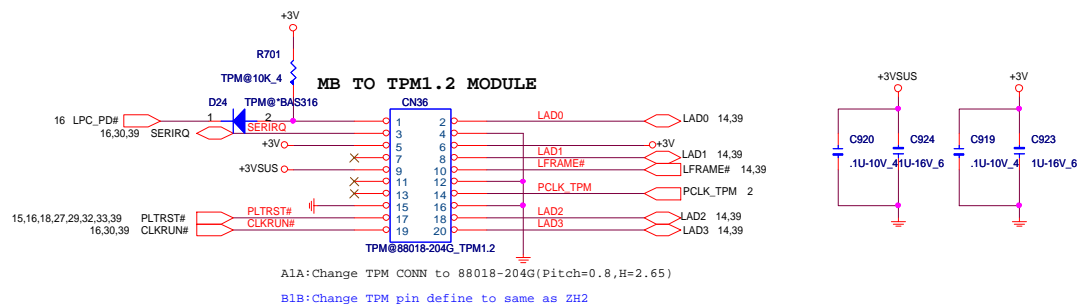
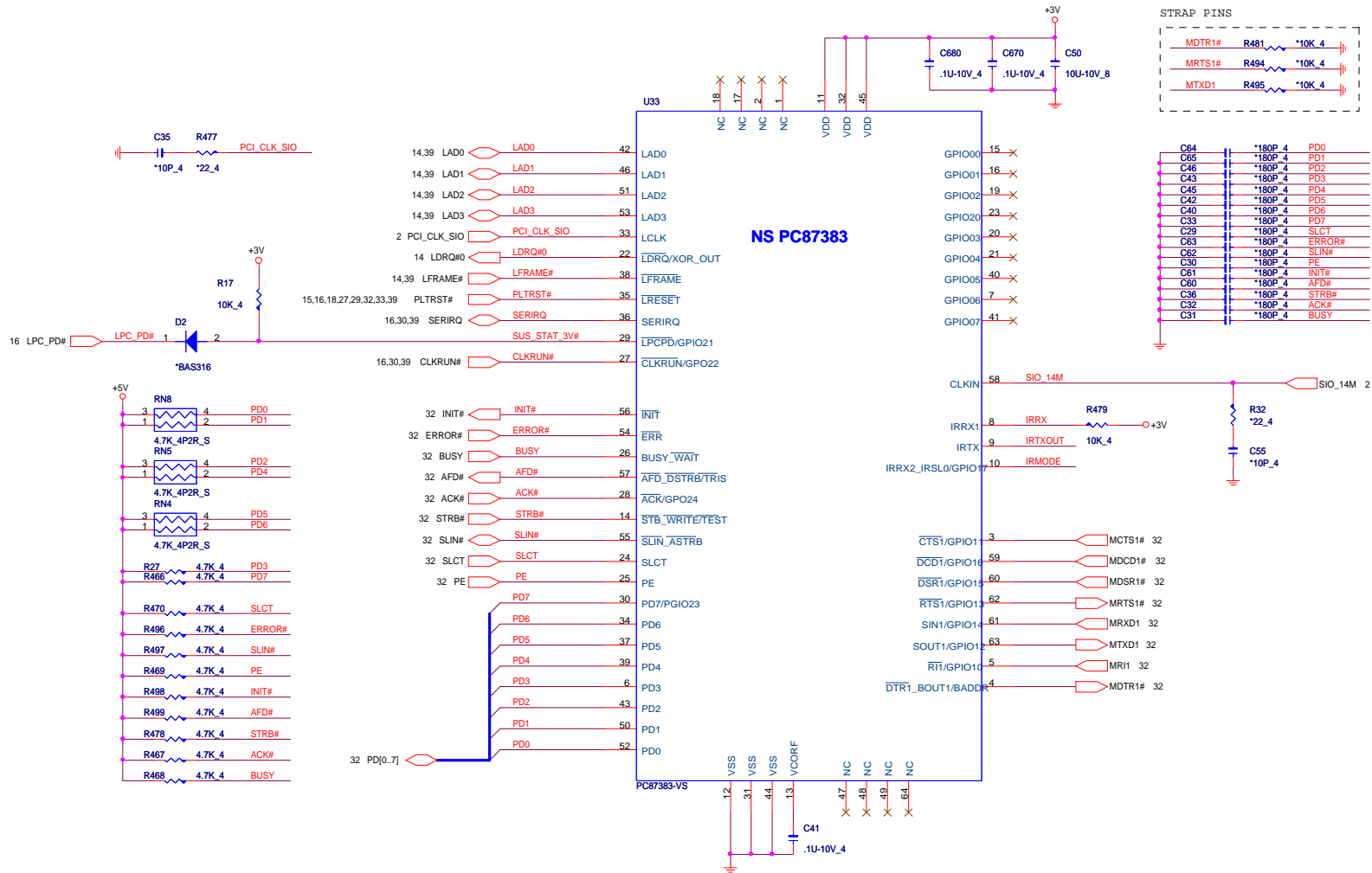


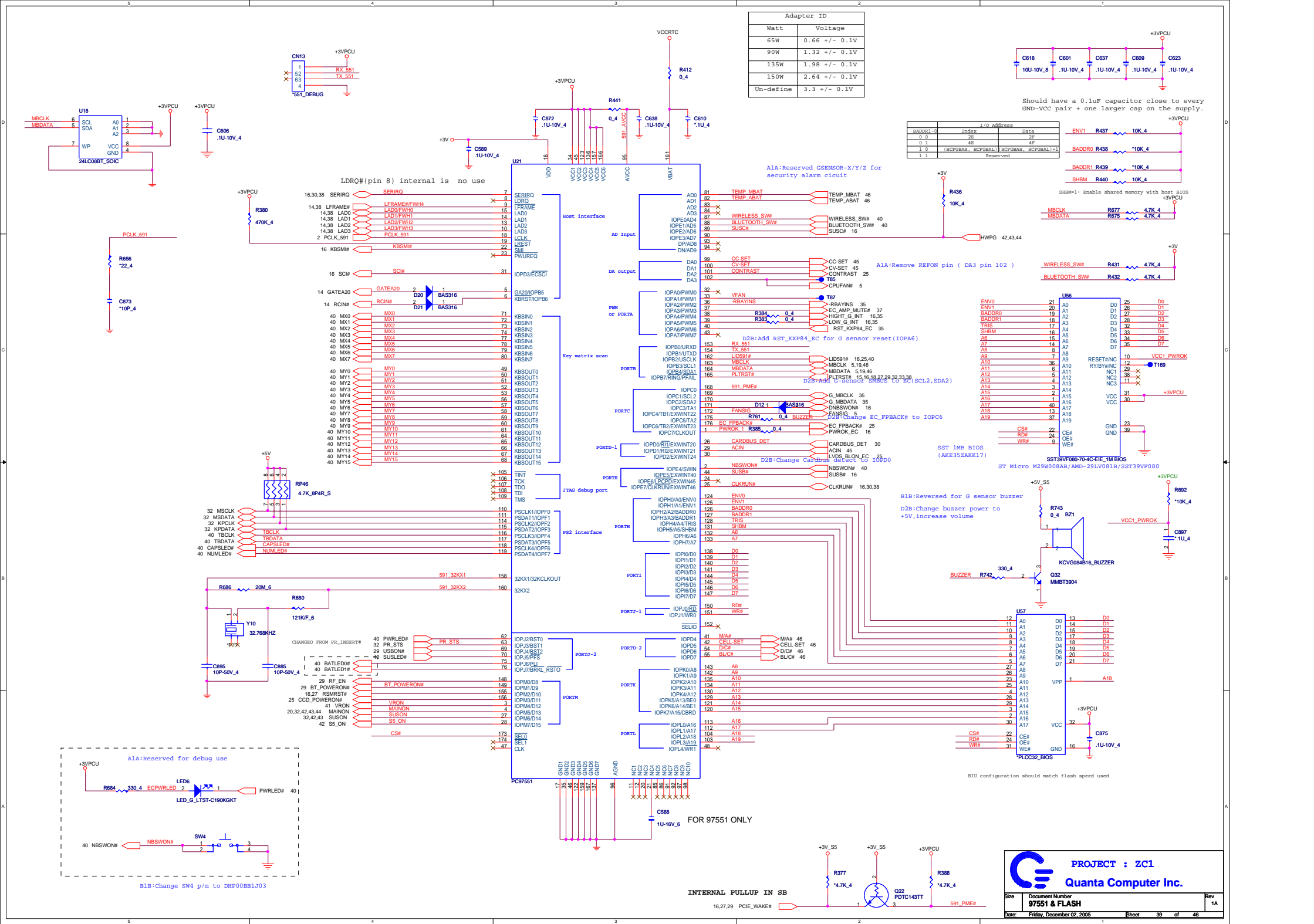
Audio amplifier

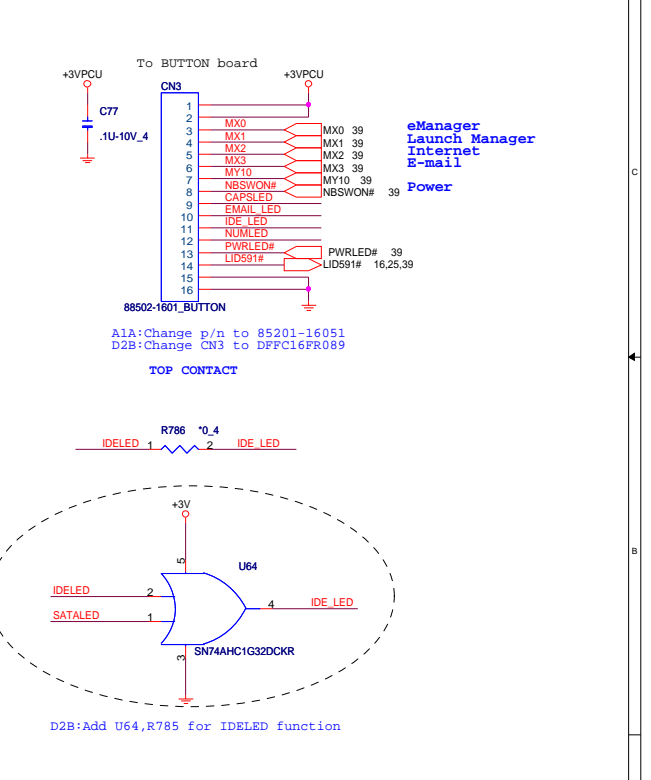
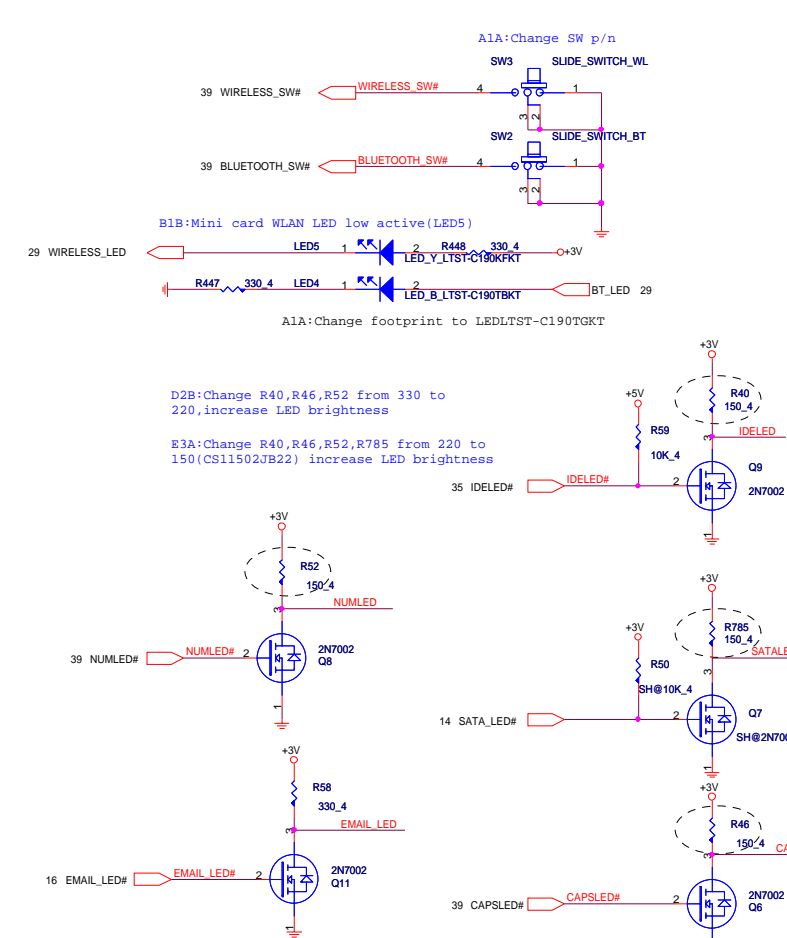
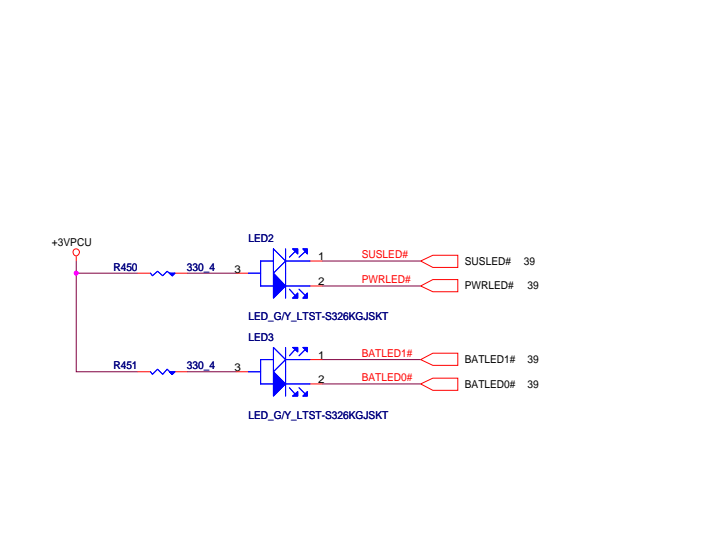
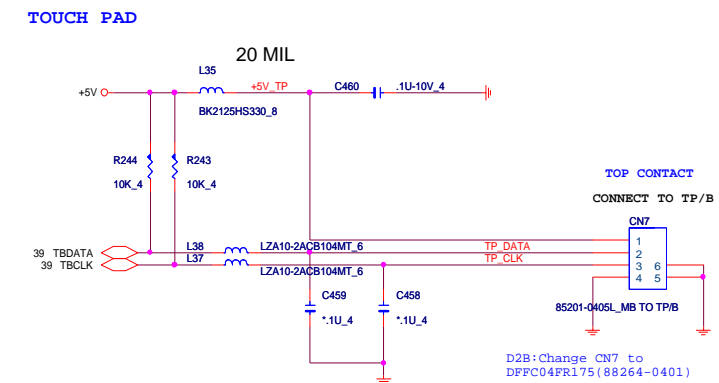
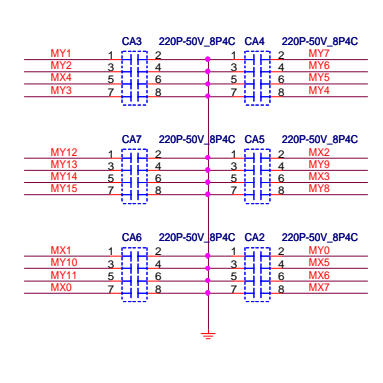
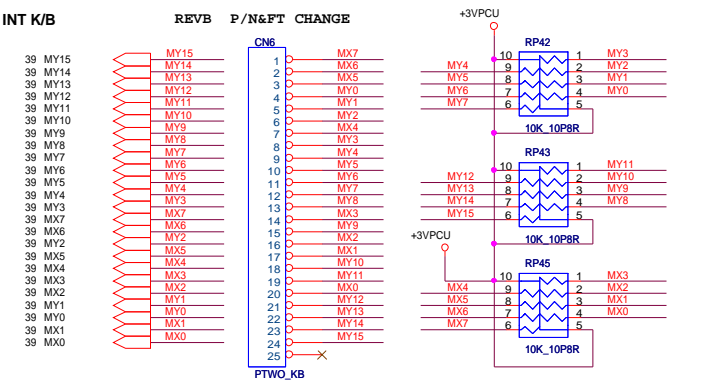


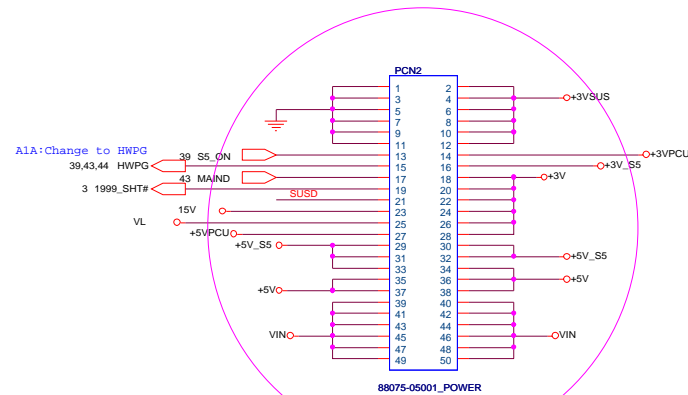
SPEAKER CONNECTOR





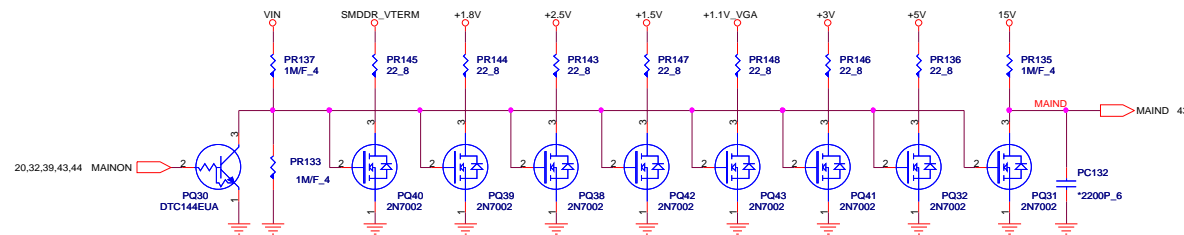
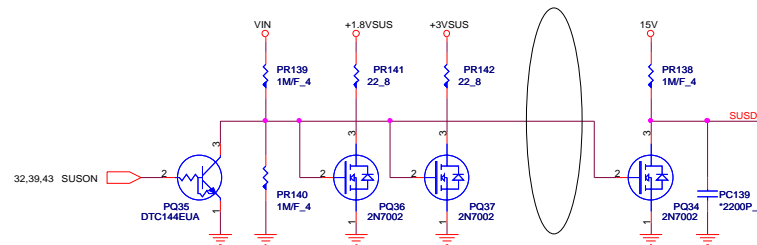






8/2 UPDATE CONN PIN DEFINE

A1A:Del +5VSUS discharge



PROJECT : ZC1
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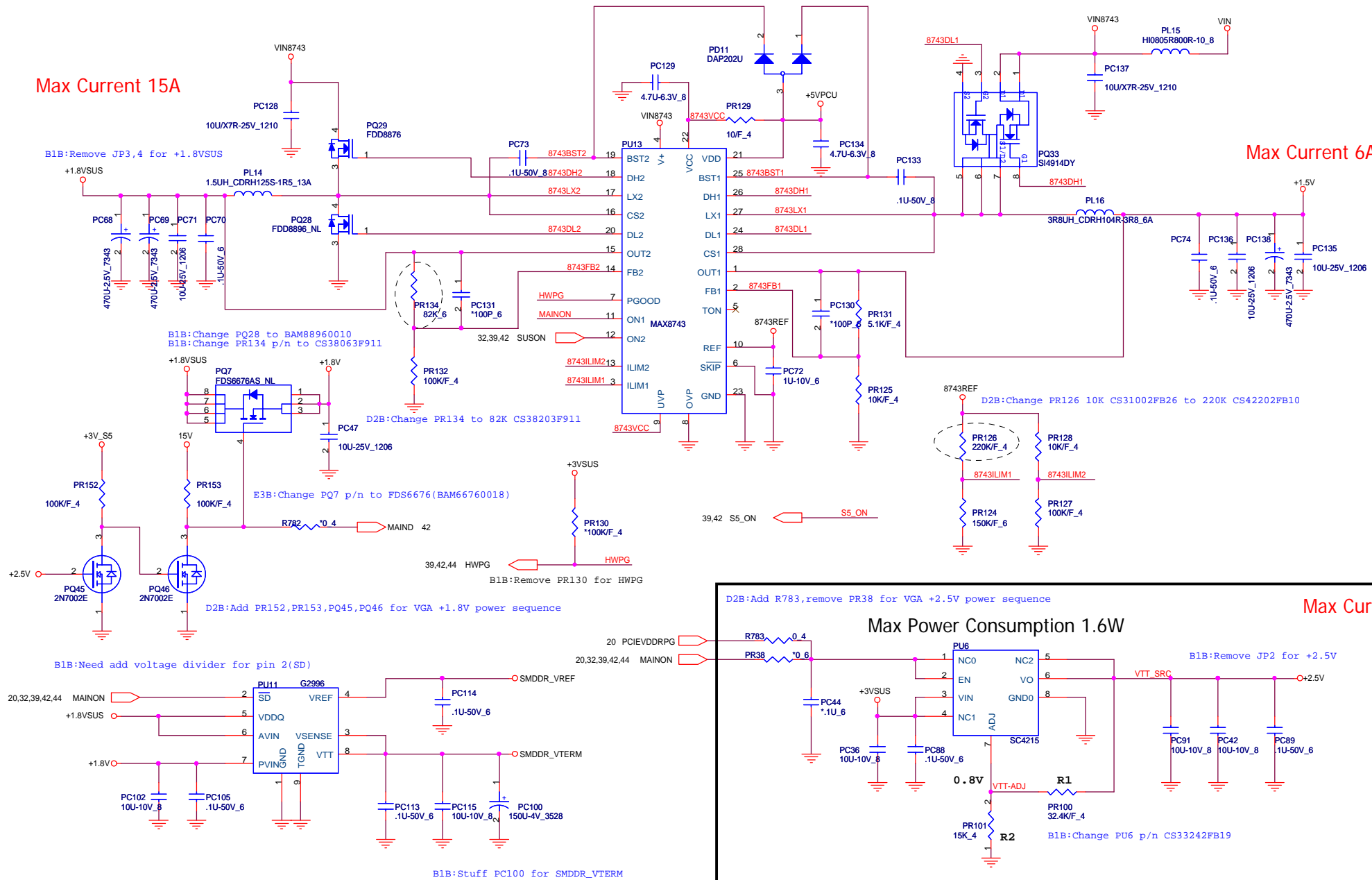
Size	Document Number	Rev
	DISCHARGE/CONNECTOR	1A
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Max Current 15A

Max Current 6A

Max Power Consumption 1.6W

Max Current 2A



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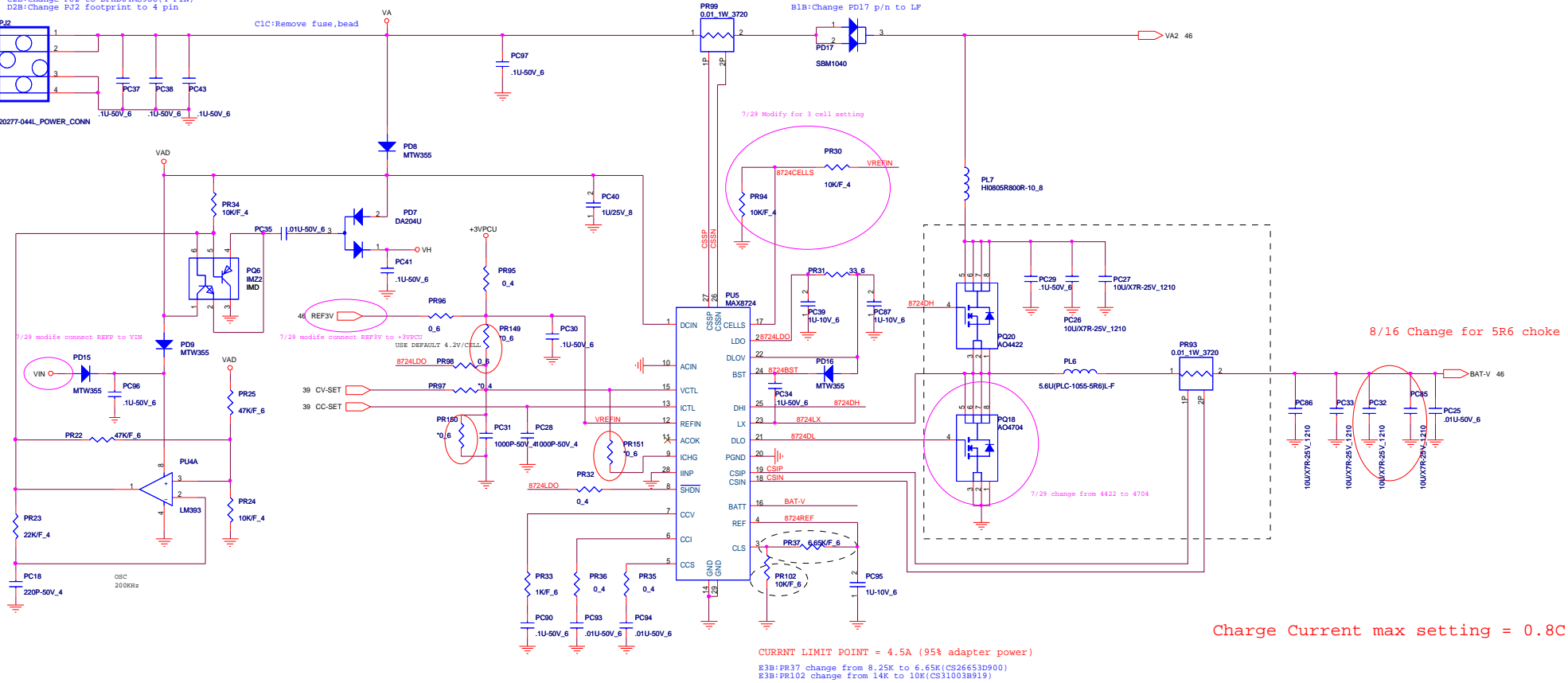
ALA:Change footprint to 20277-05XX-5P-L

C2B:Change FJ2 to DFHD04MS988(4 PIN)

C2B:Change FJ2 footprint to 4 pin

C1C:Remove fuse,bead

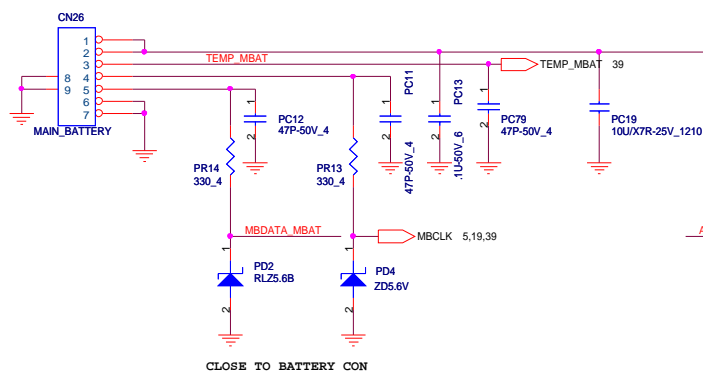
B1B:Change PD17 p/n to LF



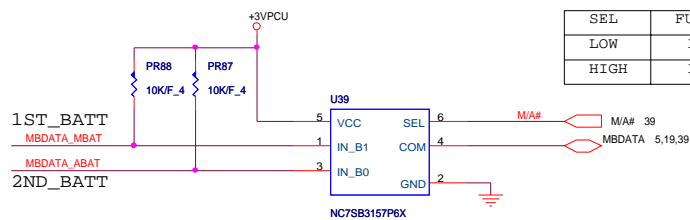
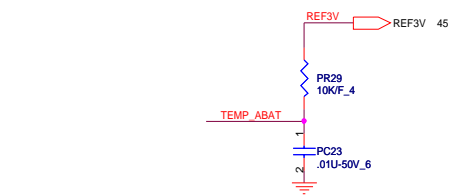
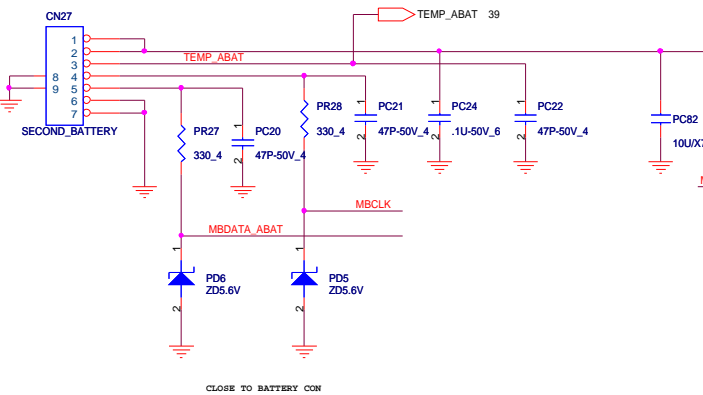
PROJECT : ZC1
Quanta Computer Inc.

A1A:Change p/n to DFHD07MR391
B1B:Change CN26 footprint to 20175A-07G1-7P-R

1ST_BATT_CONN



2ND_BATT_CONN



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

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	BATTERY SELECT	A
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