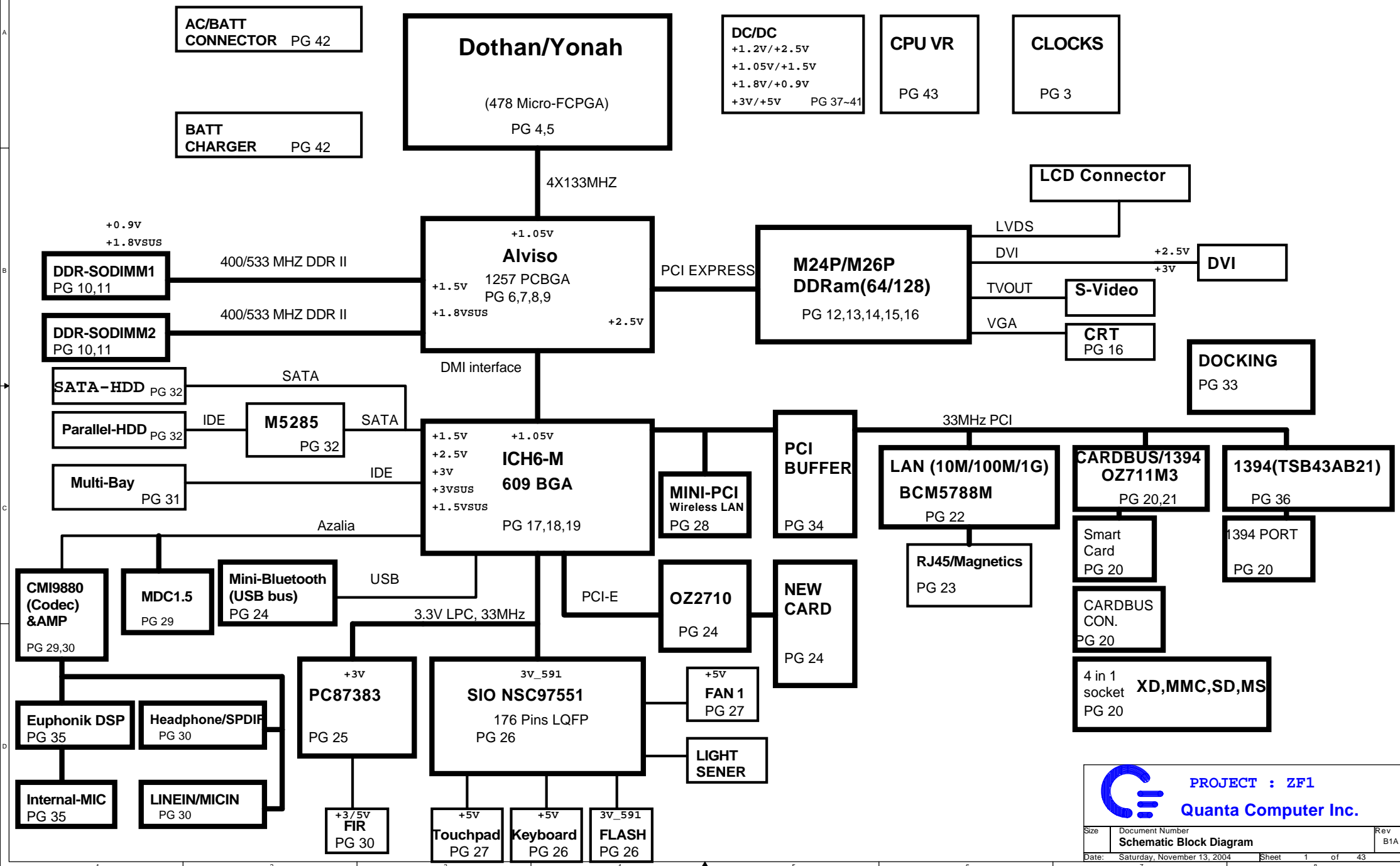


ZF1



Check again

Change History

Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT	X	X	X	X	
3V_591	X	X	X	X	
5VPCU	X	X	X	X	
+3V_S5	X	X	X	X	S5_ON
3V_LAN	X	X	X	X	
+1.5V_S5	X	X	X	X	S5_ON
+1.8VSUS	X	X			SUS_ON
+3VSUS	X	X			SUS_D
+5VSUS	X	X			SUS_D
SMDDR_VTERM DDR Termination voltage	X	X			MAIN_ON
SMDDR_VREF	X				MAIN_ON
VGA_PCIE_1.2V	X				MAIN_ON
VCC_CORE Core voltage for Processor	X				VR_ON
+VCCP 1.05V rail for Processor I/O	X				MAIN_ON
+1.5V	X				MAIN_ON
+1.8V	X				MAIN_D
+2.5V	X				MAIN_D
+3V	X				MAIN_D
+5V					MAIN_D
+12V	X				MAIN_ON
+3VRUN	X				PCI_Switch_Power_ON
+5VRUN	X				PCI_Switch_Power_ON

5/28

- System DVI DET function move in EZ port , So Del Q47,R557
- Addition AND gate for DOCKING Power Good AND DockingIN Singal combine Circuit
- Addition Power led circuit for system
- Change D34 AND D35 + -
- Addition LID Switch and LID connector
- Addition RC Delay for PCIE1.2V
- Change EC Three GPIO port same to ZL2
- 5/31
- 1.Change C145 PCB Footprint to 3528
- 2.Combine USB and bluetooth connector to 19pin connector 87212-1900
- 3.Change PCBFootprint 88216-1200 to 88213-1200
- 4.Change USB connector bypass C to 0805 10u
- 5.Adujst 80pin connector 3 singal
- 6/1
- 1.Update power all circuit for GND name
- 2.Addition OR to PRST
- 3.Change IDE RST
- 6/2
- 1.Change ICH-6 USB Port
- 2.Del CDR,CDL,CDGND Singal and DEL prevent CDR,CDL,CDGND noise circuit.
- 6/4
- 1.U49,U50, Form 3VRUN change to +3V AND CHANGE MINPCI connector to PCI BUS,And addition PCI_SWRST # AND PCI_SWRST1#
- 2.Change BT_POWER NAME
- 3.Change VOIP AGND
- 6/7
- 1.Change VOIP AGND TO AGND2 for Layout

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus+Smart Card	AD25	1	PIRQC/B
Mini-PCI	AD19	2	PIRQB/D
LAN	AD22	0	PIRQA
1394	AD23	3	PIRQD

EC SM Bus1 address


Device

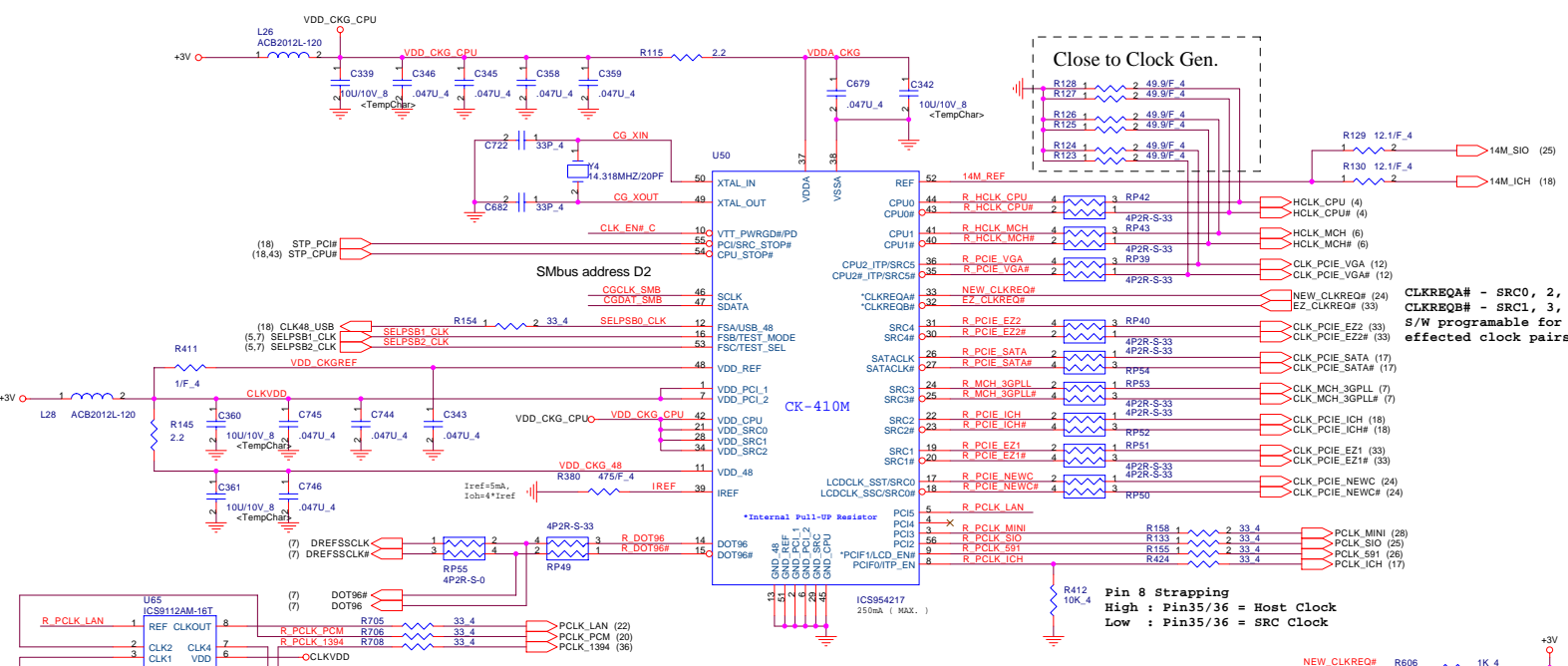
Smart Battery
THERMAL SENSOR
LIGHT SENER
VOIP FLASH ROM

ICH6-M SM Bus address

Device

SODIMM 1010 000X b
Clock Gen 1101 001x b

		PROJECT : ZF1	
		Quanta Computer Inc.	
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Resistor Stuff Table

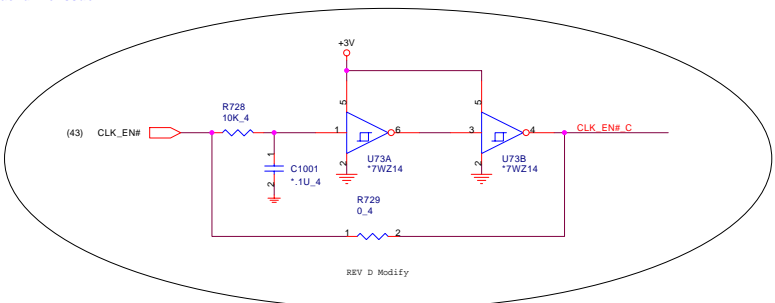
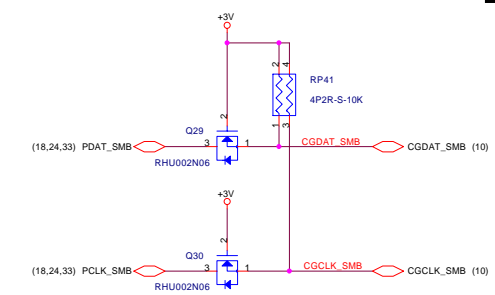
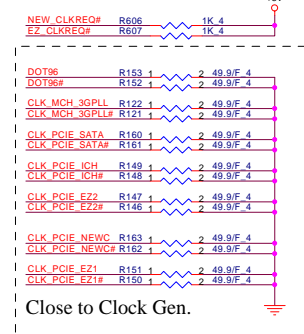
	RA	RB	RC	RD
Dothan A 400	V	X	X	V
Dothan A 533	X	V	X	V
Dothan B	X	X	X	X

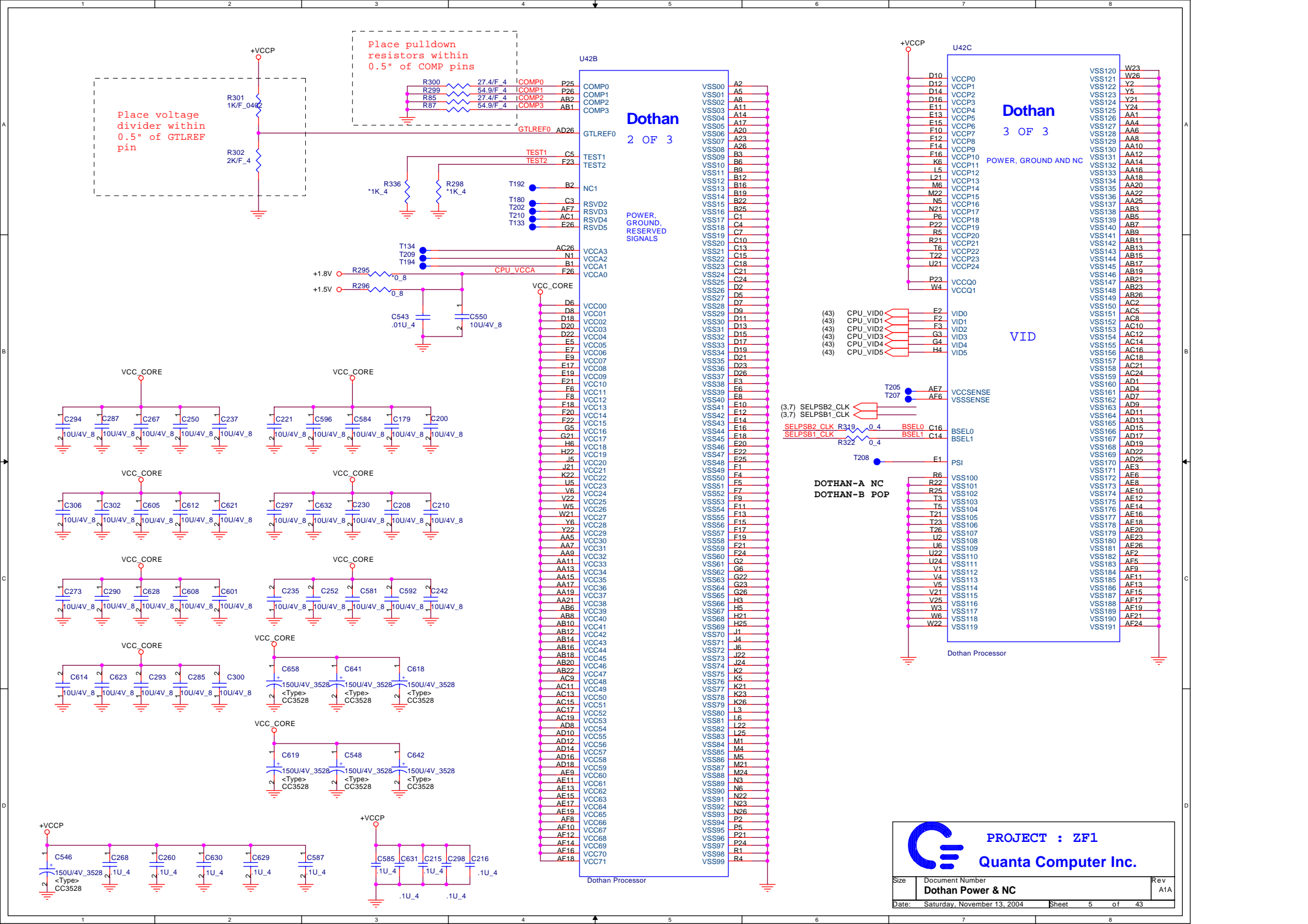
Clock Gen. Frequency Selection Table

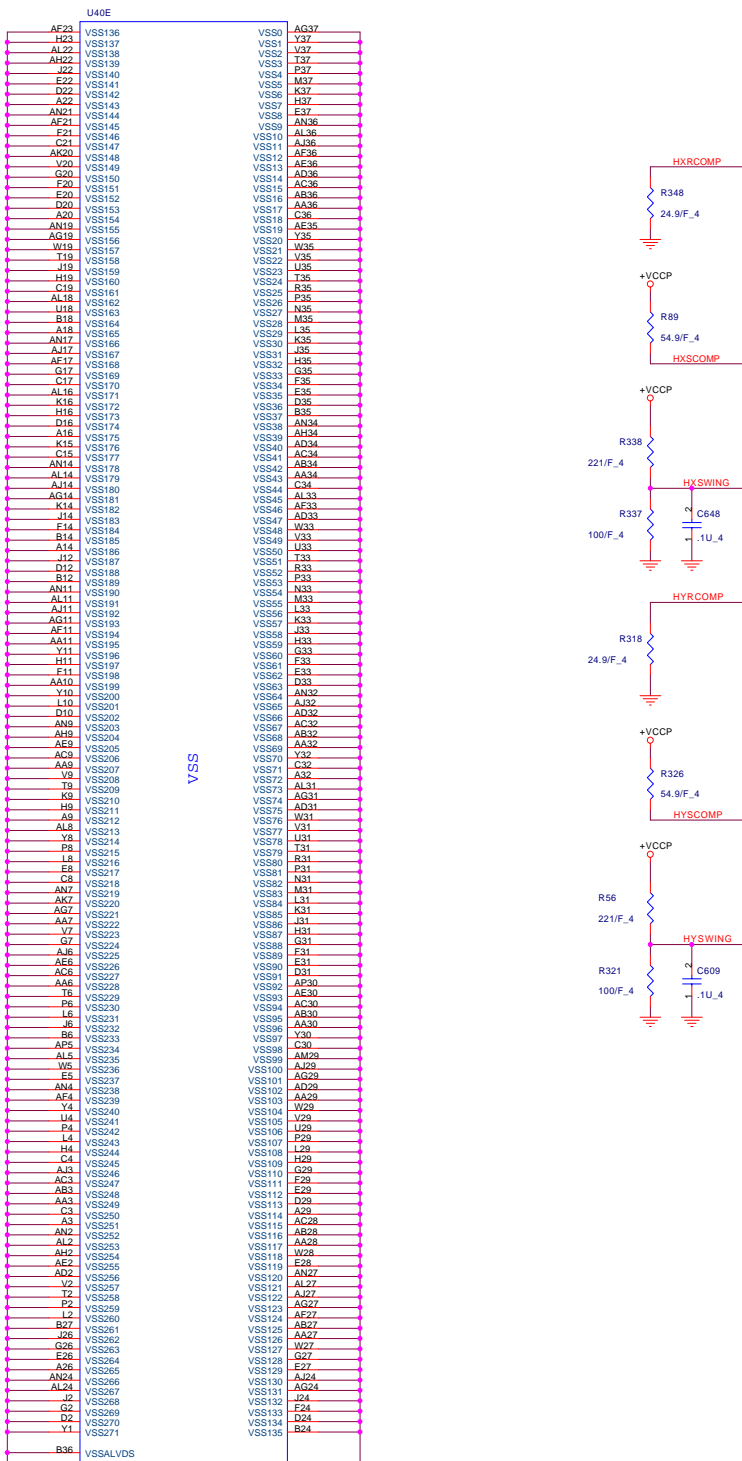
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

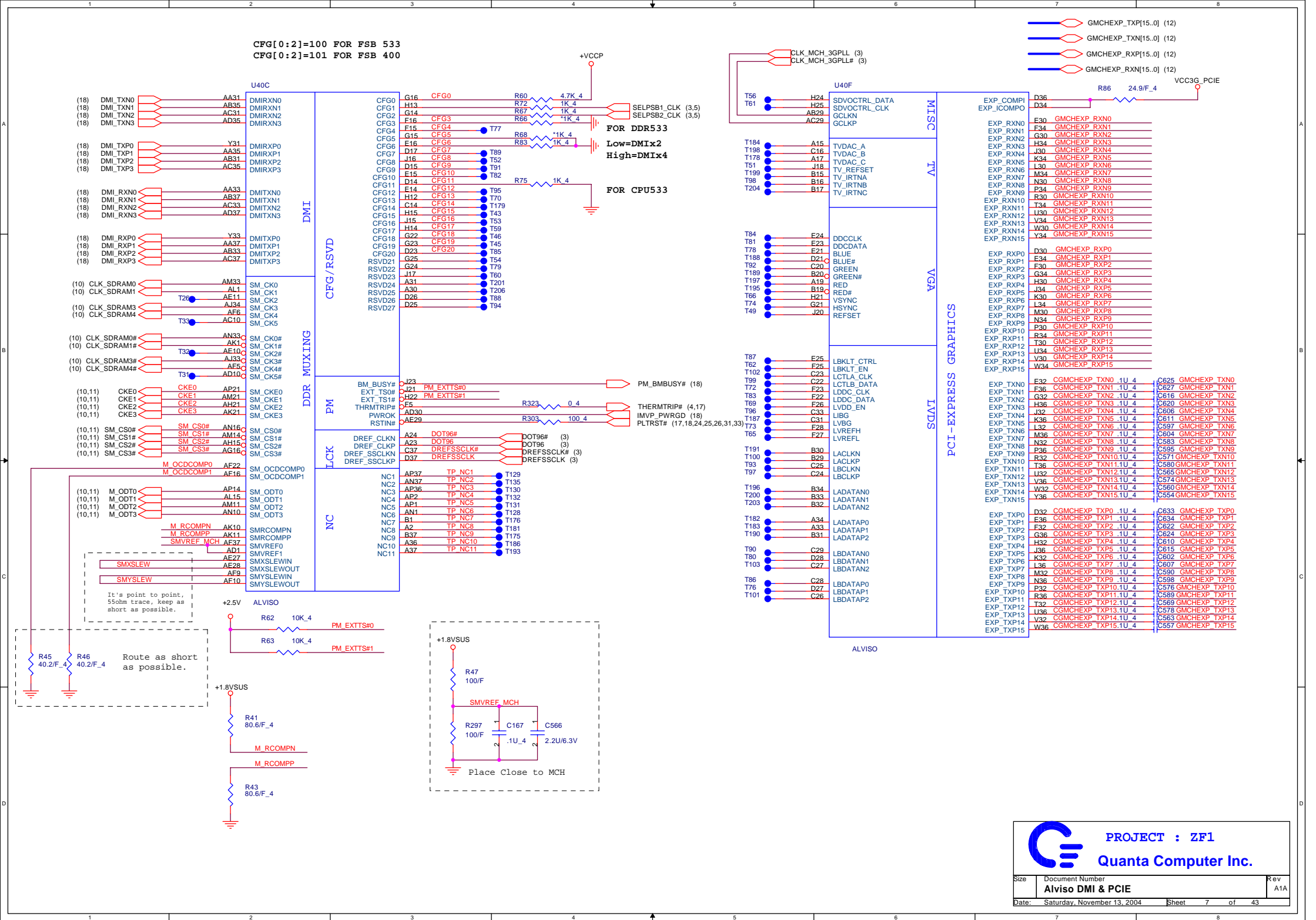
DOTHAN BSEL Output Value

FSB Frequency	DOTHAN A-Step		DOTHAN B-Step	
	BSEL1	BSEL0	BSEL1	BSEL0
400 MHz	0	0	0	1
533 MHz	0	1	0	0

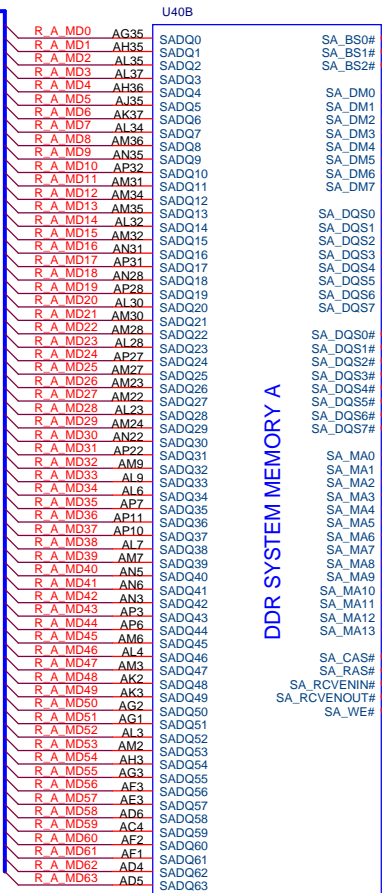








(10) R_A_MD[0..63]



DDR SYSTEM MEMORY A

ALVISO

(10) R_B_MD[0..63]



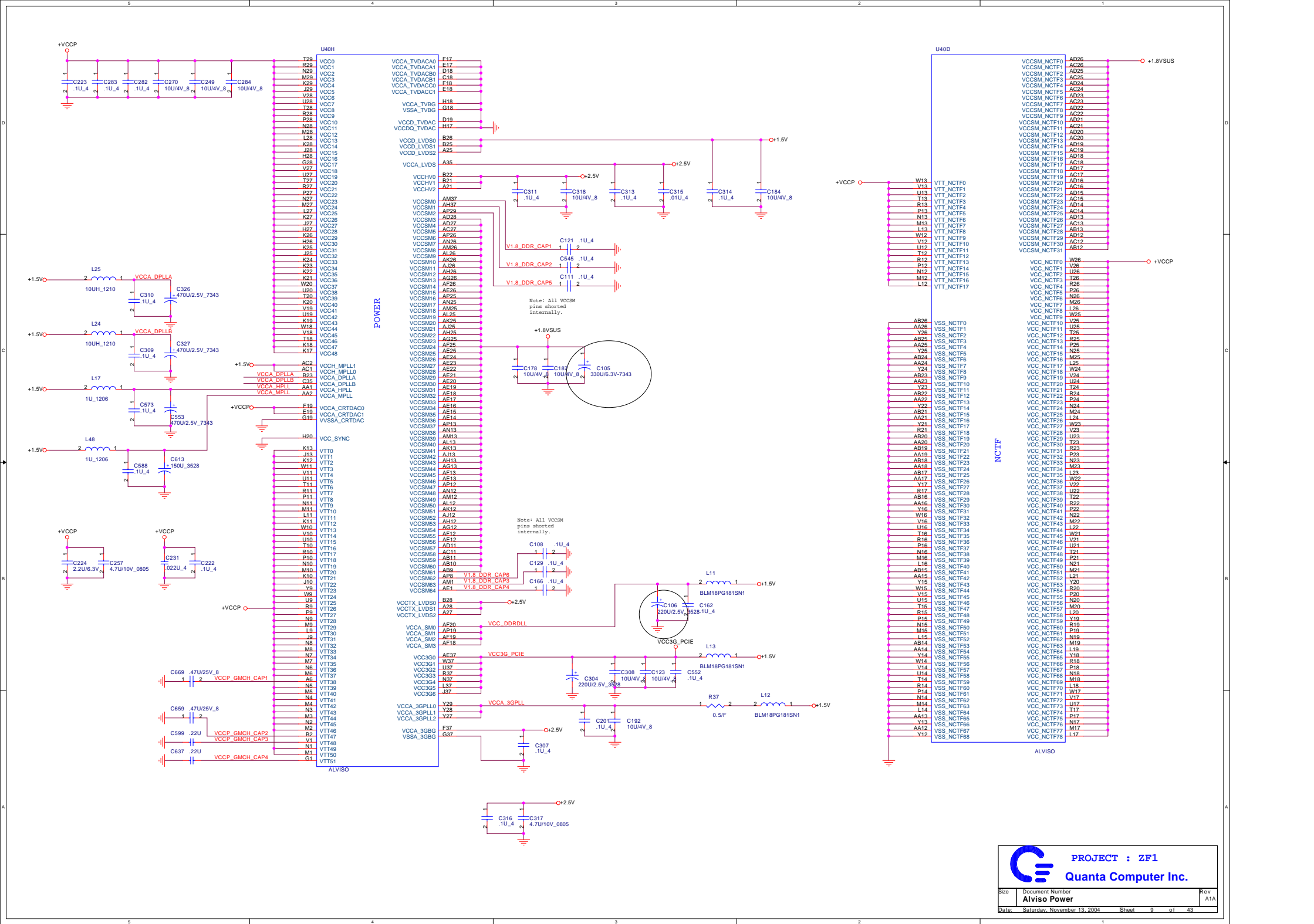
DDR SYSTEM MEMORY B

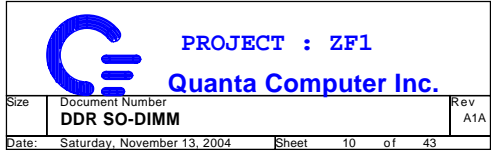
ALVISO

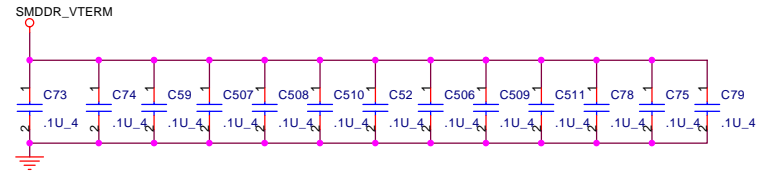


PROJECT : ZF1
Quanta Computer Inc.

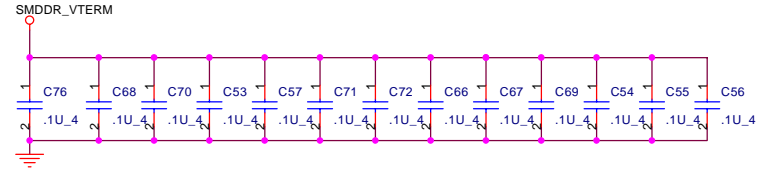
Size	Document Number	Rev
	Alviso DDR	A1A
Date:	Saturday, November 13, 2004	Sheet 8 of 43



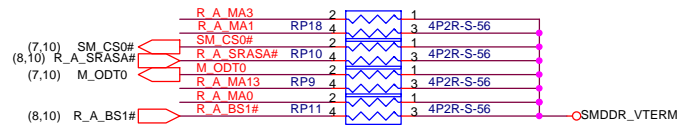
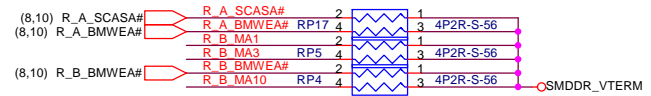
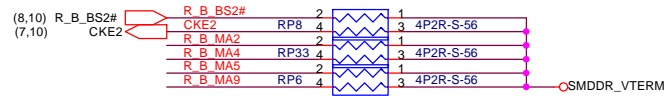
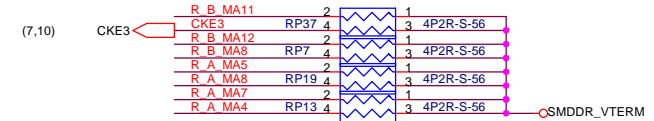
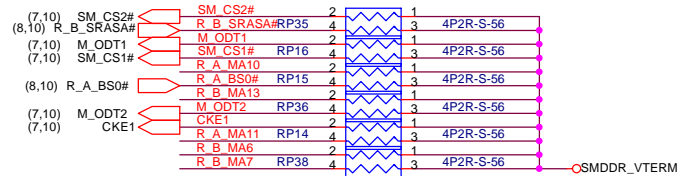
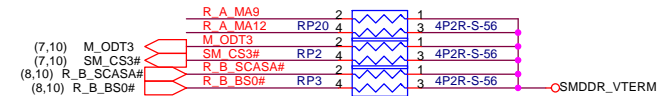
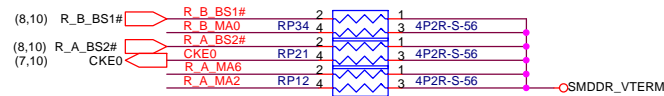





Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

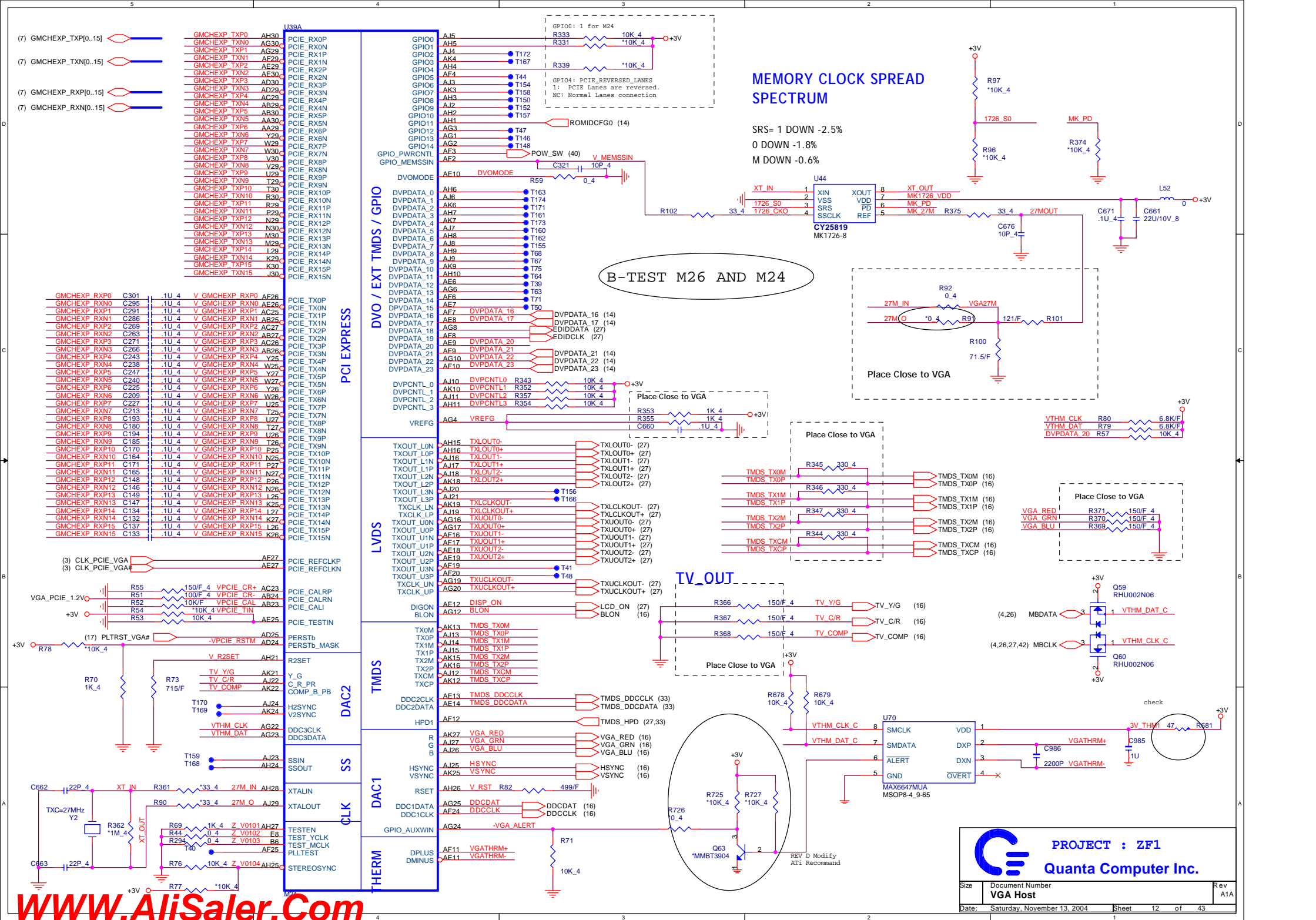


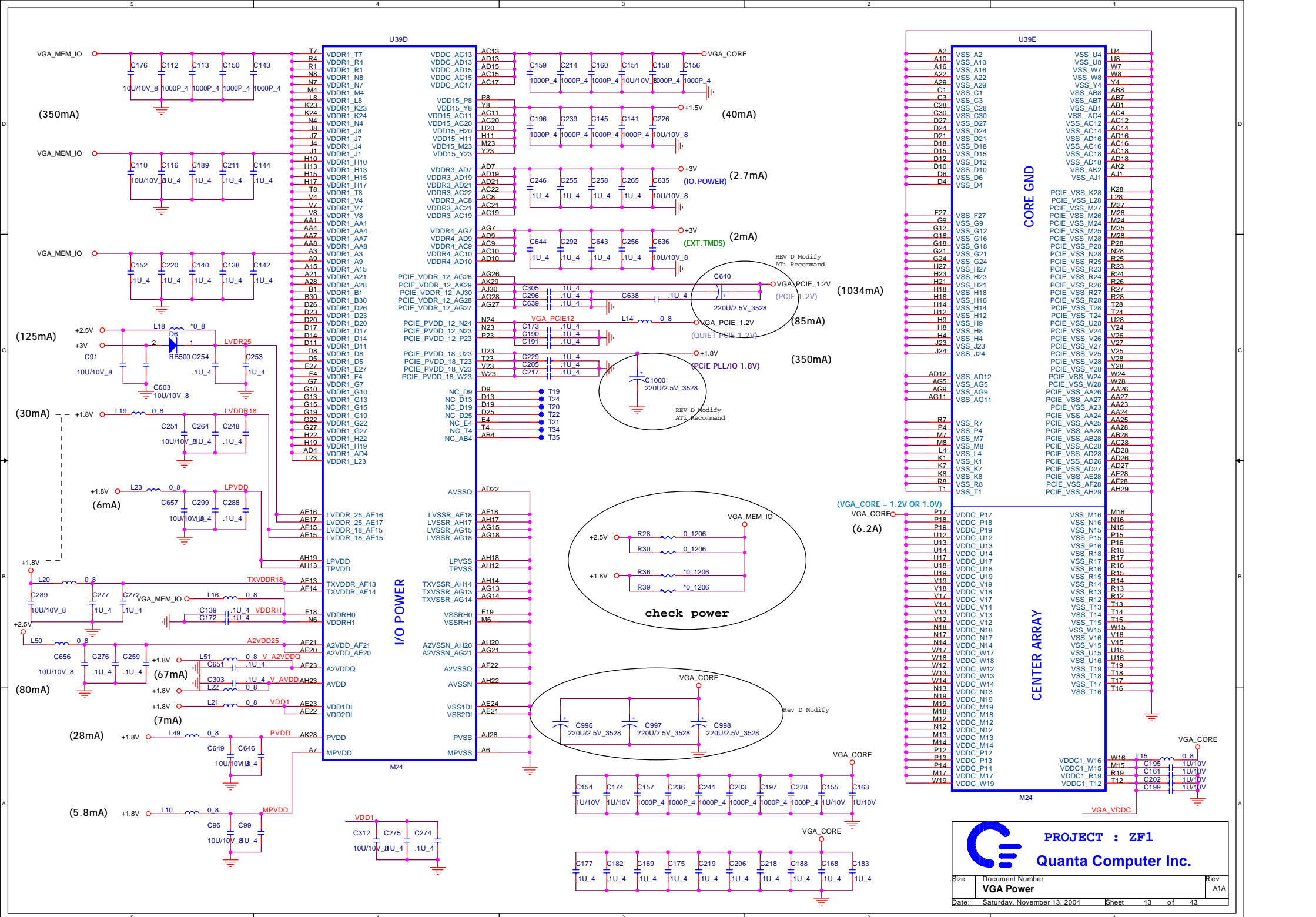


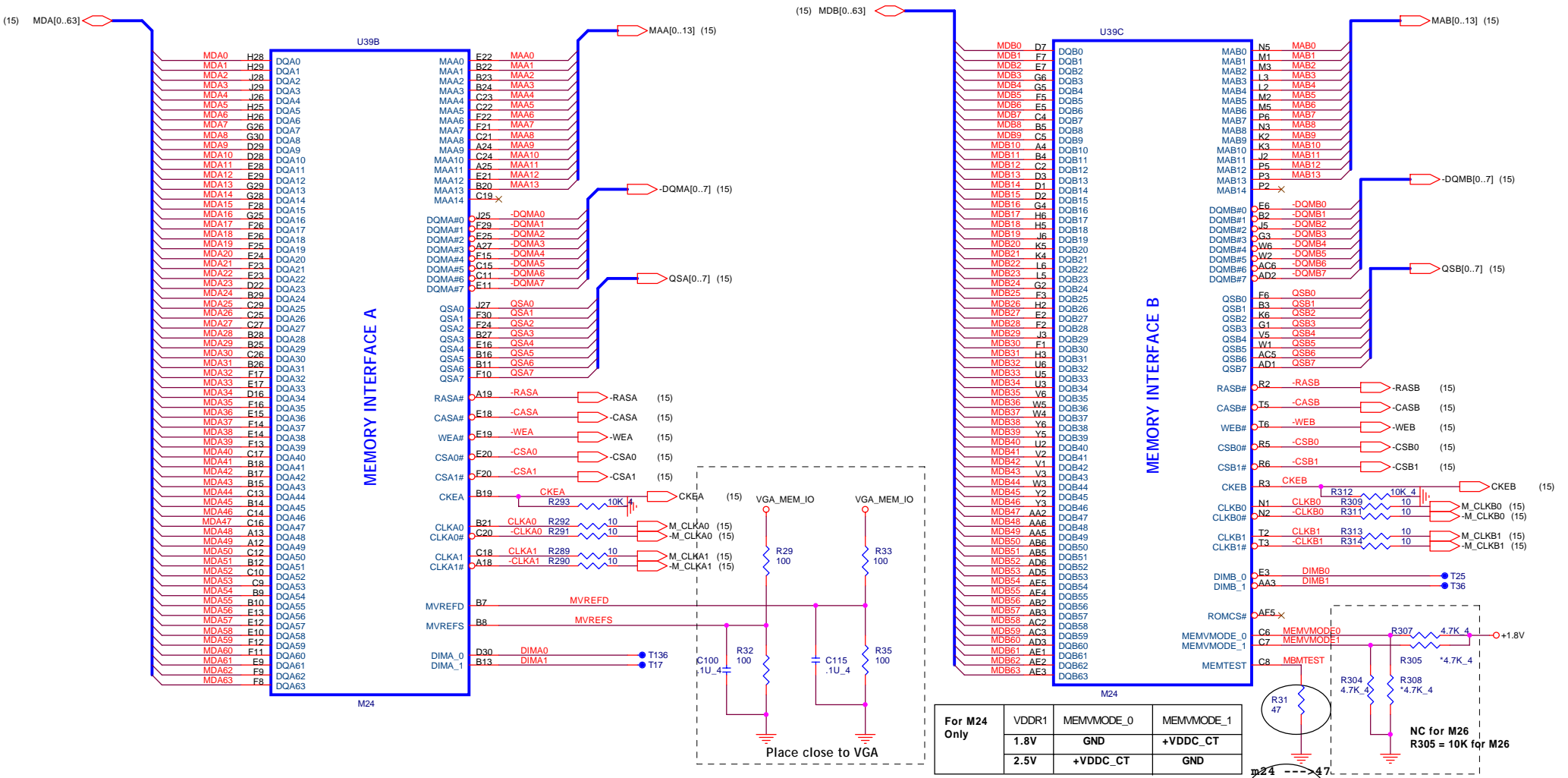
PROJECT : ZF1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR Res. ARRAY	A1A
Date:	Saturday, November 13, 2004	Sheet 11 of 43

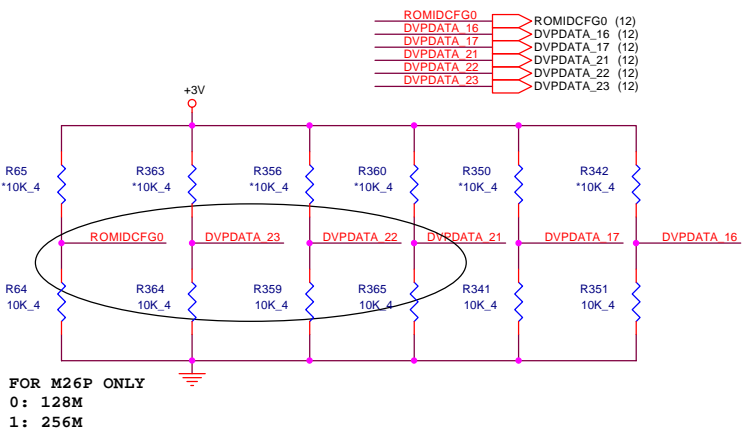






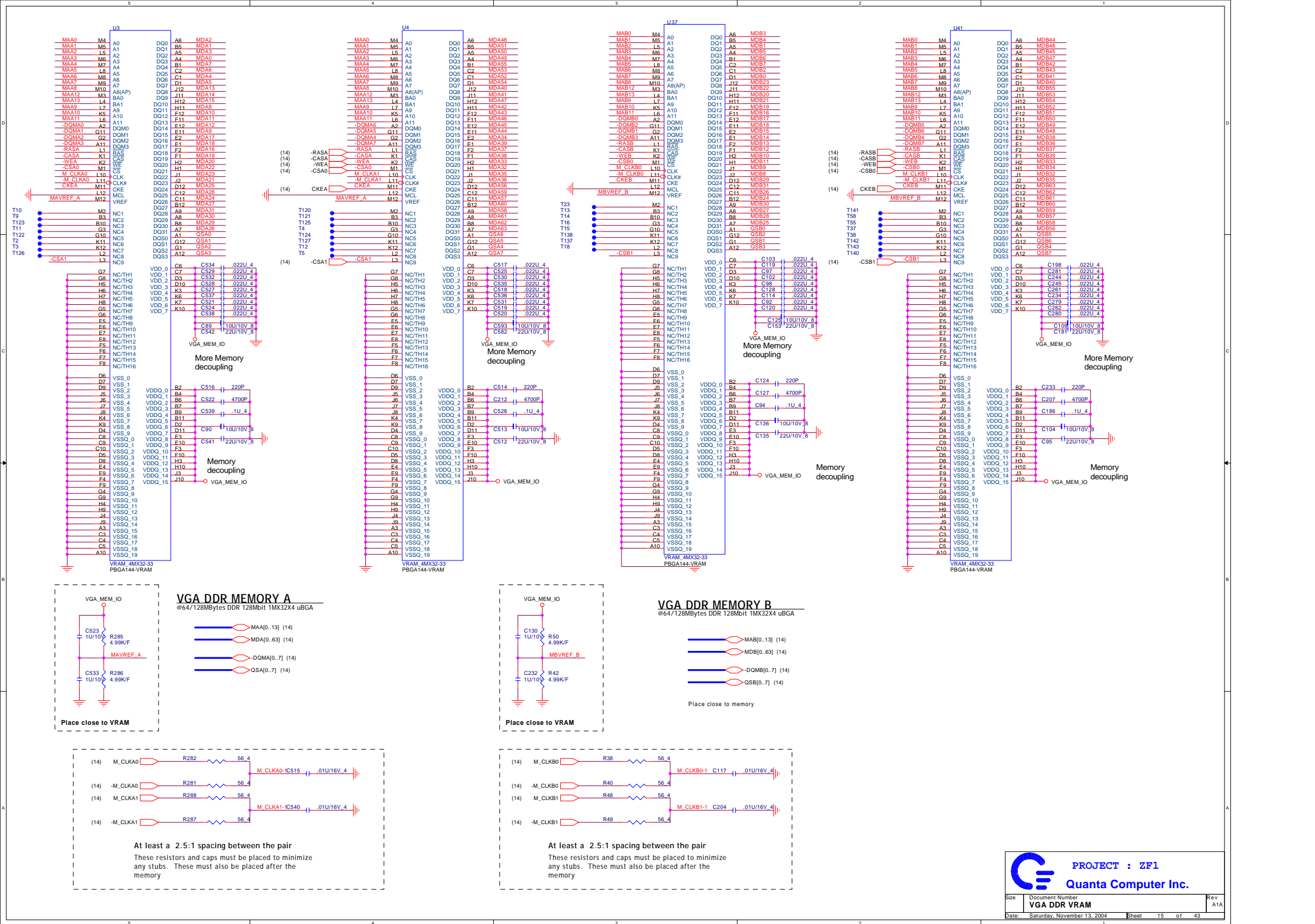
STRAPS PIN

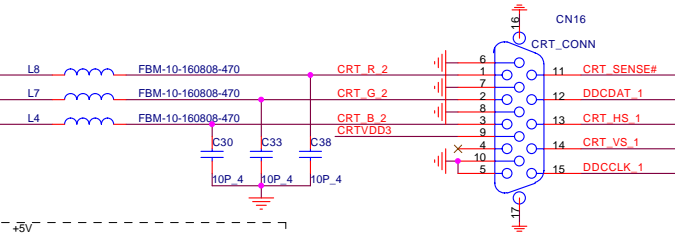
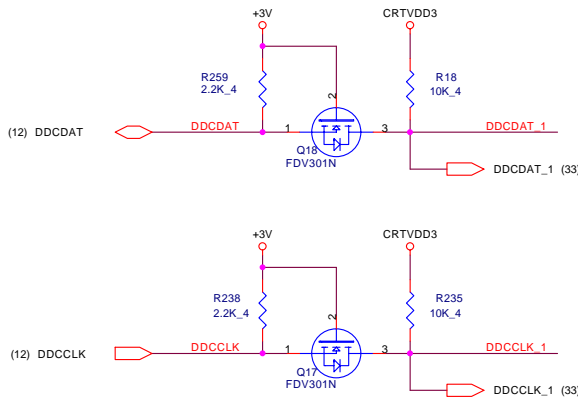
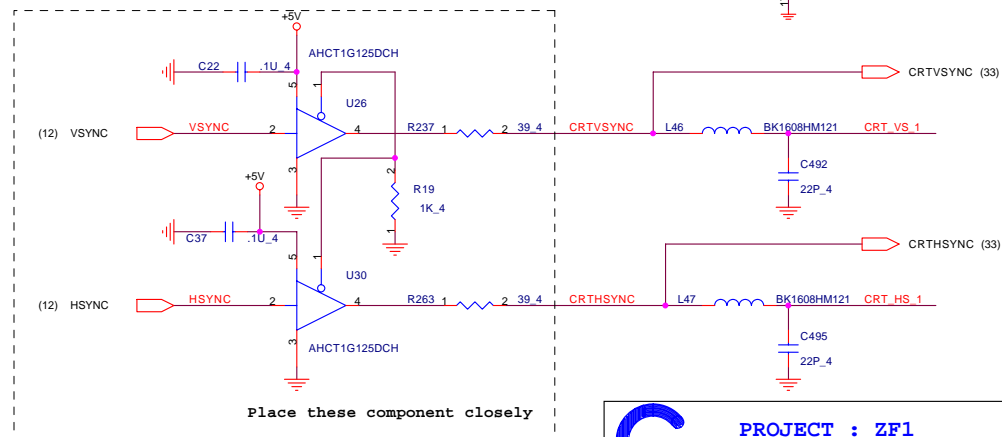
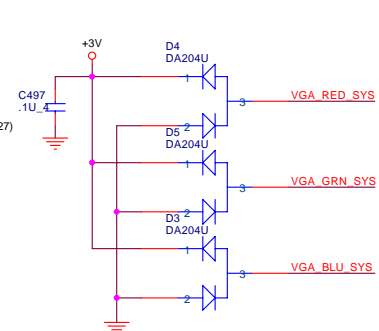
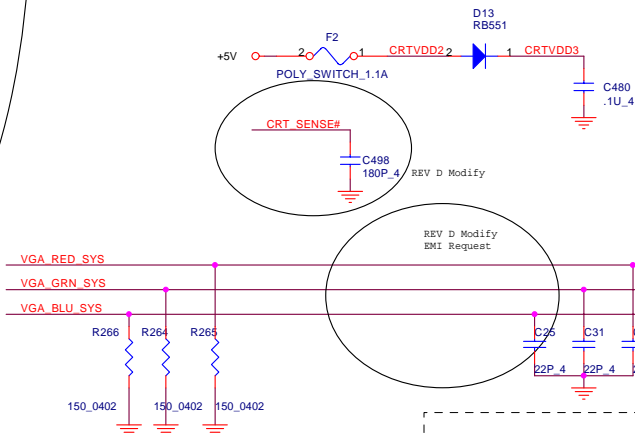
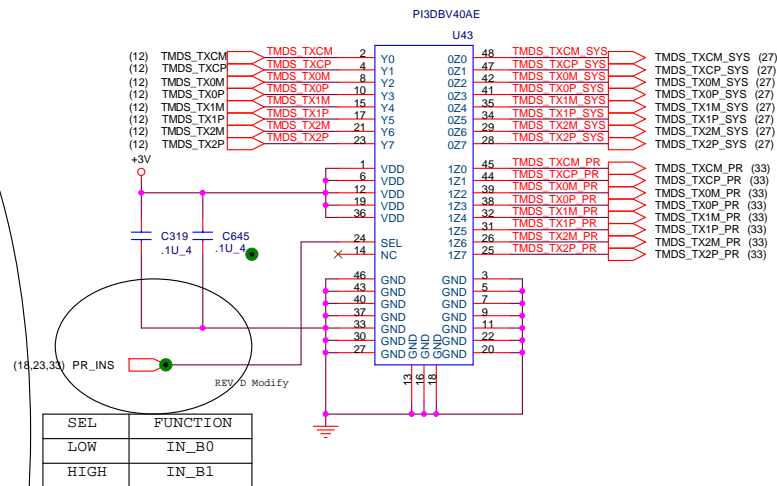
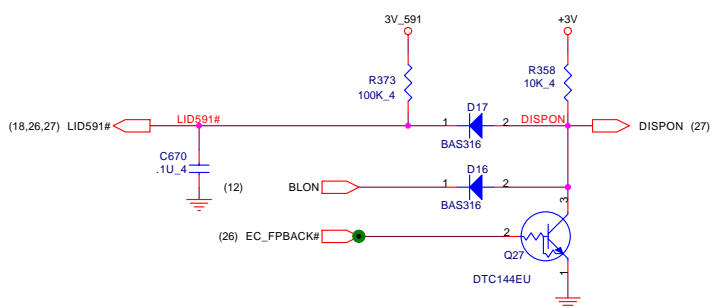
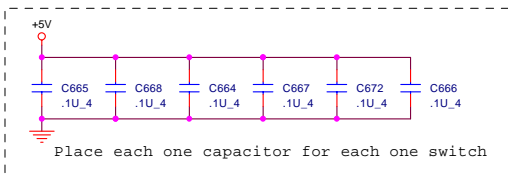
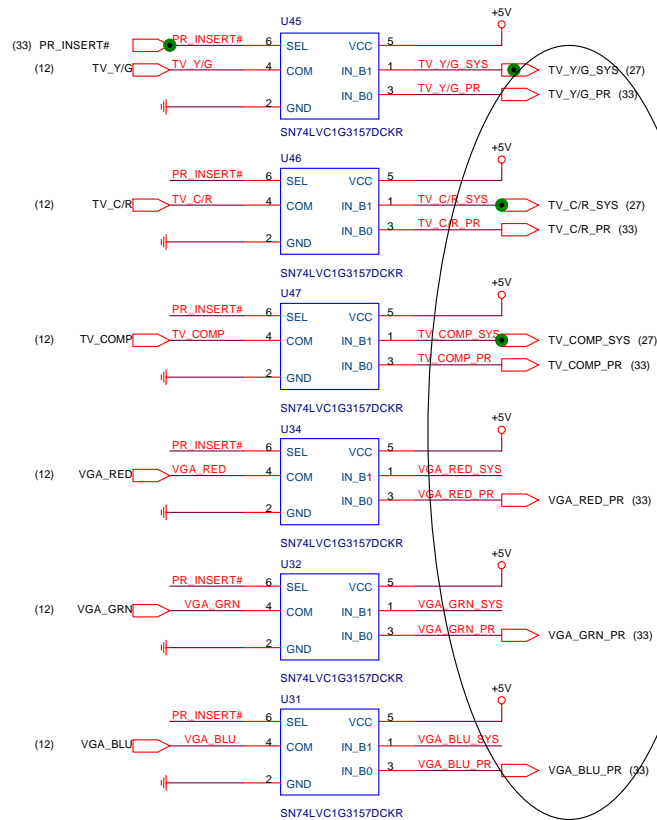
GPIO(9,13:11) INT P/D	ROMIDCFG
	0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung

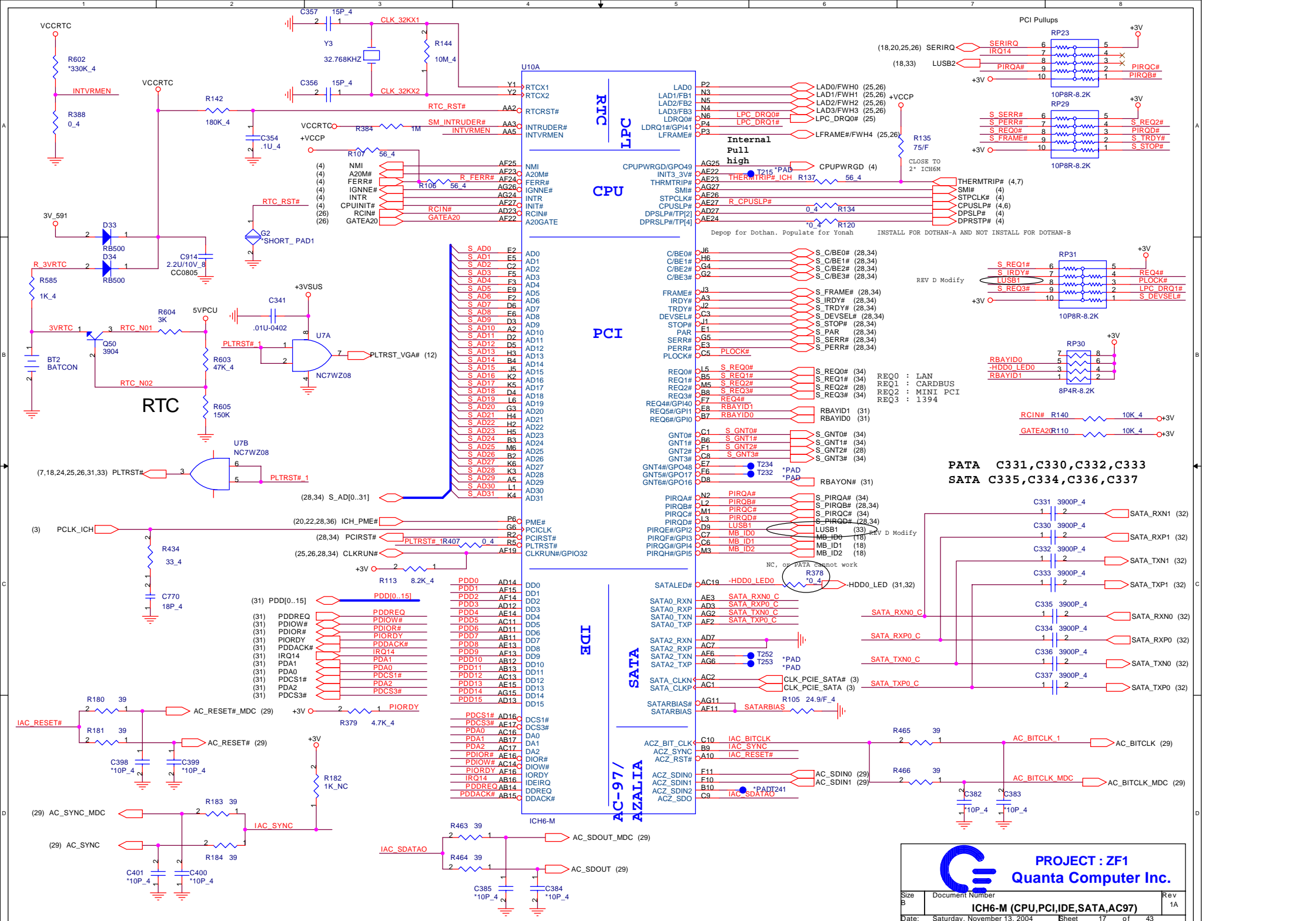


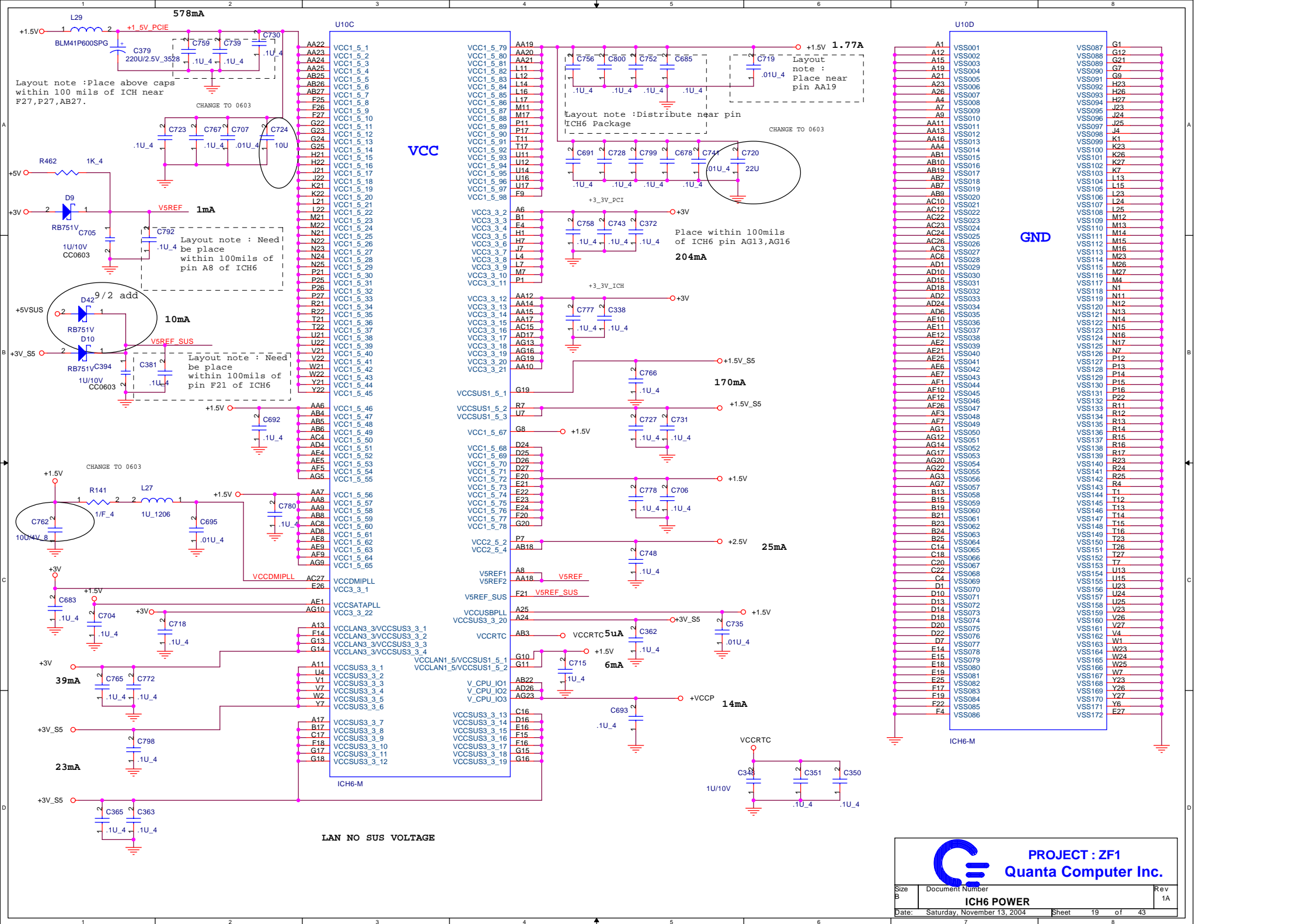
PROJECT : ZF1
Quanta Computer Inc.

Size	Document Number	Rev
	VGA MEM & Strapping	A1A
Date:	Saturday, November 13, 2004	Sheet 14 of 43

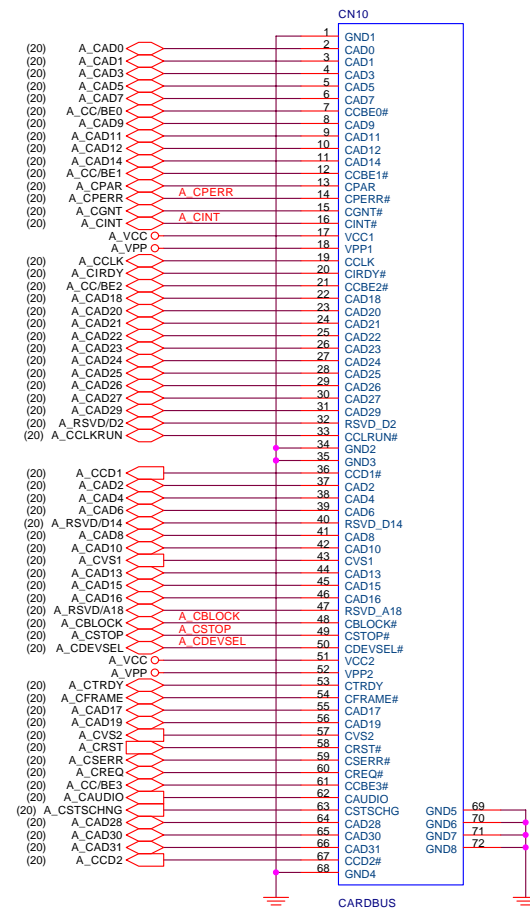








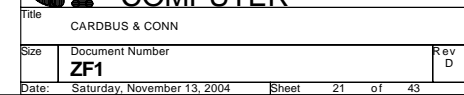
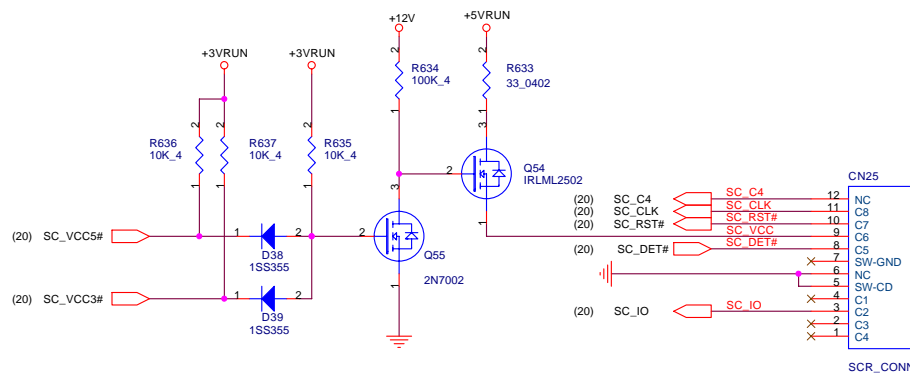


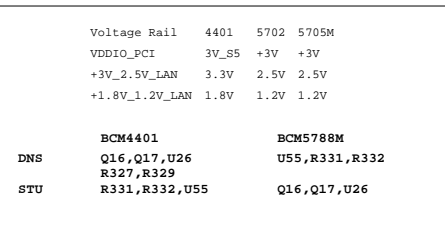
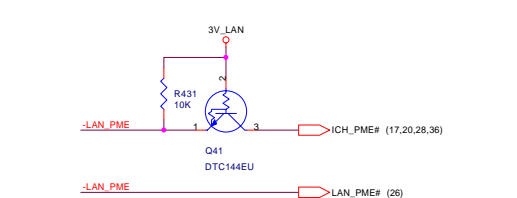


(XD, MMC/SD, MS)

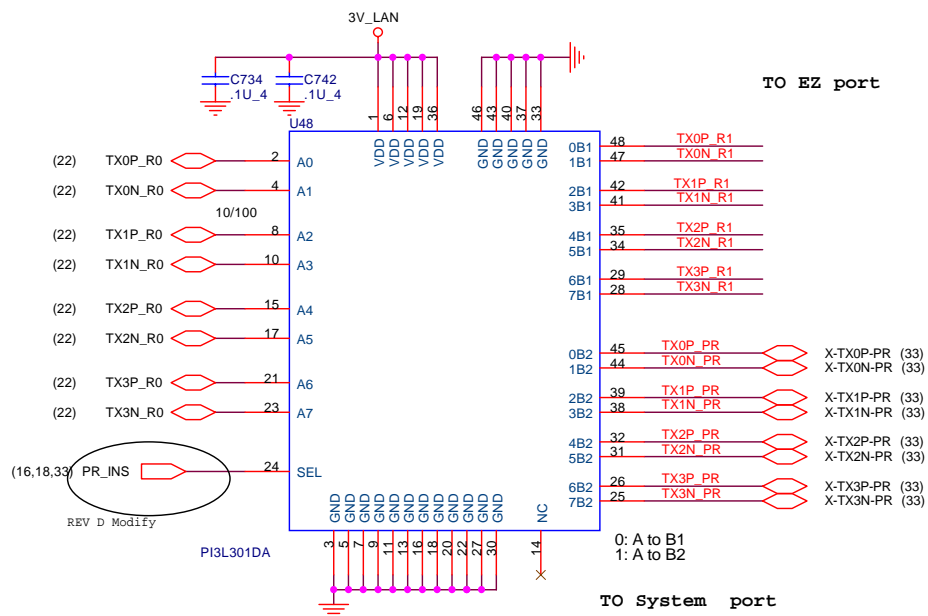
Pin	Connector Function	Board Function
1	SD-1(CD/DAT3)	SD_D3
2	SD-2(CMD)	SD_CMD
3	SD-3(VSS)	
4	SD-4(VCC)	MMC_CLK
5	SD-5(CLK)	SD_D0
6	SD-6(VSS)	SD_D1
7	SD-7(DAT0)	SD_D2
8	SD-8(DAT1)	Rev D modify SQR3Y3/SD_CD#
9	SD-9(DAT2)	MC WP
10	SD-SW(GND)	
11	SD-SW-RVS	
12	SD-SW(CD)	
13	SD-1P(GND)	
14	NAIL	
15	XD-11P(D1)	SM_D1
16	XD-12P(D2)	SM_D2
17	XD-13P(D3)	SM_D3
18	XD-14P(D4)	SM_D4
19	XD-15P(D5)	SM_D5
20	XD-16P(D6)	SM_D6
21	XD-17P(D7)	SM_D7
22	XD-18P(VCC)	
23	SD-1(CD/DAT3)	SM_D3
24	SD-2(CMD)	SM_D2
25	SD-3(VSS)	SM_D1
26	SD-4(VCC)	MC CD#
27	SD-5(CLK)	SM_D0
28	SD-6(VSS)	MMC_CLK
29	SD-7(DAT0)	
30	SD-8(DAT1)	
31	SD-9(DAT2)	
32	SD-SW(GND)	
33	SD-SW-RVS	
34	SD-SW(CD)	
35	SD-1P(GND)	
36	NAIL	
37	XD-11P(D1)	SM_R/B#
38	XD-12P(D2)	SM_RE#
39	XD-13P(D3)	SM_CE#
40	XD-14P(D4)	SM_CLE
41	XD-15P(D5)	SM_ALE
42	XD-16P(D6)	SM_WE#
43	XD-17P(D7)	SM_WP#
44	XD-18P(VCC)	SM_D0

Molex-48000-001



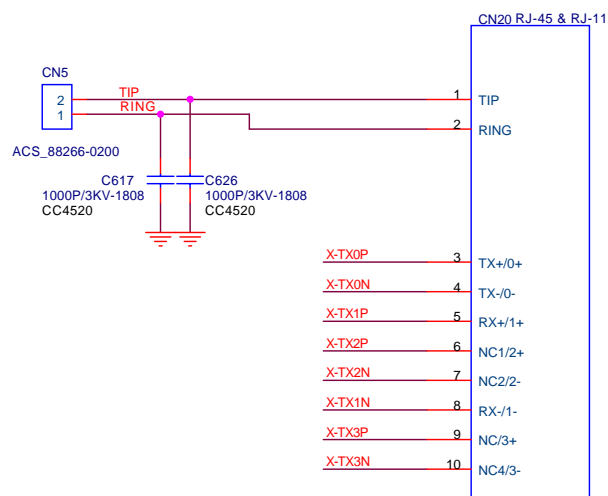


Lan Switch



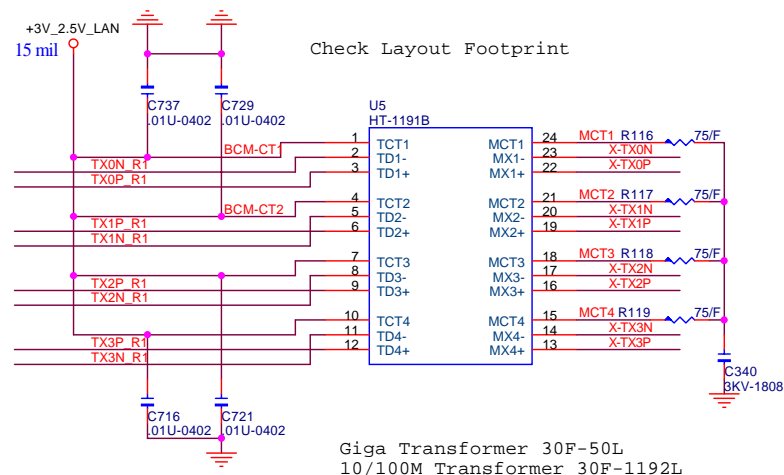
LAN and RJ11 Jack

Check Layout Footprint



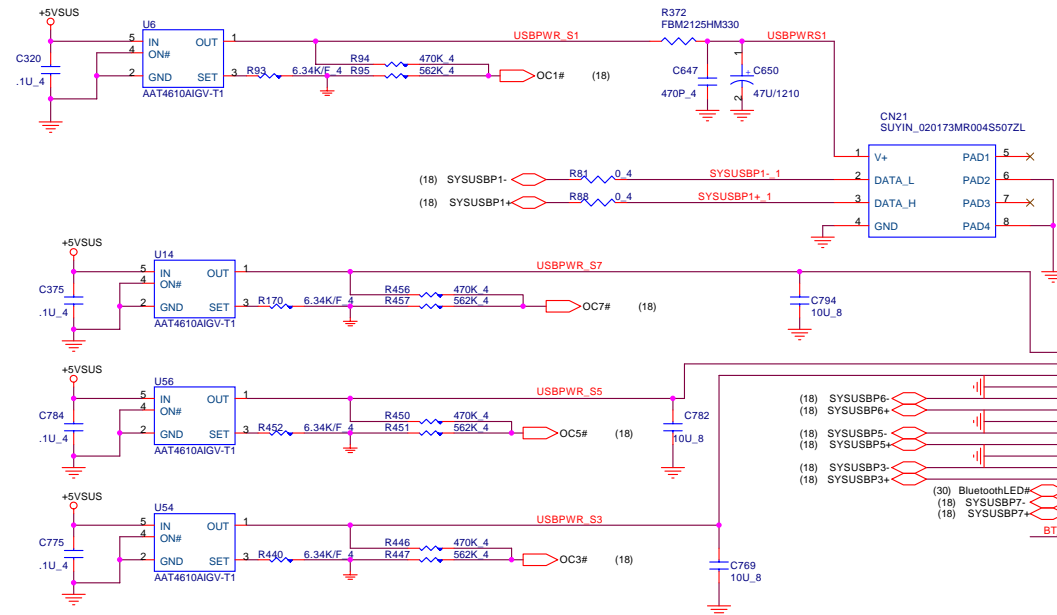
10/100/1000 M TRANSFORMER

Check Layout Footprint

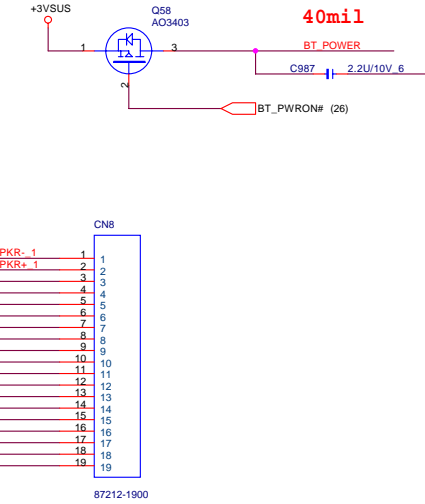


PROJECT : ZF1
Quanta Computer Inc.

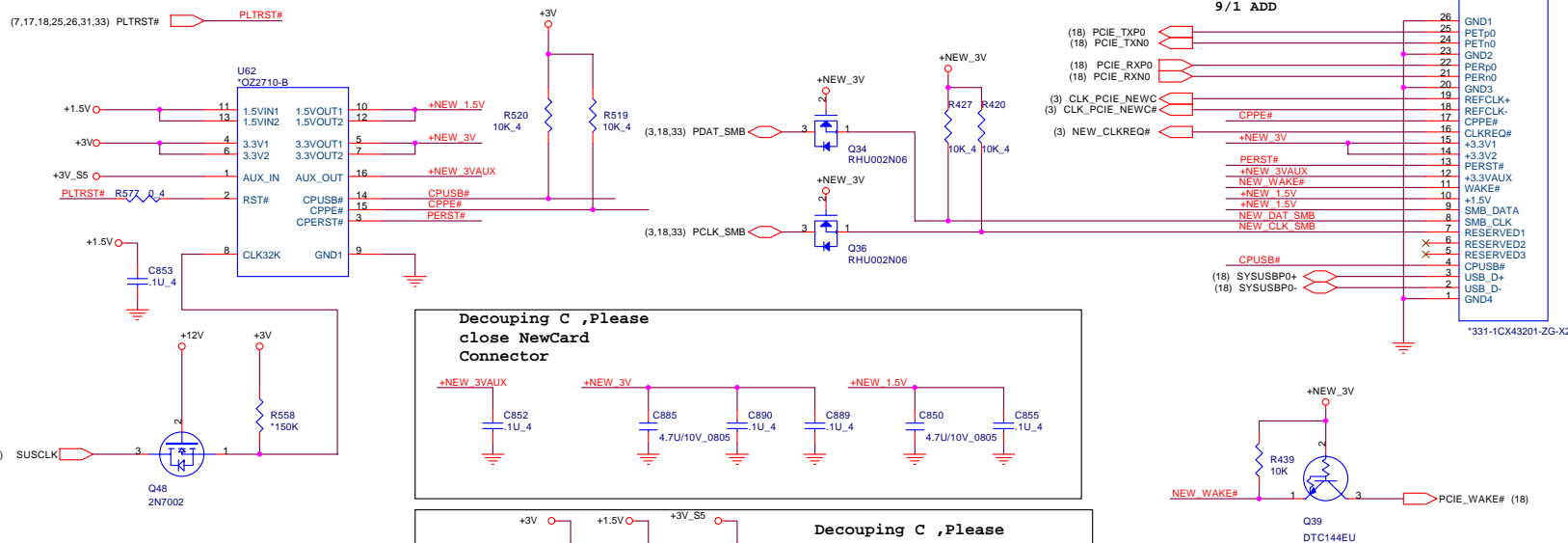
USB Connector and USB board



Bluetooth AND USB Connector

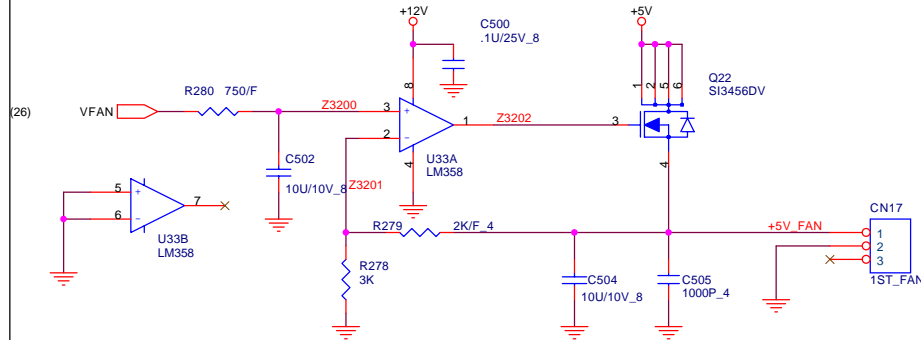


NewCard

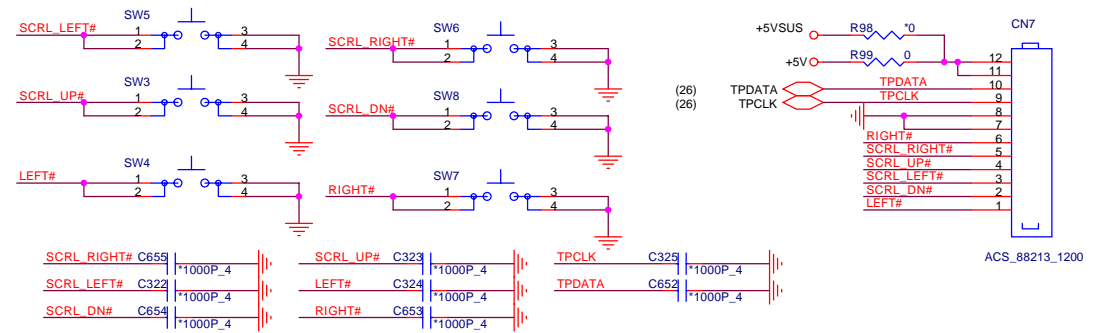




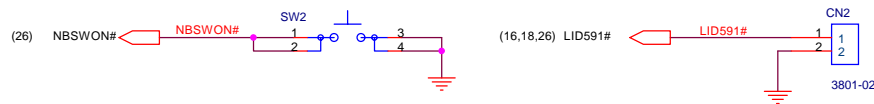
1st FAN OUT CONNECTOR



TouchPad Switch and T/P Module Connector

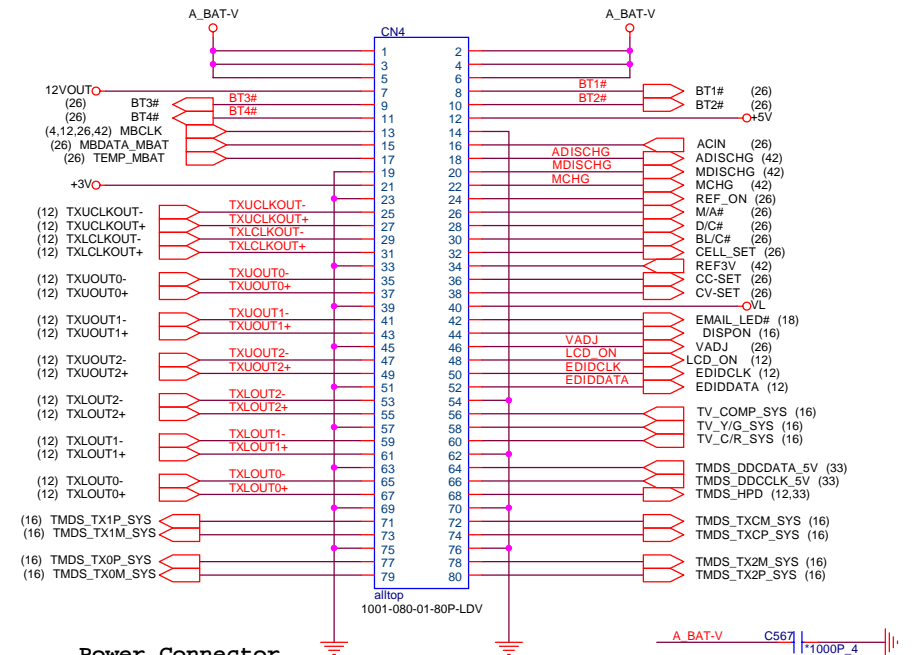
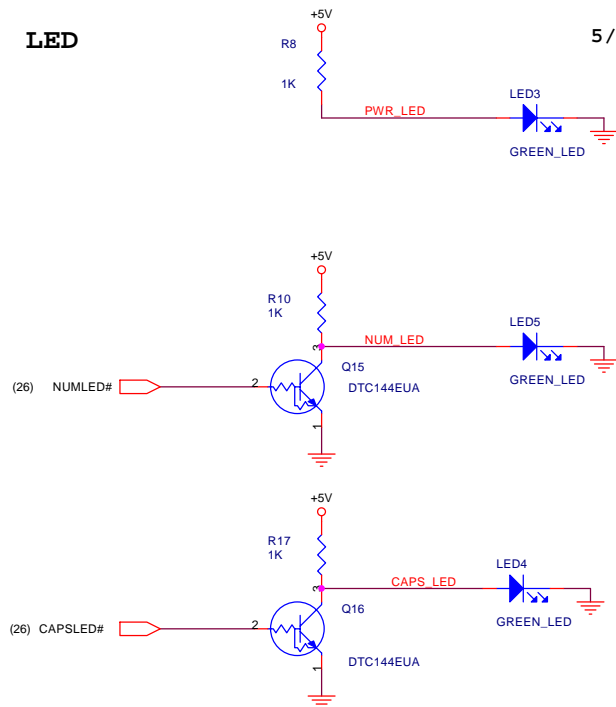


Power Switch

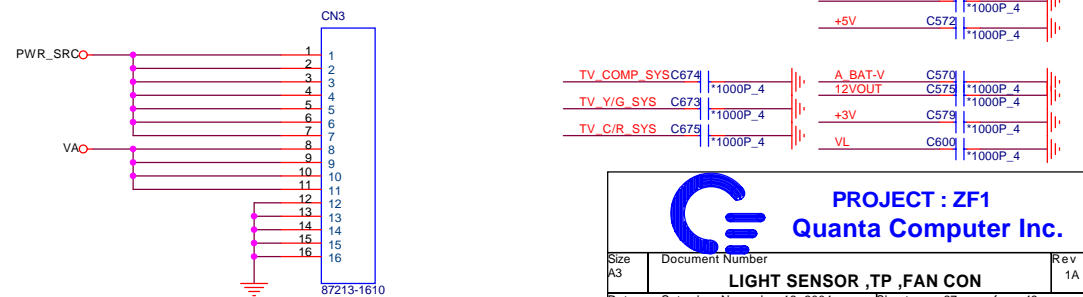


LED

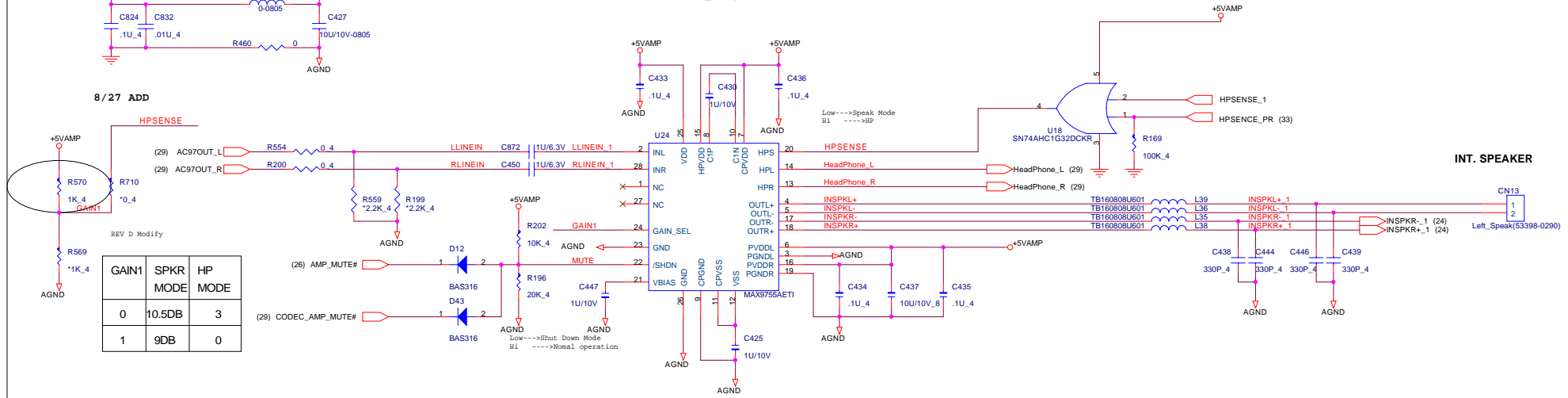
5/28 ADD



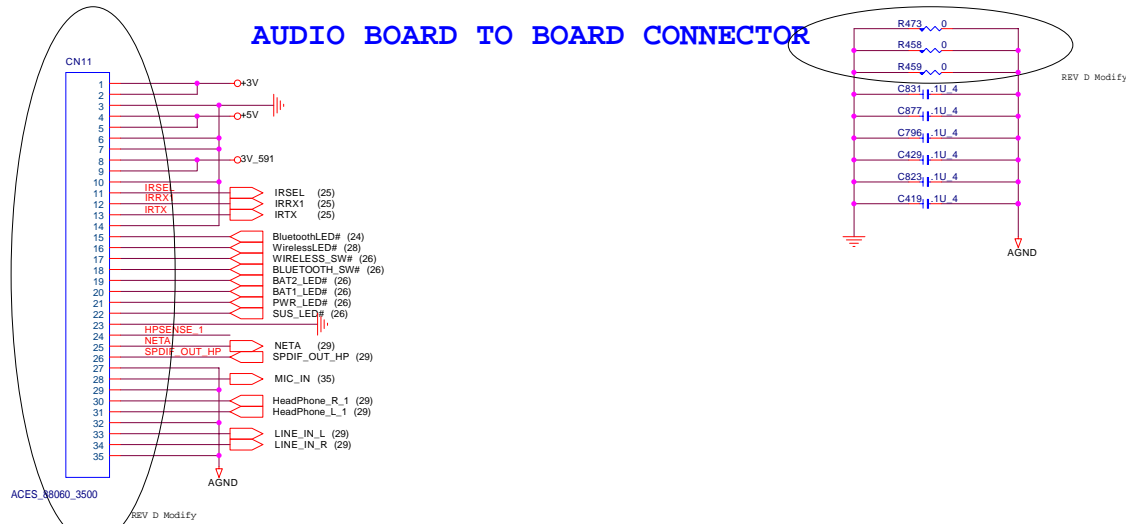
Power Connector



Audio amplifier



AUDIO BOARD TO BOARD CONNECTOR



SWAP BAY POWER CONTROL & RESET

(17) RBAYON#

+12V

R306 47K

Z1422

Q23 DTC144EUA

+5V

SIS402 Q4

C131 0.22U

C107 1000P

C568 22U_10V_1206

C562 .1U

C564 .1U

C555 .1U

C558 .1U

RBAYVCC

(18) RST_RBAY#

+3V

R25 10K

R284 0

C126 .1U_4

U35 -TC/SH08FU

C118 .1U

C101 .1U

C544 10U_10V

PLTRST#

PLTRST# (7,17,18,24,25,26,33)

-RST_RBAY0

RBAYVCC

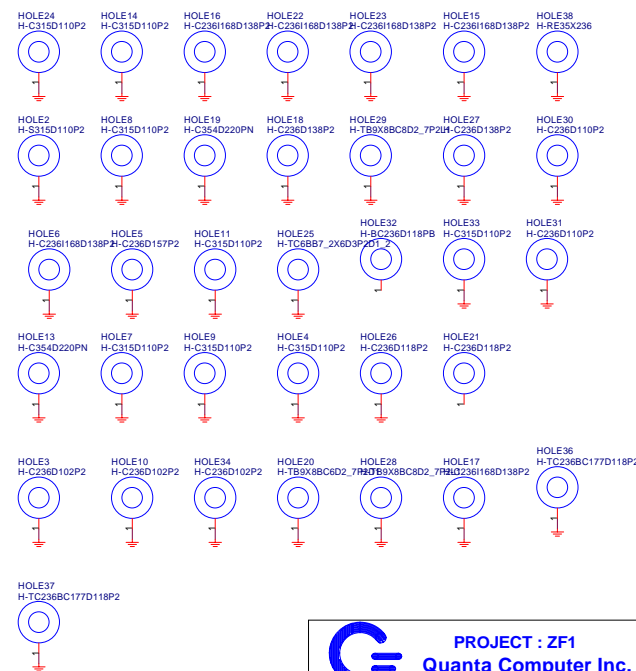
Multi-Bay Connector

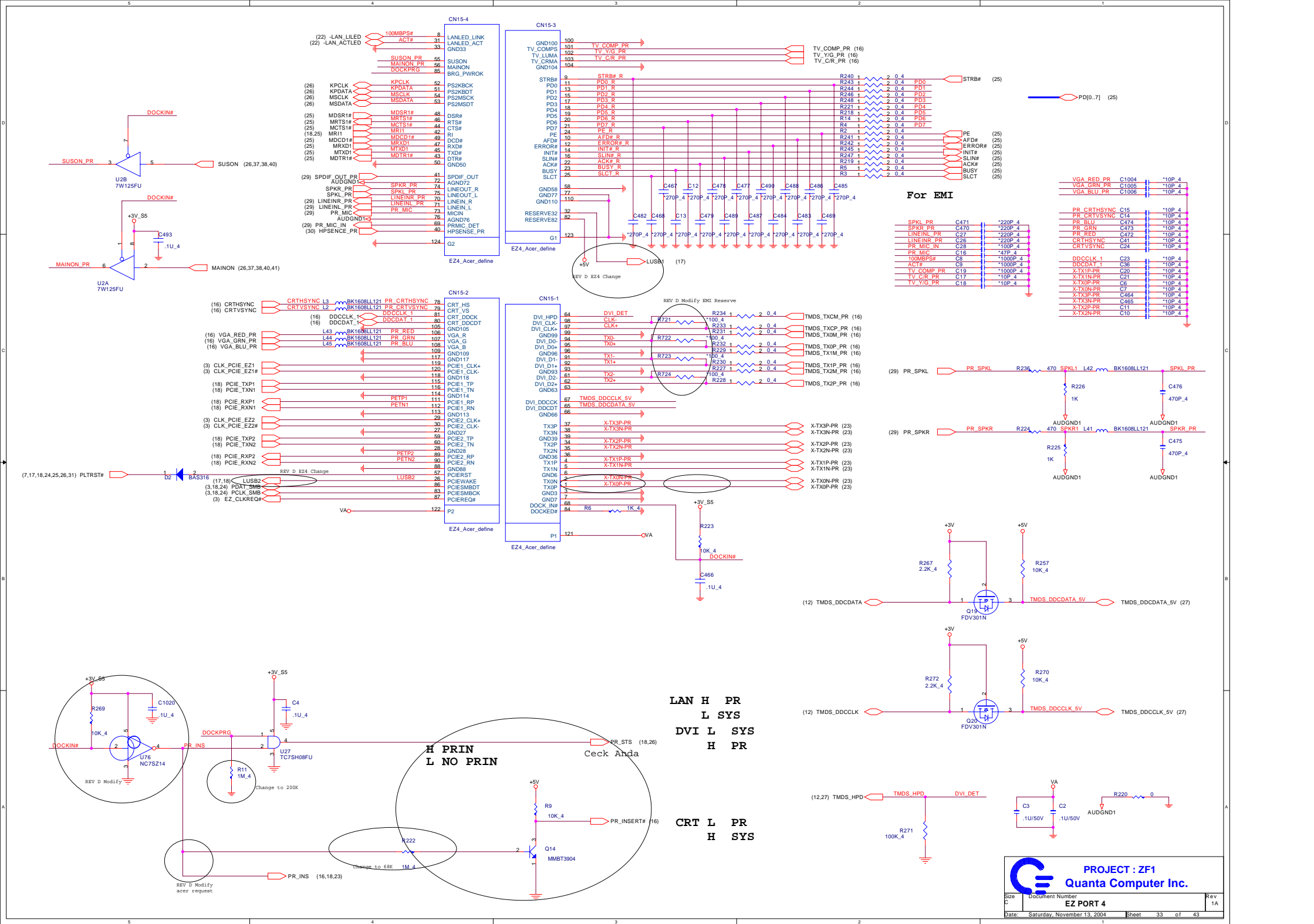
The diagram illustrates a multi-bay connector system. It features a central connector (CN19) with 64 pins. The pins are organized into four groups of 16 pins each, labeled PDD0[0..15], PDD1[0..15], PDD2[0..15], and PDD3[0..15]. The PDD0 group is connected to pins 1-15, PDD1 to pins 16-31, PDD2 to pins 32-47, and PDD3 to pins 48-63. The diagram also shows connections for RST, RBAY0, RBAY1, RBAY2, RBAY3, RBAY4, RBAY5, RBAY6, RBAY7, RBAY8, RBAY9, RBAY10, RBAY11, RBAY12, RBAY13, RBAY14, RBAY15, RBAY16, RBAY17, RBAY18, RBAY19, RBAY20, RBAY21, RBAY22, RBAY23, RBAY24, RBAY25, RBAY26, RBAY27, RBAY28, RBAY29, RBAY30, RBAY31, RBAY32, RBAY33, RBAY34, RBAY35, RBAY36, RBAY37, RBAY38, RBAY39, RBAY40, RBAY41, RBAY42, RBAY43, RBAY44, RBAY45, RBAY46, RBAY47, RBAY48, RBAY49, RBAY50, RBAY51, RBAY52, RBAY53, RBAY54, RBAY55, RBAY56, RBAY57, RBAY58, RBAY59, RBAY60, RBAY61, RBAY62, RBAY63, RBAY64. The diagram includes a table for BAY ID STATUS and a table for BAY ID STATUS.

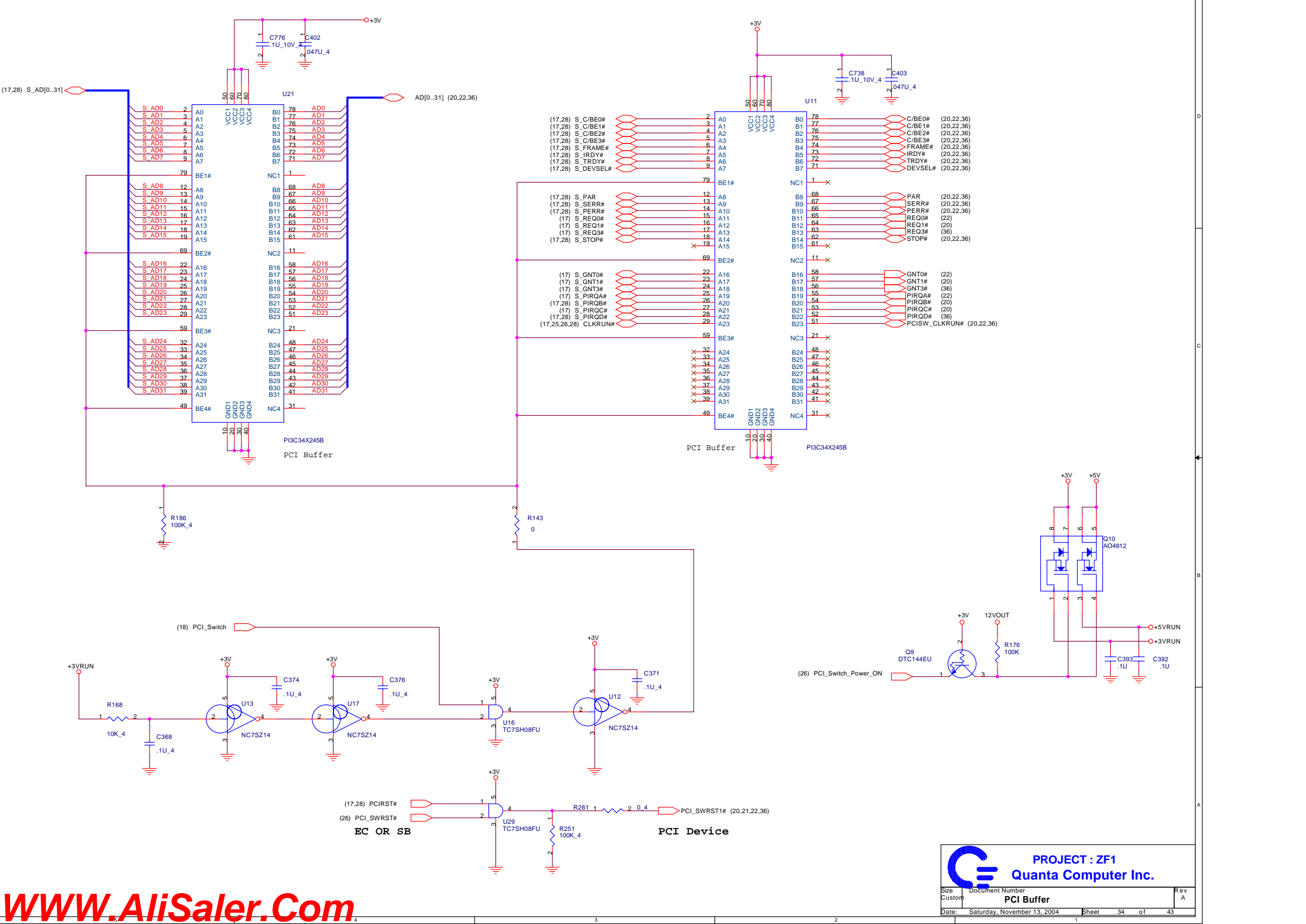
RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD

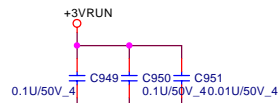
RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD



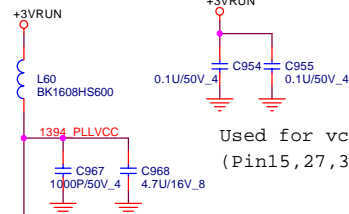




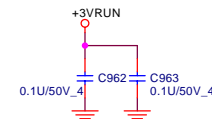


Used for vccp
(Pin20,35,48,62,78)

IEEE-1394



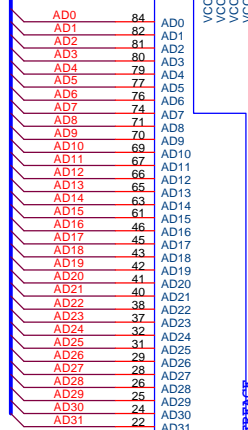
Used for vcc3
(Pin15,27,39,51,59,72,88,100)



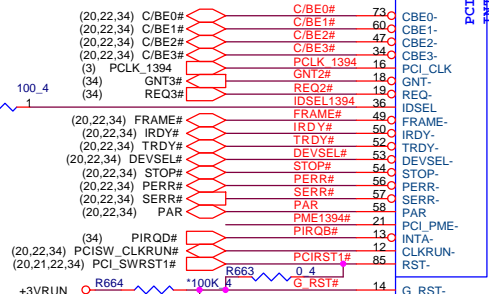
Used for AVCC
(Pin1,2,107,108,120)

ID Select : AD23
Interrupt Pin : PIRQD#
Request indicates : REQ3#
Grant indicates : GNT3#

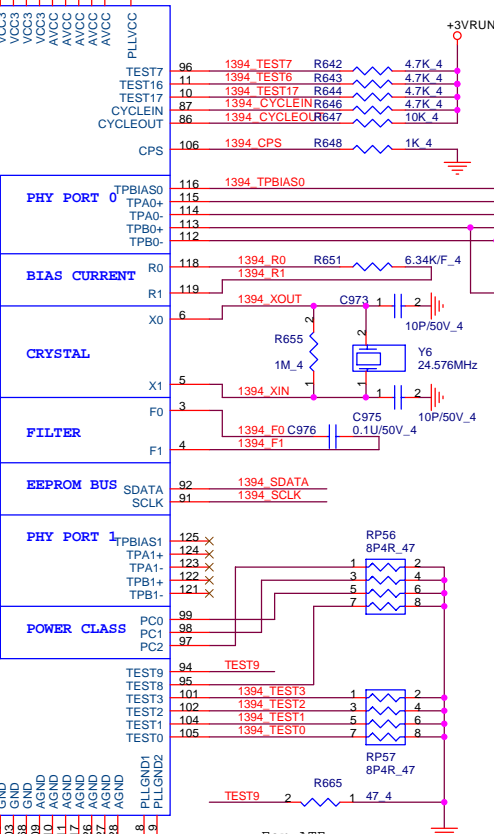
(20,22,34) AD[0..31]



PCI INTERFACE

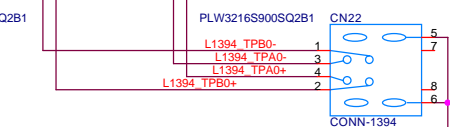
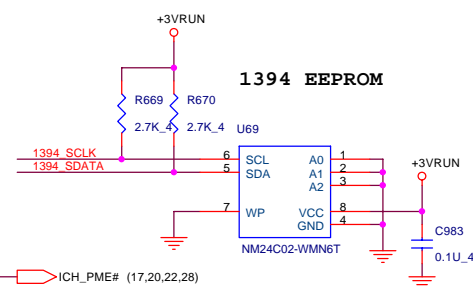


PCLK 1394



For ATE

1394 EEPROM



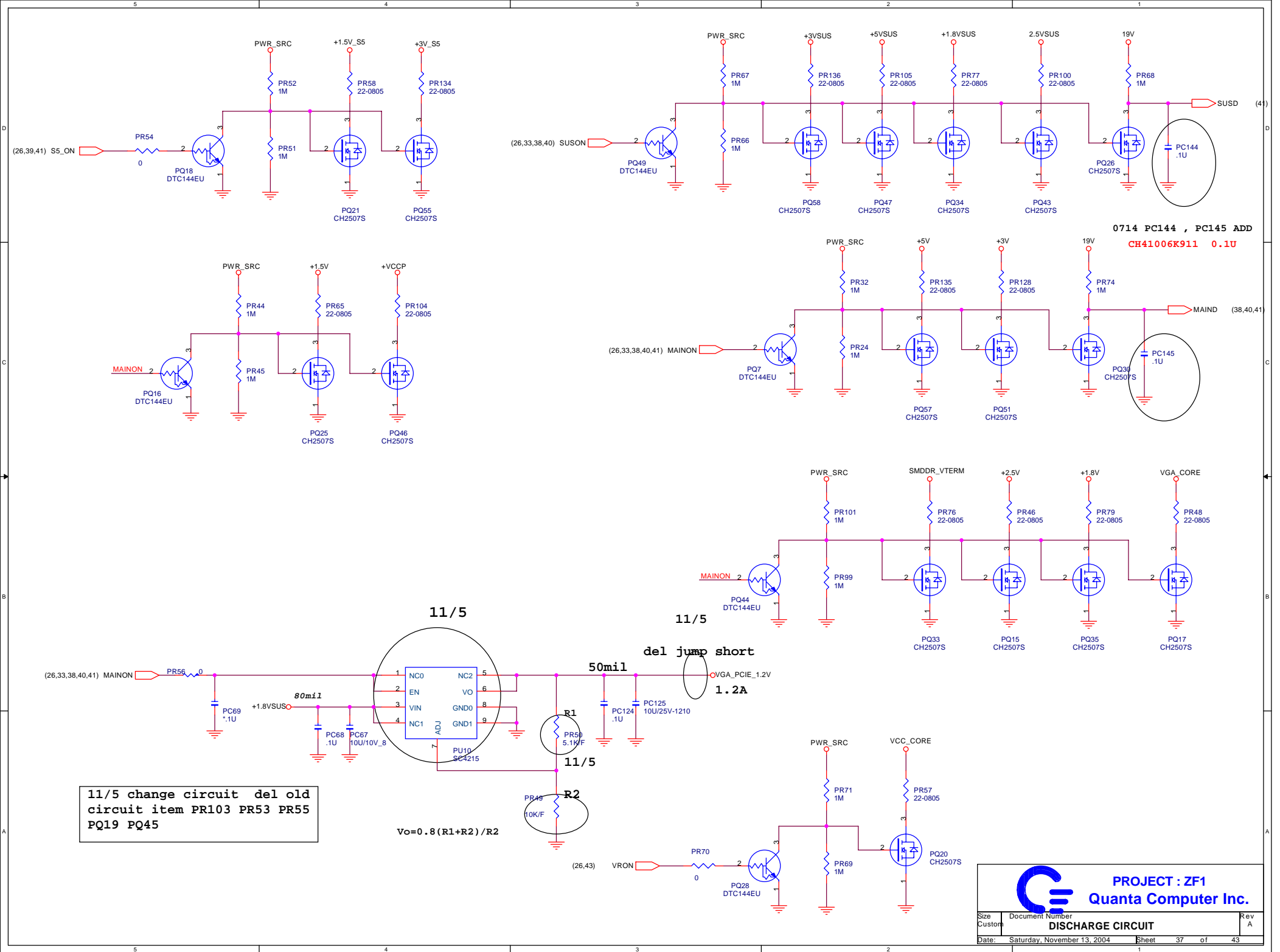
QUANTA
COMPUTER

Title: TSB43AB21[1394]

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$$L / RL(DCR) = Cqe * Rqe$$

$$3R3 \ DCR = 0.0043$$

$$3.3u / 0.0043 = 0.1u * Rqe$$

$$Rqe = 7.68K$$

0714 PR37 change from
CS21823F902 1.82K/F to CS27683F909 7.68K/F

0714 PL13 change from
CV-15A0MZ05 1R5 to CV-33E0MZ01 3R3

0714 PQ11 change from
BAM44040012 AO4404 to BAM60300Z11 FDD6030L

0714 PQ37 change from
BAM47040005 AO4704 to BAM6680Z01 FDD6688

$$L / RL(DCR) = Cqe * Rqe$$

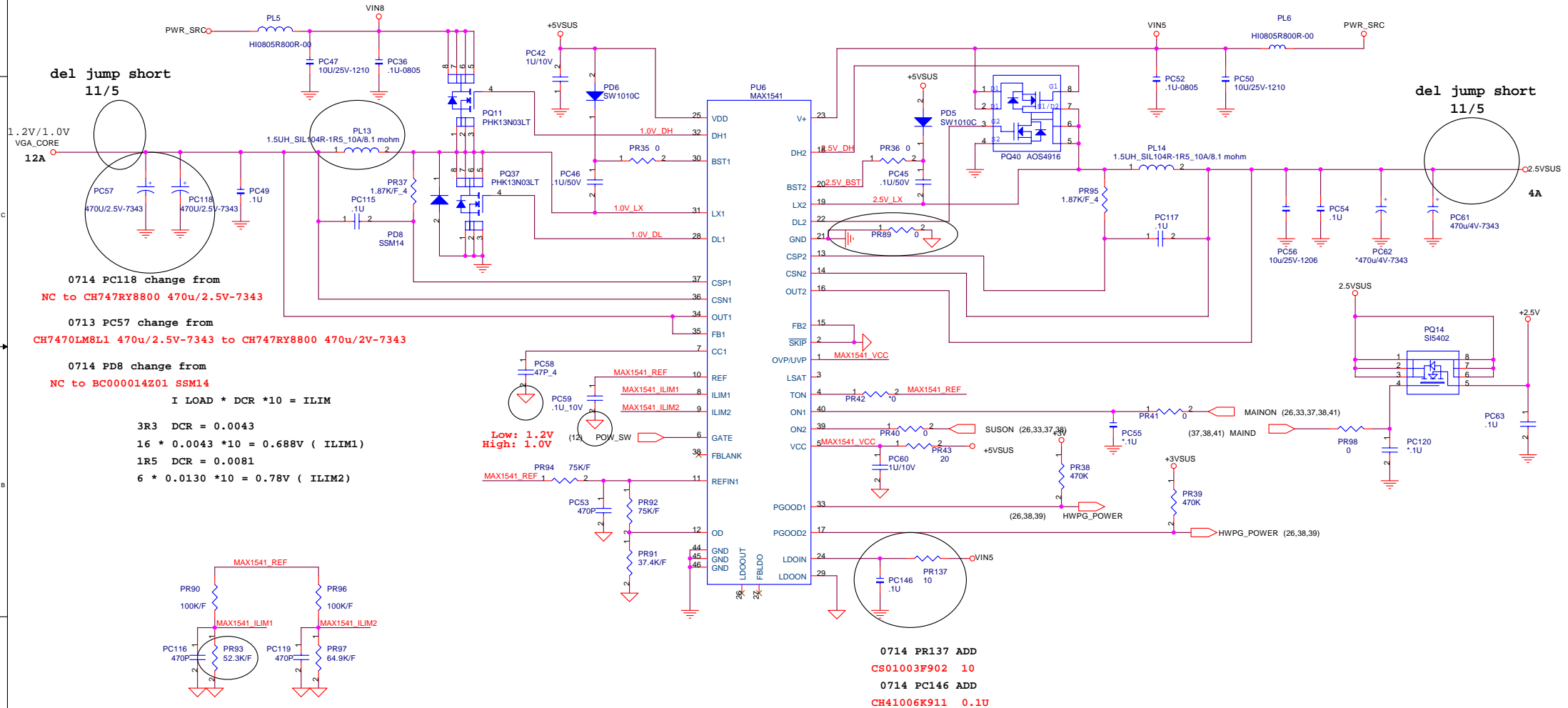
$$3R8 \ DCR = 0.0130$$

$$3.8u / 0.0130 = 0.1u * Rqe$$

$$Rqe = 2.94K$$

del jump short
11/5

del jump short
11/5



0714 PC118 change from
NC to CH747RY8800 470u/2.5V-7343

0713 PC57 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

0714 PD8 change from
NC to BC000014Z01 SSM14

$$I \text{ LOAD} * DCR * 10 = ILIM$$

$$3R3 \ DCR = 0.0043$$

$$16 * 0.0043 * 10 = 0.688V \ (\ ILIM1)$$

$$1R5 \ DCR = 0.0081$$

$$6 * 0.0130 * 10 = 0.78V \ (\ ILIM2)$$

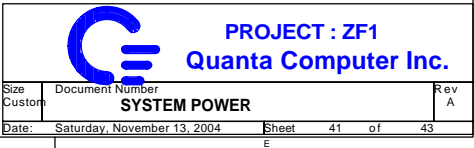
0714 PR137 ADD
CS01003F902 10
0714 PC146 ADD
CH41006K911 0.1u

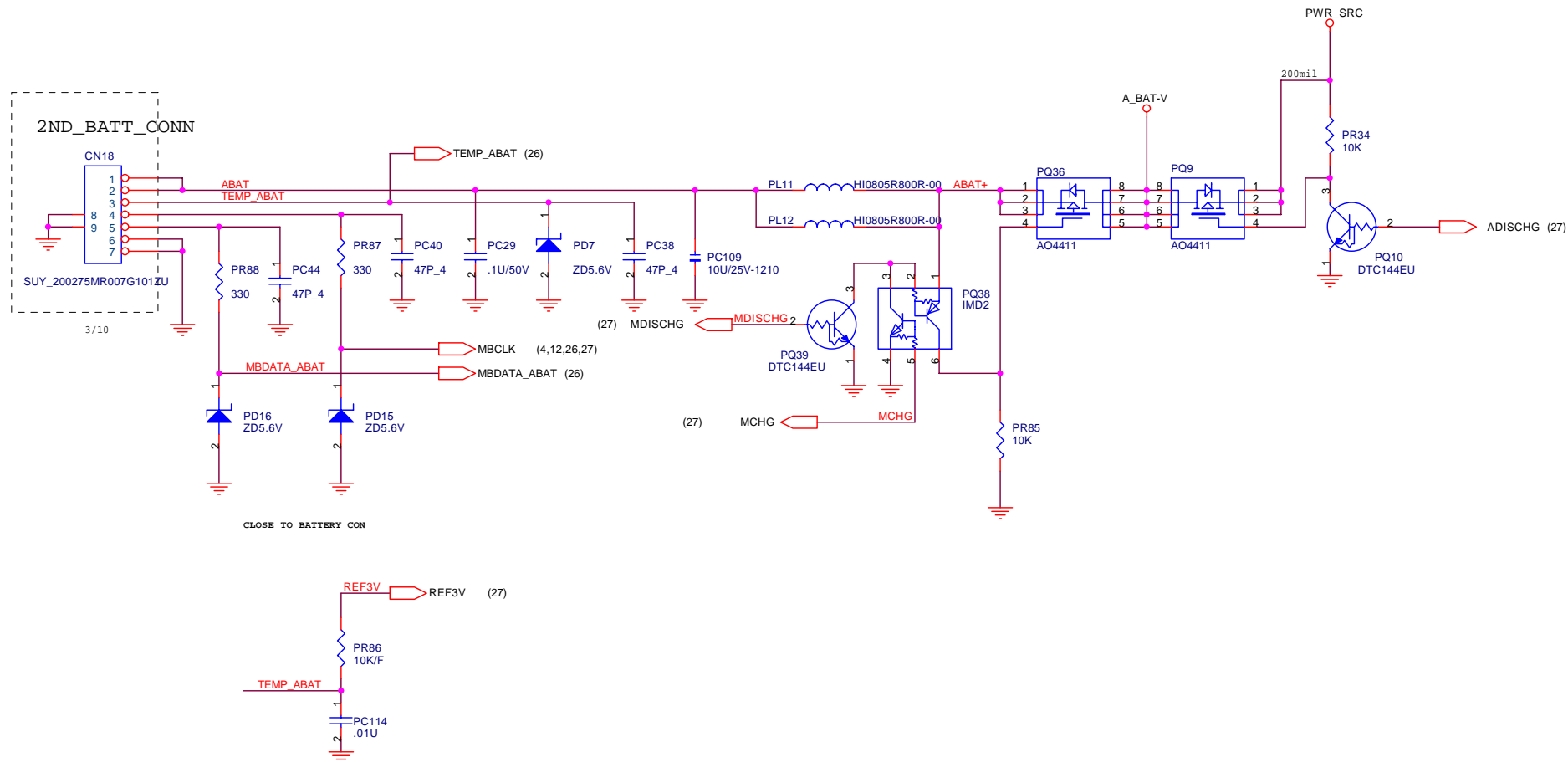
0714 PR93 change from
CS34993F908 49.9K/F to CS35233F908 52.3K/F




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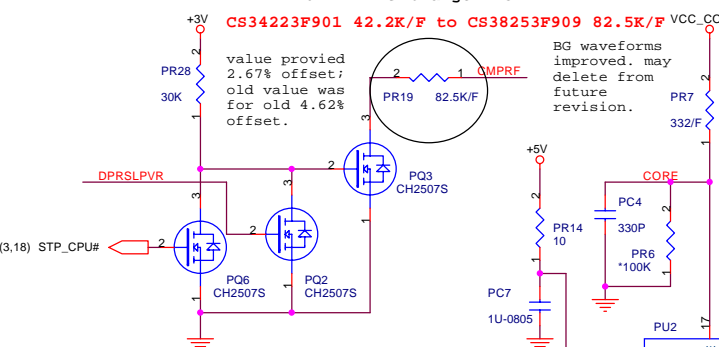


		PROJECT : ZL1	
		Quanta Computer Inc.	
Size	Document Number	Rev	
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0714 PR19 change from

CS34223F901 42.2K/F to CS38253F909 82.5K/F

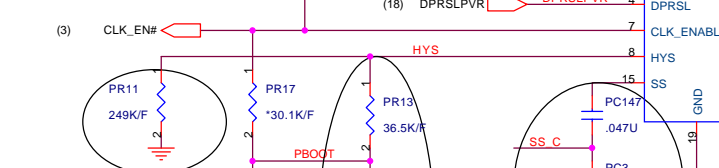
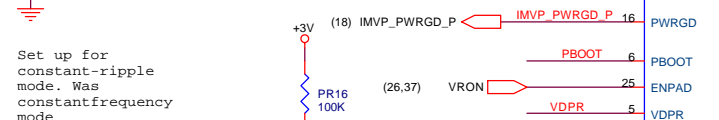
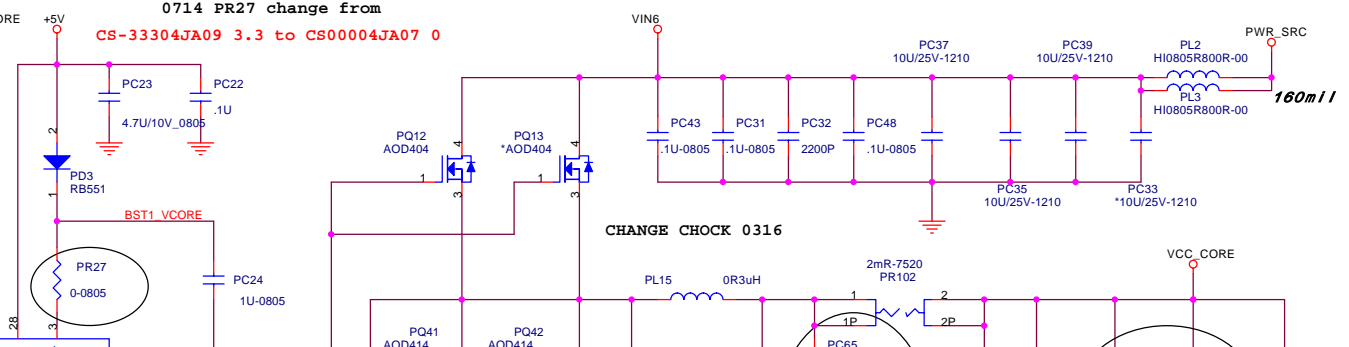
value provided
2.67% offset;
old value was
for old 4.62%
offset.



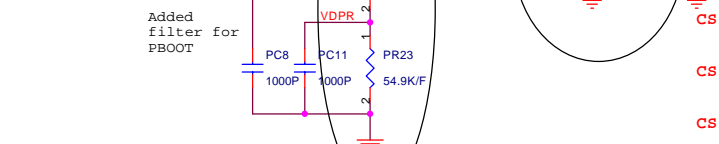
0714 PR27 change from

CS-33304JA09 3.3 to CS00004JA07 0

value provided
2.67% offset;
old value was
for old 4.62%
offset.



20 mil Trace list for layout



Added filter for PBOOT

V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0		V
0	1	0	1	1	1		1.340
0	1	1	0	0	0		1.324
0	1	1	0	1	0		1.292
0	1	1	1	0	0		1.260
0	1	1	1	0	1		1.244
0	1	1	1	1	1		1.212
1	0	0	0	0	1		1.180
1	0	0	0	1	1		1.148
1	0	0	1	1	0		1.100
1	0	1	0	0	1		1.052
1	0	1	0	1	1		1.020
1	0	1	1	1	0		0.972
1	1	0	0	0	0		0.940

0714 PC3 change from
CH31006K919 0.01u to CH31506K917 0.015u

0714 PR13 change from
CS32213F901 22.1K/F to CS33653F906 36.5K/F

0714 PR20 change from
CS32003F909 20K/F to CS33323F901 33.2K/F

0714 PR23 change from
CS33323F901 33.2K/F to CS35493F902 54.9K/F

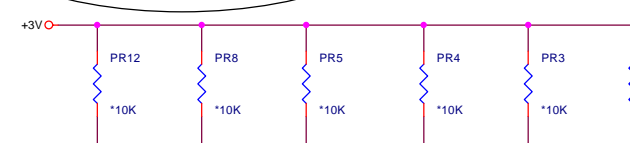
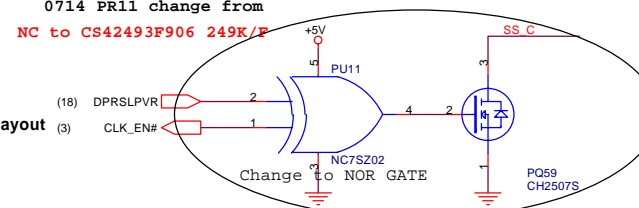
0714 PR11 change from
NC to CS42493F906 249K/F

100 mil Trace list for layout

DH_VCORE
LX_VCORE
DL_VCORE
DH_VCORE2
LX_VCORE2
DL_VCORE2

10 mil Trace list for layout

SC1476
pin 4 pin
5 pin 7
pin 25
pin 30



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