UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :None Installed
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CRV:Chief River

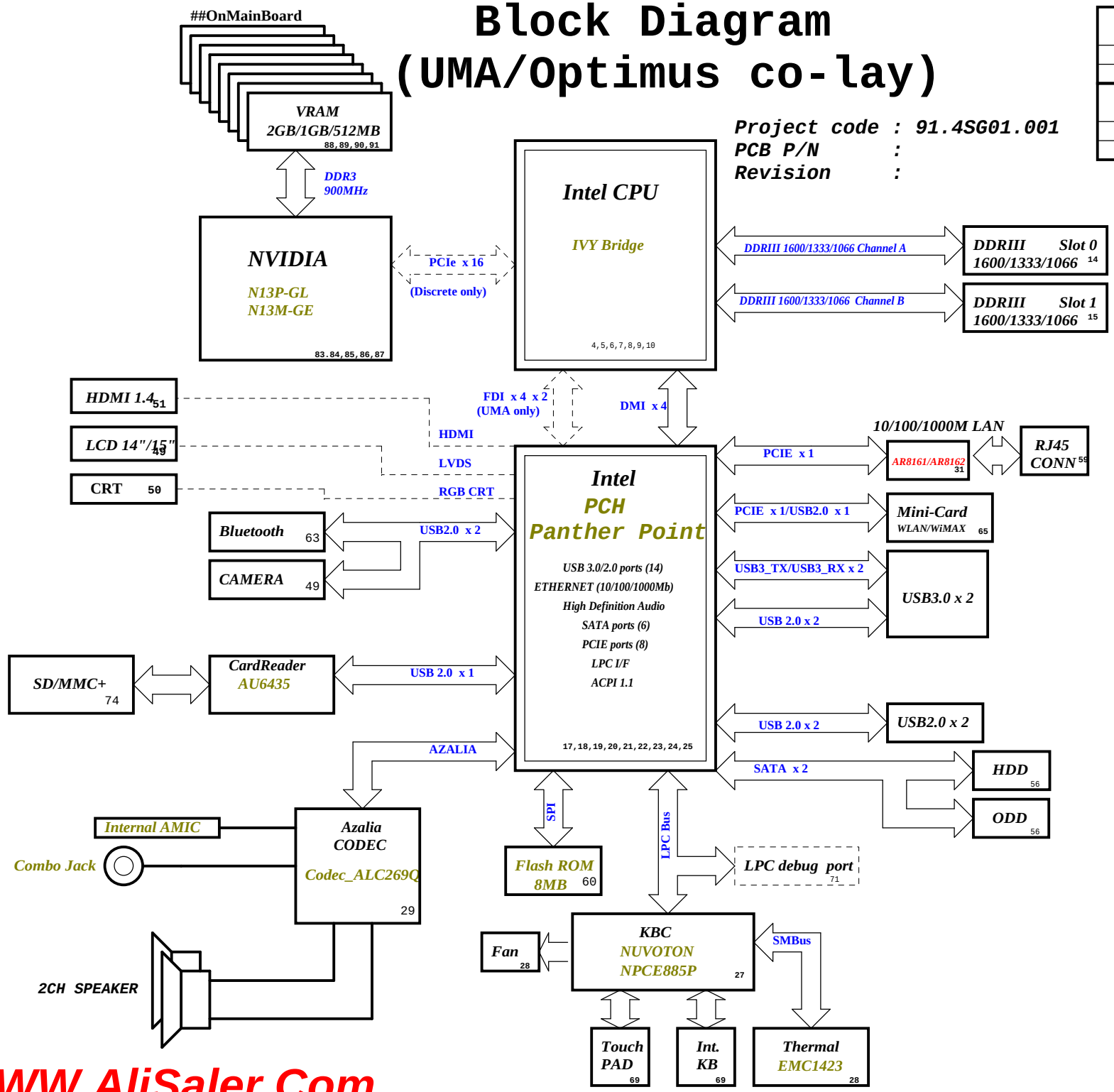
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size A3	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 1 of 103	

Block Diagram (UMA/Optimus co-lay)

Project code : 91.4SG01.001
PCB P/N :
Revision :



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	VCCSA

SYSTEM DC/DC TPS51211 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC G977F 45	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA ISL62882C 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24745 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

VGA switchs 93	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S0 1D05V_VTT	1D5V_VGA_S0 3D3V_VGA_S0 1D05V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: A3 | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 2 of 103

WWW.AliSaler.Com

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

All Not update

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	N/A
1	HDD1
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mTable of Content

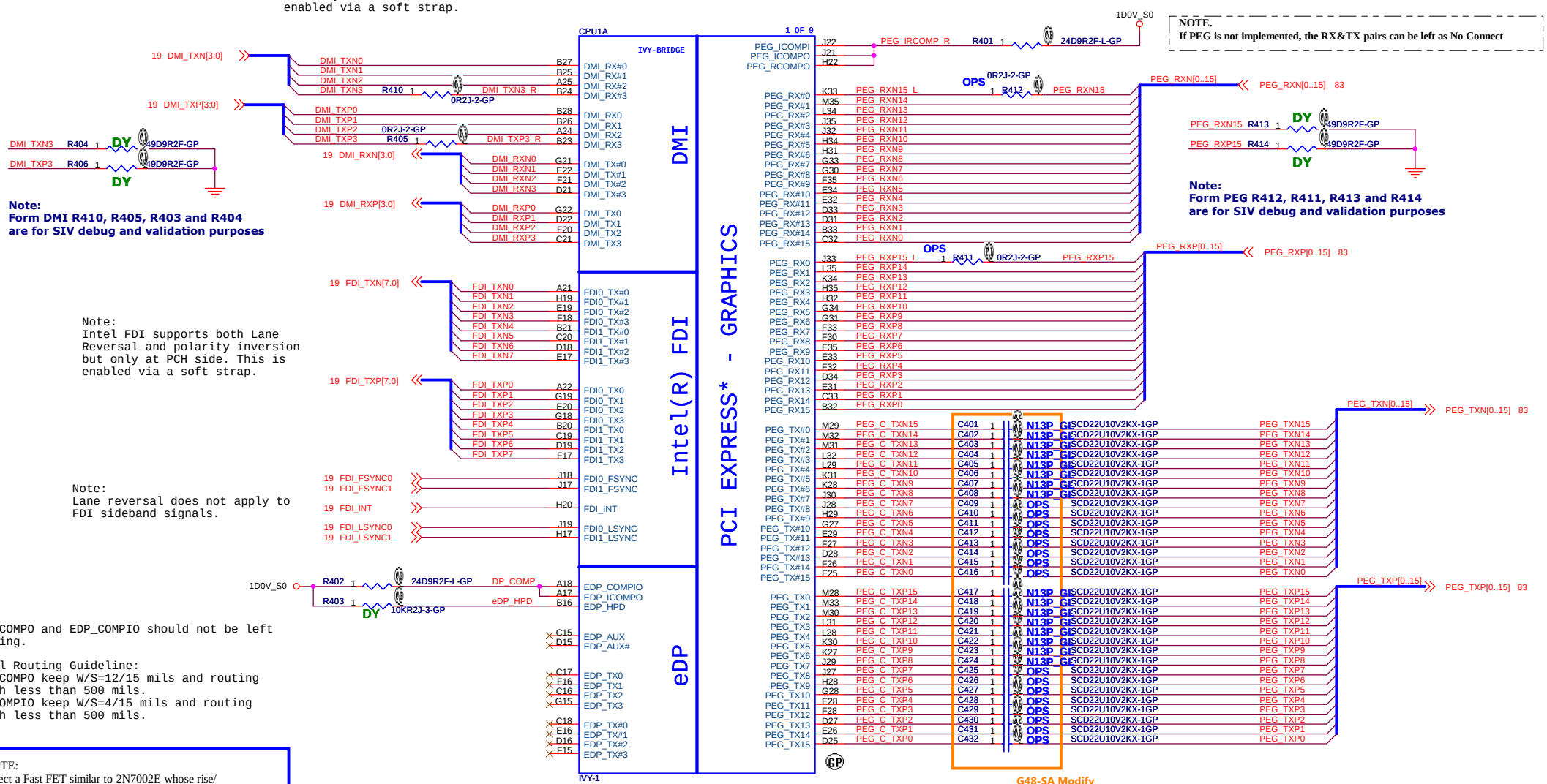
Size: A3 | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 3 of 103

SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Form DMI R410, R405, R403 and R404 are for SIV debug and validation purposes

Note:
Form PEG R412, R411, R413 and R414 are for SIV debug and validation purposes

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

62.10040.821

1st = 22.10252.171

2nd = 62.10040.821

3rd = 62.10055.551

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

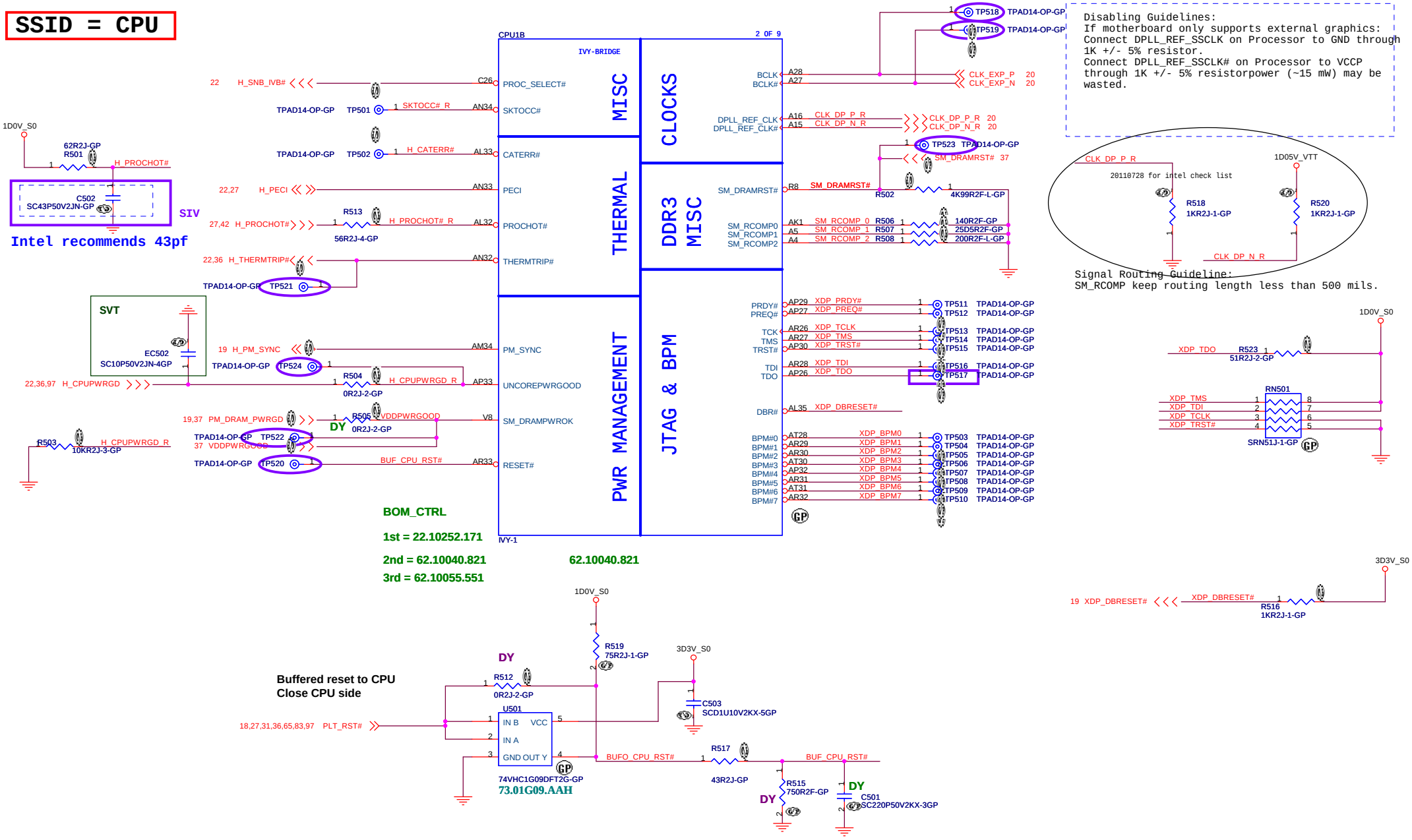
Title: CPU (PCIE/DMI/FDI)

Size: A3 | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 4 of 103

WWW.AliSaler.Com

SSID = CPU



NOTE

	U501	R512	R519	R517	R515	C503	C501
HR	DY	0 ohm 63.R0034.1DL	DY	1.5K ohm 64.15015.6DL	750 ohm 64.75005.6DL	DY	DY
CRV	73.01G09.AAH	DY	75 ohm 63.75034.1DL	43 ohm 63.43034.1DL	DY	0.1uF 78.10423.2FL	DY

Default CRV

JV10-CS

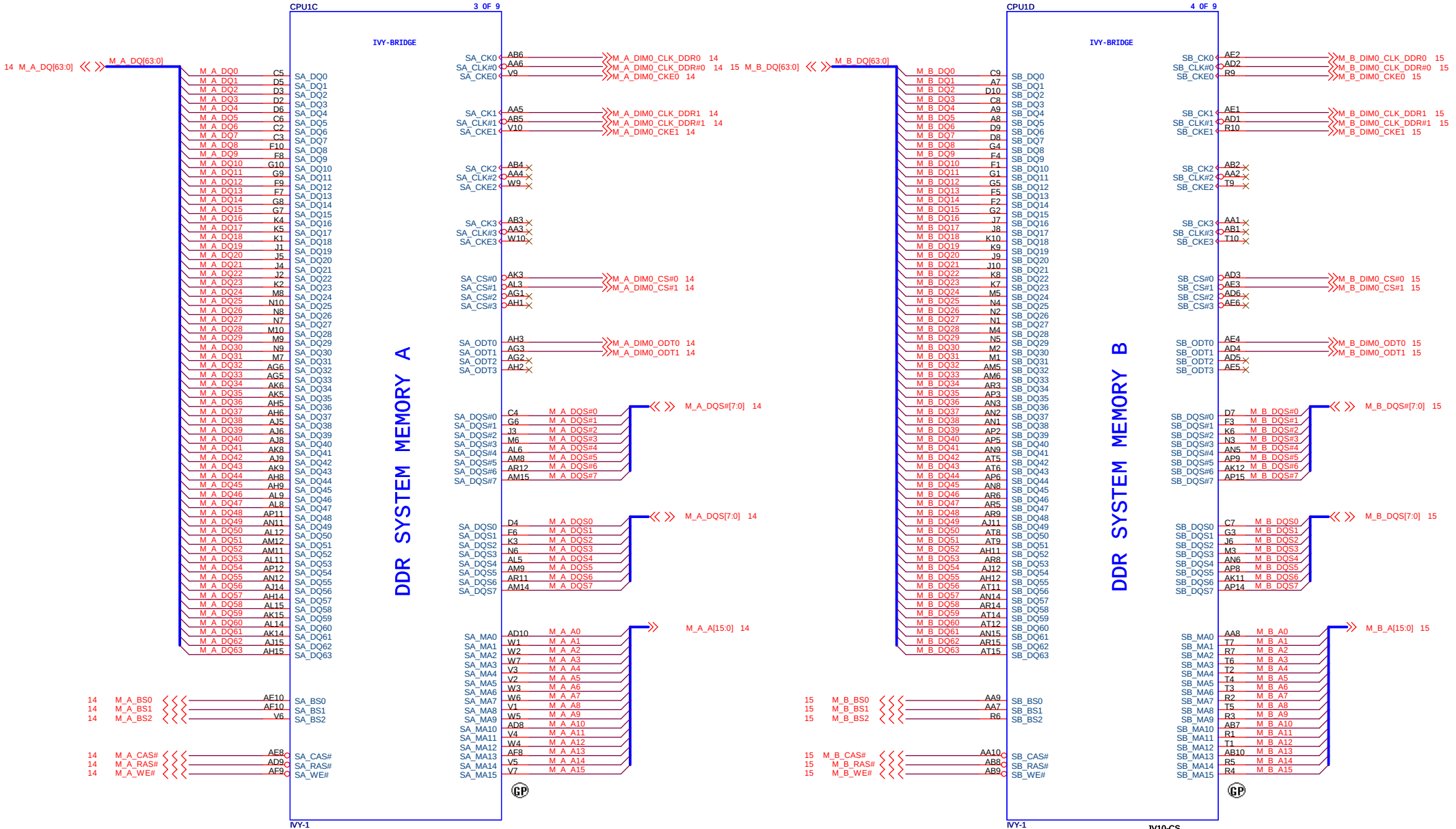
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/CLOCK/PM

Size: A3 | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 5 of 103

SSID = CPU



62.10040.821

BOM_CTRL

1st = 22.10252.171
2nd = 62.10040.821
3rd = 62.10055.551

62.10040.821

BOM_CTRL

1st = 22.10252.171

2nd = 62.10040.821

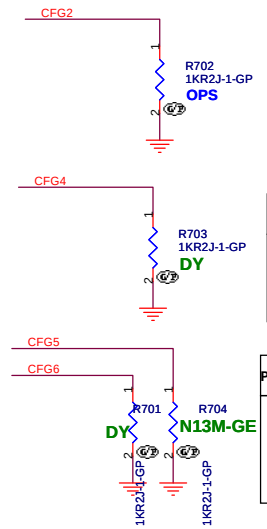
3rd = 62.10055.551

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (DDR)	
Size A3	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 6 of 103	

WWW.AliSaler.Com

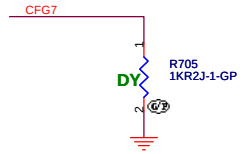
SSID = CPU



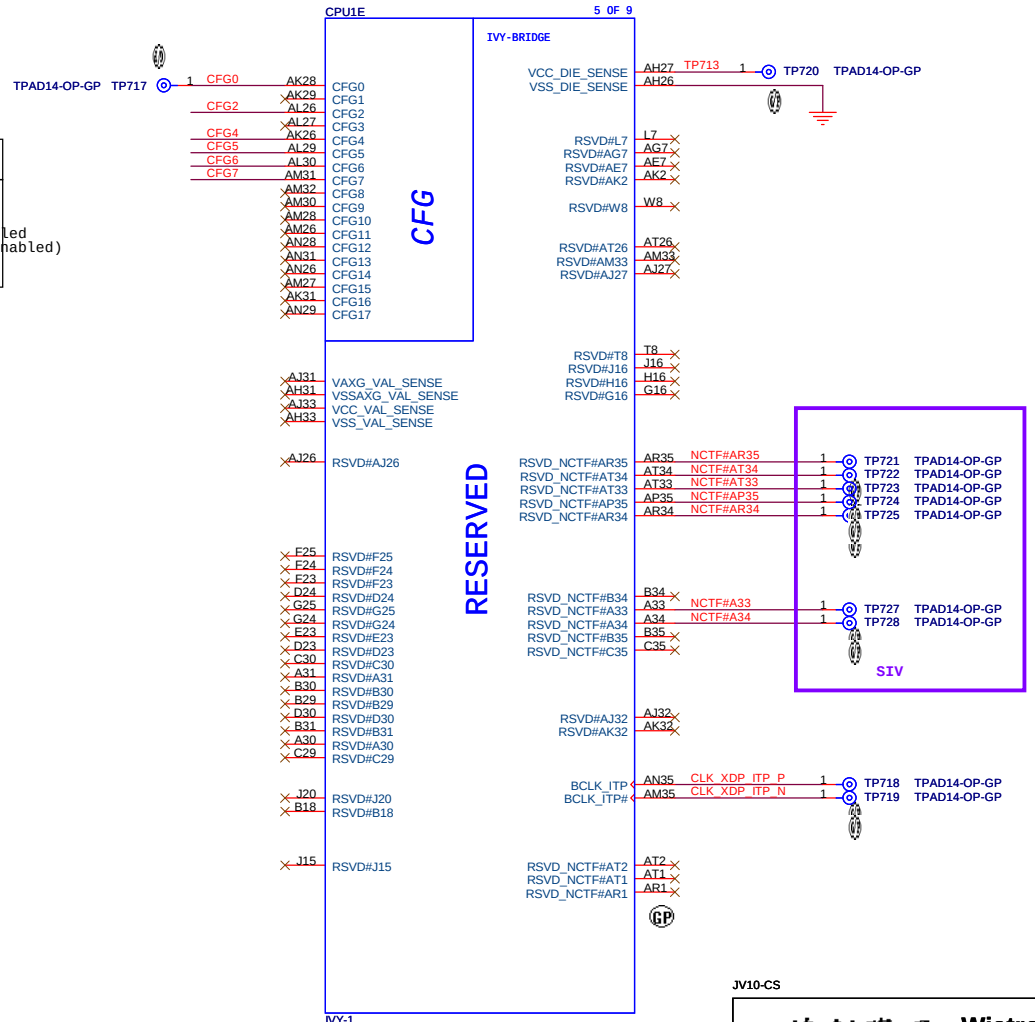
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



62.10040.821

BOM_CTRL

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (RESERVED)	
Size A3	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 7 of 103	

SSID = CPU

POWER

CPU1F — 6 OF 9 — IVY-BRIDGE

VCC CORE:53A

VCC_CORE

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP
C803 SC10U6D3V5KX-1GP
C804 SC10U6D3V5KX-1GP
C811 SC10U6D3V5KX-1GP
DY DY

C817 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 SC10U6D3V5KX-1GP
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP
DY DY

VCC_CORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

BOM_CTRL

IVY-1

CORE SUPPLY

PEG AND DDR

VCCIO:8.5A

1D0V_S0

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 E13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841
SC10U6D3V5KX-1GP

1D0V_S0

C812 C813 C814 C829 C830 C842 C843 C844 C845
SC10U6D3V5KX-1GP

-to 17pcs

TC8xx

470uF x2

SVID

R807 need to close to CPU

R807 75R2F-2-GP 110722 Ge 1D0V_S0

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK_R R805 1 0R2J-2-GP H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT_R R806 1 0R2J-2-GP H_CPU_SVIDDAT 42

R804 130R2F-1-GP 1D0V_S0

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D0V_S0

R808 10R2F-L-GP
VCCIO_SENSE
VSSIO_SENSE
R809 10R2F-L-GP

SENSE LINES

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 VCCIO_SENSE 1 TP802 TPAD14-OP-GP
VSS_SENSE_VCCIO A10 VSSIO_SENSE 1 TP803 TPAD14-OP-GP

GP

JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	mCPU (VCC_CORE)		
Size Custom	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 8 of 103		

62.10040.821

WWW.AliSaler.Com

SSID = CPU

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

M3 - Processor Generated SO-DIMM VREF_DQ

M_VREF_DQ_DIMM0 — R915 1 — DY — 0R2J-2-GP
M_VREF_CA_DIMM0 — R916 1 — DY — 0R2J-2-GP
12 DDR_WR_VREF01
12 DDR_WR_VREF02
RN903 SRN1KJ-7-GP DY

POWER

VCC_GFXCORE

CPU1G — 7 OF 9 — IVY-BRIDGE

GRAPHICS: VAXG1–VAXG54

SENSE LINES: VAXG_SENSE AK35 — VCC_AXG_SENSE 42; VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF: SM_VREF AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1

DDR3 -1.5V RAILS: VDDQ1–VDDQ15

PROCESSOR VDDQ: 12A

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP

1D5V_S0 — SIV — TC902 ST330U2D5VDM-17GP — DY

TC9xx 330uF

SA RAIL: VCCSA1–VCCSA8

VCCSA

PROCESSOR VCCSA: 6A

C916 C915 C917 — SC10U6D3V5KX-1GP

TC9xx 330uF

R902 need be close to pin H23.

Close to CPU

VCC_GFXCORE — R906 100R2F-L1-GP-U — VCC_AXG_SENSE — VSS_AXG_SENSE — R907 100R2F-L1-GP-U

SIV for intel recommend

NOTE

	R906/R907
HR	100 ohm 64.10005.6DL
CRV	10 ohm 64.10R05.6DL

Default CRV

MISC: VCCSA_SENSE H23 — VCCSA_SENSE — VCCSA_SENSE 48

VCCSA_VID0 C22 — VCCSA_SELECT0 48
VCCSA_VID1 C24 — VCCSA_SELECT1 48

VCCIO_SEL A19

1.8V RAIL: VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2

1D8V_S0

VCCPLL:1.5A

C925 C923 C922 C924 — SC10U6D3V5KX-1GP, SC1U10V2KX-1GP

TC9xx 330uF

IVY-1

62.10040.821

BOM_CTRL

SIV

3D3V_S5 — R913 10KR2F-2-GP — DY — H_VCCIO_SEL

ES2 dummy R913

1D0V_S0 — R917 10KR2J-3-GP — DY — VCCSA_SELECT0

1D0V_S0 — R920 10KR2J-3-GP — DY — VCCSA_SELECT1

R918 1KR2J-1-GP

R919 1KR2J-1-GP

SIT

JV10-CS

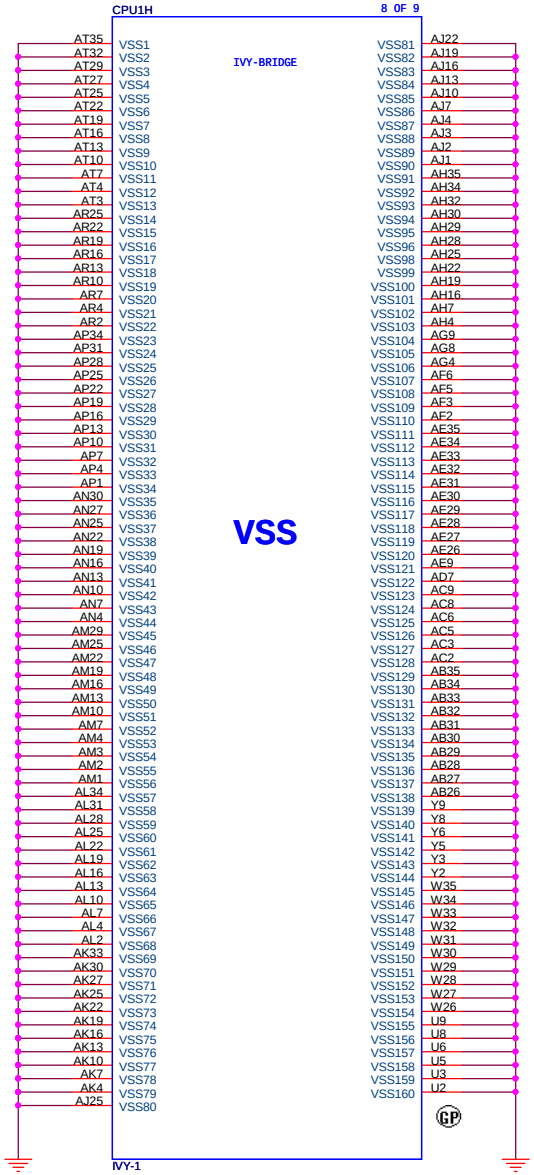
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: mCPU (VCC_GFXCORE)

Size: A3 | Document Number: G48/G58 | Rev: SC

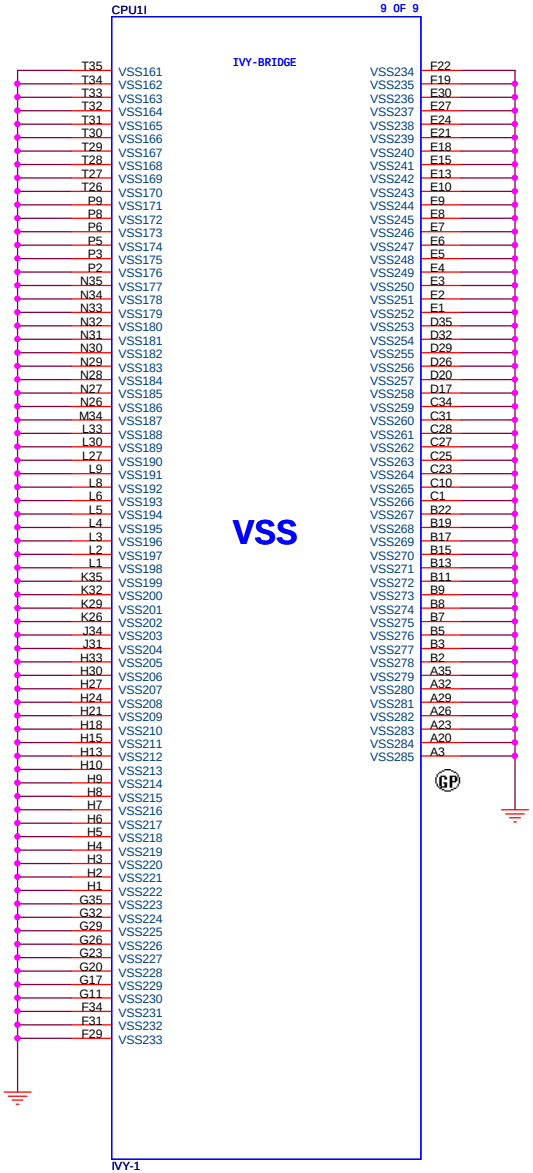
Date: Friday, February 17, 2012 | Sheet 9 of 103

SSID = CPU



62.10040.821

BOM_CTRL



62.10040.821

BOM_CTRL

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU(VSS)***	
Size A3	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 10 of 103	

WWW.AliSaler.Com

(Reserved)

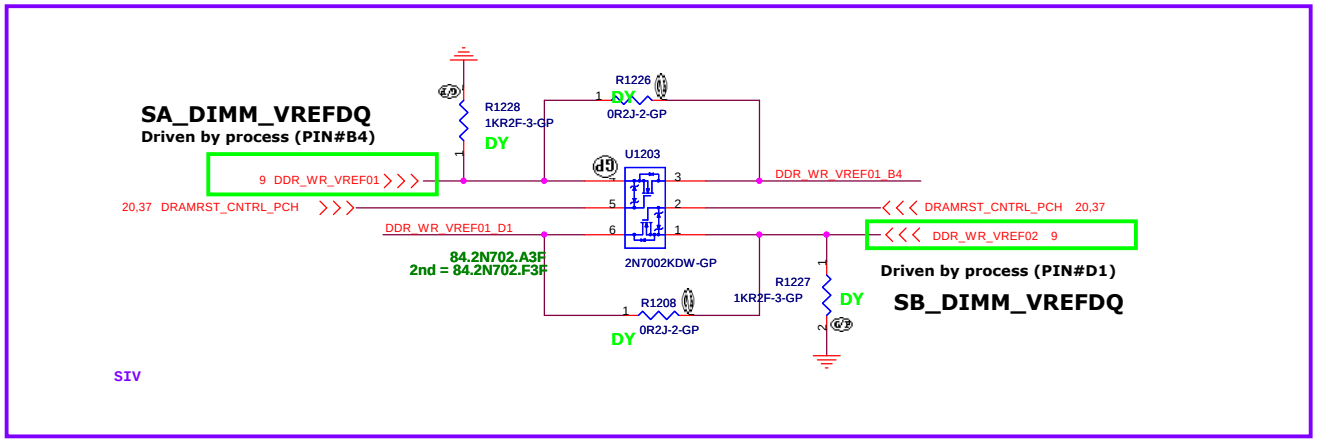
JV10-CS

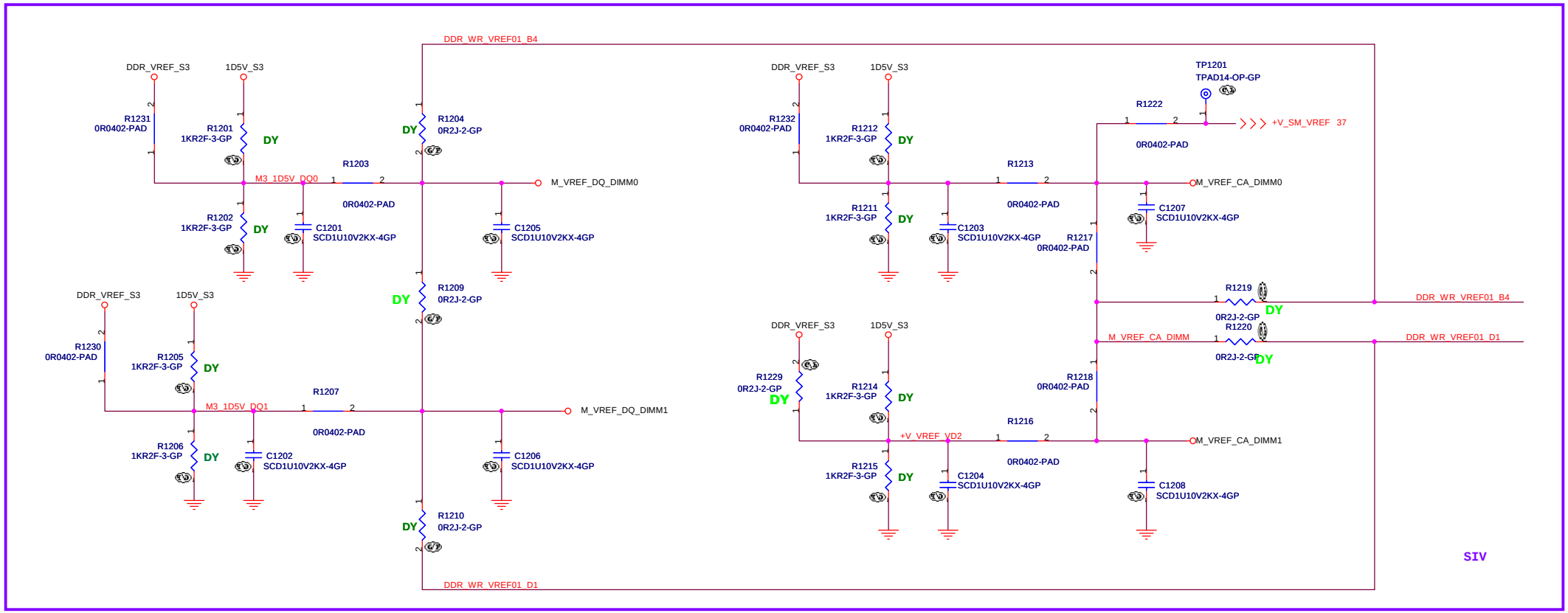
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	XDP	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 11 of 103	

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

For CRV:





JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***M1 & M3 Implementation***
Size / Document Number	**G48/G58**
Rev	**SC**
Date: Friday, February 17, 2012	Sheet 12 of 103

WWW.AliSaler.Com

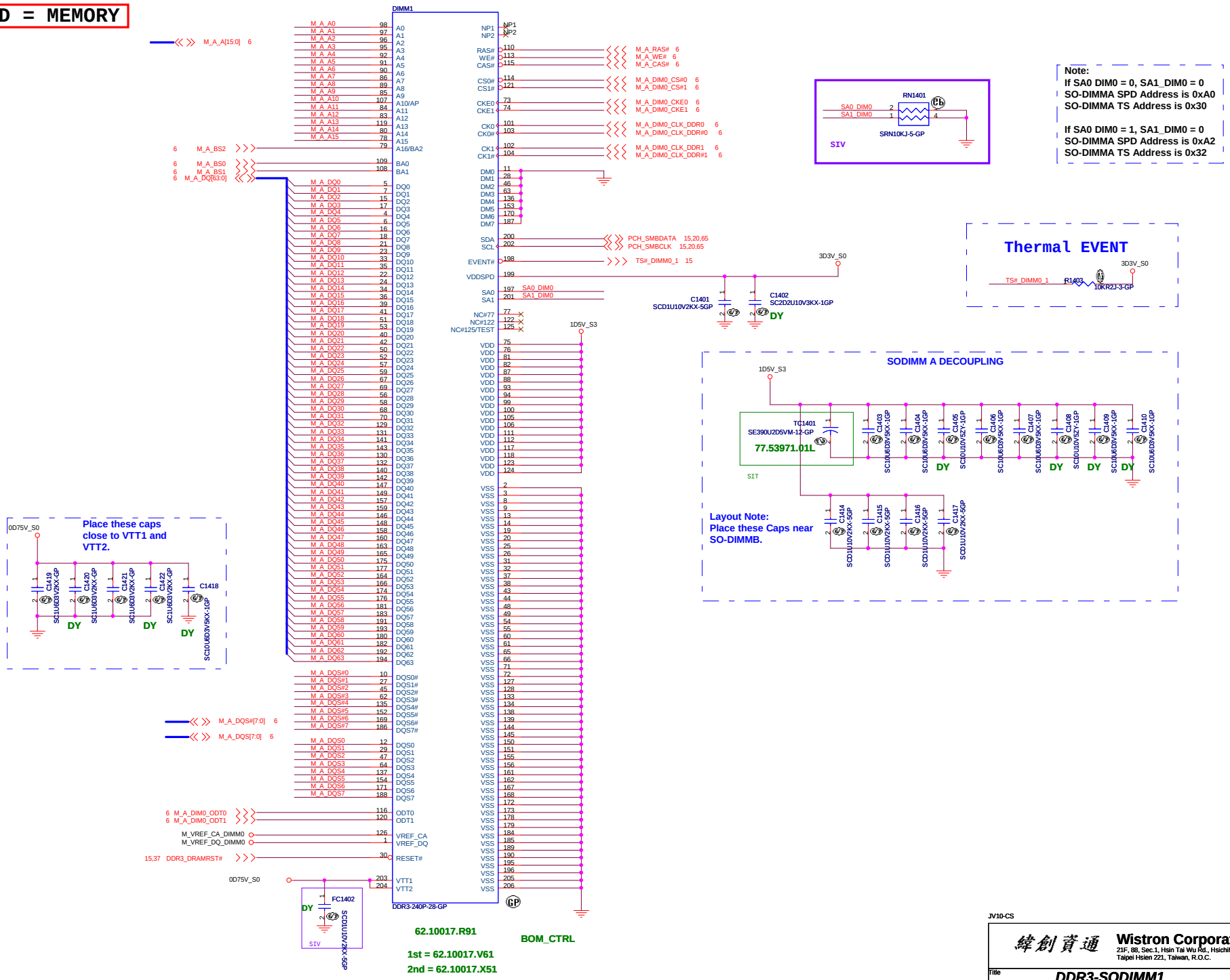
(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 13 of 103	

SSID = MEMORY



WWW.AliSaler.Com

JV10-CS

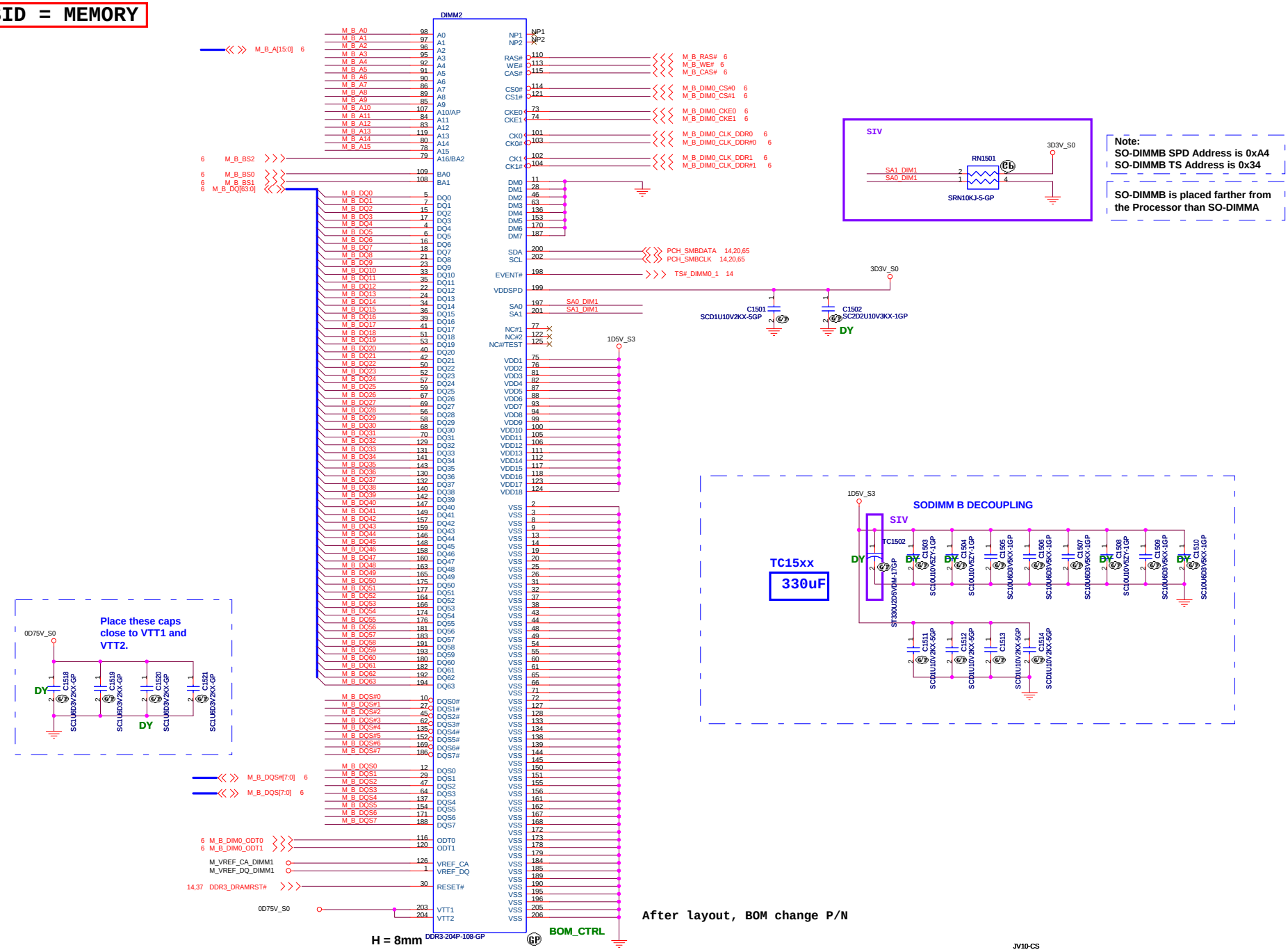
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 14 of 103

SSID = MEMORY



62.10017.X41

1st = 62.10024.G21

2nd = 62.10017.X41

3rd = 62.10017.M51

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 15 of 103

(Blanking)

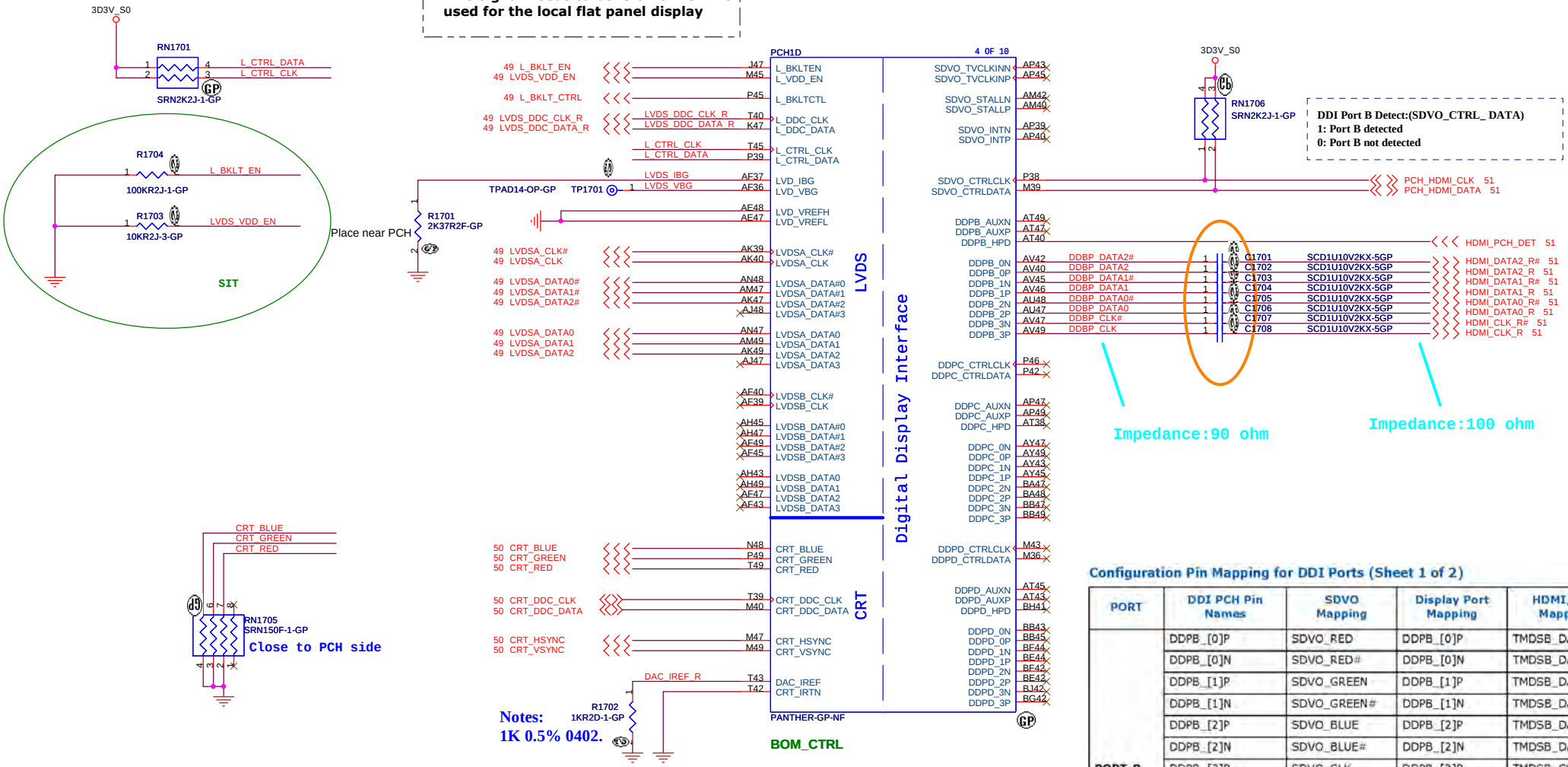
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR3-SODIMM3	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 16 of 103	

WWW.AliSaler.Com

L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

JV10-CS

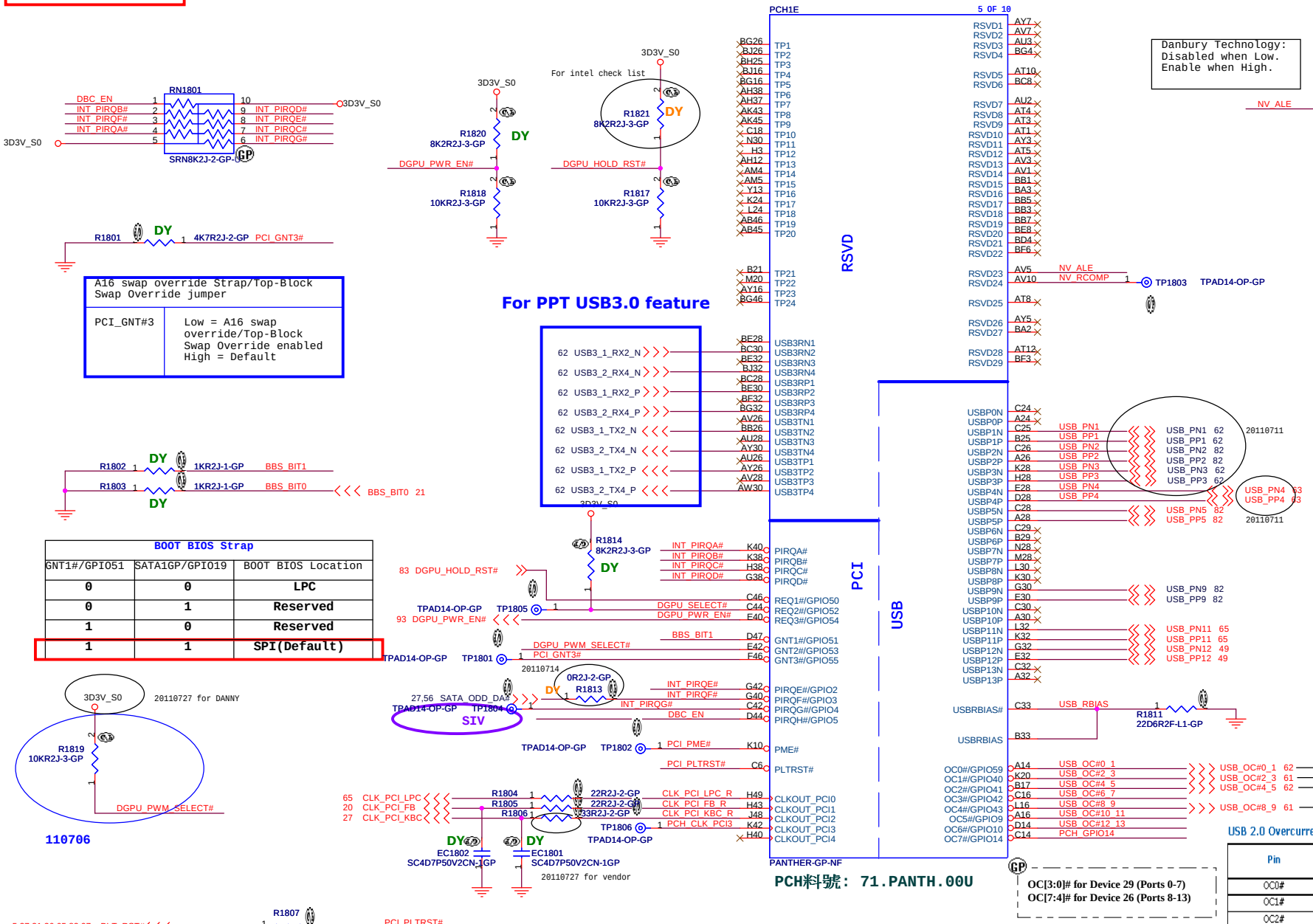
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/HDMI)**

Size | Document Number: **G48/G58** | Rev: **SC**

Date: Friday, February 17, 2012 | Sheet 17 of 103

SSID = PCH



USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

Utilize Port 9 for USB debug

USB3.0 port1
USB2.0 port4
USB3.0 port2
USB2.0 port3

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

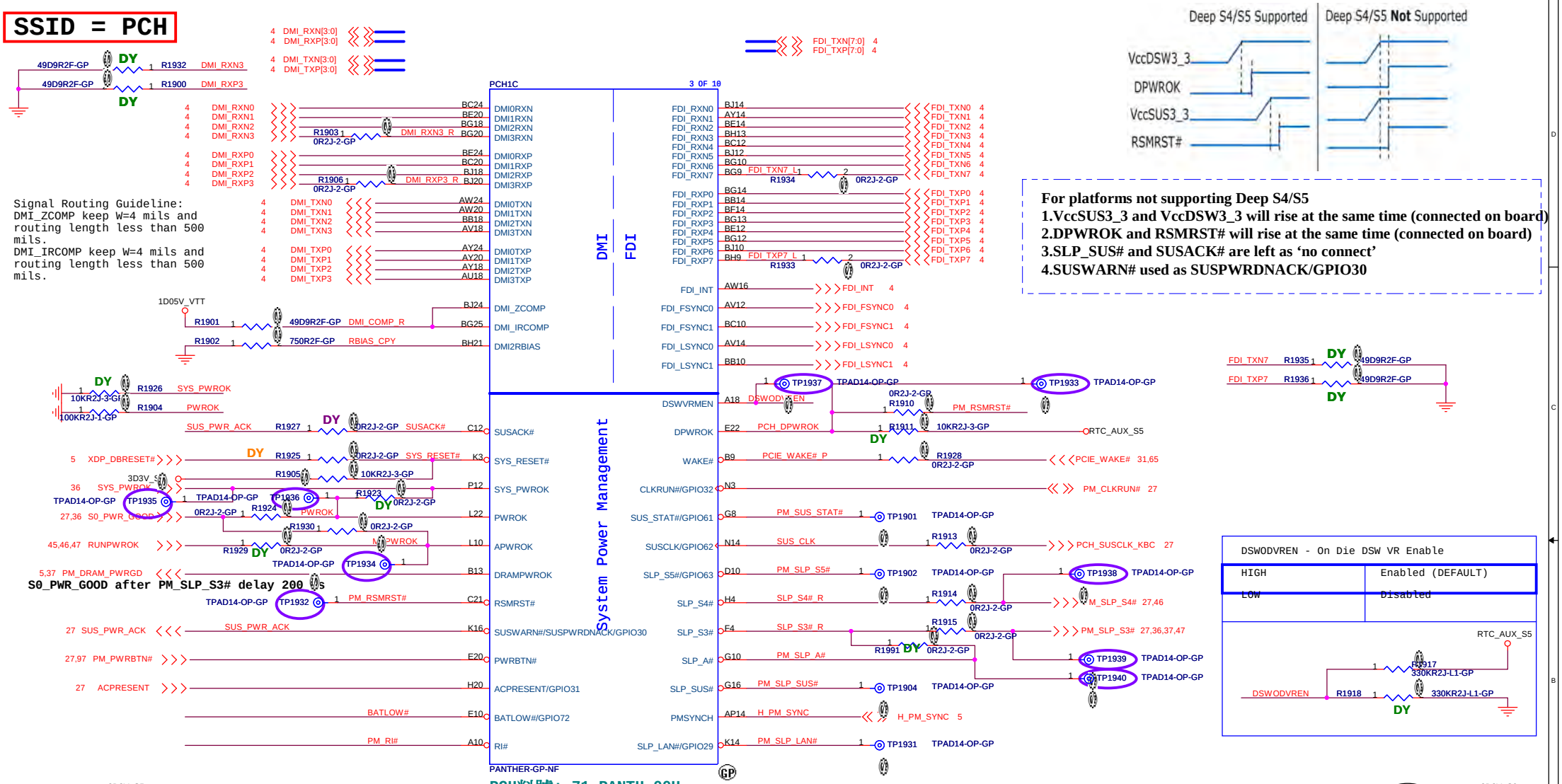
Title: PCH (PCI/USB/NVRAM)

Size | Document Number: G48/G58 | Rev: SC

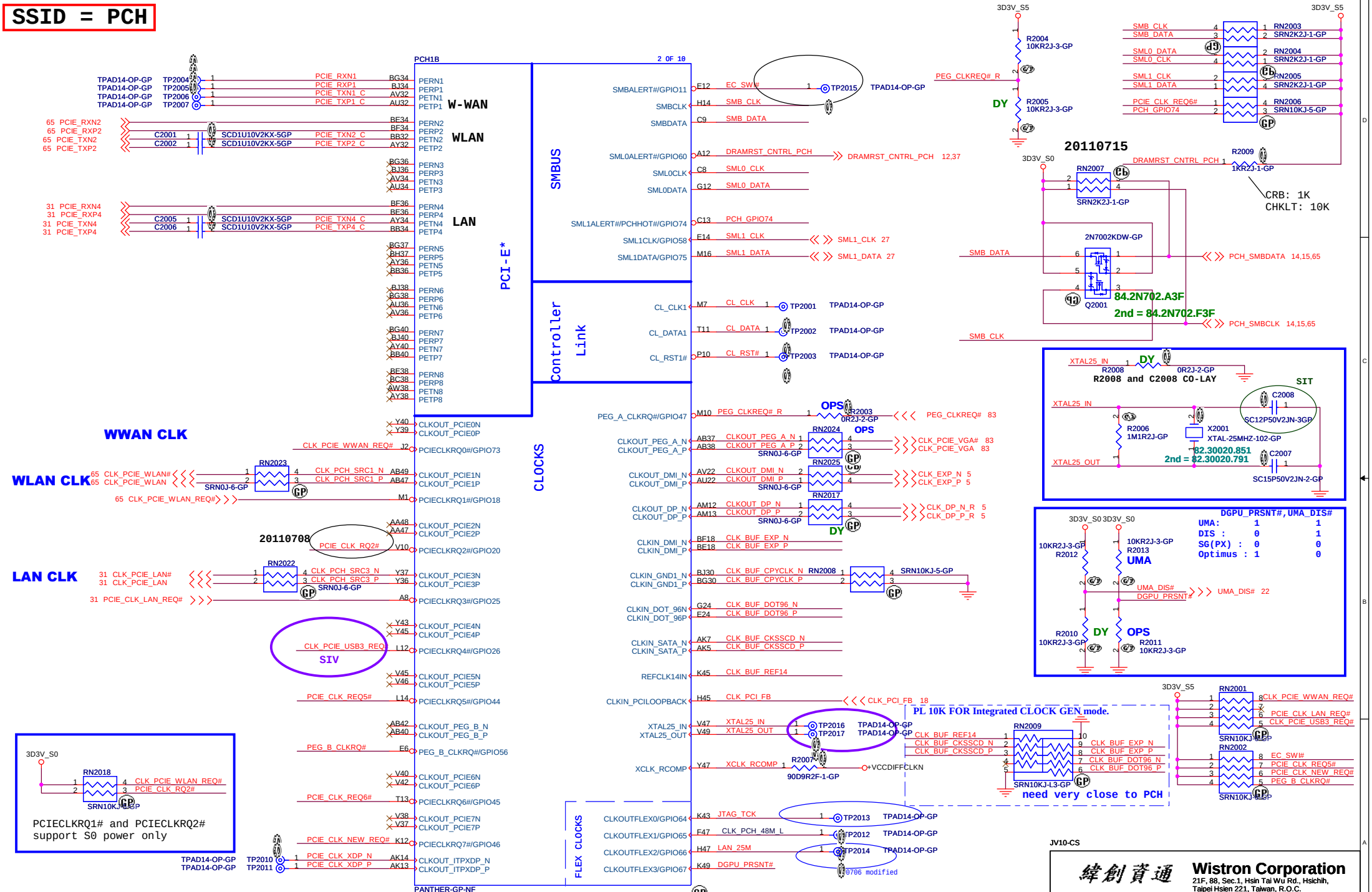
Date: Friday, February 17, 2012 | Sheet 18 of 103

WWW.AliSaler.Com

SSID = PCH


PCH1C
3 OF 10
DMI
FDI
System Power Management
PANTHER-GP-NF
DMI0RXN
DMI1RXN
DMI2RXN
DMI3RXN
DMI0RXP
DMI1RXP
DMI2RXP
DMI3RXP
DMI0TXN
DMI1TXN
DMI2TXN
DMI3TXN
DMI0TXP
DMI1TXP
DMI2TXP
DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
DMI2RBIAS
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
DSWVRMEN
DPWROK
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
Deep S4/S5 Supported
Deep S4/S5 Not Supported
VccDSW3_3
DPWROK
VccSUS3_3
RSMRST#
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.
S0_PWR_GOOD after PM_SLP_S3# delay 200 s
PCH料號: 71.PANTH.00U
DSWODVREN - On Die DSW VR Enable
HIGH Enabled (DEFAULT)
LOW Disabled
PCH_WAKE#
CRB : 1K
CHKLIST: 10K
SIV
SIV For intel
84.2N702.A3F
2nd = 84.2N702.F3F
20110728 for vendor
JV10-CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (DMI/FDI/PM)
Size
Document Number
G48/G58
Rev
SC
Date: Friday, February 17, 2012
Sheet 19 of 103

SSID = PCH



– Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
– Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

PCH料號: 71.PANTH.00U

WWW.AliSaler.Com

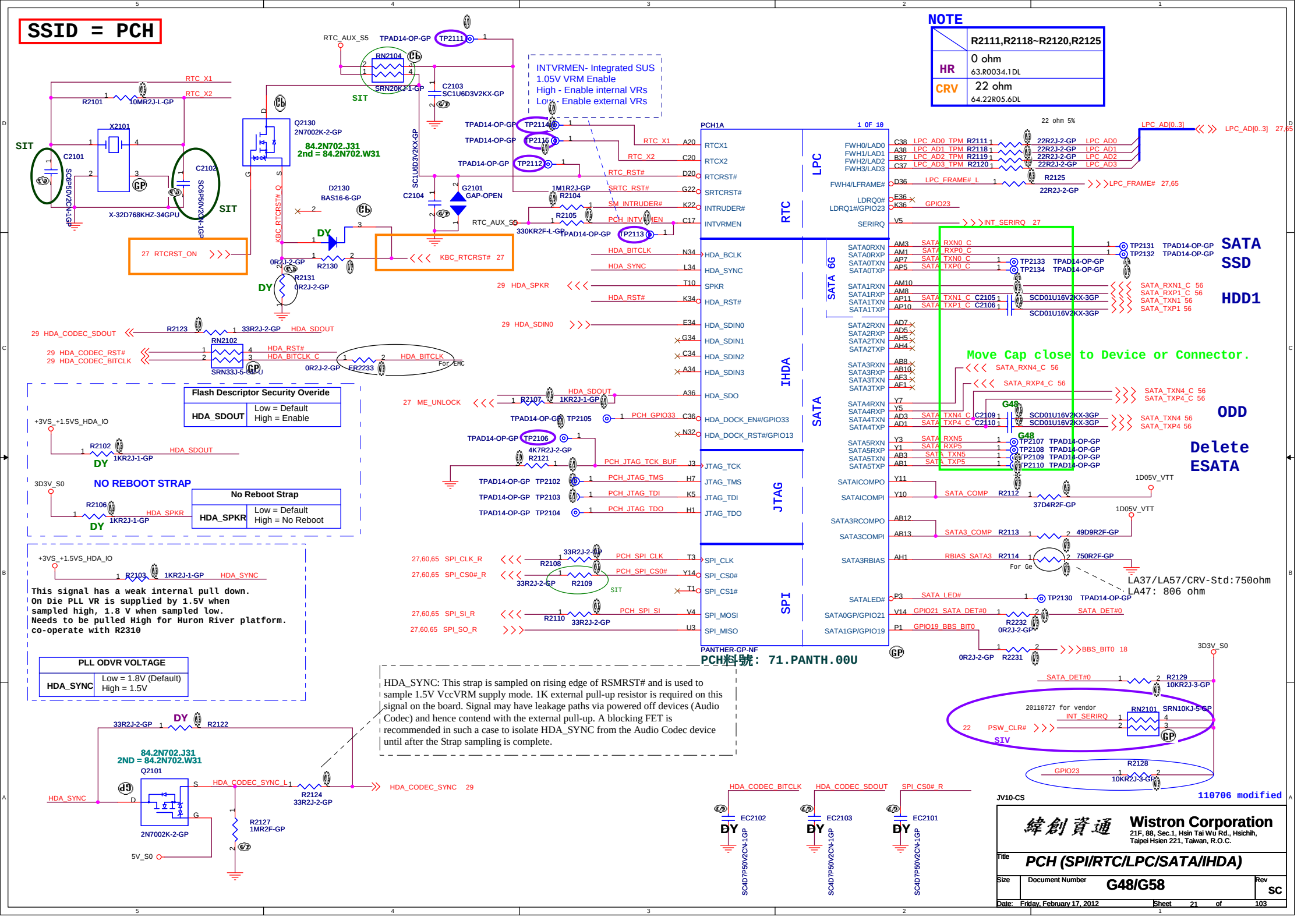
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 20 of 103


SSID = PCH
NOTE
R2111,R2118~R2120,R2125
HR
0 ohm
63.R0034.1DL
CRV
22 ohm
64.22R05.6DL
INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs
PCH1A
PANTHER-GP-NF
PCH料號: 71.PANTH.00U
RTC
LPC
IHDA
SATA
JTAG
SPI
SATA 6G
SATA SSD
HDD1
ODD
Delete ESATA
Move Cap close to Device or Connector.
LA37/LA57/CRV-Std:750ohm
LA47: 806 ohm
Flash Descriptor Security Overide
HDA_SDOUT
Low = Default
High = Enable
NO REBOOT STRAP
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310
PLL ODVR VOLTAGE
HDA_SYNC
Low = 1.8V (Default)
High = 1.5V
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.
84.2N702.J31
2nd = 84.2N702.W31
Q2130
2N7002K-2-GP
Q2101
2N7002K-2-GP
X2101
X-32D768KHZ-34GPU
SIT
DY
SIV
110706 modified
JV10-CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (SPI/RTC/LPC/SATA/IHDA)
Size
Document Number
G48/G58
Rev
SC
Date: Friday, February 17, 2012
Sheet 21 of 103

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — SIV — R2202 200KR2F-L-GP — SATA_ODD_PRSNT# — 110706 modified

3D3V_S0 — RN2203 SRN10KJ-5-GP — DY — 20110728 for Vendor — H_A20GATE, H_RCIN#

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

PCH_GPIO15 — R2233 100KR2J-1-GP — DY — SVT

LOW: ODD exist
HIGH: ODD non-exist

Note

	R2202	----
HR	200K ohm 64.20035.6DL	
CRB	10K ohm 63.10334.1DL	

PCH_GPIO15 pull high => HM76
PCH_GPIO15 pull Low => HM70

PCH_GPIO24 — R2234 100KR2J-1-GP — DY — SVT

3D3V_S5 — R2225 10KR2J-3-GP

21 PSW_CLR# — SIV

GAP-OPEN — G2201

3D3V_S0

RN2201 SRN10KJ-5-GP: DGPU_HPD_INTR#, EC_SMI#

RN2202 SRN10KJ-5-GP: PCH_GPIO48, S_GPIO, EC_SCI#, PCH_GPIO22

RN2204 SRN10KJ-5-GP: PCH_TEMP_ALERT#, MFG_MODE — SIV

3D3V_S0 — 110706 modified — R2230 10KR2J-3-GP — NC_FP_DET# — R2220 10KR2J-3-GP — DY

NC_FP_DET# => Low: FP exist
High: FP non-exist

3D3V_S5

RTC_DET# — R2229 100KR2J-1-GP — SIT

PCH_GPIO24 — R2227 10KR2J-3-GP

SVT — 10K ohm for intel check list command

PCH_GPIO15 — R2201 1KR2J-1-GP

PLL_ODVR_EN — R2226 10KR2J-3-GP

USB3_PWR_ON — R2228 10KR2J-3-GP — 20110717 — DY

3D3V_S0 — R2214 10KR2J-3-GP, R2216 10KR2J-3-GP — check remove? — VRAM_SIZE1, VRAM_SIZE2

PCH1F — 6 OF 10 — PANTHER-GP-NF

GPIO

Signal	Pin
BMBUSY#/GPIO0	T7
TACH1/GPIO1	A42
TACH2/GPIO6	H36
TACH3/GPIO7	E38
GPIO8	C10
LAN_PHY_PWR_CTRL/GPIO12	C4
GPIO15	G2
SATA4GP/GPIO16	U2
TACH0/GPIO17	D40
SCLOCK/GPIO22	T5
GPIO24	E8
GPIO27	E16
GPIO28	P8
STP_PCI#/GPIO34	K1
GPIO35	K4
SATA2GP/GPIO36	V8
SATA3GP/GPIO37	M5
SLOAD/GPIO38	N2
SDATAOUT0/GPIO39	M3
SDATAOUT1/GPIO48	V13
SATA5GP/GPIO49/TEMP_ALERT#	V3
GPIO57	D6

CPU/MISC

Signal	Pin
TACH4/GPIO68	C40
TACH5/GPIO69	B41
TACH6/GPIO70	C41
TACH7/GPIO71	A40
A20GATE	P4
PECI	AU16
RCIN#	P5
PROCPWRGD	AY11
THRMTRIP#	AY10
INIT3_3V#	T14
DF_TVS	AY1
TS_VSS1	AH8
TS_VSS2	AK11
TS_VSS3	AH10
TS_VSS4	AK10
NC_1	P37

NCTF

Signal	Pin
VSS_NCTF_15#BG2	BG2
VSS_NCTF_16#BG48	BG48
VSS_NCTF_17#BH3	BH3
VSS_NCTF_18#BH47	BH47
VSS_NCTF_19#BJ4	BJ4
VSS_NCTF_20#BJ44	BJ44
VSS_NCTF_21#BJ45	BJ45
VSS_NCTF_22#BJ46	BJ46
VSS_NCTF_23#BJ5	BJ5
VSS_NCTF_24#BJ6	BJ6
VSS_NCTF_25#C2	C2
VSS_NCTF_26#C48	C48
VSS_NCTF_27#D1	D1
VSS_NCTF_28#D49	D49
VSS_NCTF_29#E1	E1
VSS_NCTF_30#E49	E49
VSS_NCTF_31#F1	F1
VSS_NCTF_32#F49	F49
VSS_NCTF_1#A4	A4
VSS_NCTF_2#A44	A44
VSS_NCTF_3#A45	A45
VSS_NCTF_4#A46	A46
VSS_NCTF_5#A5	A5
VSS_NCTF_6#A6	A6
VSS_NCTF_7#B3	B3
VSS_NCTF_8#B47	B47
VSS_NCTF_9#BD1	BD1
VSS_NCTF_10#BD49	BD49
VSS_NCTF_11#BE1	BE1
VSS_NCTF_12#BE49	BE49
VSS_NCTF_13#BF1	BF1
VSS_NCTF_14#BF49	BF49

NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

SIV

S_GPIO — R2218 100R2J-2-GP — GPIO0
EC_SMI# — DGPU_HPD_INTR# — EC_SCI# — ICC_EN# — RTC_DET# — PCH_GPIO15 — PCH_GPIO16 — DGPU_PWROK — PCH_GPIO22 — PCH_GPIO24 — PCH_GPIO27 — PLL_ODVR_EN — PSW_CLR# — NC_FP_DET# — DMI_OVRVLTG — FDI_OVRVLTG — MFG_MODE — GFX_CRB_DET — PCH_GPIO48 — PCH_TEMP_ALERT# — USB3_PWR_ON

27 EC_SCI# — SIT
60 RTC_DET# >>>
56 SATA_ODD_PRSNT# — R2213 0R0402-PAD
92,93 DGPU_PWROK >>>

TPAD14-OP-GP TP2207 — TP2205 — TP2209 — TP2206 — TP2213 — TP2215 — TP2216 — TP2217 — TP2218 — TP2211 — TP2219 — TP2212

NCTF_3#A45 — NCTF_5#A5 — NCTF_7#B3 — NCTF_8#B47 — NCTF_9#BD1 — NCTF_10#BD49 — NCTF_13#BF1

TACH4/GPIO68 >>> SATA_ODD_PWRGT 56
TACH5/GPIO69 >>> UMA_DIS# — UMA_DIS# 20
TACH6/GPIO70 — VRAM_SIZE1
TACH7/GPIO71 — VRAM_SIZE2

A20GATE — H_A20GATE 27
PECI — H_PECI_R — R2203 0R2J-2-GP — DY — H_PECI 5,27
RCIN# — H_RCIN# 27
PROCPWRGD >>> H_CPUPWRGD 5,36,97
THRMTRIP# — PCH_THERMTRIP_R — R2204 390R2J-1-GP — H_THERMTRIP# 5,36
INIT3_3V# — INIT3_3V# — TP2201 TPAD14-OP-GP
DF_TVS — NV_CLE
TS_VSS1, TS_VSS2, TS_VSS3, TS_VSS4 — TS_VSS — R2219 0R2J-2-GP
NC_1
VSS_NCTF_16#BG48 — NCTF_16#BG48 — TP2221 TPAD14-OP-GP
VSS_NCTF_25#C2 — NCTF_25#C2 — TP2230 TPAD14-OP-GP
VSS_NCTF_26#C48 — NCTF_26#C48 — TP2231 TPAD14-OP-GP
VSS_NCTF_31#F1 — NCTF_31#F1 — TP2236 TPAD14-OP-GP

PCH料號: 71.PANTH.00U

3D3V_S0 — R2205 10KR2J-3-GP — DY — Check — GFX_CRB_DET — R2206 100KR2J-1-GP

1D8V_S0 — R1808 2K2R2J-2-GP — R1812 1KR2J-1-GP — NV_CLE — R2221 0R2J-2-GP — H_SNB_IVB# 5

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — R2212 1KR2J-1-GP — DY

3D3V_S0 — R2209 10KR2J-3-GP — DY — DMI_OVRVLTG — R2210 10KR2J-3-GP

3D3V_S0 — R2207 10KR2J-3-GP — DY — FDI_OVRVLTG — R2208 10KR2J-3-GP

ICC_EN# — R2211 1KR2J-1-GP — DY

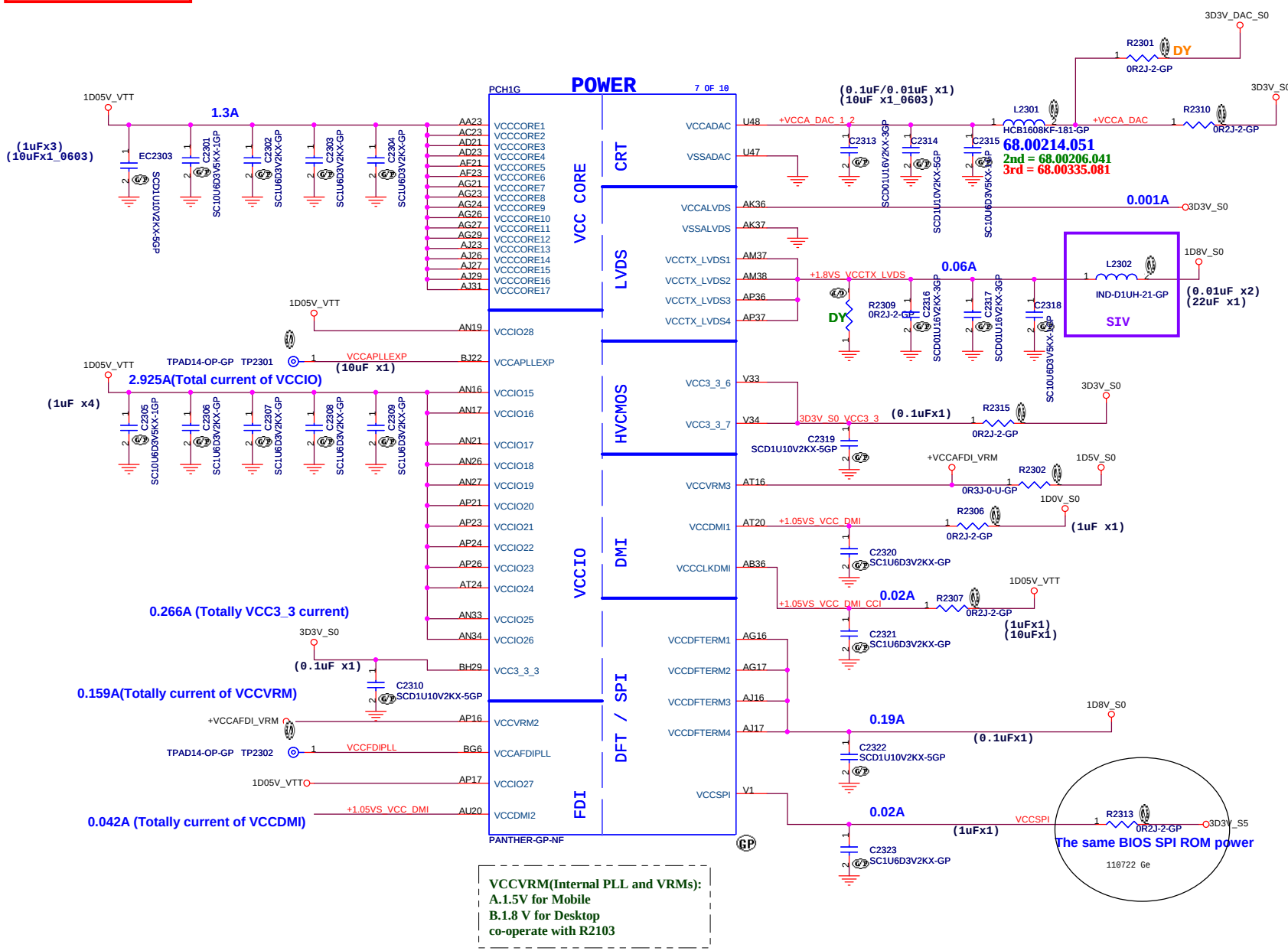
JV10-CS

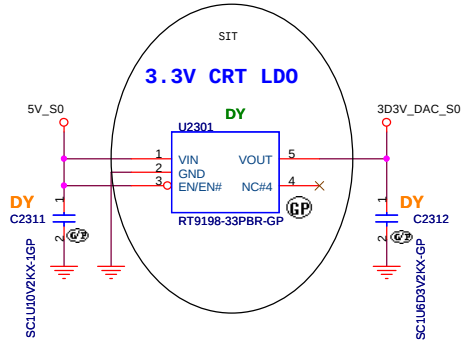
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)
Size: Document Number: G48/G58 Rev: SC
Date: Friday, February 17, 2012 Sheet 22 of 103

WWW.AliSaler.Com

SSID = PCH 6A





Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture

VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with R2103

JV10-CS

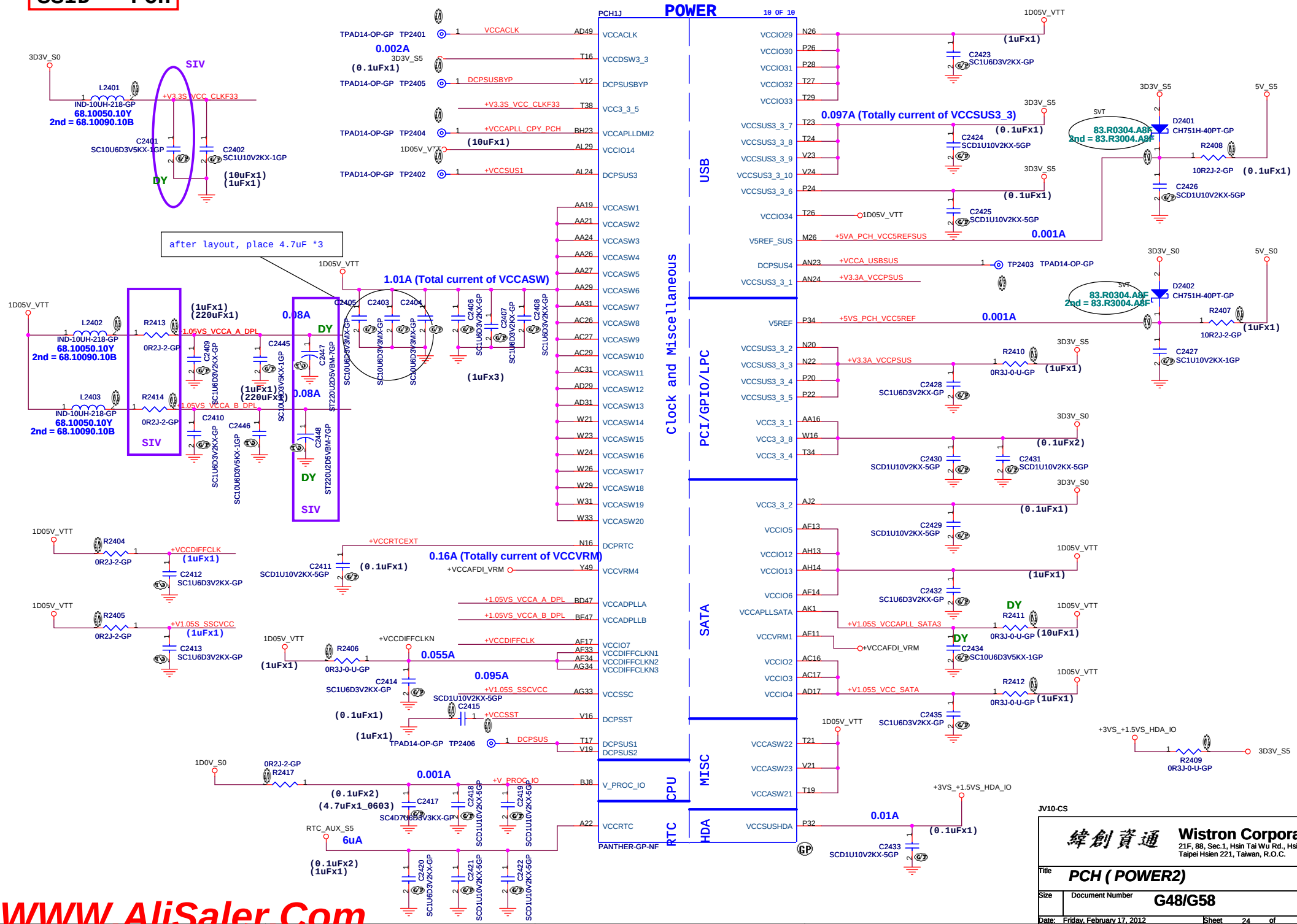
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 23 of 103

SSID = PCH



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

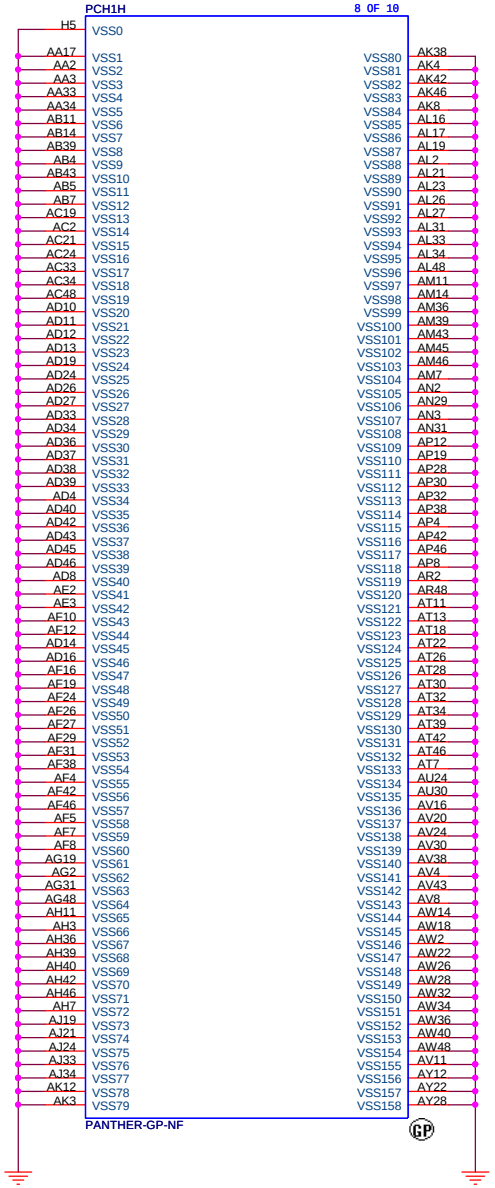
Title: PCH (POWER2)

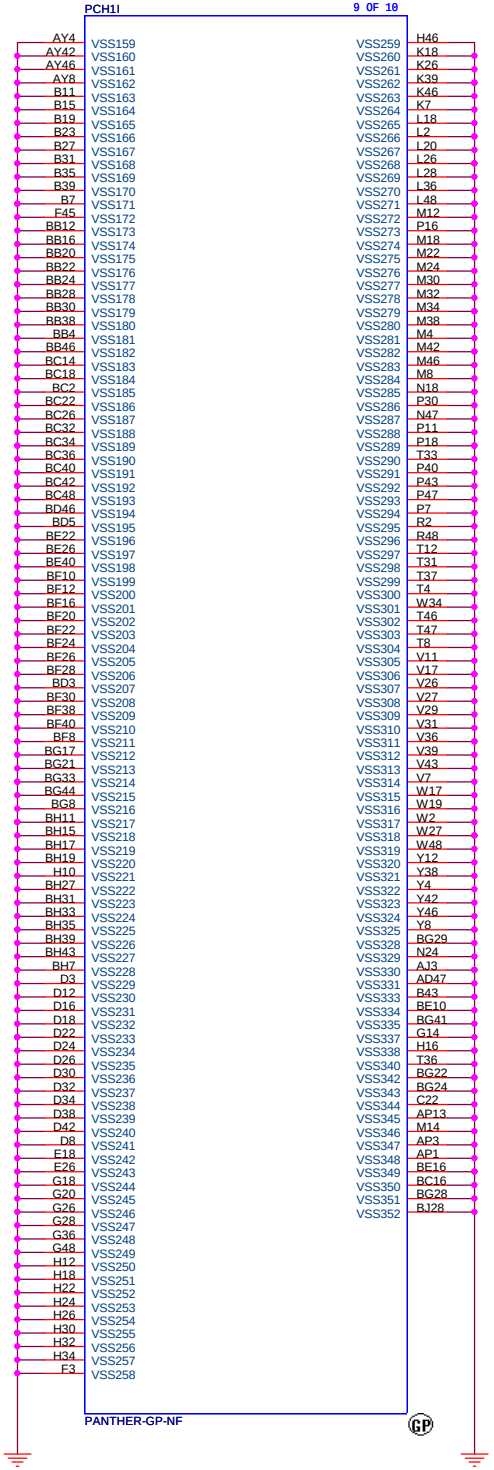
Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 24 of 103

WWW.AliSaler.Com

SSID = PCH





JV10-CS

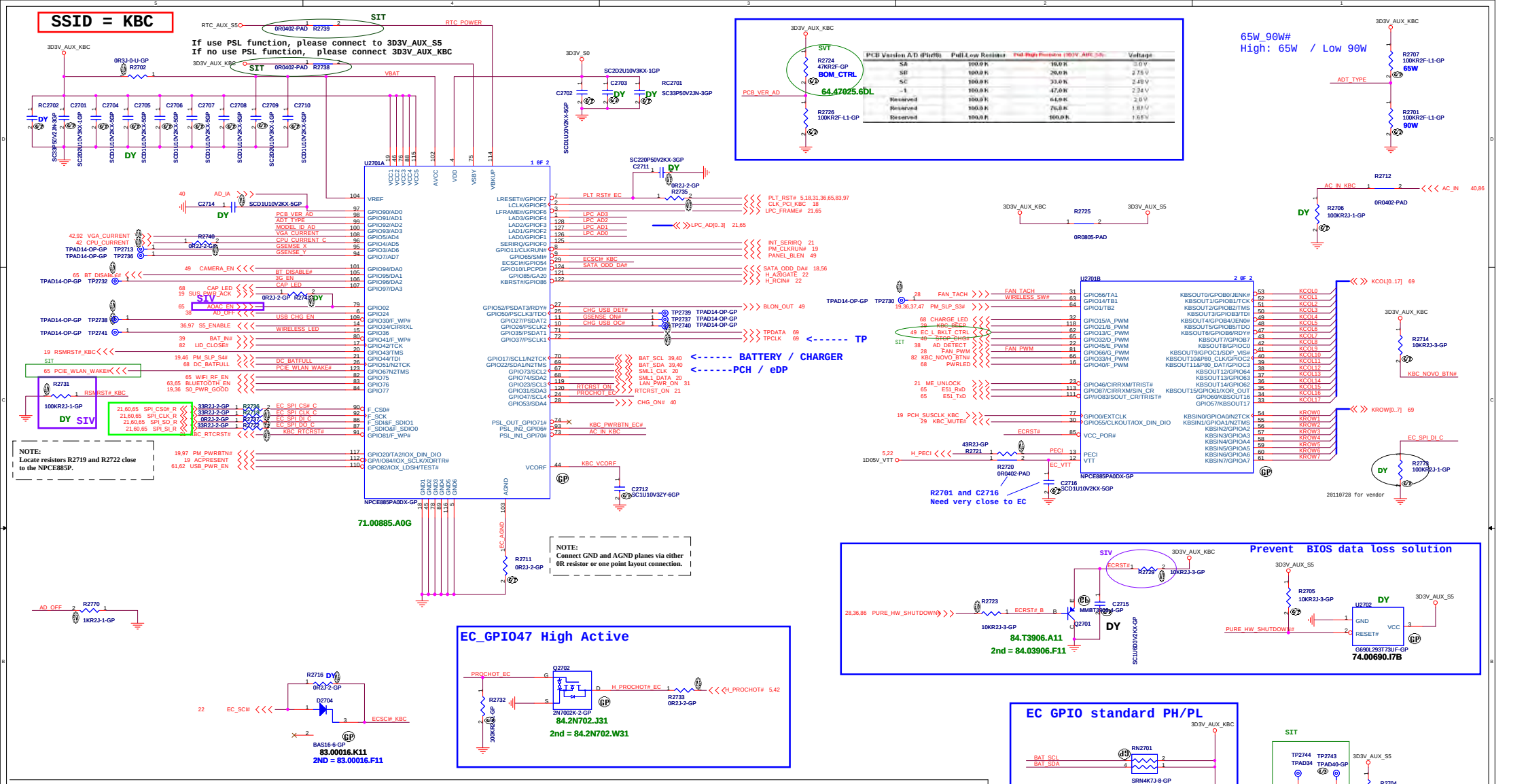
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (VSS)***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 25 of 103	

(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***Reserved***		
Size	Document Number **G48/G58**		Rev **SC**
Date: Friday, February 17, 2012		Sheet 26 of 103	

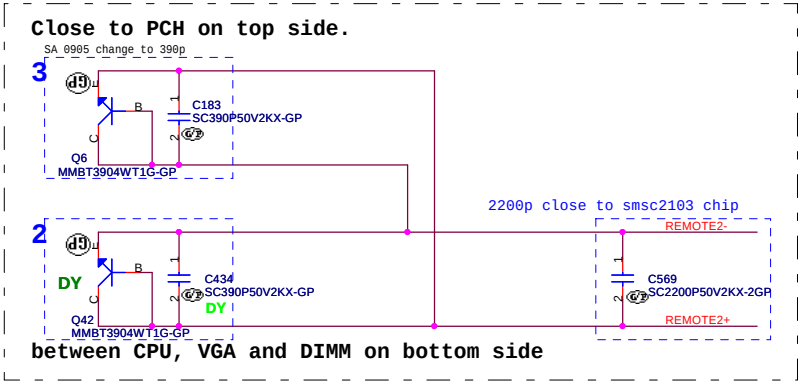
WWW.AliSaler.Com

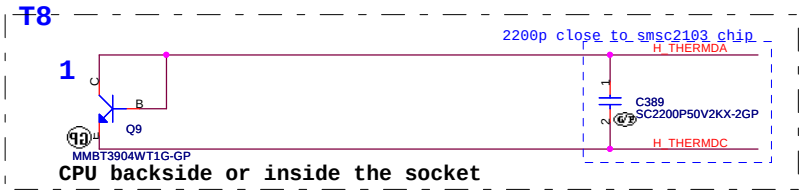


MODEL_ID_AD (Pin100)	Pull-Low Register	Pull-High Register	Voltage	
LG48 UMA	100.0 K	10.0 K	3.000 V	64.10025.6DL
LG48 OPTIMUS	100.0 K	20.0 K	2.750 V	64.20025.6DL
LG58 UMA	100.0 K	33.0 K	2.481 V	64.33025.6DL
LG58 OPTIMUS	100.0 K	47.0 K	2.245 V	64.47025.6DL

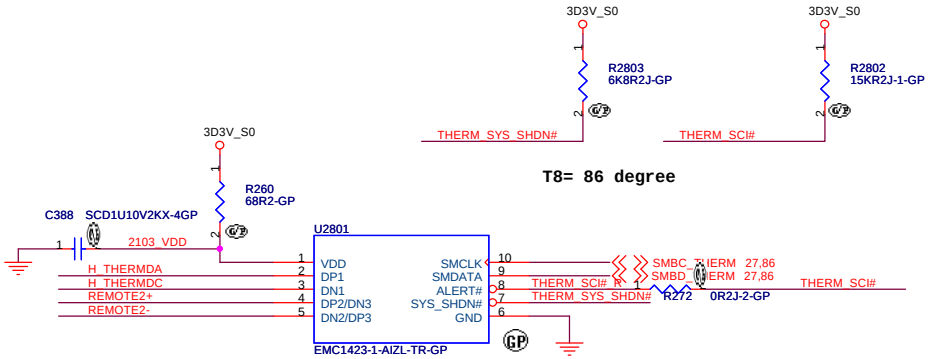
SSID = Thermal

Thermal sensor

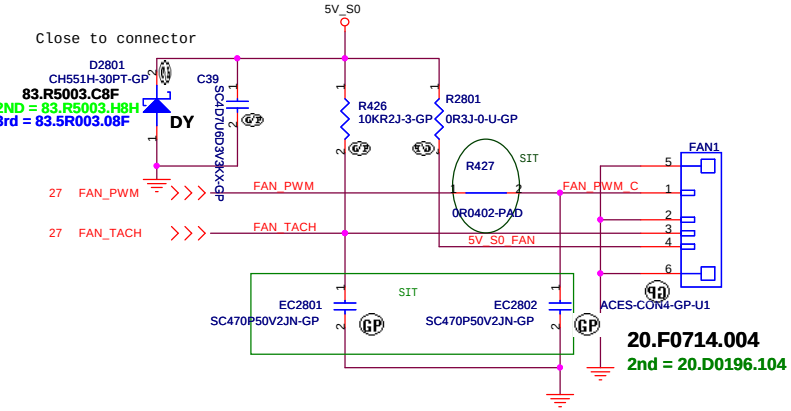


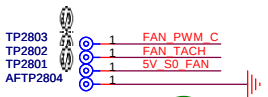


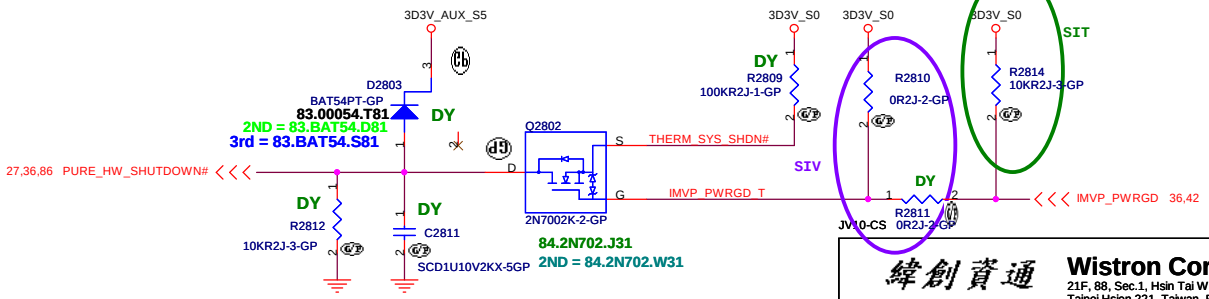
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.



4 WIRE PWM Fan Control circuit

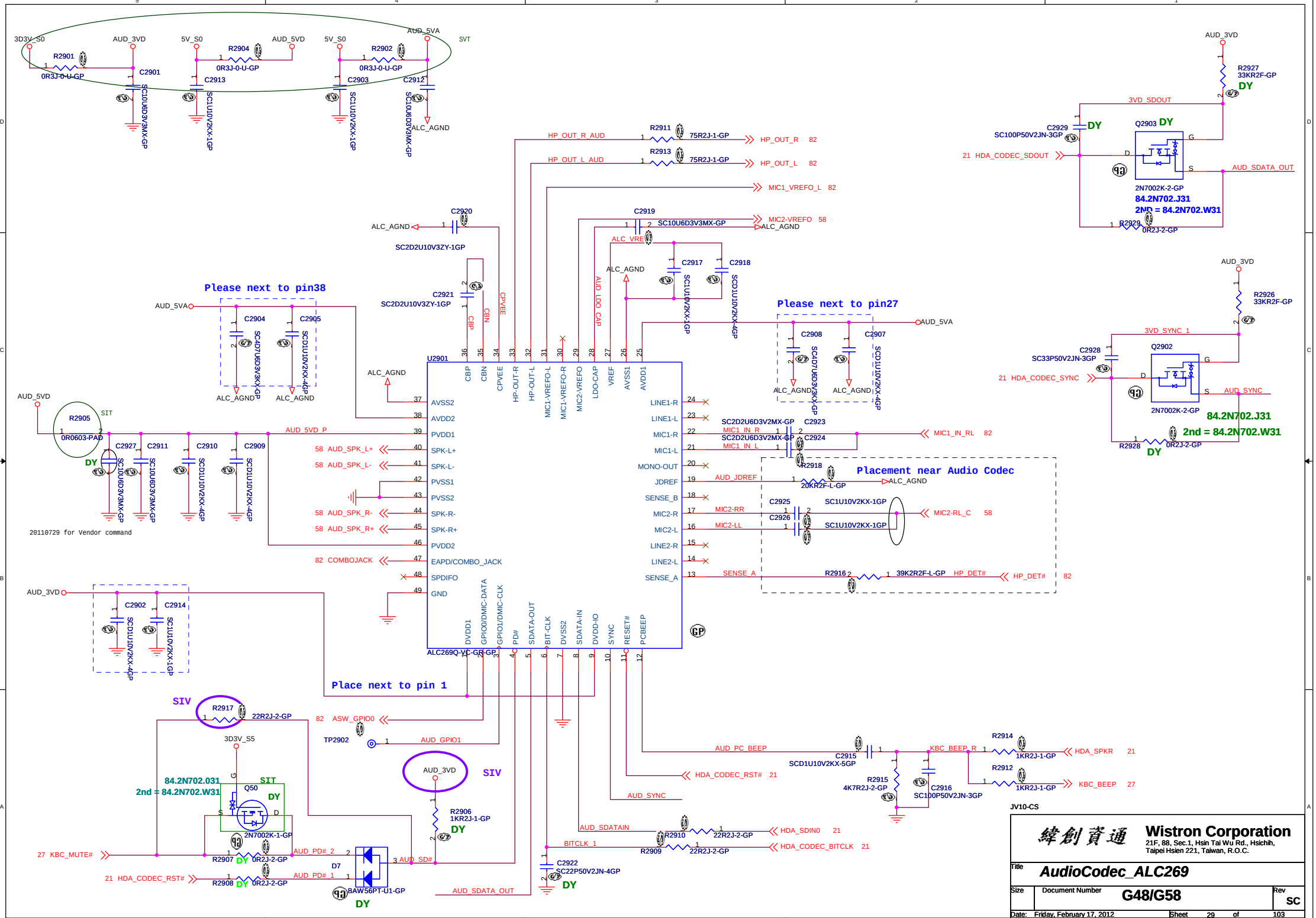






緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	THERMAL EMC1423
Size / Document Number	G48/G58
Rev	SC
Date: Friday, February 17, 2012	Sheet 28 of 103

WWW.AliSaler.Com


3D3V_S0
AUD_3VD
5V_S0
AUD_5VD
AUD_5VA
SVT
R2901
0R3J-0-U-GP
C2901
SC10U6D3V3MX-GP
R2904
0R3J-0-U-GP
C2913
SC1U10V2KX-1GP
R2902
0R3J-0-U-GP
C2903
C2912
ALC_AGND
HP_OUT_R_AUD
R2911
75R2J-1-GP
HP_OUT_R 82
HP_OUT_L_AUD
R2913
75R2J-1-GP
HP_OUT_L 82
MIC1_VREFO_L 82
C2920
SC2D2U10V3ZY-1GP
C2919
SC10U6D3V3MX-GP
MIC2-VREFO 58
ALC_VRE
C2917
C2918
SC1U10V2KX-1GP
SC1U10V2KX-4GP
Please next to pin38
C2921
SC2D2U10V3ZY-1GP
C2904
C2905
SC4D7U6D3V3KX-GP
SC1U10V2KX-4GP
Please next to pin27
C2908
C2907
U2901
ALC269Q-VC-GR-GP
AVSS2
AVDD2
PVDD1
SPK-L+
SPK-L-
PVSS1
PVSS2
SPK-R-
SPK-R+
PVDD2
EAPD/COMBO_JACK
SPDIFO
GND
LINE1-R
LINE1-L
MIC1-R
MIC1-L
MONO-OUT
JDREF
SENSE_B
MIC2-R
MIC2-L
LINE2-R
LINE2-L
SENSE_A
CBP
CBN
CPVEE
HP-OUT-R
HP-OUT-L
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
LDO-CAP
VREF
AVSS1
AVDD1
DVDD1
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PD#
SDATA-OUT
BIT-CLK
DVSS2
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
AUD_5VD_P
58 AUD_SPK_L+
58 AUD_SPK_L-
58 AUD_SPK_R-
58 AUD_SPK_R+
82 COMBOJACK
MIC1_IN_R
MIC1_IN_L
SC2D2U6D3V2MX-GP
C2923
C2924
MIC1_IN_RL 82
R2918
20KR2F-L-GP
AUD_JDREF
Placement near Audio Codec
C2925
C2926
SC1U10V2KX-1GP
MIC2-RR
MIC2-LL
MIC2-RL_C 58
R2916
39K2R2F-L-GP
HP_DET#
HP_DET# 82
R2905
0R0603-PAD
SIT
DY
C2927
C2911
C2910
C2909
SC10U6D3V3MX-GP
SC1U10V2KX-4GP
20110729 for Vendor command
C2902
C2914
SC1U10V2KX-4GP
SC1U10V2KX-1GP
Place next to pin 1
SIV
R2917
22R2J-2-GP
82 ASW_GPIO0
TP2902
AUD_GPIO1
3D3V_S5
84.2N702.031
2nd = 84.2N702.W31
SIT
Q50
DY
2N7002K-1-GP
AUD_3VD
SIV
R2906
1KR2J-1-GP
DY
27 KBC_MUTE#
R2907
0R2J-2-GP
AUD_PD# 2
D7
BAW56PT-U1-GP
21 HDA_CODEC_RST#
R2908
0R2J-2-GP
AUD_PD# 1
AUD_SD#
AUD_SDATA_OUT
C2922
SC22P50V2JN-4GP
AUD_PC_BEEP
C2915
SCD1U10V2KX-5GP
KBC_BEEP_R
R2914
1KR2J-1-GP
HDA_SPKR 21
R2912
1KR2J-1-GP
KBC_BEEP 27
R2915
4K7R2J-2-GP
C2916
SC100P50V2JN-3GP
HDA_CODEC_RST# 21
AUD_SYNC
AUD_SDATAIN
R2910
22R2J-2-GP
HDA_SDIN0 21
BITCLK_1
R2909
22R2J-2-GP
HDA_CODEC_BITCLK 21
R2927
33KR2F-GP
3VD_SDOUT
C2929
SC100P50V2JN-3GP
Q2903
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.W31
21 HDA_CODEC_SDOUT
AUD_SDATA_OUT
R2929
0R2J-2-GP
R2926
33KR2F-GP
3VD_SYNC_1
C2928
SC33P50V2JN-3GP
Q2902
2N7002K-2-GP
21 HDA_CODEC_SYNC
AUD_SYNC
84.2N702.J31
2nd = 84.2N702.W31
R2928
0R2J-2-GP
JV10-CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AudioCodec_ALC269
Size
Document Number
G48/G58
Rev
SC
Date: Friday, February 17, 2012
Sheet 29 of 103

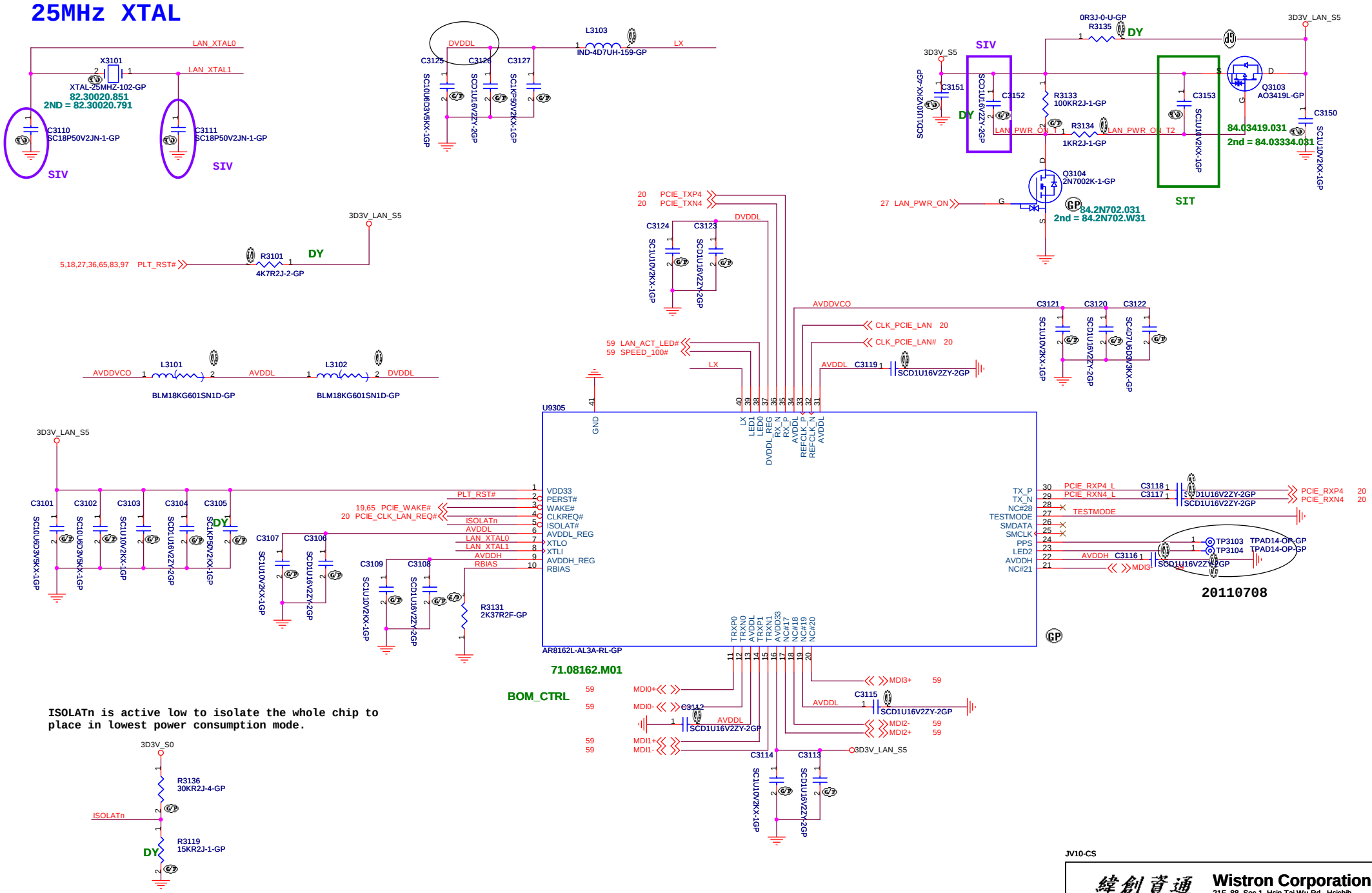
(Blanking)

JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Audio_AMP		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 30 of 103	

WWW.AliSaler.Com

25MHz XTAL



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LOM	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 31 of 103	

(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***Card reader***		
Size	Document Number **G48/G58**		Rev **SC**
Date: Friday, February 17, 2012		Sheet 32 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1394	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 33 of 103	

(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***Smart card***		
Size	Document Number **G48/G58**		Rev **SC**
Date: Friday, February 17, 2012		Sheet 34 of 103	

WWW.AliSaler.Com

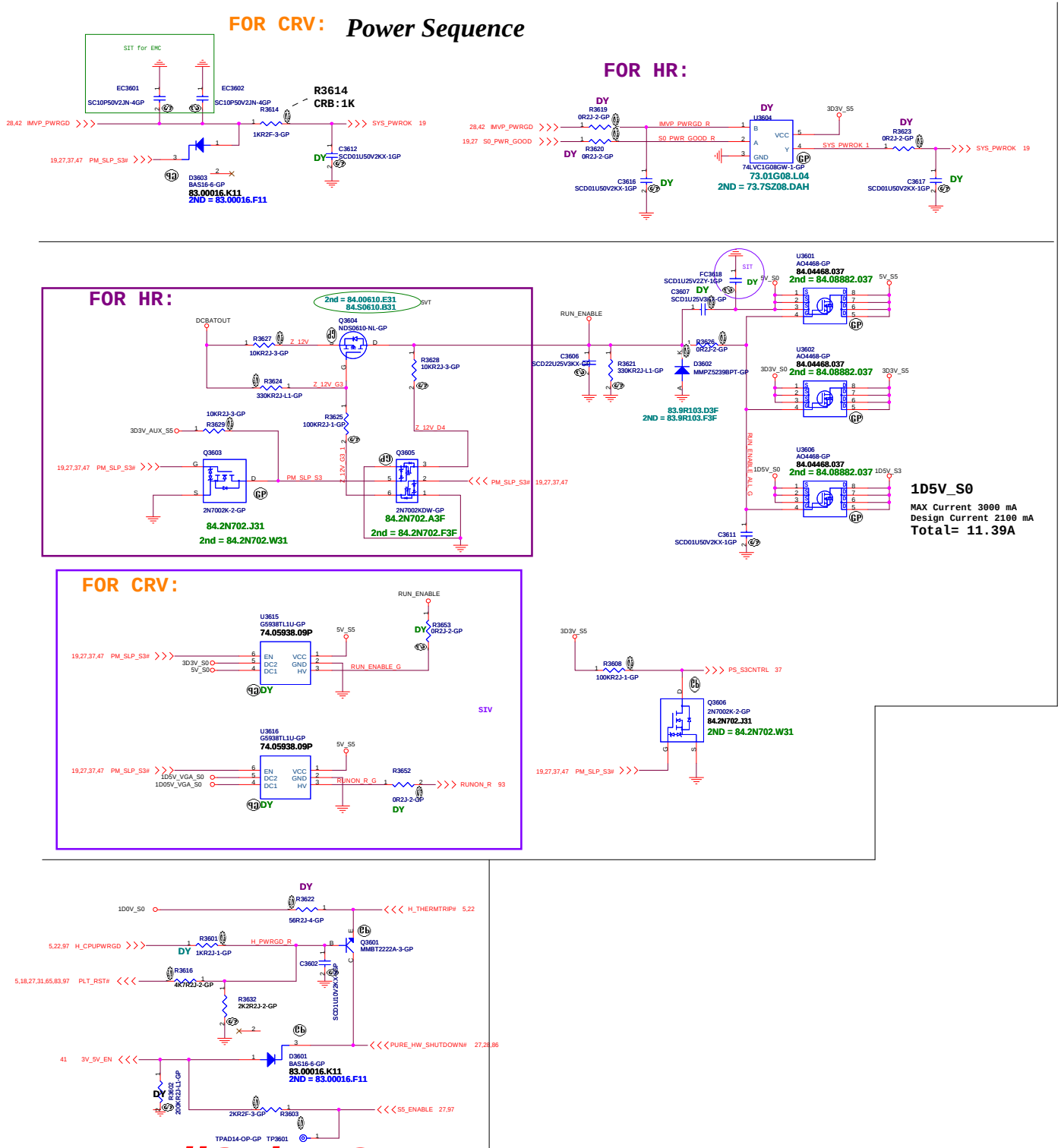
Reserved

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB 3.0 CONTROLLER		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 35 of 103	

Power Sequence

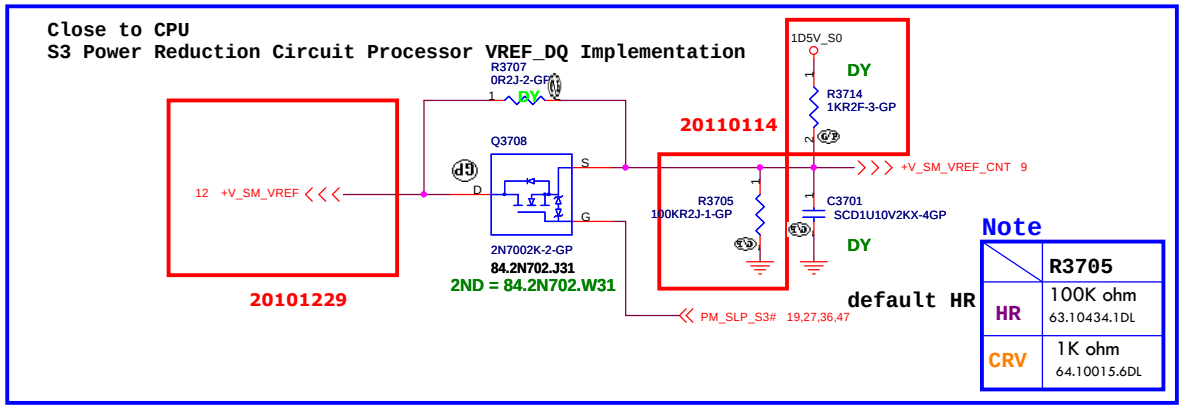


WWW.AliSaler.Com

JV10-CS

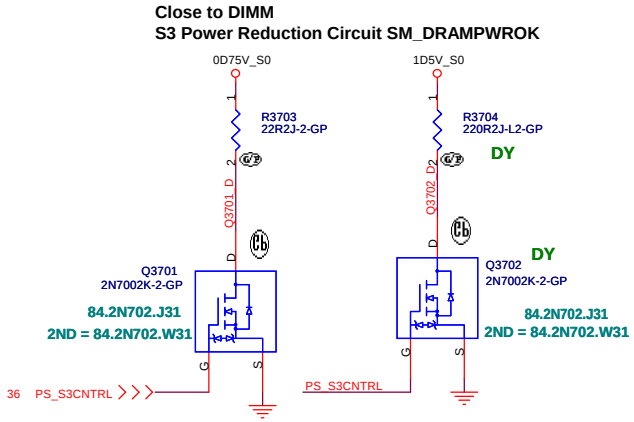
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

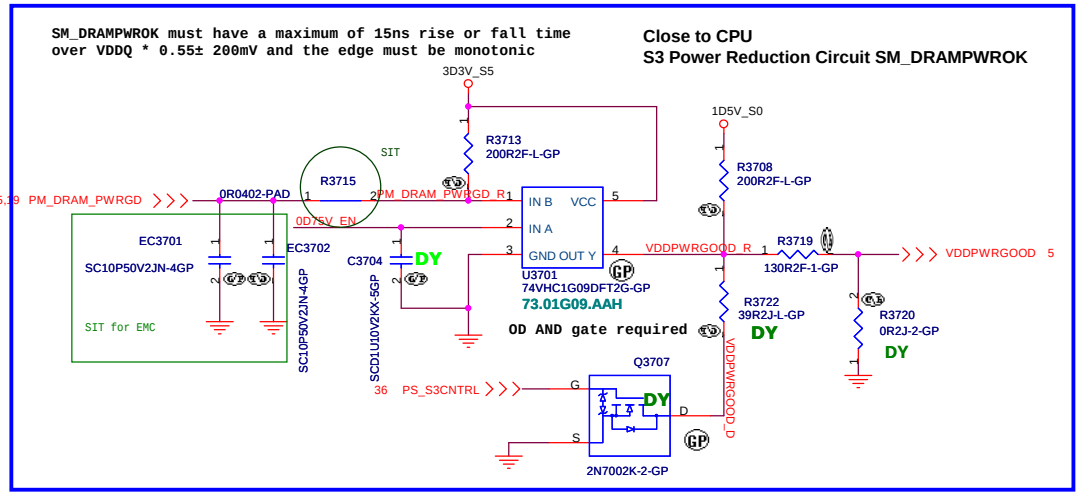
Title	PowerPlane Enable&Sequence	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 36 of 103	

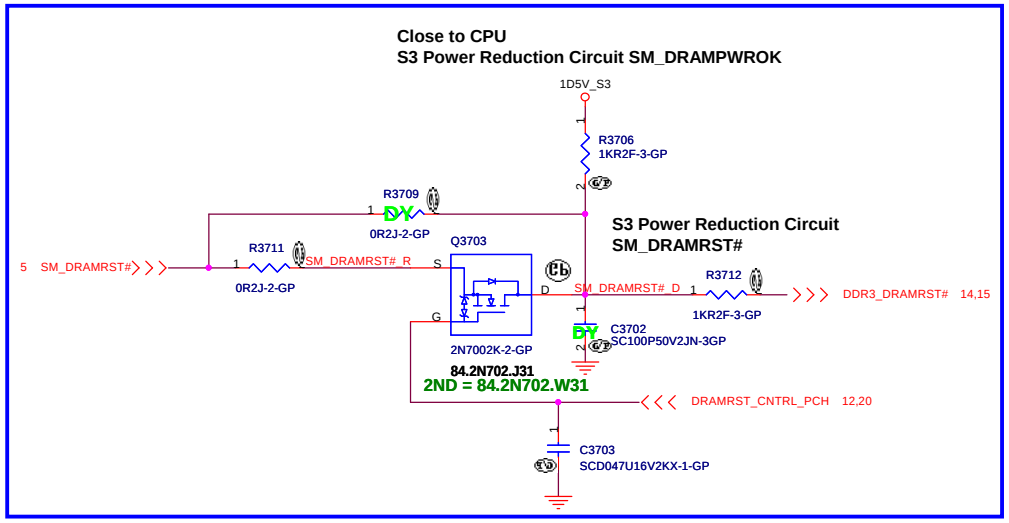


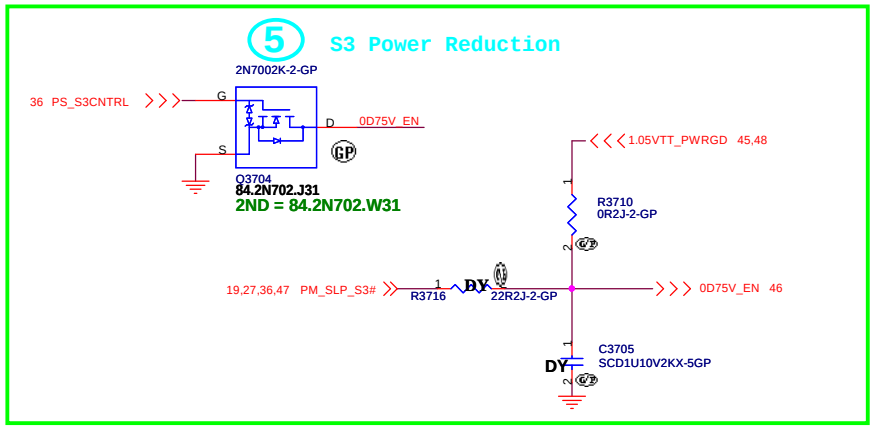
Note

	R3705
HR	100K ohm 63.10434.1DL
CRV	1K ohm 64.10015.6DL









JV10-CS

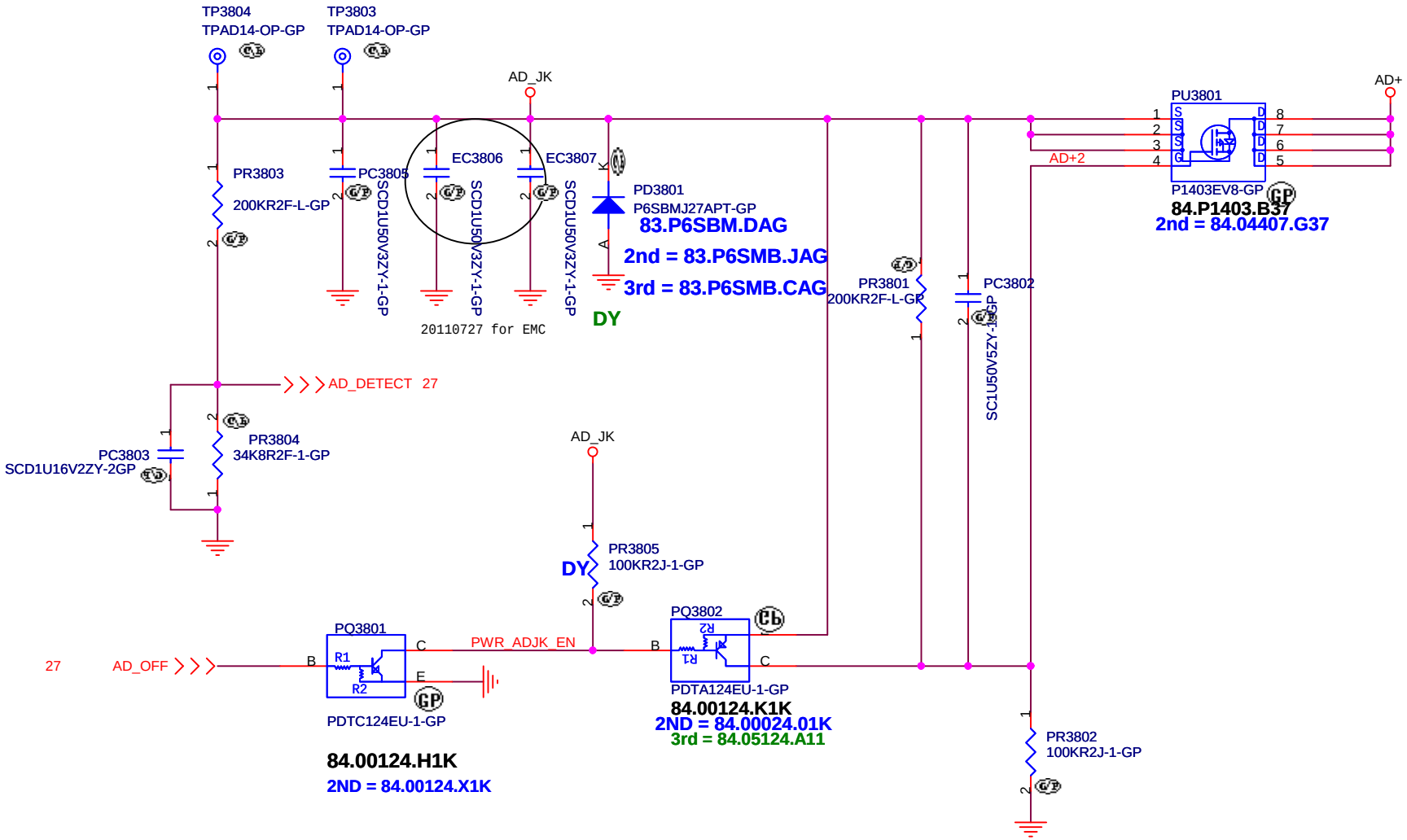
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ADAPTER OCP / S3 reduction***

Size | Document Number: **G48/G58** | Rev: **SC**

Date: Friday, February 17, 2012 | Sheet 37 of 103

Adaptor in to generate DCBATOUT

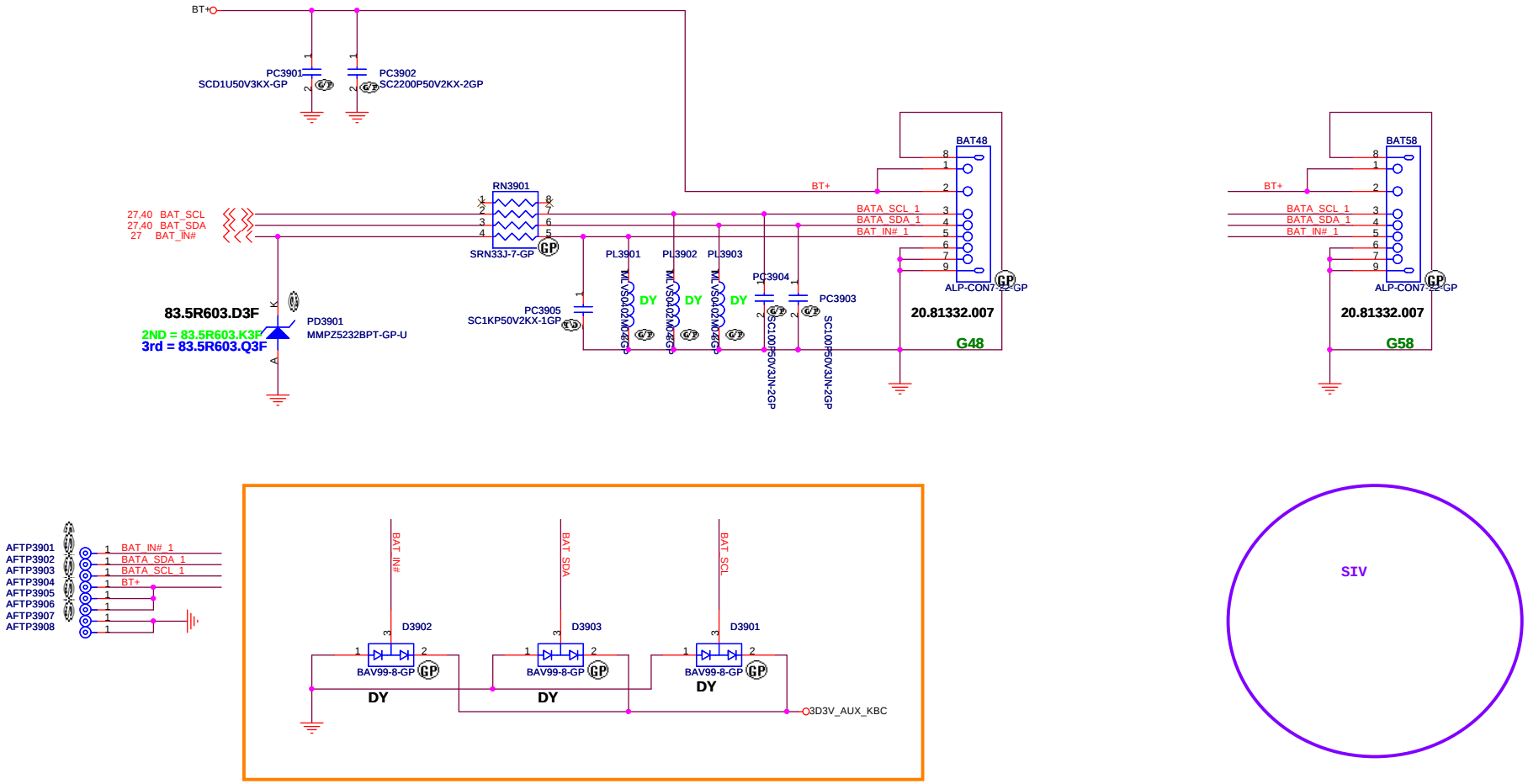


JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN JACK***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 38 of 103	

WWW.AliSaler.Com

BATTERY CONNECTOR



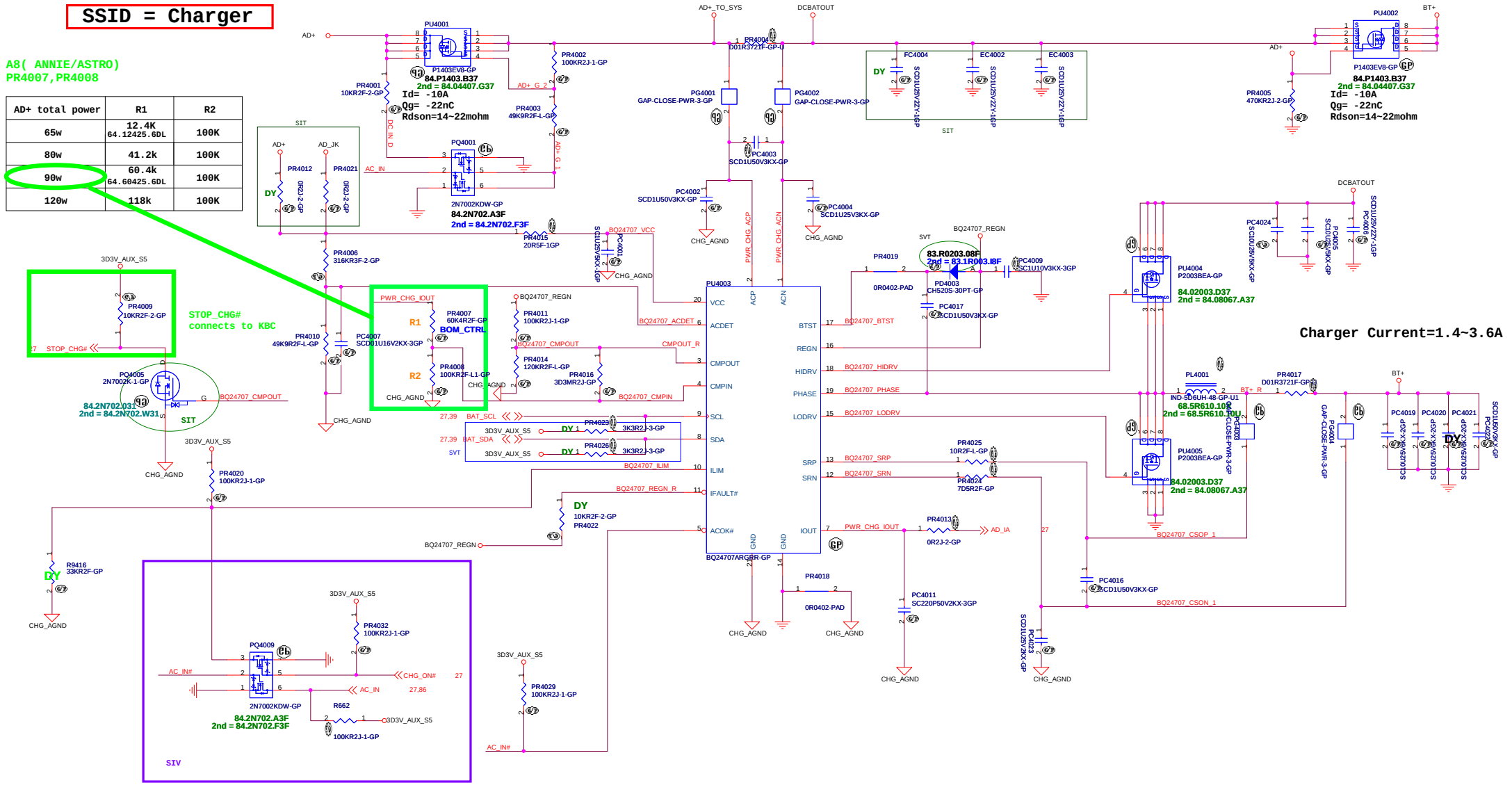
JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BATT CONN***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 39 of 103	

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118k	100K



JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

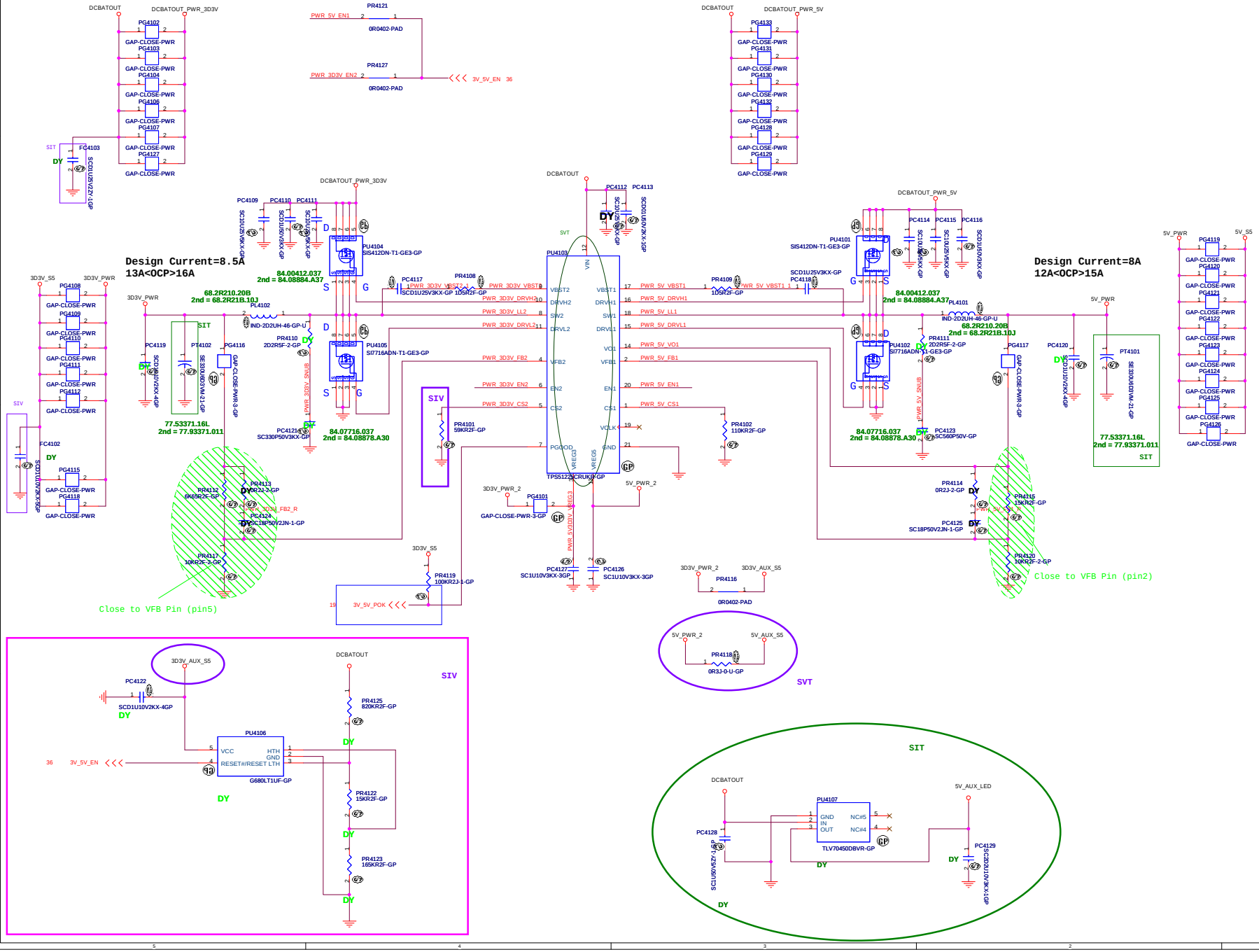
Title: BQ24745_Charger

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 40 of 103

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_5v3p3v



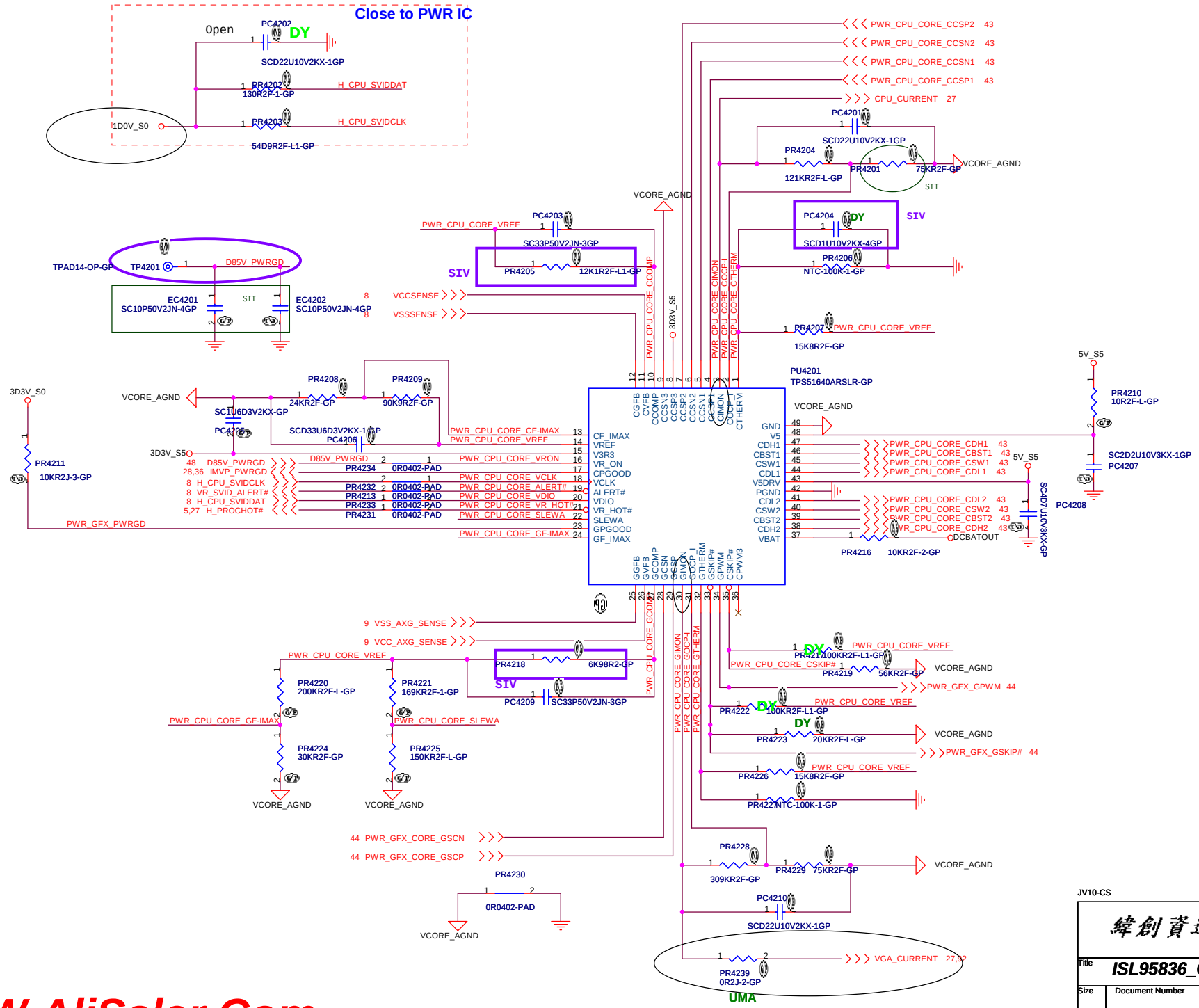
JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

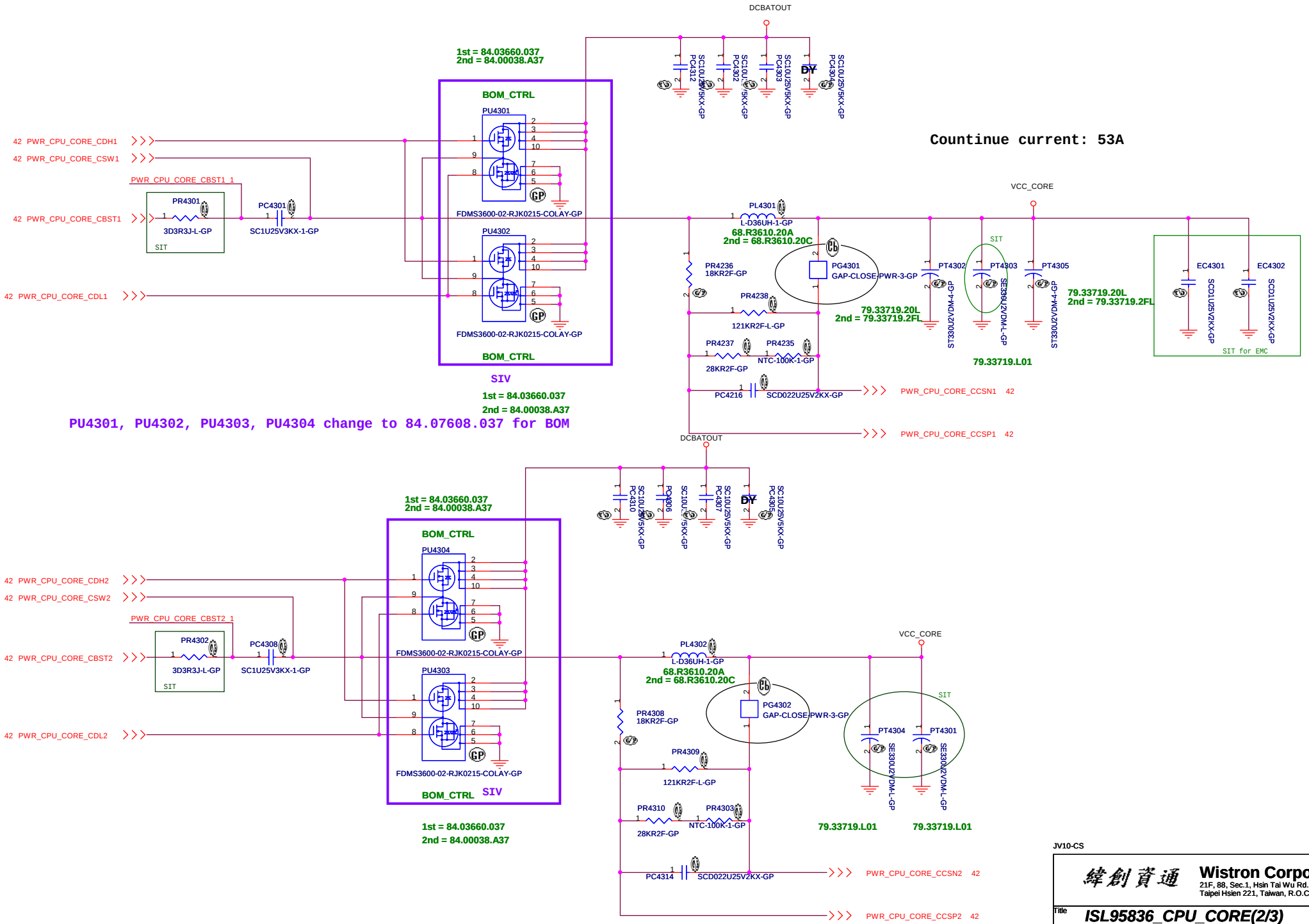
Title: TPS51123_5V_3D3V

Size: | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 41 of 103



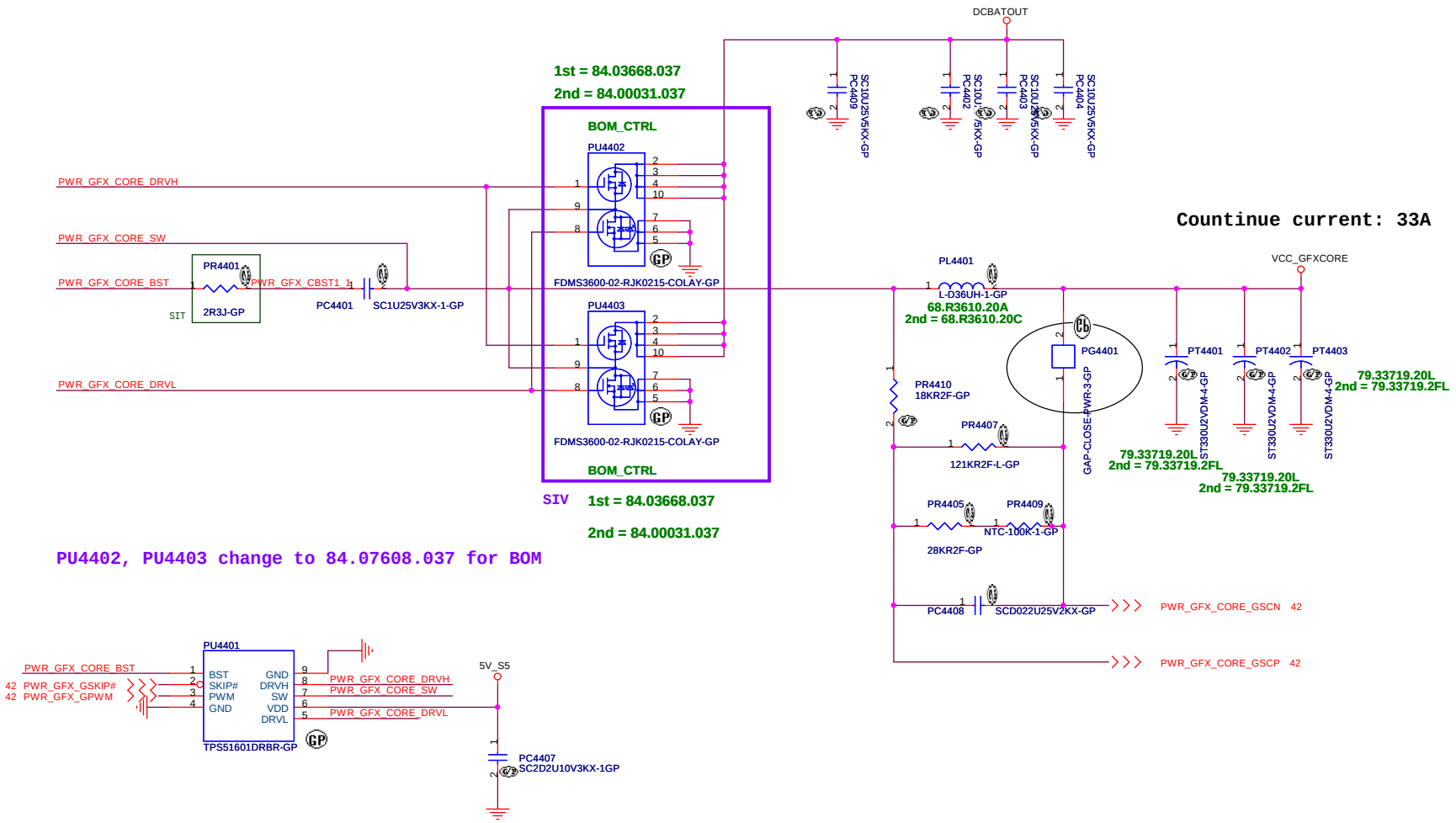
WWW.AliSaler.Com



JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*ISL95836_CPU_CORE(2/3)*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Monday, February 20, 2012	Sheet 43 of 103	

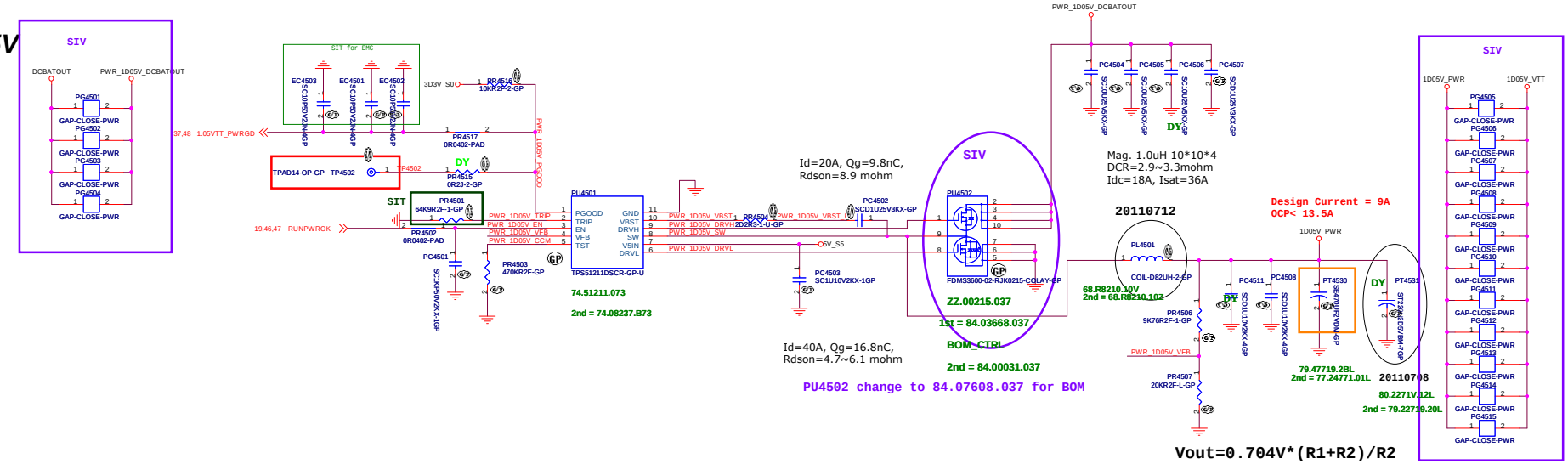


JV10-CS

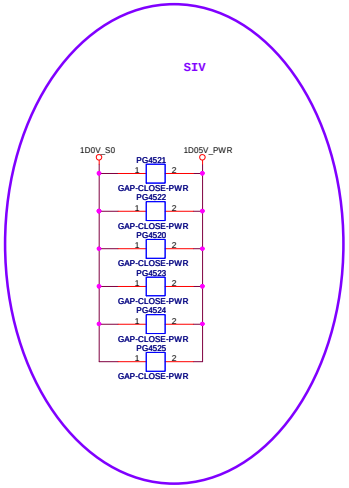
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL95836_CPU_CORE(3/3)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 44 of 103	

WWW.AliSaler.Com

TPS51211 for 1D05V



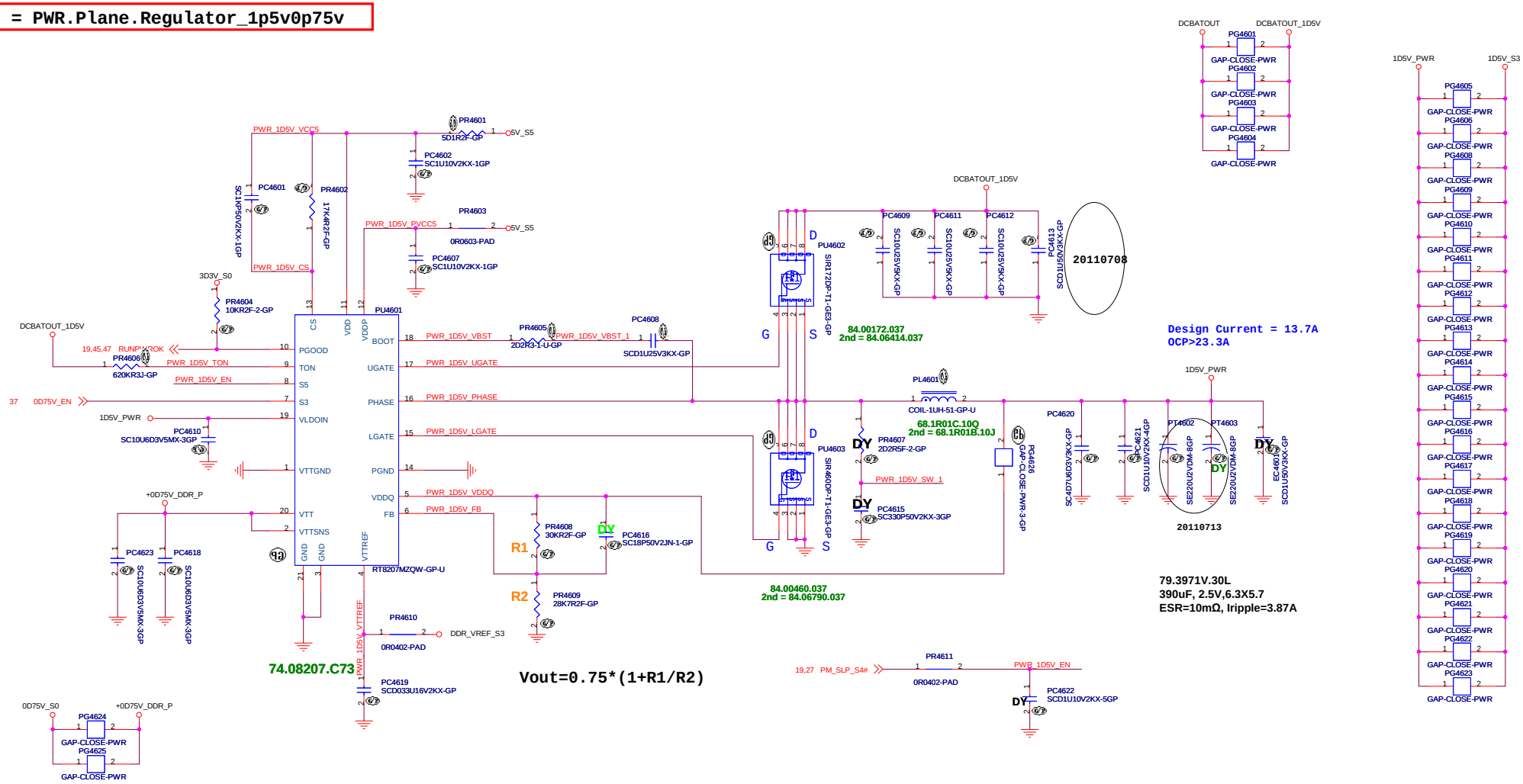
APL5916 for 1D0V



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	TPS51211_1D05V&TPS51219_1D0V	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 45 of 103	

SSID = PWR.Plane.Regulator_1p5v0p75v

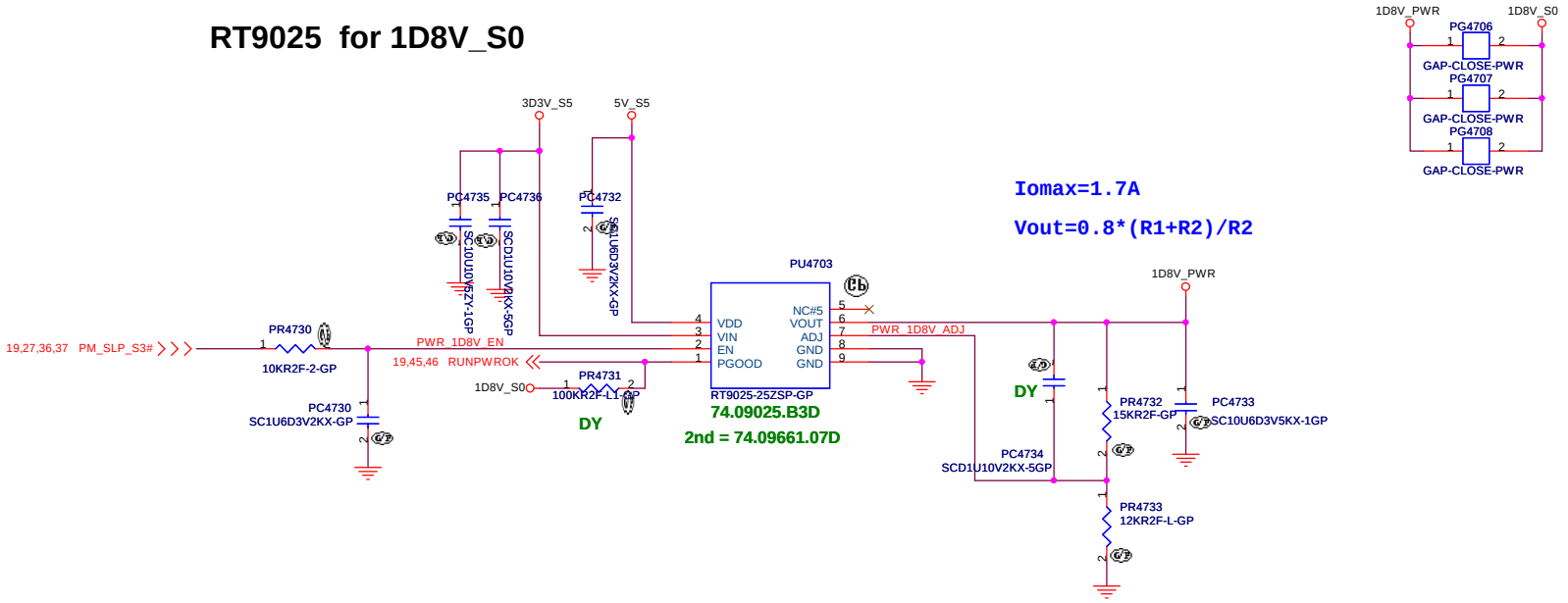


JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8207_1D5V_0D75V	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 46 of 103	

WWW.AliSaler.Com

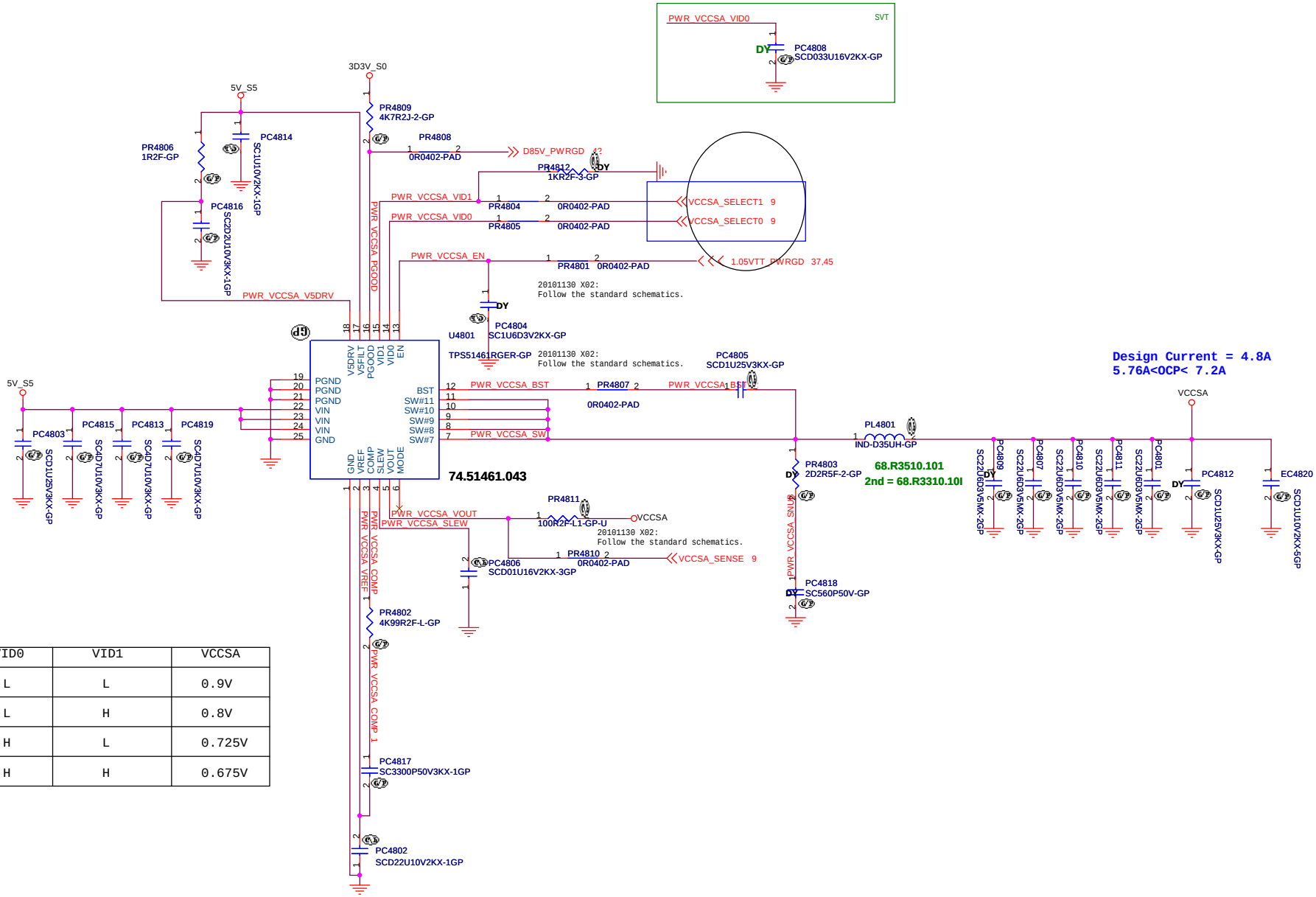
RT9025 for 1D8V_S0



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RT9205_1D8V***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 47 of 103	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

JV10-CS

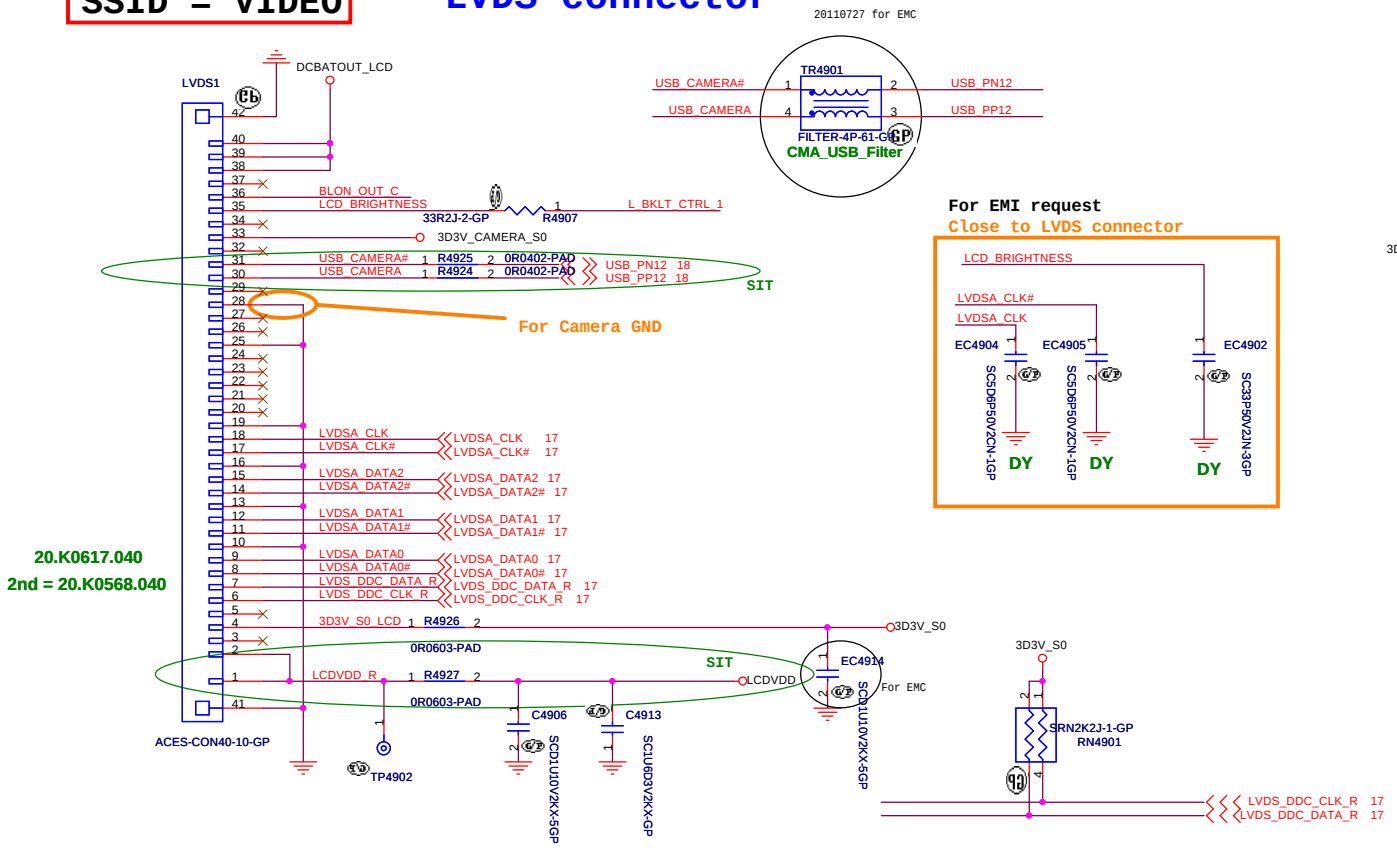
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA_TPS51461	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 48 of 103	

WWW.AliSaler.Com

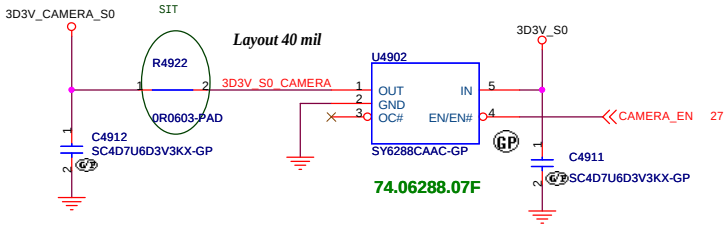
SSID = VIDEO

LVDS connector



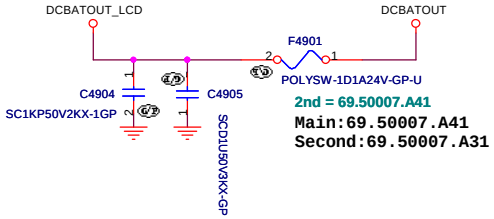
For EMI request
Close to LVDS connector

CAMERA POWER

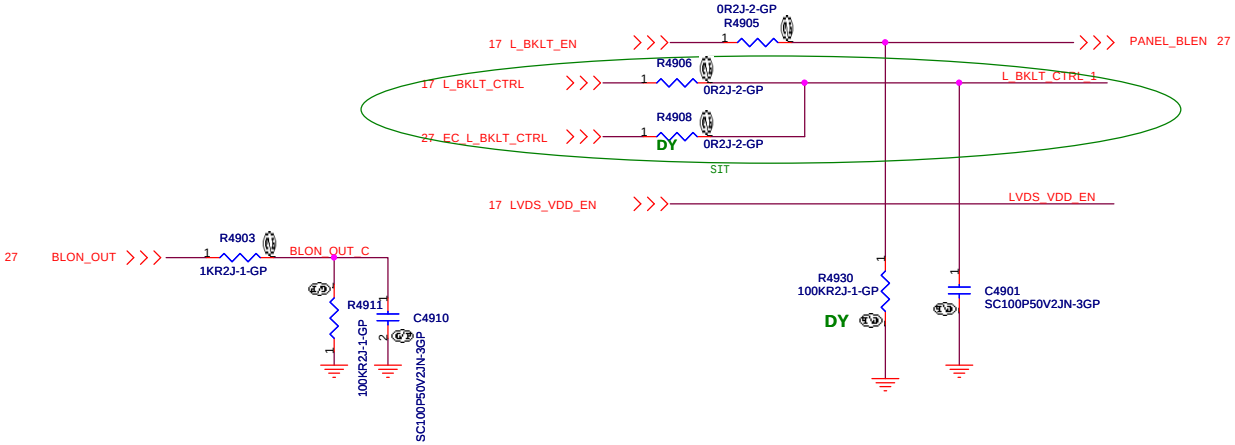


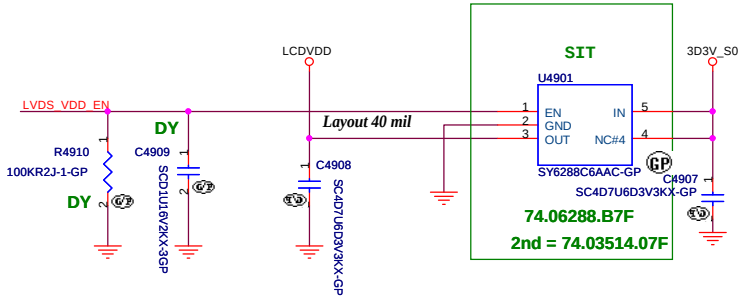
U4902 Change to 74.07534 from 74.05240.A7F for obsoleted part

LCD POWER



Panel BL brightness/Power En/BL En

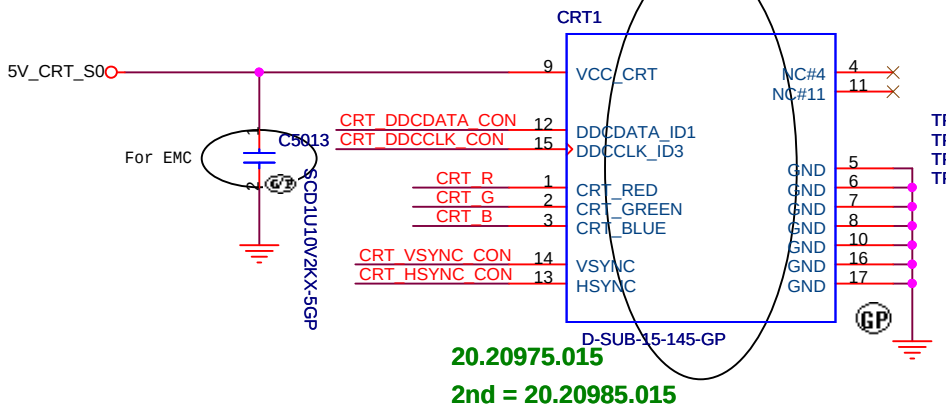


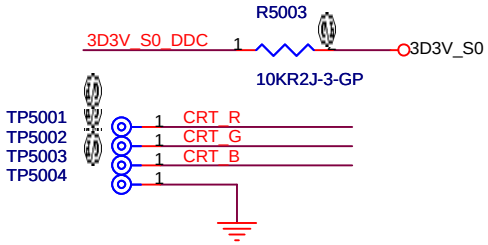


JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD/Inverter Connector	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 49 of 103	

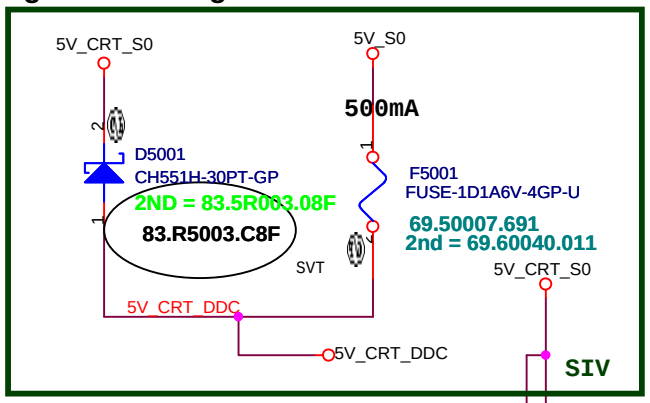
CRT connector



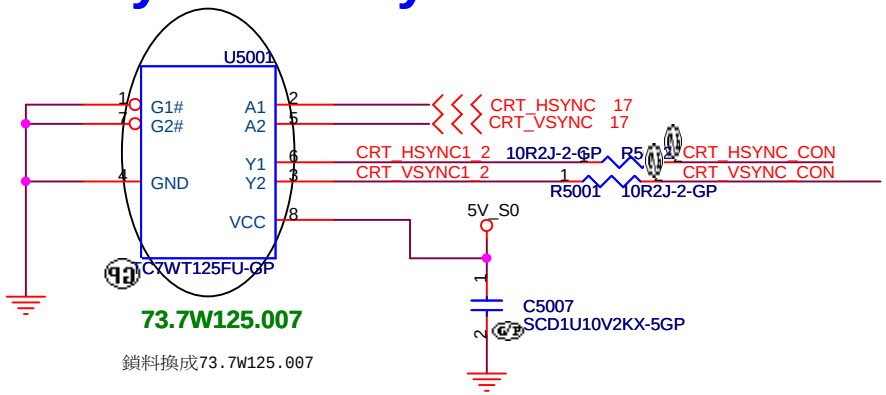


CRT DDCDATA & DDCCLK level shift

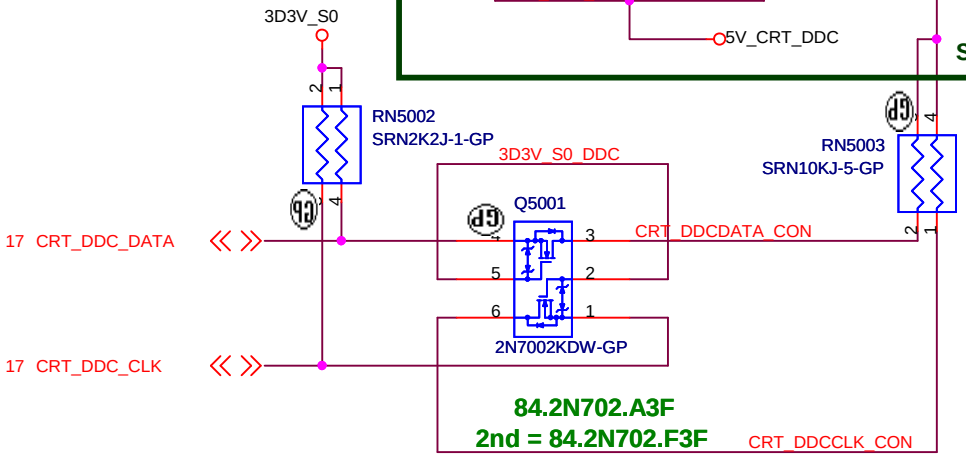
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

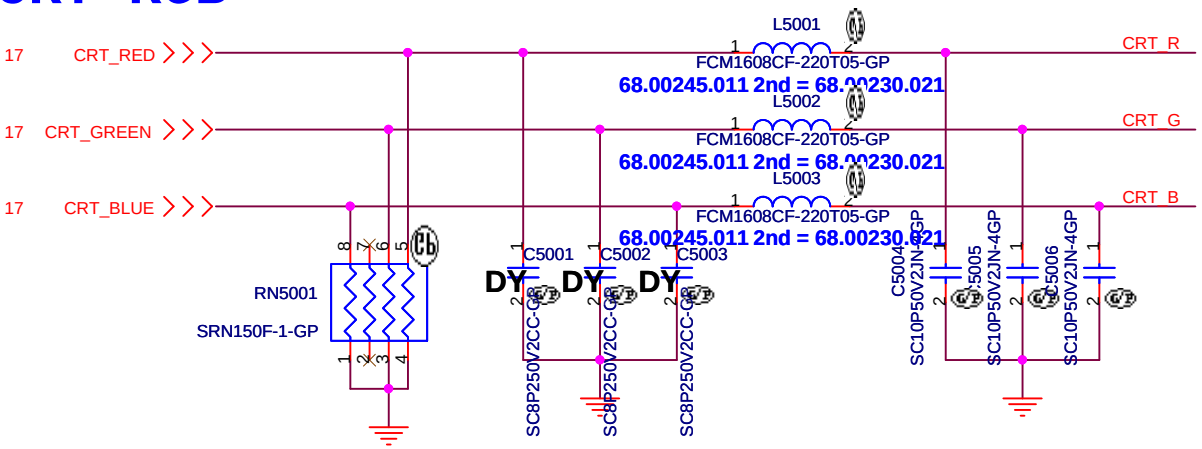


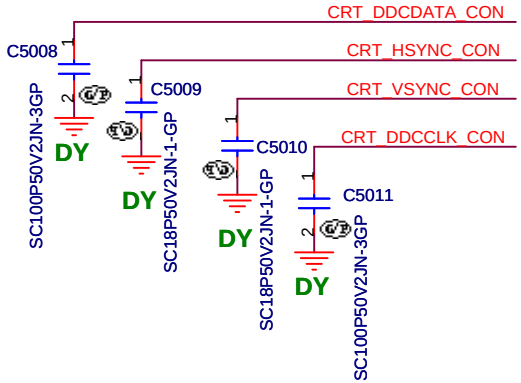
鎖料換成73.7W125.007



CRT RGB

R,G,B place 22pF and ESD diode for intel check list





JV10-CS

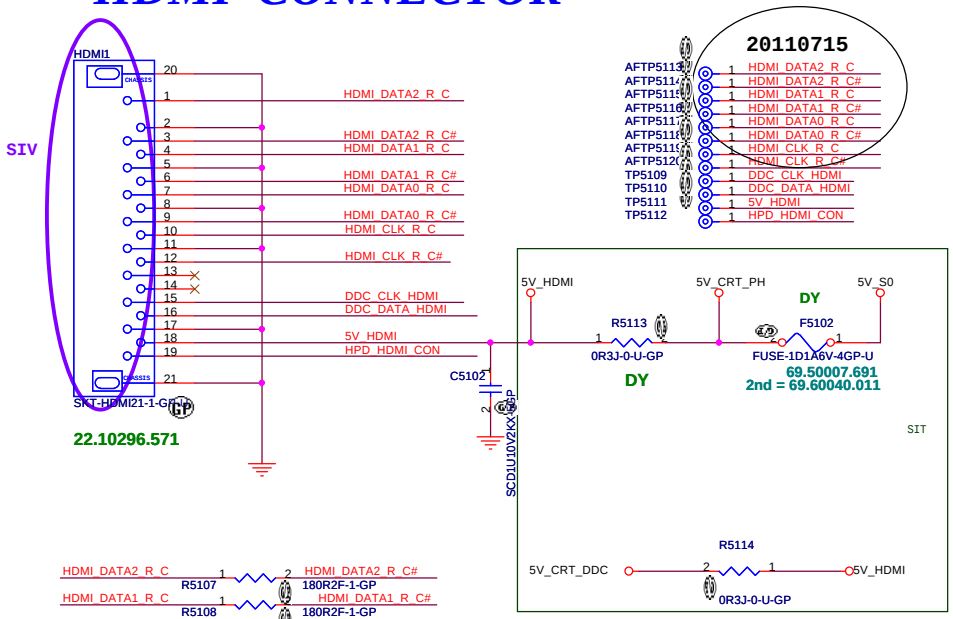
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Board Connector	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 50 of 103	

WWW.AliSaler.Com

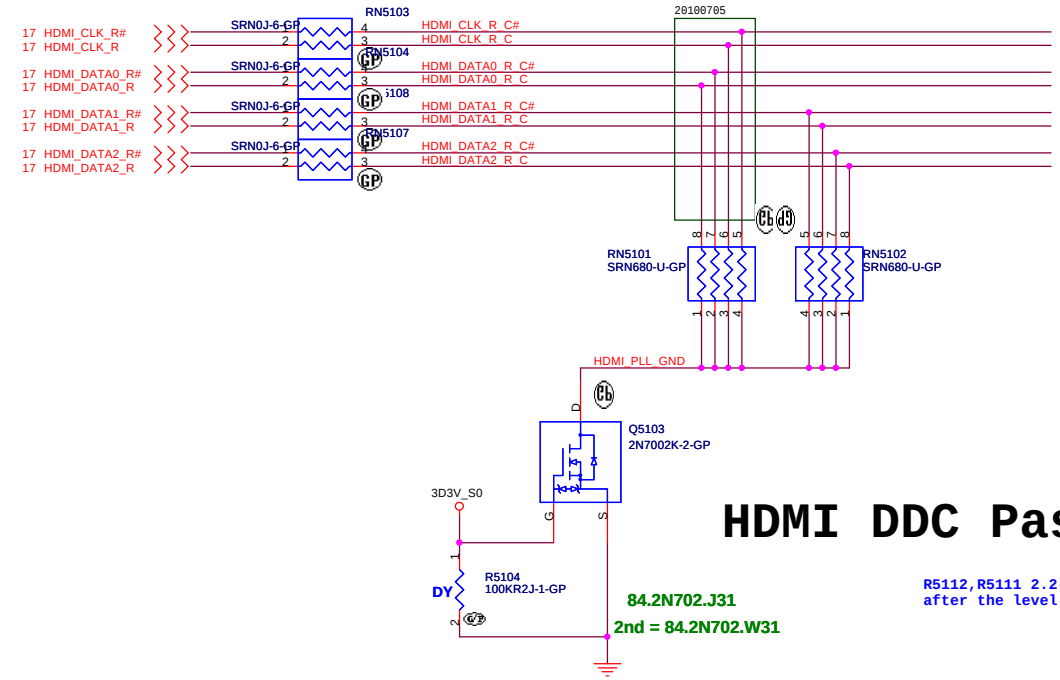
SSID = VIDEO

HDMI CONNECTOR



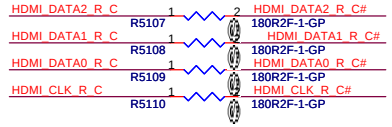
HDMI Passive Level Shifter

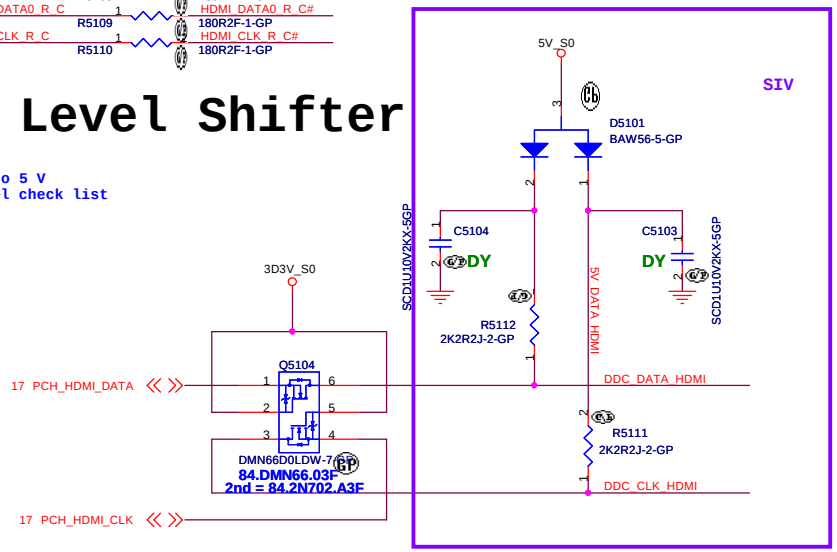
Close to HDMI Connector

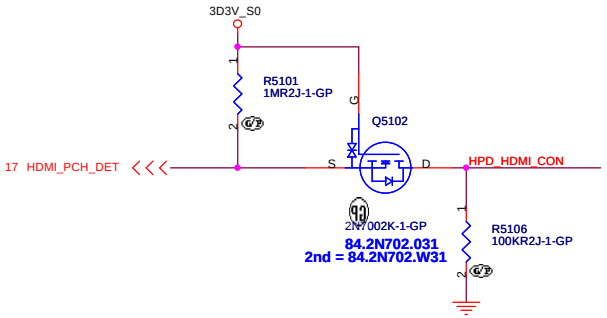


HDMI DDC Passive Level Shifter

R5112,R5111 2.2-kΩ ±5% pull-up to 5 V
after the level shifter for intel check list







JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Conn	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 51 of 103	

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)Display Port*	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 52 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)S-Video*		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 53 of 103	

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)DVI		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 54 of 103	

WWW.AliSaler.Com

(Blanking)

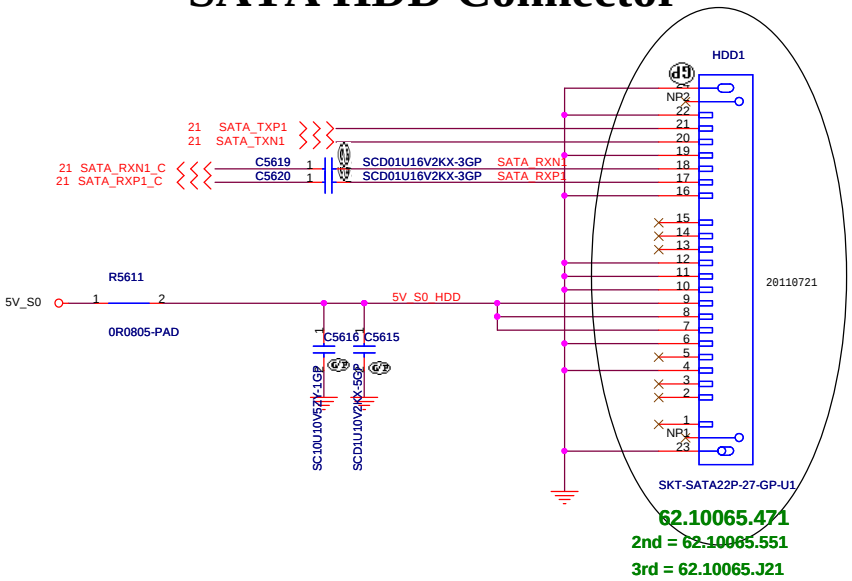
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)ITP	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 55 of 103	

SSID = SATA

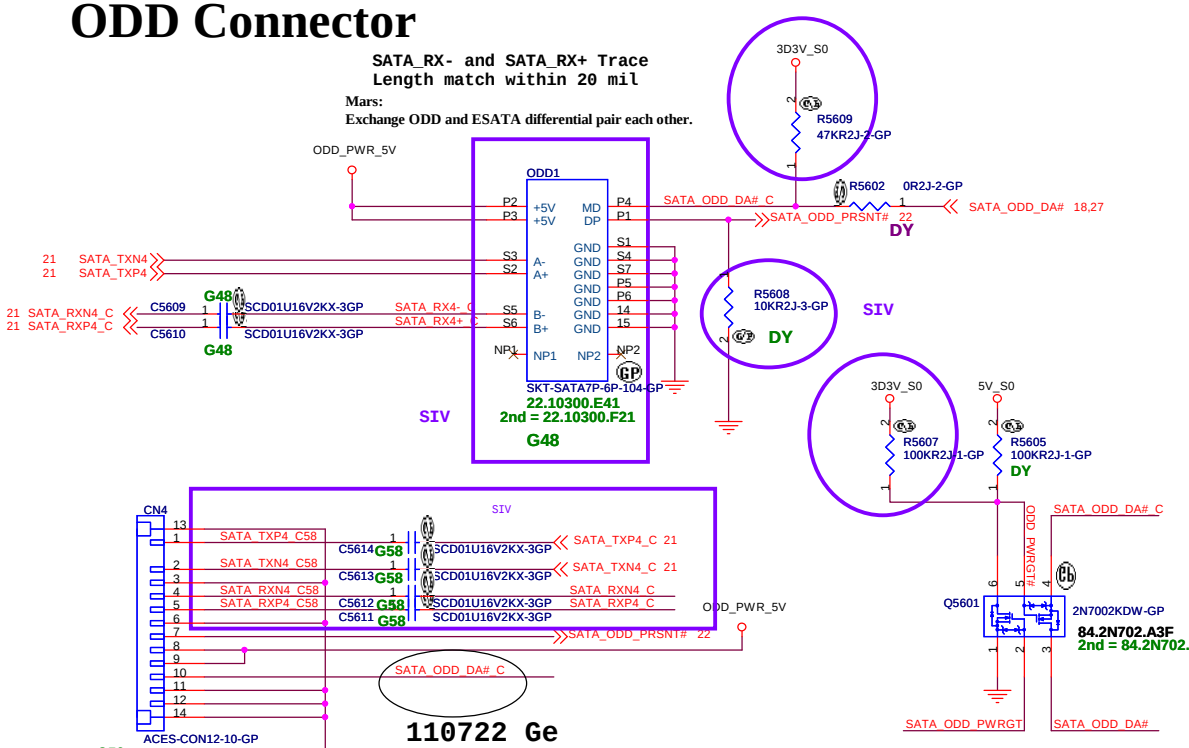
SATA HDD Connector



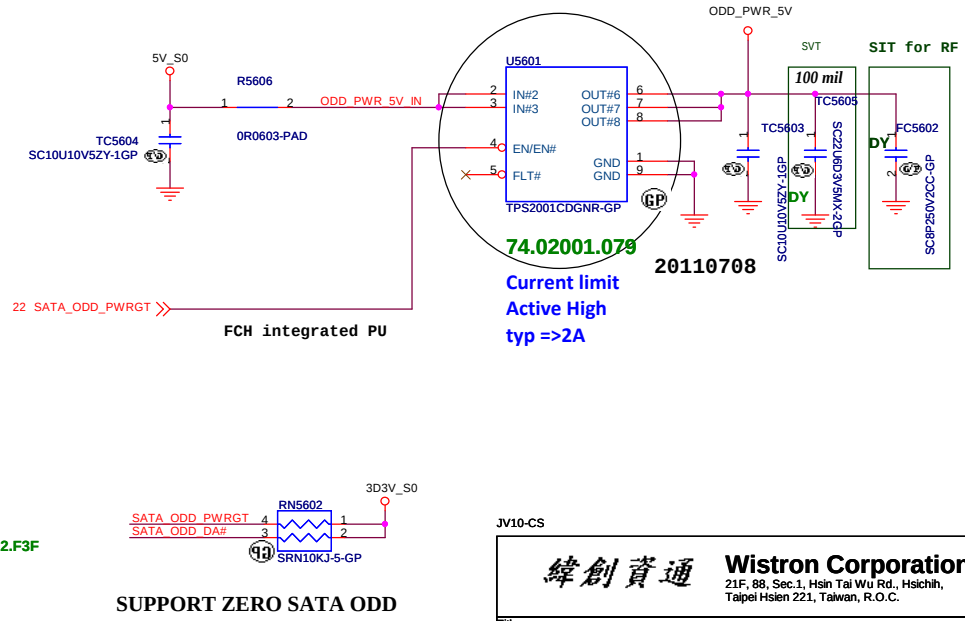
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/ODD	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 56 of 103	

WWW.AllSaler.Com

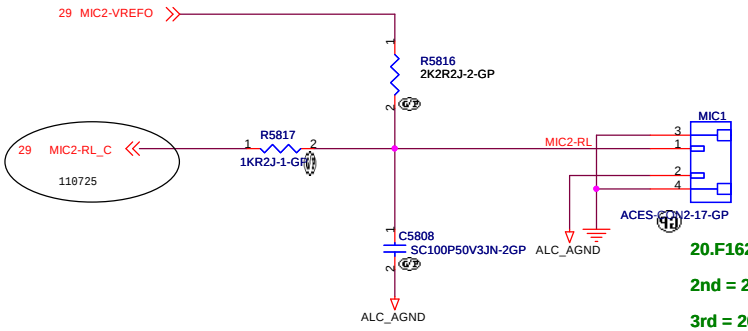
(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)E-SATA*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 57 of 103	

Analog Internal Mic



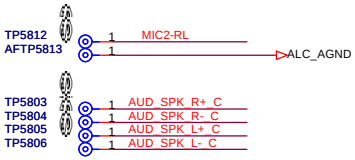
20.F1621.002

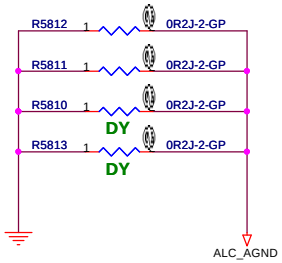
2nd = 20.F1561.002

3rd = 20.F1686.002

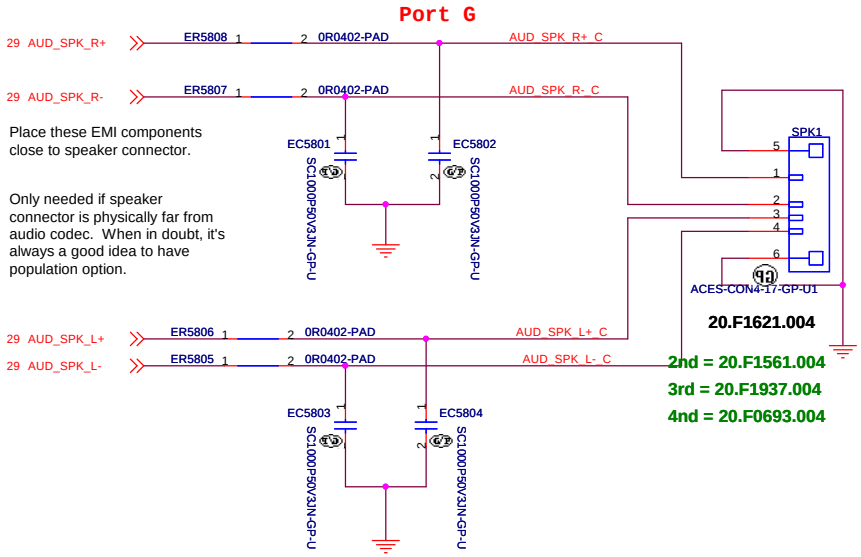
4nd = 20.F0693.002

For EMI request:
Change C5801,C5802 to varister 69.80024.001





INTERNAL STEREO SPEAKERS



20.F1621.004

2nd = 20.F1561.004

3rd = 20.F1937.004

4nd = 20.F0693.004

SIV
Remove bestbuy

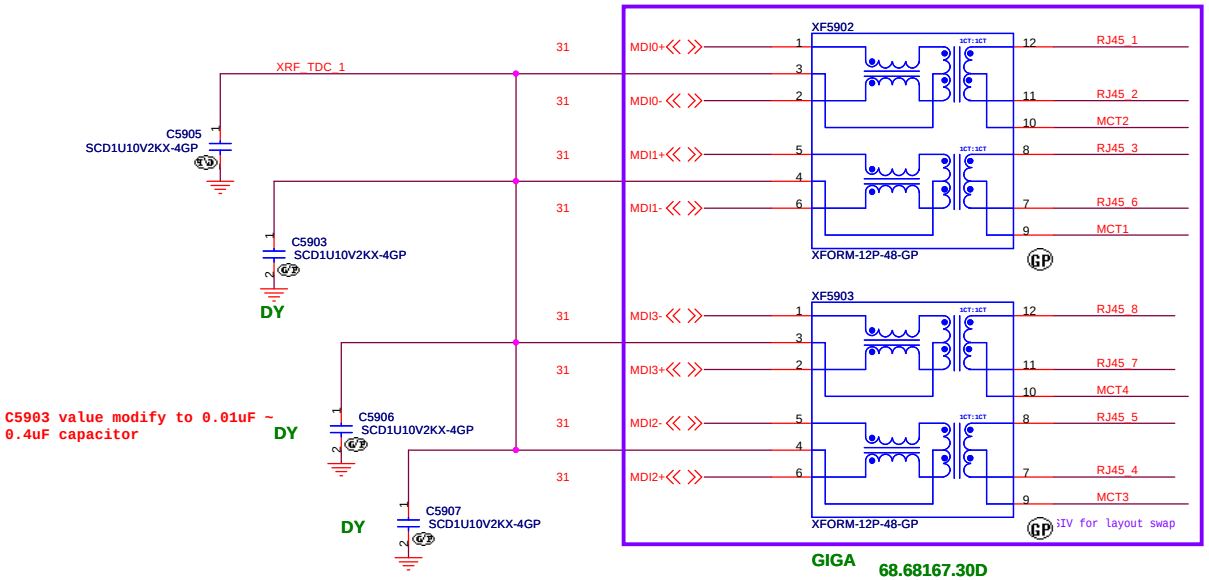
JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MIC/SPEAKER/AUDIO JACK	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 58 of 103	

WWW.AliSaler.Com

10/100M Lan Transformer

FOR CO-LAY GIGA Lan Transformer



C5903 value modify to 0.01uF ~ 0.4uF capacitor

68.68167.30D

2nd = 68.0NS14.301

3rd = 68.HD081.30B

1.route as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

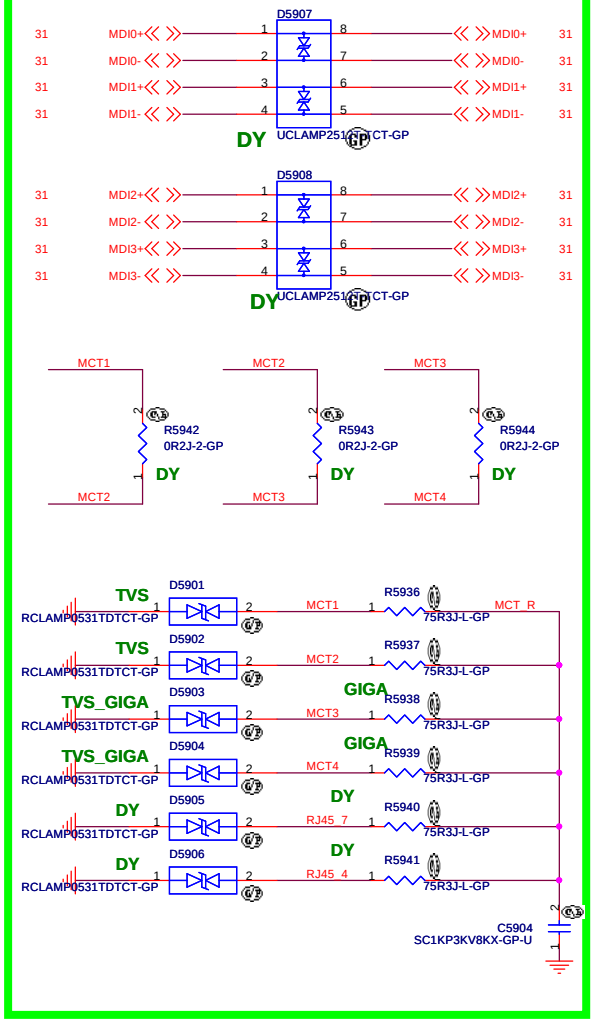
68.68167.30D

2nd = 68.0NS14.301

3rd = 68.HD081.30B

For AR8162(10/100M): C5906, C5907,R5938, R5939 can be DY.
For AR8161(GIGA): Dummy R5934, R5935, R5940,R5941

10/100 LAN surge circuit



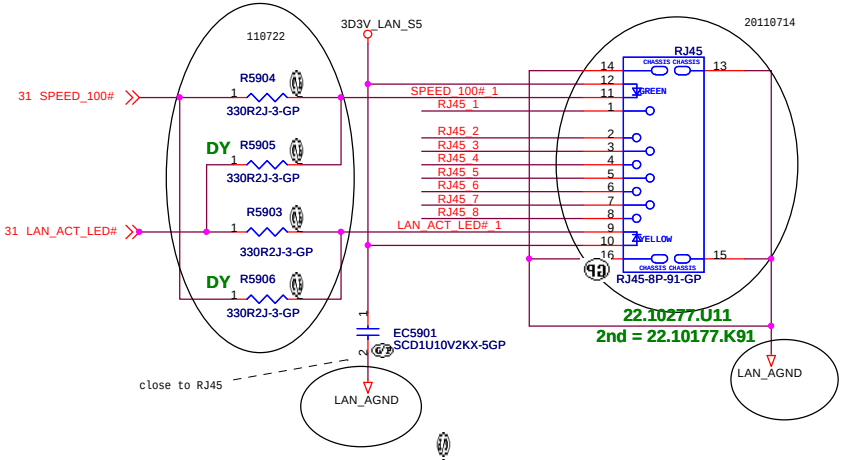
83.00531.0AF
2nd = 83.00511.0A0

83.00531.0AF
2nd = 83.00511.0A0

83.00531.0AF
2nd = 83.00511.0A0

83.00531.0AF
2nd = 83.00511.0A0

LAN Connector

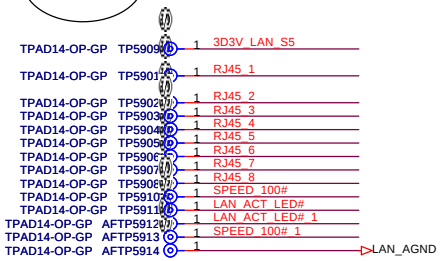


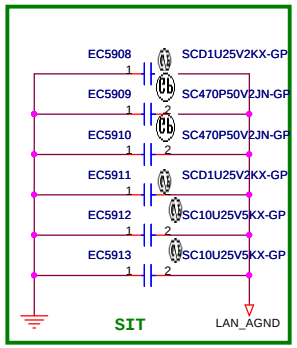
DY

R5934 RJ45_4 — RJ45_5
0R3J-0-U-GP

R5935 RJ45_7 — RJ45_8
0R3J-0-U-GP

DY





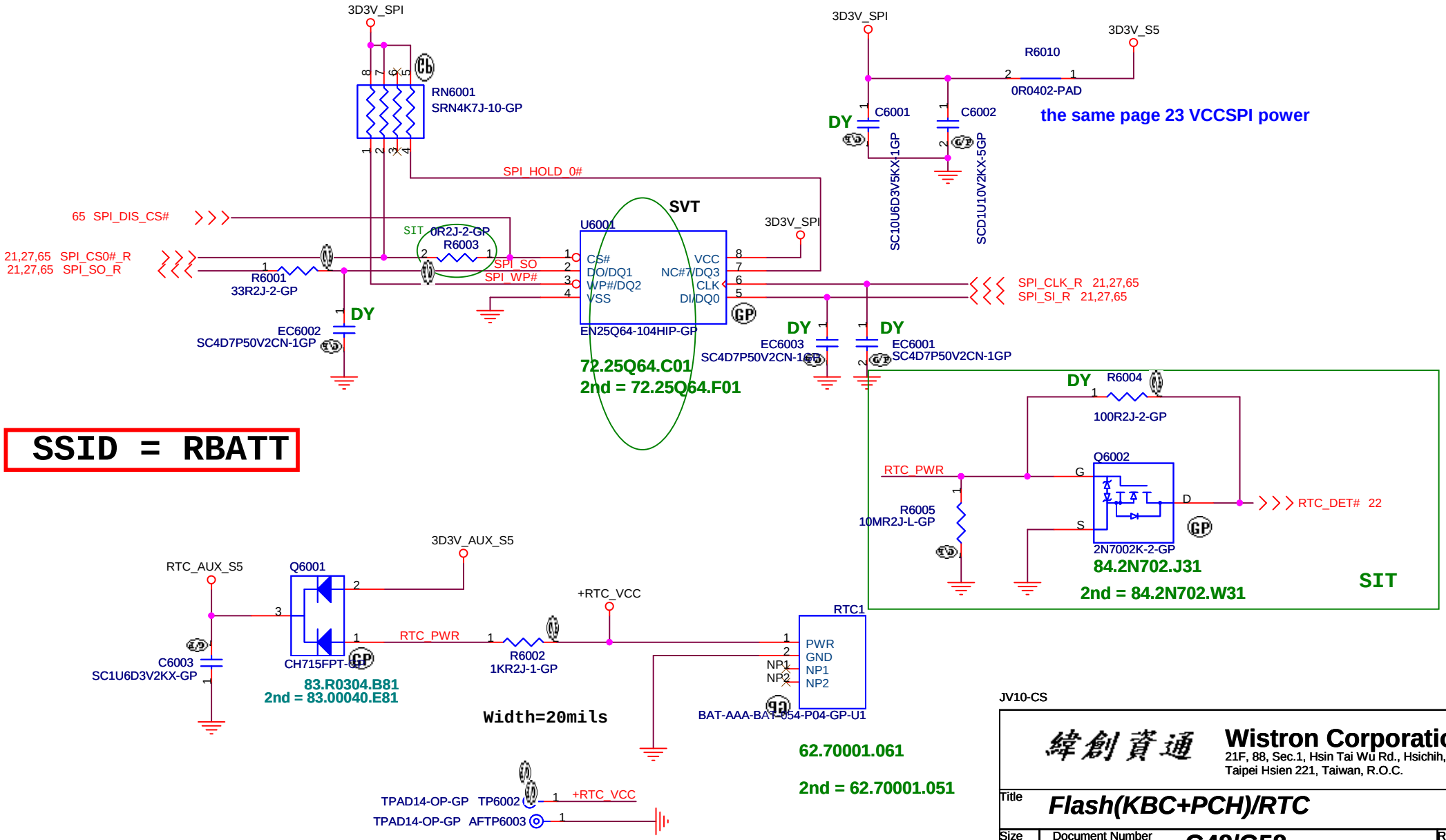
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RJ45	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 59 of 103	

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



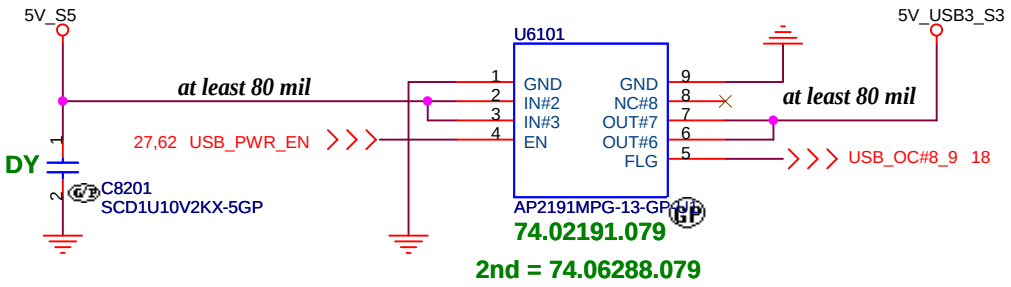
JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Flash(KBC+PCH)/RTC		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 60 of 103		

WWW.AliSaler.Com

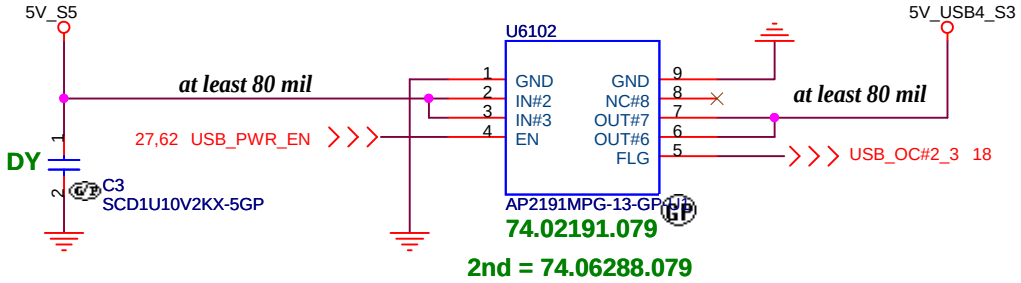
SSID = USB

USB Ext. port3 power SW



U6101 place near to USBCN3

USB Ext. port4 power SW



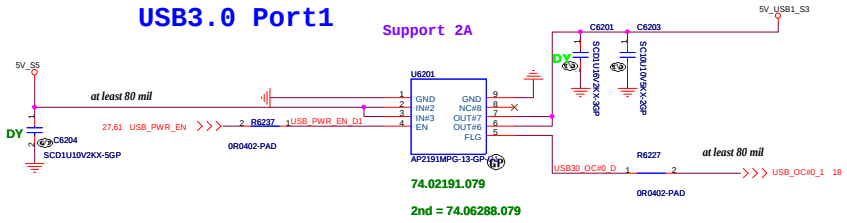
U6102 place near to CDRCN2

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***USB2.0 Port Power SW***		
Size	Document Number **G48/G58**		Rev **SC**
Date: Friday, February 17, 2012	Sheet 61 of 103		

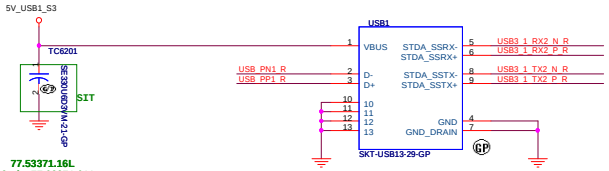
USB3.0 Port1

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

2nd = 77.93371.011

22.10339.931

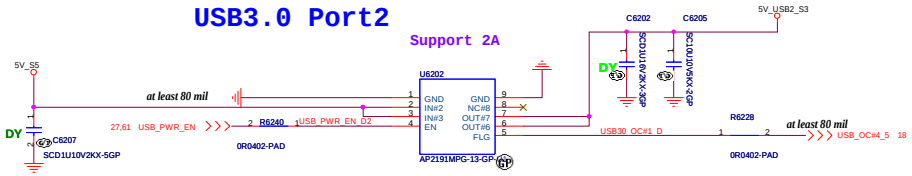
2nd = 22.10339.C11

TC6201 place near the USB1 connector

Co-Layout USB2.0 22.10321.S01

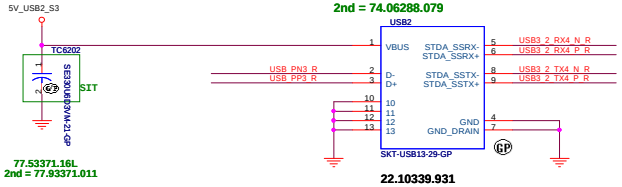
USB3.0 Port2

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

2nd = 77.93371.011

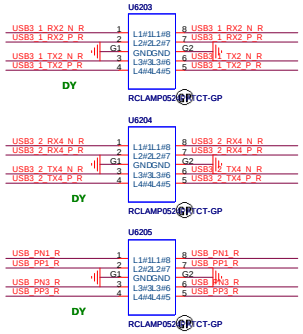
22.10339.931

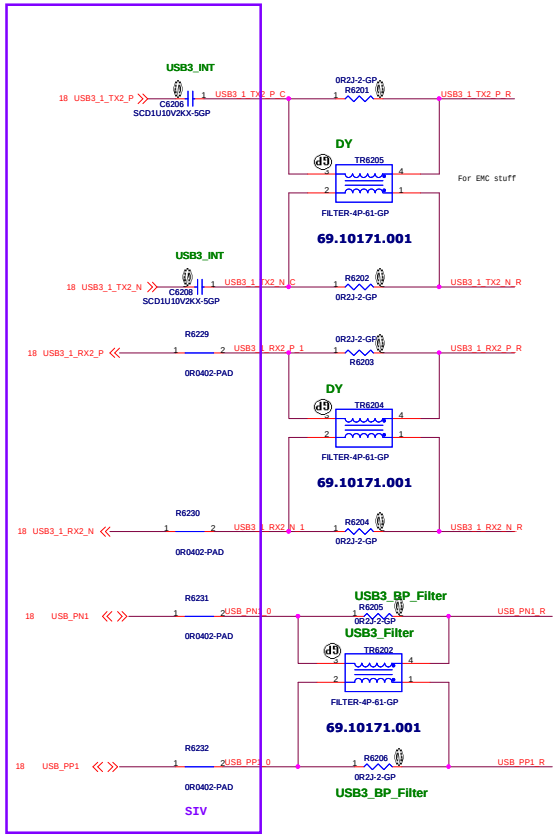
2nd = 22.10339.C11

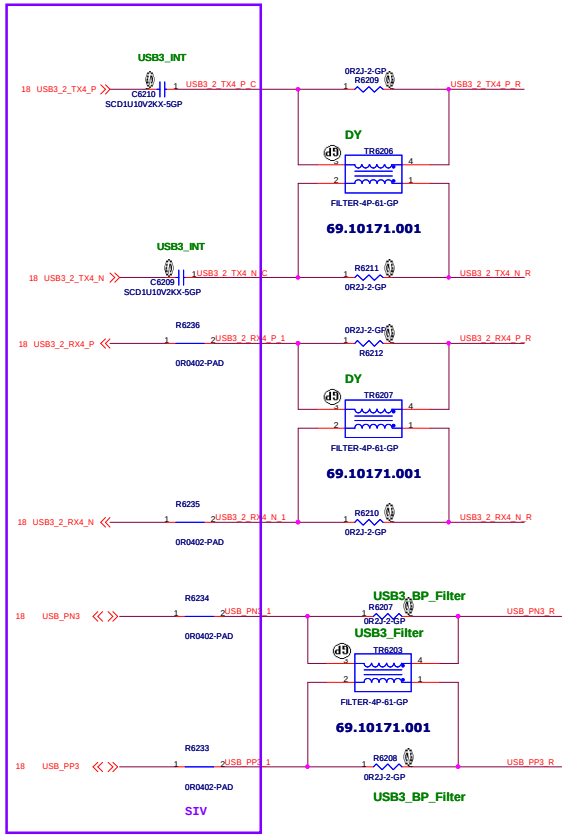
TC6202 place near the USB2 connector

Co-Layout USB2.0 22.10321.S01

LAN surge circuit







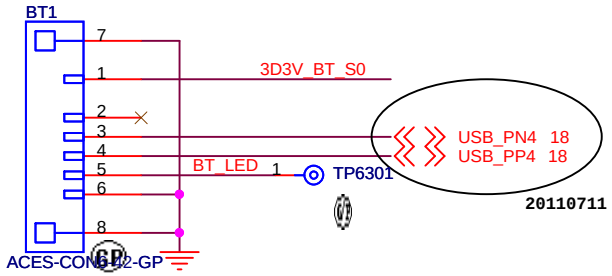
JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB3.0 Port1/2		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 62 of 103	

WWW.AliSaler.Com

SSID = User.Interface

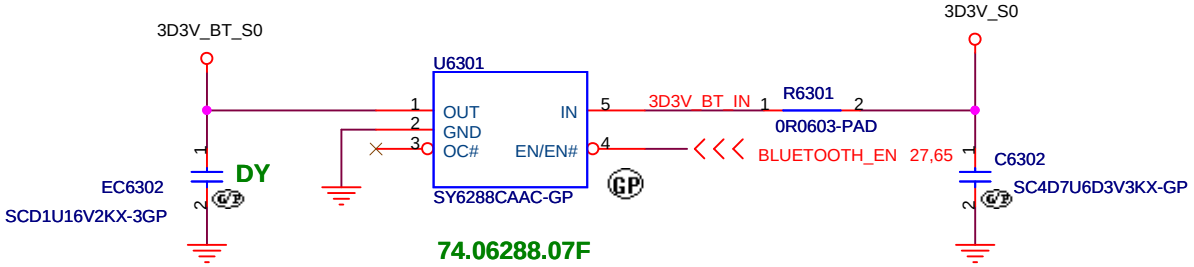
Bluetooth conn.



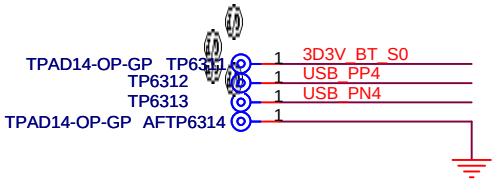
20.F1705.006

2nd = 20.F1804.006

3rd = 20.F1571.006



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BLUETOOTH***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 63 of 103	

(Blanking)

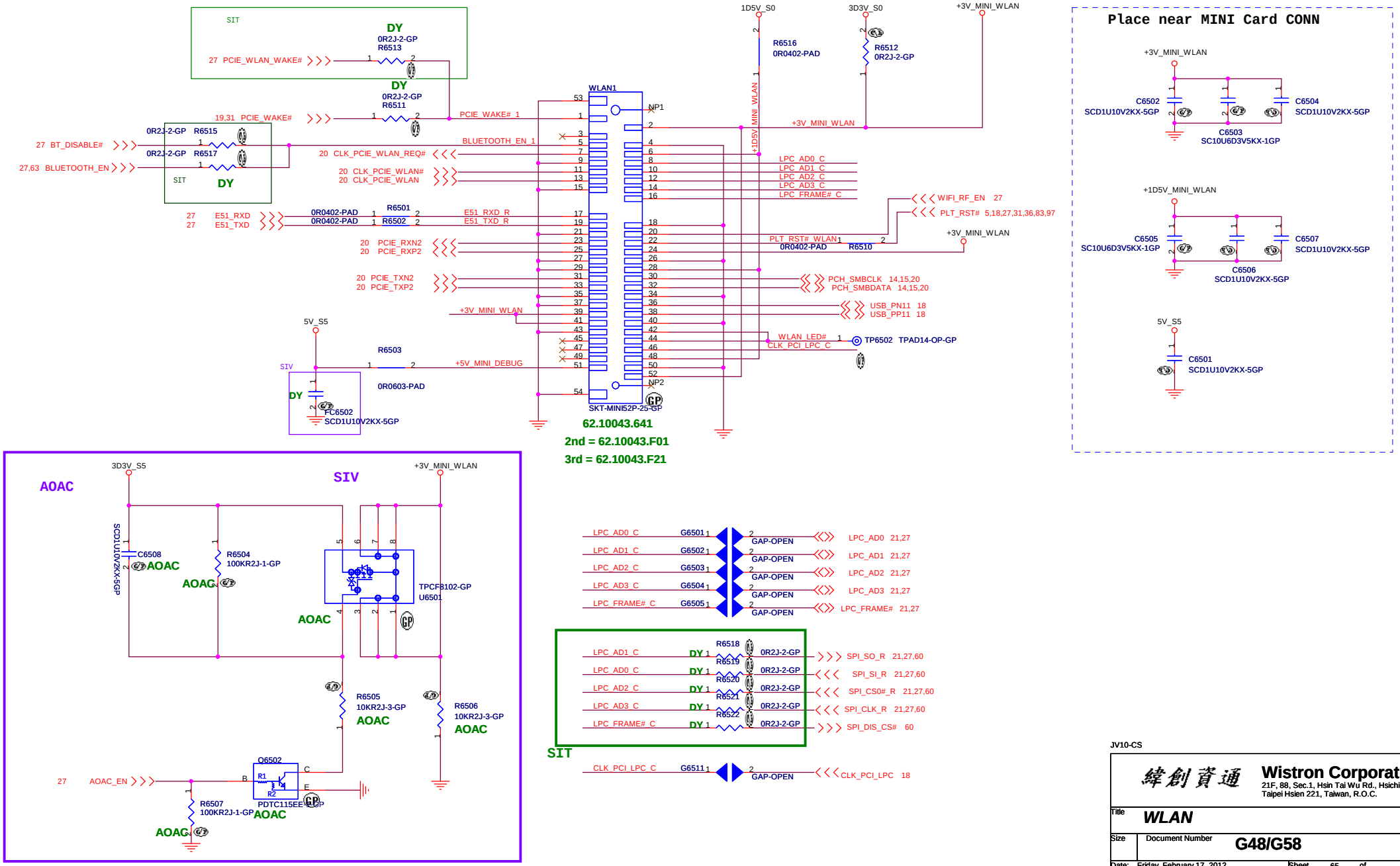
JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	(Reserved)Finger Print Con.		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 64 of 103	

WWW.AliSaler.Com

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	WLAN	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 65 of 103	

SSID = Wireless

Mini Card Connector(WWAN)

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)WWAN CONN	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 66 of 103	

WWW.AliSaler.Com

(Blanking)

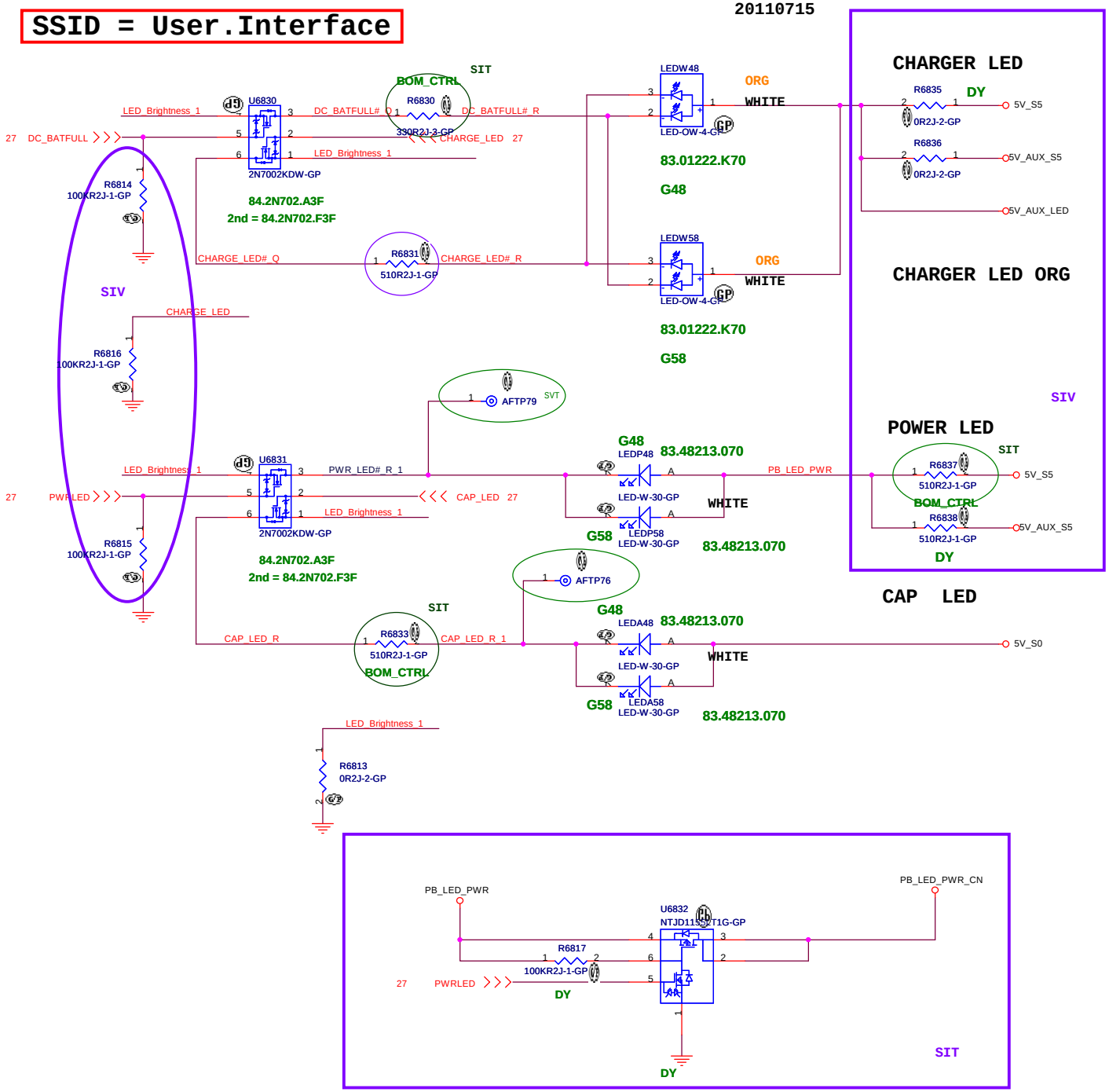
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)3rd MINICARD	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 67 of 103	

SSID = User.Interface

20110715



WWW.AliSaler.Com

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED/Power Button/key

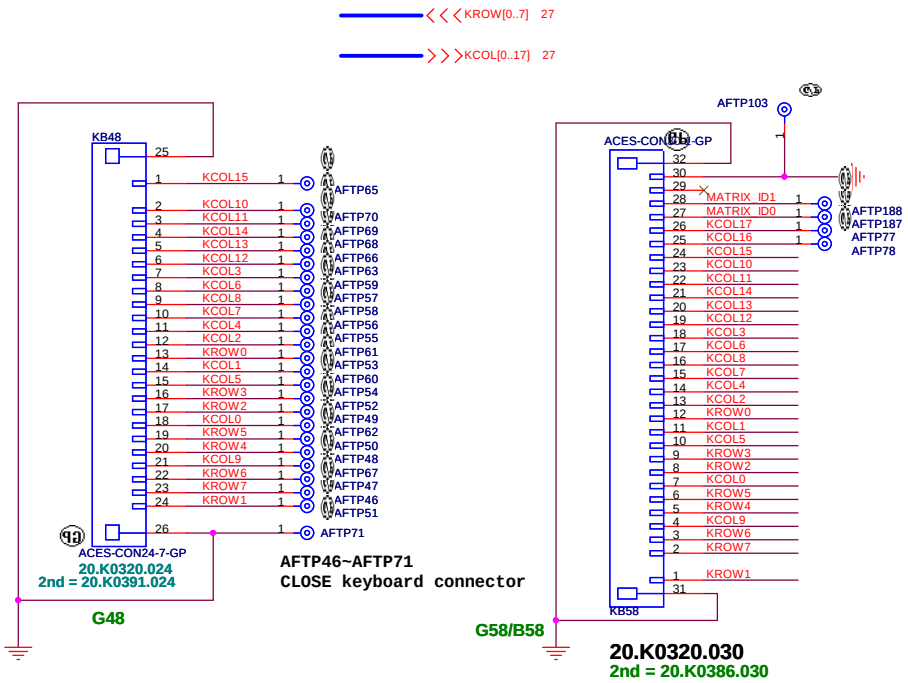
Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 68 of 103

SSID = KBC

KB1 Follow LA47

Internal KeyBoard Connector



20.K0320.030
2nd = 20.K0386.030

14"

* Membrane Pin Out Top View :

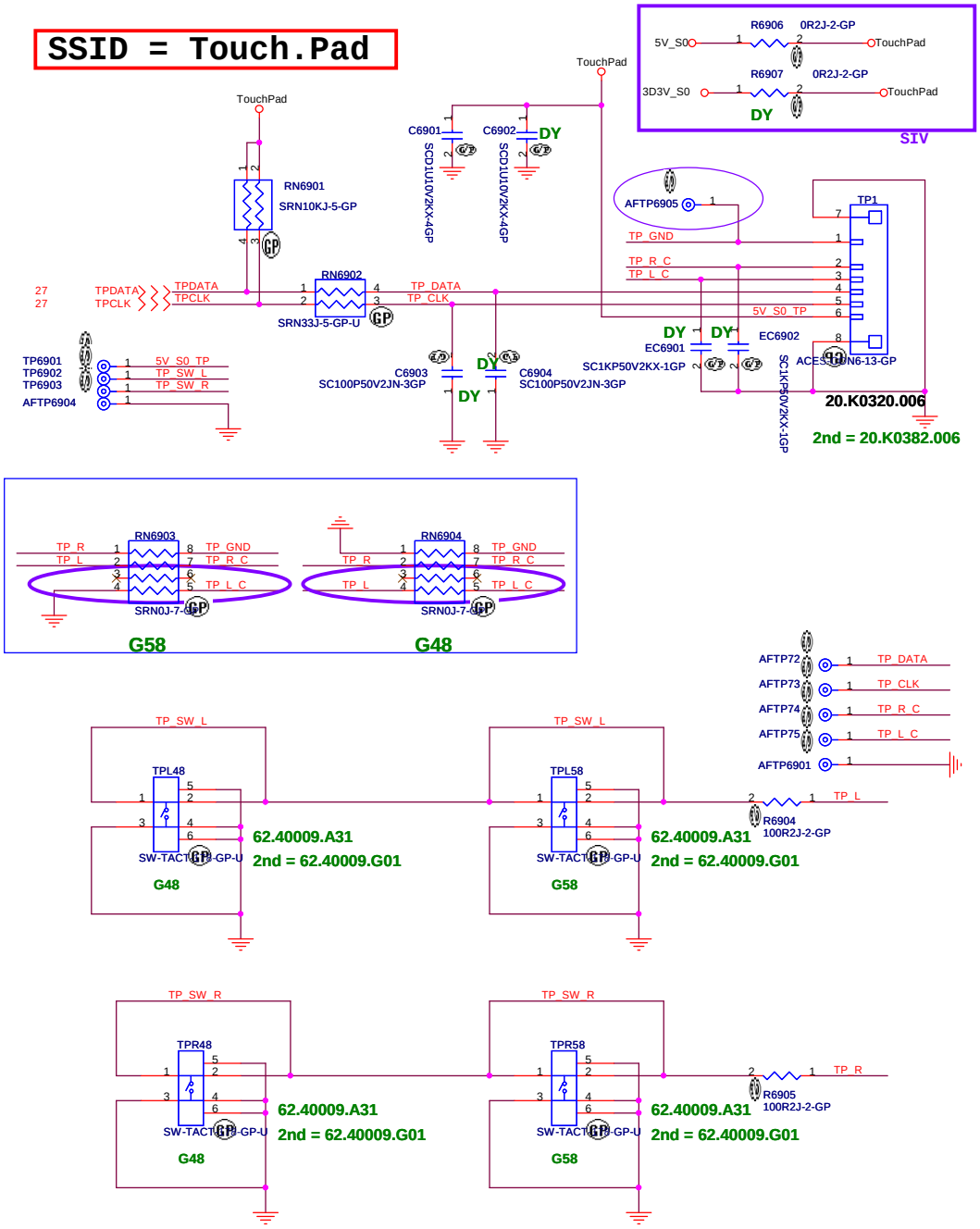
PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

15"

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	D 17	D 18	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Key Board/Touch Pad	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 69 of 103	

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Hall Sensor***

Size	Document Number	Rev
	G48/G58	**SC**

Date: Friday, February 17, 2012 Sheet 70 of 103

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)Debug connector*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 71 of 103	

(Blanking)

JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***(Reserved)RJ11+MDC***		
Size	Document Number **G48/G58**		Rev **SC**
Date: Friday, February 17, 2012		Sheet 72 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)1394 CONN*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 73 of 103	

(Blanking)

JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	(Reserved)CARD Reader CONN		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 74 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)Express Card*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 75 of 103	

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)Smart Card Socket		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 76 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)TPM	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 77 of 103	

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)SIO		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 78 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)G-Sensor*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 79 of 103	

(Blanking)

JV10-CS

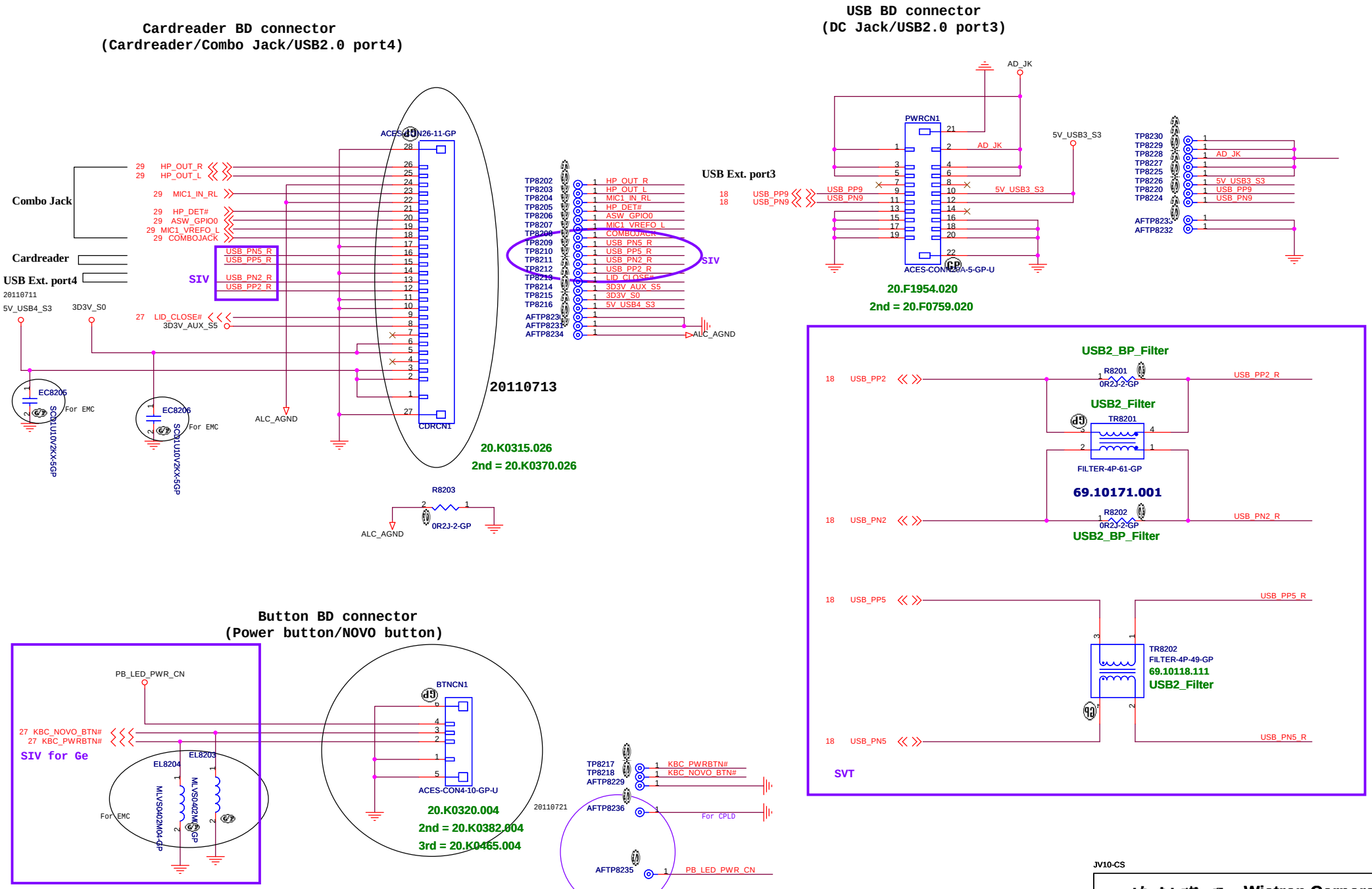
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	(Reserved)RF/Other		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 80 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

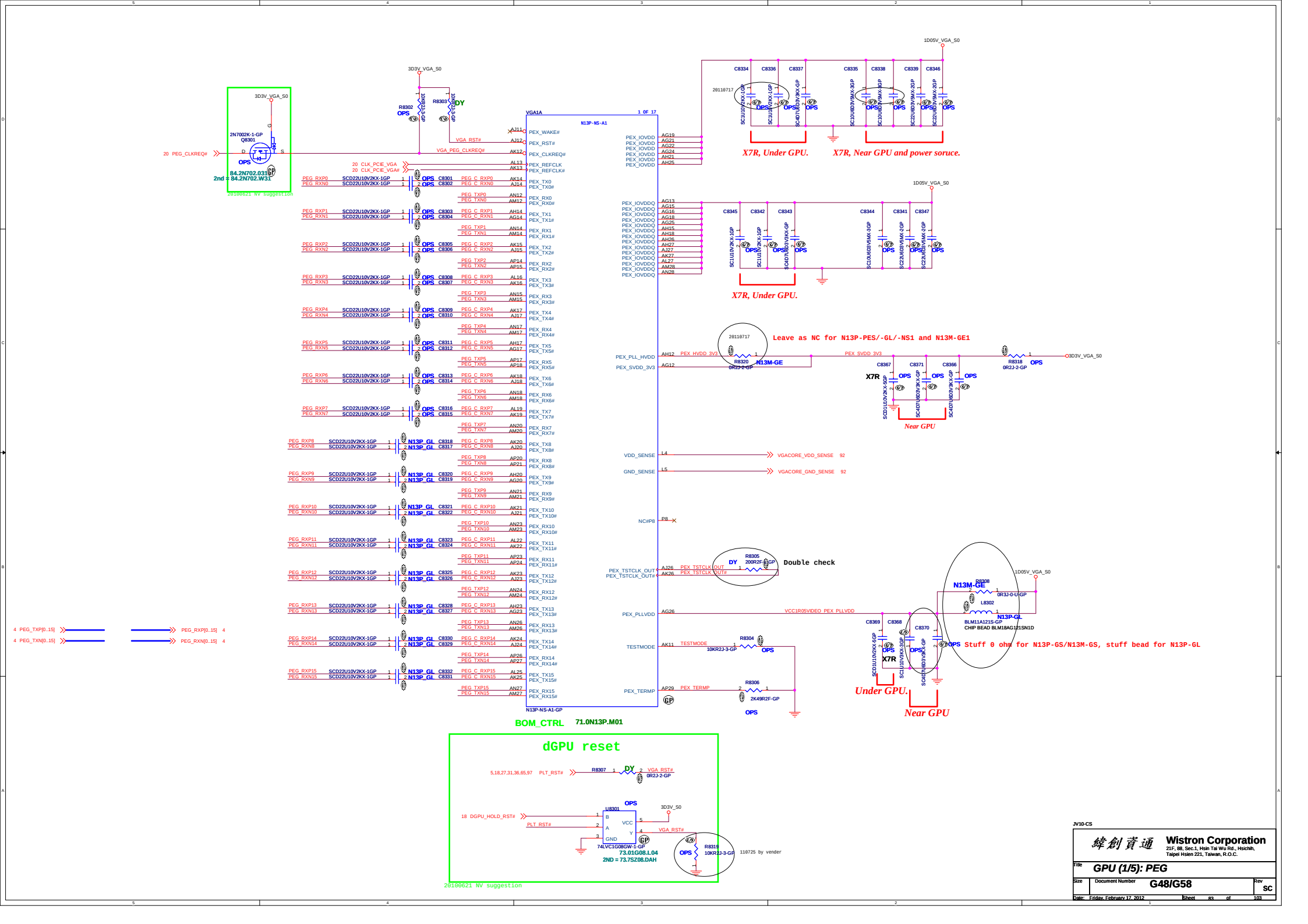
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***(Reserved)Screw Holes,SPR***		
Size	Document Number **G48/G58**		Rev **SC**
Date: Friday, February 17, 2012		Sheet 81 of 103	



JV10-CS

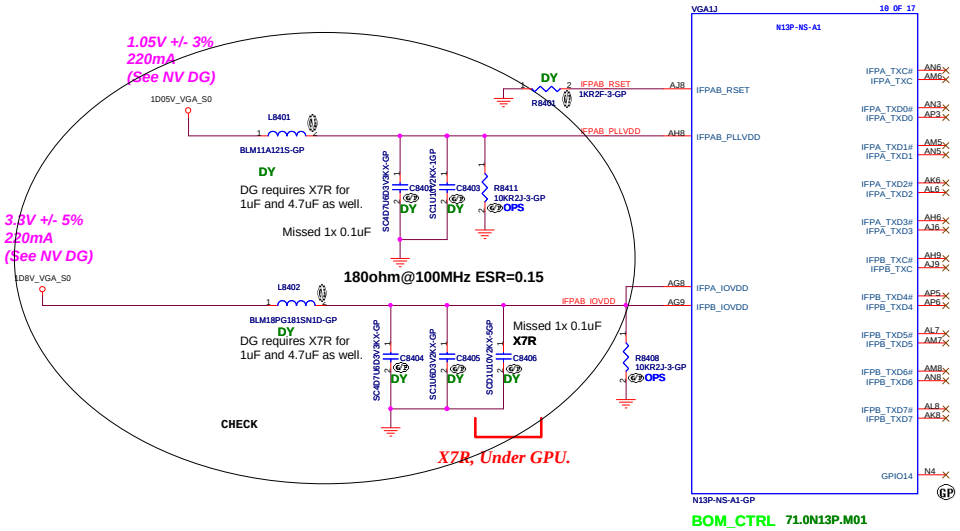
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***IO Board Connector***
Size / Document Number	**G48/G58**
Rev	**SC**
Date: Friday, February 17, 2012	Sheet 82 of 103

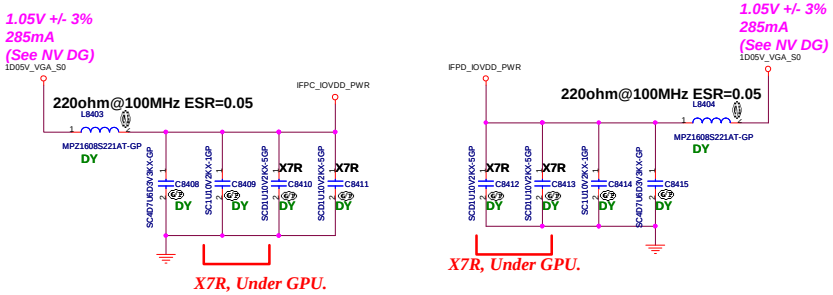
WWW.AliSaler.Com

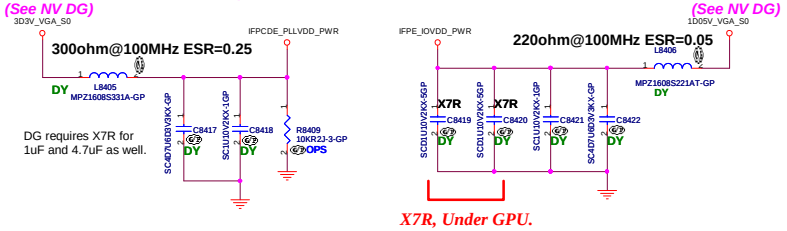

VGA1A
N13P-NS-A1
1 OF 17
N13P-NS-A1-GP
3D3V_VGA_S0
1D05V_VGA_S0
2N7002K-1-GP
Q8301
84.2N702.031
2nd = 84.2N702.W31
20 PEG_CLKREQ#
VGA_RST#
VGA_PEG_CLKREQ#
20 CLK_PCIE_VGA
20 CLK_PCIE_VGA#
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_IOVDD
PEX_IOVDDQ
PEX_PLL_HVDD
PEX_SVDD_3V3
PEX_HVDD_3V3
VDD_SENSE
GND_SENSE
VGACORE_VDD_SENSE 92
VGACORE_GND_SENSE 92
NC#P8
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_PLLVDD
VCC1R05VIDEO_PEX_PLLVDD
TESTMODE
PEX_TERMP
X7R, Under GPU.
X7R, Near GPU and power soruce.
Leave as NC for N13P-PES/-GL/-NS1 and N13M-GE1
Near GPU
Double check
Stuff 0 ohm for N13P-GS/N13M-GS, stuff bead for N13P-GL
Under GPU.
BOM_CTRL 71.0N13P.M01
dGPU reset
5,18,27,31,36,65,97 PLT_RST#
18 DGPU_HOLD_RST#
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
110725 by vender
20100621 NV suggestion
JV10-CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (1/5): PEG
Size Document Number G48/G58 Rev SC
Date: Friday, February 17, 2012 Sheet 83 of 103

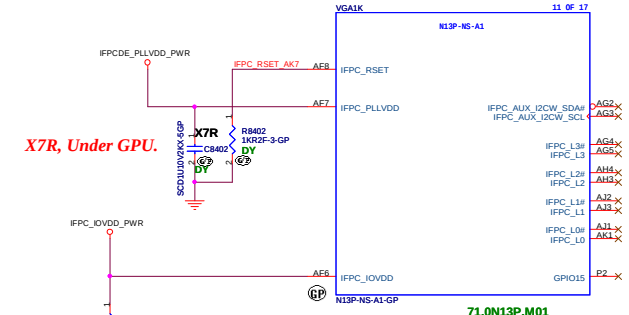
RD480_SA:71.0N12P.M08

LVDS Interface

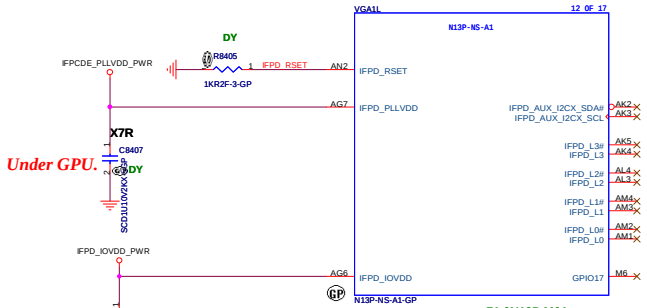


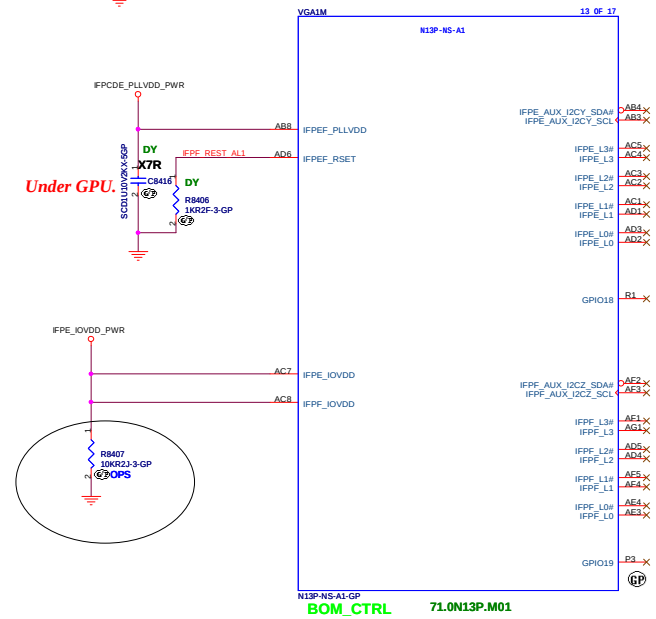






HDMI Interface

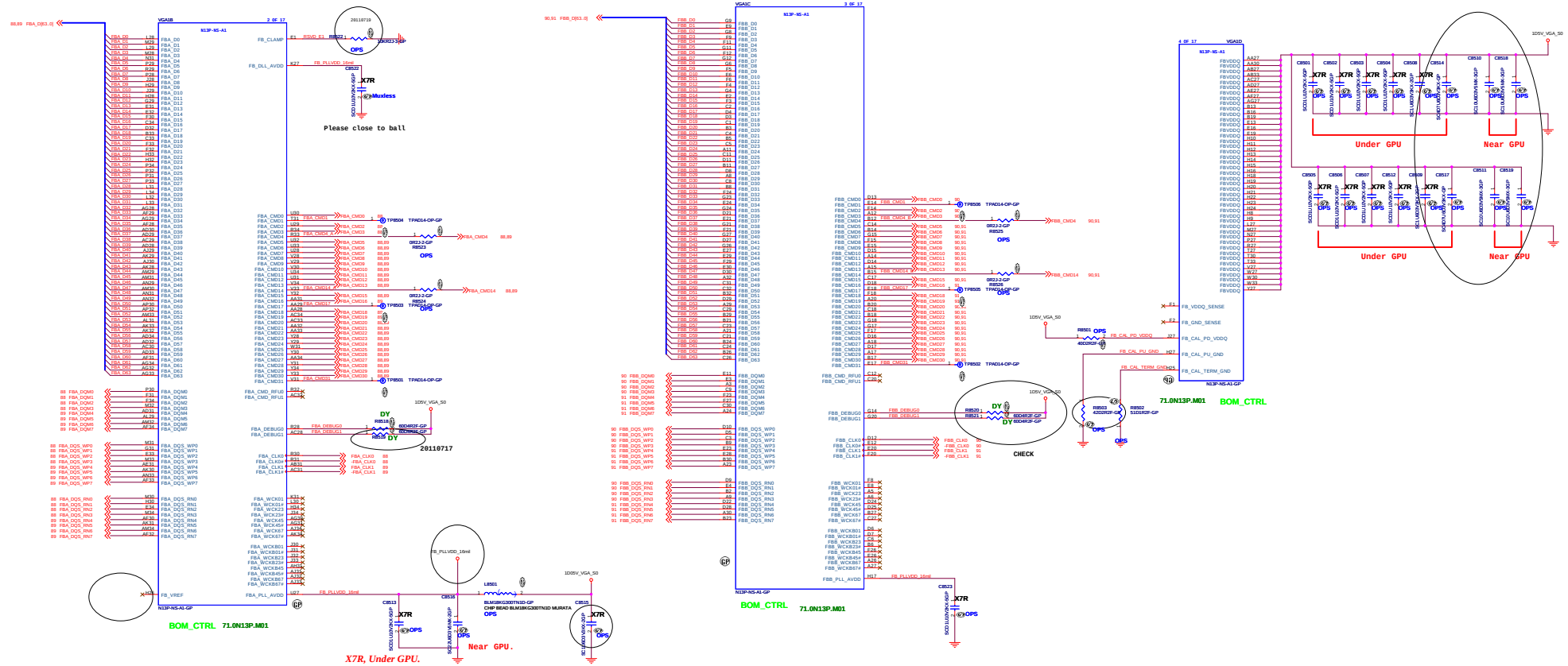




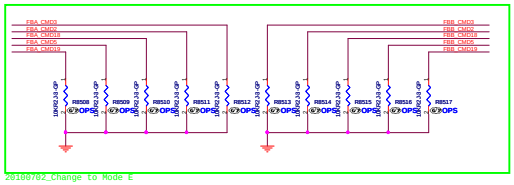
JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU (2/5): DIGITALOUT	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 84 of 103	

WWW.AliSaler.Com



FBCLK Termination place on VRAM side

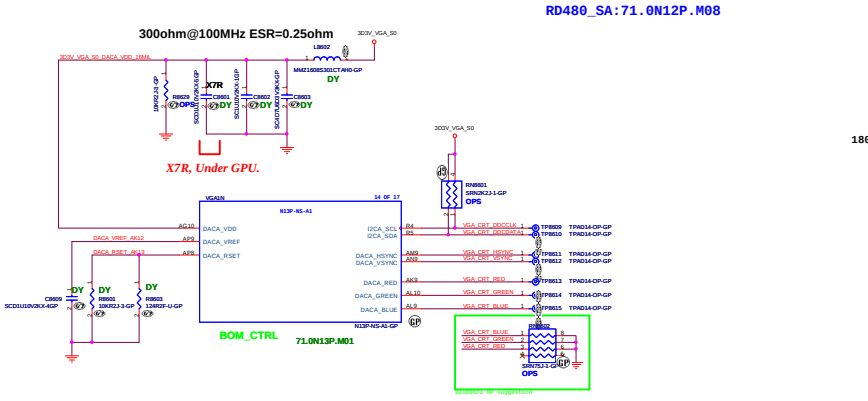


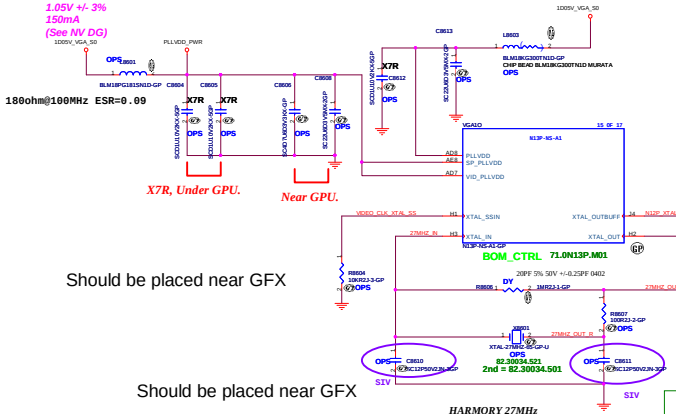
FBCLK Termination place on VRAM side

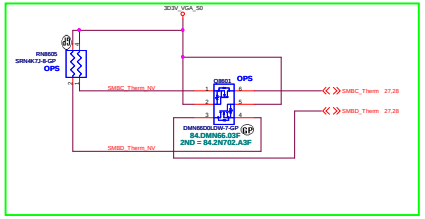
JV10-CS

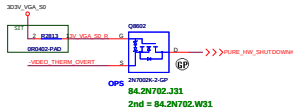
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU (3/5): VRAM I/F
Size	Document Number: G48/G58 — Rev: SC
Date: Friday, February 17, 2012	Sheet 85 of 103

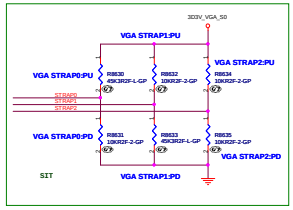
RD480_SA:71.0N12P.M08

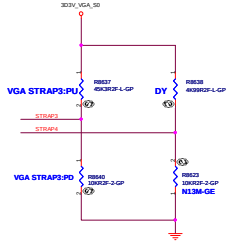












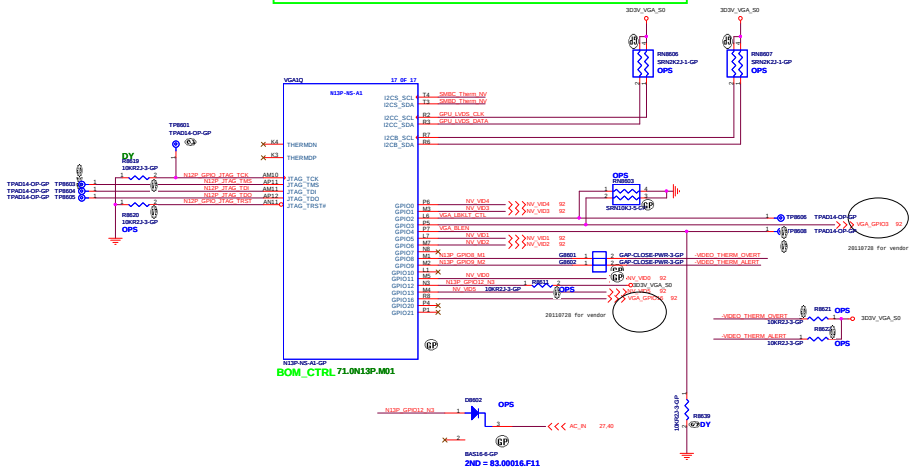
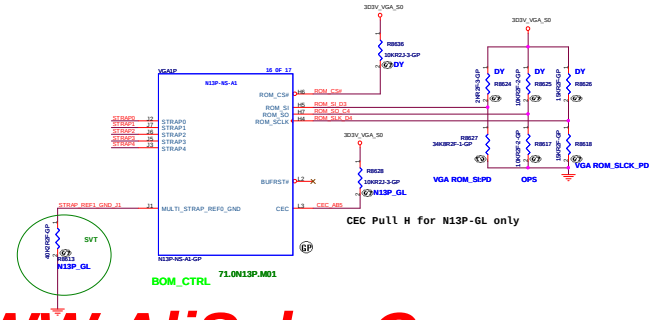


	TABLE NVIDIA	N13P-GL(PS) DEV ID: 0x0DE9
STRAP0	R8630(PU)	45.3Kohm 64.45325.6DL
	R8631(PD)	DY
STRAP1	R8632(PU)	DY
	R8633(PD)	45.3Kohm 64.45325.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL
	R8635(PD)	DY
STRAP3	R8637(PU)	DY
	R8640(PD)	DY
STRAP4	R8638(PU)	DY
	R8623(PD)	DY

	N13M-GE(PS)					
	TABLE NVIDIA	SAMSUNG 128Mx16 72.42164.D0U	SAMSUNG 128Mx16 72.42164.G0U	HYNIX 128Mx16 72.52G63.C0U	Samsung 64Mx16	HYNIX 64Mx16
STRAP0	R8630(PU)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
	R8631(PD)	DY	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP1	R8632(PU)	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
	R8633(PD)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
	R8635(PD)	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
STRAP3	R8637(PU)	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	DY
	R8640(PD)	10Kohm 64.10025.6DL	DY	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
STRAP4	R8638(PU)	DY	DY	DY	DY	DY
	R8623(PD)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL



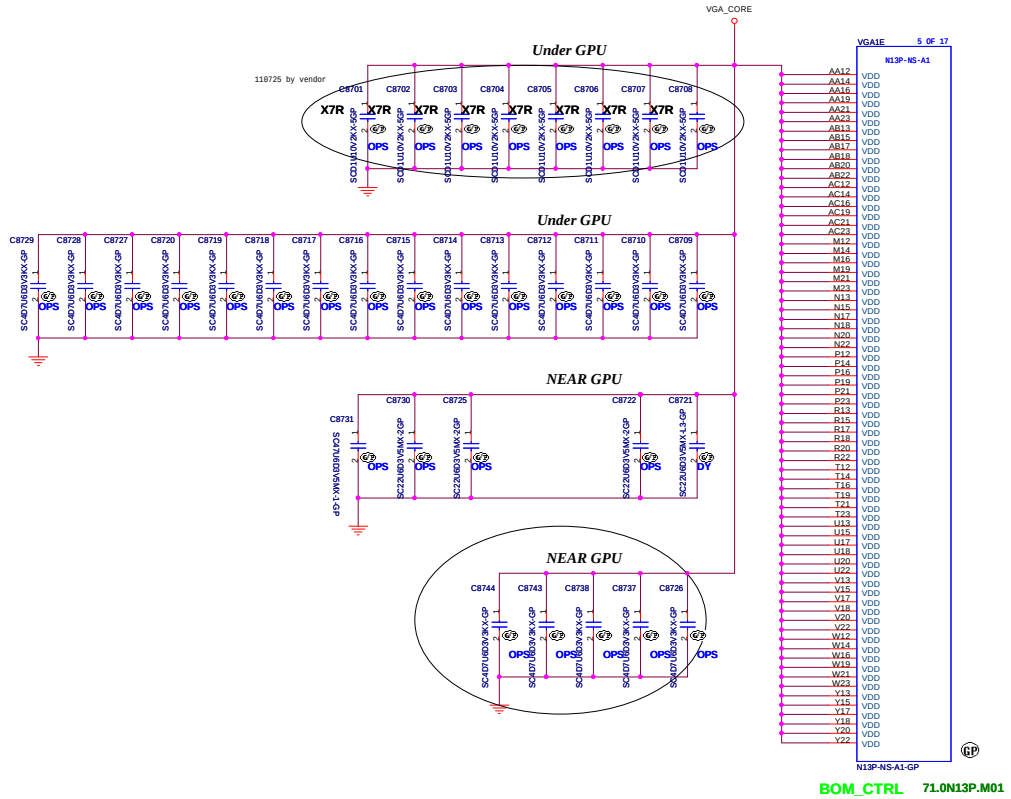
VGA	N13P-GL(PS) 71.0N13P.E0U	N13M-GE(PS) 71.0N13M.B1U
ROM_SO PD R8617	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
ROM_SCLK PD R8618	15Kohm 64.15025.6DL	10Kohm 64.10025.6DL

TABLE
VIDEO MEMORY

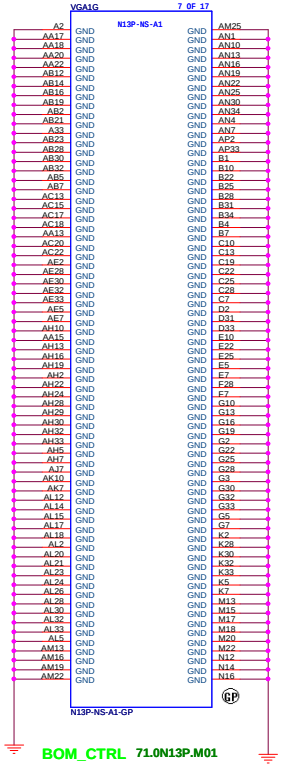
Nvidia VGA	900MHz	HYNIX 128Mx16	SAMSUNG 128Mx16	HYNIX 64Mx16	Samsung 64Mx16
		72.52G63.C0U	72.42164.D0U 72.42164.G0U	72.51G63.H0U	72.41646.Q0U
N13P-GL	ROM_SI PD R8627	30.1Kohm 64.30125.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL
N13M-GE	ROM_SI PD R8627	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL

WWW.AliSaler.Com

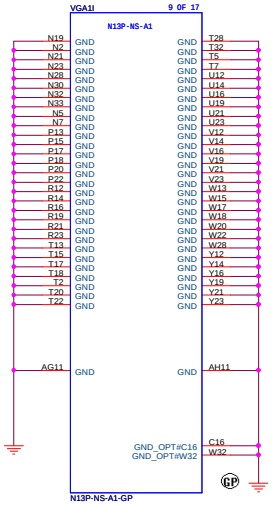
JV10-CS
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU (4/5): GPIO/STRAP
Size: | Document Number: G48/G58 | Rev: SC
Date: Friday, February 17, 2012 | Sheet 8 of 33



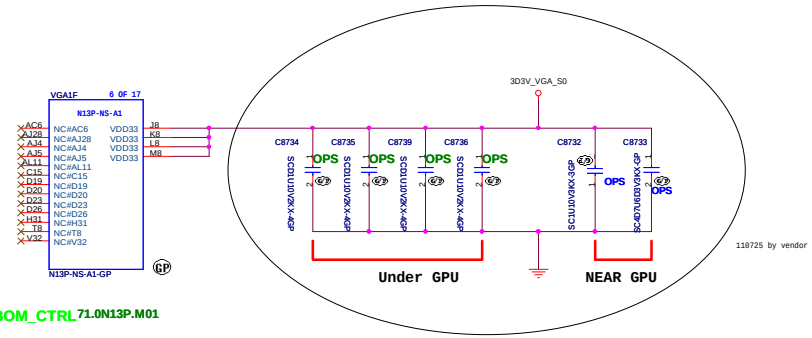
BOM_CTRL 71.0N13P.M01



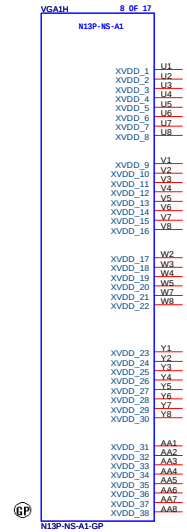
BOM_CTRL 71.0N13P.M01



BOM_CTRL 71.0N13P.M01



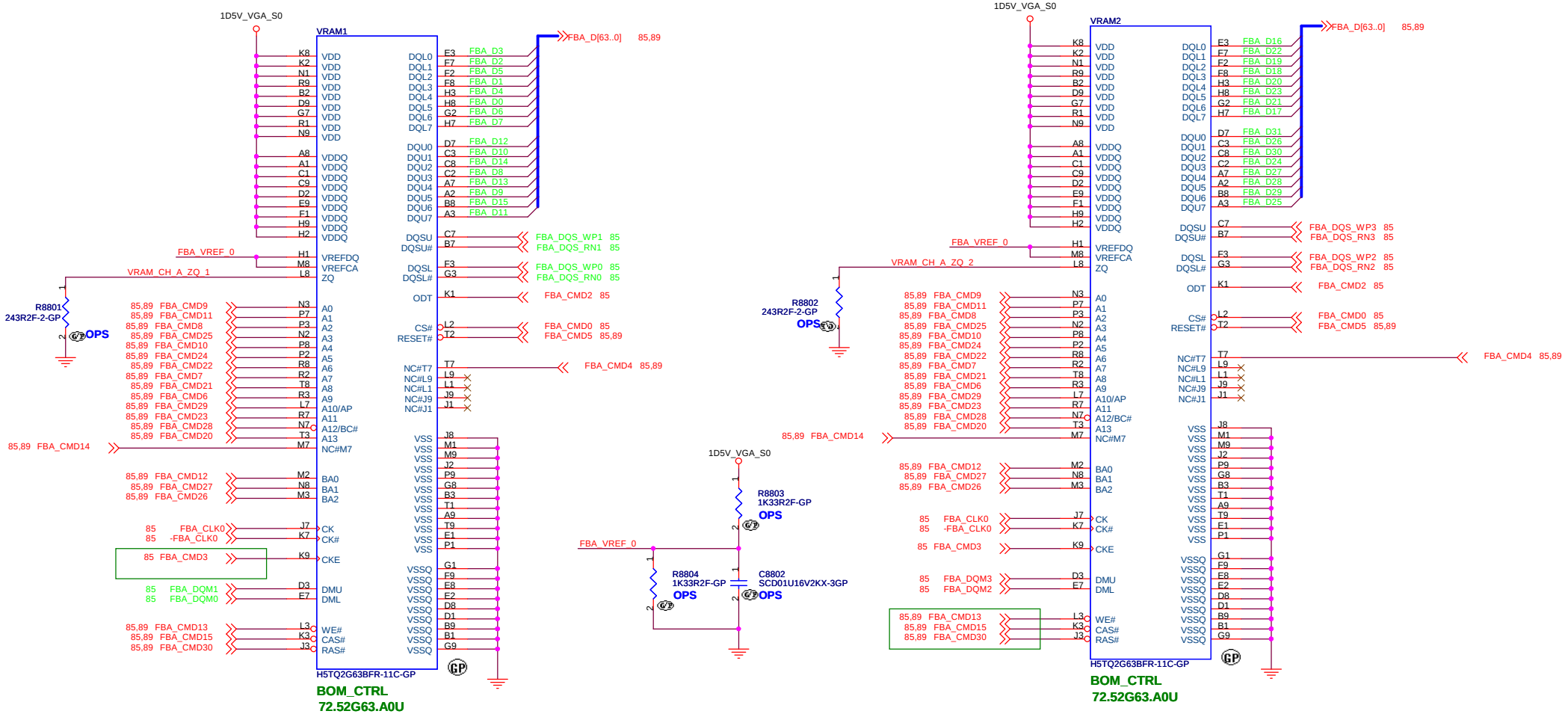
BOM_CTRL 71.0N13P.M01

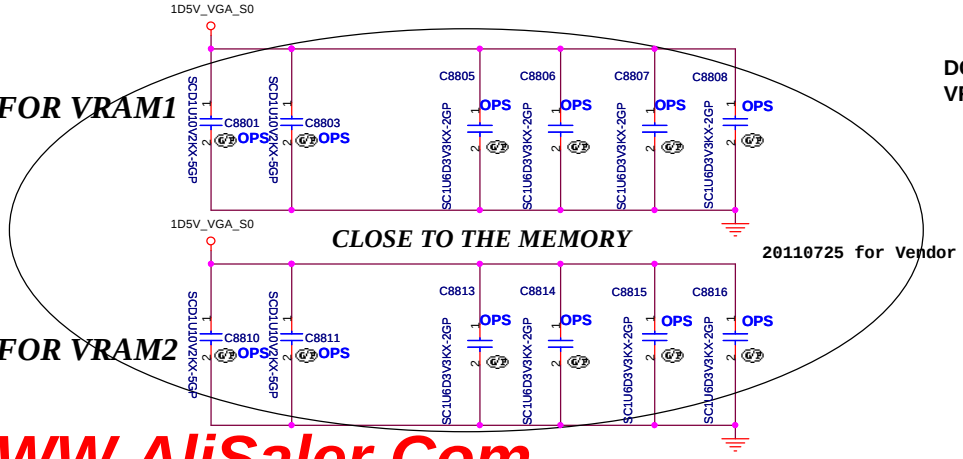


BOM_CTRL 71.0N13P.M01

JV10-CS

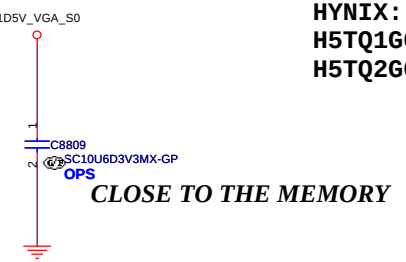
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	GPU (5/5): PWR/GND	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 87 of 103	





DG requires 4x0.1uF and 8x1.0uF per VRAM chip

20110725 for Vendor



VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

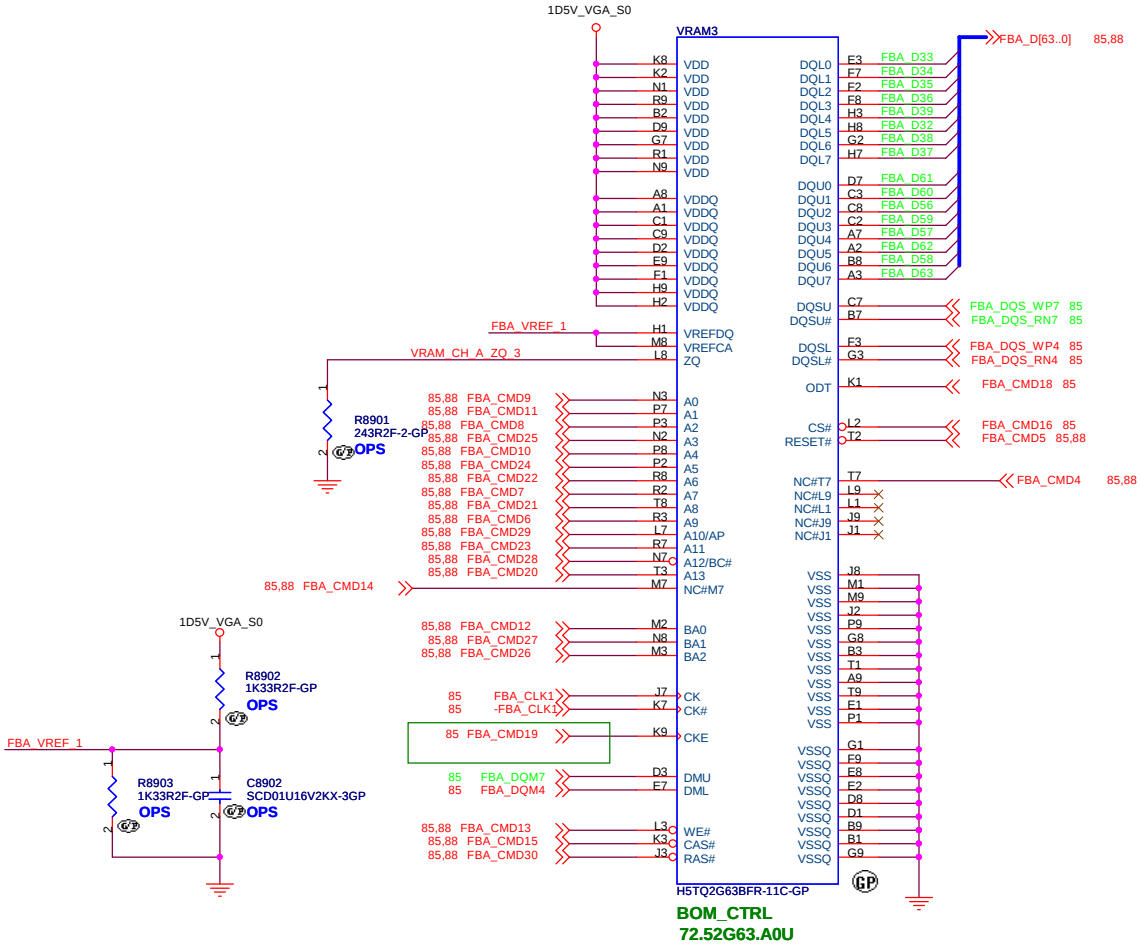
VIDEO FRAME BUFFER PORT A

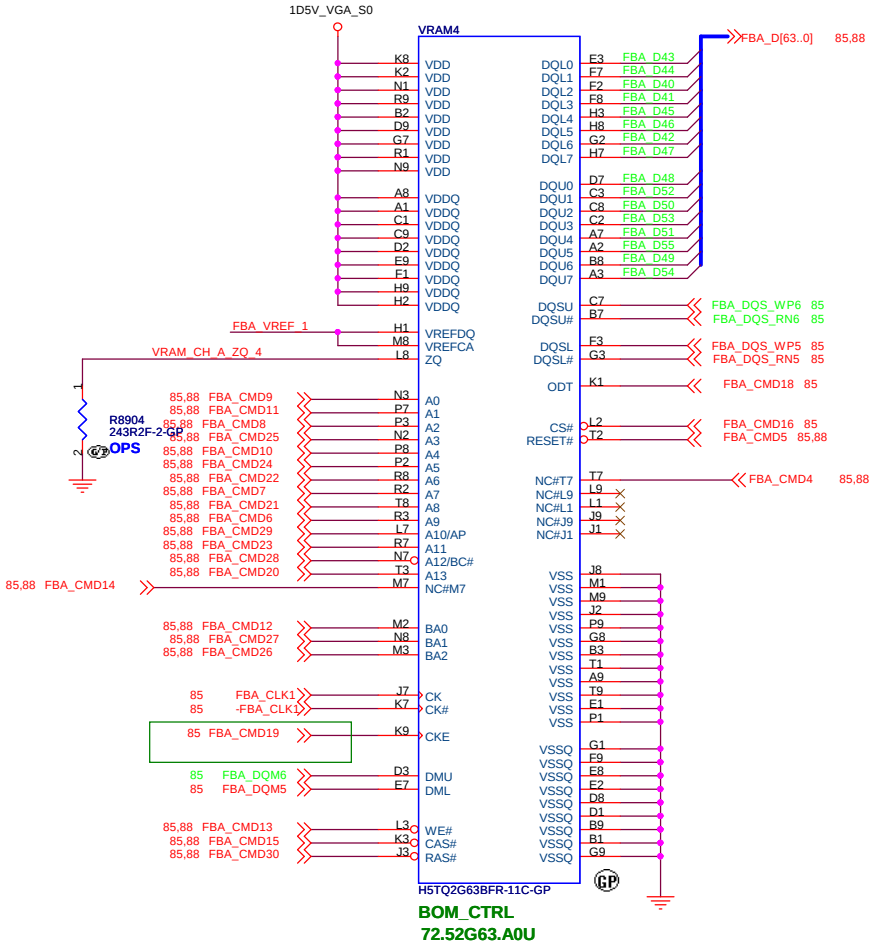
JV10-CS

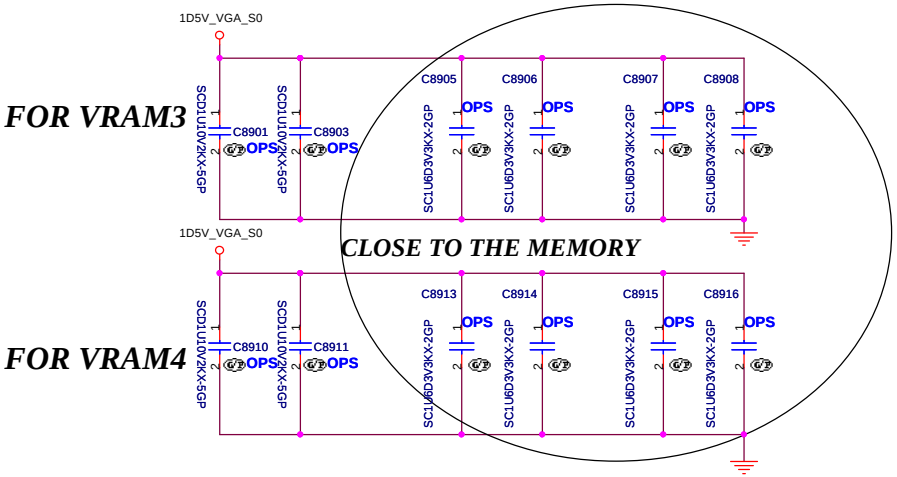
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

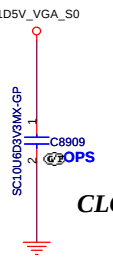
Title	*VRAM1,2 (1/4)*		
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 88 of 103		

WWW.AliSaler.Com









CLOSE TO THE MEMORY

VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

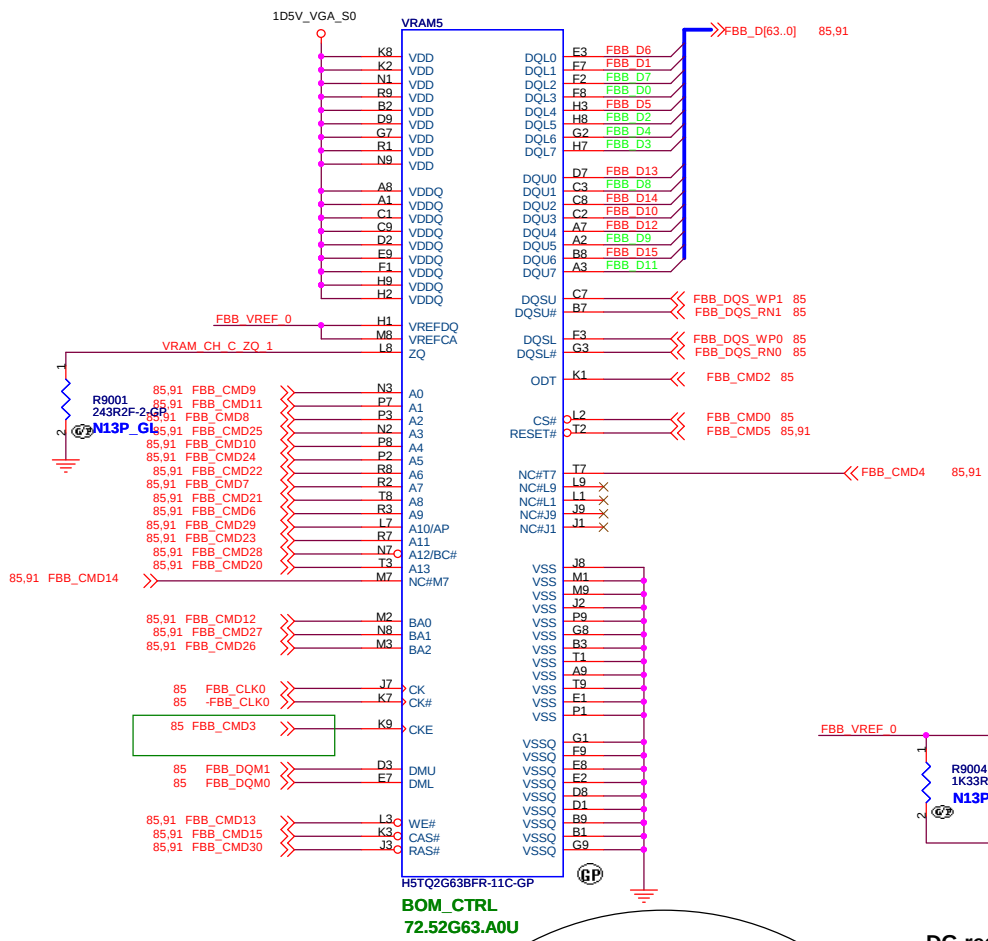
HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

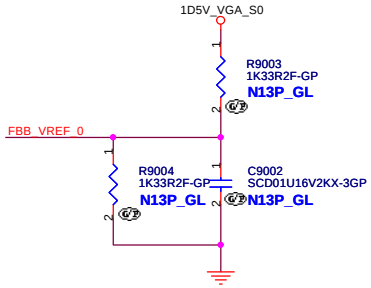
VIDEO FRAME BUFFER PORT A

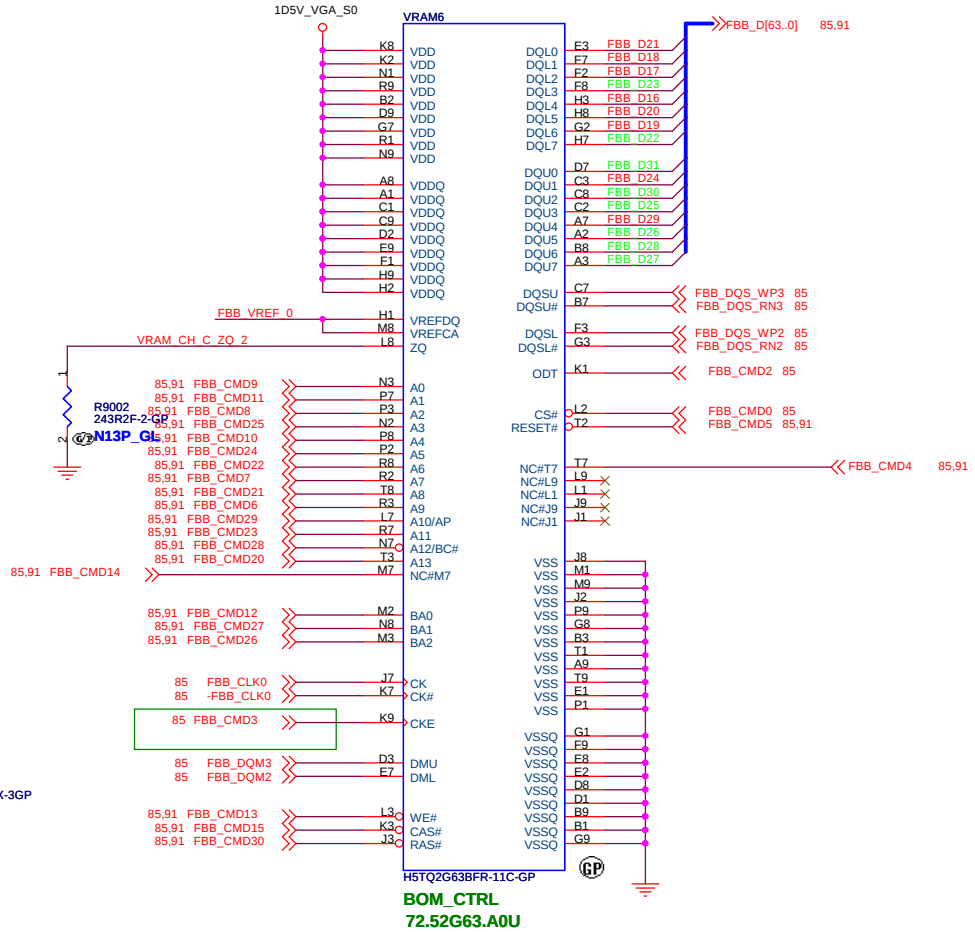
JV10-CS

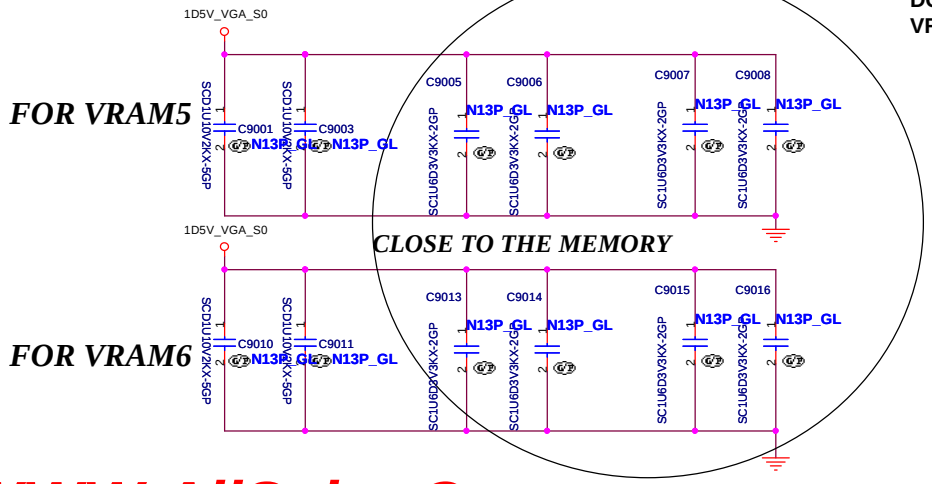
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM3,4 (2/4)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 89 of 103	

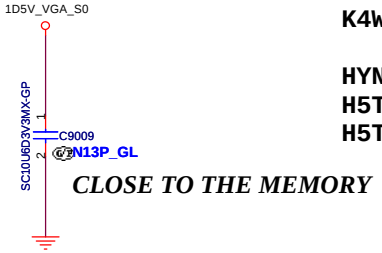








DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

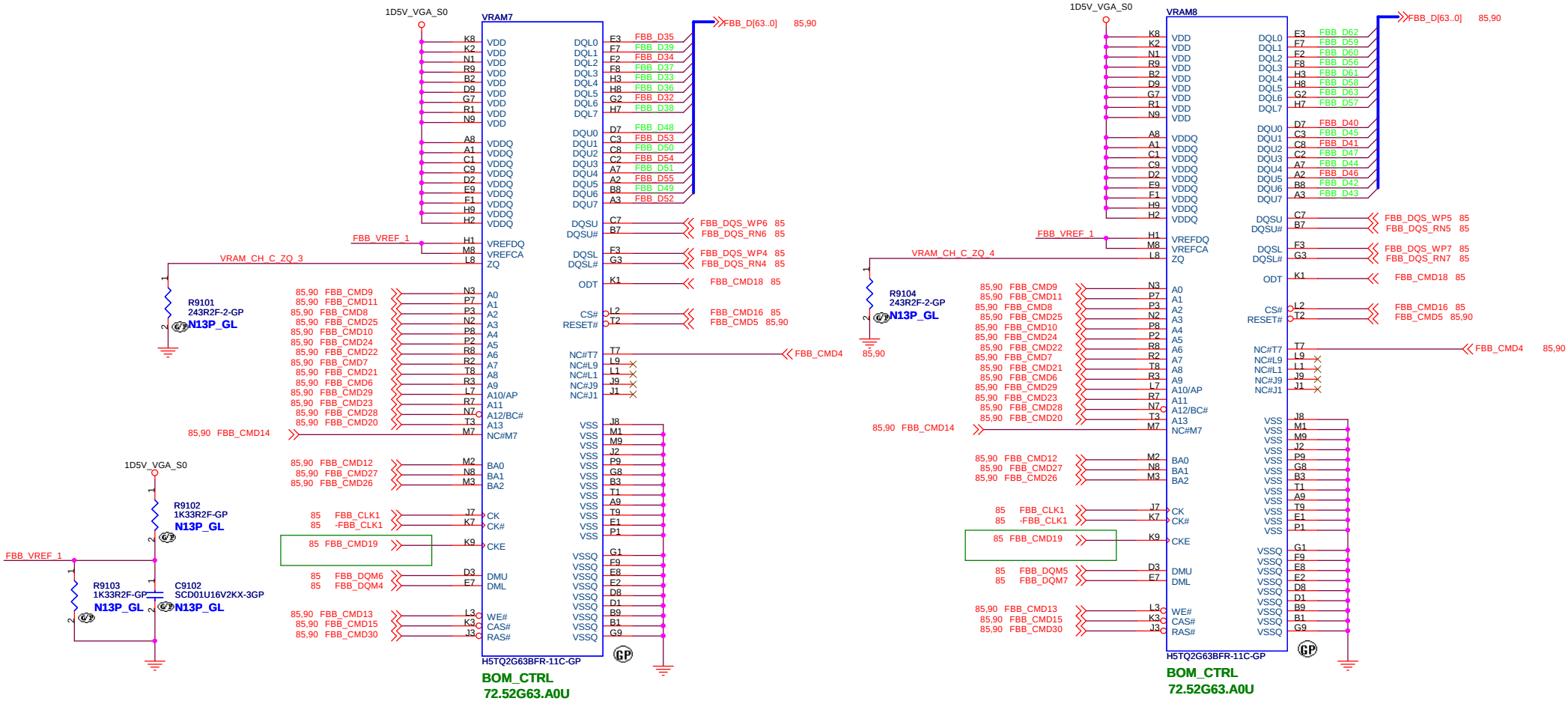
HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

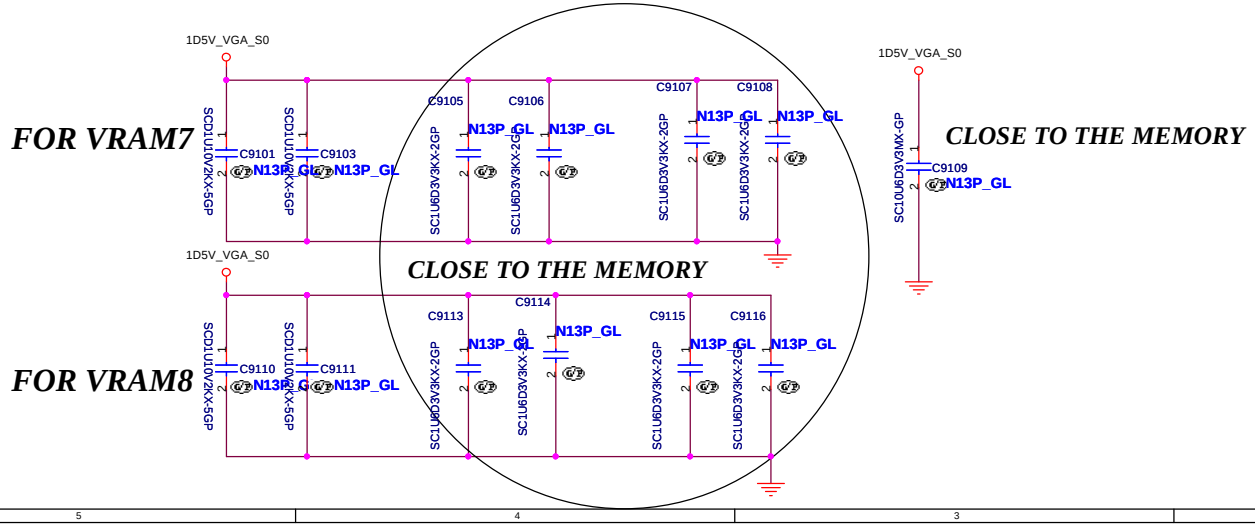
JV10-CS *VIDEO FRAME BUFFER PORT C*

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM5,6 (3/4)*	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 90 of 103	

WWW.AliSaler.Com





VRAM

SAMSUNG:

K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz

K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:

H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz

H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT C

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM7,8 (4/4)		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 91 of 103		

SSID = PWR.Plane.Regulator_VGACORE

NV_VID0-GPIO11
NV_VID1-GPIO5
NV_VID2-GPIO6
NV_VID3-GPIO1
NV_VID4-GPIO0
NV_VID5-GPIO13
NV_VID6-pull down to GND

VID[5..0]
101100 = 0.95 => N13P-GL
110010 = 0.875V => N13M-GE

Design current=

PU9202, PU9203 BOM CTRL

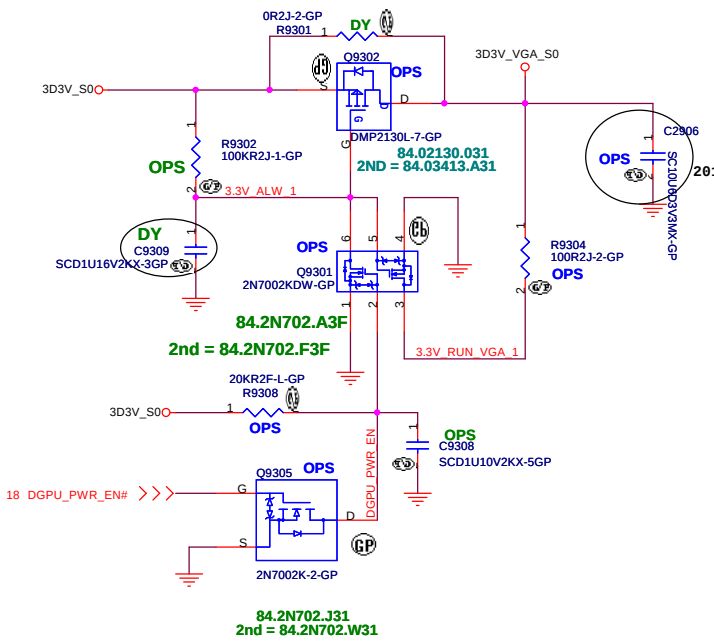
IMON
An analog output. IMON outputs a current proportional to the regulator output current.

Place near PL9201

WWW.AliSaler.Com

JV10-CS
緯創資通 Wistron Corporation
2Lf, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: ISL62882C_GPU_CORE
Size: Document Number: G48/G58 Rev: SC
Date: Friday, February 17, 2012 Sheet 92 of 103

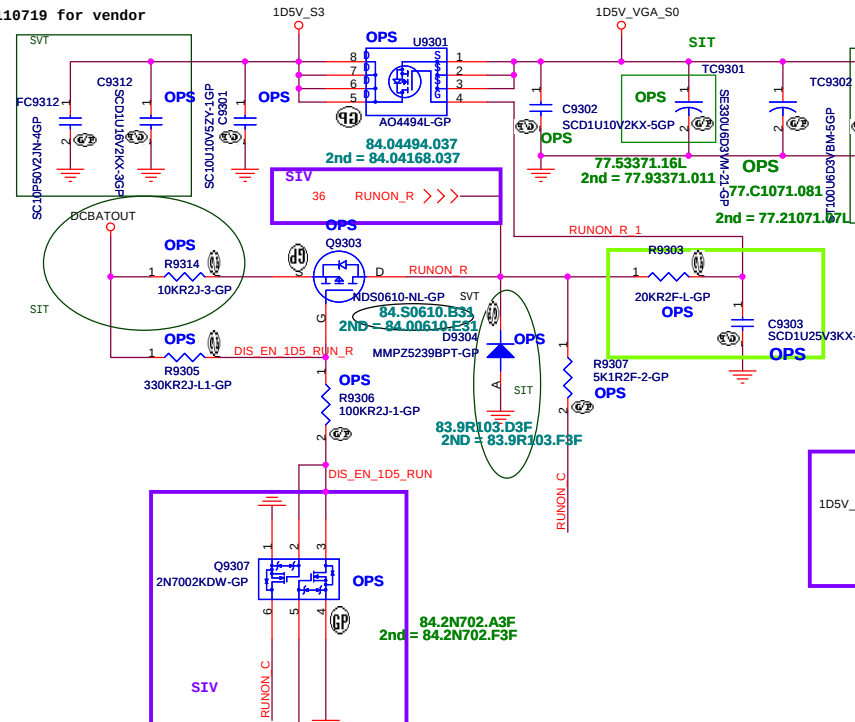
+3VS to 3.3V_DELAY Transfer



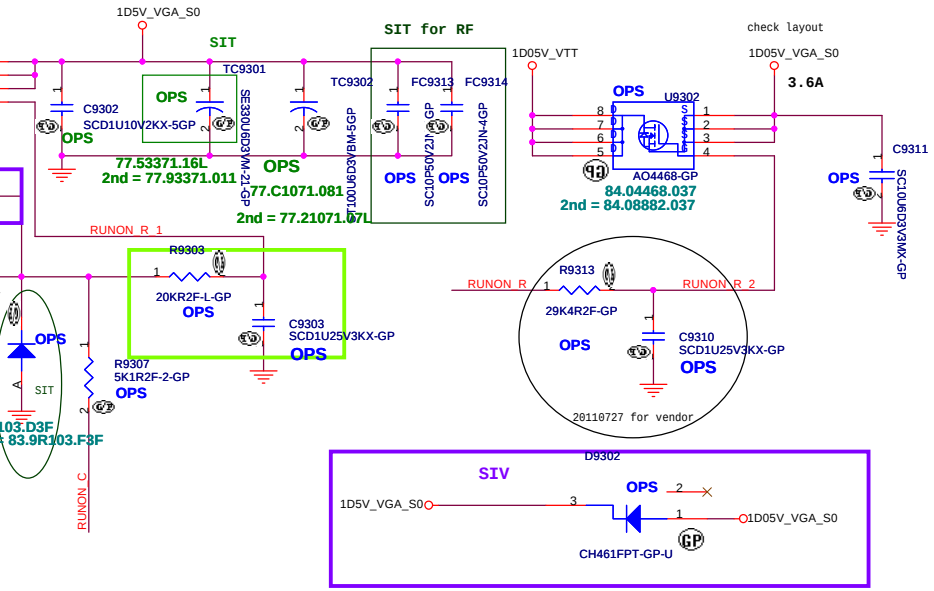
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm

20110719 for vendor

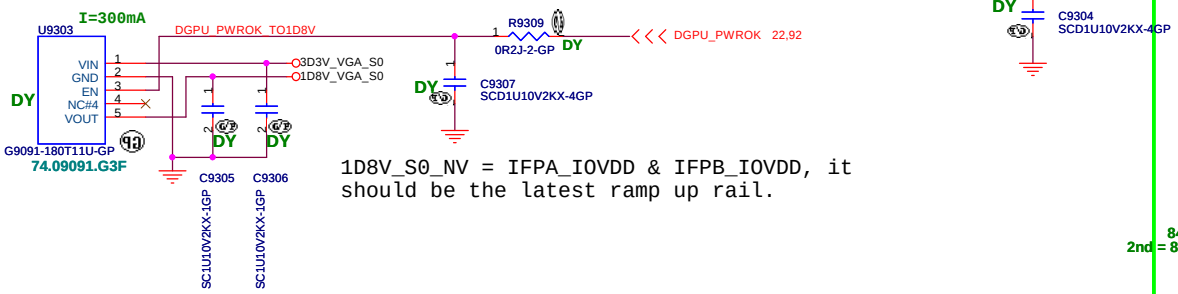
1D5V_VGA_S0



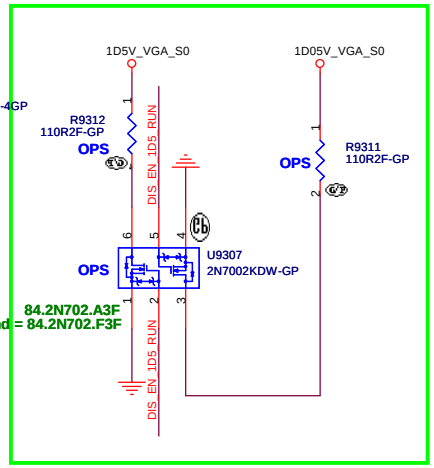
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 93 of 103	

(Blanking)

JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	(Reserved)SW GFX LCD(1/2)		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 94 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

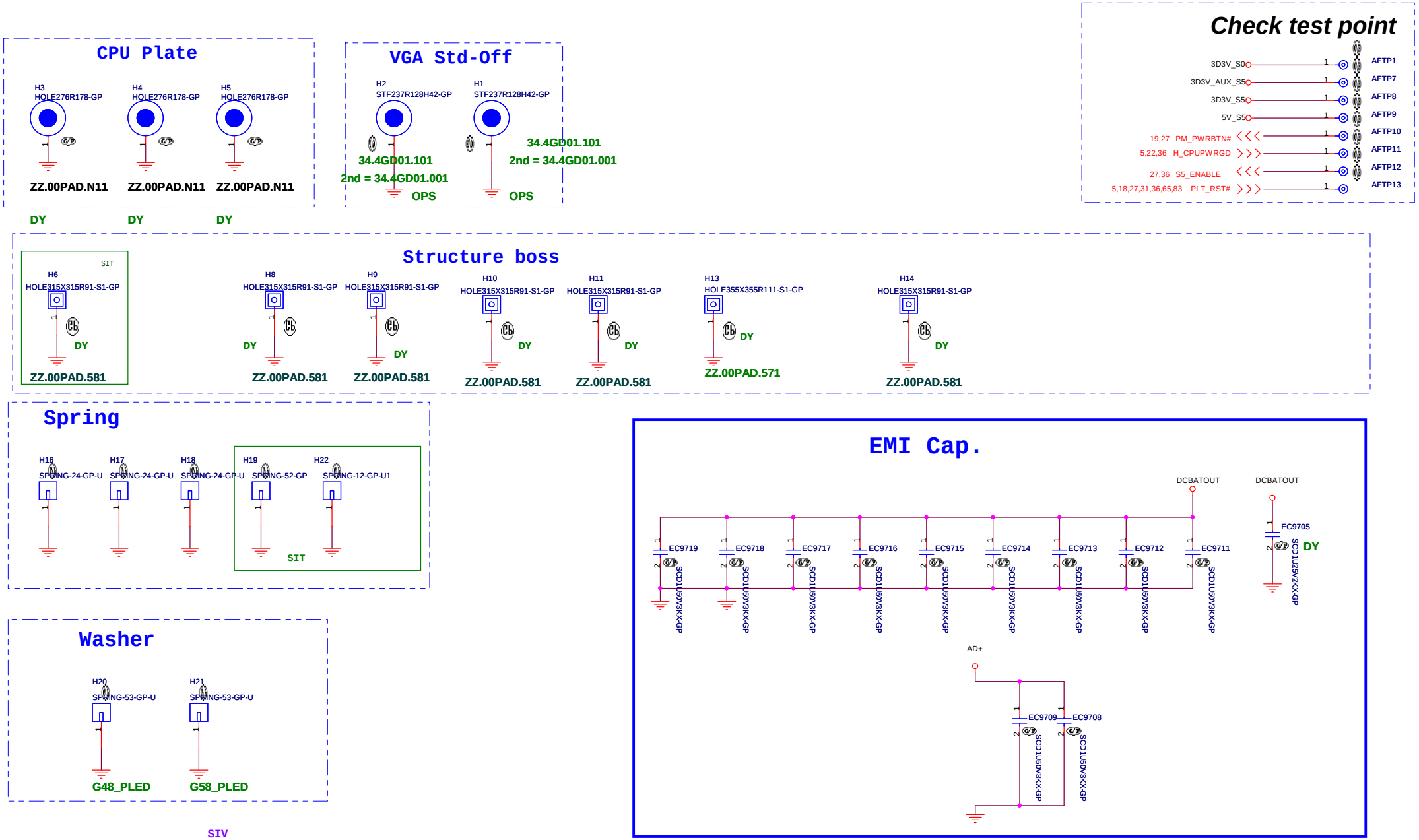
Title	*(Reserved)SW GFX CRT(2/2)*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 95 of 103	

(Blanking)

JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	(Reserved)Touch panel CONN		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 96 of 103	

WWW.AliSaler.Com



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	UNUSED PARTS/EMI Capacitors	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 97 of 103	

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Change-History		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 98 of 103	

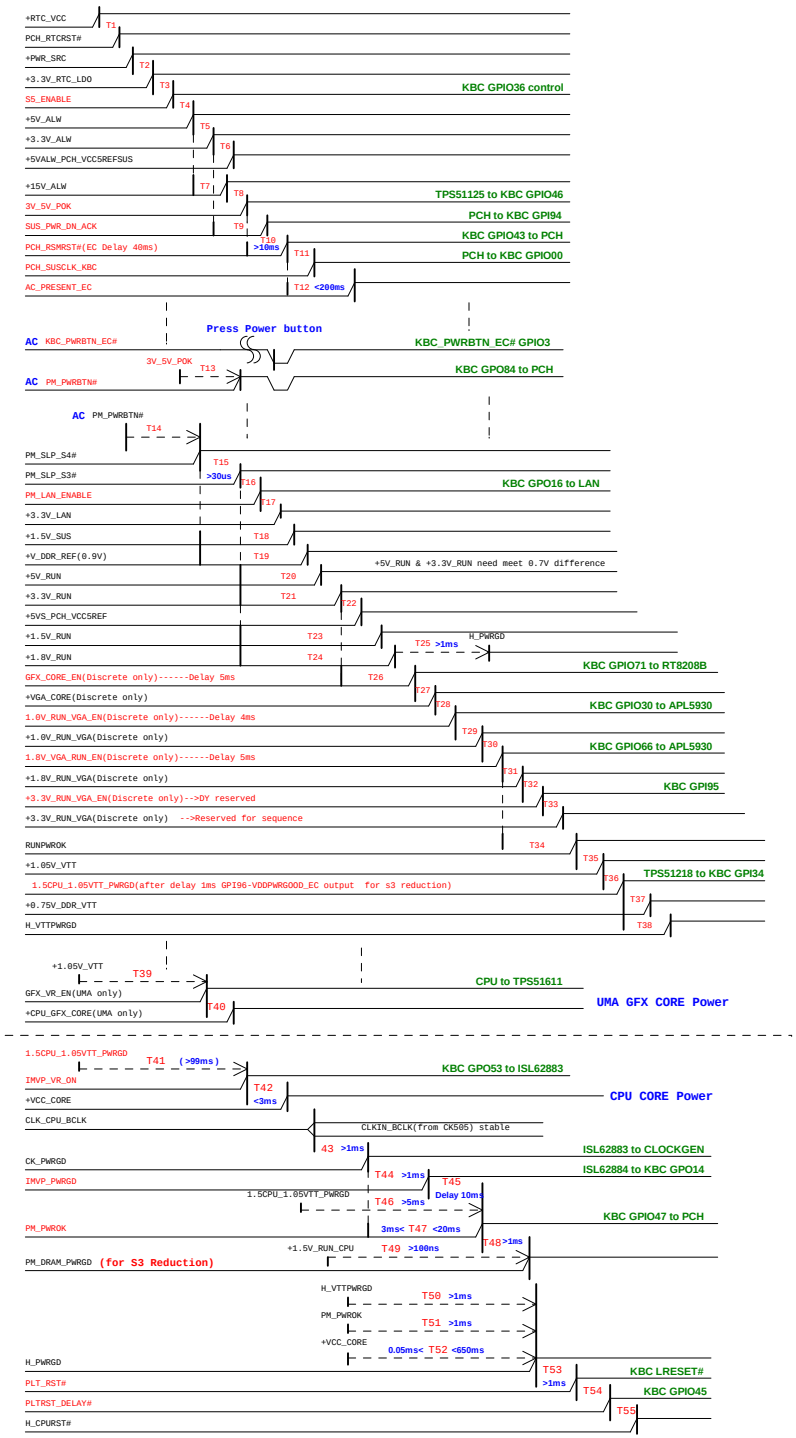
WWW.AliSaler.Com

Intel-Power Up Sequence

Not Update

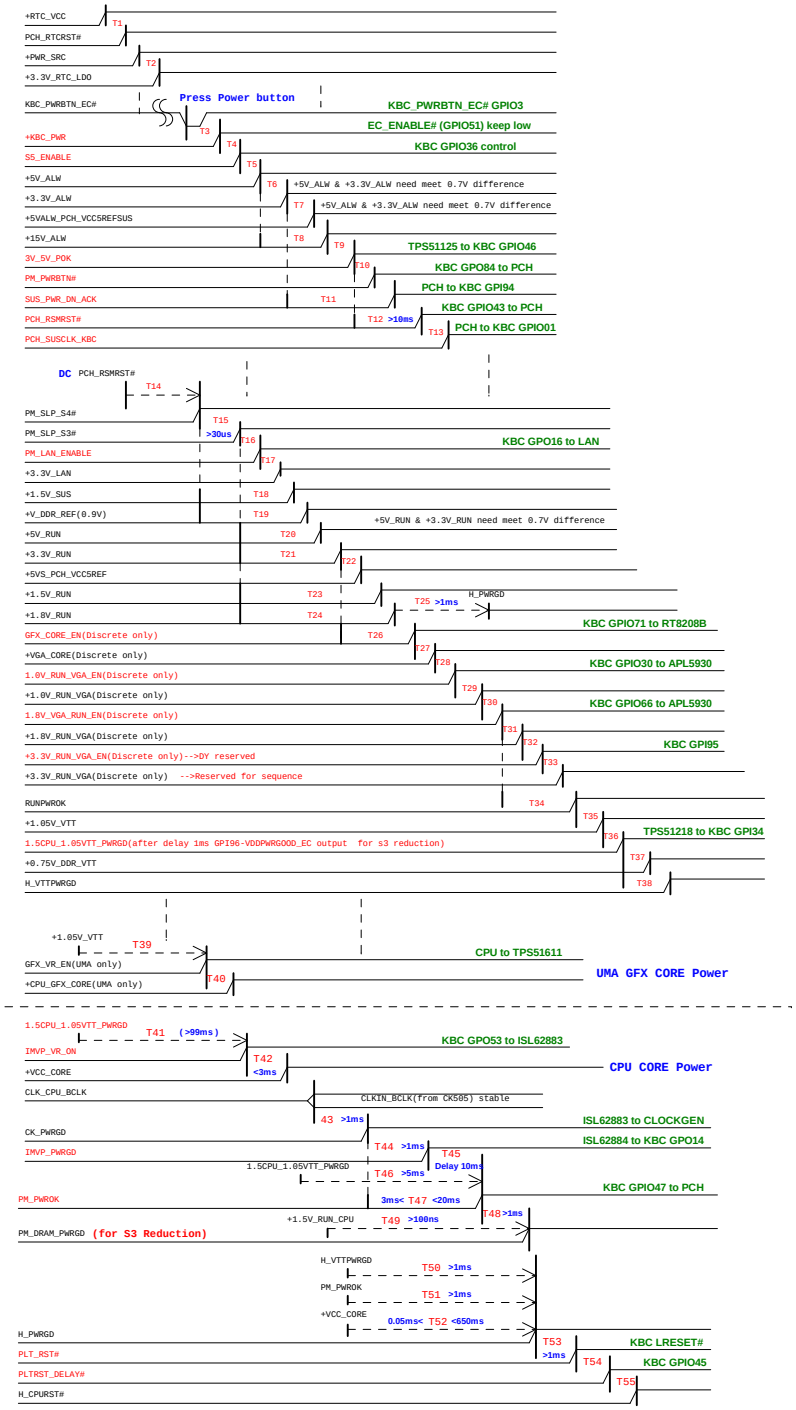
(AC mode)

red word: KBC GPIO



(DC mode)

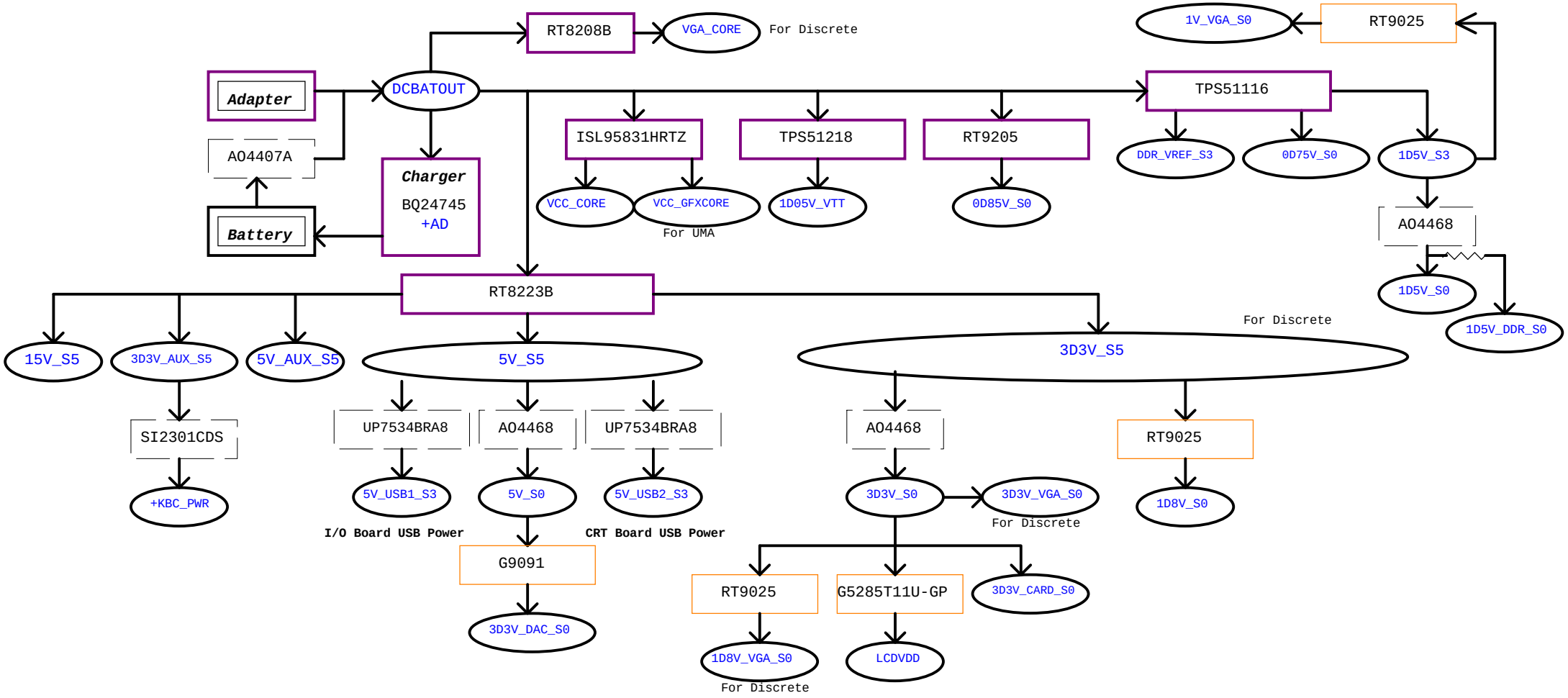
red word: KBC GPIO



JVID-C5

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: Power Sequence			
Size	Document Number: G48/G58		Rev: SC
Date: Friday, February 17, 2012	Sheet 99 of 103		

Not Update



Power Shape

Regulator	LDO	Switch

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

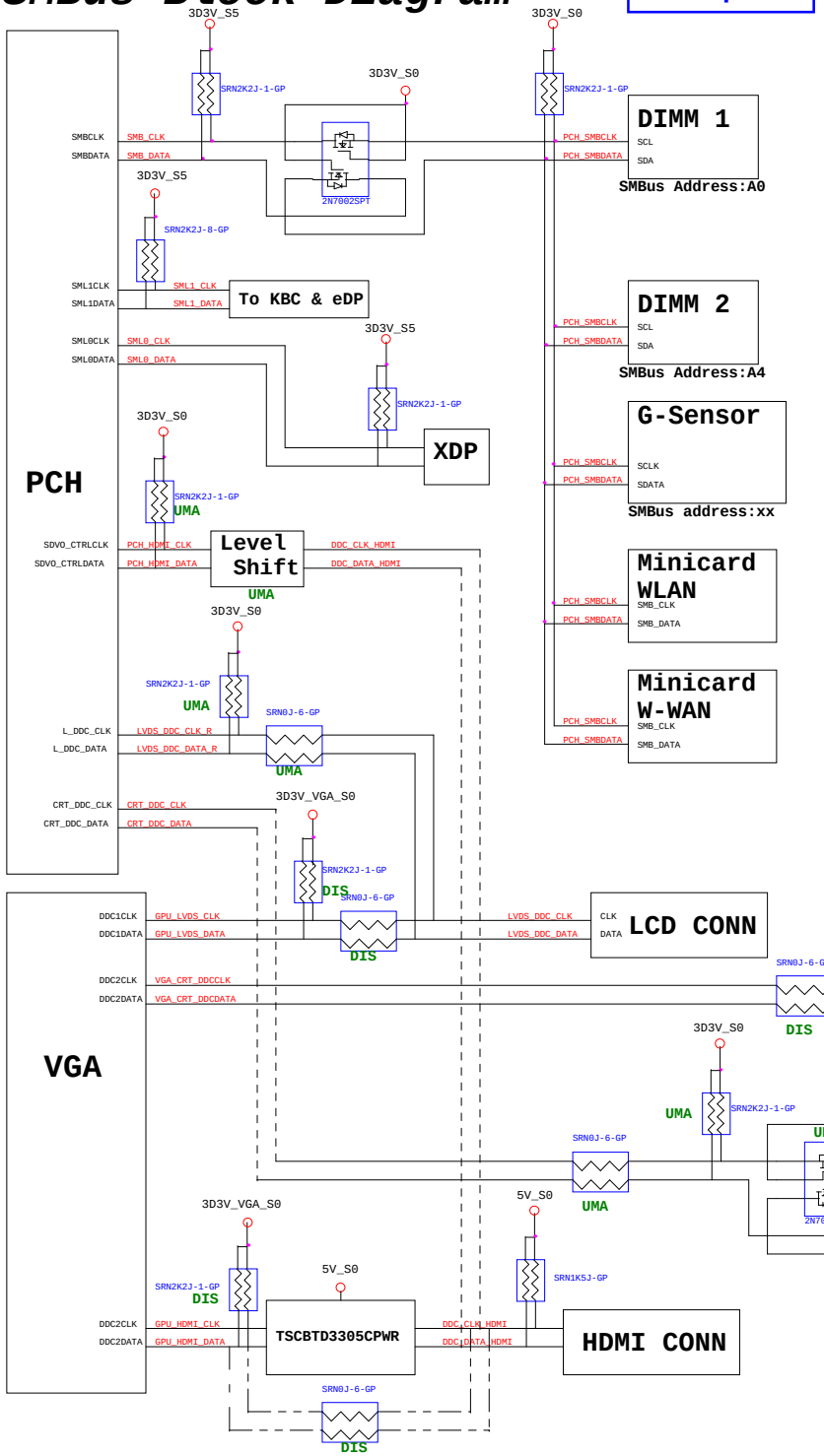
Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 100 of 103

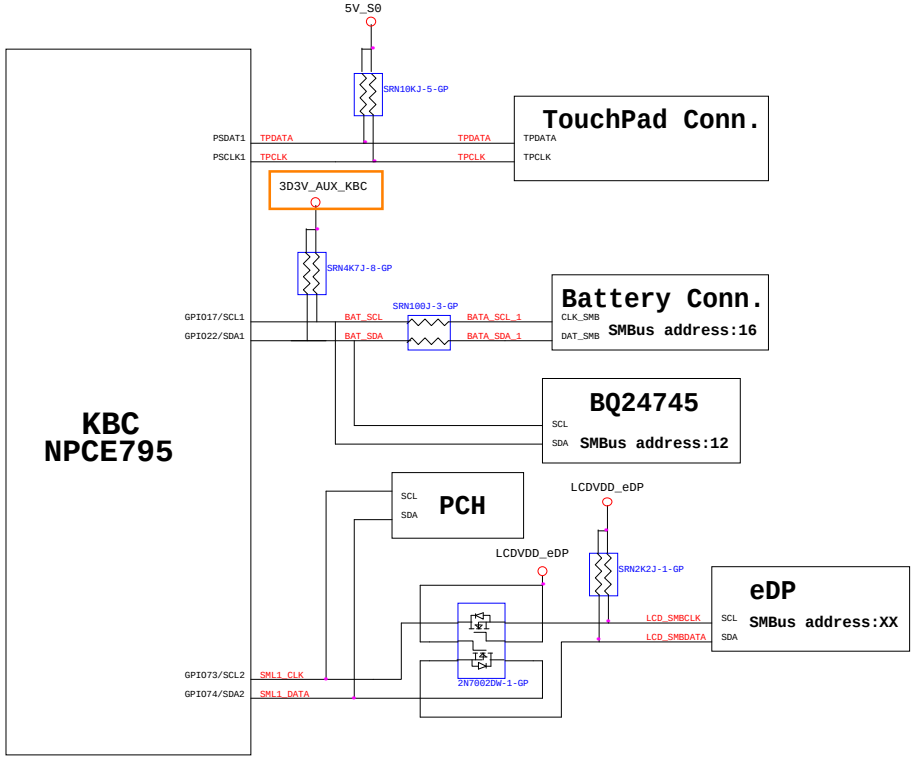
WWW.AliSaler.Com

PCH SMBus Block Diagram

Not Update



KBC SMBus Block Diagram



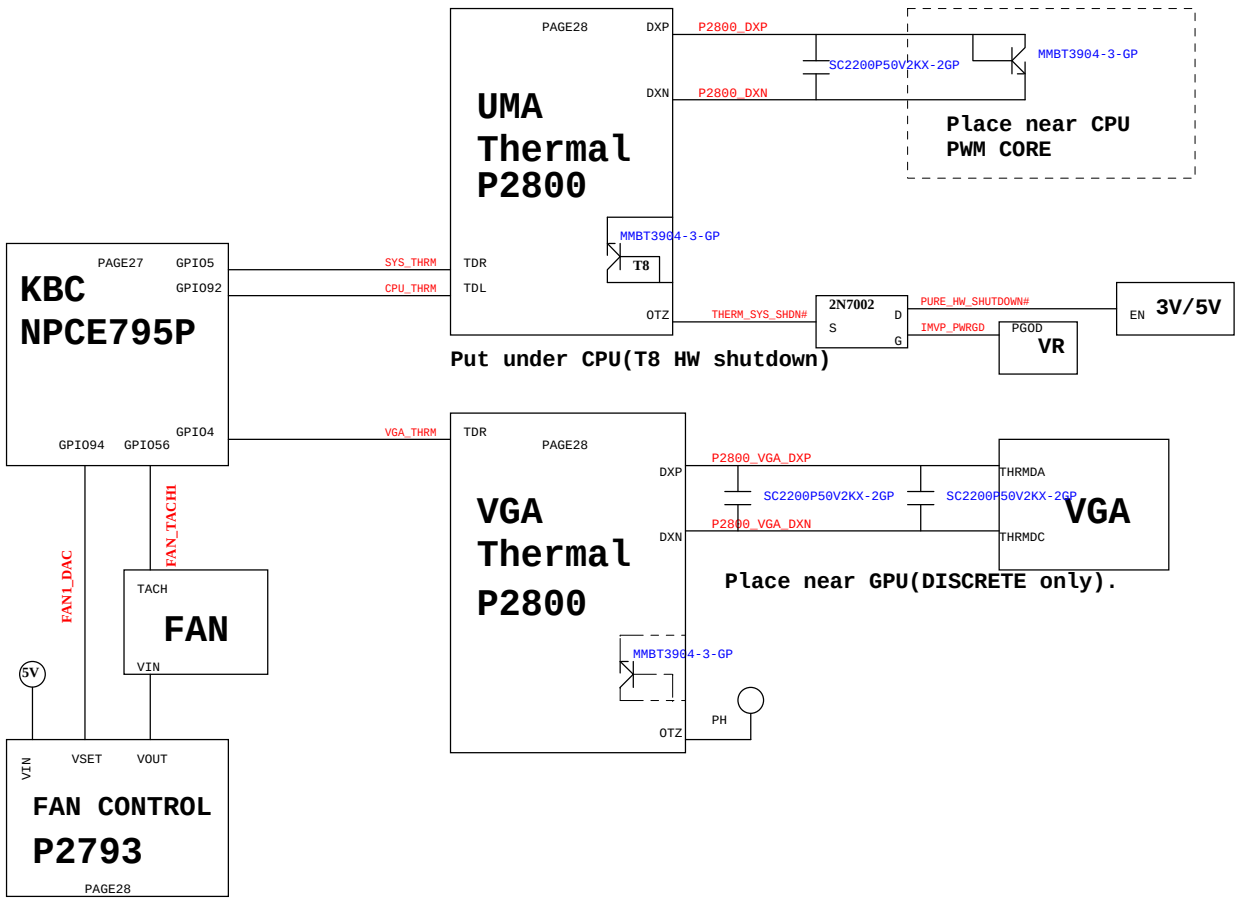
JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

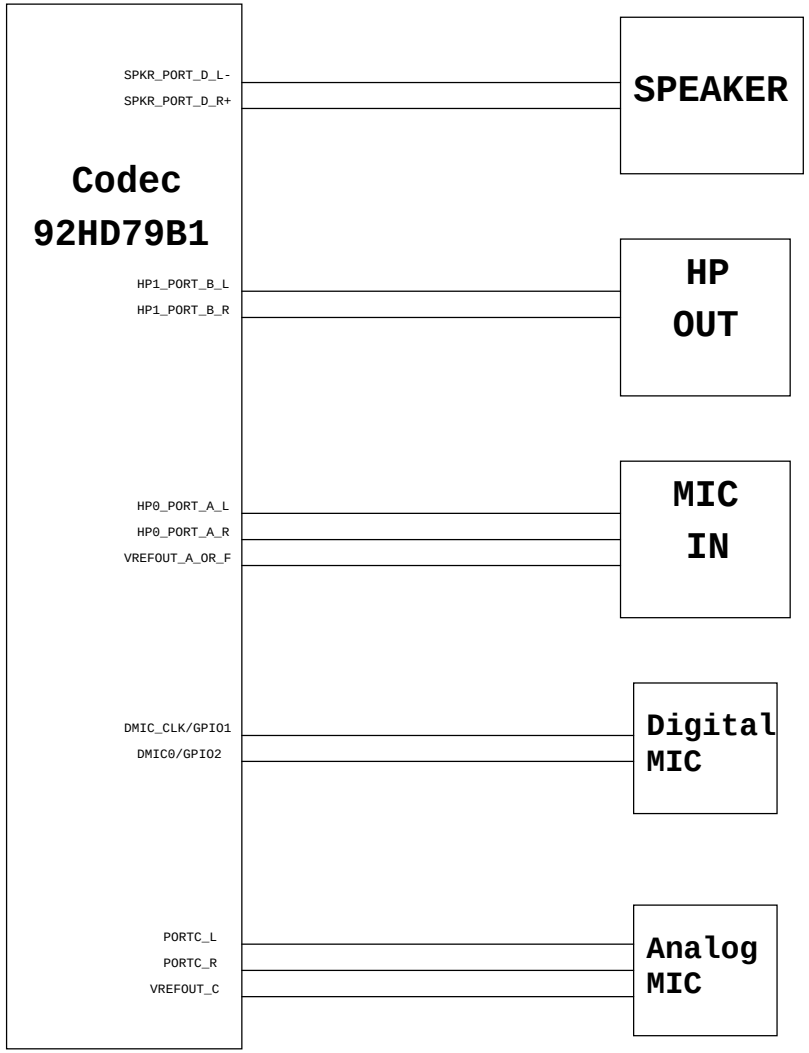
Title	SMBUS BLOCK DIAGRAM	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 101 of 103	

Thermal Block Diagram

Not Update



Audio Block Diagram



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	THERMAL/AUDIO BLOCK DIAGRAM	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 102 of 103	

WWW.AliSaler.Com

(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Change History**

Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 103 of 103