

Compal Confidential

YOGA Gloria 14" & 15" DIS M/B Schematics Document

Intel KabyLake U Processor with DDR4
N16S-GTR-S(940) (23x23mm)

2016-6-6

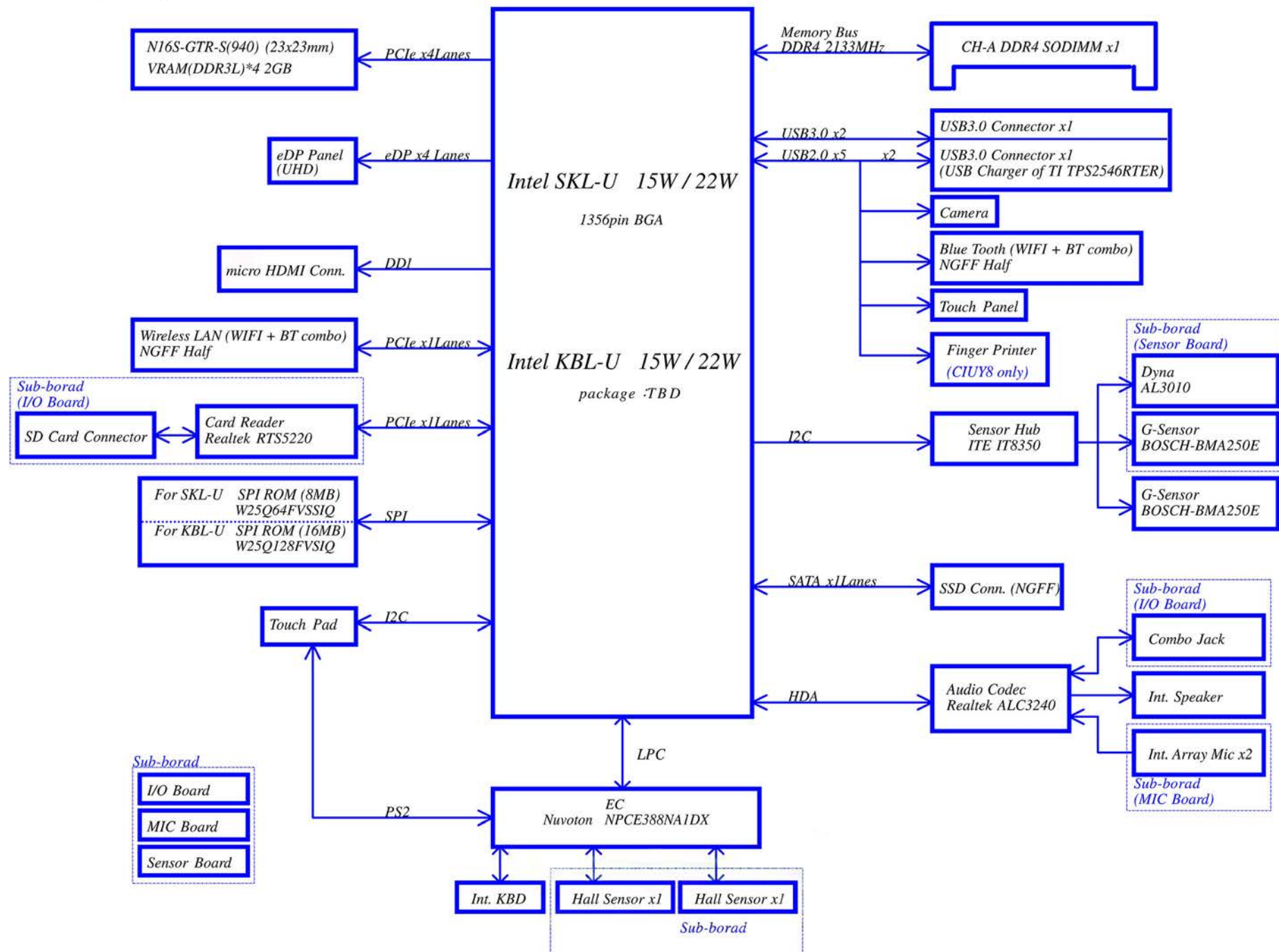
LA-D471P

REV : 2 . 0

ZZZ - BIU/2 PCB	
Part Number	Description
DAZ1JH00100	PCB BIU/2 LA-D471P LS-D471P/D472/D473 02

PCB#

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				LA-D471P	
				Date: Thursday, October 20, 2016	Sheet 1 of 53



BIVS3/ VE3 -PowerMap_SKL-U22_DDR3L_Volume_NON CS]



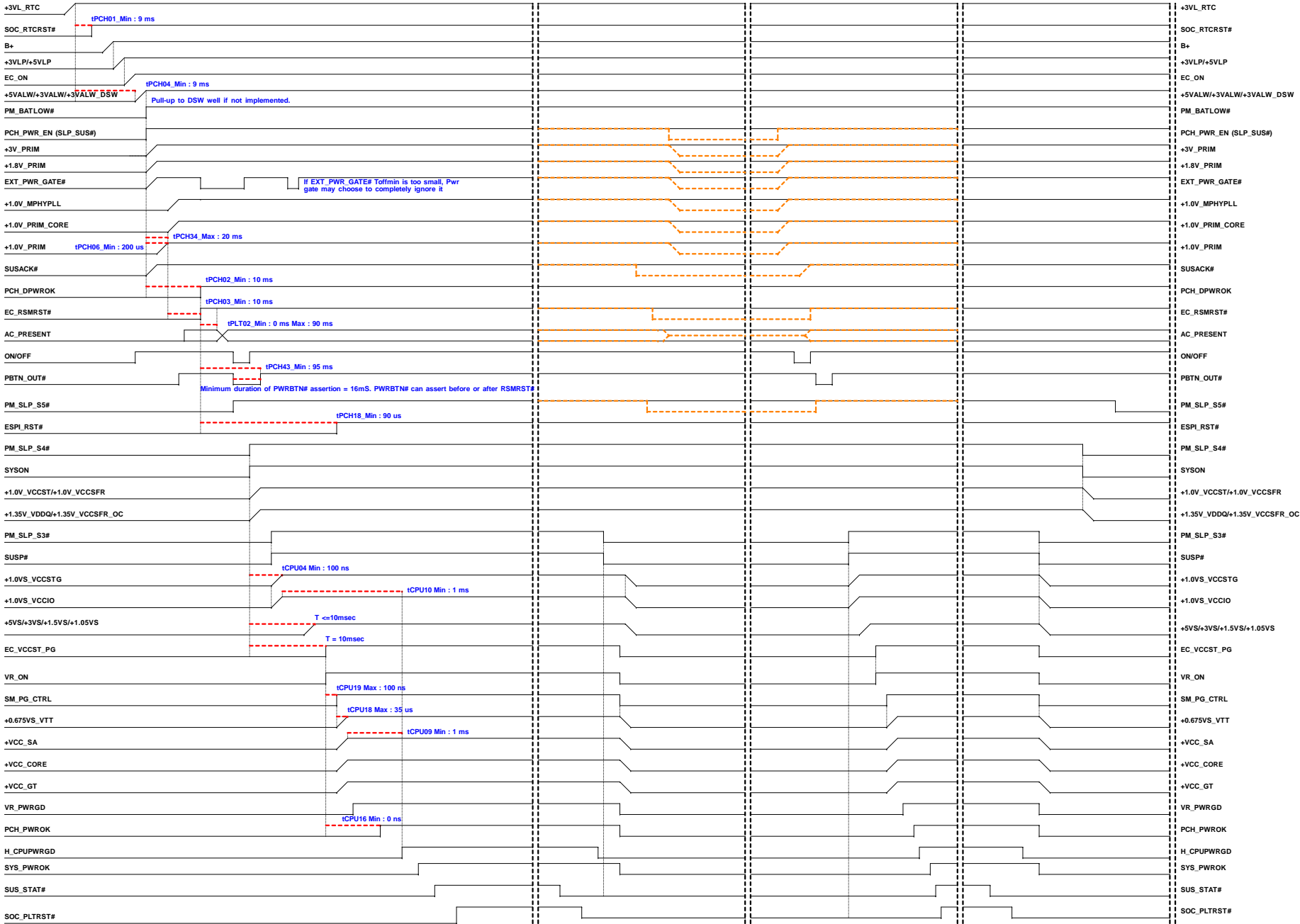
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Date:	Monday, June 08, 2016		Sheet	4 of 53	

G3->S0

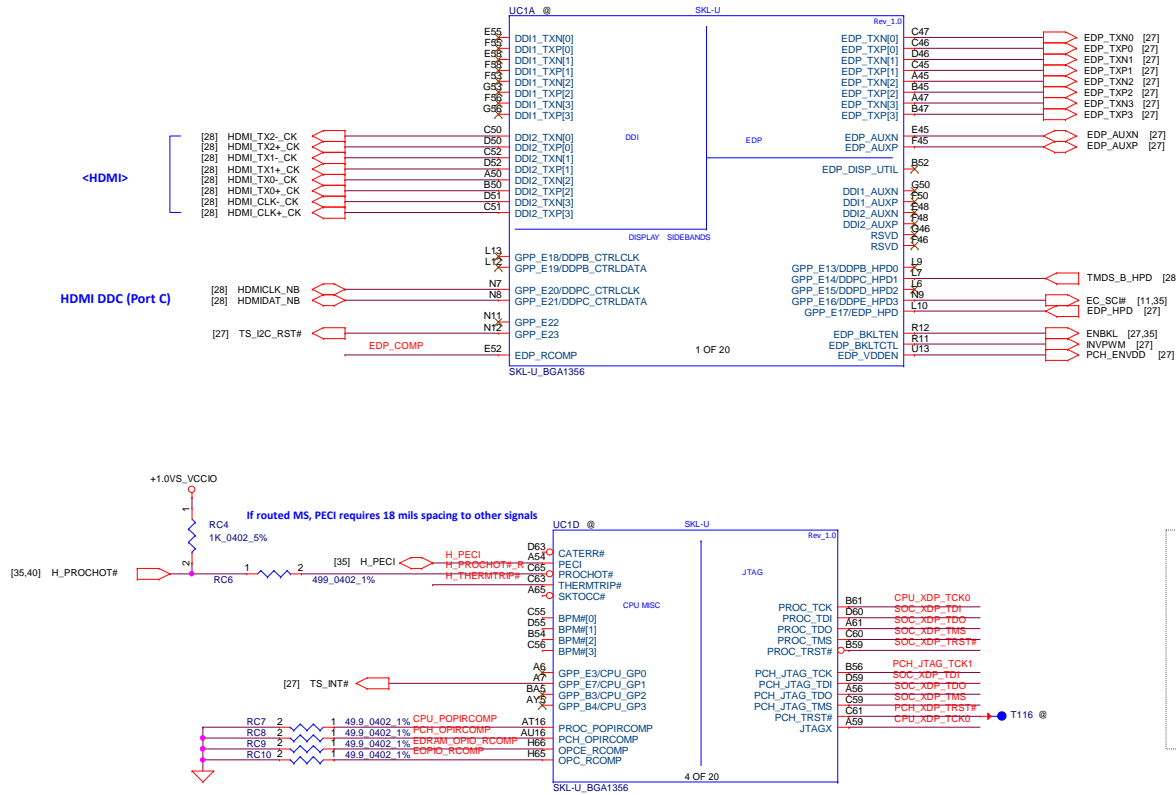
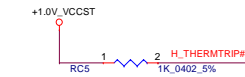
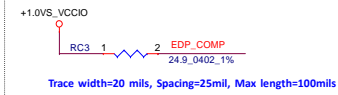
S0->S3/DS3

S0/DS3->S0

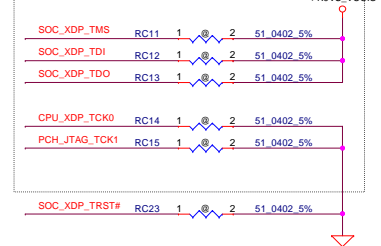
S0->S5



< Compensation PUF for eDP >



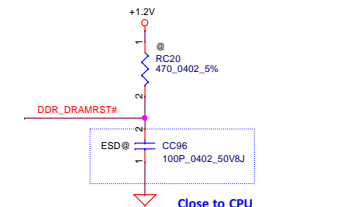
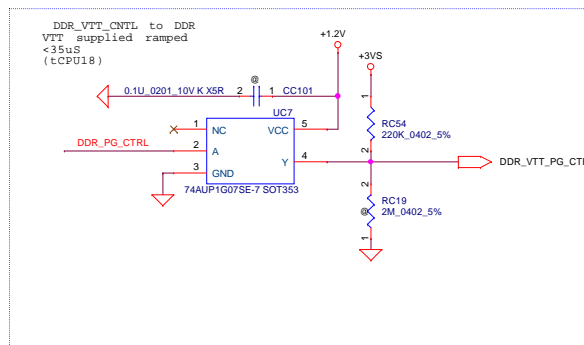
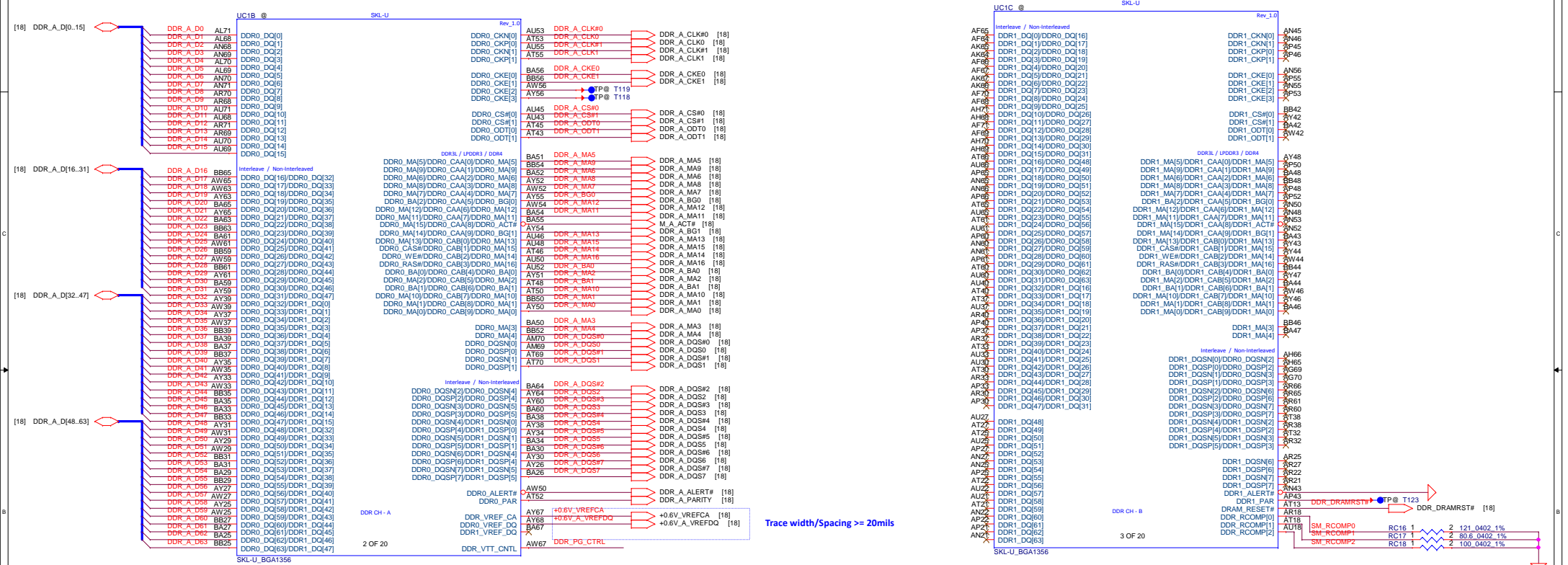
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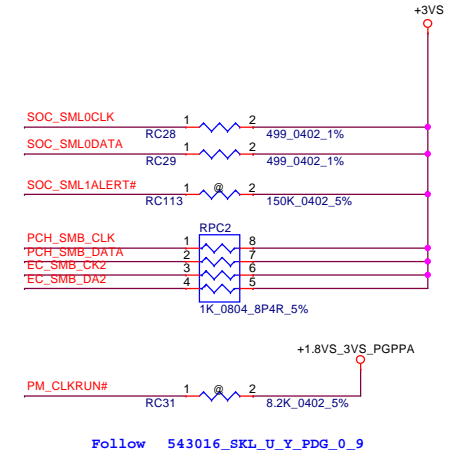
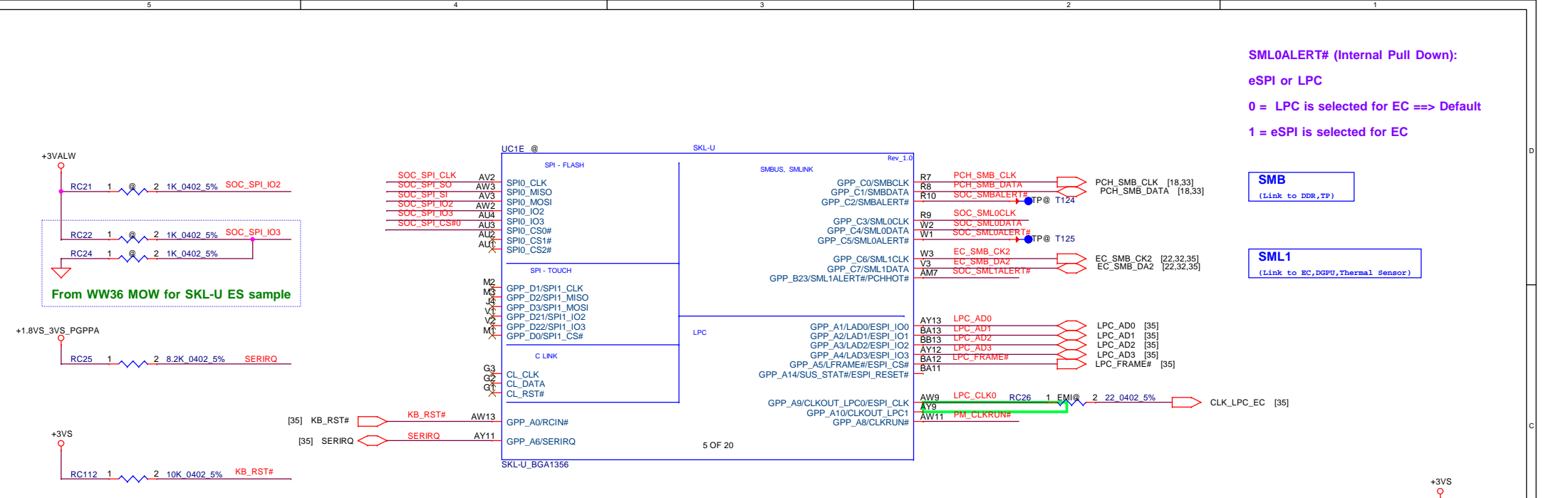
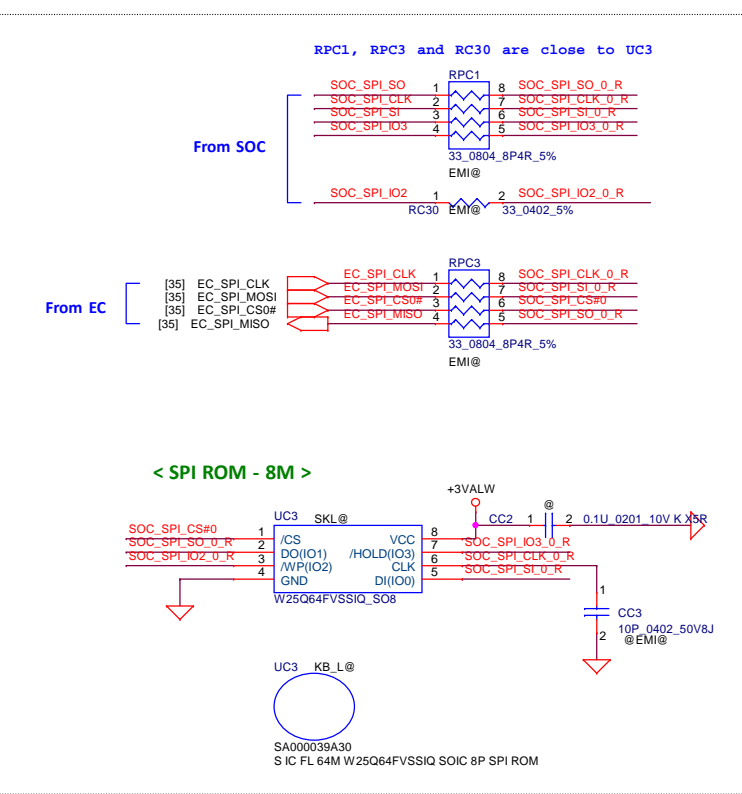
- UC1
SA0000A3700
S IC FJ8067702739739 QLDN H0 2.5G C38
B_7200U @
- UC1
SA0000A3400
S IC FJ8067702739740 QLDN H0 2.7G BGA
I7_7500U @
- UC1
SA0000A3800
S IC FJ8067702739738 QLDN H0 2.4G C38
B_7100U @

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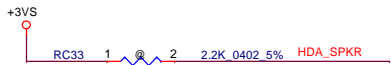
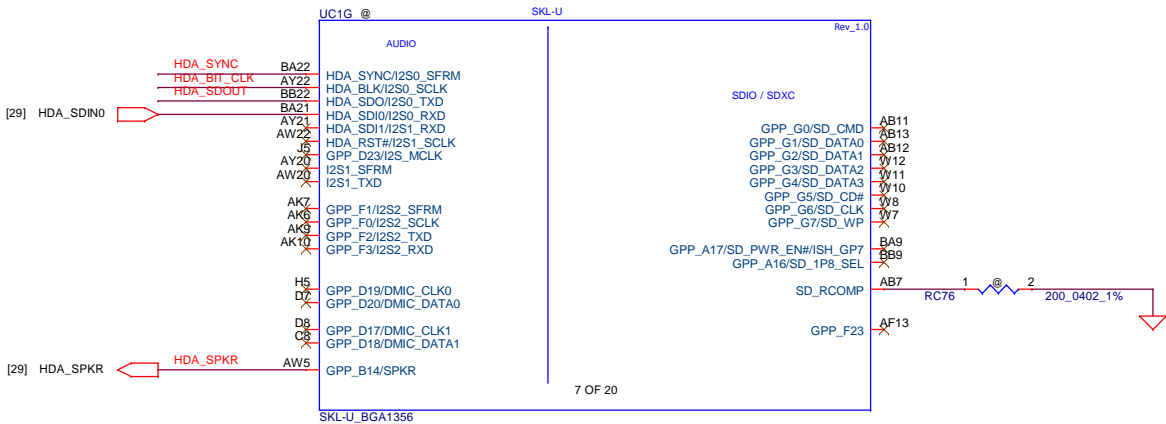
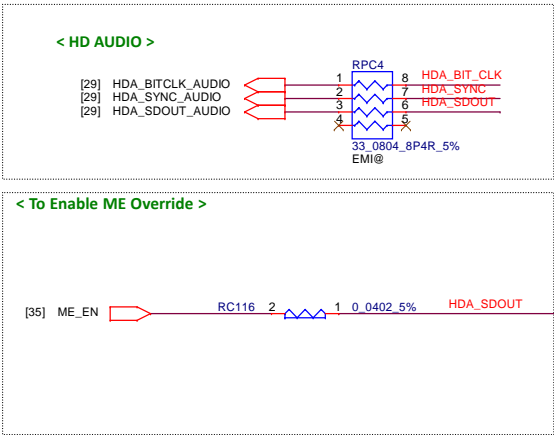
Interleaved Memory



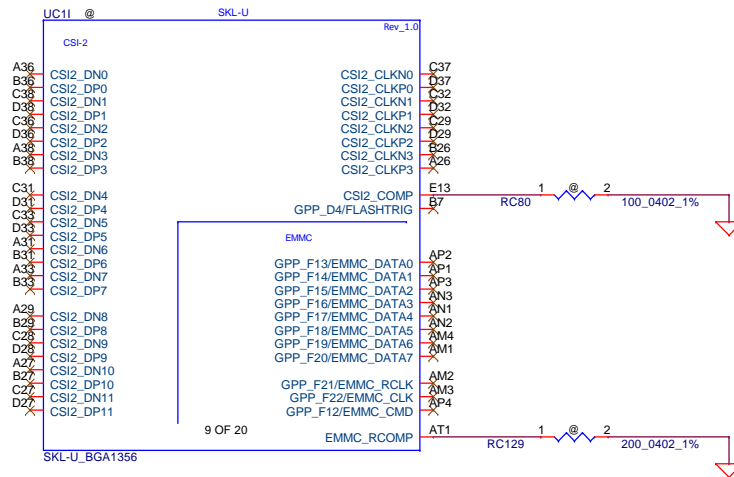
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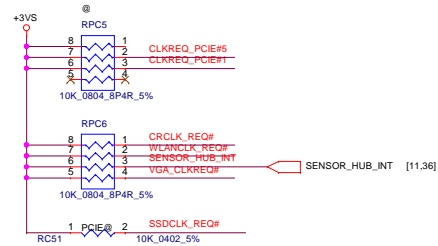
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SPKR (Internal Pull Down):
TOP Swap Override
0 = Disable TOP Swap mode. ==> Default
1 = Enable TOP Swap Mode.



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DGPU

[19] CLK_PEG_VGA#
[19] CLK_PEG_VGA
[19] VGA_CLKREQ#

NGFF WL+BT (KEY E)

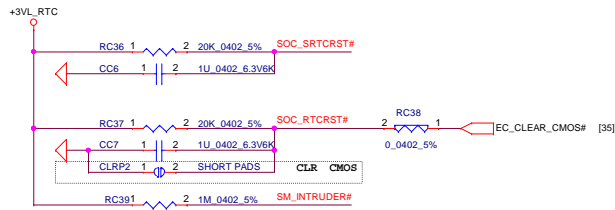
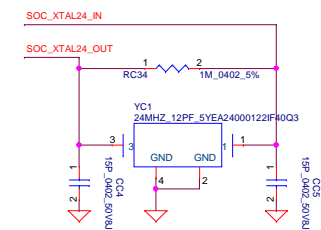
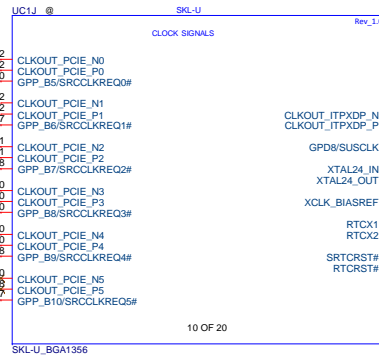
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[31] WLANCLK_REQ#

CardReader

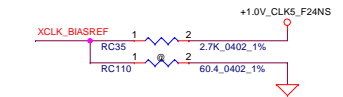
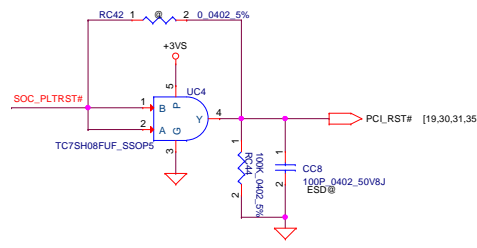
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SSD

[30] CLK_PCIE_SSD#
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[30] SSDCLK_REQ#



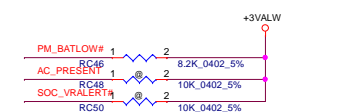
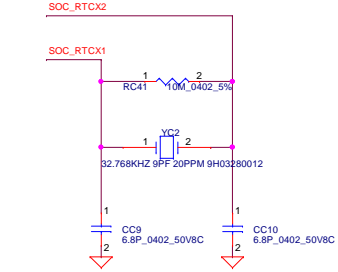
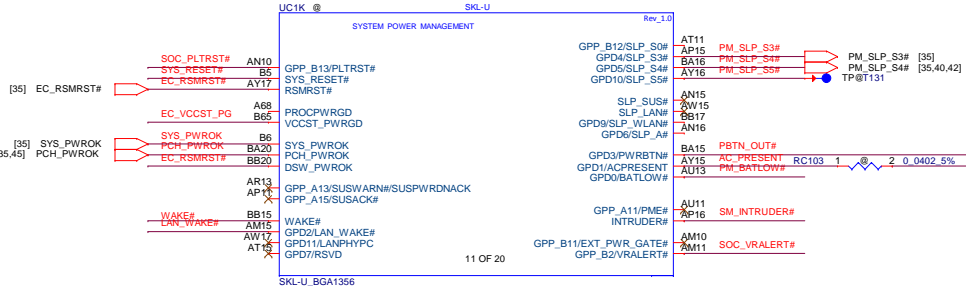
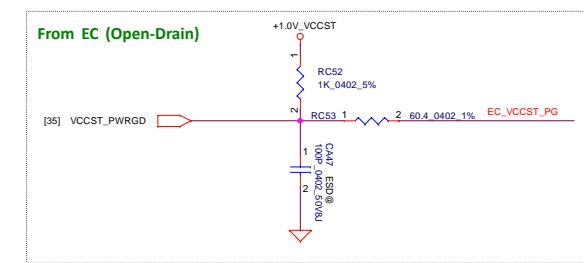
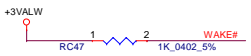
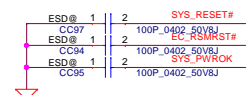
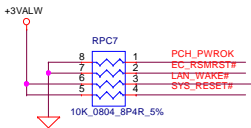
< PCH PLTRST Buffer >



Follow 546765_2014WW48_Skylake_MOW_Rev_1_0

Stuf f 2 7k oh r RC35 PUF or Skylake U

Stuf f 60.4 oh r RC110 PDF or CannonLake U



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				SKL-U(5/12)CLK,PM,GPIO	
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GPIO_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

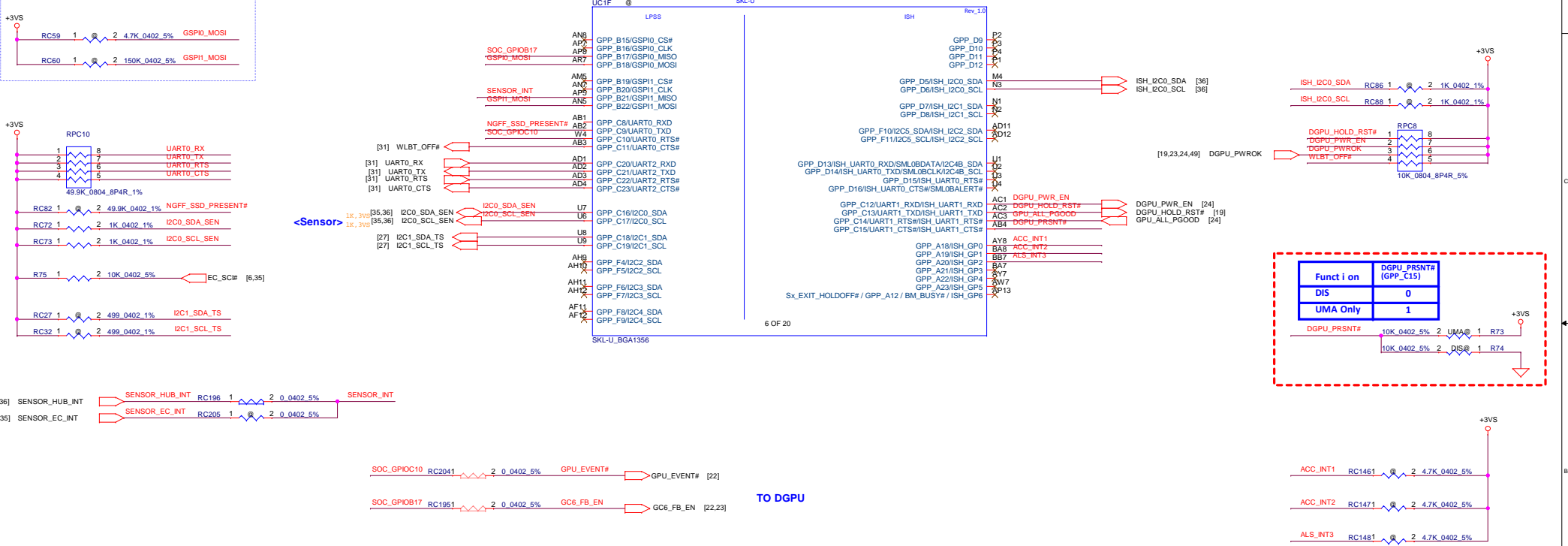
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i on is us d if u when running ITP/XDP.

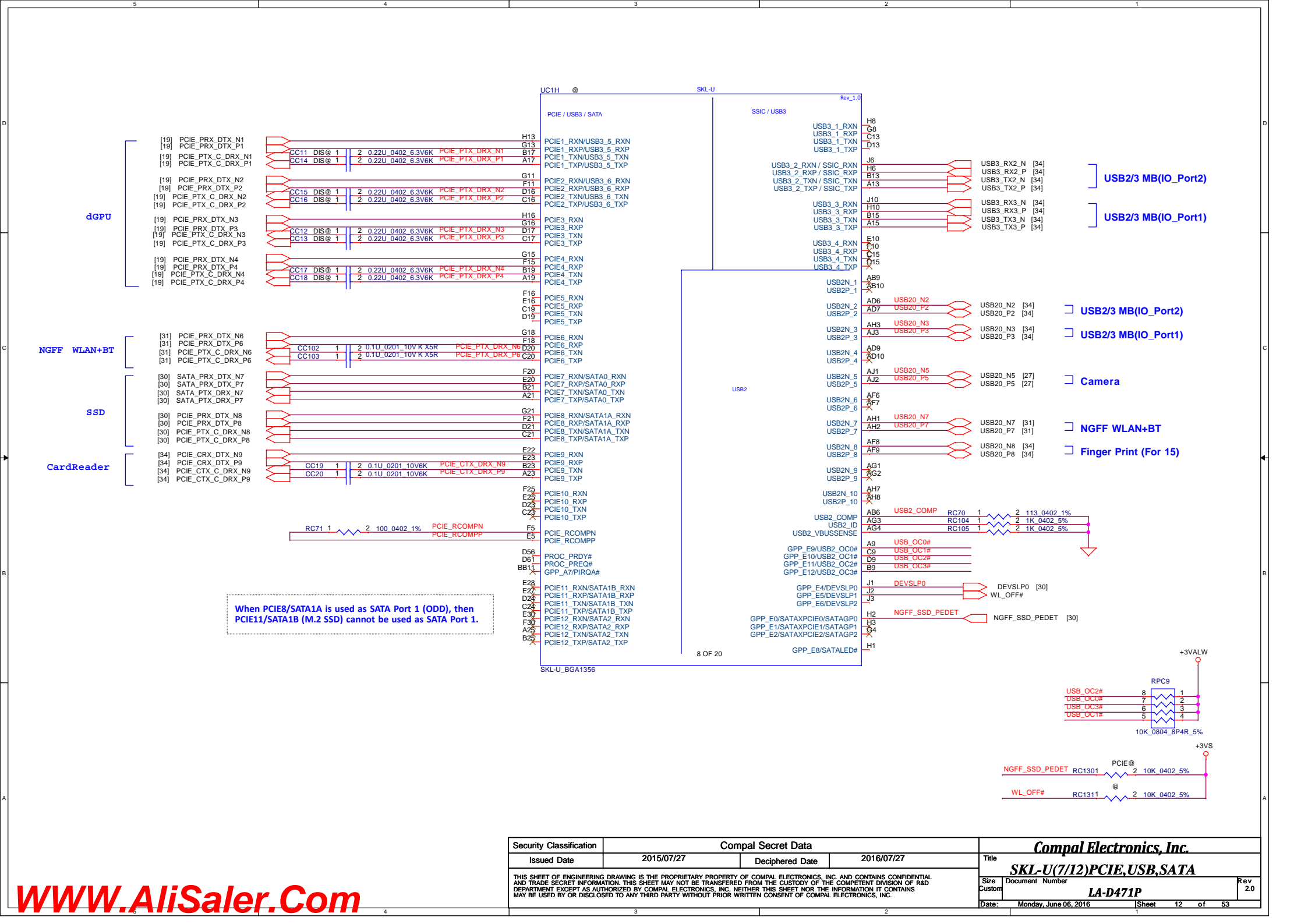
GPIO1_MOSI (Internal Pull Down):

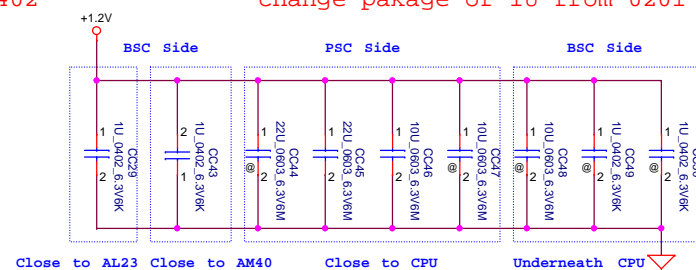
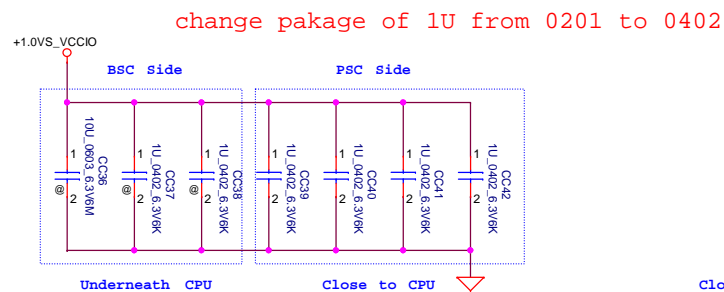
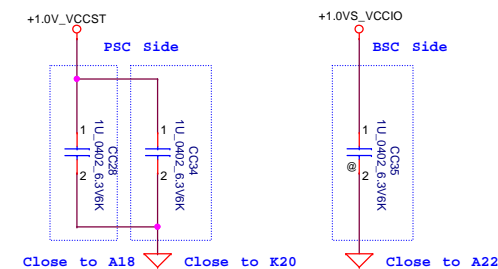
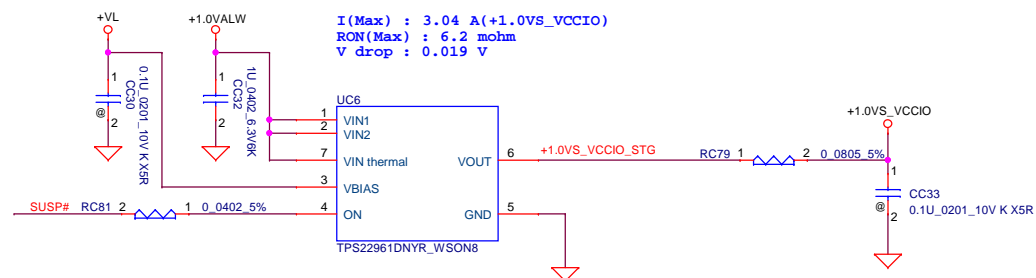
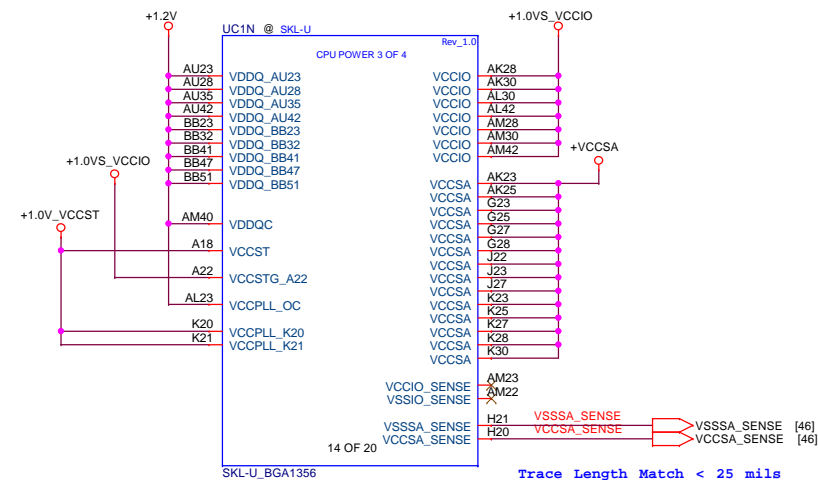
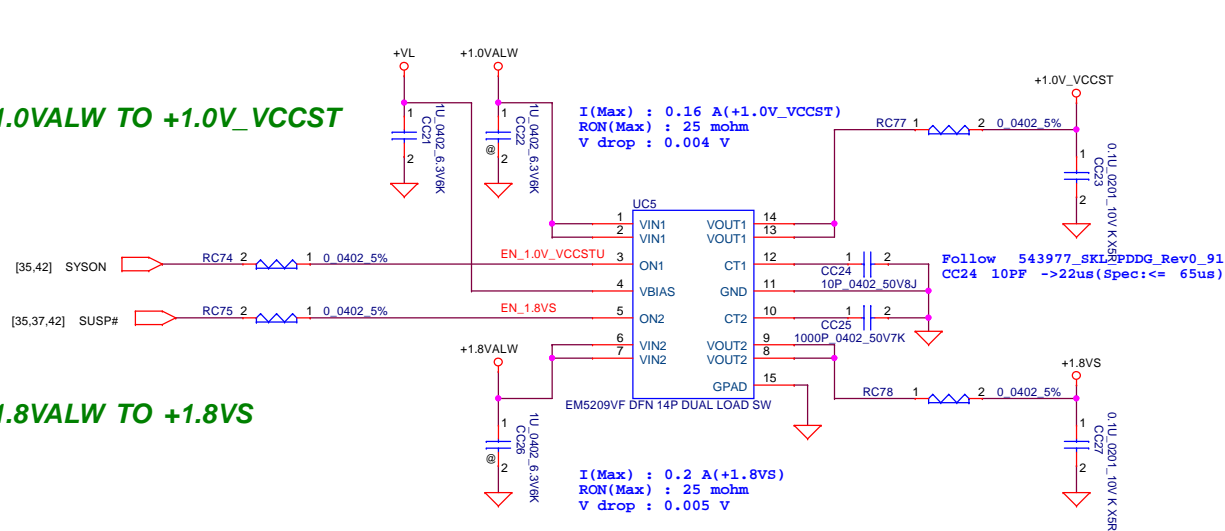
Boot BIOS Strap Bit

0 = SPI Mode ==> Default

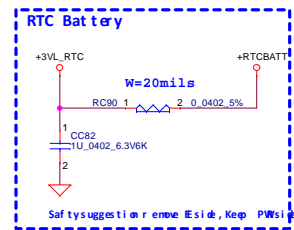
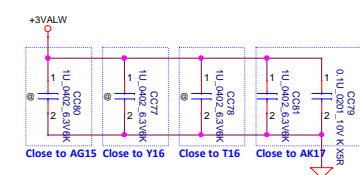
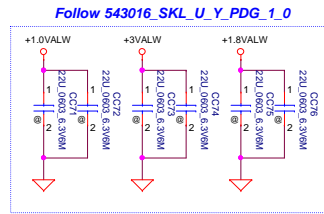
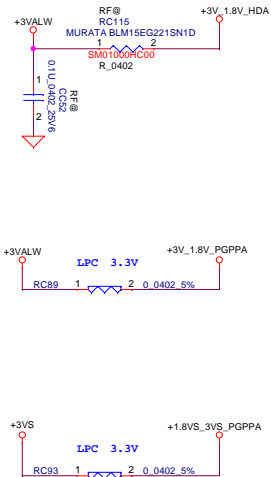
1 = LPC Mode

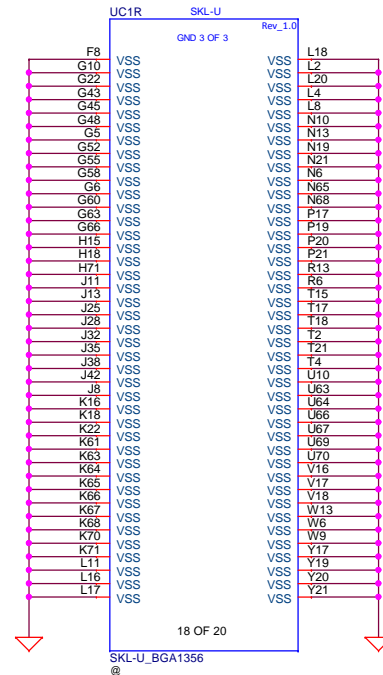
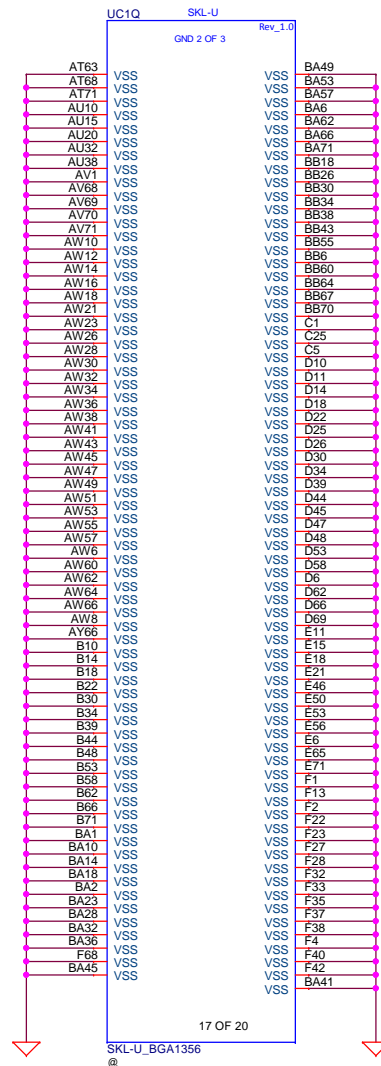
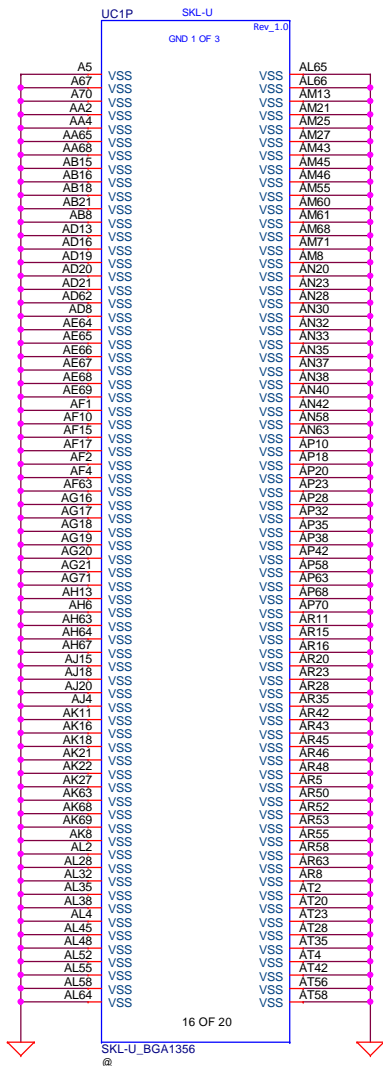




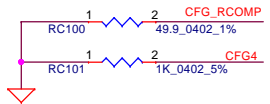
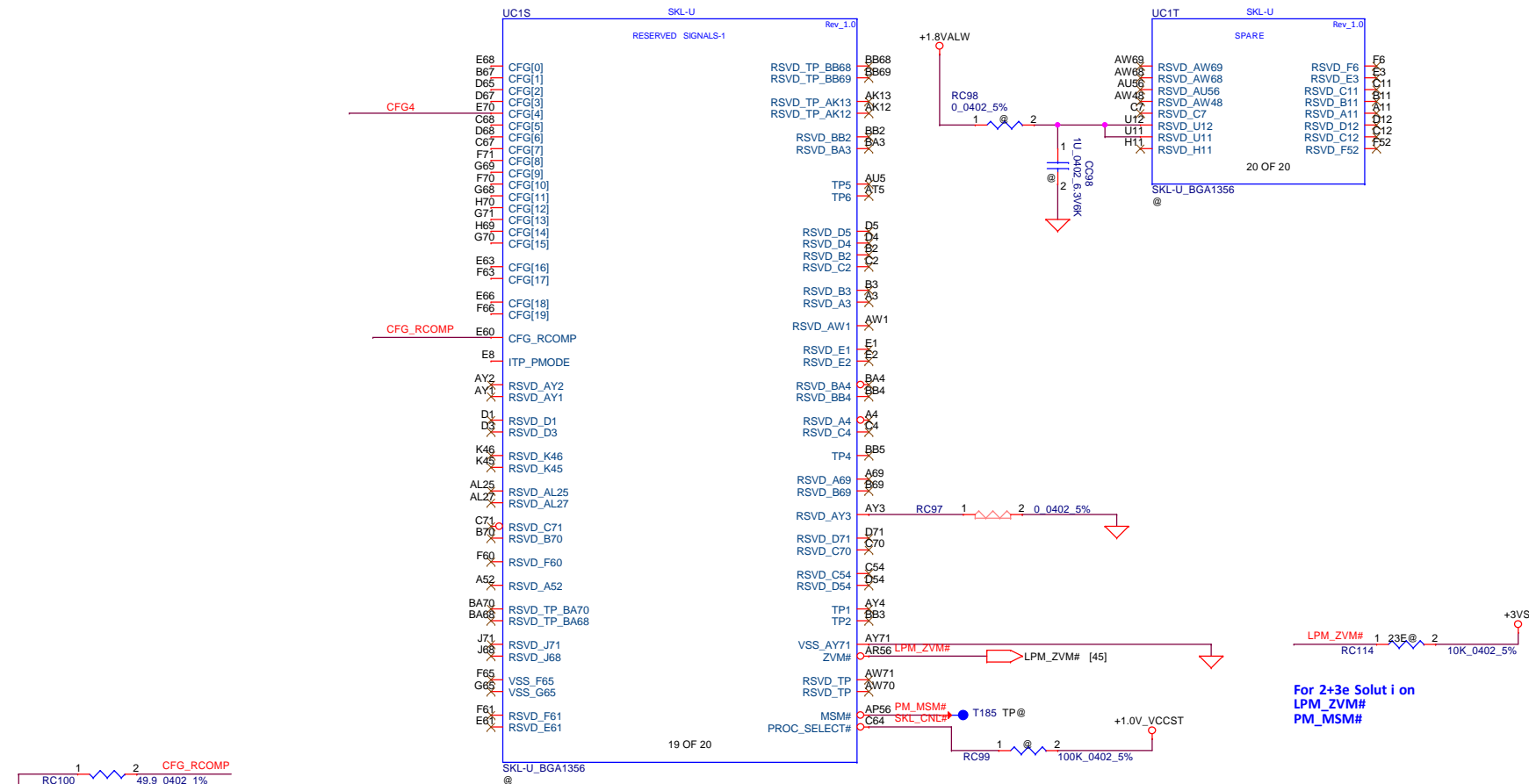


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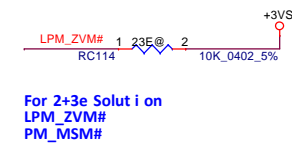


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Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port at tached to E mbedded D splay Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0
Stuf f 100K RC99 f r CannonLake U
Un-stuf f 100K RC99 f r Skylake U

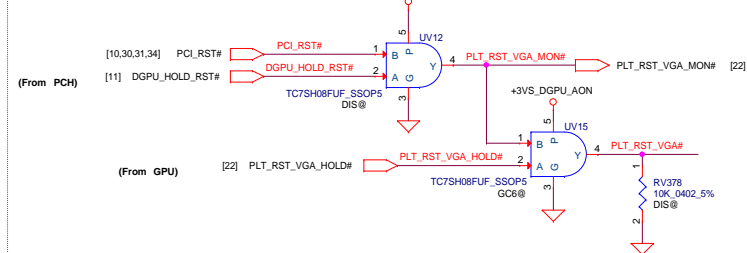


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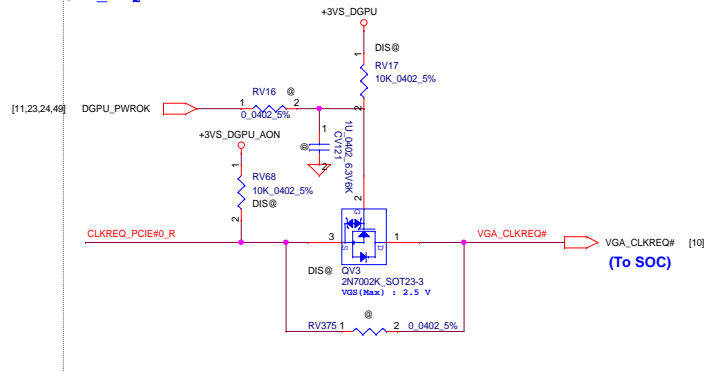


Table 3-16. PEX_I0VDD/Q Power Rail Combined				
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2-64	1.0 µF X5R	0402	1	Under GPU
GB2-64	4.7 µF X5R	0603	1	Heater GPU
GB2-64	10 µF X5R	0805	1	Midway between GPU and Power Supply
GB4B-128	1.0 µF X5R	0402	4	Under GPU
GB4B-128	4.7 µF X5R	0603	2	Heater GPU
GB4B-128	10 µF X5R	0805	4	Midway between GPU and Power Supply
GB4B-128	22 µF X5R	0805	4	Midway between GPU and Power Supply

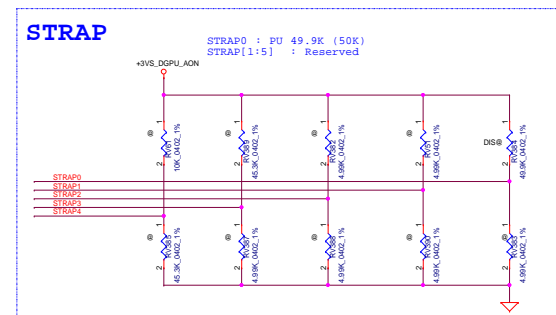
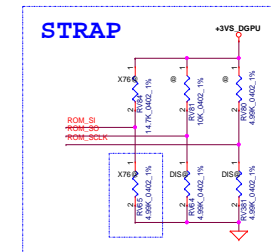
Reset Control



CLK_REQ



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2014/05/19			Deciphered Date		2015/12/31	
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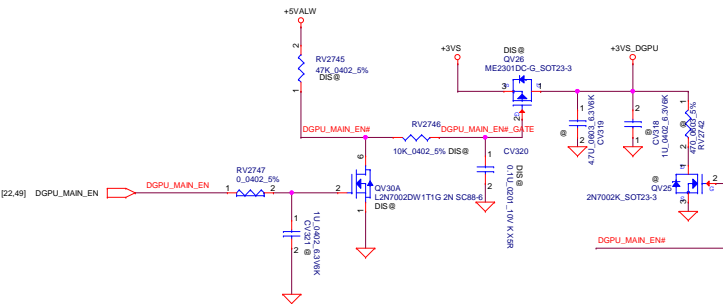
[illegible]

Memory Type	FBVDQ/ FBVDQD	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Data Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FR-11C	F-die	0x9	900	N/A	Production ready
				Micron	MT41J128M16JT-093G-K	K-die	0xA	900	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0x8	900	N/A	Production ready
				Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production ready
				Micron	MT41J256M16HA-093G-E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Samsung	K4W4G1646E-BC1A	E-die	0x1	900	N/A	Post production ready
				Hynix	H5TC4G63CFR-H0C	C-die	0x2	900	N/A	Post production ready
				Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production ready
				Micron	MT41J256M16HA-093G-E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0xF	900	N/A	Post production ready
				Hynix	H5TC4G63CFR-H0C	C-die	0xE	900	N/A	Post production ready

From EC		BAX40
RAM_CFG[3:0] (ROM_ST)		
0x9 (PU 10K)		
0xA (PU 15K)		
0xB (PU 20K)		
0x3 (PD 20K)		
0x4 (PD 24.9K)		
0x5 (PD 30.1K)		
0x1 (PD 10K)		S2G
0x2 (PD 15K)		H2G
0x3 (PD 20K)		
0x4 (PD 24.9K)		
0x5 (PD 30.1K)		
0xF (PU 45.3K)		
0xE (PU 34.8K)		

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			Sheet 22 of 53	

+3VS to +3VS_DGPU



+3VS to +3VS_DGPU_AON

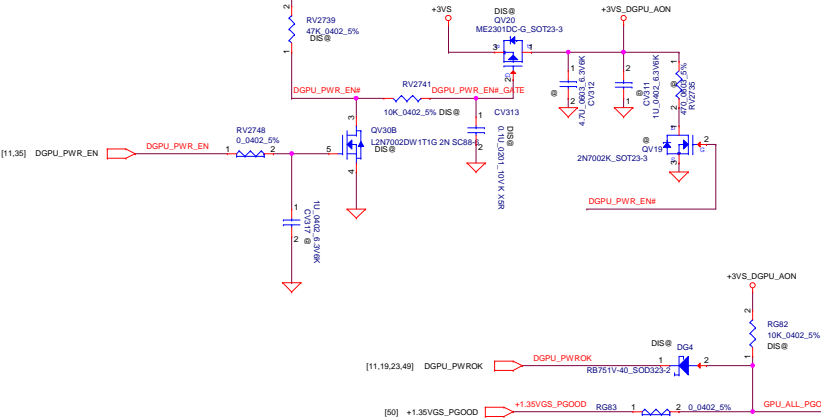


Table 3-7. Power Rail Specification for DDR3 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDDQ/FBVDD	1.5 V (DDR3) or 1.35V (DDR3L)
DC tolerance	± 3%
AC tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW

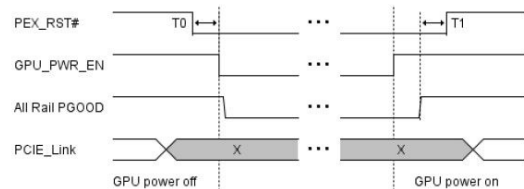
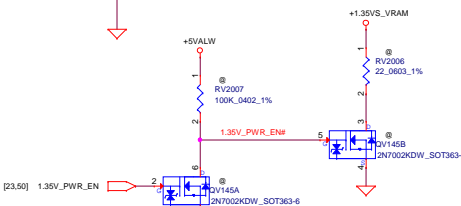
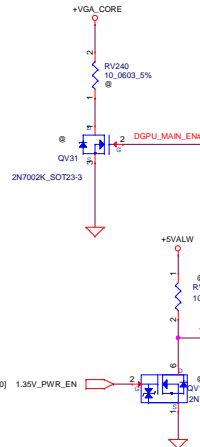


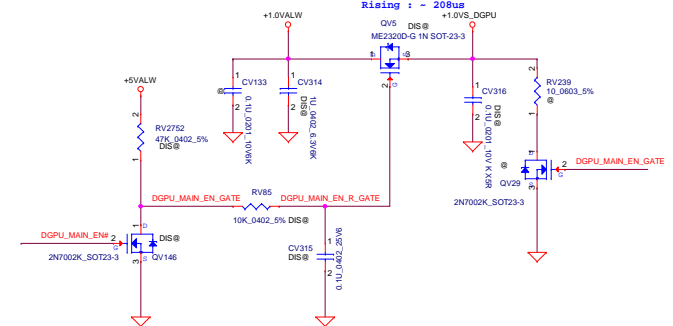
Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms



+1.0V_PRIM to +1.0VS_DGPU

Table 5. EDP-Continuous³

Products	VRM Type	GPU Core	GPU FBIO	FB Total ^{1,5}		1.05V Total ²	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GT	DDR3/L	26	1.37	1.33	2.32	2.12	0.79
N16S-GM	DDR3/L	20	1.37	1.31	2.32	2.05	0.79
N16S-LP	DDR3L	16	N/A	1.29	N/A	2.05	0.79

Table 3-15. PCI Express Power Rails Specification

GPU Package	Power Rails	Voltage	Transient Noise
GB2-64/ GB2B-64	PEX_IOVDD/Q and PEX_PLLVDD	1.05 V ± 30 mV or 1.0 V ± 15mV	100 mV pk-pk within 20 MHz (1.05V) or 70 mV pk-pk within 20 MHz (1.0V)

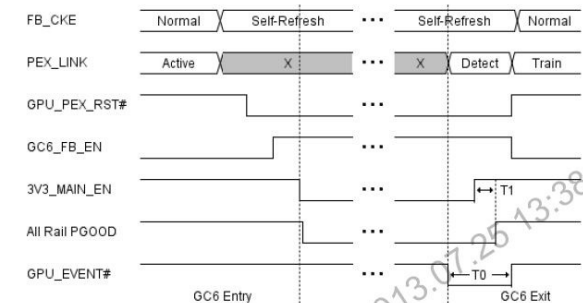


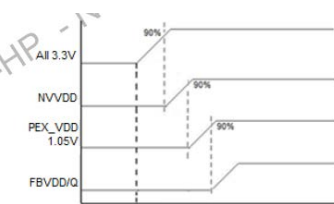
Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:

- The ramp time for any rail must be more than 40 μs and is recommended to be less than 2ms.



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

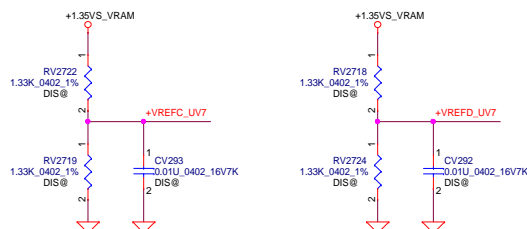
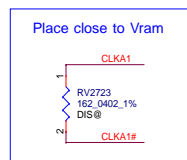
Figure 3-7. Example of Power-Up Sequencing Order

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Compal Electronics, Inc.

DGPU DC/DC Interface

Rev 2.0

[illegible]

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Memory Partition A - Lower 32 bits [31..0]

Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

Table 6-3. Mode D Command Mapping

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FbX_CMD0	CS0*	
FbX_CMD1		
FbX_CMD2	ODT	
FbX_CMD3	CKE	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE*	WE*
FbX_CMD14	A15	A15
FbX_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FbX_CMD16	CS0*	
FbX_CMD17		
FbX_CMD18	ODT	
FbX_CMD19	CKE	
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS*	RAS*
FbX_CMD31		
FbX_CMD32		
FbX_CMD33		
FbX_CMD34	DBG0*	
FbX_CMD35	DBG1*	

- Notes:
- Not available in GB2B-64 package.
 - GPU debug pins; not connected to DRAM. See section 6.1.11

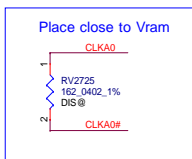
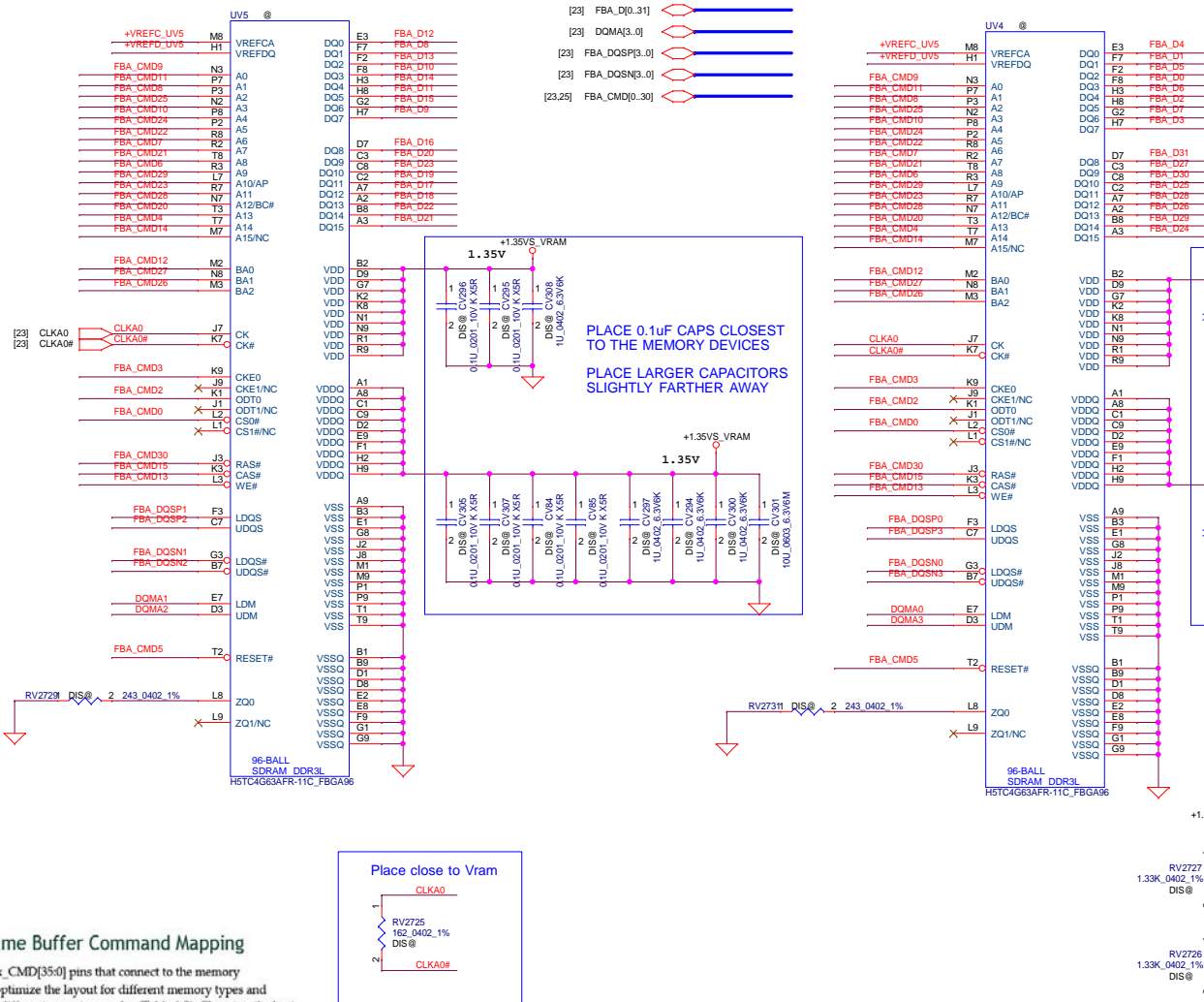
6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

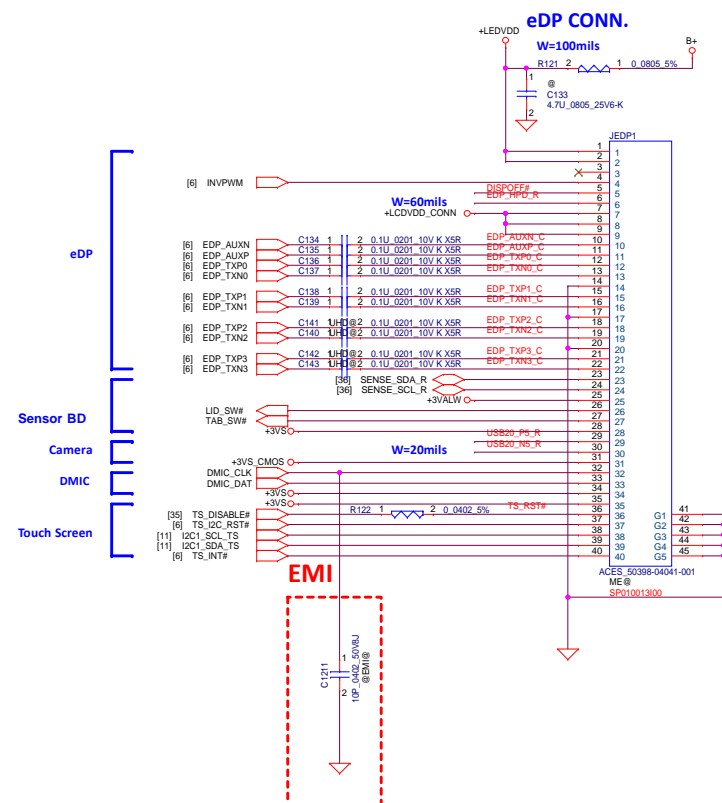
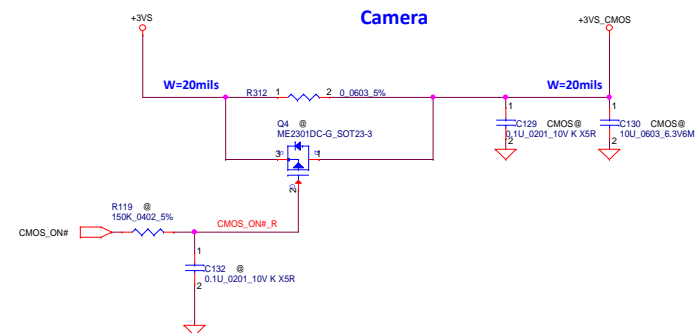
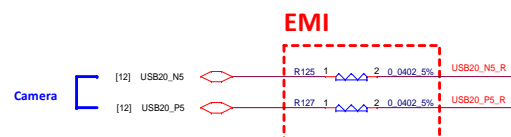
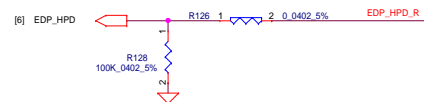
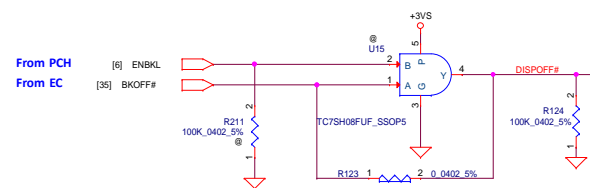
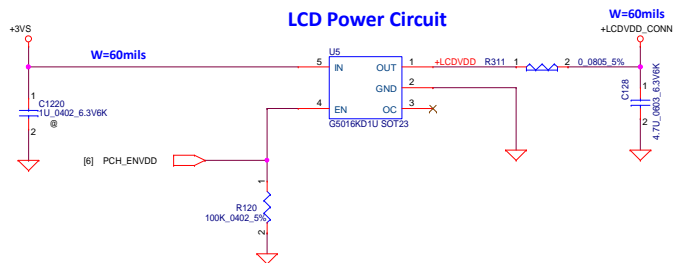
Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for H15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers*. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

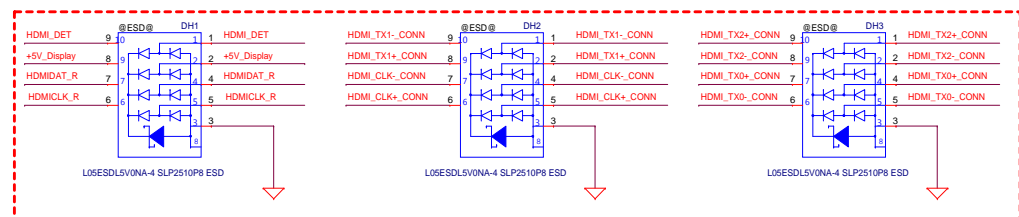
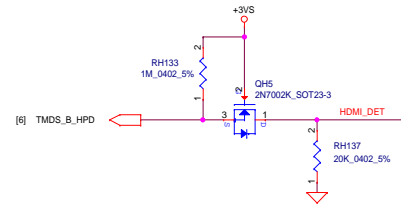
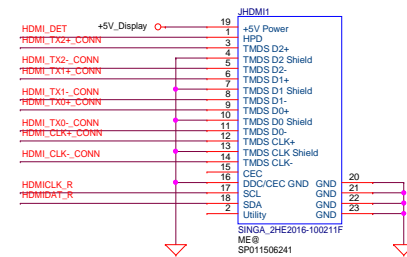
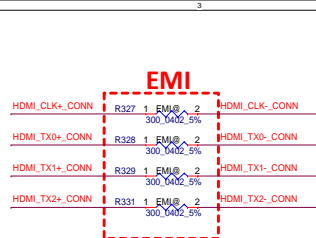
Note: *Not including two additional layers for power planes.



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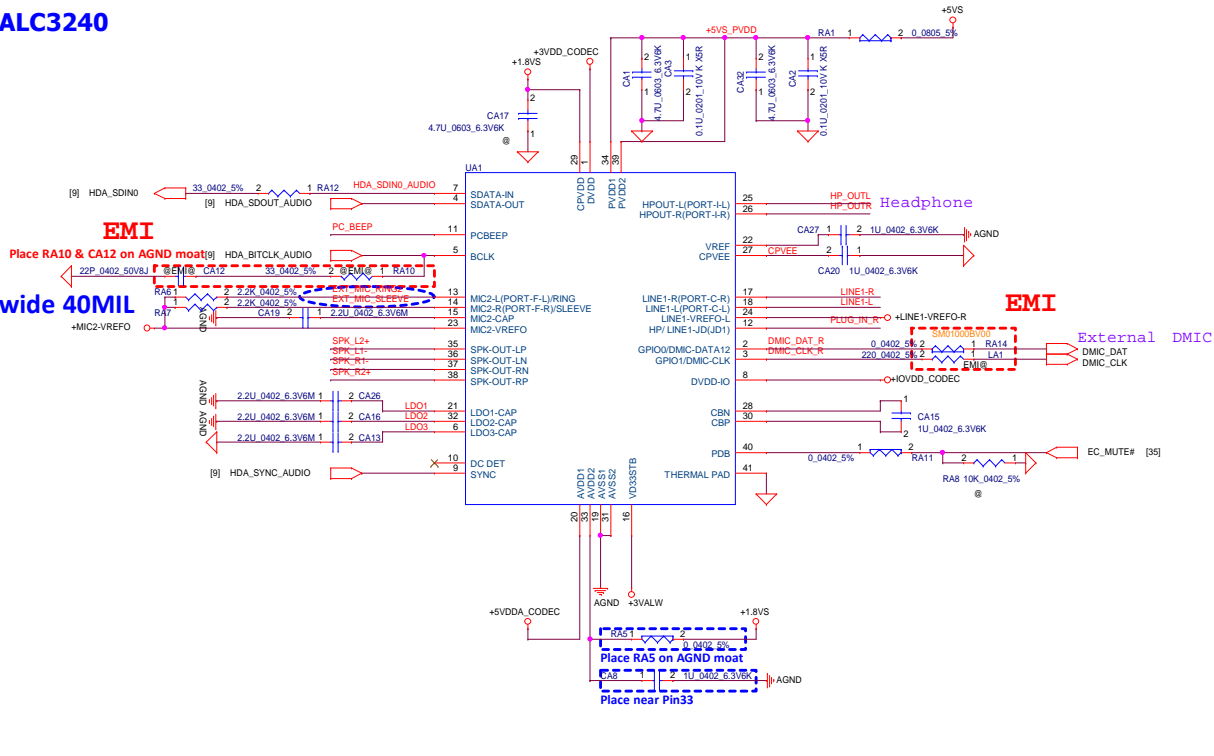


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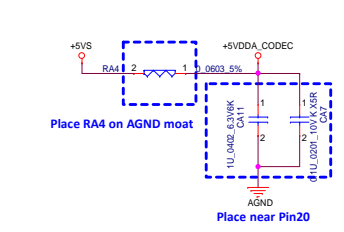


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ALC3240



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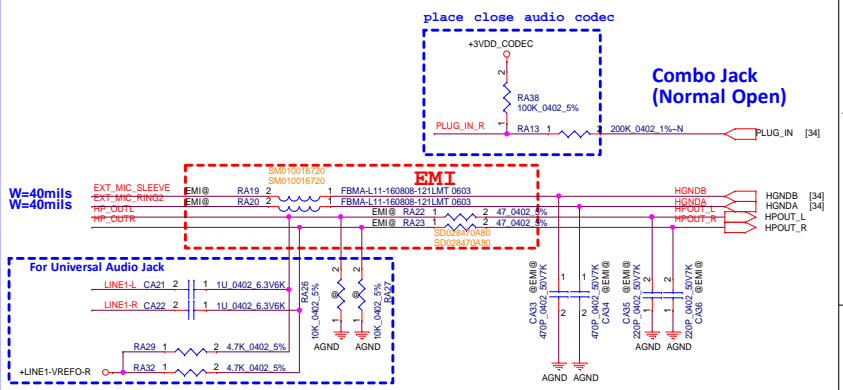
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	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

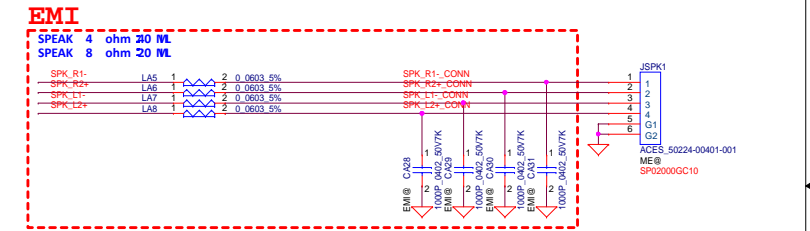
Each Platf or m HDA link Voltage Support (Pin 8):

	3.3V	1.5V
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Intel Skylake	V (default)	V

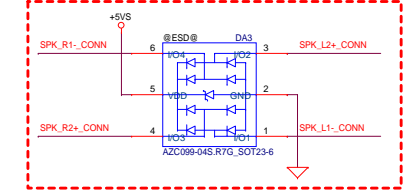
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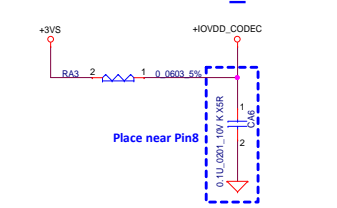
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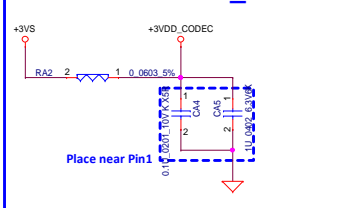
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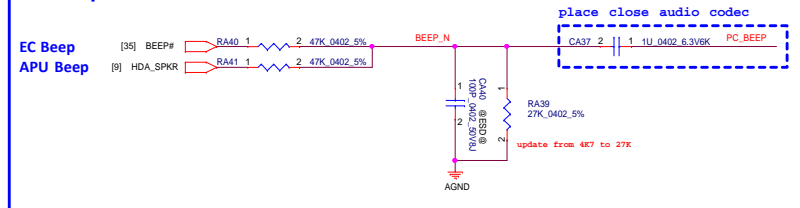
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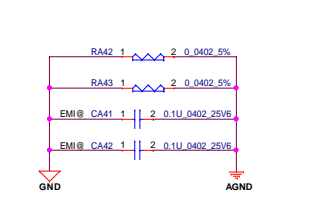
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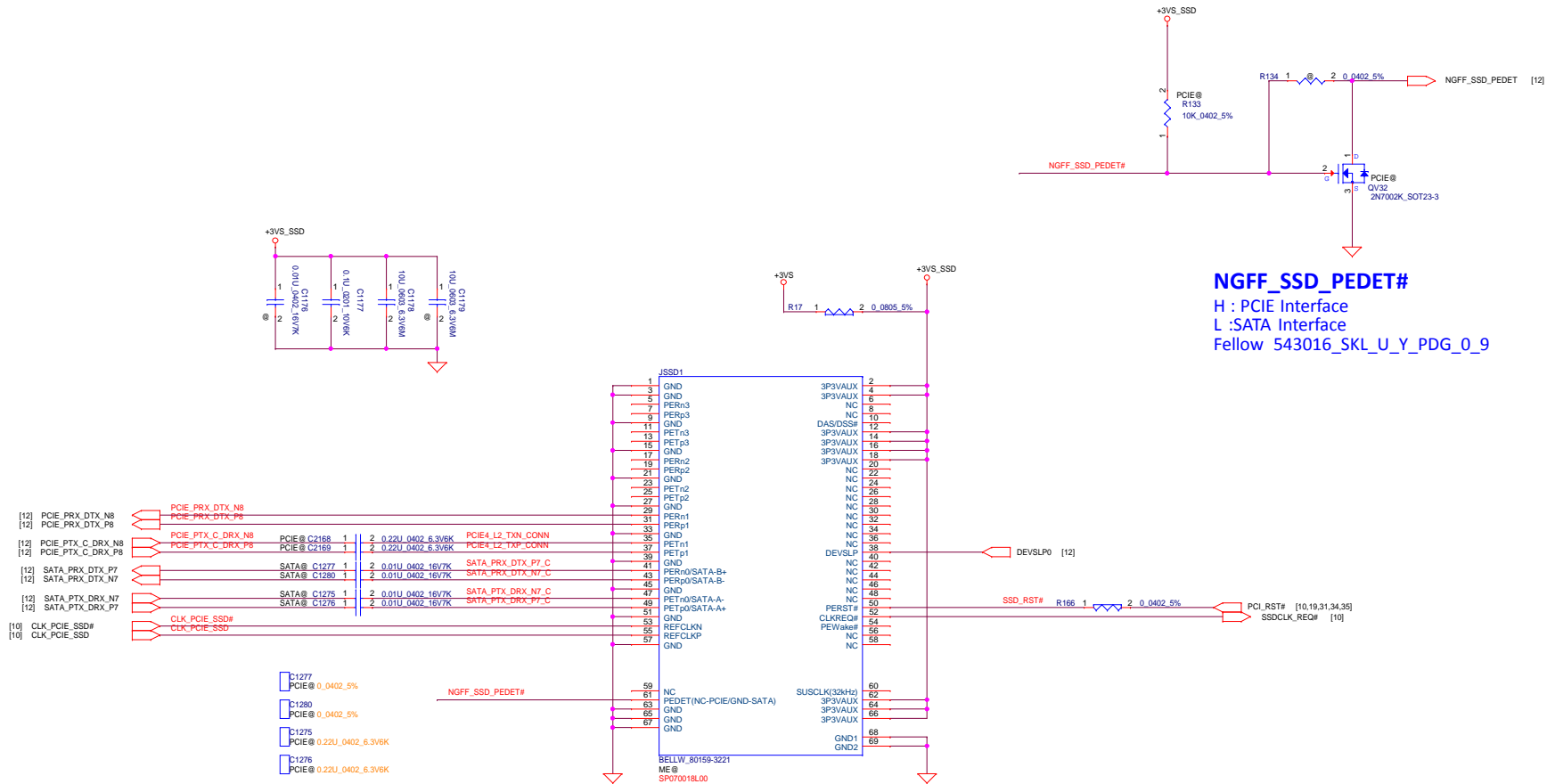


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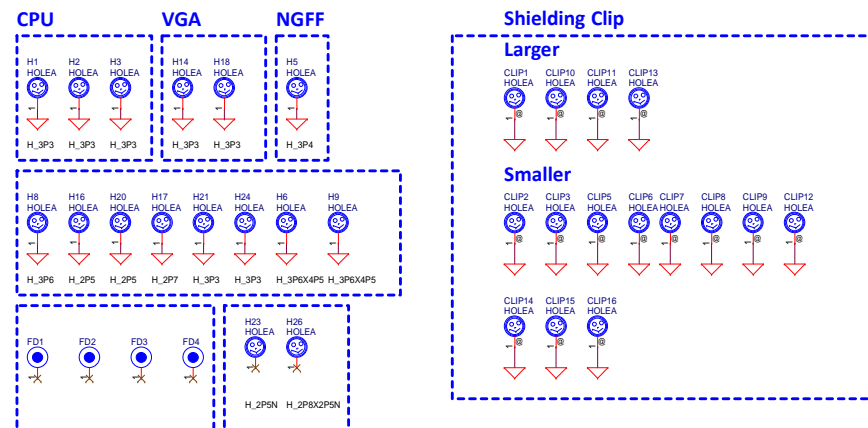
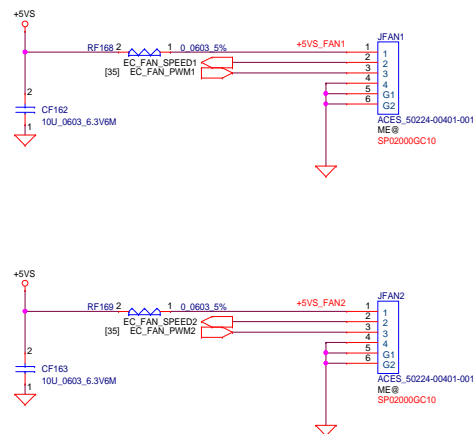
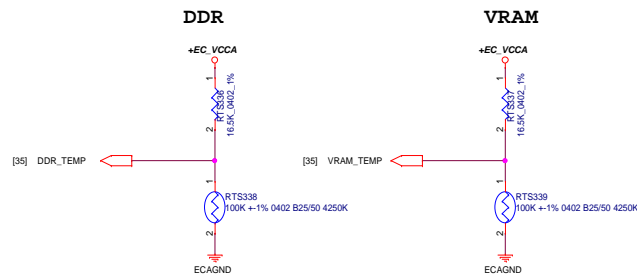
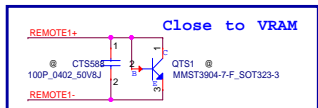
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L :SATA Interface

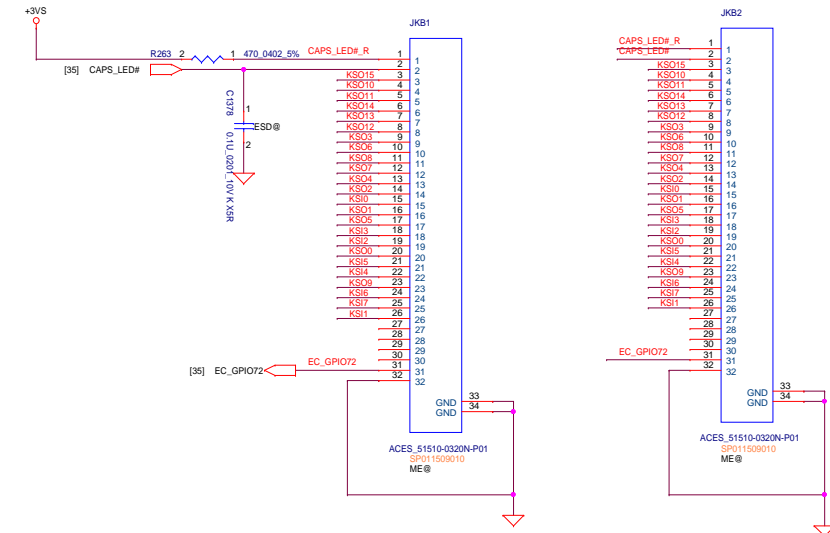
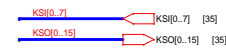
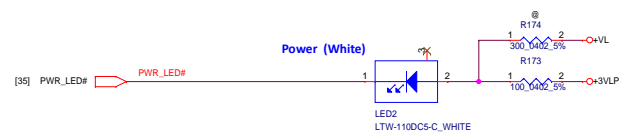
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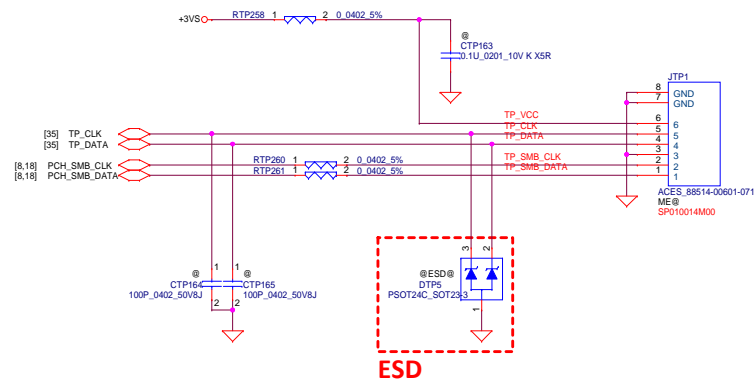
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Keyboard

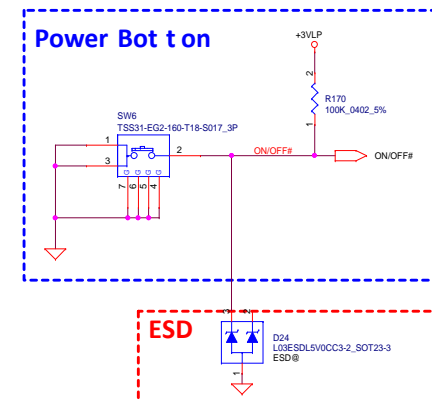
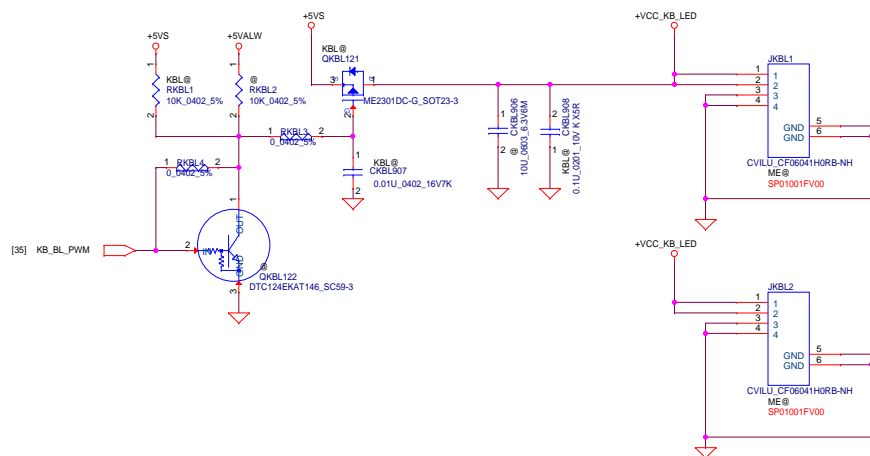


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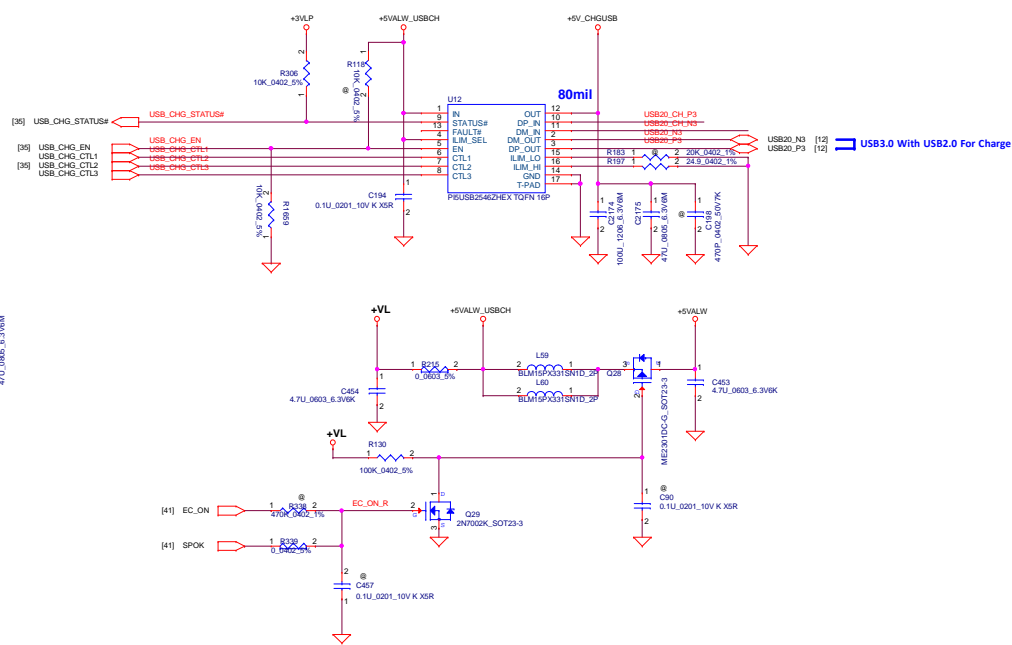
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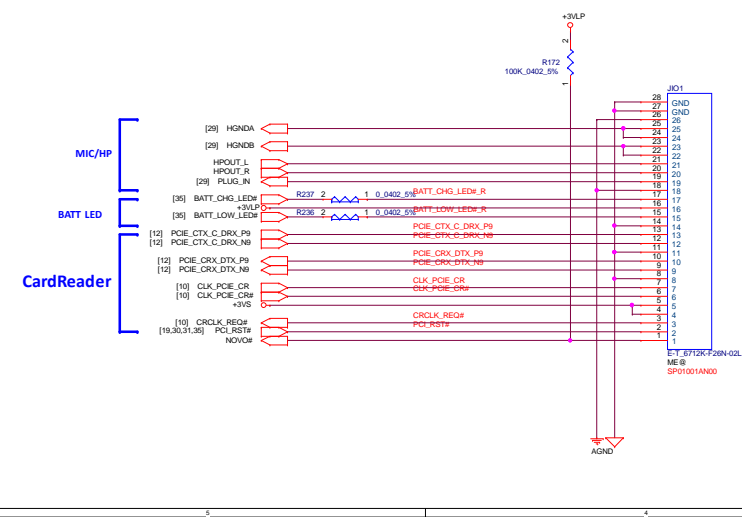


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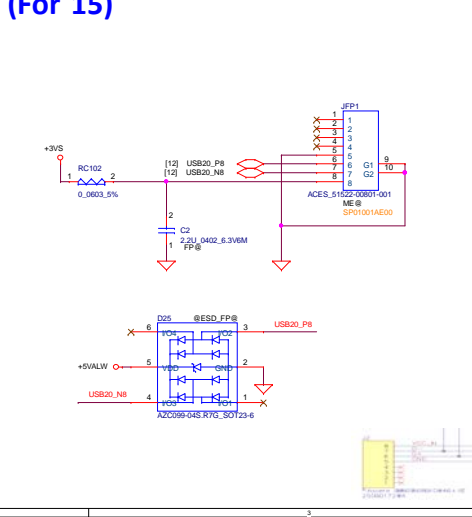
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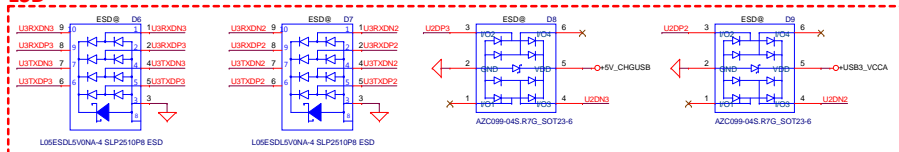
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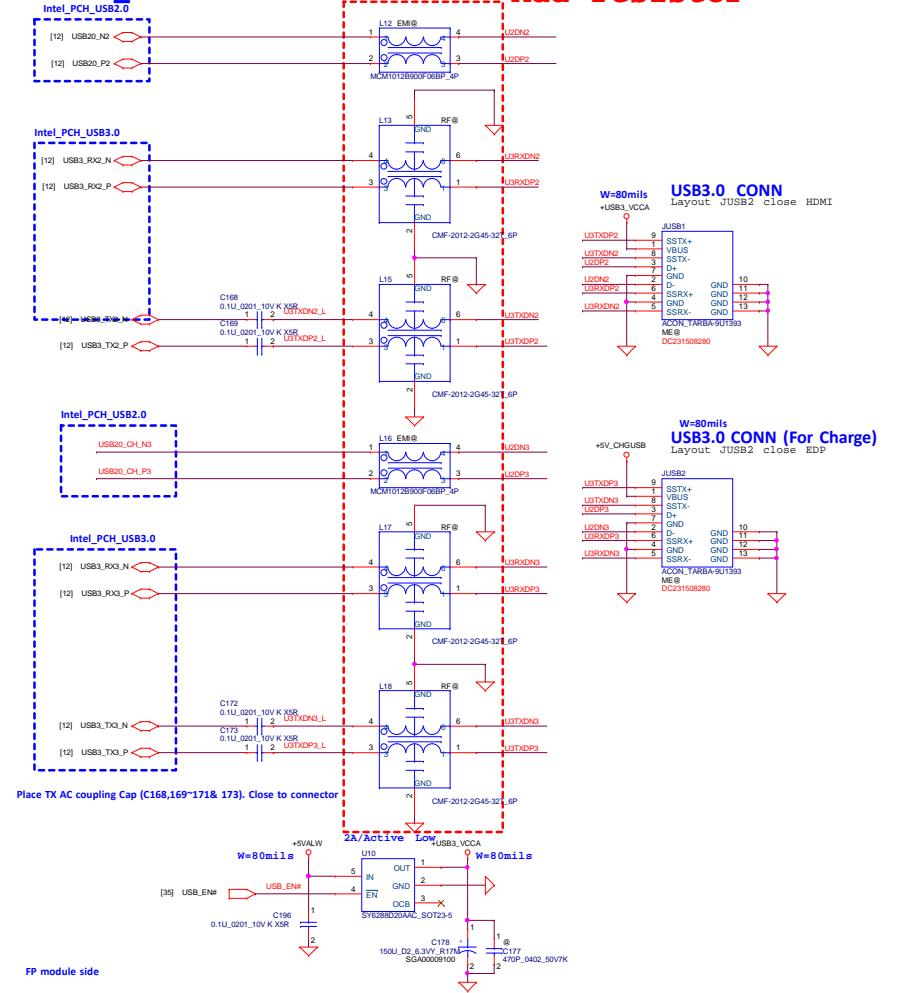
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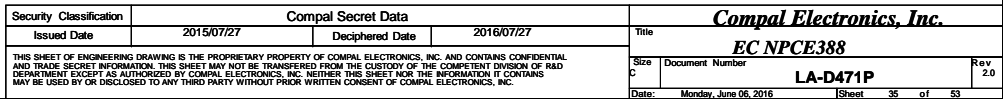
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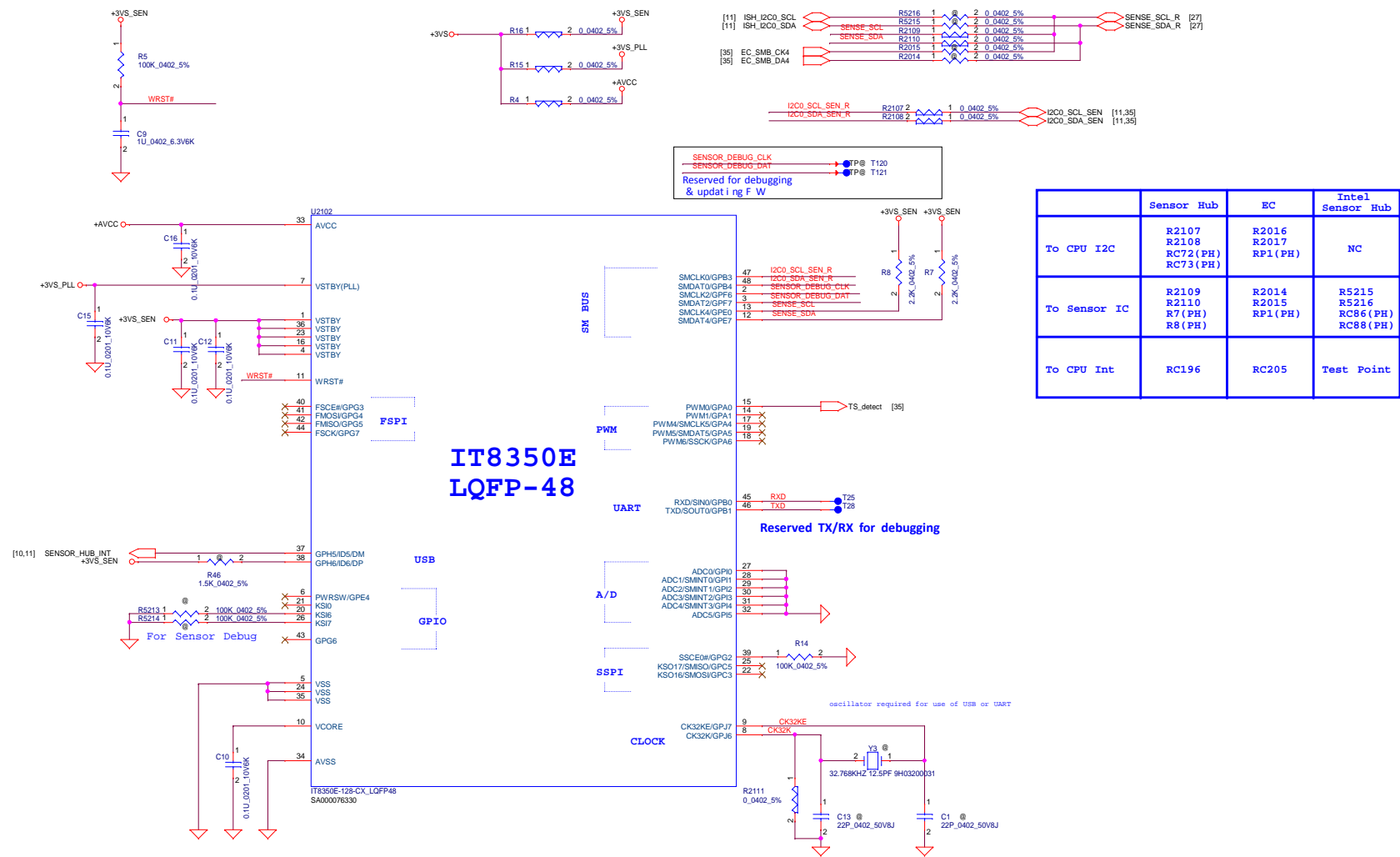
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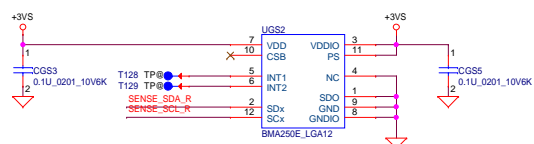
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				Quantity	Date: Monday, June 06, 2017 Sheet 34 of 83	



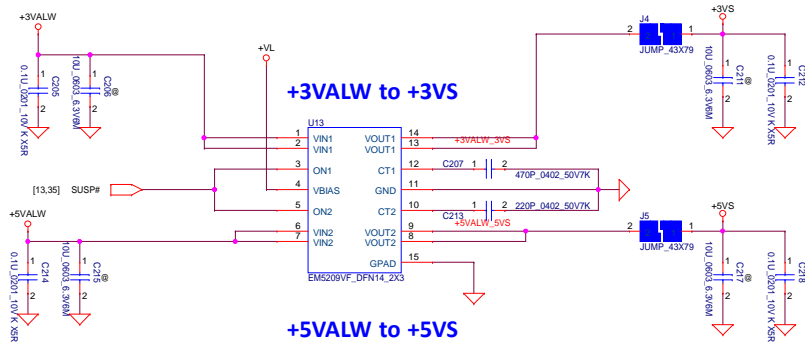
Sensor Hub



G-Sensor x1

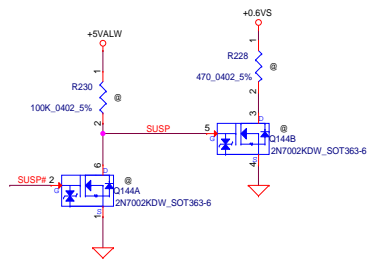
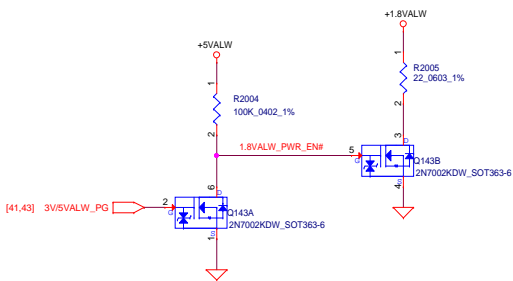


SMB Address: 0001 1000 (0X18)
when SDO is pulled to GND.

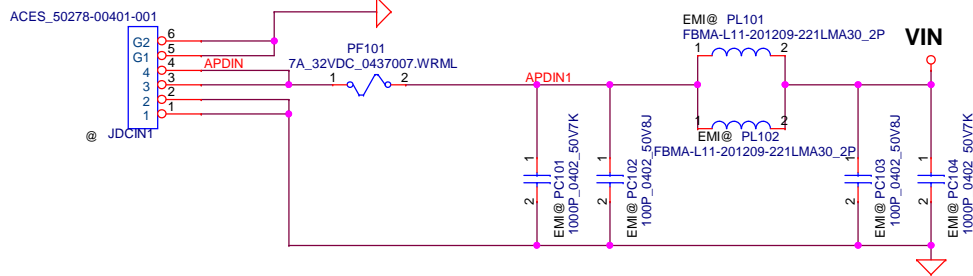


For +1.8VALW Discharge

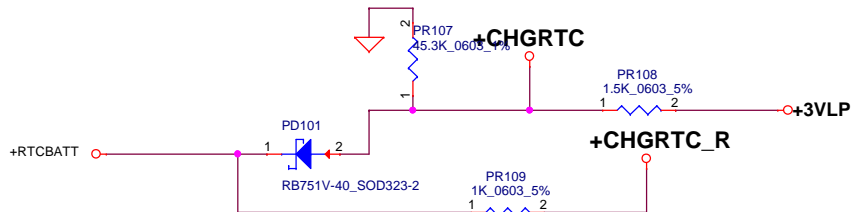
For +0.6VS Discharge



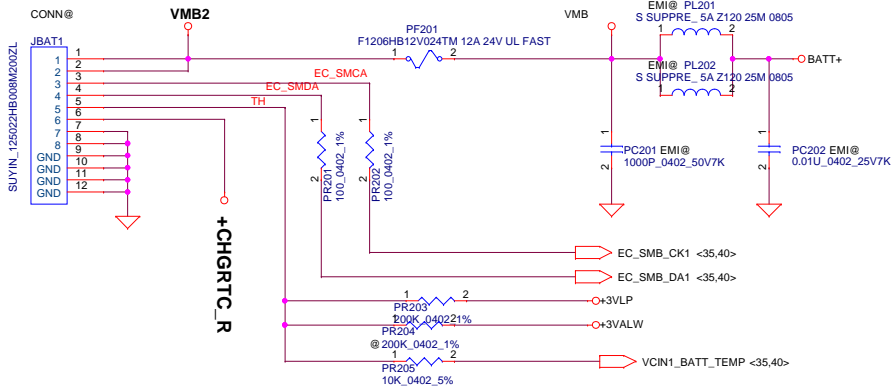
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				Date		Monday, June 06, 2016		Sheet



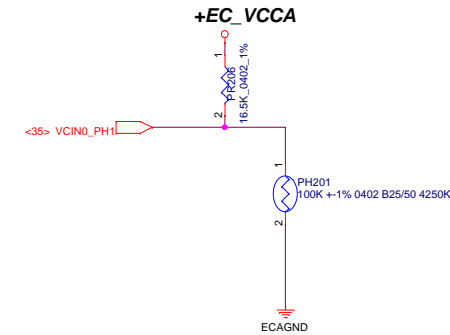
ADP_ID		
AC Adapter	65W	45W
R(ohm)	287	118
ADP_ID(V)	0.913	0.448
Detection voltage	0.693~1.134	0.234~0.663



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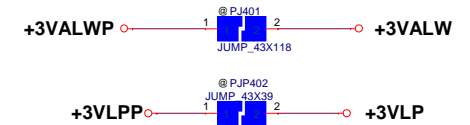
PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



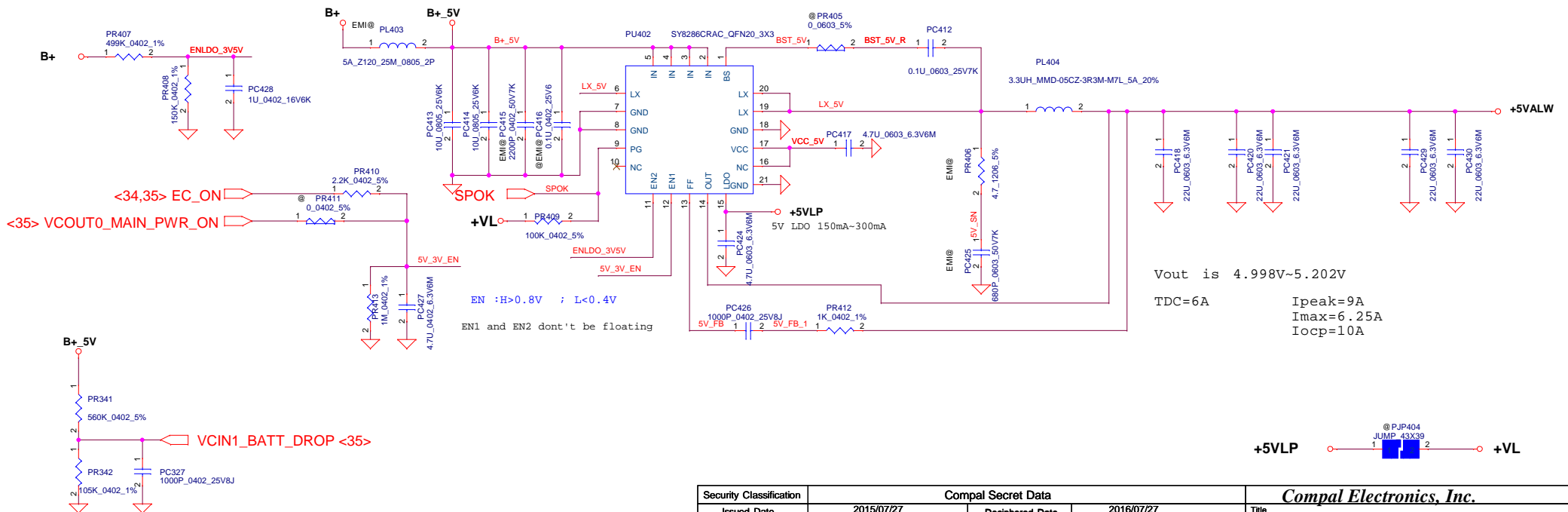
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Size				Document Number				Rev			
Custom				SKL				2.0			
Date:				Monday, June 06, 2016				Sheet 39 of 53			



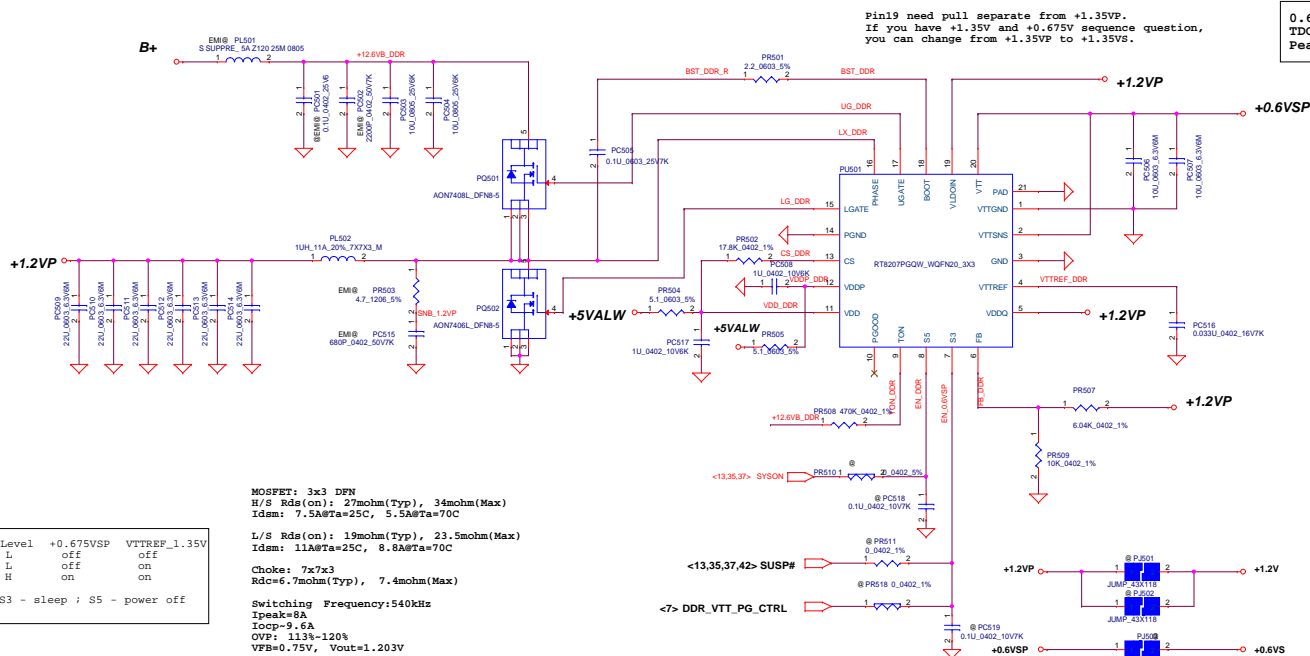
SY8286B_V1.mdd



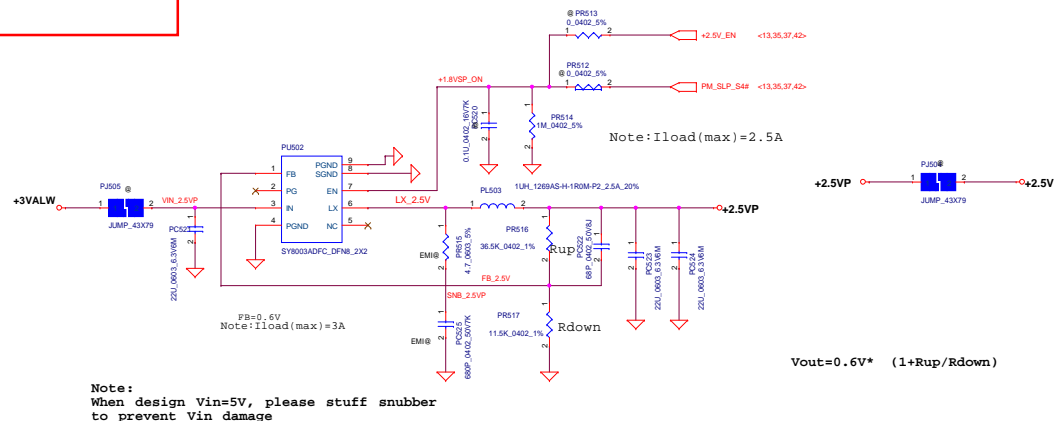
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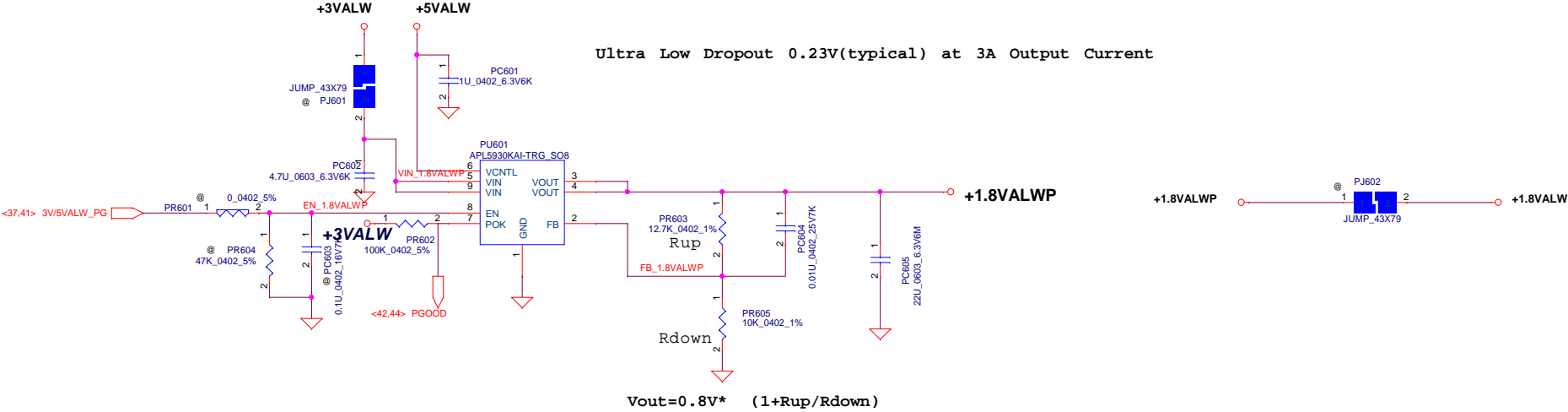


Module model information
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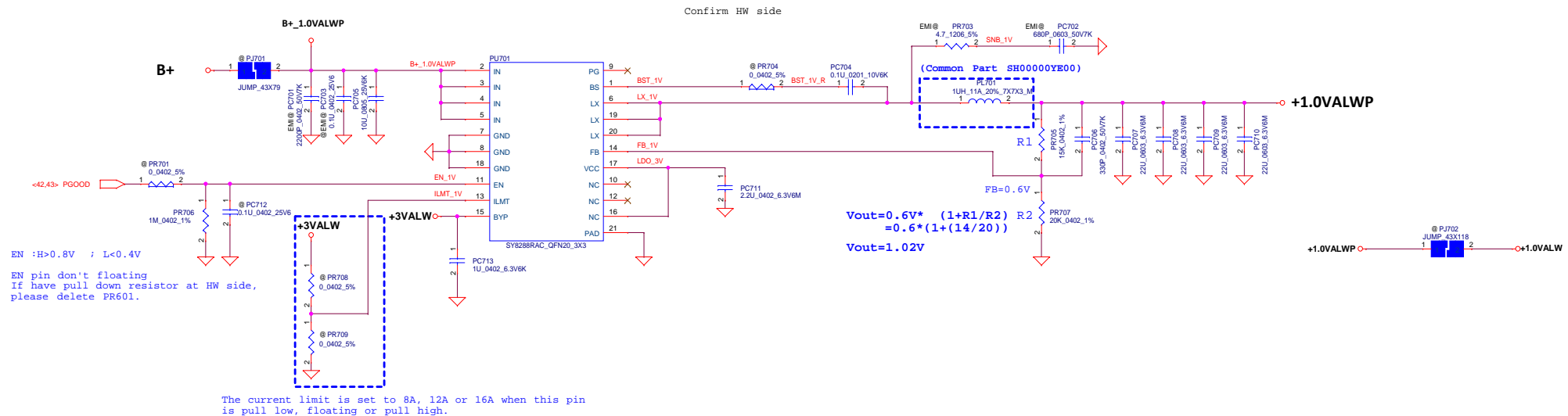
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Module model information
APL5930_V2.mdd



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Size	Document	Number	Rev	2.0	
Date:	Monday, June 06, 2016	Sheet	43	of	53

Module model information
SY8288_V1.mdd



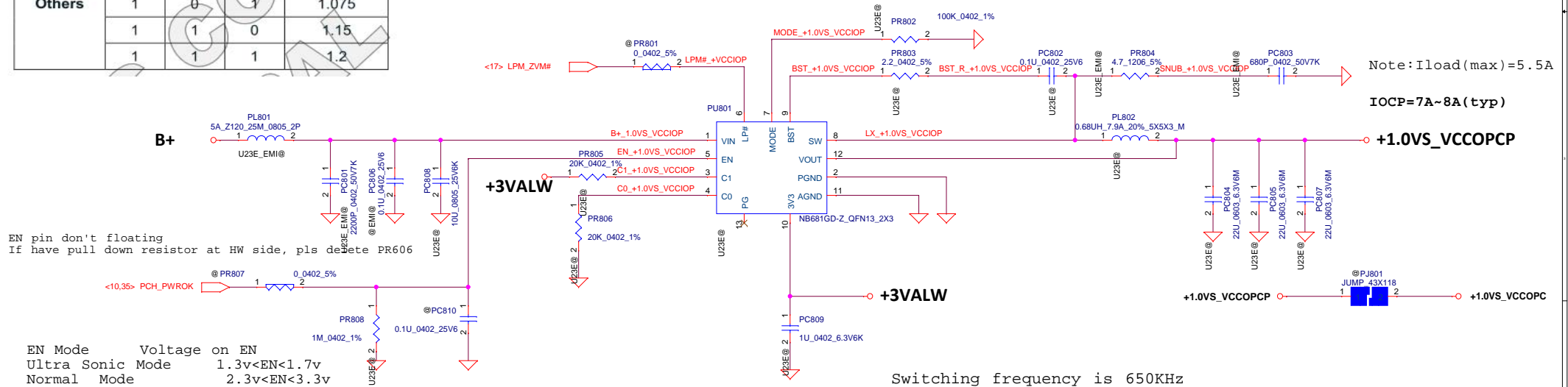
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Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

Module model information

NB681_V1.mdd



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				Size Custom	Document Number Rev. 2.0
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CPU POWER STAGES

VCC_CORE
 FSW=450kHz
 DCR = 1.19 mohm +/- 5%
 TYP
 H/S Rds(on) : 11.7mohm , 14mohm
 L/S Rds(on) : 2.7mohm , 3.3mohm

VCCGT(2 phase)
 FSW=450kHz
 DCR = 1.19 mohm +/- 5%
 TYP
 H/S Rds(on) : 11.7mohm , 14mohm
 L/S Rds(on) : 2.7mohm , 3.3mohm

VCCSA
 FSW=450kHz
 DCR 6.2mohm(TYP) , 6.51mohm(Max)
 TYP
 H/S Rds(on) : 12.4mohm , 15.8mohm
 L/S Rds(on) : 9.1mohm , 11.6mohm

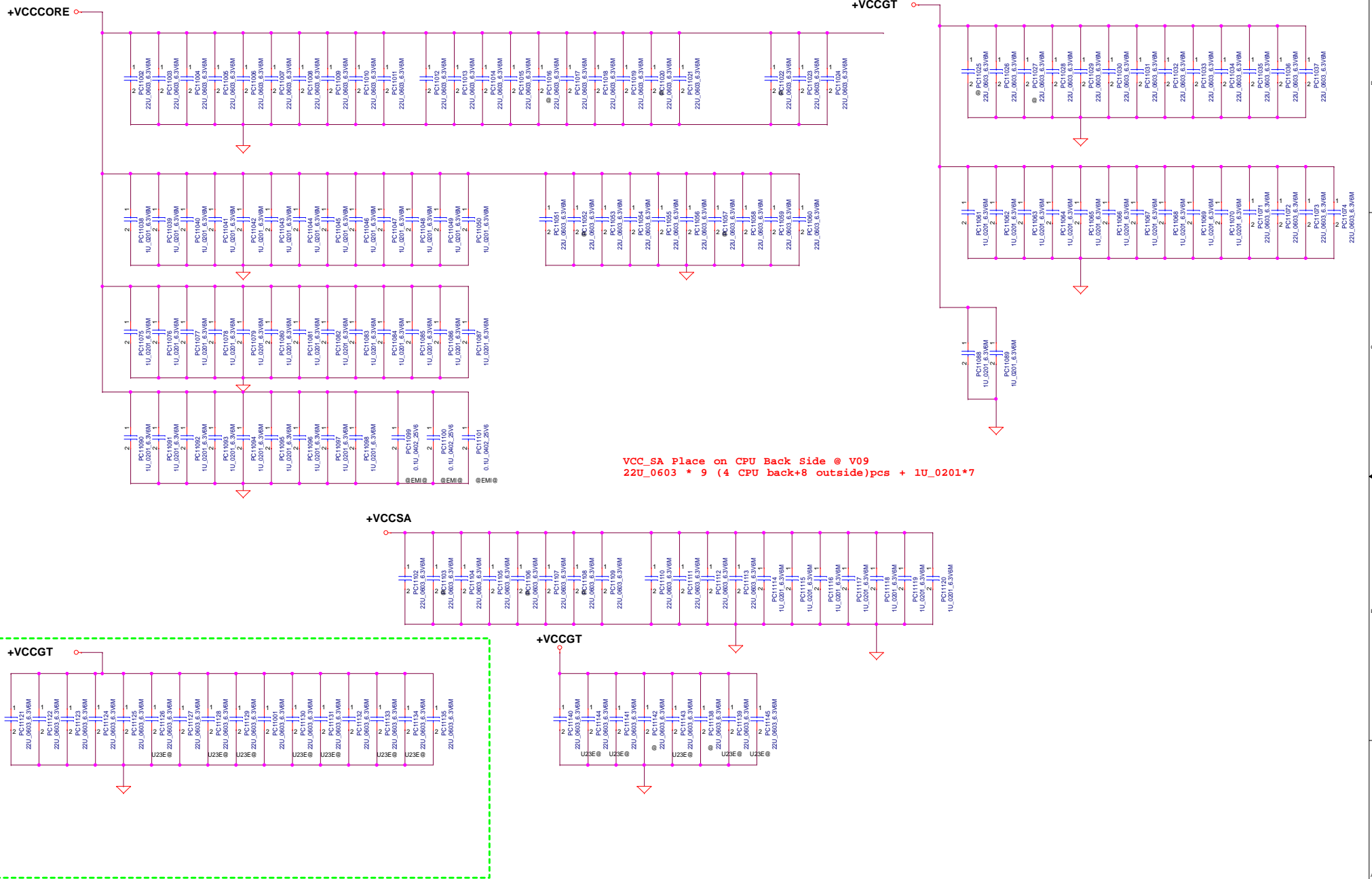
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VCCSA
FSW=450kHz
DCR 6.2mohm(TYP), 6.51mohm(Max)
H/S Rds(on) :12.4mohm , 15.8mohm
L/S Rds(on) :9.1mohm , 11.6mohm

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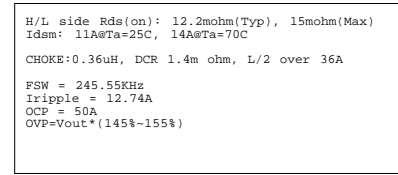
VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 28 pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 29 pcs +1U_0201*12 pcs



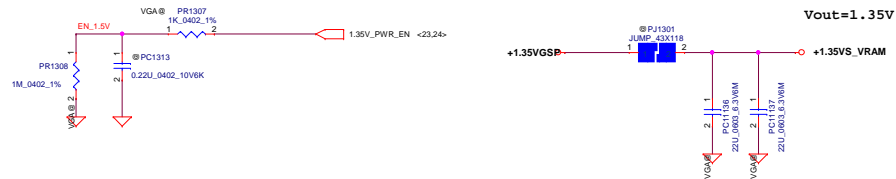
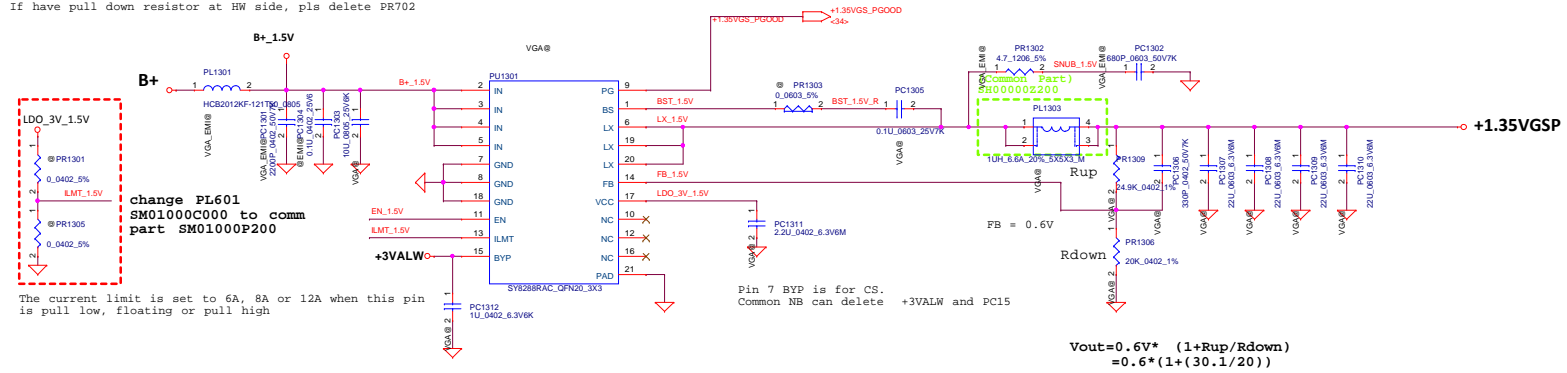
VCC_SA Place on CPU Back Side @ V09
22U_0603 * 9 (4 CPU back+8 outside)pcs + 1U_0201*7

EN High Threshold = 1.6V



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EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



Version change list (P.I.R. List)

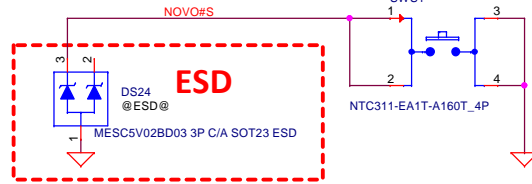
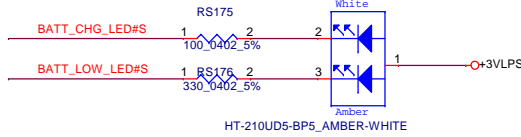
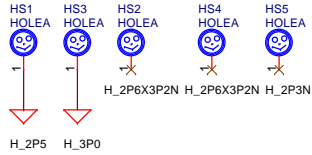
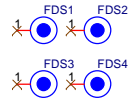
Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	request by HW	P49	change PR1206 to 0 ohm	2015/11/10	SIV
2	request by HW	P50	change PR1307 to 1K ohm	2015/11/10	SIV
3	avoid 1V0 voltage drop	P44	change PR705 to 15K ohm	2015/11/10	SIV
4	adjust charge current limit	P40	change PR334 to 178K ohm	2015/11/10	SIV
6	reduce 5v ripple voltage	P41	add PC423 on schematic	2015/11/10	SIV
7	adjust component bom structure of U23E	P47	PQ1004->U23E@,PC1020->U23E@,PC1021->POP	2015/11/10	SIV
8	adjust DDR over current protect value	P42	change PR502 to 17.8K ohm	2015/11/10	SIV
9	request by part count	P40,42-45	PR319,PR321,PR510,PR601,PR701,PR807 change to 0 ohm short pad	2015/11/10	SIV
10	optimize cpu transient	P47/48	change below value: PCI18->680P,PRI23->26.7K ohm,PRI14->64.9K ohm, PRI42 ->59K ohm,PCI21->2200P,PRI49->649 ohm	2015/11/10	SIV
11			change pop and up pop CPU OUTPUT CAP location: PC11138,PC11140,PC11142,PC11143->POP PC11126,PC11128,PC11129,PC11133->U23E@		
12	request by EMI	P40	PC317,PR318,PC304->POP change PR312 to 2.2 ohm	2015/11/10	SIV
13	request by RF	P40-50	PR318,PR403,PR406,PR503,PR515,PR703,PR804,PR1004,PR1007,PR1006, PR1009,PR1213,PR1224,PR1302 ->POP PC317,PC410,PC425,PC515,PC525,PC702,PC803,PC1009,PC1023PC1024, PC1029,PC1215,PC1218,PC1302->POP	2015/11/10	SIV
14	reduce power consumption	P40	Del PR335,Add:PR336,PQ307,PQ308	2015/11/13	SIV
15	charger ac in detect	P40	change PC306 to 0.1uA	2015/11/16	SIV
16	reduce Aucostic noise	P40,47,49	Change 10u_0805(SE00000QK00) to 10u_0603(SE00000X200)	2015/12/05	SIT
17	When battery connector first touch positive pin can't power on	P41	Reserve PC428 and change PR409 to 100K pull high +VL	2015/12/14	SIT
18	reduce Aucostic noise	P47	change PC1006 from 33u to 68u, del PC1016	2015/12/18	SIT
19	request by EMI	P38	change PL102 and PL102 PN to SM010014520	2015/12/23	SIT
20	reduce ripple current	P41	change PC419,PC422,PC423 from 22u 0603 to 47u 0805 change PL404 from 1.5uH to 3.3uH	2016/01/19	SVT
21	solve ISL95521 didn't protect function (dc prochot)	P41	change PU301 from ISL95521 to ISL95520 change PR306 from 392K to 287K	2016/01/19	SVT
22	resive PC1016 for acustic noise	P47	resive PC1016 for acustic noise	2016/04/21	CIUY7-SIT
23	Modify PRI53,PRI64,PRI42 for cpu transient test	P46	PRI53 form 33.2k to 30.3k PRI42 form 59k to 56.2k PRI64 form 90.9k to 100k	2016/04/21	CIUY7-SIT
24	change for cost priority change AOS to main source on PQ1001 and PQ1002	P46	PQ1001 from SB00000S800 to SB00000JZ00 PQ1002 from SB00000SD00 to SB000017Q00	2016/06/03	CIUY7-SVT

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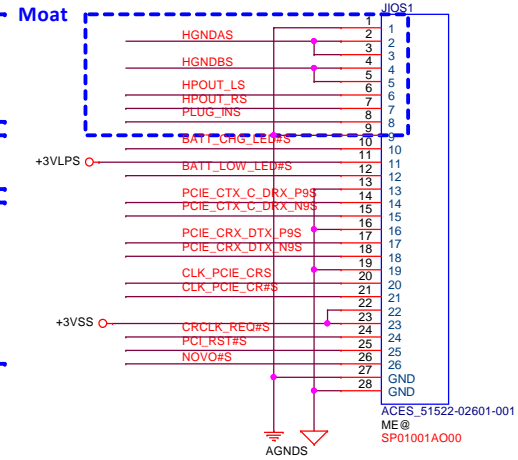
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for HW

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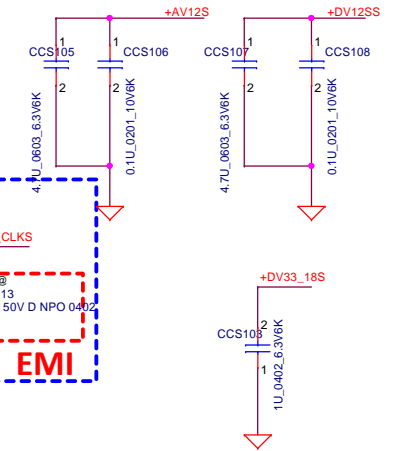
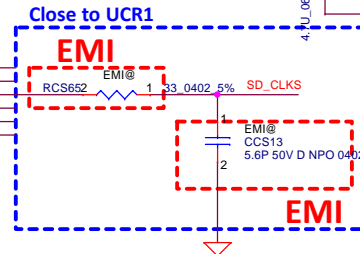
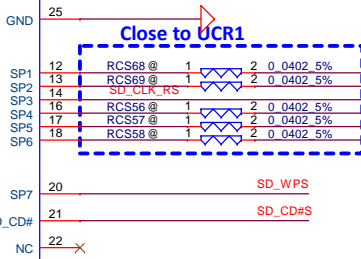
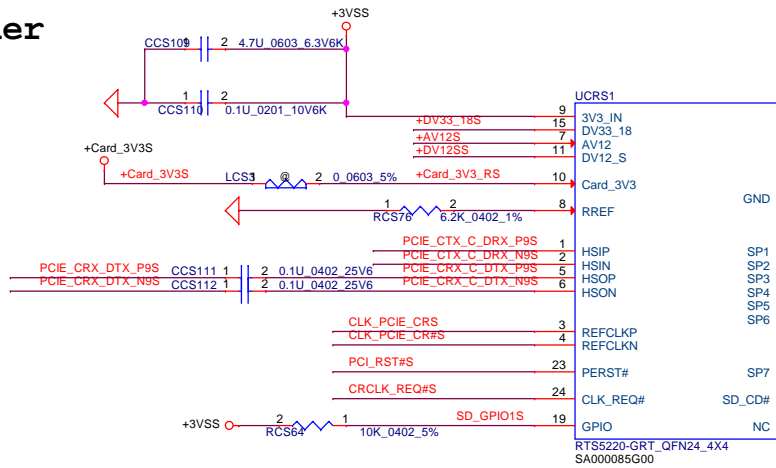


Conn.

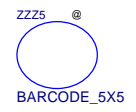
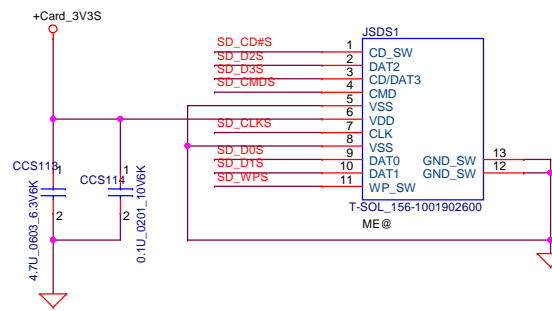
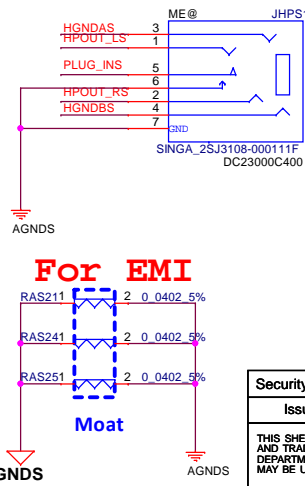
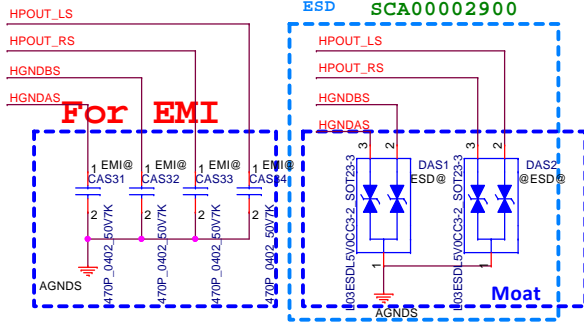
MIC/HP
BATT LED
CardReader



Card Reader



Audio Combo Jack



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