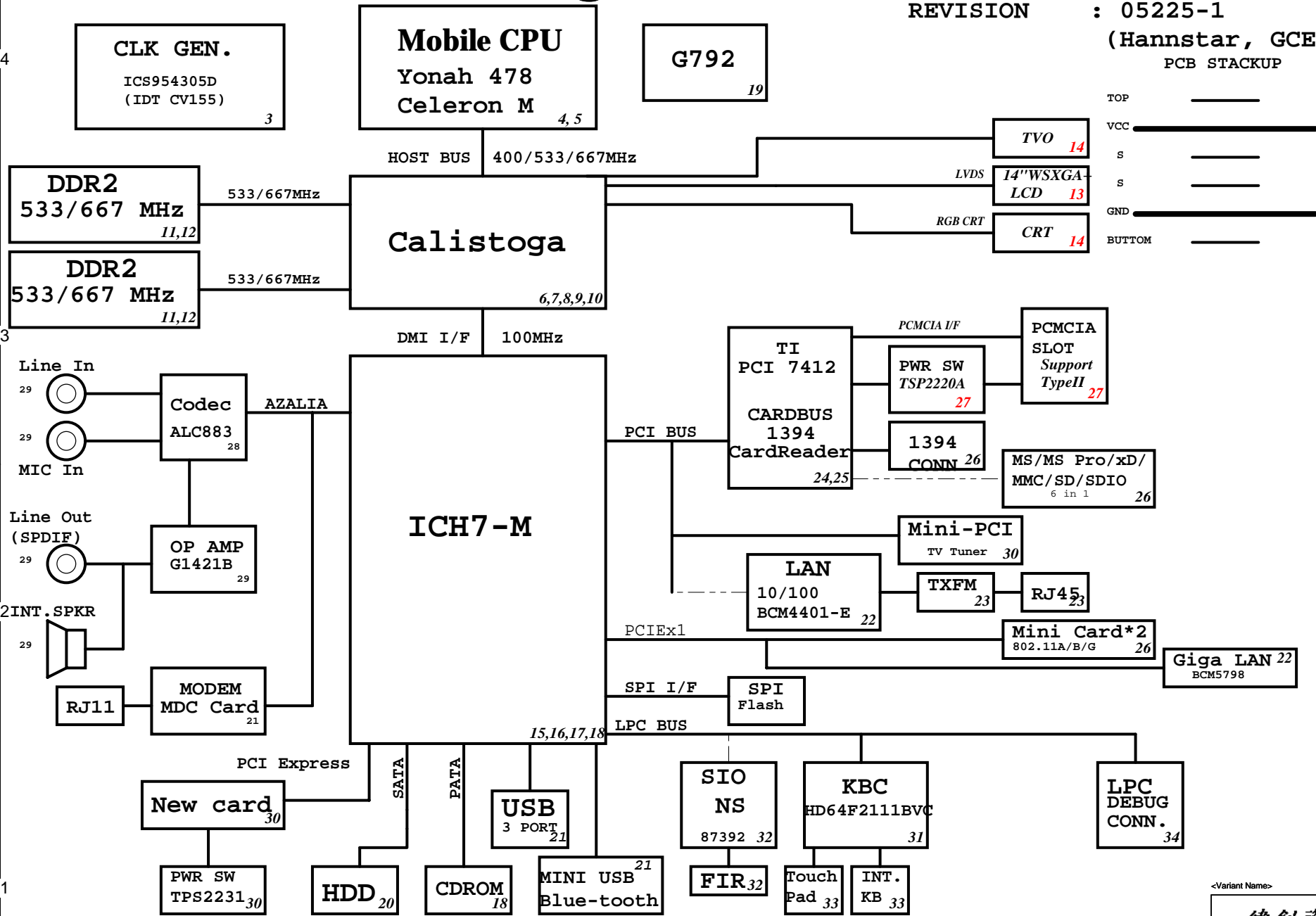


AG1 Block Diagram

Project code: 91.4A901.001
PCB P/N : 55.4A903.XXX
REVISION : 05225-1
(Hannstar, GCE)
PCB STACKUP

SYSTEM DC/DC	
TPS51120	41
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5
SYSTEM DC/DC	
MAX8743EE	42
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
TPS51100	
1D8V_S3	DDR_VREF
3D3V_S5	2D5V_S0
APL5332KAC	
3D3V_S5	2D5V_S0
APL5912-U	
3D3V_S5	1D5V_S0
MAXIM CHARGER	
MAX8725+Max1773	43
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA
CPU DC/DC	
ISL6262	39,40
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A



<Variant Name>

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Title	
BLOCK DIAGRAM	
Size A3	Document Number
AG1	
Date: Monday, January 09, 2006	Rev -1
Sheet 1 of 45	

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLFVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 Not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSusi_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSusi_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center

page 16

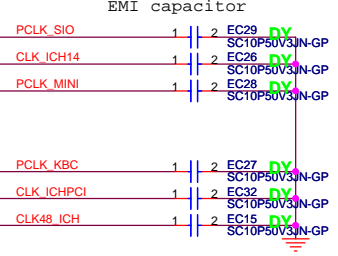
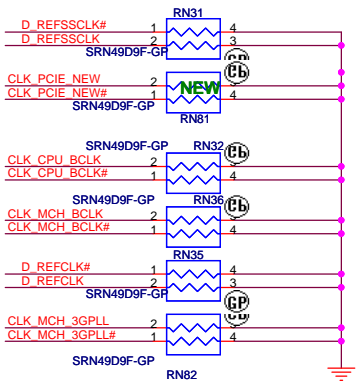
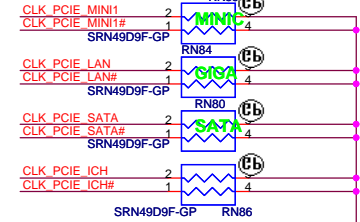
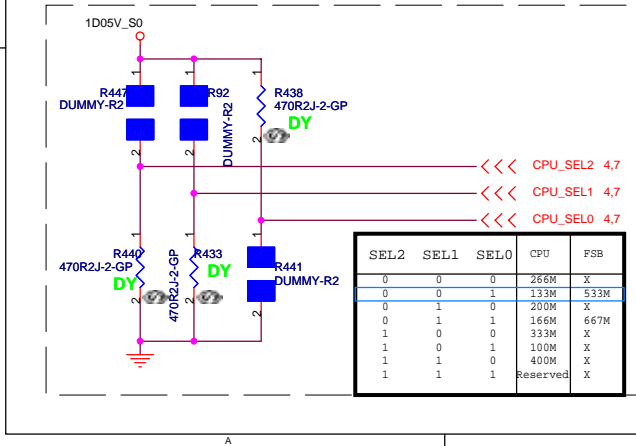
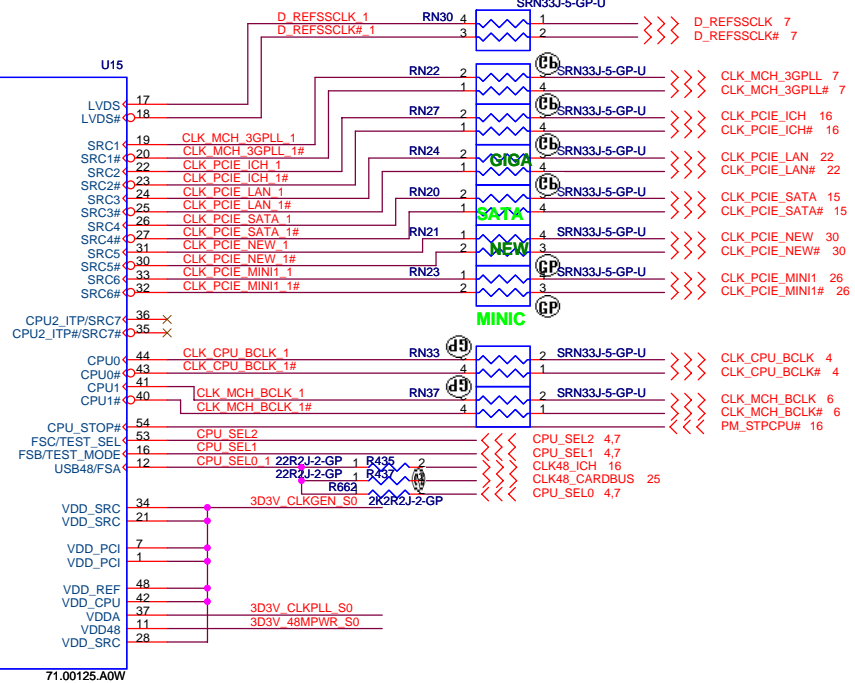
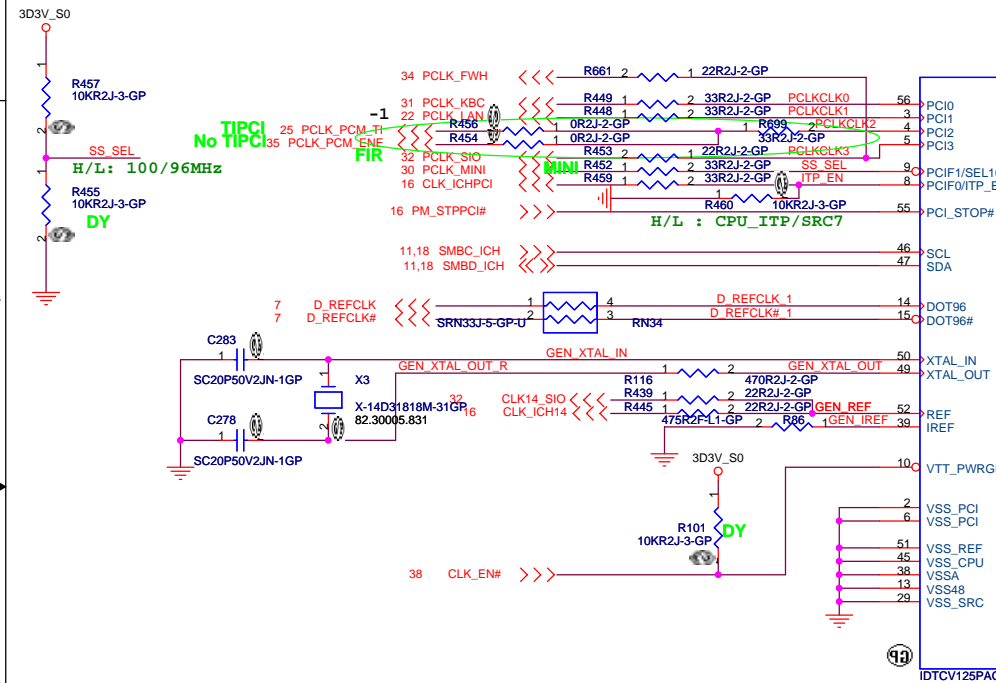
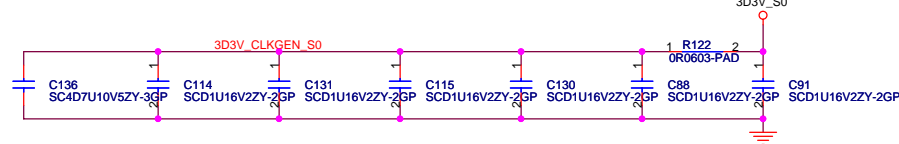
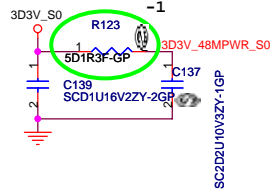
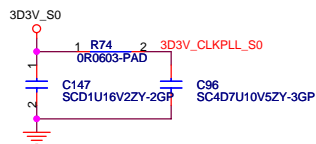
	IDSEL	INT -> PIRO	REQ/GNT
7412	22	A->G, B->B, C->F, D->G,	0
MiniPCI	21	A/C -> E B/D -> E	1
LAN	23	A -> H	2
1410	25	A->G, B->B,	0

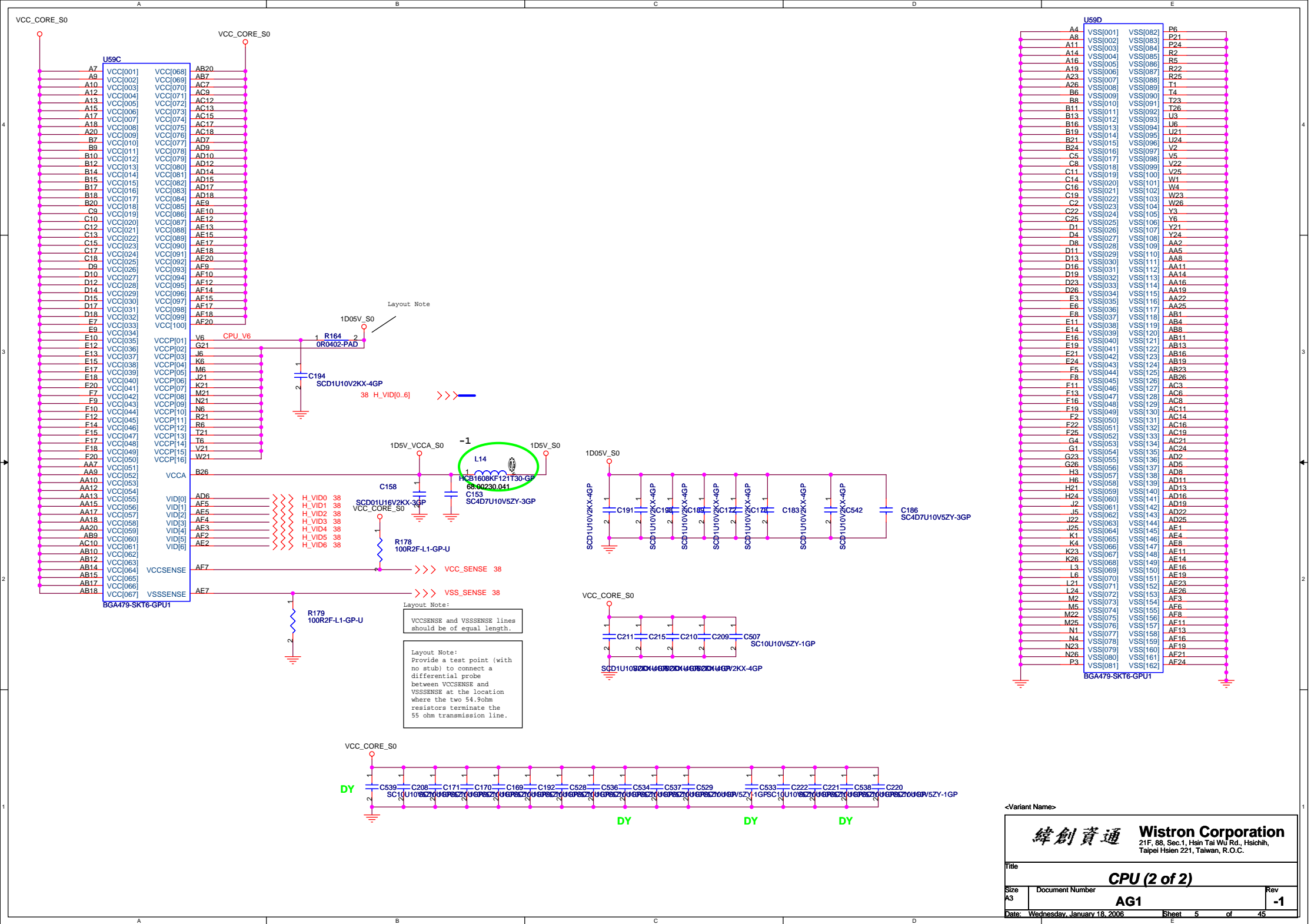
EDS 17050 0.71 page 7

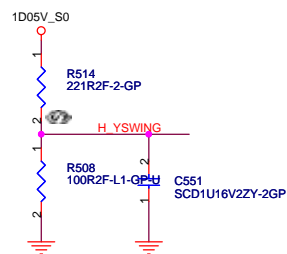
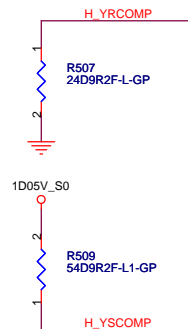
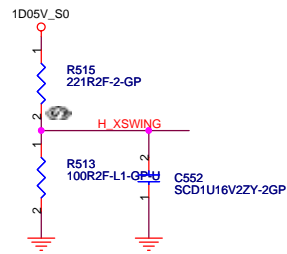
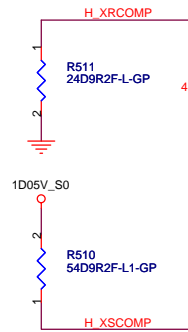
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

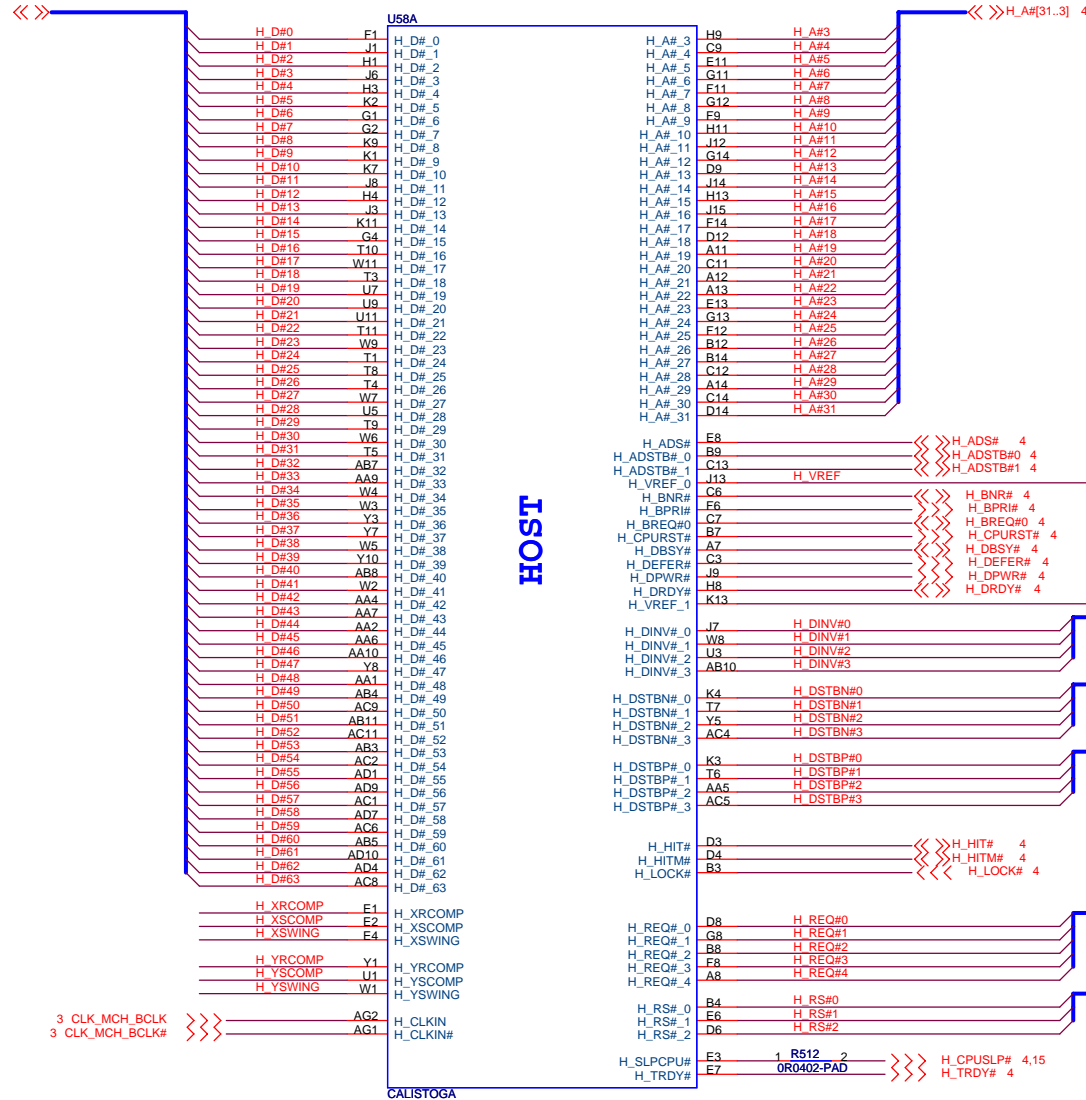
```
6/6 drawing SA
7/11 Rename for placement
```







Place them near to the chip (< 0.5")



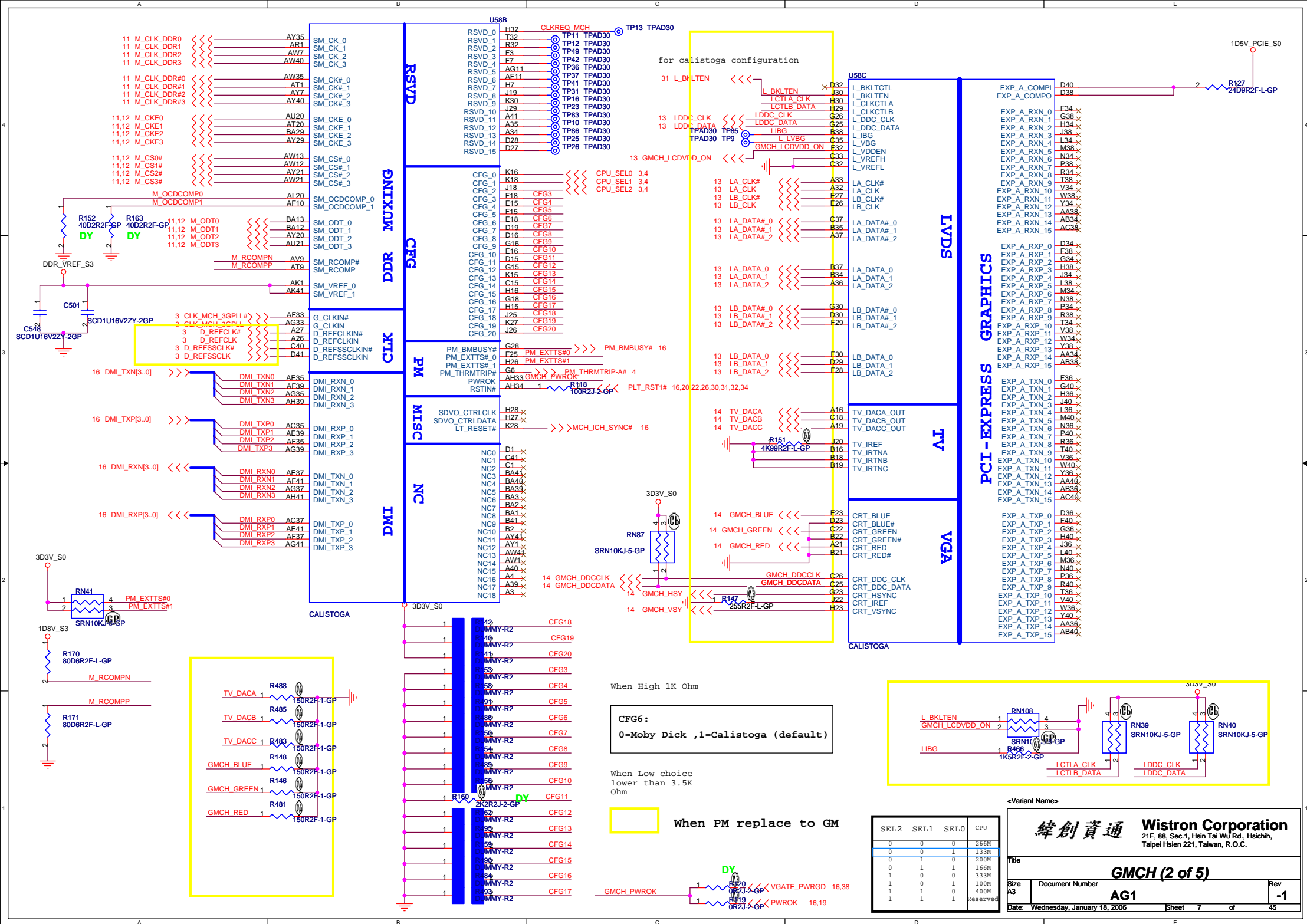
<Variant Name>

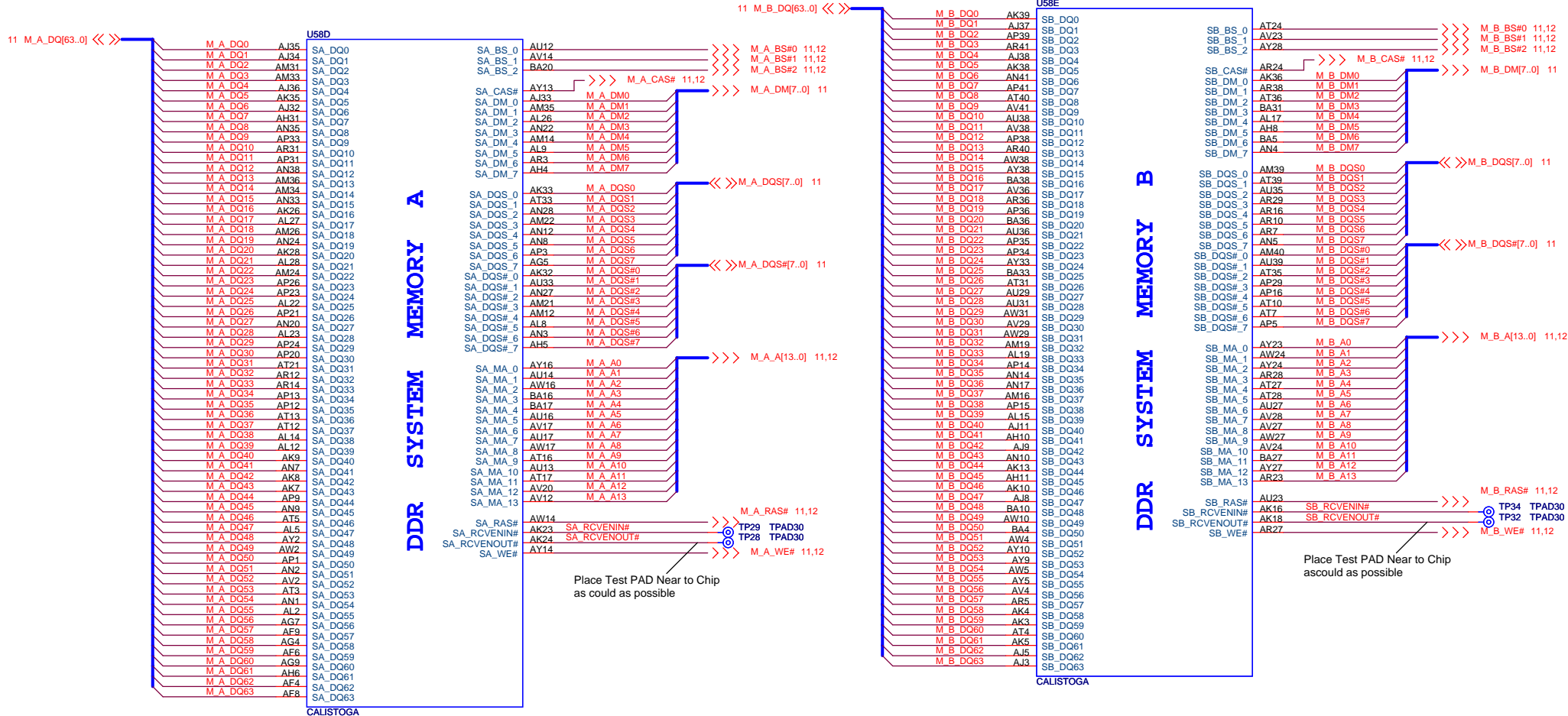
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (1 of 5)**

Size A3 Document Number **AG1** Rev **-1**

Date: Wednesday, January 18, 2006 Sheet 6 of 45

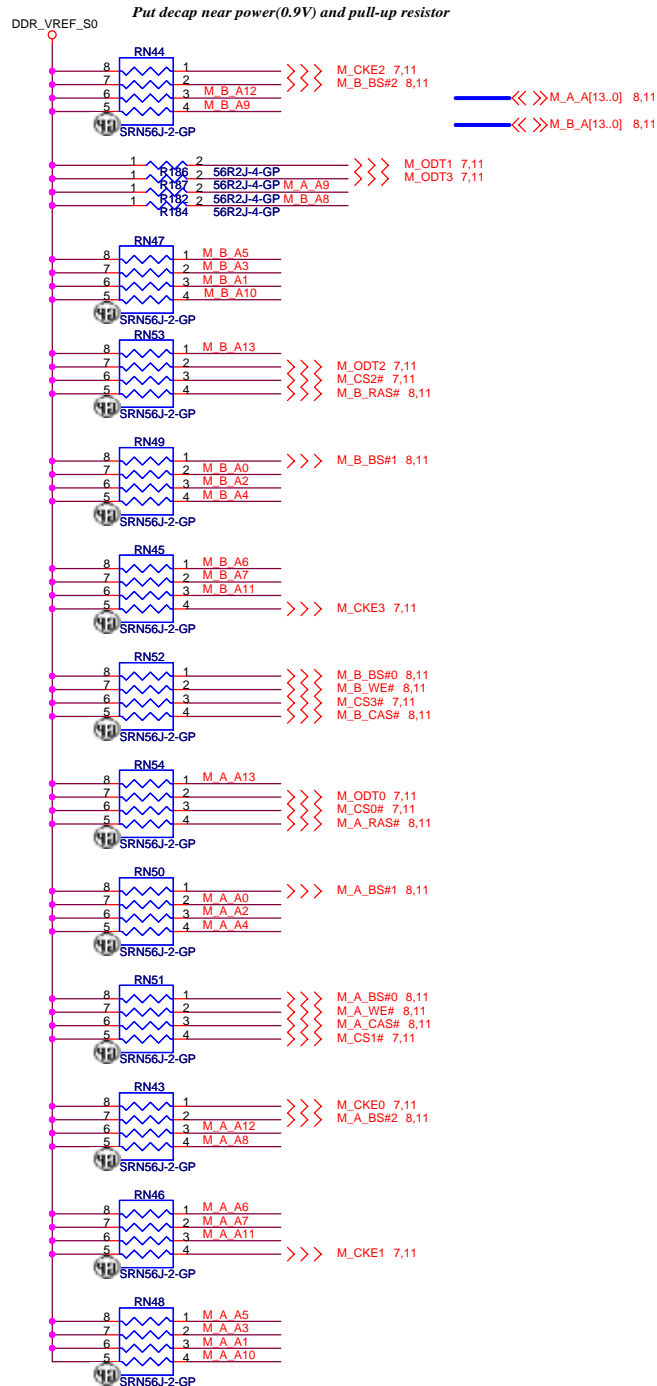




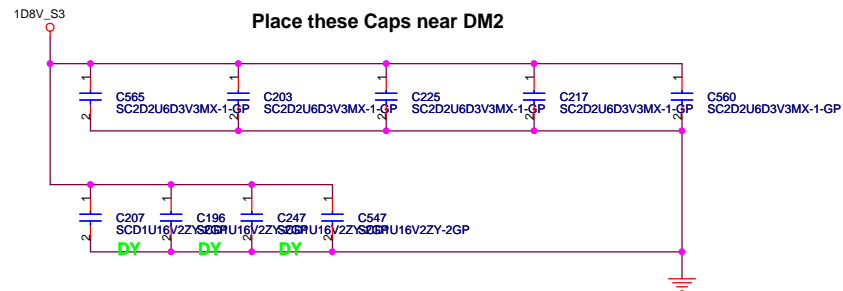
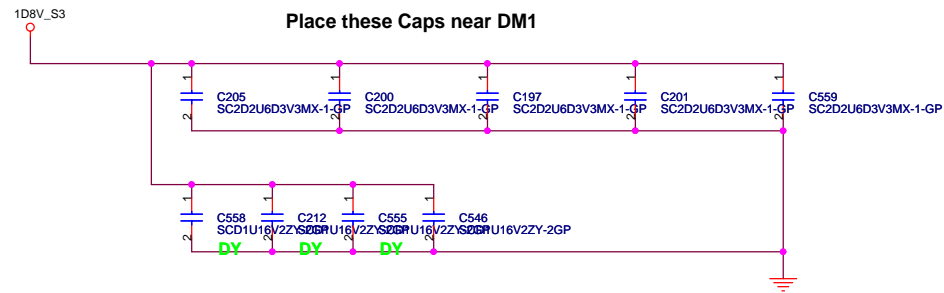
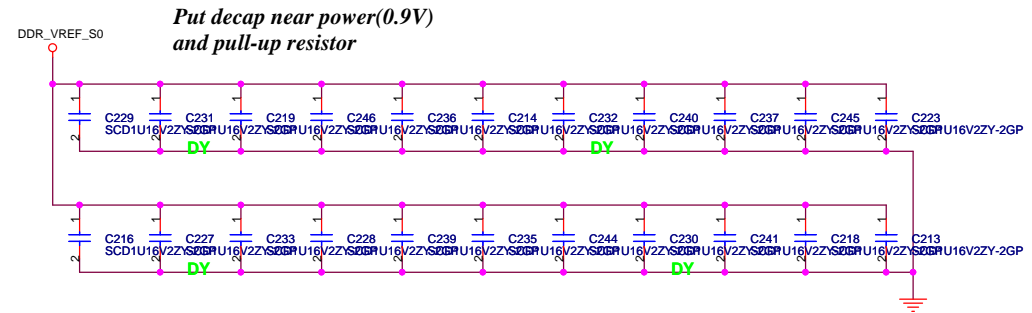




PARALLEL TERMINATION



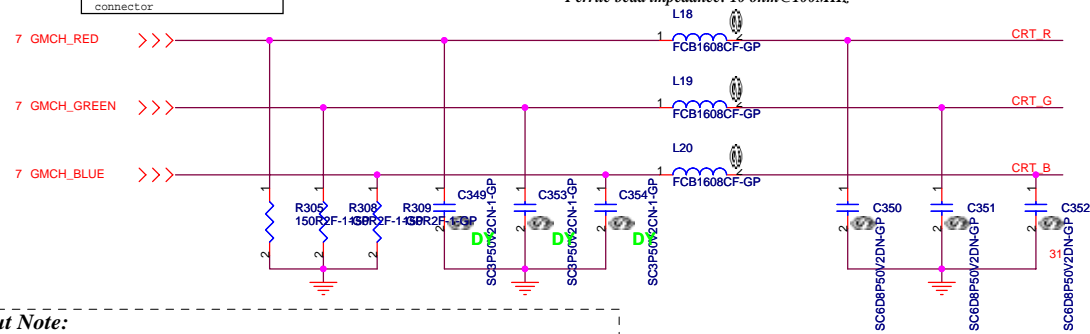
Decoupling Capacitor



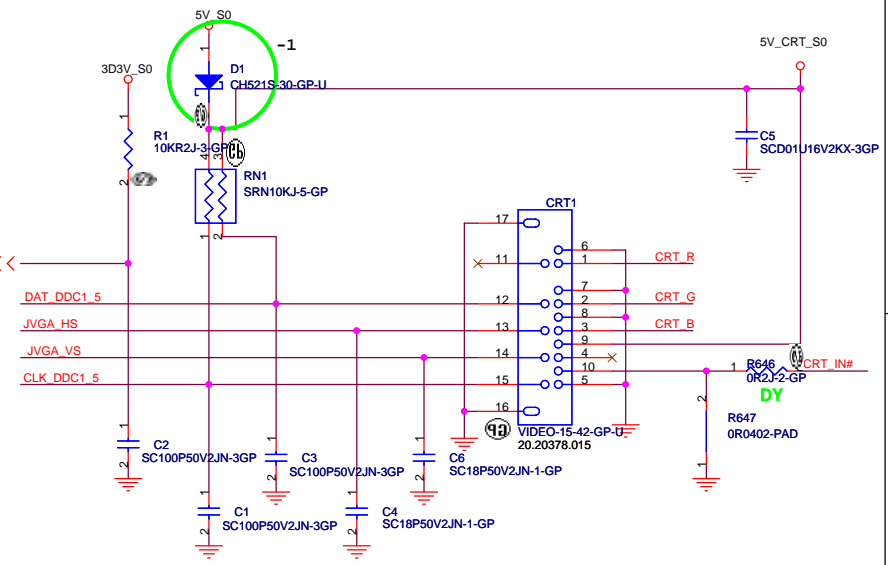
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

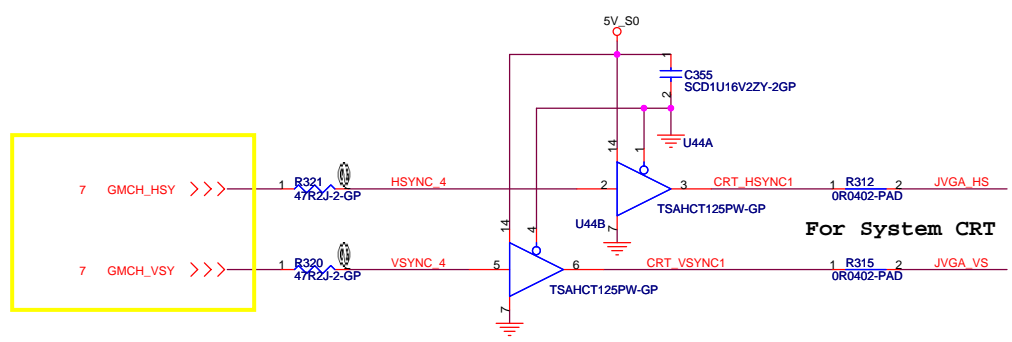
Ferrite bead impedance: 10 ohm@100MHz



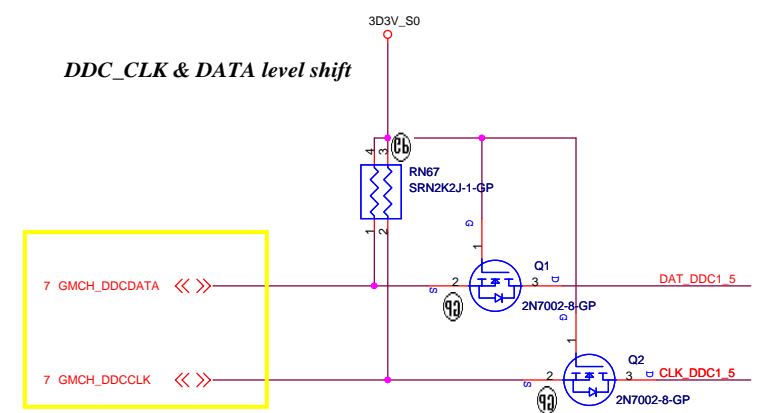
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



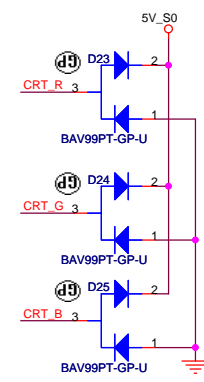
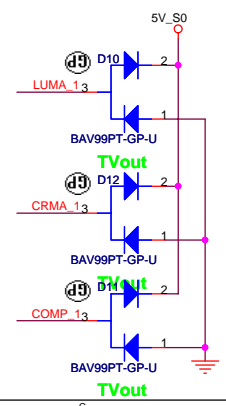
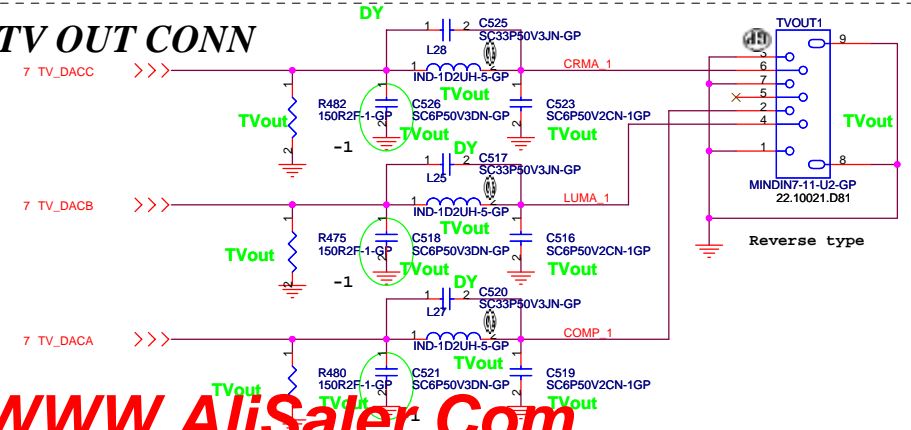
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV OUT CONN



<Variant Name>

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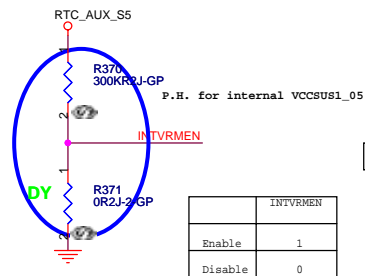
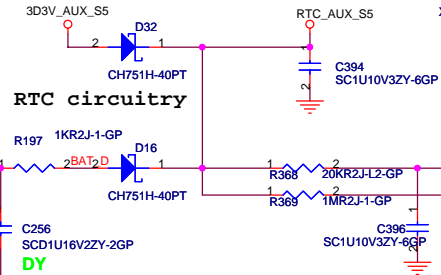
Title: **CRT/TV Connector**

Size A3 Document Number **AG1** Rev **-1**

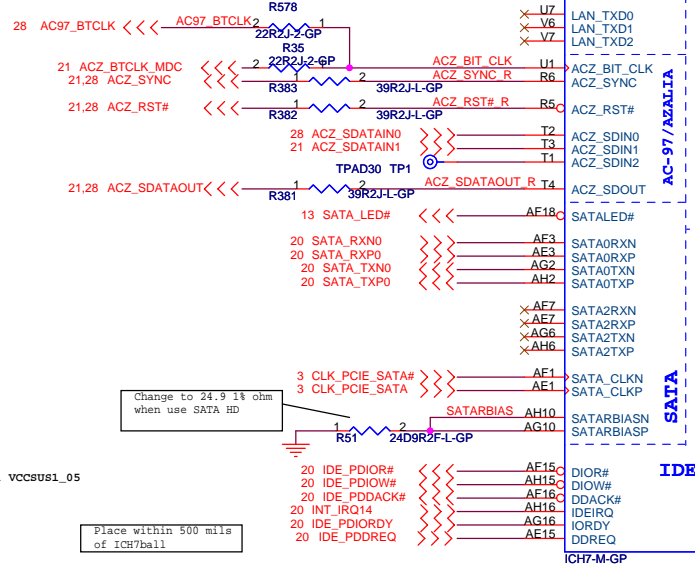
Date: Friday, February 24, 2006 Sheet 14 of 45

2nd source: 20.D0198.103

RTC circuitry



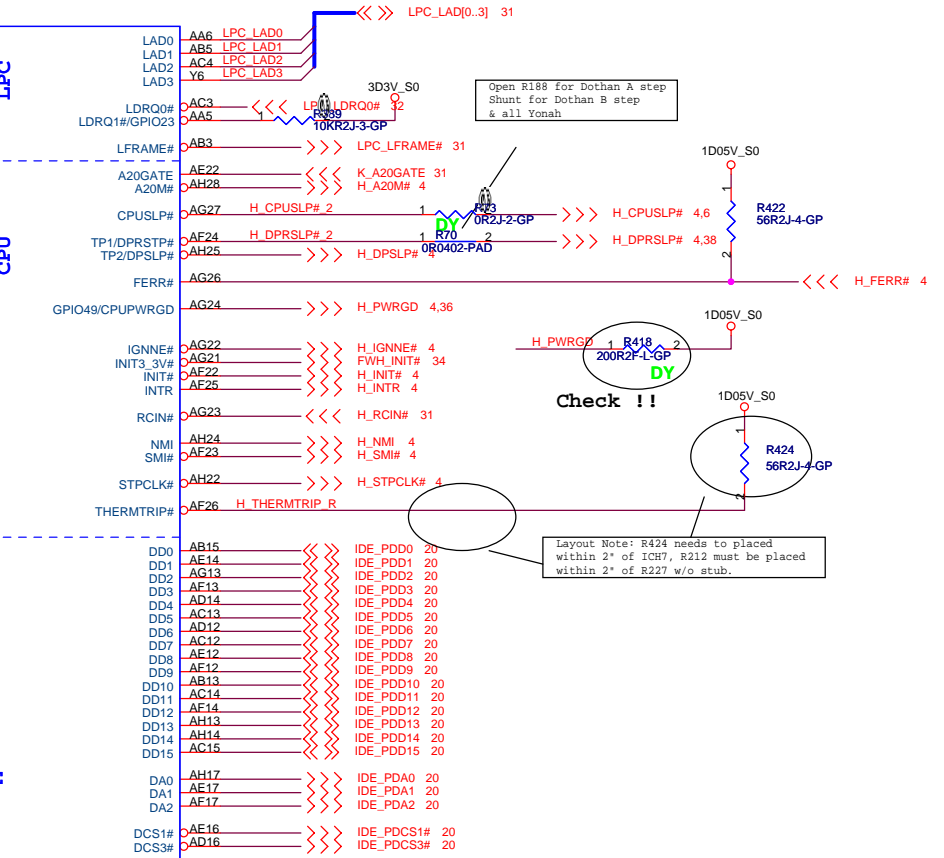
Placement Note:
Distance between the ICH7 M and cap on the "P" signal
should be identical distance between the ICH7 M and cap
on the "N" signal for same pair.

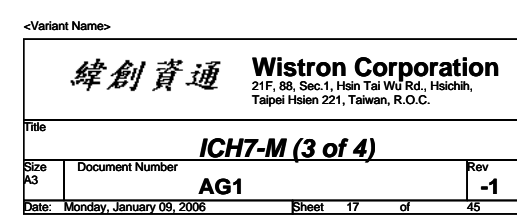


Change to 24.9 1% ohm
when use SATA HD

Place within 500 mils
of ICH7ball

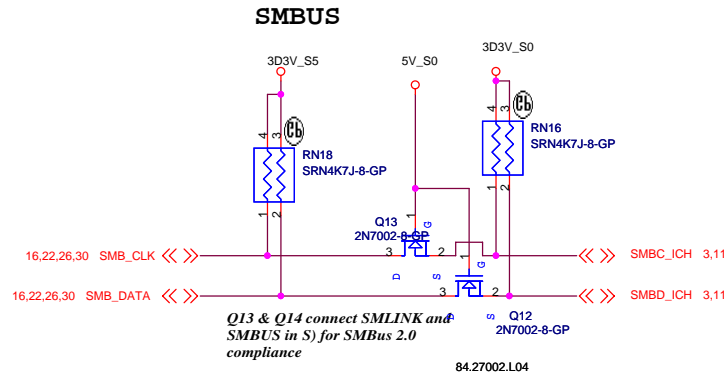
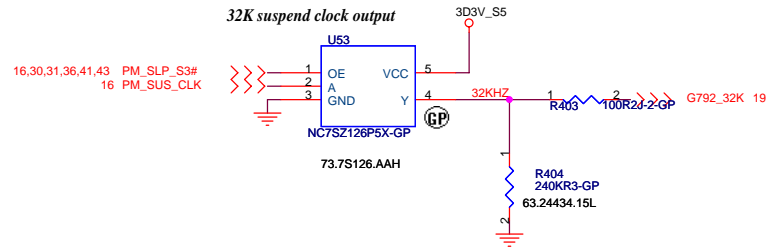
	INTVRMEN
Enable	1
Disable	0





U12E		
A4	VSS[1]	VSS[98]
A23	VSS[2]	VSS[99]
B1	VSS[3]	VSS[100]
B8	VSS[4]	VSS[101]
B11	VSS[5]	VSS[102]
B14	VSS[6]	VSS[103]
B17	VSS[7]	VSS[104]
B20	VSS[8]	VSS[105]
B26	VSS[9]	VSS[106]
B28	VSS[10]	VSS[107]
C2	VSS[11]	VSS[108]
C6	VSS[12]	VSS[109]
C27	VSS[13]	VSS[110]
D10	VSS[14]	VSS[111]
D13	VSS[15]	VSS[112]
D18	VSS[16]	VSS[113]
D21	VSS[17]	VSS[114]
D24	VSS[18]	VSS[115]
E1	VSS[19]	VSS[116]
E2	VSS[20]	VSS[117]
E4	VSS[21]	VSS[118]
E8	VSS[22]	VSS[119]
E15	VSS[23]	VSS[120]
F3	VSS[24]	VSS[121]
F4	VSS[25]	VSS[122]
F5	VSS[26]	VSS[123]
F12	VSS[27]	VSS[124]
F27	VSS[28]	VSS[125]
F28	VSS[29]	VSS[126]
G1	VSS[30]	VSS[127]
G2	VSS[31]	VSS[128]
G5	VSS[32]	VSS[129]
G6	VSS[33]	VSS[130]
G9	VSS[34]	VSS[131]
G14	VSS[35]	VSS[132]
G18	VSS[36]	VSS[133]
G21	VSS[37]	VSS[134]
G24	VSS[38]	VSS[135]
G25	VSS[39]	VSS[136]
G26	VSS[40]	VSS[137]
H3	VSS[41]	VSS[138]
H4	VSS[42]	VSS[139]
H5	VSS[43]	VSS[140]
H24	VSS[44]	VSS[141]
H27	VSS[45]	VSS[142]
H28	VSS[46]	VSS[143]
J1	VSS[47]	VSS[144]
J2	VSS[48]	VSS[145]
J5	VSS[49]	VSS[146]
J24	VSS[50]	VSS[147]
J25	VSS[51]	VSS[148]
J26	VSS[52]	VSS[149]
K24	VSS[53]	VSS[150]
K27	VSS[54]	VSS[151]
K28	VSS[55]	VSS[152]
L13	VSS[56]	VSS[153]
L15	VSS[57]	VSS[154]
L24	VSS[58]	VSS[155]
L25	VSS[59]	VSS[156]
L26	VSS[60]	VSS[157]
M3	VSS[61]	VSS[158]
M4	VSS[62]	VSS[159]
M5	VSS[63]	VSS[160]
M12	VSS[64]	VSS[161]
M13	VSS[65]	VSS[162]
M14	VSS[66]	VSS[163]
M15	VSS[67]	VSS[164]
M16	VSS[68]	VSS[165]
M17	VSS[69]	VSS[166]
M24	VSS[70]	VSS[167]
M27	VSS[71]	VSS[168]
M28	VSS[72]	VSS[169]
N1	VSS[73]	VSS[170]
N2	VSS[74]	VSS[171]
N5	VSS[75]	VSS[172]
N6	VSS[76]	VSS[173]
N11	VSS[77]	VSS[174]
N12	VSS[78]	VSS[175]
N13	VSS[79]	VSS[176]
N14	VSS[80]	VSS[177]
N15	VSS[81]	VSS[178]
N16	VSS[82]	VSS[179]
N17	VSS[83]	VSS[180]
N18	VSS[84]	VSS[181]
N24	VSS[85]	VSS[182]
N25	VSS[86]	VSS[183]
N26	VSS[87]	VSS[184]
P3	VSS[88]	VSS[185]
P4	VSS[89]	VSS[186]
P12	VSS[90]	VSS[187]
P13	VSS[91]	VSS[188]
P14	VSS[92]	VSS[189]
P15	VSS[93]	VSS[190]
P16	VSS[94]	VSS[191]
P17	VSS[95]	VSS[192]
P24	VSS[96]	VSS[193]
P27	VSS[97]	VSS[194]

ICH7-M-GP



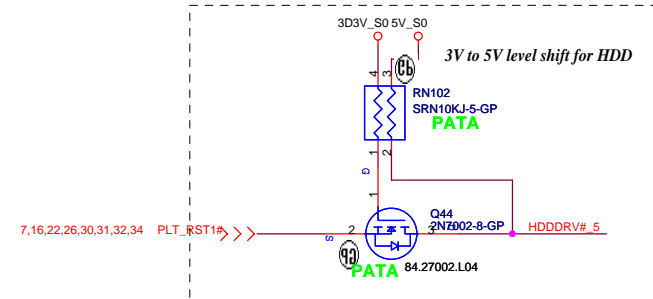
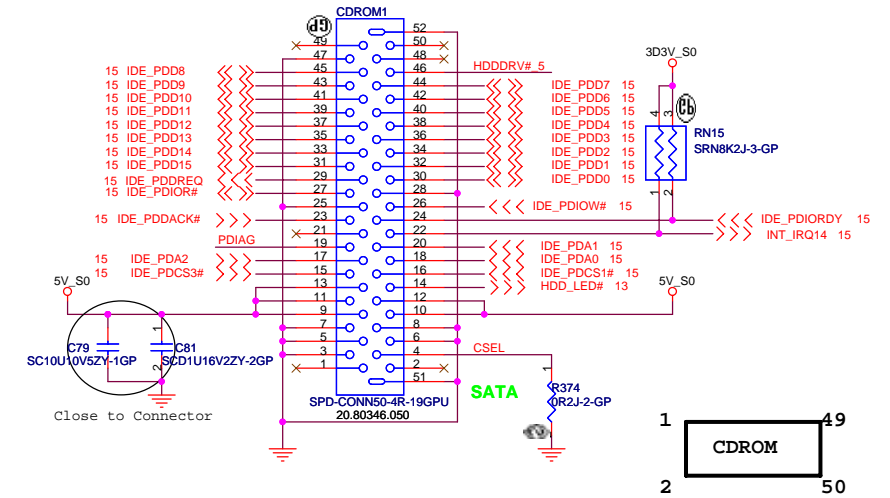
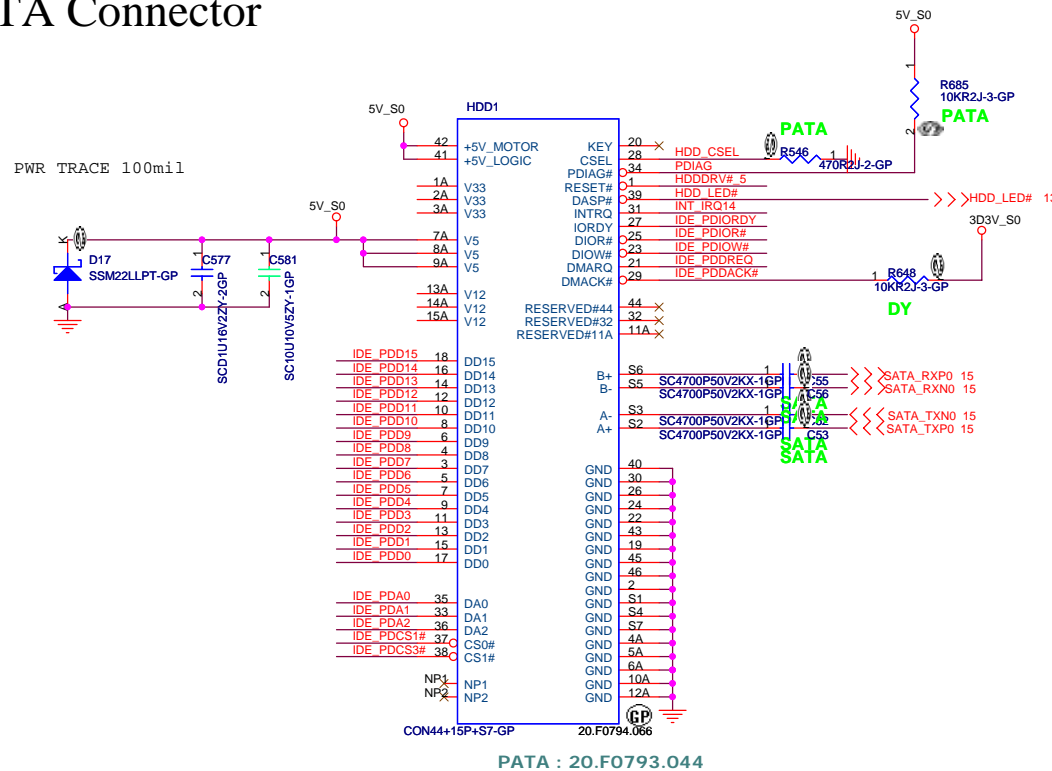
<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

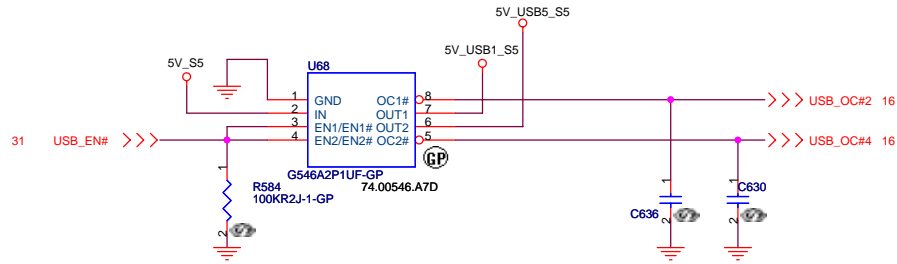
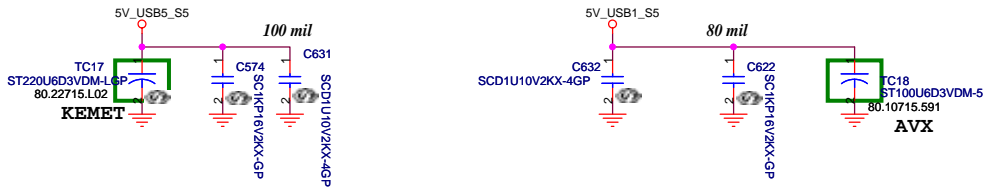
Title		
ICH7-M (4 of 4)/ODD		
Size	Document Number	Rev
A3	AG1	-1
Date: Wednesday, January 18, 2006 Sheet 18 of 45		

CDROM Connector

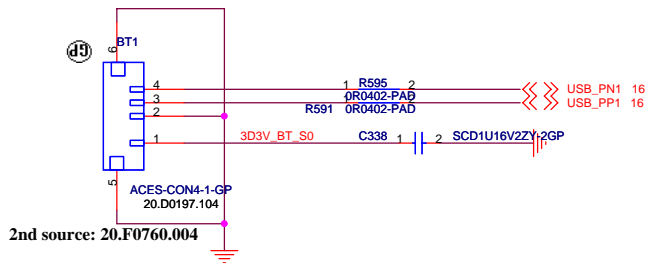
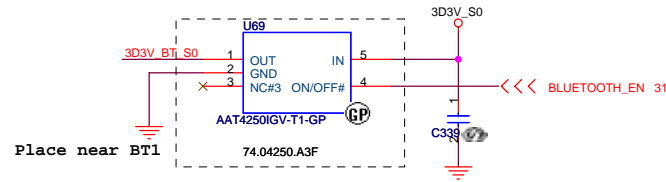
PWR TRACE 100mil



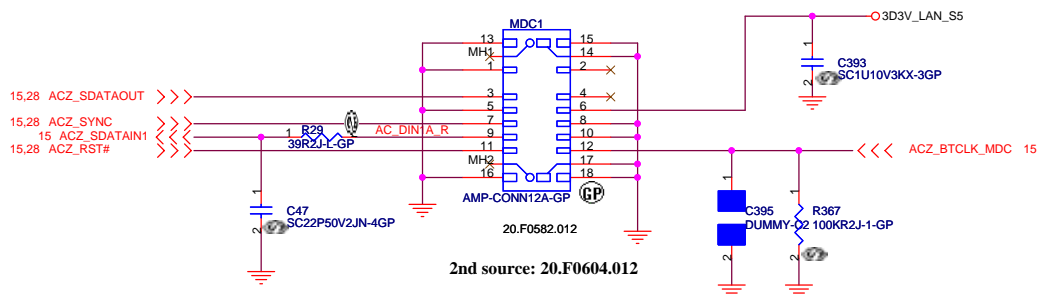
<Variant Name>



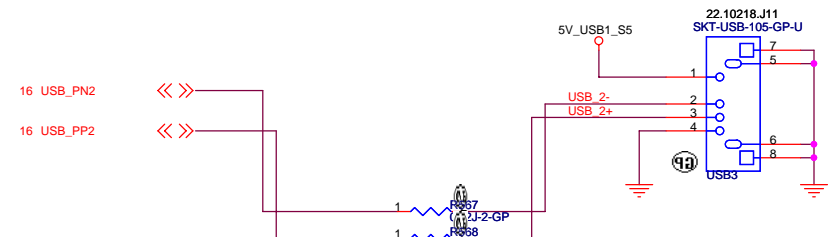
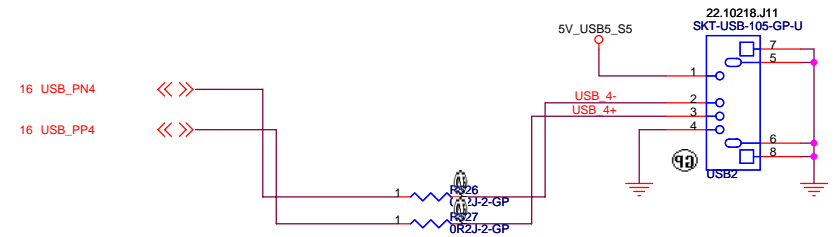
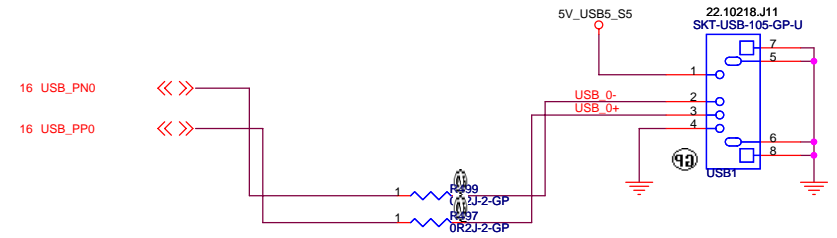
BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONN



USB PORT

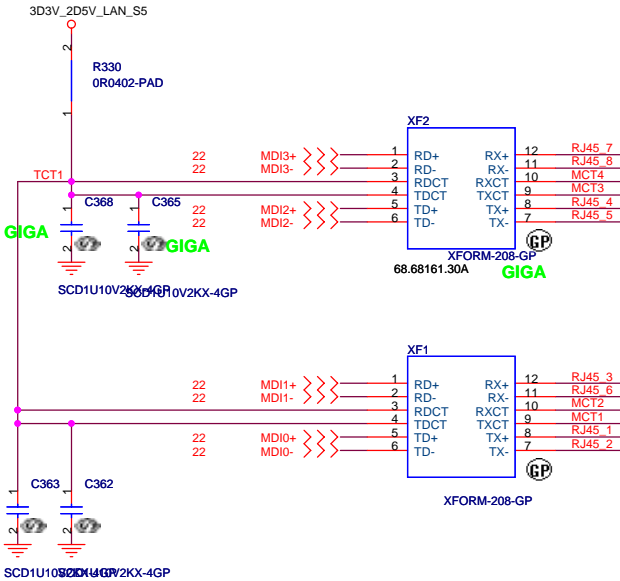


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
USB and MDC I/F			
Size	Document Number	Rev	
A3	AG1	-1	
Date:	Friday, February 24, 2006	Sheet	21 of 45

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



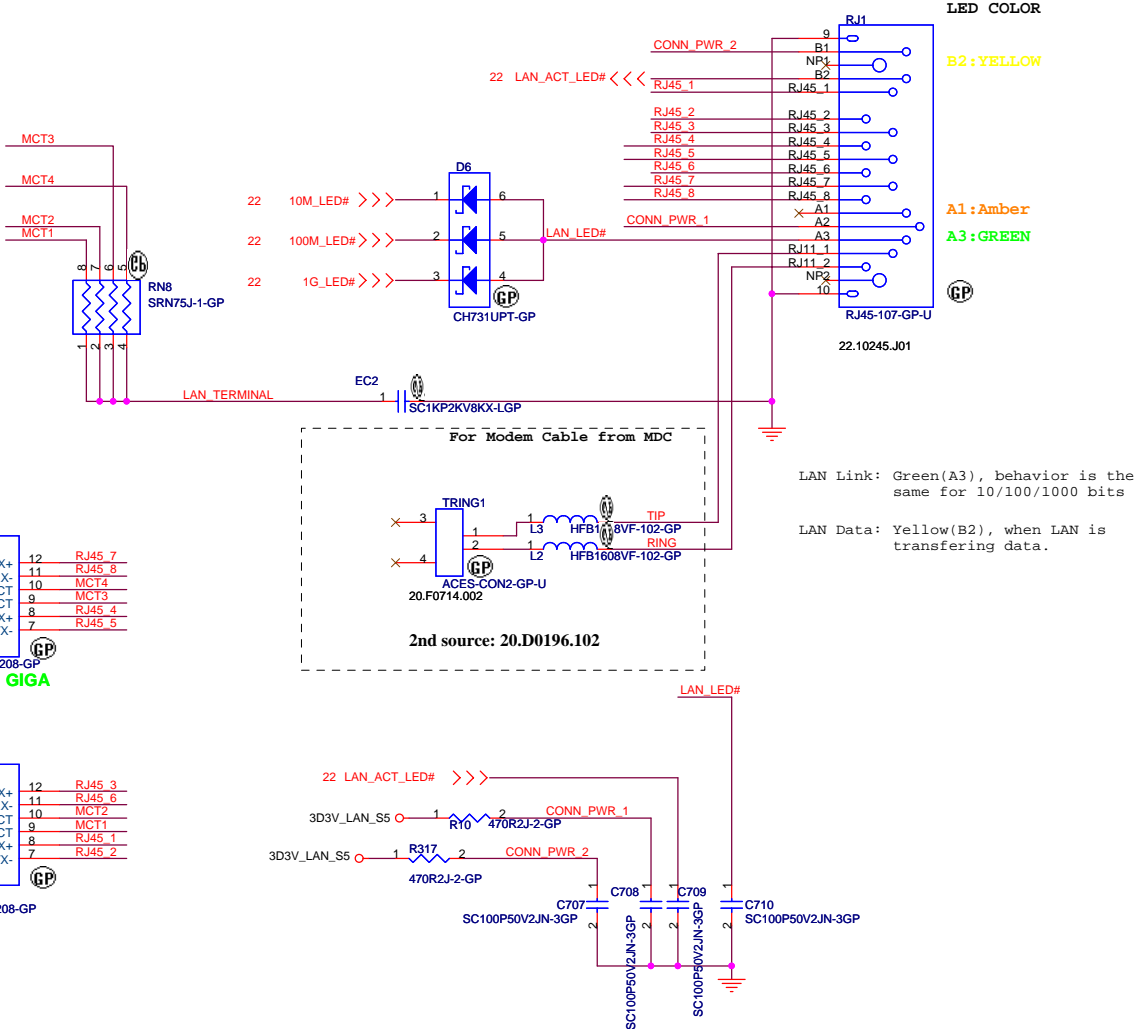
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN Connector

Size A3

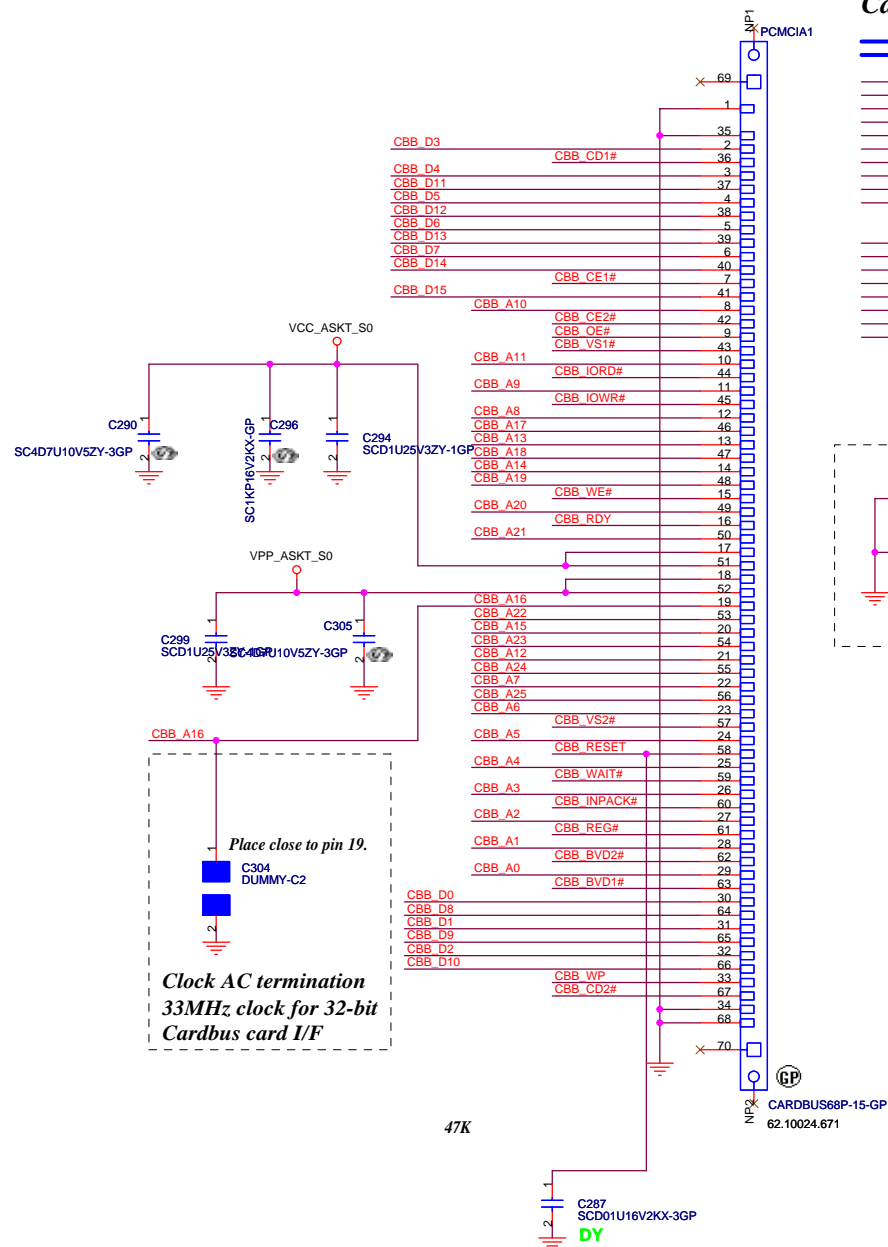
Document Number AG1

Date: Wednesday, January 18, 2006

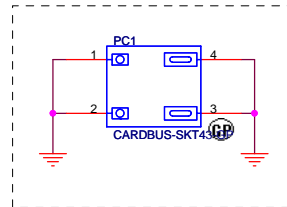
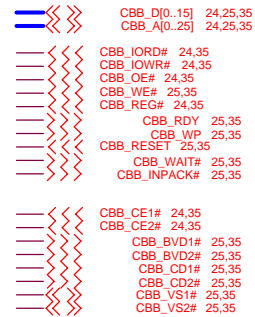
Rev -1

Sheet 23 of 45

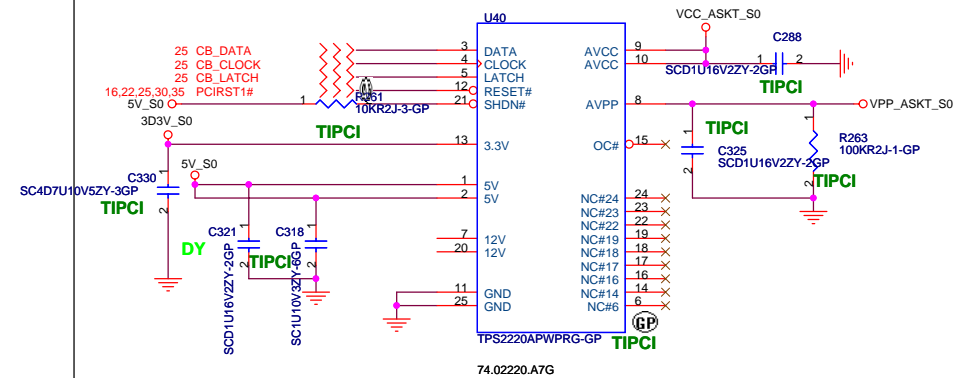
PCMCIA Socket



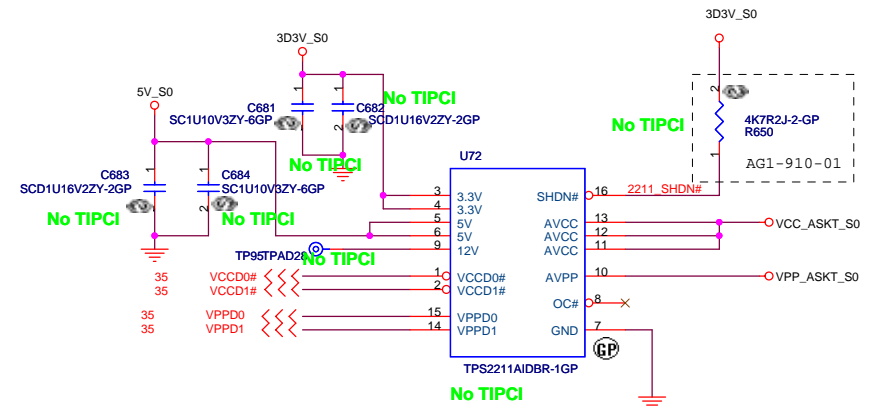
Cardbus I/F



TI Power switch



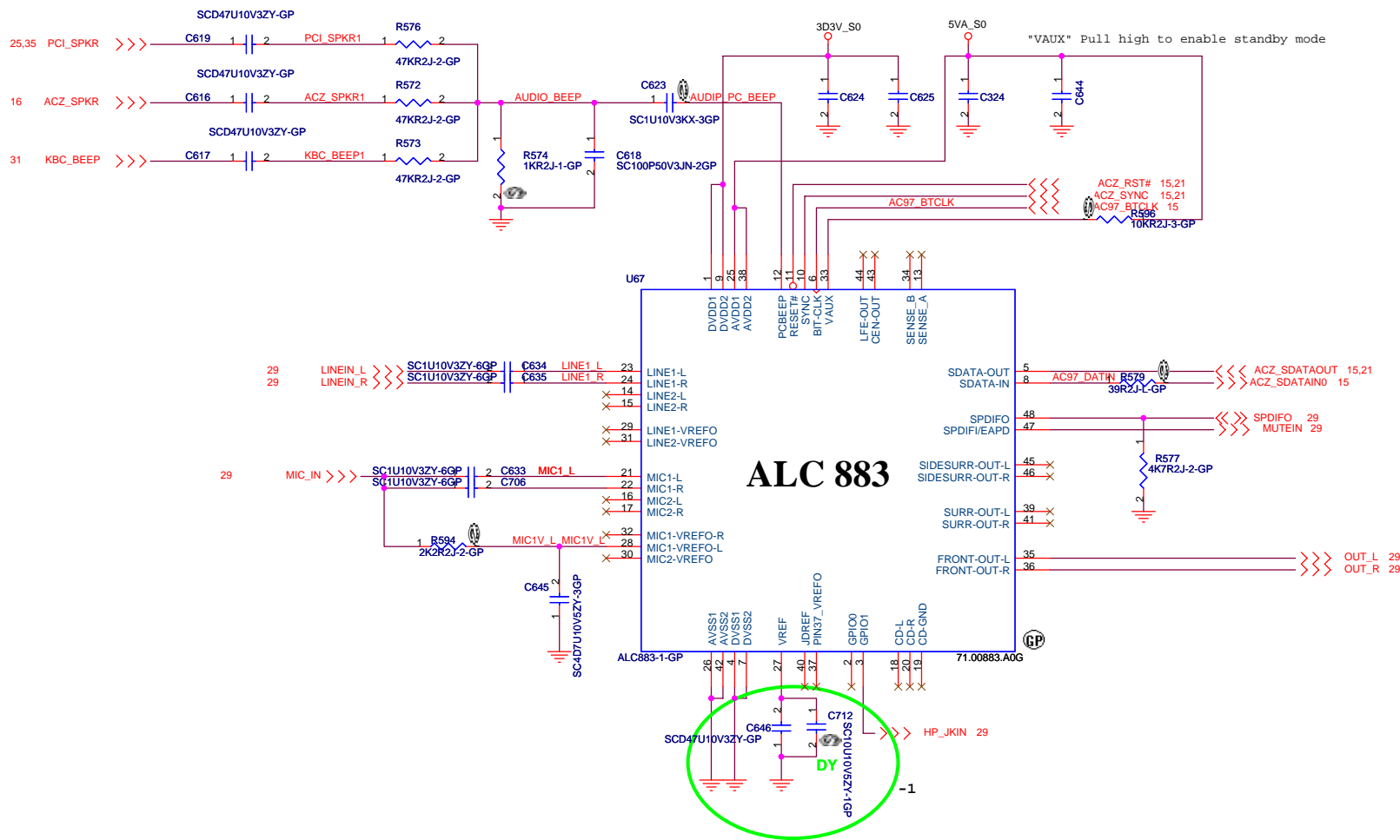
ENE Power switch



<Variant Name>

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Title				PCMCIA			
Size A3	Document Number					Rev	
	AG1					-1	
Date: Friday, February 24, 2006			Sheet	27	of	45	



- 1) When GPIO0 is asserted, AMP should be muted.
- 2) SPDIFO should be turned off when not used.

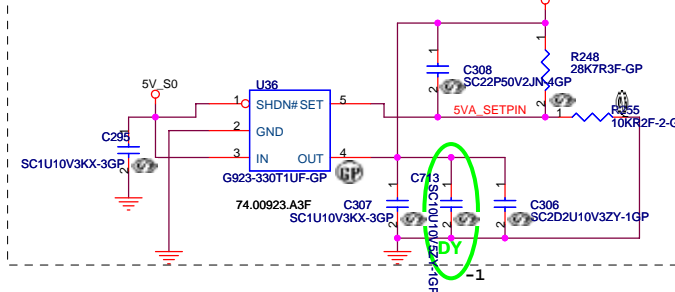
Configuration:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP, Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X

1/1/1 MIC1 MIC2 MIC3 Mic input

POWER GENERATE

Layout
20 mil



<Variant Name>

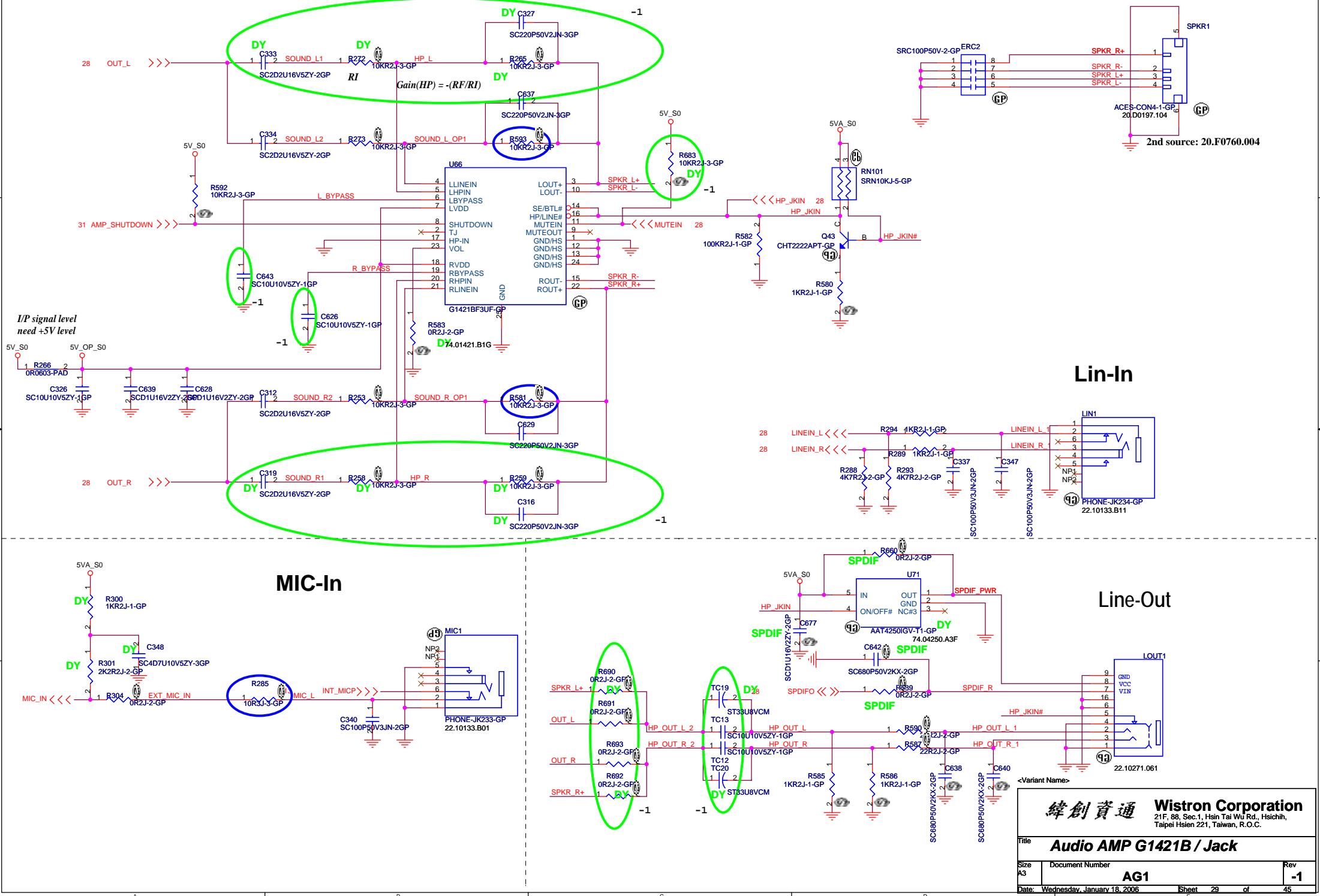
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

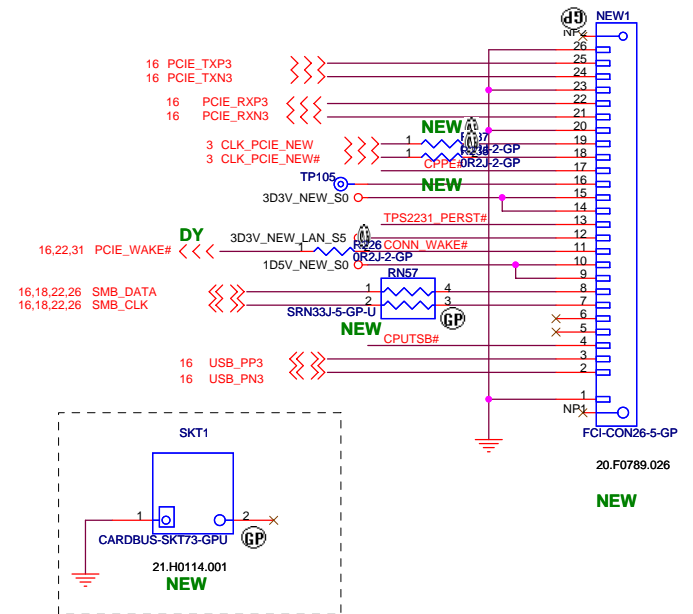
Title **Azalia codec ALC883**

Size A3 Document Number **AG1** Rev **-1**
Date: Wednesday, January 18, 2006 Sheet 28 of 45

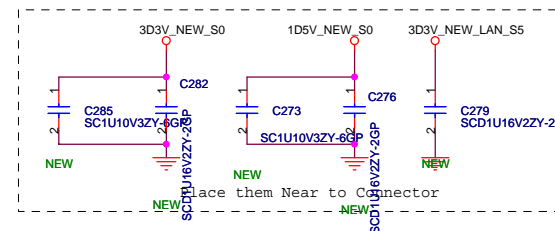
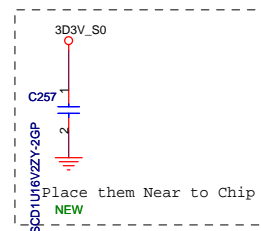
AUDIO OP AMPLIFIER

Internal SPKR



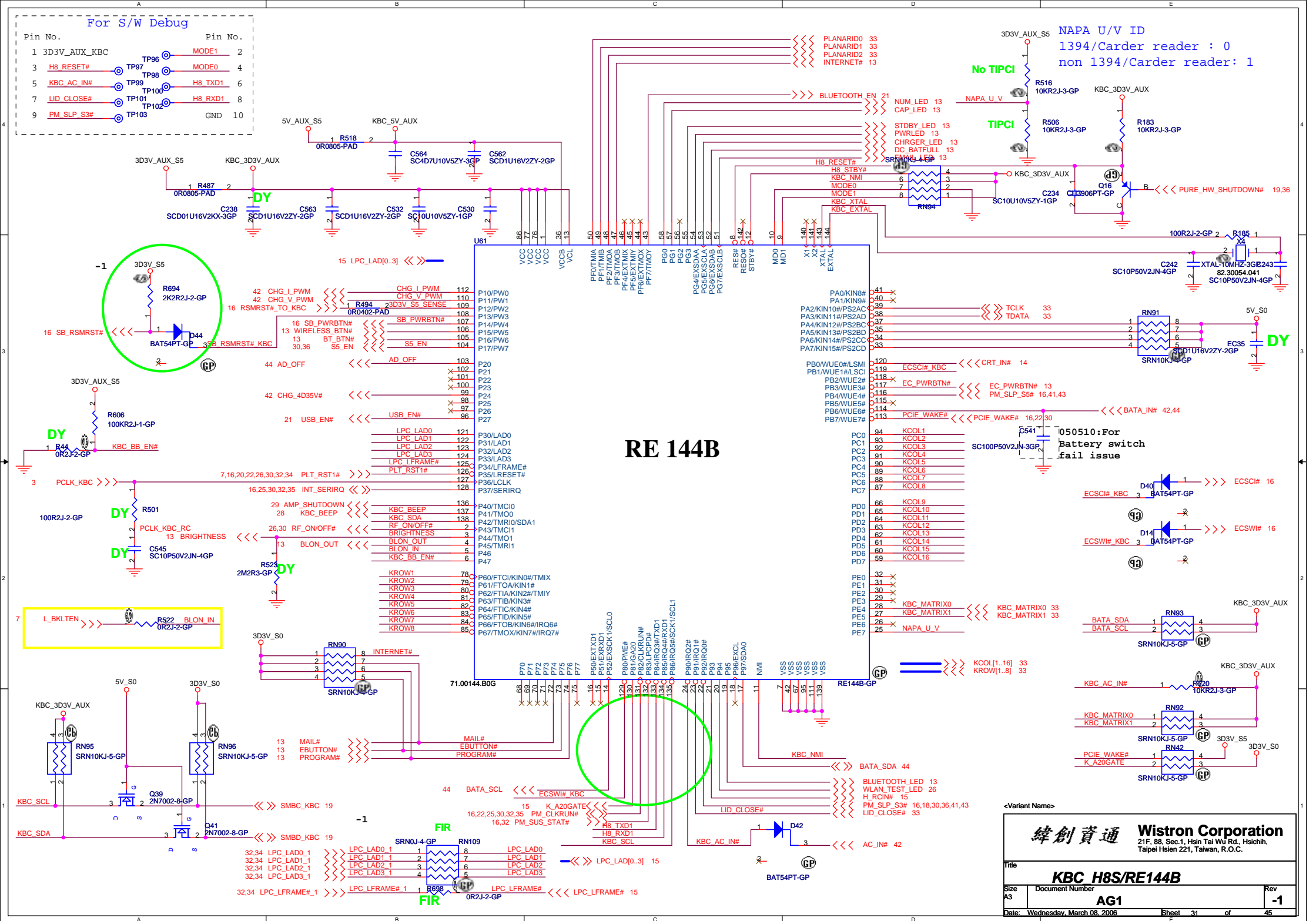


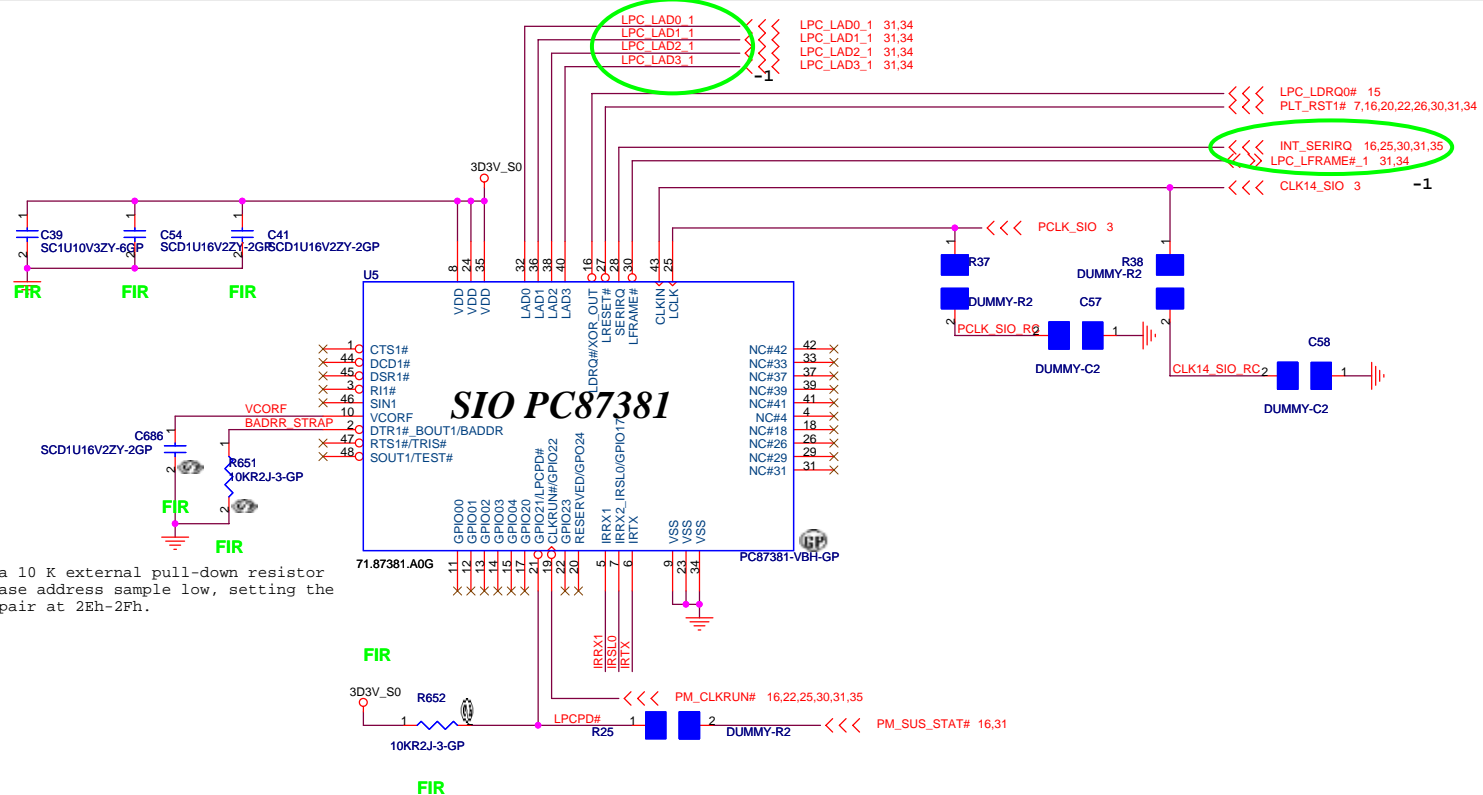
Reserve the symbol
for bottom side
connector



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Taipei Hsien 221, Taiwan, R.O.C.

Size A3	Document Number AG1	Rev -1
Date: Thursday, March 09, 2006	Sheet 30 of 45	

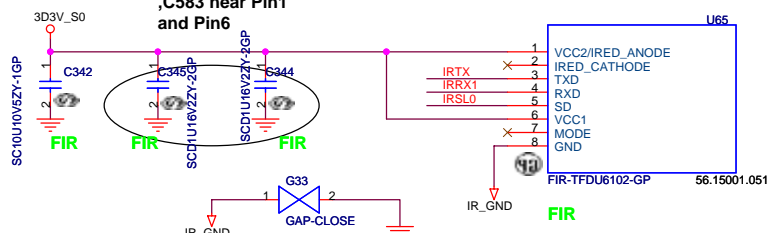




VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32

Place C581
,C583 near Pin1
and Pin6

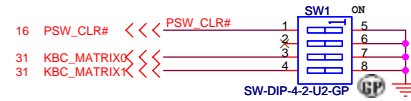


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		SIO 87392 / FIR	
Size	Document Number	Rev	
A3	AG1	-1	
Date:	Wednesday, January 18, 2006	Sheet	32 of 45

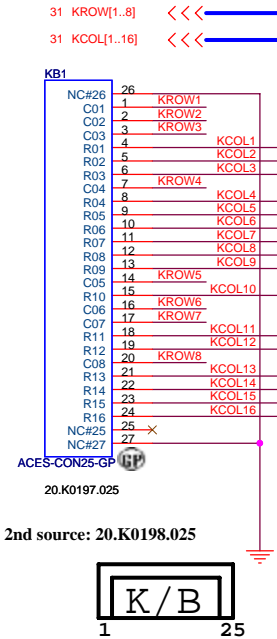
Internal KeyBoard Connector



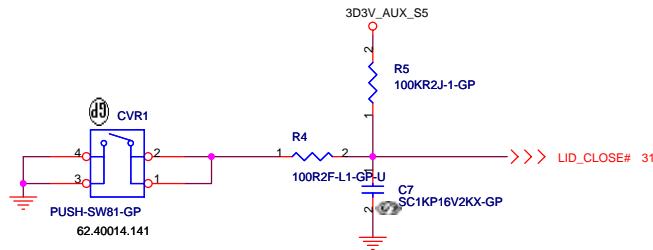
Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

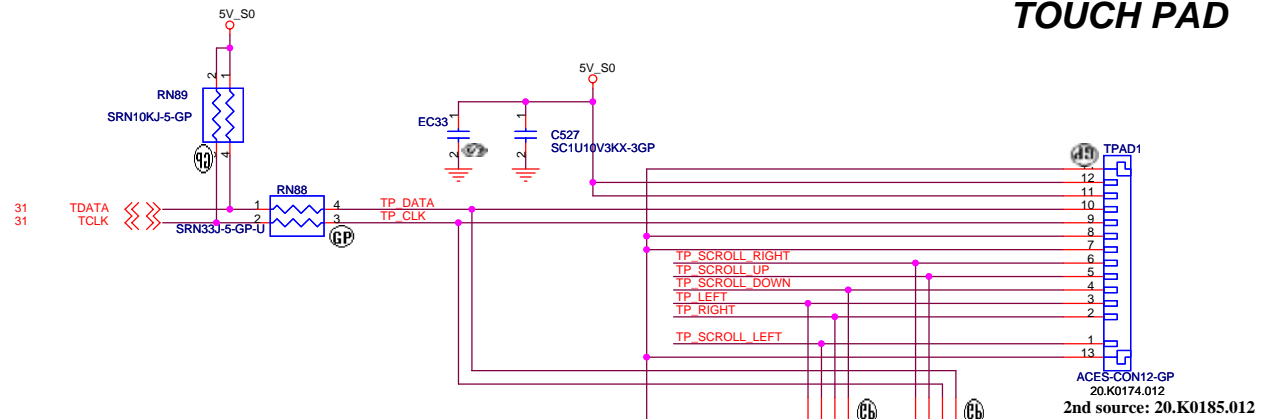
	Low Active
PSW_CLR#	1 - 5 ON
KBC_BB_EN#	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON



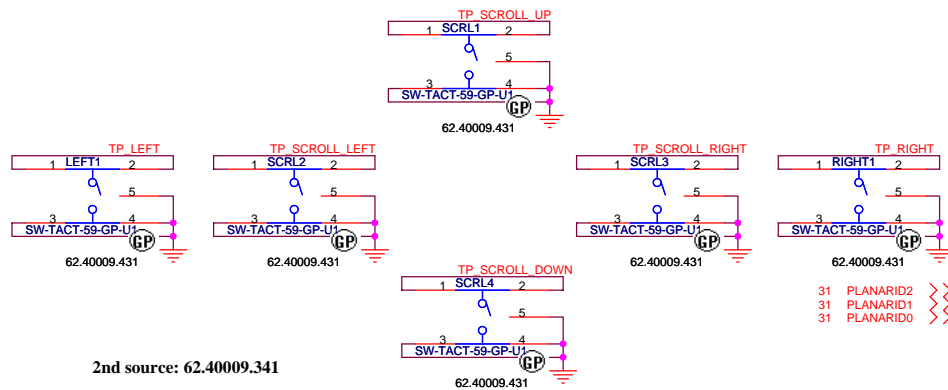
COVER SWITCH



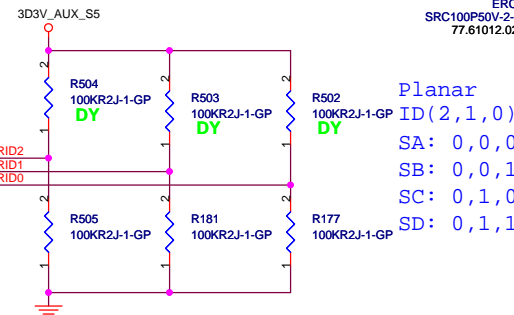
TOUCH PAD



SCROLL KEY

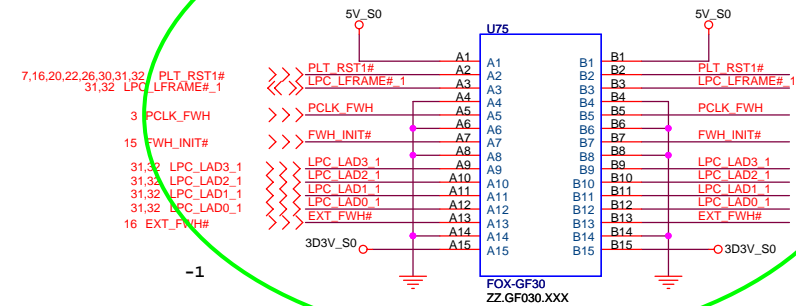


2nd source: 62.40009.431



Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1

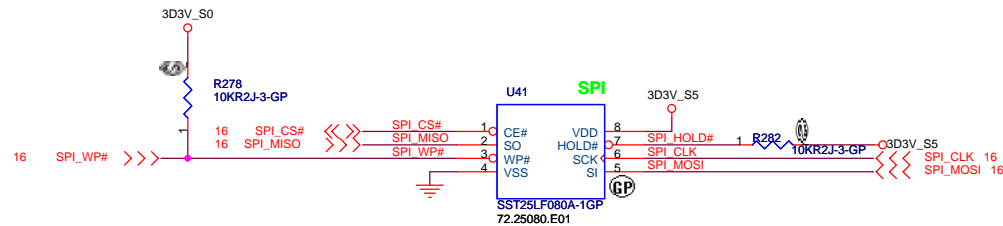
GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

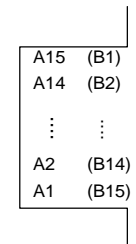
SPI FLASH ROM

8M Bits



SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

TOP VIEW



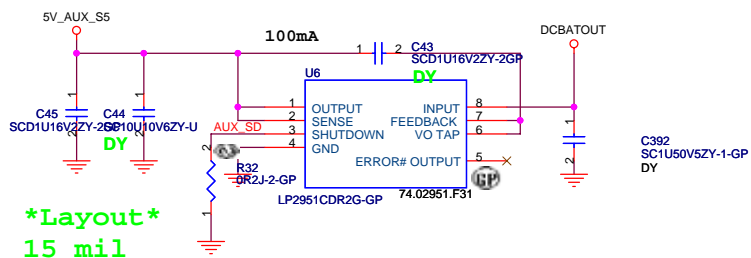
(BOTTOM VIEW)

<Variant Name>

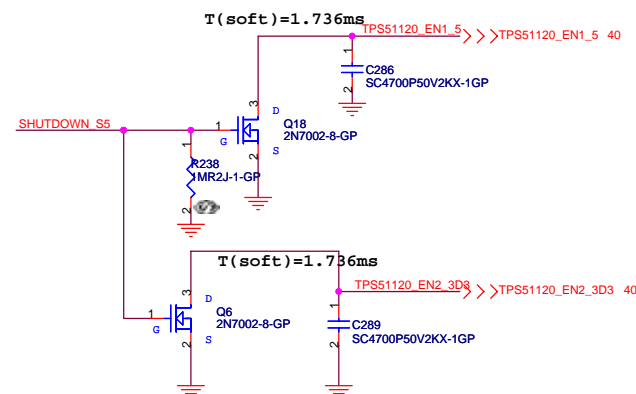
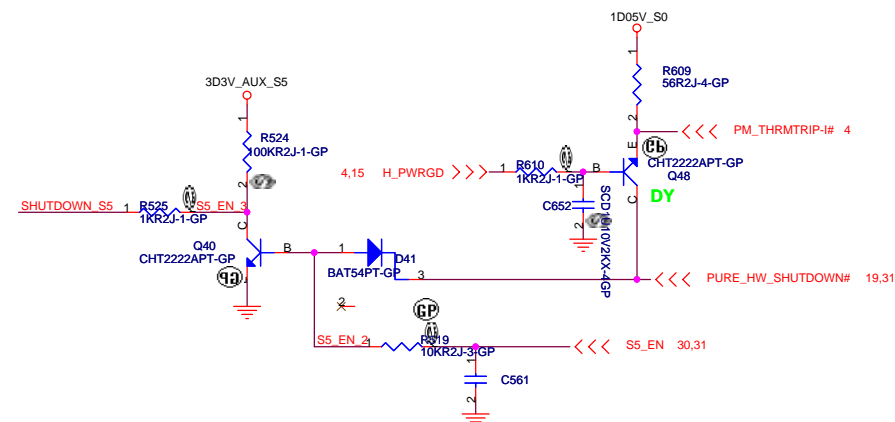
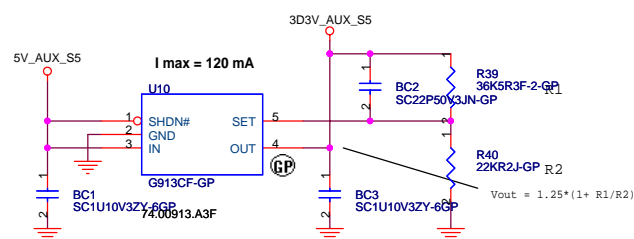
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		BIOS : SPI	
Size	Document Number	AG1	
A3		-1	
Date:	Wednesday, January 18, 2006	Sheet	34 of 45

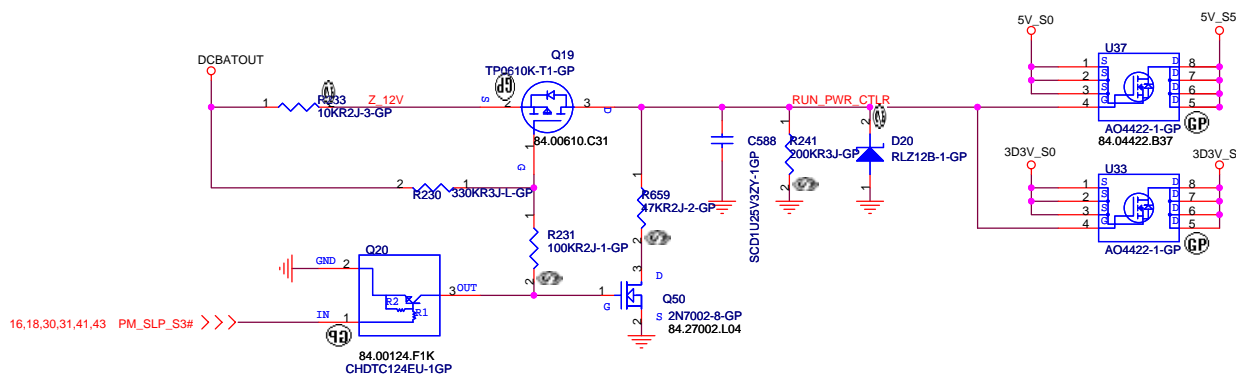
Aux Power



Layout
15 mil



Run Power

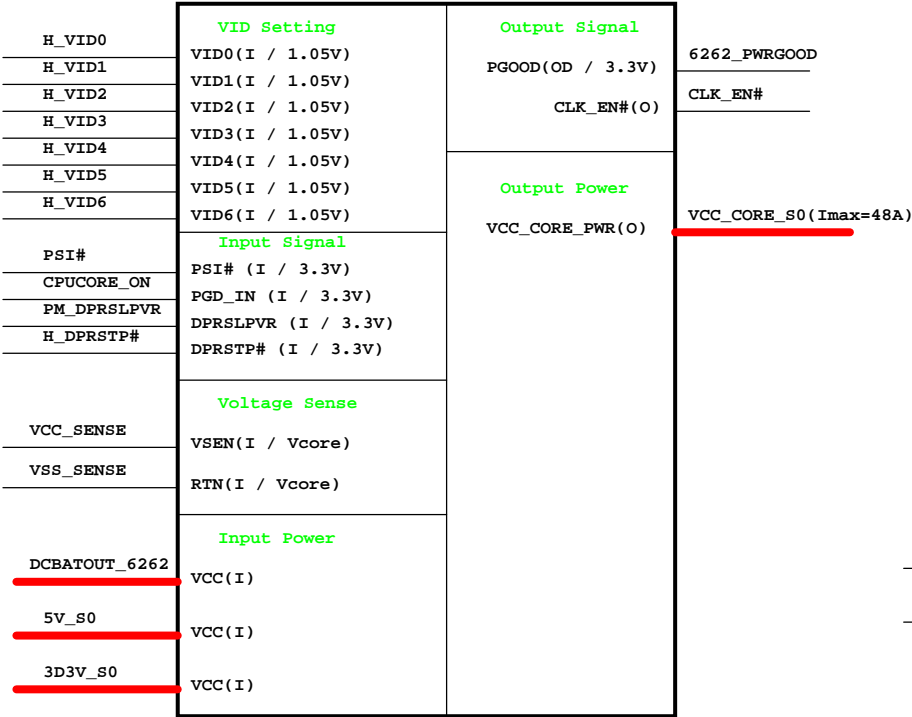


<Variant Name>

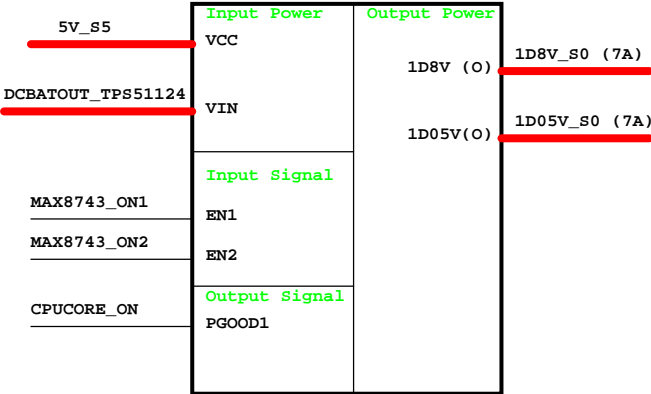
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
RUN and AUX POWER			
Size	Document Number	Rev	
A3	AG1	-1	
Date:	Wednesday, January 18, 2006	Sheet	36 of 45

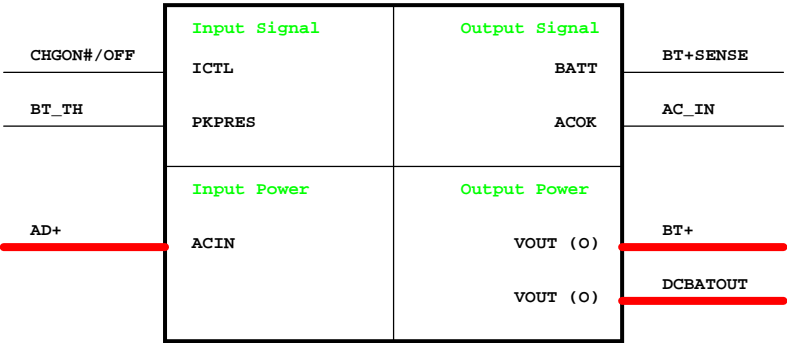
CPU_CORE
Intersil ISL6262



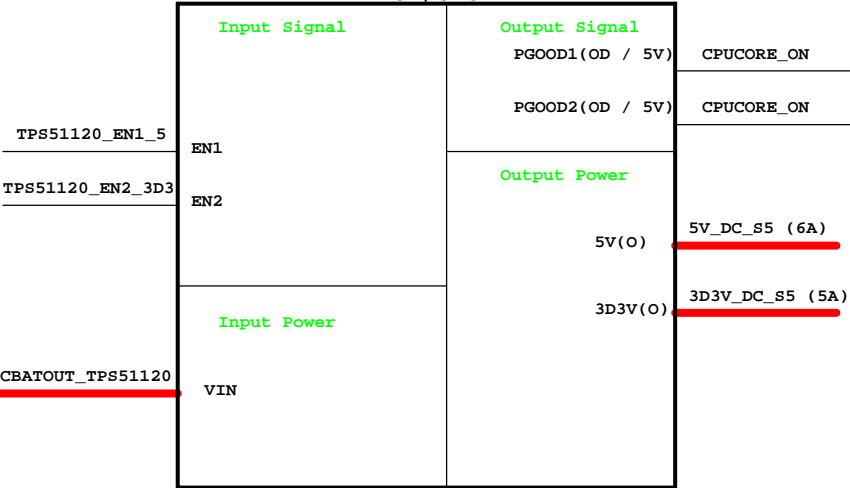
MAX8743
1D8V/1D05V



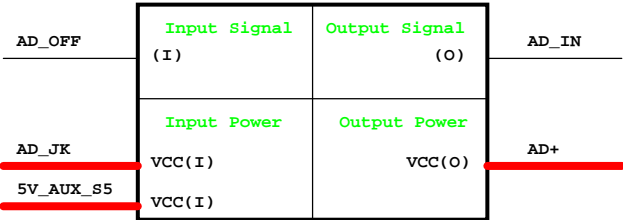
Charger Max8725

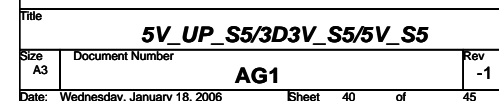
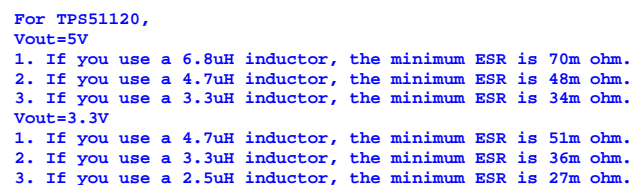


TPS51120
5V/3D3V

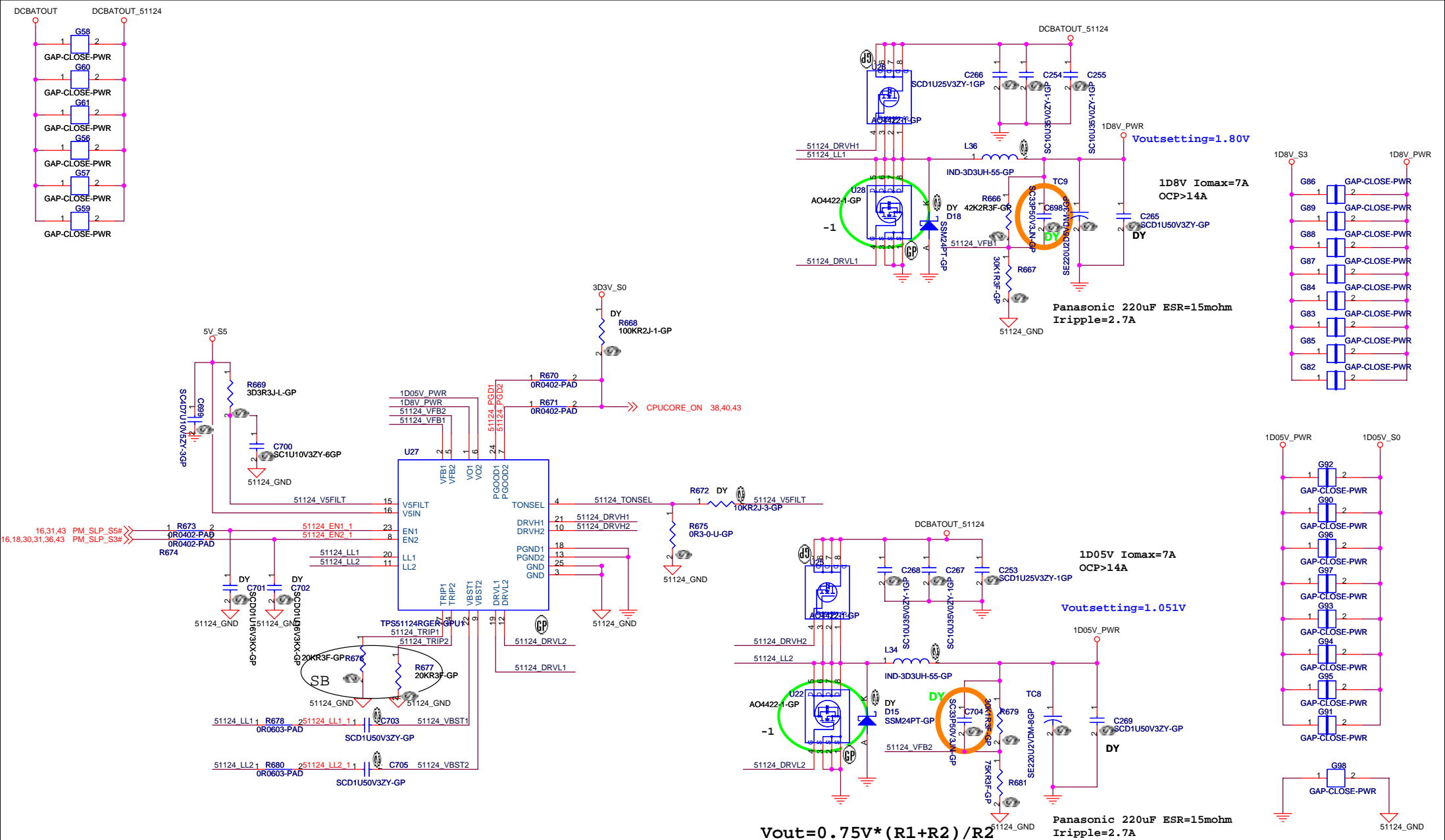


Adapter

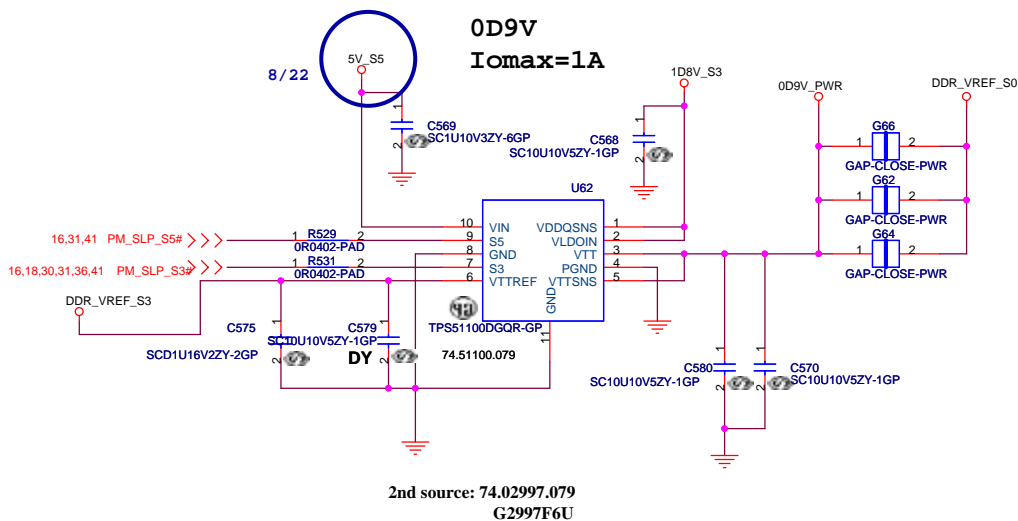
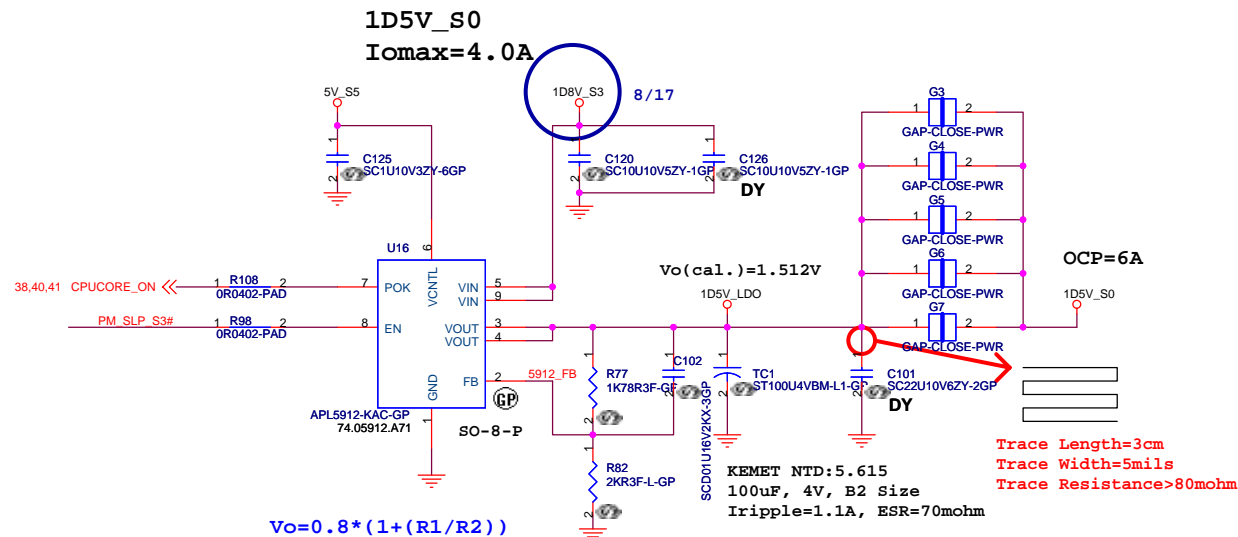
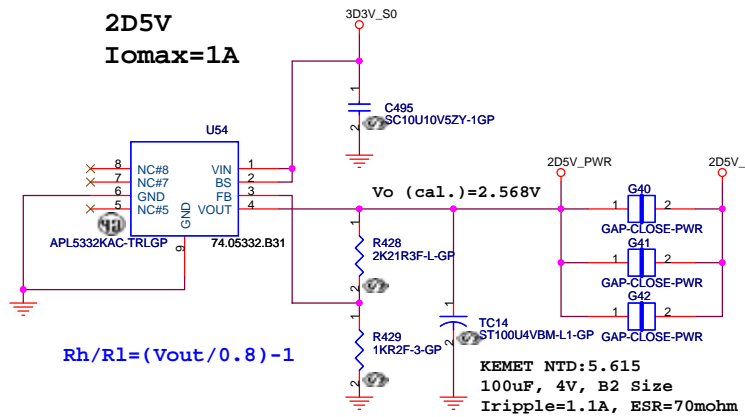




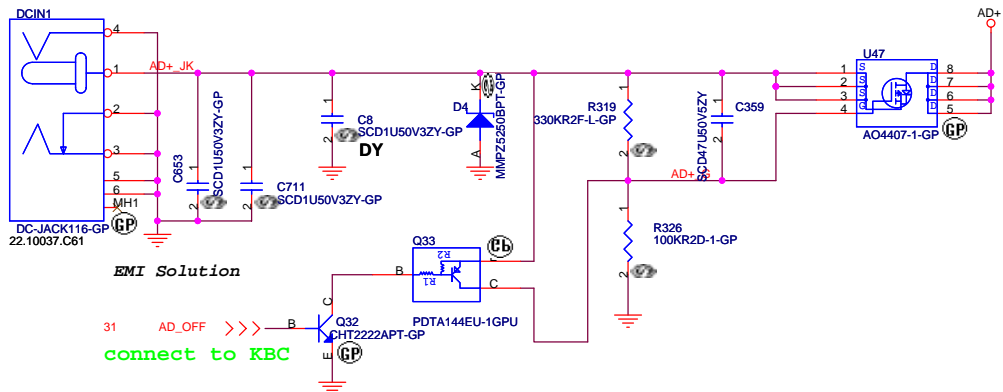
	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	not use	not use	SDO ON	SWEG3 on



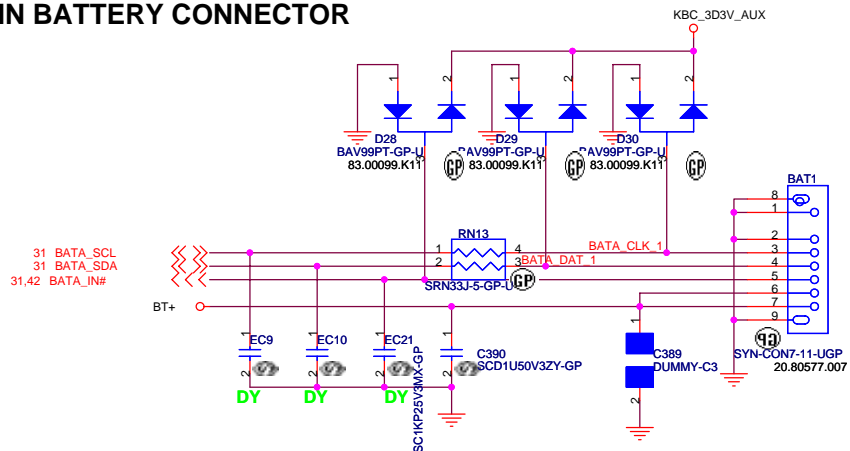




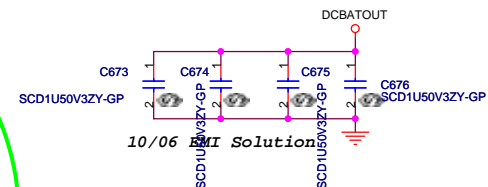
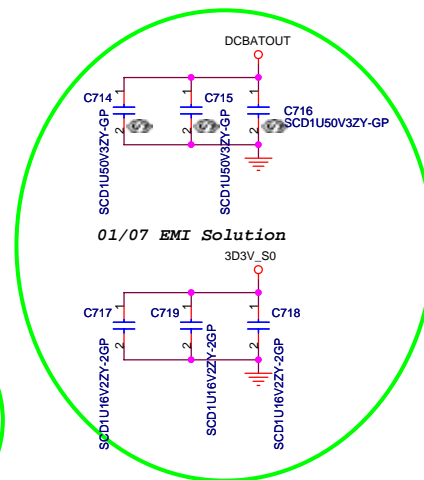
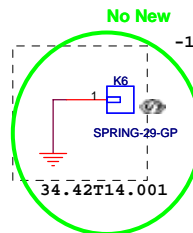
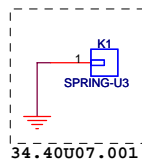
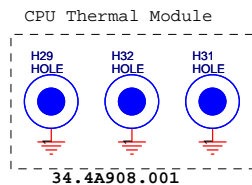
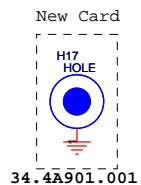
ADAPTER IN CIRCUIT



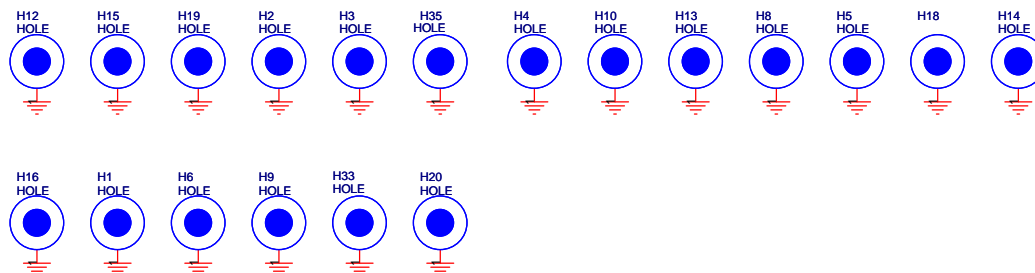
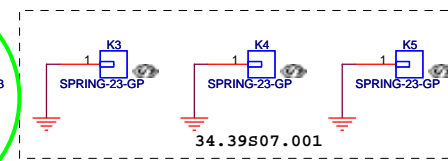
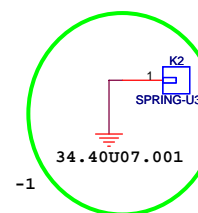
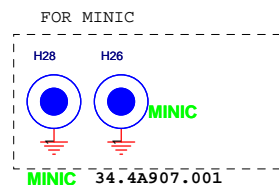
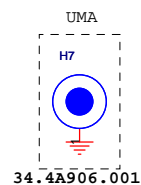
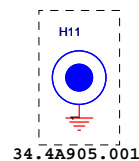
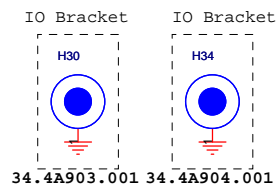
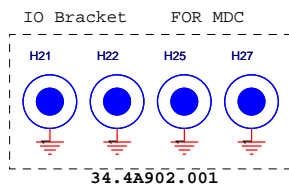
MAIN BATTERY CONNECTOR



TOP SIDE:



BOTTOM SIDE:



<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
SPRING & BOSS		
Size A3	Document Number AG1	Rev -1
Date: Tuesday, January 24, 2006		Sheet 45 of 45