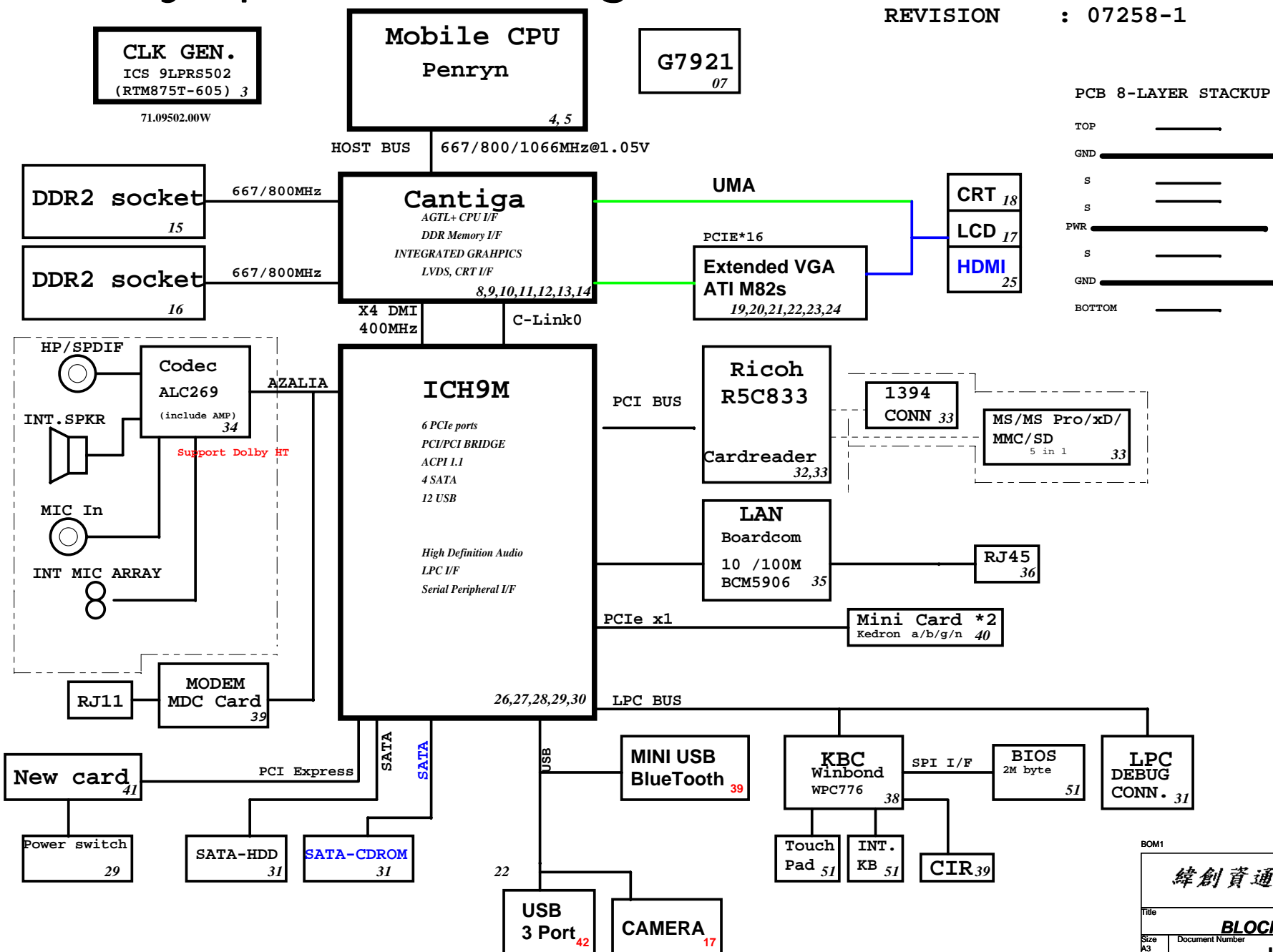


# Olympus Block Diagram

Project code: 91.4Y601.001  
PCB P/N : 48.4Y603.0SA  
REVISION : 07258-1



|  |  |    |
|--|--|----|
| <b>SYSTEM DC/DC</b><br><b>ISL6236</b>  |  | 38 |
| <b>INPUTS</b>                          | <b>OUTPUTS</b>                           |    |
| DCBATOUT                               | 5V_S5(5A)<br>3D3V_S5(5A)                 |    |
| <b>SYSTEM DC/DC</b><br><b>TPS51124</b> |  | 40 |
| <b>INPUTS</b>                          | <b>OUTPUTS</b>                           |    |
| DCBATOUT                               | 1D05V_M(11A)<br>1D5V_S3(10A)             |    |
| <b>TPS51117</b>                        |  | 39 |
| DCBATOUT                               | 1D8V_S3<br>(2.5A)                        |    |
| <b>TPS51100</b>                        |  | 39 |
| 1D8V_S3                                | DDR_VREF_S0<br>(1.5A)<br>DDR_VREF_S3     |    |
| <b>APL5308</b>                         |  | 39 |
| 3D3V_S0                                | 2D5V_S0<br>(300mA)                       |    |
| <b>CHARGER</b><br><b>BQ24750</b>       |  | 42 |
| <b>INPUTS</b>                          | <b>OUTPUTS</b>                           |    |
| DCBATOUT                               | CHG_PWR<br>18V 4.0A<br>UP+5V<br>5V 100mA |    |
| <b>CPU DC/DC</b><br><b>ISL6266A</b>    |  | 37 |
| <b>INPUTS</b>                          | <b>OUTPUTS</b>                           |    |
| DCBATOUT                               | VCC_CORE_S0<br>0~1.3V 47A                |    |
| <b>NB DC/DC</b><br><b>ISL6263A</b>     |  | 41 |
| <b>INPUTS</b>                          | <b>OUTPUTS</b>                           |    |
| DCBATOUT                               | GFX_CORE                                 |    |
| <b>SC411</b>                           |  | 48 |
| DCBATOUT                               | 1D5V_S3                                  |    |

BOM1

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|                             |                                 |                  |
|-----------------------------|---------------------------------|------------------|
| Title                       |                                 |                  |
| <b>BLOCK DIAGRAM</b>        |                                 |                  |
| Size<br>A3                  | Document Number<br><b>LT32M</b> | Rev<br><b>-1</b> |
| Date: Tuesday, May 13, 2008 | Sheet 1 of                      | 55               |

# ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

| Signal                        | Usage/When Sampled  | Comment   |
|-------------------------------|---|---|
| HDA_SDOUT                     | XOR Chain Entrance/<br>PCIE Port Config1 bit1,<br>Rising Edge of PWROK. | Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down.         |
| HDA_SYNC                      | PCIE config1 bit0,<br>Rising Edge of PWROK.                             | This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers: Offset 224h).  |
| GNT2#/GPIO53                  | PCIE config2 bit2,<br>Rising Edge of PWROK.                             | This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers: Offset 0224h).  |
| GPIO20                        | Reserved  | This signal should not be pulled high.  |
| GNT1#/GPIO51                  | ESI Strap (Server Only)<br>Rising Edge of PWROK                         | ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.  |
| GNT3#/GPIO55                  | Top-Block Swap Override,<br>Rising Edge of PWROK.                       | Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#/<br>SPI_CS1#/<br>GPIO58 | Boot BIOS Destination Selection 0:1,<br>Rising Edge of PWROK.           | Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h; bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.   |
| SPI_MOSI                      | Integrated TPM Enable,<br>Rising Edge of CLPWROK                        | Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.                                      |
| GPIO49                        | DMI Termination Voltage,<br>Rising Edge of PWROK.                       | The signal is required to be low for desktop applications and required to be high for mobile applications.  |
| SATALED#                      | PCI Express Lane Reversal, Rising Edge of PWROK.                        | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)   |
| SPKR                          | No Reboot.<br>Rising Edge of PWROK.                                     | If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.  |
| TP3                           | XOR Chain Entrance.<br>Rising Edge of PWROK.                            | This signal should not be pull low unless using XOR Chain testing.  |
| GPIO33/<br>HDA_DOCK_EN#       | Flash Descriptor Security Override Strap<br>Rising Edge of PWROK        | Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.  |

# ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

| SIGNAL                          | Resistor Type/Value  |
|---------------------------------|--|
| CL_CLK[1:0]                     | PULL-UP 20K  |
| CL_DATA[1:0]                    | PULL-UP 20K  |
| CL_RST0#                        | PULL-UP 20K  |
| DPRSLFVR/GPIO16                 | PULL-DOWN 20K  |
| ENERGY_DETECT                   | PULL-UP 20K  |
| HDA_BIT_CLK                     | PULL-DOWN 20K  |
| HDA_DOCK_EN#/GPIO33             | PULL-UP 20K  |
| HDA_RST#                        | PULL-DOWN 20K  |
| HDA_SDIN[3:0]                   | PULL-DOWN 20K  |
| HDA_SDOUT                       | PULL-DOWN 20K  |
| HDA_SYNC                        | PULL-DOWN 20K  |
| GLAN_DOCK#                      | The pull-up or pull-down active when configured for native LAN controller functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55,53,51]        | PULL-UP 20K  |
| GPIO[20]                        | PULL-DOWN 20K  |
| GPIO[49]                        | PULL-UP 20K  |
| LDA[3:0]#/FWH[3:0]#             | PULL-UP 20K  |
| LAN_RXD[2:0]                    | PULL-UP 20K  |
| LDRQ[1]/GPIO23                  | PULL-UP 20K  |
| PME#                            | PULL-UP 20K  |
| PWRBTN#                         | PULL-UP 20K  |
| SATALED#                        | PULL-UP 15K  |
| SPI_CS1#/<br>GPIO58/<br>CLGPIO6 | PULL-UP 20K  |
| SPI_MOSI                        | PULL-DOWN 20K  |
| SPI_MISO                        | PULL-UP 20K  |
| SPKR                            | PULL-DOWN 20K  |
| TACH[3:0]                       | PULL-UP 20K  |
| TP[3]                           | PULL-UP 20K  |
| USB[11:0][P,N]                  | PULL-DOWN 15K  |

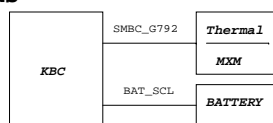
# Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5  
Page 218

| Pin Name                                     | Strap Description   | Configuration  |
|--|---|--|
| CFG[2:0]                                     | FSB Frequency Select                                      | 000 = FSB1067<br>011 = FSB867<br>010 = FSB800<br>others = Reserved   |
| CFG[4:3]<br>CFG8<br>CFG[15:14]<br>CFG[18:17] | Reserved  |  |
| CFG5   | DMI x2 Select   | 0 = DMI x2<br>1 = DMI x4 (Default)   |
| CFG6   | iTPM Host Interface                                       | 0 = The iTPM Host Interface is enabled (Note 2)<br>1 = The iTPM Host Interface is disabled (default)   |
| CFG7   | Intel Management engine Crypto strap                      | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality<br>1 = TLS cipher suite with confidentiality (default)   |
| CFG9   | PCIE Graphics Lane  | 0 = Reverse Lanes, 15->0, 14->1 ect..<br>1 = Normal operation (Default): Lane Numbered in order  |
| CFG10  | PCIE Loopback enable                                      | 0 = Enable (Note 3)<br>1 = Disabled (default)  |
| CFG[13:12]                                   | XOR/ALL   | 00 = Reserve<br>10 = XOR mode Enabled<br>01 = ALL mode Enabled (Note 3)<br>11 = Disabled (default)   |
| CFG16  | FSB Dynamic ODT   | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)  |
| CFG19  | DMI Lane Reversal   | 0 = Normal operation (Default): Lane Numbered in Order<br>1 = Reverse Lanes<br>DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3)<br>DMI x2 mode [MCH -> ICH]: (3->0, 2->1) |
| CFG20  | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE | 0 = Only Digital Display Port or PCIE is operational (Default)<br>1 = Digital display Port and PCIE are operating simultaneously via the PEG port                              |
| SDVO_CTRLDATA                                | SDVO Present  | 0 = No SDVO Card Present (Default)<br>1 = SDVO Card Present  |
| L_DDC_DATA                                   | Local Flat Panel (LFP) Present                            | 0 = LFP Disabled (Default)<br>1 = LFP Card Present; PCIE disabled  |

NOTE:  
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

## SMBus



## USB Table

| Pair | Device            |
|------|-------------------|
| 0    | Combo (ESATA/USB) |
| 1    | NC                |
| 2    | USB2              |
| 3    | USB4              |
| 4    | USB3              |
| 5    | BLUETOOTH         |
| 6    | WEBCAM            |
| 7    | FT                |
| 8    | MINICARD          |
| 9    | NEW1              |

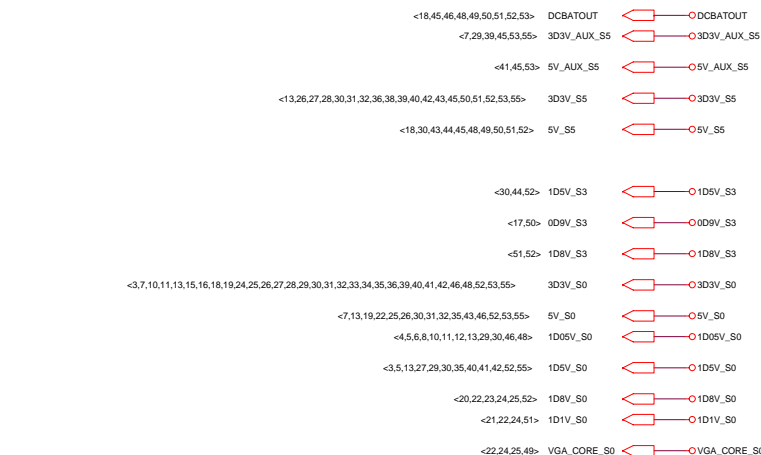
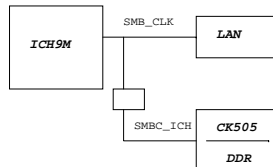
## PCI Routing

page 17

| IDSEL  | INT  | REQ   | GNT |
|--------|------|---|-----|
| TI7412 | AD22 | G: CARDBUS<br>B: 1394<br>F: Flash Media<br>S: SD Host | 0 0 |

## PCIE Routing

|       |               |
|-------|---------------|
| LANE2 | MiniCard WLAN |
| LANE3 | NewCard WLAN  |

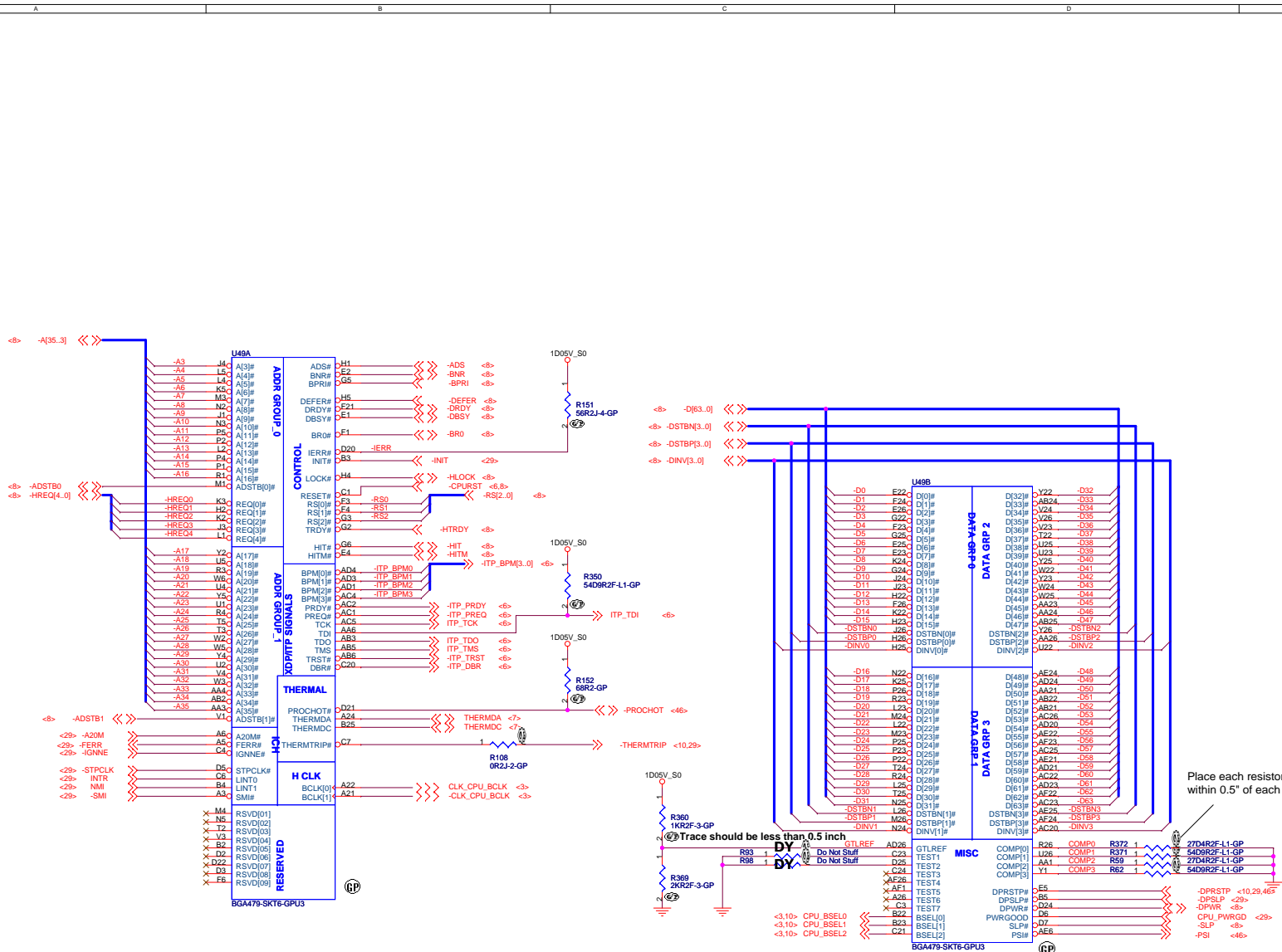


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| Reference                   |                 |       |
|-----------------------------|-----------------|-------|
| Size C                      | Document Number | Rev   |
|                             | LT32M           | -1    |
| Date: Tuesday, May 13, 2008 | Sheet 2         | of 54 |





Place each resistor within 0.5" of each pin

Trace should be less than 0.5 inch

Do Not Suf

Do Not Suf

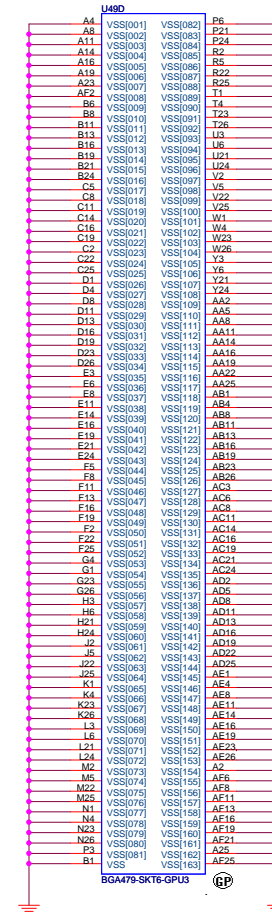
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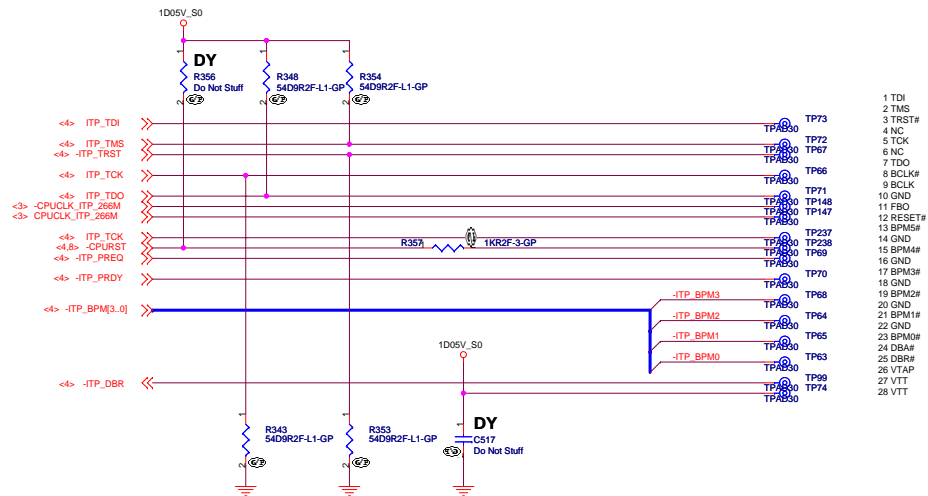
Do Not Suf

Do Not Suf

Do Not Suf

Do Not Suf



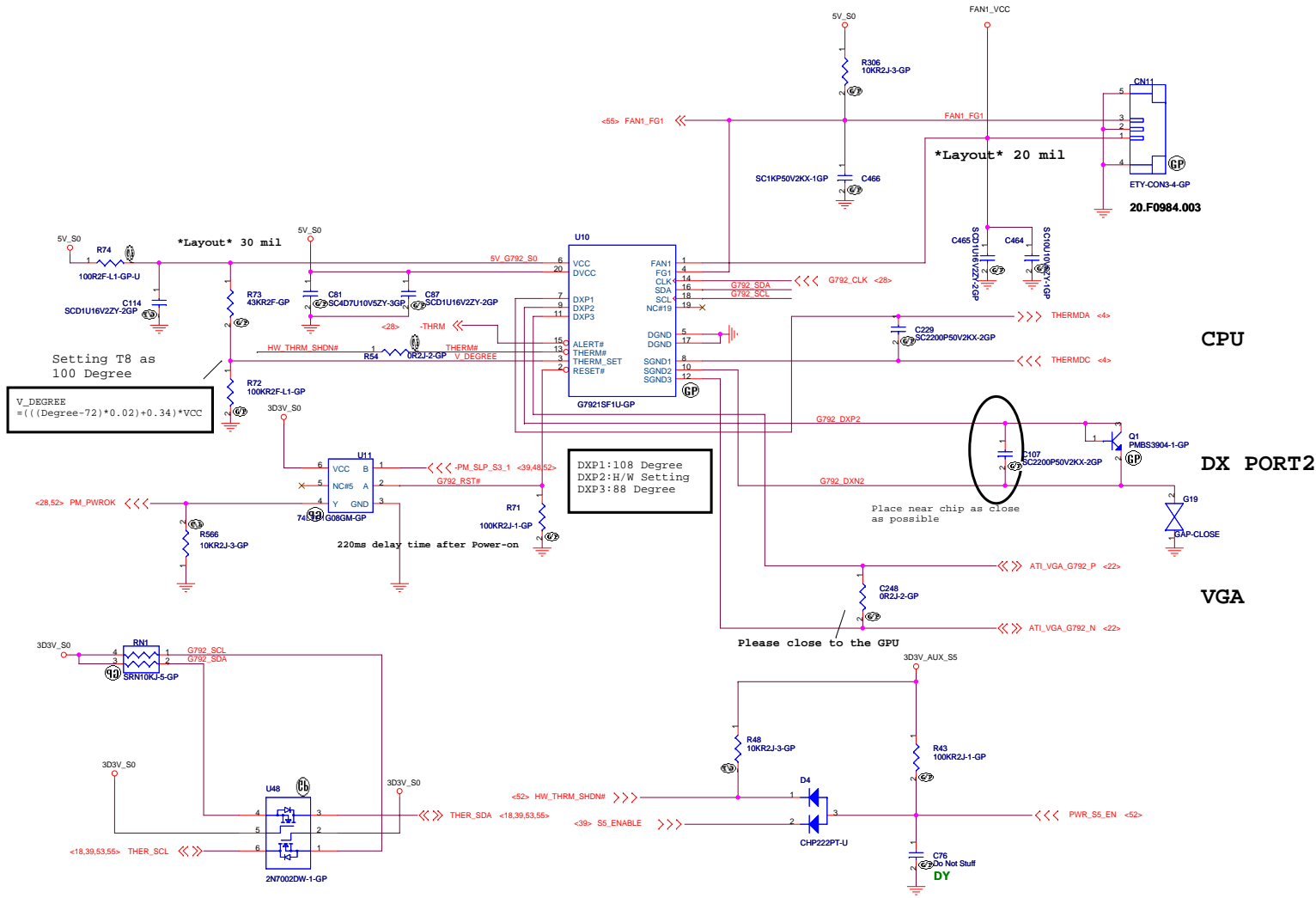


- 1 TDI
- 2 TMS
- 3 TRST#
- 4 NC
- 5 TCK
- 6 NC
- 7 TDO
- 8 BCLK#
- 9 BCLK
- 10 GND
- 11 FBO
- 12 RESET#
- 13 BPM5#
- 14 GND
- 15 BPM4#
- 16 GND
- 17 BPM3#
- 18 GND
- 19 BPM2#
- 20 GND
- 21 BPM1#
- 22 GND
- 23 BPM0#
- 24 DBA#
- 25 DBR#
- 26 VTAP
- 27 VTT
- 28 VTT

(\*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

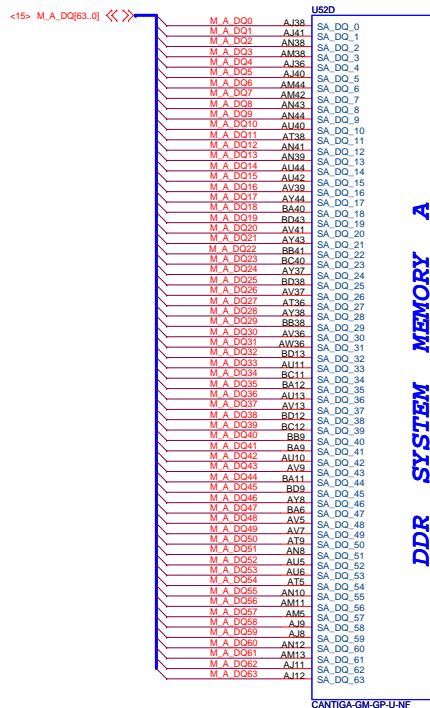
(\*2) CPURST# SIGNAL IS BRANCHED AT GMCH's PIN

| Ref Des | For ITP-XDP        |
|---------|--------------------|
| J1      | NO_ASM-->ASM       |
| C157    | NO_ASM-->ASM       |
| R140    | NO_ASM-->1K 5% ASM |
| R144    | ASM (No Change)    |
| R136    | ASM-->NO_ASM       |
| R145    | ASM (No Change)    |
| R141    | ASM-->54.9 1% ASM  |
| R143    | ASM-->54.9 1% ASM  |

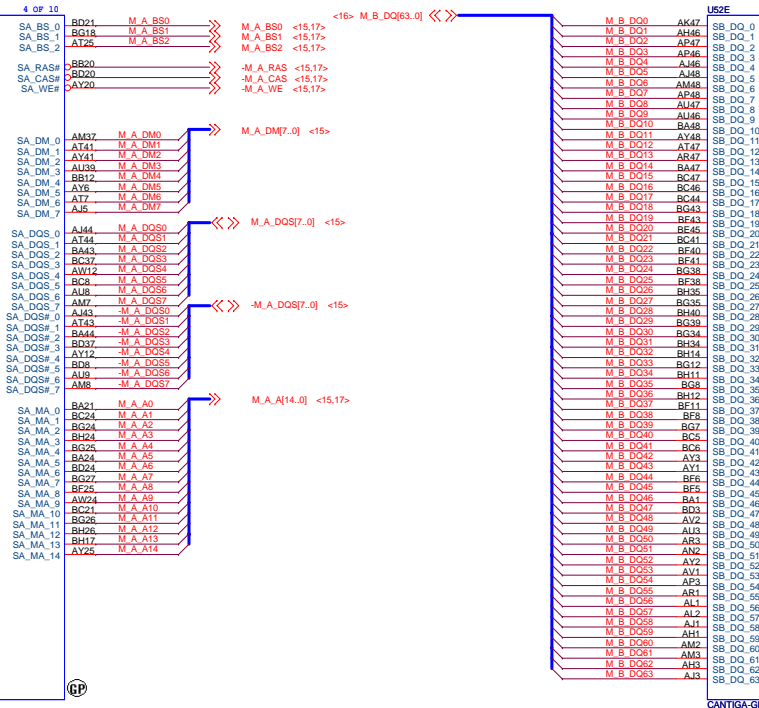








DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

BOH1

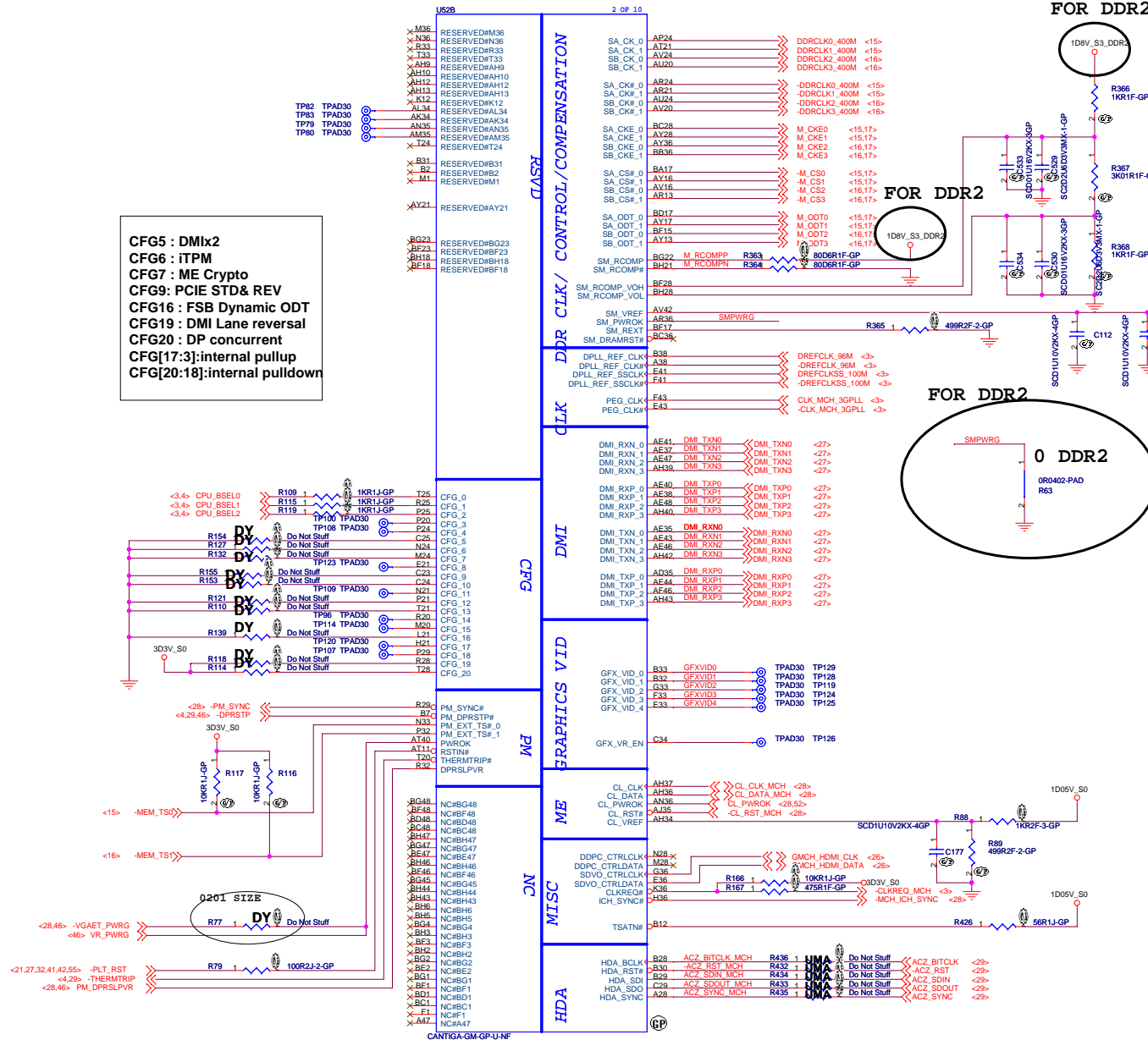
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File Cantiga(2/7):DDR3  
Size C Document Number LT32M Rev -1  
Date Tuesday, May 13, 2008 Sheet 9 of 54

ME DEBUG PORT PIN OUT TABLE

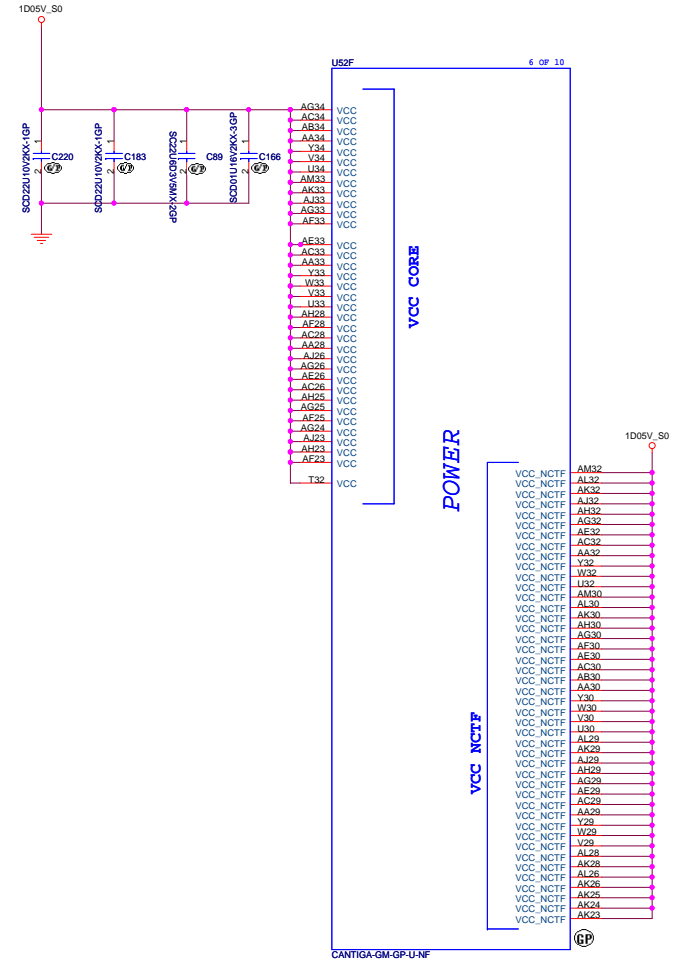
|               |             |
|---------------|-------------|
| RESERVED#AL34 | ME_JTAG_TCK |
| RESERVED#AK34 | ME_JTAG_TDI |
| RESERVED#AN35 | ME_JTAG_TDO |
| RESERVED#AM35 | ME_JTAG_TMS |

CFG5 : DMIX2  
 CFG6 : ITPM  
 CFG7 : ME Crypto  
 CFG9 : PCIE STD& REV  
 CFG16 : FSB Dynamic ODT  
 CFG19 : DMI Lane reversal  
 CFG20 : DP concurrent  
 CFG[17:3]:internal pullup  
 CFG[20:18]:internal pulldown





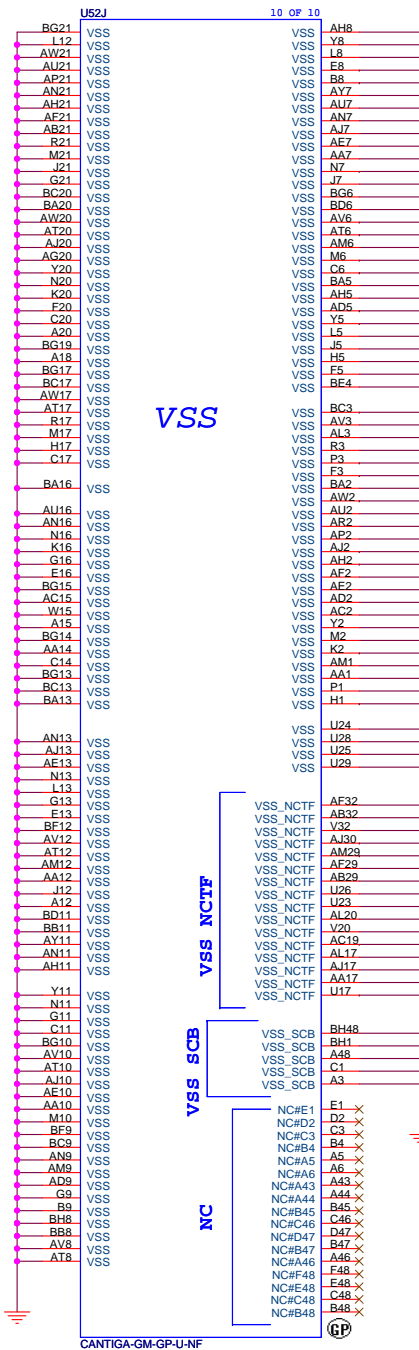
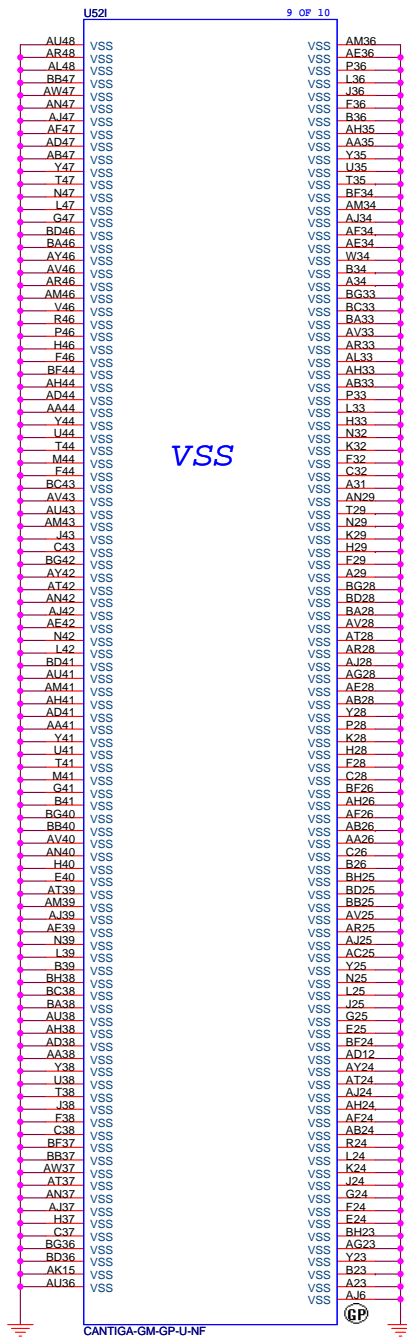
1D8V\_S3\_DDR2



|                                |                     |             |     |
|--------------------------------|---------------------|-------------|-----|
| Title                          |                     |             |     |
| <b><i>Cantiga(5/7):VCC</i></b> |                     |             |     |
| Size                           | Document Number     |             | Rev |
| C                              | LT32M               |             | -1  |
| Date                           | Tuesday May 13 2008 | Sheet 12 of | 54  |

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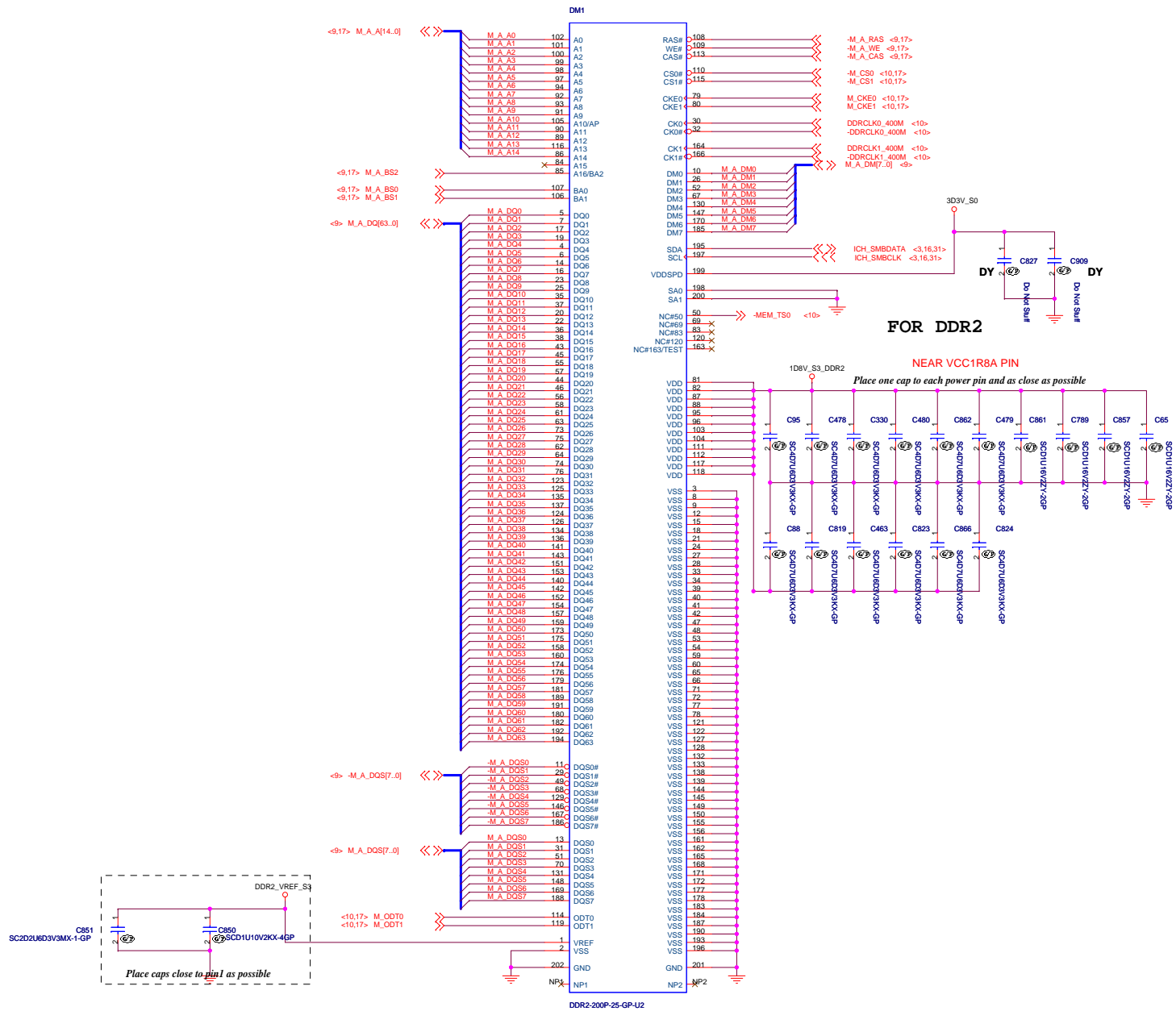




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| Title            |                       |                |
| Cantiga(8/7):GND |                       |                |
| Size             | Document Number       | Rev            |
| A3               | LT32M                 | -1             |
| Date:            | Tuesday, May 13, 2008 | Sheet 14 of 54 |



Place near VCC3B Power rail bridge via under SO-DIMM

FOR DDR2

NEAR VCC1R8A PIN  
Place one cap to each power pin and as close as possible

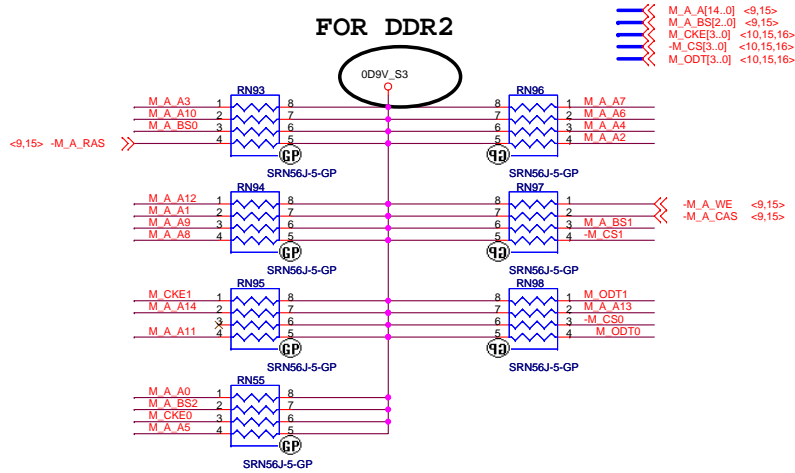






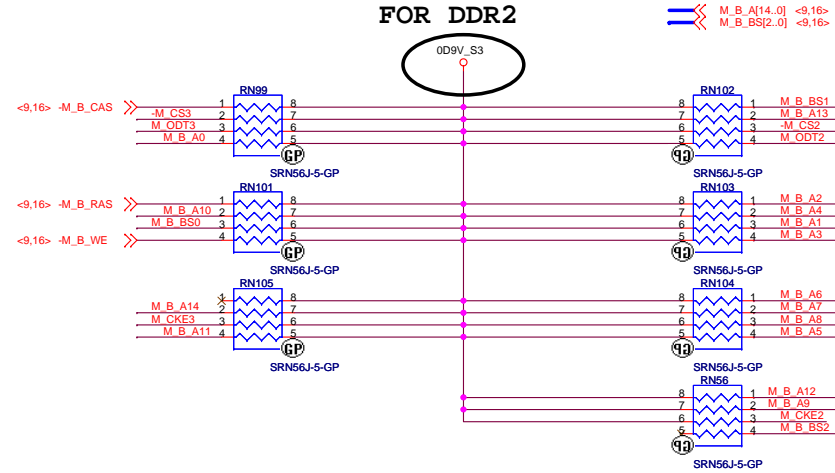
## CHANNEL A PARALLEL TERMINATION

FOR DDR2



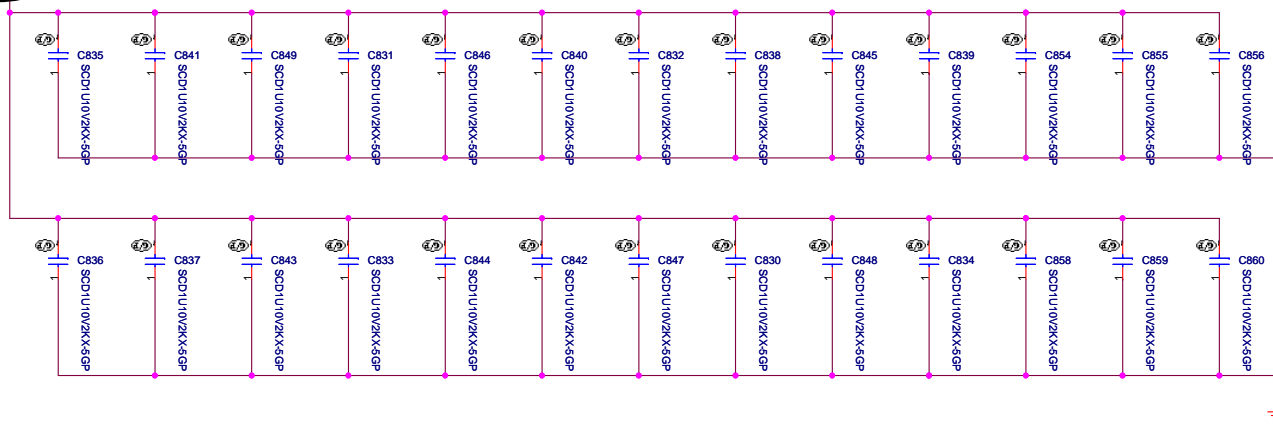
## CHANNEL B PARALLEL TERMINATION

FOR DDR2



FOR DDR2

PLACE 1 CAP FOR EVERY 2 BITS TERMINATION TO VCC0R9A.



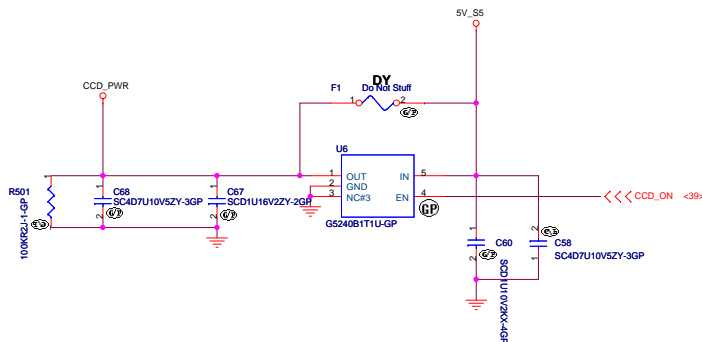
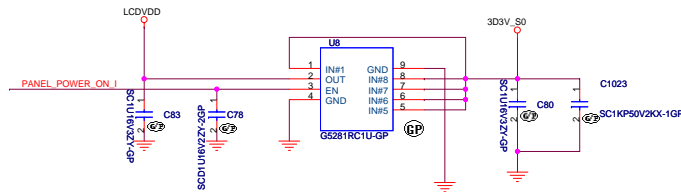
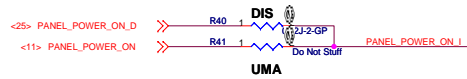
BOM1

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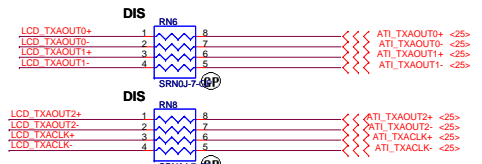
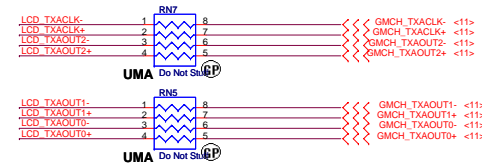
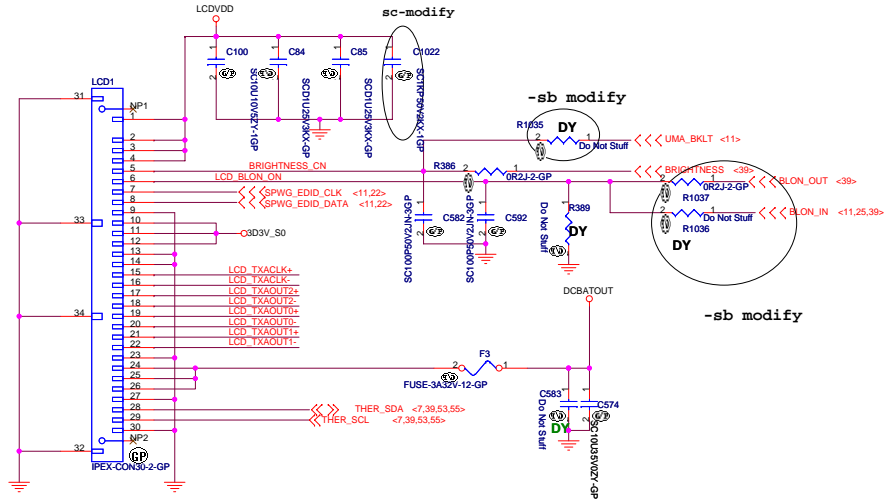
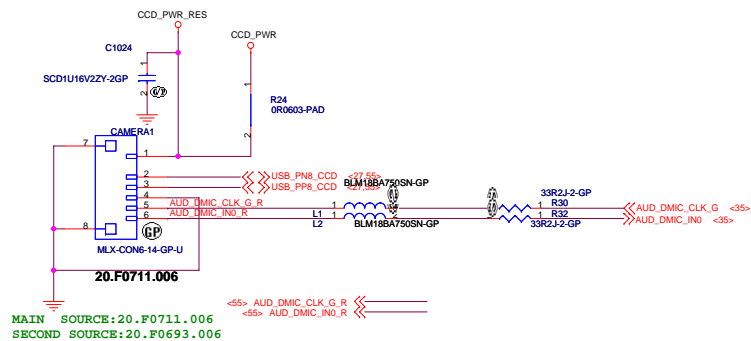
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|        |                                     |       |          |
|--------|-------------------------------------|-------|----------|
| Title  | <b>DDR-2 TERMINATION/DECOUPLING</b> |       |          |
| Size   | Document Number                     | Rev   | -1       |
| Custom | <b>LT32M</b>                        |       |          |
| Date:  | Tuesday, May 13, 2008               | Sheet | 17 of 54 |

# LCD/INVERTER CONN

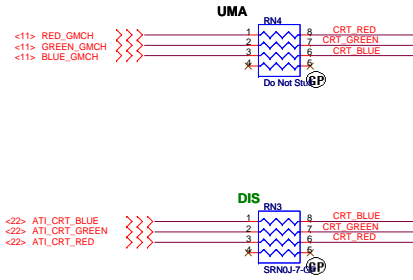


## CAMERA & DIG-MIC



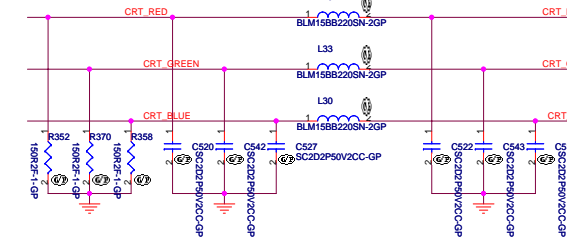
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| BOM1  |                       | Wistron Corporation         |        |
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| Size  | Document Number       | LT32M                       | Rev -1 |
| Date  | Tuesday, May 13, 2008 | Sheet 18                    | of 54  |

# CRT I/F & CONNECTOR

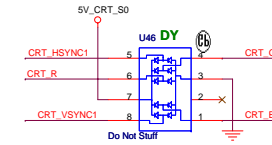
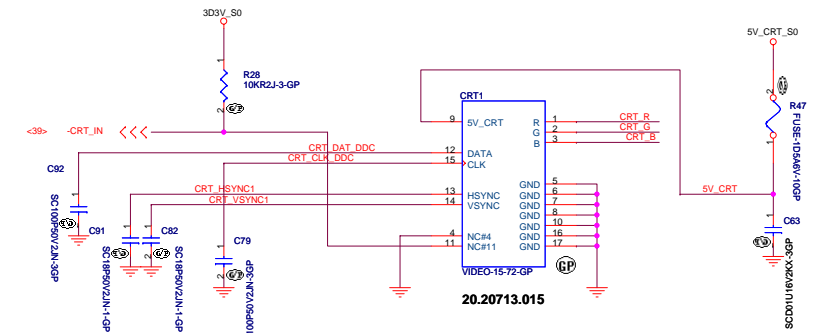


Layout Note:  
Place these resistors  
close to the CRT-out  
connector

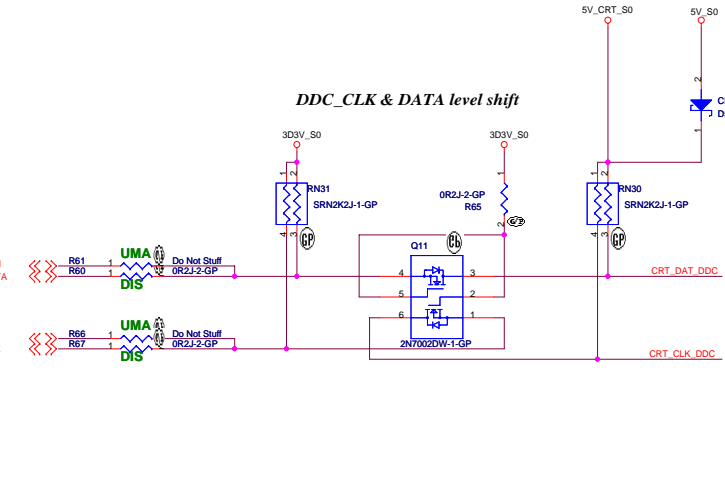
Ferrite bead impedance: 10 ohm@100MHz



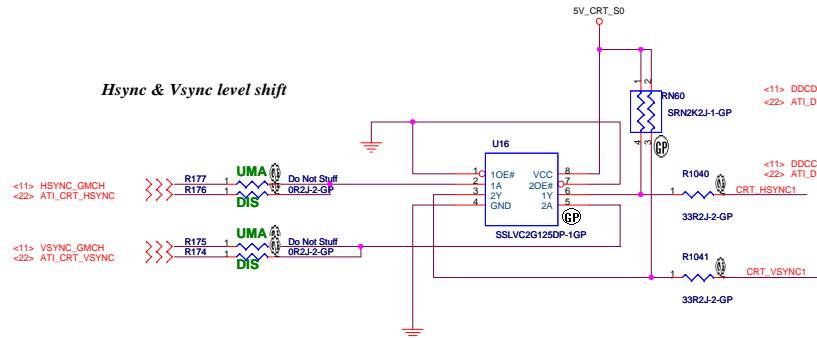
Layout Note:  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



## DDC\_CLK & DATA level shift



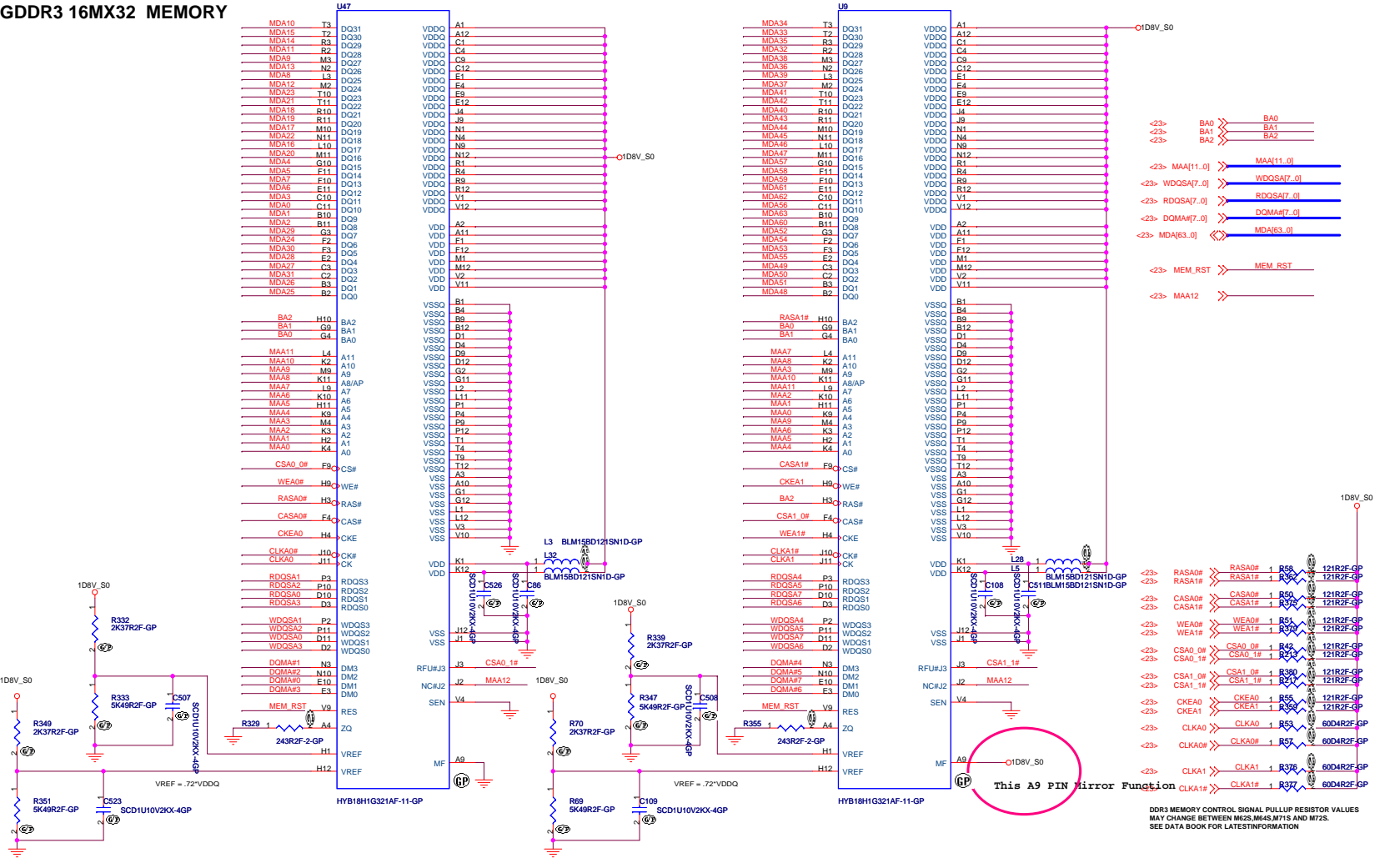
## Hsync & Vsync level shift



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|      |                       |          |        |
|------|-----------------------|----------|--------|
| File | CRT/TV Connector      |          |        |
| Size | Document Number       | LT32M    | Rev -1 |
| Date | Tuesday, May 13, 2008 | Sheet 10 | of 54  |

GDDR3 16MX32 MEMORY



DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES  
MAY CHANGE BETWEEN M82S, M71S AND M72S.  
SEE DATA BOOK FOR LATEST INFORMATION

|  |                 |       |
|--|-----------------|-------|
| BOM1   |                 |       |
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| Title: ATI M82-S VRAM(1,2)   |                 |       |
| Size C   | Document Number | Rev   |
|  | LT32M           | -1    |
| Date: Tuesday, May 13, 2008  | Sheet 20        | of 54 |





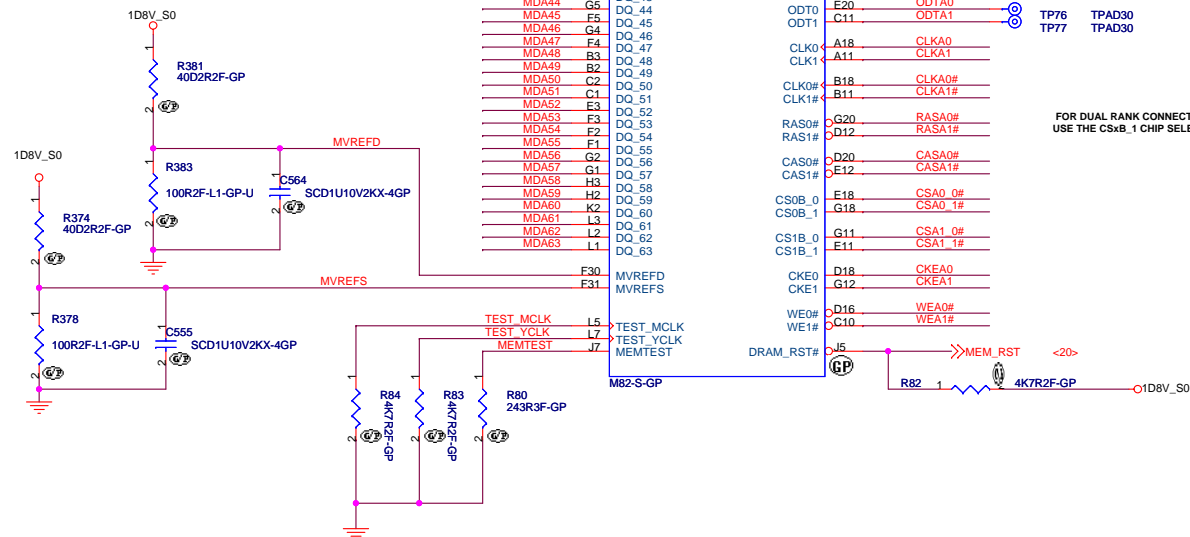
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 <20> RASA1# <<< RASA1#  
 <20> CASA0# <<< CASA0#  
 <20> CASA1# <<< CASA1#  
 <20> WEA0# <<< WEA0#  
 <20> WEA1# <<< WEA1#  
 <20> CKEA0 <<< CKEA0  
 <20> CKEA1 <<< CKEA1  
 <20> CSA0\_0# <<< CSA0\_0#  
 <20> CSA1\_0# <<< CSA1\_0#  
 <20> CSA0\_1# <<< CSA0\_1#  
 <20> CSA1\_1# <<< CSA1\_1#

<20> CLKA0 <<< CLKA0  
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 <20> CLKA1 <<< CLKA1  
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 <20> WQSA[7..0] <<< WQSA[7..0]  
 <20> RDQSA[7..0] <<< RDQSA[7..0]  
 <20> DQMA#[7..0] <<< DQMA#[7..0]  
 <20> MDA[63..0] <<< MDA[63..0]  
 <20> MAA[11..0] <<< MAA[11..0]

<20> BA0 <<< BA0  
 <20> BA1 <<< BA1  
 <20> BA2 <<< BA2  
 <20> MAA12 <<< MAA12

PLACE MVREF DIVIDERS  
AND CAPS CLOSE TO ASIC

| DIVIDER RESISTORS | DDR2 | DDR3  |
|-------------------|------|-------|
| MVREF TO 1.8V     | 100R | 40.2R |
| MVREF TO GND      | 100R | 100R  |



FOR DUAL RANK CONNECTIONS  
USE THE CSx8\_1 CHIP SELECT PINS

BOM1

**緯創資通** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title **ATI M82-S(3/6):Memory Interface**

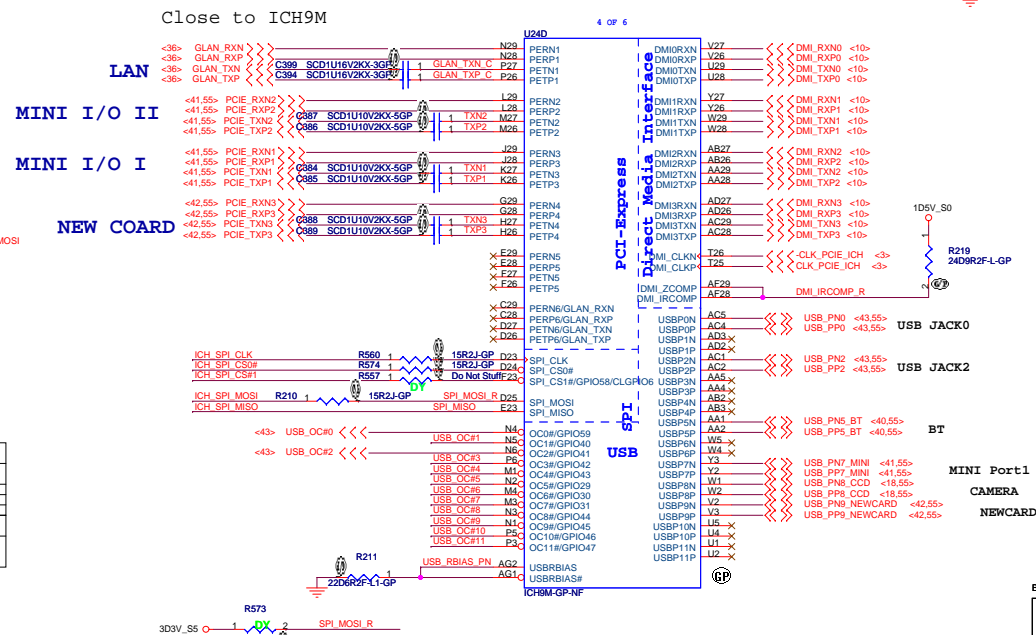
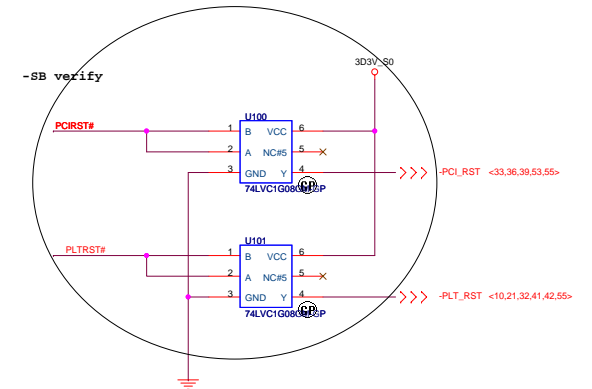
Size A3 Document Number **LT32M** Rev **-1**  
 Date: Tuesday, May 13, 2008 Sheet 23 of 54







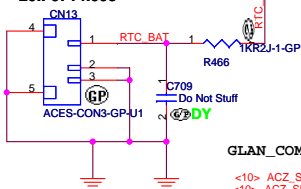






MAIN SOURCE:20.F0411.003  
SECOND SOURCE:20.D0246.103

20.F0714.003



GLAN\_COMP place within 500 mils of ICH9M

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<10> ACZ\_SDOOUT  
<10> ACZ\_SYNC  
<10> ACZ\_RST  
<10> ACZ\_BITCLK

Do Not Stuff  
Do Not Stuff

<40,55> ACZ\_BITCLK\_MDC  
<35> ACZ\_BITCLK\_RTL  
<35> ACZ\_SYNC\_RTL  
<40,55> ACZ\_SYNC\_MDC  
<40,55> ACZ\_RST\_MDC  
<35> ACZ\_RST\_RTL

<35> ACZ\_SDATIN\_RTL  
<40,55> ACZ\_SDATIN\_MDC

<40,55> ACZ\_SDATOUT\_MDC  
<35> ACZ\_SDATOUT\_RTL

3D3V\_S0

TP265

R475

Do Not Stuff

HDA\_DOCK\_EN#

HDA\_DOCK\_RST#

AG7

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AG10

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AG269

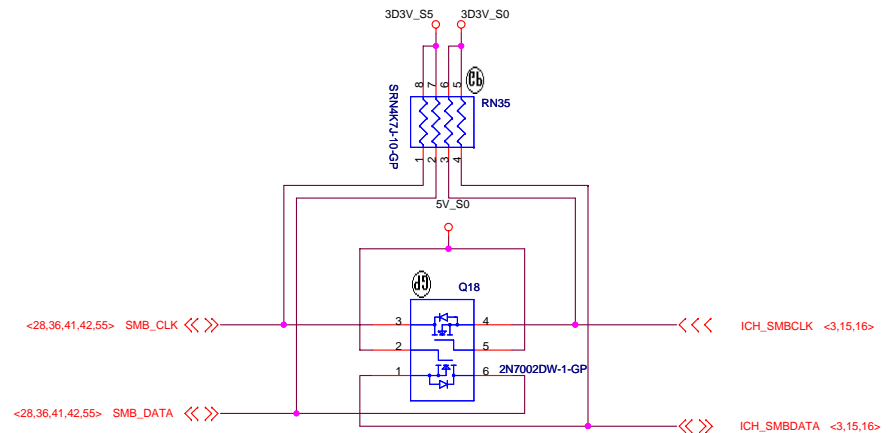
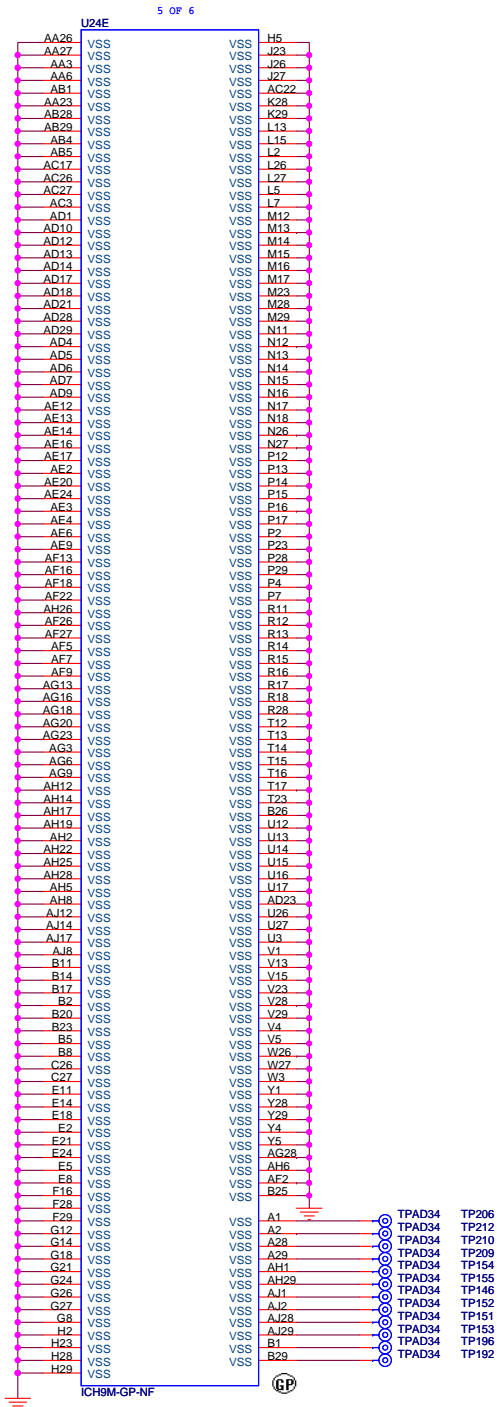
AG270

AG271

AG272

AG273





Q13 & Q14 connect SMLINK and  
SMBUS in S) for SMBus 2.0  
compliance

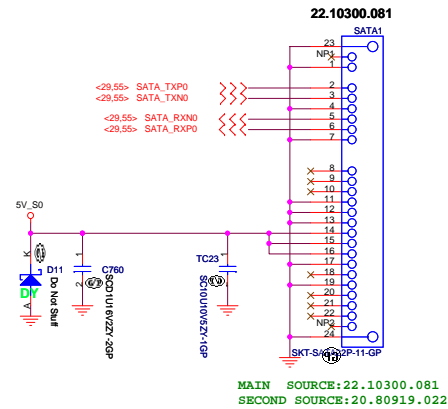
SMBUS

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Taipei Hsien 221, Taiwan, R.O.C.

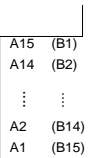
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|-----------------------------|-----------------|-----|-------|
| Title                       | ICH9-M (4 of 4) |     |       |
| Size                        | Document Number | Rev | -1    |
| LT32M                       |                 |     |       |
| Date: Tuesday, May 13, 2008 | Sheet           | 31  | of 54 |

# SATA HD Connector

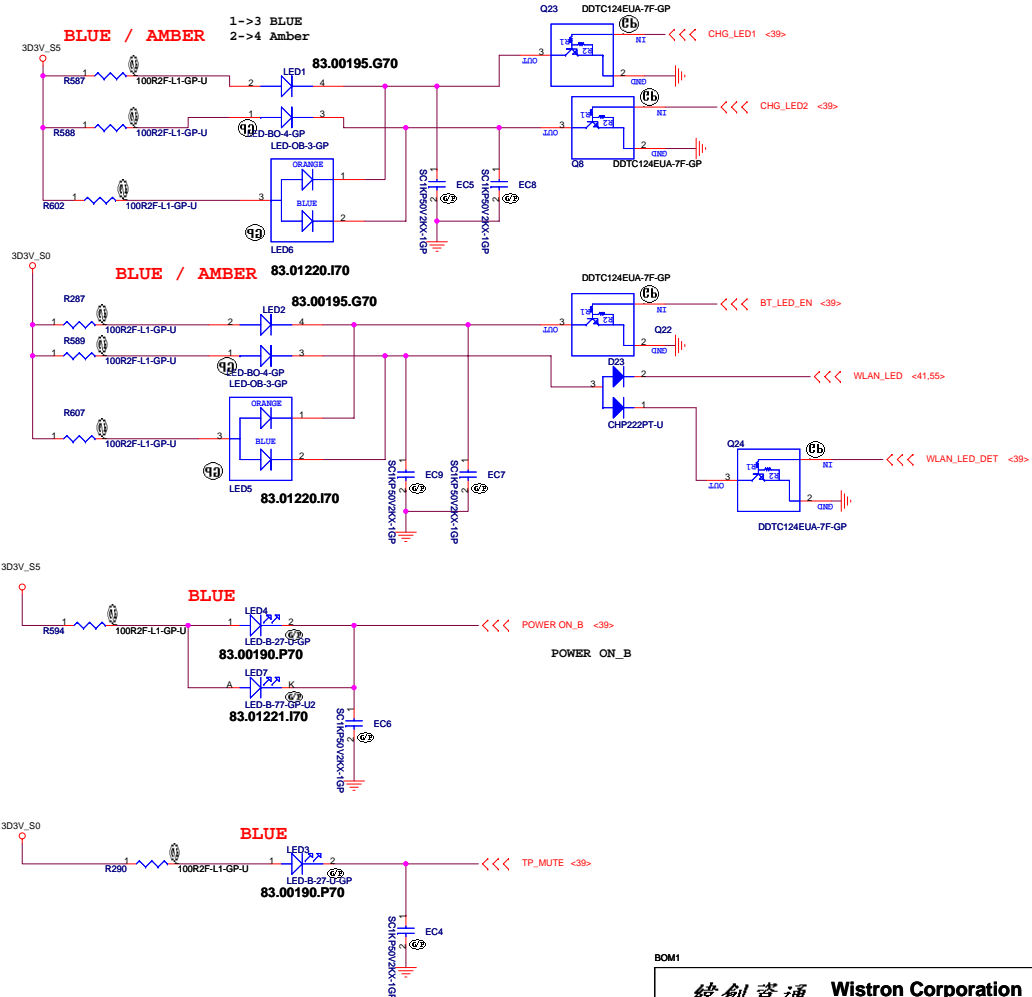
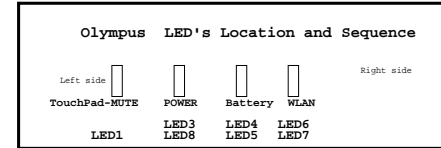
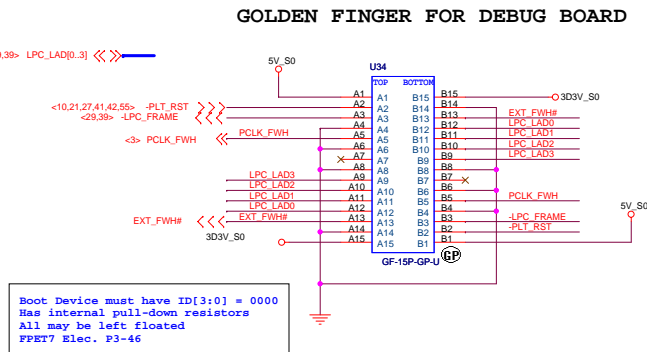
# ODD Connector



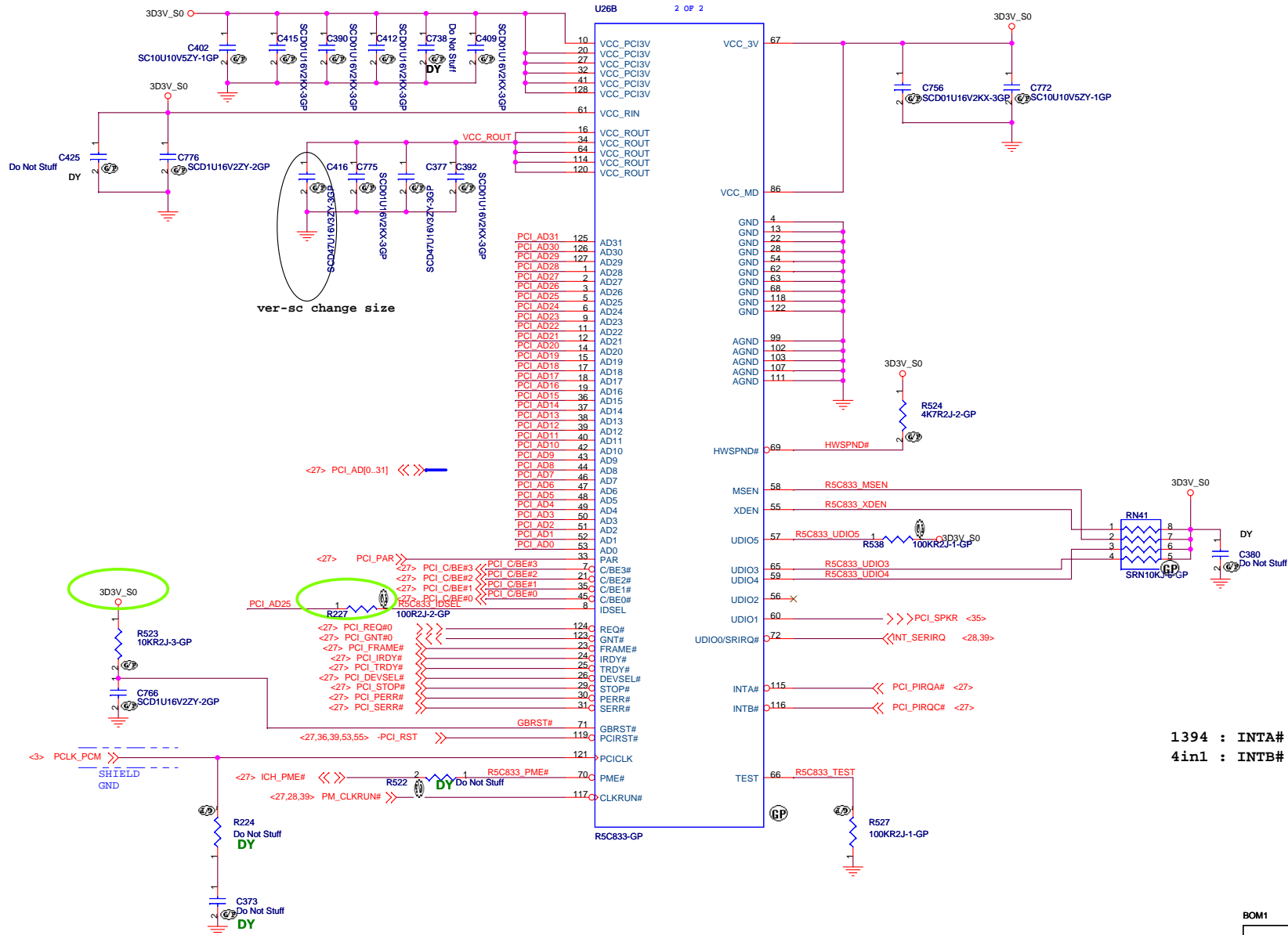
## TOP VIEW



## (BOTTOM VIEW)





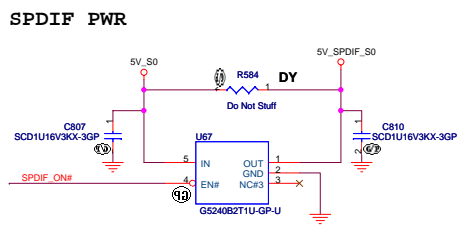
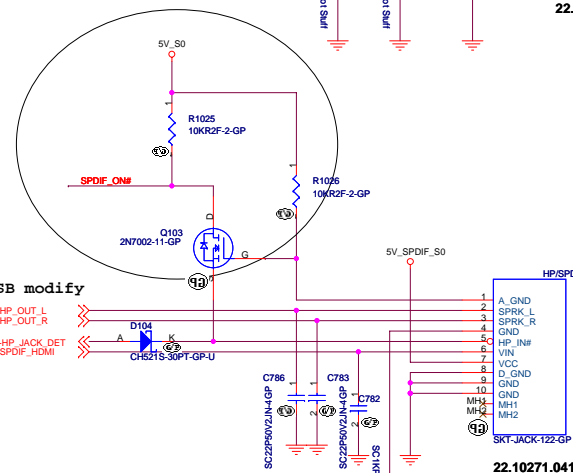
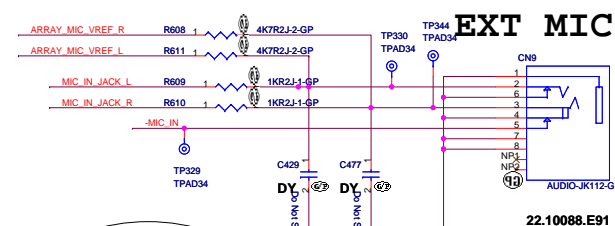
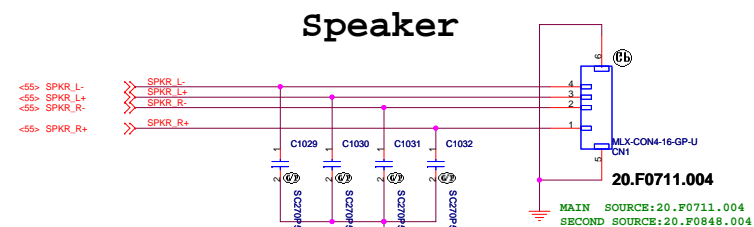


BOM1

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|            |                       |                |
|------------|-----------------------|----------------|
| Title      |                       |                |
| R5C832/PCI |                       |                |
| Size       | Document Number       | Rev            |
| A3         | LT32M                 | -1             |
| Date:      | Tuesday, May 13, 2008 | Sheet 33 of 54 |

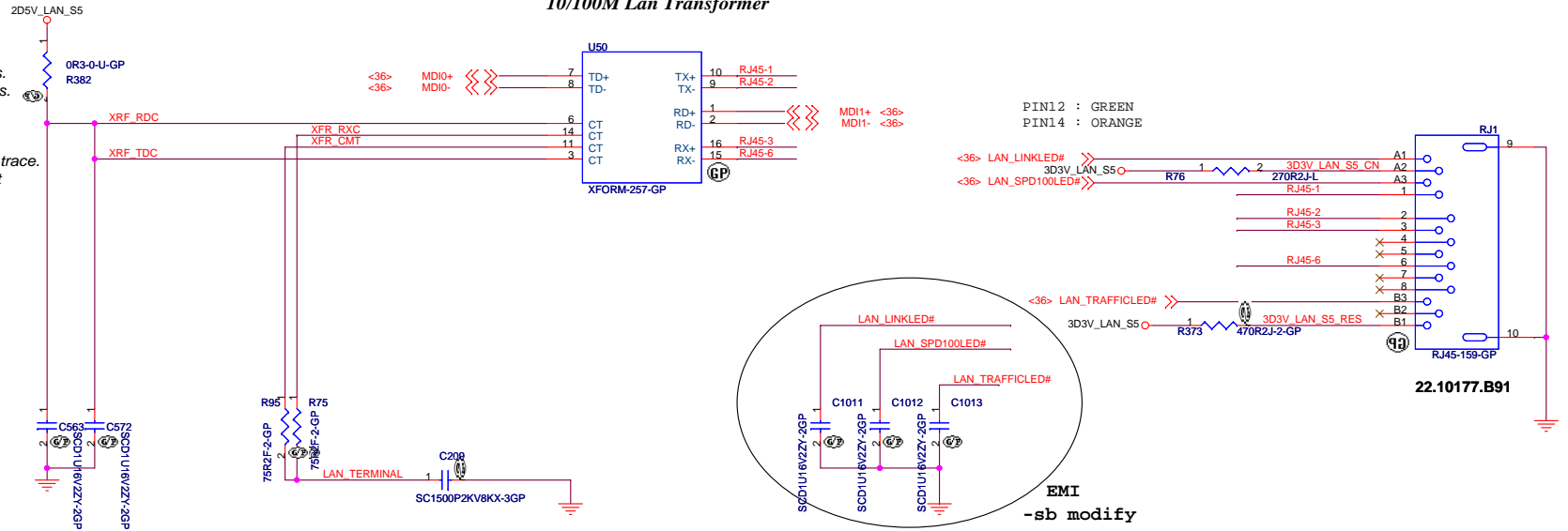






# 10/100M Lan Transformer

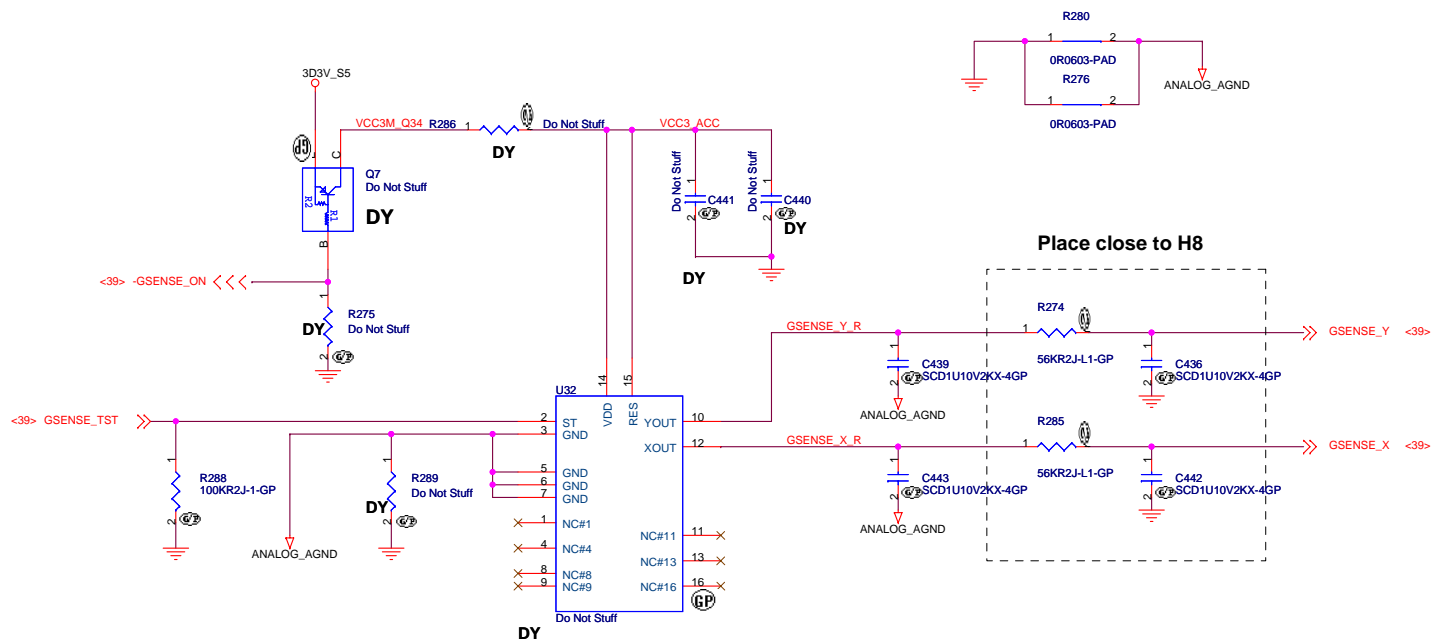
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

| Title                       |                 |                |  |
|-----------------------------|-----------------|----------------|--|
| LAN connector/NEW CARD/SIM  |                 |                |  |
| Size                        | Document Number | Rev            |  |
| A3                          | LT32M           | -1             |  |
| Date: Tuesday, May 13, 2008 |                 | Sheet 37 of 54 |  |



Primary : STMicro LIS244AL  
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil  
for three Output traces

|           |                     |          |
|-----------|---------------------|----------|
|           | ADXL322<br>LIS244AL | No Accel |
| R545      | NO_ASM              | ASM      |
| R547      | ASM                 | ASM      |
| All other | ASM                 | NO_ASM   |

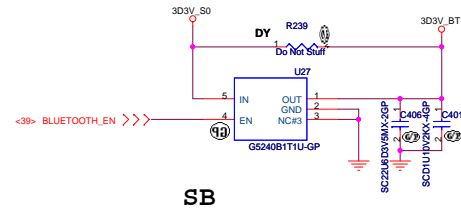
#### Layout Comment :

- (1) Place C439, C443, Q7, R286, R275, C441, C440, R288, R289 close to U32.
- (2) Avoid routing under DCDC switching area.

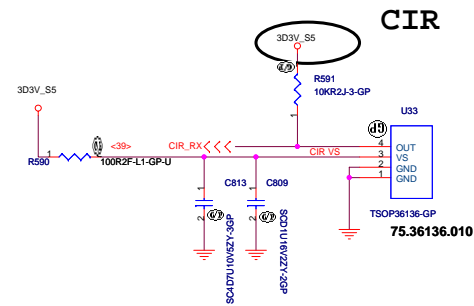
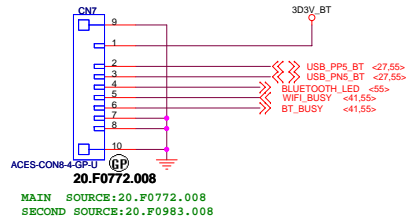
BOM1

|   |                                 |                  |
|---|---------------------------------|------------------|
| <b>緯創資通</b> <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                                 |                  |
| Title <b>G-SENSOR</b>   |                                 |                  |
| Size<br>A3  | Document Number<br><b>LT32M</b> | Rev<br><b>-1</b> |
| Date: Tuesday, May 13, 2008   | Sheet 38 of 54                  |                  |

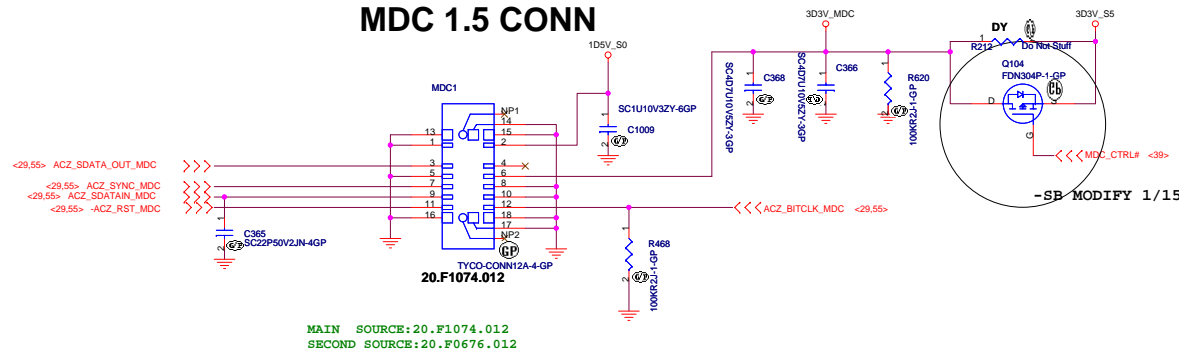




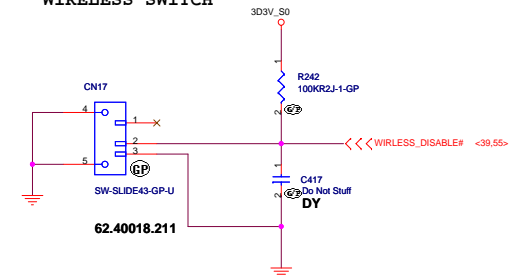
## BT CONNECTOR



## MDC 1.5 CONN



## WIRELESS SWITCH



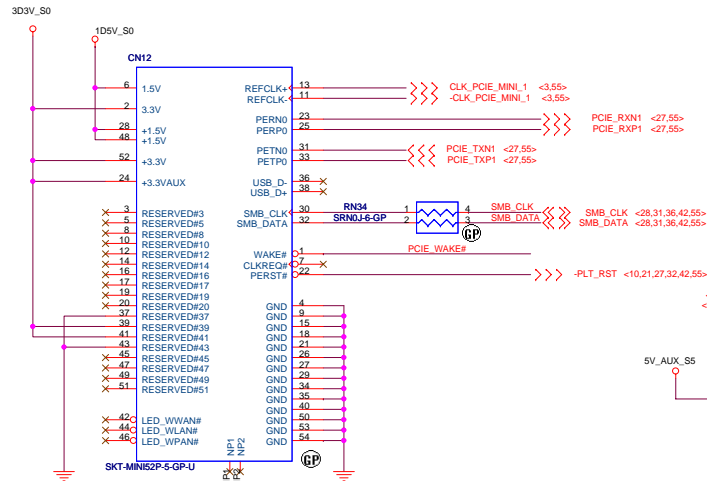


# Mini PCI-E Connector

Only port-1 support USB

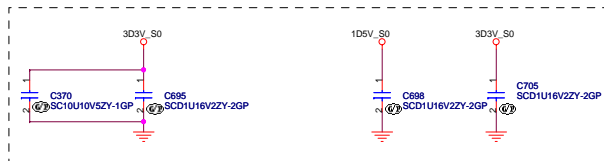
For Robson

## Port-1 High



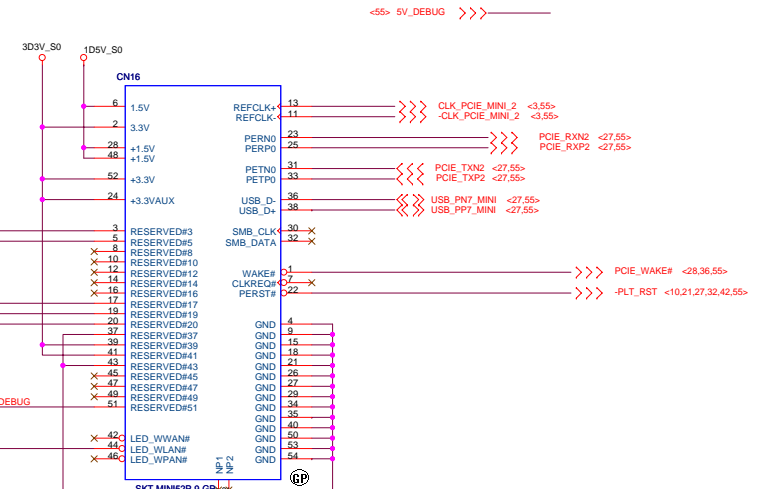
20.F0832.052

MAIN SOURCE: 20.F0832.052  
SECOND SOURCE: 20.F1107.052



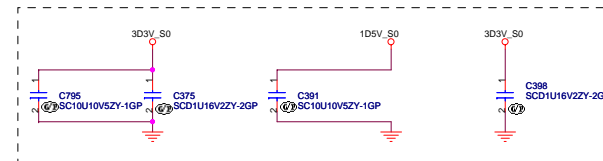
# Mini PCI-E Connector

## Port-2 low



62.10043.411

MAIN SOURCE: 62.10043.411  
SECOND SOURCE: 20.F1084.052



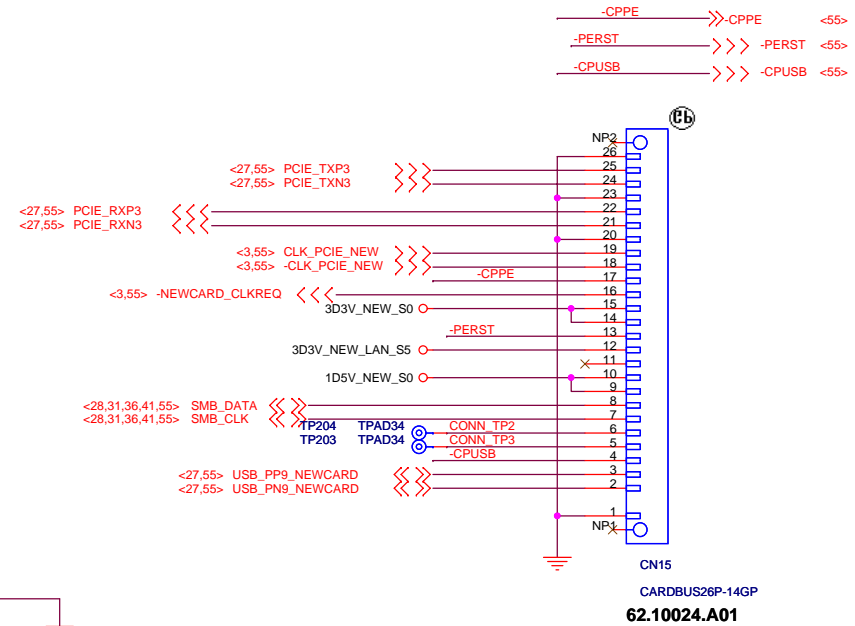
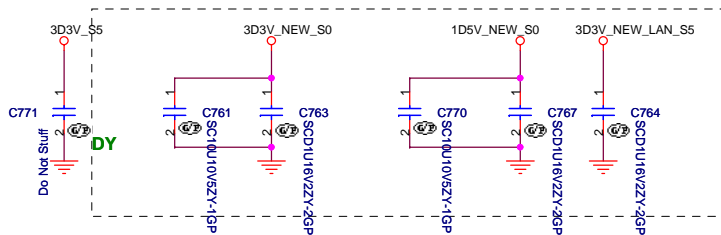
BOM1

# NEWCARD Connector

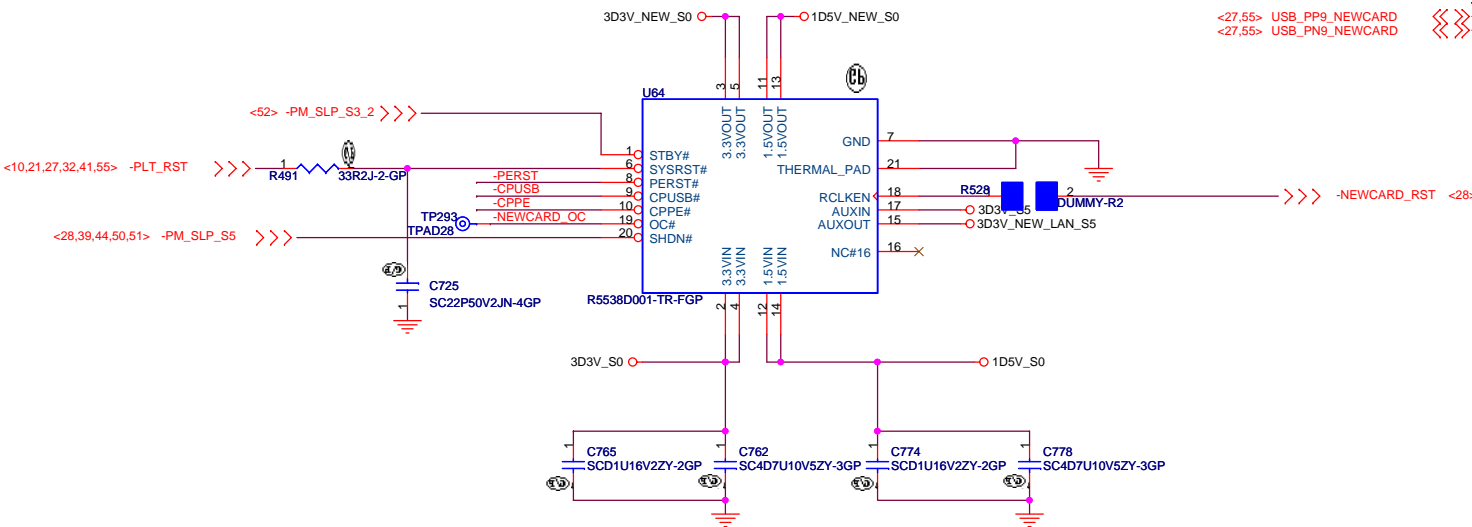
For Newcard socket

Place them Near to Chip

Place them Near to Connector



62.10024.A01



BOM1

|  |                 |
|--|-----------------|
| <b>緯創資通 Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                 |
| Title  |                 |
| Module NewCard   |                 |
| Size   | Document Number |
| LT32M  |                 |
| Date: Tuesday, May 13, 2008  | Rev -1          |
| Sheet 42   | of 54           |

## 1394



**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

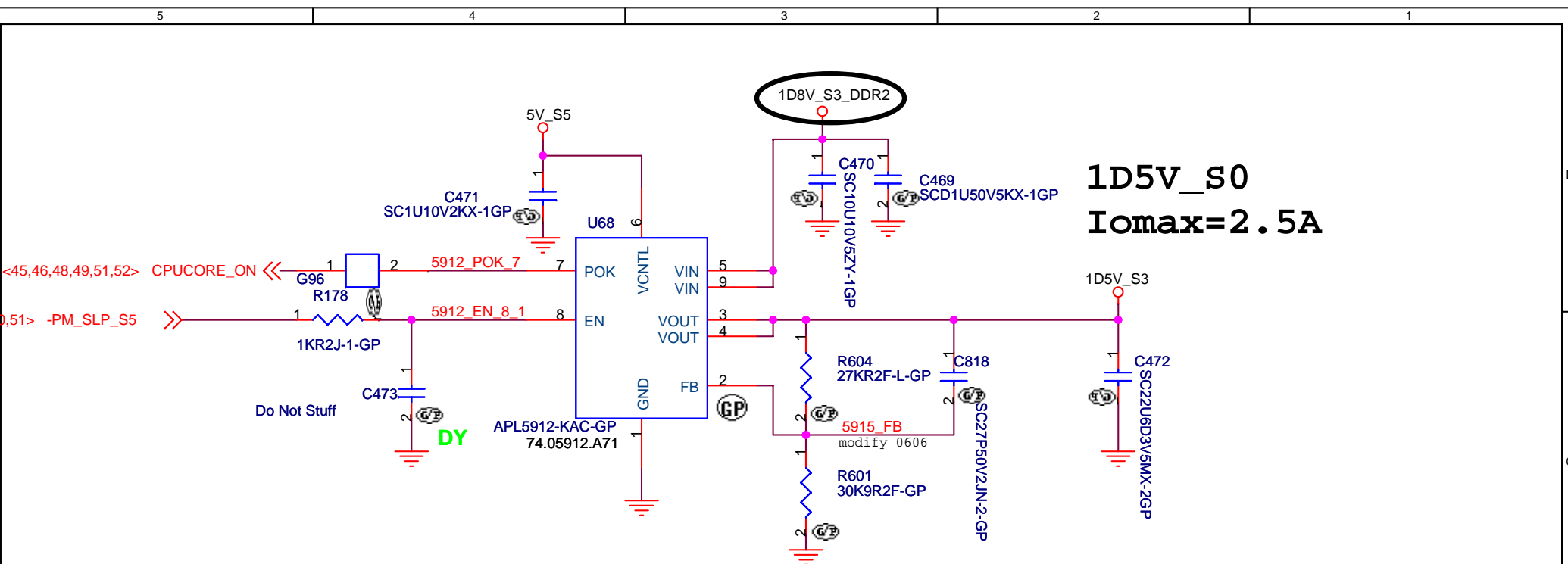
| Title | Author | Year | Journal | Volume | Page |
|-------|--------|------|---------|--------|------|
| ...   | ...    | ...  | ...     | ...    | ...  |

|      |                 |     |
|------|-----------------|-----|
| Size | Document Number | Rev |
|------|-----------------|-----|

|   |       |    |
|---|-------|----|
| B | LT32M | -1 |
|---|-------|----|

Date: Tuesday, May 13, 2008 Sheet 43 of 54

D  
C  
B  
A

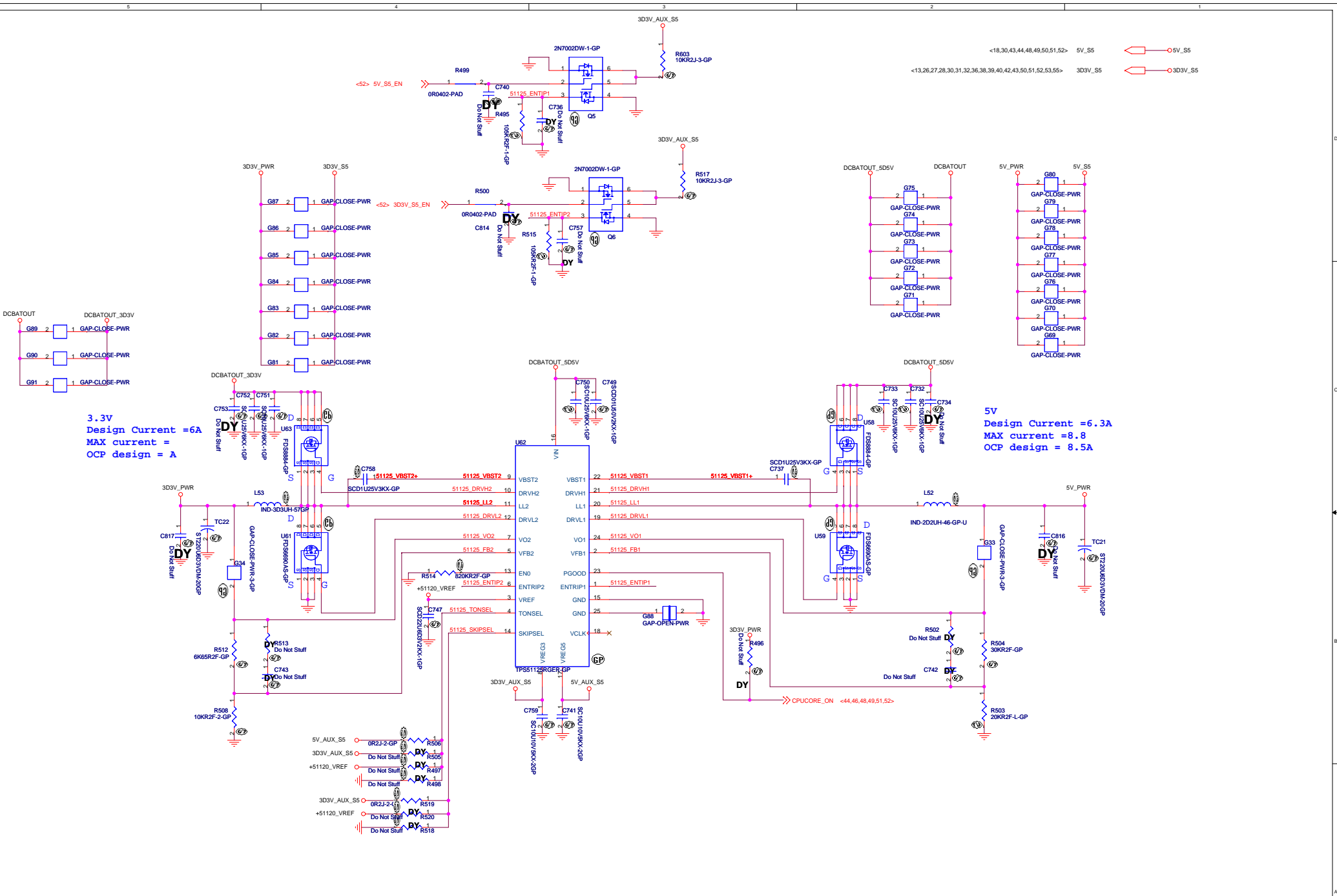


1D5V\_S0  
Iomax=2.5A

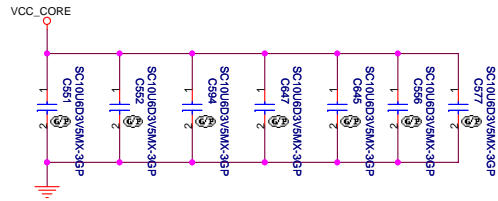
$$Vo=0.8*(1+(R1/R2))$$

BOM1

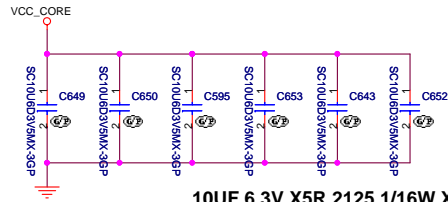
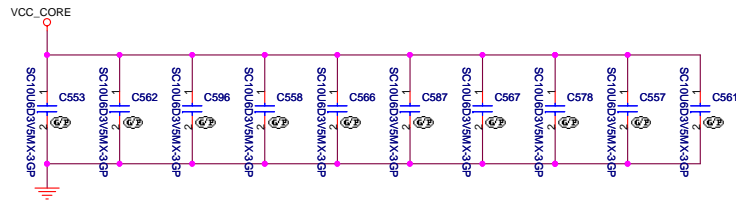
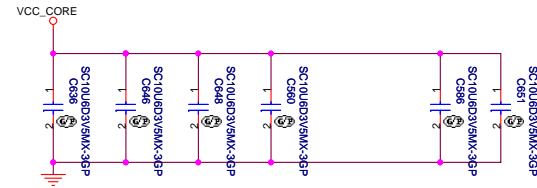
|  |                                    |
|--|------------------------------------|
| <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br/>Taipei Hsien 221, Taiwan, R.O.C.</div> |                                    |
| Title <div>1D5V_S0</div>   |                                    |
| Size   | Document Number <div>Olympus</div> |
|  | Rev <div>-1</div>                  |
| Date: Tuesday, May 13, 2008  | Sheet 44 of 55                     |







10UF 6.3V X5R 2125 1/16W X16 PCS



10UF 6.3V X5R 2125 1/16W X16 PCS

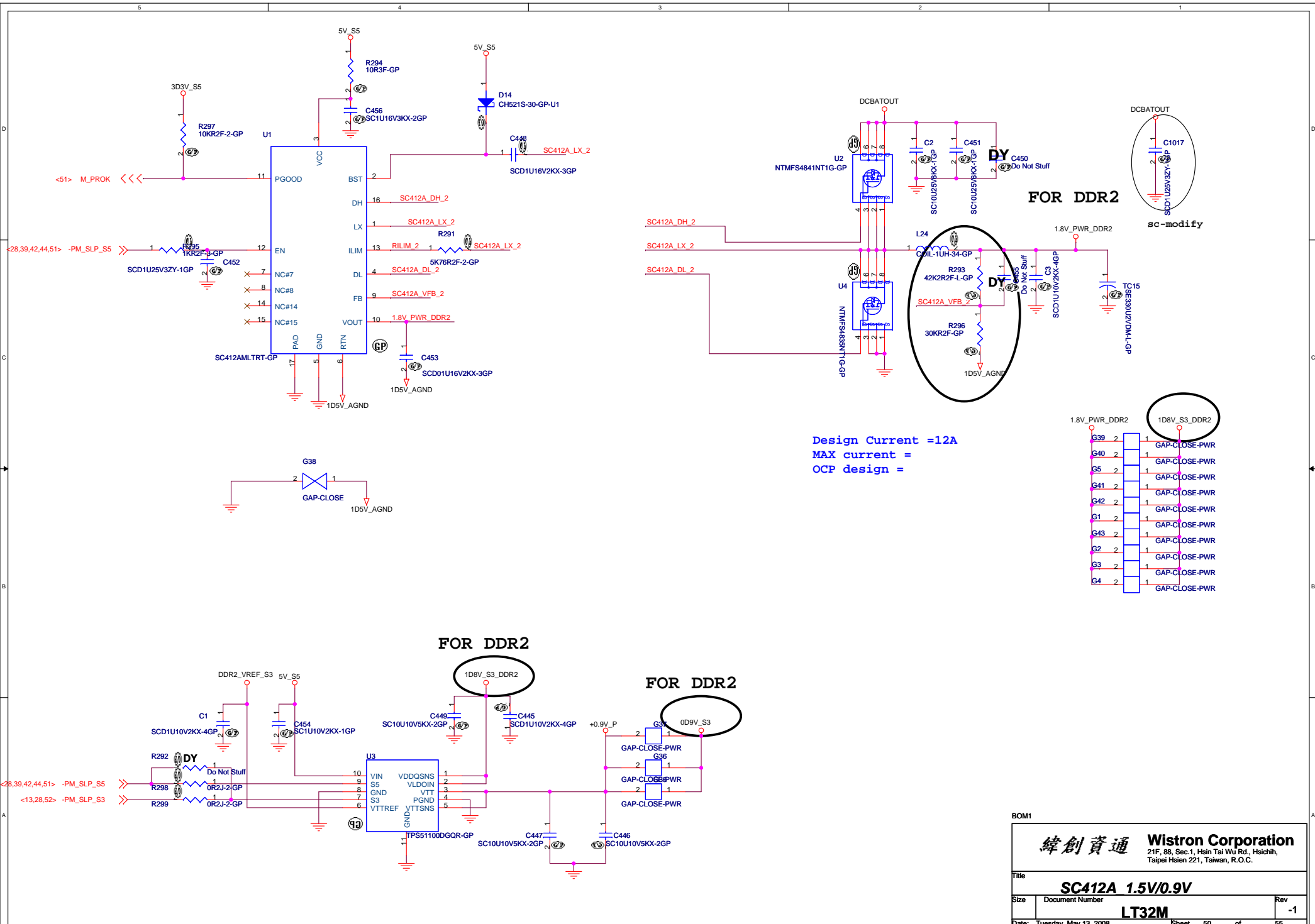
BOM1

|                                       |                                 |   |    |
|---------------------------------------|---------------------------------|---|----|
| <b>緯創資通</b>                           |                                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |    |
| Title<br><b>VCCCPUCORE DECOUPLING</b> |                                 |   |    |
| Size<br>Custom                        | Document Number<br><b>LT32M</b> | Rev<br><b>-1</b>  |    |
| Date: Tuesday, May 13, 2008           | Sheet 47                        | of  | 55 |

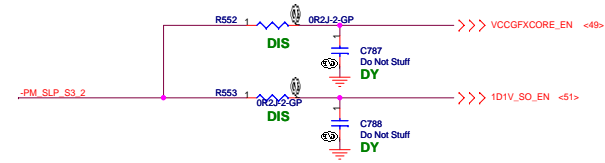


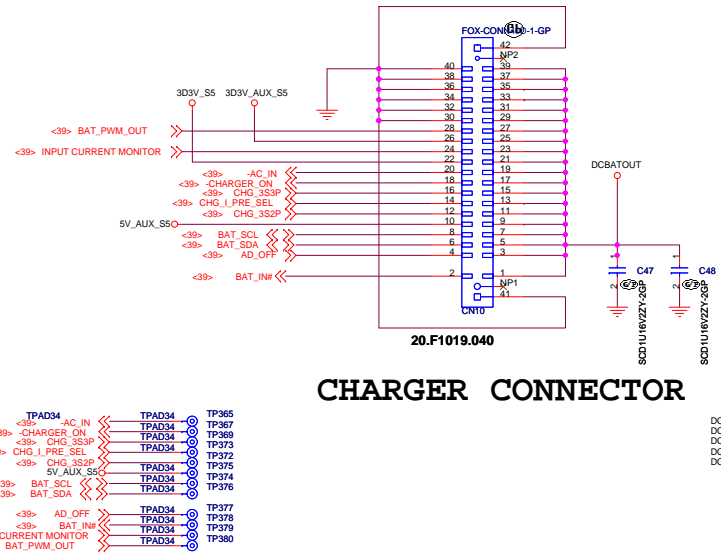
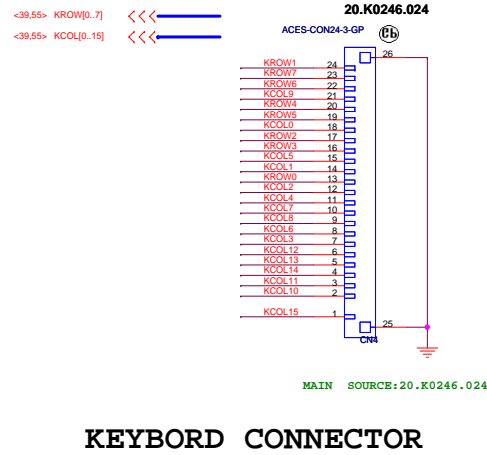
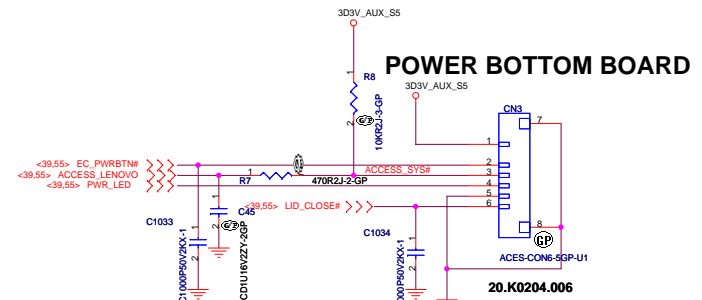
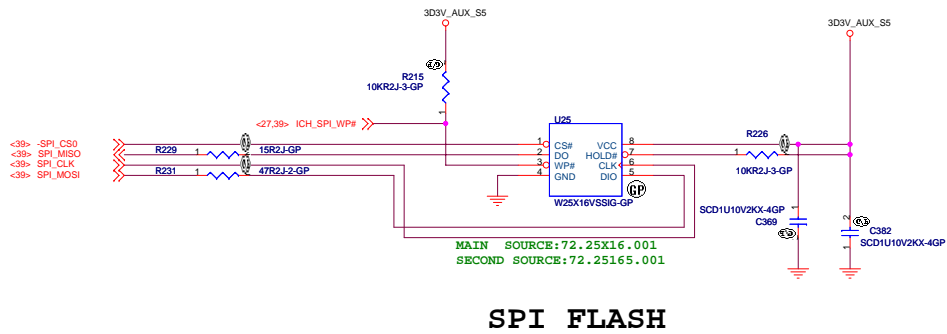




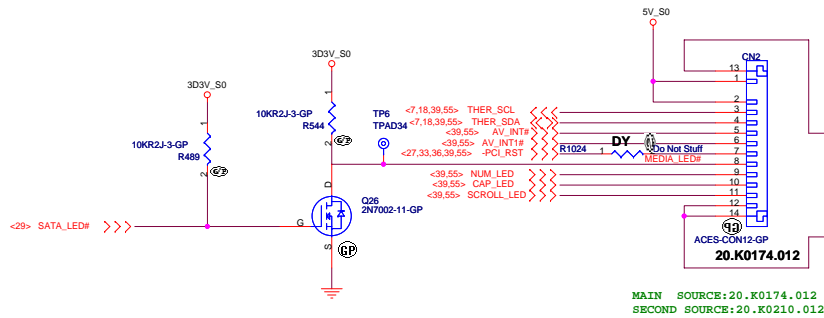




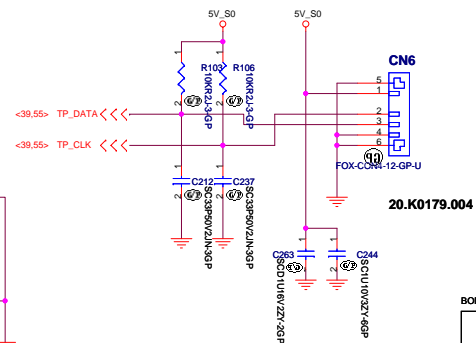


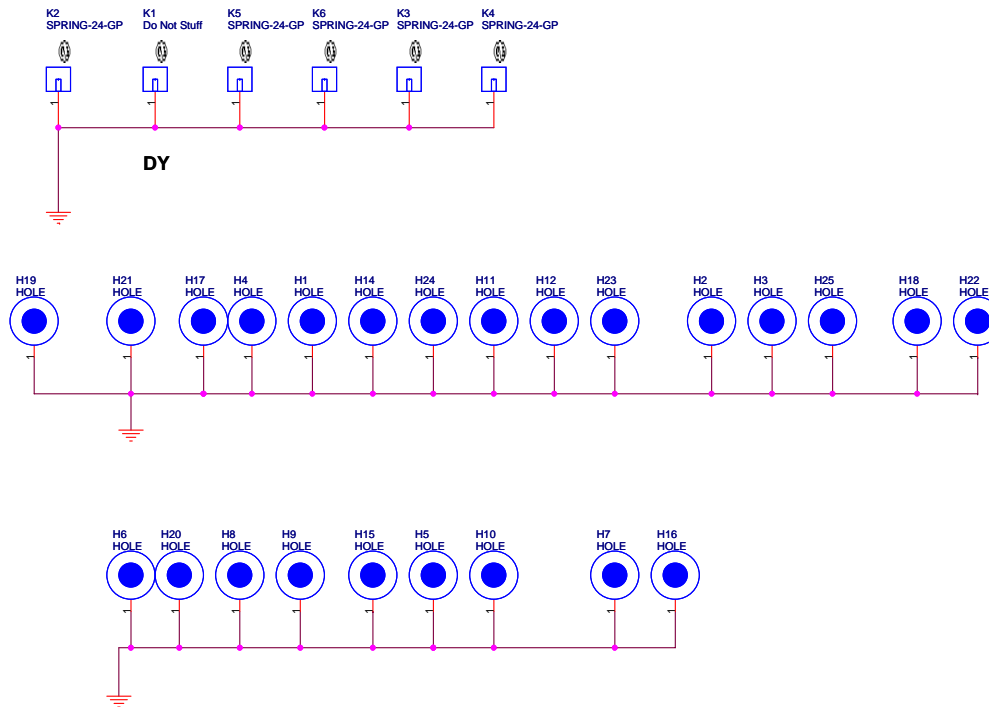


## AV Panel



## TouchPad Connector





BOM1

|                             |                 |   |       |
|-----------------------------|-----------------|---|-------|
| <b>緯創資通</b>                 |                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |       |
| Title                       |                 | <b>PTH FOR SCREW HOLES</b>  |       |
| Size                        | Document Number | LT32M   | Rev   |
| Custom                      |                 |   | -1    |
| Date: Tuesday, May 13, 2008 | Sheet           | 54  | of 55 |

