

Hulium UMA Schematics Document Sandy Bridge Intel PCH

*DY :None Installed
UMA:UMA installed*

*ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.*

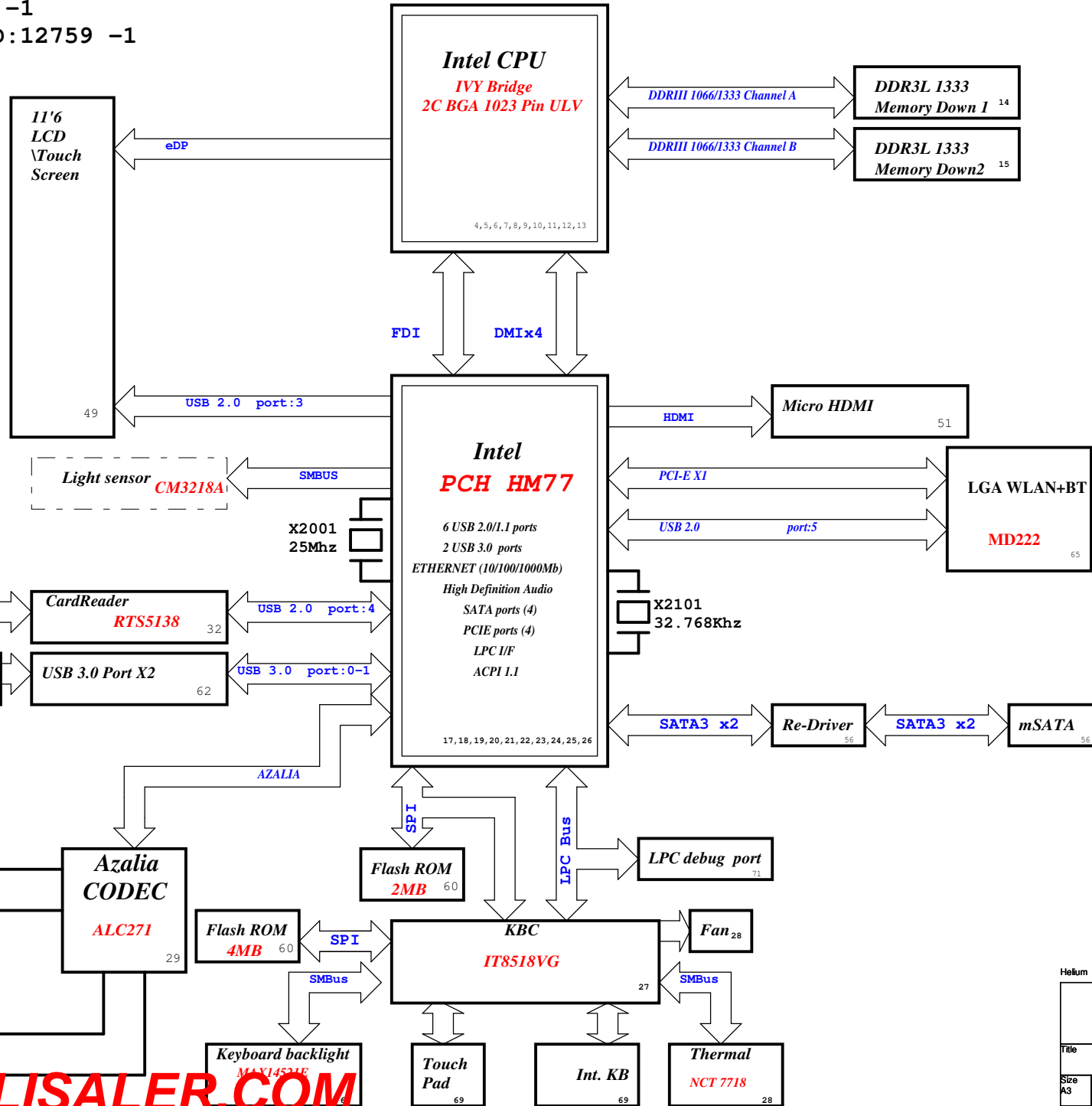
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Title			
Cover Page			
Size	Document Number	Rev	
A3	Helium	-1	
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Project code:91.4WD01.001
PCB:12222 -1
mSATA BD:12757 -1
Light Sensor BD:12759 -1
EL BD:12758 -1

Helium Block Diagram



CPU DC/DC	
VT1323SFCX 42~43	
INPUTS	OUTPUTS
5V_S5	VCC_CORE
SYSTEM DC/DC	
VT386FCX 45	
INPUTS	OUTPUTS
5V_S5	1D05V_VTT
SYSTEM DC/DC	
RT8223MZQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC	
RT9026GQW 46	
INPUTS	OUTPUTS
1D35V_S3	0D675V_S0 DDR_VREF_S3
SYSTEM DC/DC	
NCP5911MNTBG 44	
INPUTS	OUTPUTS
5V_S5	VCC_GFXCORE_PWR
VT357FCX	
46	
INPUTS	OUTPUTS
5V_S5	1D35V_S3
TI CHARGER	
BQ24760RSBR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
SYW231ABC 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
SYSTEM DC/DC	
RT9041B 93	
INPUTS	OUTPUTS
1D8V_S0	1D5V_S0
SYSTEM DC/DC	
SY8037DDCC 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0
PCB LAYER	
L1:Top	L6:Signal
L2:VCC	L7:GND
L3:Signal	L8:Signal
L4:VCC	L9:GND
L5:Signal	L10:Bottom

Helium

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Block Diagram

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2CH SPEAKER
4ohm 1w

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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: If the signal is sampled high.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high. External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor.
DF_TVS	A strap for selecting DMI and FDI termination voltage. DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms +5% resistor.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts.
SATA2GP/ GPIO36	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_SDO	Weak internal pull-down. This signal has a 20k internal pull down resistor.
HDA_SYNC	On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality.
L_DDC_DATA	When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down
SDVO_CTRLDATA/ DDPC_CTRLDATA/ DDPD_CTRLDATA	When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down
DSWVRMEN	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7K resistor to ensure proper strap setting when use as the chipset test interface.
GPIO29/ SLP_LAN#	If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN. If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	1
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	configuration lands A test point may be placed on the board for these lands.		

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	N/A
LANE2	N/A
LANE3	N/A
LANE4	WLAN
LANE5	THUNDERBOLT
LANE6	THUNDERBOLT
LANE7	THUNDERBOLT
LANE8	THUNDERBOLT

SATA Table

SATA	
Pair	Device
0	MSata
1	MSata
2	N/A
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A
8	N/A
9	N/A
10	N/A
11	N/A
12	N/A

USB Table

Pair	Device
0	USB3.0 Ext. port 2
1	USB3.0 Ext. port 1
2	NC
3	touch screen
4	Card Reader
5	BT(MD222)
6	CCD
7	X
8	X
9	NC
10	NC
11	NC
12	NC

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB Address Hex Bus
Device		
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

Helium

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SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

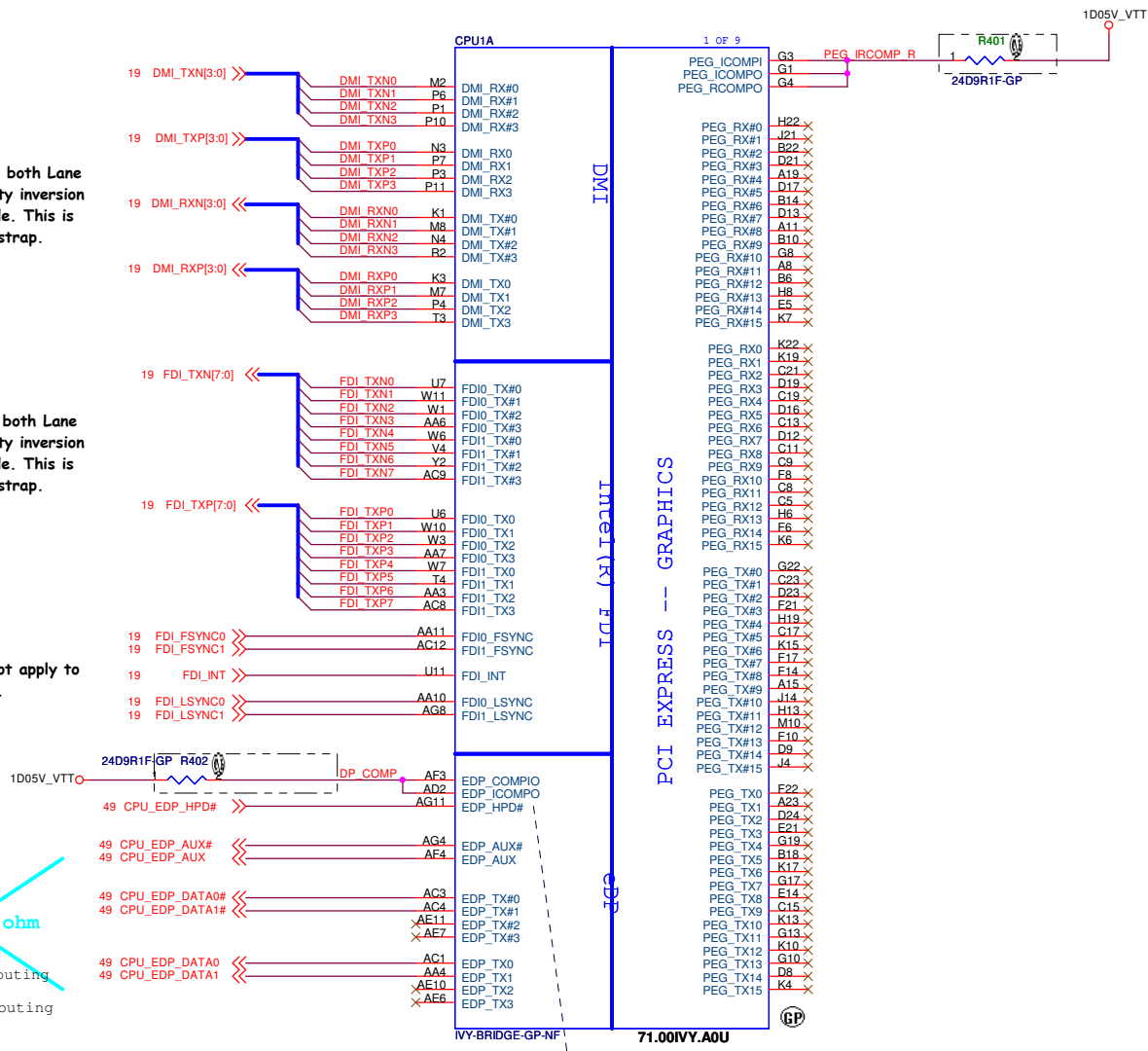
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Impedance: 85 ohm

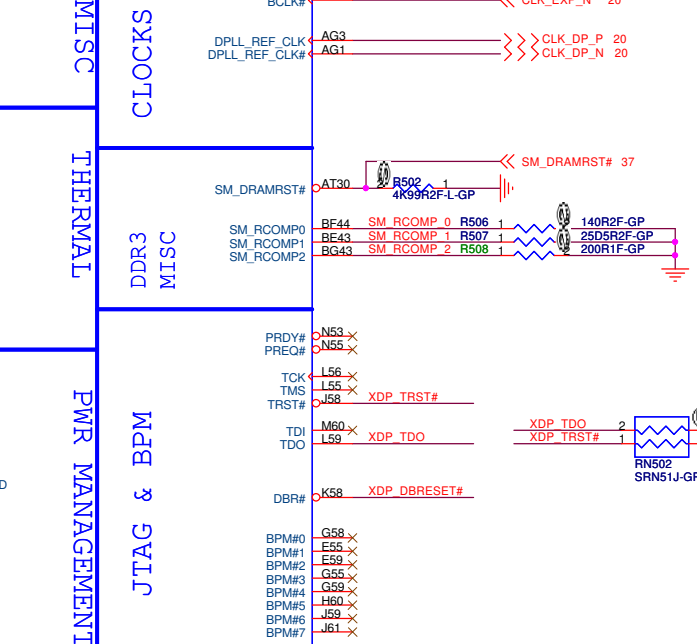
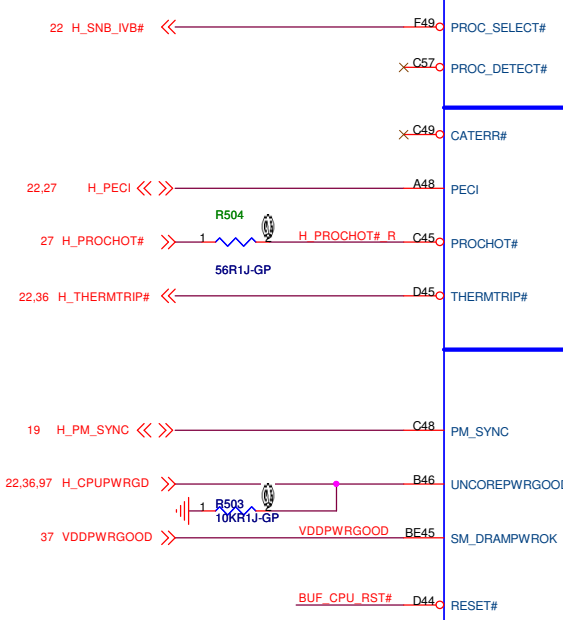
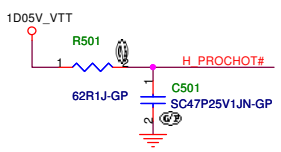
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

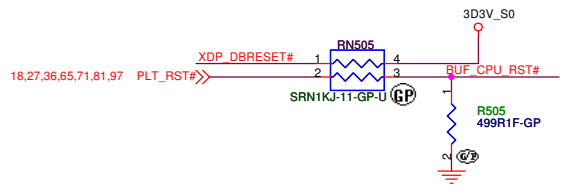
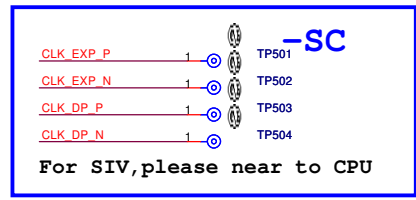


NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

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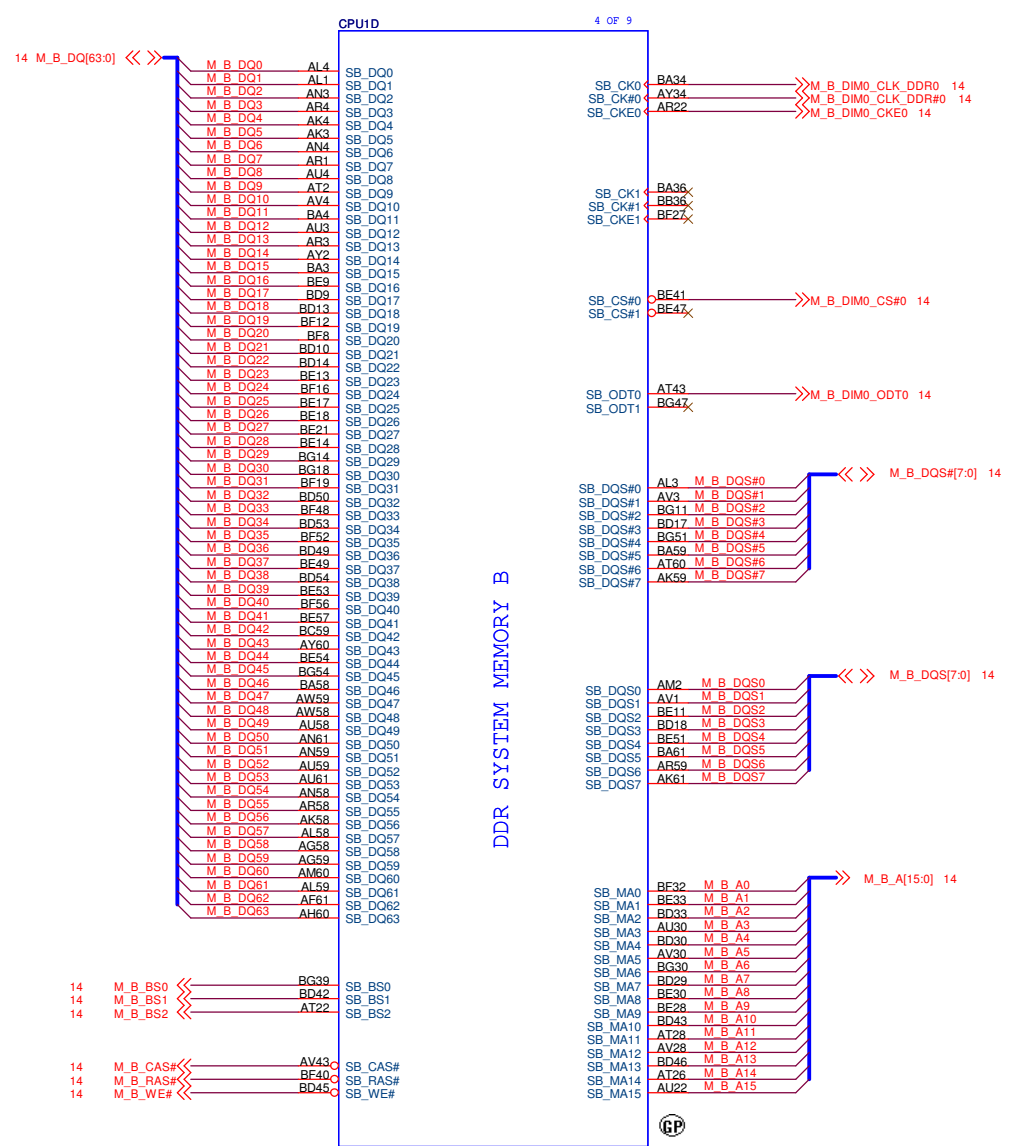
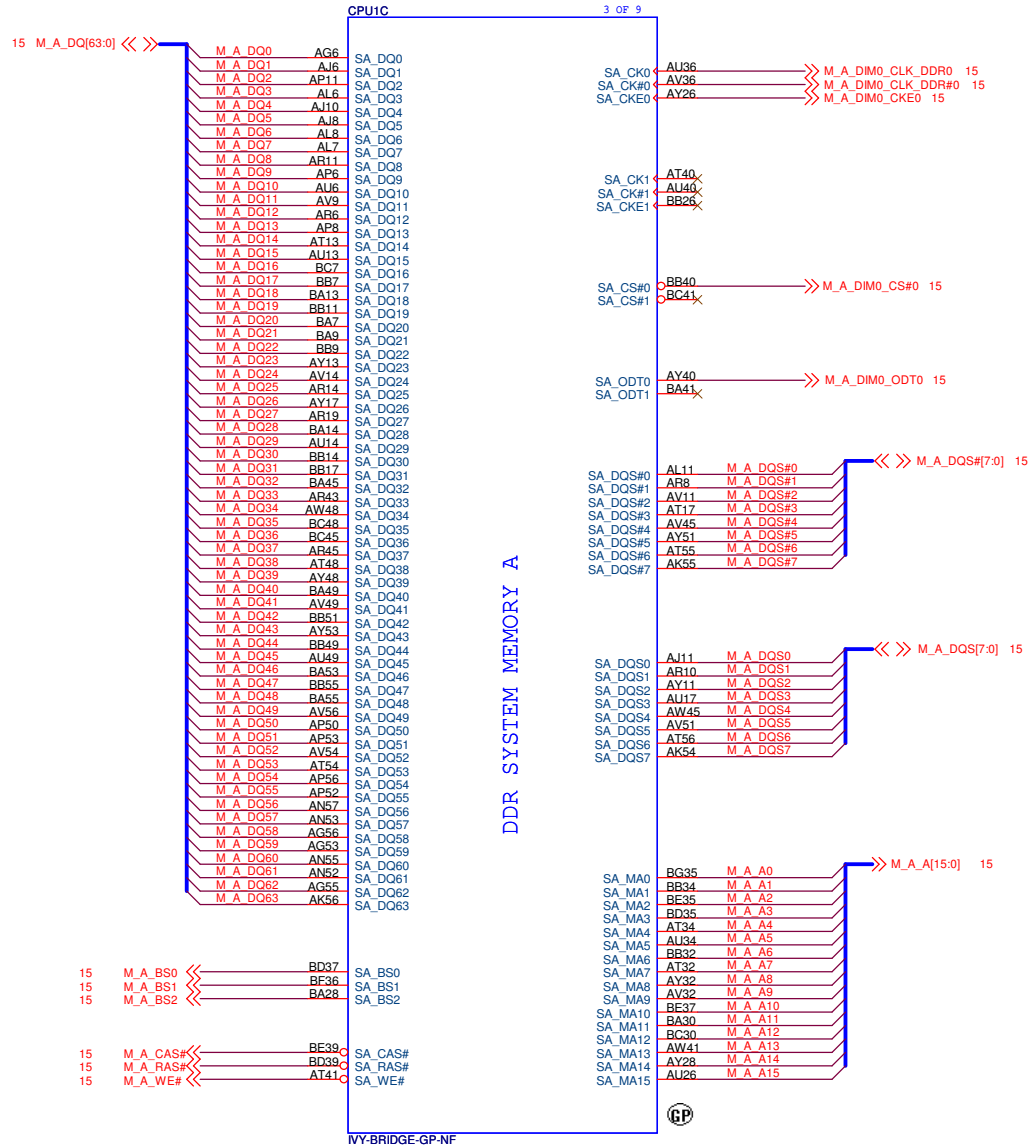


Disabling Guidelines:
If motherboard only supports external graphics or without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.



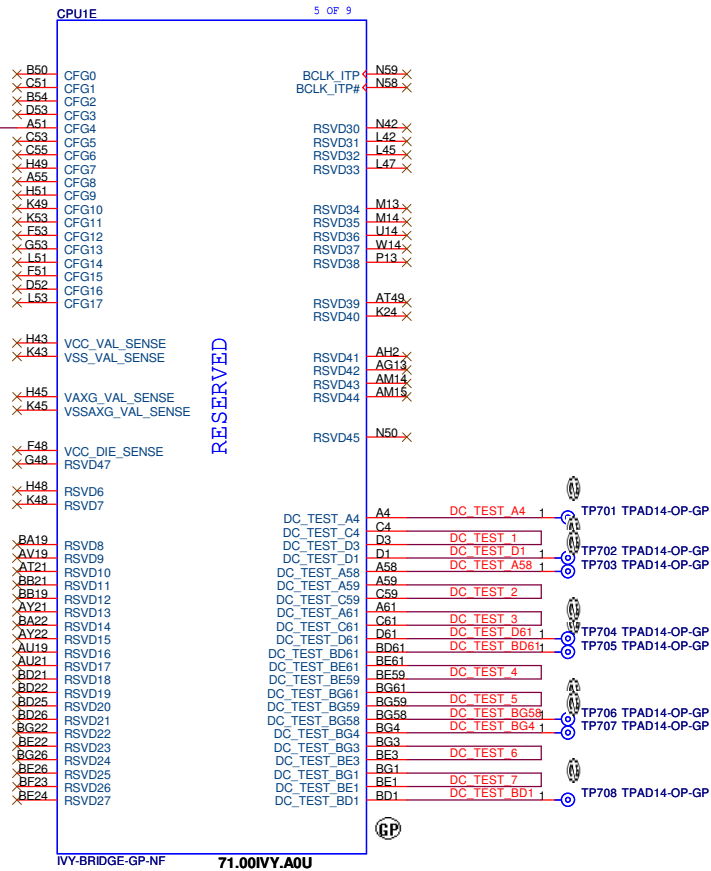
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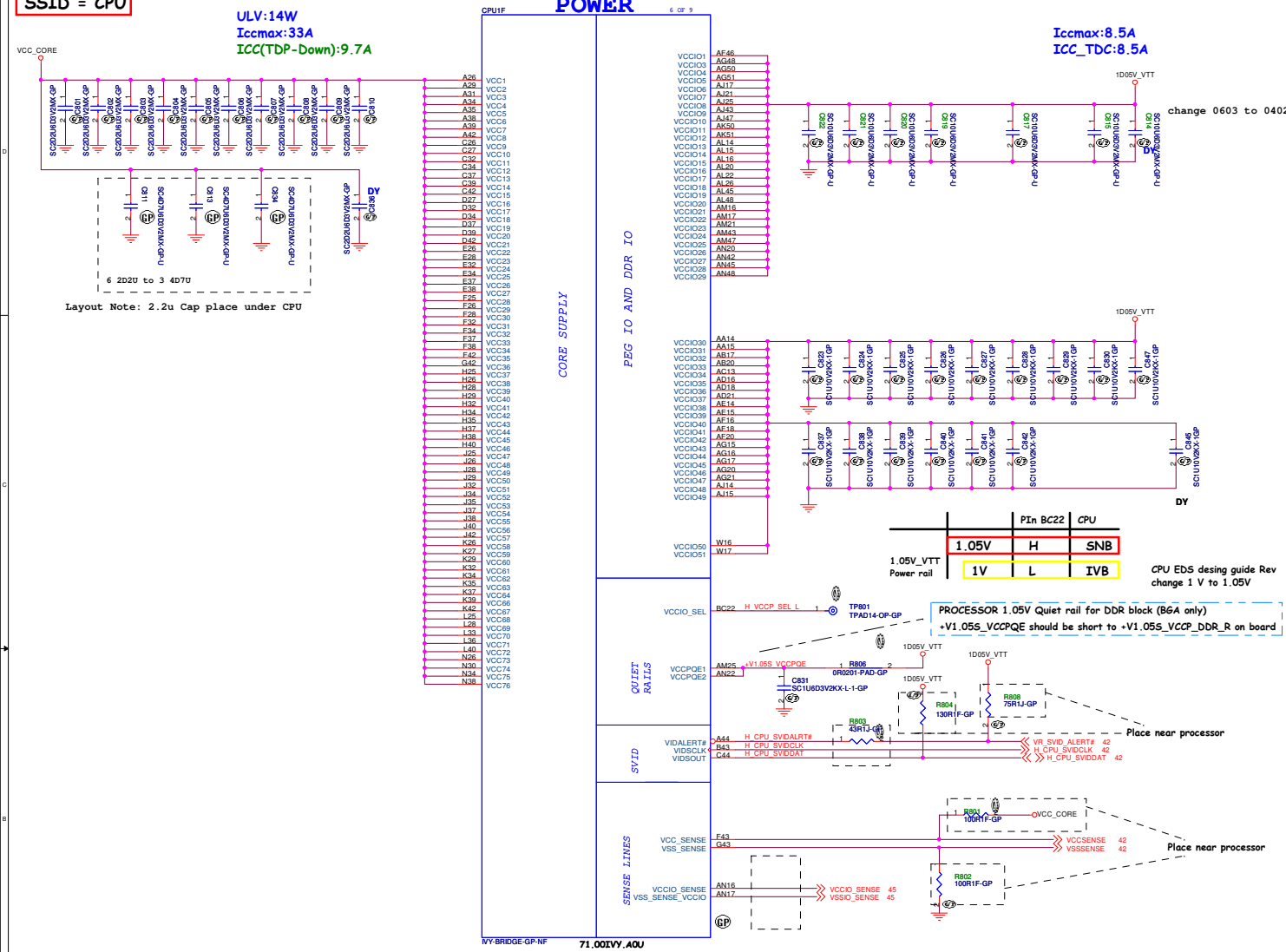
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	0
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable 0: Enabled - An external Display Port device is connected to the Embedded Display Port Full-down to GND through a 1KΩ ± 5% resistor to enable port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	00
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

SSID = CPU

ULV:14W
Iccmax:33A
ICC(TDP-Down):9.7A

POWER

Iccmax:8.5A
ICC_TDC:8.5A

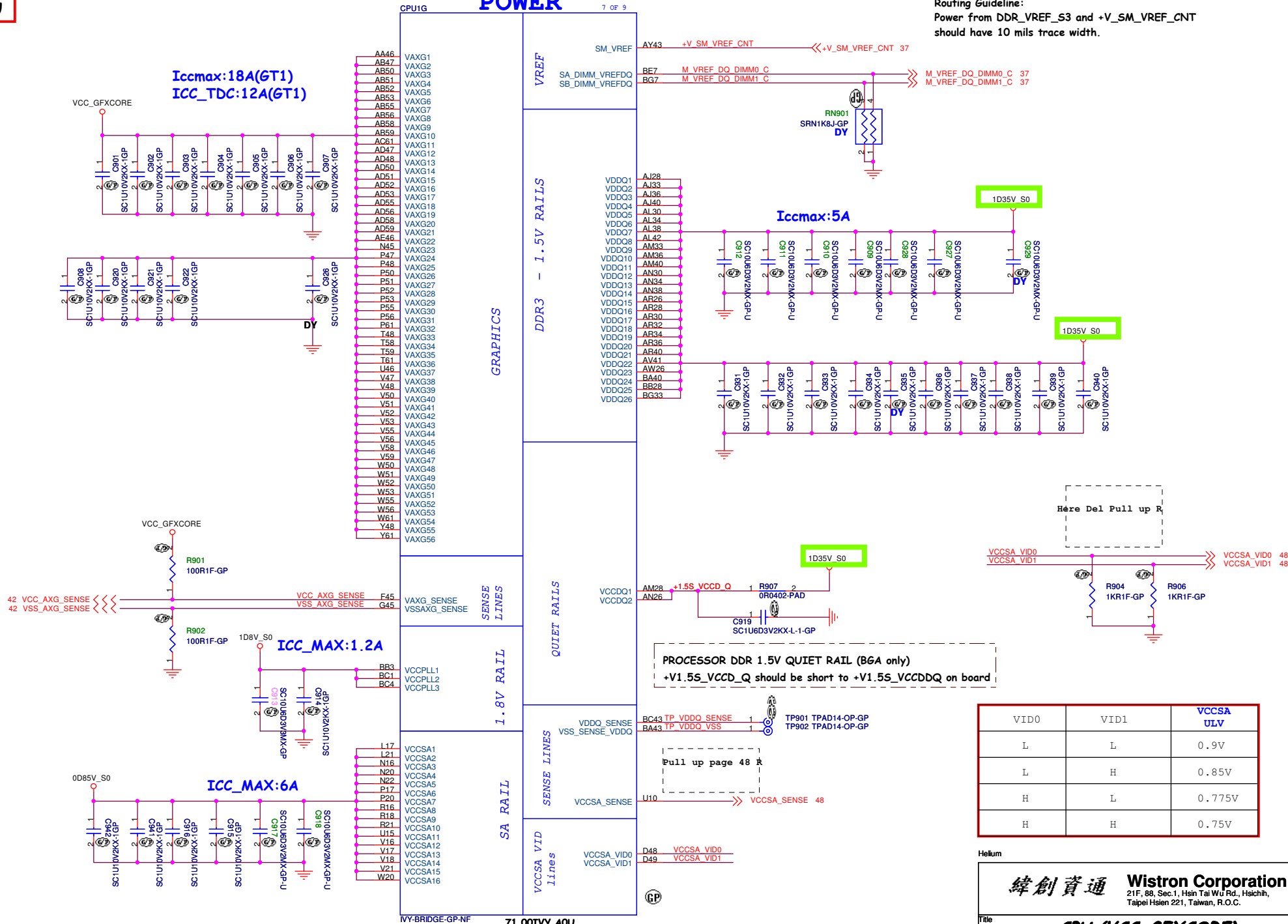


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SSID = CPU

POWER

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.



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SSID = CPU

CPU1H 8 OF 9

VSS

NCTF

GP

IVY-BRIDGE-GP-NF

CPU1I 9 OF 9

VSS

NCTF

GP

IVY-BRIDGE-GP-NF

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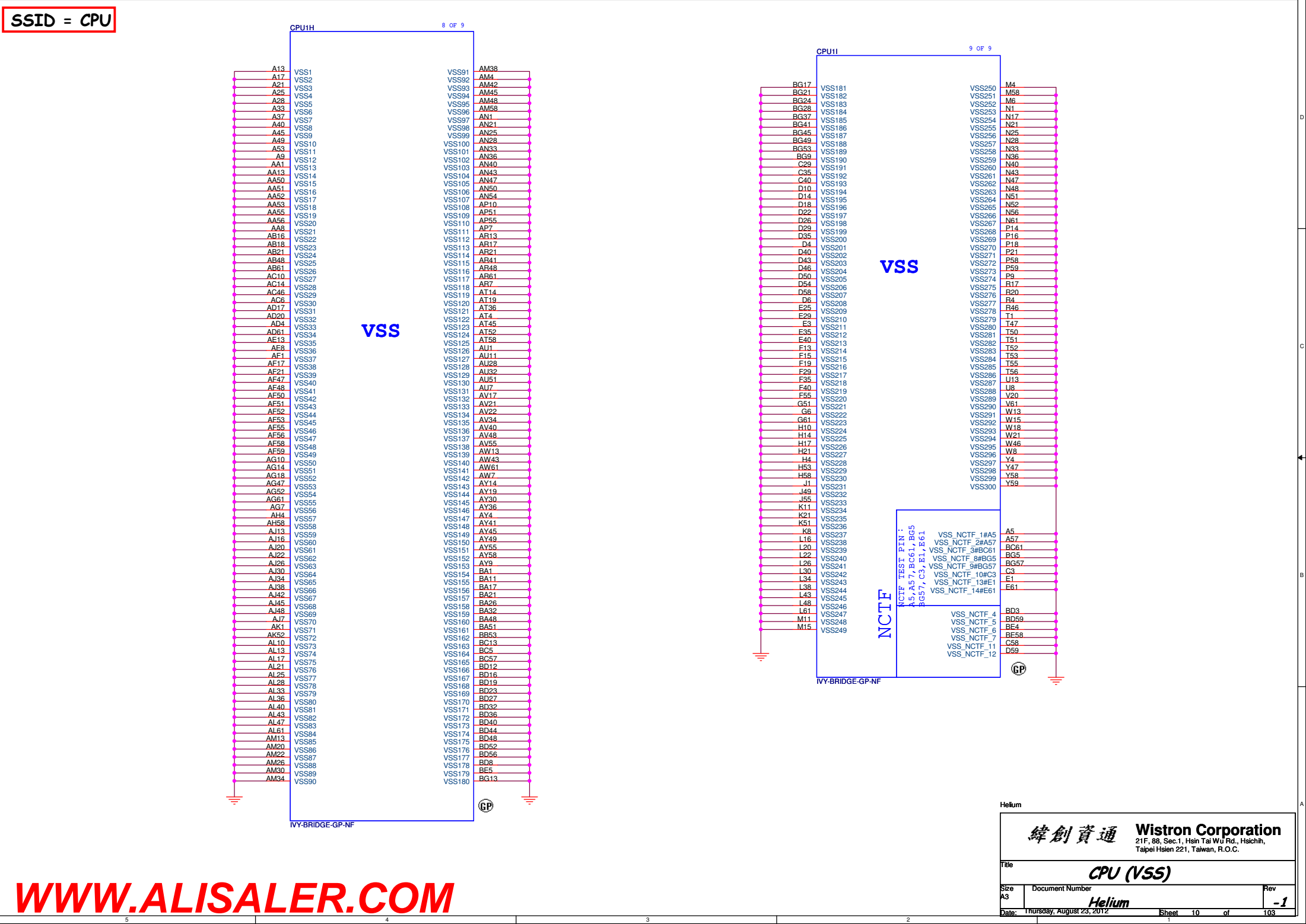
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reserve

JE40 delete XDP function		
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XDP		
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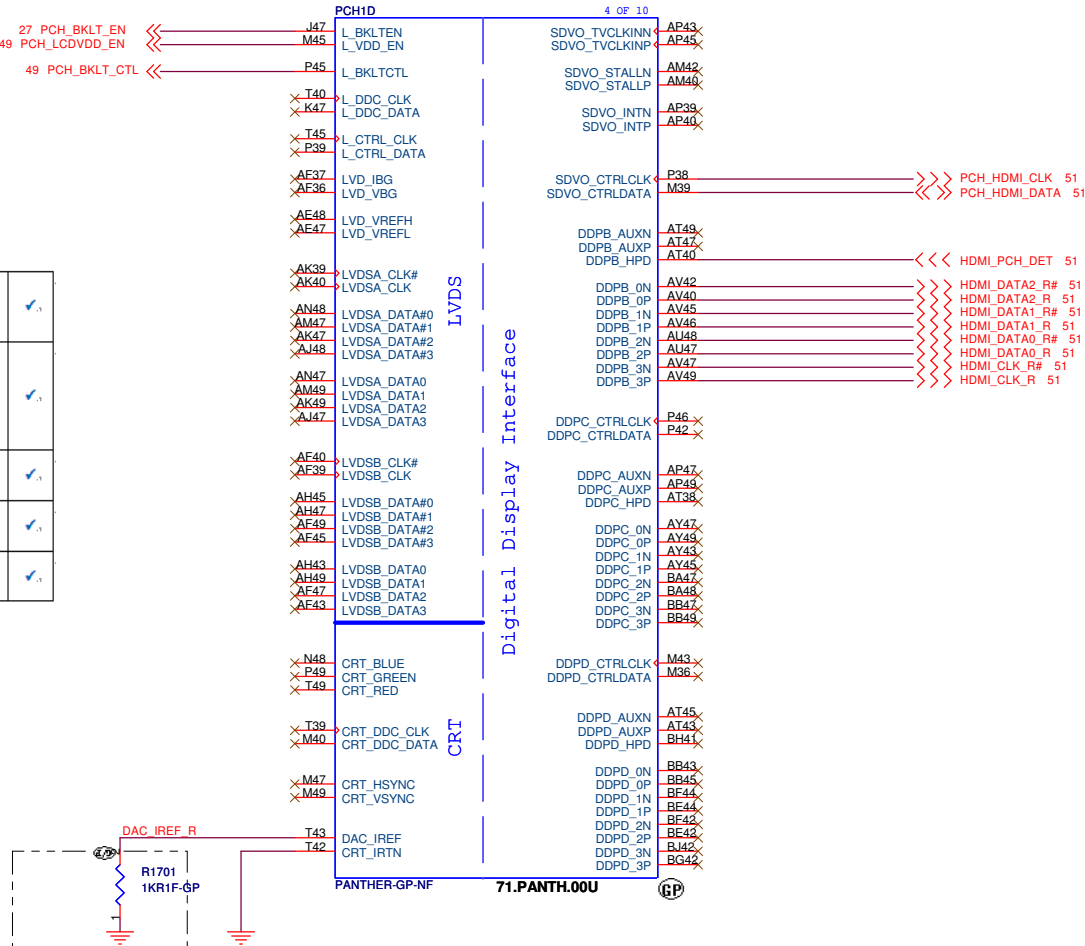
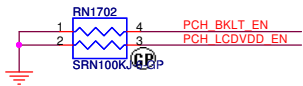


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3.24.2 LVDS Disable Guidelines

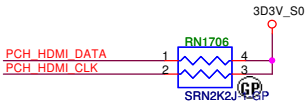
Pin Name	System Pull-up/ Pull-down	Schematic Notes	
Data/Clock/Control		All signals associated with the interface can be left as No Connect.	
Power Supply		The supply pins VCC_TX_LVDS, and VCCA_LVDS can be connected to GND.	



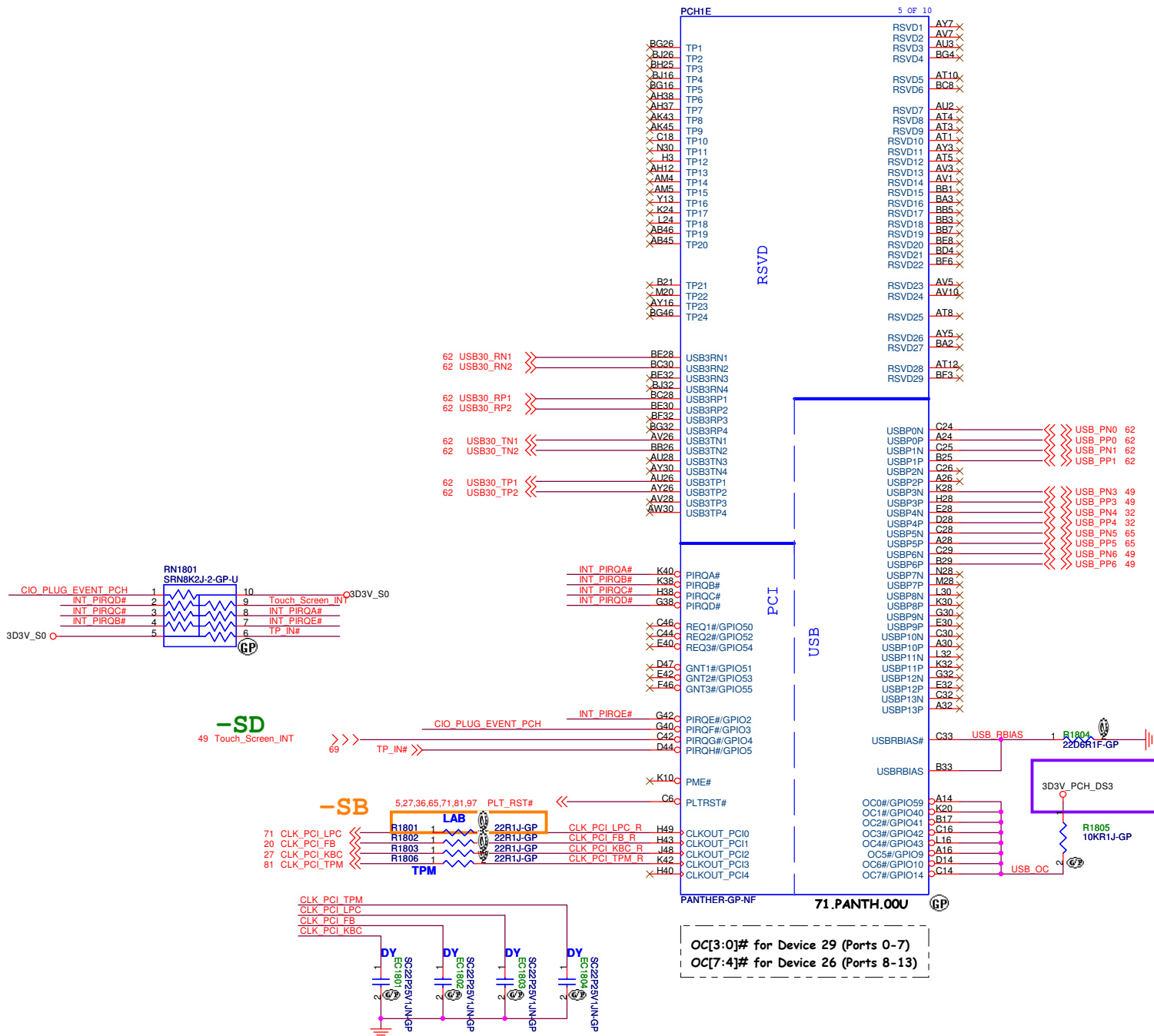
if use CRT change 1K to +/- 0.5% (64.10016.6DL)

3.24.4 CRT Disable

Name	System Pull-up/ Pull-down	Schematics Notes	
CRT_RED CRT_GREEN CRT_BLUE CRT_HSYCN CRT_VSYNC		Leave as No Connect.	
CRT_ITRN		Connect directly to GND plane on the motherboard.	
DAC_IREF	1-kΩ± 5% pull-down to GND		
VCCADAC	Connect to +V3.3 power-rail		



SSID = PCH



20120404 GPIO USB Table

Pair	Device
0	USB3.0 Ext. port 2
1	USB3.0 Ext. port 1
2	NC
3	touch screen
4	Card Reader
5	BT(MD222)
6	CCD
7	X
8	X
9	NC
10	NC
11	NC
12	NC

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

A Sku

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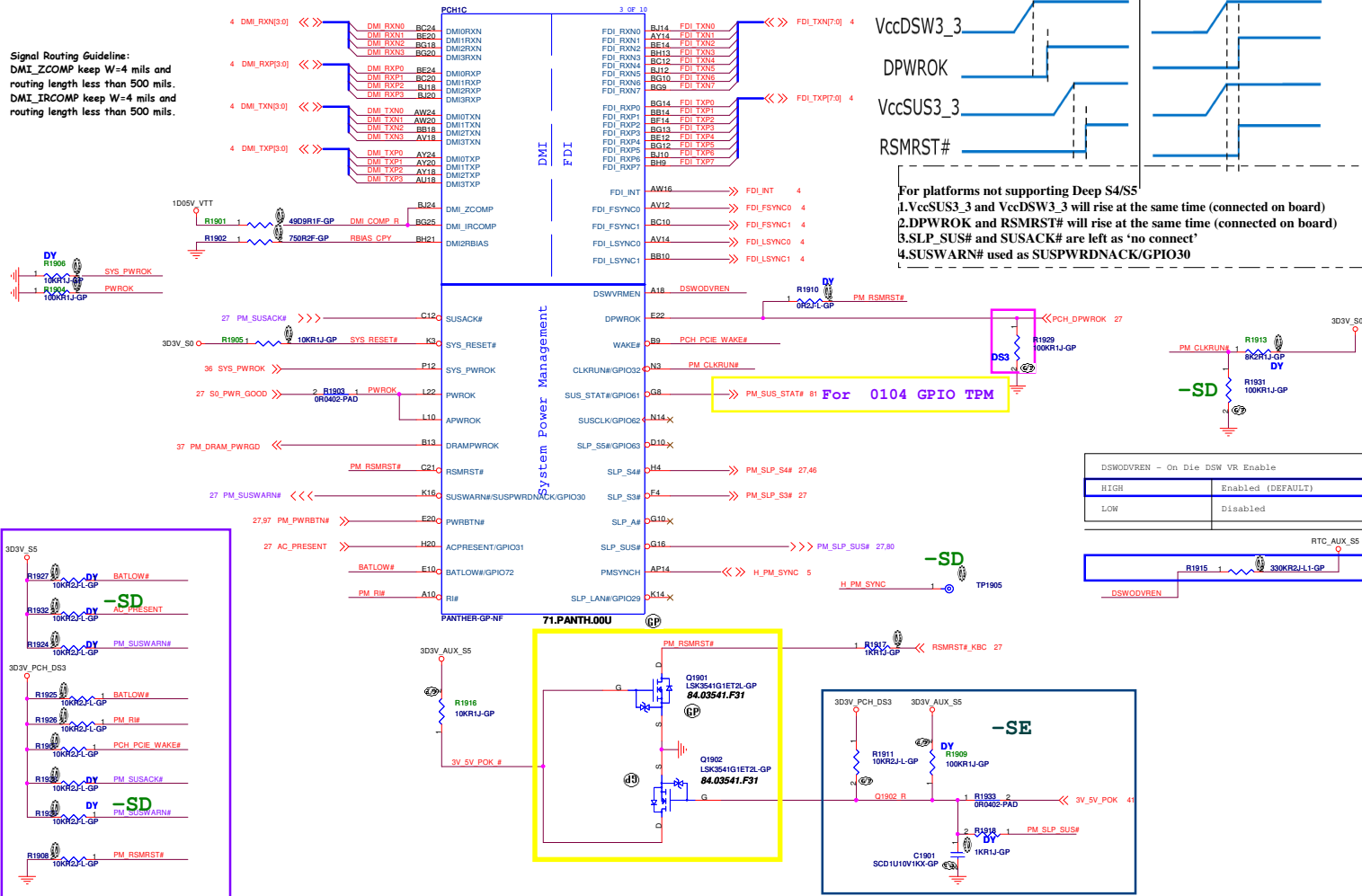
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Size		Document Number					Rev
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Deep S4/S5 Supported

Deep S4/S5 **Not** Supported

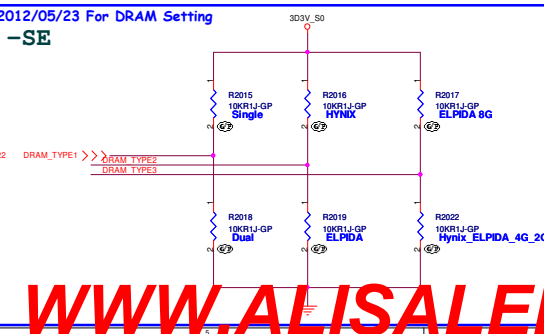
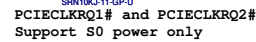
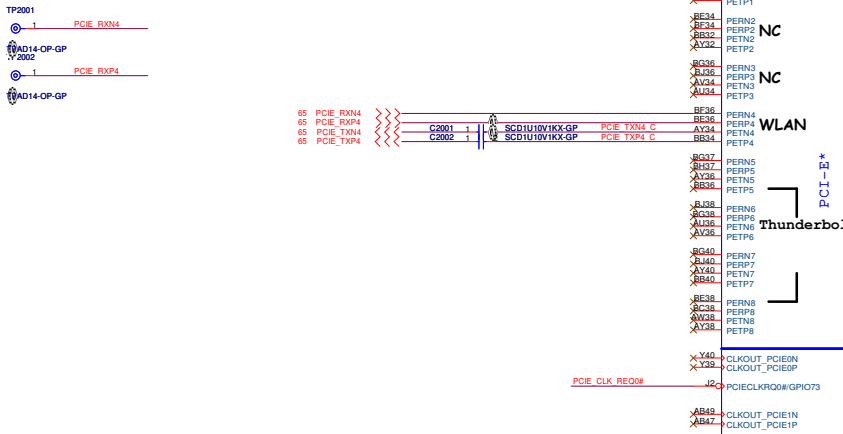
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

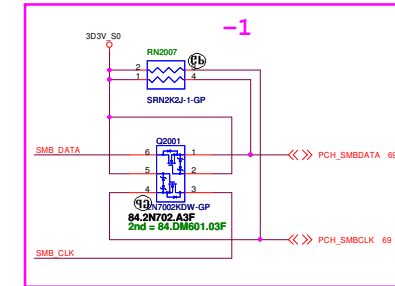
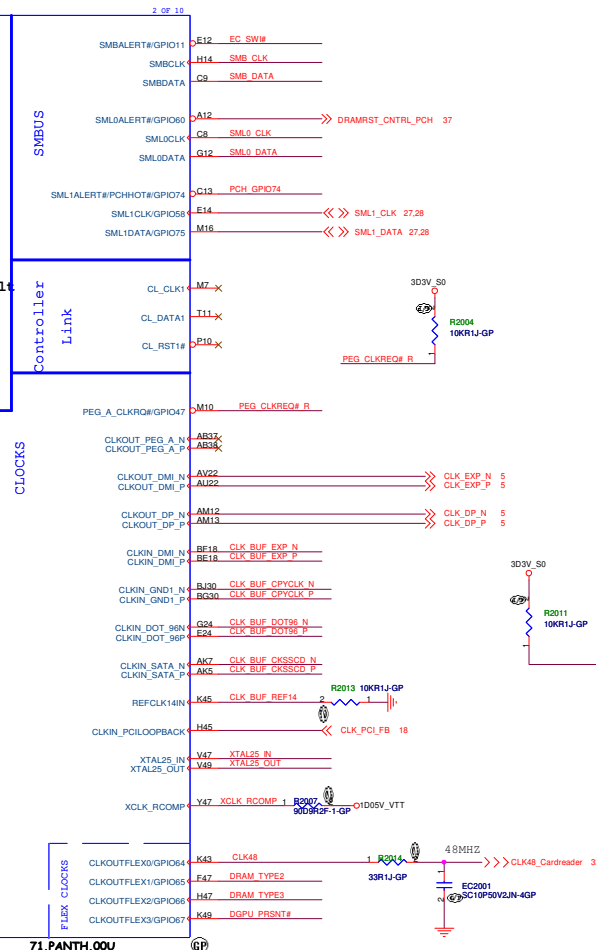
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for SIV, please near to PCH



GPIO48	GPIO66	GPIO65	Status
DRAM_Type1 single/dual channel	DRAM_Type3	DRAM_Type2	
0	0	0	ELPIDA 2G(2+2, Channel A+B)
0	0	1	HYNIX 2G(2+2, Channel A+B)
0	1	0	ELPIDA 4G(4+4, Channel A+B)
0	1	1	
1	0	0	ELPIDA 2G(channel A)
1	0	1	HYNIX 2G(channel A)
1	1	0	
1	1	1	

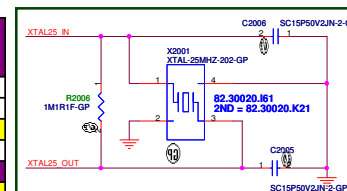
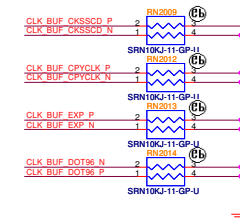
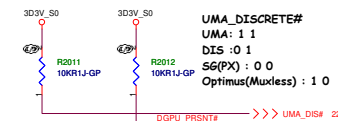
As Flex clocks, can be configured as 48 MHz, 24 MHz, 33 MHz, 27 MHz (Spread or Nonspread) 14.318 MHz. Refer to the PCH External Design Specification (EDS) for configuration options of Flex Clocks.



```
-SB David
Reserve for TP Smbus,
default DY to avoid crosstalk with L5 DDR bus
```

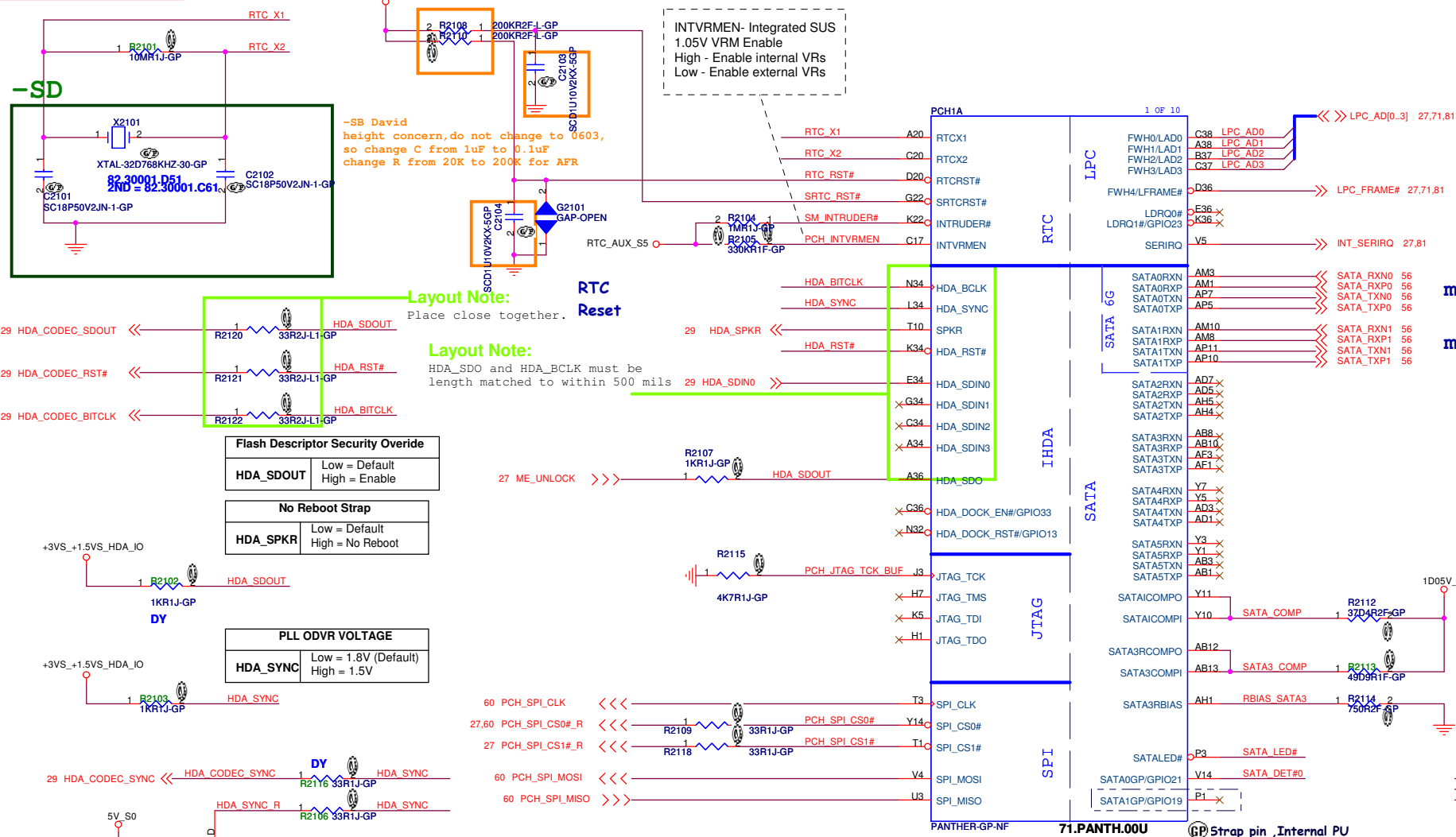
Pin number	Pin Define
1	VDD(3.3V)
2	PCClk
3	PCDt
4	DGND
5	NC*(SDA)
6	NC*(SCL)
7	NC*(INT)
8	NC

Note: Reserve for SMBus

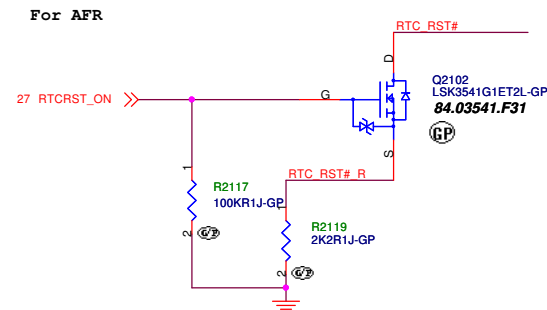


-SD

SSID = PCH



HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board.
Signal may have leakage paths via powered off devices(Audio Codec) and hence contend with the external pull-up.
A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



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Pass Word Clear

These four balls must connect to GND shared 1 Via

KBC(Recommended):EC collect all thermal data and
Performs Turbo power control

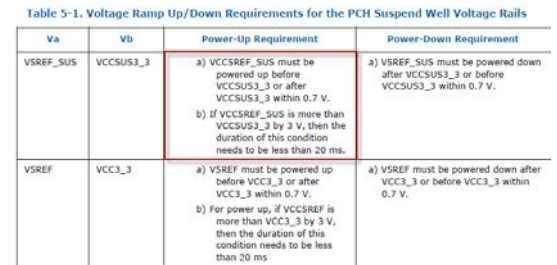
DMI_OVRVLTG (GPIO36)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)
-------------------------	--

PLL_ODVR_EN	HIGH- DISABLED [DEFAULT]
-------------	--------------------------

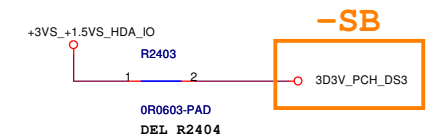
Size A3	Document Number <i>Helium</i>	Rev <i>-1</i>
Date: Thursday, August 23, 2012	Sheet 22 of	103

NCIF TEST PIN:
A4,A44,A45,A46,A5,A6,B3,B47,
BD1,BD49,BE1,BE49,BF1,BF49,
BG2,BG48,BH3,BH47,BJ4,BJ44,
BJ5,BJ46,BJ5,BJ6,C2,C48,D1,
D40,E1,E49,E1,E49

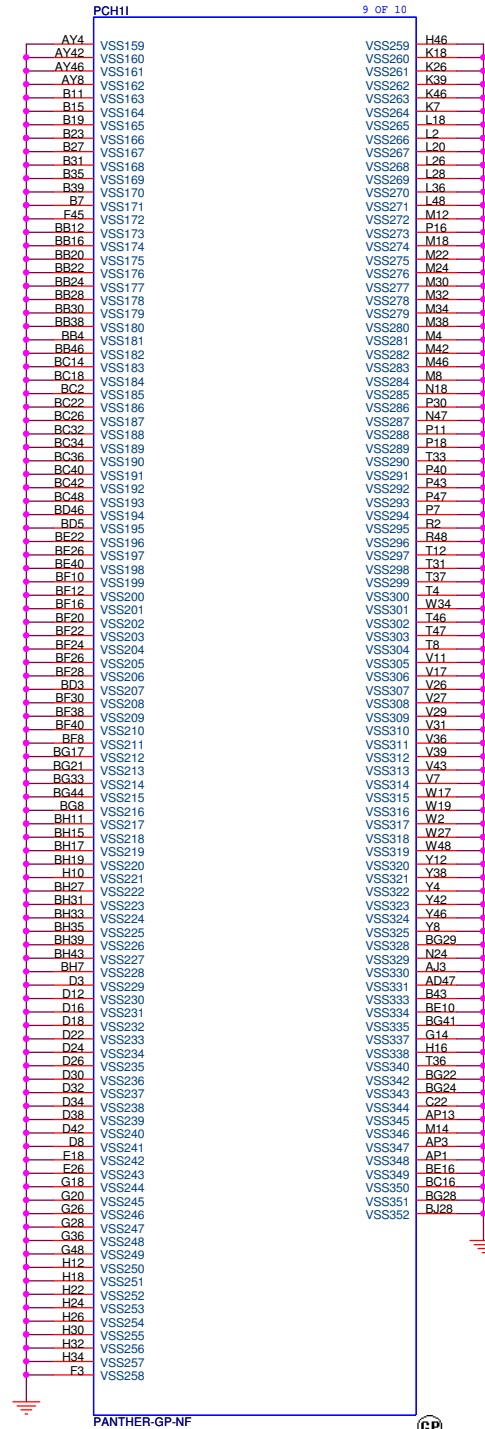
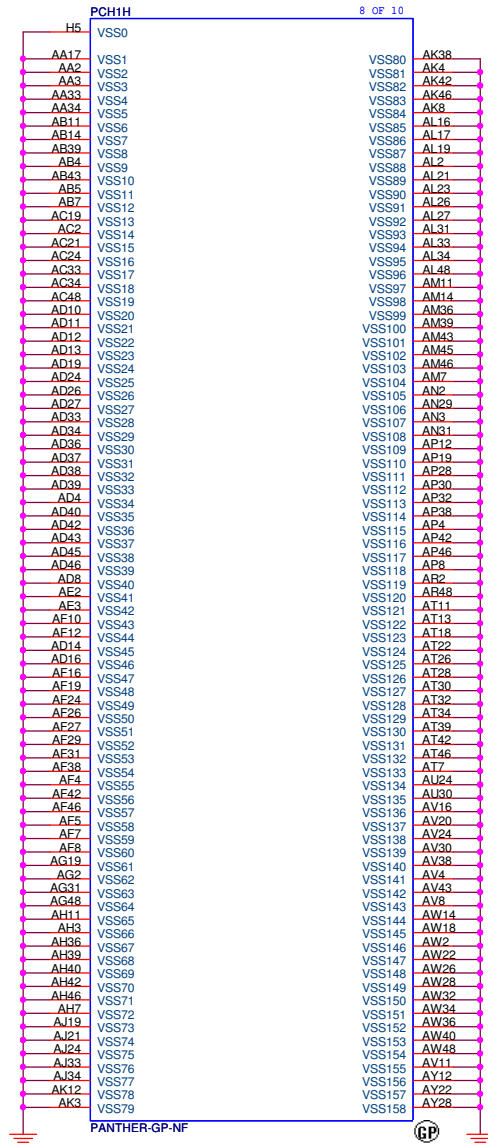
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VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)



SSID = PCH

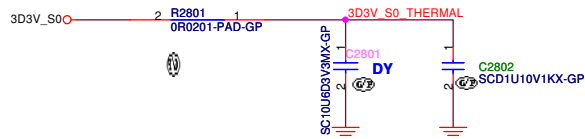


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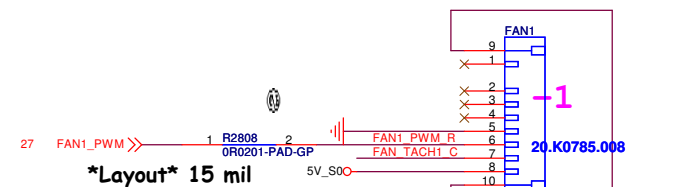
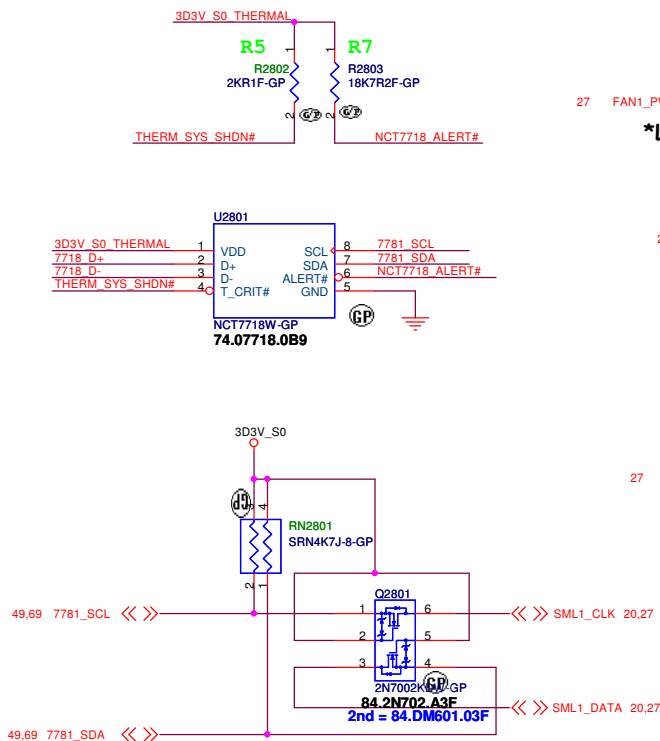
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Size	Document Number	Rev	
A3	Helium		-1
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SSID = Thermal

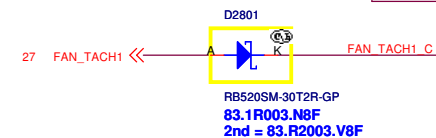


Layout notice :

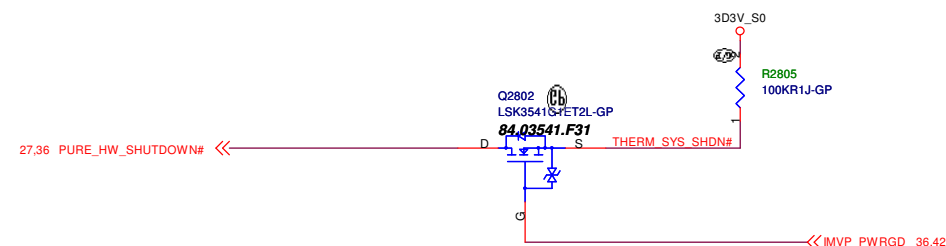
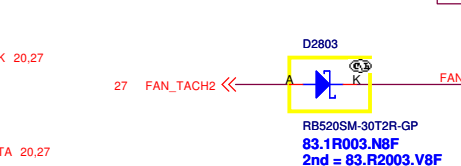
- * Put the C1 2200pF to close the nct7718W
- * Add ground shielding for D+ and D- traces
- * D+/D- route has to be away from the high noise area
- * The recommended traces width and ground shielding spacing are 10mils



Layout 15 mil



Layout 15 mil



Setting 85°C

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

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AUDIO OP AMPLIFIER

JE40 delete AMP function

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Title

Audio AMP

Size
A4

Document Number

Helium

Rev
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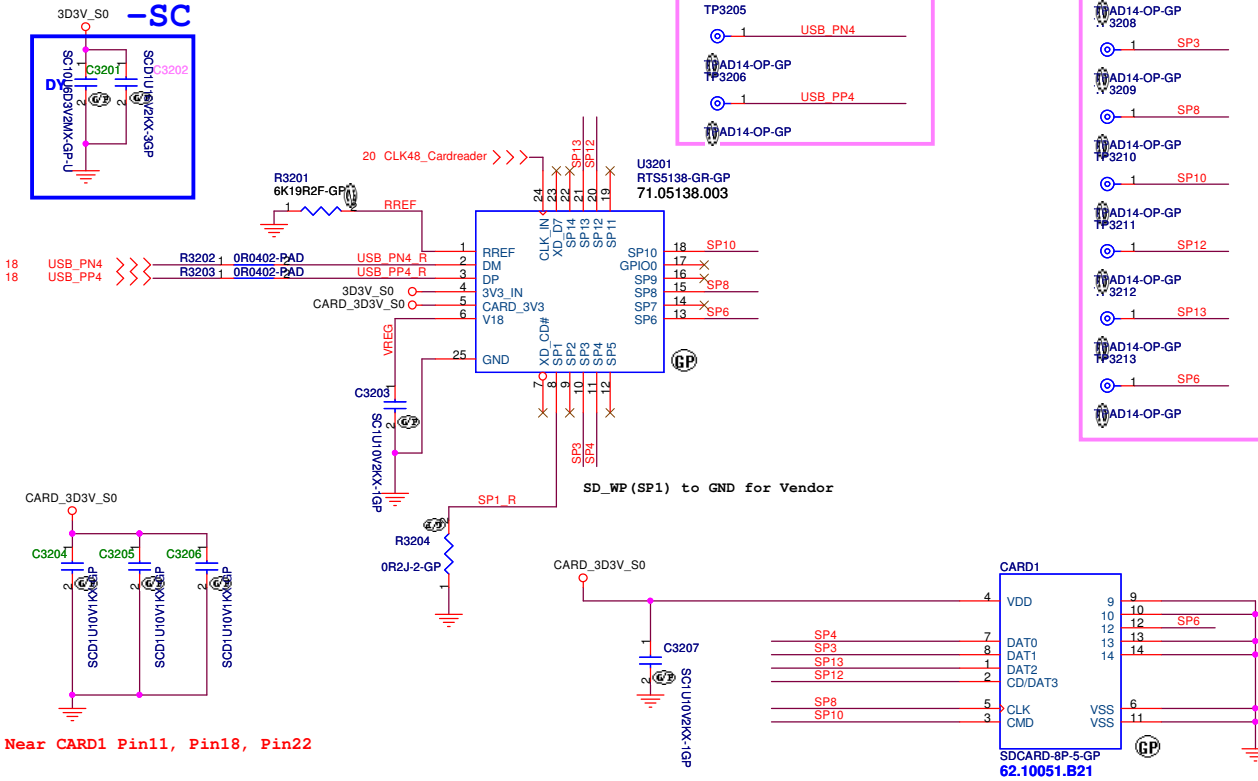
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Title			
AR8158			
Size	Document Number		Rev
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5 IN1 CARD-READER

For SIV, please near to u3201



please near to CARD1

Pin#	Name	I/O Type	Description
1	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	V18	O	Regulated supply voltage (1.8V ± 10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected
7	XD_CD#	I	xD Card Detect (xD_CD#)
8	SP1	I/O	xD Ready Signal (xD_RDY), SD Write Protect (SD_WP) and MS Clock (MS_CLK)
9	SP2	I/O	xD RE# and MS Card Detect (MS_INS#)
10	SP3	I/O	xD CE# and SD Data 1 (SD_DAT1)
11	SP4	I/O	xD_CLE, SD Data 0 (SD_DAT0) and MS Data 7 (MS_D7)
12	SP5	I/O	xD ALE, SD Data 7 (SD_DAT7) and MS Data 3 (MS_D3)
13	SP6	I/O	xD_WE# and SD Card Detect (SD_CD#)
14	SP7	I/O	xD Write Protect (xD_WP), SD Data 6 (SD_DAT6) and MS Data 6 (MS_D6)
15	SP8	I/O	xD Data 0 (xD_D0), SD Clock (SD_CLK) and MS Data 2 (MS_D2)
16	SP9	I/O	xD Data 1 (xD_D1), SD Data 5 (SD_D5) and MS Data 0 (MS_D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD_D2) and SD command signal (SD_CMD)
19	SP11	I/O	xD Data 3 (xD_D3), SD Data 4 (SD_DAT4) and MS Data 4 (MS_D4)
20	SP12	I/O	xD Data 4 (xD_D4), SD Data 3 (SD_DAT3) and MS Data 1 (MS_D1)
21	SP13	I/O	xD Data 5 (xD_D5), SD Data 2 (SD_DAT2) and MS Data 5 (MS_D5)
22	SP14	I/O	xD Data 6 (xD_D6) and MS BS
23	XD_D7	I/O	xD Data 7 (xD_D7)
24	CLK_IN	I	48MHz clock directly input

Helium		
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Title		
Reserved		
Size A3	Document Number Helium	Rev -1
Date: Thursday, August 23, 2012		
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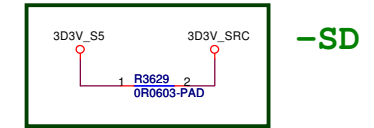
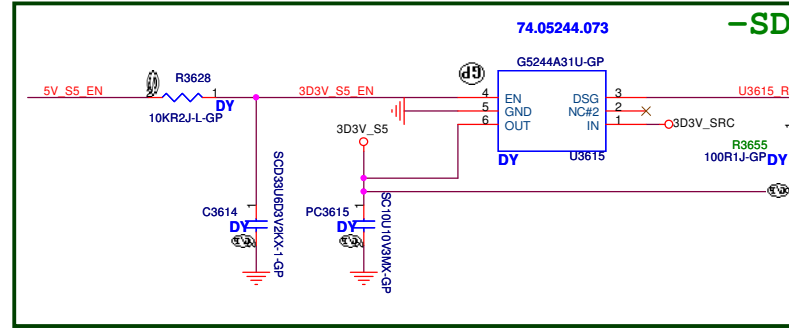
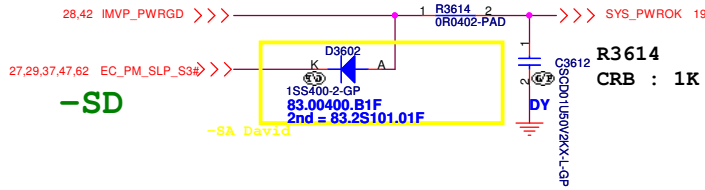
Helium

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 34 of 103

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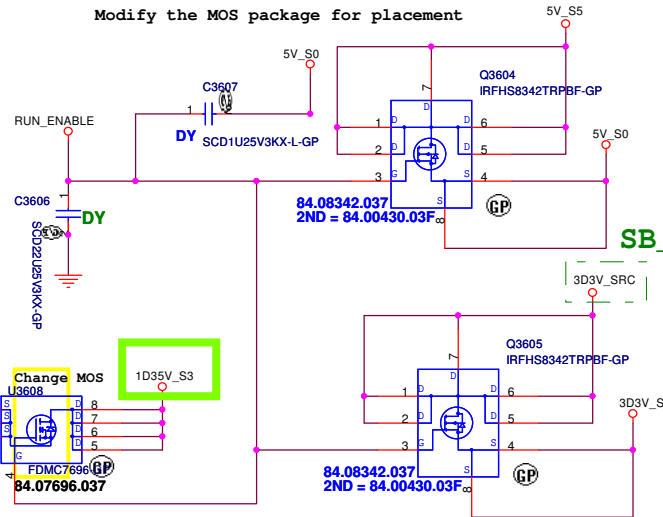
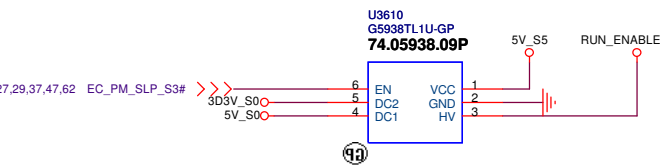
Power Sequence

SB_20120117_IOAC

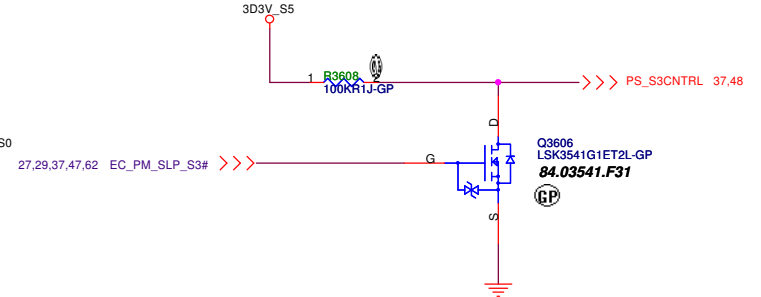


ANNIE Run Power

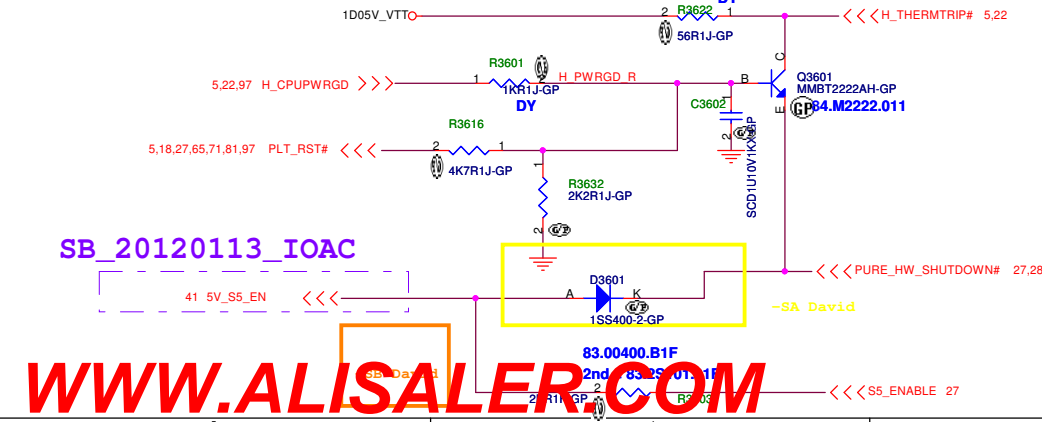
Modify the MOS package for placement



SB_20120117_IOAC

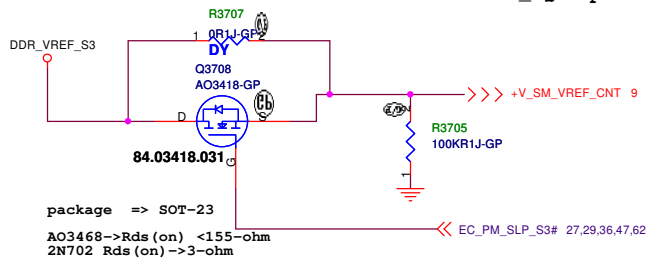


SB_20120113_IOAC

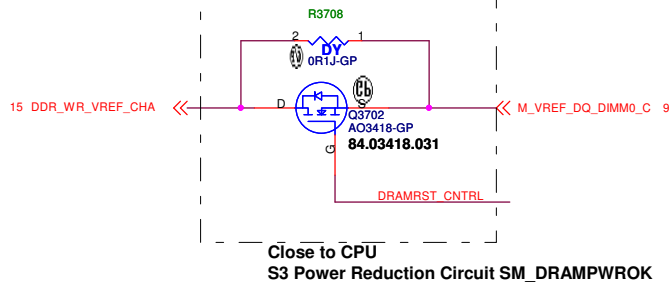


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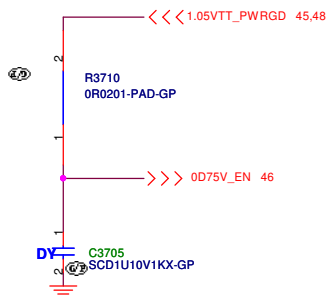
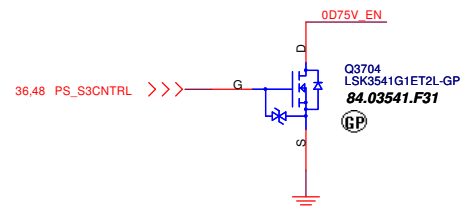
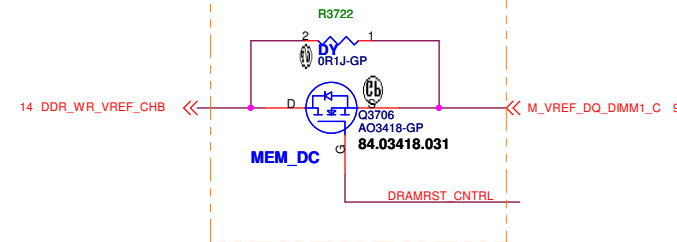
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



M3 power



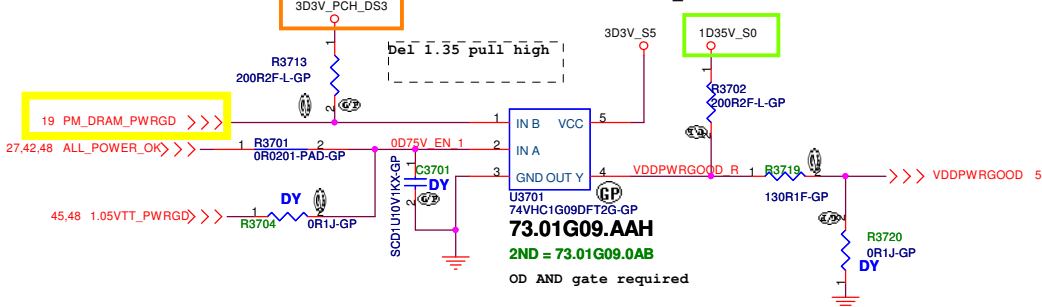
M3 power



For Leakage concern

-SB

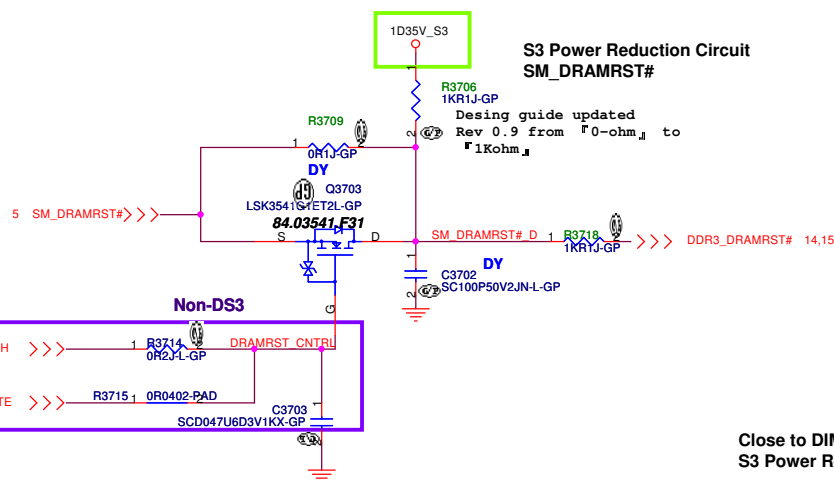
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



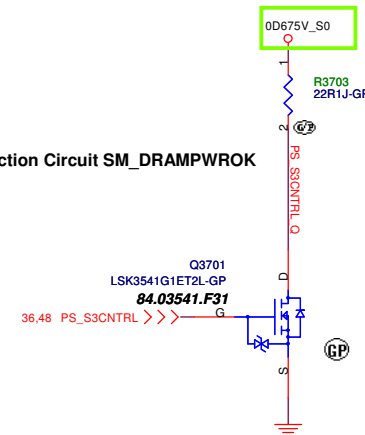
For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ 1.0-55±200mV and the edge must be monotonic

S3 Power Reduction Circuit
SM_DRAMPWROK



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Helium

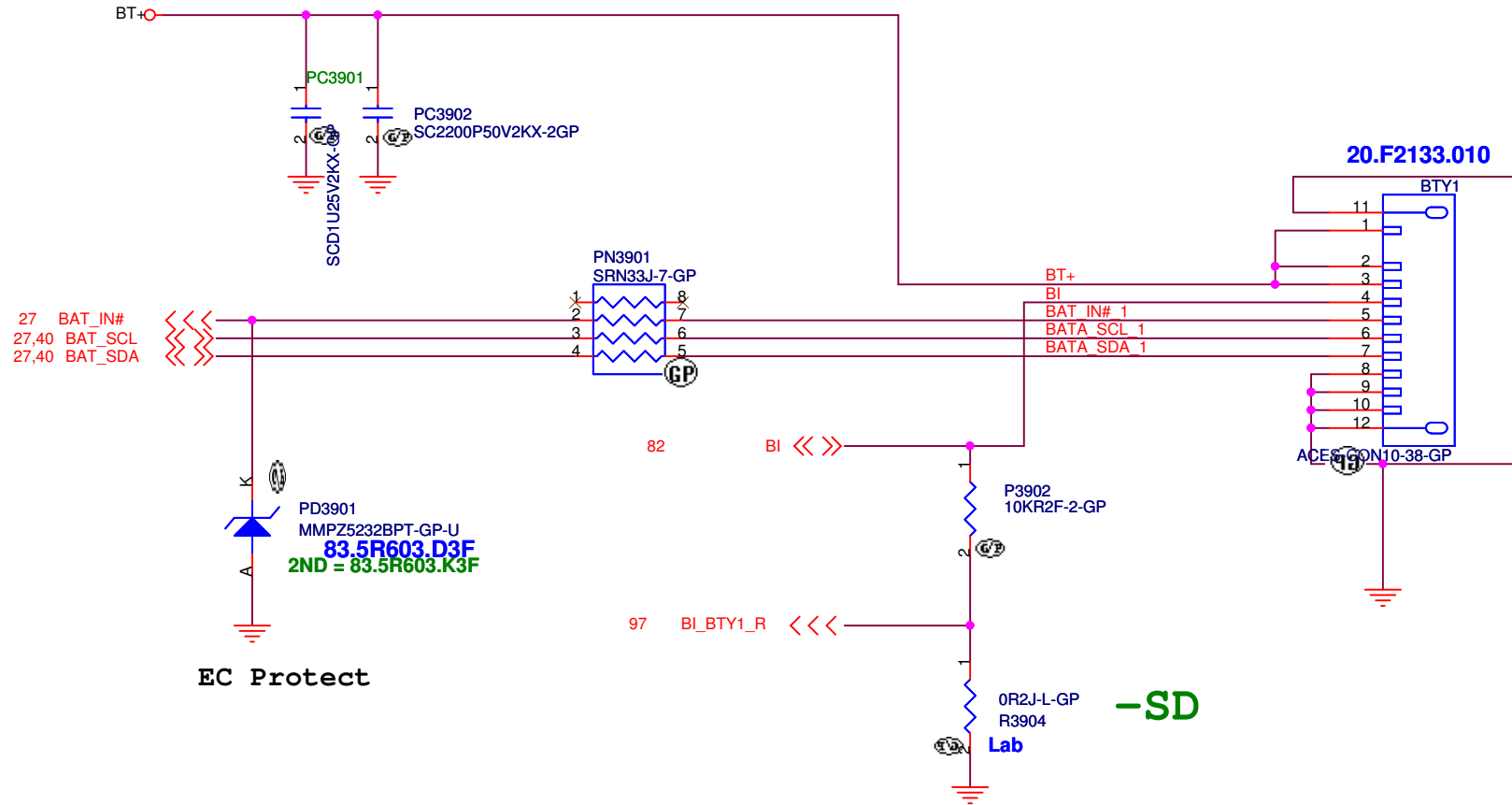
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Title			ADAPTER
Size	Document Number	Rev	
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1

BATTERY CONNECTOR



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Title

BATT CONN

Size
A4

Document Number

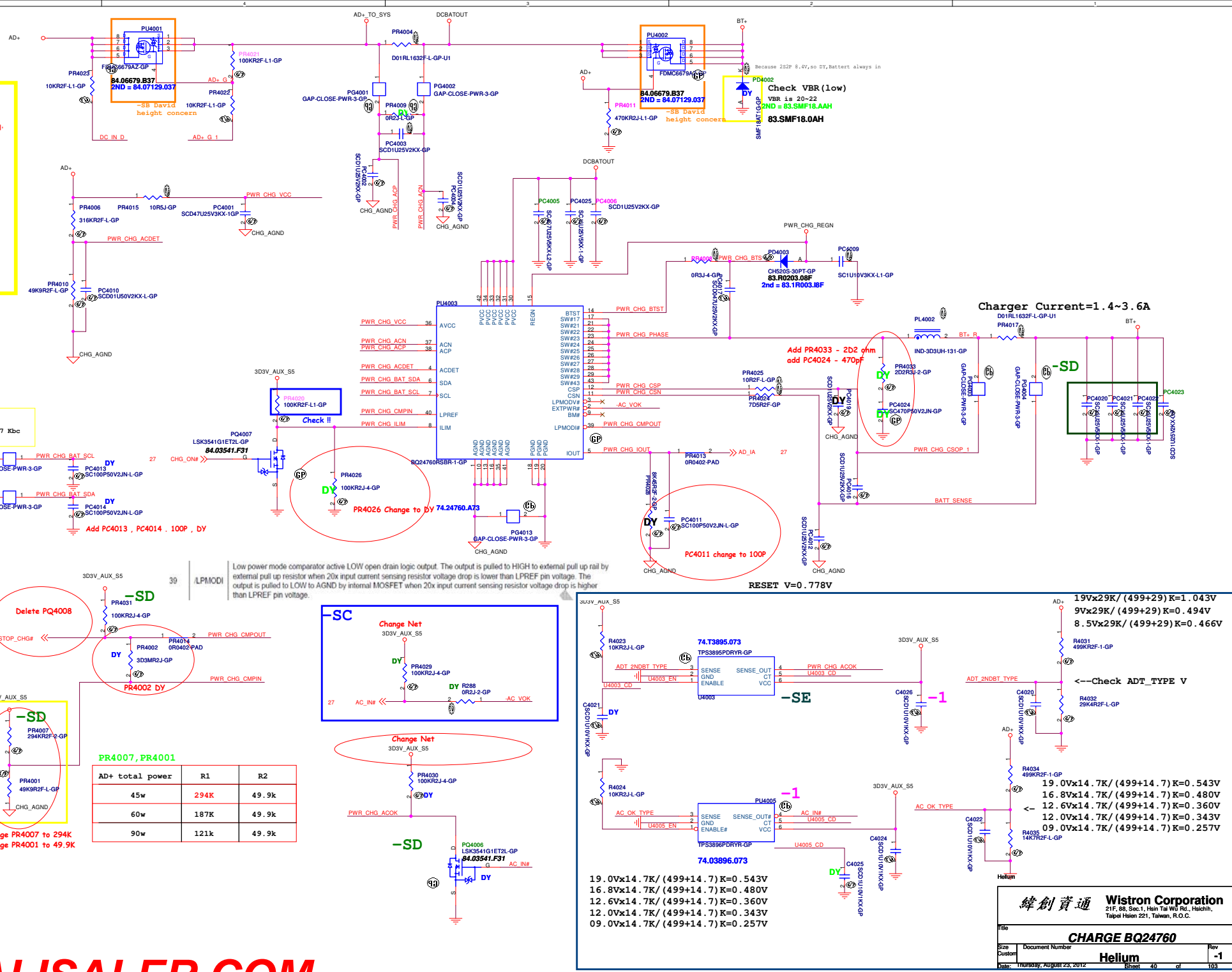
Helium

Rev
-1

Date: Thursday, August 23, 2012

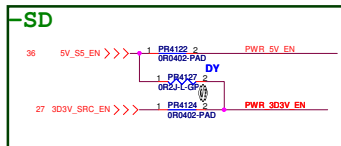
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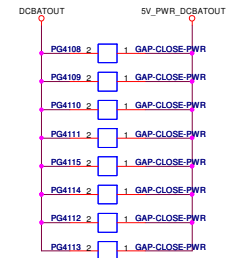
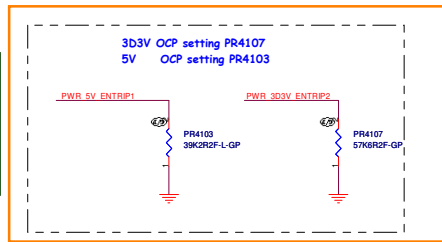


SSID = PWR.Plane.Regulator_3p3v5v

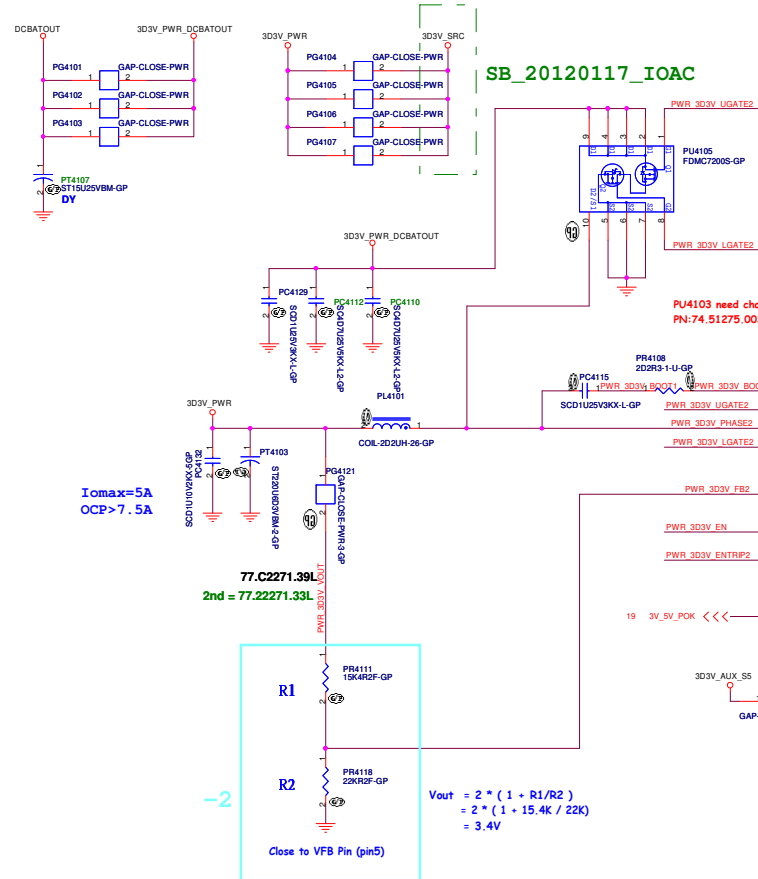
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-SB David

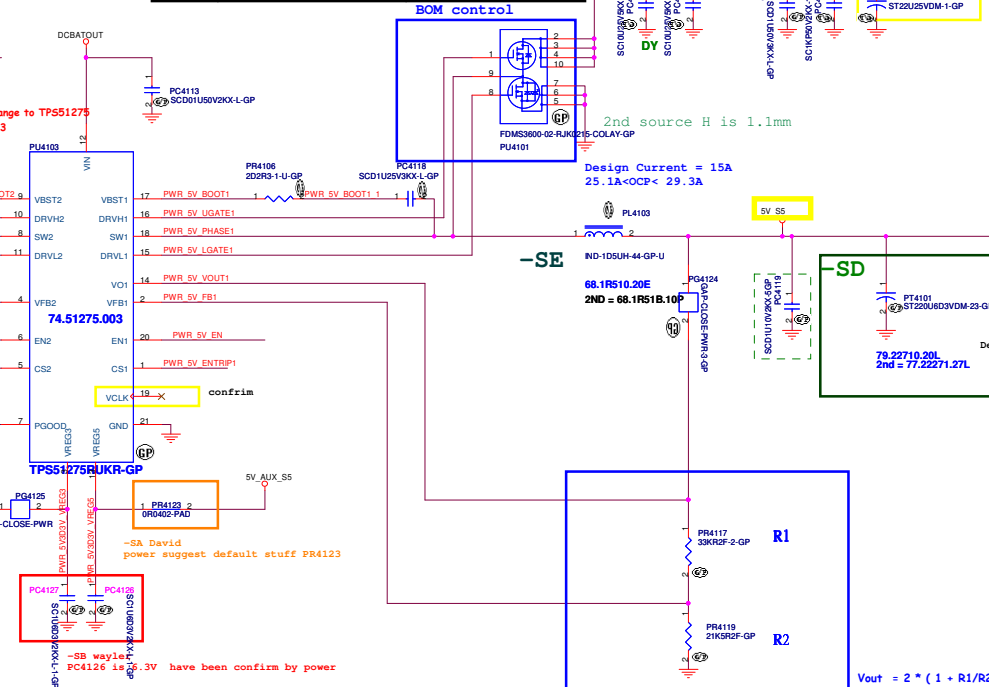


SB_20120117_IOAC



	Main source	2nd source
PU4101	84.03664.037 (FDM3664S)	84.00038.A37 (RJK03P8DPA)

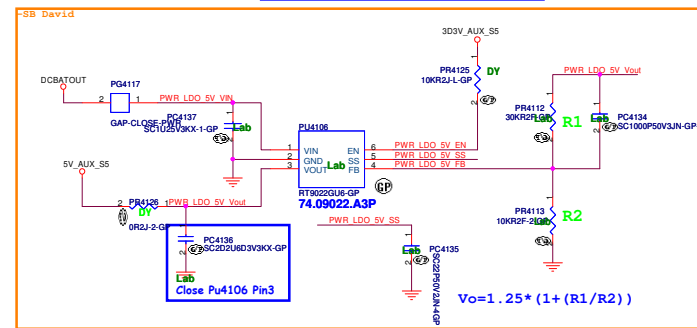
BOM control



DEL OUTPUT GAP

Delete

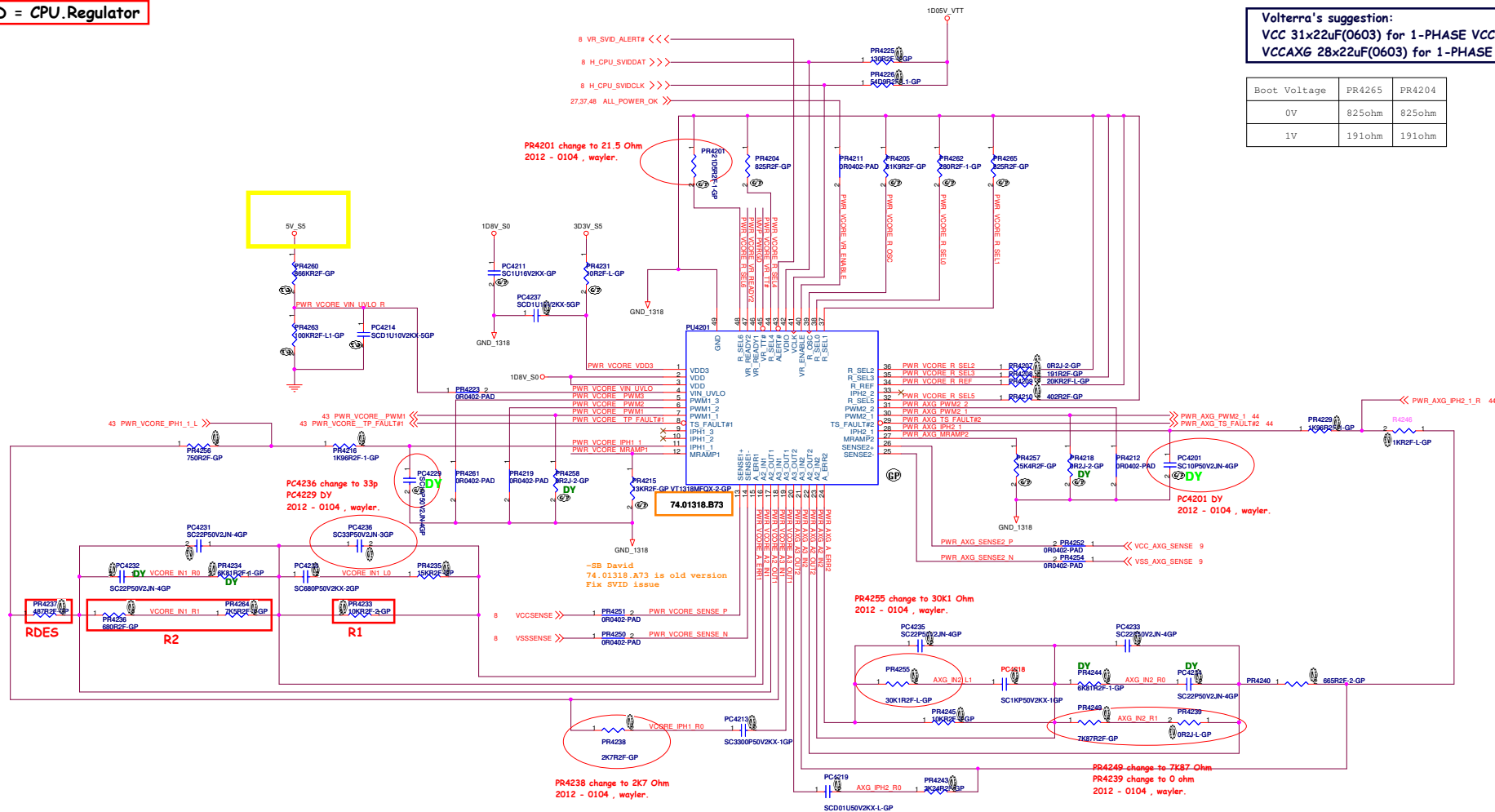
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SSID = CPU.Regulator

Volterra's suggestion:
VCC 31x22uF(0603) for 1-PHASE VCC
VCCAXG 28x22uF(0603) for 1-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	825ohm	825ohm
1V	191ohm	191ohm

Table 1: R_{DES} Selection Table

N _{PH}	I _{CCMAX} (Å)	I _{LIM} (Å)	P _{DES} (%)
1	20	24	1180
1	24	32	976
1	28	36	845
1	32	45	732
1	36	45	649
1	40	56	590
1	44	56	536
1	48	64	487
2	40	48	590
2	48	64	976
2	56	72	845
2	64	80	732
2	72	96	649
2	80	104	590
2	88	112	536
2	96	128	487
3	60	72	787
3	72	96	787
3	84	108	665
3	96	120	590
3	108	144	523
3	120	156	475
3	132	168	432
3	144	192	392

R₁ and R₂ Selection

Along with R_{DES} , The values of R_1 and R_2 determine the load line according to Equation 4.

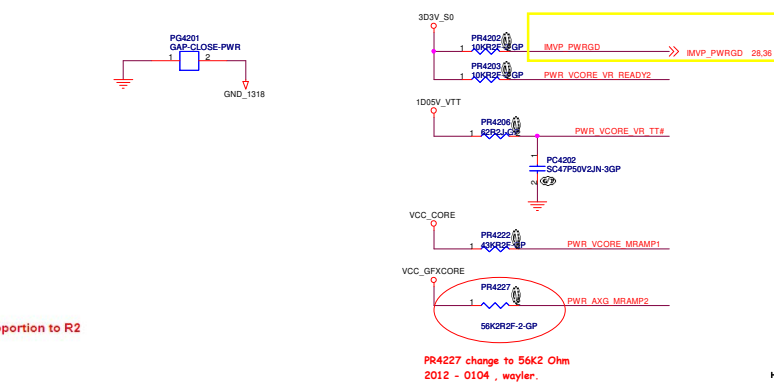
Equation 4

$$R_{LL}[\Omega] = \frac{R_1}{R_2} \cdot \frac{1}{2.2} \cdot R_{DES} \cdot \frac{1}{K_f}$$

→ RLL is inverse proportion to R2

 $K_i = 95000$

With K_I being the slave current feedback gain and R_1 having a typical value of $10k\Omega$. Next, the required value of R_2 can be calculated to achieve the desired load line via Equation 4 and previously selected values for R_1 and R_{DES} .

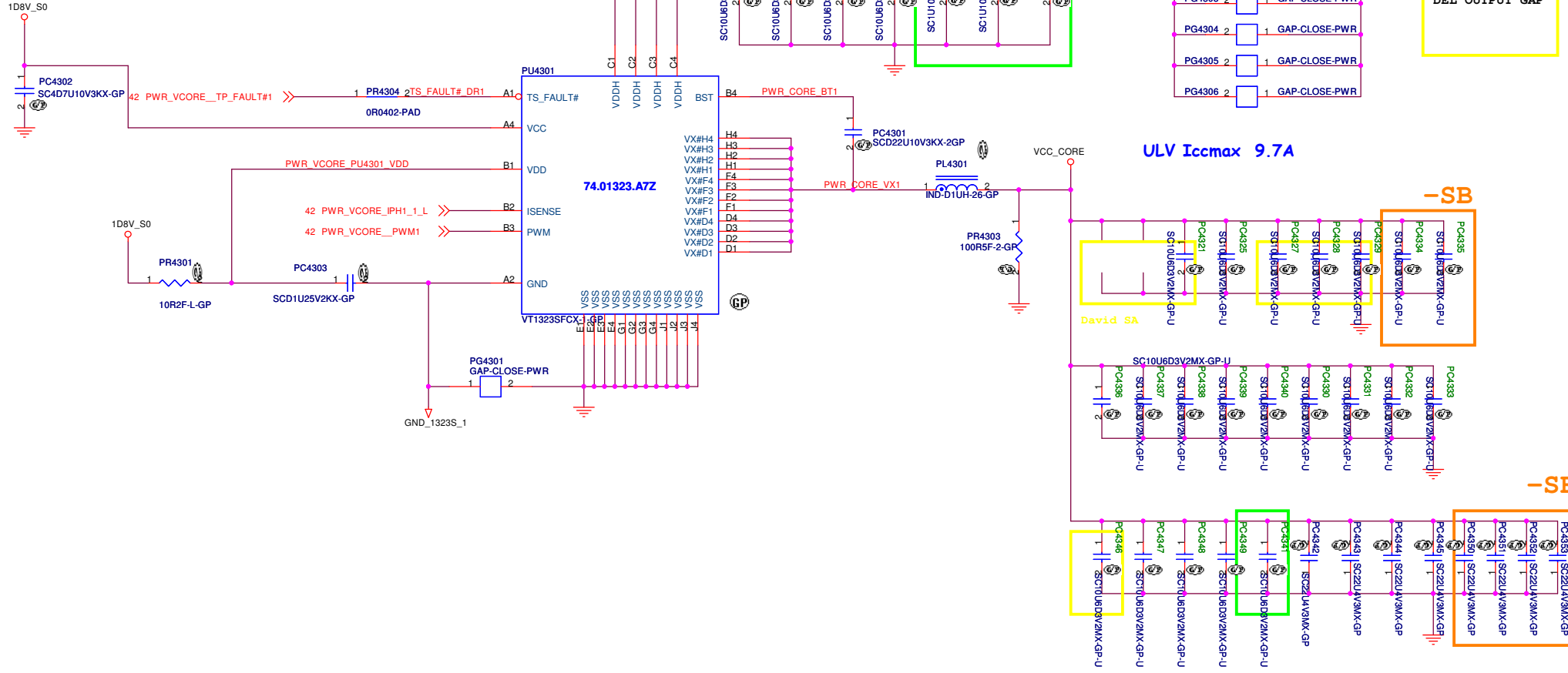


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Title	VT1318+1323_CPU_CORE2+1(1/3)
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Size	Document Number	Rev
	Helium	-1



Delete the old version VT386F circuit

140mils or Copper Shape

DEL OUTPUT GAP

400mils or Copper Shape

Design Current = 12A
OCP > 19.5A

Change to 0603_4V

**VSENSE-TRACE
ROUTED DIFFERENTIALLY
PARALLEL TO VSENSE+**

close output MLCC

close output MLCC

Change OR PAD to OR and DY

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Title

VT386 +1.05V VTT

Size

Document M

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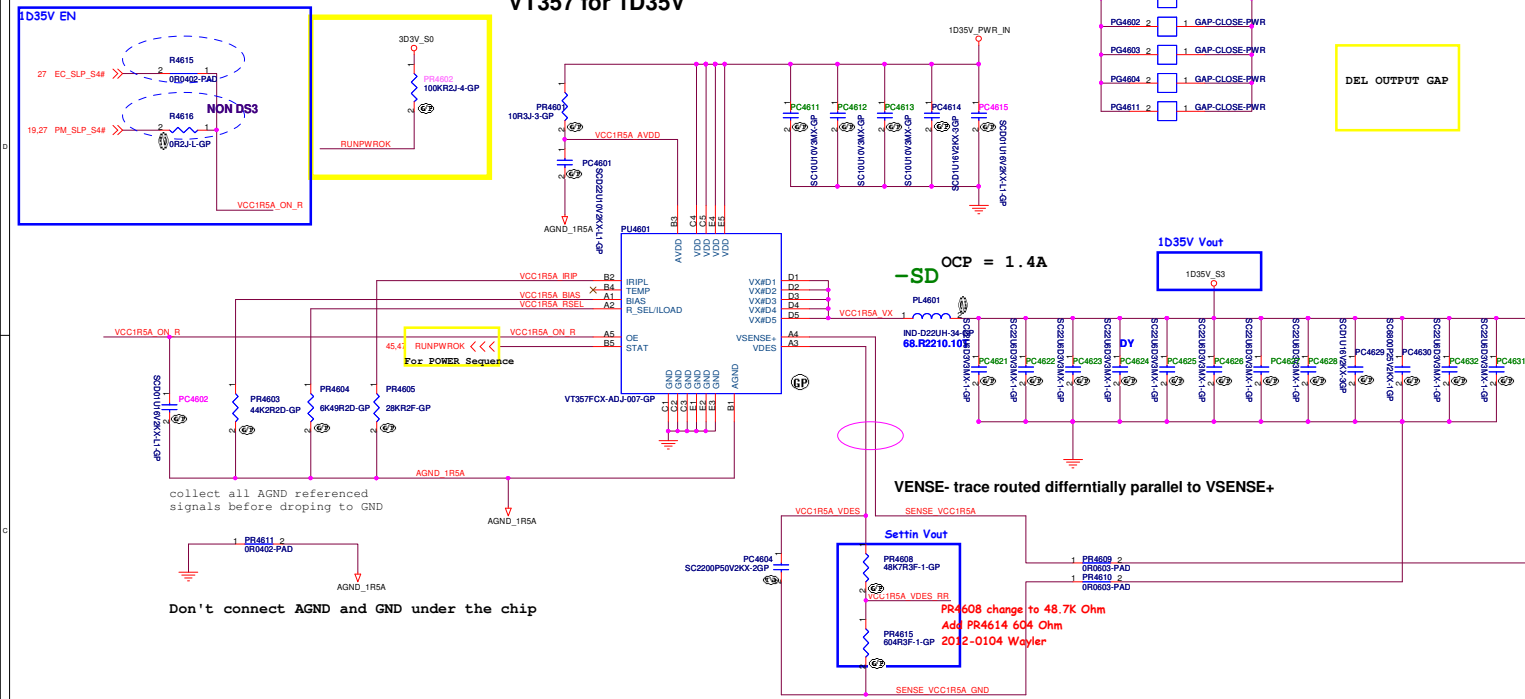
Date: Thursday, August 23, 2012

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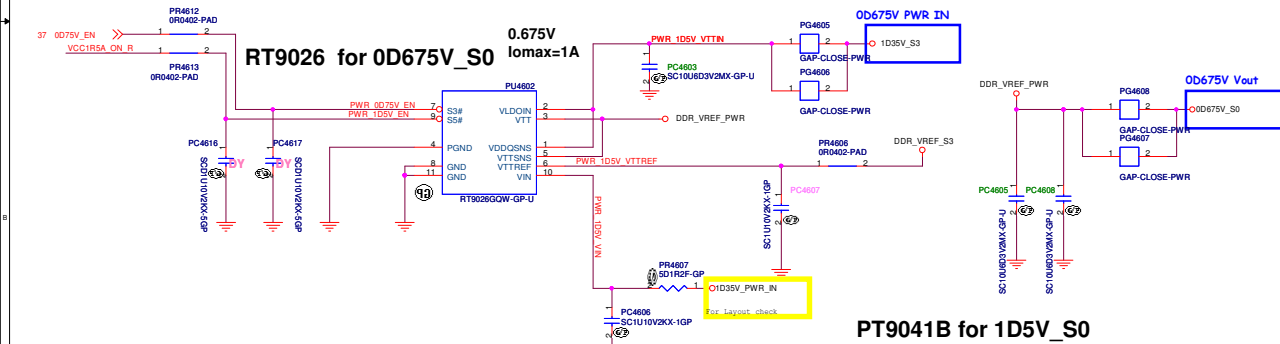
Rev

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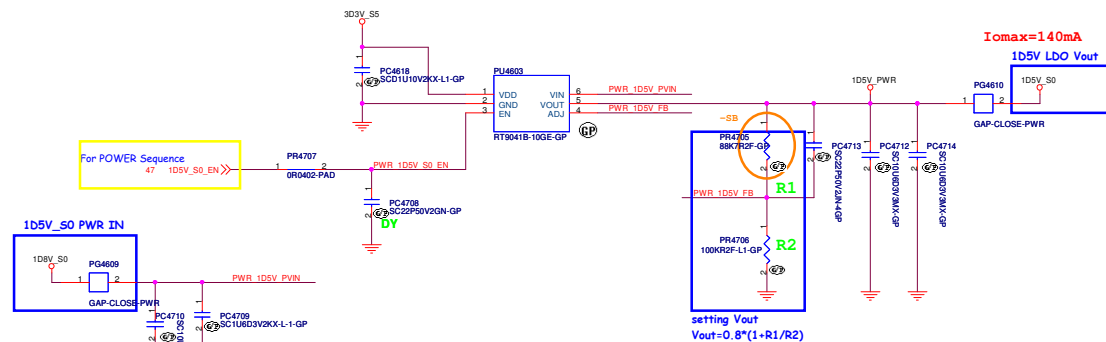
VT357 for 1D35V

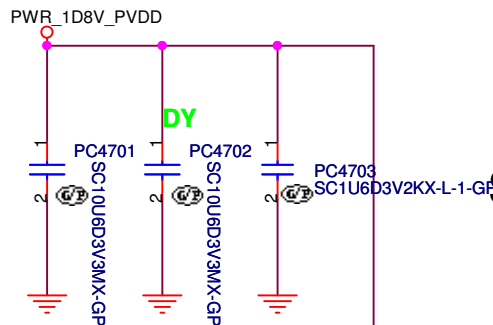


RT9026 for 0D675V_SC

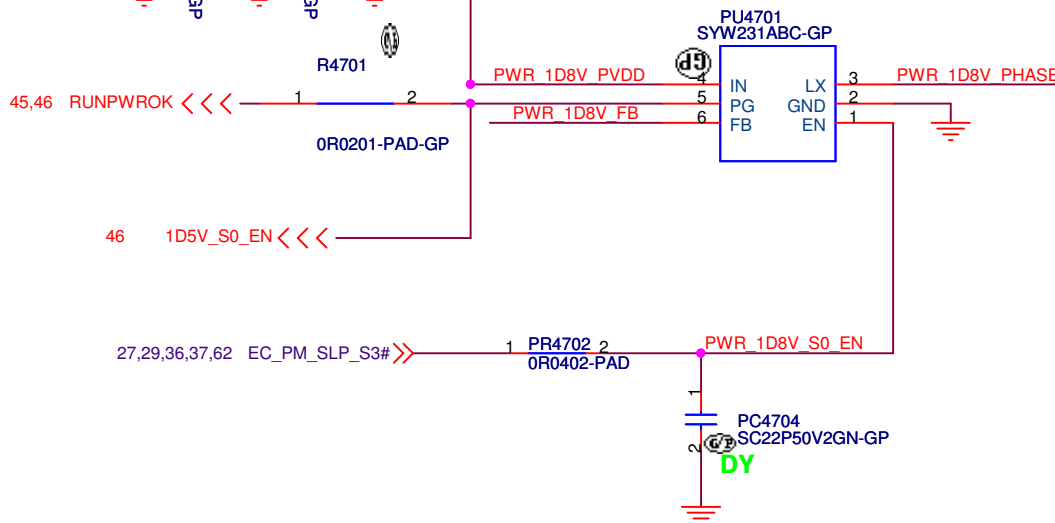


PT9041B for 1D5V_S0



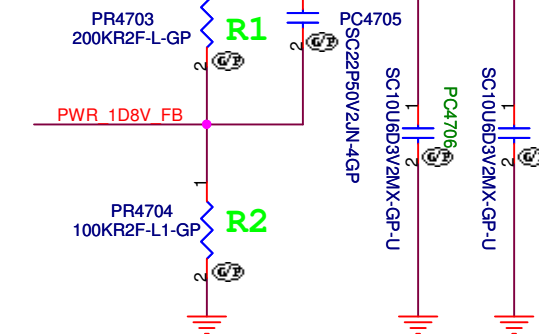
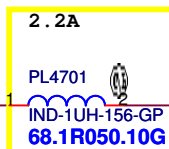


SYW231 for 1D8V_S0



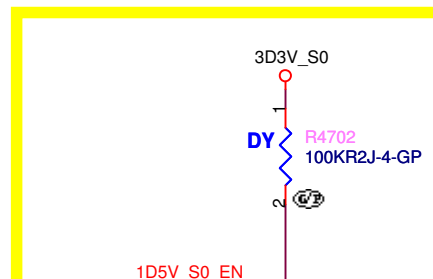
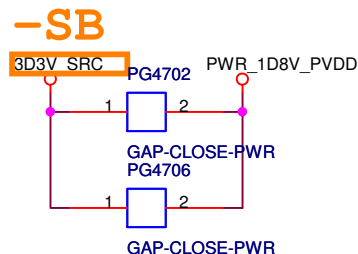
DEL OUTPUT GAP

$I_{omax}=1.242A$
 $OCP>5A$



$$V_o = 0.6 * (1 + (R1/R2))$$

For layout concern



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Title

1D8V_S0 SYW231

Size
A4

Document Number

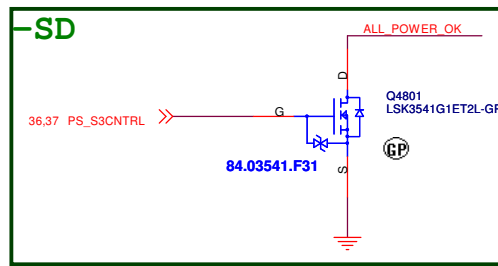
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Rev
-1

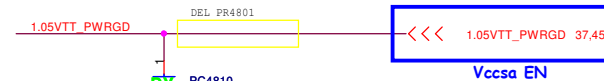
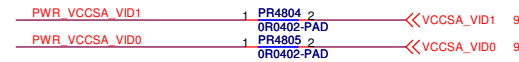
Date: Thursday, August 23, 2012

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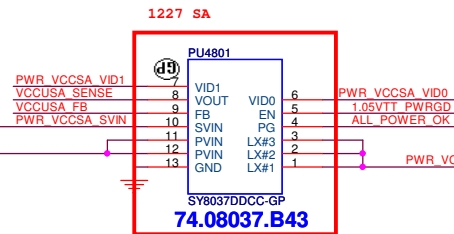
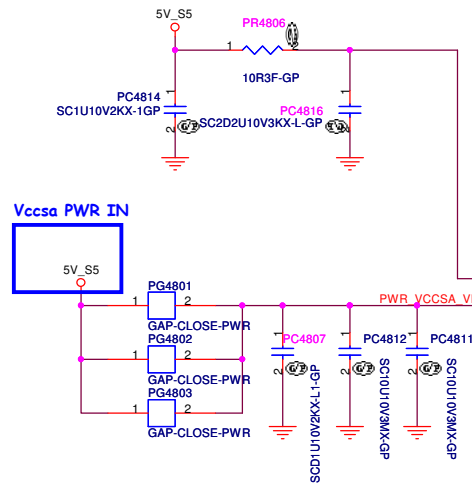
SY8037 for VCCSA



VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

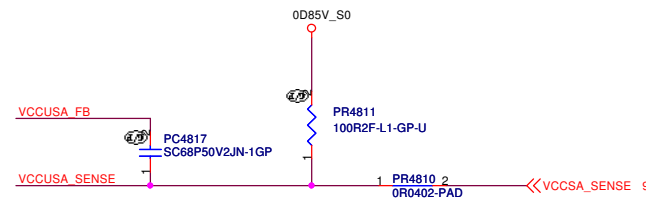
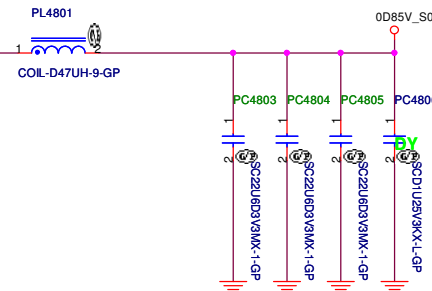


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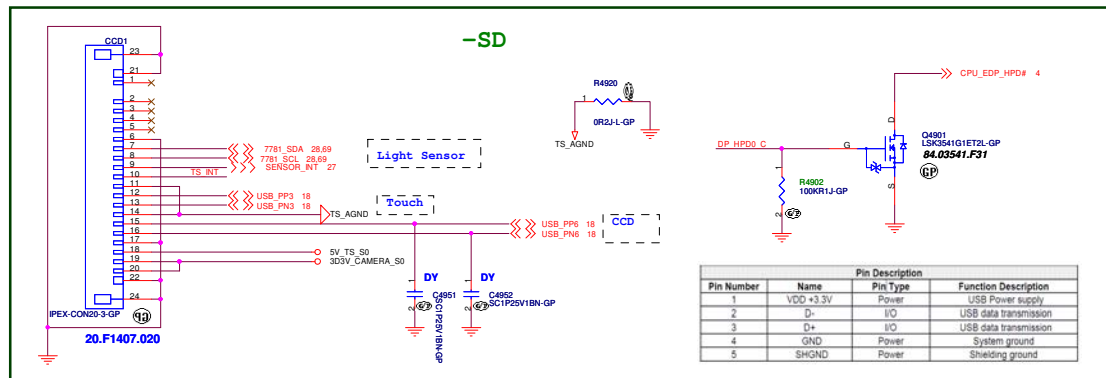
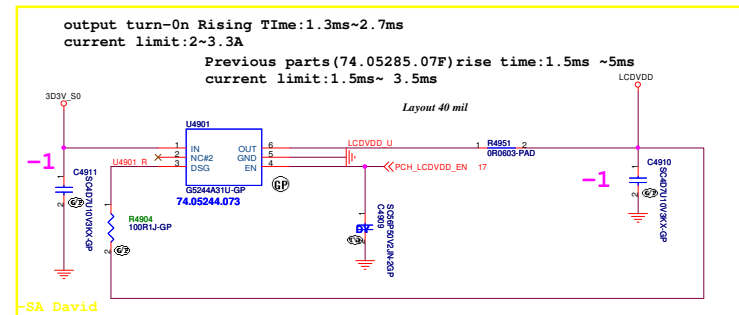
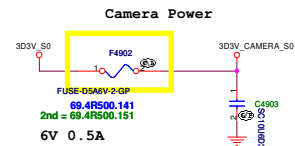
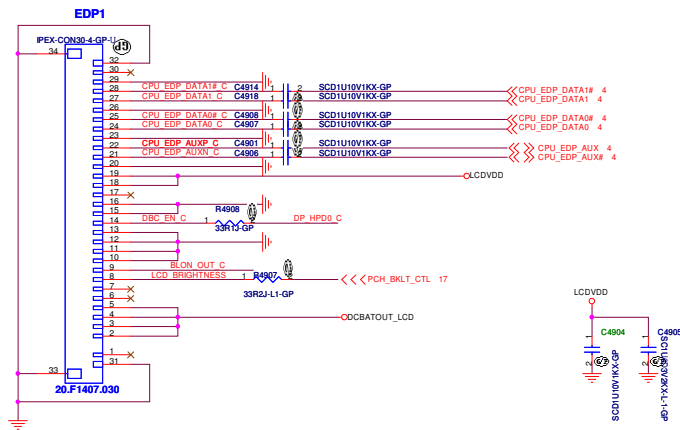


CYNTEC - PCMB042T-R47MS
package : 4.15 * 4 * 1.8
ID 7 A ~ 9.5A
DCR = 12.5 ~ 14mOhm

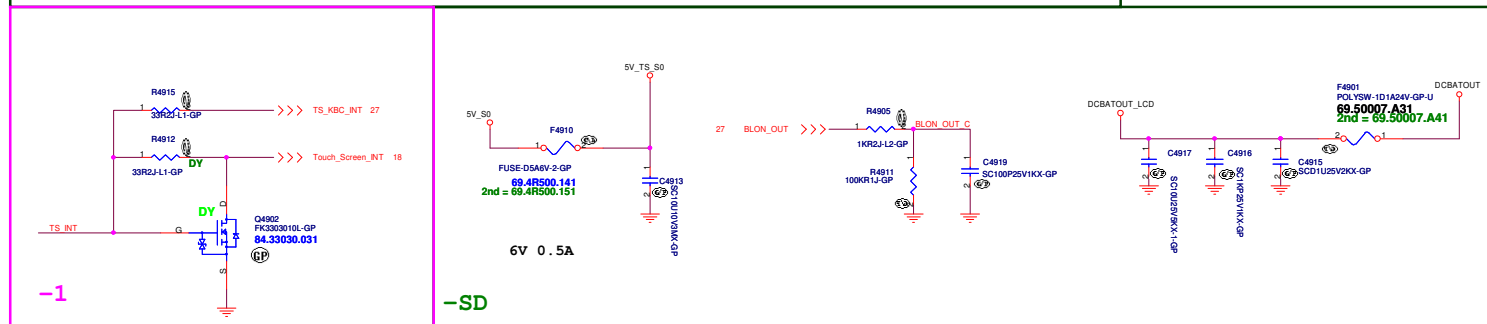
Design Current = 4 A
6.6A < OCP < 7.8A



EDP CONNECTOR



Pin Description			
Pin Number	Name	Pin Type	Function Description
1	VDD +3.3V	Power	USB Power supply
2	D-	I/O	USB data transmission
3	D+	I/O	USB data transmission
4	GND	Power	System ground
5	SHGND	Power	Shielding ground



Pull High 5V Design on CRT Board
CRT DDCDATA & DDCCLK level shift

Helium

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Connector			
Size	Document Number		Rev
A3	Helium		-1
Date:	Thursday, August 23, 2012		Sheet 50 of 103

SSID = VIDEO

HDMI Level Shifter

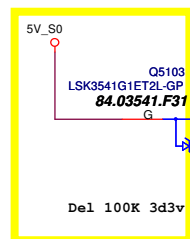
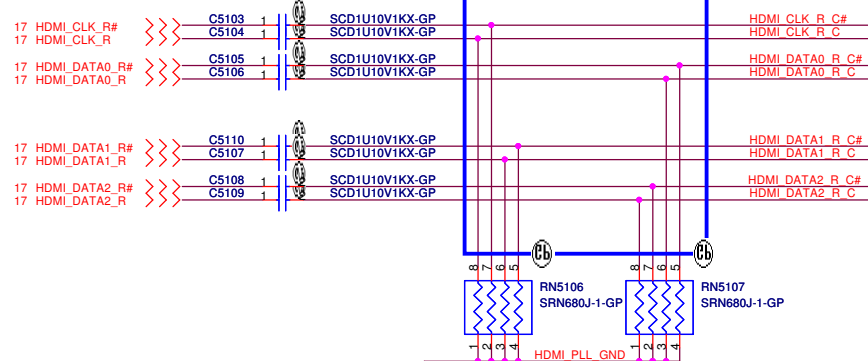
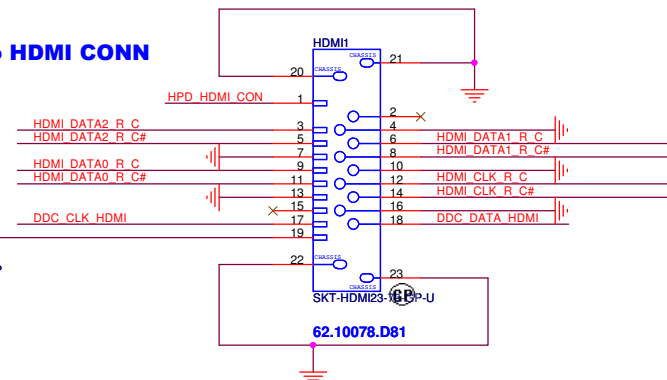
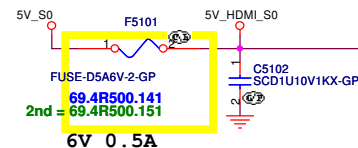


Table 4-5 Type D Connector Pin Assignment

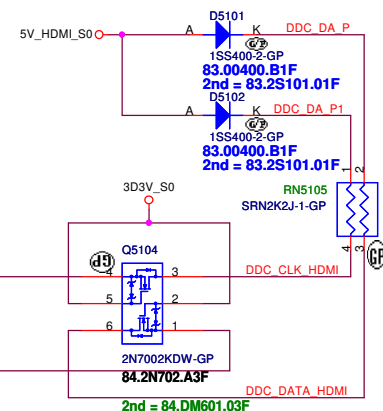
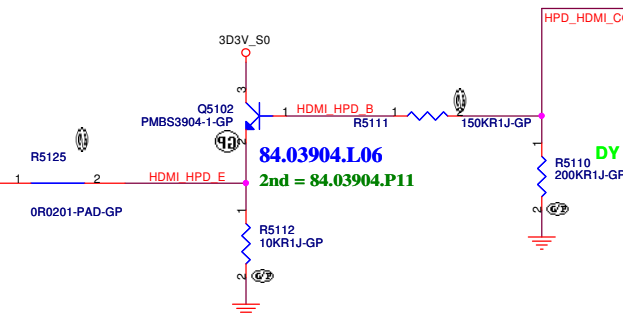
PIN	Signal Assignment
1	Hot Plug Detect
3	TMDS Data2+
5	TMDS Data2-
7	TMDS Data1 Shield
9	TMDS Data0+
11	TMDS Data0-
13	TMDS Clock Shield
15	CEC
17	SCL
19	+5V Power

PIN	Signal Assignment
2	Utility
4	TMDS Data2 Shield
6	TMDS Data1+
8	TMDS Data1-
10	TMDS Data0 Shield
12	TMDS Clock+
14	TMDS Clock-
16	DDC/CEC Ground
18	SDA

Micro HDMI CONN



7 HDMI_PCH_DET <<<



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Title HDMI Level Shifter/Conn
 Size A3 Document Number Helium Rev -1
 Date Thursday, August 23, 2012 Sheet 51 of 103

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Title

Size
A3

Document Number
Helium

Date: Thursday, August 23, 2012

eDP

Rev
-1

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(Blanking)

Helium		
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Title		
S-VIDEO		
Size	Document Number	Rev
A4	Helium	-1
Date: Thursday, August 23, 2012		Sheet 53 of 103

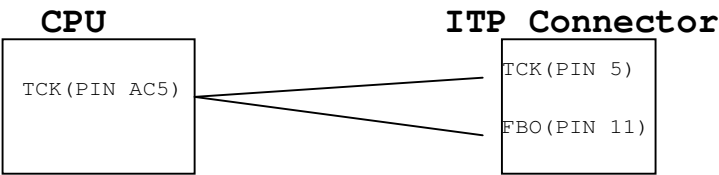
(Blanking)

Helium		
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 54 of 103

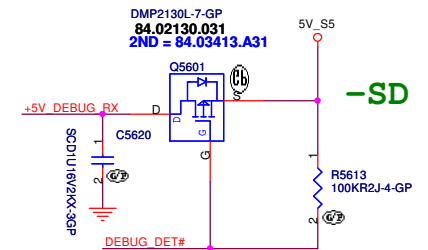
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



MSATA Connector

[illegible]

Chip test mode enable, internally pulled down at ~150KΩ
L: Normal operation
H: Test mode enable
For SATA/SAS PHY test, this pin should be pulled to High

9,19	A_PRE0 A_PRE1	I	<p>Programmable output pre-emphasis level setting for channel A</p> <p>3.3V tolerant. Internally pulled down at ~150KΩ</p> <p>[A_PRE1, A_PRE0] ==</p> <p>LL: 0dB, no pre-emphasis</p> <p>VL: 1.5dB pre-emphasis is selected</p> <p>HL: 2.5dB pre-emphasis is selected</p> <p>HH: 3.5dB pre-emphasis is selected</p>
0,17	B_PRE0 B_PRE1	I	<p>Programmable output pre-emphasis level setting for channel B</p> <p>3.3V tolerant. Internally pulled down at ~150KΩ</p> <p>[B_PRE1, B_PRE0] ==</p> <p>LL: 0dB, no pre-emphasis</p> <p>VL: 1.5dB pre-emphasis is selected</p> <p>HL: 2.5dB pre-emphasis is selected</p> <p>HH: 3.5dB pre-emphasis is selected</p>

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ESATA Power

USB CHARGER

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Title

E-SATA/USB CHARGER

Size
A3

Document Number
Helium

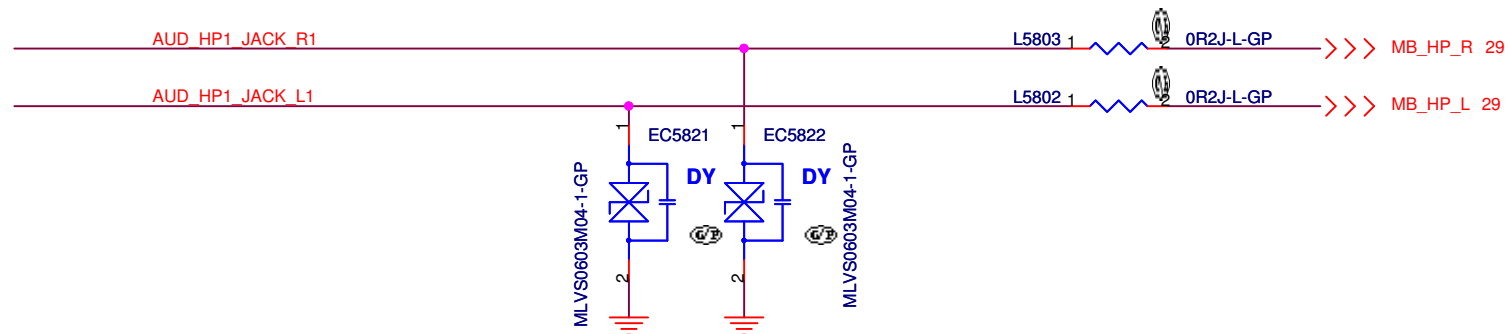
Date: Thursday, August 23, 2012

Rev
-1

Sheet 57 of 103

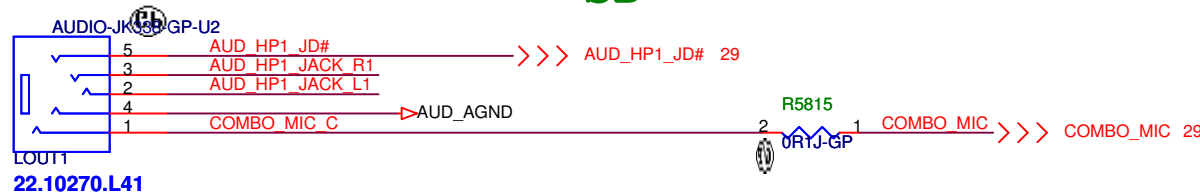
SSID = AUDIO

LINE OUT

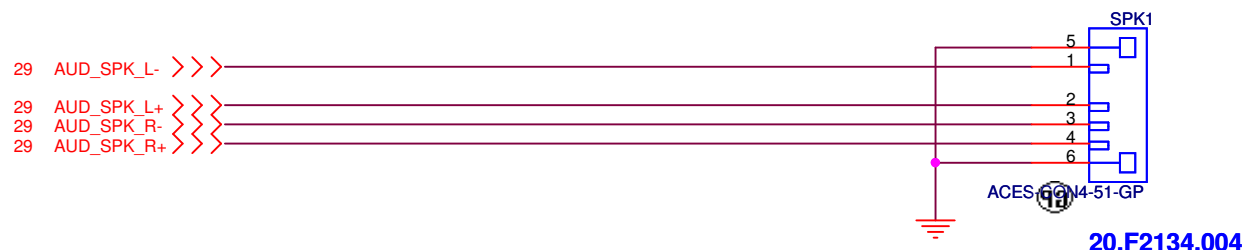


U2版的~!!!

-SD



Speaker Connector



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Title

Audio Jack

Size
A4

Document Number

Helium

Rev
-1

Date: Thursday, August 23, 2012

Sheet 58 of 103

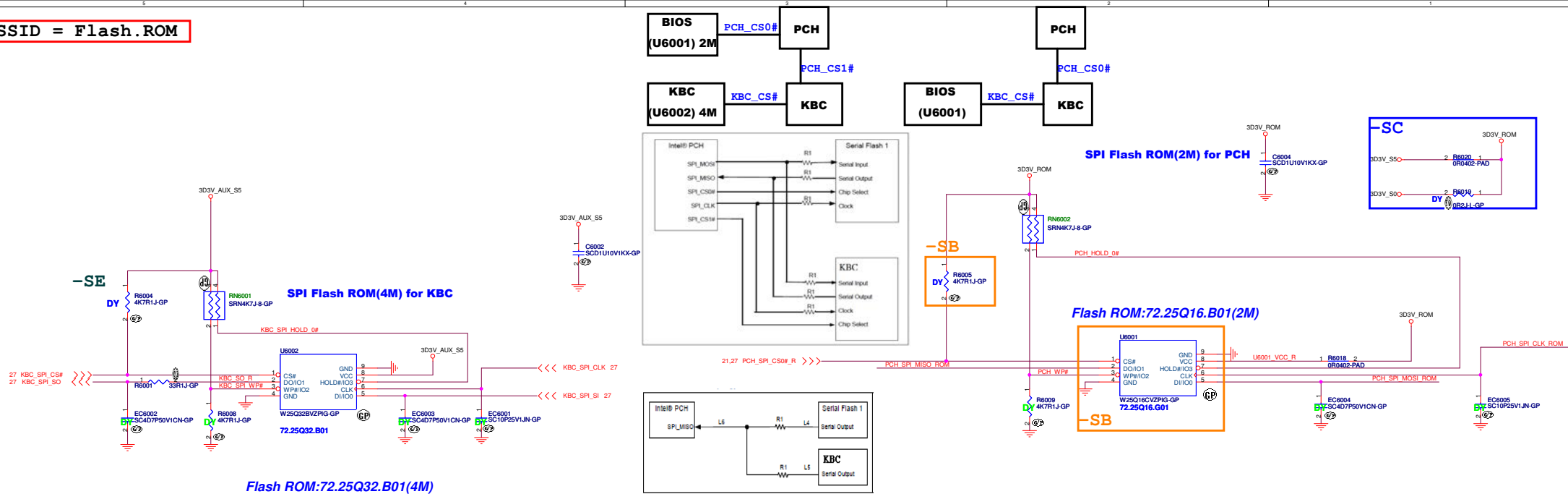
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

Without LAN

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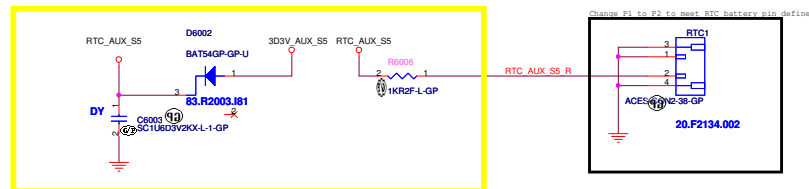
Helium		
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
LAN CONNECTOR		
Size	Document Number	Rev
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Date: Thursday, August 23, 2012		Sheet 59 of 103

```
SSID = Flash.ROM
```

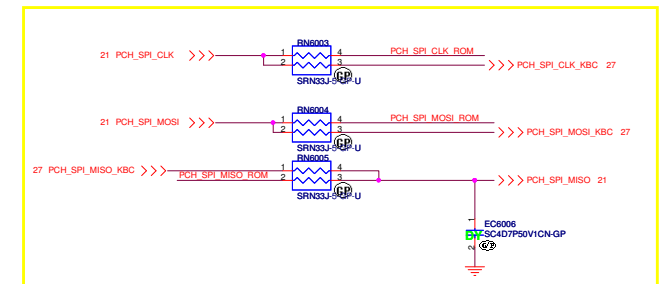


SSID = RBATT

-SB David(layout placement concern)



RTC battery charger circuit



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Title			
Flash(KBC+PCH)/RTC			
Size Custom	Document Number		Rev
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SSID = USB

Change Main source
Support 2.45A

U6101
SY6288CCAC-GP
74.06288.079
2ND = 74.02001.079

at least 80 mil

62 USB_PWR_EN_R >>>

H active

at least 80 mil

Right ON MB

Change Main source
Support 2.45A

U6102
SY6288DCAC-GP
74.06288.A79
2nd 74.02000.B71

at least 80 mil

27,62 USB_PWR_EN >>>

L active

at least 80 mil

Left ON MB

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Title

USB Power SW

Size
A4

Document Number

Helium

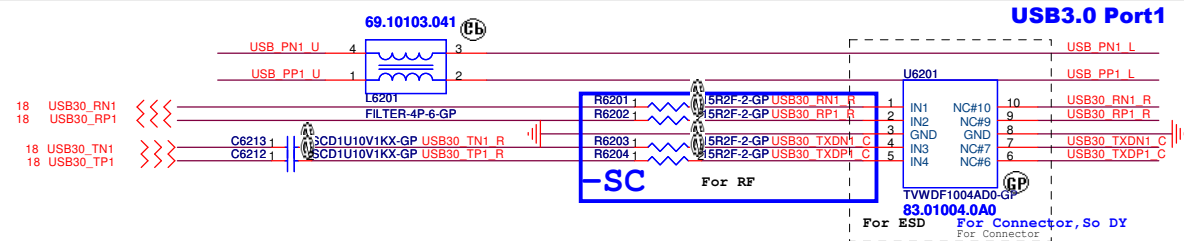
Rev

-1

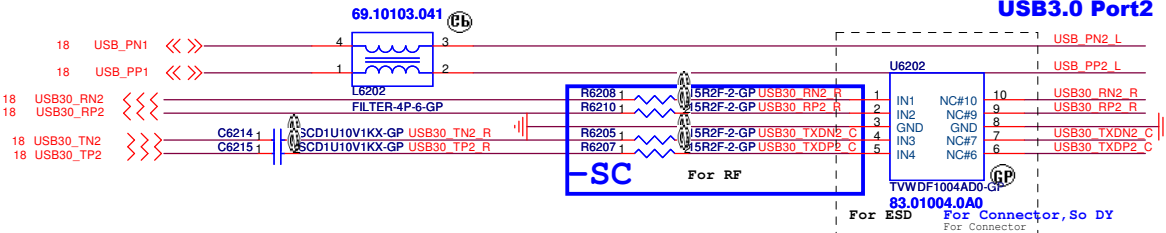
Date: Thursday, August 23, 2012

Sheet 61 of 103

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USB3.0 Port1

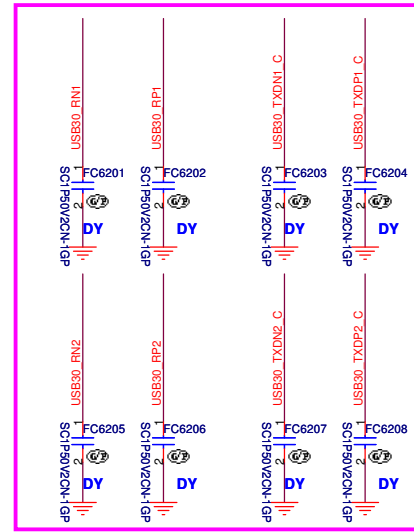


USB3.0 Port2

JE40 modify

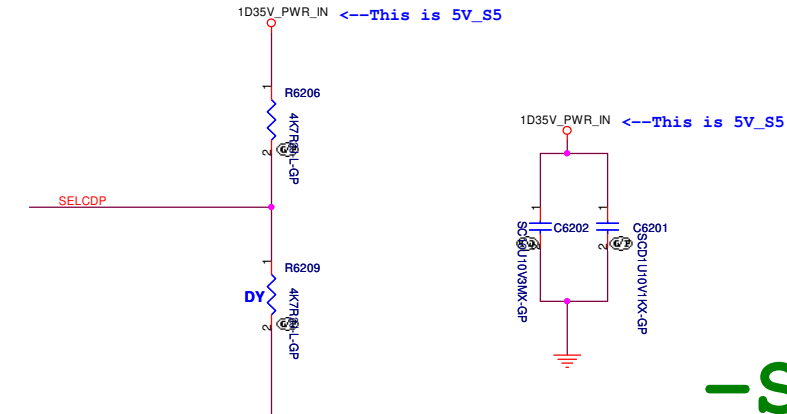
USB 3.0 Connector
Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

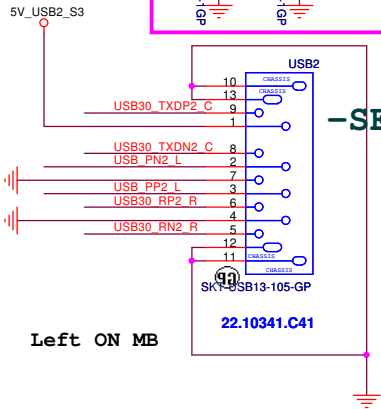


-1

-1

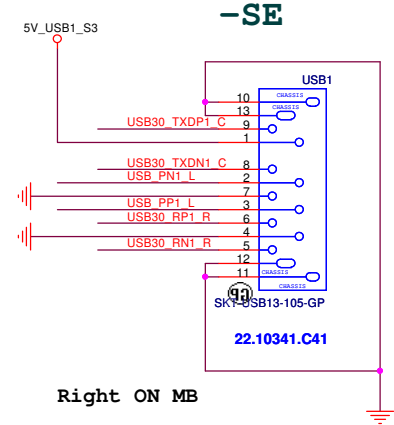


-SD



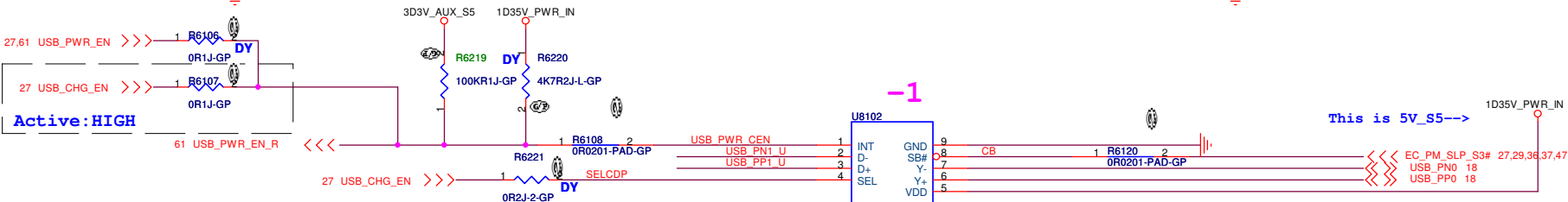
Left ON MB

-SE



Right ON MB

-SE



-1

This is 5V_S5-->

Pin Description - SLG55583A

Pin #	Name	Type	Description
1	CEN	Output	N-FET Open Drain Output. Current Limit Switch (CLS) Control Output. CB changes from 0 to 1 or 1 to 0. CEN will be low for 2 seconds (typ)
2	DM	Input/Output	USB Connector D-
3	DP	Input/Output	USB Connector D+
4	SMART-CDP	Input	Input Control logic (see truth table)
5	VDD	PWR	Power Supply. Connect a 0.1μF capacitor between VDD and GND as close as possible to the device.
6	TDP	Input/Output	Host USB Transceiver D+ Connection
7	TDM	Input/Output	Host USB Transceiver D- Connection
8	CB	Input	Switch Control Bit 0 = autodetection charger identification active 1 = charging down area (not with active USB 2.0 data communication)
9	Internal	NC	Internal

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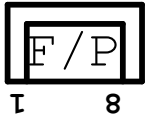
Title	USB 3.0 Port	
Size A3	Document Number	Rev
Date: Thursday, August 23, 2012	Helium	-1
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SSID = User.Interface
Bluetooth Module conn.

Without BT

Finger printer

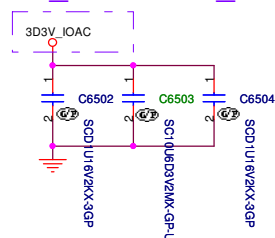
JE40 delete FP function



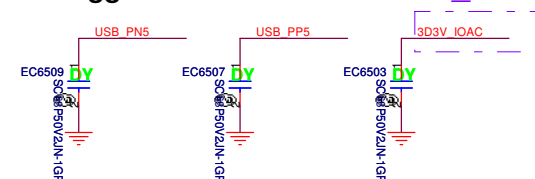
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

SB_20120113_IOAC

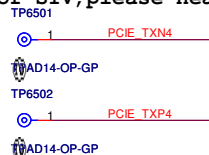


RF suggestion

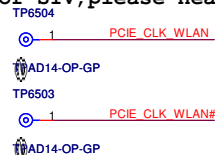


SB_20120113_IOAC

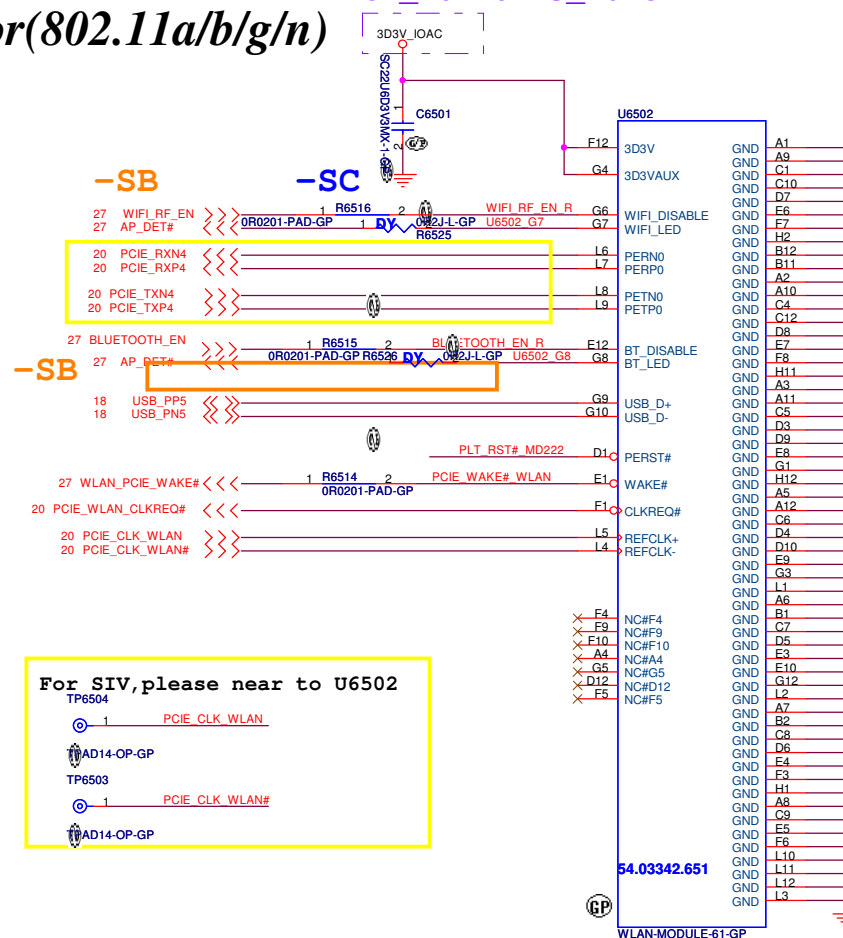
For SIV, please near to U6502



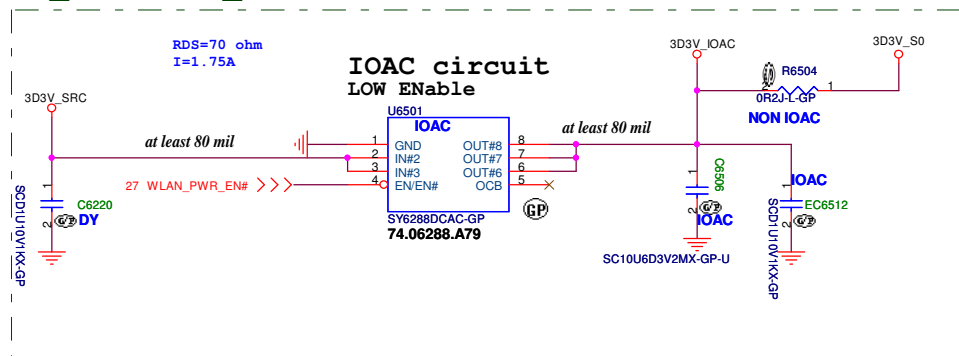
For SIV, please near to U6502



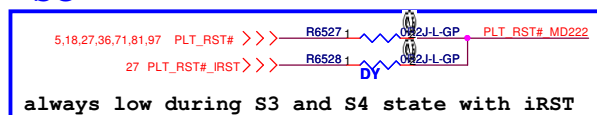
SB_20120113_IOAC



SB_20120117_IOAC

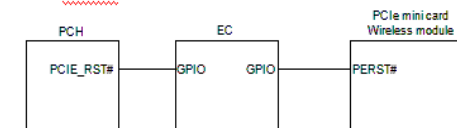


-SC



PCIe reset control method 2

- EC filters the PERST# signal.
- PERST# must be always low during S3 and S4 state with iRST.



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Title <div>WWAN Connector(mSATA)</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 66 of 103

Blanking

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Title		
M-SATA		
Size	Document Number	Rev
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Date: Thursday, August 23, 2012		Sheet 67 of 103

SSID = User.Interface

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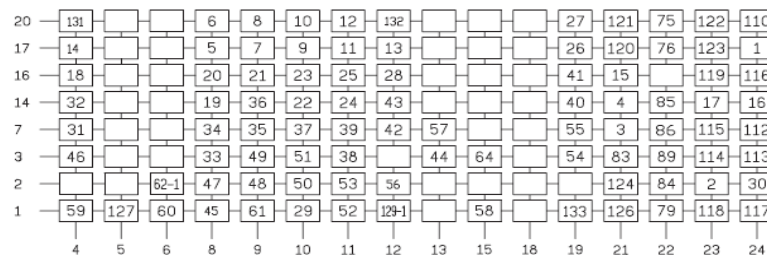
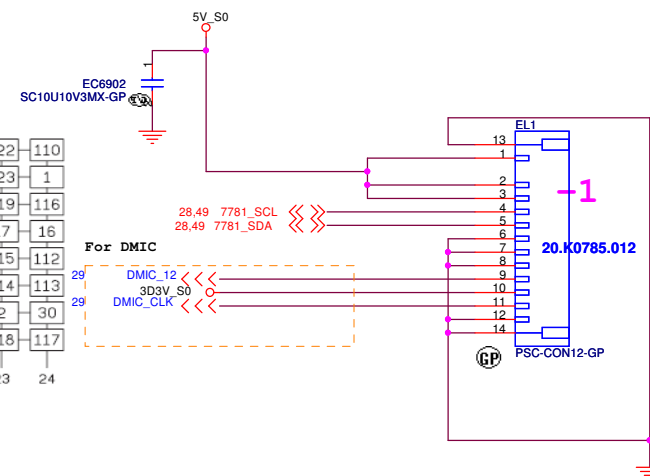
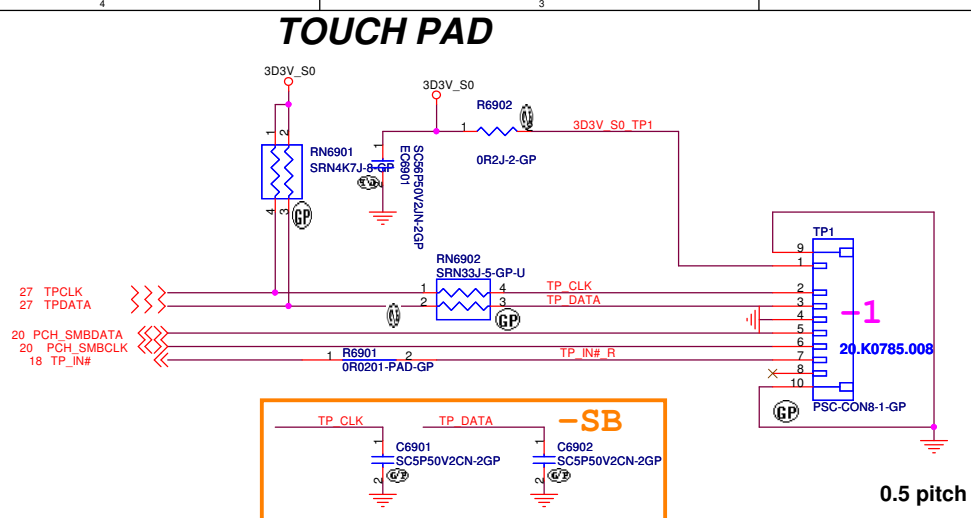
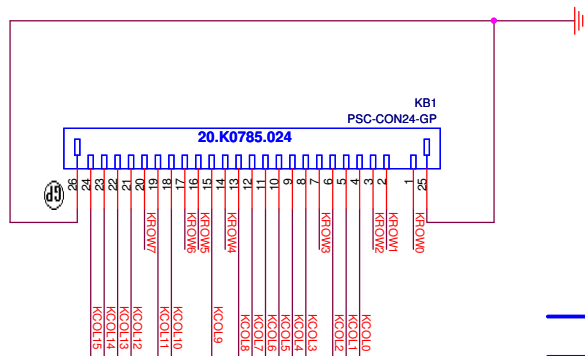
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Light SENSOR</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
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SSID = KBC

Pin number	Pin Define
1	VDD(3.3V)
2	PCClk
3	PCDt
4	DGND
5	NC*(SDA)
6	NC*(SCL)
7	NC*/INT)
8	NC

Note: Reserve for SMBus

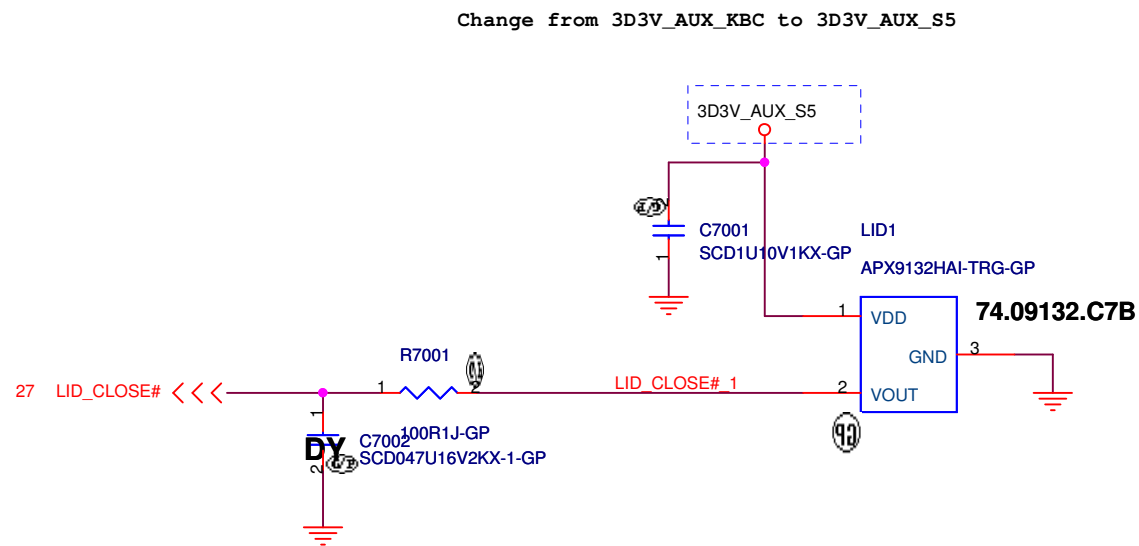
Internal KeyBoard Connector



————<<< KROW[0..7] 27

_____ >>> KCOL[0..15] 27

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Title

Hall Sensor

Size
A4

Document Number

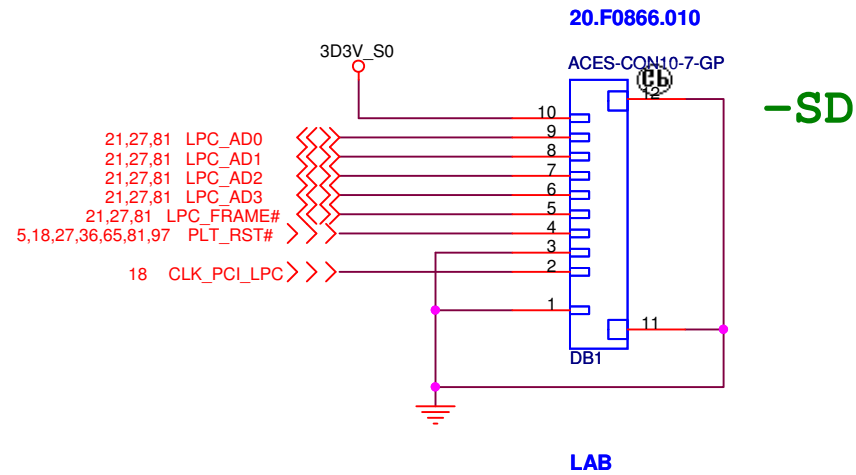
Helium

Rev
-1

Date: Thursday, August 23, 2012

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Title

Dubug connector

Size
A4

Document Number

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 72 of 103

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
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Micro SD Card Reader

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Title <div>Micro SD Card Reader</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 74 of 103

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

(Blanking)

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Title			
Reserved			
Size	Document Number		Rev
A4	Helium		-1
Date: Thursday, August 23, 2012		Sheet	76 of 103

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 77 of 103

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 78 of 103

SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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Title

G- Sensor

Size
A4

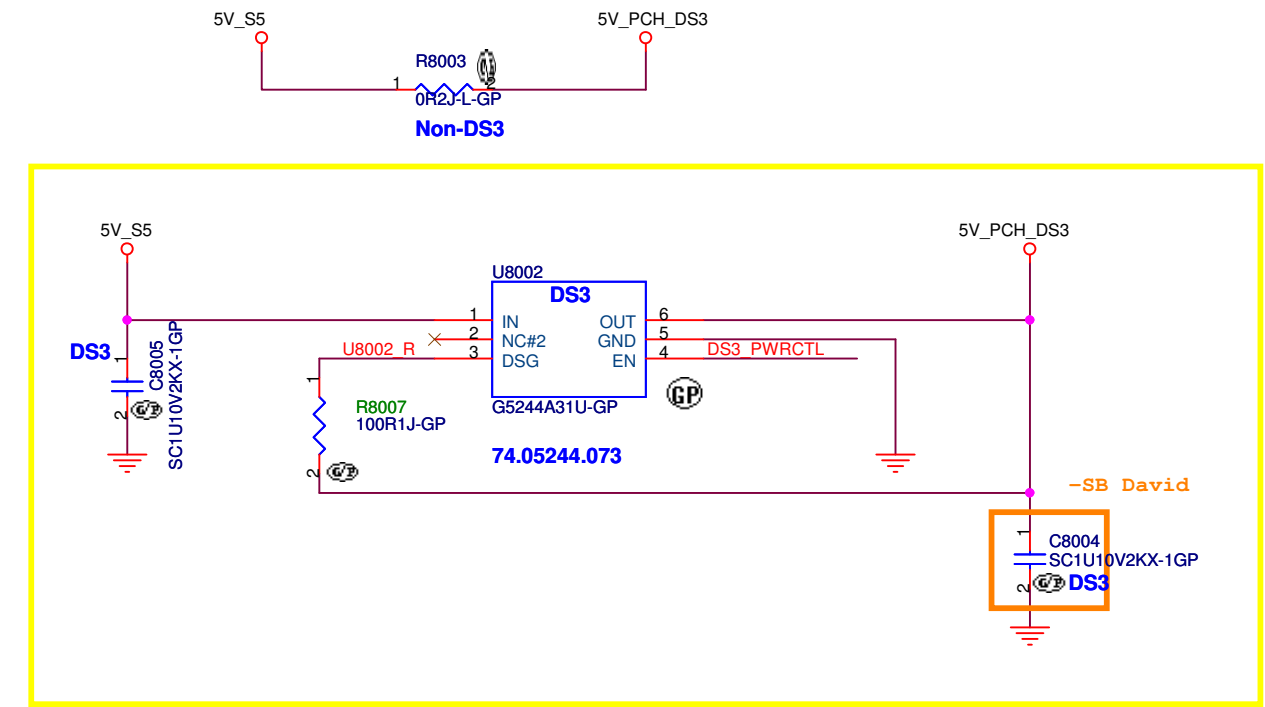
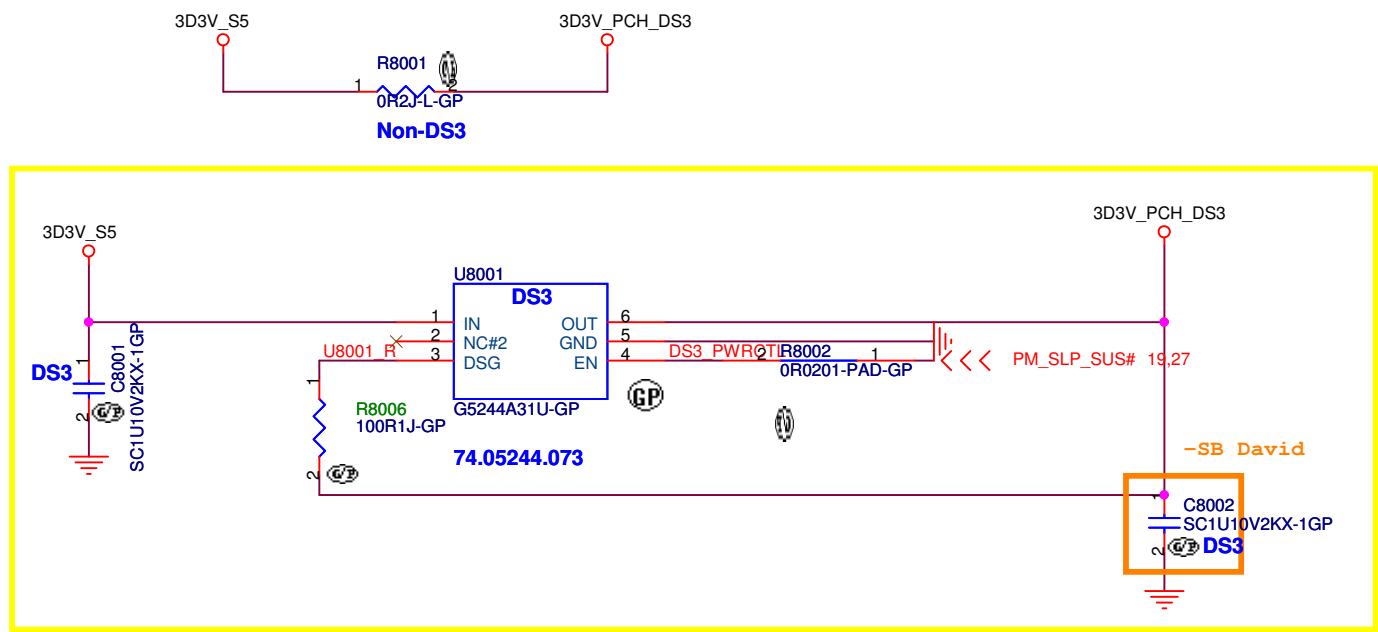
Document Number

Helium

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-1

Date: Thursday, August 23, 2012

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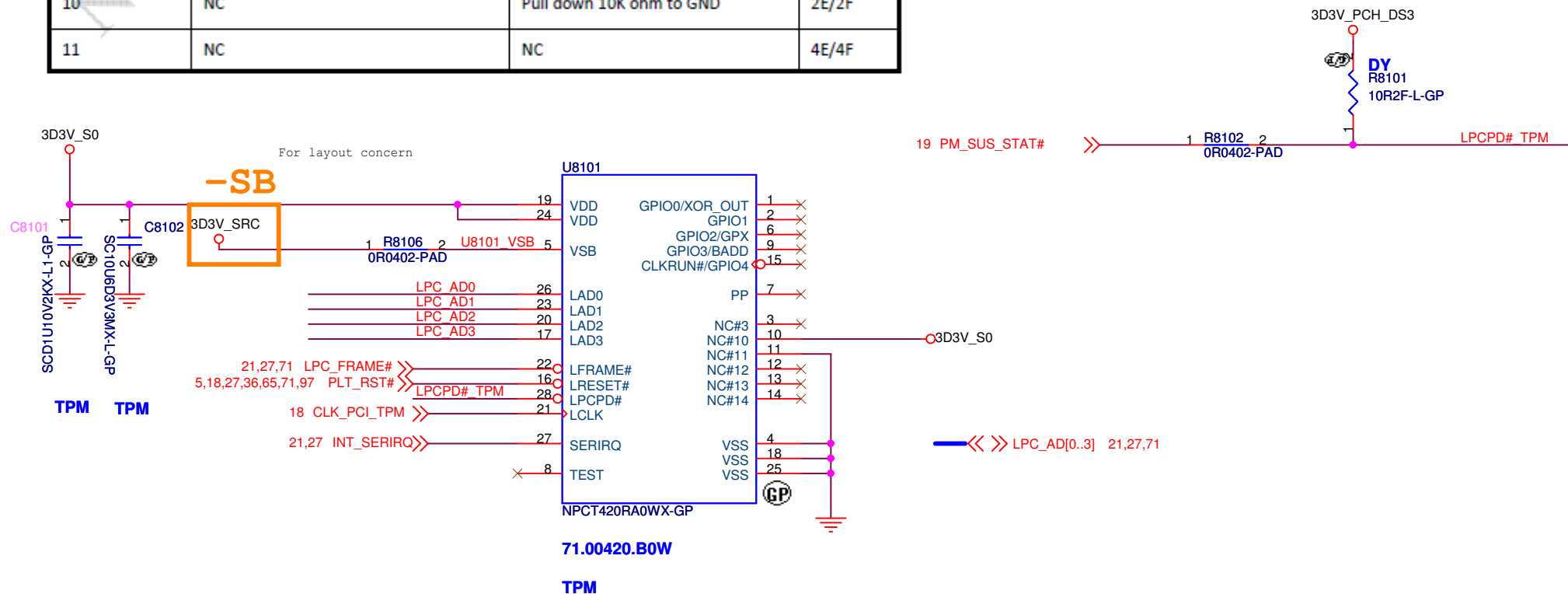


Helium

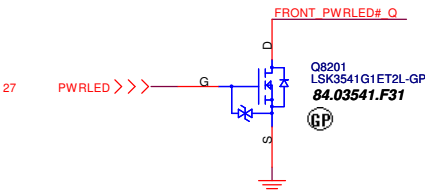
<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title</p> <p>Deep Standby</p>	
Size	Document Number
A4	Helium
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Table 3-1 TCM LPC Legacy IO port configuration

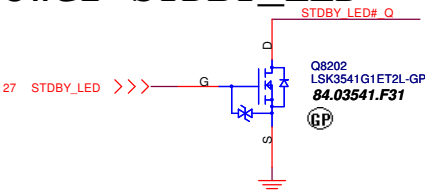
BADDR[1:0]	BA1	BA0	IO Port
00	Pull down 10K ohm to GND	Pull down 10K ohm to GND	EE/EF
01	Pull down 10K ohm to GND	NC	7E/7F
10	NC	Pull down 10K ohm to GND	2E/2F
11	NC	NC	4E/4F



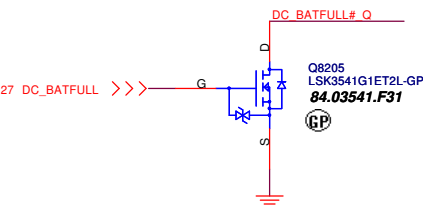
Power button LED



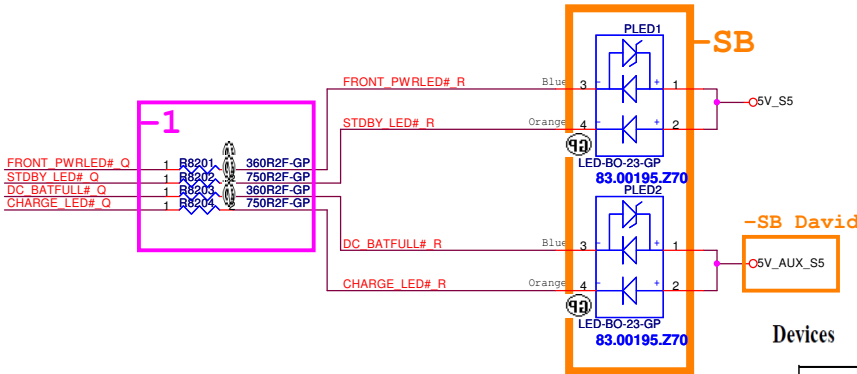
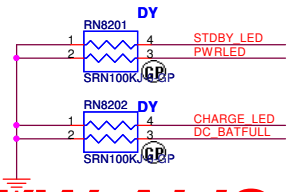
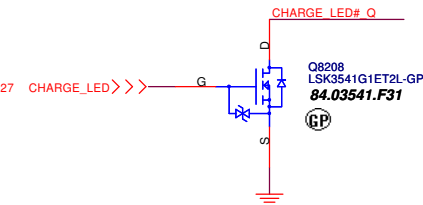
Power STDBY_LED



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)

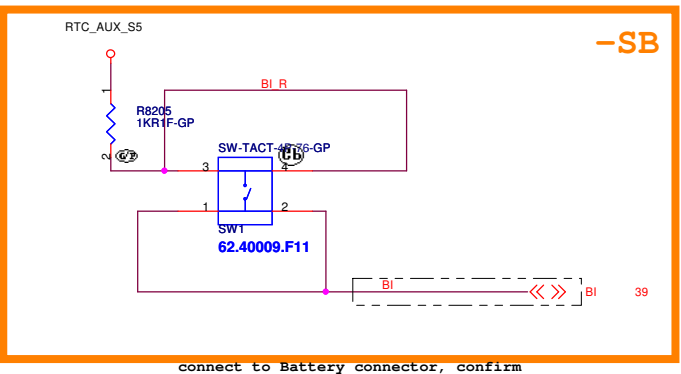
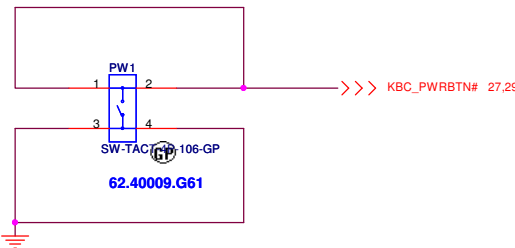


Forward Voltage

VF	MIN.	Blue	Orange	V	IF =20mA
		2.90	1.80		
		TYP. 3.30	2.00		
	MAX.	3.50	2.40		

Devices

Part No.	Lens	Source Color	Pin Assignment
LTST-C195ZBKFKT	Water Clear	InGaN Blue	1,3
		AlInGaP Orange	2,4



connect to Battery connector, confirm

Helium	
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Title	
GPU PCIE/STRAPPING(1/5)	
Size	Document Number
A2	Helium
Date: Thursday, August 23, 2012	Rev -1
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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

Helium		<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div>	
Title		GPU Memory(2/5)	
Size	Document Number	Rev	
Custom	Helium	-1	
Date:	Thursday, August 23, 2012	Sheet	84 of 103

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Helium	
<div>緯創資通Wistron Corporation 21F, Sec. 1, Hsin-Tai Wu Rd., Hsuehshui, Taipai Hsien 221, Taiwan, R.O.C.</div>	
Rev	
GPU_DP/LVDS/CRT/GPIO(3/5)	
Doc	Document Number
Custom	Helium
Date	Monday, August 25, 2014
Sheet	85 of 103
Rev	-1

Helium		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
GPU DPPWR/GND(5/5)		
Size	Document Number	Rev
A3	Helium	-1
Date:	Thursday, August 23, 2012	Sheet 87 of 103

Helium

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM1,2 (1/4)

Size
Custom

Document Number
Helium

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-1

Date: Thursday, August 23, 2012

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	5	4	3	2	1
D					
C					
B					
A					

Helium		<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title		GPU-VRAM3,4 (2/4)	
Size Custom	Document Number		Rev
	Helium		-1
Date:	Thursday, August 23, 2012	Sheet 89 of 103	

Helium

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5.6 (3/4)

Size
Custom

Document Number

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Title

GPU-VRAM7,8 (4/4)

Size

Document Number

Rev

Custom

Helium

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Date: Thursday, August 23, 2012

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Helium		緯創資通 Wistron Corporation <small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipai Hsien 221, Taiwan, R.O.C.</small>	
Title		RT8208B +VGA CORE	
Size	Document Number		Rev
Custom	Helium		-1
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Blanking

Helium		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
DISCRETE VGA POWER		
Size	Document Number	Rev
A4	Helium	-1
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5

4

3

2

1

D

D

C

C

B

B

A

A

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Title <div>LVDS Switch</div>		
Size <div>A4</div>	Document Number <div>Helium</div>	Rev <div>-1</div>
Date: Thursday, August 23, 2012		Sheet 94 of 103

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB CHG

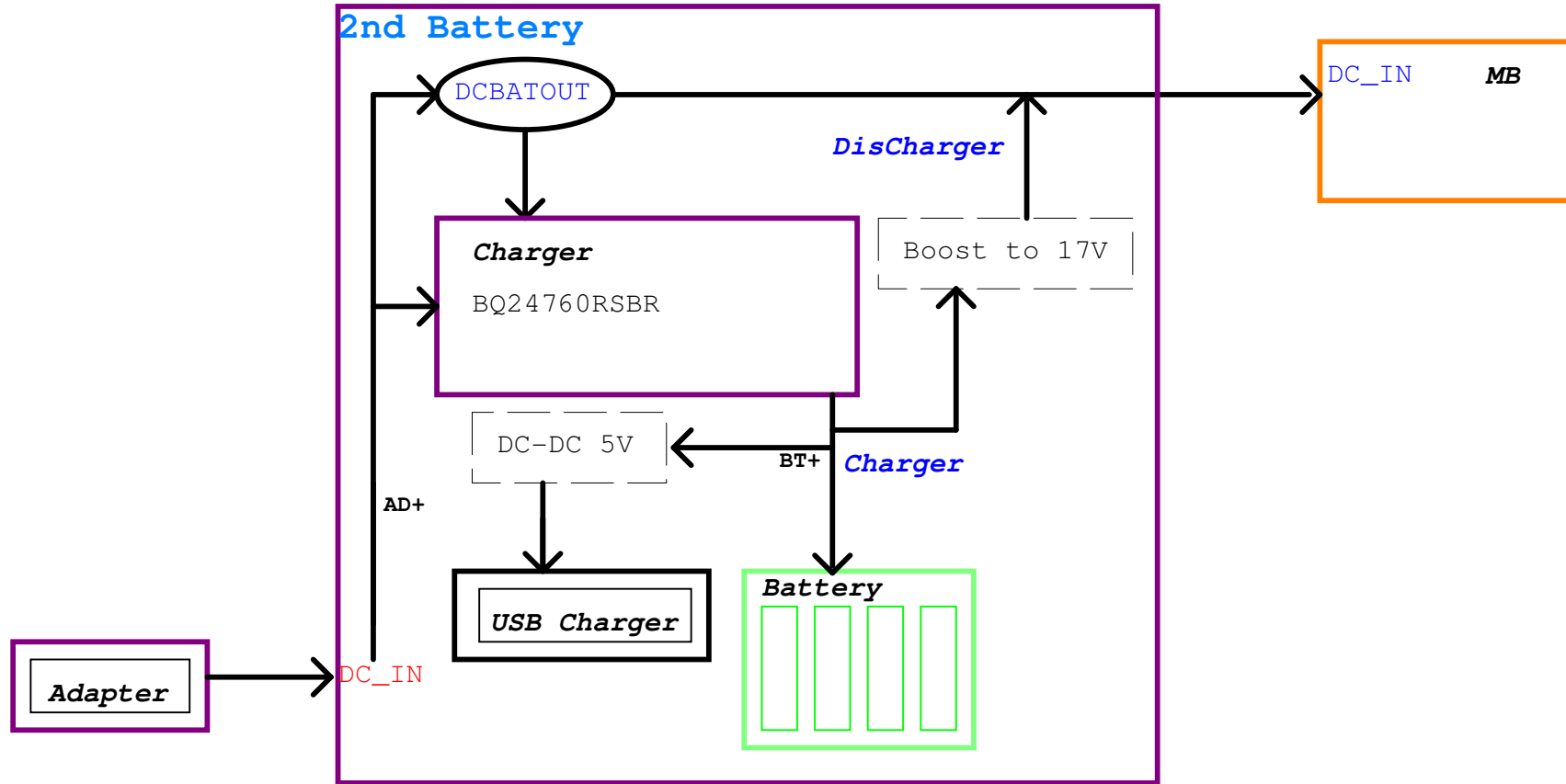
Size
A3

Document Number
Helium

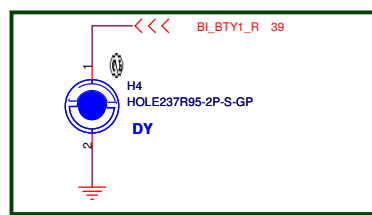
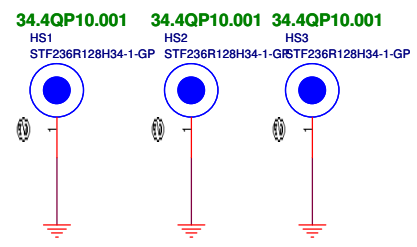
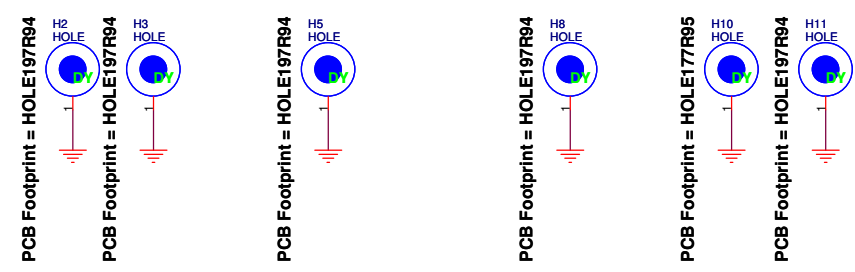
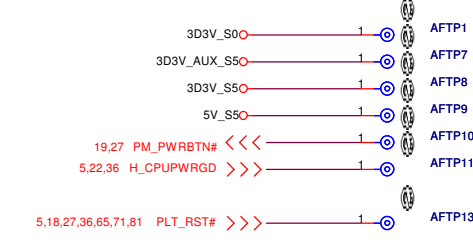
Rev
-1

Date: Thursday, August 23, 2012

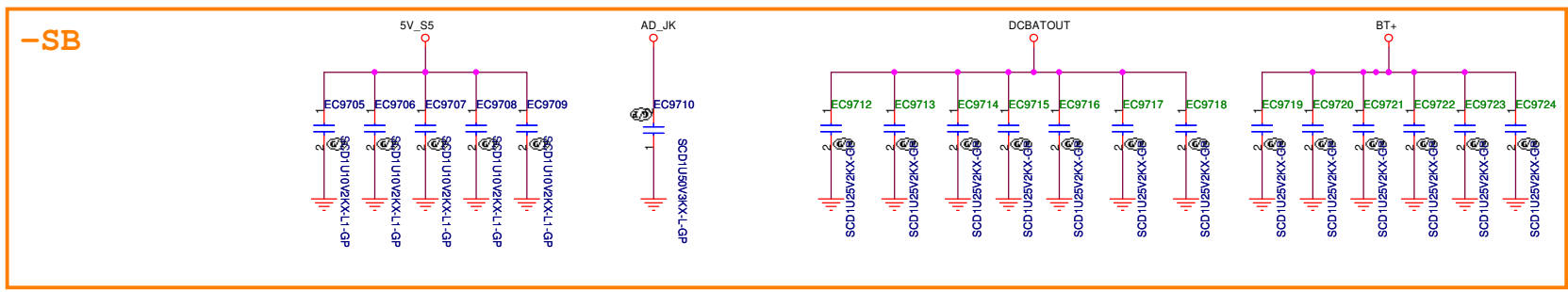
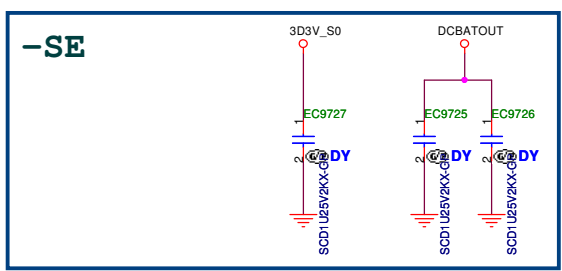
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Check test point

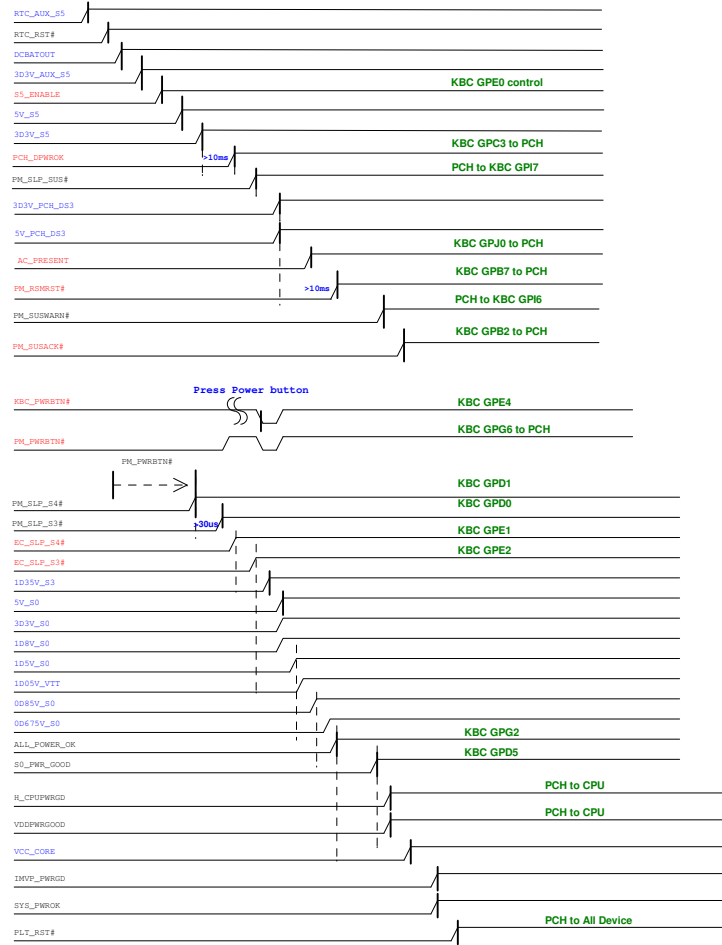


-SD

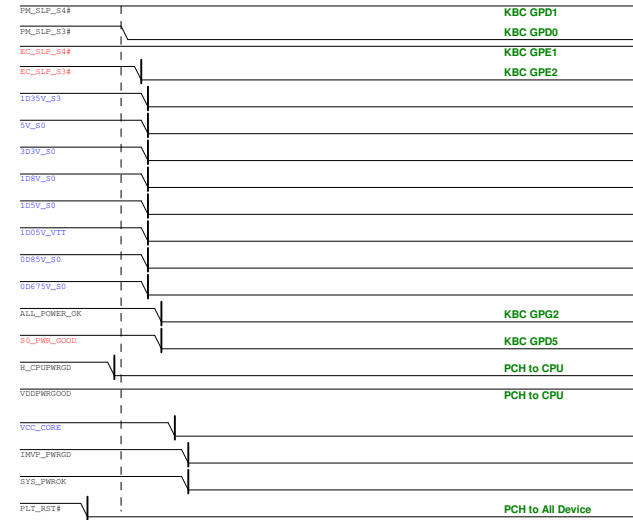


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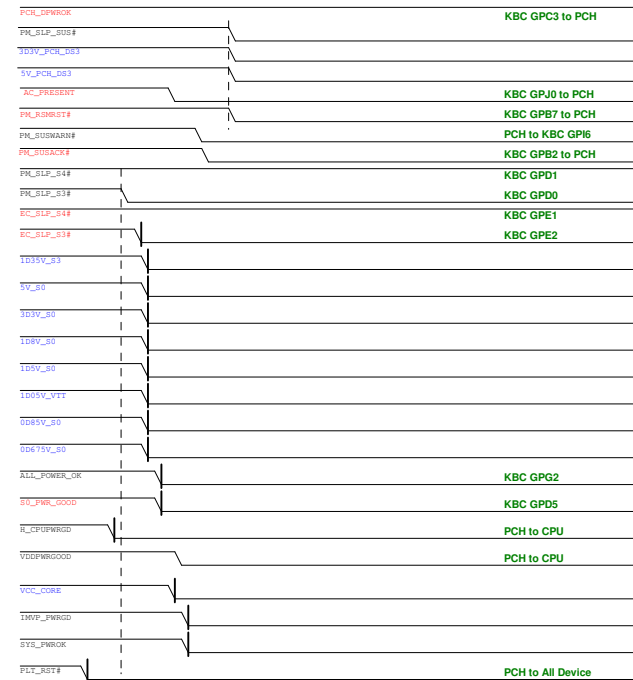
Intel Power Up Sequence



Intel S3 Sequence

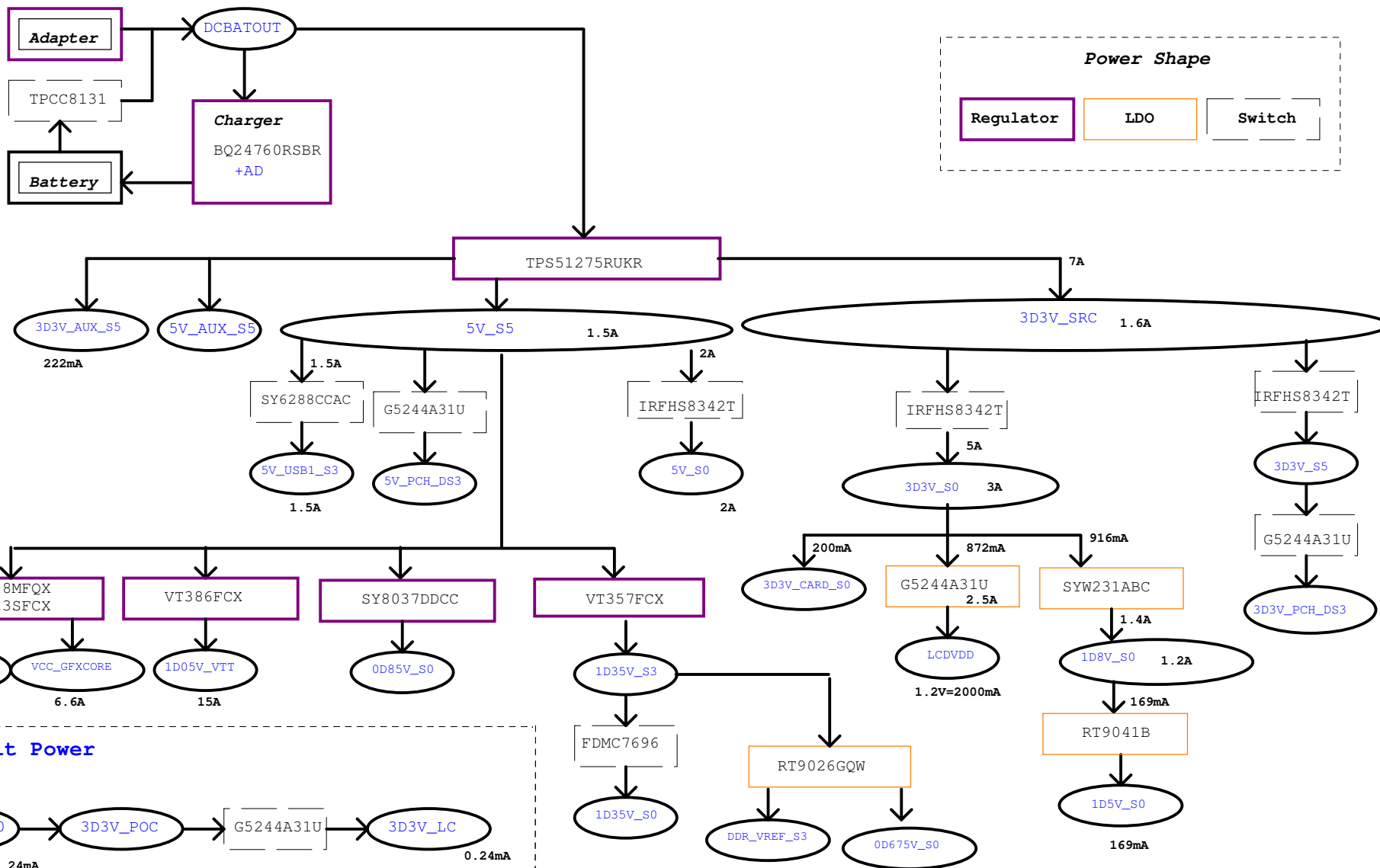


Intel Deep S3 Sequence



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5V_S5->1.5A
 5V_S0->(5V_S5 to 5V_S0)->2A
 CPU Core ->(Vin is 5_S5, power 約2.4A)->9.7A
 GFX Core ->(Vin is 5_S5, power 約1.7A)->6.6A
 1.05V_S0->(Vin is 5_S5, power 約3.8A)->15A
 0.85V_S0->(Vin is 5_S5, power 約0.8A)->4A
 1.35V_S3->(Vin is 5_S5, power 約3A)->8A(包含1D35V_S0)
 12V_MP->(Vin is 5_S5, power 約2.8A)->1A
 so 5V約18A,DCBATOUT DC mode電壓約為5V,

1D8V_S0->(Vin is 3.3V_S5, power 約1A)->1242mA
 3D3V_S5約6A,請設240mA

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Title

Power Block Diagram

Size

Document Number

Helium

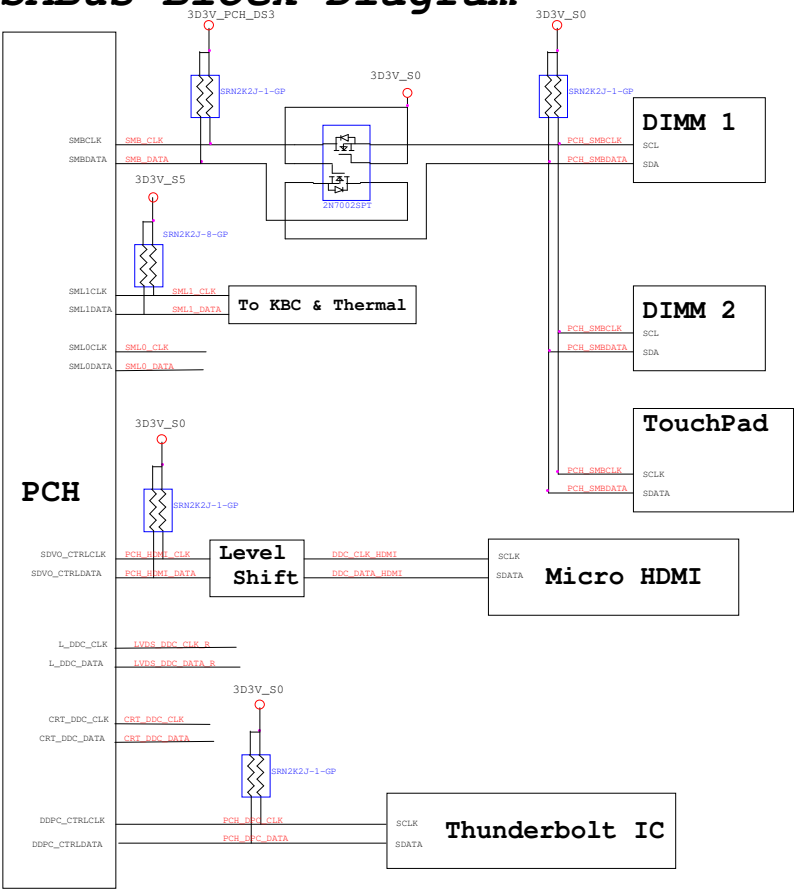
Rev

-1

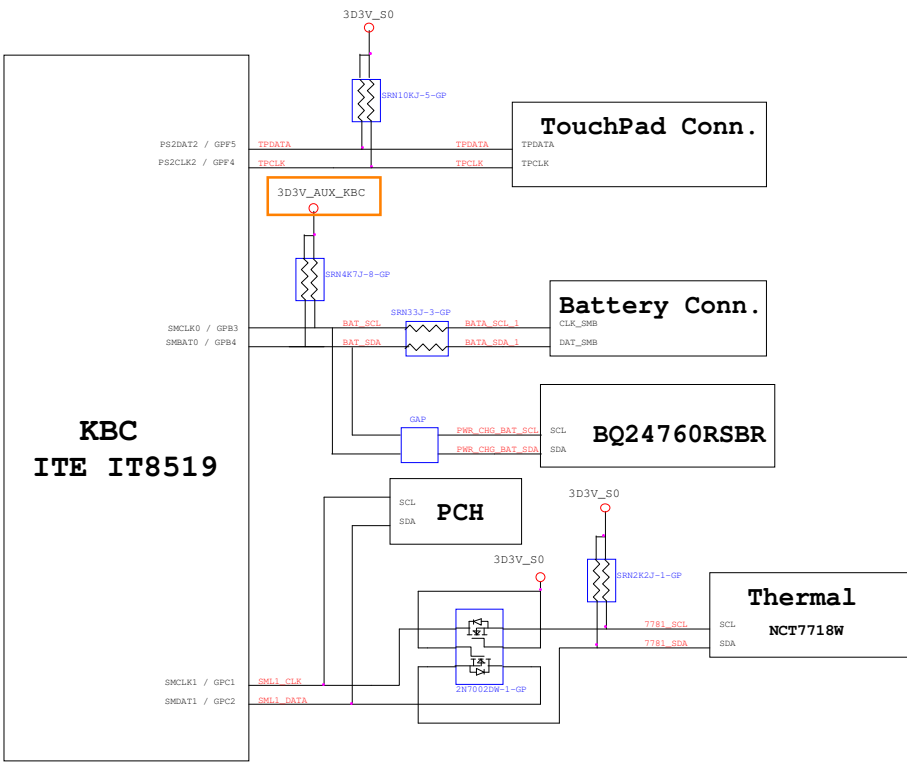
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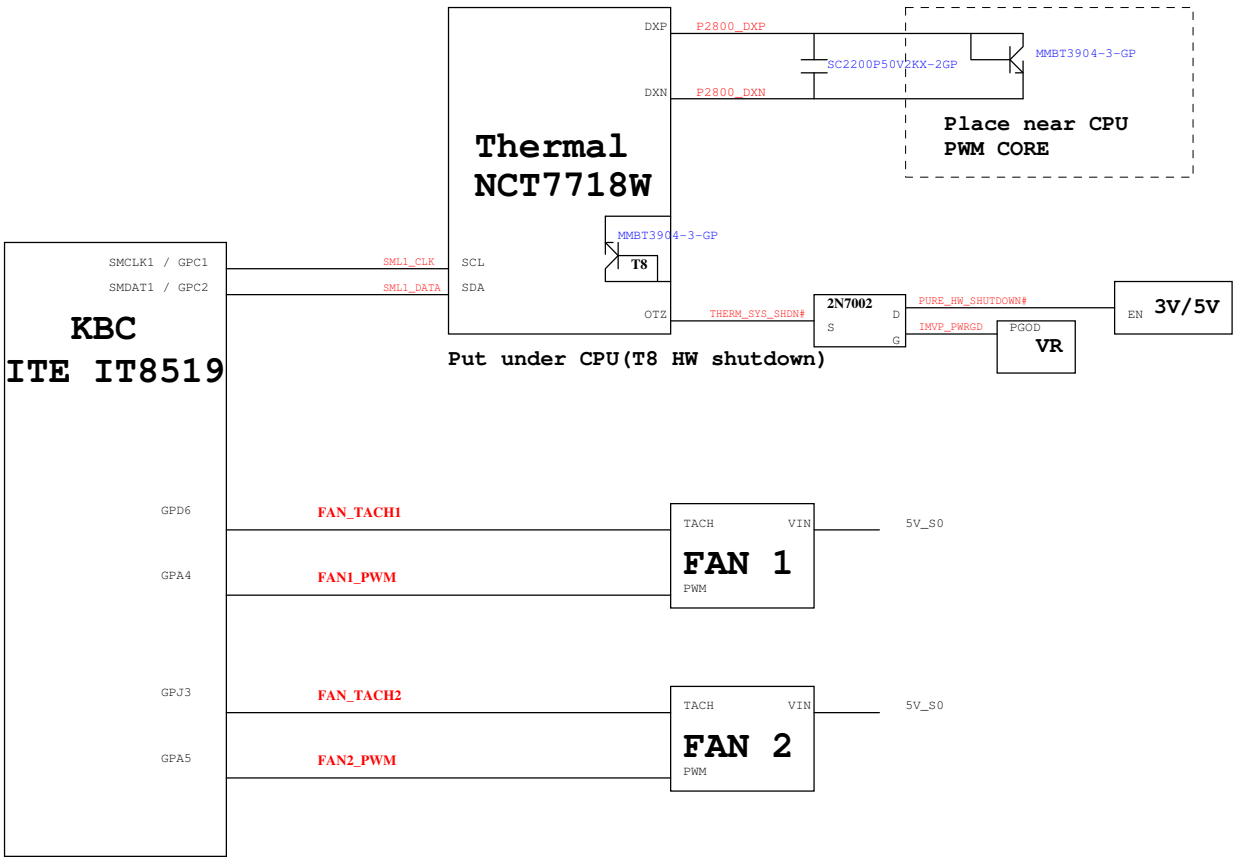
PCH SMBus Block Diagram



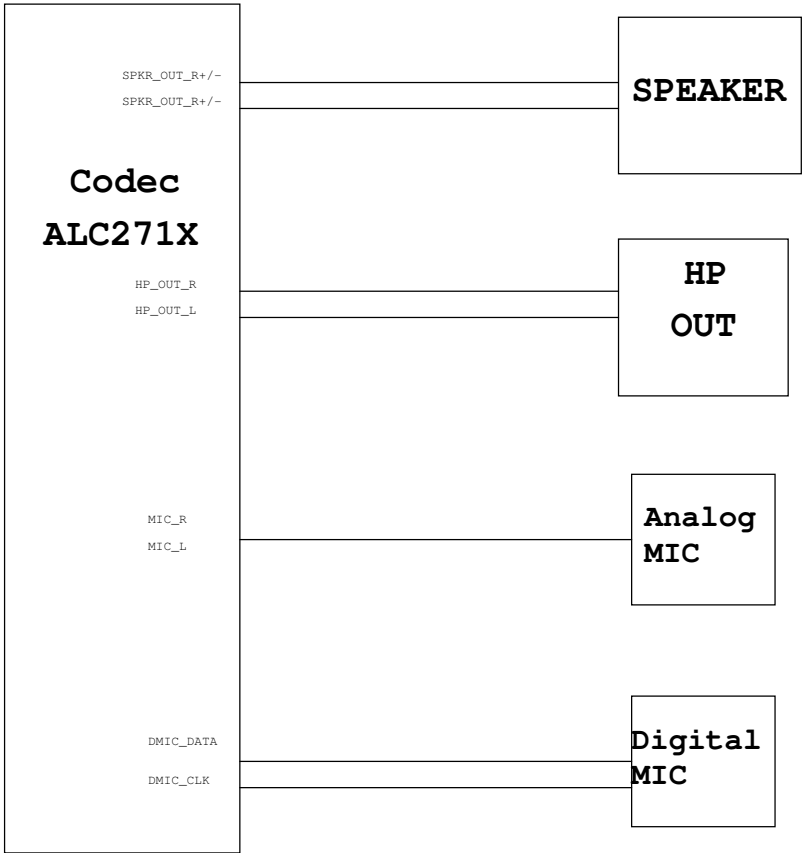
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



[Design-Kent]

- (1) change 1U6D3V2 78.10520.LAL to 78.10520.5FL(M)
(2) RAM1~8 change XX.XXXXX.XX
(3) BOM DEL RTC,CPU,PCH PN,PN for PM
(4) LAB1 BOM CHECK
(5) BOM U6003,4 Change to XX.XXXXX(Lab)
(6) BOM DCIN2 DEL(Lab)
(7) PL4502 to 68.R2210.10R
(8) BTY1 Only 4 pcs
(9) SW1 Del Lab1 不上件
(10)LID1 change to 74.05712.0BB (BOM)

[Lab2-Kent]

- (1) SKU 3 use 2nd source
(2) Change 7" to 13"
(3) 84.03541.F31 Change
ADD 2ND=84.33030.031 (BOM) (For ESD 2KV)
(4) PLED1 and PLED2 change from 『83.00195.G70』
to 『83.00195.Z70』 for CSD 1KVESD request

(5) RTC Cable PN place on DIP BOM -SB David

- (6) Del U6002 WSON package on SMT BOM
ADD U6003 TSOP package (72.25Q32.A01)on DIP BOM

[Lab3-Kent]

- (1) 84.03541.F31 Change 84.02N05.A3K (ROHM) (For ESD 2KV)
(2) Change 7" to 13"
(3) RTC Cable PN place on DIP BOM(2nd Source)
(4) Change CPU,PCH, RAM, Thunderbolt
(5) U2702 Change 74.00809.S7B
(6) 78.10323.20L Change 78.10323.5SL (COMMON)
(7) Check page 60 S0 or S5 by david
(8) KBC change 71.08518.B0U

[Lab4-Kent]

- (1) Change 7" to 13" (新版的)
(2) 84.03541.F31 Change 2ND=84.33030.031 (BOM) (For ESD 2KV)
2ND=84.02N05.A3K (ROHM)
(3) 78.10323.20L Change 78.10323.5SL (COMMON PN)
(4) Change CPU,PCH, RAM, Thunderbolt
(6) RTC cable 2nd source
(7) 83.R2003.V8F Lab3 缺料記得Lab4

	Main source	2nd source
PU4101	84.03664.037 (FDMS3664S) Mount	84.00038.A37 (RJK03P8DPA) Mount

(8) XTAL要上2nd Source

CPU Table

CPU	
Stage	P/N
ENG-A	71.00IVY.C3U(1.7G)
ENG-B	71.00IVY.E1U(1.8G)
ENG-C	71.00IVY.H0U(1.9G)
	N/A
	N/A
	N/A

Thunderbolt Table

Thunderbolt	
Stage	P/N
ENG-A	N/A
ENG-B	N/A
ENG-C	N/A
	N/A
	N/A
	N/A

ROM Table

U6003/2 ROM 4M	
Stage	P/N
LAB1	62.10076.011
LAB2-DIP	72.25Q32.A01
LAB2-SMT	62.10076.011
LAB3	As Lab2
LAB4	As Lab2

PCH Table

PCH	
Stage	P/N
ENG-A	71.0HM77.00U
ENG-B	71.0HM77.00U
ENG-C	71.0HM77.A0U
	71.0HM77.A0U
	71.0HM77.M01
	N/A

RAM Table

RAM		
Stage	P/N	Stage
ENG-A	72.04216.00U	ELPIDA 4G
ENG-B	72.05463.00U	Hynix 4G
ENG-C	72.04216.00U	Hynix 2G

[ENG-Kent]

- (1) Change 7" to 13" (新版的)
(2) 84.03541.F31 Change 1st=84.33307.031 (松下)
2ND=84.02N05.B3K (ROHM)
(3) 78.10323.20L Change 78.10323.5SL (COMMON PN)
(4) Change CPU,PCH, RAM, U6502

	Main source	2nd source
PU4101	84.03664.037 (FDMS3664S) Mount	84.00038.A37 (RJK03P8DPA) Mount

- (8) U3701 3rd source (73.7SH09.0AG)
(9) U7501 Change NC.25411.002 (ENG1才有)



-SA



-SB



-SC



-SD



-SE



-1



-2

[Source]

BOM	
ENG A Sku	1st Source
ENG B Sku	2nd Source
ENG C Sku	1st Source

[PD-Kent]

- (1) Change 7" to 13" (新版的)
(2) 84.03541.F31 Change 1st=84.33307.031 (松下)
2ND=84.2N022.031 (ROHM)
(4) Change CPU,PCH, RAM, U6502, R2735

	Main source	2nd source
PU4101	84.03664.037 (FDMS3664S) Mount	84.00038.A37 (RJK03P8DPA) Mount

(5) U3701 3rd source (73.7SH09.0AG)